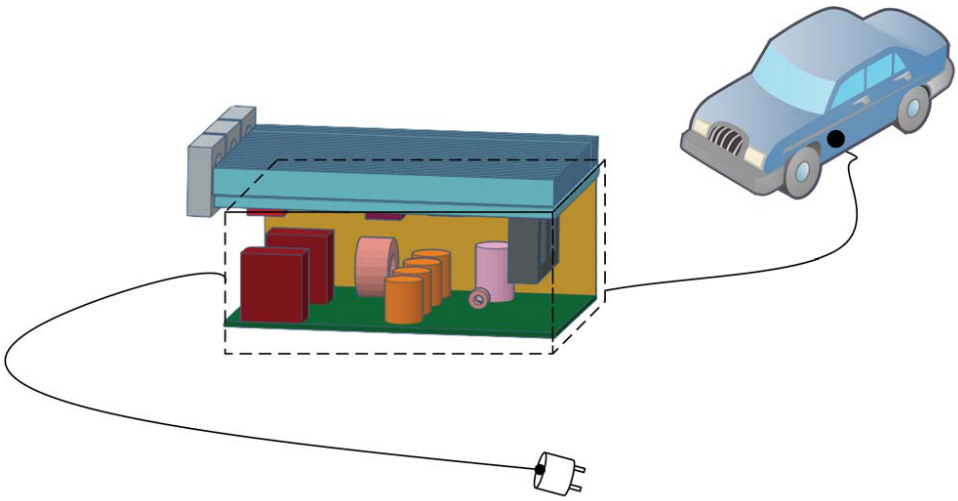
CHALMERS
UNIVERSITY OF TECHNOLOGY



Power Control of a External Charging System for Electric Vehicle

Master's thesis in Electric Power Engineering

VASANTH RAMESH
VISHAG BASKER

Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2019

Master's thesis 2019

Power Control of an External Charging System for Electric Vehicle

VASANTH RAMESH
VISHAG BASKER

CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
Gothenburg, Sweden 2019

Power Control of an External Charging System for Electric Vehicle
VASANTH RAMESH
VISHAG BASKER

Supervisor: Name, Company or Department
Examiner: Name, Department

Master's Thesis 2019
Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Printed by Chalmers Reproservice
Gothenburg, Sweden 2019

Power Control of an External Charging System for Electric Vehicle
VASANTH RAMESH
VISHAG BASKER
Department of Electric Power Engineering
Chalmers University of Technology

Abstract

Today, electrified vehicles are usually equipped with an onboard charger. Although it has the power to charge the high voltage battery, it's size and weight is a matter of concern for the electric vehicle. Hence an external charging system is suggested in this thesis, which can replace the onboard charger.

In this master thesis, an external charging system used in the electric vehicle is investigated. The power control is done using a totem pole bridgeless Power Factor Correction (PFC) topology. Initially, the totem pole PFC is compared with the conventional PFC based on the losses, components, and efficiency theoretically and its selection based on the operation is motivated. The totem pole PFC is analyzed in open-loop control where the switching characteristics are studied based on two switch types - Silicon Carbide (SiC) and Gallium Nitride (GaN). The power control of the totem pole PFC is done in closed-loop control where both voltage and current are controlled in the totem pole PFC circuit. To avoid overheating due to high current, a temperature analysis is also done in the totem pole PFC circuit using the lumped thermal model network where the temperature analysis of both the switches is studied.

The weight and volume estimation of the main components used in the totem pole PFC circuit is also illustrated. A Life-Cycle Cost Analysis (LCCA) is done where a cost comparison of two switches (GaN and SiC) is done. Finally, the efficiency of the complete totem-pole PFC circuit is analyzed for various power levels by varying the load and the overall efficiency of the converter at full load is found out to be 98.72 %.

Keywords: SiC - Silicon Carbide, GaN - Gallium Nitride, PFC - Power Factor Correction, Totem-pole, Lumped thermal, LCCA - Life cycle cost analysis

Acknowledgements

We are grateful to Annevo AB for providing us the infrastructure and support to complete this master thesis project.

Foremost we would like to thank Björn Isaksson, Avishek Mohanty and Martin Gow for having the trust and providing us the opportunity to be a part of this amazing thesis project. It was a pleasurable experience working with you people. Thank you for motivating us and help us maintain the energy throughout the thesis project.

We would also like to thank Odyssefs Lykartsis whose technical guidance helped us to move forward in this project. Special gratitude and thanks to our supervisor and examiner, Torbjörn Thiringer for guiding us in report writing. We also would like to extend our gratefulness to our manager, Alfred Andersson for his enormous support and mentoring in our presentation.

Lastly, we would like to thank our family and friends for all support and encouragement throughout the project and also our study in Chalmers.

Vasanth Ramesh and Vishag Basker, Gothenburg, July 2019

List of abbreviations

AC	Alternating Current
BEV	Battery Electric vehicles
BJT	Bipolar Junction Transistor
CCM	Continuous Conduction Mode
CrCM	Critical Conduction Mode
DCM	Discontinuous Conduction Mode
DC	Direct Current
DSP	Digital Signal Processing
ESR	Equivalent Series Resistance
FEA	Finite Element Analysis
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IGBT	Insulated Gate Bipolar Transistor
LCCA	Life Cycle Cost Analysis
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NTC	Negative Temperature Coefficient
OEM	Original Equipment Manufacturing
PF	Power Factor
PI	Proportional Integral
PWM	Pulse Width Modulation
RCD	Residual Current Device
RMS	Root Mean Square
SiC	Silicon Carbide
SMPS	Switch Mode Power Supply
THD	Total Harmonic Distortion

Contents

1 Introduction **1**
1.1 Background . . . 1
1.2 Purpose of work . . . 1
1.3 Scope . . . 1

2 Theory **3**
2.1 Electric Vehicle Chargers . . . 3
2.1.1 Portable off-board charger . . . 3
2.2 Power factor correction . . . 3
2.3 PFC Circuit Topology . . . 4
2.3.1 Conventional PFC Topology . . . 4
2.3.2 Totempole bridgeless topology . . . 4
2.3.3 Totem Pole PFC operation . . . 5
2.4 Semiconductors Description . . . 6
2.4.1 SiC material . . . 7
2.4.2 GaN material . . . 7
2.5 Control system of PFC circuit . . . 8
2.5.1 Calculation of parameters for totem pole PFC circuit . . . 8
2.5.1.1 Calculation of Inductance . . . 8
2.5.1.2 Calculation of Capacitance . . . 9
2.5.2 Closed control loop system . . . 9
2.5.2.1 Current Control Implementation . . . 10
2.5.2.2 PI Controller parameters for current controller . . . 11
2.5.2.3 Calculating the ripple of the control signal in Current Controller . . . 12
2.5.2.4 Voltage control Implementation . . . 13
2.5.2.5 PI Controller parameters for voltage controller . . . 15
2.6 Power losses in the charging system . . . 16
2.6.1 Boost inductor losses . . . 17
2.6.2 DC-link capacitor losses . . . 17
2.6.3 Gate losses . . . 17
2.6.4 Power Mosfet Losses . . . 18
2.7 Thermal derating of power electronic components . . . 19
2.7.1 Heat transfer modes . . . 19
2.7.2 Lumped thermal modelling . . . 20
2.8 Power losses for thermal analysis . . . 20

2.9 Cost Analysis 21

3 Case Set-up **23**
3.1 Design of PFC circuit 23
3.1.1 Designing Inductance 24
3.1.2 Designing Capacitance 24
3.1.3 Choosing the suitable transistors 24
3.1.4 Modelling of SiC and GaN switches 24
3.1.5 Implementation of gate driver circuit 25
3.1.5.1 Mosfet switching leg 26
3.1.5.2 GaN switching leg 27
3.2 Set up of a control loop system 28
3.2.1 Implementation of feedback loop 28
3.2.2 Implementation of PI controller 29
3.3 Power Losses Calculations 30
3.3.1 Boost inductor 30
3.4 Implementation of lumped thermal model 30

4 Results & discussion **33**
4.1 Open loop characteristics 33
4.2 SiC switching characteristics 33
4.3 GaN switching characteristics 34
4.4 Comparison of SiC and GaN 34
4.5 PWM control in a closed loop 35
4.6 Current control loop 36
4.7 Voltage Control loop 37
4.7.1 With Constant Reference 37
4.7.2 With an additional step 38
4.8 Complete Closed loop Simulation Results 40
4.9 Temperature analysis of SiC and GaN switches 42
4.10 Power Factor Correction of the circuit 43
4.11 Volume and Weight Estimation 43
4.12 Life Cycle Cost Anlaysis 45
4.13 Efficiency 46

5 Safety and Sustainability **49**
5.1 Safety 49
5.2 Sustainability 50

6 Conclusion **51**
6.1 Future Works 51

Bibliography **53**

A Appendix 1 **I**
A.1 Matlab Scripts I
A.1.1 Current Controller I

A.1.2 Voltage Controller II
A.1.3 Current Controller with filter II
A.1.4 Voltage Controller with filter III
A.1.5 Life Cycle Cost Analysis for GaN and SiC III
A.2 System Level Simulations V

1
Introduction

1.1 Background

Electric vehicles are developing at a rapid pace in the automotive industry. They can reduce the reliance on fossil fuels and eventually reducing the impact of emissions caused by transportation. An Electric Vehicle (EV) is powered by an electric motor by extracting power from a rechargeable energy storage device. They receive electricity by charging from the grid and storing the energy in batteries. An EV charger is an electrical device in which the alternating current is converted into direct current and the converted energy can be stored in batteries. The EV chargers can be divided into two types: on-board charger and off-board charger [1].

In this project, a portable off-board mobile charger will be designed. This will enable the consumer to charge the vehicle wherever a power supply is available and also there will be no extra installation cost which is an advantage. An external portable (off-board) charger is suggested here to enable fast charging capability since it eliminates the power limitation due to the presence of an on-board charger. Since a charging system is an important aspect in an EV, the control of power in the external charger is essential. This encourages to design of a power control module in the external charger and simulate the losses in the system which will be monitored by a temperature sensor.

1.2 Purpose of work

The purpose of the work is to design, simulate and optimize the efficiency of the SMPS circuit. A current and voltage control loop is designed to maintain the power flow. Furthermore, the thermal behavior of silicon carbide and gallium nitride are analyzed and a comparison is made to make a better selection of the MOSFET switches and also to implement an efficient temperature control. Finally, a cost and volume estimation, as well as a comparison of the converter circuits, are made to motivate the selection of the topology and switches.

1.3 Scope

As the main aim of this project is to design a power control for an off-board charger, certain considerations will be taken into account to make the scope of this project feasible.

- The components used in the simulation circuit will be defined manually from the datasheets available to develop a more realistic model.
- All the losses in the system such as the conduction losses, switching losses, core losses in the inductors and losses due to heat will be estimated to obtain the efficiency of the circuit.
- Although the main aim is to build a charging system for EV batteries, the main focus will be to construct a charger. This project will not focus on building a practical battery model.
- A current and voltage control loop is designed based on the feedback from the battery using a PI controller.
- The thermal behavior of the MOSFET switches will be analyzed by implementing a lumped parameter thermal model.
- The volume is estimated by considering the weights of the components from the datasheet. There can be some differences during practical implementation.
- The cost of the converter is also estimated according to the current market prices. Hence there could be some deviation in the future.
- Even though it will be a working simulation model, immediate practical implementation of the same can be difficult since the soft start of the switch and other protection devices are not implemented which are important to meet the IEC standards.

2

Theory

2.1 Electric Vehicle Chargers

During recent years, electric vehicles have seen an increase in demand. They offer good potential to reduce local air pollution, greenhouse gas emissions and resulting climate change impacts, and the use of oil from the transport sector. When it comes to electric vehicles, charging a battery plays an important role. The on-board charger is predominantly used nowadays in electrical vehicles. But here, a portable off-board charger is implemented and the necessary background about its implementation will be explained in the following sections.

2.1.1 Portable off-board charger

A portable off-board charger is analogous to an on-board charger which is often used in electric vehicles nowadays. A charger aids in the AC-DC conversion and helps in the charging of batteries. The major advantage of having an off-board charger is that the weight of the vehicle is reduced by 4 kg depending on the size of the charger and vehicle. There is also extra space provided inside the vehicle due to the removal of the on-board charger which allows room for new components inside the vehicle or helps inefficient packaging of the components. Another major advantage of the off-board charger is that the battery charging is not limited due to the ratings of the on-board charger.

2.2 Power factor correction

The power factor correction circuit is widely implemented in AC to DC conversions. Mostly the PFC stage is used as the first stage in the converter where the major factors such as displacement and distortion factors could be improved so that the minimum apparent power can be obtained from the supply. The major function of the PFC stage is to make the input current drawn from the system sinusoidal and in phase with the supply voltage. This enables the charger to draw minimum apparent power from the supply, thus resulting in improvement of power quality and overall efficiency of the system [6]. Hence here we use the PFC method to have improved efficiency and the topology which is used to implement the PFC circuit will be discussed subsequently.

2.3 PFC Circuit Topology

Implementing a PFC circuit improves the efficiency of the system, and thus PFC circuit topology with minimum power losses is designed.

2.3.1 Conventional PFC Topology

The most commonly used PFC topology is the conventional boost PFC topology. The boost PFC topology uses a standard diode rectifier along with a boost converter topology. This topology is most sought due to the simple construction and the boost topology allows low distorted input current, thus helping in achieving a power factor close to unity. See figure 2.1 for it's circuit representation. But the major disadvantage is that during any instant of time three semiconductor switches are conducting which contribute to losses, thus reducing the efficiency of the system [12]. Also, to achieve higher power and transient response, the switches need to operate at higher frequencies which leads to higher reverse recovery losses. One of the major components which are contributing to the power loss in the switching power supplies is the front end bridge converter. Also, the bridge converter is termed to consume 2 to 3 % of the output power at low line voltages and full load [7]. Hence a totem pole bridgeless topology will be implemented here, neglecting the rectifier bridge and additionally reducing the conduction loss as well.

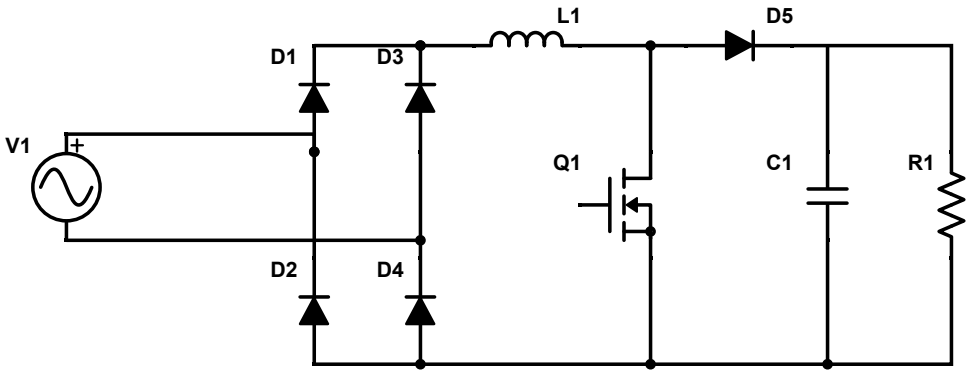


Figure 2.1: Conventional bridgless PFC Topology

2.3.2 Totempole bridgeless topology

The totem pole bridgeless PFC circuit will focus mainly on minimizing power loss in the conduction path. It can be operated in three modes such as Continuous Conduction Mode (CCM), Critical Conduction mode (CrCM) and Discontinuous Conduction Mode (DCM). The boost converter is rarely operated in DCM as it produces immense harmonics due to discontinuous current and hence it is not considered in this case. While CCM and CrCM are the most commonly used modes for the PFC circuits. CCM has merit of lower current ripple applying less stress on the semiconductors and inductors. CrCM on the other side enables Zero Current

Switching and Zero Voltage Switching due to that the current reaches zero every switching cycle, reducing the switching losses. But the major drawback of this mode is that it generates a large ripple current which is twice the average current and further increases the stress of the components. Thus for high power applications, it is common to operate in CCM, so that the components are not stressed severely [8]. Hence a CCM topology is implemented here for the PFC circuit.

2.3.3 Totem Pole PFC operation

The totem pole PFC operates in both the positive and negative half cycles of the input AC voltage. The totem pole bridgeless PFC consists of four switches. The switches in the first leg operate at a high switching frequency and the switches in the second leg operate at a low frequency, usually operating at the same frequency as the input AC voltage. Hence the two high-frequency switches along with the boost inductor act as a synchronous boost converter and the other two low-frequency switches help in rectifying AC to DC. The operation of the totem pole bridgeless PFC in both the negative and positive half cycle is shown in the figure below.

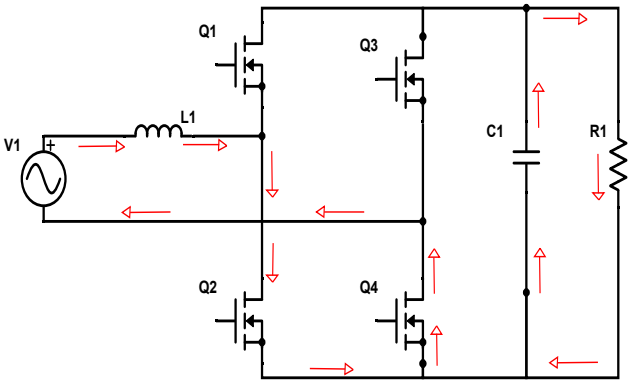


Figure 2.2: PFC circuit positive half cycle capacitor discharging

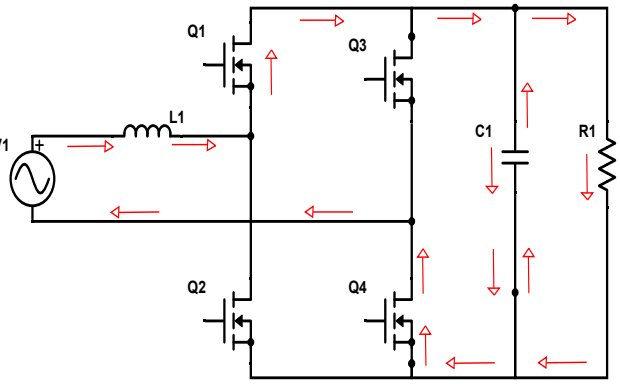


Figure 2.3: PFC circuit positive half cycle capacitor charging

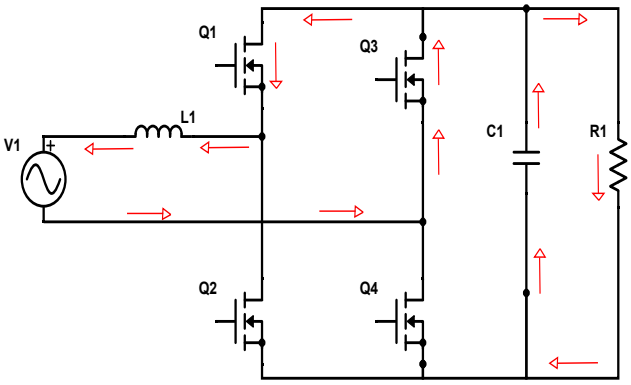


Figure 2.4: PFC circuit negative half cycle capacitor discharging

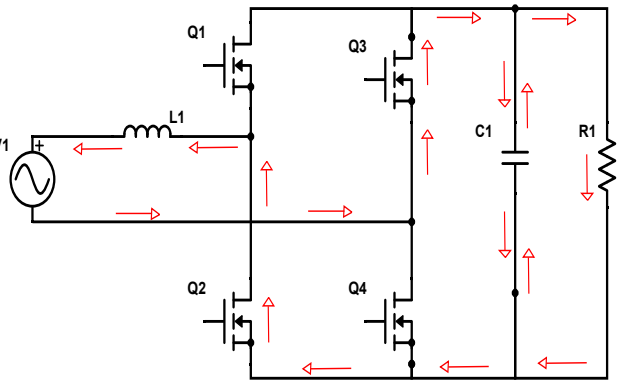


Figure 2.5: PFC circuit negative half cycle capacitor charging

As shown in figures above, the two low-frequency switches are on throughout the entire half-cycle and the high-frequency switches act alternately thus forcing the current in different ways to boost and rectify the voltage.

2.4 Semiconductors Description

The totem pole bridgeless PFC circuit will be implemented with the help of four switches, where two switches will be used for the boost converters which will operate at high frequencies. Initially silicon-based MOSFETs were used for these applications but later on, wide bandgap components emerged. These devices operate well at high frequencies, high temperatures, and high voltages compared to silicon-based MOSFETs.

The two most prominent wide bandgap devices that can be used for both switching and high-frequency applications are the Gallium Nitride (GaN) and Silicon Carbide (SiC) MOSFETs [31]. The other two switches used are low resistance silicon-based MOSFET's which can eliminate the diode voltage drop, thus improving efficiency. The conduction in the semiconductor devices takes place by pushing electrons present in the top of the valence band to the bottom of the conduction band and the energy is released. Materials that require energies more than one or two electron volts(EVs) are classified as wide bandgap devices. The table below shows the bandgap energy comparison for different semiconductors

Table 2.1: Band gap energy comparison

Material	Band Gap Energy (eV)
Germanium	0.2
Silicon	1.1
Gallium arsenide	1.4
Silicon Carbide	3.3
Gallium Nitride	3.4

Figure 2.6 shows the power split up for different power devices based on different operating frequencies. It can be seen from figure 2.6 that the Silicon carbide (SiC) and Gallium Nitride (GaN) devices can operate at both high power and frequencies, hence a focused study in these two devices are done.

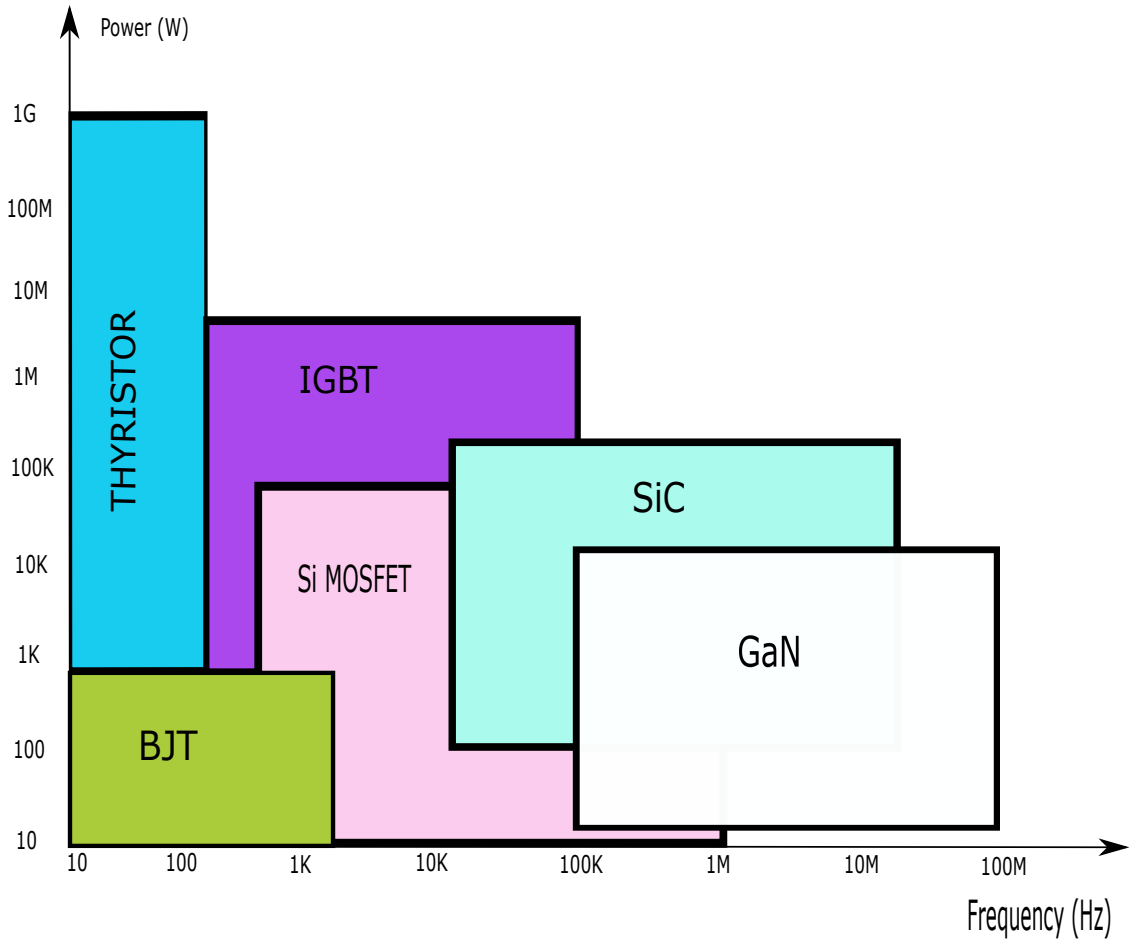


Figure 2.6: Power devices split up based on power rating and operating frequencies by IHS marketing firm [32]

2.4.1 SiC material

As shown in table 2.1 the silicon carbide material has a higher bandgap energy compared to silicon. The increased energy required to move the valence band electron to the conduction band enables higher electric field breakdown strength. This is the reason that a silicon carbide Mosfet switch can withstand high temperatures before the breakdown and it also has better thermal conductivity, about 3.5 times compared to the silicon counterparts [32]. Also, the electron mobility of the silicon carbide MOSFET is much better than the silicon-based MOSFETs which allows silicon carbide MOSFETs to operate at higher frequencies.

2.4.2 GaN material

Both SiC and GaN have a superior relationship between on-state resistance and breakdown voltage due to their higher electric field strength. GaN and SiC have a higher bandgap and electric field strength that allows the devices to be smaller for a given breakdown voltage requirement. Also, the GaN switches have the extra advantage of enhanced mobility of electrons. This makes the GaN devices much

smaller than SiC device for a given rating. For the similar on-state resistance, the power losses will be much lesser compared to SiC [33]. Due to a fast turn on and turn off time, the switching losses will be much lower which is attained by the very low gate capacitance.

2.5 Control system of PFC circuit

Power factor correction is increasingly important due to the high regulation of controlling the harmonic content on the supply side. The digital PFC is related to the conventional boost PFC with the product of output voltage feedback combined with input current and voltage to provide essential harmonic correction and a high power factor for AC/DC systems. For the design of an apt control system, it is necessary to know the parameters of the totem pole PFC circuit initially. Thus the parameters needed for the totem pole PFC circuit is calculated and later they are implemented to design a control system.

2.5.1 Calculation of parameters for totem pole PFC circuit

The design of a PFC circuit is much dependent on the dimension of the components. A DC link capacitor will have a huge impact on controlling the ripple of the DC link voltage. The apt choice of the transistor is necessary for any switched-mode converter to operate efficiently. The boost inductance will state the slope of the inductor current in every interval. It needs to be small enough to allow for the high switching frequency and large enough to limit the current ripple to its maximum allowed value [8]. Thus it is necessary to model the parameters with the right values for an optimal design. Thus, various parameters for a totem pole PFC circuit which needs to be designed is calculated as follows.

2.5.1.1 Calculation of Inductance

The inductor current ripple at any given point in AC mains cycle can be given as [10],

$$\Delta i_L(t) = \frac{1}{L} \int_{t=0}^{D \cdot T_{sw}} v_{AC}(t) dt \tag{2.1}$$

where D is the duty cycle which can be calculated as,

$$D_{boost}(p) = 1 - \frac{V_{AC}(p)}{V_{DC}} \tag{2.2}$$

As the switching frequency is higher than the fundamental frequency, it can be considered as constant over one switching period giving,

$$\Delta i_L(t) = \frac{T_{sw}}{L} D(t) V_{AC}(t) \tag{2.3}$$

Now using the boost converter voltage ratio, taken from [9]

$$\frac{V_{DC}(t)}{V_{AC}(t)} = \frac{1}{1 - D(t)} \tag{2.4}$$

Now by simplifying, (2.3) can be rewritten as,

$$\Delta i_L(t) = \frac{T_{sw} V_{DC}}{L} D(t)(1 - D(t)) \tag{2.5}$$

For the operation of a PFC in CCM at full load, the input inductor current is designed to keep the current ripple under 20% of the maximum peak input current. The maximum input current occurs at the peak input RMS voltage in full load and based on these factors the inductance value can be calculated as,

$$L \geq \frac{D(1 - D)V_{DC}V_{AC}}{\Delta i_L \sqrt{2} P_{out} f_{sw}} \tag{2.6}$$

V_{out} is the DC output voltage, V_{AC} is the input voltage, P_{out} is the output power [11].

2.5.1.2 Calculation of Capacitance

The basic equation for the capacitor used to give a peak to peak voltage ripple of 20 V is depicted as [8],

$$\Delta v_{DC}(t) = \frac{1}{C} \int_t i_{DC}(t) dt \tag{2.7}$$

The fundamental component is always sinusoidal and hence the integral will be as largest over one positive or negative cycle of i_{DC}. Thus integrating over the positive half period and inserting ωt with dt= dωt/ω, the voltage ripple will become [8]

$$\Delta v_{DC}(t) = \frac{1}{\omega C} \int_{\omega t=0}^{\pi} I_{DC} sin(\omega t) d\omega t \tag{2.8}$$

$$= \frac{2}{\omega C} I_{DC} \tag{2.9}$$

Due to input double-line frequency ripple on the DC link capacitor, it's capacitance is mainly determined by the output voltage ripple. It can be given by,

$$C_{min} \geq \frac{(\frac{P_{out}}{V_{DC}})}{4\pi f_{grid} \Delta v_{DC}} \tag{2.10}$$

2.5.2 Closed control loop system

The Power Factor (PF) is defined as the ratio between an AC input's real and apparent power. PF can be further defined as the product of current distortion and phase shift while assuming the input voltage to be a perfect sine wave. For the consideration of this, two tasks are primarily necessary to be accomplished. Initially, there must be a control of the inductor current while making the current sinusoidal and in phase to the input voltage. Secondly, there must be a control of the output

voltage to ensure voltage stability. This is done with the help of two control loops such as the current control loop and voltage control loop. Furthermore, the detailed functionality and theoretical modeling of the current and voltage control loops will be discussed in the following subsections.

2.5.2.1 Current Control Implementation

The current control loop which is the inner control loop is implemented first since it needs to be fastest to provide a proper response to the reference signal from the outer control loop. Thus current control is developed first which is the inner control loop.

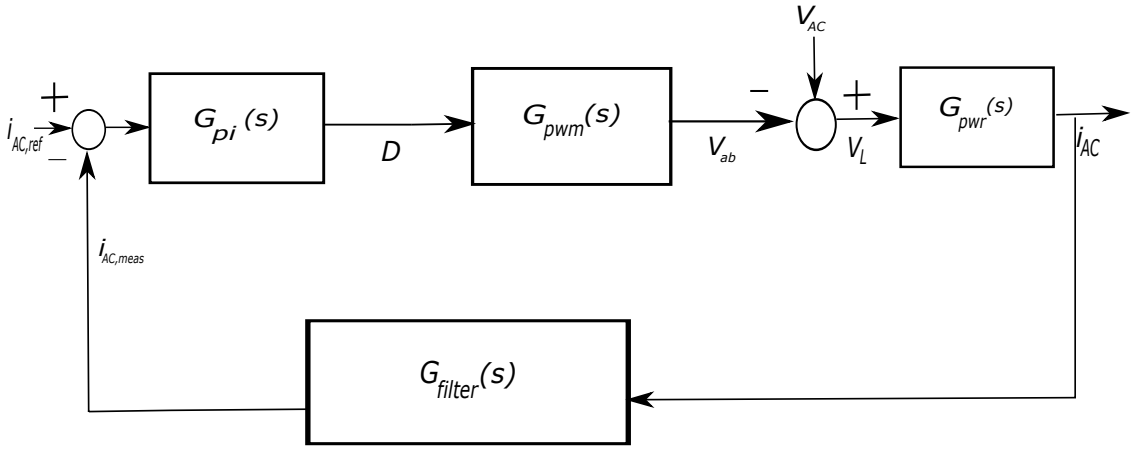


Figure 2.7: Current Control Loop

The laplace transform for the current control is shown in figure 2.7 where G_{pi}, G_{pwm}, G_{pwr}, G_{filter} represent the transfer function of a PI controller, pulse width modulation, power stage and current measurement filter respectively. The general transfer function for a PI controller is as follows,

$$G_{pi} = K_{pi}(\frac{T_{ii}(s)+1}{T_{ii}(s)}) \tag{2.11}$$

where K_{pi} is the proportional gain of the controller and T_{ii} is the integrator time constant. Now the transfer function of the PWM is normally modelled as a switching frequency time dependent delay where the time delay can be given as $T_{delay,pwm} = T_{sw}$ / 3. Thus the transfer function of PWM is given by,

$$G_{pwm}(s) = \frac{1}{1+T_{delay,pwm}(s)} = \frac{1}{1+\frac{T_{sw}}{3}(s)} \tag{2.12}$$

Since the fundamental harmonic current through the inductor needs to be controlled, the power stage can be considered as an inductor. Thus the inductor current can be expressed as,

$$i_{AC} = \frac{V_{AC}(s) - V_{ab}(s)}{R_L L(s)} \tag{2.13}$$

where R_L is the equivalent inductor resistance. From the control point of view V_{AC} and V_{ab} can be visualized as disturbances. Hence from (2.13), the transfer function of the power stage can be written as,

$$G_{pwr}(s) = \frac{V_{AC}(s)}{V_{ab}(s)} = \frac{1}{R_L} \frac{1}{1 + \frac{L}{R_L}(s)} \tag{2.14}$$

The purpose of the current measurement filter is to suppress the switching high frequencies going into the controller and generating more harmonics. Hence a simple first-order low pass filter is used, with the transfer function,

$$G_{filter}(s) = \frac{1}{1 + T_{filter}(s)} \tag{2.15}$$

where T_{filter} is the filter time constant.

The open loop transfer function will become as follows,

$$G_{ol,}i_{(}s) = G_{pi}(s)G_{pwm}(s)G_{pwr}(s)G_{filter}(s) \tag{2.16}$$

$$= \frac{K_{pi}}{T_{ii}R_L} \frac{1 + T_{ii}(s)}{s(1 + T_{pwm}(s))(1 + \frac{L}{R_L}(s))(1 + T_{filter}(s))} \tag{2.17}$$

In order to simplify the equation we use $T_L = \mathrm{L}/R_L$ and $T_{tot,i} = T_{ii} + T_{filter}$ Hence, now the open loop transfer function in (2.17) can be given as,

$$G_{ol,i}(s) = \frac{K_{pi}}{T_{ii}R_L} \frac{1 + T_{ii}(s)}{s(1 + \frac{L}{R_L}(s))(1 + T_{tot,i}(s))} \tag{2.18}$$

$$= \frac{K_{pi}}{T_{ii}L} \frac{1 + T_{ii}(s)}{s^2(1 + T_{tot,i}(s))} \tag{2.19}$$

And finally the resulting closed loop transfer function can be found out as,

$$G_{cl,i}(s) = \frac{1 + T_{ii}(s)}{1 + T_{ii}(s) + \frac{L \cdot T_{ii}}{K_{pi}}(s^2) + \frac{L \cdot T_{ii} \cdot T_{tot,i}}{K_{pi}}(s^3)} \tag{2.20}$$

2.5.2.2 PI Controller parameters for current controller

The PI controller parameters can be chosen based on the symmetrical optimum design equations which are taken from the reference compendium [14],

$$T_{ii} = \beta T_{tot}, i \tag{2.21}$$

$$K_{pi} = \frac{L}{\sqrt{\beta} T_{tot,i}} \tag{2.22}$$

$$\omega_{ci} = \frac{1}{\sqrt{\beta} T_{tot,i}} \tag{2.23}$$

Here ω_{ci} is the crossover frequency and β is given by the phase of the transfer function that is shifted from $(1/\beta T_{tot,i})$ to $T_{tot,i}$.

The current control loop is necessary to be at least half a decade slower than the switching frequency to make the switches act based on the control signals. Hence on consideration of this, the control parameter ω_{ci} in (2.23) is taken at a range of $10^{-0.5} * \omega_{sw}$, where ω_{sw} is the switching angular frequency.

For determining the parameters of the controller based on (2.21), (2.22) and (2.23), initially the filter time constant T_{filter} has to be known. The main use of the filter time constant is that it reduces the ripple of the duty cycle generated and it allows the control loop to maintain a quick response as well. The normal value chosen for the ripple of the duty cycle can be in the range of 0.04 to 0.08, where the larger ripple enables a quicker response [8].

2.5.2.3 Calculating the ripple of the control signal in Current Controller

The ripple of the control signal which is D is caused by the proportional gain and will be limited by the integrator time constant. Considering this and neglecting the integrator part of the PI controller and reference current which has no ripple the following equation can be established based on figure 2.7 and (2.11), [8]

$$\frac{D_{ripple}(s)}{i_{AC,ripple}(s)} = K_{pi} \frac{1}{1 + T_{filter}} \tag{2.24}$$

However at the actual frequency the amplitude of the ripple can be expressed as,

$$D_{ripple}(s) = K_{pi} \frac{1}{\sqrt{1 + (T_{filter} \omega_{ripple})^2}} (\Delta I_L(\omega_{ripple})) \tag{2.25}$$

Now substituting the value of K_{pi} from (2.22) in (2.25) tends to give out the ripple value as,

$$D_{ripple}(s) = \frac{1}{\sqrt{\beta} T_{tot,i}} \frac{1}{\sqrt{1 + (T_{filter} \omega_{ripple})^2}} (0.5 \Delta I_L(\omega_{ripple})) \tag{2.26}$$

Now on substituting β in 2.26, with the value of ω_{ci} from (2.23), the final expression for the ripple can be expressed as,

$$D_{ripple}(s) = \omega_{ci} L \frac{1}{\sqrt{1 + (T_{filter}\omega_{ripple})^2}} (0.5\Delta I_L(\omega_{ripple})) \tag{2.27}$$

From (2.27), we can see that there are two free variables ω_{ci} and T_{filter} which are responsible for deciding the ripple of duty cycle. As discussed in (2.23), the crossover frequency ω_{ci} can be chosen at a range near to $10^{-0.5} * \omega_{sw}$ where β can be in reasonable limits from the range of 1 to 25 [8].

Hence, (2.27) can be solved graphically by plotting D_{ripple} and T_{filter} at the switching frequency where ω_{ripple} is equal to ω_{sw}. Estimating and categorizing the quick controller response compared to low control signal ripple, the amplitude of D_{ripple} can be chosen to be at 0.08. This is shown in figure 2.8,

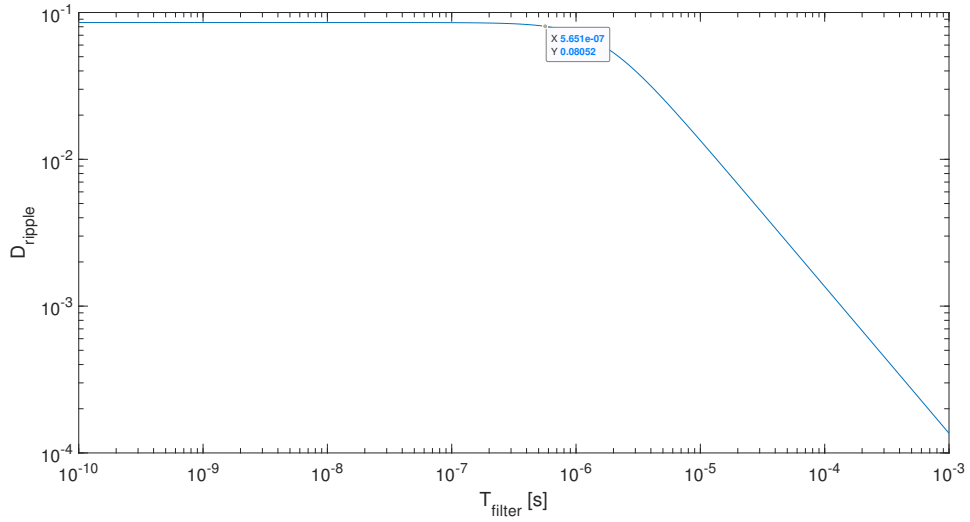


Figure 2.8: Graphical solver for current controller

where T_{filter} is obtained to be 0.56 μsecs at a chosen ripple of 0.08.

On substituting this in (2.21), (2.22) and (2.23), the control parameters could be found to be as $\beta = 6.5280$, $K_{pi} = 0.8545$ and $T_{ii} = 25.6$ μsecs.

These values are implemented in the PI controller and the response of the current controller is discussed in the results section.

2.5.2.4 Voltage control Implementation

The voltage control loop is the outer control loop which is slow as compared to the current control loop. It has the major responsibility of controlling the output DC voltage so that it is maintained at specified values. As the DC voltage is controlled based on an AC grid voltage and since the chances of occurring complete alterations in the voltage will be small. Hence the control of the voltage do not need to be as quick as it will only respond to slow alterations. Although if there are large

alterations, the slow voltage is enough to ensure that the DC voltage does not drop below the minimum level. Furthermore, if there is a large voltage drop occurring on an AC side for instance like a lightning strike, a surge diode can be added for the protection by shorting the AC voltage to DC link capacitor when the grid voltage is greater than the DC link voltage [8].

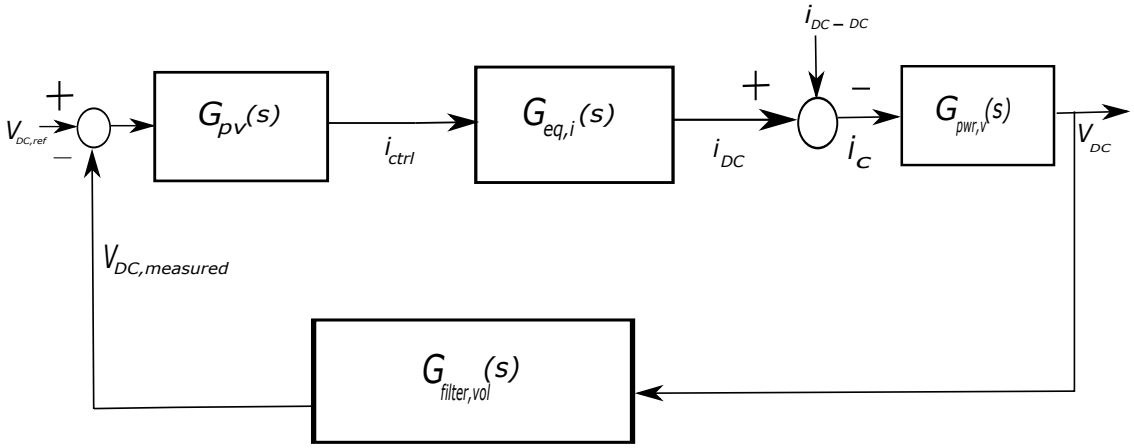


Figure 2.9: Voltage Control Loop

The voltage controller is also implemented similarly as the current controller where the transfer function is defined as follows,

Figure 2.9 shows the block diagram of the voltage control loop. The PI controller of the voltage control loop is defined similar to a current controller and can be modeled as,

$$G_{pv} = K_{pv}\frac{T_{iv}(s)+1}{T_{iv}(s)} \tag{2.28}$$

As the voltage loop need not necessarily to be as quick as a current controller, and hence a simple low pass filter is chosen and the transfer function for the chosen low pass filter is given as,

$$G_{filter,vol}(s) = \frac{1}{1+T_{filter,v}(s)} \tag{2.29}$$

For simplifying things, we can approximate the equivalent first order transfer function to the current controller closed loop transfer function which has a delay of $T_{eq,}i$ = 2 ·$\mathrm{T}_{tot,i}$, where $T_{tot,i} = T_{pwm} + T_{filter,v}$. Hence the equivalent transfer function becomes

$$G_{eq,i}(s) = \frac{1}{1+T_{eqi}(s)} = \frac{1}{1+2T_{tot,i}(s)} \tag{2.30}$$

The power stage of the voltage controller is given by the DC link capacitor. The Laplace equation for the power stage transfer function can be given as,

$$G_{pwr,v}(s) = \frac{V_{DC}(s)}{i_c(s)} = \frac{1}{C(s)} \tag{2.31}$$

On seeing figure 2.9 we can say that, the DC link voltage V_{DC} is governed by a DC link capacitor current where i_c= i_{DC} - i_{DC-DC} which implies that $i_c(t)$ = C (dV_{DC}/dt). As the ESR is negligible in a DC-link capacitor, it can be modelled as a pure capacitance.

Now on combining (2.28), (2.29), (2.30) and (2.31) along with figure 2.9, the voltage controller open loop transfer function becomes:

$$G_{ol,v}(s) = G_{pv}G_{eq,i}(s)G_{pwr,v}\,(s)G_{filter,vol}(s) \tag{2.32}$$

$$= \frac{K_{pv}}{T_{iv} \cdot C} \frac{1 + T_{iv}(s)}{s^2(1 + 2(T_{tot,i})(s))(1 + T_{filter,v}(s))} \tag{2.33}$$

Similar to current controller, the filter and PWM time constant can be combined to one where $T_{tot,v}$ = 2 ·$T_{tot,i}$ + $T_{filter,v}$. Thus, the open loop transfer function becomes,

$$G_{ol,v} = \frac{K_{pv}}{T_{iv}C} \frac{1 + T_{iv}(s)}{s^2(1 + T_{tot,v}(s))} \tag{2.34}$$

Hence from the open-loop transfer function of the voltage controller, we can see that the PI control parameters are unknown. This can be found out by using the method of symmetrical optimum, similar to the current controller. This shall be discussed in the following.

2.5.2.5 PI Controller parameters for voltage controller

As discussed in the section 2.5.2.2, the voltage control parameters can also be taken from the reference compendium [14] such as,

$$T_{iv} = \beta T_{tot,v} \tag{2.35}$$

$$K_{pv} = \frac{L}{\sqrt{\beta} T_{tot,v}} \tag{2.36}$$

$$\omega_{cv} = \frac{1}{\sqrt{\beta} T_{tot,v}} \tag{2.37}$$

Since the bandwidth of the voltage controller is slower than the voltage controller, the crossover frequency ω_{cv} is chosen to be at least half a decade slower than the current controller frequency. The filter of the voltage controller can be designed

similar to the current controller and the output ripple of the controller can be found in an exact way as a current controller. It can be found out to be as,

$$i_{ripple}(s) = \omega_{cv} C \frac{1}{\sqrt{1 + (T_{filter,v}\omega_{ripple})^2}} (0.5\Delta v_c(\omega_{ripple})) \tag{2.38}$$

where i_{ripple} is the output from the voltage PI controller. The major responsibility of the voltage controller is to reduce the ripple in i_{ripple} to reduce the harmonics generated in the current controller. Since the crossover frequency is low, it is quite hard for the controller to respond to quick changes. It would give a poor stability performance of the controller.

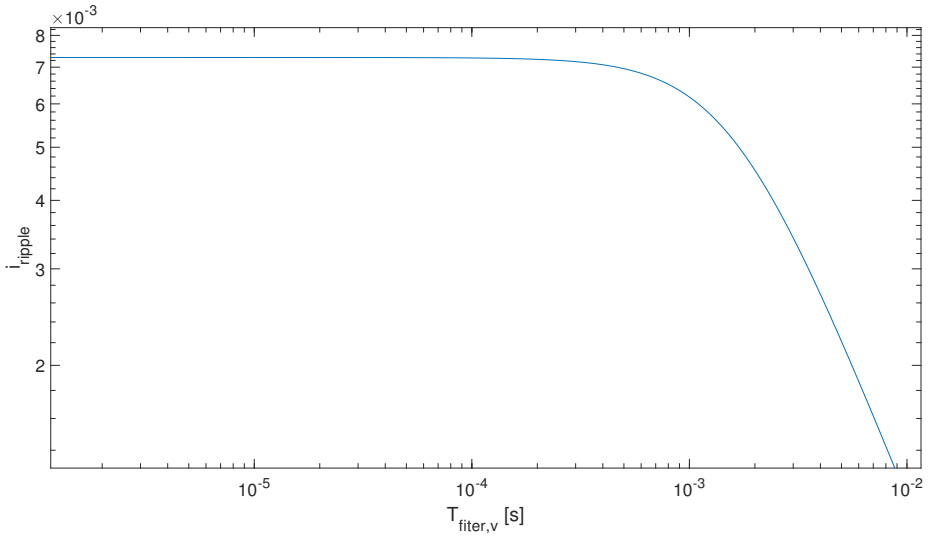


Figure 2.10: Graphical solver for Voltage controller

While plotting i_{ripple} and $T_{filter,v}$ in figure 2.10, we tend to see that i_{ripple} never exceeds 0.01. This low value will not be able to damp the ripple, as the current controller is quicker. Thus, $T_{fiter,v}$ can be chosen to be approximately 100 μ secs which will have the β value at an acceptable range of 1 to 25 of about 8.60. On substituting this in (2.35) and (2.36), we tend to get $K_{pv} = 0.29$ and $T_{iv} = 930$ μ secs. These controller parameters can be used while designing the controller and the obtained waveform for the voltage controller is illustrated in the results section.

2.6 Power losses in the charging system

The power losses in the circuit is an important aspect that needs to be considered while designing the circuit. The most predominant power loss components in the charging system are the boost inductor, the power MOSFET, and a DC link capacitor.

2.6.1 Boost inductor losses

Boost inductors require a huge space in a PFC converter. For a compact PFC converter, inductor design is needed to be taken into account. Furthermore, the power loss associated with the inductor has a relationship with inductors size as well. The inductor power loss is calculated based on the following equations which are taken from reference [14],

$$P_{loss} = P_{core} + P_{L,cu} \tag{2.39}$$

The core loss here is not taken into consideration as it is negligible. The inductor current $I_{L,RMS}$ is found out by using the CCM boundary condition,

$$I_{L,RMS} \geq \frac{\Delta I}{2} \tag{2.40}$$

where ΔI is the current ripple which is given by,

$$\Delta I = \frac{V_L D}{L f_{sw}} \tag{2.41}$$

Hence the inductor copper loss can be calculated by,

$$P_{L,cu} = (I_{L,RMS})^2 DCR \tag{2.42}$$

where DCR is the DC resistance specification of the inductor which can be taken from the datasheet [13] [14].

2.6.2 DC-link capacitor losses

While calculating the DC-link capacitor losses the reactance of the capacitance needs to be determined

$$X_c = \frac{1}{2\pi f_{sw} C} \tag{2.43}$$

After knowing the reactance, ESR of the capacitor can be calculated as follows

$$ESR = tan\delta Xc \tag{2.44}$$

where $tan\delta$ is take from datasheet [20]. Now the losses can be calculated as

$$P_{cap} = I_{c,rms}^2 ESR \tag{2.45}$$

where $I_{c,rms}$ is the rms output capacitor current.

2.6.3 Gate losses

A gate is an important pin in a Mosfet switch. It is capable of turning on and off of the MOSFET switch. A gate driver loss is nothing but the energy required to charge the MOSFET gate. The gate driver losses are frequency-dependent and also depends on the gate capacitance of the MOSFET. Thus losses in the MOSFET

switch increase as the switching frequency increases[30]. The gate driver loss is given by

$$P_{gate} = Q_{G(tot)} V_G f sw \tag{2.46}$$

where $Q_{G(tot)}$ is the total gate charge, V_G is the gate voltage and f_{sw} is the switching frequency.

2.6.4 Power Mosfet Losses

The efficiency of the charging system highly depends on the performance of the switching devices. There are two kinds of losses in the power MOSFET; the on-state losses or the conduction losses and switching losses. In low-frequency applications, the conduction losses will be dominant. But in high-frequency applications such as SMPS circuits, the switching losses play a pivotal role in the efficiency of the charging system.

The conduction losses in the power MOSFET can be expressed as

$$P_{conduction} = R_{ds,on} I_d^2 D \tag{2.47}$$

where $R_{ds,on}$ is the on-state drain-source resistance, the I_d is the drain current through the power mosfet and where D is the the duty cycle. The duty cycle of the totem pole circuit can be calculated by using

$$D = \frac{V_o - V_{in}}{V_o} \tag{2.48}$$

where V_o and V_{in} are the output and input voltages respectively. The duty cycle for a normal buck or boost converter can be calculated using

$$D = \frac{t_{on}}{T_s} \tag{2.49}$$

where t_{on} and T_s are the switching on-time and total switching time.

The switching losses of the power mosfet can be calculated using the following expression,

$$P_{switching} = 0.5 V_{ds} I_d f_{sw} t \tag{2.50}$$

where V_{ds} is the voltage between drain and source and f_{sw} is the switching frequency and t is the switch on and off time. The total power loss in the Mosfet can be calculated as

$$P_{loss} = P_{conduction} + P_{switching} + P_{gate} \tag{2.51}$$

The loss calculation mentioned above is done considering various approximations. The other way to perform the same is to find the product of the actual voltage and the current and to plot them in LTSpice and calculate the energy by integrating the power waveform for the specified on, off and conduction time period. Now, the loss can be calculated by dividing the energy by the total switching time period.

2.7 Thermal derating of power electronic components

The power electronic components are much dependent on the temperature. Their performance tends to affect due to the influence of temperature. The main reason behind this is that the resistance changes with temperature. The resistance of the component is directly proportional to temperature. Any power electronic component operation leads to different kinds of losses in the system which leads to an increase in temperature. The increase in temperature also leads to an increase in power losses which in turn reduces the total power dissipated by the MOSFET thus causing derating of the MOSFET. Hence the temperature of the switch needs to be maintained within the safe limits as mentioned in the component's datasheet to improve the efficiency and also to increase the longevity of the component.

2.7.1 Heat transfer modes

Heat conduction is the thermal diffusion via atomic level randomized interaction in solids, as well as in stationary fluids and gases [21]. In solids, the mechanisms are molecular lattice vibration and movement of free electrons and in fluids and gases with randomly moving molecules by diffusion and collisions[21]. In power electronic circuits the conductive heat transfer happens within the MOSFET switch like from case to the thermal pad and heat sink. The heat transfer due to conduction is given by

$$q_{cond} = -\lambda A \frac{dT}{dx} = -\lambda A \frac{\delta T}{l_{thick}} \tag{2.52}$$

where λ (W/mK) is the thermal conductivity of the material and A is the area of the cross-section in m^2 and dT is the temperature gradient between the two parts in K and l_{thick} is the thickness of the material.

The convective heat transfer occurs between a surface and a moving liquid or air. The process incorporates both conduction close to the surface interface where cooling medium motion rate approaches zero speed, and heat transfer by the moving cooling medium increases where the heat transfer rate increases with increasing fluid motion rate [21]. If the heat transfer takes place by any external factor where the fluid motion rate is increased by pumps, a fan is called forced convection else it is natural convection. The convective heat transfer is given by

$$q_{conv} = hA(T_{surf} - T_{fl}) \tag{2.53}$$

where T_{surf} and T_{fl} are the surface and fluid temperature respectively.

The thermal radiation is the heat transfer in the form of electromagnetic waves and photon from the surface to the colder surroundings [21]. The thermal heat radiation is given by

$$q_{rad} = \epsilon \sigma A(T_{surf}^4 - T_{surr}^4) \tag{2.54}$$

where $\sigma = 5.678010^{-}8\ W/m^2K^4$ is the Stefan Boltzmann constant [13] and T_{surf} , T_{surr} are the surface and surrounding temperature in K

2.7.2 Lumped thermal modelling

The temperature analysis of the MOSFET switch can be done in different ways. Since Finite element Analysis (FEA) is not used in this project a simple lumped thermal model is built to analytically determine the junction temperature. Heat transfer, in reality, will be three dimensional. However, it is modeled in fewer dimensions for simplicity under the assumption of dimensional interdependence. An ideally working thermal model must capture the main flows of heat transfer between the components. In a lumped thermal model thermal resistance of different component are determined and these individual thermal resistances are lumped together so that it can represent the complete switch. These thermal impedances are determined using geometric and material properties[21]. The thermal network is analogous to an electric network where heat transfer represents the current flow and temperature as voltage.
During the thermal steady state, the temperature difference between the two adjacent nodes can be described by the relation [21]

$$T_i - T_j = G^{-1}P \tag{2.55}$$

where P is the power loss injected into the power node and G is the thermal conductance of the component. T_i, in this case, will be the junction temperature and T_j is the ambient temperature.

2.8 Power losses for thermal analysis

As the on-state resistance of the MOSFET varies with temperature, the power losses of the MOSFET tends to increase with temperature. To perform an efficient thermal analysis, this condition has to be considered. Hence by performing a thermal analysis with constant on-state resistance initial temperature values of the MOSFET can be obtained. With these values, the change in resistance with temperature can be obtained which will be explained late in the coming sections. By determining the new varying resistance the power loss can be calculated accordingly. The power loss calculation explained in section 2.6.4 can be used to calculate the power loss for one switching period. But to calculate for the entire time period, the following equation can be used [30]

$$P_{conduction} = I_d R_{ds}^2 \tag{2.56}$$

where I_d is the rms drain current and R_{ds} is the on-state resistance.

$$P_{switching} = V_{ds} I_d f_{sw} \frac{Q_{gs} + Q_{gd}}{I_g} \tag{2.57}$$

where Q_{gs}, Q_{gd} are the gate-source and gate-drain charges. I_g is the gate current.
The gate drive losses are calculated as explained in section 2.6.4. Since there are no drivers implemented for the MOSFET switches in Simulink the driver losses are neglected.

2.9 Cost Analysis

The cost of the product is the prior objective in any design. High production costs may cause hindrance to use certain technologies which are highly useful for many applications. It is necessary to optimize the converter within its costs. To make a cost-effective comparison of two different materials, in this case, SiC and GaN switches, a life cycle cost analysis (LCCA) is performed. Life cycle costs are all the costs generated during the lifetime of an item [25]. The different costs occurred at different time during the life cycle of the material is illustrated through LCCA. The LCCA of a converter can be chosen based on the sum of initial cost, maintenance cost and energy cost where the calculation of each cost is discussed further [24].

The initial cost is the purchase costs of the system components which include inductor cost, capacitor cost, two silicon MOSFET costs, and two GaN or SiC switch costs. It also includes the sum of heat sink costs, digital signal processing controller costs, current sensor costs, two temperature sensor costs, two auxiliary power supply costs, and three RCD relays costs. The energy costs are the total energy consumed for a given year and it is calculated based on the function below, [25].

$$C_{eng} = \sum_{n=1}^{N_{life}} \frac{C_{elec,n} \cdot E_{loss,n}}{(1+r)^n} \tag{2.58}$$

where C_{eng} is the energy costs, N_{life} is the operational life, $C_{elec,n}$ is the cost of electricity and $E_{loss,n}$ is the total energy loss in the nth year. The total energy loss $E_{loss,n}$ is calculated amount of energy lost per year in both SiC and GaN, which is calculated from the power losses in the switch. Similarly 'r' is the discount factor and is assumed to be 2.5 % which represents the impact of interest and inflation rate [25]. The cost of electricity is the constant value of about 0.199 SEK/kwh. The maintenance cost is taken with an assumption of 250 SEK per annum. As this is an off-board portable charger the installation costs are neglected. The operation cost and the downtime cost are not considered for this analysis since it is analyzed for household purposes. The LCCA is analyzed for 15 years period and the cost is compared between SiC and GaN switches. The obtained results are discussed further in the results section.

3
Case Set-up

To implement control for an off-board charger, a PFC circuit is designed in an open-loop and a closed-loop system. The open-loop design is done in Ltspice, while the closed-loop is implemented in Simulink where a feedback loop involving a PI controller for the control of the switches was designed. In an open-loop system, various parameters are calculated and the difference between the SiC and GaN switch while implementing is studied along with the gate driver circuit. The switching characteristics of SiC and GaN are mainly studied when the open-loop design is made in LTSpice. Finally, a lumped thermal model and various thermal losses will be calculated to analyze the thermal performance of the switch.

3.1 Design of PFC circuit

In a totem PFC circuit, calculating and evaluating the values of the components are necessary to the specification of the design of the circuit. The specification of the design of the totem pole PFC is based on producing a prototype that has high efficiency and power density. These specifications are tabulated as shown in table 3.1,

Table 3.1: Design Specifications

Specification	**Value**	**Units**
Input Voltage - AC	230	V_{rms}
Frequency	50	Hz
Input Current - AC	16	A
Output Voltage - DC	400	V
Output Power - DC	3300	W
Switching Frequency - PFC	100	kHz
Grid Frequency	50	Hz
Maximum Inductor Current Ripple	20	%
Maximum DC link Voltage Ripple	20	V

Several parameters such as inductance, capacitance will play a huge role in a change in voltage and current of the circuit. Hence it is essential to model them with the right values for the building of the basic simulation model of the circuit. The calculation of the parameters for the design specification is discussed in the following.

3.1.1 Designing Inductance

Based on design specifications and the inductance derived in section 2.5.1.1, the optimal inductance for the design can be calculated as

$$L \geq \frac{(0.19(1-0.19))(400)(230)}{0.2(\sqrt{2})(3300)(100kHz)} = 152\mu H \tag{3.1}$$

3.1.2 Designing Capacitance

Similarly the optimal capacitance can be calculated with the assumption of voltage ripple as 20 V,

$$C_{min} \geq \frac{(\frac{3300}{400})}{(4\pi 50)20} = 0.65mF \tag{3.2}$$

3.1.3 Choosing the suitable transistors

The apt choice of the transistor is required in any part of the design. Here the transistors are chosen based on switching frequency, keeping in mind the high-efficiency requirement of the portable charger. The major importance of the transistor is the ability to withstand a high peak current, RMS current, and peak blocking voltages. Considering the heat sink as well, the transistor should handle its dissipated heat without melting. When considering the different aspects of the switch, the other major factor is that the current should be able to flow in both the directions of all the switches. It also needs to handle high switching frequencies, around 100 kHz with minimum losses and high-efficiency [8].

3.1.4 Modelling of SiC and GaN switches

As mentioned in the previous section, based on the constraints it is required to design the control based on four transistors which are operating at a high-frequency range of around 100 kHz. In the high-frequency range and with the required rating, silicon power MOSFETs and GaN HEMTs proves to be the most suitable transistors. They are efficient at high switching frequency due to the lack of minority carriers required to be moved in and out of the transistor during switching whereas this is a loss concern in BJTs and IGBTs. The high breakdown field of GaN allows for the smaller physical embodiment of transistors compared to SiC and Si MOSFETs. Hence they help in quicker switching transients and lower switching losses. GaN HEMTs does not have a reverse body diode which significantly acts as an advantage compared to other MOSFETs. As the reverse recovery losses are severe in CCM operation of a totem pole PFC, the lack of a reverse body diode is beneficial for reducing the losses [8].

In this project, a comparison is to be made between Silicon carbide and Gallium nitride MOSFET switches. The ratings of the MOSFET are chosen such that, it can withstand the power of the rectifier circuit. The minimum and maximum limit of different ratings for choosing the suitable MOSFET are shown in the table below.

Table 3.2: Maximum and minimum parameters for choosing the right mosfet

Parameters	Minimum	Maximum
Blocking voltage	650 V	1200 V
Current	25 A	40 A
On state resistance	$15m\Omega$	$150m\Omega$
Temperature	-55° C	150° C

Based on the limits mentioned in table 3.2, MOSFET switches from different companies are surveyed to choose the suitable MOSFET for this study. It is found that the silicon carbide switch from CREE and gallium nitride switch from Transphorm fulfills all the limitations required for the circuits and also it is suitable from the business perspective as the switches are cheap and reliable compared with other manufacturers. The SiC and GaN switches are chosen in such a way so that the ratings are similar to make a fair comparison. The rating of both the switches is shown in the table below.

Table 3.3: SiC and GaN switch ratings

Parameters	Cree C2M0080120D(SiC)	Transphorm TP65H050WS (GaN)
Blocking voltage	1200 V	650 V
Continuous drain Current	36 A	36 A
On state resistance	$80m\Omega$	$60m\Omega$

LTSpice SiC and GaN models are used from these manufacturers to implement the open-loop system in Ltspice to analyze the switching characteristics. A similar method is used to model the other two silicon MOSFET. Since there are no readily available silicon MOSFET models in LTSpice, an inbuilt model from LTSpice is taken and their properties are modified to match the requirements mentioned in the table 3.2.

The SiC and GaN HEMTs are modeled only in LTSpice, however, they are not modeled in Simulink while performing the closed-loop. Thus they are implemented in Simulink as MOSFETs with no reverse recovery charge or forward voltage in a body diode. They are also implemented with the same on-state resistance. Further, the MOSFETs which are in the library of Simulink itself does not contain a parasitic capacitance and thus the gate charge is assumed to be small. Hence the switching will be much faster.

3.1.5 Implementation of gate driver circuit

Similar to any other switched-mode converter, in a PFC as well as in the gate driver circuit and control systems it is equally important as they control the voltage and

current across the switches by making them flow in the right way. Gate circuits act as a link between a nonlinear behavior of the transistors and the linear behavior of the converter. The gate drivers make the linear control signal to switch the transistors on and off so that the voltages and current of the switching period behave in the right way. The gate drive logic is implemented in Simulink. For a simple understanding, the switches and delay blocks can be ignored as they do not affect the logic perspective [8]. Two legs are used for PWM switching namely MOSFET switching leg and GaN switching leg. The gate drive logic circuit for the PWM generation is shown in figure 3.1,

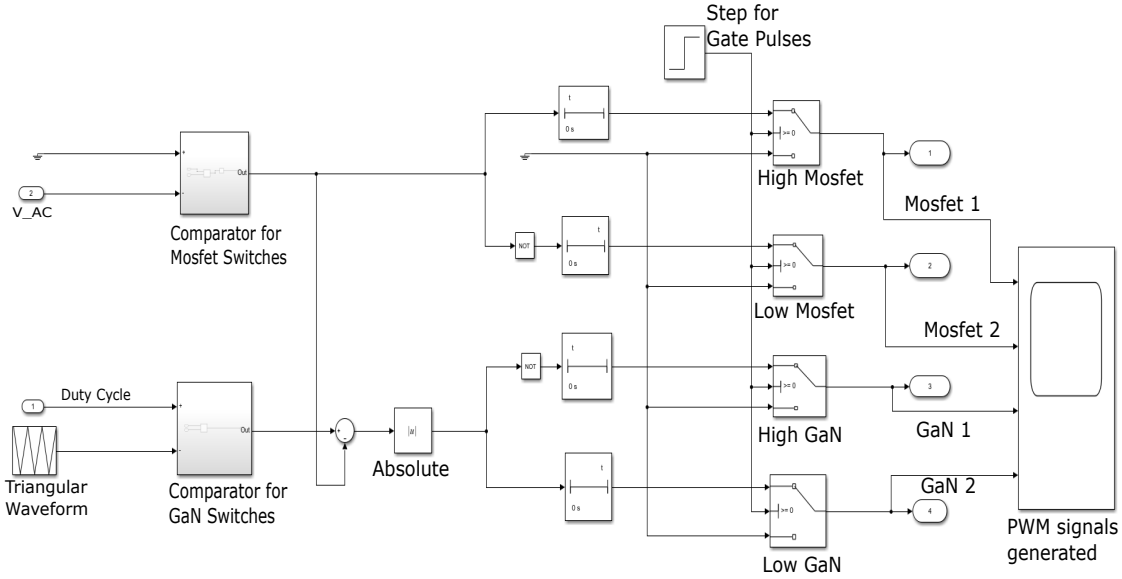


Figure 3.1: Gate Driver Logic

3.1.5.1 Mosfet switching leg

The MOSFET switching leg alternates the DC voltage polarity sensed by the inductor every main half-cycle according to AC voltage polarity. The comparator for MOSFETs as seen in figure 3.1, will make sure that the DC voltage is always with the same sign and the magnitude is higher than the AC voltage so that the power flows in the same direction during both the half cycles [8]. When the AC voltage is compared with the ground, it generates a high voltage when $V_{AC} < 0$ and zero when $V_{AC} > 0$. Hence MOSFET 1 will always conduct during the negative cycle and MOSFET 2 will always conduct during the positive cycle. Both the MOSFETs are complementary to each other, i.e the gate signals need to be logically reverse for the functioning. Hence we use the NOT operator for the switching. For a clear understanding, the functioning of the MOSFET switching leg can be tabulated as follows,

Table 3.4: Functioning of Mosfet switching leg

Mosfets	State	Condition
mosfet 1(t)	0	$V_{AC}(t) > 0$
mosfet 1(t)	High	$V_{AC}(t) < 0$
mosfet 2(t)	High	$V_{AC}(t) > 0$
mosfet 2(t)	0	$V_{AC}(t) < 0$

3.1.5.2 GaN switching leg

The GaN switching legs are switched at a high frequency to shape the boost inductor current. Here the comparator for GaN compares the positive signal of the duty cycle to a reference triangular waveform with an amplitude of 1 generating an output which is nothing but the gate signal. The gate signal is the gate voltage of the boost switch. But the handling of the gate signal varies for the totem pole PFC as compared to the regular boost PFC controller. Similar to the MOSFET switching leg, these GaN switching legs are also acting complimentarily where one switch acts as the boost switch while the other imitates the boost diode. There will be no reverse body diode connected to the two switches which are at the GaN leg and the complementary switch is operated effectively with the help of NOT operator as shown in figure 3.1. Depending on the gate voltage amplitude which can be represented as V_{gate}, the functioning of the two GaN switching legs will vary [8]. The gate signal depends highly on the duty cycle which is strictly positive and the functioning of these gate signals is tabulated as presented in table 3.5

Table 3.5: Functioning of GaN switching leg

GaN switches	State	Condition
GaN 1(t)	1-V$_{gate}(t)$	$V_{AC}(t) > 0$
GaN 1(t)	V$_{gate}(t)$	$V_{AC}(t) < 0$
GaN 2(t)	V$_{gate}(t)$	$V_{AC}(t) > 0$
GaN 2(t)	1-V$_{gate}(t)$	$V_{AC}(t) < 0$

The gate voltages are logical signals true or false. That means the negative half cycle gate signals can be achieved by logically inverting the positive half cycle gate cycles [8]. Thus the gate signals for the negative half cycle can be tabulated as presented in table 3.6,

Table 3.6: GaN switching leg for negative half cycle

GaN switches	State	Condition
GaN 1(t)	V$_{gate}(t) = 1 - \|V_{gate}(t) - 1\|$	$V_{AC}(t) < 0$
GaN 2(t)	1-V$_{gate}(t) = \|V_{gate}(t) - 1\|$	$V_{AC}(t) < 0$

From table 3.6, it can be seen that GaN 1(t) is of the form "1-u" and GaN 2(t) is of the form "u" as that from the positive half cycle depicted in table 3.5. Now for the

gate voltages to function properly, it is necessary to handle "u" properly. An easy way of handling "u" and creating gate voltages can be done by

$$GaN1(t) = 1 - |V_{gate}(t) - mosfet1(t)| \tag{3.3}$$

$$GaN2(t) = |V_{gate}(t) - mosfet1(t)| \tag{3.4}$$

where these equations are implemented in figure 3.1, with the forward connection from the mosfet leg to the GaN leg [8].

3.2 Set up of a control loop system

As discussed in section 2.5.2, two control loops i.e. the current control loop and the voltage control loop are designed to have control of the inductor current and output voltage. The control loops are designed based upon small-signal modeling and quasi-steady-state approach, where the nonlinear voltage and currents are represented as a linear voltage and current around the switching period average [8]. The control of inductor current is done with the help of a current controller where the switching period inductor current is controlled to be shaped sinusoidally in phase with the supply voltage. Similarly, the control of the output voltage is done with the voltage controller where it regulates the DC link voltage to be equal to a defined DC value. PI controllers are used in both the current and voltage loop. The entire PFC control system is designed in Simulink. The design and implementation of a feedback control loop system in Simulink are further discussed below.

3.2.1 Implementation of feedback loop

According to the PFC theory, the arithmetic of the PFC can be categorized into three parts such as:

- The external voltage control loop which ensures that the output voltage follows the reference constant value of the voltage.
- The arithmetic reference which makes the current reference follow the sine reference
- The internal current control loop which makes the input measured current follow the reference current.

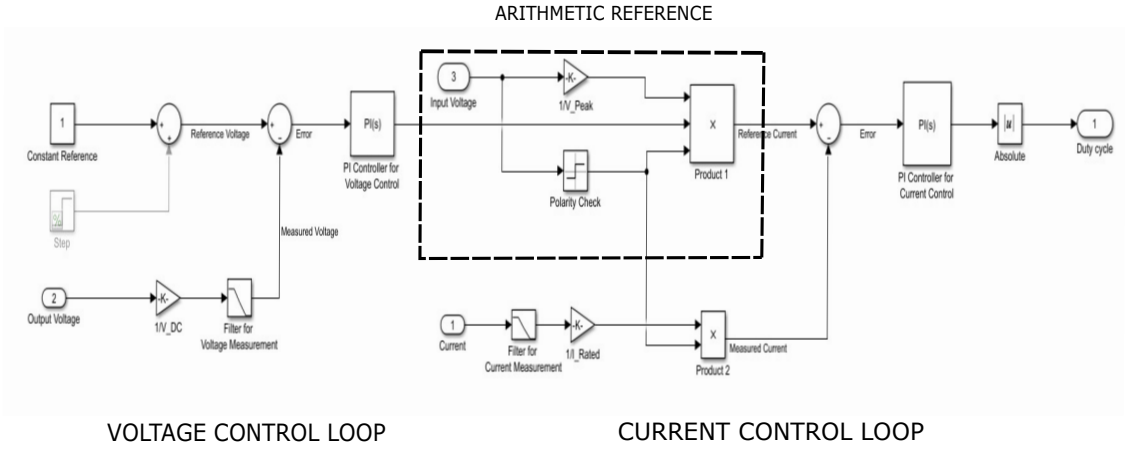


Figure 3.2: Feedback Control Loop

The implementation of the feedback loops for both the controllers are shown in figure 3.2. The current and voltage power stages are analyzed separately. The current mode control is implemented by multiplying the output of voltage controller with the reference of the current control loop where the output of the current control is the duty cycle, which enables the PWM switches to act accordingly. Thus the current control directly controls the duty cycle generated. The prior motive of the current control is to shape the input current to be in phase with the input voltage. Since the inductor current has the possibility of generating more harmonics, a current measurement filter is added to reduce the harmonics. The filter time constant is found according to the procedure discussed in section 2.5.2.1.

Similarly, a power stage of the voltage control is also implemented where a constant value is given as a reference along with the step. The measured DC output voltage is also filtered out with a time constant where the harmonics of the DC output voltages are reduced. The output of the voltage loop control is multiplied with the arithmetic reference where the input AC voltage is divided by the peak value and feed as an input to the current controller. This is done to normalize the loop gain and make it independent of the line voltage through the complete input range. The second input to the multiplier is the instantaneous input voltage that will shape the current reference in phase with the AC voltage to achieve the PFC. The prior motive of the voltage control is to keep the output voltage within a range of control.

3.2.2 Implementation of PI controller

The controller which is implemented is based on a basic current-mode PFC. Since it enables the required CCM operation and constant switching frequency, it is highly suitable for this high power application [8]. PI control is widely used and indeed termed as classical in the control industry. Here, the voltage and current control follow PI arithmetic. The PI control parameters in the PFC are responsible for the power factor, total harmonic distortion (THD), overshoot, undershoot, rise time, steady-state error and settling time. Tuning of the parameters is done by the sym-

metrical optimum method as discussed in sections 2.5.2.1 and 2.5.2.5. The PI control can adapt to different load and line conditions to improve the THD at various levels. Since here we use a power factor based application, voltage, and current errors and total harmonic distortion should be minimized yielding a high power factor and a low THD. PI coefficients which have been derived are added to the PI controller so that the controller is more optimal and yields an efficient result.

3.3 Power Losses Calculations

Based on the equations given in section 2.6, the power losses for various components are calculated here.

3.3.1 Boost inductor

As discussed in section 2.6.1, the inductor loss is calculated here. We know the inductor value which is found out to be 156 μH. The current ripple is calculated from equation given in 2.41,

$$\Delta I = \frac{(110.4)(0.19)}{(156\mu H)(100kHz)} = 1.344A \tag{3.5}$$

The rms voltage of V_L is found to be as 110.4 V from the plots. The inductor current can now be found by substituting ΔI as,

$$I_{L,RMS} \geq \frac{1.344}{2} = 0.672A \tag{3.6}$$

Now on substituting the $I_{L,RMS}$ in power loss equation we get,

$$P_{L,cu} = (0.672)^2(0.052) = 0.0234W. \tag{3.7}$$

where the DCR value is taken from the datasheet [13] for the rated near by inductance used. As mentioned in section 2.6, the core loss is not taken into consideration and the total power loss associated with the inductor will account to copper loss only [14].

3.4 Implementation of lumped thermal model

As explained in section 2.7.2 the heat flows through different materials of the switch which has different areas, material, thickness, and thermal conductivity. Hence the thermal impedance of different materials needs to be determined. The junction to case thermal resistance is available from the datasheet of the switch. Likewise, a thermal pad made of silicon will be attached to the case of the switch to have better thermal performance and also to prevent any short circuit between MOSFET and heat sink. Hence the thermal pad resistance has to be determined to model the conductive heat transfer between the case to the thermal pad. The thermal pad

dimensions will be available in the datasheet and it can be calculated using the following expression [21]

$$R_{th} = \frac{l_{thick}}{\lambda A} \tag{3.8}$$

where l_{thick} is the thickness of the material, λ is the thermal conductivity of the material and A is the area of the material.

In real devices, the heat flows through different layers in a switch. During the steady-state, the thermal model will be represented by a simple resistive network, but in reality, each material has it own specific heat capacity which is capable of storing some heat and every layer has its own time constant. This can be represented by a simple RC network as shown in figure 3.3. The storage capacity of the material can be determined by

$$C_{th} = C_s m \tag{3.9}$$

where C_s is the specific heat capacity of the material and m is the mass of the material.

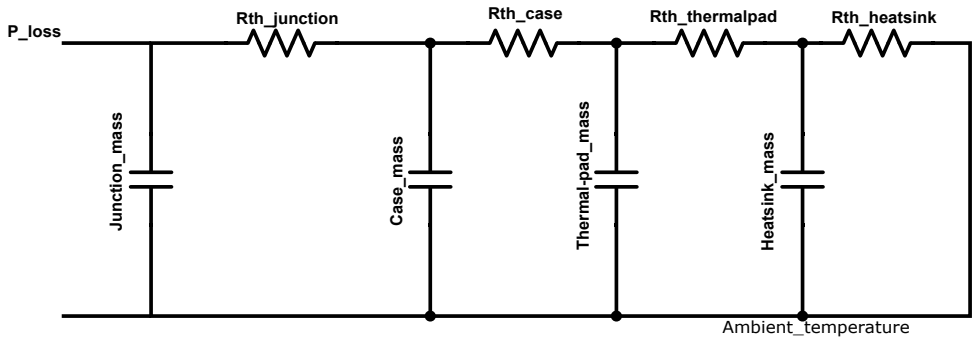


Figure 3.3: Lumped thermal model of a Mosfet switch

In a totem pole arrangement, there are four MOSFET switches and the temperature of these four switches needs to be in safe limits to protect the system from failure as well as maintain the efficiency of the circuit. To achieve this the thermal behavior of the switch needs to be analyzed to implement an efficient temperature control. For simplicity, a thermal model for two upper switches on both legs; 1 silicon and gallium nitride switch are developed. Figure 3.4 shows the thermal model of the MOSFET switches. The junction to case resistance is taken from the datasheet and the junction mass is determined by calculating the volume and multiplying it with junction material (GaN/Si). The thermal pad resistance is calculated as explained above. A heat sink for each pair of MOSFET is assumed. The two MOSFET are connected in parallel to the heat sink mount as shown in figure 3.4.

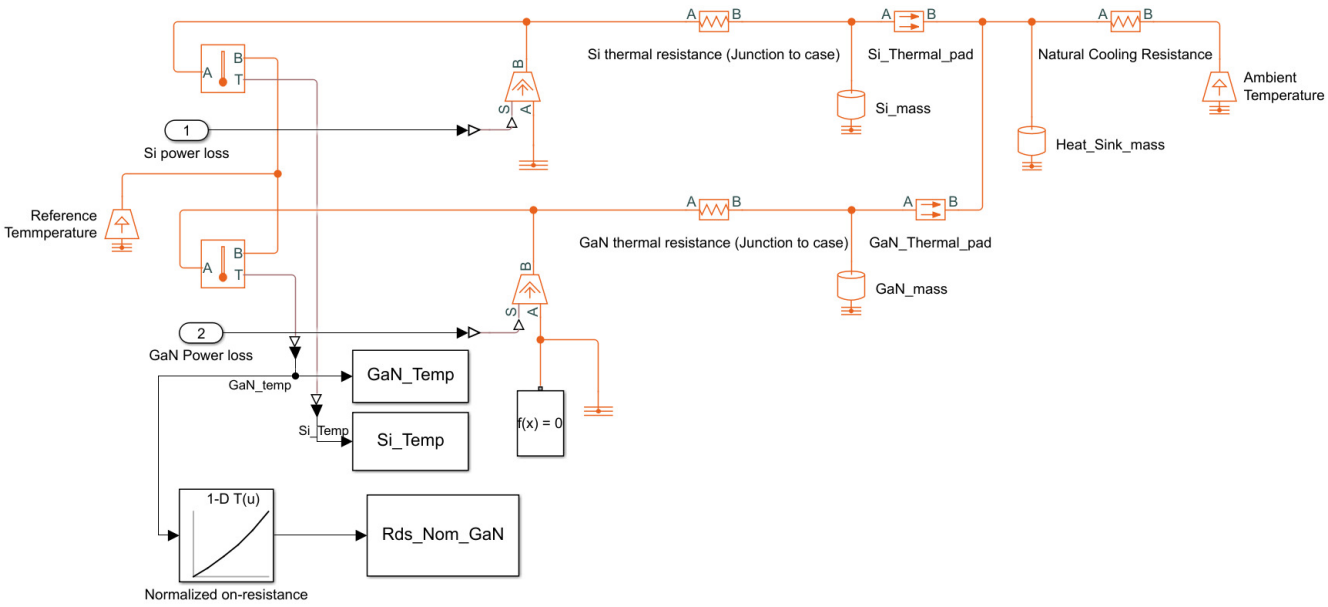


Figure 3.4: Lumped thermal model of GaN and Si Mosfet switch

A normalized on-resistance plot data from the data-sheet is entered in a lookup table so that it can determine the change in resistance with temperature. The power losses from the MOSFET switches are injected into the thermal model and the junction temperature can be estimated by placing a temperature sensor. The temperature can also be estimated analytically as explained in section 3.3

4

Results & discussion

4.1 Open loop characteristics

As explained in section 2.3.3 the output capacitor on the DC side charges and discharges according to the switching pattern. This enables to have a DC voltage and current with some ripple. Figures below shows the open-loop output voltage and current waveforms for the silicon carbide and gallium nitride MOSFET switches.

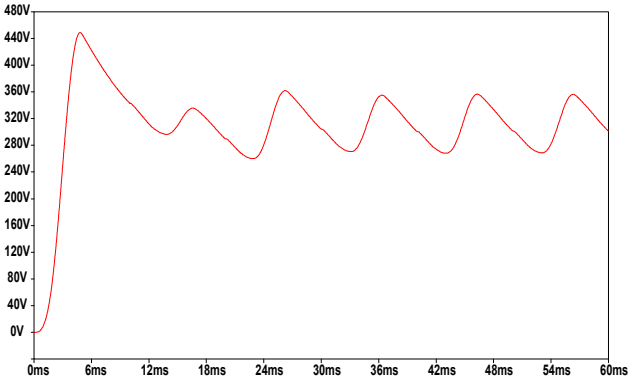


Figure 4.1: Open loop voltage waveform

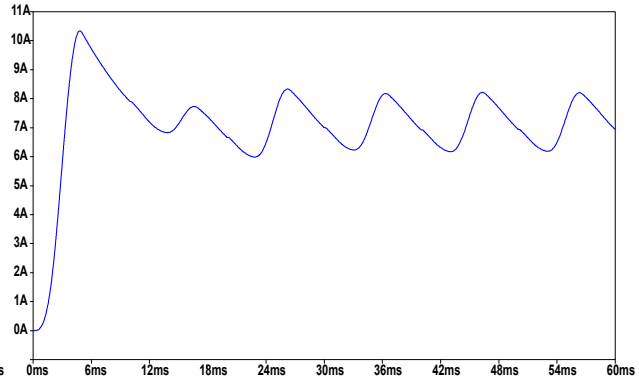


Figure 4.2: Open loop current waveform

Since the boost inductor and the DC side capacitors are the same for both the switches there will not be any distinct difference in the open-loop current and voltage waveforms. Both the switches are capable of providing 362 V maximum with a ripple of 84 V. Likewise the current can reach up to a maximum of 8.7 A maximum with a ripple of 2.5 A. As this is an open-loop setup the ripple in the output waveforms are large, since there are no feedback to monitor the output voltage and thereby adjusting the duty cycle.

4.2 SiC switching characteristics

The switching characteristics determine the turn on and turn off patterns of the switch. If the current through the switch is high then it denotes that the switch is conducting, otherwise, it is blocking or turned off. Figure 4.3 and 4.4 show the turn-off and turn on characteristics of the silicon carbide MOSFET switch. It can be seen from figure 4.3 that the time required to turn off the switch is 60 ns and the turn off losses are estimated by calculating the energy consumed by the switch within the time period by integration and the power loss is calculated by the multiplying with

total time period as explained in section 2.6.4. The turn off losses is found to be 15 W. Similarly the total turn-on time of the switch is 60 ns and the turn off losses are found to be 19 W. The conduction losses in the switch are found to be 63 W.

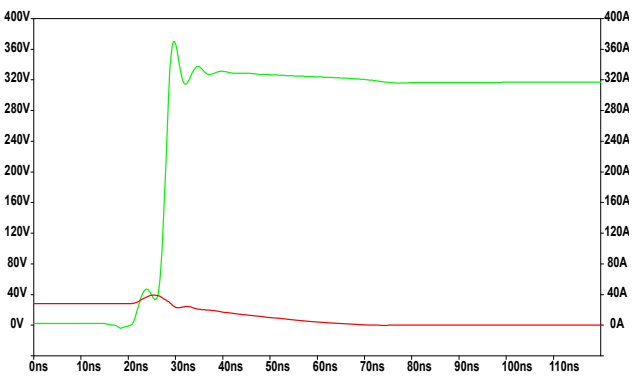


Figure 4.3: SiC turn off switching characteristics; Drain-source voltage (Green),Drain current (Red)

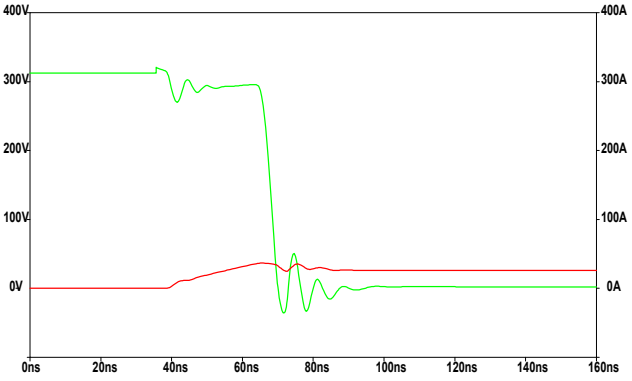


Figure 4.4: SiC turn on switching characteristic; Drain-source voltage (Green),Drain current (Red)

4.3 GaN switching characteristics

Figure 4.5 and 4.6 represent the turn on and turn off switching of the gallium nitride switch. It can be seen from the figure that the turn off time of the switch is 45 ns and turn-on time is 48 ns. The fast switching is due to the low gate-source and gate-drain capacitance of the MOSFET switch which makes the switching instantaneously. The turn-off and turn on losses are found to be 10.9 W and 11 W. The conduction losses are found to be 14 W

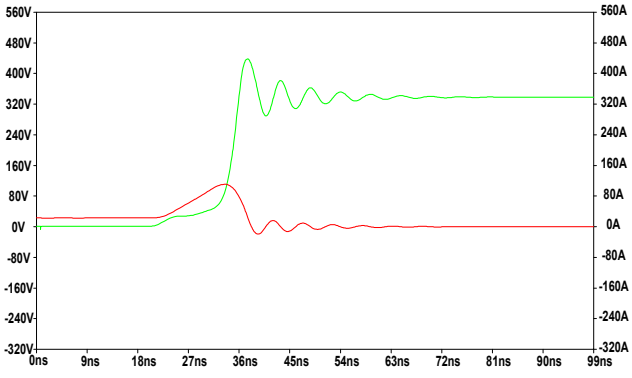


Figure 4.5: GaN turn off switching characteristics; Drain-source voltage (Green),Drain current (Red)

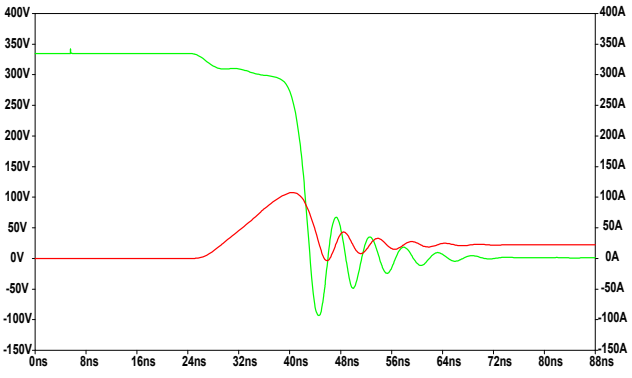


Figure 4.6: GaN turn on switching characteristic; Drain-source voltage (Green),Drain current (Red)

4.4 Comparison of SiC and GaN

As mentioned in sections 4.2 and 4.3 it can be seen that that gallium nitride switches have faster turn on and turn off time which makes gallium nitride more suitable for

operating at higher switching speeds also this makes it optimal to operate at higher frequencies with lower losses.

Table 4.1: SiC Vs GaN Loss comparison

Loss type	Silicon Carbide Power Loss (W)	Gallium Nitride Power Loss (W)
Turn On Losses	19	11
Turn Off Losses	15.2	10.9
Conduction Losses	63	13.3

It can be seen from the values presented in table 4.1 that the losses in the gallium nitride switch is much lower compared with the silicon carbide. Hence the gallium nitride is much preferred in areas where efficiency of the system is a major concern. Also from figures 4.3, 4.4, 4.5, 4.6 the over-currents during turn on and turn off can be seen to be much more prominent in GaN switches. This over-current is caused due to the transfer of energy from the boost inductor on the AC side when it is fully energized. Hence the gallium nitride switches cannot be operated without extra protection circuits such as snubber circuits to suppress the over-currents and over-voltages to prevent the switch from damage.

4.5 PWM control in a closed loop

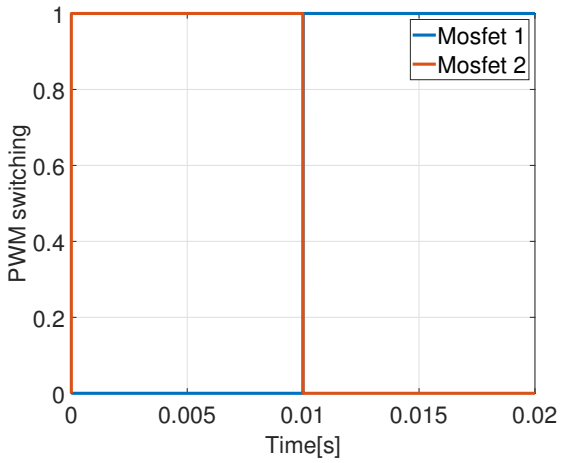


Figure 4.7: PWM control of Mosfet leg Switches

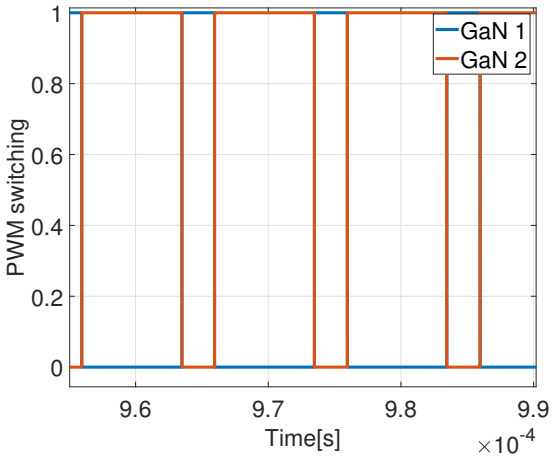


Figure 4.8: PWM switching of GaN switches in a zoomed view

The PWM logic is implemented as stated in section 3.1.5 and the results are verified here. Figure 4.7 reveals the functioning of PWM switching of MOSFET leg switches for one cycle period and figure 4.8, shows the PWM switching of GaN switches in a zoomed view. We can see from both figures that the switches are acting complementary to each other. It could be seen from figure 4.7 that, MOSFET 1 is 0 and MOSFET 2 is high, as the condition is $V_{AC}(t) > 0$. As discussed in section 3.1.5.1, we can notice that the MOSFET legs are acting based on the assigned states by

checking the polarity change, and ensuring that DC voltage is the same irrespective of any change in polarity. We can also see from figure 4.7, that MOSFET 1 is conducting completely during the positive cycle and MOSFET 2 is conducting completely during the negative half cycle.

Similarly it could be seen from figure 4.8, that GaN 1 and GaN 2 are acting in states, 1-$V_{gate}(t)$ and $V_{gate}(t)$ respectively. Thus GaN leg switches with the assigned states help in shaping the boost inductor current as stated in the section 3.1.5.2. We can also notice that GaN 1 switch acts as the boost switch shaping up the inductor current while the GaN 2 acts in a way of the imitating the diode (i.e) acting complementary to GaN 1. Through this, we can see that at least one MOSFET and one GaN is always turned ON at any instant for a given time period to generate a boost control of the output voltage.

4.6 Current control loop

To verify the controller design, simulations are performed with the closed loop current control system where the current controller is tuned with symmetrical optimum as discussed in section 2.5.2.1. The current controller is implemented initially as it is a quick controller, where the output of the voltage controller (current reference) is taken as a constant.

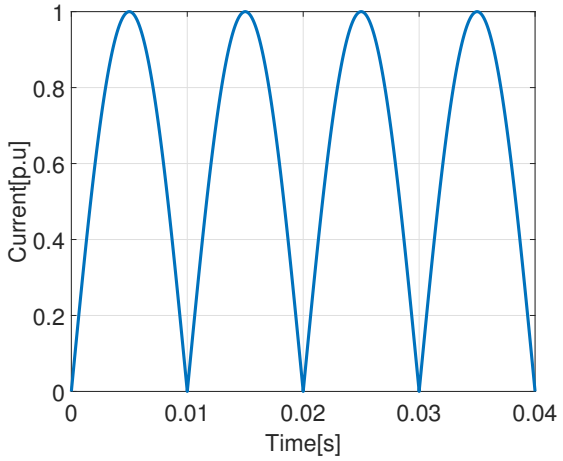


Figure 4.9: Reference current of the Current controller

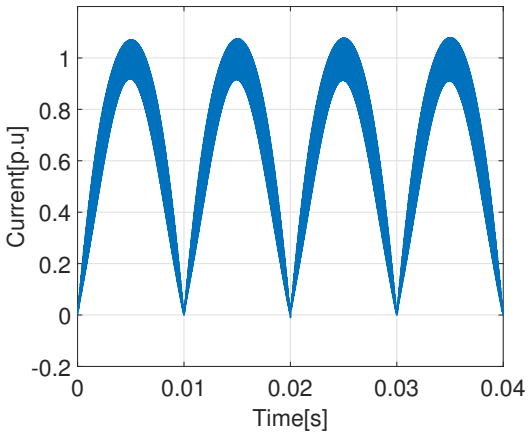


Figure 4.10: Measured current of the Current controller

The obtained results are shown in figures 4.9, 4.10, 4.11 and 4.12 where the reference current is the current generated from the arithmetic reference and the measured current is the current measured from the inductor. The error is the result generated from the difference between reference current and measured current. The error is fed to the PI controller where the PI controller tries to compensate for the error and generate the most optimal output which is required to operate the PWM switches. The output of the PI controller is the duty cycle generated which is in the range from 0 to 0.9.

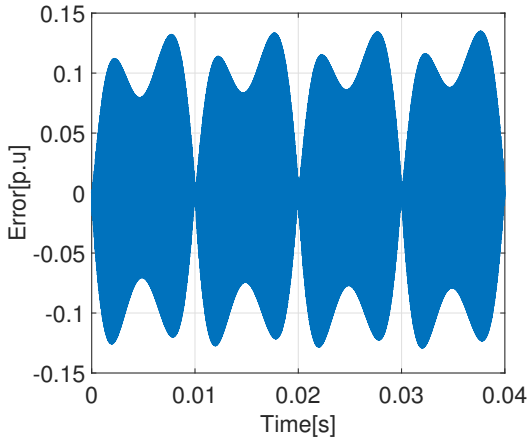


Figure 4.11: Current controller error

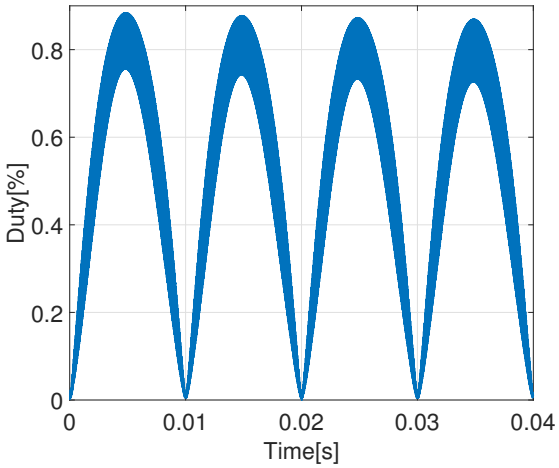


Figure 4.12: Duty cycle generated

It can be seen from figures 4.9 and 4.10 that the inductor current which is then measured current follows the reference current equally where both the currents are sinusoidal. It is also noted from figure 4.11, that the error produced from the reference and measured current is governed by the switching frequency ripple. However, we can see from 4.11, that there is a minimum error ripple. This may be due to a small delay in the PWM switching and the time constant calculated in the current measurement filter. This may be reduced by controlling the phase of the current where a separate loop can be designed featuring the control of the phases. Since there seems to be a good response of the controller for the symmetrical optimum itself, a separate loop controlling the phases is not implemented here. Additionally, we can see also ensure from figure 4.12, that the duty cycle generated is positive and does not go to negative.

4.7 Voltage Control loop

As it is known for complete control design, a current control alone is not sufficient. It is necessary to control the output voltage as well. Hence as discussed in section 2.5.2.4, a voltage control loop is also implemented and the results are obtained. The voltage control is implemented in two cases: one with the constant reference voltage and the other with an additional step to check the response of the controller for fluctuation in reference voltage. The simulations for both cases are discussed in the following subsections.

4.7.1 With Constant Reference

The simulation of the voltage controller for a constant reference voltage is shown in figures 4.13, 4.14 and 4.15. It can be seen from figure 4.13, the measured voltage is the output from the low pass filter which tries to follow up the reference voltage. The reference is given as a constant without any fluctuations in the voltage. The difference in reference and measured voltage is the voltage control error which is the input to the PI voltage controller. The voltage control error as shown in figure

4.14, is stable as the measured voltage except at the initial stage. This may be because the capacitor is in it's fully charged state initially and tries to discharge when there is a current. The error of the voltage controller is given as an input to the PI controller where the controller tries to compensate for the error and produce a stable output as shown in figure 4.15. The output of voltage PI controller is $i_{control}$ acts as a stable input to the arithmetic of the current controller. It is the control signal to the current loop, on which the current control acts.

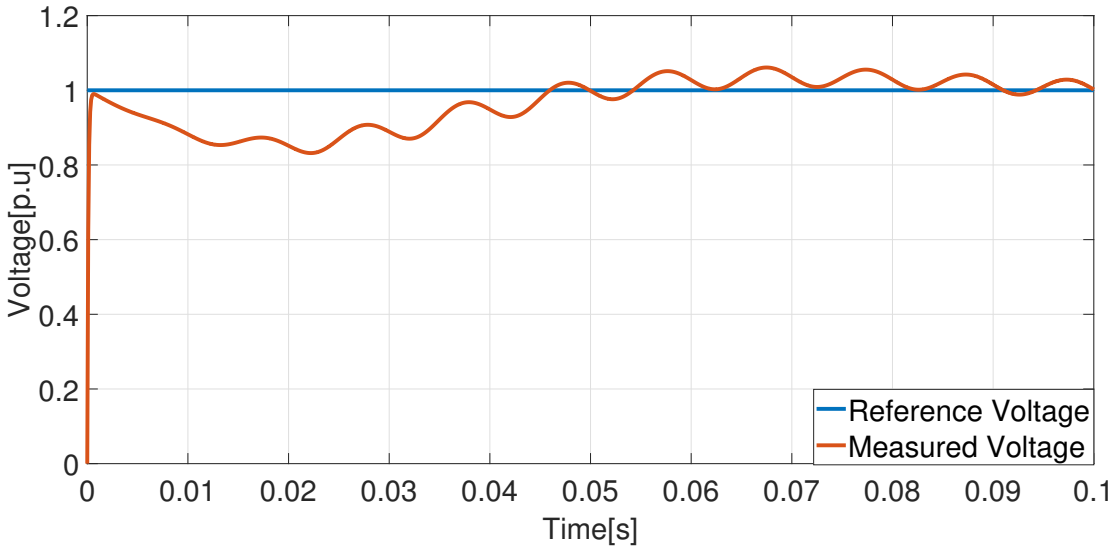


Figure 4.13: Reference and Measured voltage with constant reference

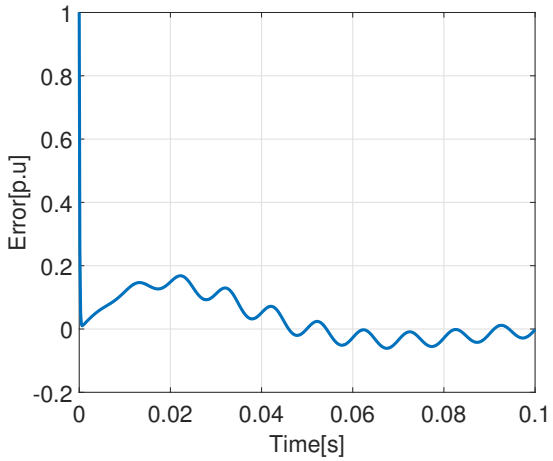


Figure 4.14: Voltage controller error

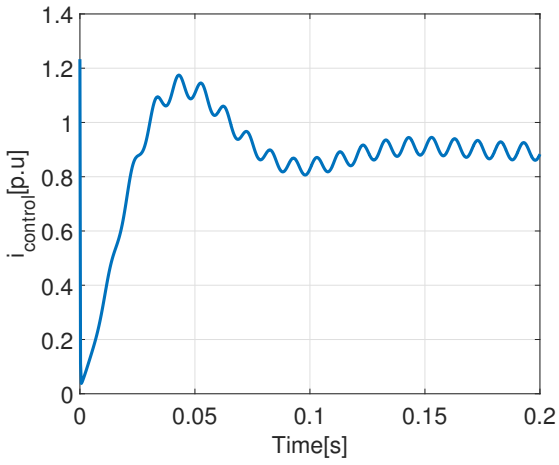


Figure 4.15: Output of PI voltage controller

4.7.2 With an additional step

The simulation for a 5% increase in a DC voltage is given in the form of a step and the waveform is illustrated as shown in figures 4.16, 4.17 and 4.18 . The measured

voltage is the per-unit output from the low pass filter of the measure DC output voltage. It can be seen from figure 4.16 that an additional step is added at 0.1 secs, where the measured voltage tries to follow the reference voltage. It can be seen from the simulation that, the voltage can stabilize even when the step is added and it is following the reference of the step voltage. Similarly, it could be seen from figure 4.17, that the voltage control error is decreased after a step is added. The PI controller compensates for the error, initially decreasing it and later on making it more stable. The response of the controller could be slower because it makes the AC voltage amplitude not to be larger than the DC voltage amplitude. Otherwise, it would affect the boost operation until the AC voltage drops below.

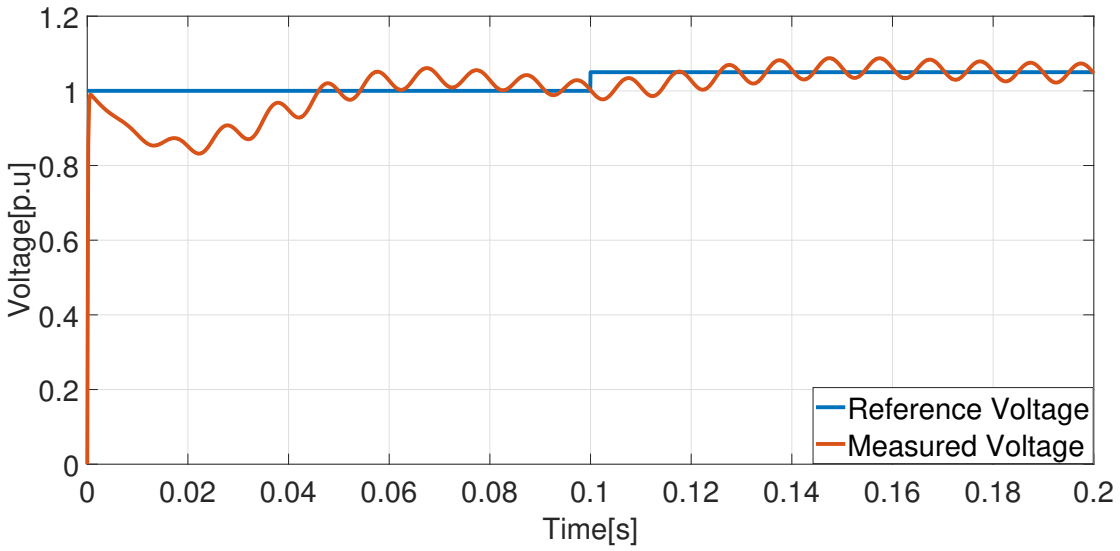


Figure 4.16: Reference and Measured voltage with a step reference

The output from the controller is $i_{control}$, where it can be seen from figure 4.18 that the controller produces a stable output after an step at 0.1 secs. The response of the controller to make $i_{control}$ more stable could also be easily achieved with the apt low pass filter value. Meanwhile, for a quicker response, a high order low pass filter or a band-pass filter can be used. These filters give out more precise filtering of ripple frequency while passing through high frequency and thus giving a quicker feedback loop. Another way of filtering is by having a voltage measurement filter where the ripple is calculated based on average voltage and current and subtracted from the measured signal. Here a simple low pass filter is enabled for a precise control of the ripple frequency and making the system more stable.

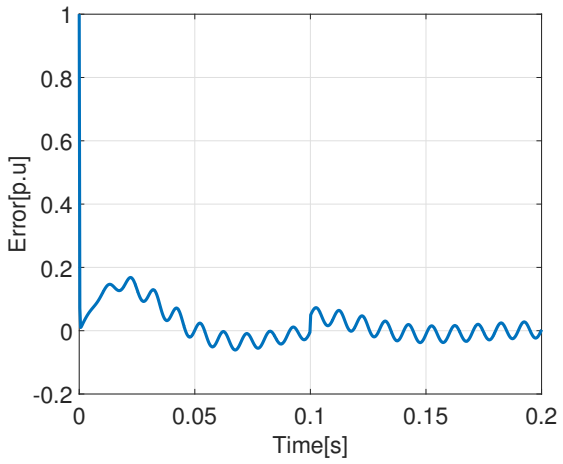


Figure 4.17: Voltage controller error for a step reference

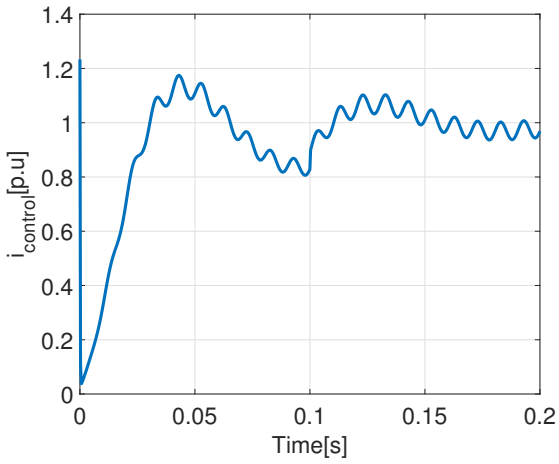


Figure 4.18: Output of PI voltage controller for a step reference

4.8 Complete Closed loop Simulation Results

For the verification of a complete PFC converter, simulations are done at system level keeping the rated values in mind. It is necessary to check the functionality of the closed-loop involving voltage and current control. The simulations are carried out based on a closed-loop and the waveform involving the entire closed-loop is shown here. As can be seen from figure 4.19, the input voltage and current are in phase with each other. The power factor correction of the circuit is found out and verified in section 4.10 further. The red waveform shows the inductor current and the blue waveform shows the input voltage. The passive rectifier bridge rectifies the voltage to the waveform of the absolute value of sine, and the current is scaled by the voltage over the inductor. This current waveform is then shaped like a sine wave by controlling the duty cycle of the switches implemented in the current control. With the AC main current shaped like sine, there are harmonics and ripples in the AC supply current. However, these harmonics are limited to the switching frequency ripple which are compensated by low pass filter used in the current controller. Hence as discussed in the section 3.2.1, the current controller is responsible for enabling the input inductor current follow the input sine voltage wave.

It can also be seen from figures 4.20 and 4.21, that the DC voltage and current can be operated at a rated value range over the whole main period without having a huge DC link capacitor on the output of the rectifier bridge [8]. The output voltage and current are stated when the capacitor is in the fully charged state where it can be seen that it tries to get more stable after an initial oscillation along with the rated output values. We can notice that the DC voltage is around 400 V and the output current is around 8.5 A which is found to be as the rated output values of the charger. It can also be seen that it took around 0.1 secs to reach the steady-state value at the output. The higher input current impacts the overshoot which can be reduced with a higher value capacitor. Meanwhile, we can also verify from figure 4.22 that the rated output power is 3300 W, which is also the rated power value of the charger.

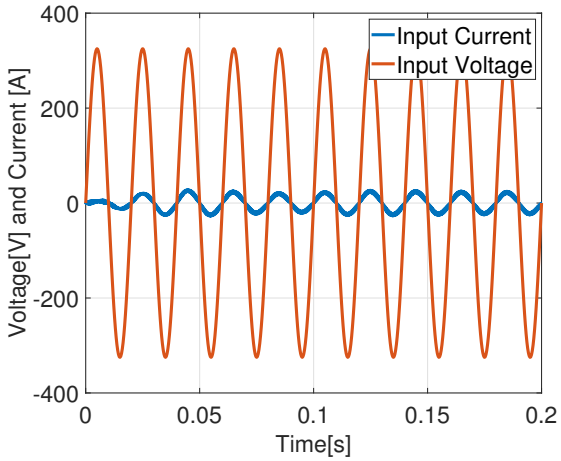


Figure 4.19: Behaviour of input voltage and input current

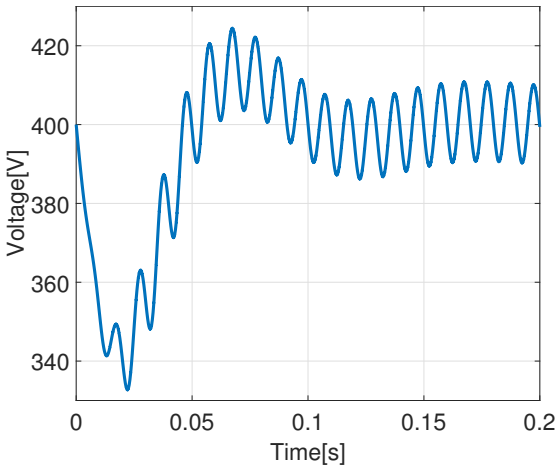


Figure 4.20: Output voltage of a PFC

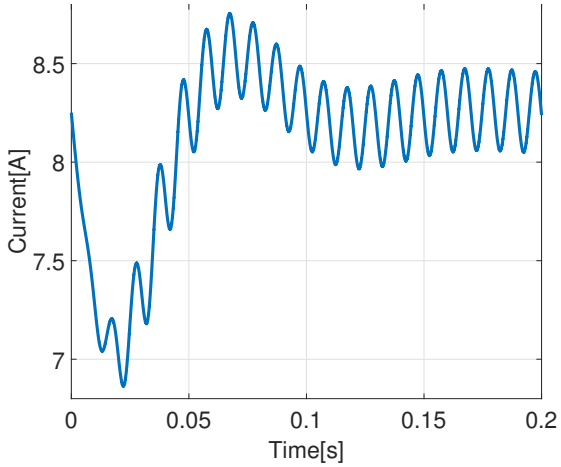


Figure 4.21: Output Current of a PFC

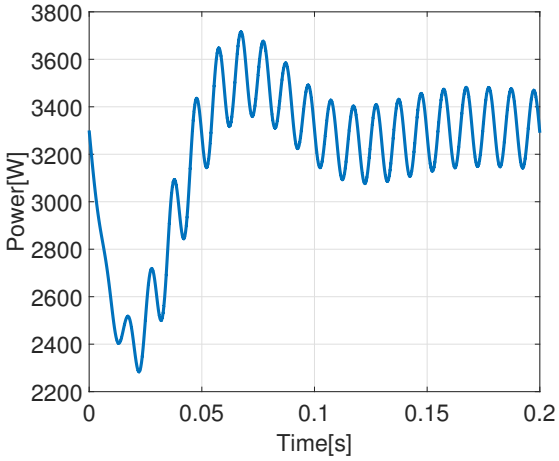


Figure 4.22: Output Power of a PFC

4.9 Temperature analysis of SiC and GaN switches

As explained in section 3.4 a lumped thermal model is implemented. To have a fair comparison, even though there is a difference in on-state resistance of the two switches table 3.3 they are made equal to have similar conductive losses of the MOSFET. However, the other parameters such as the capacitance, normalized on-state resistance will remain different. Initially, the junction temperature is estimated by injecting the power from the Simulink MOSFET model and the ambient temperature is considered to be 80°C. For better analysis and viewing of plots, the injected power is average power since the actual power creates a temperature transient in the thermal model. Even with the transient, it is ensured that the temperature does not exceed the limits. The junction temperature of the silicon carbide and gallium nitride switch, considering that on-state resistance remains constant with change in temperature is shown in figure [4.23,4.24].

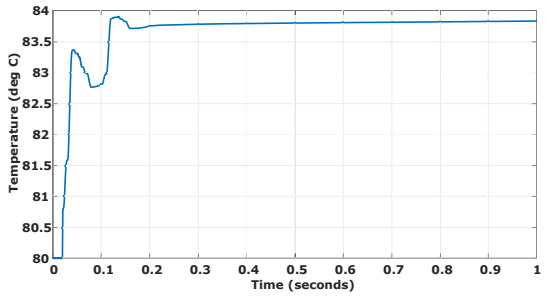


Figure 4.23: Thermal behaviour of GaN switch without temperature feedback

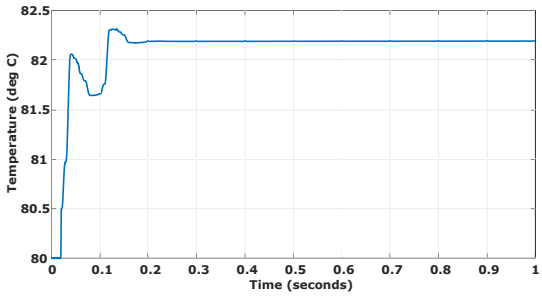


Figure 4.24: Thermal behaviour of SiC switch without temperature feedback

It can be seen from figure [4.23,4.24] that the thermal response of the silicon carbide switch is much better than that of the gallium nitride switch. The temperature reaches a steady state at around 82.25 °C for the silicon carbide switch whereas it reaches a steady-state around 83.75 °C for the gallium nitride switch. This is due to the poor thermal conductivity of the GaN switch and also due to higher junction to case thermal resistance.

As this analysis considers that the on-state resistance remains constant with varying temperature, the power losses in the MOSFET is low. But in reality, the power losses will be much higher if the temperature is taken into effect. Hence, power losses in the MOSFET are calculated analytically as explained in section 2.8, considering the temperature change due to losses. Hence the temperature from the previous analysis is taken to calculate the change in the on-state resistance. This data is available in the components datasheet [17, 18]. The junction temperature of the silicon carbide and gallium nitride switch with temperature feedback is shown in figure [4.25,4.26]. It can be seen in both figures that there is an increase in temperature due to the increase in average power. Even though the power loss in the MOSFET has increased, the silicon carbide MOSFET switch has better thermal performance than the Gallium nitride. Hence a better cooling system has to be designed for the gallium nitride switch to prevent any damage to the component and also to maintain

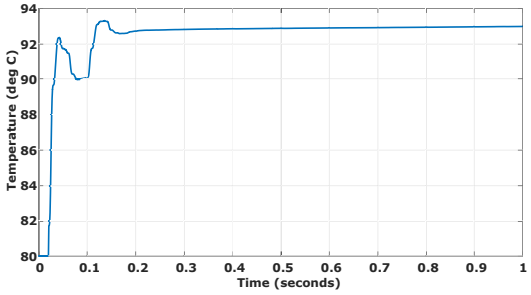


Figure 4.25: Thermal behaviour of GaN switch with temperature feedback

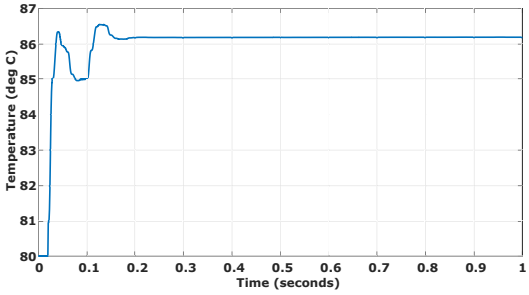


Figure 4.26: Thermal behaviour of SiC switch with temperature feedback

the efficiency of the system.

4.10 Power Factor Correction of the circuit

The quality of power in the AC line can be quantified using the power factor (PF) and total harmonic distortion(THD). The current harmonics can be reduced by providing power factor correction circuits in the converters [37]. Hence, to obtain the highest power quality in the converter, it is essential to enumerate THD and PF of the converter. The Total Harmonic Distribution (THD) of the AC component is evaluated in Simulink which is found to be,

$$THD = 0.11 \tag{4.1}$$

The phase angle of the fundamental AC current component is found in simulink as well. It is computed to be as,

$$\phi = 3.14° \tag{4.2}$$

where the equation for the power factor evaluation is taken from reference [8]. It is calculated as,

$$PF = \frac{1}{\sqrt{(1 + THD^2)}} \cdot cos(\phi) = 0.992 \tag{4.3}$$

4.11 Volume and Weight Estimation

Several components are used for the design of a totem pole PFC circuit in an offboard charger. Larger weighing components will have a huge impact on packaging and production. Also, since this will be an off-board charger, the weight of the unit should be kept as low as possible for commercial benefits. It is always essential to reduce the size of large components such as the boost inductor, output capacitor, and switching components. The volume of these components is dimension based upon their geometrical figure. The main components which are used for the design of a PFC circuit in an offboard charger along with their volume and weight consumed are tabulated in table 4.2. The weight and volume of the components used are taken

based on data from datasheets of the components [16, 17, 18, 19, 20, 24]. They are not weighed actually for the purpose and based on the value of the components, the closest data of weight and volume are assumed from datasheets. The components are chosen based on the assumption that the inductor and capacitor are designed in a cylindrical shape, the two switches and the current sensor are designed in a rectangular shape. The controller is neglected while considering the weight and volume as for the simulation purpose PI controllers are used.

Table 4.2: Volume and Weight Analysis of main components in an offboard charger

Component	**Values**	**Dimension[cm]**	**Volume[cm^3]**	**Weight[g]**
Inductor	152 μH	1.21 x 1.4	6.44	18.23
Si Mosfet switches	650V/130A	1.53 x 1.97 x 0.47	2 x 1.417 = 2.83	2 x 38 = 76
GaN switches	650V/36A	2.085 x 1.59 x 0.5	2 x 1.657 = 3.314	2 x 9.5 = 19
Output Capacitor	150 μF	1.5 x 2.5	4 x 17.67 = 70.68	68
Current Sensor	30 A	3.1 x 1.6 x 2.6	12.9	60.3
Total			95.664	241.53

Thus it could be seen from table 4.2 that, the total weight of the main components used in PFC circuit is around 241 grams and has a volume of around 43 cm^3. However, in real-time additional components such as a DSP controller, an auxiliary power supply, two heat sinks, NTC thermistor, and RCD relays are considered as well. The weight and volume of the PFC circuit would increase accordingly in real-time when these components are added. This is discussed in table 4.3,

Table 4.3: Practical Volume and Weight Analysis

Component	**Values**	**Dimension[cm]**	**Volume[cm^3]**	**Weight[g]**
Auxiliary Power supply	12 V	6.4 x 4.5 x 2.5	72 x 2 = 144	2 x 125 = 250
DSP controller	3.3 V	0.12 x 1.5 x 1.5	0.27	0.72
Heat Sink	TO-247	5.8 x 3.2 x 4.38	2 x 81.3 = 162.6	2 x 71 = 142
NTC thermistor	4.7K to 100K	0.425 x 1.68	2 x 0.95 = 1.9	2 x 1.0 = 2.0
RCD relay			380	209
Total			688.7	603.72

The data of the components are taken from their respective datasheets which is mentioned in reference [22],[23] and from [34] to [36]. Hence in real-time with the inclusion of these components the weight of the PFC circuit in the charger would be around 845 grams and volume would be around 784 cm^3. It is to be noted that this is an approximate estimation of weight and volume and there will be differences in the final product. Since the EMI circuits and other measuring op-amp circuits are not considered, an increase in the volume and weight is expected.

4.12 Life Cycle Cost Anlaysis

As discussed in section 2.9, the life cycle cost analysis of both the SiC and GaN switches are compared here. The characteristics of both the switches differ very much and so do their costs. It is always essential to analyze the life cycle cost while comparing the economic performance of the product rather than just comparing the market prices of the product. Here the life cycle cost of both SiC and GaN switches is analyzed for 15 years since the life expectancy of the switches is also 15 years. It is shown in figure 4.27,

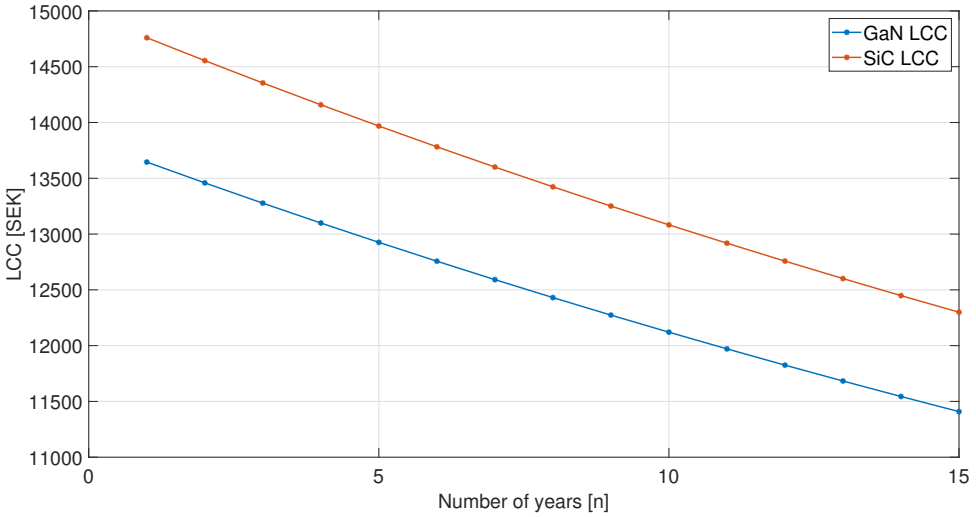


Figure 4.27: LCCA of SiC and GaN

The initial costs of the GaN switch are lower compared to the SiC switch. The cost of each switch is calculated for every year and plotted accordingly. It could be seen from figure 4.27, that the LCC during the first year for the GaN switch is around 13650 SEK which includes the initial cost, operation cost, maintenance cost and also taking into account the change in rates (2.5 in percentage). It could also be seen from figure 4.27 that during the fifteenth year the LCC is around 11410 SEK. Similarly from figure 4.27 the LCC of the SiC switch during the first year is 14760 SEK and during the fifteenth year is 12300 SEK. The initial costs that include the cost of the switch, capacitor, inductor, DSP main controller and the components mentioned in table 4.2,4.3. It is noted that the GaN switch is much cheaper compared with the SiC switch. It is also noted that the power losses in the GaN switch are less compared with the SiC switch. The operation and maintenance cost of the product is considered to be constant as the product has to be disposed of in case of any fault or damage. As all the costs involved in the LCC analysis are constant except for the cost of GaN switch and energy cost, the initial LCC of GaN switch lower compared with the SiC switch due to the above-mentioned reasons. A rate of discount of 2.5 %, as mentioned in section 2.9 is considered to calculate the energy cost, thus the energy cost tends to reduce with time. Due to this, the LCC of the switches reduces with time. Thus it is concluded that the GaN switch

is less expensive compared to the SiC switch and also the GaN switch is much more profitable in the long run. Hence it seems to be an ideal switch to be used for this application.

4.13 Efficiency

The efficiency of the totem pole PFC is shown in figure 4.28. The efficiency is plotted from 50% of the power i.e. from the half to full power. It could be seen from figure 4.28, that the efficiency increases linearly when the output is increased. It could be noticed that at 50% power output the efficiency is around 85.5% and during 100% power output the efficiency is around 98.72%. In reality, the efficiency does not drop linearly as shown in figure 4.28. This may be due to soft switching which is not implemented in this circuit. Also, it does not have an input AC rectifier bridge, the accuracy of AC voltage crossover detection directly impacts the current waveform and THD. Tens of detection micro seconds error could result in shorting the AC line and a high current distortion at the crossover area [15]. It could be improved by an additional dead time circuit which enhances low THD. However, this dead time circuit is not implemented in this circuit which could be the other main reason for impacting the efficiency.

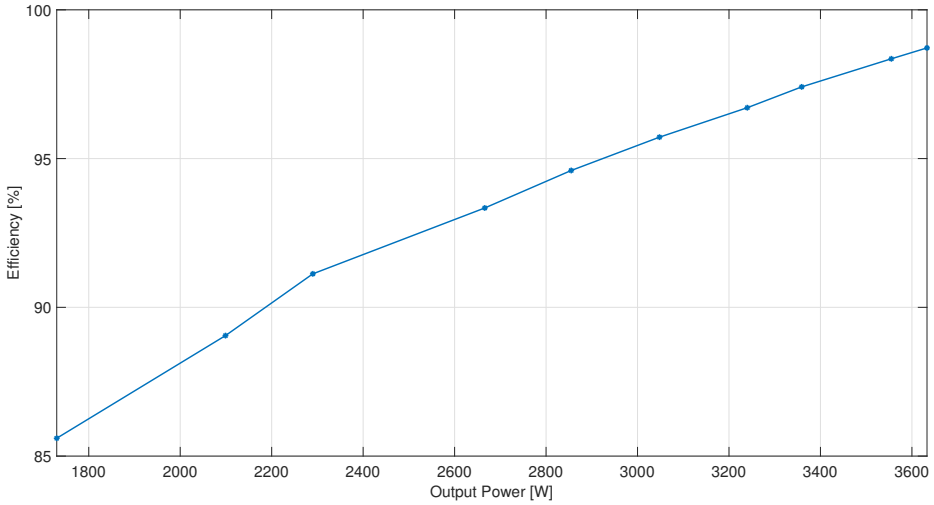


Figure 4.28: Efficiency of a totem PFC circuit

Figure 4.29 shows the power loss split-up of the main components in the PFC circuit. It can be seen that as the output power decreases losses in the component reduces due to reduction in current in the circuit but on the other hand from figure 4.28 it can also be seen that the efficiency of the charger reduces as the power decreases.

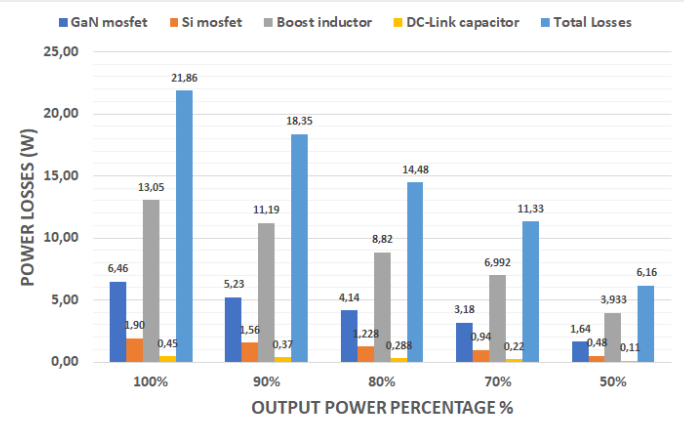


Figure 4.29: Losses split up of main components in the PFC circuit

5

Safety and Sustainability

5.1 Safety

Nowadays power electronics are entering more and more in technology which normally belongs to different engineering sectors. Electric Vehicle charger is one of those [27]. During recent times, the growth of EV's popularity and several charging methods has made it possible to charge a vehicle at home. Depending on the circumstances it is always worth invest to have a dedicated wall-mounted charger at home [14]. However, it is necessary to keep in mind certain precautions when using the charging cable for an EV from a wall-mounted plug as it draws high current (around 22 A). It is necessary to talk about a charging cable as people prefer it more than obtaining a wall-mounted box in case it is expensive to invest in. Any application with high current requires safety precautions while implementing practically. Hence for this application also precautions are considered for its implementation which would be discussed further here.

It proves to be more convenient for people to use home charging as many people in Sweden tend to switch to EV recently. When it comes to portable charging, the customers directly connect the charging cable to the wall socket which could cause cable fires or any fluctuations in the cable. The charging cable must be able to withstand a higher rating for a longer time. If that is not the case then the possibility of a failure in the cable is very high. This can be prevented by following the Original Equipment Manufacturing (OEM) standards of the cables. Through these standards, the components inside the cable do not exceed the required ratings and hence can be optimized for the design of the cable. The cables can also be insured for the damages caused by insurance given by the company. The customers can claim their failures easily through insurance [14].

The PFC board inside the charger must be tested in adequate test conditions with consideration of all the aspects. The board should be designed with the accurate specification needed for the charger as the components in the board should be able to withstand higher ratings and higher temperature. When the charger is used, it should also be ensured that it does not have any impact environmentally and externally.

Another important aspect to consider is when there is a sudden fault in the system due to higher current, the system needs to stop instantly ensuring the detection

of occurrence of a fault. This could be managed by having a Residual Current Device (RCD) on the system which can break the current instantly to avoid faults from leading to serious conditions. RCD also ensures complete protection against all kind of leakage current and strong resistance against unwanted tripping [28].

5.2 Sustainability

As stated already for any EV, charging is highly important. To have sustainability in charging, the power system should facilitate multiple connections to the wall sockets at the same time. The power supply from the grid encourages a substantial increase in communication and control at the customer side of the electric power grid. It also introduces a high problem of overproduction yielding stability issues for the utilities. To overcome this and for a sustainable perspective, the implementation of the ”smart grid” is gradually growing in many industrial countries. The smart grid concept encourages more distributed renewable electricity production and increased consumption flexibility of the customer [8]. Hence loads can be charged at different times during the day and can be ensured the system is not under heavy load at the same time [14].

Similarly, for a sustainable perspective, it is essential to find resources other than coal and nuclear power in the future to achieve a high power availability for EV's. For this purpose, the bidirectional power supply could be used where the vehicles are operated as batteries to supply to the grid so-called vehicle to grid operation [14].

For more vulnerable solutions in the future, it could be possible to redesign the current AC to DC grid where the wall boxes provide DC supply. Through this, the conversion of AC to DC can be neglected. This can reduce conversion loss and thereby improving the sustainable nature of the system.

6
Conclusion

This master thesis illustrated the power control of an external charging system for an electric vehicle. Initially, the switching characteristics of the SiC and GaN switches were studied and it was found that the power loss of GaN is less compared to SiC. This was implemented through an open-loop control of a totem pole bridgeless PFC circuit. The totem pole bridgeless PFC was also compared with the conventional PFC circuit theoretically based on losses, components, and efficiency. Additionally, a fundamental simulation model for the closed-loop control of the totem pole bridgeless PFC was built in Simulink. The general equations for the current and voltage control were developed considering the dimensions of the main components in the circuit. The obtained results ensured that the output voltage is controlled to the rated 400V DC and that the input current is in phase with an input voltage as well as the rated output power of 3.3 kW is achieved with a power factor of 0.992. The efficiency of the PFC circuit is calculated and it is found out to be 98.72 % at full load.

Furthermore, a temperature analysis was also done in Simulink comparing SiC and GaN switches. To perform temperature analysis, a lumped thermal model was implemented initially for the MOSFET switches. It was found that the thermal response of SiC was much better compared to GaN due to the poor thermal conductivity of the gallium nitride. The volume and weight of the main components used in the PFC circuit were also estimated considering the effect of PFC circuit in an external charger. The volume of a GaN totem-pole PFC circuit is estimated to be 784.4 cm^3 and the weight of the circuit is estimated to be 845.3 g. Finally, LCCA of both the GaN and SiC was done for 15 years and it was found that the GaN switch is more economical to use than the SiC switch.

6.1 Future Works

From completing the power control of the PFC circuit, the initial future work will be to implement a bidirectional control of the PFC circuit for the vehicle to grid operation. The temperature control of the complete PFC circuit can be done in the future considering the effects of high current across the switches and high temperature in the PFC circuit. The PFC circuit also needs to be checked in a single fault condition to ensure whether it meets the safety standards such as IEC standards of the Electric Vehicle Charger. The single fault condition has to be checked by designing the Residual Current Device (RCD). The RCD will act accordingly when there is an occurrence of faults in the system ensuring complete protection of the

system.

Additionally, a microcontroller needs to be implemented in the system for controlling the voltage and current as the control logic here is implemented through a PI controller only. It was also found that the efficiency could need to reach the expected range from the above half load as the soft switching was not implemented in the circuit. Hence it is necessary to implement soft switching in the circuit which can be done as a future work of this project. Further investigation of reducing the size of the components in the whole charger is necessary as it is the most beneficial aspect of the charger. The thermal analysis is done considering each switch only (one GaN and one MOSFET). It is necessary to perform thermal analysis of the complete system with a high accuracy software such as COMSOL for better results. The cooling system will also play a major role in the thermal analysis which is not implemented here and maybe an important task to consider for the future of this project.

Final future work will be to implement a prototype of the project so that it can be tested with several external conditions. It is also necessary to analyze the duration of the charging time of this charger where the battery model has to be implemented separately.

Bibliography

[1] C. Dericioglu, E. Yirik, E. Una, M.U. Cuma, B. Onur, M. Tumay *Review of Charging technologies for commercial electrical vehicles* [Online]. Available: http://www.makalesistemi.com/panel/files/manuscript_files_publish/aa0cfcd5888ff2211e8791d25e8cffef/60ab0b64358d17ad684c91b37acf666b/6bf488fe100cf16.pdf

[2] B. Fincan, M. Yilmaz, A. Goynusen, and K. Erenay *Design and Optimization of a High Power Density and Efficiency Boost PFC* [Online]. Available: http://dergipark.gov.tr/download/article-file/334573

[3] Jin-kwei Lee, Yung-Chung Chang, Chia-chin Chuang *Conversion Circuit Design for High Efficiency Bridgeless Interleaved Power Factor Correction* [Online]. Available: http://article.sapub.org/10.5923.j.ijee.20130302.06.html

[4] Omer Turksoy, Unal Yilmaz, Ahmet Teke *Overview of Battery Charger Topologies in Plug-in Electric and Hybrid Electric Vehicles* [Online]. Available: https://www.researchgate.net/publication/286221468_Review_on_Electric_Vehicle_Battery_Charger_Charging_Station_and_Standards

[5] Dale Hall, Nic Lutsey *Emerging Best practices for Electric Vehicle Charging infrastructure* [Online]. Available: https://www.theicct.org/publications/emerging-best-practices-electric-vehicle-charging-infrastructure

[6] Vinaya Skanda, Anusheel Nahar *Interleaved Power Factor Correction (IPFC) Using the dsPIC® DSC* [Online]. Available: http://ww1.microchip.com/downloads/en/appnotes/01278a.pdf

[7] Salil Chellappan *A comparative analysis of topologies for a bridgeless-boost PFC circuit* [Online]. Available: http://www.ti.com/lit/an/slyt750/slyt750.pdf

[8] Sondre Westby Johannessen *Power Factor Correction for a Bi-directional On-board charger for Electric Vehicles and Plug-in Hybrid Vehicles* [Online]. Available: https://brage.bibsys.no/xmlui/bitstream/handle/11250/2508091/19635_FULLTEXT.pdf?sequence=1&isAllowed=y

[9] Laszlo Huber, Member, IEEE, Yungtaek Jang, Senior Member, IEEE, and Milan M. Jovanovic´, Fellow, IEEE *Performance Evaluation of Bridgeless PFC Boost Rectifiers* [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4483680

[10] Ned Mohan, Tore M. Undelan, William P. Robbins *Power Electronics - Converters, Applications, and Design* [Literature].

[11] Mike Zhu *1.5 kW Totem-pole PFC Using 650V USCi SiC Cascodes* [Online]. Available: http://unitedsic.com/wp-content/uploads/2017/06/Totem-Pole-PFC-v2-AppNote-2017-06-23.pdf

[12] João Paulo M. Figueiredo, Fernando L. Tofoli, Bruno Leonardo A. Silva *A Review of Single-Phase PFC Topologies Based on The Boost Converter*

[13] Mouser Electronic (2003)*Low core loss, High Current Toroid Inductors* [Online],Available: https://www.mouser.se/datasheet/2/54/200ll_series-776025.pdf

[14] Martin Alerman, Therese Stenberg *Compact AC/DC module for Electric Vehicle Charging* [Online],Available: http://publications.lib.chalmers.se/records/fulltext/255738/255738.pdf

[15] Serkan Dusmez and Zhong Ye *Designing a 1kW GaN PFC Stage with over 99Efficiency and 155W/in3 Power Density* [Online],Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8170551

[16] Mouser Electronic *High Temperature, High Current Toroid Inductors* [Online],Available: https://www.mouser.se/datasheet/2/54/200ht_series-776003.pdf

[17] Transphormusa *TP65H050WS* [Online],Available: https://www.transphormusa.com/en/document/datasheet-tp65h050ws-650v-gan-fet/

[18] Cree Wolfspeed *C2M0080120D* [Online],Available: http://www.farnell.com/datasheets/2047787.pdf?_ga=2.96896535.900282188.1562164754-210258859.1561962820&_gac=1.150795716.1562164754.Cj0KCQjwpPHoBRC3ARIsALfx-_LtLHCk104tEThIFued9n1zUMo2BAd8DXcMzG-p-KBo8zyONtvO42UaAmm4EALw_wc

[19] GaN systems *Gallium Nitride Power Transistors in the EV World* [Online],Available: https://gansystems.com/wp-content/uploads/2018/01/The-Benefits-of-Gallium-Nitride-Power-Transistors-Span-Multiple-Markets.pdf

[20] Mouser Electronic *B43501B9157M* [Online],Available: https://eu.mouser.com/ProductDetail/EPCOS-TDK/B43501B9157M?qs=sGAEpiMZZMsprRPEdcYqIvmyehJ%252BUxJF

[21] Emma Arfa Grunditz, *Design and Assessment of Battery Electric Vehicle Powertrain, with Respect to Performance, Energy Consumption and Electric Motor Thermal Capability* [Online]. Available: http://publications.lib.chalmers.se/records/fulltext/236616/236616.pdf

[22] Texas Electronics *TMS320F2833x, TMS320F2823x Digital Signal Controllers (DSCs)* [Online],Available: http://www.ti.com/lit/ds/symlink/tms320f28335.pdf

[23] Mouser Electronic *CRD-060DD17P-2: Auxiliary Power Supply evaluation board for C2M1000170J SiC MOSFET* [Online],Available: https://eu.mouser.com/pdfdocs/Wolfspeed_evaluation_board_for_c2m1000170j.pdf

[24] Mouser Electronic *CCT261631-30-06-02* [Online],Available: https://eu.mouser.com/ProductDetail/TDK/CCT261631-30-06-02?qs=sGAEpiMZZMt5HSdYdJgvyQhJf3FYbZmpw6bgTb7QP8YeAwxK%252BVlwRA%3D%3D

[25] Haibo Li, Liyan Qu, and Wei Qiao *Life-Cycle Cost Analysis for Wind Power Converters* [Online],Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8053439&tag=1

[26] GLORIA PUGLIA *Life cycle cost analysis on wind turbines* [Online],Available: http://publications.lib.chalmers.se/records/fulltext/179861/179861.pdf

[27] D. Aggeler, F. Canales, H. Zelaya - De La Parra, A. Coccia, N. Butcher, and O. Apeldoorn *Ultra-Fast DC-Charge Infrastructures for EV-Mobility and Future Smart Grids* [Online],Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5638899

[28] ABB *Residual current devices - RCDs Ultimate protection of people and equipment* [Online],Available: https://new.abb.com/low-voltage/products/system-pro-m/residual-current-devices

[29] *Electric Vehicles Drive a Sustainable Future* [Online],Available: https://www.chargepoint.com/about/sustainability/

[30] George Lakkas *MOSFET power losses and how they affect power-supply efficiency* [Online],Available: http://www.ti.com/lit/an/slyt664/slyt664.pdf

[31] *Gallium Nitride (GaN) versus Silicon Carbide (SiC) In The High Frequency (RF) and Power Switching Applications* [Online],Available: https://www.richardsonrfpd.com/docs/rfpd/Microsemi-A-Comparison-of-Gallium-Nitride-Versus-Silicon-Carbide.pdf

[32] *Where SiC outperforms GaN* [Online],Available: https://www.powerelectronictips.com/sic-outperforms-gan/

[33] *Gallium Nitride (GaN) Technology Overview* [Online],Available: https://epc-co.com/epc/Portals/0/epc/documents/publications/GaN

[34] Mouser Electronics,*C40-058-AE* [Online],Available: https://www.mouser.se/ProductDetail/Ohmite/C40-058-AE?qs=%2Fha2pyFaduiLEulab2ZIRYZGDpKaYQtFw%252B5QRzQ%2FxUAtzYICWVDibw%3D%3D

[35] Mouser Electronics,*NTCALUG02A103FL* [Online],Available: https://www.mouser.se/ProductDetail/Vishay-BC-Components/NTCALUG02A103FL?qs=%2Fha2pyFaduhffizA81Cq75v2t%2Fi%2FaLLGC43t5hp%252Blve5DcOPtc40Gg%3D%3D

[36] Legrand,*RCD relay* [Online],Available: https://www.legrand.com/ecatalogue/411504-rcd-dx-id-2p-230.html

[37] Kalkidan Amare Gobena,*Single-Phase Bidirectional Power Factor Correction Boost Converter:* [Online],Available: https://pdfs.semanticscholar.org/5397/61d92d4801ae469e0f1268b19c3935e96b18.pdf

A

Appendix 1

A.1 Matlab Scripts

A.1.1 Current Controller

% Initialization of parrameters
V_{ac}=230 V;
V_{acpeak}= sqrt(2)*V_{ac};
V_{dcmax}= 400 V;
V_{dc}= V_{dcmax};
I_{ac}= 16 A;
I_{acpeak}= sqrt(2)*I_{ac};
P_{ac}= V_{ac}*I_{ac};
f_{sw}= 100 kHz;
w_{sw}=2*pi*f_{sw};
f_{normal}= 50 Hz;
$K_{iripple}$= 0.2;
$K_{vripple}$= 0.2;
$I_{Lpeak2peak}$= $K_{iripple}$*I_{acpeak};
$V_{Cpeak2peak}$= 20 V;
% base values
V_{base}= V_{dc};
I_{base}=16*sqrt(2) A;
R_{base}=V_{base}/I_{base};
% Intitializing the components
L= 151.69μH;
C=1.313 mF;
% design of current controller
% base values
V_{base}= V_{dc};
I_{base}=16*sqrt(2);
R_{base}=V_{base}/I_{base};
% PU parameters
L_{pu}=L./R_{base};
% Time constants and gains
T_{pwm}= 1/(3*f_{sw});
f_{ci}= $10^($ − 0.8) ∗ f_{sw};

T_{fi}= 5.97e-7;
T_{sumi}= T_{fi}+T_{pwm};
% Functioning of symmetrical optimum
beta= 1/(2*pi*f_{ci}*T_{sumi})^2
T_{ii}=beta*T_{sumi}
K_{pi}= L_{pu}/(sqrt(beta)* T_{sumi})

A.1.2 Voltage Controller

V_{dc} = 400 V;
C=1.641 mF;
V_{base}= V_{dc};
I_{base}=16*sqrt(2) A;
R_{base}=V_{base}/I_{base};
C_{pu}= C/ R_{base};
f_{grid}=50 Hz;
$K_{vripple}$= 0.2;
T_{sumi}=4.2413 μs;
T_{fiv}=100μs;
T_{sumv}= T_{fiv}+2*T_{sumi};
f_{cv}=500 ;
beta$_v$=1/(2*pi*f_{cv}*T_{sumv})^2
K_{fiv}=1;
T_{iv}= beta$_v$*T_{sumv}
K_{pv}=C_{pu}/(K_{fiv}*sqrt(beta$_v$)*T_{sumv})

A.1.3 Current Controller with filter

V_{base}= V_{dc};
I_{base}=16*sqrt(2);
R_{base}=V_{base}/I_{base};
L_{pu}=L./R_{base};
f_{sw}= 100kHz;
f_{ci}= $10^{-0.8} * f_{sw}$;
% it should be less than half a decade than switching frequency
w_{ci}= 2*pi*f_{ci};
T_{fistep}= 1e-10;
T_{fimax}= 1e-3;
$T_{fivector}$= 0:T_{fistep}:T_{fimax};
$m_{aripple}$= zeros(1,length($T_{fivector}$));
for i= 1:length($T_{fivector}$)
$m_{aripple}$(i)=0.5*$K_{iripple}$*L_{pu}*w_{ci}/sqrt(1+($T_{fivector}$(i)*2*pi*f_{sw})^2);
end
closeall
figure
loglog($T_{fivector}$,$m_{aripple}$)

xlabel('$T_{filter}[s]'$)
$ylabel('D_{ripple}')$
$set(gca,'fontsize', 18)$

A.1.4 Voltage Controller with filter

f_{grid}=50 Hz;
V_{dc}=400 V;
C=1.641 mf;
V_{base}= V_{dc};
I_{base}=16*sqrt(2) A;
R_{base}=V_{base}/I_{base};
C_{pu}= C/ R_{base};
$V_{Cpeak2peak}$=20 V;
K_{vdc}=$V_{Cpeak2peak}$/V_{dc};
w_{cv}= 2*pi*500;
T_{fvstep}= 1e-8;
T_{fvmax}= 1e-2;
$T_{fvvector}$= 1e-6:T_{fvstep}:T_{fvmax};
$i_{currentripple}$= zeros(1,length($T_{fvvector}$));
for i= 1:length($T_{fvvector}$)
$i_{currentripple}$(i)=0.5*K_{vdc}*C_{pu}*w_{cv}/sqrt(1+($T_{fvvector}$(i)*2*pi*2*f_{grid})^2);
end
closeall
figure
loglog($T_{fvvector}$,$i_{currentripple}$)
xlabel('$T_{fiter,v}[s]'$)
$ylabel('i_{ripple}')$
$set(gca,'fontsize', 18)$

A.1.5 Life Cycle Cost Analysis for GaN and SiC

$E_{lossgan}$ = 39420
$c_{pricegan}$ = 0.199;
r = 0.025;
c_{intgan} = 610.18 + 123.7 + 239 + 141.5 + 10.76 + 595.98 + (3*173.73);
$c_{maingan}$ = 3750;
for n = 1:15
years (n) = n;
$c_{engtotgan}$ (n) = ($c_{pricegan}$*$E_{lossgan}$)/(1+r)^n;
LCC_{gan} (n)=$c_{maingan}$ + c_{intgan} + c_{enggan} (n);
end

$c_{engtotgan}$ =0;
for i = 1:15
$c_{engtotgan}$ = ($c_{pricegan}$ *$E_{lossgan}$)/(1+r)^i + $c_{engtotgan}$;
end
figure(1)
plot(years, LCC_{gan}, '-*' , 'LineWidth', 1.5) $E_{losssic}$=43362;
$c_{pricesic}$=0.199;
r=0.025;
c_{intsic}=959.32+123.7+239+141.5+10.76+595.98+(3*173.73);
$c_{mainsic}$=3750;
for n= 1:15
years (n) = n;
c_{engsic} (n) = ($c_{pricesic}$ * $E_{losssic}$)/ (1+r)^n;
LCC_{sic} (n)= $c_{mainsic}$+c_{intsic}+c_{engsic} (n);
end
$c_{engtotsic}$ = 0;
for i= 1:15
$c_{engtotsic}$ = ($c_{pricesic}$*$E_{losssic}$)/(1+r)^i + $c_{engtotsic}$;
end
figure(2)
plot(years, LCCsic, '-*', 'LineWidth', 1.5)
figure(3)
plot(years, LCCgan, '-*', 'LineWidth', 1.5)
hold on
plot(years, LCC_{sic}, '-*', 'LineWidth', 1.5)
hold off
xlabel('Number of years [n] ',' LineWidth', 1.5)
ylabel('LCC [SEK]','LineWidth',1.5)
legend('GaN LCC','SiC LCC');
grid on

A.2 System Level Simulations

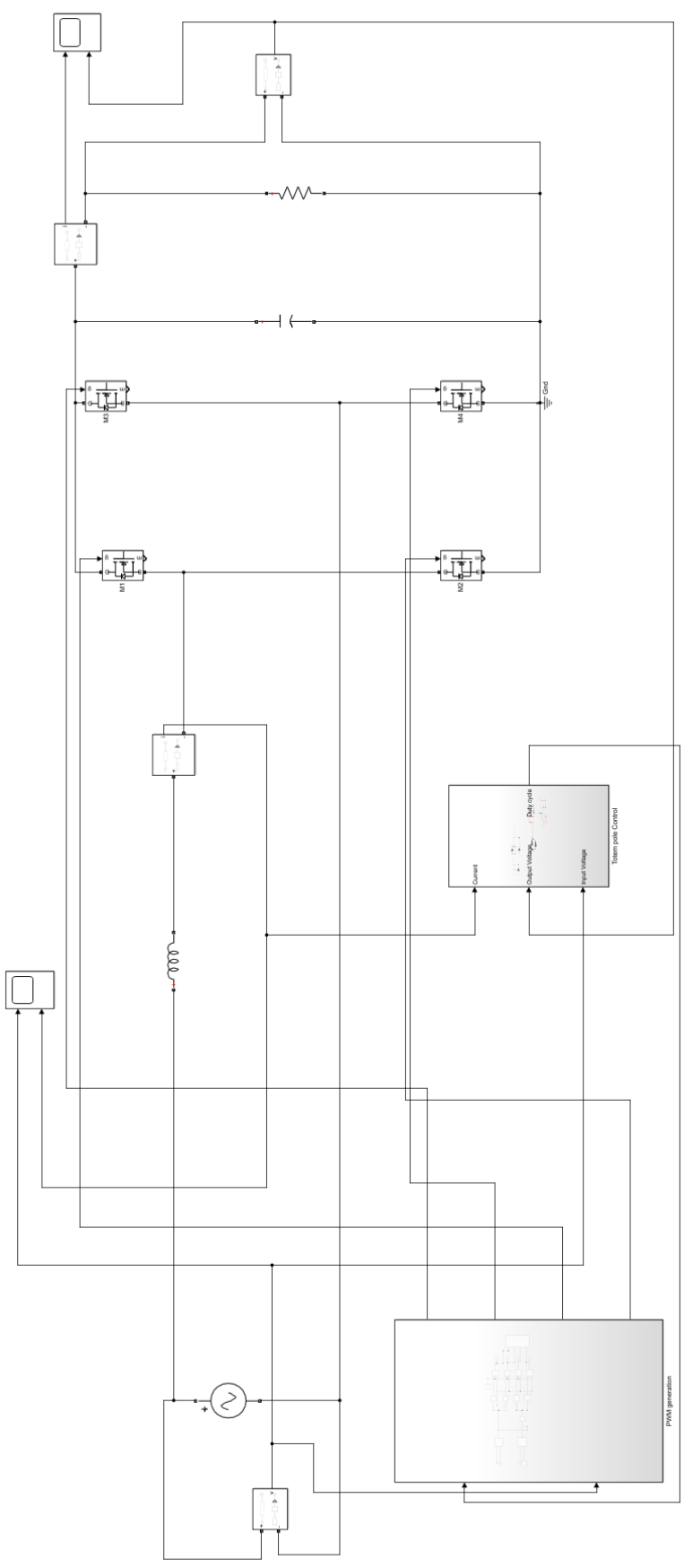


Figure A.1: Closed loop implementation of totem pole PFC in simulink

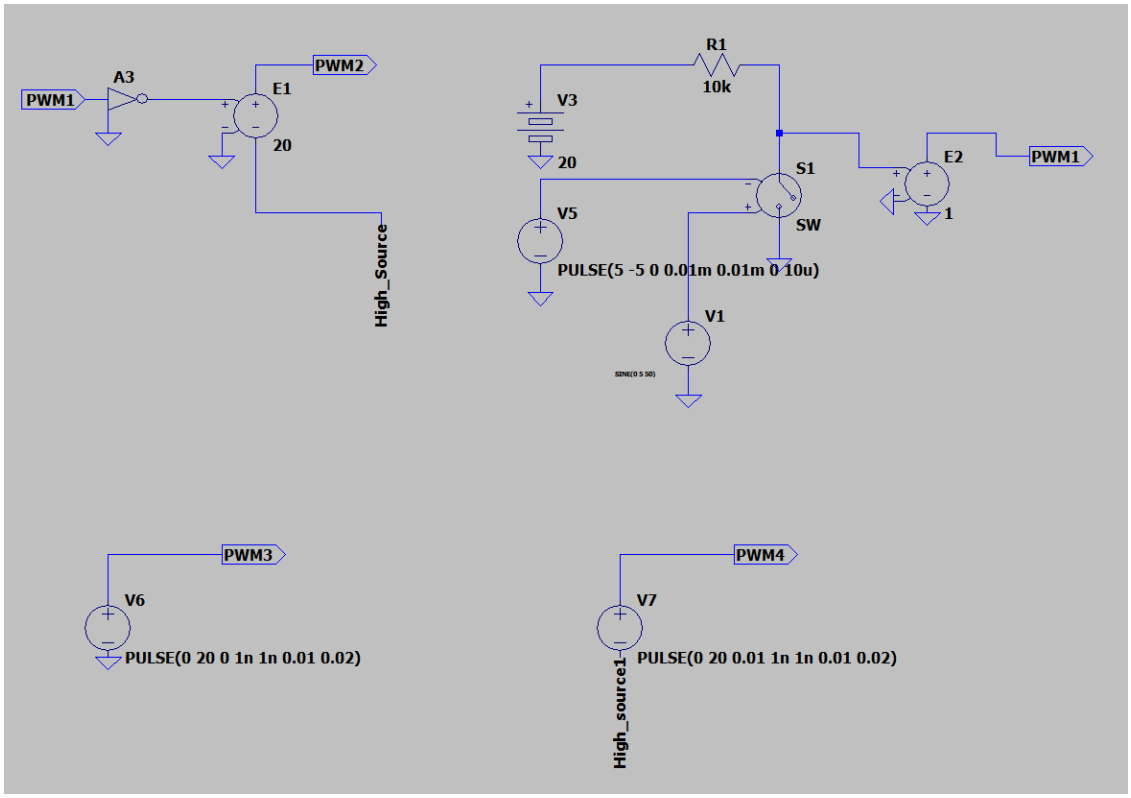


Figure A.2: PWM implementation of totempole PFC in LTSpice

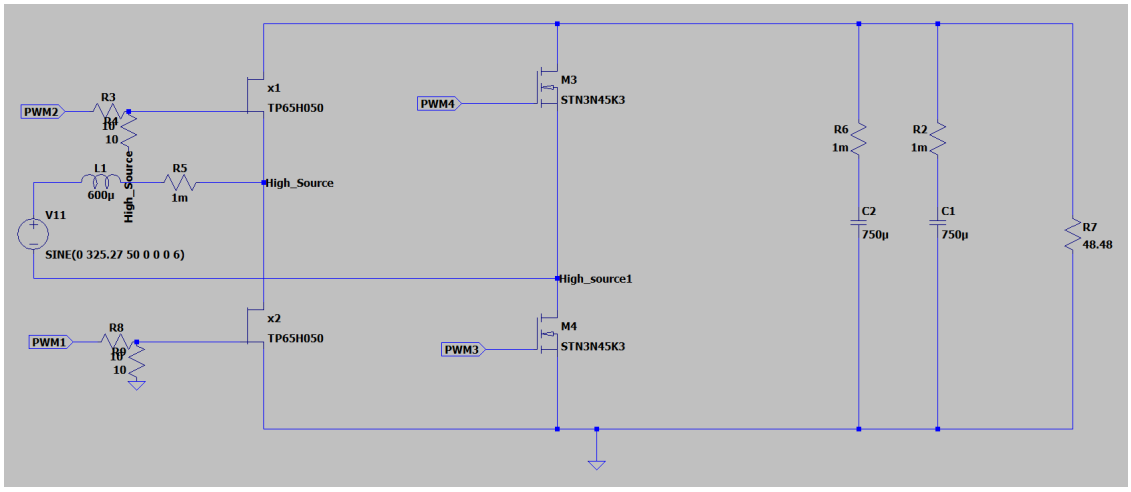


Figure A.3: Open loop implementation of totempole PFC in LTSpice