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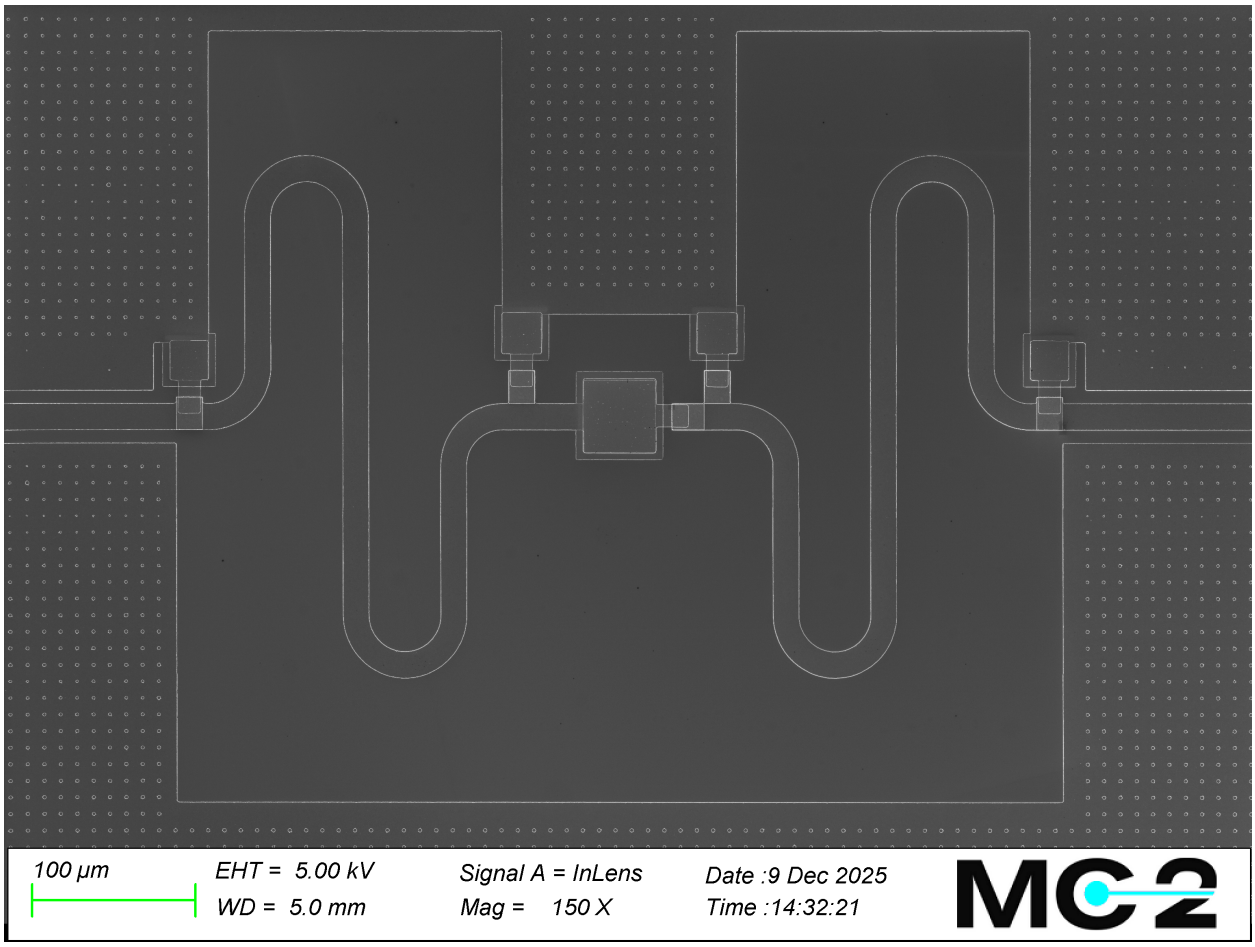

On-Chip Bandpass Filter for Superconducting Devices

Master's Thesis in Nanotechnology

Job Winkel

DEPARTMENT OF MICROTECHNOLOGY AND NANOSCIENCE
CHALMERS UNIVERSITY OF TECHNOLOGY
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Master's thesis 2026

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Cover: SEM image of the fabricated second-order on-chip bandpass filter designed and measured in this thesis.

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Abstract

On-chip lumped element bandpass filters offer a pathway to tightly integrate noise suppression directly at the chip level in superconducting quantum devices. Despite the widespread use of filters in cryogenic qubit setups, co-fabricated lumped element bandpass filters remain relatively unexplored. This work evaluates their feasibility, design constraints, and performance when embedded directly on a superconducting qubit chip, paving the way for scalable quantum architectures.
The filter design follows a standard radio frequency (RF) synthesis approach, adapted to cryogenic operation, co-fabrication constraints, limited footprint, and superconducting drive requirements. A scalable design flow is developed to implement arbitrary-order bandpass filters using lumped inductors and capacitors. Electromagnetic (EM) simulations are employed to extract effective component parameters and refine circuit models beyond ideal lumped element approximations.
Simulations show that on-chip lumped element bandpass filters can achieve well-defined passband characteristics and support higher-order architectures. However, ideal and extended lumped element models alone are insufficient to predict device response accurately. Direct optimization with computationally intensive EM simulations were therefore necessary to achieve reliable filter performance.
The filter response also directly influences the thermal noise spectrum experienced by the qubit. Modeling indicates that appropriately designed bandpass filters can reduce unwanted thermal occupation, providing a tool for engineering and investigating the qubit's EM environment.
A prototype device was fabricated and characterized at cryogenic temperatures. The measured response did not exhibit the intended passband, with analysis pointing to fabrication issues, particularly unreliable capacitor connections, rather than limitations of the filter concept or design methodology.
Overall, this work establishes a simulation-driven platform for co-fabricated lumped element bandpass filters in superconducting quantum circuits. The results demonstrate their feasibility, scalability, and potential for controlled thermal noise engineering in cryogenic quantum hardware.

Keywords: superconducting quantum computing, driveline, bandpass filter, on-chip, lumped element, thermal noise

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Finally, I would like to express my appreciation for the love and support of my family. You are always there for me.

Job Winkel, Gothenburg, Feb 2026

List of Acronyms

ADS	Advanced Design System
Al	aluminum
ALD	atomic layer deposition
AlO_x	aluminum oxide
Ar	argon
AWG	arbitrary waveform generator
BCS	Bardeen–Cooper–Schrieffer
BW	bandwidth
CPW	coplanar waveguide
DC	direct current
EM	electromagnetic
HfO_x	hafnium oxide
JJ	Josephson junction
PVD	physical vapor deposition
RF	radio frequency
SEM	scanning electron microscope
SNR	signal to noise ratio
SNAIL	superconducting nonlinear asymmetric inductive elements
SQUID	superconducting quantum interference device
VNA	vector network analyzer

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Introduction

1.1 Motivation and Aim

The current state of quantum computing resembles the semiconductor industry in the 1960s. At that time, the transistor had been invented, but it was still unclear which platform, such as vacuum tubes, silicon based semiconductors, or germanium based semiconductors, would dominate the emerging field of microelectronics. Yet the breakthrough of silicon-based integrated circuits eventually triggered the exponential scaling of transistors known as Moore's law. Today, quantum computing finds itself in a similar position: several promising physical platforms exist, such as superconducting qubits [1], trapped ions [2], photonic systems [3], neutral atoms [4], and semiconductor spin qubits [5]. However, it remains an open question which of these technologies will ultimately scale in a way comparable to silicon-based transistors. Resolving this question will depend on the scalability, coherence, and manufacturability of each platform. Not only high-level theoretical performance matters, but also practical feasibility and technology readiness. This has led scientists and engineers worldwide to actively research and develop quantum hardware in order to overcome fundamental technical challenges.

Among the existing contenders, superconducting qubits have emerged as one of the most advanced and commercially adopted approaches. Decades of research in superconductivity and Josephson junction (JJ) physics—recognized by the 2025 Nobel Prize in Physics [6]—have enabled practical implementations of superconducting quantum processors. Major industrial players such as IBM, Google, IQM, and Rigetti have built large scale prototypes, achieving rapid progress in gate fidelities, coherence times, and system integration [7–9]. Superconducting qubits offer several advantages: fast gate operations, high fidelity readout, compatibility with GHz control electronics, and well established lithographic fabrication methods. However, they remain limited by relatively short coherence times, largely due to strong coupling to the electromagnetic environment, sensitivity to microwave noise, and material defects. In addition, the current fabrication techniques are not fully compatible with semiconducting manufacturing [10].

To reduce this noise, superconducting quantum systems employ a combination of cryogenic attenuators and filters distributed along the microwave signal chain [11, 12]. While effective for small setups, this approach scales poorly as system size increases. Each qubit requires a filtered control line, a readout line and optionally a flux line, leading to higher thermal load, signal loss, and overall hardware complexity. Efforts to reduce the number of lines through multiplexing cryogenic

CMOS [13], row column addressing [14], adiabatic superconducting logic [15], or optimized drive pulses [16] have been investigated; however, these techniques remain in early development and currently have limited applicability. Furthermore, conventional broadband filters provide only partial suppression of thermal noise and offer little flexibility in their frequency response due to their physical integration along the wiring.
A more scalable alternative is to integrate noise filtering directly at the chip level. Previous approaches, such as quantum Josephson filters [17, 18], have shown promising results, but suffer from increased AC Stark shifts, limiting their practical use. This thesis investigates an alternative design: an on-chip bandpass filter intended to suppress out of band noise while maintaining strong coupling in the qubit control band. Such an integrated filter, co-fabricated alongside qubit devices, can reduce thermal noise coupling, eliminate the need for additional discrete filter components, and enable more compact and scalable architectures for future superconducting quantum processors. The main objective of this work is to design, simulate, and experimentally validate a bandpass filter suitable for integration with superconducting qubit systems. The design begins with an ideal lumped element model to establish the initial filter parameters and gain physical intuition. Subsequently, EM simulations are performed to refine the geometry and align the frequency response with the desired qubit operating band, typically in the range of 4–8 GHz. These simulations also provide data for refining the equivalent lumped model, forming the basis of a scalable and automated design workflow. Following the design phase, the filter was fabricated and characterized at cryogenic temperatures to assess its performance and validate the simulation results. The outcome will demonstrate the feasibility of integrating filters directly onto superconducting chips, contributing to more scalable quantum hardware design.

1.2 Thesis Structure

This thesis begins with the theoretical framework required for filter synthesis and its application in superconducting quantum hardware in Chapter 2. This chapter introduces the fundamentals of quantum computing, superconducting qubit operation, decoherence mechanisms, and classical microwave filter theory.
In Chapter 3, two experimental implementations in the form of two-port and four-port devices are proposed to validate and benchmark the filter concept. This chapter outlines the complete design flow for the filter synthesis, following a standard RF filter design procedure modified for superconducting applications, and describes the software tools used for circuit synthesis and EM simulation. It further presents the fabrication process, the cryogenic measurement setup in a dilution refrigerator, and the calibration procedures for both two-port and four-port measurements. These elements are described to clarify how the designed devices are experimentally realized and characterized.
In Chapter 4, the filter synthesis, modeling, and iterative optimization are presented in the first part, including the development of circuit models, parameter extraction, and physical layout optimization. Experimental validation and characterization of the fabricated devices are then discussed in the second part, including comparison

between simulation and measurement, analysis of deviations, and identification of potential shortcomings. In addition, a thermal model is introduced to analyze the expected thermal environment of the four-port device and to quantify the effectiveness of the designed filter.
Finally, the main findings are summarized in Chapter 5, where the results are critically assessed and directions for future work are outlined. Supplementary material on signal bandwidth considerations, inductance extraction, parameter fitting, and resistive measurements is provided in Appendices A to D.

2

Theory

2.1 Quantum Computing

The idea of a quantum computer first popularized by Richard Feynman, who in 1982 proposed that simulating quantum systems efficiently would require a computer based on quantum mechanics itself [19]. This initiated the search for a practical quantum computing platform. The first question to address is: What kind of physical system can realize a quantum computer?
Each platform offers its own strengths and weaknesses, but the key challenge remains identifying a scalable and reliable platform for useful quantum computation. To assess the suitability of candidate systems, DiVincenzo formulated a now standard set of criteria [20] that any quantum computing architecture must meet:

- Scalable qubits with well characterized behavior,
- Reliable initialization,
- Long coherence times,
- A universal set of quantum gates, and
- The ability to perform qubit specific measurements.

Superconducting qubits are widely considered to satisfy all of these requirements and, as discussed previously, are among the leading platforms for scalable quantum computing. For further details on the current state of the art in quantum computing architectures, see Wilhelm *et al.* [10]. For a general introduction to superconductivity and superconducting qubits, please see Tinkham [21] and Krantz *et al.* [22].

2.2 Superconducting Qubits

Superconducting qubits are based on the phenomenon of superconductivity [23]. This effect is observed when a superconducting material is cooled below its critical temperature and starts to exhibit zero electrical resistance; hence the name. The Bardeen–Cooper–Schrieffer (BCS) theory is often used to describe this phenomenon. In the model, Cooper pairs, which are two electrons paired together, form a condensate. This condensate exhibits quantum mechanical behavior and can be described by a single macroscopic wavefunction [24]. The nonlinear element of a superconducting qubit, enabled by this macroscopic wavefunction, is the JJ, a thin insulating barrier separating two superconductors, as shown in Fig. 2.1. The JJ behaves as a nonlinear, lossless inductor governed by the current-phase and voltage-phase rela-

tions

$$I = I_c \sin\phi, \qquad V = \frac{\hbar}{2e}\frac{d\phi}{dt}, \tag{2.1}$$

where I_c is the critical current, ϕ is the superconducting phase difference across the junction, $\hbar$ is the reduced Planck constant, and e is the elementary charge [25]. This phase represents the quantum mechanical phase accumulated by Cooper pairs tunneling through the barrier. When combined with a shunting capacitor, the JJ forms a nonlinear LC oscillator. The resulting anharmonicity makes the energy level spacing slightly unequal compared to a harmonic oscillator, as illustrated in Fig. 2.2. This property enables selective control of specific energy transitions fundamental for qubit control.

The first superconducting qubit to demonstrate coherent quantum oscillations, reported by Nakamura *et al.* [26], was the charge qubit, also known as the Cooper pair box. This architecture, in the simplified model shown in Fig. 2.4, consists of a superconducting island coupled to a reservoir via a JJ, and capacitively coupled to a gate electrode. The reservoir inherently provides a stray capacitance to the superconducting island. The Hamiltonian of such a system is given by

$$\hat{H} = 4E_C(\hat{n} - n_g)^2 - E_J \cos\hat{\phi}, \tag{2.2}$$

where $E_C = \frac{e^2}{2C}$ is the charging energy, $E_J = \frac{\hbar I_c}{2e}$ is the Josephson energy, $\hat{n}$ is the number operator for Cooper pairs on the island, and $n_g = \frac{C_g V_g}{2e}$ is the dimensionless offset charge induced by the gate voltage V_g. Approximating $\cos\phi \approx 1 - \frac{\phi^2}{2}$ for small ϕ simplifies the Hamiltonian to

$$\hat{H} = 4E_C(\hat{n} - n_g)^2 - E_J\left(1 - \frac{\hat{\phi}^2}{2}\right), \tag{2.3}$$

which corresponds to a particle in a quadratic potential. In this approximation, the energy levels are equally spaced. However, retaining higher-order terms in the cosine expansion introduces a weak anharmonicity, which breaks the equidistant level spacing. This anharmonicity enables selective addressing of the lowest two energy levels and gives rise to atom-like behavior, motivating the description of superconducting qubits as *artificial atoms* [27].

Early implementations of these qubits suffered from strong charge noise sensitivity, as seen in Fig. 2.3. At small ratios $\frac{E_J}{E_C}$, the qubit transition frequencies shift significantly with offset charge, causing decoherence. Increasing $\frac{E_J}{E_C}$ by adding a shunt capacitor between the island and reservoir, as seen in Fig. 2.4, suppresses this sensitivity but introduces greater susceptibility to flux noise due to the conjugate nature of $\hat{n}$ and $\hat{\phi}$ [28].

When $\frac{E_J}{E_C} \gg 1$, the device enters the *transmon* regime [28], where the energy levels become nearly flat and coherence improves dramatically. Additional tunability is achieved by replacing the single JJ with a SQUID loop, enabling flux-tunable variants such as the flux-tunable transmon [29]. A complementary approach increases the inductance rather than the capacitance, leading to architectures such as the *fluxonium* qubit [30]. These three families represent the most widely used designs

today, although many other qubit types exist, each offering their own trade-offs [31–33].

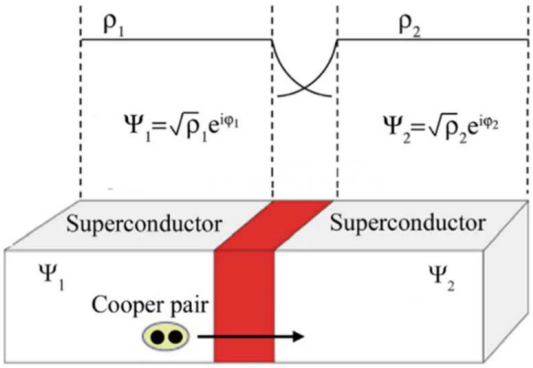

Figure 2.1: Schematic representation of a Cooper pair tunneling across the JJ, where coherent tunneling gives rise to the Josephson effect [34].

In practical implementations, superconducting qubits are most commonly fabricated using aluminum (Al) on silicon. While alternative superconducting materials such as tantalum and niobium, as well as alternative substrates such as sapphire, are actively investigated and increasingly employed, Al on silicon remains the dominant platform due to its reliable, well-established, and comparatively straightforward fabrication processes [35–37].

2.2.1 Bloch sphere

To represent the state of a qubit, the Bloch sphere is typically used to provide physical intuition. The Bloch sphere is a unit sphere centered at the origin, where the two lowest energy states, $|0\rangle$ and $|1\rangle$ of the qubit, form the computational basis. Any pure qubit state can then be expressed as

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle\,, \qquad |\alpha|^2 + |\beta|^2 = 1, \tag{2.4}$$

where α and β are complex probability amplitudes. The qubit state can then be mapped on the Bloch sphere as a Bloch vector, as seen in Fig. 2.5, with $|0\rangle$ at the north pole and $|1\rangle$ at the south pole. In this picture, the Pauli operators generate rotations: $\hat{\sigma}_x$ rotates the state around the x-axis, $\hat{\sigma}_y$ around the y-axis, and $\hat{\sigma}_z$ around the z-axis, with $\hat{\sigma}_z$ corresponding the change of the qubit state [38]. This visualization can be further extended to mixed states. For further details, see Krantz *et al.* [22].

2.2.2 Qubit Readout

Since the energy transitions of qubits are relatively small, superconducting qubits must be isolated from thermal noise in the environment to prevent unwanted excitations. However, strong isolation makes direct measurement of the qubit state difficult. To overcome this, qubits are weakly coupled to a microwave resonator that acts as a readout element.

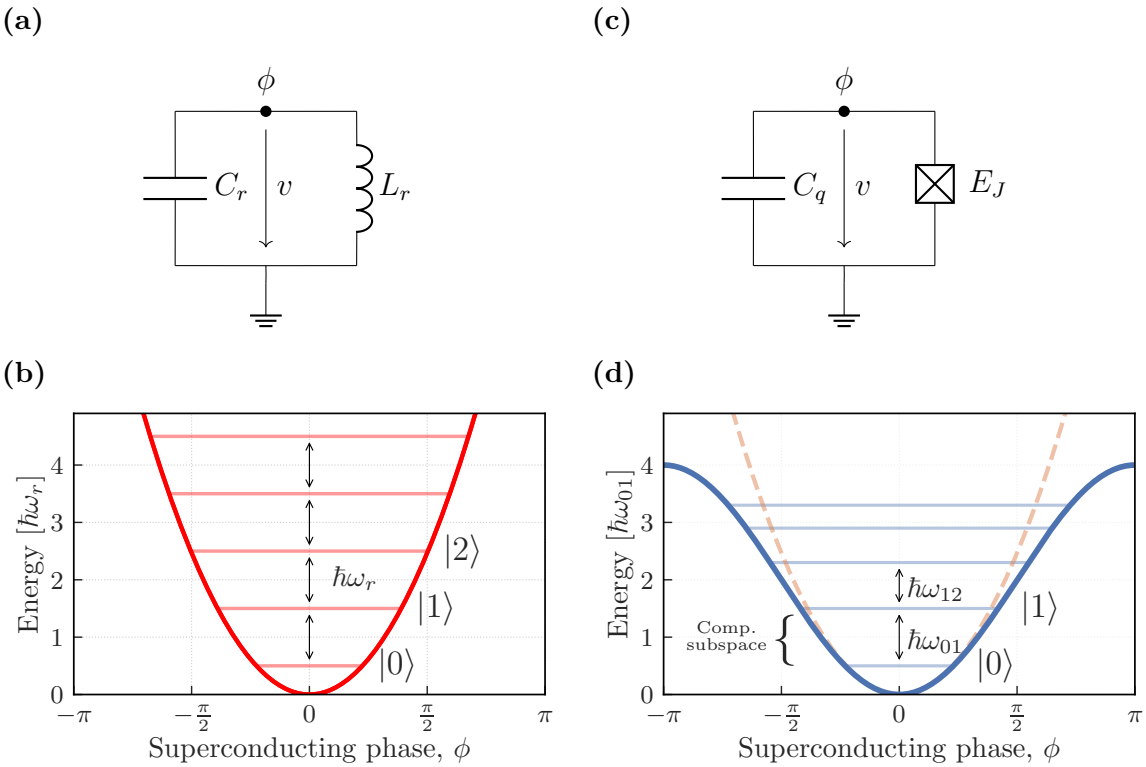

Figure 2.2: Simplified circuit diagram of (a): quantized harmonic parallel LC oscillator with inductance L_r in parallel with capacitance C_r, where φ represents the superconducting phase difference of the upper island with respect to ground and v the voltage across the capacitor. (b) is the corresponding energy potential with equidistant energy levels separated by $\hbar\omega_r$. In comparison simplified circuit diagram of (c): quantized JJ qubit consisting of a capacitor C_q in parallel with the nonlinear Josephson inductance with Josephson energy E_J. (d) is the corresponding energy potential with anharmonicity $\alpha = \hbar(\omega_{12} - \omega_{01})$. The lowest energy states form a two-level system commonly used as the computational subspace [22].

In the dispersive regime ($|\Delta| = |\omega_q - \omega_r| \gg g$), such a qubit-resonator system can be modeled by the Jaynes–Cummings Hamiltonian:

$$\hat{H} = \frac{\hbar\omega_q}{2}\hat{\sigma}_z + \hbar\omega_r\left(\hat{a}^\dagger\hat{a} + \frac{1}{2}\right) + \hbar\chi\left(\hat{a}^\dagger\hat{a} + \frac{1}{2}\right)\hat{\sigma}_z, \tag{2.5}$$

where ω_q and ω_r are the qubit and resonator frequencies, g is the coupling energy, and χ is the dispersive frequency shift given by $2\chi = \frac{g^2}{\Delta}$ [39]. We observe that the frequency of the readout resonator shifts by $2\hbar\chi$ depending on the state of the qubit. Therefore by probing the resonator's frequency at low photon numbers, the qubit state can be inferred without directly disturbing it. This allows a weak measurements of the qubit state. It exemplifies that the readout resonator decoupled the qubit from the environment while preserving the ability to determine the state of the qubit. Further details can be found in Krantz *et al.* [22].

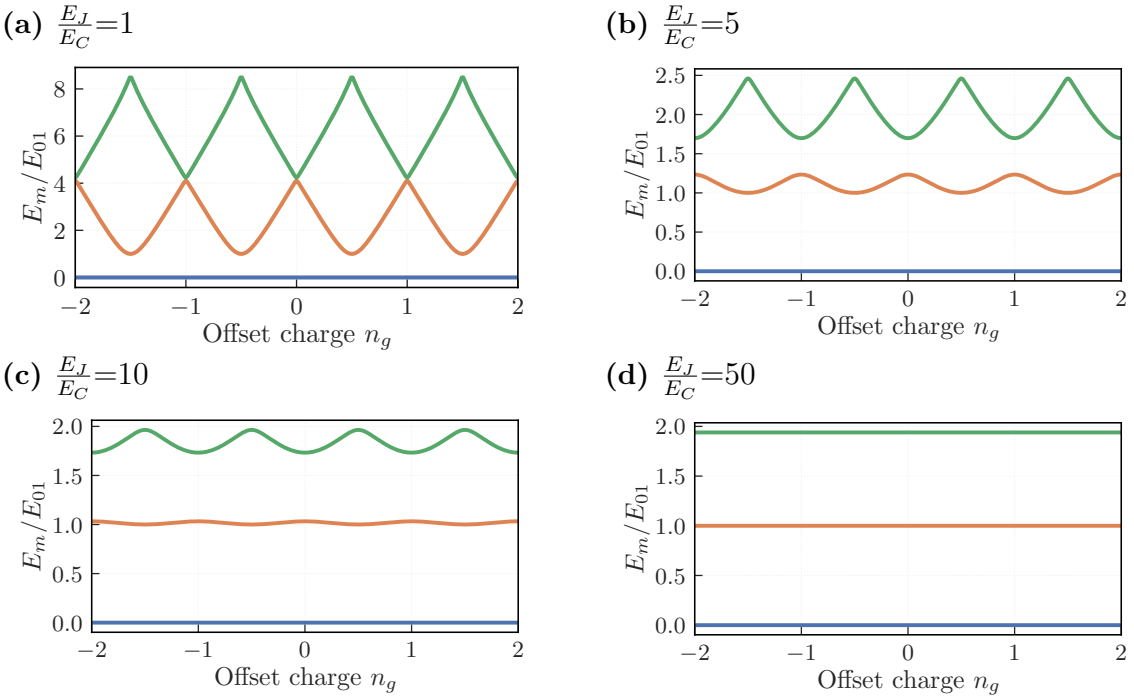

Figure 2.3: First three eigenenergies E_m from lowest to highest (blue, orange, green) for the Hamiltonian of a transmon qubit in Eq. (2.2) for varying ratios of $\frac{E_J}{E_C}$ as a function of the offset charge [28].

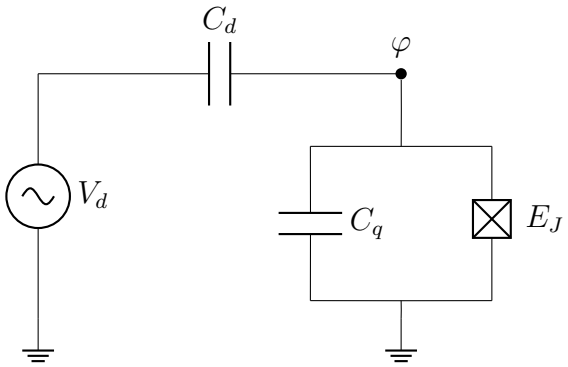

Figure 2.4: Simplified circuit representation of a qubit, referenced in Fig. 2.2c. The charge island is capacitively coupled to a voltage drive V_d through the coupling capacitance C_d. The capacitance C_q represents the total stray capacitance of the island to the surrounding circuit. The phase difference across the JJ with Josephson energy E_J, is denoted by φ.

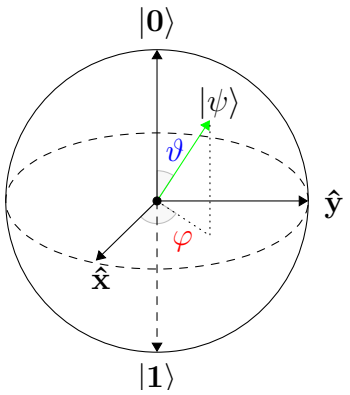

Figure 2.5: Example Bloch sphere represented as a unit sphere with $|0\rangle$ at the north pole and $|1\rangle$ at the south pole. $|\psi\rangle$ represents the qubit state as a Bloch vector with spherical coordinates $(1, \vartheta, \varphi)$.

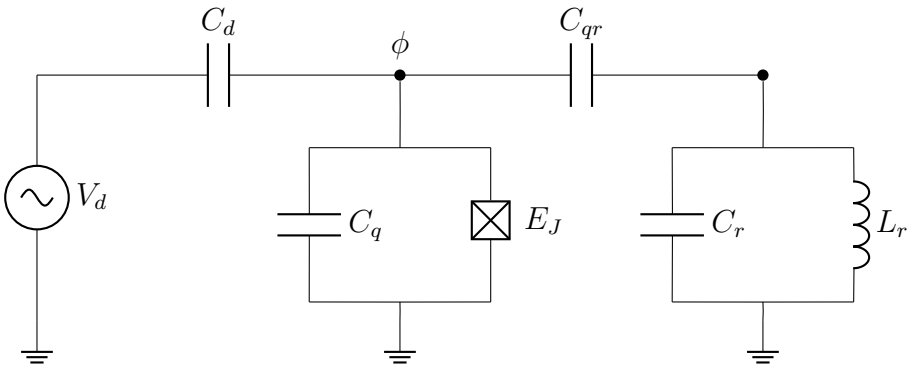

Figure 2.6: Simplified schematic of a transmon-style qubit coupled to a external drive as seen in Fig. 2.4, coupled to a readout resonator with capacitance C_{qr} coupling the readout resonator to the qubit separately from the drive.

2.2.3 Qubit Drive

To manipulate the qubit state, an external microwave drive is applied through a dedicated drive line, as illustrated in Fig. 2.6. The dedicated drive line provides direct capacitive coupling to the qubit. Neglecting the readout resonator, the effective Hamiltonian can be found as:

$$\hat{H} = -\frac{\hbar\omega_q}{2}\hat{\sigma}_z + g_d V_d(t)\hat{\sigma}_y, \tag{2.6}$$

where g_d is the drive coupling strength and $V_d(t)$ is the drive voltage. In the rotating frame at ω_q and for a sinusoidal envelope $V_d(t) = V_0 s(t)\sin(\omega_d t + \theta)$, the drive Hamiltonian becomes

$$\hat{H}_d = -\frac{g}{2}V_0 s(t)\left(I\hat{\sigma}_x + Q\hat{\sigma}_y\right), \tag{2.7}$$

with $I = \cos(\theta)$ and $Q = \sin(\theta)$ representing the in-phase and quadrature components. On the Bloch sphere, I-components generate rotations about the x-axis and Q-components about the y-axis, enabling precise control over the qubit state. Further detailed deviation skipped here can be found in [22, 40, 41].

2.2.4 Decoherence and Noise

Qubits are delicate systems that inevitably interact with their environment, leading to energy relaxation and dephasing. Both processes reduce the information stored in the qubit state. The characteristic timescales for these processes are denoted by $T_1 = \frac{1}{\Gamma_1}$ and $T_2 = \frac{1}{\Gamma_2}$, where Γ_1 represents the longitudinal decay rate and Γ_2 represents the transverse relaxation rate. These rates satisfy

$$\frac{1}{T_2} = \frac{1}{2T_1} + \frac{1}{T_2^*}, \tag{2.8}$$

where $\Gamma_2^* = \frac{1}{T_2^*}$ is the pure dephasing rate. On the Bloch sphere, T_1 processes correspond to rotations of the Bloch vector towards the $|0\rangle$ state, while pure dephasing corresponds to rotations around the Bloch vector towards the z-axis.
Energy relaxation, or T_1 decay, can be described by Fermi's golden rule:

$$\frac{1}{T_1} = \sum_{\lambda} \frac{2}{\hbar} \left| \langle e| \hat{D}_\lambda |g\rangle \right|^2 S_\lambda(\omega_q), \tag{2.9}$$

where the sum runs over all environmental noise channels λ. For each channel λ, $S_\lambda(\omega_q)$ denotes the corresponding environmental noise spectral density evaluated at the qubit transition frequency ω_q, and $\hat{D}_\lambda$ is the transition dipole operator describing the coupling of the qubit to that noise channel. Typically, the dominant noise sources include charge noise, photon number fluctuation, quasiparticle noise, and flux noise in flux-tunable qubits. Since $\hat{D}_\lambda$ is generally proportional to the coupling strength k_λ, the relaxation rate increases with stronger coupling to the environment. Therefore, the coupling between the qubit and its environment, such as drive and readout lines, should be minimized to prevent leakage. However, reducing this coupling also reduces control and readout coupling, requiring larger drive amplitudes [38, 42].
A main contributor to the coherence time T_2 for dispersive readout is the residual thermal photon population in the readout resonator. Photon number fluctuations in the resonator induce fluctuations of the qubit transition frequency via the AC Stark effect,

$$\Delta_{\text{Stark}}^{\text{th}} = \eta\, 2\chi\bar{n}, \tag{2.10}$$

which in turn lead to a resonator-induced dephasing rate

$$\frac{1}{T_2^{\text{th}}} = \eta\, \frac{4\chi^2}{\kappa}\bar{n}, \tag{2.11}$$

where $\eta = \frac{\kappa^2}{\kappa^2+4\chi^2}$, $\bar{n}$ is the mean thermal photon number in the resonator, κ is the resonator linewidth (decay rate), and χ is the dispersive shift [42]. This highlights why superconducting qubits must operate in the millikelvin regime. Even though the dilution refrigerator reaches ∼10 mK, the effective qubit temperature is usually significantly higher [12, 42, 43]. One of the causes is thermal noise coupling through the drive line directly to the qubit and can inadvertently inject photons into the readout resonator, increasing the dephasing rate [44].
To mitigate this, extensive filtering and attenuation are implemented along the drive path. Each attenuator at temperature $T_{i,att}$ adds thermal noise according to

$$n_i(\omega) = \frac{n_{i-1}(\omega)}{A_i} + \frac{A_i - 1}{A_i} n_{BE}(T_{i,att}, \omega), \tag{2.12}$$

where A_i is the attenuation factor and n_{BE} is the Bose–Einstein distribution. This shows how the temperature of each stage critically affects the thermal photon population seen by the qubit and requires cryo engineering to achieve optimal results [11]. The attenuation inherently causes heating of the dilution refrigerator while requiring increased drive power. This illustrates the dilemma between weak coupling and strong attenuation at low temperatures to improve coherence and the need for sufficient drive power without excessive thermal load.

2.3 Passive Microwave Filters

In the following, a concise overview of the most relevant background information on passive microwave filters is provided, closely following Pozar [45] and Hong [46].
Passive microwave filters are essential components in superconducting quantum hardware, as they shape the spectral content of control, readout signals, and noise. In superconducting qubit systems, filtering is typically implemented along cryogenic drive lines to suppress unwanted frequency components and thermal radiation originating from higher temperature stages, while preserving efficient coupling at the qubit transition frequency. Out-of-band signals can induce decoherence, residual qubit excitation, quasiparticle generation, and an increased effective thermal population [11].
The filter behavior is fully characterized by its scattering parameters, which relate incident and reflected traveling waves at the network ports. The forward transmission coefficient $S_{21}(\omega)$ describes the ratio of the transmitted wave at port 2 to the incident wave at port 1 and therefore quantifies how strongly signals propagate through the filter at a given frequency. The reflection coefficient $S_{11}(\omega)$ characterizes the impedance matching at the input port. For a linear reciprocal two-port network, the transmission is symmetric, such that $S_{21} = S_{12}$, and the reflection properties at both ports are identical for a symmetric design, i.e., $S_{11} = S_{22}$. For qubit control applications, the filter must provide strong attenuation outside the passband while maintaining a 50 Ω match within the passband to avoid reflections.
The passive microwave filters examined in this work focus on reflective filters, which are ideally lossless and based on reactive network synthesis. Other implementations, such as absorptive filters including Eccosorb [47] or HERD filters [48], rely on lossy transmission mechanisms and are widely used for infrared suppression and high-frequency noise filtering. In contrast, reflective filters are implemented using reactive elements and can be realized with either lumped or distributed components.
Lumped element filters consist of discrete capacitive and inductive components, such as parallel-plate capacitors, spiral inductors, or others, enabling compact on-chip integration. However, at higher frequencies, the signal wavelength becomes comparable to the physical dimensions of these components. As a result, parasitic inductances and capacitances increasingly dominate their behavior, and the assumption of an lumped elements breaks down. This limits the applicability of purely discrete components when the wavelength approaches a significant fraction of the components size.
In this regime, distributed elements become relevant. Distributed filters exploit the wave nature of the signal, using transmission line sections to engineer constructive

and destructive interference in order to realize the desired frequency response. Their physical dimensions are typically on the order of the wavelength, making the filter size directly dependent on the operating frequency. In the GHz regime, both lumped and distributed implementations are commonly used separately and together, depending on the specific application and footprint constraints.
In this work, the focus is placed on lumped element implementations due to their significantly smaller footprint, low insertion loss, and step roll off, making them suitability for compact on-chip integration.

2.3.1 Low-Pass Prototype Synthesis

The synthesis of passive filters is commonly performed by approximating a desired transfer function with a polynomial that corresponds to a physically realizable circuit. The chosen approximation method and polynomial define a large design parameter space. A common starting point is the squared magnitude of the transmission coefficient S_{21},

$$|S_{21}(j\Omega)|^2 = \frac{1}{1 + \epsilon^2 F_n^2(\Omega)}, \tag{2.13}$$

where Ω denotes the normalized frequency, ϵ controls the passband ripple, and $F_n(\Omega)$ is an n-th order polynomial defining the approximation type. The filter order n determines the achievable transition steepness and stopband attenuation. The approximation polynomial $F_n(\Omega)$ uniquely defines the filter prototype, with each prototype exhibiting distinct properties. The most common prototype are:

- **Butterworth Prototype**
  Defined by $F_n(\Omega) = \Omega^n$. The magnitude response is maximally flat at $\Omega = 0$, meaning all derivatives up to order $2n - 1$ vanish. This results in a comparatively slow roll-off, where roll-off denotes the rate at which attenuation increases beyond the cutoff frequency.
- **Chebyshev Prototype**
  Defined using Chebyshev polynomials of the first kind, $F_n(\Omega) = T_n(\Omega)$. This introduces equal ripple in the passband with amplitude determined by ϵ. The ripple corresponds to periodic variations in $|S_{21}|$ within the passband. For a given order, the Chebyshev approximation yields a steeper roll-off than the Butterworth response.
- **Elliptic (Cauer) Prototype**
  By introducing equal ripple in both the passband and stopband, this prototype achieves the fastest possible roll-off for a given order. Although, this increases the sensitivity to parameter variations.
- **Bessel Prototype**
  Based on polynomials related to Bessel functions, this prototype is optimized for maximally flat group delay,

  $$\tau_g = \frac{d}{d\Omega} \arg[H(\Omega)].$$

  A flat group delay reduces signal distortion at the expense of a slower amplitude roll-off.

A comparison of the resulting bandpass filters derived from these prototypes, in terms of transmission and reflection behavior, is shown in Fig. 2.7.

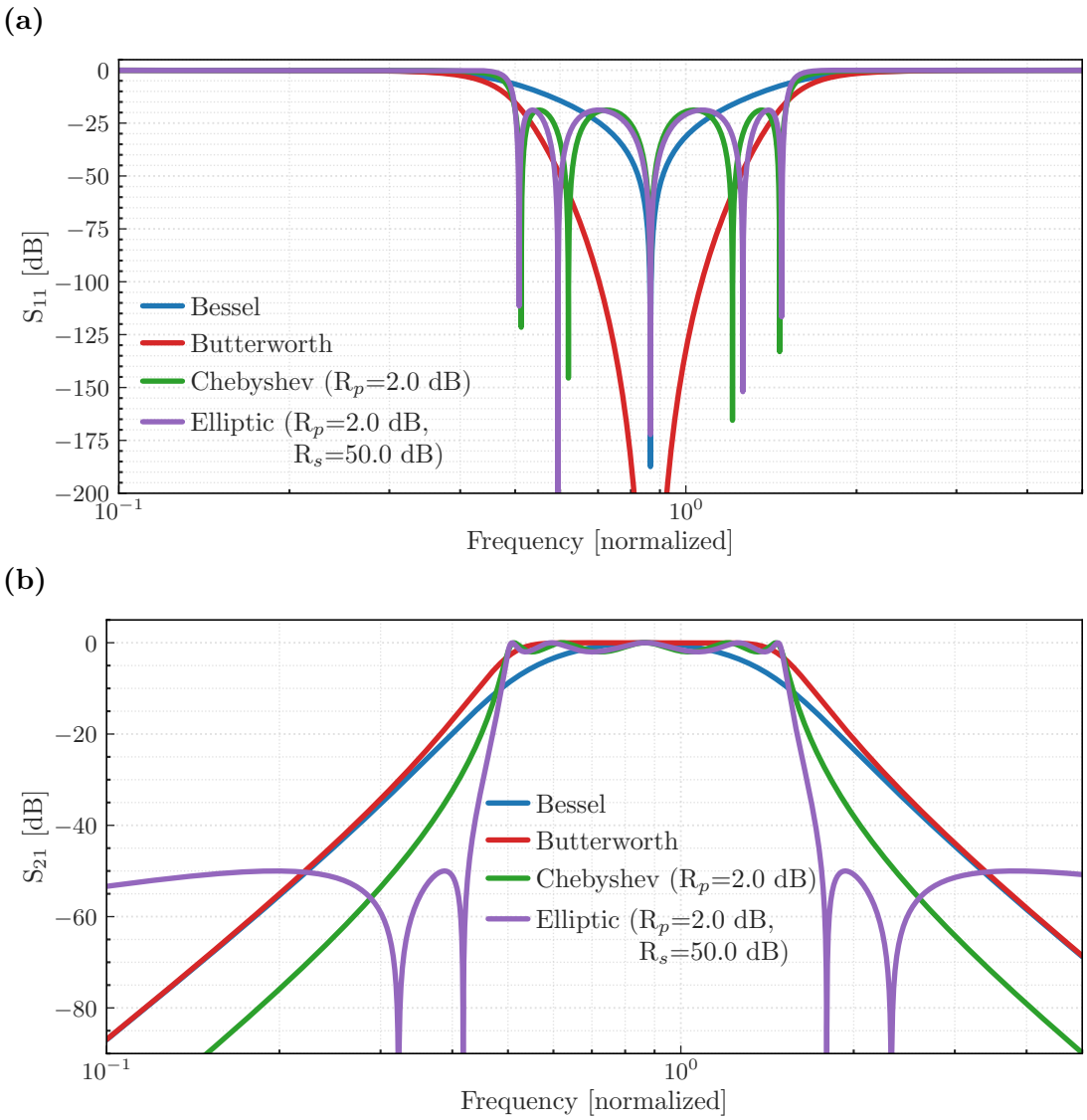

Figure 2.7: Normalized (a) reflection S_{11} and (b) transmission S_{21} responses for different passive bandpass filter types, where R_p denotes the passband ripple and R_s the stopband attenuation.

The synthesis procedure begins with a normalized low-pass ladder network characterized by element values z_k for $k = 1, \ldots, n$, where n is the filter order. These parameters define the normalized reactances of the elements, as illustrated in Fig. 2.8. The prototype is defined for a cutoff frequency $\Omega_c = 1$, source impedance $z_0 = 1\,\Omega$, and load impedance z_{n+1}. The specific values z_k depend on the chosen approximation.
The normalized values are transformed into physical inductances and capacitances through impedance and frequency scaling by selecting the desired cutoff frequency Ω_c and source impedance z_0. To obtain a bandpass filter, the low-pass prototype is further subjected to the frequency transformation

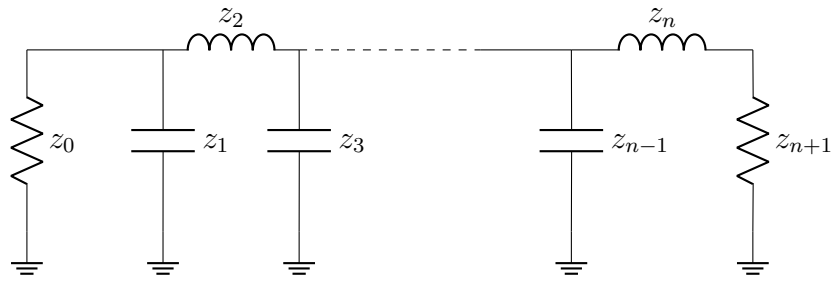

Figure 2.8: Exemplary low-pass prototype of a filter of even order, where z_k corresponds to the normalized element values.

$$\frac{\Omega}{\Omega_c} = \frac{\omega_0}{\omega_2 - \omega_1}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right), \tag{2.14}$$

where ω_1 and ω_2 define the passband edges, and $\omega_0 = \sqrt{\omega_1\omega_2}$ is the center frequency. Under this transformation, each reactive element of the low-pass prototype is converted into a resonant LC branch.
The resulting network can be algebraically simplified using linear transformations such as impedance inverters, series–parallel conversions, or equivalent resonator representations. These operations preserve the transfer function while enabling topologies that are better suited for compact on-chip realization.
In superconducting qubit applications, Chebyshev and elliptic prototypes are typically used due to their steep roll-off behavior.

3
Methods

In the following sections, the experiment design and the design flow used for the filter synthesis is outlined, prior to describing the thermal model and the experimental setup used to measure the designed filter.

3.1 Experiment Design

The goal of this thesis is to design a bandpass filter and experimentally validate its performance. To achieve this, two complementary experiments are proposed: a 2-port filter characterization and a 4-port qubit validation experiment.

3.1.1 2-Port Filter Characterization

In the first experiment seen in Fig. 3.1a, the transfer function of the bandpass filter is characterized using a 2-port measurement. The filter is placed between two CPW, allowing standard radio frequency (RF) S-parameter characterization. Under cryogenic conditions, reliable S_{11} and S_{22} measurements are not feasible due large attenuation and amplification as well es low signal to noise ratio (SNR). In a typical set up only a S_{21} measurement is possible. In addition, the required cryogenic components such as attenuators, filters, connectors, and amplifiers between the sample and VNA introduce static losses and systematic errors.
To account for this, a reference 2-port through line consisting only of a CPW line is measured in parallel. By comparing the transmission of the filter device to this reference, the intrinsic transfer function of the filter can be extracted while minimizing the influence of cryostat wiring and background attenuation.

3.1.2 4-Port Qubit Validation

To go beyond transfer-function validation and directly benchmark the filter's effectiveness, a second experiment based on a qubit device is introduced. This device consists of a standard transmon qubit coupled to a readout resonator and driven by two nominally identical drive lines as seen in Fig. 3.1b. One drive line contains the on-chip bandpass filter, while the other serves as an unfiltered reference.
This configuration enables the same qubit to be driven either through the filtered or the unfiltered signal path, providing a direct and controlled comparison of the filter's impact on qubit performance. By keeping the two drive lines and the chip layout symmetric, systematic errors from attenuation imbalance and coupling asymmetries

are minimized. Using the same qubit for both paths further eliminates uncertainties arising from qubit to qubit variation, fabrication variances, and qubit crosstalk.

The presence of an unfiltered drive line ensures that the qubit can still be operated and characterized even if the passband of the filter does not perfectly align with the qubit frequency, thereby increasing the robustness of the experiment.

The readout resonator is placed well outside the filter passband and is coupled to a CPW through line, enabling S_{21} measurements for qubit readout by probing the readout resonators frequency. This through line can also serve as a reference for the 2-port filter measurements, removing the need for a separate reference structure.

Together, a 2-port device enables the extraction of the filter transfer function, while a 4-port device allows for benchmarking the filter performance on a qubit and simultaneously provide a reference measurement, making this combination of devices particularly well suited for the experimental validation.

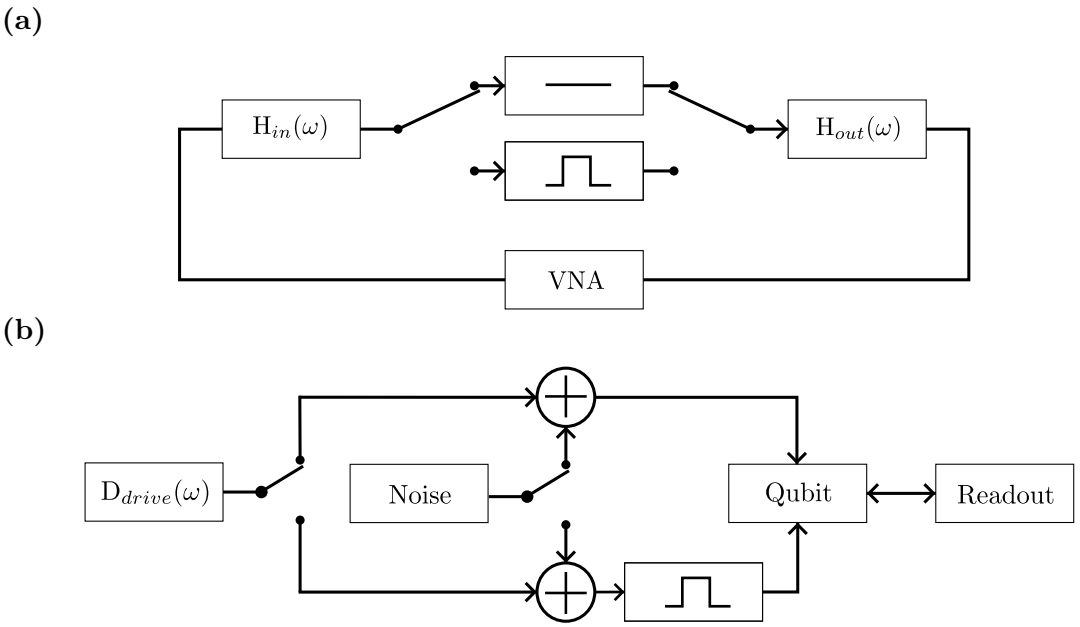

Figure 3.1: (a) Schematic of the proposed 2-port device to characterize the transfer function of the bandpass filter in a dilution refrigerator setup. A cryogenic switch allows toggling between a reference through line and the filter device, both measured using a VNA. The combined effect of cryostat wiring, filtering, attenuation, and amplification is described by the transfer functions $H_{\text{in}}(\omega)$ and $H_{\text{out}}(\omega)$. (b) Schematic of the proposed 4-port device used to benchmark the filter performance with a qubit. The qubit is driven by two capacitive coupled, nominally identical drive lines, allowing the drive signal $D_{\text{drive}}(\omega)$ to be applied either through the on-chip bandpass filter or through a standard driveline, with the option of additional noise injection. The readout consists of a readout resonator capacitive coupled to the qubit. In addition, the readout resonator is capacitive coupled to a CPW through line, enabling transmission-based measurements of the readout resonator frequency and thereby allowing determination of the qubit state.

3.2 Design flow

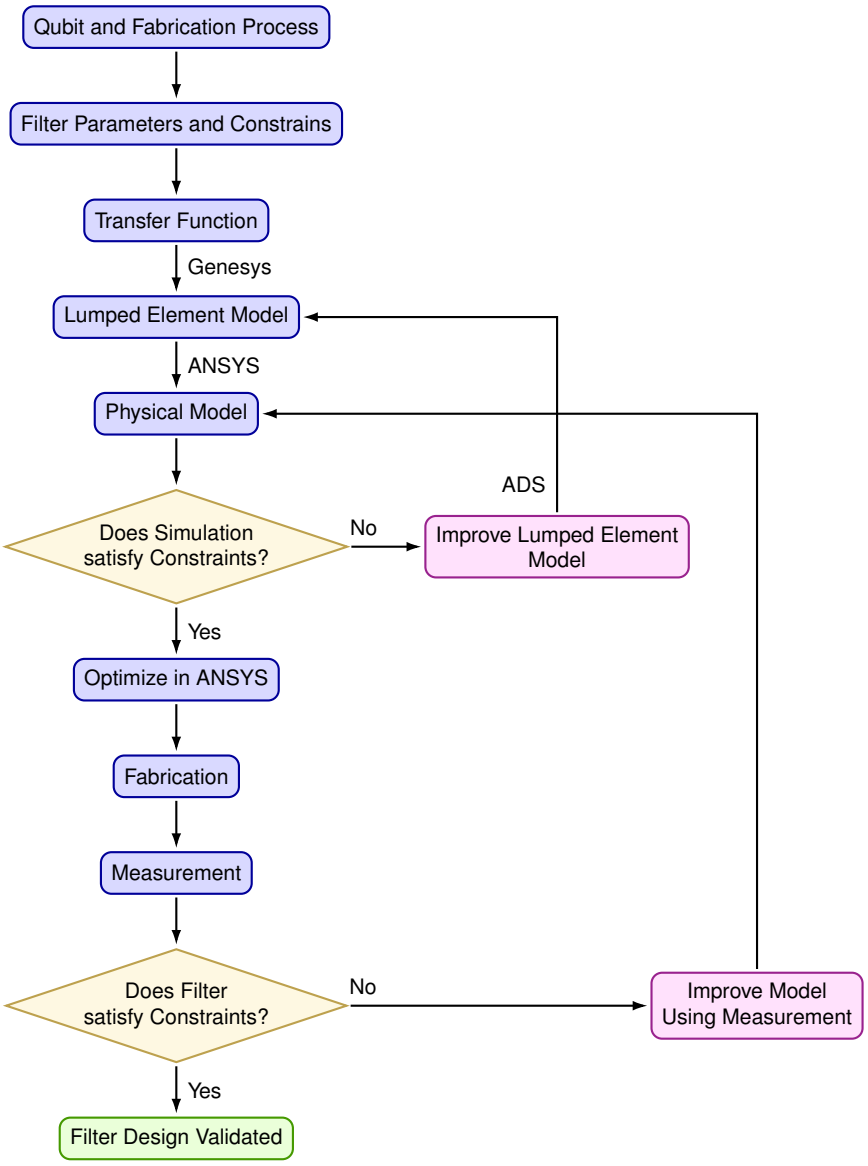

Figure 3.2: Modified design flow of a typical RF filter design, adapted for the development of a bandpass filter for superconducting applications in this thesis.

The design flow used for the bandpass filter, as shown in Fig. 3.2, follows the standard processes for the development of microwave filters [49]. In our case, this process has to be slightly modified to account for the additional constraints due to the cryogenic application. The goal of following the normal hardware design flow is to establish a fast and robust pipeline that allows design validation throughout the process.
In the first step, the key design parameters are defined. This ensures that the final design can be evaluated against all required specifications.

Next, a transfer function is derived and used to create an initial lumped element model. This simplified model enables quick simulations and efficient optimization of the filter response before proceeding to EM modeling.
From the optimized lumped model, a physical layout is generated, and an EM simulation is performed. The simulation results are compared to the design goals. Significant discrepancies indicate that the lumped element model lacks sufficient accuracy. In such cases, the model is refined to include more detailed parasitic or geometric effects, and the design flow is repeated from the lumped element stage. Although direct optimization of the EM model is possible, it is typically kept to a minimum due to the high computational cost.
If the simulated performance meets the design goals, the filter proceeds to fabrication. Fabrication is carried out on a wafer containing multiple devices in a cleanroom environment. The fabricated devices are subsequently measured and validated against the expected response.
Conventional room-temperature VNA characterization is not feasible, as the normal-state resistances of the superconducting structures are so large that the resulting attenuation exceeds the measurable range of the instrument. The associated losses effectively bury the signal in the noise floor, preventing any meaningful extraction of the transfer function. Therefore, the devices must be in the superconducting state to be properly characterized, which requires measurements at cryogenic temperatures. The chips are placed in a dilution refrigerator, making the validation step both complex and time-consuming. As a result, cryogenic measurements should be minimized whenever possible. This makes accurate simulation of the devices crucial in order to reduce the number of required fabrication and measurement cycles.
If measurement results deviate from the simulations, the EM model is refined using more accurate material parameters before re-entering the design loop.
This allows for the development of not only the target design, but also accurate models for future devices.
In the following, each step of the design flow is examined in detail, together with the techniques used. Goal is to induce the software and techniques used, while the concrete implementation and numerical realization of the filter are presented in Chapter 4.

3.2.1 Design Parameters

In the case of a bandpass filter, the design starts with defining the transfer function by specifying the key parameters: passband, stopband, attenuation at the cutoff frequency, passband ripple, insertion loss, and attenuation in the stopband. For the physical implementation, additional constraints arise from the device size and fabrication limitation. The fabrication process also introduces uncertainties that must be considered and limits the possible technologies to be used. All parameters will be grouped into hard and soft constraints to reflect their relative importance and the degree of flexibility in the design.
In this work, the goal is to realize an on-chip bandpass filter for driving the first and second transitions of a transmon qubit. The filter must also be compact, making a lumped element implementation the most suitable choice. Within the fabrica-

tion process described in Section 3.2.5, several inductive elements are available, of which meander inductors are particular interesting. While simple to fabricate, these structures provide predominantly geometric inductance with only a small kinetic inductance contribution, as they are formed from pure Al, which exhibits low kinetic inductance. Without modifying the process to include high-kinetic-inductance materials, such as granular aluminum or niobium-based compounds, their total inductance cannot be significantly increased without increasing their size for a constant conductors cross-section area.
In principle, the inductance can be enhanced by exploiting kinetic inductance effects in nanowires, where the reduced cross-section of the conductor leads to a stronger kinetic contribution. However, such approaches require well-controlled fabrication processes due to their strong sensitivity to geometric variations. Given the lack of prior characterization and the additional process development required, nanowire-based inductors were considered impractical for this design.
Furthermore, the chip footprint of meander inductors cannot be significantly reduced using spiral geometries. Spiral geometries are not purely planar and require conductor crossovers, which necessitate airbridges for proper routing. In the fabrication process used in this work, airbridges were not included, although they could in principle be implemented in an extended process. As a result, meander inductors remain the dominant contributor to the overall filter size.
Alternatively, JJ-based inductors such as superconducting nonlinear asymmetric inductive elements (SNAIL)s or RF-superconducting quantum interference device (SQUID)s offer high inductance in a compact area, but they require additional flux-bias lines to operate in the linear regime. Since the number of available lines in the cryostat is limited and each additional line introduces extra noise paths, meander inductors were chosen as the most practical option. For the capacitances, interdigital and parallel plate capacitors are viable options. The parallel plate capacitor is used, as it achieves higher capacitance, specifically through the use of hafnium oxide (HfO_x) with a high dielectric constant, than interdigital capacitors, while being compact in size, making it ideal for this application to offset the low inductances and achieve high impedances.
Using these design choices, the target specifications are implemented and translated in Sec. 4.1.1 initially into an ideal transfer function defined by the passband and stopband requirements. Since we are implementing a physical filter, additional practical constraints are applied to account for attenuation at the cutoff frequency, passband ripple, insertion loss, and stopband attenuation to find a real filter transfer function. On the fabrication side, lithographic linewidths and device dimensions determine the achievable inductance and capacitance values and thereby set the attainable cutoff frequencies. Process variations, including lithographic tolerances and dielectric uncertainties, introduce deviations in these parameters, which propagate to shifts in pole locations and bandwidth. Consequently, these variations ultimately limit the maximum filter order that can be reliably implemented within the given fabrication constraints.

3.2.2 Genesys

For the initial design stage, the software Genesys from Keysight is used [50]. The Filter Synthesizer tool in Genesys enables rapid synthesis of bandpass filters across various response types and orders. It automatically transforms and scales normalized low-pass prototype filters, as discussed in Section 2.3.1, to the desired center frequency and bandwidth.
Both the filter type and order can be specified, and multiple topology templates are available. The tool further allows circuit transformations and simplifications to obtain practical lumped element implementations.
Design parameters such as passband width, filter order, cutoff attenuation, and passband ripple are defined in the settings. Based on these specifications, the software directly generates a lumped element model, enabling rapid comparison of different architectures under given component constraints. In addition, sensitivity and optimization tools facilitate the analysis of parameter variations and tolerances, extending beyond purely analytical synthesis.

3.2.3 EM Simulation

The lumped element model derived in the previous step is mapped onto a physical layout. During component placement and ground plane design, a compact and symmetric layout strategy was adopted. A common ground plane is used for all components to reduce sensitivity to ground offset charges, which is particularly important due to the absence of airbridges in the fabrication process. Spacing to ground and spacing between components were kept consistent across all layouts in order to avoid introducing unnecessary geometric variability and to enable controlled comparisons between different designs. This design practice was applied uniformly throughout the entire work.
The resulting physical layout is simulated using an EM field solver. All EM simulations were performed using Ansys HFSS, an industry-standard tool for EM analysis. To reduce computational cost while preserving the relevant electromagnetic behavior, only a reduced subsystem was simulated. This subsystem consists of the filter structure and a limited section of the connected CPW, as shown in Fig. 3.3. The full CPW length and the chip pads used for wire bonding were removed from the model. Although the wire bonds do not constitute a perfectly matched 50 Ω CPW, their influence is neglected and they are assumed to behave as a well-matched 50 Ω transmission line with well-defined characteristics. This simplification allows the simulation to focus on the intrinsic filter response rather than parasitic effects arising from the packaging and interconnections, while significantly reducing the simulation domain size and runtime.
The superconducting metal layers were modeled as planar perfect electrical conductors, which is an appropriate approximation in the frequency and temperature regime of interest. The superconducting metal layers were represented as planar perfect electrical boundaries.
Two capacitor modeling approaches were employed. In the simplified approach, capacitors were implemented as lumped RLC impedance boundaries, where the capacitance is represented by a planar sheet with assigned capacitances. In the more

detailed approach, the parallel-plate capacitors were modeled as full 3D structures, where the top metal layer is vertically offset by the dielectric thickness. The dielectric material was modeled as a 3D box using the measured cryogenic properties of HfO_x, with a relative permittivity of $\varepsilon_r = 25$ with an estimated uncertainty of approximately 20% and a loss tangent of 2.51×10^{-3}. These material parameters were characterized by other members of the group prior to this work at cryogenic temperatures and are consistent with values reported in the literature [51, 52]. However, subsequent fabrication and additional measurements raised questions about this value and reduced confidence in this estimate. In regions where the top superconducting layer extends over the ground superconducting layer without an intermediate dielectric, a perfect electrical boundary was introduced to represent the electrical connection between the two layers and to account for the 3D structure of the parallel-plate capacitors.
Wave ports, with dimensions chosen according to ANSYS, Inc. [53, 54], were placed sufficiently far from the active region to minimize their influence, while remaining close enough to keep the simulation domain compact. Wave ports were selected because they enable de-embedding of the solution, thereby reducing phase contributions arising from the lead lengths. The reduced domain size significantly decreases the total simulation time. The initial mesh for the signal line was set to a length-based value of 8 µm, chosen from prior experience as a balance between accuracy and computational complexity.
To improve accuracy, the detailed mesh settings were adjusted to allow mixed-order elements. The frequency sweep was configured in "fast" mode to reduce total runtime.

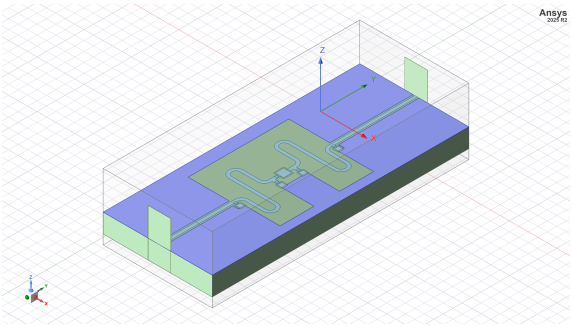

Figure 3.3: Subsection model of the physical EM simulation of the designed pass-band filter containing the lumped filter and partly CPW . The horizontal rectangles represents the wave port of the incoming signal.

3.2.4 ADS

For more advanced lumped element modeling, Advanced Design System (ADS) was used due to its flexibility and support for user defined components. Since both ADS and Genesys belong to the same software ecosystem, migration between tools is seamless. To extract parameters for complex models, S-parameters obtained from the EM simulations were embedded into ADS. The simulated behavior was then used to fit a lumped element network over a selected frequency range.

The fitting process minimized the error between simulated and model S-parameters. Equal weighting was applied to all optimization goals since no single parameter required prioritization. A good initial seed was essential for convergence, obtained either manually or through a random walk optimization routine. The model was then refined using gradient descent until no further improvement was observed, maximizing the likelihood of reaching the global minimum.

3.2.5 Fabrication

Two device architectures were fabricated: the 2-port device containing only the designed filter, and a 4-port qubit chip. The 4-port chip is a single qubit design used in the Quantum Computing group at Chalmers, featuring two drive lines. Only one drive line includes the on-chip filter.
The chip fabrication was carried out using the standard multi-wafer process employed by the Quantum Computing group at Chalmers, without airbridges and with the addition of an HfO_x dielectric step. The high-level overview of the available layers and their deposition order is as follows:

1. 160 nm Al ground plane deposited by physical vapor deposition (PVD),
2. 40 nm HfO_x dielectric deposited by atomic layer deposition (ALD),
3. 260 nm Al top layer deposited by PVD,
4. JJ fabrication following a similar procedure described in [55],
5. 350 nm Al patch layer deposited by PVD after argon (Ar) ion milling.

The manufacturing itself was performed by other group members and is therefore not discussed in further detail here.

3.3 Experimental Setup

Two chips were measured at cryogenic temperatures to validate the filter design and quantify its performance on the drive line.

3.3.1 Cryostat Setup

All measurements were performed in a Bluefors LD 250 Gen. 1 dilution refrigerator, referred to as *Lumi* in the Quantum Computing group at Chalmers. The base temperature during operation was approximately 10 mK, providing a low-noise thermal environment. The wiring and filtering configuration used in the experiment is shown in Fig. 3.4 following typical fridge setup [56]. The drive lines of the 4-port device were directly connected via the XY lines, while a Subminiature SP6T cold switch [57] was used to switch between the 2-port and 4-port S_{21} measurements.
All input lines: In, XY drive, and XY drive (Filter) contained distributed attenuation to suppress thermal noise originating from higher temperature stages. In addition, 8 GHz low-pass filters were placed at the 10 mK stage to attenuate infrared radiation. The two drive lines were configured identically in order to ensure a symmetric experimental setup. Since the drive lines are directly coupled to the

qubit, additional care was taken to provide sufficient attenuation to minimize the effective thermal noise seen by the qubit [11].
The readout line (Out) consists of two double isolator [58] surrounded by an low pass and high pass filter resulting in an effective passband from 3.9 to 8 GHz. In addition to the HEMT amplifier [59] at the 3 K stage, two room-temperature amplifiers [60] were placed outside the dilution refrigerator. Together, these components define the accessible measurement bandwidth, which spans 3.9–8.0 GHz for all experiments. For the 2-port device, a Keysight VNA was used to measure S_{21}. For the 4-port qubit chip, an Intermodulation Products Presto-16-QC-DC arbitrary waveform generator (AWG) and readout module [61] were installed for control and measurement.

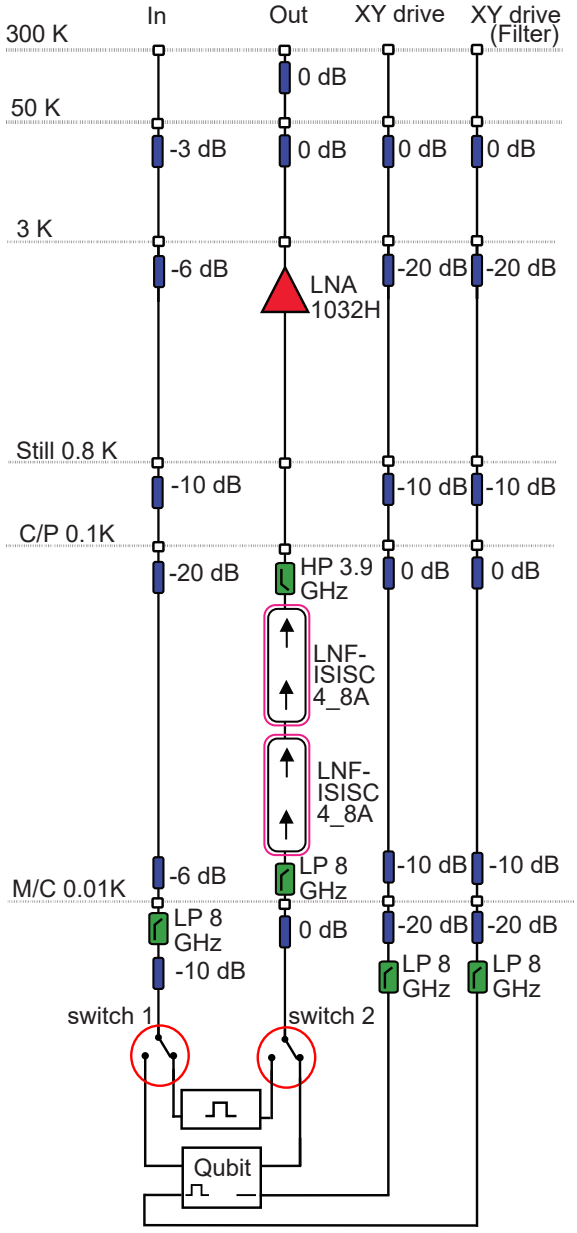

Figure 3.4: Schematic wiring diagram of the dilution refrigerator *Lumi* used for the measurements, including the 2-port and 4-port devices outlined in Section 3.1 with great detail.

3.3.2 Measurement and Calibration

3.3.2.1 2-Port Device

A standard VNA S_{21} transmission measurement was performed on the 2-port device. Since the network is passive and reciprocal, the measurement was performed in one direction only. The same procedure was repeated using the readout line of the 4-port chip. The readout resonator for the 4-port device lies around 6.5 GHz, which is outside the passband of the filter. This line effectively provides a through reference for the 2-port device.

3.3.2.2 4-Port Device

To evaluate how effectively the filter suppresses noise entering the qubit, a single qubit chip with two drive lines was used. Only one drive line contains the on-chip filter. T_1 and T_2 measurements are performed under different applied noise levels to quantify the impact of the filter on the qubit coherence.
The calibration and tune up procedure is summarized below; detailed descriptions follow Naghiloo [62].

1. **Resonator Spectroscopy.** The readout resonator is swept in frequency for different power levels to identify the resonator "punshout" and the Lamb shift. At low power, the sweep determines the optimal readout amplitude that keeps the qubit in the dispersive regime and maximizes the SNR.
2. **Qubit Spectroscopy** A frequency sweep drive tone is applied while continuously monitoring the resonator. At the qubit transition, the resonator frequency shifts, providing an initial estimate of the qubit frequency.
3. **Rabi Calibration** A fixed length drive π-pulse is applied and repeated for different amplitudes. The resulting Rabi oscillations are fitted to calibrate the π-pulse amplitude.
4. **Ramsey Interferometry** Two $\pi/2$ pulses separated by a delay τ are applied. Repeating the sequence with slightly detuned pulses yields Ramsey fringes [63], which oscillate at the detuning frequency and refine the estimate of the qubit frequency.
5. T_1 **Measurement** A standard T_1 experiment is performed by preparing the qubit in $|1\rangle$ using a π-pulse, allowing free evolution for a delay τ, and reading out the population decay.
6. T_2 **Echo Measurement** For the T_2 echo sequence, two $\pi/2$ pulses are applied with a variable delay τ, and a refocusing π-pulse is inserted at $\tau/2$ to cancel out slow fluctuations and low frequency noise. Effectively acting as a high pass filter. [42].

3.4 Thermal Model

To quantify the filters effect on the thermal bath, simulation of its effect is necessary. To model the thermal bath experienced by the qubit through the drive line,

a cascaded noise model following [11] is employed. Each temperature stage of the dilution refrigerator is treated as an independent thermal bath that generates noise according to the Bose–Einstein distribution

$$n_{\mathrm{BE}}(T,\omega) = \frac{1}{e^{\frac{\hbar\omega}{k_B T}} - 1}.$$

The corresponding blackbody radiation of an one-dimensional cable is described as Johnson–Nyquist noise,

$$S_{\mathrm{V}}^{\mathrm{th}}(T,\omega) = \int_{-\infty}^{\infty} dt\, \langle \delta V(0)\, \delta V(t) \rangle = 2R\hbar\omega n_{\mathrm{BE}}(T,\omega),$$

for a resistor of characteristic impedance $R = 1$ and voltage fluctuations $\delta V(t)$.
Assuming perfect thermalization at each stage and point-like attenuation, the full cryogenic wiring can be represented by the equivalent circuit shown in Fig. 3.5. Losses of the wiring itself are ignored. In this description, noise emitted by higher-temperature stages is progressively attenuated by the colder stages before reaching the qubit, leading to an effective mixed thermal bath.
The drive transfer function $H(\omega)$ is neglected, and the attenuators are modeled as ideal components with constant attenuation $A(\omega) = A$. The filters are included as an additional frequency-dependent attenuation, such that the total attenuation becomes

$$A(\omega) = A_{\mathrm{att.}} + A_{\mathrm{filter}}(\omega).$$

This allows the spectral shaping of the thermal noise reaching the qubit to be evaluated.
Despite its simplicity, this model provides a useful tool for cryogenic engineering: it highlights the trade-off between minimizing thermal noise at the qubit and limiting attenuation, especially at the coldest temperature stages where cooling power is most limited. The optimal operating point is therefore determined by the balance between achievable noise suppression and acceptable dissipation in the refrigerator.

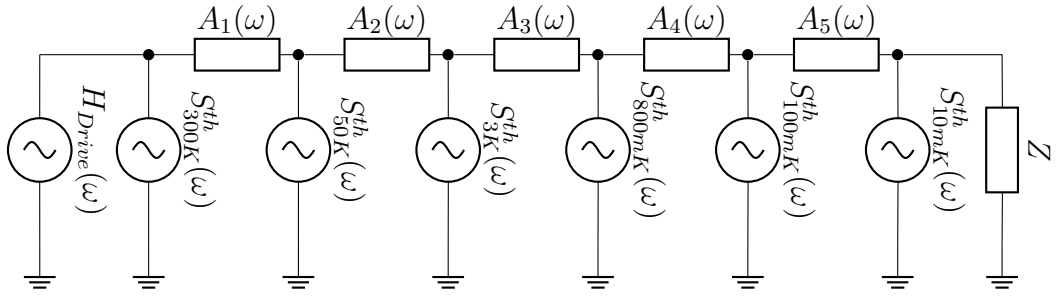

Figure 3.5: Simplified thermal model of a drive line, where the room-temperature drive source $H_{\mathrm{Drive}}(\omega)$ is coupled via frequency-dependent attenuators $A(\omega)$ to a load Z, such as a qubit. At each thermal stage, additive Johnson–Nyquist noise $S_T^{\mathrm{th}}(\omega)$ corresponding to the local thermalized temperature T is introduced between the attenuators.

4
Results and Discussion

In this section, the synthesis of the filter is examined first, following the design flow shown in Fig. 3.2. Afterwards, the filter measurements are evaluated; however, since the filter performance could not be validated, potential causes for the observed behavior are subsequently discussed.

4.1 Filter Synthesis

In this first part, the synthesis of a the filter from parameters to a final physical design is analyzed.

4.1.1 Filter Parameters

Starting by examining the filter parameters required for the intended application. The proof of concept design targets a fixed frequency transmon qubit at 5 GHz with an anharmonicity of 200 MHz. The filter must reliably drive the first two transitions, with the shortest considered control pulse being a 20 ns raised cosine pulse. To estimate the necessary bandwidth (BW), an ideal bandpass filter simulation is used to quantify leakage and distortion introduced by the filter. As shown in Fig. 4.1, a BW of 200 MHz is sufficient to keep both effects negligible for non-rectangular drive pulses. The simulation details are provided in the Appendix A.
Next, the resulting design parameters are summarized in Tab. 4.1 , which include manufacturing uncertainties of 5% in qubit frequency and 15% in anharmonicity. Using the worst case approximation, the required passband is 4.42–5.35 GHz to satisfy the drive requirements, which translates into an ideal transfer function shown in Fig. 4.2. Since the control electronics typically used, such as Qblox, rely on upconversion of an AWG signal and use the lower sideband for control, it is advantageous for the filter to have a sharp upper cutoff.
In the next step, the ideal transfer function is translated into a realizable filter function by specifying additional constraints, which are summarized in Tab. 4.2. For the filter, the passband return loss should remain above 7 dB. In a lossless filter, this directly implies a maximum passband ripple of approximately -0.77 dB. Such ripple can in principle be compensated by predistortion of the drive signal.
Achieving a stopband attenuation below -40 dB is challenging in practice due to stray coupling paths and parasitic effects. Therefore, the stopband attenuation is treated as a soft design objective. The intermediate frequency range marking the transition from passband to stopband should ideally be as narrow as possible, cor-

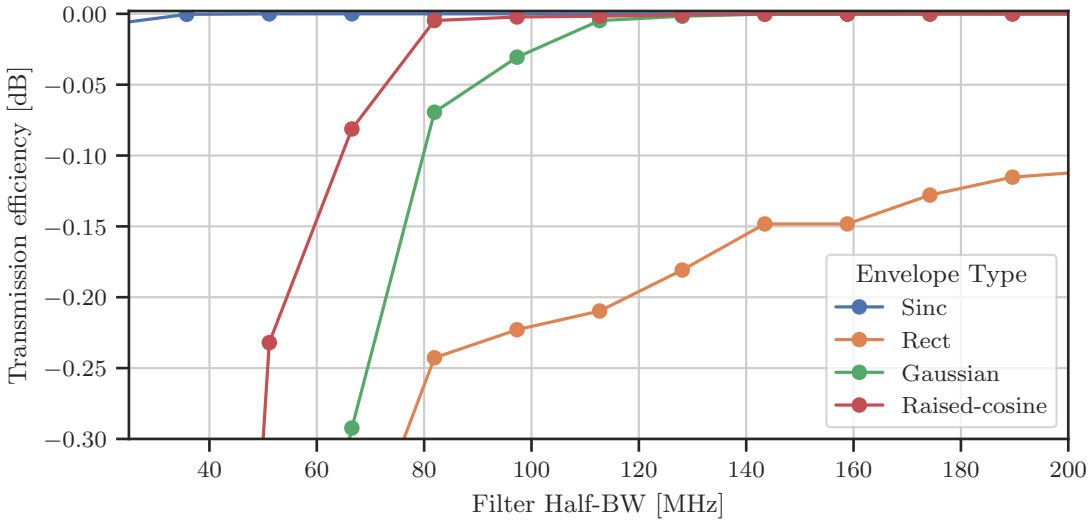

Figure 4.1: Transmission efficiency of an exemplary 5 GHz, 20 ns drive pulse as a function of the half bandwidth of an ideal bandpass filter centered at 5 GHz, for various envelope functions applied to the drive pulse.

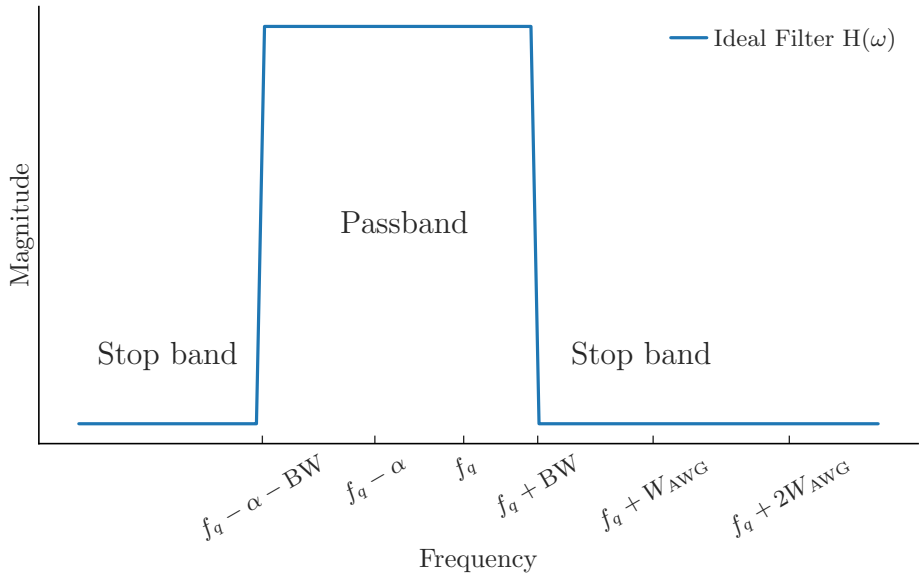

Figure 4.2: Ideal transfer function of a bandpass filter for the drive line of a superconducting qubit, designed to address the first and second transitions for the parameters given in Table 4.1.

responding to a sharp cutoff. However, since this transition is primarily determined by the filter type, stopband attenuation, and filter order, it is also treated as a soft constraint.

The filter range specifies the frequency interval over which the filter behavior is evaluated, and thereby limits the considered stopband width. In addition, physical compactness is treated as a soft objective to support scalable integration. To limit complexity, the filter order is intentionally kept low.

Further constraints arise from the physical implementation of the inductors and capacitors. Lumped elements implementations are selected as discussed in Sec. 3.2.1. Considering chip size, fabrication constraints, and uncertainties, the parameters ranges for parallel plate capacitors and meander inductors are summarized in Tab. 4.3. The dielectric thickness is fixed and not tunable as it is a whole wafer parameter, therefore the capacitor size is the main tuning factor. A meander line thickness of 16 µm is chosen to reduce sensitivity to over etching while keeping the footprint small. Together, these considerations define the complete constraint set for the filter implementation.

Table 4.1: Parameter overview of the qubit and bandpass filter requirements for qubit drive operations.

Parameter	**Symbol**	**Value**	**Error (%)**	**Unit**
Qubit frequency	f_q	5.00	5	GHz
Frequency shift (mixer)	W_{AWG}	400	–	MHz
Qubit anharmonicity	α_q	200	10	MHz
Bandwidth	BW	200	–	MHz

Table 4.2: Overview of the bandpass filter requirements, categorized into soft and hard constraints.

Constraint Type	**Symbol**	**Value**	**Unit**
Hard Constraints			
Order of the filter	N	2	–
Passband ripple	A_{p}	-0.77	dB
Passband range	f_{p}	4.42–5.35	GHz
Number of components	N_{c}	few	–
Soft Constraints			
Return Loss	A_{RL}	7	dB
Attenuation in stopband	A_{s}	-20	dB
Roll-off width	Δf_{r}	1.5	GHz
Full filter working range	f_{range}	2–8	GHz

Table 4.3: Overview of parameters and ranges of capacitances and inductances based on the chosen fabrication process.

Component	Parameter	Value	Error	Unit
Capacitor				
Oxide type: HfO_x	ϵ_r	25	10%	–
Oxide thickness	t_{ox}	40	±2	nm
Capacitor side length	a_{cap}	15–90	±1	µm
Capacitance range	C_{cap}	1.25–45.16	±0.18 - 5.10	pF
Inductor				
Dimensional range	d_{L}	16	±1	µm
Inductance range	L	100–600	–	pH

4.1.2 Initial model

The only viable candidate topologies after analyzing all options in Genesys include Chebyshev networks with shunt capacitors and Cauer (elliptic) variants. To minimize chip area, we restrict the design to the lowest feasible order and select the Chebyshev topology with a tubular layout. This topology offers robustness to parameter uncertainty while keeping the number of components low.

Next, a physical layout is generated by placing the parallel plate capacitors and meander inductors according to the lumped values.

To translate the parameters defined in Sec. 4.1.1 into an initial design, low-order filter prototypes are considered with emphasis on the passive element constraints summarized in Tab. 4.3. The synthesis tool in Genesys provides a range of filter topologies. Some of these allow the inductance values to be fixed while the corresponding capacitances are calculated accordingly. This functionality relies on additional impedance-transforming elements within the topology, which introduce extra components but allow the inductors to be set to a predefined value.

Fixing the inductance is advantageous in the present design, since capacitor values can be conveniently adjusted through their physical area, whereas modifying inductors requires changing the conductor geometry and therefore the layout. Since accurate characterization of the inductances has not been done, topologies that permit fixed inductance values are preferred.

After evaluating the available topologies in Genesys under the imposed component constraints, only a limited number of viable candidates remained. Most available topologies require inductance values significantly larger than those achievable with the available inductors. The remaining candidates include Chebyshev networks with shunt capacitors and Cauer (elliptic) variants. To minimize chip area, the design is restricted to the lowest feasible filter order, and a Chebyshev topology with a tubular layout is selected. This topology offers good robustness to parameter uncertainties while keeping the number of components low.

For the inductor model, the meander inductance is fixed to 0.483 nH, obtained from an initial inductor analysis in HFSS (see Appendix B for details). Using this

value, the Genesys synthesizer generates the initial lumped element design shown in Fig. 4.3, with component values listed in Tab. 4.4.

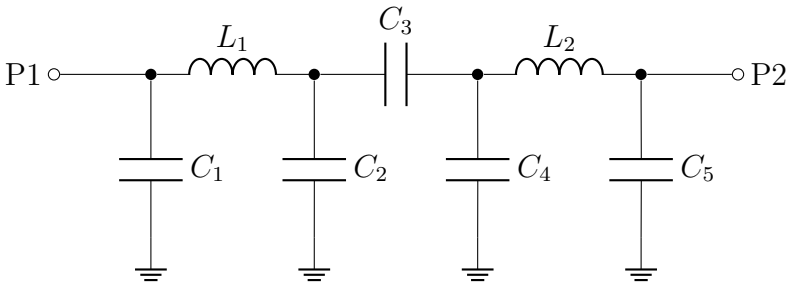

Figure 4.3: Lumped element model of a second-order Chebyshev bandpass filter using a tubular topology synthesized in Genesys.

Next, a physical layout is generated by placing the parallel-plate capacitors and meander inductors according to the synthesized lumped element values.

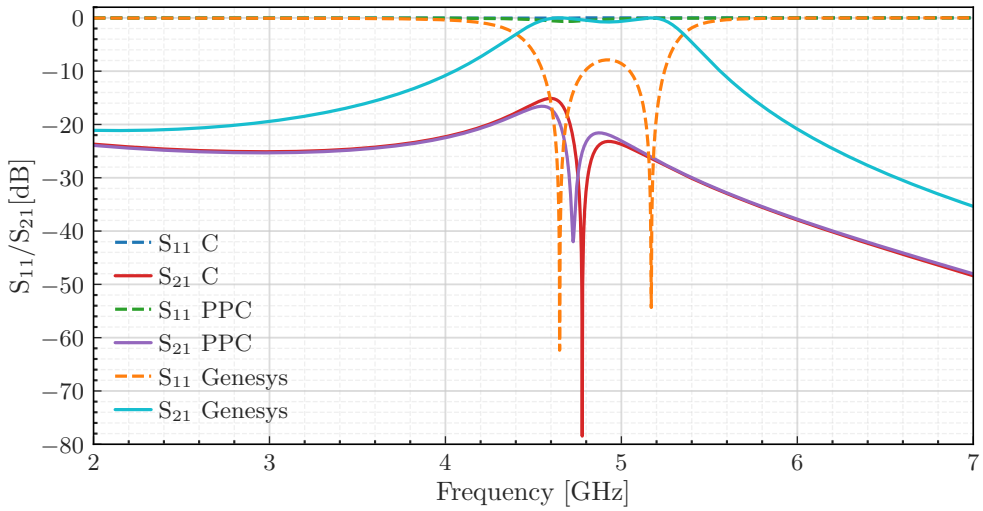

Figure 4.4: Filter transfer function comparison of the initial designs of the lumped element model (Genesys) created in Genesys and the corresponding physical model in Ansys, using either an ideal capacitor model (C) or a 3D parallel-plate capacitor model (PPC).

When examining the results of the EM simulation for the physical model, seen in Fig. 4.4, it lacks a well defined passband behavior. In comparison to the lumped element simulation, it appears to suffer from a notable frequency mismatch. This mismatch causes the resonant structures to be destructive, leading to this unexpected behavior with a pole at $\approx 4.7\,\mathrm{GHz}$. This clearly indicates the need to further refine the lumped element model.

Table 4.4: Dimensions and corresponding capacitance values utilized for the initial physical filter design.

Parameter Set	Element	Value	Error	Unit
Lumped Element Design				
Capacitor values	$C_1 = C_5$	3.90	–	pF
	$C_2 = C_4$	3.66		
	C_3	1.59		
Physical Design				
Capacitor values	$C_1 = C_5$	4.06	±0.50	pF
	$C_2 = C_4$	3.77	±0.47	
	C_3	1.61	±0.22	
Capacitor physical sizes	$a_1 = a_5$	27	±1	µm
	$a_2 = a_4$	26		
	a_3	17		

4.1.3 Inductor S-parameters Model

To refine the model accuracy, the inductor was simulated individually in HFSS, and its full S-parameter response was extracted, as seen in Fig. 4.5. The simulation setup was kept as described in Sec. 3.2.4. Using the measured S-matrix for the fixed meander inductor and retaining ideal capacitors, the synthesis of the filter, as in Sec. 4.1.2, is repeated. The updated parameters are listed in Tab. 4.5.
The corresponding full-field validation shows that this first iteration of the improved lumped element model does not substantially outperform the initial ideal model, as seen in Fig. 4.6. The simulated response exhibits a passband attenuation of approximately -10 dB and a narrowed transmission window around 3.9–4.1 GHz, indicating a clear mismatch between the predicted and actual behavior. In other words, incorporating only the inductor S-parameters is insufficient to recover the intended passband characteristics. This highlights that further refinement is required, and the next step is to replace the ideal capacitor representation with a more realistic model.

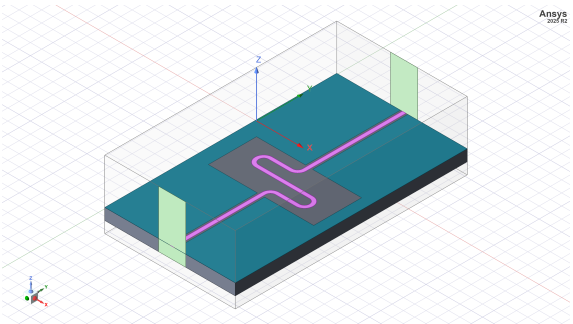

Figure 4.5: Physical model of the inductor used to perform S-parameter extraction in Ansys.

Table 4.5: Dimensions and corresponding capacitance values utilized for the first iterative physical filter design.

Parameter Set	Element	Value	Error	Unit
Lumped Element Design				
Capacitor values	$C_1 = C_5$ $C_2 = C_4$ C_3	4.32 5.73 4.69	–	pF
Physical Design				
Capacitor values	$C_1 = C_5$ $C_2 = C_4$ C_3	4.37 6.07 4.69	±0.54 ±0.73 ±0.57	pF
Capacitor physical sizes	$a_1 = a_5$ $a_2 = a_4$ a_3	28 33 29	±1	µm

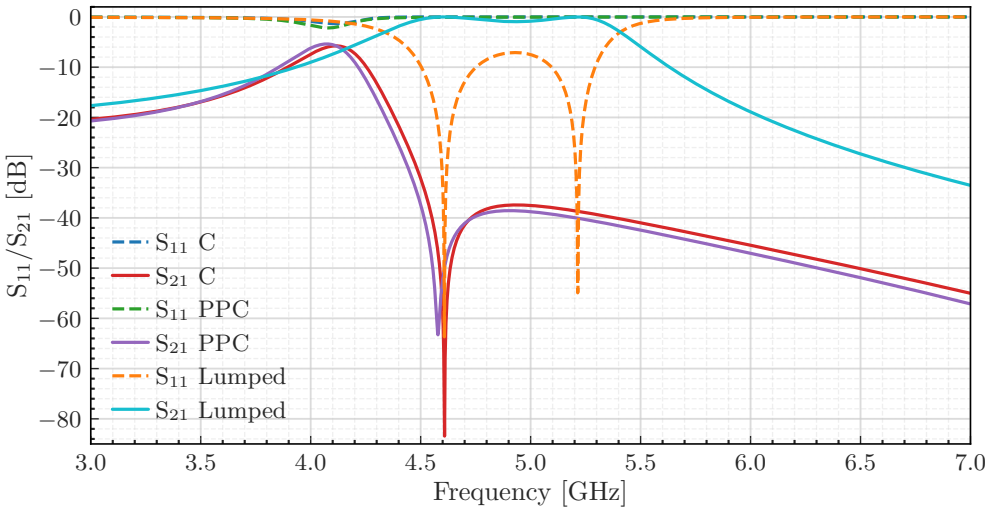

Figure 4.6: Filter transfer function comparison of the first iterative designs of the lumped element model (Lumped) and the corresponding physical model in Ansys, using either an ideal capacitor model (C) or a 3D parallel-plate capacitor model (PPC).

4.1.4 RLC Capacitor model

Since the simple lumped element model does not provide sufficient accuracy, the capacitor representation is refined using an RLC based approach. Series capacitor geometries are simulated over a range of sizes, as seen in Fig. 4.7, and, in parallel, modeled using lumped RLC boundaries in HFSS for validation. Here, for the capacitors in parallel, the main differentiation is by the proximity of the ground surrounding the capacitor. An equivalent RLC circuit, seen in Fig. 4.8, is fitted in ADS by minimizing the S-parameter error across the frequency band of interest. A subset of capacitor sizes is used for fitting, and the remaining geometries serve as interpolation tests. The extracted parameters are listed in Tab. 4.6. The details of the fitting can be found in Appendix C.
For parallel capacitors to ground, the stray capacitances are removed in the model, seen in Fig. 4.9, and the same fitting procedure is applied. As shown in Tab. 4.7, the extracted stray inductances vary considerably, highlighting the importance of geometry dependent parasitics.

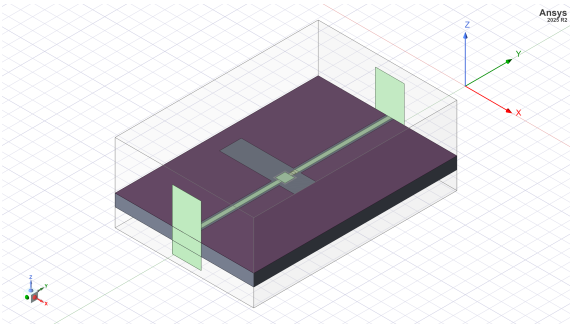

Figure 4.7: Physical model of the capacitor in series with a CPW used to perform S-parameter extraction in Ansys and fitting to a lumped element model.

Table 4.6: Extracted model parameters for the capacitor models of the parallel and two series capacitors. The distinction between C_1 and C_2 originates from the location of the ground plane.

Capacitor Model	C_s	R_s	L_s	C_g
Series Model – Capacitor C3				
C3 (Series)	33.2 fF	87.0 nΩ	98.9 pH	4.93 fF
Parallel Models – Capacitors C1 and C2				
C1 (Parallel)	12.9 fF	283 nΩ	43.0 pH	–
C2 (Parallel)	11.5 fF	571 nΩ	50.1 pH	–

With improved models for both inductors and capacitors, the passband is optimized directly in ADS rather than relying on the Genesys synthesizer. The optimized lumped network is then translated to a physical layout and simulated in HFSS. The EM simulation exhibits a passband around 4.45–4.75 GHz with minimal ripple.

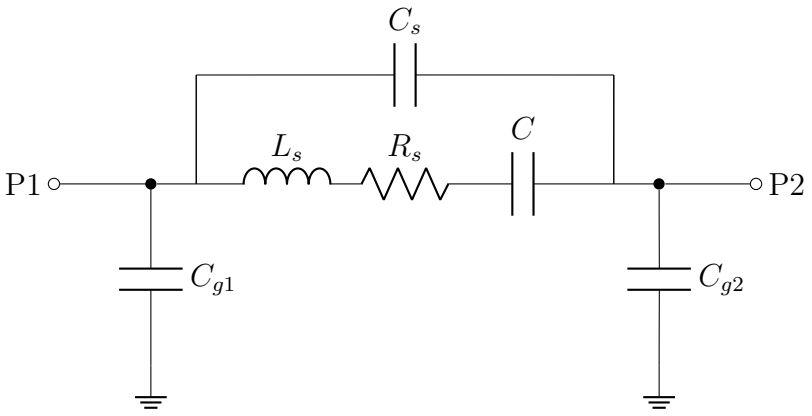

Figure 4.8: Lumped element model of the capacitor coupling two CPWs, used for fitting to the simulated S-parameters.

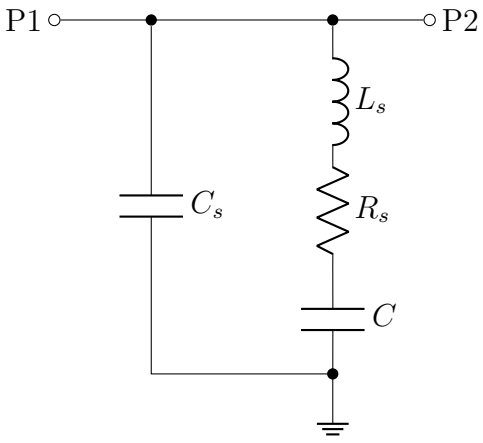

Figure 4.9: Lumped element model of the capacitor connecting a CPW to ground, used for fitting to the simulated S-parameters.

Table 4.7: Dimensions and corresponding capacitance values utilized for the second iterative physical filter design.

Parameter Set	Element	Value	Error	Unit
Lumped Element Design				
Capacitor values	$C_1 = C_5$	3.23	–	pF
	$C_2 = C_4$	4.88		
	C_3	7.48		
Physical Design				
Capacitor values	$C_1 = C_5$	2.95	±0.38	pF
	$C_2 = C_4$	5.02	±0.61	
	C_3	7.98	±0.95	
Capacitor physical sizes	$a_1 = a_5$	23	±1	µm
	$a_2 = a_4$	30		
	a_3	38		

However, discrepancies remain between the physical parallel plate capacitors and their ideal RLC boundary representations. While the predicted response improves relative to Fig. 4.10, the predicted passband has improved; nonetheless, it still lacks sufficient accuracy.

4.1.5 Physical layout optimization

Due to time constraints, further refinement of the lumped element model was replaced by direct optimization of the physical layout in Ansys. An automated optimization using lumped element capacitor boundaries was not feasible, as earlier results demonstrated that geometric stray inductances play a critical role in determining the filter response. This limitation is illustrated in Fig. 4.11. For the initial design, the capacitive values of the boundary conditions are changed to the values listed in Tab. 4.5. The results are then compared to the EM simulation shown in Fig. 4.5, where the model reflects the physical dimensions of the capacitors. The initial model predicts a shifted passband to some extent, but other key features are not captured correctly. In particular, the mismatch induced dip is offset by approximately 500 MHz, and the passband attenuation is overestimated by nearly 5 dB. This indicates that the boundary condition capacitor model remains insufficient to accurately represent the physical capacitor behavior.
Consequently, a manual and intuition guided optimization strategy was adopted. Insight from the simplified RLC boundary model was used to identify dominant parameter dependencies, as seen in Fig. 4.12: increasing C_1 lowers the passband center frequency, increasing C_3 reduces the passband width, and C_2 primarily controls the passband ripple. Using these relationships, the capacitor geometries were iteratively adjusted in the physical layout until the constraints defined in Sec. 4.1.1 were met. The resulting transfer function and extracted parameters are shown in Fig. 4.13.
This design marks a good compromise between the competing constraints summa-

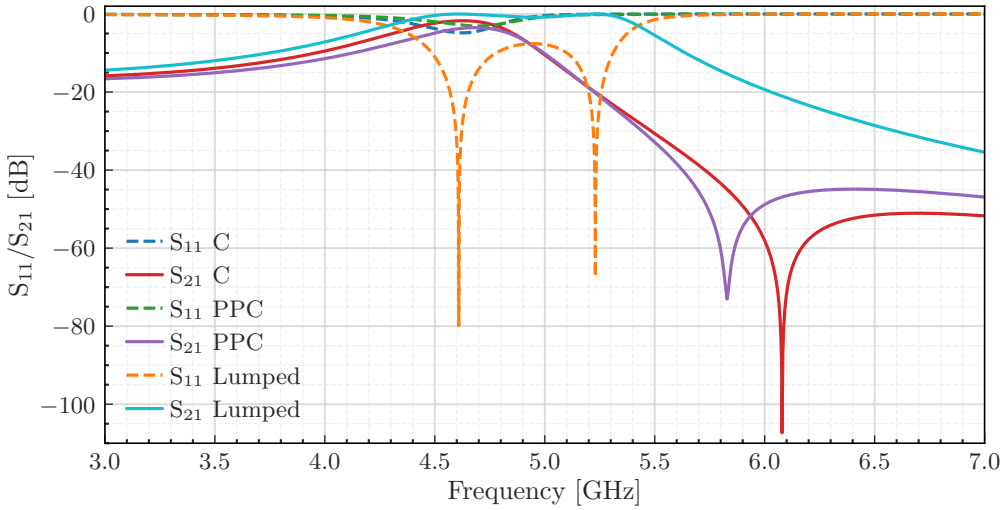

Figure 4.10: Filter transfer function comparison of the second iterative designs of the lumped element model (Lumped) and the corresponding physical model in Ansys, using either an ideal capacitor model (C) or a 3D parallel-plate capacitor model (PPC).

rized in Tab. 4.2. The achieved passband spans approximately 4.27–5.40 GHz, while the passband ripple reaches −0.77 dB, at the specified limit. The lower band roll off remains relatively shallow, whereas the upper band roll off is significantly steeper, which aligns with the intended design priorities.

Compared to the lumped RLC boundary model, the 3D parallel plate capacitor implementation exhibits a slightly shifted passband and increased ripple. This difference arises from dielectric losses included in the 3D capacitor model via the loss tangent, and therefore the EM simulation is expected to provide a more realistic prediction of the fabricated device performance.

Table 4.8: Dimensions and corresponding capacitance values utilized for the final optimized physical filter design.

Parameter Set	Element	Value	Error	Unit
Physical Design				
Capacitor values	$C_1 = C_5$	2.95	±0.38	pF
	$C_2 = C_4$	3.32	±0.41	
	C_3	10.79	±1.26	
Capacitor physical sizes	$a_1 = a_5$	23	±1	µm
	$a_2 = a_4$	24		
	a_3	44		

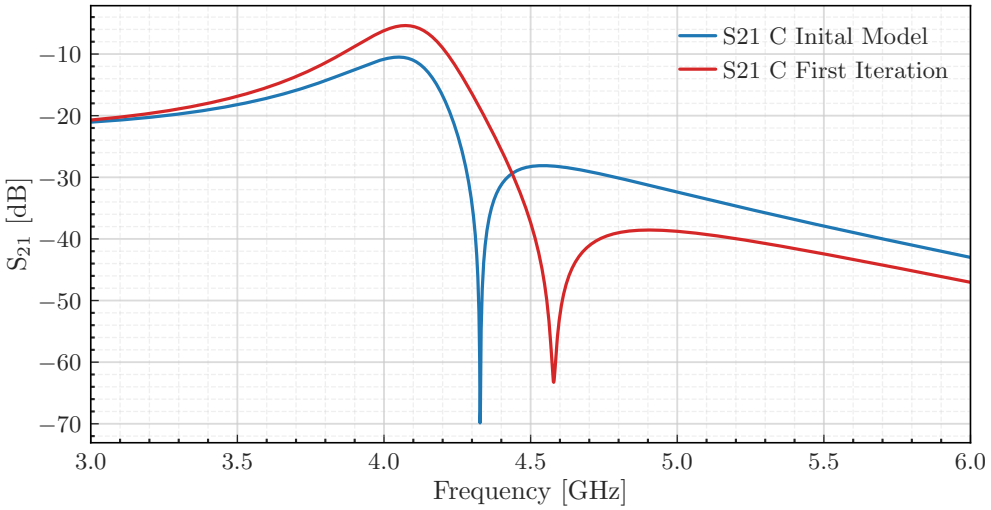

Figure 4.11: Comparison of the filter transfer functions using an ideal capacitor model (C). The first curve corresponds to the first iteration physical model in Ansys, reflecting the accurate physical dimensions of the capacitors as in Fig. 4.6. The second curve corresponds to the initial design with the capacitance values adjusted to match the first iteration design parameters listed in Table 4.5.

4.1.6 Error Analysis

To investigate the stability of the design, an error analysis was performed. When examining the tolerances in Tab. 4.3, the dominant source of uncertainty originates from variations in the dielectric constant, which directly affect the capacitance values. To quantify this effect, the final design was simulated while sweeping the dielectric constant of the HfO_x layer.
The results, shown in Fig. 4.14, demonstrate that the design remains functional for dielectric variations between $-5.5\,\%$ and $+1\,\%$. Beyond this range, the passband no longer satisfies the filter constraints, primarily due to a shift in the center frequency. Further optimization would be required to achieve a more even error robustness, as well as a wider passband to ensure that the required passband is met. Since this work serves as a proof of concept, this step was not pursued further. Additional process development is necessary to reduce the parameter variance and is left for ongoing and future work. Instead, to compensate for this uncertainty, multiple variants of the design were fabricated with different assumed dielectric constants for the HfO_x layer.

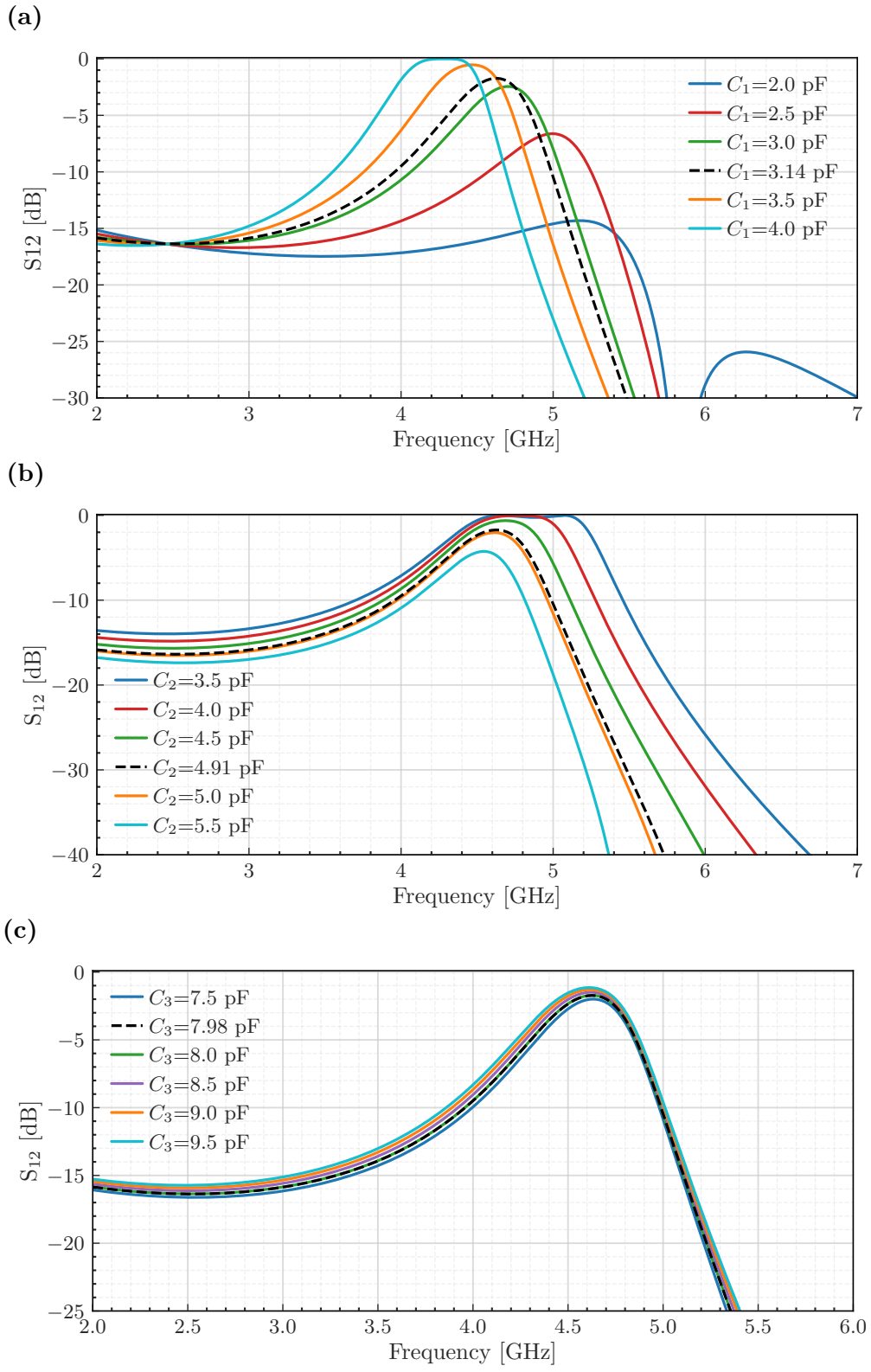

Figure 4.12: Empirical analysis of the influence of capacitor values on the filter response for the second iteration model. The reference design (black dashed line) uses $C_1 = C_5 = 3.14\,\text{pF}$, $C_2 = C_4 = 4.91\,\text{pF}$, and $C_3 = 7.98\,\text{pF}$. The filter response is shown for variations of (a) $C_1 = C_5$, (b) $C_2 = C_4$, and (c) C_3.

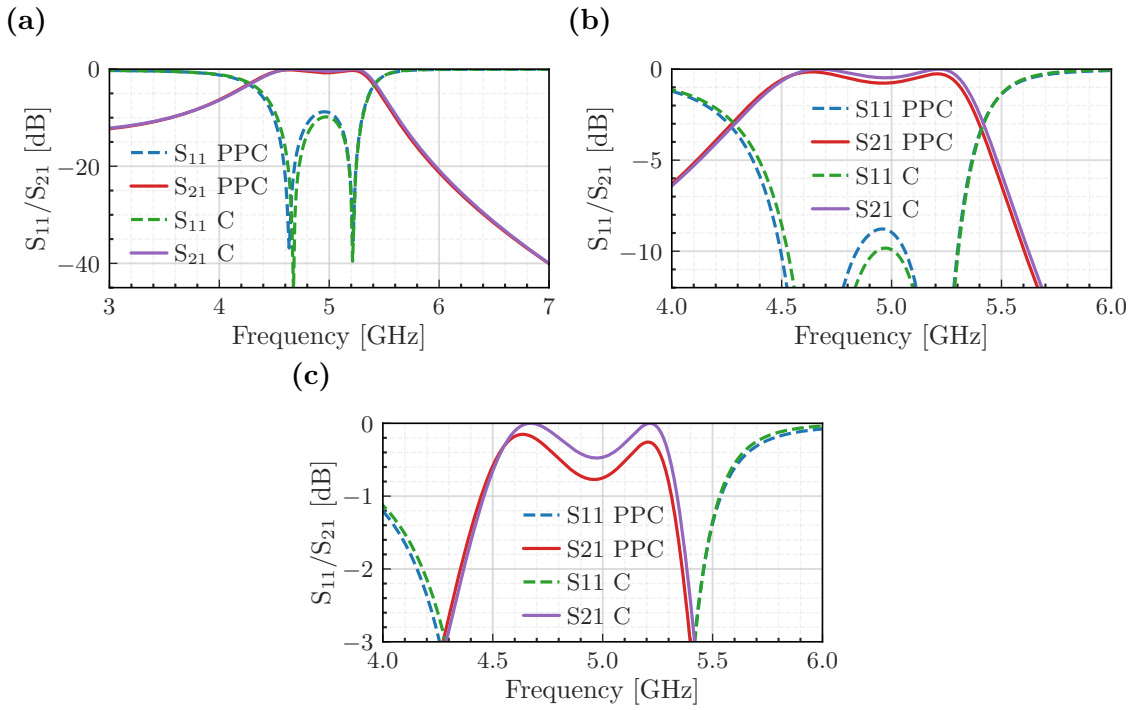

Figure 4.13: Filter transfer function of the empirically optimized final design obtained from the physical model in Ansys, using either an ideal capacitor model (C) or a 3D parallel-plate capacitor model, shown at different zoom levels (a)-(c).

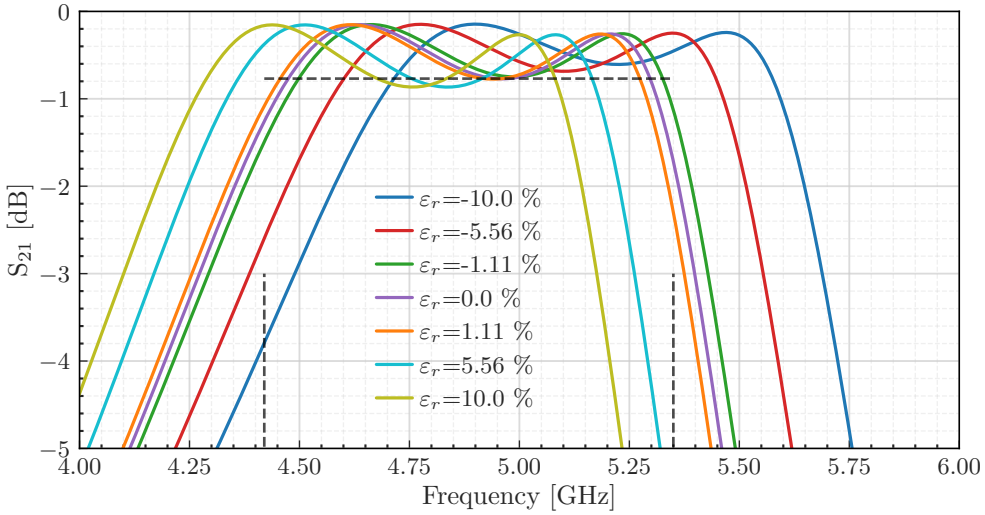

Figure 4.14: Empirical influence of varying dielectric constant ($\varepsilon_r = 25$) on the filter transfer function of the optimized final design.

4.1.7 Higher order comparison

To ensure model validity and to avoid overfitting, a third-order filter version based on the second-order model was investigated. The main objective was to assess whether the lumped element model developed for the second-order filter can be meaningfully extended to synthesize higher-order filters. Since the model already exhibits limitations for the second-order case, its direct extension is not expected to yield quantitatively accurate results. Nevertheless, a proof of concept study for a higher-order filter was carried out, and the simulation and design of a third-order filter were performed.

For the design procedure, the same workflow as in the previous section was followed. First, the filter order was increased in Genesys to generate the initial lumped element architecture of the higher-order filter. As shown in Fig. 4.15, the second-order filter topology scales naturally to third and higher orders by adding an additional inductor and three capacitors for every order. This lumped element model forms the basis of the subsequent optimization. In the next step, the extracted S-parameter models of the inductors and the RLC models of the capacitors were implemented in ADS and optimized to meet the target bandpass specifications, following the same bandpass filter optimization as previously. For both designs, a corresponding physical model was created and simulated in Ansys. The results are shown in Fig. 4.16.

It is clear that, as expected, the simple model based on the lumped element model from Genesys is significantly mismatched and the passband is non-existent. It rather exhibits unexpected behavior with a resonator at 3.38 GHz. On the other hand, the iterated and improved lumped element model of the capacitors and S-parameter model of the inductors exhibit significantly improved behavior. The model is able to predict a passband filter. The model falls short of the required bandwidth and passband ripple. As previously, this model was then with a limited iteration improved empirically and results in a third-order filter. The empirically improved filter has a significantly improved bandpass filter and the poles of the filter are clearly visible in the filter reflection behavior. Overall, the filter passband is shifted 500 MHz upwards and exhibits a passband ripple above the constraints outlined previously, but it nevertheless demonstrates that it is possible to create higher-order filters using the proposed filter design.

As expected, the initial model based purely on the lumped element parameters obtained from Genesys shows a significant mismatch and does not exhibit a well-defined passband. Instead, it displays an unintended resonator behavior around 3.38 GHz. In contrast, the iteratively improved model based on refined capacitor RLC models and inductor S-parameter models shows a substantially better agreement with the desired bandpass behavior. This model successfully predicts a passband filter, although it still falls short of the required bandwidth and passband ripple. As in the second-order case, the model was further improved through limited empirical optimization, resulting in the final third-order design shown in Fig. 4.16b. The empirically optimized filter exhibits a clearly defined bandpass response, and the filter poles are distinctly visible in the frequency response. While the final design still does not fully meet the target specifications, it demonstrates that higher order filters can, in principle, be synthesized using this approach, provided that more extensive empirical optimization and a more accurate physical modeling of the components are

employed. However, due to the significantly larger parameter space, such empirical optimization becomes increasingly time consuming for higher-order designs.

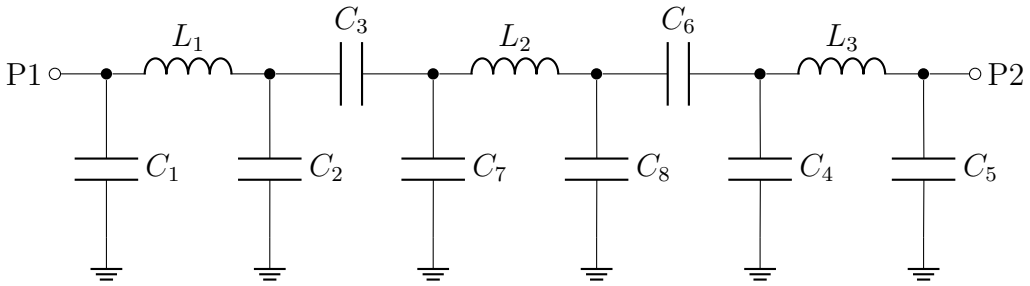

Figure 4.15: Lumped element model of a third order Chebyshev bandpass filter using a tubular topology synthesized in Genesys.

Table 4.9: Dimensions and corresponding capacitance values utilized for the 3rd Order filter using Genesys.

Parameter Set	**Element**	**Value**	**Error**	**Unit**
Physical Design				
Capacitor values	$C_1 = C_5$	3.77	±0.47	pF
	$C_2 = C_4$	4.06	±0.50	
	$C_3 = C_6$	1.25	±0.18	
	$C_7 = C_8$	3.48	±0.44	
Capacitor physical sizes	$a_1 = a_5$	26	±1	µm
	$a_2 = a_4$	27		
	$a_3 = a_6$	15		
	$a_7 = a_8$	25		

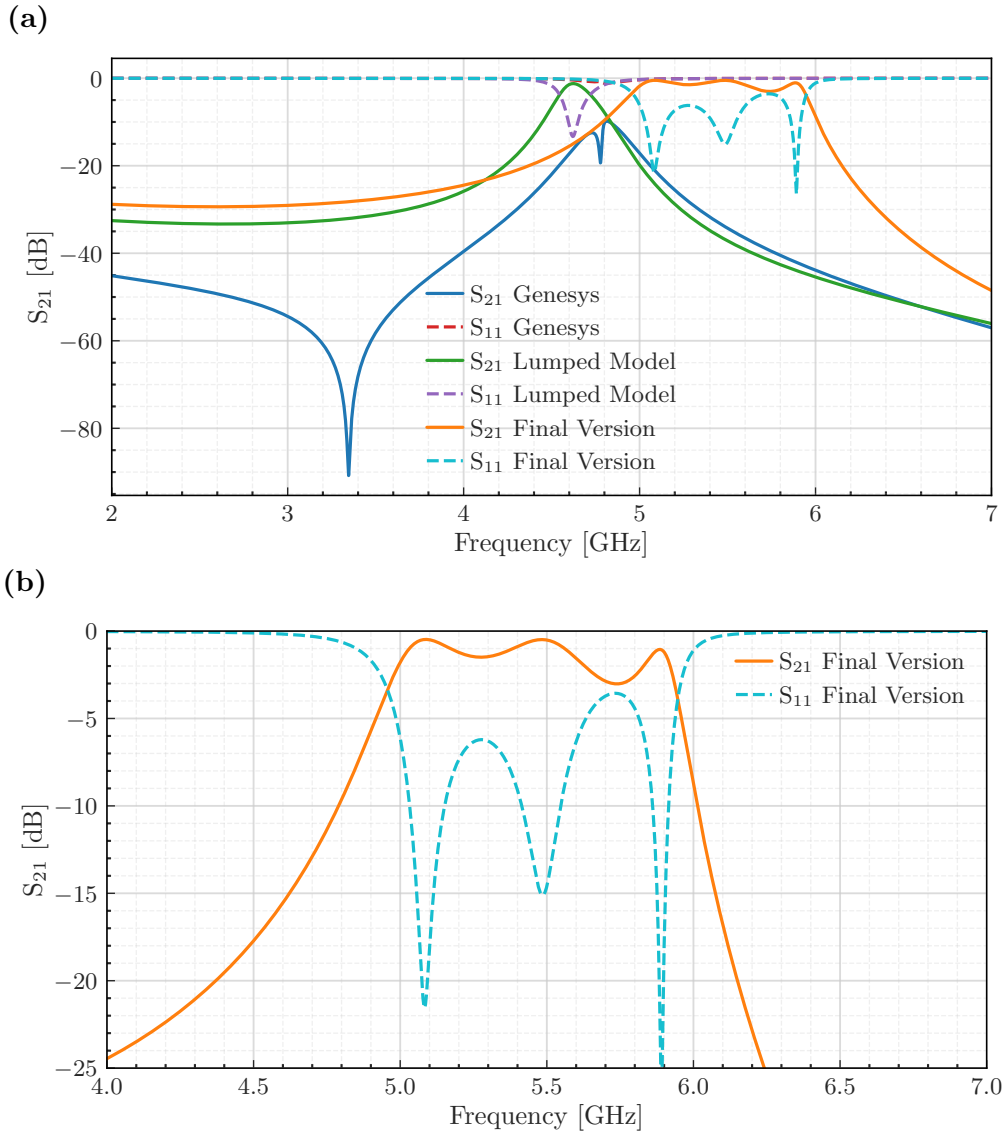

Figure 4.16: (a) Comparison of the simulated filter transfer functions for different third-order filter designs based on physical models using 3D parallel-plate capacitor structures. The designs correspond to parameters derived from Table 4.9, obtained from the initial lumped element model created in Genesys (Genesys); Table 4.10, obtained from the optimized model in ADS using the complex RLC component models described in Section 4.1.4 (Lumped Model); and Table 4.11, corresponding to the final model obtained through empirical optimization (Final Version). (b) Transfer function of the final optimized model, zoomed in around the target bandpass frequency.

Table 4.10: Dimensions and corresponding capacitance values utilized for the 3rd Order filter using the improved lumped element model.

Parameter Set	Element	Value	Error	Unit
Physical Design				
Capacitor values	$C_1 = C_5$	3.21	±0.44	pF
	$C_2 = C_4$	5.71	±0.69	
	$C_3 = C_6$	2.95	±0.38	
	$C_7 = C_8$	2.70	±0.35	
Capacitor physical sizes	$a_1 = a_5$	24	±1	µm
	$a_2 = a_4$	32		
	$a_3 = a_6$	23		
	$a_7 = a_8$	22		

Table 4.11: Dimensions and corresponding capacitance values utilized for the 3rd Order filter after performing empirical optimization.

Parameter Set	Element	Value	Error	Unit
Physical Design				
Capacitor values	$C_1 = C_5$	3.21	±0.44	pF
	$C_2 = C_4$	2.23	±0.30	
	$C_3 = C_6$	2.01	±0.27	
	$C_7 = C_8$	2.23	±0.30	
Capacitor physical sizes	$a_1 = a_5$	24	±1	µm
	$a_2 = a_4$	20		
	$a_3 = a_6$	19		
	$a_7 = a_8$	20		

4.2 Measurement

4.2.1 Filter characterization

For the characterization, the second-order filter is measured at cryogenic temperatures. As outlined in Section 3.3, a S_{21} measurement is performed for the 2-port device with the through line of the 4-port devices acting as references measurement. The extracted transfer function of the designed filter is shown in Fig. 4.17. Contrary to the expected bandpass filter response, the measured behavior resembles that of a resonator, with a central frequency at approximately 4.26 GHz. This response deviates significantly from the intended filter functionality and indicates a fundamental issue in the realized design. Additionally, the readout resonator of the 4-port qubit device is visible at approximately 6.5 GHz.

4.2.2 Filter Rebuttal

Since the measured transfer function deviated significantly from the expected response, a systematic investigation was conducted to identify the root cause. A primary hypothesis was a malfunction arising from a faulty chip. Visual inspection of the fabricated chip, however, revealed no obvious defects, and the overall fabrication quality appeared sound.
To test whether a single capacitor failure could explain the observed behavior, HFSS simulations were performed in which individual capacitors were forced to extreme values (0.1 pF and 200 pF), emulating either an open or shorted connection. None of these scenarios reproduced the measured response, indicating that a simple single component failure was unlikely to be the sole cause.
Next, potential resonances associated with larger chip structures were investigated. Full-chip simulations are computationally demanding and prone to convergence issues; nevertheless, simulations of the complete layout, seen in Fig. 4.18a, revealed resonator like behavior, most likely originating from the extended lead contacts. To isolate this effect, the simulation was repeated using a reduced chip model, seen in Fig. 4.18b, in which only the ports were shortened. This reduced model exhibited similar behavior, but shifted to higher frequencies, as seen in Fig. 4.18c. This observation suggests that higher-order resonances of the lead structures contribute to the measured response. However, these resonances alone do not fully account for the observed spectral features.
In the next step, multi-component failures were considered. Here, multiple capacitors are set to extreme values to investigate more systematic errors. For the case in which capacitors C1 and C5 are assigned a very small capacitance value (0.5 pF), corresponding to the absence of a galvanic connection, the simulated response shown in Fig. 4.19 closely resembles the measured data. This result strongly suggests that the device suffers from multiple faulty capacitor connections.

4.2.2.1 SEM

To start verify this hypothesis, an identical chip was inspected using scanning electron microscope (SEM). Fig. 4.21 shows the SEM images of the devices. Figs. 4.21a

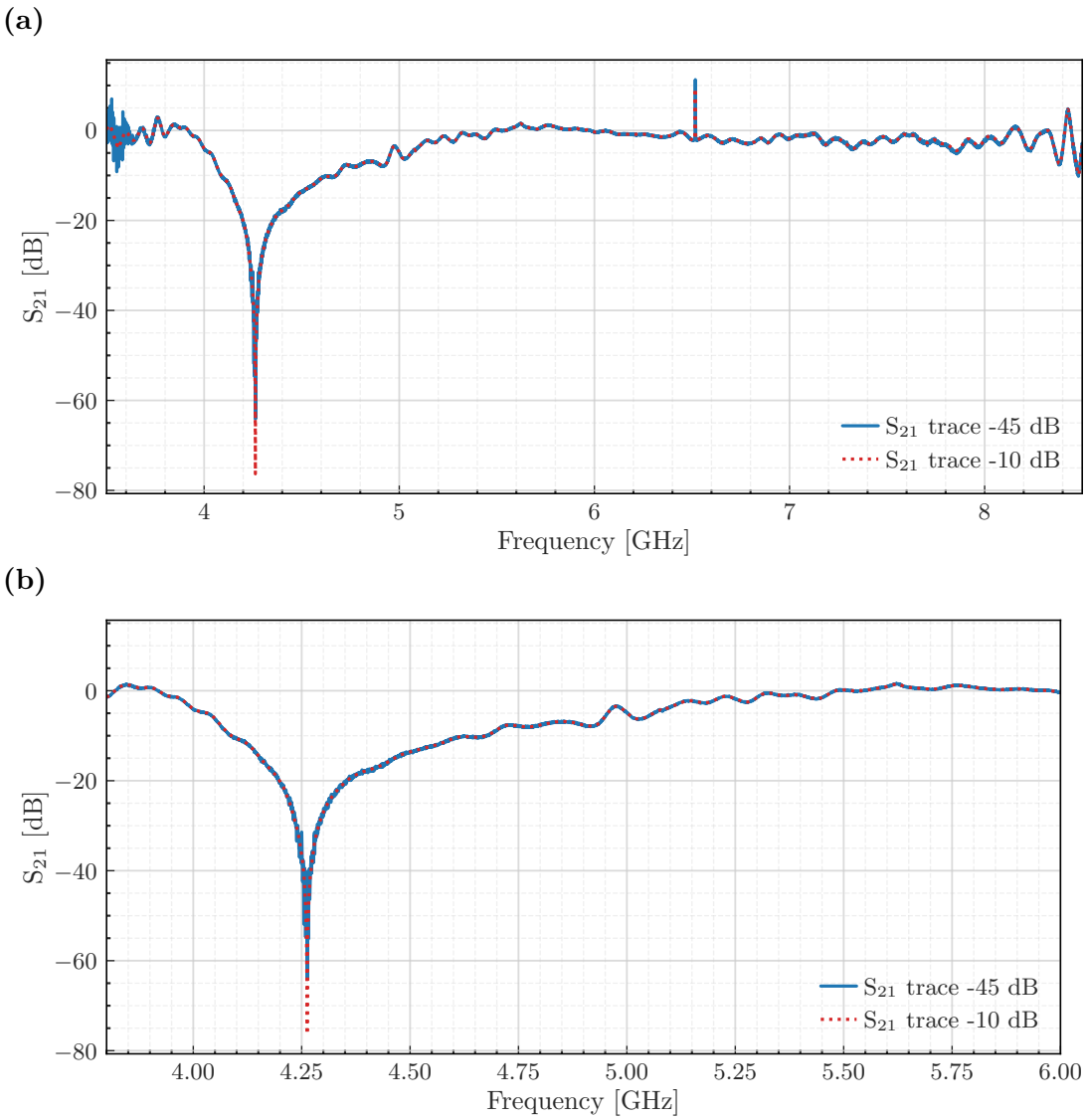

Figure 4.17: (a) VNA transmission measurement of the transfer function of the 2-port devices for different drive power. (b) Zoomed view of the relevant frequency band.

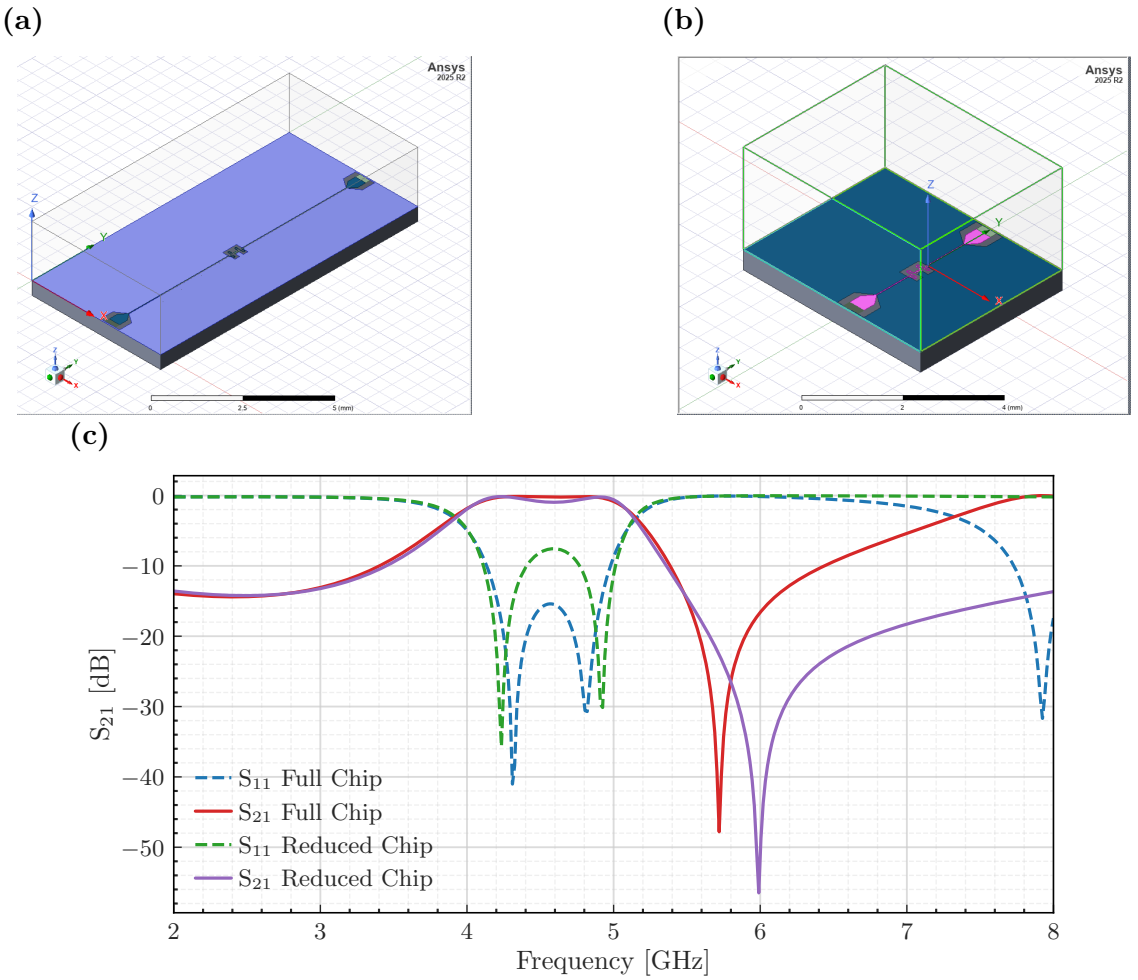

Figure 4.18: Physical model of the optimized final design showing (a) the full chip, (b) a reduced chip size containing only the relevant structures in proximity to the filter, and (c) the corresponding filter transfer functions of both models.

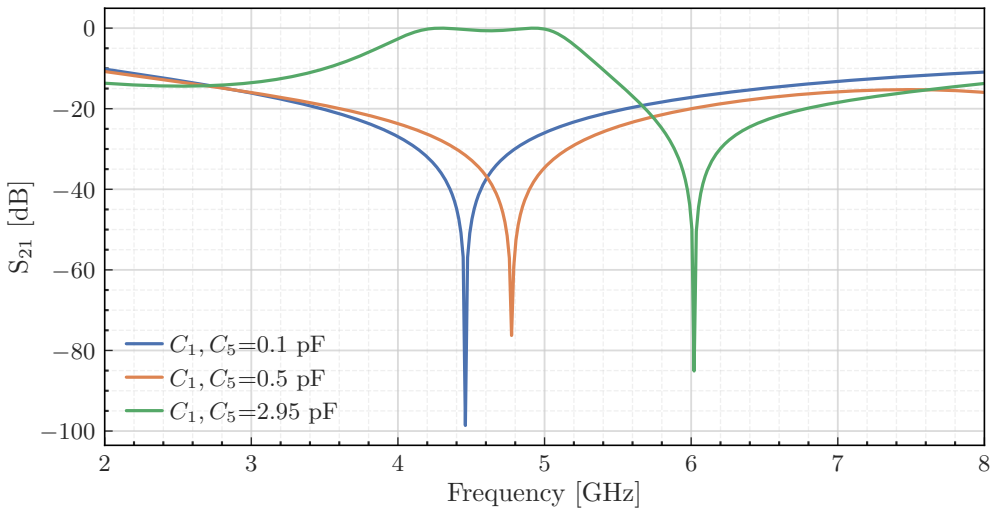

Figure 4.19: Filter transfer function of the reduced filter chip with an ideal capacitor model, where a reduction in capacitance corresponds to a defective capacitor.

and 4.21d show the capacitor connection of C_1 and C_5, where the lead connection appears to be defective. This failure can be attributed to a fault in the connection design, where step coverage was neglected. In addition, a fabrication issue suggests deviations in layer thickness, as seen in Figs. 4.21e and 4.21f. It appears that the top layer of Al is thinner then the ground plane. This would lead to faulty connection of the capacitors. This becomes clear by analyzing the fabrication process in more detail, as shown in Fig. 4.20.

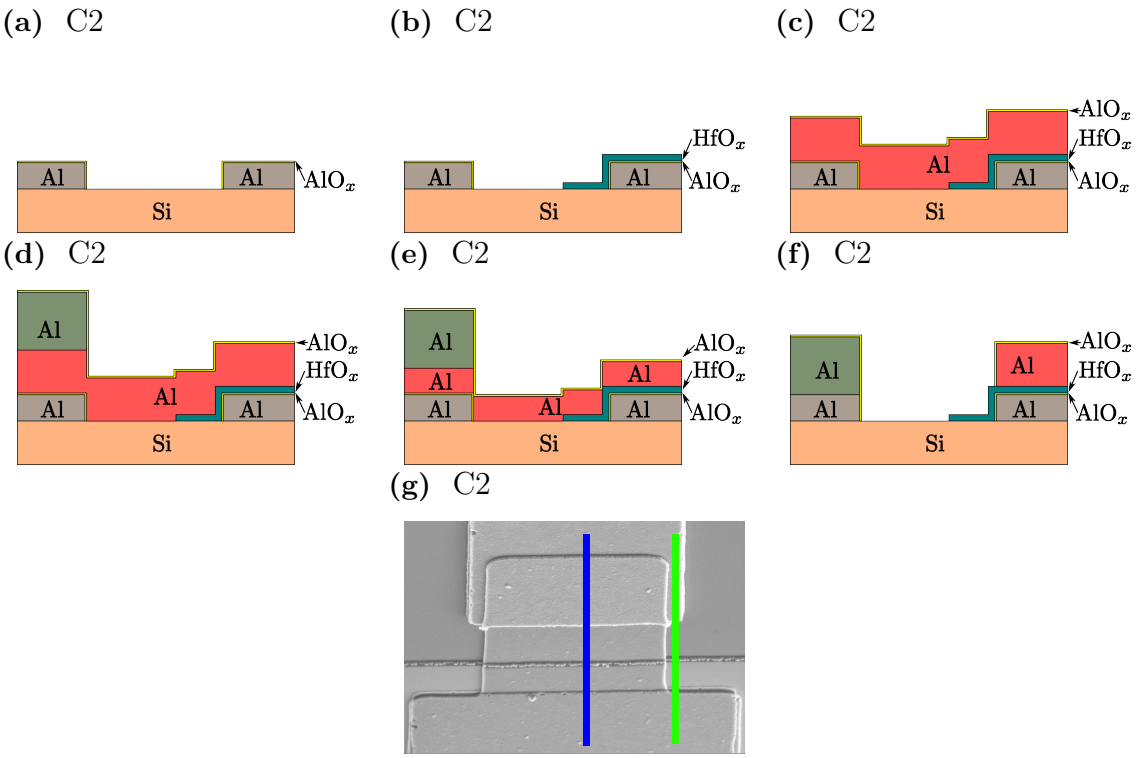

Figure 4.20: Schematic cross-section along the blue line in Fig. 4.20g during the fabrication process outlined in Section 3.2.5, illustrating the step coverage: (a) after the initial ground deposition where a native AlO_x forms on the Al, (b) ALD deposition of HfO_x, (c) top-layer deposition, (d) Al patch deposition after Ar milling to remove the native AlO_x on the top Al layer, (e) illustration of insufficient step coverage for reduced top-layer thickness, leading to missing galvanic contact, (f) cross-section along the green line where the patch ensures galvanic connection between the top Al layer and the ground plane, (g) SEM image of the 4-port device indicating the cross-section locations seen in (a)-(e) in blue and (f) in green.

The fabrication process provides insight into this failure mechanism. First, the ground plane was deposited using PVD under vacuum conditions. After removal from the chamber, a native aluminum oxide (AlO_x) layer formed on the Al surface. Subsequently, the HfO_x dielectric was deposited using ALD, which provides good step coverage. The top Al layer was then deposited using PVD, a process that offers limited step coverage as the wafer is not tilted during deposition.
While the thickness of the top Al layer is sufficient for covering the high deviation of the dielectric, the capacitor lead experiences a large step height originating from the bottom layer and native AlO_x. Additionally, SEM inspection indicates that the top

Al layer is thinner than expected, likely due to deposition issues during fabrication. As a result, the metal coverage over the step is insufficient, breaking the top layer into two islands. This leads to potentially unreliable or broken electrical connections. Finally, the Al patch layer is deposited after Ar ion milling to remove the native AlO_x. The patch connects the ground layer with the top layer. Since the patch does not extend to both top layer islands, it does not compensate for the step coverage issue.
Overall, this results in a potentially unreliable connection, as the overlap region is very thin and may vary between leads. It is therefore unclear which connections provide reliable galvanic contact. This issue could be mitigated in future designs by extending the patch over the edge and ensuring a sufficiently thick top metal layer. An additional investigation in the form of a room-temperature resistive measurement of the lead contacts was performed and can be found in Appendix D, but the results were inconclusive.

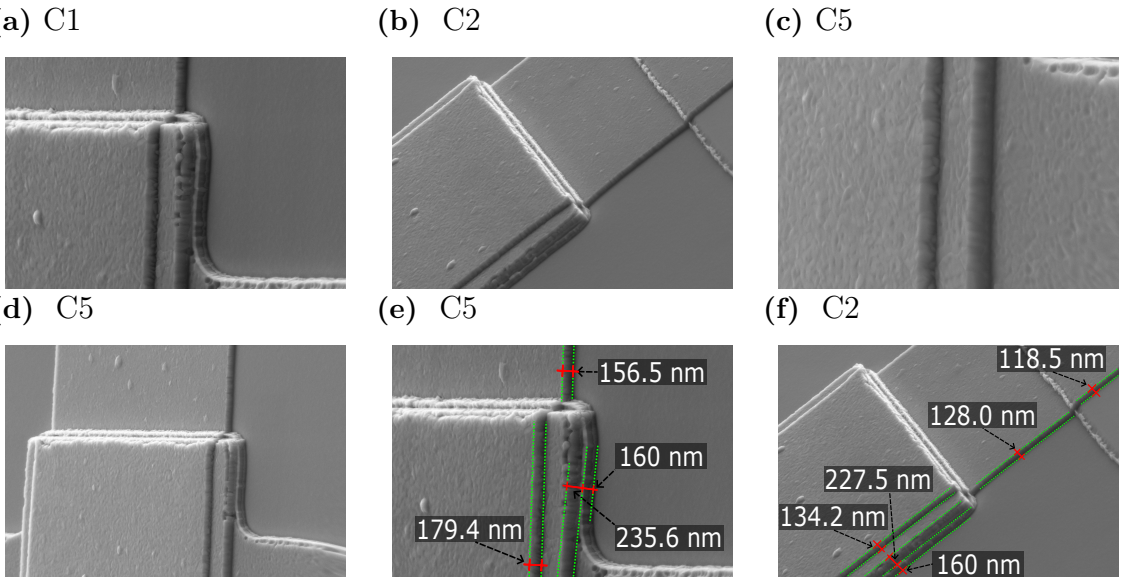

Figure 4.21: SEM images of the 4-port device for various capacitors: (a)–(d) analysis of the capacitor leads, (e) and (f) estimated layer thicknesses extracted from the images. The ground layer thickness was measured using profilometry (160 nm) and serves as a reference.

4.2.3 4-port Device

In the following the experimental results of the 4-port devices is analyzed.

4.2.3.1 Expected Filter Effect

Prior to experimental characterization, the thermal model described in Sec. 3.4 is used to estimate the expected impact of the on-chip filter in the 4-port device. The thermal noise spectrum from the drive line reaching the qubit is shown in Fig. 4.23 for the standard driveline.

For the baseline configuration, a seventh-order low-pass filter with a cutoff at 8 GHz is included, as inferred from the manufacturer specifications, seen in Fig. 4.22 [64]. The resulting thermal noise contribution is relatively uniform across the stages, indicating that the attenuators are well distributed along the drive line. The model does not account for additional attenuation and loss from the microwave wiring itself and therefore represents a conservative estimate.
Fig. 4.23 shows the thermal noise spectrum at the qubit with and without the on-chip bandpass filter, using the transfer function for the Bandpass filter shown in Fig. 4.22. The integrated bandpass filter strongly suppresses out of band thermal noise while preserving the signal band required for qubit control. When integrating over the frequency range from 2–8 GHz, the mean thermal power is reduced by approximately 59%. This reduction is substantial and highlights the potential of on-chip filtering to lower thermal noise coupling without compromising the usable control BW. This significant improvement is estimated to be substantial enough to detect in the 4-port devices.

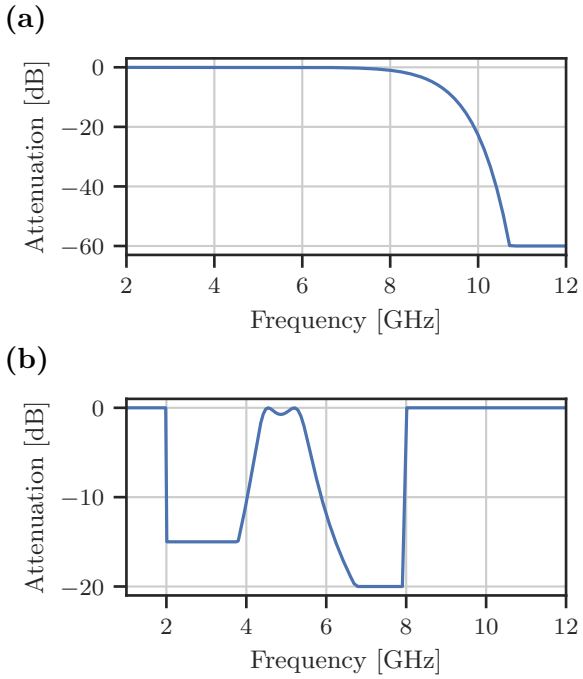

Figure 4.22: Filter transfer function models for: (a) a low-pass filter [64] with constant −60 dB attenuation above 11 GHz, and (b) the designed passband filter with lower stopband attenuation of 15 dB and upper stopband attenuation of −20 dB over the frequency range from 2–8 GHz.

4.2.3.2 Measurement

To evaluate the filter performance in mitigating thermal fluctuations, the 4-port device was prepared for measurement in the cryogenic setup. However, because the experimental validation of the filter transfer function was unsuccessful, these measurements were not carried out.

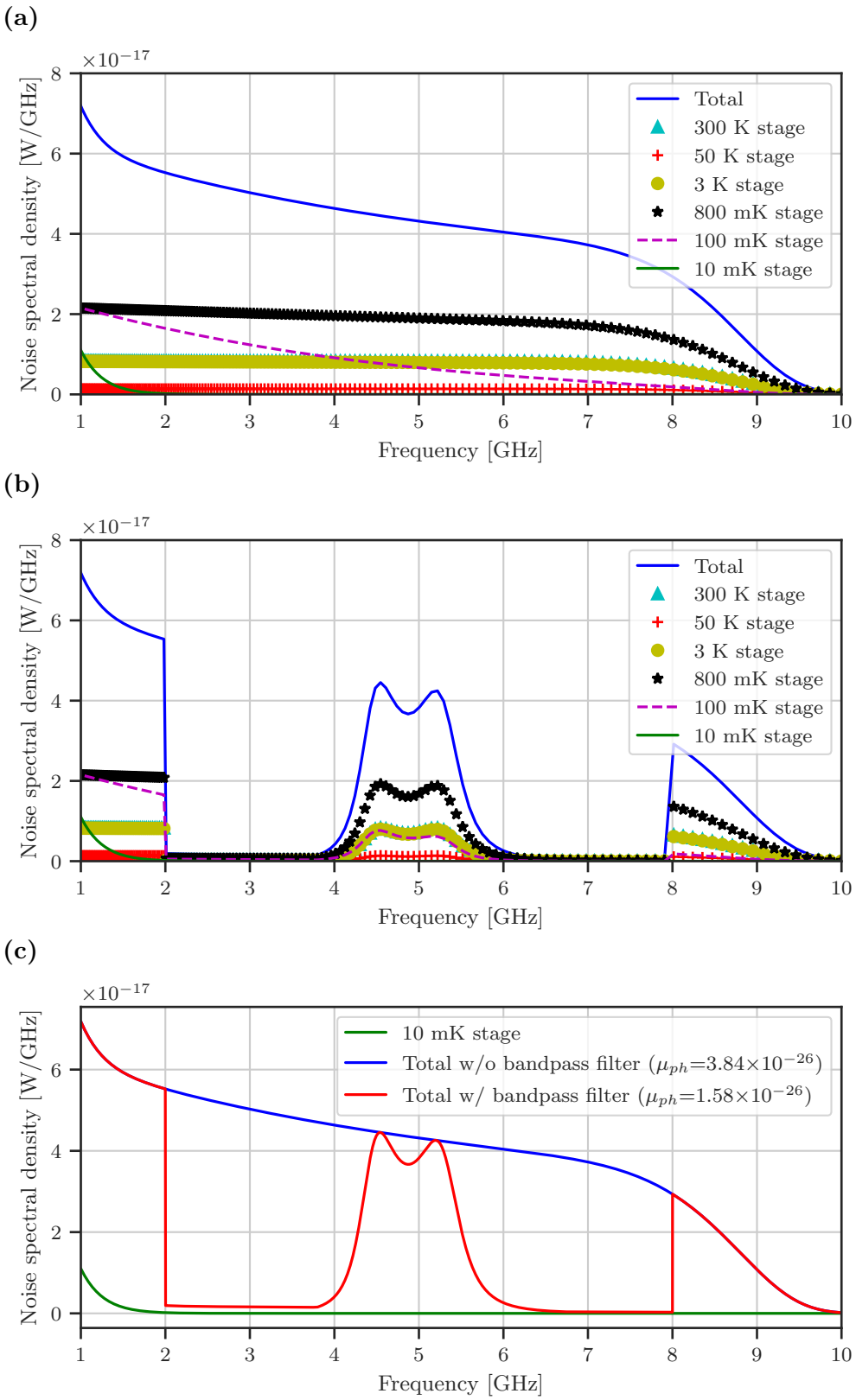

Figure 4.23: Spectral noise density for the cascaded noise model in Fig. 3.5 for the idealized setup shown in Fig. 3.4 without (a) and with (b) an on-chip bandpass filter, including individual noise stage contributions. (c) Direct comparison of the total spectral noise density in (a) and (b), and the corresponding mean photon number for the total noise spectrum within the filter operating range from 2–8 GHz.

Further investigation is therefore required to identify and resolve the underlying issues in the fabricated device before meaningful thermal noise measurements can be performed. The implementation and validation of this measurement will therefore be part of future work and is discussed in more detail in the following chapter.

5
Conclusion and Outlook

This work presents the investigation of on-chip filters for superconducting drive lines. The focus was the modeling and development of a lumped element bandpass filter for superconducting applications, covering the full design flow from initial parameter definition to a fabricated on-chip device. Through iterative development of simulation models, the objective was to improve model precision and establish a foundation for scalable and rapidly designed on-chip filters tailored to individual qubits.

The initial part of this work defined the key constraints required for a practical filter design and outlined the challenges of implementing on-chip filters under cryogenic conditions. Relevant parameters such as cutoff frequencies and the required BW for qubit drive applications were identified. Manufacturing uncertainties and fabrication limitations were explicitly considered in order to derive realistic design targets. These constraints significantly limited the accessible parameter space and restricted feasible filter topologies. The specifications were first translated into a lumped element circuit model and subsequently into physical layouts. Iterative refinement of the circuit model aimed to improve its predictive accuracy and to provide a reliable starting point for the physical design while reducing reliance on computationally expensive EM simulations.

In practice, the lumped element modeling approach did not reach the level of accuracy required to substantially reduce the need for EM simulations. While such simplified models are commonly used as an initial design step in RF engineering, parasitic inductances and capacitances were not captured with sufficient accuracy in the circuit-level representation. As a result, the lumped element model primarily served as an improved starting point rather than a predictive substitute for physical simulation. Consequently, direct optimization of the physical structure was required. By performing parameter sweeps and optimization directly in Ansys HFSS, a EM model was obtained that satisfied the defined design objectives at a significantly increased computational cost. The resulting design exhibited limited robustness to parameter variations, with uncertainty in the dielectric constant identified as a dominant limitation for achieving high precision and accuracy.

Nevertheless, the extended lumped element model, which incorporated extracted S-parameter models for inductors and RLC representations for capacitors, provided an improvement over the idealized lumped element model. While the extended model remained significantly less accurate than the physical EM simulation, it offered a more realistic starting point for the design process compared to purely ideal elements. The extended model was used to demonstrate the conceptual scalability of the filter architecture to higher-order designs. However, its quantitative accuracy re-

mained insufficient for reliable direct synthesis. It should therefore be regarded as an improved initial approximation rather than a predictive design tool. The simulations additionally underscore the non-ideal behavior of the lumped element components and highlight the importance of investigating their physical characteristics in greater detail.

The simulations further demonstrated the general feasibility of realizing lumped element filters on-chip using parallel plate capacitors and meander inductors, scalable to arbitrary filter order. The ability to achieve relatively large capacitances within a small footprint highlights the technological potential of passive RF circuit integration for superconducting qubit platforms. In principle, this enables more complex microwave circuitry to be integrated directly on-chip, which is a key requirement for scalable superconducting quantum processors. Although the present simulation accuracy is not yet sufficient for predictive design, the results indicate that lumped element architectures remain a promising direction for future filter implementations.

The fabricated device was subsequently measured in a cryogenic setup; however, full validation of the physical design could not be achieved. The measured response did not exhibit the expected passband behavior and instead showed an inverse behavior; a resonator response. Further investigation through simulations of faulty capacitors suggested that a dual-capacitor failure could reproduce similar resonator behavior. SEM imaging revealed a previously unnoticed design flaw which, combined with reduced top layer metal thickness, likely resulted in unreliable capacitor connections between the top and bottom metal layers. Room temperature resistance measurements were inconclusive, suggesting that galvanic connections may still be partially intact. Overall, these observations point towards fabrication-related issues as the likely cause of the observed device failure.

Beyond the specific device outcome, this work highlights the broader challenges associated with implementing on-chip bandpass filters for superconducting devices. While the behavior of distributed elements at cryogenic temperatures has been investigated extensively, lumped element designs remain comparatively poorly characterized, leading to substantial uncertainty in component accuracy and predictive precision. This lack of well characterized device behavior manifests in significant difficulties when designing larger and more complex structures, primarily due to their strong sensitivity to parasitic effects and fabrication imperfections. These challenges underscore the need for improved simulation models, systematic validation strategies, and enhanced reproducibility in the fabrication of superconducting devices.

Looking forward, further refinement of the lumped element modeling approach would require explicit inclusion of physical dimensions and a more accurate treatment of parasitic inductances and capacitances. On the other hand, with the continued increase in available computational resources, fully automated physical optimization in HFSS is becoming a viable alternative, potentially reducing the practical relevance of highly accurate simplified lumped element models by allowing direct optimization using the physical model. This may ultimately reduce the relevance of highly simplified lumped element models in favor of direct optimization using physical models.

In practice, the limitations of simplified circuit models are well known in RF engineering and occur even in conventional applications using established manufacturing

processes and design methodologies. For this reason, commercial RF design workflows often rely on measurement-based model extraction to achieve higher predictive accuracy. For example, companies such as Modelithics [65] specialize in the characterization and extraction of high-accuracy circuit device models.
At the same time, the continued increase in available computational resources is making direct physical optimization increasingly practical. Automated optimization using EM simulations in Ansys HFFS may therefore provide an alternative design approach, enabling the filter structure to be optimized directly from the physical model without requiring highly accurate simplified circuit representations.
The design workflow used in this work would also benefit from early-stage validation of individual components to detect fabrication flaws before full integration. Although such validation was planned, it was not carried out in this work due to limited cryogenic measurement availability and long fabrication cycles. Further investigation of the observed device failure is therefore necessary. Measurements on additional chips, targeted test structures, and dedicated validation of capacitor interconnects would help clearly identify the root cause.
This work, nevertheless, outlines a viable blueprint for a scalable approach to lumped element filters that can be tailored to individual qubits. Simulations indicate that a passband can effectively shape the qubit's thermal environment while still enabling fast and precise drive control at the target frequency. In addition, the proposed 4-port dual-driveline qubit architecture provides a particularly promising platform for experimentally investigating the influence of on-chip filtering on the qubit's thermal population, enabling controlled comparisons between filtered and unfiltered drive paths within the same device.

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Appendices

A

Bandwidth of a drive signal

For an initial ideal analysis of the drive pulse, a dedicated bandwidth simulation script was developed. Although analytical solutions for simple cases exist, a numerical approach was chosen to account for future incorporation of realistic signals and filter functions. For determining the required bandwidth, the shortest physically relevant drive pulse is considered, with a carrier at the qubit frequency $f_q = 5\,\mathrm{GHz}$ modulated by a finite envelope of duration $T = 20\,\mathrm{ns}$. The time-domain signal can therefore be written as

$$s(t) = A(t)\cos(2\pi f_q t), \tag{A.1}$$

where $A(t)$ denotes the pulse envelope. The pulse envelope can be chosen arbitrarily. Some of the most common examples are the rectangular envelope,

$$A_{\mathrm{rect}}(t) = \begin{cases} 1, & 0 \le t \le T, \\ 0, & \text{otherwise}, \end{cases} \tag{A.2}$$

the raised cosine envelope,

$$A_{\mathrm{rc}}(t) = \begin{cases} \frac{1}{2}\left[1 - \cos\left(\frac{2\pi t}{T}\right)\right], & 0 \le t \le T, \\ 0, & \text{otherwise} \end{cases} \tag{A.3}$$

the sinc envelope,

$$A_{\mathrm{sinc}}(t) = \mathrm{sinc}\left(\frac{t - T/2}{\tau}\right), \tag{A.4}$$

and the Gaussian envelope without truncation,

$$A_{\mathrm{gauss}}(t) = \exp\left[-\frac{(t - T/2)^2}{2\sigma^2}\right], \tag{A.5}$$

where τ and σ control the effective temporal width of the pulse. Each envelope comes with its own strengths and weaknesses, such as smoothness, required bandwidth, and spectral leakage.
To model the filter behavior on the drive pulse, the signal is first transformed into the frequency domain via the Fourier transform

$$S(f) = \mathcal{F}\{s(t)\}. \tag{A.6}$$

For simplicity, an ideal bandpass filter centered at f_q with bandwidth B is then applied,

$$H(f) = \begin{cases} 1, & |f - f_q| \le \frac{B}{2}, \\ 0, & \text{otherwise}, \end{cases} \tag{A.7}$$

resulting in the filtered signal spectrum

$$S_{\text{filt}}(f) = H(f)\, S(f). \tag{A.8}$$

To investigate the distortion introduced by the finite bandwidth, the signal is transformed back into the time domain via the inverse Fourier transform

$$s_{\text{filt}}(t) = \mathcal{F}^{-1}\{S_{\text{filt}}(f)\}. \tag{A.9}$$

The inverse mapping of the Fourier transform underpins the fundamental trade-off between bandwidth in the frequency domain and temporal broadening in the time domain. Reducing the bandwidth leads to a spreading of the time-domain signal, and vice versa. In general, signals with sharp temporal features are more susceptible to distortion due to filtering.
In addition to analyzing waveform distortion, the loss of signal energy due to the finite filter bandwidth is also examined. The energy of the signal in the frequency domain is given by

$$E = \int_{-\infty}^{\infty} |S(f)|^2 \, df, \tag{A.10}$$

and is evaluated before and after applying the filter. The filter function effectively acts as a weighting function on the signal spectrum. Therefore, the choice of filter bandwidth represents a trade-off between bandwidth, distortion and energy loss, with narrower bandwidths generally increasing distortion and energy loss.[66, 67]

B

Induction Extraction

To extract the inductance of the meander inductor, a simple HFSS simulation was employed. Instead of estimating the inductance per unit length using an isolated CPW line, the inductor geometry was placed in parallel with a capacitor, as shown in Fig. B.1. This configuration was chosen to account for the non-uniform proximity of the ground plane and the surrounding layout, which influences the effective inductance. Compared to an CPW biased design, this approach results in a larger inductance.
The simulation was performed using lumped ports. From the known capacitance value of the capacitor and the simulated resonance frequency of the LC structure, the inductance was extracted and used as an initial parameter for the lumped element model.

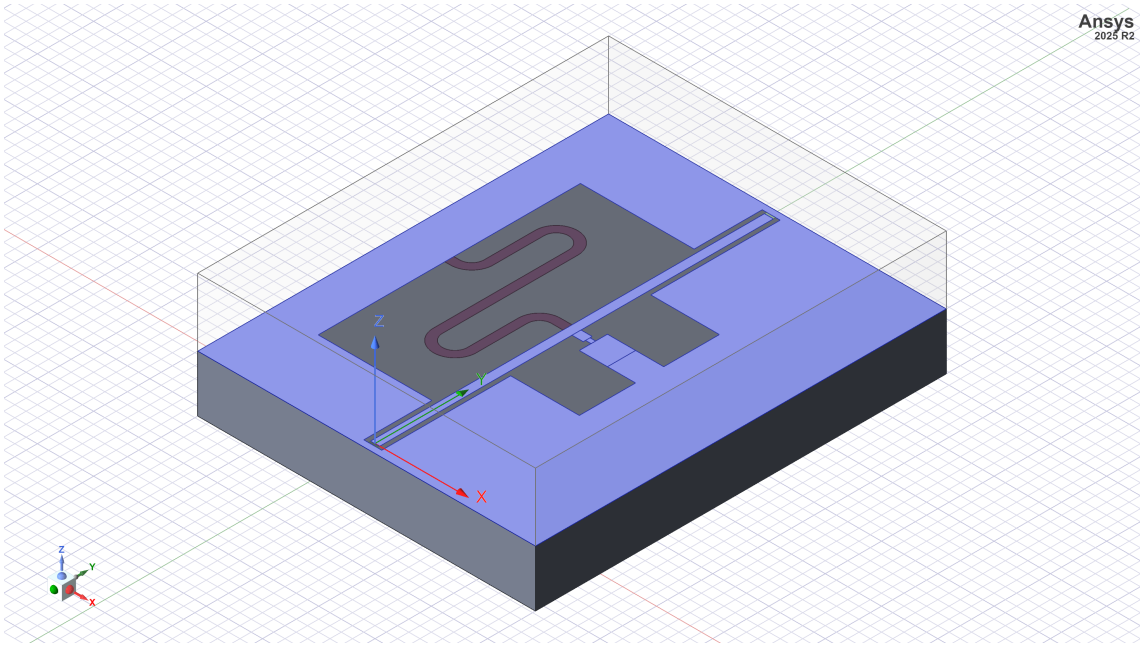

Figure B.1: Physical model of the resonator used to extract the inductances of a meander inductor in *Ansys*.

C

Fitting model parameter

To fit the simulation data to the lumped element model, each capacitor geometry was simulated for a range of physical sizes. The lumped element models shown in Figs. 4.8 and 4.9 were fitted by minimizing the absolute differences between the simulated and modeled scattering parameters S_{11} and S_{21}. All capacitor sizes were treated with equal weight in the fitting procedure.
The minimization was performed using a gradient descent algorithm, initialized with a random optimization step to obtain a suitable starting point. For the fitting process, every second capacitor size was used as training data, while the remaining sizes were used as an interpolation validation set to assess the predictive capability of the model. The resulting fitted capacitor models, shown in Figs. C.1 to C.6, demonstrate that the interpolation across different capacitor sizes is successful.
Overall, the results indicate that as the physical dimensions of the capacitor increase, the accuracy of the lumped element model decreases, particularly at higher frequencies. This behavior suggests that distributed effects and parasitic elements become increasingly significant for larger structures and cannot be fully captured by a size insensitive model.

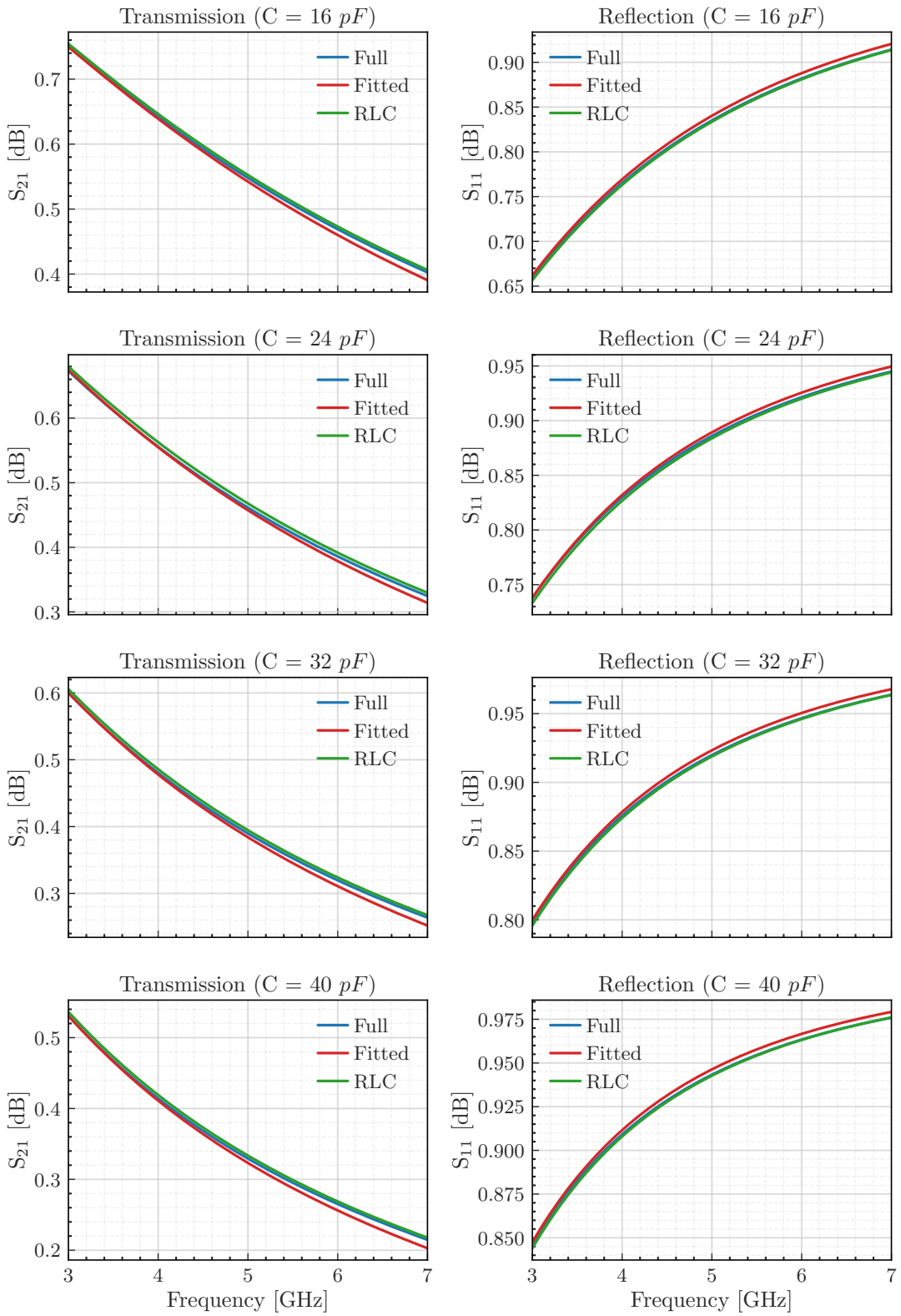

Figure C.1: Transmission S_{21} and reflection S_{11} parameters of the physical model simulation fitted to the lumped element model of capacitor C_1 shown in Fig. 4.9.

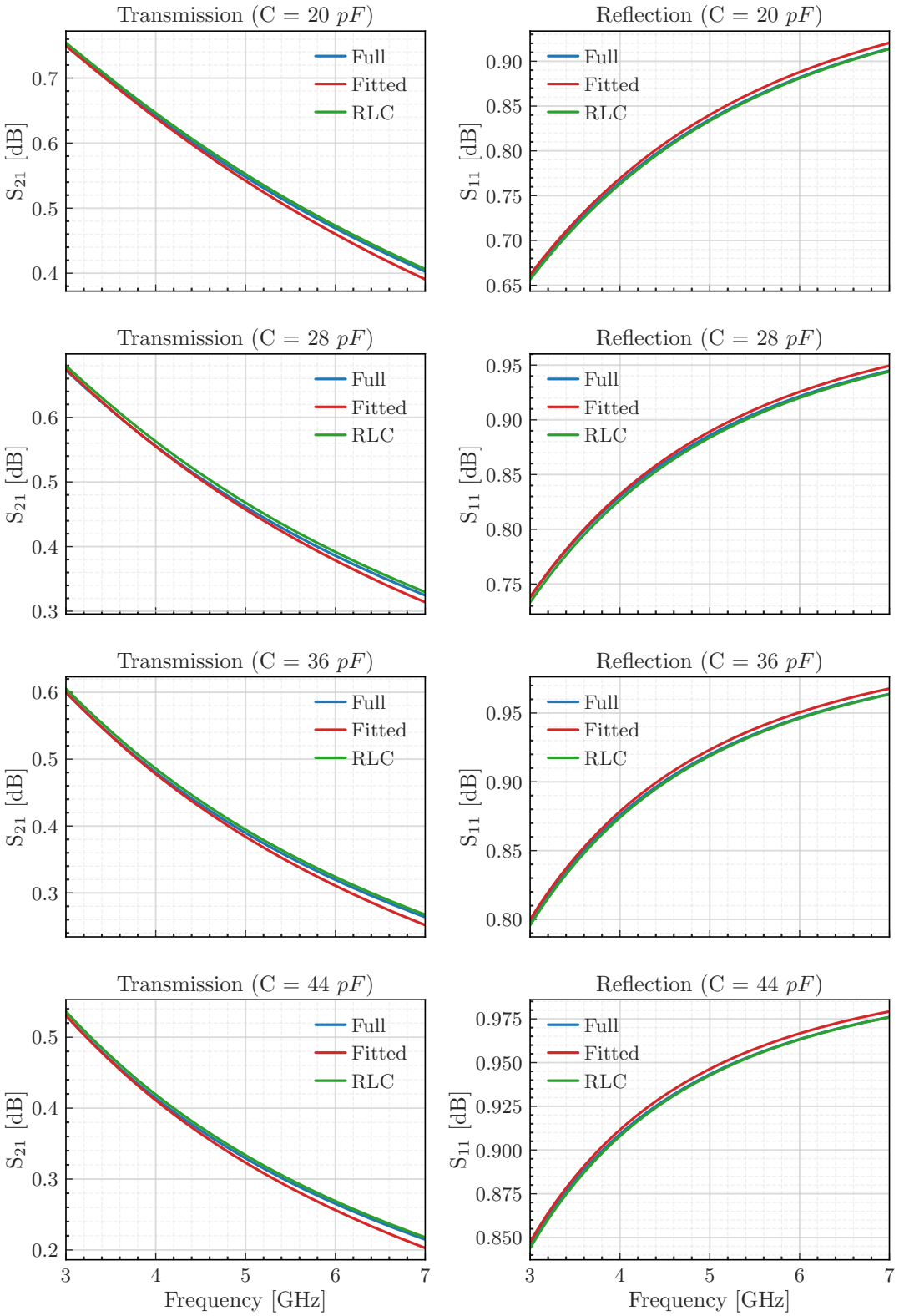

Figure C.2: Transmission S_{21} and reflection S_{11} parameters of the physical model simulation used as interpolation points to validate the lumped element model of capacitor C_1 shown in Fig. 4.9.

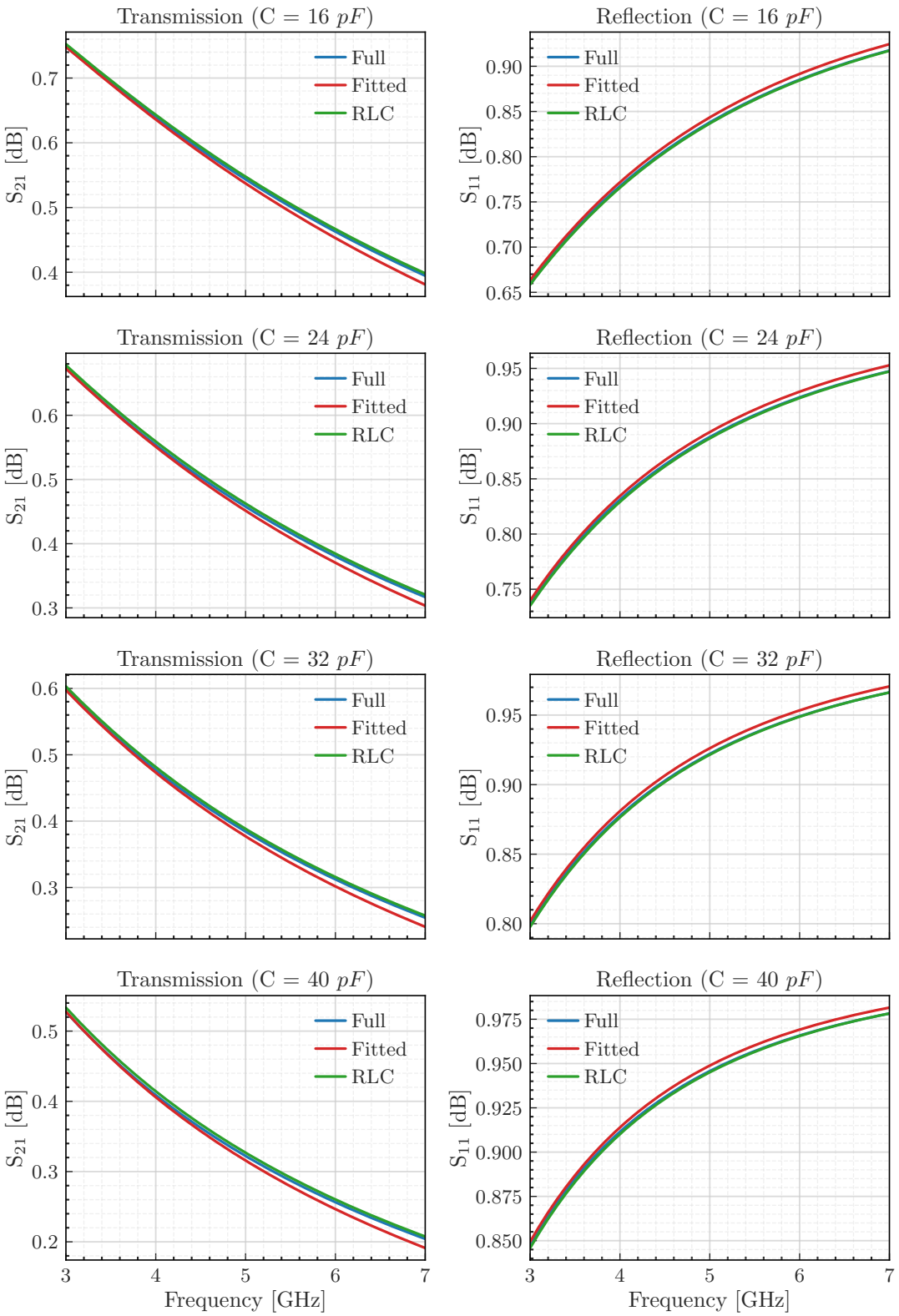

Figure C.3: Transmission S_{21} and reflection S_{11} parameters of the physical model simulation fitted to the lumped element model of capacitor C_2 shown in Fig. 4.9.

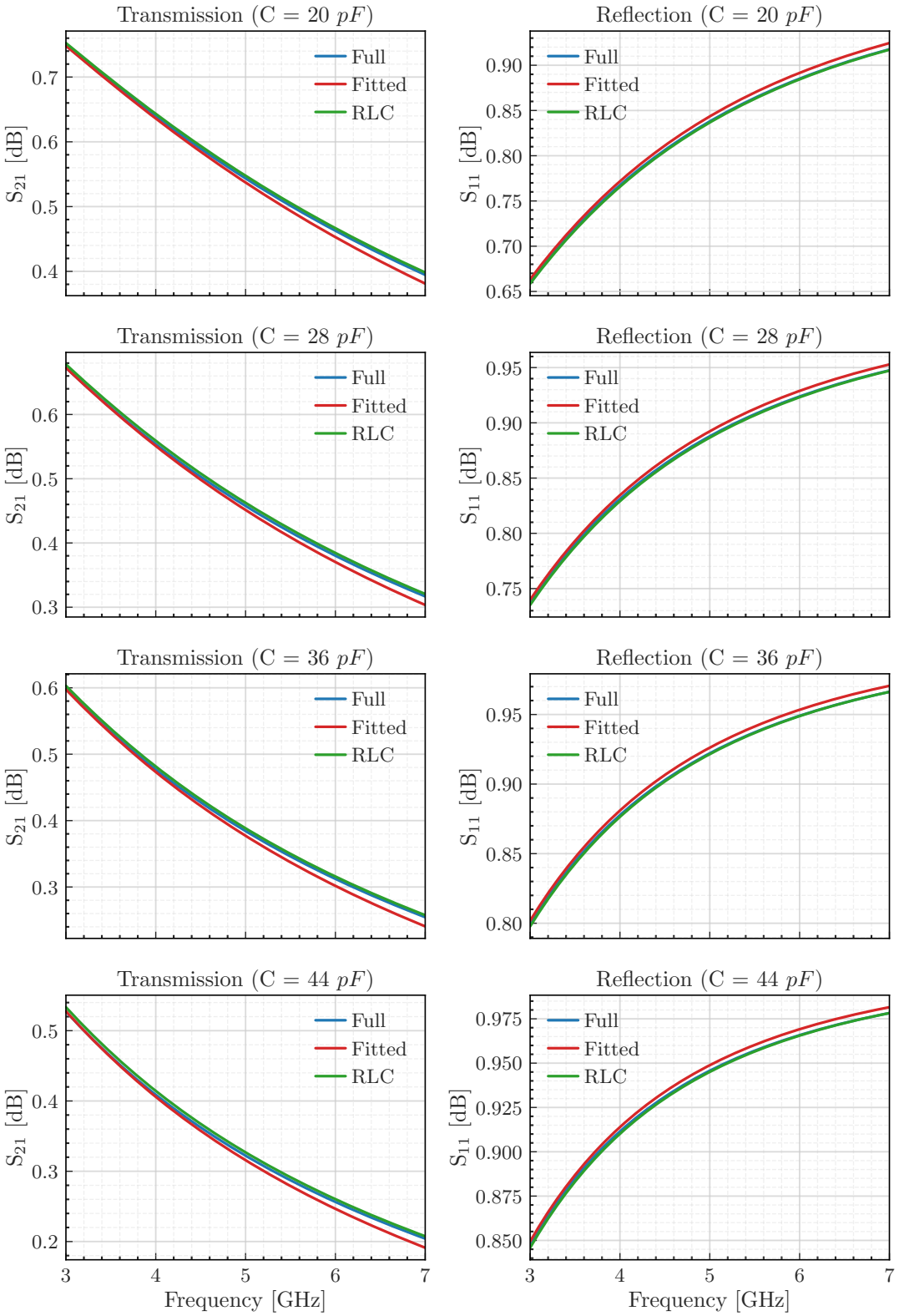

Figure C.4: Transmission S_{21} and reflection S_{11} parameters of the physical model simulation used as interpolation points to validate the lumped element model of capacitor C_2 shown in Fig. 4.9.

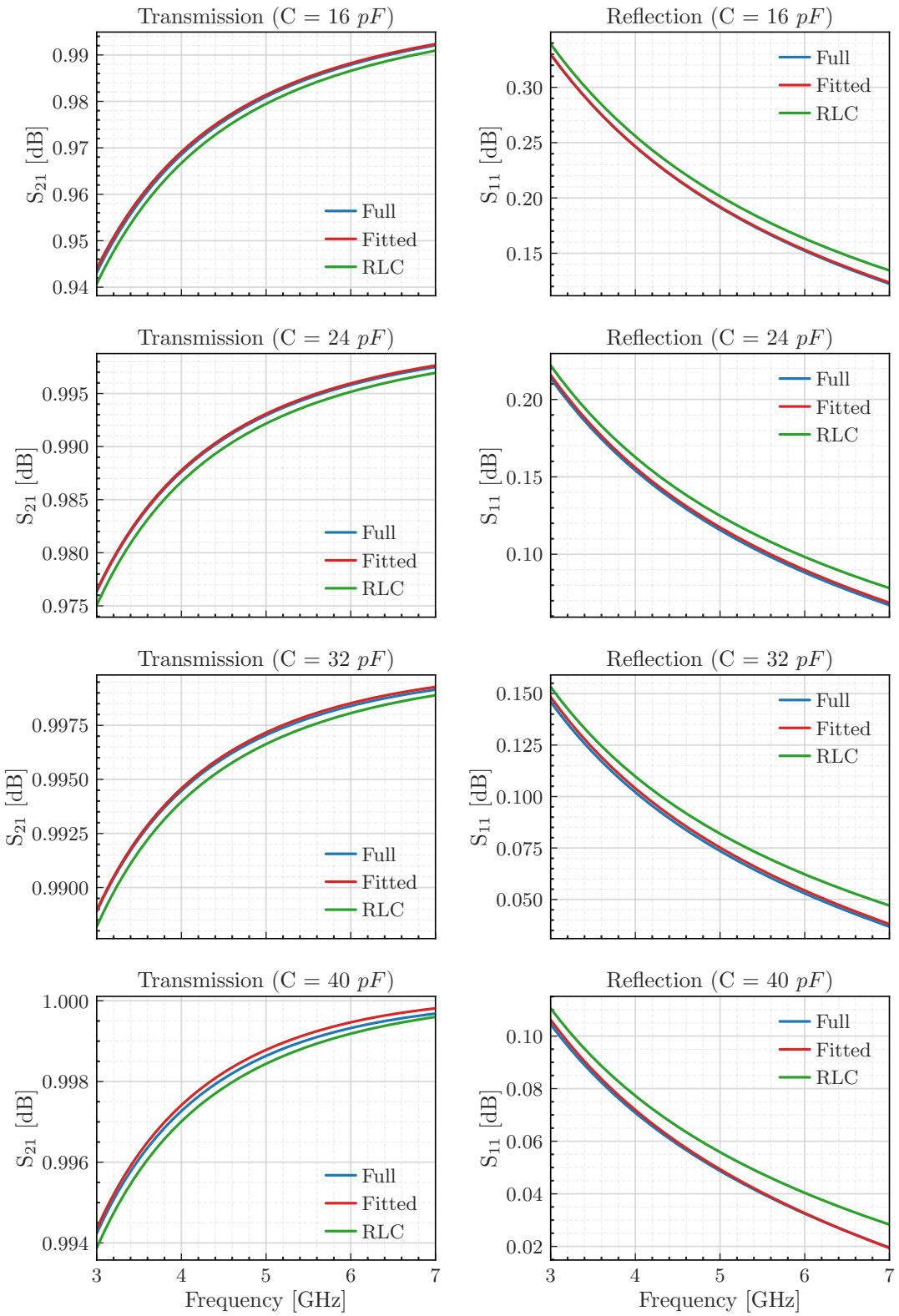

Figure C.5: Transmission S_{21} and reflection S_{11} parameters of the physical model simulation fitted to the lumped element model of capacitor C_3 shown in Fig. 4.8.

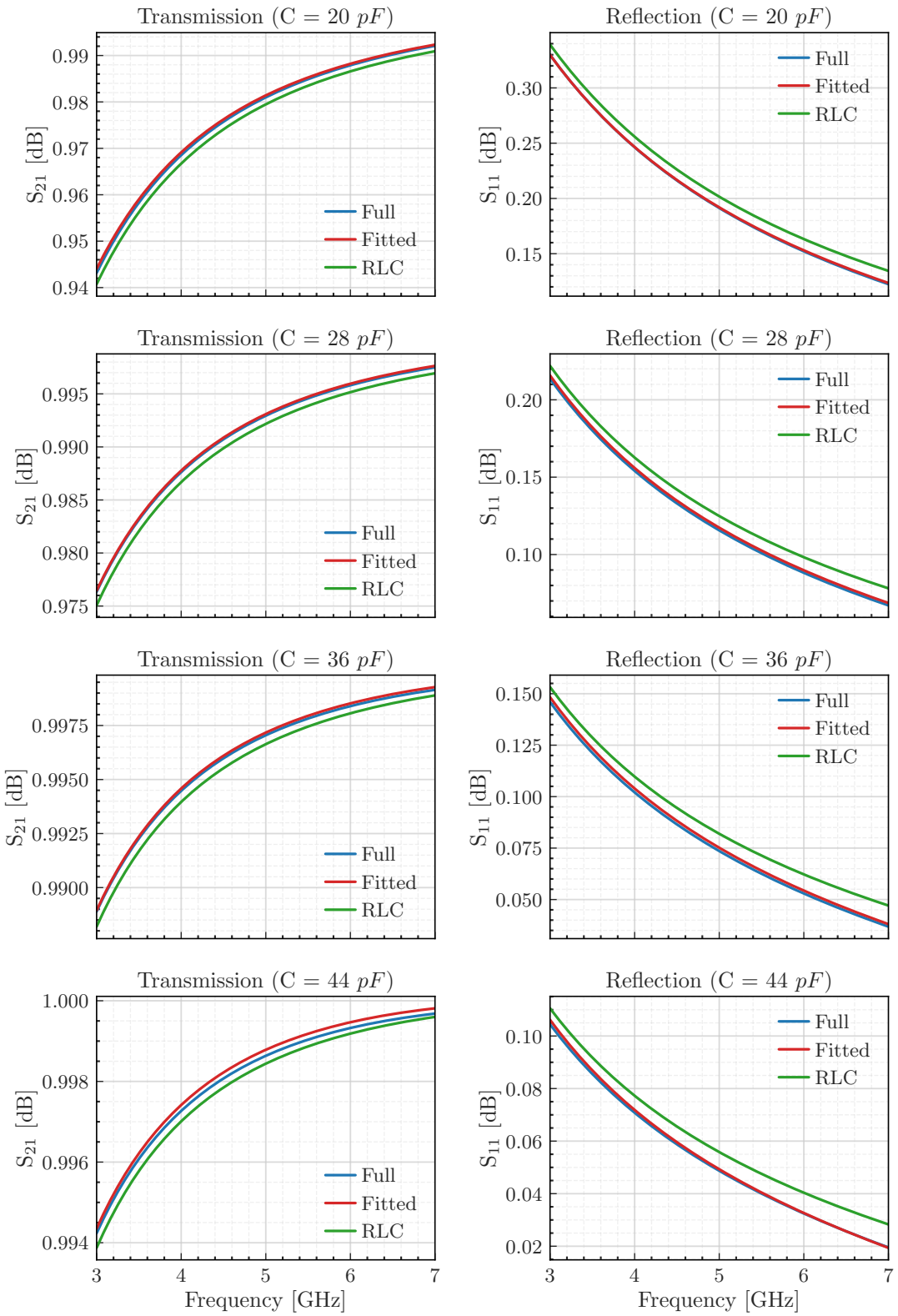

Figure C.6: Transmission S_{21} and reflection S_{11} parameters of the physical model simulation used as interpolation points to validate the lumped element model of capacitor C_3 shown in Fig. 4.9.

D

Resistance Measurements

To further investigate the galvanic connectivity, direct current (DC) resistive measurements at room temperature were performed using the automated probe station MBI TS2000 [68]. Due to the probe needle size being on the order of 10 μm, only 2-port measurements were feasible. The resistance between each capacitor top pad and the CPW was measured and compared to the resistance of an approximately equivalent length of CPW.
Because 2-port resistance measurements are susceptible to static offsets, an additional reference measurement was performed using a 4-port configuration on a roughly 40 μm long CPW section. This reference was used to benchmark the expected resistance level. For a broken connection, an order of magnitude increase in resistance is expected.
The extracted resistance values are summarized in Tab. D.1, together with notes on the individual measurements. Most capacitors show resistance values consistent with expectations. However, C_2, C_3, and C_4 show deviations. Both C_2 and C_4 exhibit increased resistance, although the C_2 result is affected by uncertainty due to the challenging probe placement required for the reference measurement. In contrast, C_3 appears to be shorted since the resistances across the two Pads were in the order of the CPW resistance.
It should be noted that resistive measurements on a single device are inherently unreliable. Elevated resistance values may arise from static measurement errors, imperfect probe contact, or local damage caused by scratching from the probe tips. Nevertheless, these results indicate no order of magnitude increase in the resistance between the capacitor top pads and the CPW. Despite these limitations, the measurements do not indicate an order of magnitude increase in resistance between the capacitor top pads and the CPW, suggesting that fully open connections are unlikely. However, further investigation is required. In particular, the inclusion of dedicated test structures would allow the validation of the reliability of galvanic connectivity to be assessed in future device iterations.

Table D.1: Resistive measurement results of a 2-port measurement of the CPW-to-capacitor top-pad connection, and reference measurements along the CPW.

Capacitor	$\boldsymbol{R}_{\mathbf{meas}}$ (mΩ)	**Error** (mΩ)	$\boldsymbol{R}_{\mathbf{ref}}$ (mΩ)	**Error** (mΩ)	$\boldsymbol{\Delta R}$ (mΩ)	$\boldsymbol{\Delta R}$ (%) (%)
C_1	7.37	0.50	7.67	0.50	−0.30	−3.9
C_2	7.01	0.51	13.18	0.99	−6.17	−46.8
C_3	14.23	1.03	7.24	0.48	+6.99	+96.6
C_4	6.98	0.46	11.27	0.79	−4.29	−38.1
C_5	8.46	0.54	7.97	0.49	+0.49	+6.1
4-Port Reference Measurement						
≈40 µm CPW	1.433	0.113	–	–	–	–

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