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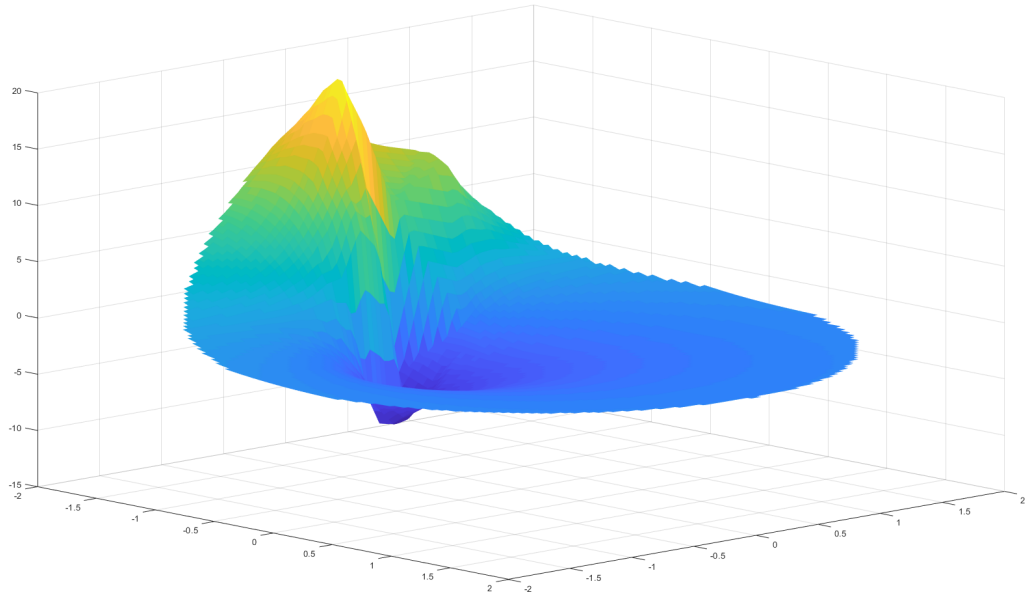

Linear and Efficient Power Amplifier Design Based on a New Optimisation Method

Master's thesis in Wireless, Photonics and Space Engineering

CHRIS JEAN ANTONY

Department of Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY
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Supervisor: Asst. Prof. Koen Buisman, Department of Microtechnology and Nanoscience
Tech. Lic. William, Department of Microtechnology and Nanoscience
Dr. Kristoffer Andersson, Ericsson AB
Dr. David Gustafsson, Ericsson AB

Examiner: Prof. Christian Fager, Department of Microtechnology and Nanoscience

Master's Thesis 2018
Department of Microtechnology and Nanoscience
Microwave Electronics Laboratory
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover: Visualization of incident wave of third order IMD products plotted against the reflection coefficient of main amplifier constructed in MATLAB® showing the irregularities due to its non-linear nature.

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Abstract

Power Amplifiers (PAs) are an integral part of any communication system. Power Amplifiers dominate the overall power consumption of the transmitter. In order to simplify the design procedure, simulations and measurements of PAs are usually done with simple signals such as continuous wave (CW). However, in reality the signals are modulated and this calls for a design requirement using complex modulated signals in order to achieve the optimal design. A Doherty Power Amplifier, operating at a frequency of 2.14 GHz, is designed and simulated using two-tone signals. A detailed study on linearity and efficiency constraints in the design of a DPA was carried out by simulating different combinations of efficiency vs linearity trade-offs. A study on the possibility of predicting the IMD components from the DPA was also done using a novel concept of IMD3 load-pull simulations. Finally, an emulation measurement study of a classical DPA using Chalmers Weblab setup for one-tone and two-tone has been done, where the time-varying load modulation is recreated in a measurement setup.

Keywords: Multiple-Input and Multiple-output (MIMO), 5^{th}-Generation Wireless Systems (5G), two-tone signal, Doherty, load modulation, Power Amplifier(PA), load-pull, Third-Order intermodulation Distortion (IMD3), Fifth-Order Intermodulation Distortions (IMD5), IMD3 Load-Pull, power wave, Load Impedance Spectrum.

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Chris Jean Antony, Gothenburg, June 2018

Notations and Abbreviations

Notations

b_{2m}	Power wave going out from the main amplifier
b_{2a}	Power wave going out from the auxiliary amplifier
a_{2m}	Power wave going into the main amplifier
a_{2a}	Power wave going into the auxiliary amplifier
η	Drain efficiency
λ	Wavelength of the signal
G_T	Transducer Power Gain
G_{comp}	Gain Compression
I_{ds}	Drain-source current, DC component
$I_{ds,max}$	Maximum fundamental drain-source current
P_{DC}	DC power
P_{del}	Power delivered to the fundamental load termination
R_L	Fundamental load termination resistance
V_{ds}	Drain-source voltage, DC component
V_{gs}	Gate-source voltage, DC component
Z_L	Load Impedance
Z_S	Source Impedance
Z_{opt}	Optimum Load-Impedance

Abbreviations

5G	Fifth Generation Mobile Networks
CW	Continuous Wave
IMD	Intermodulation Distortion
DPA	Doherty Power Amplifier
DPD	Digital Pre-distortion
PA	Power Amplifier
LTE	Long-Term Evolution
UMTS	Universal Mobile Telecommunications System
ICT	Information and Communication Technology
MIMO	Multiple-Input and Multiple-Output
NMSE	Normalized Mean Square Error
OPBO	Output Power Back-off
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
RF	Radio Frequency

Contents

Chapter 1

Introduction

1.1 Motivation

Power Amplifiers (PAs) are used in applications where high power is needed, typically in transmitter sections. Radio frequency (RF) amplifiers can be required to produce output powers up to a few hundred kilowatts [1]. RF PAs are found not only in mobile communications but also in other wireless communication techniques such as Wi-Fi, Bluetooth, radar etc. However, RF components used in mobile communication base stations are the most power hungry components. It can be seen in Figure 1.1, that RF equipments (mainly PAs) consume almost 50 - 80 % ($\approx$ 65 %) of the total energy [6]. Hence, it is one area where we can focus in order to reduce the total energy consumption.

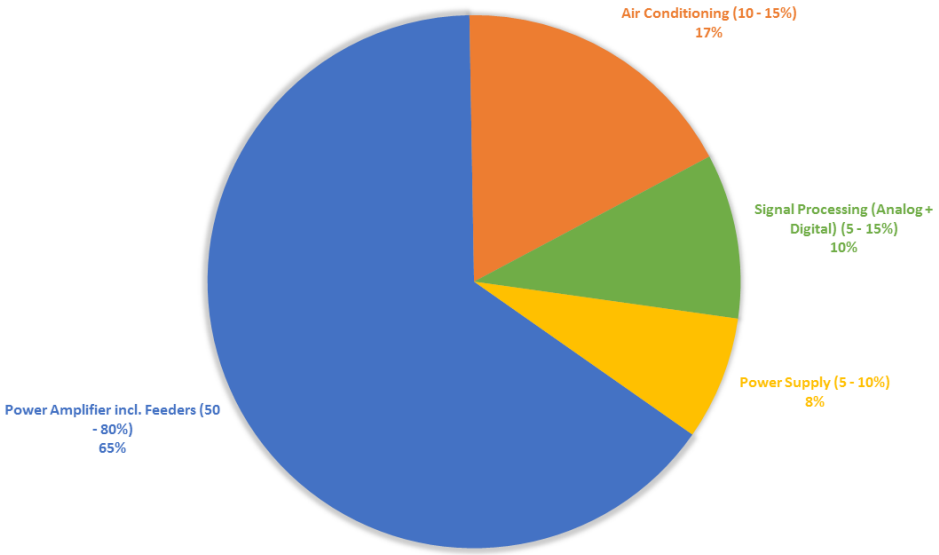


Figure 1.1: Power Consumption at Radio Base Stations [6]

Increasing complexity in modulation schemes of transmitted signals aimed at

providing higher spectral efficiency, added to the fact that the growing advancements in 5G telecommunication which makes use of MIMO systems will increase the power demands in the base station, calls for even more stringent power consumption requirements. Power amplifiers tend to have a highest efficiency point which usually does not coincide with the most linear region of operation. In order to compensate for the non-linear behaviour of PAs operating at maximum efficiency, Digital Pre-distortion (DPD) technique is used. Higher the non-linearity of a PA, more linearisation has to be done, which increases the complexity of DPD circuitry and implementation, which in turn increases the power consumption of the PA circuit as a whole.

1.2 Thesis Contribution

Energy efficient PAs are therefore needed to reduce the power consumption of modern and future communication standards which thereby help in avoiding the excessive heating of the products. This will in turn also be helpful in reducing the carbon footprint. In order to simplify the design procedure, simulations and measurements of PAs are usually done with simple signals such as continuous wave (CW) or two-tone, but in reality the communication signals, such as LTE, are complex in nature [4]. Since the correlation for the PA performance between simple and complex signal is complicated and non-intuitive, it will lead to a sub-optimal design [5]. Furthermore, often a compromise between the linearity and efficiency has to be made since it might not be possible to linearise the most efficient PA. This is mainly due to the fact that the complexity of DPD is limited in real world applications. This means that PAs should be designed for the intended signals and this is studied, measured and verified using a simple(memoryless) DPD in this thesis. Consequently, it will lead to a reduced power consumption by DPD as well as a more efficient design of a PA.

1.3 Thesis Outline

The thesis discusses the CW and two-tone load-pull design methods for Doherty PAs. In Chapter 2, a brief description of Doherty Power Amplifier can be found, while in Chapter 3, basic concepts of load-pull measurement system are discussed. The CW and two-tone load-pull design methods for Doherty PAs are shown in Chapter 4 and we also get introduced to the IMD products and its effects on the signal. In Chapter 5, the study is then extended to evaluate the design of a DPA using two-tone signals for different trade-off conditions between efficiency and linearity. Furthermore, the possibility of designing an optimal DPA is investigated in the chapter. The results obtained from the investigation provided insights on the effects of IMD products at the output of Doherty PA. This lead to the investigation of a simplified approach to possibly predict the IMD components of the DPA even without the need to actually design it, which is discussed in Chapter 6. Chapter 7 presents the emulation of a Doherty Power Amplifier through Chalmers Weblab system using a classical Doherty combiner parameters. In Chapter 8, the approach is extended to two-tone signals.

Chapter 2

Doherty Power Amplifiers

The Doherty Power Amplifier was first introduced in 1936 by William H. Doherty of Bell Telephone Laboratories [7]. This chapter first introduces the operation of a conventional Doherty PAs. The Doherty amplifier is a modified form of a class B/AB amplifier, along with a class C amplifier, that is used as RF power amplifier to amplify RF signals in a linear and efficient way. It operates according to a simple concept: a main (or carrier) amplifier is used to drive the load when the input power is low while an auxiliary (or peaking) amplifier, along with the main amplifier, is used to drive the load when the input power is higher than a specified threshold. This way we can achieve high efficiency peaks at two power levels, one when input power level is low and another when input power is maximum. The current data transmission methods such as UMTS, LTE have high density constellations, which in turn corresponds to increasing peak to average power ratio (PAPR), and this makes it difficult for conventional power amplifiers with single class of operation to provide high efficiency without any distortion of the signal. This makes Doherty PAs the preferred choice of power amplifier for many applications.

2.1 Operation of a Conventional Doherty PA

The incoming signal is split into two, the -3 dB power split being one of the preferred ways, even though any arbitrary power split can be applied. The main (or carrier) amplifier is usually a Class A, AB or B amplifier and provides gain at any power level while the auxiliary (or peaking) amplifier is a Class C amplifier as it only handles higher power levels. This is achieved by biasing the auxiliary amplifier in such a way that it only operates when a large input signal is presented to the input of the amplifier. This proves the importance of the Doherty PA in modern era of wireless communications due to the enhancement in efficiency that it can provide [11].

The outputs of the main amplifier is combined with the output of the auxiliary amplifier and an impedance transformer using a 50 Ω, quarter wave transmission line. When main amplifier is under operation at lower power levels (back-off, BO), the auxiliary amplifier is in non-conducting state and the quarter wave transformer sees the optimum load, Z_{opt} (e.g. 50 Ω), at the end. This means that the optimum load, Z_{opt} (50 Ω) is transformed to 25 Ω by 35 Ω transmission line which is inverted by the 50 Ω quarter wave transformer such that the main amplifier sees twice the

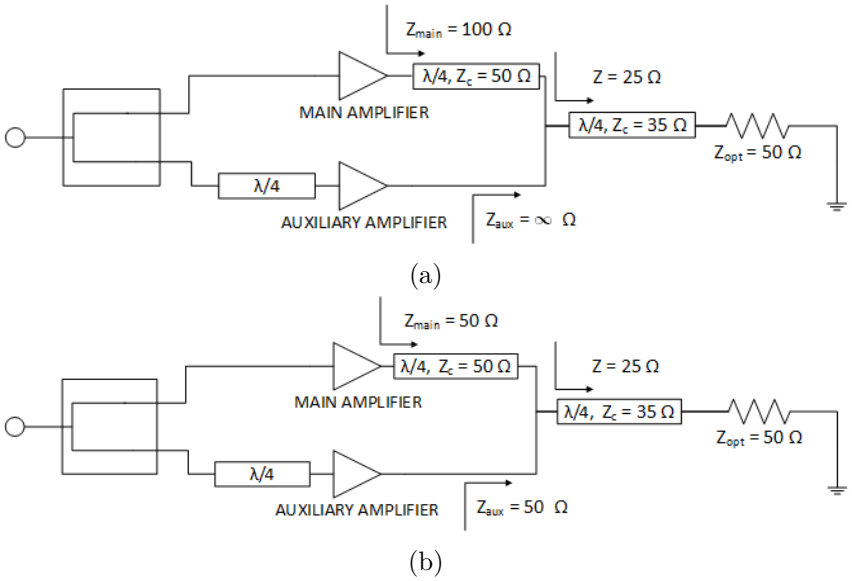


Figure 2.1: Schematic of conventional DPA operation in (a) Back-off [12] (b) Full Power [12]

optimum impedance, $2Z_{opt}$ (100 Ω), at its output. This is shown in Figure 2.1a.

When the auxiliary amplifier starts to conduct beyond this power level, the current flowing from the output of the auxiliary amplifier increases which results in decreasing load impedance of main and auxiliary amplifiers from $2Z_{opt}$ (100 Ω) to Z_{opt} (50 Ω) and ∞ to Z_{opt} (50 Ω), respectively [12]. This is shown in Figure 2.1b. This indicates that the load line becomes steeper since slope of load line is given by $\frac{1}{Z_{load}}$. This effect is termed as *load modulation*, which allows for constant voltage swing at high powers for the main amplifier. In order to accommodate for load modulation due to the quarter wave transformer at the output of the main amplifier, we include a similar quarter wave transformer at the input of the auxiliary amplifier. Both the main and the auxiliary amplifier reaches saturation at maximum power level (full-power, FP). This architecture allows for two efficiency peaks to show up - one efficiency peak at back-off (BO) power level and another peak at full power (FP), as shown in Figure 2.2.

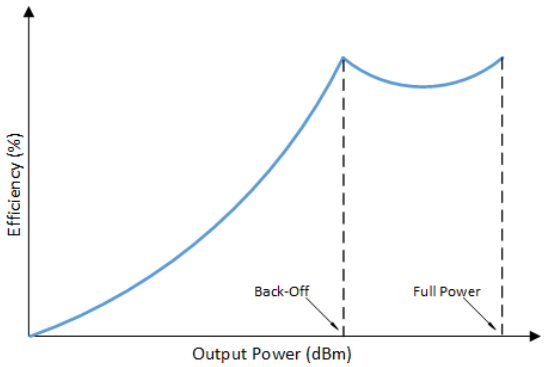


Figure 2.2: Doherty PA efficiency curve

Chapter 3

Load-Pull Measurement System

In this chapter the fundamental principle behind load-pull measurement system and the different types of load-pull system will be discussed.

3.1 Load-Pull Basics

Load-Pull is one of the most effective tools in characterizing high power devices in non-50 Ω environment. Load-Pull can be described as the process in which the impedance presented to a device under test (DUT) is varied to evaluate its performance in order to find the optimum load. Hence it is arguably the most common technique used in the designing of power amplifiers. The optimum load is determined by adjusting the load-reflection coefficient, Γ_L, that is seen by the DUT. Parameters such as transducer power gain (G_T), power delivered to the load (P_{del}), drain efficiency (η) and power added efficiency (PAE) are evaluated for different load impedances presented to the DUT by analyzing the contours of the parameters on a Smith Chart. Load-Pull technique can be broadly classified into two: (i) Passive Load-Pull and (ii) Active Load-Pull.

3.1.1 Passive Load-Pull

The passive load-pull technique primarily relies on slide screw tuners in order to vary the reflection coefficient presented at the output of DUT. The system makes use of a mechanical sliding probe that can be moved in a pair of possible directions - up and down, right and left - which in turn changes the phase of the reflections thereby varying the impedance presented at the DUT [13]. A simplified diagram of a passive load-pull system is shown in Figure 3.1.

The main advantages of the system is its simplicity of usage and also its high power handling capacity [13]. However, its disadvantages includes the restriction induced by the mechanical movement of the slider that causes losses which in turn limits the maximum reflection coefficient that can be presented to the DUT, and also the limitation in bandwidth of the tuner [13].

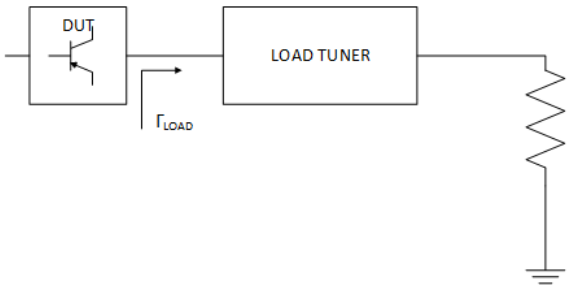


Figure 3.1: Simplified block diagram of a passive load-pull [14]

3.1.2 Active Load-Pull

Active load-pull provides more flexibility by removing the mechanical slider and instead injecting real signals towards the DUT [9][10]. This can help map areas which are beyond the smith chart which would not be possible with passive load-pull. The two main architectures of active load-pull are closed-loop active load-pull and open-loop active load-pull.

Closed-loop active load-pull is done by reflecting the signal back into the DUT after readjusting its magnitude and phase [13]. This is shown in Figure 3.2a. It is useful to get fast results through real time adjustments of the reflection coefficient. It has the advantage of not requiring an additional signal source [13]. The disadvantages include producing possible oscillations in the output of DUT due to the uninterrupted continuous wave in the feedback loop, which may damage the DUT.

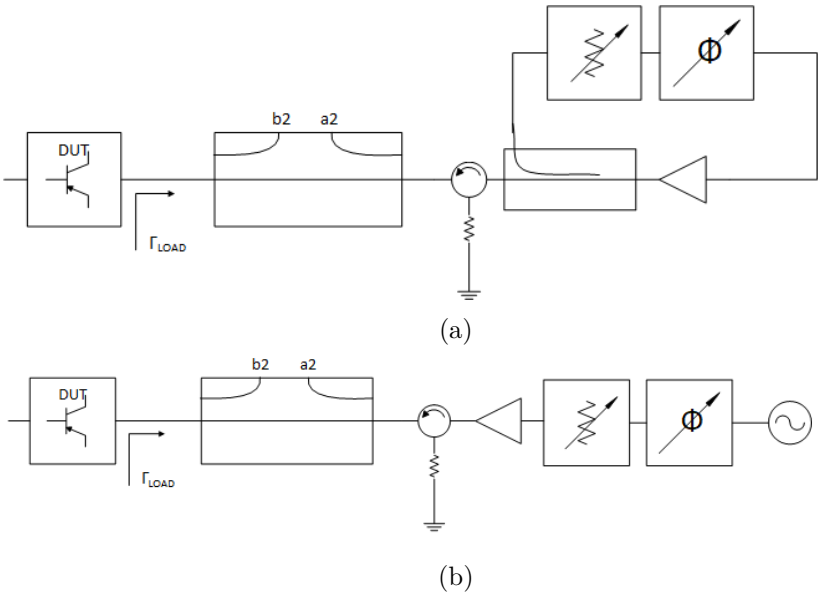


Figure 3.2: Simplified block diagram (a) a closed-loop active load-pull [14]. (b) an open-loop active load-pull [14].

In open-loop active load-pull systems, a signal generator is used in order to inject the signal towards the DUT. This is shown in Figure 3.2b. This will help achieve the desired load reflection coefficient in a much more controlled way since the amplitude and the phase of the signal presented at the output of the DUT are

independent of the signal generated at the output of the DUT. The open-loop active load-pull system has the advantage of not causing any oscillations and possibility of controlling the injected signal in a digital environment.

Chapter 4

Designing a Doherty Power Amplifier

The main goal is to design a Doherty power amplifier (DPA) using two-tone and modulated signal to demonstrate improved performance over the Doherty PA designed using a continuous-wave (CW). Therefore, a DPA is designed using a CW signal first and its performance is compared with the same DPA simulated using a two-tone signal. The following sections will describe in detail the design steps followed.

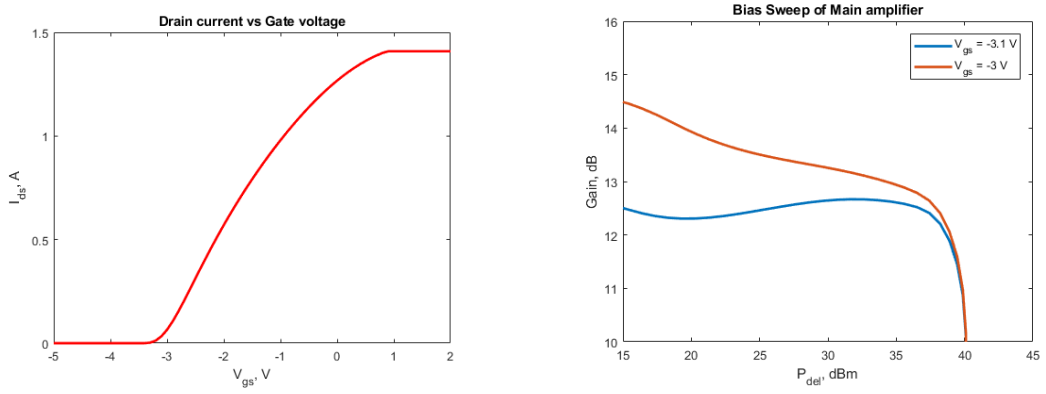
4.1 Doherty power amplifier design steps

The design of DPA includes two amplifiers, one operating as main amplifier and the other as auxiliary amplifier as discussed in Chapter 2. The circuit used in the design process is same as the one used to develop the test board in [8]. This circuit includes stabilizing network, harmonic terminations and bias network for a Cree-CGH40010F transistor operating at 2.14 GHz. The DPA was designed to be symmetrical which meant that the same device had to be used as main and auxiliary amplifier and also to have the input power split equally between them.

The DC bias point for main and auxiliary amplifiers were selected in the first step. The Cree-CGH40010F transistor is designed to operate at a drain-source voltage, V_{ds}, of 28 V and the absolute minimum and maximum ratings for gate-source voltages, V_{gs}, are -10 V and 2 V, respectively. To bias the transistor in a safe range of operation, the V_{gs} sweeps ranging from -8 V up to 1 V was done for a fixed V_{ds}. In order to find an optimum bias level for Class B operation the bias sweep was narrowed down to a maximum of -2 V, beyond which the transistor enters Class A operation. From Fig.4.1a we can see that the V_{gs} has to be near -3 V in order to operate main amplifier in a deep class AB region. In order to select a bias point in the range, the gain response of the amplifier can be plotted for different bias points. From Fig.4.1b it can be seen that even though V_{gs} = -3.1 V gives lesser gain than V_{gs} = -3 V, it gives a more flatter gain over wider range of delivered power.

The V_{gs} of the auxiliary amplifier was selected by performing a bias point sweep similar to the main amplifier. The criterion for selecting the bias point was that the auxiliary amplifier should turn on once the input power level exceeds the back-off

(BO) power level. However, it also has to operate in class C region and turn on the auxiliary amplifier when the main amplifier approaches 1 dB compression point. Hence the bias level had to be selected taking these factors into consideration. A bias sweep was done for V_{gs} ranging from -5 V up to -8.5 V to determine the class C operation mode. The value of V_{gs} that satisfied the above criteria was found to be -8.1 V.



(a) (b)

Figure 4.1: (a) I_{ds} vs V_{gs} curve to find the bias point of the amplifier (b) Power sweeps of the main device for bias point of -3 V and -3.1 V

4.1.1 Design using CW

After determining the gate bias point for the main and auxiliary amplifier, load-pull simulation was done for both the amplifiers to determining the optimum load-impedance, Z_{opt}, for the two power levels - Back-off (BO) and Full-Power (FP). The BO input power level was set as 21 dBm and the FP input power level was set at 29 dBm. The Z parameters of the main and auxiliary amplifier at 2.14 GHz are shown in Table 4.1. The radius of sweep was kept to cover the whole area of the Smith chart initially and once the PAE and P_{del} contours were found, the radius was decreased to find a more accurate point in the Smith chart. The load-pull for main amplifier was carried out by giving importance to PAE at BO state since it is one of the main design criteria. This is because, the DPA will be operating at BO for most of the time for a modulated signal, and hence it is required to have high efficiency at BO. On selecting a load from the load-pull contours that gives the desired PAE, the source impedance is taken as the conjugate of input impedance for the optimum load impedance. A similar approach is carried out for the load-pull of auxiliary amplifier as well. The load-pull simulation data used to design the Doherty power amplifier us shown in Table 4.2.

The load-pull simulation data is a result of four different combinations - main device at BO, main device at FP, auxiliary device at BO and auxiliary device at FP. The auxiliary device at BO will not be conducting and hence it can be represented as S-Parameter of auxiliary amplifier in off state.

Table 4.1: Small signal Z parameters of the main and auxiliary amplifiers at 2.14 GHz

$Amplifier$	Z_{11}	Z_{12}	Z_{21}	Z_{22}
Main	10.912+j7.314	-0.110-j1.451	128.278-j21.398	5.904-j8.878
Auxiliary	5.013+j3.930	-0.185-j1.359	-0.185-j1.359	0.657-j12.042

Table 4.2: CW Load-Pull Data

$Op.State$	P_{avs} (dBm)	P_{del} (dBm)	$PAE(\%)$	$Z_{L,opt}(\Omega)$	$Z_s(\Omega)$
Main BO	21	36.76	61.24	4.423+j3.727	9.95-j22.7
Main FP	29	41.26	72.83	12.511-j0.770	9.95-j22.7
Aux FP	29	39.17	62.92	4.883+j1.221	4.31-j9.94

The load-pull data is then used to obtain the Z parameters of the two port output combiner network required to design the DPA, as mentioned in [4]. The results are shown in Table 4.3. The input phase delay of the phase shifter was calculated to be -84.3°. The simulated gain and efficiency curves of the designed DPA can be seen in Fig.4.2.

Table 4.3: Calculated 2-Port Z parameters of the output combiner at 2.14 GHz

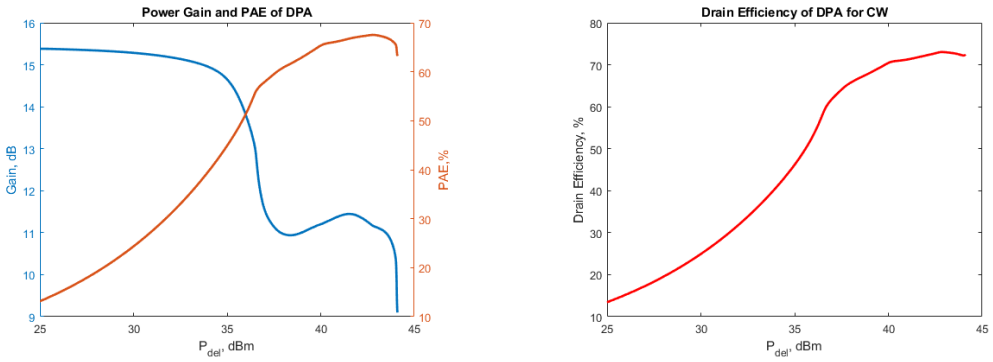
	Z_{11}	Z_{12}	Z_{21}	Z_{22}
2-Port Combiner	0.084+j0.908	-1.077-j9.907	-1.077-j9.907	12.775-j1.873

The predicted Doherty PA performance from the load-pull data and the output combiner network is shown in Table 4.4.

Table 4.4: CW Doherty Performance

	$Back-Off$	$Full\ Power$
P_{del} (dBm)	36.7	43.7
G_T (dB)	12.7	11.3
PAE (%)	59.6	68.8

The simulated Doherty PA results are shown in the Fig. 4.2. It can be seen that the simulation agrees with the predicted values and high efficiency was achieved as intended in the design goal.



(a) (b)

Figure 4.2: CW simulation of DPA: (a) Power-added-efficiency and Gain plots of DPA across different output power levels (b) Drain efficiency across different output power levels

The same Doherty PA was also simulated with a two-tone signal as input to compare the parameters obtained from the CW signal. The observed DPA performance is shown in Table 4.5 and the corresponding simulated results are shown in Fig. 4.3.

Table 4.5: Two-Tone Doherty Performance

	$Back-Off$	$Full\ Power$
P_{del} (dBm)	33.9	40.7
G_T (dB)	12.9	11.3
PAE (%)	45.5	63.0
IMD3 (dBc)	-25.3	-19.5
IMD5 (dBc)	-34.4	-32.4

4.1.2 Design using Two-Tone

The two tone Doherty simulations were done by fixing the same bias point as used for the CW Doherty design. In order to achieve this, the two-tone load-pull simulations had to be carried out. Care must be taken regarding the power levels used in the simulations since the input power will be split equally among the two tones and this has to be taken into consideration while taking the results of the two-tone load-pull. Additionally, in two-tone load-pull simulations, the intermodulation distortion (IMD) products are also taken into consideration and its contours are plotted in the smith chart in addition to the PAE and power delivered contours. Off all the IMD products, the third order IMD (IMD3) components are of most importance since they lie near to the two fundamental frequency components.

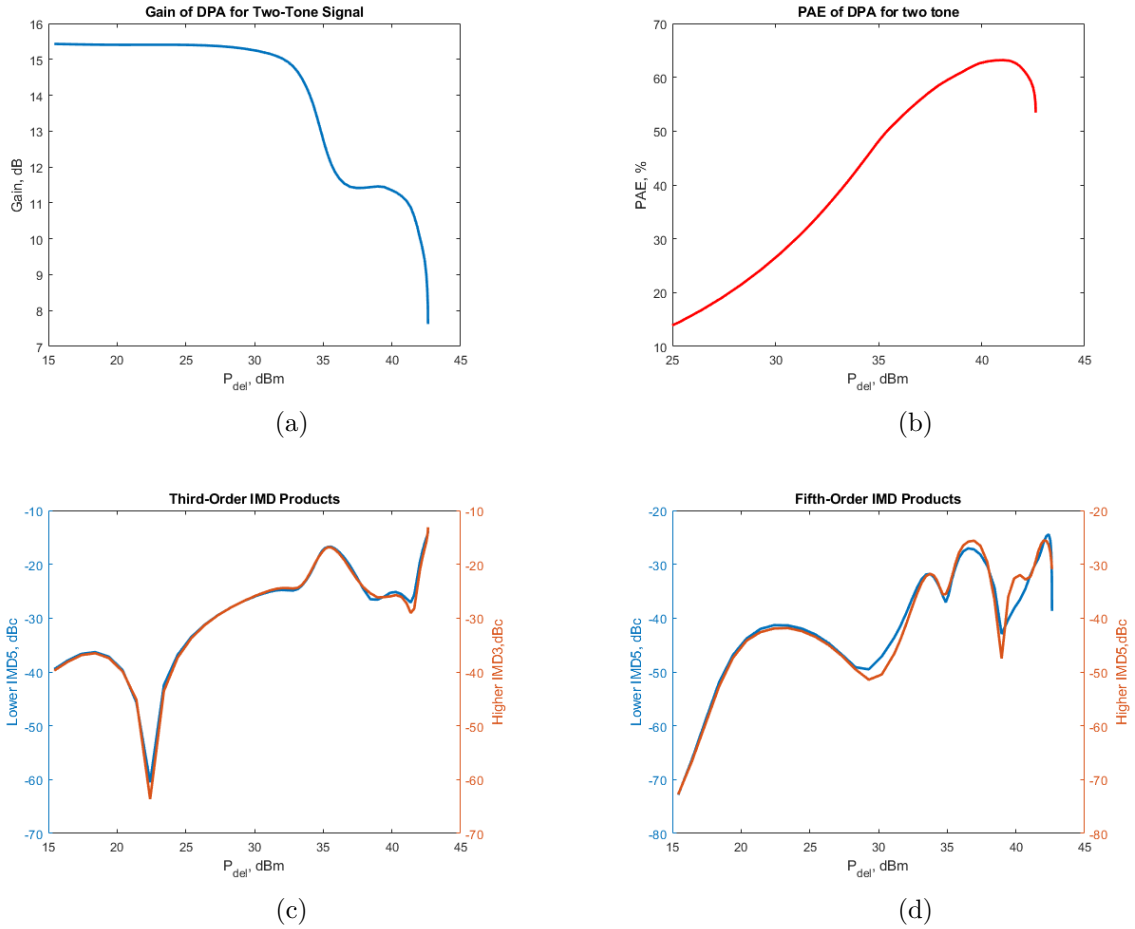


Figure 4.3: Two tone simulation of the same DPA: (a) Gain curve of DPA across different output power levels (b) Power added efficiency across different output power levels (c) Third Order IMD Products (d) Fifth Order IMD Products

4.1.2.1 Intermodulation Distortion

The two tones when given as input to a nonlinear system, it will give rise to not only harmonic frequency components but also to additional components that arise from sum and difference between the fundamental frequencies. These additional products are called intermodulation products. If the fundamental frequencies are represented as f_1 and f_2, then the distortion products will be produced at frequencies $mf_1 \pm nf_2$ where m and n = 0, 1, 2, 3,.. [16]. The order of the IMD products will be given by the sum of the coefficients, m and n. This can be understood clearly from the following table.

Table 4.6: Illustration of 2^{nd} and 3^{rd} Order IMD Products [16]

2^{nd} *Order IMD*	3^{rd} *Order IMD*
$f_1 - f_2$	$2f_1 + f_2$ & $2f_2 + f_1$
$f_1 + f_2$	$2f_1 - f_2$ & $2f_2 - f_1$

It can be seen that the third order IMD products (IMD3) has to be considered while doing the two-tone load-pull and thus it will be included as an important and additional design parameter for a Doherty PA. The IMD3 is simply the difference between the powers of fundamental tones to the third order components in logarithmic scale. The load-pull simulation data and design of DPA using two-tone signals is discussed in detail in Chapter 5.

Chapter 5

Design of Doherty Power Amplifier for Different Trade-Offs

The design of Doherty PA using two tone signals were studied for three different trade-offs. The design procedure followed were discussed in the section 4.1.2 of Chapter 4. The load-pull simulations were done for three different trade-offs:

- Doherty design with equal emphasis for both efficiency and linearity
- Doherty design with emphasis on efficiency
- Doherty design with emphasis on linearity

The design trade-offs are only considered for load-pull simulation of main amplifier. This is because the average power of a modulated signal is mainly concentrated at the back-off (BO) power level and that makes it of particular interest. Also, in BO condition the linearity contribution of main amplifier is likely to dominate over the auxiliary amplifier since the auxiliary amplifier is in non-conducting state. Hence, the linearity at BO is most likely to have the biggest impact for the overall linearity of a modulated signal.

5.1 Aim of the study for different trade-offs

The objective of this study is to determine the impact of each trade-off in designing of a Doherty power amplifier and also to investigate the possibility of designing a Doherty power amplifier using the combination of data that gives the best linearity results.

5.2 Simulated results for different trade-offs

In order to achieve the above said goals, the two-tone load-pull was done for each of the different trade-offs at a fixed power level initially, as discussed in section 5.2.1, and later it was extended for different output power levels, as discussed in section 5.2.3.

5.2.1 DPA design for a fixed output power levels

The two-tone load-pull simulations were done for a fixed power level. The center frequency was kept as 2.14 GHz and the two tones were separated by 2 MHz, which meant that the fundamental frequencies of the two tones are 2.139 GHz and 2.141 GHz. The input power for back-off was set to 21 dBm which meant that the power of the two fundamental tones will be 18 dBm. Similarly, the input power for full power was set to 29 dBm which meant that the power of the fundamental tones are set to 26 dBm. The load-pull simulation results of the main amplifier and auxiliary amplifier when operating at full power are given in the Table 5.1.

Table 5.1: Two-Tone Load-Pull data of Main and Auxiliary amplifier at FP

	$Main\ Amplifier$	$Auxiliary\ Amplifier$
P_{del} (dBm)	40.55	38.2
PAE (%)	58.39	51.6
$Z_L(\Omega)$	14.03-j5.07	5.47-j2.47
$Z_s(\Omega)$	12.20-j14.88	4.04-j8.43
IMD3 (dBc)	-11.43	-20.59
IMD5 (dBc)	-25.68	-13.64

5.2.1.1 Doherty design with equal emphasis for efficiency and linearity

The two-tone load-pull results for the main amplifier, simulated by taking an equal trade-off between the efficiency and linearity are shown in Table 5.2. The trade-off was done by selecting a suitable load reflection coefficient which lies on the intersection of PAE and IMD3 contours in the smith chart.

Table 5.2: Two-Tone Load-Pull data of Main at BO (for equal emphasis on PAE and linearity)

	$Main\ Amplifier$
P_{del} (dBm)	36.45
PAE (%)	50.23
$Z_L(\Omega)$	17.69+j5.67
$Z_s(\Omega)$	12.20-j14.88
IMD3 (dBc)	-29.52
IMD5 (dBc)	-37.04

Table 5.3: Calculated 2-Port Z parameters of the output combiner at 2.14 GHz *for equal emphasis on PAE and linearity*

	Z_{11}	Z_{12}	Z_{21}	Z_{22}
2-Port Combiner	18.529+j11.841	-14.243-j1.615	-14.243-j1.615	10.963-j18.813

The calculated two-port network parameters for the Doherty PA for the trade-off condition mentioned in this section is shown in Table 5.3. The input phase delay of the phase shifter was calculated to be -56.9°. The Doherty PA performance from the load-pull data and the output combiner network is shown in Table 5.4 and the simulation results are shown in Fig. 5.1.

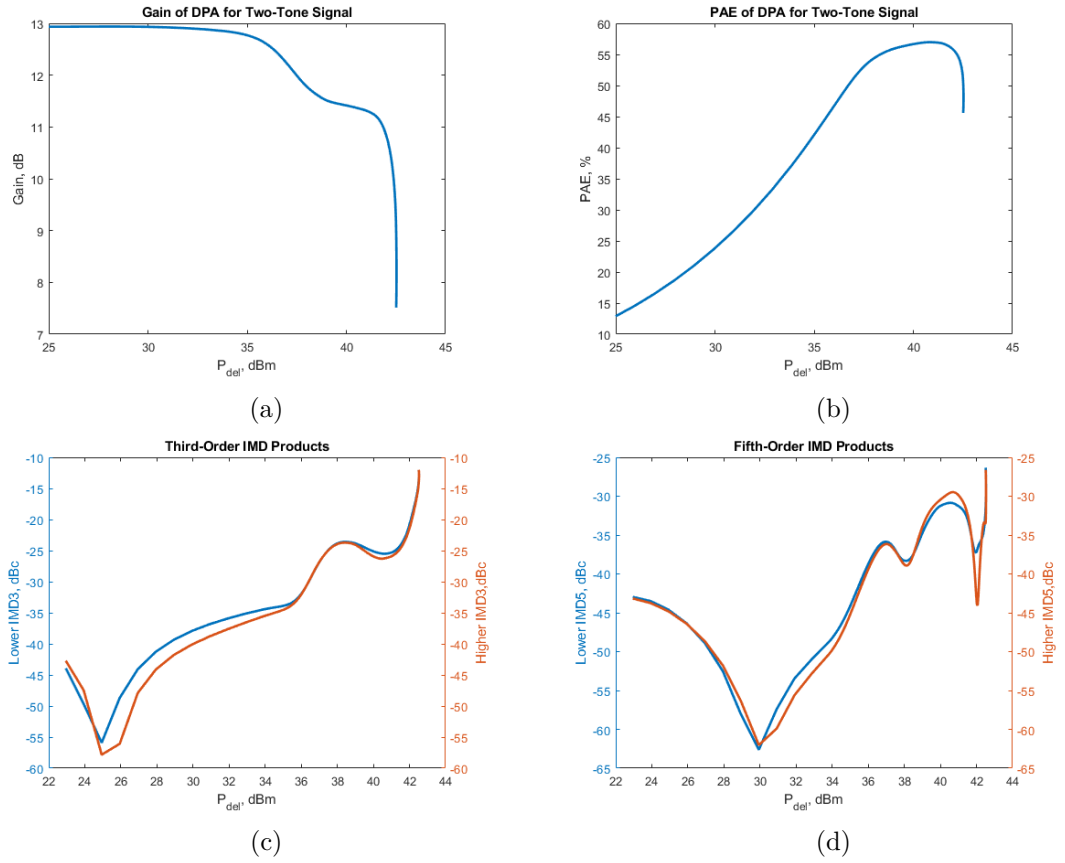


Figure 5.1: Equal trade-off between PAE and linearity: (a) Gain of DPA (b) PAE of DPA (c) Third Order IMD Products (d) Fifth Order IMD Products

The results show that an acceptable trade-off between the efficiency and linearity has been considered as the main amplifier has not reached 1 dB compression point at back-off and also provides satisfactory IMD3 levels. Hence, this can be used as a benchmark for the remaining two trade-off situations to be compared with.

Table 5.4: Two-Tone Doherty Performance for equal trade-off between PAE and Linearity

	$Back-Off$	$Full\ Power$
P_{del} (dBm)	36.45	42.3
PAE (%)	48.9	54.4
G_T (dB)	12.45	10.29
G_{comp} (dB)	0.9	3.05
IMD3 (dBc)	-29.54	-17.52
IMD5 (dBc)	-36.69	-35.24

5.2.1.2 Doherty design with emphasis on PAE

The two-tone load-pull results for the main amplifier, simulated by giving more emphasis on efficiency. This meant that the load impedance chosen was closer to the highest efficiency point compared to that of the IMD3 contours. This was done so as to ensure that the linearity performance of the DPA should not be below an acceptable level. The load-pull data is shown in Table 5.5.

Table 5.5: Two-Tone Load-Pull data of Main at BO (for emphasis on PAE)

	$Main\ Amplifier$
P_{del} (dBm)	36.65
PAE (%)	58.90
$Z_L(\Omega)$	10.75+j4.56
$Z_s(\Omega)$	12.20-j14.88
IMD3 (dBc)	-23.35
IMD5 (dBc)	-35.03

The calculated two-port network parameters for the Doherty PA for the trade-off condition mentioned in this section is shown in Table 5.6. The input phase delay of the phase shifter was calculated to be -70°. The Doherty PA performance from the load-pull data and the output combiner network is shown in Table 5.7 and the simulation results are shown in Fig. 5.2.

Table 5.6: Calculated 2-Port Z parameters of the output combiner at 2.14 GHz *with emphasis on PAE*

	Z_{11}	Z_{12}	Z_{21}	Z_{22}
2-Port Combiner	4.723+j8.010	-8.466-j10.062	-8.466-j10.062	15.196-j7.122

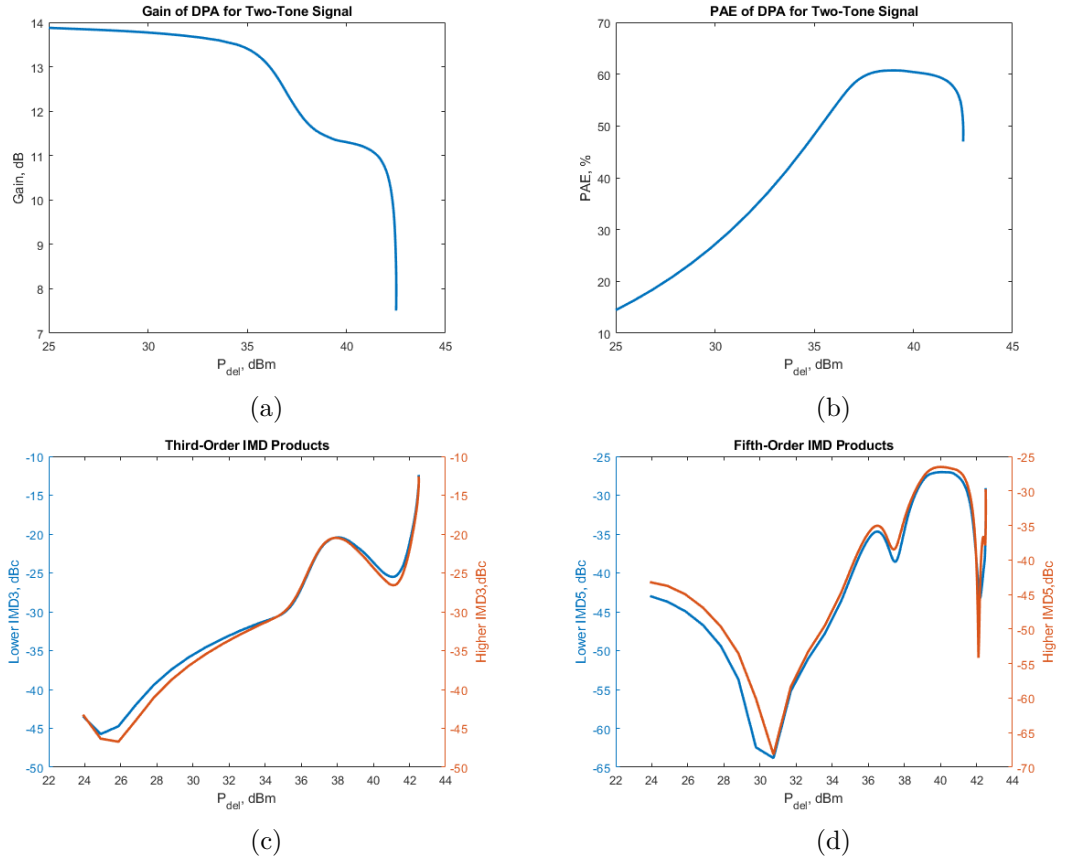


Figure 5.2: Emphasis on PAE: (a) Gain of DPA (b) PAE of DPA (c) Third Order IMD Products (d) Fifth Order IMD Products

Table 5.7: Two-Tone Doherty Performance with emphasis on PAE

	$Back-Off$	$Full\ Power$
P_{del} (dBm)	36.67	42.2
PAE (%)	56.96	56.56
G_T (dB)	12.67	10.2
G_{comp} (dB)	1.63	3.91
IMD3 (dBc)	-23.28	-19.09
IMD5 (dBc)	-34.88	-42.79

It can be seen from Fig. 5.2c and Fig. 5.2d that the linearity performance of the DPA gets compromised as compared to the DPA operation when equal trade-off between efficiency and linearity. This is because, in order to obtain high efficiency at both back-off and at full power, the main and auxiliary amplifiers are pushed much into compression region thereby making it more non-linear. This distorts the signal and gives rise to higher ratio between the third order products and the fundamental frequency components.

5.2.1.3 Doherty design with emphasis on linearity

The two-tone load-pull results for the main amplifier, simulated by giving more emphasis on linearity. This meant that the load impedance chosen was closer to the best linearity point in IMD3 contours compared to that of the PAE contours. This was done so as to ensure that the efficiency performance of the DPA should not be below an acceptable level. The load-pull data is shown in Table 5.8.

Table 5.8: Two-Tone Load-Pull data of Main at BO (for emphasis on linearity)

	$Main\ Amplifier$
P_{del} (dBm)	34.88
PAE (%)	30.91
$Z_L(\Omega)$	37.66+j9.56
$Z_s(\Omega)$	12.20-j14.88
IMD3 (dBc)	-38.72
IMD5 (dBc)	-47

Table 5.9: Calculated 2-Port Z parameters of the output combiner at 2.14 GHz *with emphasis on linearity*

	Z_{11}	Z_{12}	Z_{21}	Z_{22}
2-Port Combiner	12.498+j42.012	-20.832-j32.481	-20.832-j32.481	34.622+j3.813

The calculated two-port network parameters for the Doherty PA for the trade-off condition mentioned in this section is shown in Table 5.9. The input phase delay of the phase shifter was calculated to be -23.1°.

Table 5.10: Two-Tone Doherty Performance with emphasis on linearity

	$Back-Off$	$Full\ Power$
P_{del} (dBm)	35	42.5
PAE (%)	29.82	52.65
G_T (dB)	11	10.54
G_{comp} (dB)	1.02	1.3
IMD3 (dBc)	-34.36	-19.31
IMD5 (dBc)	-46.73	-26.29

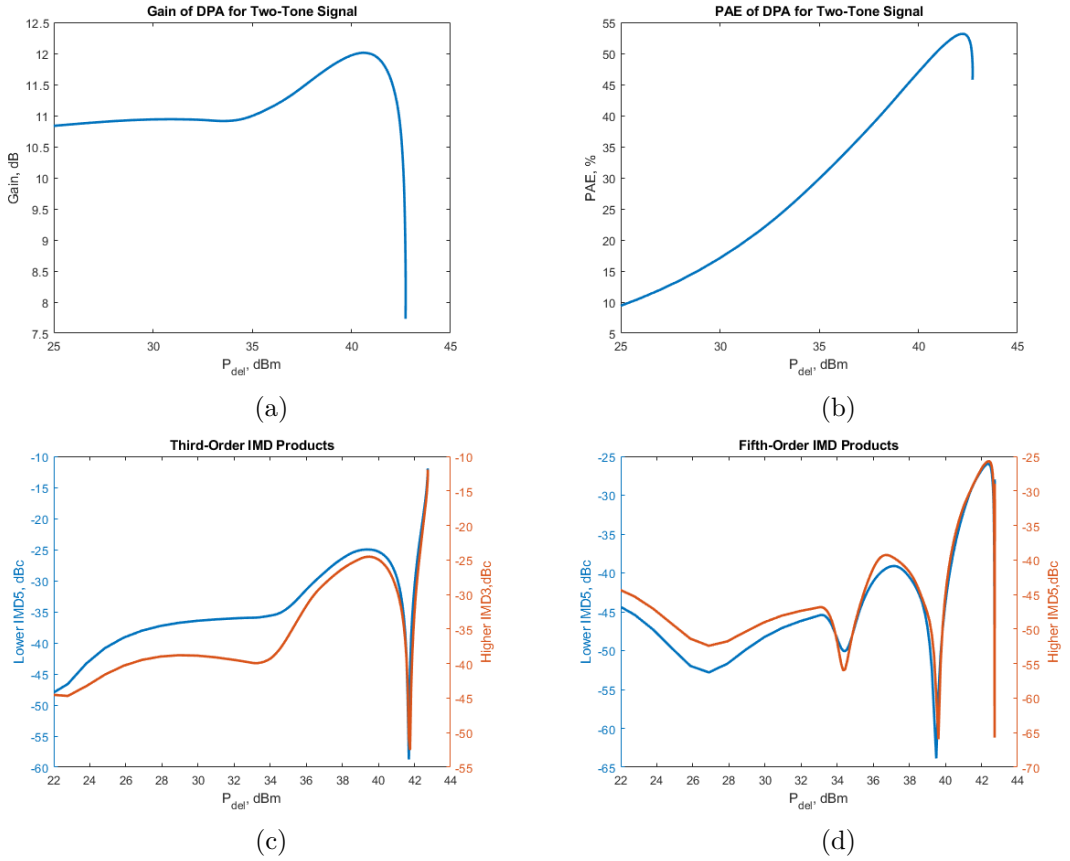


Figure 5.3: Emphasis on IMD3: (a) Gain of DPA (b) PAE of DPA (c) Third Order IMD Products (d) Fifth Order IMD Products

The Doherty PA performance from the load-pull data and the output combiner network is shown in Table 5.10 and the simulation results are shown in Fig. 5.3. It is interesting to note that, when design based on improved linearity is done, we manage to obtain a very low IMD3 component near to the back-off power region and also near to the full power region. The IMD3 "dip" near to the full power region is of particular interest since the DPA is in a non-linear region of operation as both the amplifiers - main and auxiliary - approaches saturation at full power and this provides us an opportunity to find a good trade-off point for the design of a Doherty PA.

5.2.2 Conclusions on design of DPA for different trade-offs with fixed power levels

The different studies provides an insight into the performance of a Doherty based on two-tone load-pull simulations. The study on linearity and the results shows the possibility of designing a Doherty by considering the same different trade-offs for main and auxiliary amplifiers at full power. This then can be used to design a Doherty power amplifier based on best of all the results thereby providing the best results at back-off and at full power. This is the motivation behind analyzing the DPA design for each trade-off for different output power levels and this will be

discussed in section 5.2.3.

5.2.3 DPA design for different output power levels

This study was done as an extension of the DPA design based on different trade-offs mentioned in section 5.2, where we mainly concentrated only on Main amplifier operating at back-off power level. The possibility of designing a DPA based on best results from each trade-offs for the back-off and maximum power levels can possibly be investigated in this way. In order to add more flexibility to the design the input power level was varied from 10 dBm to 35 dBm which meant that there was a higher degree of freedom while doing the load-pull. The bias point of the amplifiers, the fundamental frequency of operation and the frequency spacing were all kept the same as the previous setup. Initially the two-tone load-pull for different trade-offs were done only for the Main amplifier operating at Back-Off. But it was found that the linearity and the efficiency performance of the DPA can be improved by subjecting the main and auxiliary amplifier to the operate at different trade-off conditions at full power. The methodology of investigation is illustrated in the Fig. 5.4.

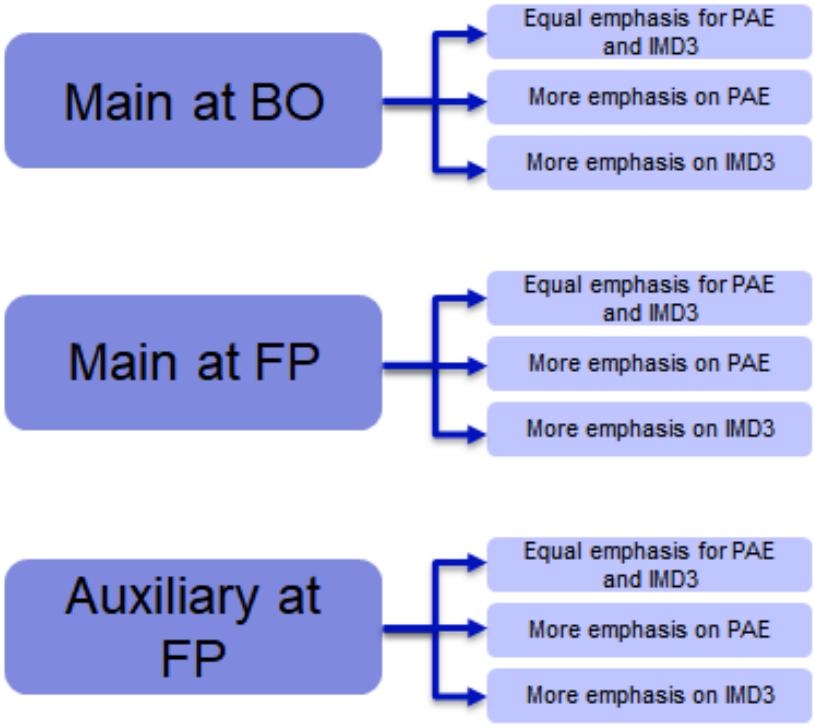


Figure 5.4: Illustration of different combinations of load-pull setup required for the study

For simplicity, 4 different output power levels for main and auxiliary amplifiers operating at back-off and full power were carried out for each trade-off condition, for most part. This meant that 64 different combinations were possible for each trade-off condition in addition to the combinations between the trade-off conditions for

each power level. The optimum impedance of main amplifier operating at back-off was calculated by selecting a suitable point that satisfies each trade-off conditions as specified in the sections 5.2.1. This process was carried out for 3 more different power levels. Similarly, the optimum impedance for a given output power level for main amplifier and auxiliary amplifier operating at full power were selected by choosing a suitable point that was closer to the center of PAE contours or IMD3 contours for trade-offs emphasizing more on efficiency and linearity, respectively. The same step was carried out for different power levels for that specific trade-off.

The Table 5.11 shows the source and load impedances that were selected for different operating conditions of main and auxiliary amplifiers for each trade-off. The source impedance was kept a constant after finding a suitable source impedance initially in order to simplify the procedure. The optimum load impedance was verified by selecting the sample points that provided the best results for the respective trade-off condition for each output power level. The difference in the optimum parameters due to changing load impedance was found to be negligible to obtain the best results, and hence it was decided to fix on one particular load impedance. However, this was not the case while analyzing the trade-off for emphasis on IMD3 for auxiliary amplifier. The optimum results for the trade-off for the auxiliary amplifier operating at full power were different for different output power levels. This can be seen in the cell describing the load impedance of auxiliary amplifier at FP as the output power is mentioned for which the specific load impedance provided optimum results is mentioned along with it.

Table 5.11: Source and Optimum load impedances of the main and auxiliary amplifier for different trade-offs

		Emphasis on both PAE and IMD3	Emphasis on PAE	Emphasis on IMD3
	Z_s	Z_L	Z_L	Z_L
Main at BO	13.571-j16.929	11.286+j9.703	9.347+j5.198	34.202+j18.755
Main at FP	13.571-j16.929	16.454-j3.556	13.505-j5.959	13.594-j7.619
Aux. at FP	5.837-j8.28	7.733-j0.696	10.866-j0.401	17.716-j4.104

A comparison of simulated results for the main and auxiliary amplifiers for different trade-off conditions and power levels are provided in the Appendix A.

5.2.4 Conclusions on design of DPA for different trade-offs with different output power levels

An extensive study was done for both amplifiers for all possible combinations. The simulations provided interesting results for obtaining best linearity and efficiency. A design for DPA using the best results for each trade-off was tried but it was found that it will be difficult to implement a Doherty amplifier with flat gain since the main amplifier operating at FP and auxiliary amplifier operating at FP have vastly different gains for the best results. This is also partly due to the fact that the Doherty PA was designed using a fixed input power level instead of a fixed output.

This meant that it would be difficult to implement the Doherty PA that satisfies the design equations in [4]. Nevertheless, the results of Main amplifier at BO is still relevant as we can make use of it to improve the linearity at input powers lower than BO power level.

Chapter 6

Study of Doherty Power Amplifier For Linearity Improvements

6.1 Aim of the study

The conclusion from the study of different trade-offs paved the way to analyze the possibility of establishing a relation between the third order IMD components obtained from load-pull simulations of main and auxiliary amplifier to that of the third order IMD components at the output of Doherty amplifier. This would help in predicting the non-linear behaviour of a Doherty PA without having the requirement to design the DPA and thus it would enable for a much better linear DPA design.

6.2 Methodology for predicting the third order IMD products of a Doherty PA

In order to study the third order IMD components of the main and auxiliary amplifier, an "IMD3 Load-Pull" setup has to be designed. The first step towards the setup was to verify the IMD3 currents and voltages at the output of Doherty PA and at the output of main and auxiliary amplifiers. The following equations,

$$V_l = \hat{Z_{31}} I_m + \hat{Z_{32}} I_a + \hat{Z_{33}} I_l \tag{6.1}$$

$$I_l = -\left(\frac{V_l}{R_L}\right) \tag{6.2}$$

$$\implies V_l = \left[\frac{\hat{Z_{31}} I_m + \hat{Z_{32}} I_a}{1 + \left(\frac{\hat{Z_{33}}}{R_L}\right)}\right] \tag{6.3}$$

as shown in [4] were used to verify the output of Doherty PA. V_l and I_l are node voltage and current at the output of the Doherty PA, respectively. V_m and I_m, and V_a and I_a are node voltages and currents at the output of the main and auxiliary amplifiers, respectively. $\hat{Z_{31}}$, $\hat{Z_{32}}$ and $\hat{Z_{33}}$ are the Z-Parameters of the 3-Port network.

The Doherty PA simulated under FP was used for verification. The calculated V_l was 4.186∠114.391° V and the V_l at the output of simulated Doherty PA was 4.191∠114.541° V, which is found to agree closely.

The study of interaction between IMD3 components is carried out by analysis the interaction between the main and auxiliary amplifiers in form of incident and reflected waves through the two port network. The analysis is illustrated using Fig. 6.1.

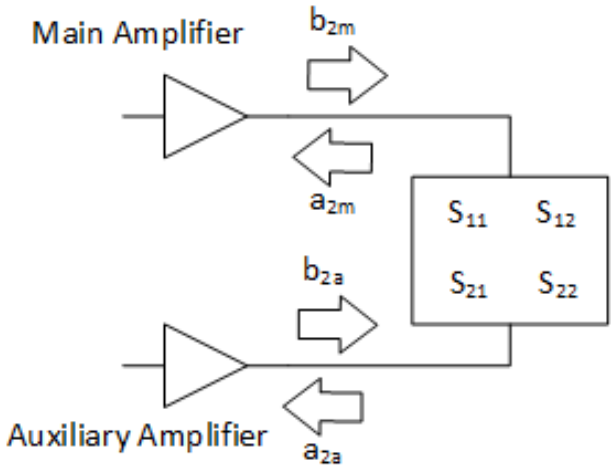


Figure 6.1: Simplified illustration of interaction between main and auxiliary amplifiers used for the analysis

The incident "power wave" from the output of the amplifier is denoted as b_2 while the reflected "power wave" from the load is represented as a_2. The subscripts m and a denote the *Main* and *Auxiliary* amplifiers respectively. The S-Parameters of the two-port network shown here are obtained from the calculated Z-Parameters of the Doherty PA. The interaction between the incident and reflected wave of the IMD3 products are believed to converge and produce the incident and reflected waves at the output of the Doherty PA. This coupling effect can be modelled according to the equations in [18].

6.2.1 IMD3 Load-Pull

The IMD3 load-pull setup was designed and setup for main and auxiliary amplifiers. The setup will allow for the IMD products to be load-pulled while the fundamental frequency and the corresponding harmonics and its IMD products will see a fixed load. The setup of load pull is shown in Fig. 6.3. The b_2 and a_2 values of IMD3 products of the main and auxiliary amplifiers are extracted from the IMD3 load-pull using the equations:

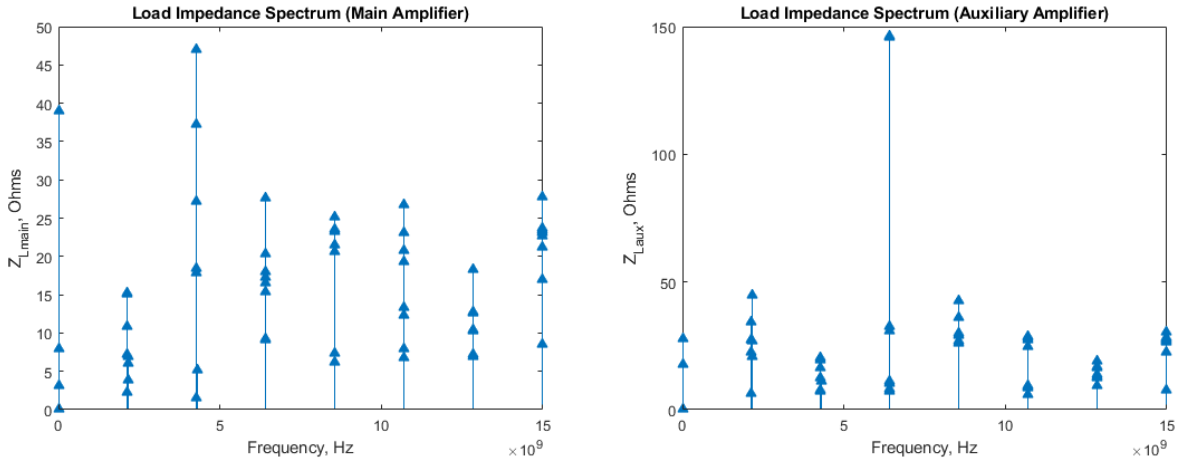
$$b_{2m} = \left(\frac{V_m + Z_0 I_m}{2}\right) \tag{6.4}$$

$$a_{2m} = \left(\frac{V_m - Z_0 I_m}{2}\right) \tag{6.5}$$

$$b_{2a} = \left(\frac{V_a + Z_0 I_a}{2}\right) \tag{6.6}$$

$$a_{2a} = \left(\frac{V_a - Z_0 I_a}{2}\right) \tag{6.7}$$

The load impedance spectrum of the main and auxiliary amplifiers operating in Doherty configuration is used to calculate the S_{11} parameters of for the s3p file is shown in Fig. 6.2.



(a) (b)

Figure 6.2: Load impedance spectrum of (a) main amplifier (b) auxiliary amplifier

The Γ radius for the load-pull sweep was made to cover areas beyond the smith chart as well.

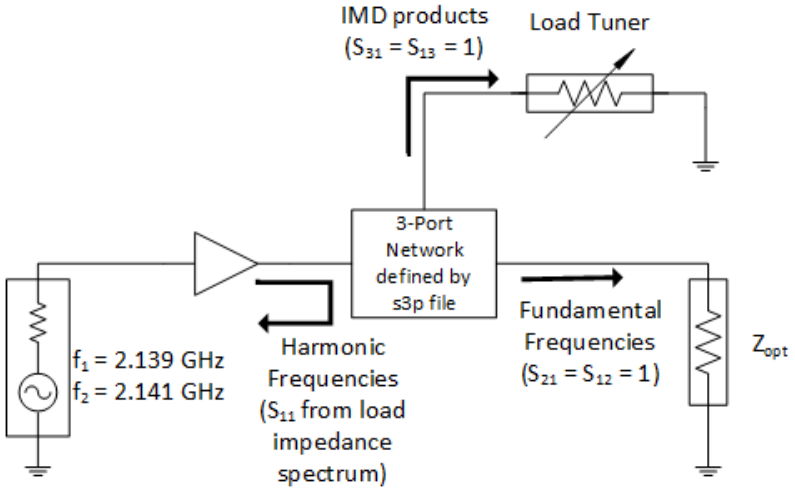


Figure 6.3: Schematic diagram of IMD Load-Pull Setup

The study can be carried out by considering any one of the 3 different Doherty PA designs discussed in section 5.2.1, and here the trade-off with emphasis on PAE was considered. The calculated a_2 and b_2 values are then exported to MATLAB® to run the algorithm for verify the possibility of predicting the final IMD products.

6.2.2 Algorithm for finding the power waves

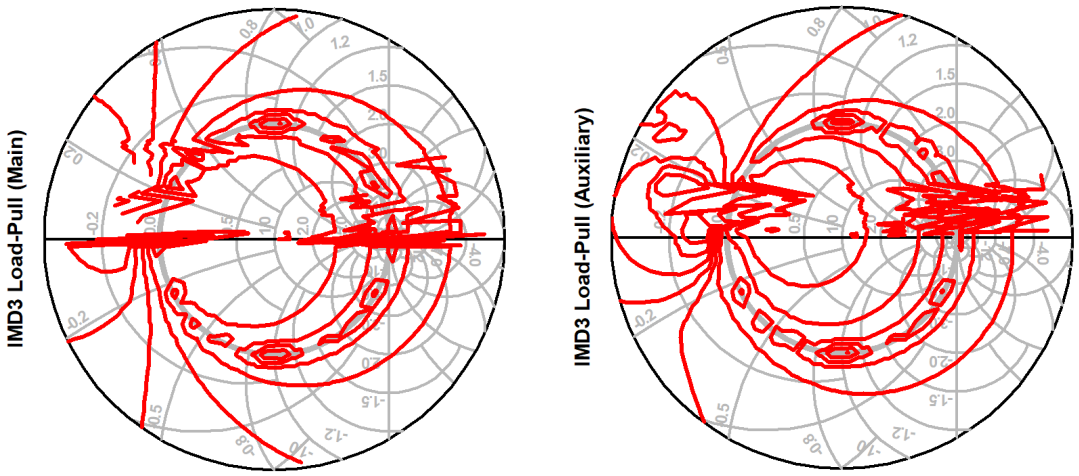
The equations required to predict the power waves were obtained from [18]. Although coupling between the amplifiers investigated in [18] is much lesser compared to the coupling between the main and auxiliary amplifiers in a Doherty, it was decided to proceed with such a simplified assumption. The equations showing the interaction between the main and auxiliary amplifiers during each instance of time for different iterations can be found in Table 6.1. The algorithm used to find the values is represented as a flow-chart in Appendix 9.2.

Table 6.1: Equations for analysis of IMD3 products [18]

Iteration	Scenario	Amplifier o/p	
1	1	a_m	$S_{11}b_m$
		a_a	Off
	2	a_m	$S_{11}b_m$
		a_a	$S_{12}b_m$
2	1	a_m	$S_{11}b_m$
		a_a	$S_{12}b_m + S_{22}b_a$
	2	a_m	$S_{11}b_m + S_{12}b_a$
		a_a	$S_{12}b_m + S_{22}b_a$
...	...	...	...
N	1	a_m	$S_{11}b_m$
		a_a	$S_{12}b_m + S_{22}b_a$
	2	a_m	$S_{11}b_m + S_{12}b_a$
		a_a	$S_{12}b_m + S_{22}b_a$

6.3 Simulated results based on the method

The Load-Pull contours for the IMD products of main and auxiliary amplifiers are as shown in Fig. 6.4. The load-pull set-up was verified by changing the marker point in the load-pull contours to select different loads and it was found to affect only the IMD products. The b_2 and the a_2 values of the lower 3rd Order IMD component (i.e., at 2.137 GHz) were calculated for every load that was mapped for main and auxiliary amplifiers. The convergence algorithm was defined using an error function that was calculated by taking the difference the current and previous values of the power waves. The final value after convergence was expected to be close to the real value obtained from the simulation of Doherty PA. A verification of the algorithm was done for the fundamental frequency tones and it was found to closely agree with the simulated values. Table 6.2 gives a comparison between the predicted data, the data extracted from IMD3 load-pull simulation and the final Doherty simulation results.

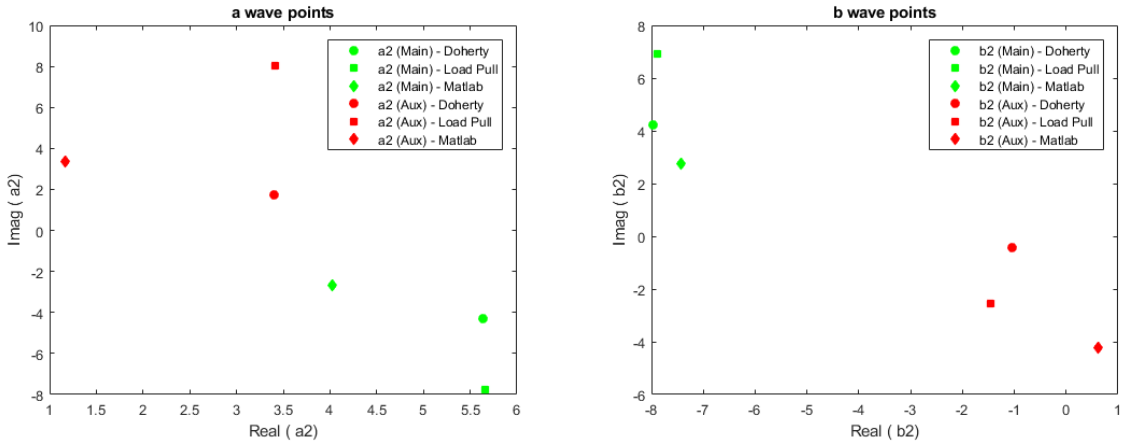


(a) (b)

Figure 6.4: IMD3 load-pull contours of (a) main amplifier (b) auxiliary amplifier for Lower IMD3 component 2.137 GHz

Table 6.2: Comparison of IMD3 power waves between simulated and converged values

Wave-state	Doherty PA configuration	Nearest value in IMD3 load-pull data	Converged value from algorithm
a_{2main}	5.642-j4.323	5.655-j7.766	4.028-j2.676
b_{2main}	-7.979+j4.206	-7.896+j6.93	-7.421+j2.757
a_{2aux}	3.403+j1.717	3.413+j8.010	1.164+j3.385
b_{2aux}	-1.037-j0.445	-1.467-j2.568	0.615-j4.240



(a) (b)

Figure 6.5: Power wave plots of IMD3 products. The circular points shows the actual values of a simulated Doherty DPA, the square points shows the nearest value found in the IMD3 load-pull data and the diamond shaped points shows the converged values obtained from the algorithm. (a) a_2 values of main (green) and auxiliary (red) amplifier (b) b_2 values of main (green) and auxiliary (red) amplifier

6.4 Conclusion on the methodology

From the Fig. 6.5 it can be seen that the convergence value from MATLAB® algorithm was not able to predict the final behavior of IMD components out of a Doherty PA. This could be due to the following reasons:

- Load modulation in Doherty PA is a time varying phenomenon, which is not accounted for when doing the load-pull of individual amplifiers with a fixed load.
- The IMD components of the auxiliary amplifier deviates more than the main amplifier from the predicted value. This can be because of the highly non-linear nature of the auxiliary amplifier.
- Another reason for difficulty in predicting the exact value in MATLAB® is due to the fact that the load-pull data extracted has invalid data (due to convergence issues in harmonic balance simulations), thereby resulting in an in-accurate interpolation to fill the missing data. These invalid data causes abrupt changes in the values between two points and this can lead to inaccurate interpretation of data which is then used for the remaining calculations, thereby increasing the error.

Chapter 7

Doherty Power Amplifier : 1-Tone Emulation

A new design approach for Doherty PA was to be evaluated where it will facilitate the analysis of the output of a Doherty PA, without the actual requirement of designing and measuring it. This study was carried out using the Chalmers RF WebLab Measurement Setup [1]. An algorithm similar to the one discussed in [18] is developed to emulate. A single tone signal provided as input to the amplifier. A single amplifier is made to mimic as the main and auxiliary amplifiers by toggling between the bias levels.

Initially, the coupled signals are not known and the output from the amplifier is stored in as b_2 in the *Output Processing Unit* [18]. In the next time interval, the b_2 is then injected into the output of the amplifier through a coupling factor provided by the S-Parameter matrix and the resulting reflected wave is then stored as the new b_2 and this process repeats [18].

As a proof of concept, a simplified approach was evaluated and therefore, the S-Parameters of a classical Doherty combiner was used to replace the combiner matrix. The combiner was created in ADS and the extracted S-Parameters are shown in the Table 7.1.

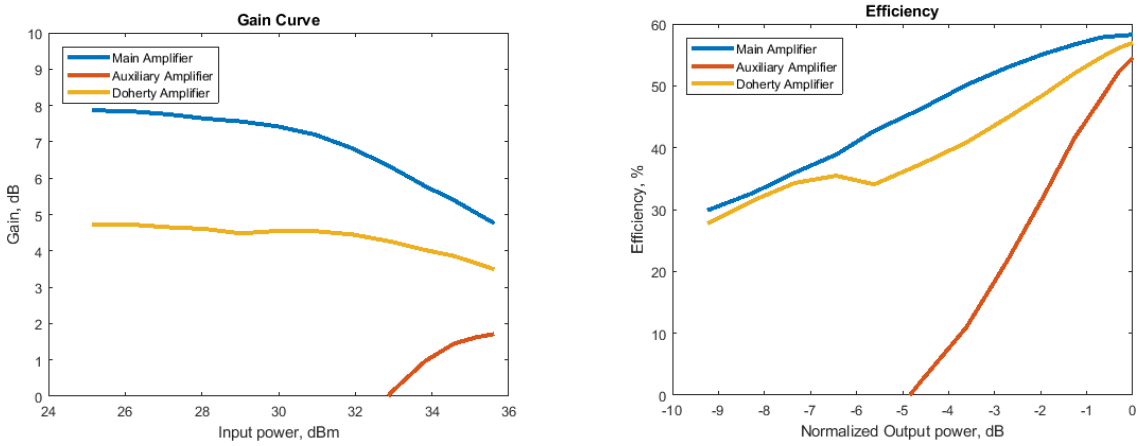
Table 7.1: Simulated 2-Port Z parameters of a classical Doherty combiner at 2.14 GHz

	Z_{11}	Z_{12}	Z_{21}	Z_{22}
2-Port Combiner	0.505	-j0.4950	-j0.4950	-0.505

The bias levels were chosen such that the amplifier will operate in Class B and Class C region and a power sweep was done emulating it.

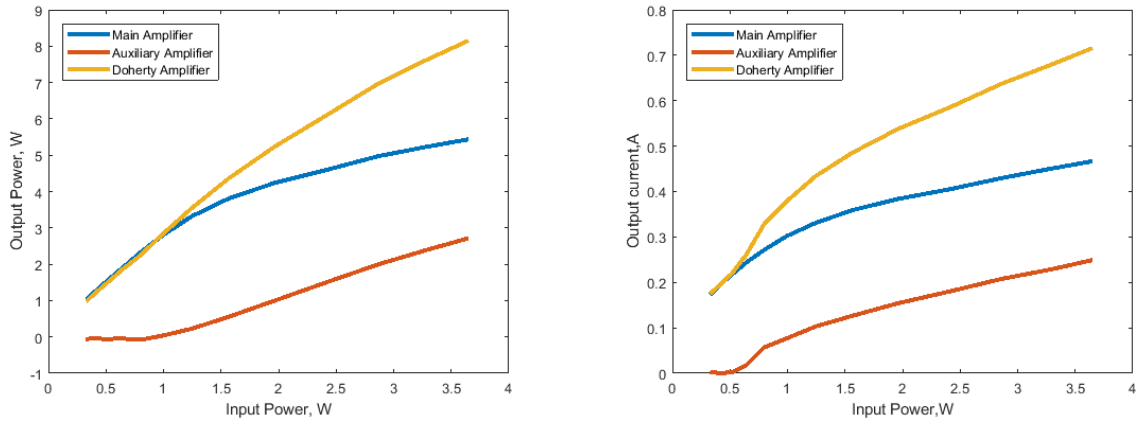
The emulated Doherty had identical gain curves to that of the ideal Doherty, however, the efficiency curves had anomalies. A "valley" can be found in the efficiency curves of the DPA just before the auxiliary turns-on. This was further investigated by plotting the P_{out} vs P_{in} curves and the drain current, I_{ds}, vs input power,P_{in}, curves, thereby evaluating the contribution of output power and drain current from the auxiliary amplifier to that of the total Doherty PA.

[1] "RF WebLab," Chalmers University of Technology, http://dpdcompetition.com/rfweblab/.



(a) (b)

Figure 7.1: (a) Gain plots of emulated classical DPA across different output power levels (b) Drain efficiency of emulated classical DPA across different output power levels



(a) (b)

Figure 7.2: (a) P_{out} vs P_{in} curves (b) I_{ds} vs P_{in} curves

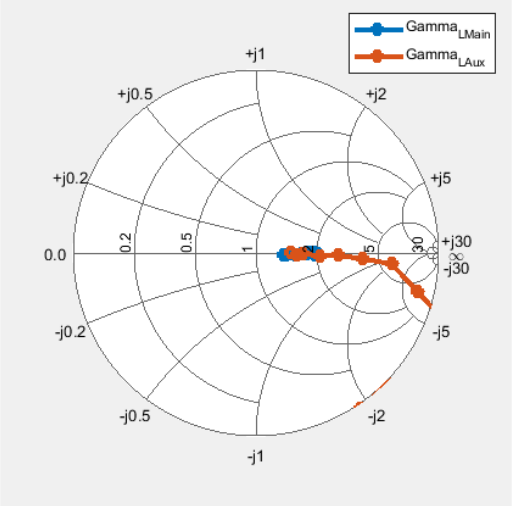


Figure 7.3: Recreated time-varying load-modulation in the Doherty PA emulation setup [6]

As it can be seen from the Figures 7.2, the drain current of the auxiliary amplifier rises much faster compared to the output power contribution of the auxiliary amplifier. The ratio of output power contribution of the auxiliary to that of the Doherty PA was found to be 12.3 % whereas, the ratio of drain current of the auxiliary to that of the Doherty PA was found to be 25.9 %, at an input power of 1.5 W. Hence, it was verified that the drop in efficiency curve of the Doherty PA after the auxiliary amplifier turns-on, can be attributed to the above mentioned effect.

Nevertheless, the study is valid since the time-varying load modulation was recreated in a measurement setup and it can be seen in the Figure 7.3. The final load impedances seen by the main and auxiliary amplifiers are 63 Ω and 70 Ω, respectively.

Chapter 8

Doherty Power Amplifier : 2-Tone Emulation

This chapter deals with the emulation of the Doherty PA in Chalmers Weblab using a two-tone signal. A similar approach to that evaluated in the CW emulation was done, except for the fact that two signals, had to be created. The two tone were separated by 1.5 MHz and the center frequency was kept as 2.14 GHz. The amplifier was successfully emulated in Class B and Class C configurations as shown in Figure 8.1.

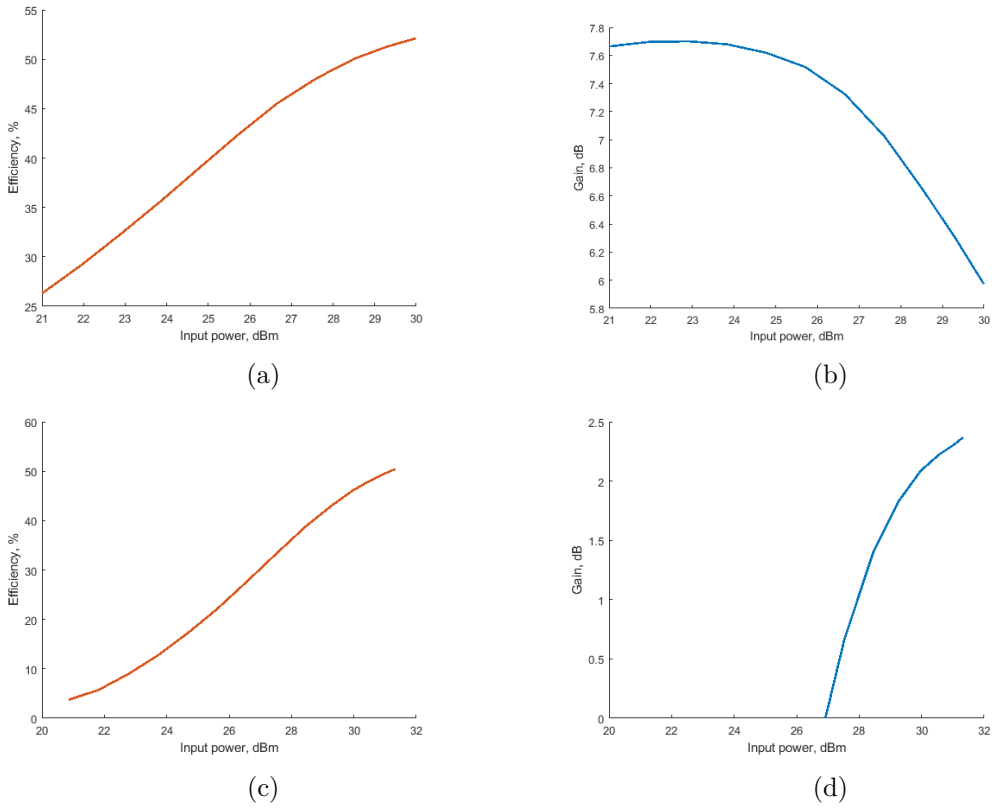


Figure 8.1: (a) Two-tone efficiency curve of emulated Class B amplifier (b) Two-tone gain curve of emulated Class B amplifier (c) Two-tone efficiency curve of emulated Class C amplifier (d) Two-tone gain curve of emulated Class C amplifier

The amplifier was then emulated using a similar approach as discussed in Chapter 7. However, there were difficulties in the convergence when the setup was emulated as a Doherty PA. The re-sampling of the signal, showed abnormal gain characteristics when it was done for two tone separately. Although, the gain characteristic behaved normally when the re-sampling was done for the combined signal, the phase error and magnitude of error still needs more investigation for fixing.

Chapter 9

Conclusion and Future Work

9.1 Conclusion

This thesis investigated the possibility of a two-tone signal being used to design a Doherty Power Amplifier. In depth analysis of non-linear components and its estimation algorithms were further carried out. In section 4.1.1, a Doherty PA was designed and simulated using a continuous wave signal centered at 2.14 GHz. A high efficiency DPA was designed that was capable of providing a PAE of 59.6 % at back-off power level of 36.7 dBm and 68.8 % at full-power of 43.7 dBm.

A simulation of the same DPA under two-tone conditions showed lesser PAE of 45.5 % and 63 % at back-off and full-power, respectively. This further led to the investigation of a Doherty PA based on different trade-off conditions between efficiency and linearity, as discussed in Chapter 5. As one of the main goals of this thesis was to study the linearity issues of the Doherty PA, the trade-off condition emphasizing more on third-order IMD products was of utmost importance in this study. At first, the trade-off conditions were only evaluated for the main amplifier operating at back-off power level. It was further expanded to main and auxiliary amplifiers operating at full-power level in section 5.2.3. The purpose of the study was to find the possibility of combining the best results from different trade-off conditions and possibly designing a Doherty PA out of it. However, it was found that it would be difficult to implement a Doherty amplifier with flat gain since the main amplifier operating at FP and auxiliary amplifier operating at FP have vastly different gains for the best results. However, the results of main amplifier operating at BO is still relevant as we can make use of it to improve the linearity at input powers lower than BO power level.

In Chapter 6, a comprehensive analysis of IMD3 components and its estimation was carried out. A novel method of IMD3 load-pull was carried out and the power wave data calculated from the load-pull setup was then used to interpolate and predict the IMD3 components of a Doherty PA. A simplified approach was done by fixing the load impedances of the fundamental frequency components (2.139 GHz and 2.141 GHz) and the harmonics. The investigation was primarily done at lower third-order IMD component (2.137 GHz) at a fixed power level. It was found that this method was unsuccessful in predicting the IMD3 components due to the simplifications made, as discussed in the section 6.4.

In Chapter 7, a Doherty PA was emulated using Chalmers RF Weblab Measurement setup for single tone signal. The Doherty PA was realized using a classical Doherty combiner and emulated in an approach similar to the one mentioned in [18]. The primary goal of the study was a proof of concept that the load-modulation can be emulated using the Weblab setup and this was successfully implemented. The load modulation can directly be observed at the relevant measurement reference planes for both main and auxiliary amplifier. In Chapter 8, the method was further extended to two tone signals using the same combiner S-parameters. The amplifier was successfully emulated to work individually as main and auxiliary amplifiers, however, there were difficulties in the convergence when the setup was emulated as a Doherty PA.

9.2 Future Work

The work done in emulation of two-tone Doherty PA in Chalmers Weblab needs to be expanded further. A deeper analysis of the convergence issue is required to be studied and fixed, in order to successfully implement it. This method can then be further extended to study and predict the IMD3 components, similar to the study that was discussed in Chapter 6, except that in this case real time analysis can be done. Going further, the measurement setup can be replaced using the actual test board setup and the emulation results can be compared and evaluated.

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Appendix A

The two-tone load-pull simulated results for the main and auxiliary amplifiers for different trade-off conditions and power levels for designing of Doherty Power Amplifier as shown below. Table 9.1 shows the load-pull simulations results for main amplifier operating at BO for the 3 trade-off conditions that were discussed in Chapter 5 for different output power levels. Similarly, the Table 9.2 and Table 9.3 shows the simulation results for main and auxiliary amplifiers operating at FP, respectively.

Table 9.1: Load-pull parameters of main amplifier operating at BO for different output power levels

Op-State	Main Amplifier at BO											
Trade-Off	Emphasis on both PAE & IMD3				Emphasis on PAE				Emphasis on IMD3			
P_{del} (dBm)	34	34.5	35	35.5	35	35.5	36	36.5	34	34.5	35	35.5
PAE (%)	47.29	49.79	52.24	54.65	52.69	55.43	58.22	61.01	28.52	30.02	31.59	33.17
G (dB)	15.43	15.29	15.09	14.78	16.36	16.15	15.84	15.38	13.47	13.41	13.31	13.16
G_{comp} (dB)	0.48	0.62	0.83	1.13	0.63	0.84	1.15	1.60	0.09	0.16	0.26	0.41
IMD3 (dBc)	-31.30	-29.44	-26.92	-24.05	-28.15	-26.18	-23.60	-20.87	-38.14	-38.04	-38.77	-32.02

Table 9.2: Load-pull parameters of main amplifier operating at FP for different output power levels

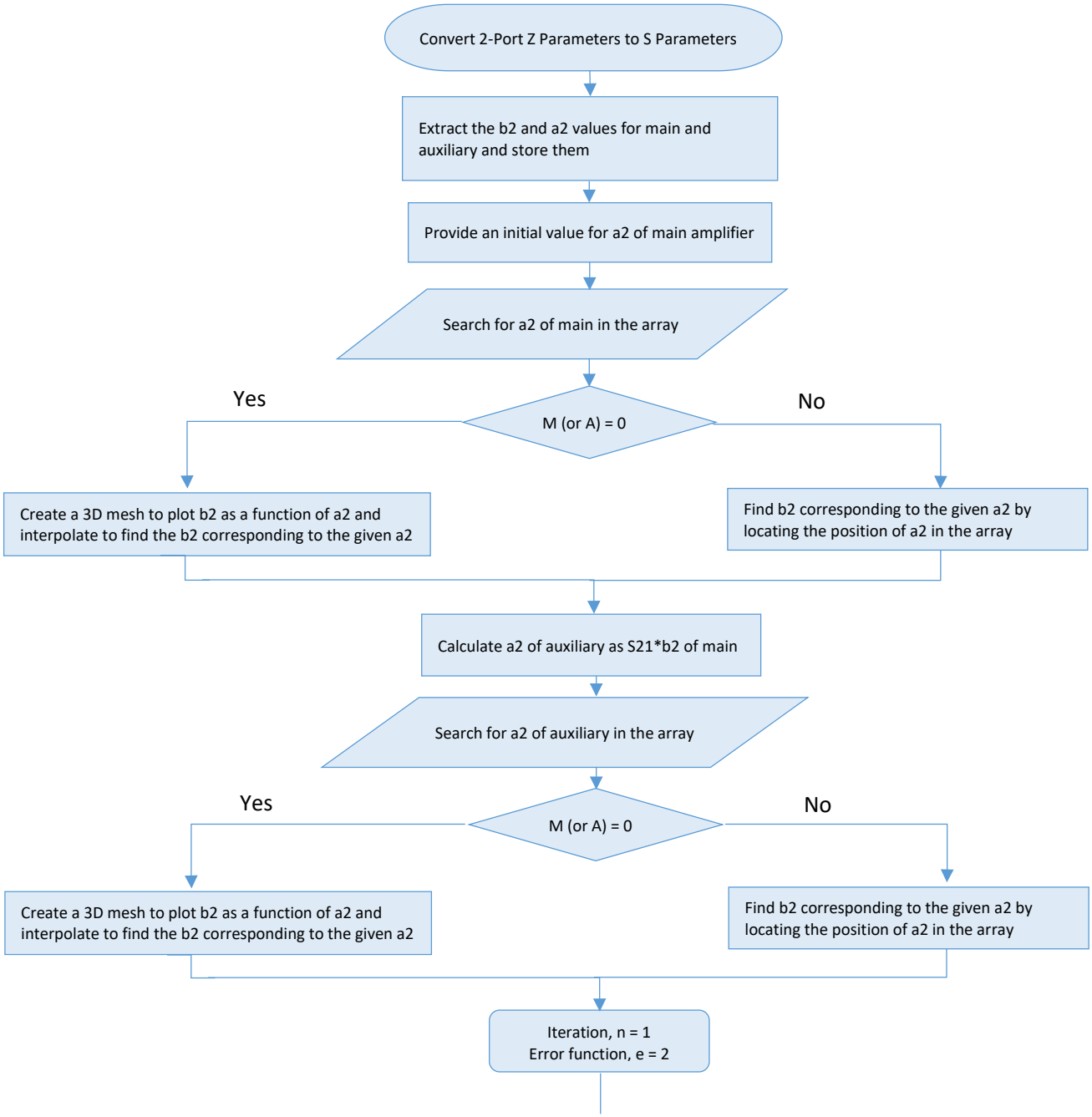
Op-State	Main Amplifier at FP												
Trade-Off	Emphasis on both PAE & IMD3				Emphasis on PAE				Emphasis on IMD3				
P_{del} (dBm)	39	39.5	40	40.5	39	39.5	40	40.5	38	38.5	39	39.5	40
PAE (%)	55.86	58.24	60.04	58.95	52.86	55.42	57.73	59.03	45.08	47.49	50.07	52.46	54.60
G (dB)	15.39	14.88	13.84	11.78	15.94	15.59	14.93	13.38	16.05	15.94	15.75	15.44	14.83
G_{comp} (dB)	0.91	1.42	2.46	4.52	0.57	0.93	1.58	3.14	0.21	0.32	0.50	0.82	1.43
IMD3 (dBc)	-29.96	-20.53	-16.12	-12.03	-26.85	-23.33	-19.17	-13.98	-32.18	-30.76	-28.08	-24.36	-19.86

Table 9.3: Load-pull parameters of auxiliary amplifier operating at FP for different output power levels

Op-State	Auxiliary Amplifier at FP												
Trade-Off	Emphasis on both PAE & IMD3				Emphasis on PAE				Emphasis on IMD3				
P_{del} (dBm)	37	37.5	38	38.5	37	37.5	38	38.5	37	37.5	38	38*	38.5**
PAE (%)	52.94	54.29	54.96	53.78	52.43	53.81	53.80	47.54	44.08	45.12	44.04	48.69*	44.88**
G (dB)	8.16	7.98	7.64	6.84	7.38	7.20	6.73	5.03	6.75	6.55	5.84	6.79*	7.73**
G_{comp} (dB)	0.10	0.27	0.62	1.42	0.04	0.23	0.69	2.40	0.02	0.22	0.93	0.47*	0.98**
IMD3 (dBc)	-15.24	-19.24	-23.12	-17.15	-17.45	-22.47	-22.21	-14.38	-18.55	-25.68	-22.40	-27.33*	-28.97**

** Z_L = 14.611-j3.666*
*** Z_L = 7.487-j5.590*

Appendix B



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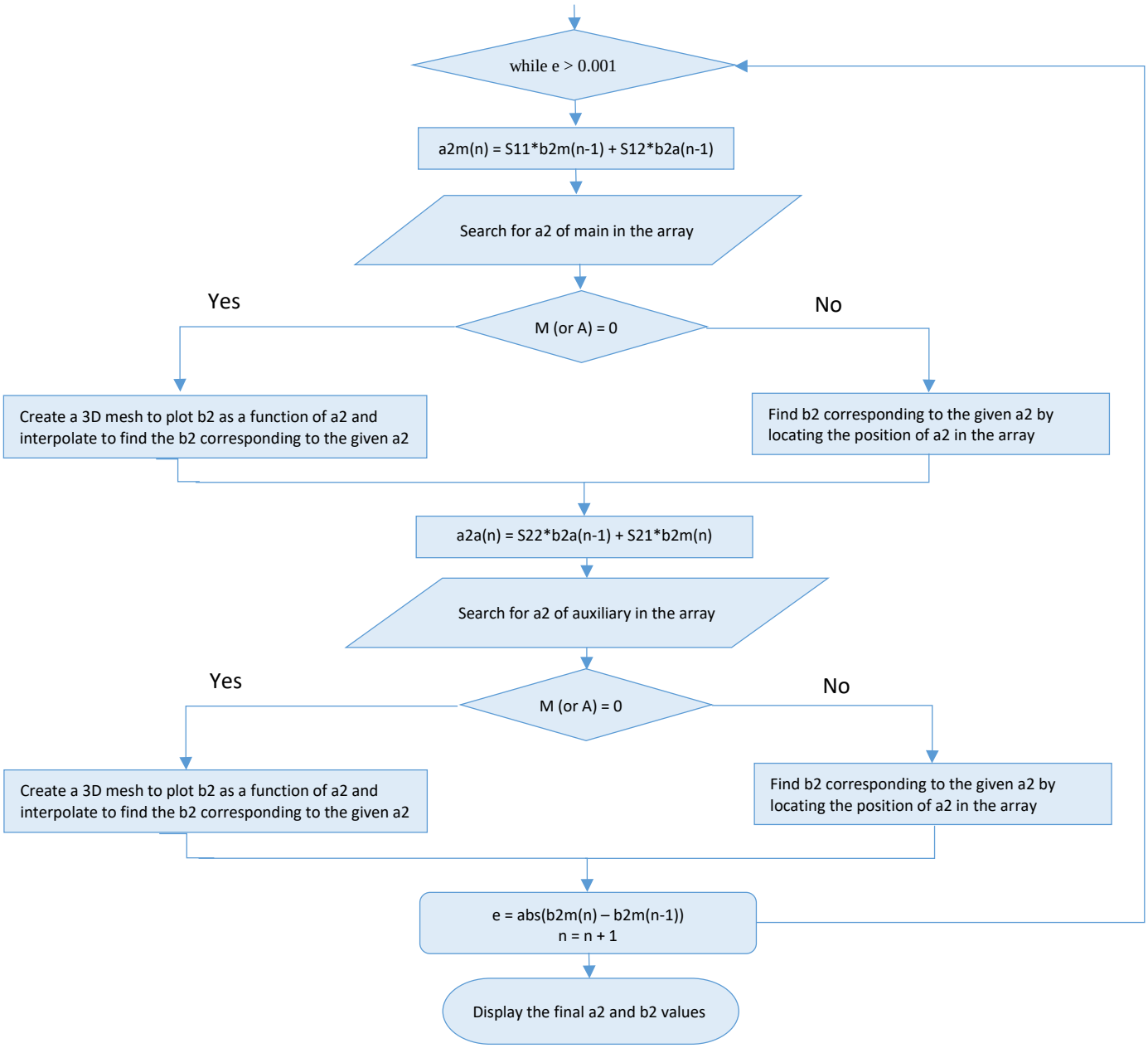
while e > 0.001
a2m(n) = S11*b2m(n-1) + S12*b2a(n-1)
Search for a2 of main in the array
M (or A) = 0
Yes
No
Create a 3D mesh to plot b2 as a function of a2 and interpolate to find the b2 corresponding to the given a2
Find b2 corresponding to the given a2 by locating the position of a2 in the array
a2a(n) = S22*b2a(n-1) + S21*b2m(n)
Search for a2 of auxiliary in the array
M (or A) = 0
Yes
No
Create a 3D mesh to plot b2 as a function of a2 and interpolate to find the b2 corresponding to the given a2
Find b2 corresponding to the given a2 by locating the position of a2 in the array
e = abs(b2m(n) – b2m(n-1))
n = n + 1
Display the final a2 and b2 values