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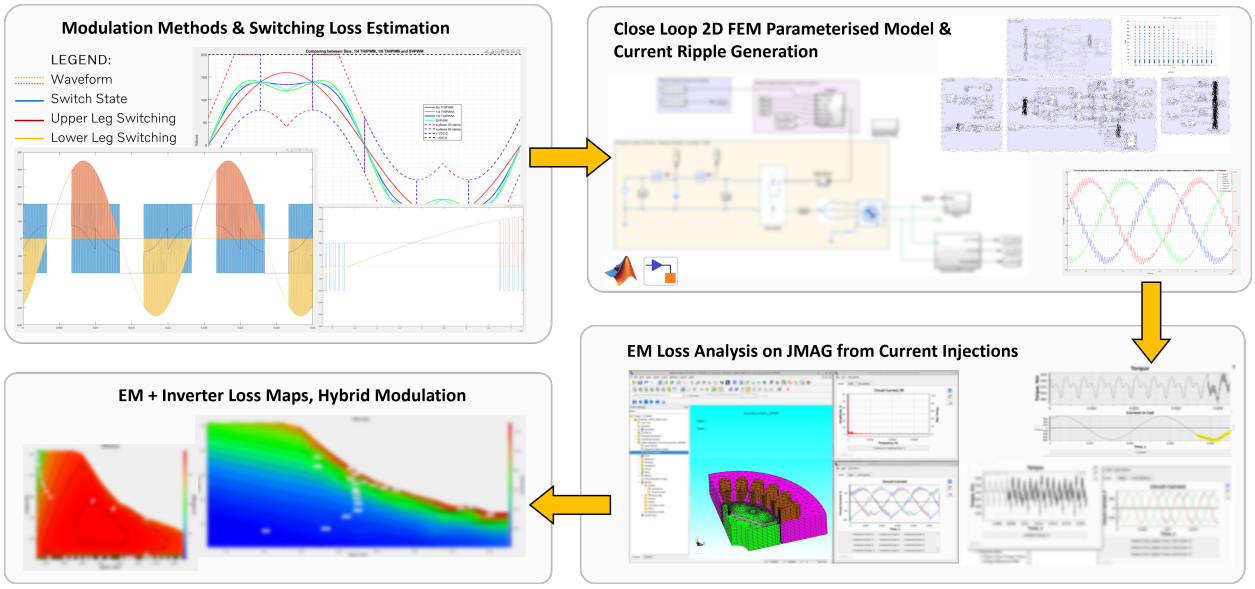

Performance Improvement Of Electric Driveline Using Modulation Techniques

Master of Science Thesis

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CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2024

Master's thesis 2024

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Cover: Visualization of the methodology implemented in this thesis work, which includes the inverter and motor plant model in MATLAB/Simulink, FEM modelling of a PMSM from JMAG, custom modulator development and loss analysis.

Typeset in LaTeX
Printed by Chalmers Reproservice
Gothenburg, Sweden 2024

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Abstract

This thesis work will study different modulation techniques and their effects on the system losses of a traction motor and inverter for automotive applications. The machine, inverter and total system losses are simulated and analyzed for Space Vector Pulse Width Modulation (SVPWM), Active Zero State Pulse Width Modulation (AZSPWM), Near State Pulse Width Modulation (NSPWM) and Discontinuous Pulse Width Modulation (DPWM) techniques across the torque-speed map at 10 and 15kHz switching frequencies. Motor losses are estimated using current fed simulations to a FEM model in JMAG. These current injections are generated using a custom closed loop coupled analysis, performed using a 2-D partial derivative model of a permanent magnet synchronous machine (PMSM), a 3-phase inverter circuit with speed, torque and current control and a custom modulator block in MATLAB/Simulink. Inverter losses are on the other hand estimated using a numerical approach on MATLAB.

The result of this study is an optimal modulation map where Hybrid DPWM techniques outperform SVPWM over a majority of the torque speed map, by a discernible margin for this studies model. This work, will also discuss the methodology and implementation of different DPWM techniques, along with their efficacy across different power factors, and the resultant reasoning and logic devised to develop a custom Hybrid DPWM technique optimized for efficiency. The variations of AZSVPWM, its logic and limitations, as well as that of NSPWM, with its loss maps and THD maps are also discussed and presented.

Keywords: Pulse Width Modulation, SVPWM, NSPWM, AZSPWM, DPWM, Harmonic Analysis, Inverter Switching Losses, Electric Motor Losses, Electric Drive Efficiency.

Acknowledgements

This thesis was carried out in collaboration between Volvo Cars Corporation and the Department of Electrical Engineering at Chalmers University of Technology.

First and foremost, we want to express our appreciation to our academic supervisor and examiner, Prof. Torbjörn Thiringer, who offered us the opportunity to engage in this remarkable thesis project. The efficacy of the study and work of this thesis is in large part due to the support and guidance provided by him.

Additionally, our gratitude extends to our supervisors at Volvo Cars, Shayan Halder and Rishabh Raj, for their invaluable mentorship, unparalleled support and contributions. Special thanks are also due to our manager, Anders Thulin, whose assistance and managerial support proved to be invaluable throughout this thesis work.

Prajwal Bharadwaj, Gothenburg, 2024
Sriyan Garapati, Gothenburg, 2024

List of Acronyms

This is a list of acronyms that have been used throughout this thesis listed in alphabetical order:

A	Ampere
AC	Alternating Current
AZPWM	Active Zero State Pulse Width Modulation
BEV	Battery Electric Vehicle
CM	Common Mode
CMC	Common Mode Current
CMV	Common Mode Voltage
DC	Direct Current
DPWM	Discontinuous Pulse Width Modulation
EMF	Electro-Motive Force
FE	Finite Element
FEM	Finite Element Method
FOC	Field Oriented Control
GDPWM	Generalised Discontinuous Pulse Width Modulation
HDF	Harmonic Distortion Factor
HEV	Hybrid Electric Vehicle
ICE	Internal Combustion Engine
IPMSM	Internal Permanent Magnet Synchronous Motor
MMT	Maximum Magnitude Test
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTPA	Maximum Torque per Ampere
MTPAV	Maximum Torque per Amp-Volt
MTPV	Maximum Torque per Volt
NSPWM	Near State Pulse Width Modulation
PI	Proportional Integral
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulation
RCMVPWM	Reduced Common Mode Voltage Pulse Width Modulation
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
V	Voltage
WLTC	Worldwide harmonized Light vehicles Test Cycles

Nomenclature

This is a list of variables and their acronyms that have been used throughout this thesis:

v_a	A - phase voltage
v_b	B - phase voltage
v_c	C - phase voltage
V_{ac}	Fundamental AC voltage
ω	Angular velocity
t	time
f	frequency
ϕ	Phase angle
i_a	A - phase current
i_b	B - phase current
i_c	C - phase current
I_{rms}	Root mean square value of current
I_{peak}	Peak value of current
U_{dc}	DC-link voltage
MI	Modulation index
V_{cm}	Common mode voltage
$\mathrm{v}_{\mathrm{a\_ref}}$	Reference phase A voltages
$\mathrm{v}_{\mathrm{b\_ref}}$	Reference phase B voltages
$\mathrm{v}_{\mathrm{c\_ref}}$	Reference phase C voltages
v_{max_cm}	Common mode voltage maxima
v_{min_cm}	Common mode voltage minima
S_a, S_b, S_c	Switch states (On)
S_{0a}, S_{0b}, S_{0c}	Switch states (Off)
V_{tri}	Carrier triangle wave
$-V_{tri}$	180° opposed carrier triangle wave
v_{cm_pos}	Positive common mode voltage
v_{cm_neg}	Negative common mode voltage
v_{a_Sin}	Reference sinusoidal phase A voltages
v_{b_Sin}	Reference sinusoidal phase B voltages
v_{c_Sin}	Reference sinusoidal phase C voltages
THD_{factor}	Total Harmonic Distortion factor
N	Frequency range
P_{sw}	switching loss
P_{total}	total inverter loss

i_{mos}	MOSFET current
i_{diode}	diode current
i_{phase}	Phase current
V_{GS}	MOSFET forward voltage
V_{SD}	diode forward voltage
$R_{DS,mos}$	MOSFET resistance
$R_{DS,diode}$	diode resistance
$P_{cond,mos}$	MOSFET conduction loss
$P_{cond,diode}$	Diode conduction loss
$P_{cond,leg}$	conduction loss across a leg
P_{cond}	conduction loss
T_{sw}	Switching period
$V_{mos,sat,0}$	MOSFET saturation voltage drop
$V_{ds,sat,0}$	Diode saturation voltage drop
R_{mos}	MOSFET resistance
R_{ds}	Diode resistance
R_{on}	On-state resistance
f_{sw}	Switching frequency
E_{sw-on}	Switching energies (On)
E_{sw-off}	Switching energies (Off)
T_{dj}	Semiconductor junction temperature
W_{h_i}	Hysteresis loss
W_{e_i}	Joule loss
B	Magnetic flux density
n	Number of pole pair
i_d	Direct-axis current
i_q	Quadrature-axis current
L_d	Direct-axis inductance
L_q	Quadrature-axis inductance
phi_m	Permanent magnet flux linkage
ϕ_d	Direct-axis flux linkages
ϕ_q	Quadrature-axis flux linkages
T	Electrical torque
U_d	Direct-axis voltage
U_q	Quadrature-axis voltage
i_s	Current magnitude
T_{peak}	Peak electrical torque
T_{rot}	Rated temperature of the rotor
I_{rms}	RMS current
N_{peak}	Maximum speed in RPM
N_{rated}	Base rated speed in RPM

Contents

1
Introduction

1.1 Background

With sustainability in mind, and in accordance with the EU directives under the Green New Deal [1], significant efforts are being applied to reduce or eliminate emissions in the transportation sector. This shift in strategy and targets fuels the research efforts in battery technology and electric drives to extract higher efficiency, improve Battery Electric Vehicle's (BEV) performance, extend range, develop cost-optimised solutions and enhance safety and reliability.

The electrical drive train in a BEV comprises the electric motor, which is responsible for converting electrical energy into mechanical power, and the inverter, which controls the motor. Electric drive trains are significantly more efficient than traditional combustion-based power trains because electric motors exhibit high efficiency and torque across a broad speed range while ensuring seamless and instantaneous power delivery. The inverter is vital, converting Direct Current (DC) from the vehicle's battery into Alternating Current (AC), as desired to drive the electric motor. Sophisticated control algorithms enable precise power modulation, ensuring peak efficiency under diverse driving conditions. Working in reverse, the inverter also enables regenerative braking, which harvests kinetic energy through the motor acting as a generator that enhances overall efficiency and extends the vehicle's driving range. Moreover, the simpler design, lack of combustion, reduced moving parts and fewer parasitic auxiliary components in the electrical drive train means reduced losses and maintenance requirements, translating to lower operational costs throughout the vehicle's lifespan.

In summary, these electrical drivetrains signify a paradigm shift in automotive propulsion, embodying efficiency, response, control and sustainability. The integration of these advanced drives highlights the industry's dedication to a cleaner and more sustainable future in transportation. This work intends to further investigate potential performance improvements on the electric driveline using various continuous and discontinuous inverter modulation techniques that might potentially reduce electric machine and inverter losses.

1.2 Aim

The efficiency of the powertrain is mainly governed by the efficiency of the electric machine and the inverter. Different modulation techniques can differently affect the harmonics throughout the system and directly affect the motors and inverters efficiency. Amongst the various Pulse Width Modulation (PWM) techniques, Space Vector Pulse Width Modulation (SVPWM) is the most widely used modulation technique. [3] This work investigates additional modulation techniques besides SVPWM, such as Active Zero State Pulse Width Modulation (AZSPWM), Near State Pulse Width Modulation (NSPWM) and Discontinuous Pulse Width Modulation (DPWM) techniques, in an attempt to study their impact on electric drive performance. This work will attempt to,

- Identify, study and implement alternative modulation techniques while evaluating their effectiveness and relevance for automotive traction drives.
- Utilise a FEM parameterised electric machine loss model and a numerical inverter loss system model along with the associated toolchain to study and compare the system losses for different continuous and discontinuous modulation techniques such as SVPWM, DPWM, AZSPWM and NSPWM at different switching frequencies.
- Demonstrate a custom modulator that can work within a pre-existing closed-loop control model.
- Investigate electric machine losses in a Finite Element (FE) environment with different modulation techniques, along with a coupled Field Oriented Control (FOC) in MATLAB/Simulink.
- Investigate inverter switching and conduction losses for the different modulation techniques.
- Compare loss studies, to identify the ideal operating regions for different modulation methods and frequencies.
- Evaluate a hybrid modulation strategy using continuous and discontinuous modulation techniques in a combined hybrid model for optimal efficiency in each zone across the entire torque-speed map.

1.3 Limitations

Having now clearly defined the background, scope, and aims of the work, and filtering out research topics, the following aspects will not be taken into consideration in this work,

- This work strictly investigates only the linear modulation region and not the overmodulation region.
- This work is built on pre-existing toolchains and system models, thus details regarding the characterisation, control strategy and control system design, case setup and calibration are not included.
- The model is in the discrete-time domain and does not look at performance and behaviour during transients and thus, strictly studies the losses for specific operating points at steady state.
- A suitable resolution and limits are set when generating the operating points for this study, for practical reasons.
- Similarly, a numerical approach is chosen when modelling the inverter losses, where switching delays, duty cycle compensation, diode reverse recovery and component parasitic and transient behaviour are not taken into consideration.
- The Permanent Magnet Synchronous Motor (PMSM) machine model to be implemented will only focus on electromagnetic analysis. Thermal aspects of the electric machine will not be considered in this work.
- The scope of the model will only be for the power module and the DC link, i.e. no battery interaction is taken into consideration.
- Throughout the study, a fixed nominal operating temperature of 60 °C and a DC Link voltage of 605 V are considered.

2

Theory

2.1 An overview of modulation

The inverter of an electric drive system is utilised to regulate the flow of electric power from a DC energy storage source, to an AC source. The inverter switching signals are determined by using a modulator that uses sinusoidal reference signals that are compared to a triangle carrier wave operating at a very high switching frequency.

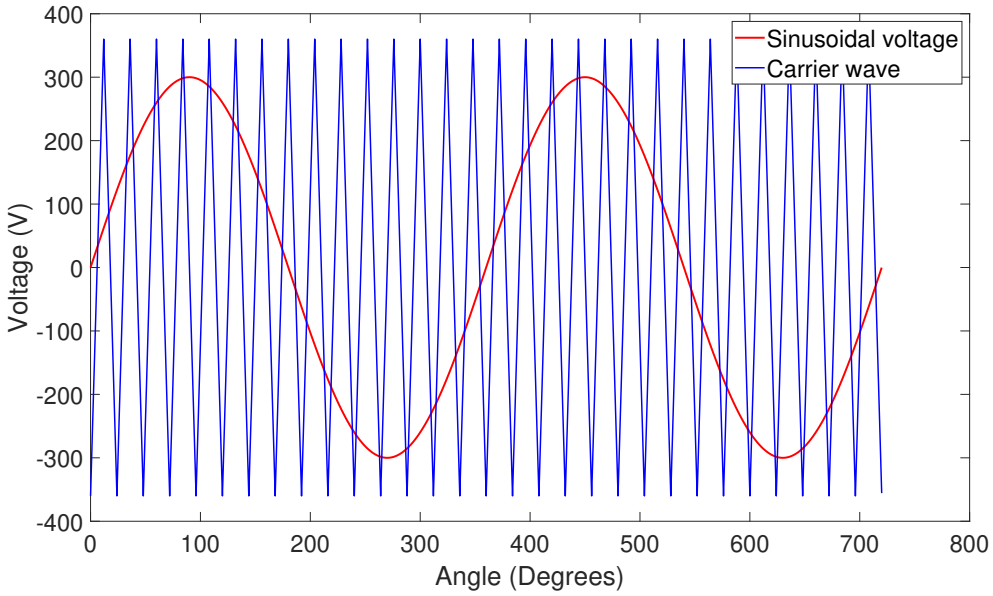


Figure 2.1: Sinusoidal voltage wave vs Triangle carrier

The three fundamental phase voltages are calculated using,

$$V_a = V_{\text{ac\_peak}} \sin(\omega t) \tag{2.1}$$

$$V_b = V_{\text{ac\_peak}} \sin(\omega t - \frac{2\pi}{3}) \tag{2.2}$$

$$V_c = V_{\text{ac\_peak}} \sin(\omega t + \frac{2\pi}{3}) \tag{2.3}$$

where (V_{ac_peak}) is the AC voltage sine wave peak amplitude defined by implementing appropriate modulation index values. A balanced 3-phase system with a 120-degree

phase shift i.e. $\frac{2\pi}{3}$ between the phases, b and c is modelled. Angular frequency (ω) is calculated from frequency (f) as,

$$\omega = 2\pi f \tag{2.4}$$

Although the modulator primarily deals with voltage modulation, the 3 phase-shifted currents are represented similarly. AC sine current wave peak amplitude is ($I_{\text{ac\_peak}}$), with the balanced 3 phases, phase shifted from the voltage by a phase angle (ϕ),

$$i_{\text{a}} = I_{ac\_peak} \sin(\omega t - \phi) \tag{2.5}$$

$$i_{\text{b}} = I_{ac\_peak} \sin(\omega t - \phi - \frac{2\pi}{3}) \tag{2.6}$$

$$i_{\text{c}} = I_{ac\_peak} \sin(\omega t - \phi + \frac{2\pi}{3}) \tag{2.7}$$

2.1.1 Linear modulation

Linear modulation encompasses various techniques, with Sinusoidal Pulse Width Modulation (SPWM) being among the most prevalent. In SPWM, a sinusoidal waveform, serving as the reference signal, reflects the desired output voltage or current. This reference signal is compared with a high-frequency carrier signal, to generate switching sequences.

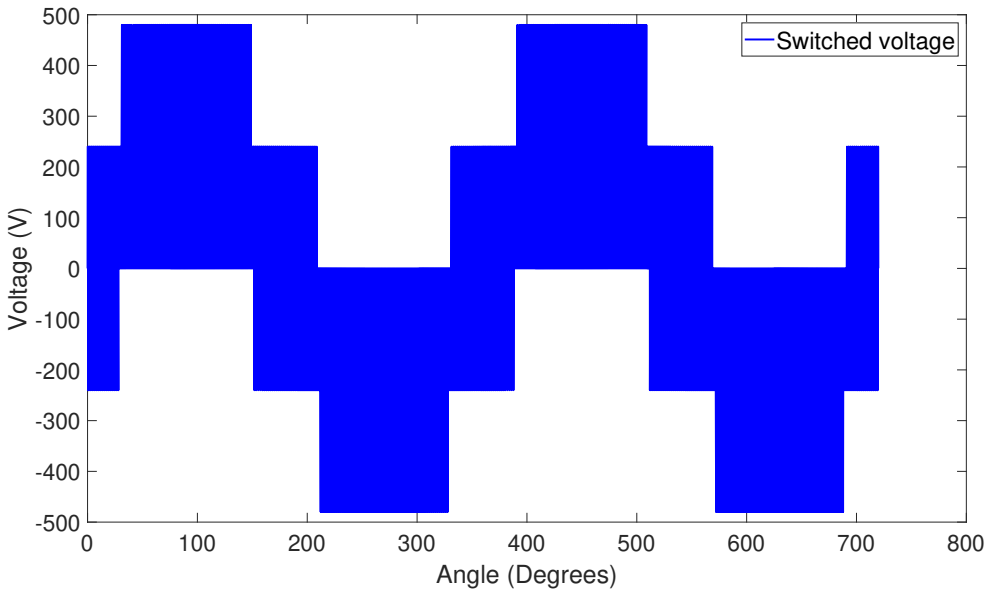


Figure 2.2: Modulated Output Voltage

In the linear modulation and overmodulation range, the Modulation Index (MI) influences the amount of DC voltage that can be extracted from a given AC voltage.[7] The variation in modulation index also correlates to the influence of harmonics on the drive system. An increase in MI reduces the significance of harmonics in the

drive system.[26] It is mathematically calculated as a ratio of modulated fundamental AC voltage signal (V_{ac}) to half of the total DC link amplitude (U_{dc}) value. The modulation index serves as a condition that signifies inverter saturation. The modulation index is defined as,

$$MI = \frac{V_{ac}}{\frac{U_{dc}}{2}} \tag{2.8}$$

The maximum modulation index achievable in the linear modulation range is 1.1547,[7] where the voltage in a phase can be calculated from the line to line voltage (V_{ll}) as,

$$V_{ll} = \frac{V_{ac}}{\sqrt{3}} \tag{2.9}$$

where the line-to-line voltage in the 2 level 3 phase inverter is (U_{dc}). Thus,

$$MI = \frac{2}{\sqrt{3}} = 1.1547 \tag{2.10}$$

Any modulation index greater than 1.1547 implies that the voltage lies in the overmodulation region, which is outside the scope of this thesis.

2.1.2 Switching of a three-phase 2-level inverter

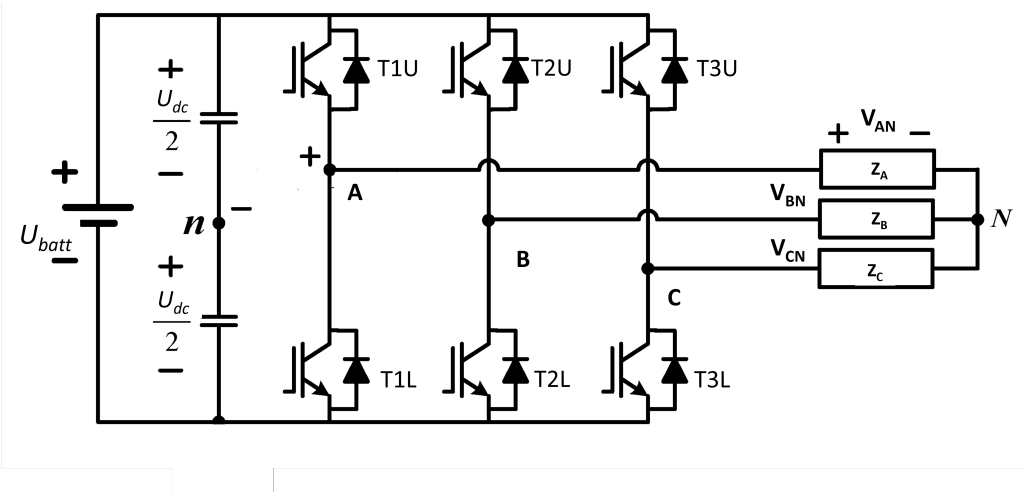


Figure 2.3: 3-Phase inverter

A simplified diagram of a 3-phase, 2-level inverter is depicted in Fig 2.3. U_{batt} is the DC voltage source of voltage U_{dc}. The input capacitors are charged to $\frac{U_{dc}}{2}$ and are coupled to create the neutral point n. The three-phase legs A, B and C have 2 controllable switches each, one upper TnU and lower TnL that have loads Z_A,Z_B and Z_C connected in a star configuration with a floating neutral N.

The switch states $S_a, S_b, S_c, S_{0\mathrm{a}}, S_{0\mathrm{b}}, S_{0\mathrm{c}}$ are determined based on the configuration of the switches across each leg. The definition of a switching state entails denoting "1" as switch on and "0" as switch off. In cases where the upper switch is turned

on, the lower switch should be turned off, hence necessitating consideration for only three upper switches. There exist eight potential switching states, among which the scenarios where all three switches are either on or off result in a short circuit of the output voltage. Consequently, these two configurations are termed as the "zero vector". Conversely, the remaining six combinations of switches can form a set of voltage space vectors with identical amplitudes of $\frac{2U_{dc}}{3}$ but varying phases. Hence, these six vectors are referred to as "active vectors".

The switch state determination among the switches $S_a, S_b, S_c, S_{0\mathrm{a}}, S_{0\mathrm{b}}, S_{0\mathrm{c}}$ in Fig.2.3 is dictated by the intersections of the fundamental voltage and carrier wave using scalar based implementation, as observed in Fig.2.1. For a given phase, a switch is turned on if the amplitude of the sinusoidal voltage signal is instantaneously greater than the amplitude of the triangular carrier wave. Similarly, a switch is turned off if the amplitude of the sinusoidal fundamental voltage wave is less than that of the triangular wave. The intersection point of the sine or modulated wave with the triangular wave determines the timing of the state transitions. The frequency of the triangular wave far exceeds that of the reference wave, resulting in a switched pulse width pattern as a derivative of the fundamental output voltage. The duration of each pulse is adjusted in correlation with the instantaneous value of the reference signal, thus earning the technique its name "Pulse Width Modulation".

2.2 Continuous modulation techniques

Continuous modulation techniques involve a type of voltage waveform generation in which voltage amplitude is continuously changing instantaneously across a period and is never clamped or saturated to the DC rail for any sequence of time within a single time period. Such techniques are known to have better harmonic performance in comparison with discontinuous modulation techniques.[7] Examples of continuous modulation techniques include Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM) and Active Zero State Pulse Width Modulation (AZPWM). They find extensive applications in scenarios where precise control of output waveforms and minimal harmonic distortion are critical, such as motor drives, renewable energy systems, and power supplies.

2.2.1 Carrier Based Space Vector Pulse Width Modulation

To enable better DC utilisation and increased fundamental output, an external voltage pulse is introduced into the conventional voltage sinusoid. This external pulse is introduced in every half-wave period. This introduction of an external voltage pulse is termed Common Mode Voltage (CMV) injection (v_{cm}).[2] The three-phase fundamental vectors ($\mathrm{v}_{aref}, \mathrm{v}_{bref}, \mathrm{v}_{cref}$) are used as reference to calculate common mode voltages to create a voltage maxima (v_{max-cm}) and minima (v_{min-cm}) that generate the desired CMV,

$$v_{max\_cm} = max[v_{aref}, v_{bref}, v_{cref}] \tag{2.11}$$

$$v_{min\_cm} = min[v_{aref}, v_{bref}, v_{cref}] \tag{2.12}$$

$$v_{cm} = \frac{1}{2}(v_{max\_cm} + v_{min\_cm}) \tag{2.13}$$

The calculated CMV is then added from all the three 120-degree phase shifted voltages respectively,

$$v_{SVPWM} = v_{ac}\sin(\omega t + \theta) - v_{cm} \tag{2.14}$$

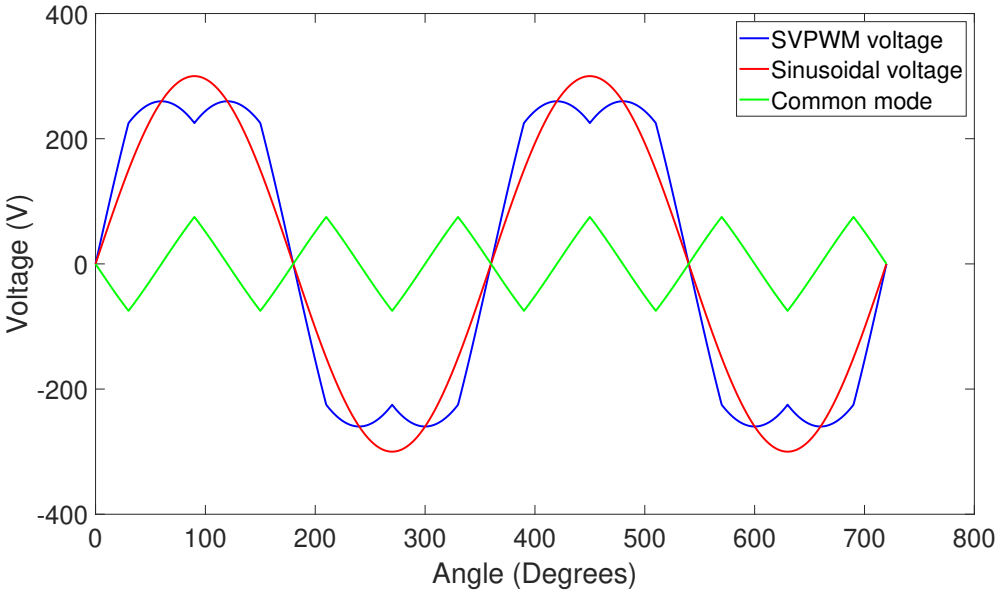


Figure 2.4: SVPWM

The resultant waveform is termed Space Vector Pulse Width Modulation (SVPWM) and besides utilizing up to 15.47% more of the DC bus voltage, offers lower low-order harmonics and Total Harmonic Distortion (THD). [7]

2.2.2 Active Zero State Pulse Width Modulation

Active Zero State Pulse Width Modulation (AZSPWM) are a group of reduced CMV PWM techniques, (i.e. AZSPWM1, AZSPWM2 and AZSPWM3) with high performance [10] that do not utilise zero voltage vectors. This results in a CMV of $\frac{U_{dc}}{6}$, instead of the conventional $\frac{U_{dc}}{2}$. While these methods, specifically AZSPWM1 and AZSPWM3 use the default SVPWM waveform shape as seen in Fig.2.5, all 3 differentiate themselves by using 2 alternating carrier triangle waves ($-V_{tri}$, V_{tri}), opposed 180° apart for each phase. While all AZSPWM methods have voltage linearity between $0 \leq (MI) \leq 1$ [10], AZSPWM2 requires simultaneous switching between inverter legs that make it impractical for typical applications [12]. On the other hand, AZSPWM1 and AZSPWM3 are continuous modulation methods with 6 switching states per sector like SVPWM as seen in Table 2.2 [13].

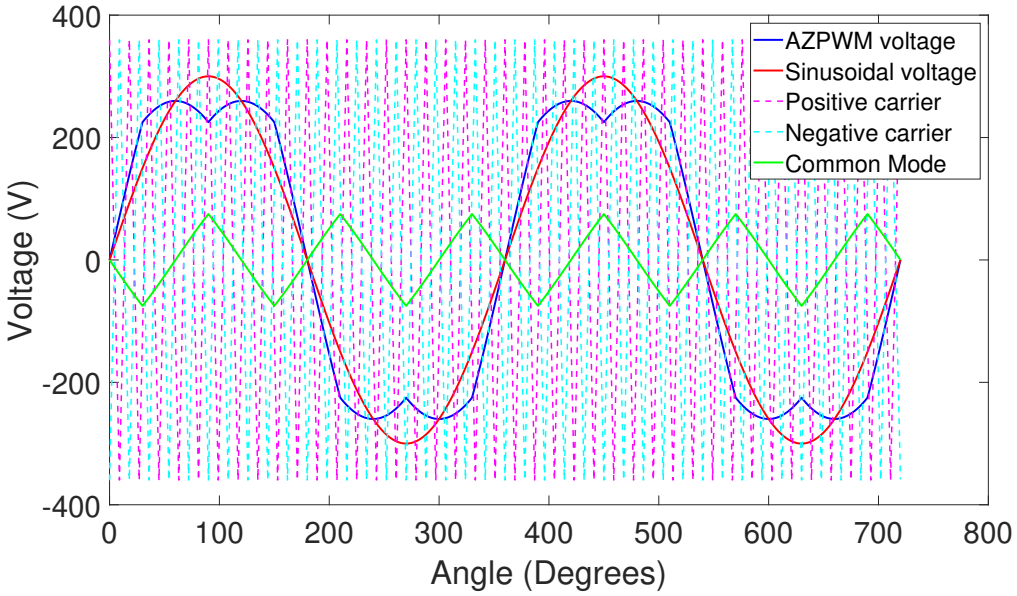


Figure 2.5: AZSPWM1 Voltage Waveform using V_{tri} and $-V_{\text{tri}}$

Table 2.1: AZSPWM1 Phase and carrier comparison in each sector

	B1	**B2**	**B3**	**B4**	**B5**	**B6**
Phase A	$-V_{tri}$	$-V_{tri}$	$-V_{tri}$	V_{tri}	V_{tri}	V_{tri}
Phase B	V_{tri}	V_{tri}	$-V_{tri}$	$-V_{tri}$	$-V_{tri}$	V_{tri}
Phase C	$-V_{tri}$	V_{tri}	V_{tri}	V_{tri}	$-V_{tri}$	$-V_{tri}$

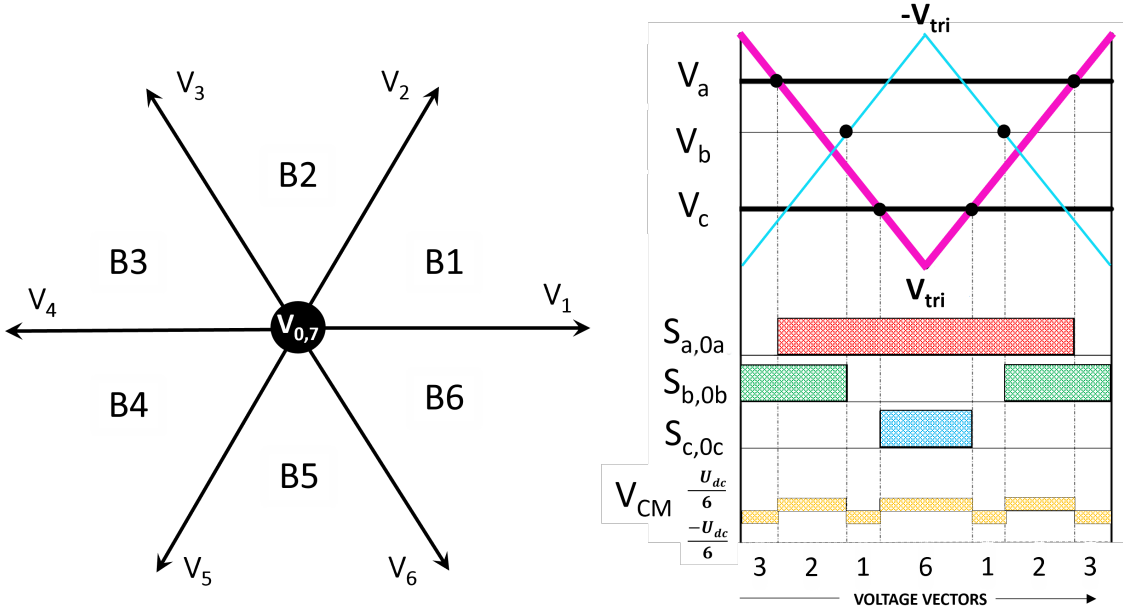


Figure 2.6: Pulse pattern of AZSPWM1 in sector B1

Table 2.2: Voltage vector patterns of AZSPWM vs SVPWM

	B1	**B2**	**B3**	**B4**	**B5**	**B6**
SVPWM	7210127	7230327	7430347	7650567	7610167	7610167
AZSPWM1	3216123	4321234	5432345	6543456	1654561	2165612
AZSPWM2	6213126	1324321	2435342	3546453	1654561	2165612
AZSPWM3	1124211	2235322	3346433	4451544	5562655	6613166

While AZSPWM1 and AZSPWM3 do offer better CMV and Common Mode Current (CMC), they do so with higher current ripple and Total Harmonic Distortion (THD) / Harmonic Distortion factor (HDF) [12] than SVPWM, DPWM or even NSPWM. Especially AZSPWM3 [10] [14], which performs worse than AZSPWM1. Moreover, previous works comment on the almost instantaneous line-to-line voltage pulse reversals, which are partially bipolar and result in overvoltages at the motor's terminals, worsened with the implementation of inverter dead times and high-frequency effects [12]. Overall, this puts AZSPWM methods at a disadvantage for practical implementation, and has thus, not been further explored in this work.

2.3 Discontinuous modulation techniques

Discontinuous modulation techniques, unlike continuous modulation techniques, involve voltage waveforms which are saturated or clamped equally between the positive and negative DC rails for different partial segments of the period. The clamping occurs for one-third of the period (120 degrees out of 360) during which no switching occurs. The angles during which the clamping occurs vary between the various DPWM techniques. Examples of discontinuous modulation techniques include techniques such as DPWM 0, DPWM 1, DPWM 2, DPWM 3 and low CMV PWM methods like NSPWM. These techniques have $\frac{2}{3}$ of the switching instances compared to SVPWM but can benefit from even lower losses if clamped at the sinusoidal current's peaks and troughs. However, these methods may induce higher levels of harmonic distortion in the output waveform, especially in the higher harmonic spectrum.[7]

The scalar implementation of DPWM techniques involves the use of Maximum Magnitude Tests (MMT) [27] of the phase voltage to determine the maximum of the 3 phase voltages instantaneously, to define and implement MMT results in a preset logic condition loop that eventually generates the required common mode voltage.

2.3.1 Discontinuous Pulse Width Modulation - DPWM 0

This particular form of discontinuous modulation technique is also referred to as the "60-degree leading clamp". The CM signal from the reference sinusoidal phase voltages is generated using the Maximum Magnitude Tests (MMT) of phase voltages. In this clamping technique, the first 60 degrees (30-90) of the clamping window between (30-150) degrees is clamped. This clamping technique is especially effective for capacitive load or operating points where the current is leading voltage. The

resulting waveform consists of two segments that are clamped at 60-degree intervals at the earliest part of the clamping window, 120 degrees apart on the positive and negative DC rails.

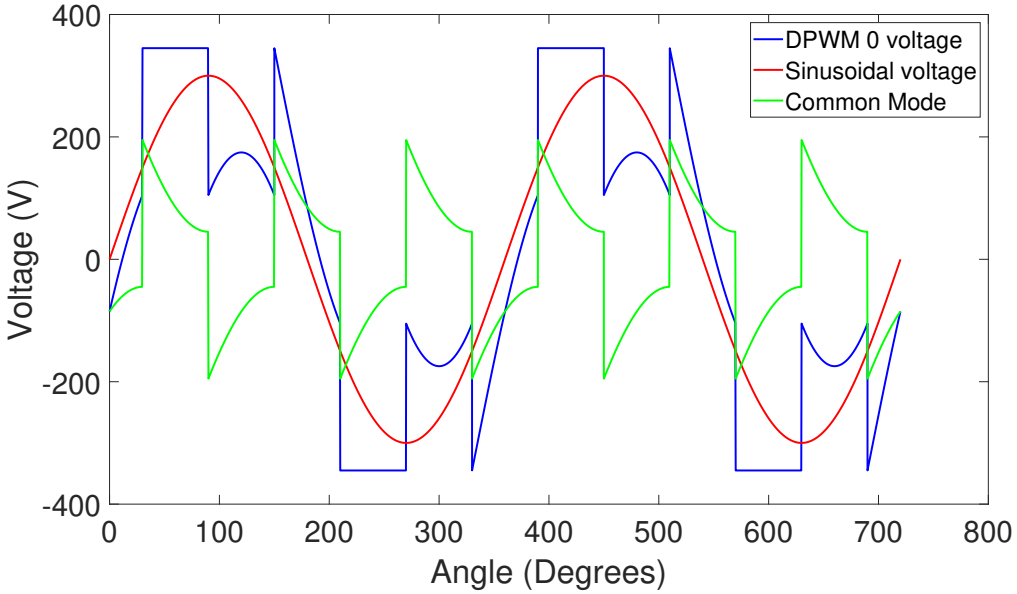


Figure 2.7: DPWM 0 (DPWM 60 leading clamp)

2.3.2 Discontinuous Pulse Width Modulation - DPWM 1

This particular form of discontinuous modulation technique is also referred to as the "60-degree conventional clamp". In this clamping technique, the middle 60 degrees (60-120) of the clamping window between (30-150) degrees is clamped. This clamping technique is especially effective for operating points that have a near-zero phase angle, representing a resistive load or operating points where voltage and current are phase-shifted by a small angle. The resulting waveform consists of two segments that are clamped at 60-degree intervals, 120 degrees apart on the positive and negative DC rails.

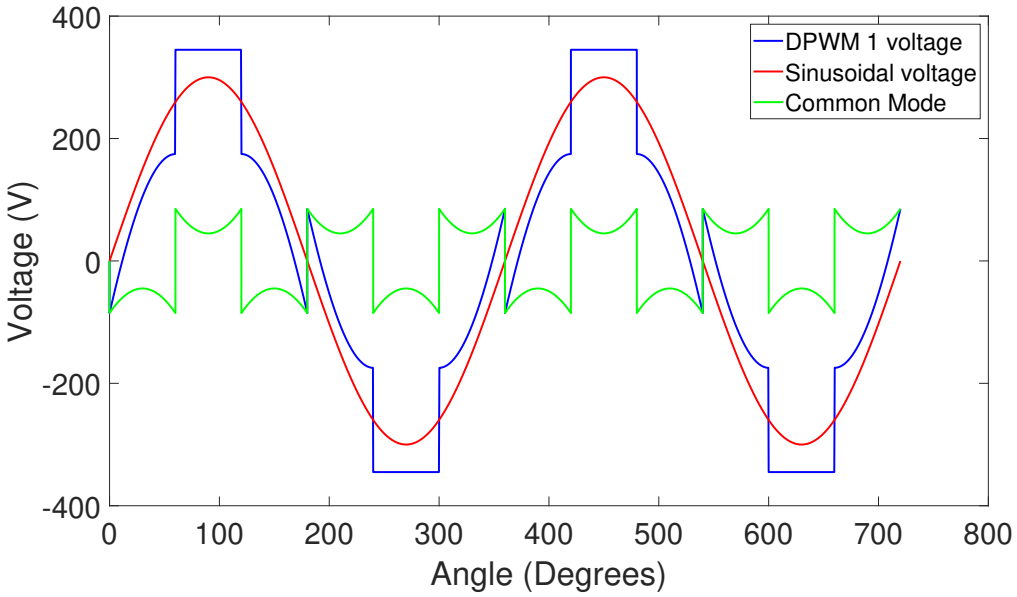


Figure 2.8: DPWM 1 (DPWM 60 conventional clamp)

2.3.3 Discontinuous Pulse Width Modulation - DPWM 2

This particular form of discontinuous modulation technique is also referred to as the "60-degree lagging clamp". The CM signal from the reference sinusoidal phase voltages is also generated using the Maximum Magnitude Tests (MMT) of phase voltages. In this clamping technique, the last 60 degrees (90-150) of the clamping window between (30-150) degrees is clamped. This clamping technique is especially effective for operating points that have a positive phase angle, representing an inductive load. After adding the CM signal as described earlier, the resulting waveform consists of two segments that are clamped at 60-degree intervals at the earliest part of the clamping window, 120 degrees apart on the positive and negative DC rails.

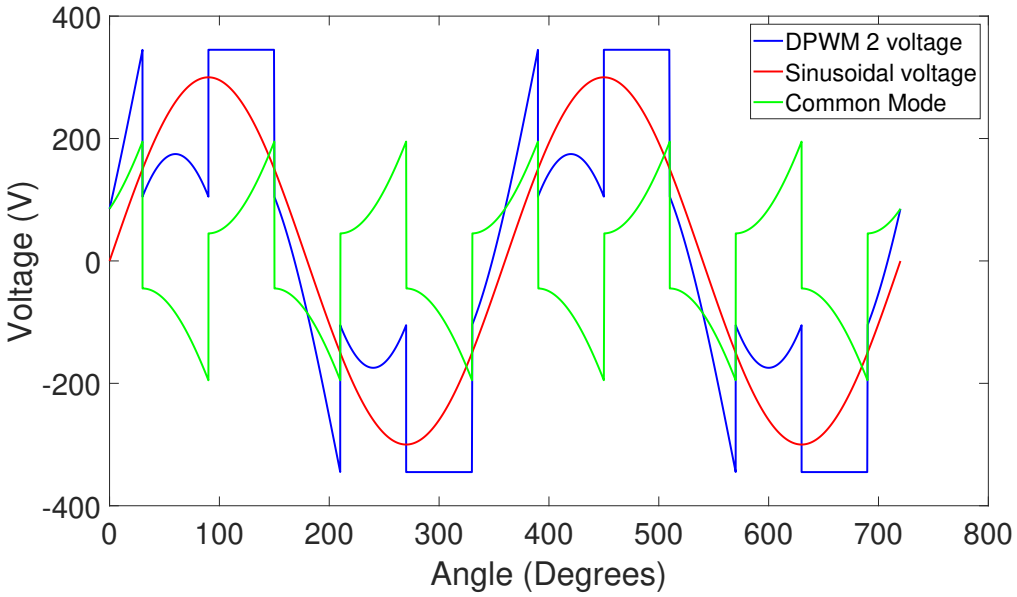


Figure 2.9: DPWM 2 (DPWM 60 lagging clamp)

2.3.4 Discontinuous Pulse Width Modulation - DPWM 3

This particular form of discontinuous modulation technique is also referred to as the "30-degree clamp". Generating the common mode signal which is injected into the three-phase sinusoidal modulating signals, is relatively similar to the DPWM 60-degree clamp common mode generation. This clamping technique is especially effective for operating points that have a very high phase angle, representing a highly inductive load or operating points where voltage and current are phase-shifted by a large angle. After adding the CM signal as described earlier, the resulting waveform consists of two segments that are clamped at distinguished 30-degree intervals on the positive and negative DC rails.

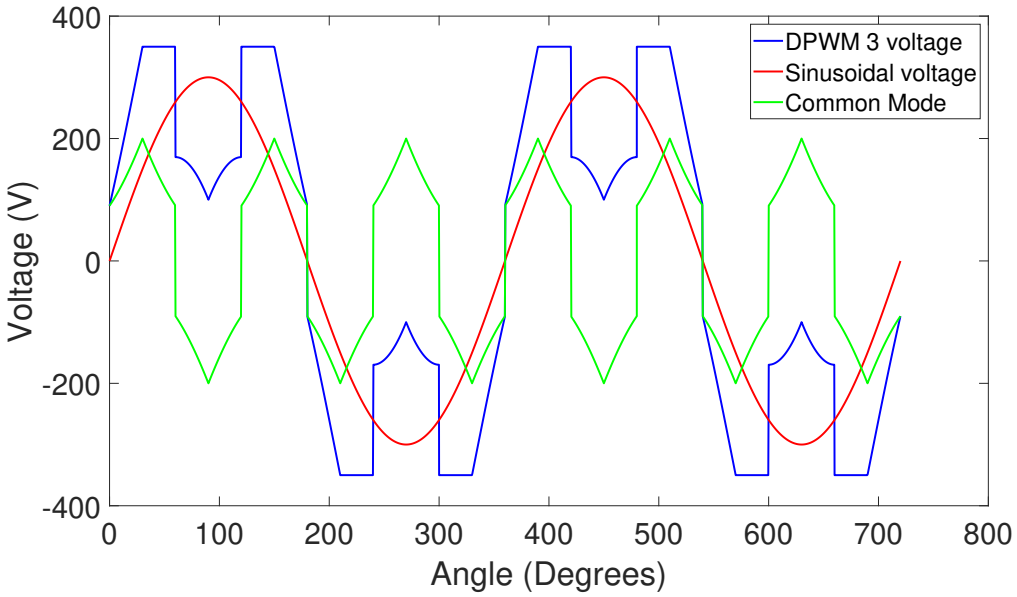


Figure 2.10: DPWM 3 (DPWM 30 conventional clamp)

2.3.5 Near State Pulse Width Modulation - NSPWM

Near-state pulse width modulation is a discontinuous modulation technique that uses the CMV and final phase voltage waveform of DPWM 1. This technique was designed to have a lesser overall CMV of $\frac{U_{dc}}{6}$, instead of the conventional $\frac{U_{dc}}{2}$ voltage obtained in the conventional DPWM techniques. This is achieved by implementing a dual carrier comparison instead of a single carrier to determine switch states. The carrier comparison changes for each phase for every 30 degrees across a 360-degree time period. The carrier comparison for a region B2 as per Fig.2.12 is represented in Table.2.3. As a result, the reduced CMV is $\frac{U_{dc}}{6}$ in Fig.2.12.

Table 2.3: NSPWM Phase and carrier comparison in each zone

	B1	**B2**	**B3**	**B4**	**B5**	**B6**
Phase A	V_{tri}	$-V_{tri}$	$-V_{tri}$	V_{tri}	V_{tri}	V_{tri}
Phase B	V_{tri}	V_{tri}	V_{tri}	$-V_{tri}$	$-V_{tri}$	V_{tri}
Phase C	$-V_{tri}$	V_{tri}	V_{tri}	V_{tri}	V_{tri}	$-V_{tri}$

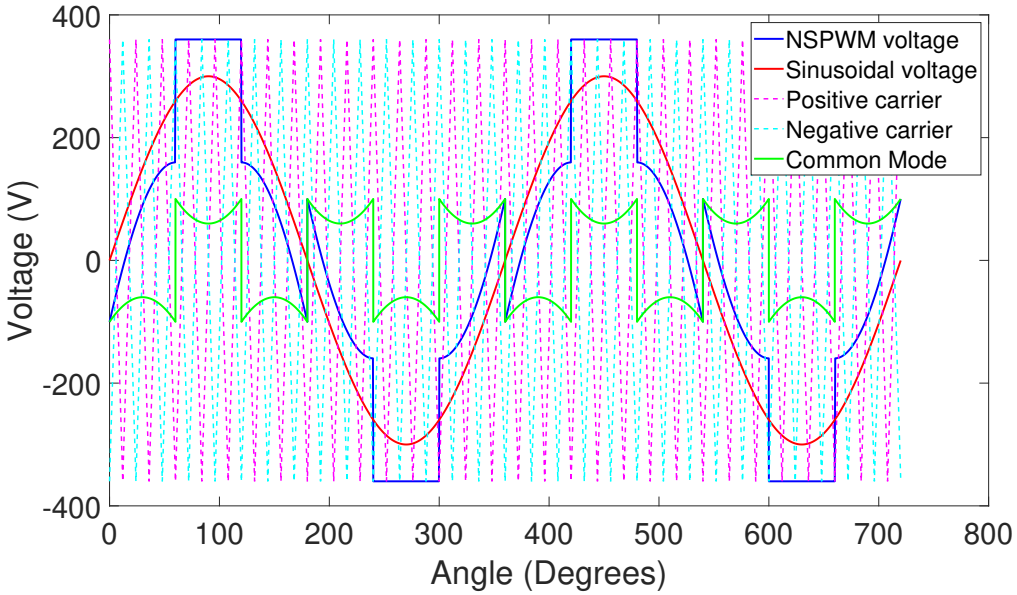


Figure 2.11: Near State Pulse Width Modulation Voltage Waveform

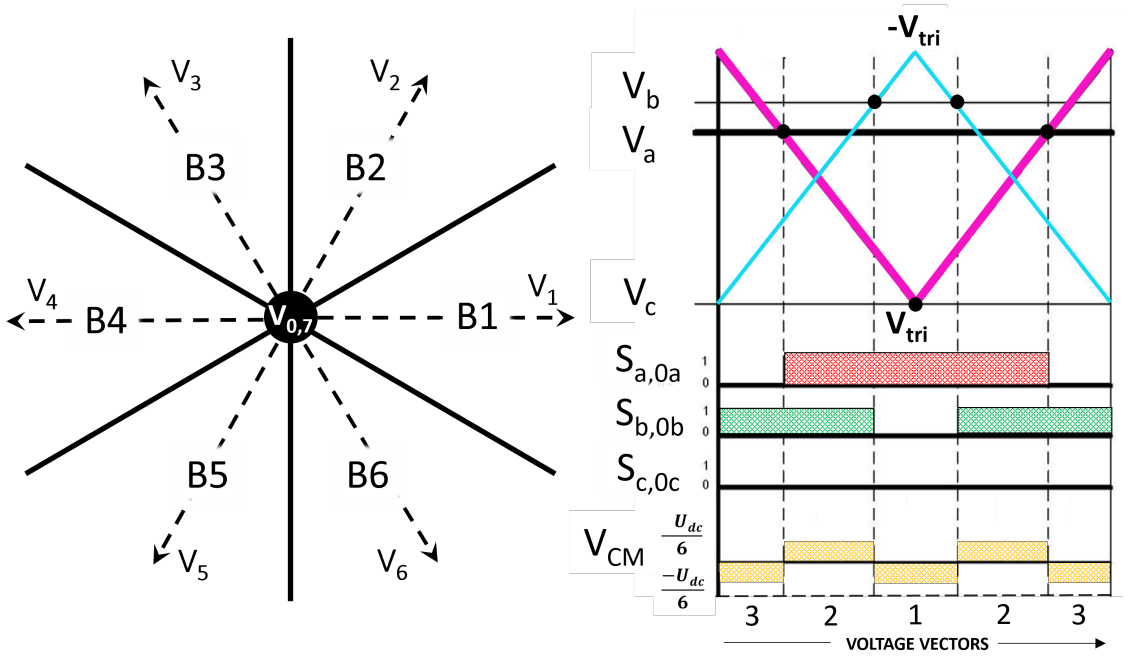


Figure 2.12: Pulse pattern of NSPWM in sector B1

The CMV of conventional DPWM 60 spans (DPWM 1) from $+\frac{U_{dc}}{2}$ to $-\frac{U_{dc}}{2}$, [12]. On the contrary, Fig.2.12 represents the CMV of NSPWM to be limited from $+\frac{U_{dc}}{6}$ to $-\frac{U_{dc}}{6}$, unlike the DPWM 60 CMV.

Besides this, while the line-to-line voltage pulse pattern for NSPWM is partiality bipolar since the method only switches one inverter leg at a time, its performance is

not adversely affected by switching dead times, and switch driver delays and can operate within realistic hardware tolerances. Additionally, while the THD of NSPWM is worse than SVPWM and DPWM between 0.7 and 1 MI, it is superior compared to other Reduced Common Mode Pulse Width Modulation techniques (RCMPWM) and outperforms SVPWM at MI greater than 1, while still inferior if not comparable to DPWM. [14] [12] This yields a PWM current waveform with reduced ripple characteristics and lower CMV, thereby making it a reasonable technique to be investigated in this thesis work.

2.4 Total Harmonic Distortion - THD

In practical applications of power electronic equipment, achieving an ideal sinusoidal power supply is challenging due to the inherent switched nature of these systems. This switching action introduces undesirable harmonics into the waveform. A distorted waveform can be decomposed and represented by a set of harmonics of varying amplitudes. These harmonic components have frequencies that are integer multiples of the fundamental frequency. To quantify the extent of harmonic distortion and assess the performance of voltage control systems, various performance indices are developed. These indices provide a measure of how closely the output waveform resembles the ideal sinusoidal waveform. By analyzing the harmonic content and distortion levels, one can evaluate the quality of the power supply and identify areas for improvement in the design of electric machines and other electrical appliances.

Total Harmonic Distortion (THD), also called the Harmonic Distortion Factor (HDF) is usually expressed as the ratio of the root mean square of the total harmonic component or harmonic disturbance, to the fundamental voltage component, across a frequency range (N). The harmonics here are the positive integer multiple of the fundamental frequency.

$$THD_{factor} = 100 \times \frac{\sqrt{\sum_{i=2}^{N} Harmonic\ amplitudes(i)^2}}{Fundamental\ amplitude} \tag{2.15}$$

As the THD increases, the higher amplitudes of the harmonic components increase the electrical machine loss, especially the motor losses [16]. In addition, a measurable increase in torque ripple and worsening of acoustic performance is observed [15]. Thus, a lower THD factor is preferable when comparing across different modulation methods.

2.5 Power losses in inverters

To produce the sinusoidal phase voltages required by the electrical machine, a bipolar 3-phase full bridge rectifier configuration is typically used. This setup employs six Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) as switching devices to drive the current and body diodes to enable freewheeling, back-Electro Motive Force (EMF) bleeding. Power losses in the phase legs of

inverters are primarily influenced by the phase waveforms, comprising both fundamental and harmonic components. The characteristics of the load determine the fundamental values, but the induced losses are a result of the intersections between the high-frequency triangular carrier wave and the sinusoidal reference waveform signal that control the instances where the inverter switches.

For the scope of this work, only switching losses (P_{sw}) and conduction losses (P_{cond}) are considered, with dc-link, busbar, cable, circuitry, blocking and switching driver circuit losses neglected. As such, the total inverter losses (P_{total}) can be defined as,

$$P_{total} = P_{cond} + P_{sw} \tag{2.16}$$

2.5.1 Conduction losses

Besides having better switching and conduction losses than IGBTs, SiC MOSFETs have an intrinsic body diode, that is formed by a p-n junction between the source and drain. This results in a phenomenon termed 'freewheeling', wherein an inductive load, the SIC MOSFETs can continue to conduct passively in reverse, from the source to the drain when turned off. Hence, current passes only through the forward conducting activated SiC MOSFET, with the SiC MOSFET and diode working in parallel during freewheeling respectively when turned OFF as seen in Fig. 2.13.[17]

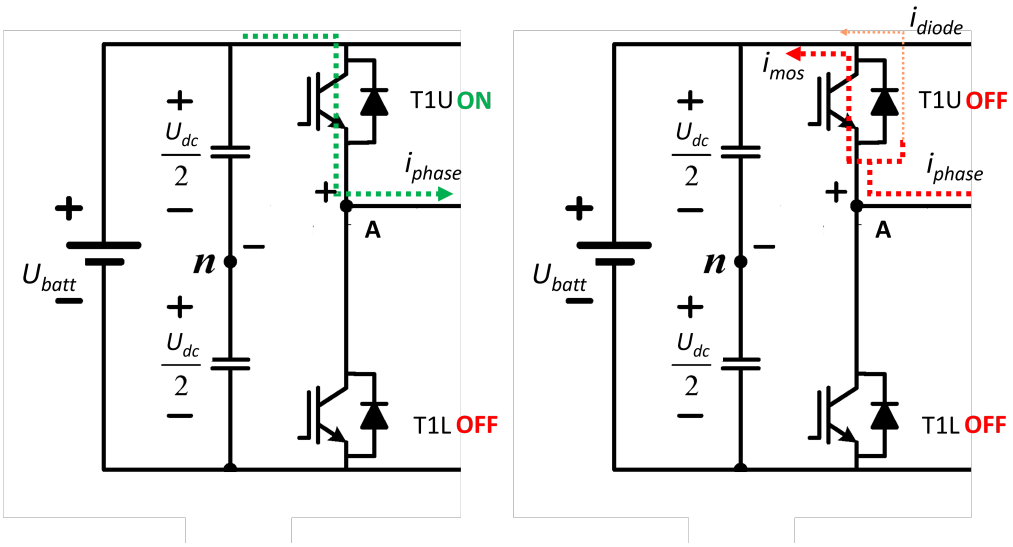


Figure 2.13: SIC MOSFET in forward conduction when turned ON (left), and freewheeling with current splits between the SIC MOSFET and diode (right)

Here again, SiC MOSFETs exhibit two different loss mechanisms during freewheeling. The phase current (i_{phase}) split between the diode (i_{diode}) and MOSFET (i_{mos}) is a function of the MOSFET forward voltage (V_{GS}), the diode forward voltage (V_{SD}) and their individual resistances ($R_{DS,mos}$) and ($R_{DS,diode}$). This can be formulated as,

$$i_{mos} = \frac{R_{DS,diode} i_{phase} + sign(i_{phase}) V_{SD}}{R_{DS}} \tag{2.17}$$

$$i_{diode} = \frac{R_{DS,mos} i_{phase} - sign(i_{phase}) V_{SD}}{R_{DS}} \tag{2.18}$$

where,

$$i_{phase} = (i_{mos}) + (i_{diode}) \tag{2.19}$$

$$R_{DS} = (R_{DS,mos}) + (R_{DS,diode}) \tag{2.20}$$

However, since the resistance of a MOSFET is generally much lower, in some cases, within a current threshold ($i_{mos,threshold}$), determined by the ratio of diode forward voltage (V_{SD}) to the resistance of the MOSFET ($R_{DS,mos}$), the instantaneous negative phase current (i_{phase}) will pass through only the MOSFET rather than being split. In this case, this threshold is calculated as,

$$|i_{mos,threshold}| < |\frac{V_{SD}}{R_{DS,mos}}| \tag{2.21}$$

Once the current split is calculated for each case, conduction power for the diode $P_{cond,diode}$ and MOSFET $P_{cond,mos}$ can be calculated as,

$$P_{cond,mos} = \frac{1}{T_{sw}} \int_0^{T_{sw}} ((V_{GS} + (R_{DS,mos} i_{mos,sat,0})) i_{mos,sat,0}) dt \tag{2.22}$$

$$P_{cond,diode} = \frac{1}{T_{sw}} \int_0^{T_{sw}} ((V_{SD} + (R_{DS,diode} i_{ds,sat,0})) i_{ds,sat,0}) dt \tag{2.23}$$

This is then scaled from one leg $P_{cond,leg}$ across the three legs and summarised to give the final net conduction loss P_{cond}.

$$P_{cond,leg} = P_{cond,mos} + P_{cond,diode} \tag{2.24}$$

$$P_{cond} = 3(P_{cond,leg}) \tag{2.25}$$

2.5.2 Switching losses

The switching losses for a semiconductor switch occur when it is turned on or off. The instantaneous change in current and voltage across the MOSFET and its body diode results in switching losses. These can further be differentiated into switch-off losses when the MOSFET turns off with no reverse recovery diode loss and switch-on losses when the MOSFET is turned on with reverse recovery diode losses caused by the large recovery current that flows in reverse when the diode is switched from forward to reverse biased. These losses are directly proportional to the number of switching events, a result of the switching frequency (f_{sw}) and the magnitude of the switching energies (E_{sw-on}), and (E_{sw-off}). The switching energies again are a function of the operational DC-link voltage (V_{dc}), the magnitude of the conducting

current (i_{phase}) at which the switching takes place, as well as the junction temperature (T_{dj}) of the semiconductor. When dealing with discontinuous methods, due to the varying clamping duration, angle and modulation methods, a numerical rather than analytical model is required. Thus, switching losses are expressed as,

$$P_{sw} = f_{sw} E_{sw-on/off}(V_{dc}, i_{phase}, T_{dj}, MI, t, S_{a,b,c}) \tag{2.26}$$

For the scope of this work, leakage current and reverse recovery energy are not considered, since characteristic curves and information on the reverse recovery charge versus their variation with current, load and environmental factors are not in the public domain. Additionally, the operational DC-link voltage is fixed to the nominal battery voltage.

2.6 Estimation of machine losses using Finite Element Analysis

JMAG, a Finite Element Modelling (FEM) tool is used for the electromagnetic simulations, to estimate the electric motor losses in this work. In PMSMs, the primary contributors to total losses are copper losses and iron losses. Copper losses are related to the resistance in the machine winding and are influenced by proximity and skin effects, which alter the current distribution inside the conductor. This leads to a virtual reduction in conductor cross-section and an increase in resistance. Iron losses consist of hysteresis and eddy current losses. Hysteresis losses are generated by the friction between magnetic domains during their orientation along an external field, while eddy current losses are related to currents induced inside the magnetic core according to Lenz Law.

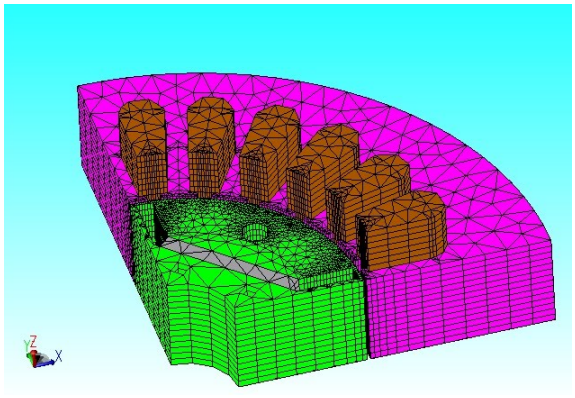


Figure 2.14: Sample 3D FEM model - JMAG

With the intent of generating loss maps, one methodology is to build a co-simulation model of the inverter that mimics the control system, switches and electrical equations. A voltage injection simulation is performed to induce currents that are used to generate loss maps. There is relevant work that shares similar methodologies

[4][5][6], but this method is more time-intensive as it takes longer for the voltage injections to stabilize to a steady state. An alternative method is to use a PWM current injection with preserved current angles. [21] [22]. In this method, using the current waveform generated using a closed-loop FOC control plant model, a current-fed FEM simulation is performed using JMAG to estimate machine losses.

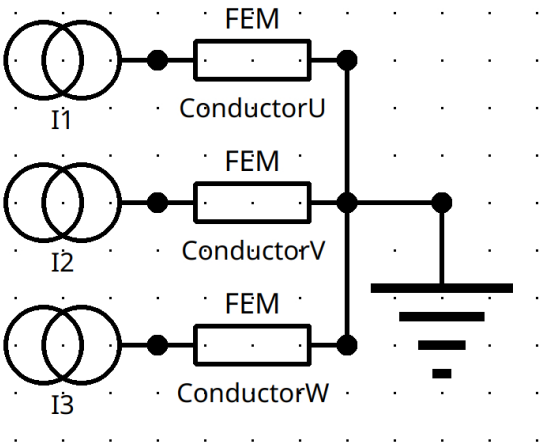


Figure 2.15: Current Injection Source - JMAG

2.7 FEM parameterised PMSM model

The FEM-Parameterized PMSM block in Simulink [18] is parameterised to model an Interior Permanent Magnet Synchronous Motor (IPMSM) of (n) number of pole pairs, characterized by tabulated data in terms of d-axis (i_d) and q-axis (i_q) currents generated from MTPA for the entirety of the Torque-Speed map. This model assumes sinusoidal back EMF and nonlinear flux maps that are a function of (i_q) when ($i_d = 0$). D-axis (L_d) and q-axis (L_q) inductance maps that are a function of i_d and i_q are used to estimate d-axis (ϕ_d) and q-axis (ϕ_q) flux linkages and electrical torque (T) as,

$$\begin{bmatrix} \phi_d \\ \phi_q \end{bmatrix} = \begin{bmatrix} L_d(i_d, i_q) & \\ & L_q(i_d, i_q) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \phi_m(i_q) \\ \end{bmatrix} \tag{2.27}$$

$$T = \frac{3}{2} n \left(i_q \left(i_d L_d(i_d, i_q) + \phi_m(i_q) \right) - i_d i_q L_q(i_d, i_q) \right) \tag{2.28}$$

The characteristic maps are characterised at a point where the iron losses are low and don't significantly interfere with the magnitudes of the i_d, i_q currents. The inductance maps are also not frequency dependent, as the skin effect phenomenon does not significantly influence the generated flux fields.

2.8 Field-Oriented Control

Field-Oriented Control (FOC), is employed to achieve precise control over a wide range of torques and speeds. It necessitates transforming stator currents from the stationary reference frame to the rotor flux reference frame (d-q reference frame) with Clarke, Park, and inverse Park transformations. Commonly used control modes in FOC include speed control and torque control, with position control being less prevalent. Traction applications typically utilize torque control mode, where the motor control system adheres to a reference torque value [25].

The implementation of the FOC requires real-time feedback of currents and rotor position. This control system includes a current controller composed of two proportional-integral (PI) controllers with a current reference generator that can use a position observer to accurately estimate angular position. The current reference generator uses Maximum Torque per Ampere (MTPA), either via an estimation algorithm or lookup charts to determine the best current combination for each operating point. When operating above the base speed, FOC integrates field weakening control, i.e. Maximum Torque per Ampere and Volt (MTPAV) to maintain performance. The architecture of a typical field-oriented control system is seen here in Fig.2.16.[25]

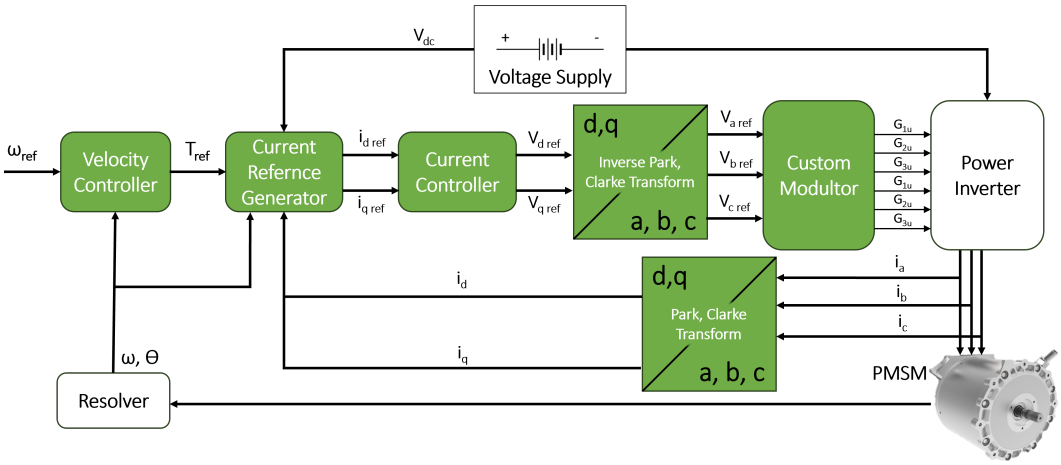


Figure 2.16: Field-Oriented Control

3

Case Setup

This work is a multi-tool analysis with an overview of the workflow visualised in Fig.3.1 with subsequent sections covering these topics in depth.

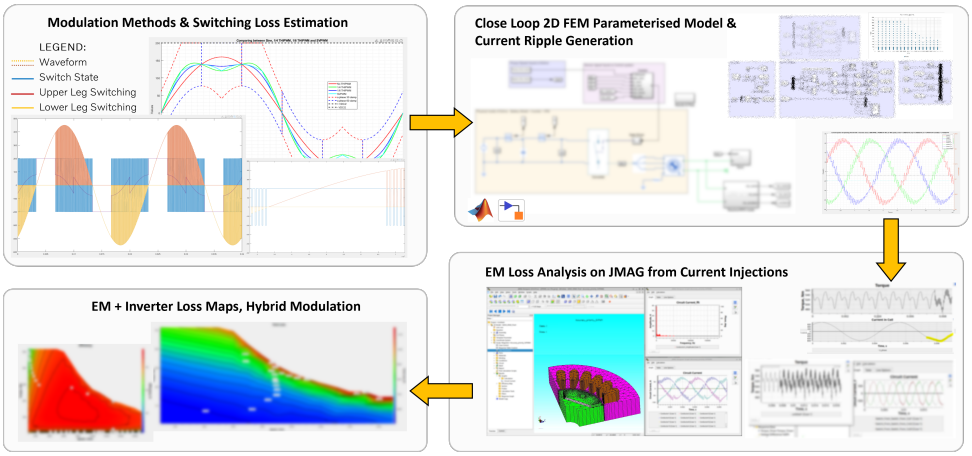


Figure 3.1: Overview of the methodology and workflow

3.1 Modulation techniques

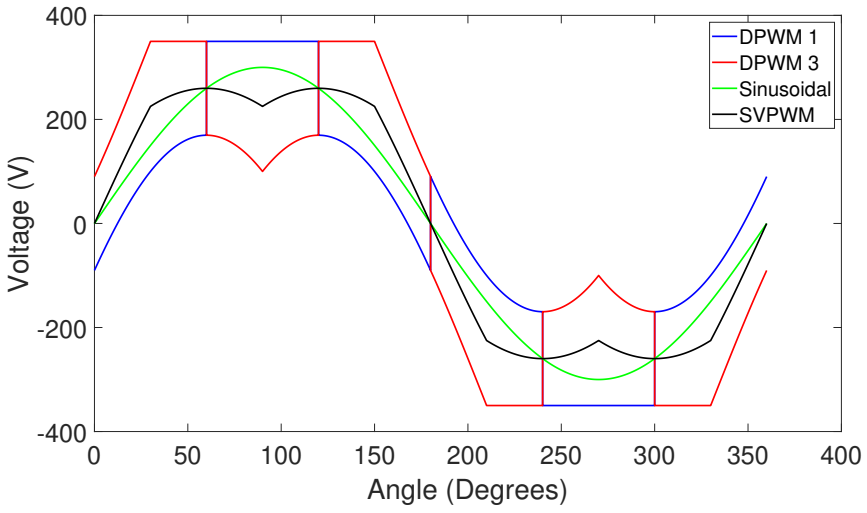


Figure 3.2: DPWM waveforms

The modulation techniques and voltage waveform generation are performed using Matlab R2023b. PWM techniques such as SVPWM, DPWM 0, 1, 2, 3 and NSPWM are investigated.

3.1.1 DPWM 0

This discontinuous method is also called the DPWM 60 leading or the 'Leading Clamp'. To achieve a modulated voltage of the waveform of DPWM 0, a common mode wave is introduced which is computed with the fundamental voltage waveform to achieve the final waveform. The common mode is initially calculated at each instant using the Maximum Magnitude Test (MMT) of the 3 phase voltage waveforms as seen in Fig.3.3. If v_a, v_b, and v_c are the 3 fundamental phase voltages, the common mode waveforms are termed as v_a*, v_b*, and v_c*.

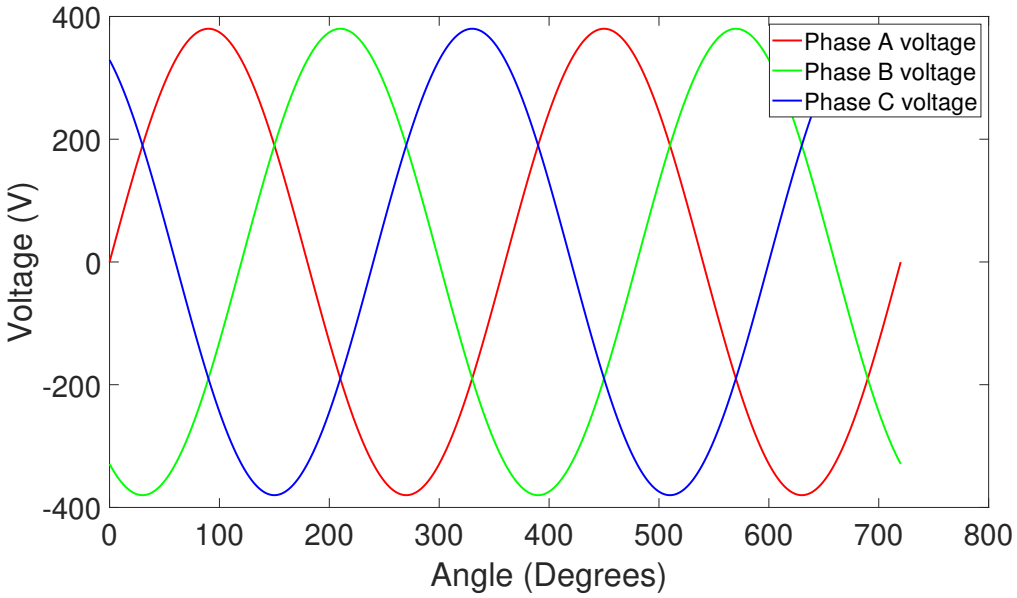


Figure 3.3: 3 phase voltages

The next step involves the imposition of MMT criteria to compute the common modes for each phase as,

$$if\ |v_a| > |v_b|\ \ and\ |v_c| > |v_b|$$

$$v_a^* = \text{sign}(v_a)\frac{U_{dc}}{2} - v_a$$

$$if\ |v_b| > |v_c|\ \ and\ |v_a| > |v_c|$$

$$v_b^* = \text{sign}(v_b)\frac{U_{dc}}{2} - v_b$$

$$if\ |v_c| > |v_a|\ \ and\ |v_c| > |v_b|$$

$$v_c^* = \text{sign}(v_c)\frac{U_{dc}}{2} - v_c$$

The common mode to be added to the fundamental is obtained as,

$$v_{cm} = v_a^* + v_b^* + v_c^*$$

The combined common mode waveform post calculation of MMT is represented in Fig.3.4. The final resultant waveform post addition of common mode to the fundamental voltage waveforms is represented in Fig.3.5

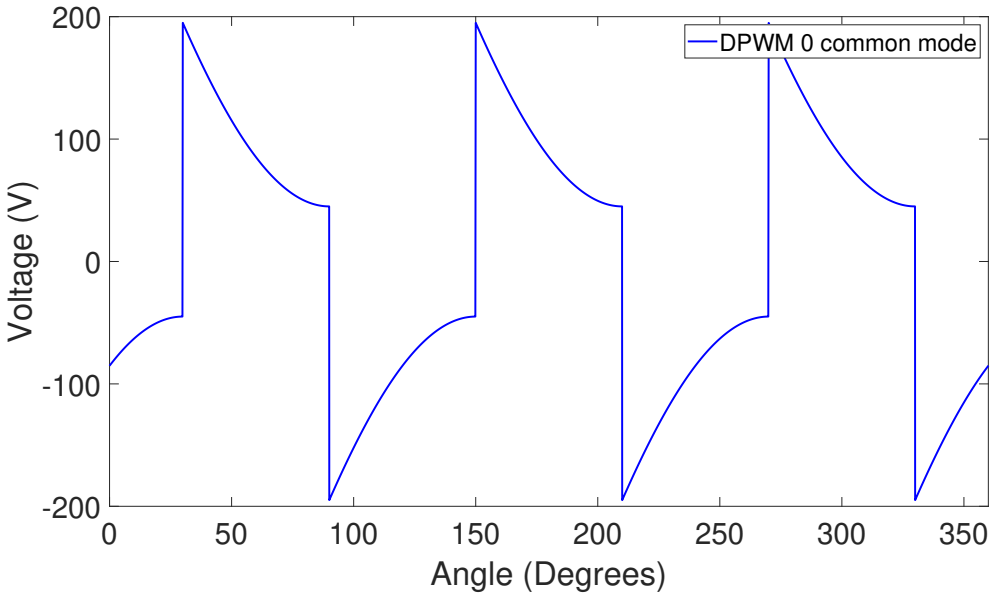


Figure 3.4: DPWM 0 Common Mode

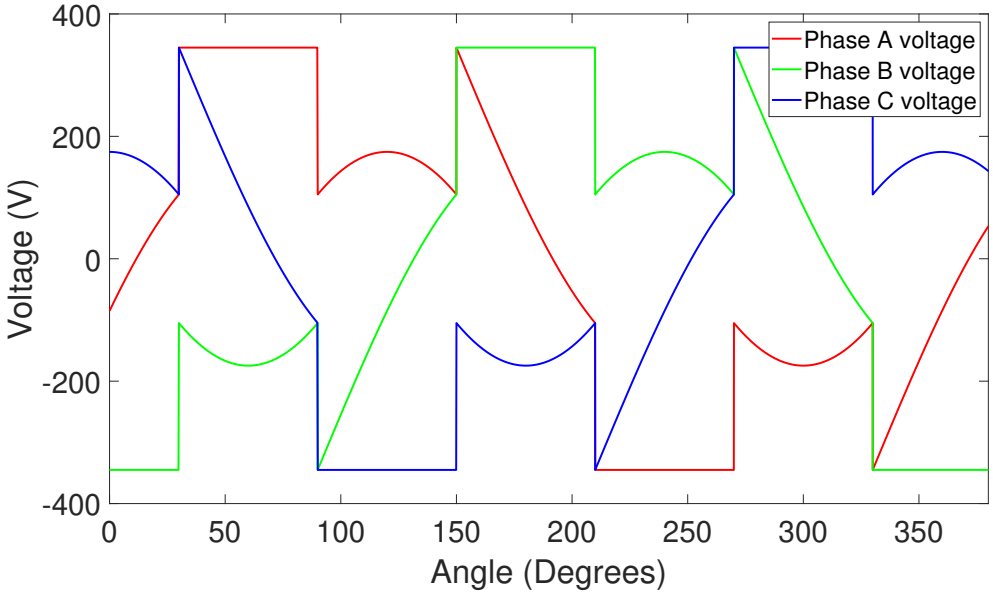


Figure 3.5: 3 phase voltage for DPWM 0

3.1.2 DPWM 1

This discontinuous method is also called the DPWM 60 or the 'Conventional Clamp'. To achieve a modulated voltage of the waveform of DPWM 1, a common mode wave is introduced which is computed with the fundamental voltage waveform to achieve the final waveform. The common mode is initially calculated at each instant using the maximum magnitude test of the 3 phase voltage waveforms. If v_a, v_b, and v_c are the 3 fundamental phase voltages, the common mode waveforms are termed as v_a*, v_b*, and v_c*.

The next step involves the imposition of MMT criteria to compute the common modes for each phase as,

$$\begin{aligned} &if\ |v_a| > |v_b|\ \ and\ |v_a| > |v_c| \\ &\quad v_a^* = \text{sign}(v_a)\tfrac{U_{dc}}{2} - v_a \\ &if\ |v_b| > |v_a|\ \ and\ |v_b| > |v_c| \\ &\quad v_b^* = \text{sign}(v_b)\tfrac{U_{dc}}{2} - v_b \\ &if\ |v_c| > |v_a|\ \ and\ |v_c| > |v_b| \\ &\quad v_c^* = \text{sign}(v_c)\tfrac{U_{dc}}{2} - v_c \end{aligned}$$

The common mode to be added to the fundamental is obtained as„

$$v_{cm} = v_a^* + v_b^* + v_c^*$$

Alternatively, the CM signal(v_{cm_pos}, v_{cm_neg}) is generated from the reference sinusoidal phase voltages ($v_{a\_sin}, v_{b\_sin}, v_{c\_sin}$), using the Maximum Magnitude Tests (MMT). Among the three-phase sinusoidal modulating signals, the maximum and minimum of the three voltage phases during a specific time interval are subtracted from half the DC voltage value and designated as the positive (v_{cm_pos}) and negative (v_{cm_neg}) common mode signal,

$$v_{max\_cm} = \max\{v_{a\_sin}, v_{b\_sin}, v_{c\_sin}\} \tag{3.1}$$

$$v_{min\_cm} = \min\{v_{a\_sin}, v_{b\_sin}, v_{c\_sin}\} \tag{3.2}$$

$$v_{cm\_pos} = \frac{U_{dc}}{2} - v_{max\_cm} \tag{3.3}$$

$$v_{cm\_neg} = -\frac{U_{dc}}{2} - v_{min\_cm} \tag{3.4}$$

The combined common mode waveform post calculation of MMT is represented in Fig.3.6. The final resultant waveform post addition of common mode to the fundamental voltage waveforms is represented in Fig.3.7.

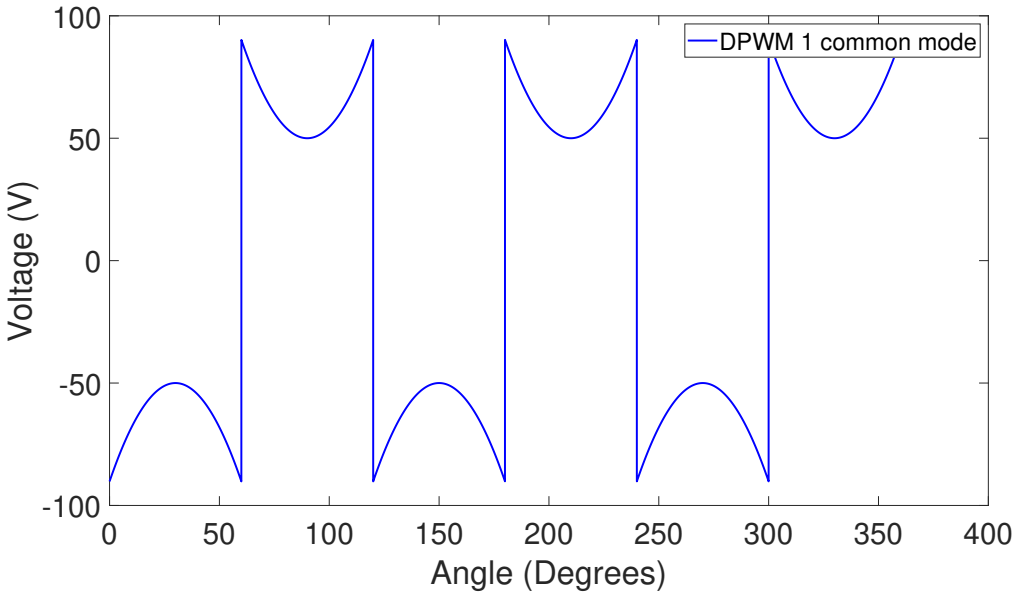


Figure 3.6: DPWM 1 Common Mode

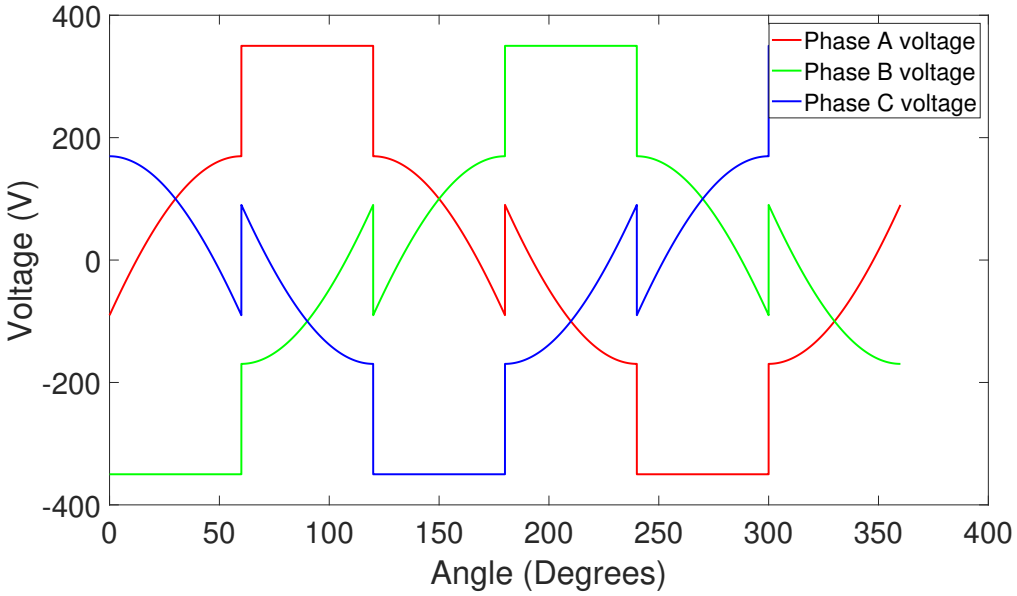


Figure 3.7: 3 phase voltages for DPWM 1

3.1.3 DPWM 2

This discontinuous method is also called the DPWM 60 lagging or the 'Lagging Clamp'. To achieve a modulated voltage of the waveform of DPWM 2, a common mode wave is introduced which is computed with the fundamental voltage waveform to achieve the final waveform. The common mode is initially calculated at each instant using the maximum magnitude test of the 3 phase voltage waveforms. If v_a, v_b, and v_c are the 3 fundamental phase voltages, the common mode waveforms are termed as v_a*, v_b*, and v_c*.

The next step involves the imposition of MMT criteria to compute the common modes for each phase as,

$$
\begin{aligned}
&if \ \ |v_a| > |v_b| \ \ and \ |v_c| > |v_b| \\
&\qquad v_a^* = \text{sign}(v_a)\tfrac{U_{dc}}{2} - v_a \\
&if \ \ |v_b| > |v_c| \ \ and \ |v_a| > |v_c| \\
&\qquad v_b^* = \text{sign}(v_b)\tfrac{U_{dc}}{2} - v_b \\
&if \ \ |v_c| > |v_a| \ \ and \ |v_b| > |v_a| \\
&\qquad v_c^* = \text{sign}(v_c)\tfrac{U_{dc}}{2} - v_c
\end{aligned}
$$

The common mode to be added to the fundamental is obtained as,

$$v_{cm} = v_a^* + v_b^* + v_c^*$$

The combined common mode waveform post calculation of MMT is represented in Fig.3.8. The final resultant waveform post addition of common mode to the fundamental voltage waveforms is represented in Fig.3.9.

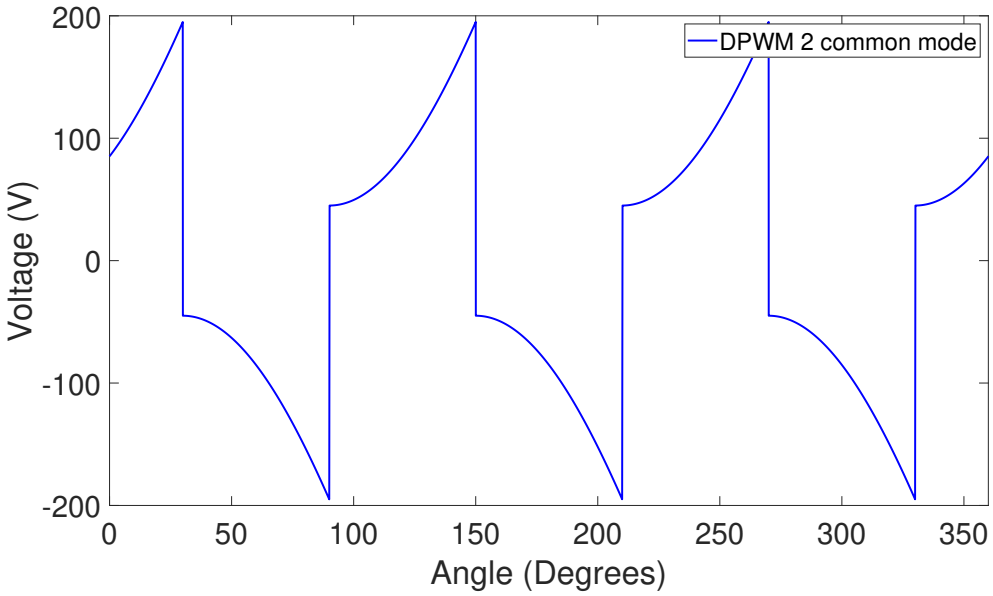


Figure 3.8: DPWM 2 Common Mode

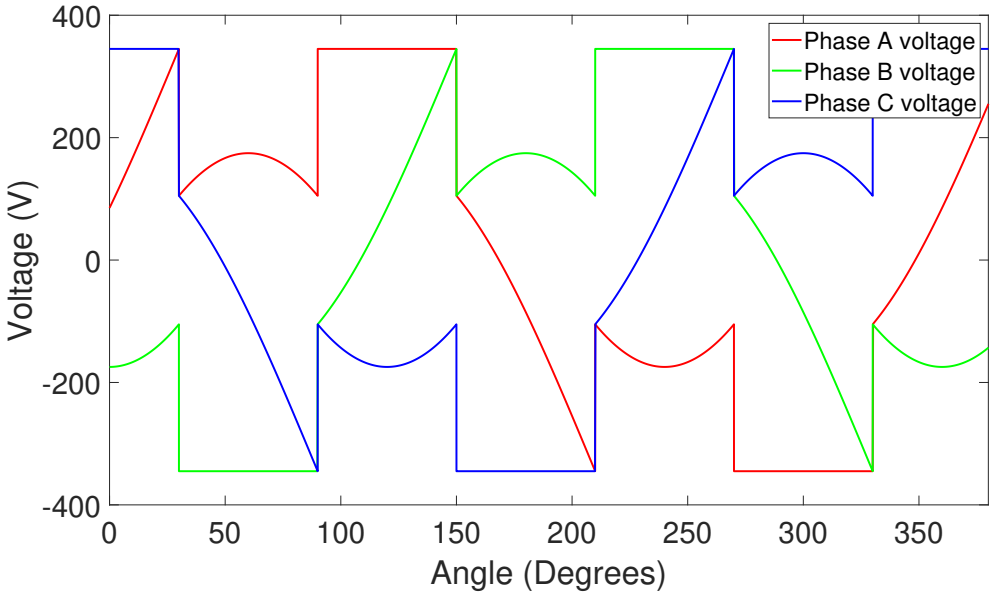


Figure 3.9: 3 phase voltages for DPWM 2

3.1.4 DPWM 3

This discontinuous method is also called the DPWM 30 or the 'Split Clamp'. To achieve a modulated voltage of the waveform of DPWM 3, a common mode wave is introduced which is computed with the fundamental voltage waveform to achieve the final waveform. The common mode is initially calculated at each instant using the maximum magnitude test of the 3 phase voltage waveforms. If v_a, v_b, and v_c are the 3 fundamental phase voltages, the common mode waveforms are termed as v_a*, v_b*, and v_c*.

The next step involves the imposition of MMT criteria to compute the common modes for each phase as,

$$
\begin{aligned}
&if\ \ |v_c| > |v_a|\ \ and\ |v_a| > |v_b| \\
&\quad v_a^* = \text{sign}(v_a)\frac{V_{dc}}{2} - v_a \\
&if\ \ |v_c| > |v_b|\ \ and\ |v_b| > |v_a| \\
&\quad v_b^* = \text{sign}(v_b)\frac{U_{dc}}{2} - v_b \\
&if\ \ |v_a| > |v_c|\ \ and\ |v_c| > |v_b| \\
&\quad v_c^* = \text{sign}(v_c)\frac{U_{dc}}{2} - v_c
\end{aligned}
$$

The common mode to be added to the fundamental is obtained as,

$$v_{cm} = v_a^* + v_b^* + v_c^*$$

Alternatively, the three-phase sinusoidal modulating signals, the maximum of the three voltage phases during a specific time interval is subtracted from half the DC voltage value and designated as the common mode signal. ,

$$v_{\text{max\_cm}} = \max\left\{\text{v}_{\text{a\_sin}}, v_{\text{b\_sin}}, \text{v}_{\text{c\_sin}}\right\} \tag{3.5}$$

$$v_{\text{min\_cm}} = \min\left\{\text{v}_{\text{a\_sin}}, v_{\text{b\_sin}}, \text{v}_{\text{c\_sin}}\right\} \tag{3.6}$$

$$v_{\text{cm\_pos}} = \frac{U_{\text{dc}}}{2} - \text{v}_{\text{max\_cm}} \tag{3.7}$$

$$v_{\text{cm\_neg}} = -\frac{U_{\text{dc}}}{2} - \text{v}_{\text{min\_cm}} \tag{3.8}$$

The combined common mode waveform post calculation of MMT is represented in Fig.3.10. The final resultant waveform post addition of common mode to the fundamental voltage waveforms is represented in Fig.3.11.

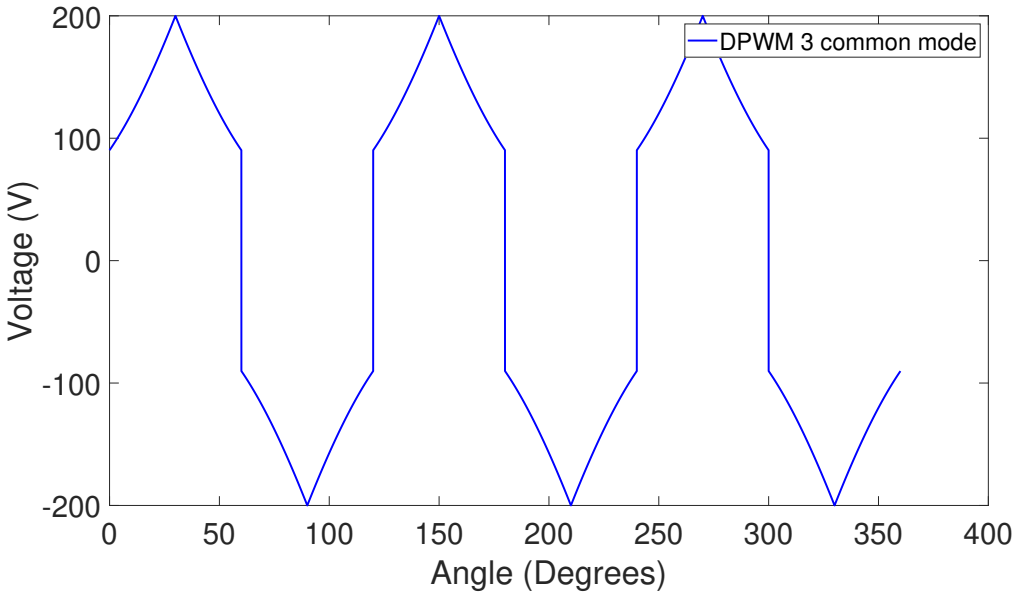


Figure 3.10: DPWM 3 Common Mode

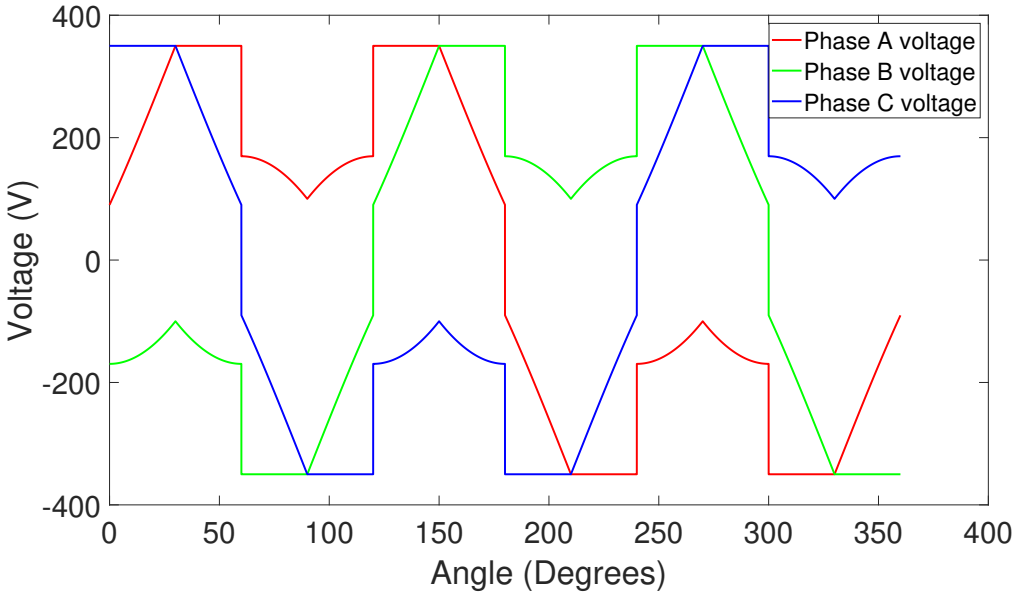


Figure 3.11: 3 phase voltages for DPWM 3

3.1.5 NSPWM

This reduced common mode voltage discontinuous method is also called the DPWM 60 double carrier method. To achieve a modulated voltage of the waveform of NSPWM, a common mode wave is introduced which is the same as the common mode of DPWM 1. [12] The common mode is initially calculated at each instant using the maximum magnitude test of the 3 phase voltage waveforms. If v_a, v_b, and v_c are the 3 fundamental phase voltages, the common mode waveforms are termed as v_a*, v_b*, and v_c*.

The next step involves the imposition of MMT criteria to compute the common modes for each phase as,

$$\begin{aligned} &if\ |v_a| > |v_b|\ \ and\ |v_a| > |v_c| \\ &\quad v_a^* = \text{sign}(v_a)\tfrac{U_{dc}}{2} - v_a \\ &if\ |v_b| > |v_a|\ \ and\ |v_b| > |v_c| \\ &\quad v_b^* = \text{sign}(v_b)\tfrac{U_{dc}}{2} - v_b \\ &if\ |v_c| > |v_a|\ \ and\ |v_c| > |v_b| \\ &\quad v_c^* = \text{sign}(v_c)\tfrac{U_{dc}}{2} - v_c \end{aligned}$$

The common mode to be added to the fundamental is obtained as,

$$v_{cm} = v_a^* + v_b^* + v_c^*$$

The switching states using variable carriers are calculated zone-wise as described in section 2.3.5. If (i) is instantaneous time, then the switching logic to achieve reduced CMV is,

$$S_{a,\text{NSPWM}}(i) = \begin{cases} 1 & \text{if } v_{a,\text{exp60}}(i) > v_{\text{tri1}}(i) \text{ and } 0^\circ \leq \omega\text{t} < 30^\circ, \\ 1 & \text{if } v_{a,\text{exp60}}(i) > v_{\text{tri1}}(i) \text{ and } 30^\circ \leq \omega\text{t} < 90^\circ, \\ 1 & \text{if } v_{a,\text{exp60}}(i) > v_{\text{tri1}}(i) \text{ and } 90^\circ \leq \omega\text{t} < 150^\circ, \\ 1 & \text{if } v_{a,\text{exp60}}(i) > v_{\text{tri2}}(i) \text{ and } 150^\circ \leq \omega\text{t} < 210^\circ, \\ 1 & \text{if } v_{a,\text{exp60}}(i) > v_{\text{tri1}}(i) \text{ and } 210^\circ \leq \omega\text{t} < 270^\circ, \\ 1 & \text{if } v_{a,\text{exp60}}(i) > v_{\text{tri1}}(i) \text{ and } 270^\circ \leq \omega\text{t} < 330^\circ, \\ 1 & \text{if } v_{a,\text{exp60}}(i) > v_{\text{tri1}}(i) \text{ and } 330^\circ \leq \omega\text{t} < 360^\circ. \end{cases}$$

$$S_{b,\mathrm{NSPWM}}(i) = \begin{cases} 1 & \text{if } v_{b,\mathrm{exp60}}(i) > v_{\mathrm{tri2}}(i) \text{ and } 0° \leq \omega t < 30°, \\ 1 & \text{if } v_{b,\mathrm{exp60}}(i) > v_{\mathrm{tri2}}(i) \text{ and } 30° \leq \omega t < 90°, \\ 1 & \text{if } v_{b,\mathrm{exp60}}(i) > v_{\mathrm{tri1}}(i) \text{ and } 90° \leq \omega t < 150°, \\ 1 & \text{if } v_{b,\mathrm{exp60}}(i) > v_{\mathrm{tri1}}(i) \text{ and } 150° \leq \omega t < 210°, \\ 1 & \text{if } v_{b,\mathrm{exp60}}(i) > v_{\mathrm{tri2}}(i) \text{ and } 210° \leq \omega t < 270°, \\ 1 & \text{if } v_{b,\mathrm{exp60}}(i) > v_{\mathrm{tri1}}(i) \text{ and } 270° \leq \omega t < 330°, \\ 1 & \text{if } v_{b,\mathrm{exp60}}(i) > v_{\mathrm{tri1}}(i) \text{ and } 330° \leq \omega t < 360°. \end{cases}$$

$$S_{c,\mathrm{NSPWM}}(i) = \begin{cases} 1 & \text{if } v_{c,\mathrm{exp60}}(i) > v_{\mathrm{tri1}}(i) \text{ and } 0° \leq \omega t < 30°, \\ 1 & \text{if } v_{c,\mathrm{exp60}}(i) > v_{\mathrm{tri1}}(i) \text{ and } 30° \leq \omega t < 90°, \\ 1 & \text{if } v_{c,\mathrm{exp60}}(i) > v_{\mathrm{tri2}}(i) \text{ and } 90° \leq \omega t < 150°, \\ 1 & \text{if } v_{c,\mathrm{exp60}}(i) > v_{\mathrm{tri1}}(i) \text{ and } 150° \leq \omega t < 210°, \\ 1 & \text{if } v_{c,\mathrm{exp60}}(i) > v_{\mathrm{tri1}}(i) \text{ and } 210° \leq \omega t < 270°, \\ 1 & \text{if } v_{c,\mathrm{exp60}}(i) > v_{\mathrm{tri2}}(i) \text{ and } 270° \leq \omega t < 330°, \\ 1 & \text{if } v_{c,\mathrm{exp60}}(i) > v_{\mathrm{tri2}}(i) \text{ and } 330° \leq \omega t < 360°. \end{cases}$$

The combined common-mode voltage for NSPWM (*CMV_NSPWM*) is computed using the formula:

$$CMV\_NSPWM(i) = \frac{U_{dc}\left(S_{a,\mathrm{NSPWM}}(i) + S_{b,\mathrm{NSPWM}}(i) + S_{c,\mathrm{NSPWM}}(i) - 1.5\right)}{3} \tag{3.9}$$

where:

- U_{dc} is the DC link voltage,
- $S_{a,\mathrm{NSPWM}}$ is the switching state for phase A in NSPWM,
- $S_{b,\mathrm{NSPWM}}$ is the switching e for phase B in NSPWM,
- $S_{c,\mathrm{NSPWM}}$ is the switching state for phase C in NSPWM,
- The constant 1.5 adjusts the sum state of the switching states.

As observed from Fig.3.12, the computed CMV for DPWM 0 varies between $+v_{\mathrm{dc}/2}$ and $-v_{\mathrm{dc}/2}$, making it a high CMV discontinuous method. On the contrary, as observed from Fig.3.14, the dual carrier NSPWM method yields a lower CMV of $+v_{\mathrm{dc}/6}$ and $-U_{\mathrm{dc}/6}$.[12] This lives up to the convention of NSPWM being classified as a 'Reduced Common Mode Voltage Pulse Width Modulation' (RCMVPWM) technique.[12] The results from these claims are discussed in detail in section 4.1.

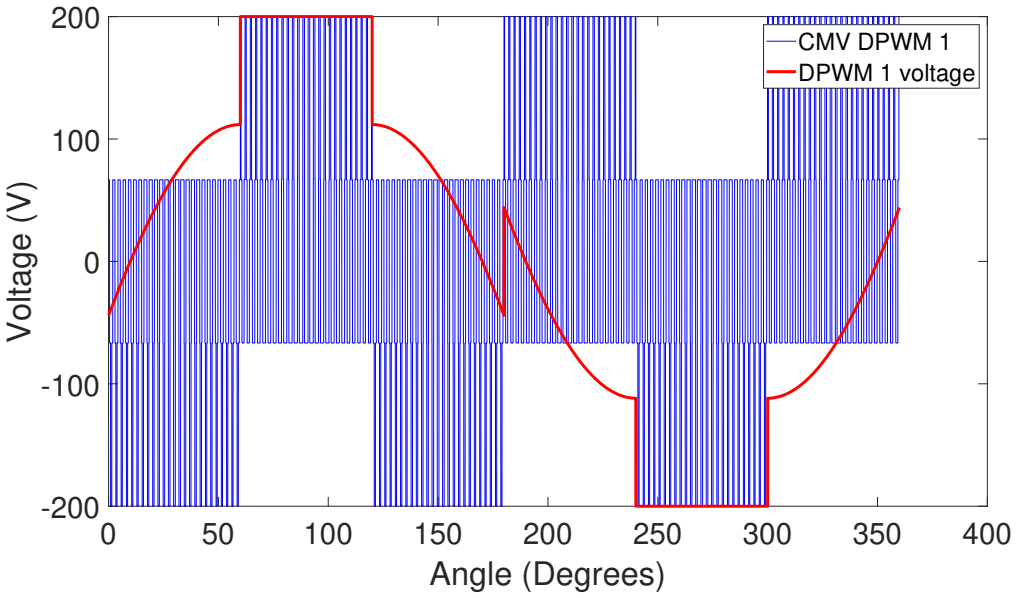


Figure 3.12: High CMV for DPWM 1 ($+U_{\mathrm{dc}/6}$ to $-U_{\mathrm{dc}/6}$)

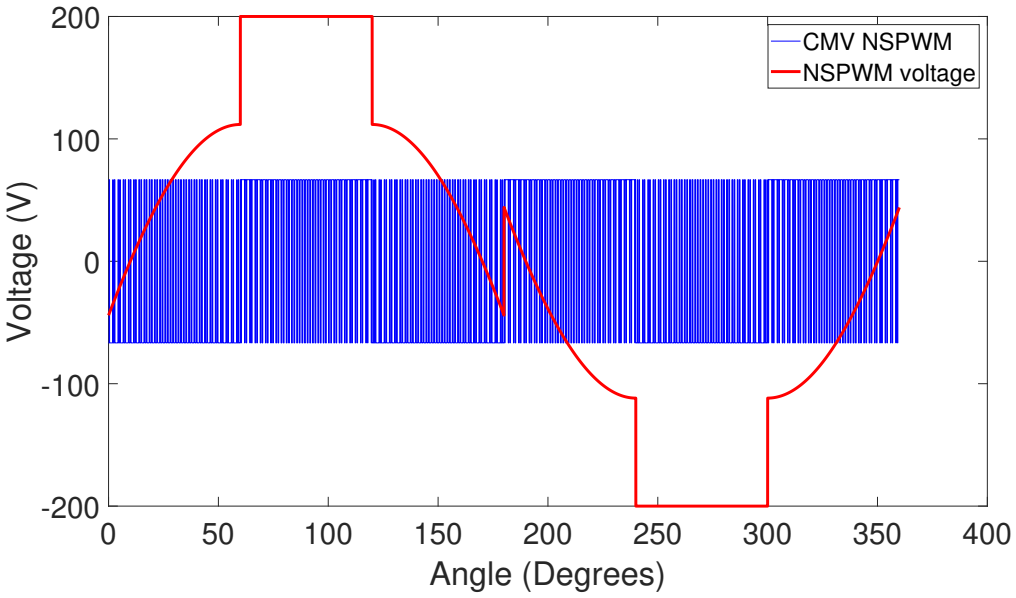
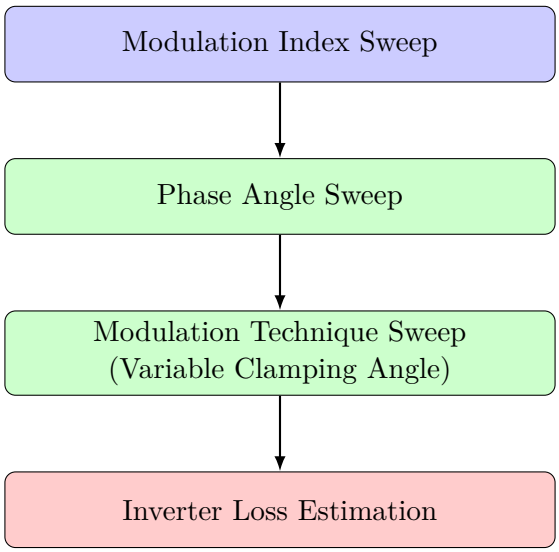


Figure 3.13: Reduced CMV for NSPWM ($+U_{\mathrm{dc}/6}$ to $-U_{\mathrm{dc}/6}$)

3.2 Active clamping implementation

Each discontinuous modulation technique demonstrates different behaviour across various regions of the torque-speed map of the electric machine, indicating that relying on just one modulation technique is not ideal for all operating conditions. To address this, a detailed analysis is conducted to determine the optimal modulation technique for each phase angle of the electric machine. This analysis demands the creation of a hybrid modulation technique, which combines all the individual DPWM techniques. The hybrid approach utilizes a highly sensitive phase angle map of the electric machine to dynamically switch between modulation techniques to achieve the lowest switching losses. By applying this characterization to the phase angle map, a comprehensive hybrid modulation map is developed. This map integrates all the modulation techniques and selects the most suitable one based on the specific phase angle, thereby optimizing for efficiency. This approach enables the use of a combination of modulation techniques rather than relying on a single one, effectively minimizing inverter losses across the entire operating range of the electric machine. The core of this implementation is the inverter loss modelling as described in section 3.4. The model calculates the switching and conduction loss values across the torque speed map using custom-built switching and conduction loss functions, for all techniques swept through. The loss calculation workflow is as follows,



The optimisation begins by selecting an initial modulation index, for which an initial phase angle is also selected. All possible clamping angles are evaluated for this combination from (0 to +90 degrees). Switching and conduction losses are computed for all clamping angle possibilities for this combination. The loop is next updated to the following phase angle and losses for all clamping angles are computed again. The phase angle sweep is swept from (-90 to +90 degrees) from purely capacitive to purely inductive loads. Once all combinations of phase angles and clamping angles are computed, the modulation index is updated. This intensive loop continues again until all combinations are executed. The most optimal combinations are then stored

and computed for further optimisation.

For instance, a few examples of the active clamping optimisation function estimation are,

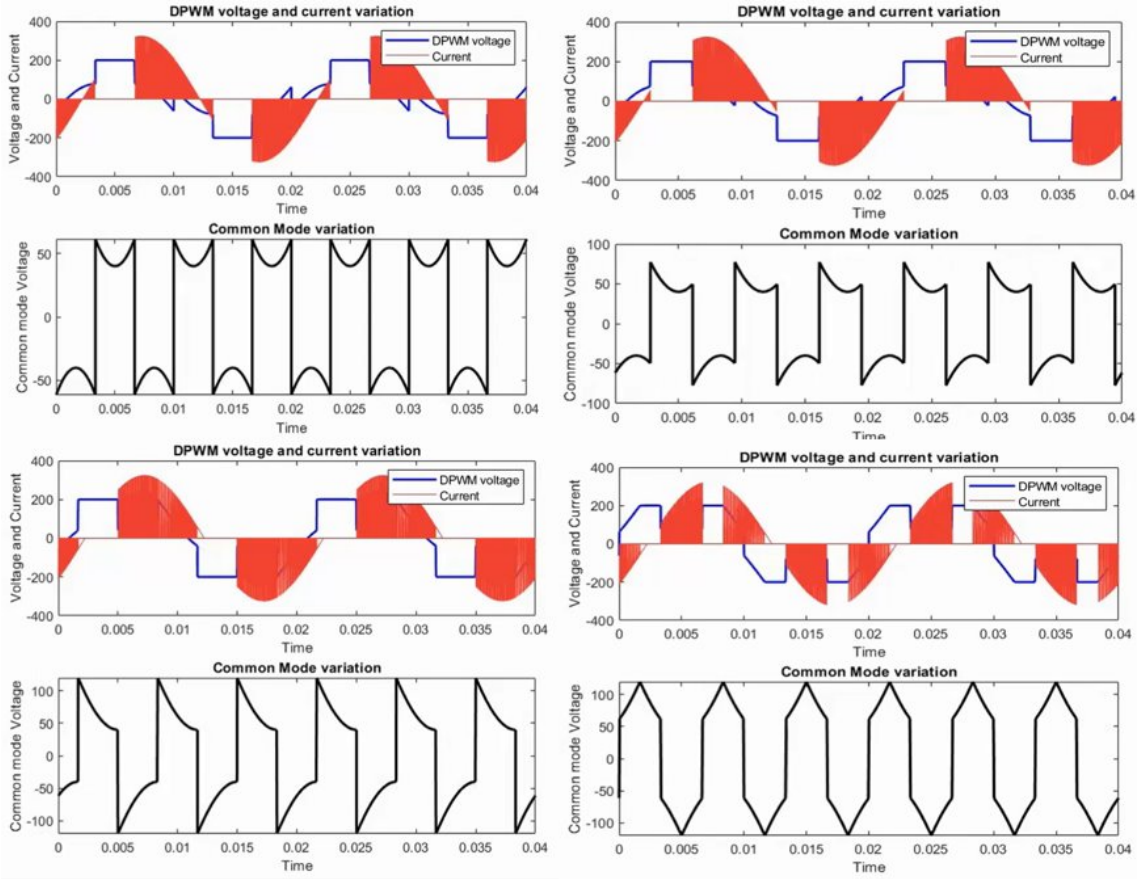


Figure 3.14: Active clamping optimisation examples

The results from the optimisation are narrowed down to the trend presented in Fig.3.15 for phase angles of (-90 to +90) degrees. The modulation techniques in turn are then narrowed down against phase angles, as shown in Table.3.1.

Table 3.1: Selection of DPWM Techniques Based on Phase Angles

Phase Angle Range	**DPWM Technique**
$\phi < 0°$	DPWM 0
$0° \leq \phi < 17.5°$	DPWM 1
$17.5° \leq \phi < 77°$	DPWM 2
$77° \leq \phi \leq 90°$	DPWM 3

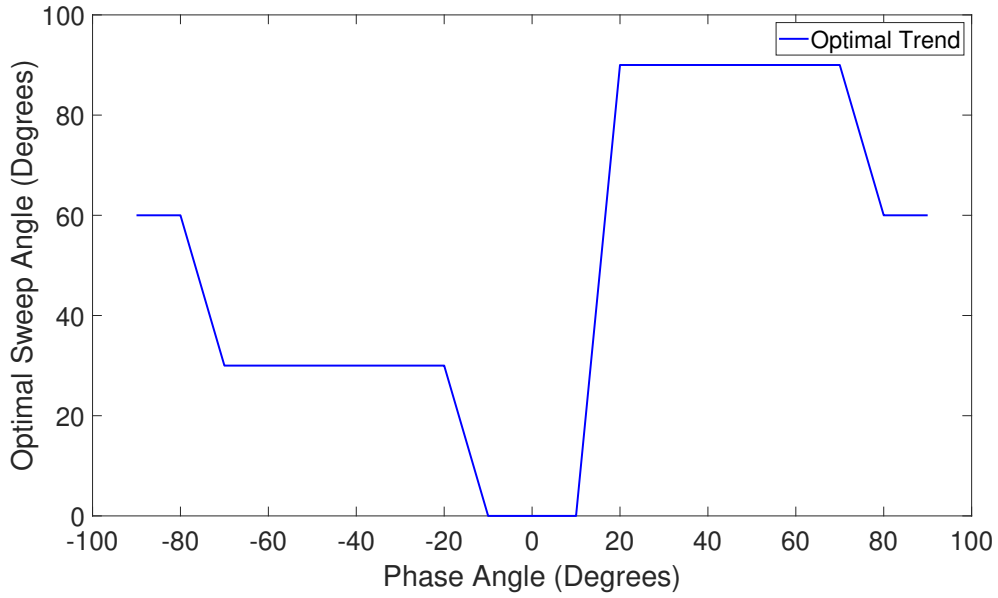


Figure 3.15: Active clamping optimisation trend

The individual techniques are displayed in Fig.3.16, Fig.3.17, Fig.3.18 and Fig.3.19 as a function of phase angle.

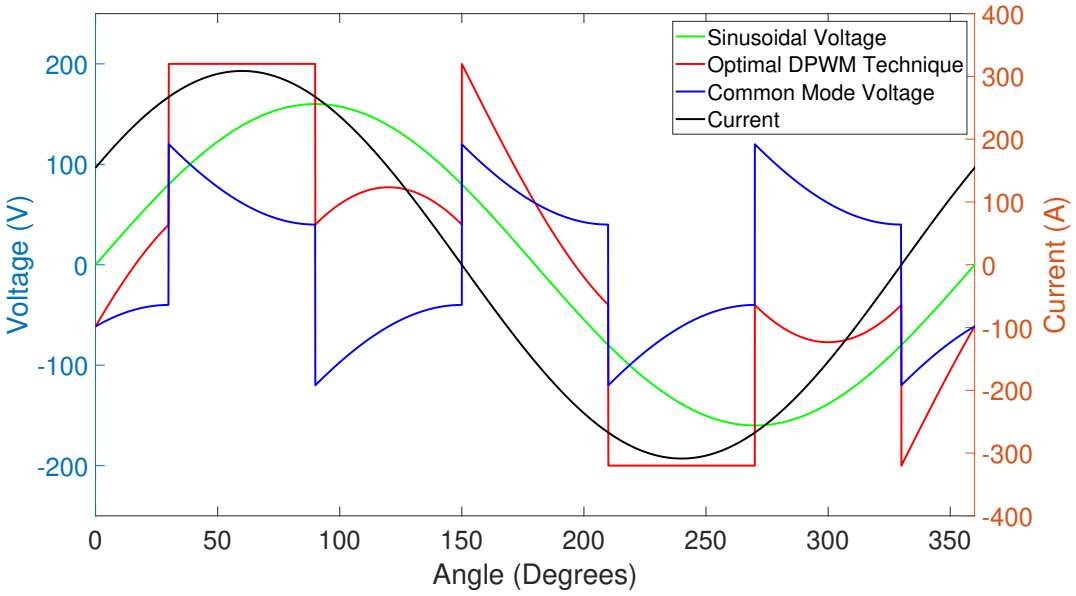


Figure 3.16: Optimised DPWM technique for phase angle of -30 degrees

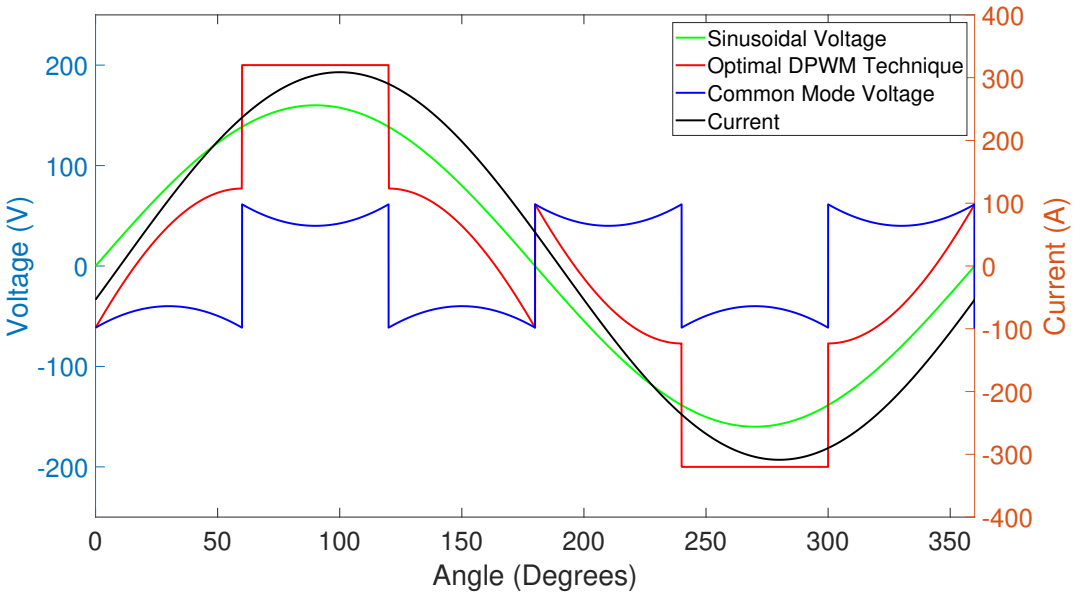


Figure 3.17: Optimised DPWM technique for phase angle of 10 degrees

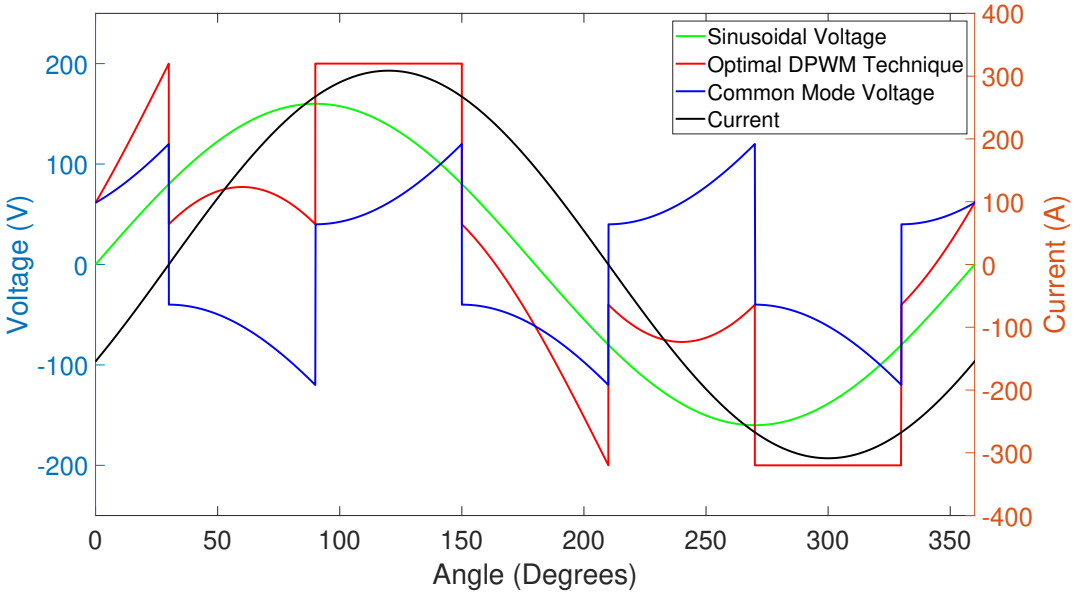


Figure 3.18: Optimised DPWM technique for phase angle of 30 degrees

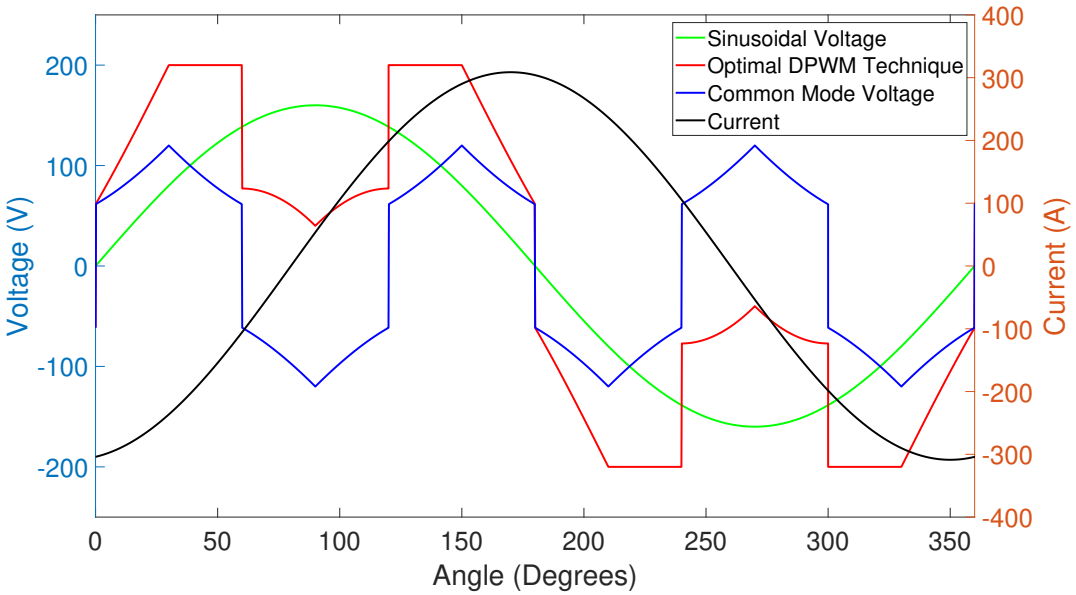


Figure 3.19: Optimised DPWM technique for phase angle of 80 degrees

The non-linear 3D variation plot of switching loss trend variation vs clamping angle vs phase shift is presented in Fig.3.20.

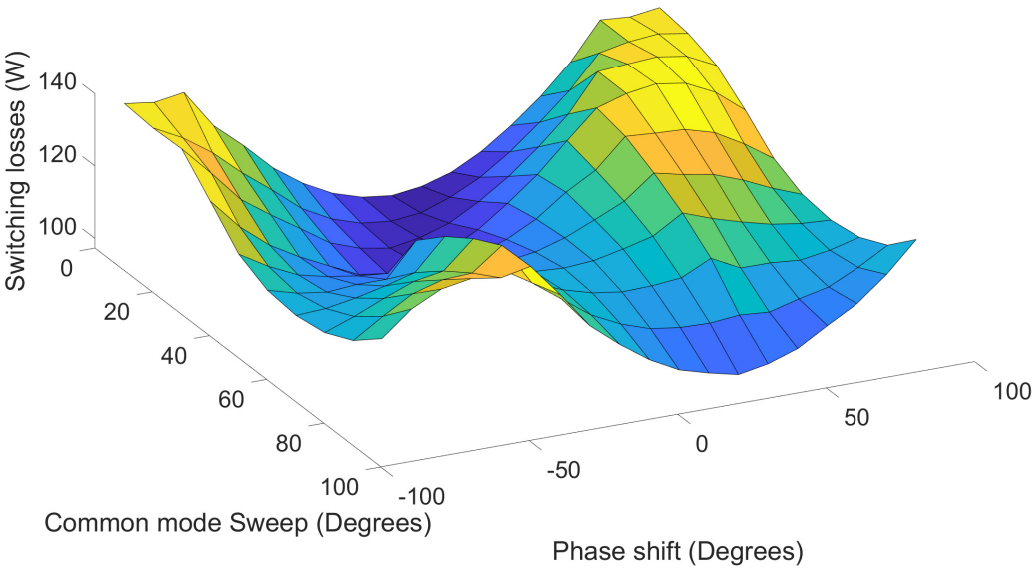


Figure 3.20: Switching loss trend variation vs clamping angle vs phase shift

The electric machine is characterised for different phase angles, which are plotted against the torque-speed curve as presented in Fig.3.21.

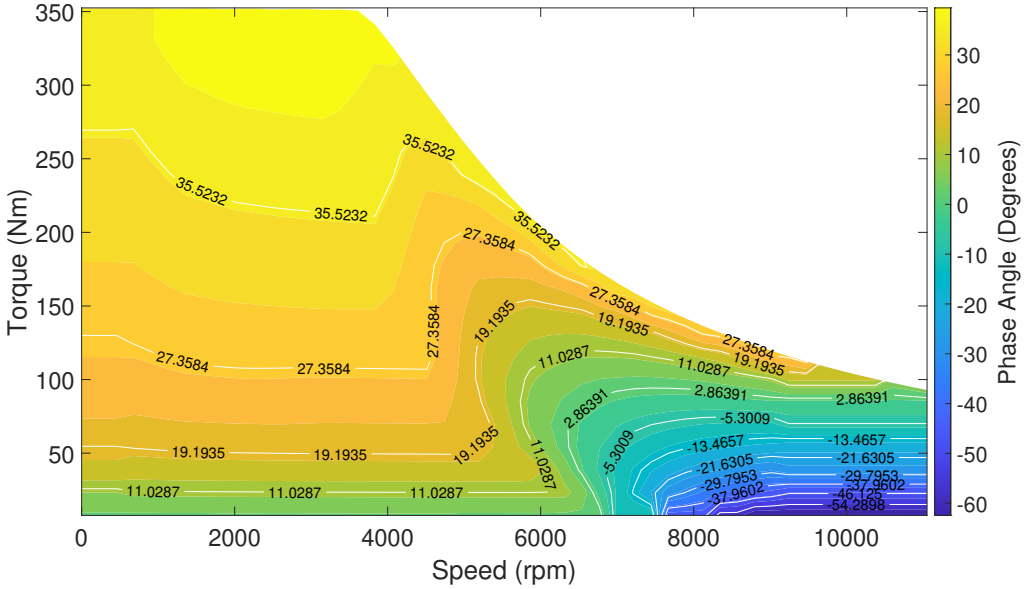


Figure 3.21: Electric machine phase angle map vs T-w

In conclusion, based on the phase angle characterisation map in Fig.3.21 and results from the dynamic active clamping script, the two results are combined in tandem to produce an optimised hybrid modulation technique for inverter loss optimisation, for this particular electric machine. This script is scalable and applicable to other electric machine topologies. The final hybrid modulation map for optimised inverter efficiency is visualised in Fig.4.1.

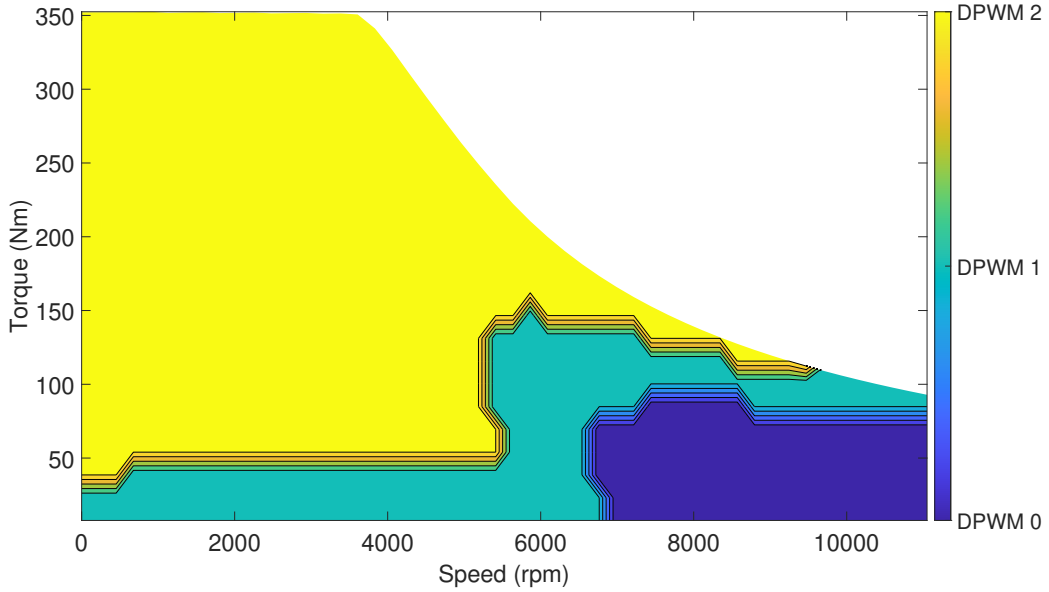


Figure 3.22: Hybrid Modulation Map

3.3 Hybrid Modulation in closed loop control

The active clamping algorithm is verified and validated for several test cases to ensure dynamic phase angle adaptation while implemented onto the FOC model on Simulink. This involves extraction of voltage signals using Inverse Clarke and Park transformations from the direct-axis voltage (U_d) and quadrature-axis voltage (U_q) outputs from the current controller using a feed-forward reference control.

A custom hybrid modulator is designed within the electric drive control block set with reference voltages and phase angles as the inputs into the block. The output from the custom hybrid modulator block is sent to the gate terminals as signals for the switches to turn on or off according to their respective optimised switching patterns. The input to the hybrid modulator is a combined 3-phase signal which is then demuxed to separate the 3-phase voltages. These phase voltages are manipulated using a combined logic of active clamping as a function of phase angle as described earlier, and also the modulation technique implementation as described in section 2.3. The output signals are the final modulated voltage waveforms which are then compared against the triangle carrier wave, which then sends the gate signals to the gate driver terminals.

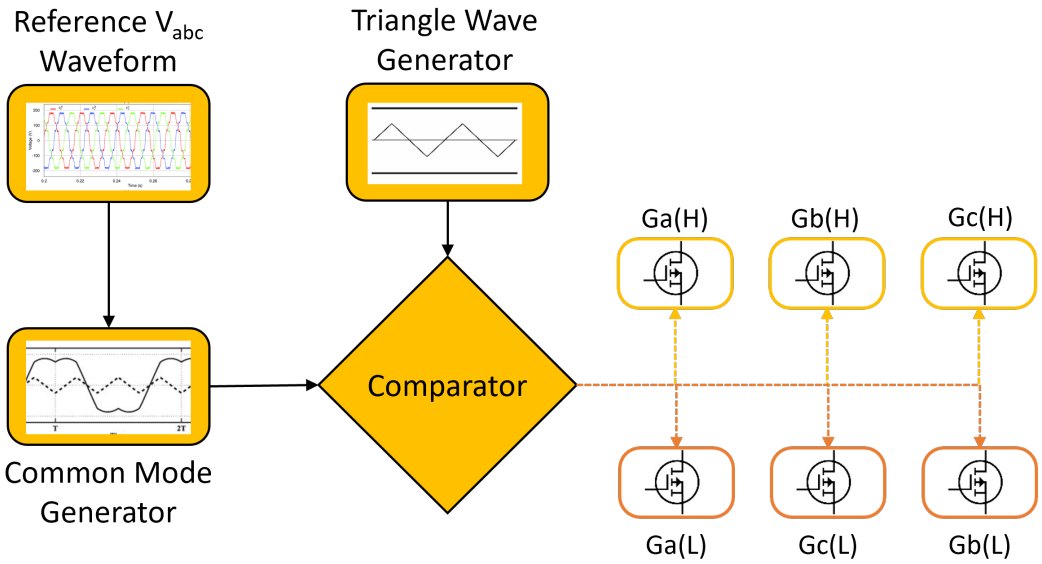


Figure 3.23: Simplified flow of the Custom Modulator

The core of the custom modulator is a MATLAB function within Simulink that takes in v_a, v_b, v_c and phase angle(ϕ) as inputs. The $v_{a_{\sin}}$, $v_{b_{\sin}}$, $v_{c_{\sin}}$ variables are identical to v_a, v_b, v_c and are extracted as separate comparison waves in the logic blocks. The conditions within the function to calculate common mode and modulated waveform are as follows,

1. **Input:** ϕ, v_a, v_b, v_c, $v_{a_{\sin}}$, $v_{b_{\sin}}$, $v_{c_{\sin}}$, $U_{\text{dc\_query}}$

2. **Determine the Range of ϕ:**

   (a) If $0 < \phi < 17.5$: DPWM 1
   - Determine which voltage signal has the highest magnitude:

$$\begin{aligned} \text{If } |v_a| > |v_b| \text{ and } |v_a| > |v_c| &\Rightarrow v_{a_{\sin}} \\ \text{If } |v_b| > |v_a| \text{ and } |v_b| > |v_c| &\Rightarrow v_{b_{\sin}} \\ \text{Otherwise} &\Rightarrow v_{c_{\sin}} \end{aligned}$$

   (b) If $17.5 \leq \phi < 73$: DPWM 2
   - Determine which voltage signal has the highest magnitude:

$$\begin{aligned} \text{If } |v_a| > |v_b| \text{ and } |v_c| > |v_b| &\Rightarrow v_{a_{\sin}} \\ \text{If } |v_b| > |v_c| \text{ and } |v_a| > |v_c| &\Rightarrow v_{b_{\sin}} \\ \text{Otherwise} &\Rightarrow v_{c_{\sin}} \end{aligned}$$

   (c) If $\phi < 0$: DPWM 0
   - Determine which voltage signal has the highest magnitude:

$$\begin{aligned} \text{If } |v_a| > |v_b| \text{ and } |v_c| > |v_b| &\Rightarrow v_{c_{\sin}} \\ \text{If } |v_b| > |v_c| \text{ and } |v_a| > |v_c| &\Rightarrow v_{a_{\sin}} \\ \text{Otherwise} &\Rightarrow v_{b_{\sin}} \end{aligned}$$

   (d) If ϕ is outside the specified ranges:
   - Set $v_{\text{cm}} = 0$ (or any default value or behavior).

3. **Calculate Common-Mode Voltage for Each Phase:**

   - Compute v_{cm} for the selected phase:

$$\begin{aligned} v_{\text{cm},a} &= \text{sign}(v_{a_{\sin}}) \cdot \left(\frac{U_{\text{dc\_query}}}{2} \right) - v_{a_{\sin}} \\ v_{\text{cm},b} &= \text{sign}(v_{b_{\sin}}) \cdot \left(\frac{U_{\text{dc\_query}}}{2} \right) - v_{b_{\sin}} \\ v_{\text{cm},c} &= \text{sign}(v_{c_{\sin}}) \cdot \left(\frac{U_{\text{dc\_query}}}{2} \right) - v_{c_{\sin}} \end{aligned}$$

   - Sum the calculated common-mode voltages:

$$v_{\text{cm}} = v_{\text{cm},a} + v_{\text{cm},b} + v_{\text{cm},c}$$

Similar to the above workflow, the modulator flow for NSPWM is the same as DPWM 1. The difference here between the techniques is the switch states using a dual carrier comparison method as described in section 2.3.5. If v_{tri1} and v_{tri2} are 2 polar opposite carrier waves with the same switching frequency, the switching logic workflow is,

1. **Input:** v_a, v_b, v_c, v_{tri}, v_{tri2}, $U_{\text{dc\_query}}$

2. **Determine Switching States:**

   (a) For each phase voltage:

   - **If** $v_a = \frac{U_{\mathbf{dc\_query}}}{2}$**:**

     $$S_a = \text{true}, \quad S_b = (v_b \geq v_{\text{tri}}), \quad S_c = (v_c \geq v_{\text{tri2}})$$

   - **If** $v_b = \frac{U_{\mathbf{dc\_query}}}{2}$**:**

     $$S_a = (v_a \geq v_{\text{tri2}}), \quad S_b = \text{true}, \quad S_c = (v_c \geq v_{\text{tri}})$$

   - **If** $v_c = \frac{U_{\mathbf{dc\_query}}}{2}$**:**

     $$S_a = (v_a \geq v_{\text{tri}}), \quad S_b = (v_b \geq v_{\text{tri2}}), \quad S_c = \text{true}$$

   - **If** $v_a = -\frac{U_{\mathbf{dc\_query}}}{2}$**:**

     $$S_a = \text{false}, \quad S_b = (v_b \geq v_{\text{tri2}}), \quad S_c = (v_c \geq v_{\text{tri}})$$

   - **If** $v_b = -\frac{U_{\mathbf{dc\_query}}}{2}$**:**

     $$S_a = (v_a \geq v_{\text{tri}}), \quad S_b = \text{false}, \quad S_c = (v_c \geq v_{\text{tri2}})$$

   - **If** $v_c = -\frac{U_{\mathbf{dc\_query}}}{2}$**:**

     $$S_a = (v_a \geq v_{\text{tri2}}), \quad S_b = (v_b \geq v_{\text{tri}}), \quad S_c = \text{false}$$

   - **Otherwise:**

     $$S_a = (v_a \geq v_{\text{tri}}), \quad S_b = (v_b \geq v_{\text{tri2}}), \quad S_c = (v_c \geq v_{\text{tri}})$$

3.3.1 Hybrid Modulator Validation

The hybrid modulator is constructed as described in section 3.3.1, the working of the modulator is validated against the default modulators available as a part of the Simscape electrical package. The default Simscape electrical modulator block allows freedom in selecting one type of continuous or discontinuous modulation technique across the entire computation time range. However, due to the scope of this thesis work involving dynamic optimisation using modulation techniques, the default modulator is limiting.

The custom hybrid modulator is set up and tested to replicate the behaviour of the default modulator, for DPWM 0, DPWM 1 and DPWM 2, which are the most optimal for this electric machine as derived from the active clamping script. The performance of the default modulator vs the custom hybrid modulator is compared below. Using Simulink monitors to track the outputs of each modulator block at each instant, the variation in output voltages is observed. The visualisations comparing output voltage waveforms from the default and custom modulators are presented below in Fig. 3.24, Fig. 3.25, and Fig. 3.26.

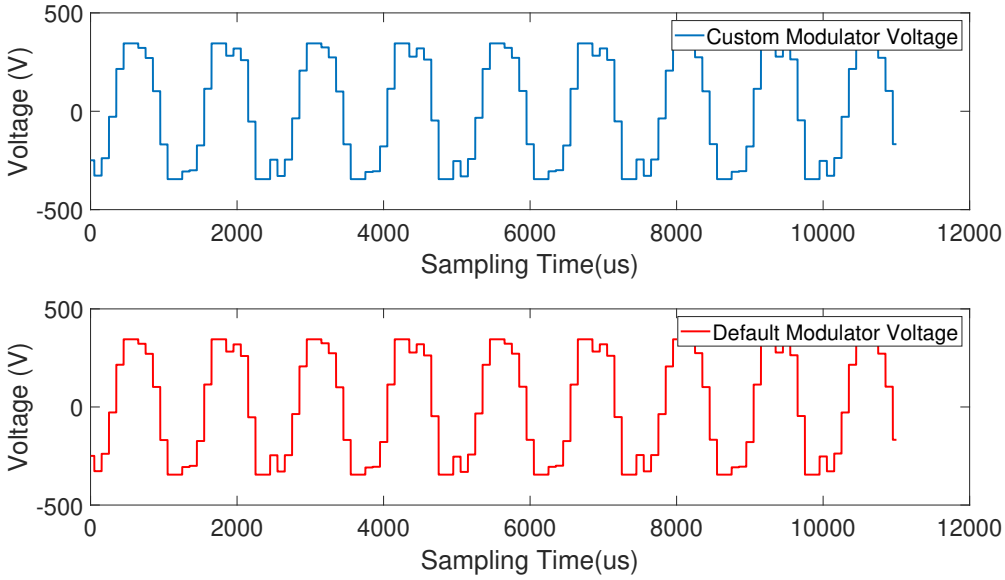


Figure 3.24: Custom vs Default modulator voltage for DPWM 0

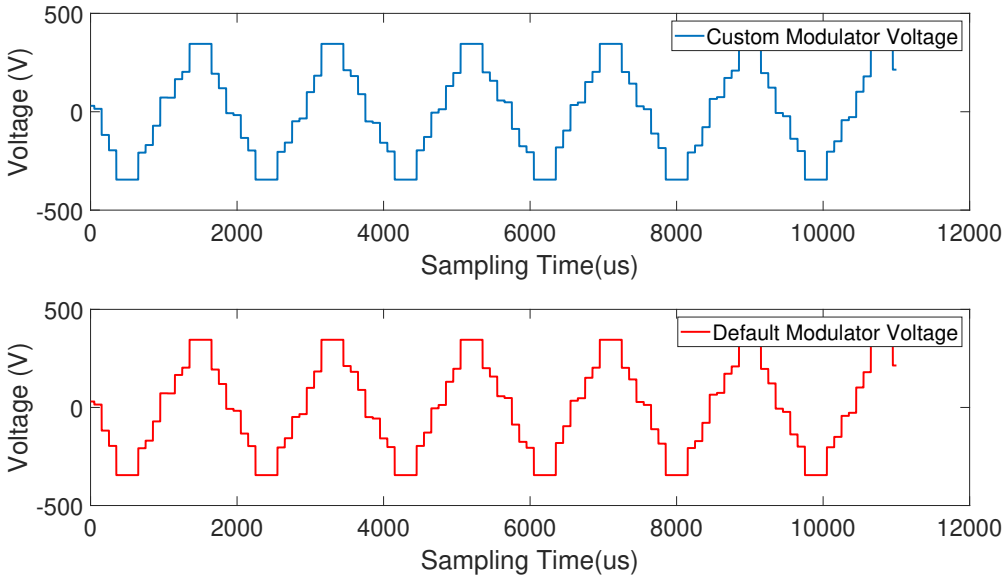


Figure 3.25: Custom vs Default modulator voltage for DPWM 1

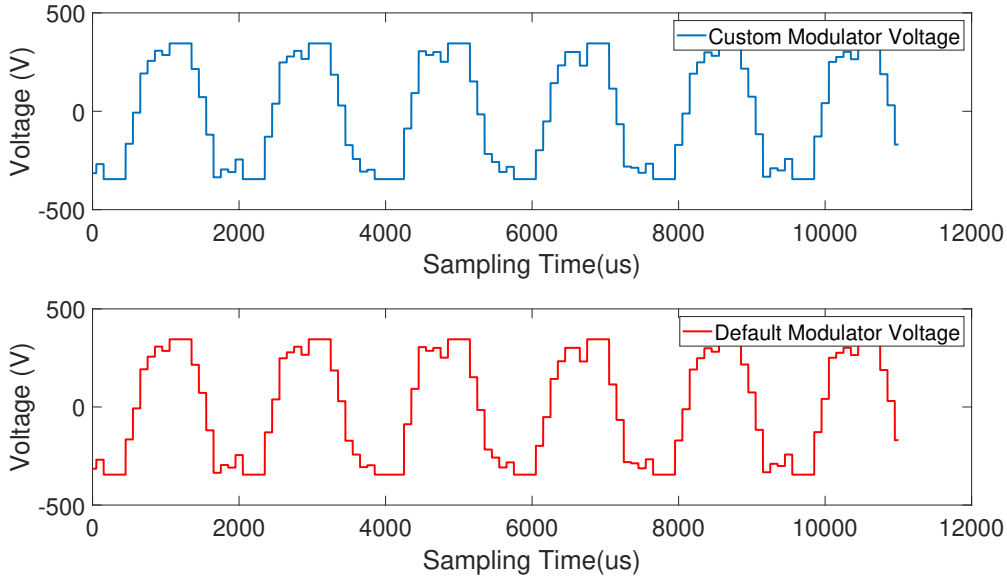


Figure 3.26: Custom vs Default modulator voltage for DPWM 2

As observed from Fig. 3.24, 3.25, and 3.26, the output voltage waveforms from the custom modulator perfectly align with the output voltage waveforms from the default modulator. This ensures that the hybrid modulator's behaviour is consistent with the default system modulator and that there is no discrepancy in output currents obtained from the Simulink blocks which are eventually used in the JMAG current feeding loss analysis.

3.4 SiC MOSFET inverter loss modelling

To estimate the switching and conduction losses in the inverter, a numerical model is used in MATLAB. This keeps the underlying model flexible, to operate across all the modulation techniques. Current, voltage and power factors are used to evaluate the inverter losses, for different I_d, I_q vs frequency (that translates for different torques and speeds) generated as a series of maps.

For the scope of this work, a series of lookup tables are used to reference switching energies, resistance and forward voltage for different operational voltages, currents and temperatures. An equivalent automotive grade SiC MOSFET module as compared to the one used in this thesis work [23] and its published specifications at 25°C are provided in Table. 3.2 for reference. A time step resolution of 1μs is taken, balancing accuracy with computational requirements. This however, doesn't allow for the modelling of dead time that is typically in nanoseconds, and the associated compensations and voltage behaviours, and is hence not considered in this work.

Table 3.2: SiC MOSFET Specifications & Parameter List

Parameter	Symbol	Value
Manufacturer		Wolfspeed
Model		EAB450M12XM3
Drain source breakdown voltage	v_{DS}	1200 V
Continuous drain current	I_D	450 A
Instantaneous drain current	I_{DM}	900 A
Switching frequency	f_{sw}	10/15 kHz
MOSFET forward voltage	v_{GS}	2.5 V
Diode forward voltage	v_{SD}	4.7 V
On state Resistance (450A)	R_{DS}	2.6 mΩ
Switch ON Energy (600V, 450A)	E_{on}	11 mJ
Switch OFF Energy (600V, 450A)	E_{off}	10.1 mJ

An example of the current split between the upper and lower MOSFET and diode of a phase leg is shown in Fig.3.27 as per the equations in Section.2.5.This current split is then used to calculate the conduction power loss as seen in Fig.3.28 and the switching power losses as visualised in Fig.3.29 3.30. The case shown here is an implementation of DPWM1, where both the voltage clamping as well as the lack of switching instances when clamped can be observed. This leads to an improvement in switching losses, while conduction losses stay the same and are not affected by clamping.

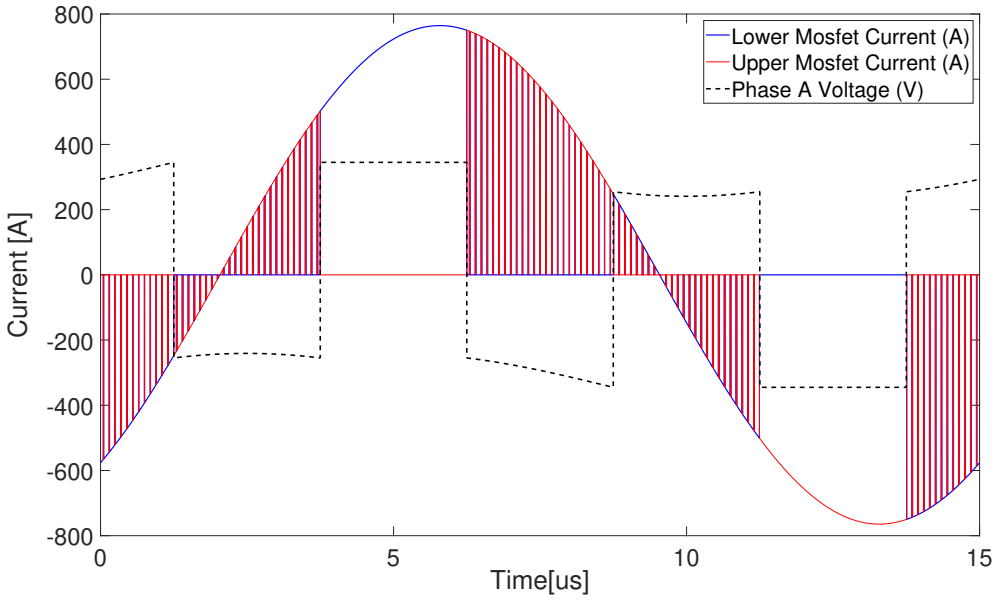


Figure 3.27: Current split within a phase leg for DPWM1

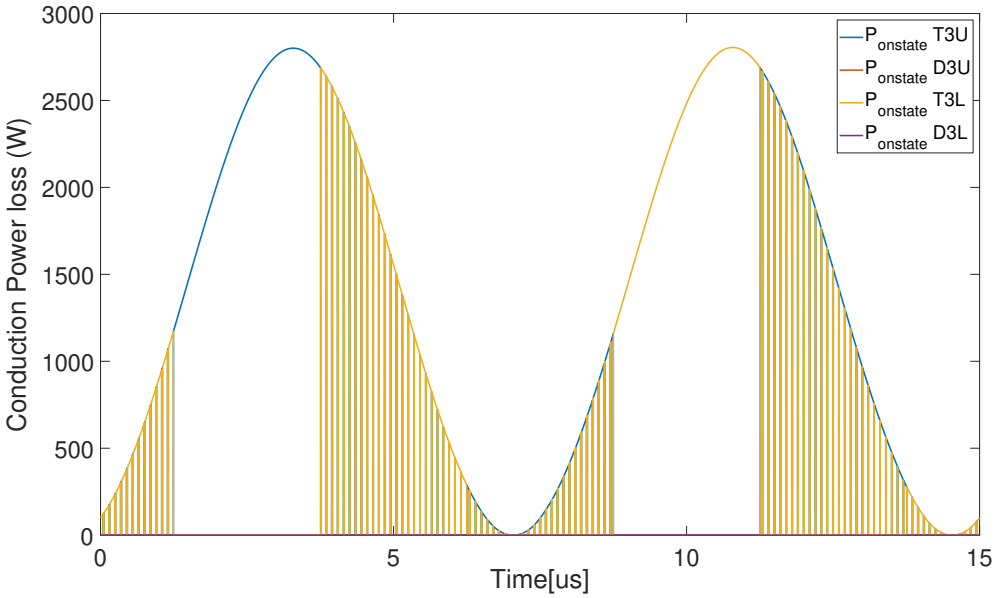


Figure 3.28: Onstate conduction losses in a phase leg for DPWM1

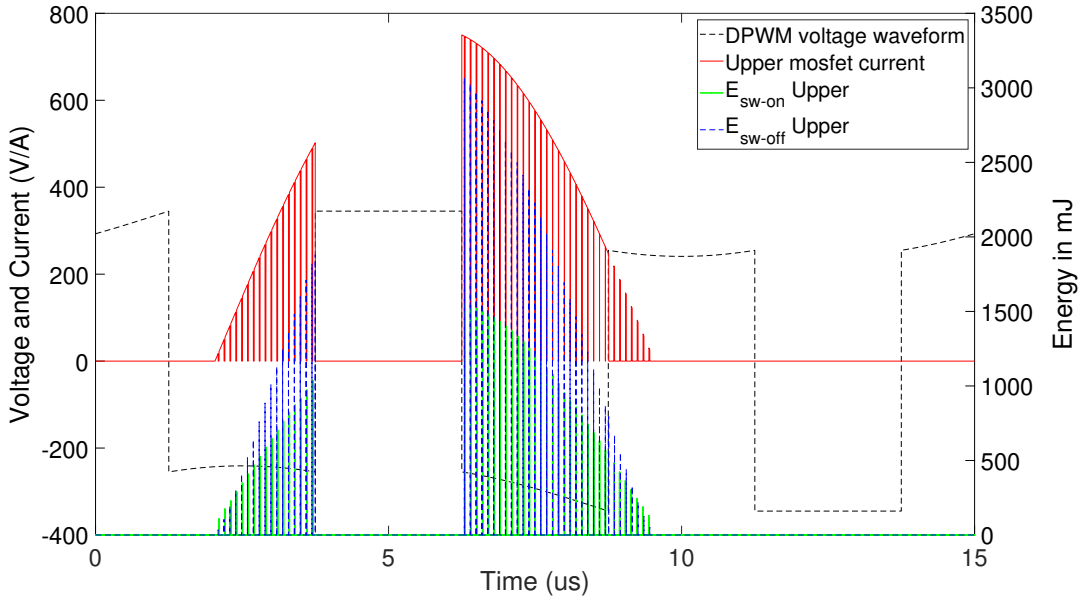


Figure 3.29: Switching instances and energies in the upper phase leg for DPWM1

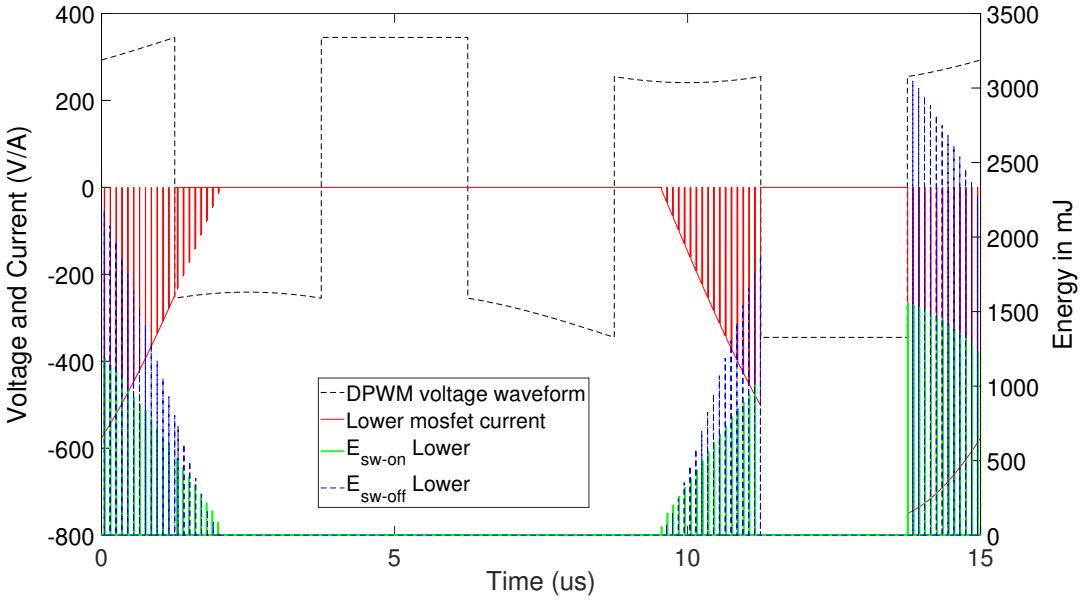


Figure 3.30: Switching instances and energies in the lower phase leg for DPWM1

3.5 FEM parameterised IPMSM plant model

The IPMSM FEM model used is a previously configured and verified model with 2D inductance, current and permanent magnet flux maps. This discrete steady-state model uses an FOC algorithm using MTPA, with feedback from current sensors and a resolver, to control the FEM-parameterised PMSM block with a dynamometer load. A custom modulator is developed using a scalar carrier approach to generate voltage waveforms for SVPWM, DPWM or NSPWM techniques, that then feed gate signals into a 3-phase inverter model. The inverter model outputs 3 3-phase current time series with harmonic content for each Torque-speed (T-ω) point. These T-ω points are extracted from the 2D current maps, with a specified resolution across the torque speed range. This gives us a T-ω grid with 333 points. The steps seen in subsequent loss and THD plots are a limitation of the T-ω grid resolution. Attempts to extrapolate to the max torque line introduce artefacts and islands and present disingenuous data. This grid is then used to interpolate for the current, inductance and magnetic flux. The current magnitude grid i_s is visualised in Fig.3.31 and the phase angle in Fig.3.21.

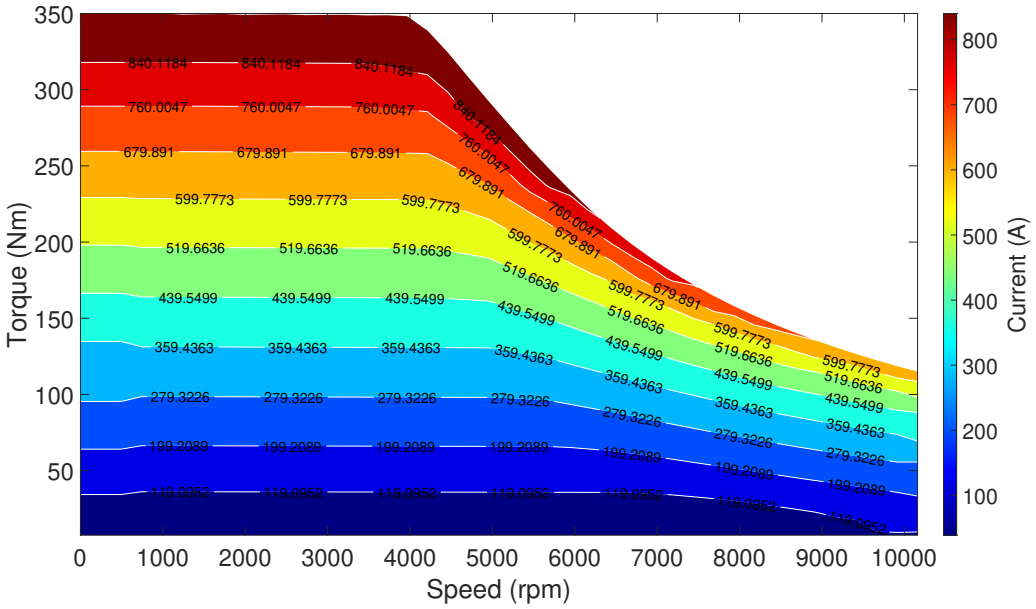


Figure 3.31: Current magnitude map

Having extracted the phase currents, a custom script is deployed to post-process the currents for the current injection. Since JMAG requires at least a period of current injection, in addition to some minimum data points, the current waveform needs to be cut down. In addition, care needs to be taken to ensure that the current waveforms are,

- Taken when the system is at steady state, where u_d, u_q are within the voltage limit of the system, and have converged to the desired i_d, i_q.
- Cut down to the minimum desired duration and data points as seen in Fig.3.33, with reference to the reference phase voltage as per JMAG.
- That the current is displaced by the appropriate angle as seen in Fig.3.34, with reference to the reference phase voltage as per JMAG.
- Meeting the required torque and i_d, i_q when analytically verified from the three phase current.
- Use FFT to establish some linearity between the current map, load and speed across the operating points and later the AC losses.

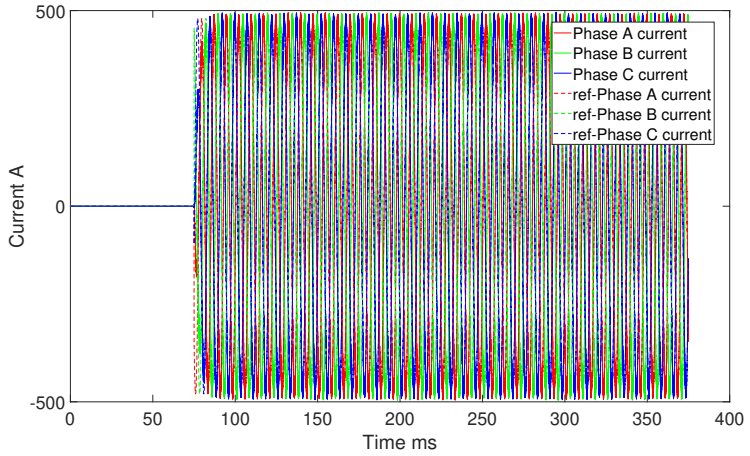


Figure 3.32: Phase currents generated from the model

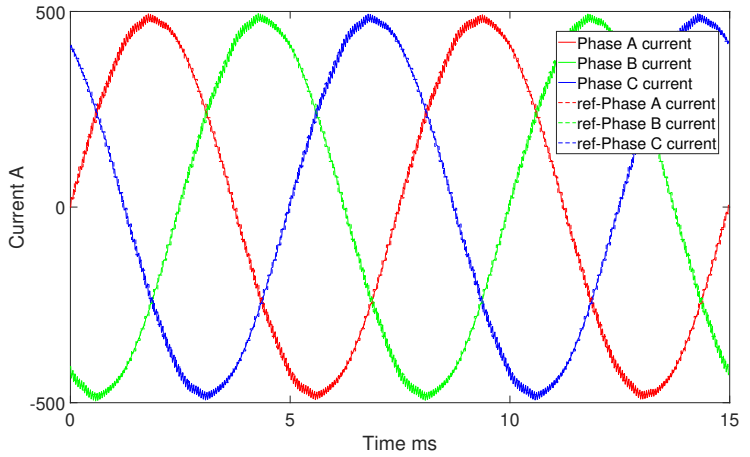


Figure 3.33: Current Harmonics of Phase A for 2 periods

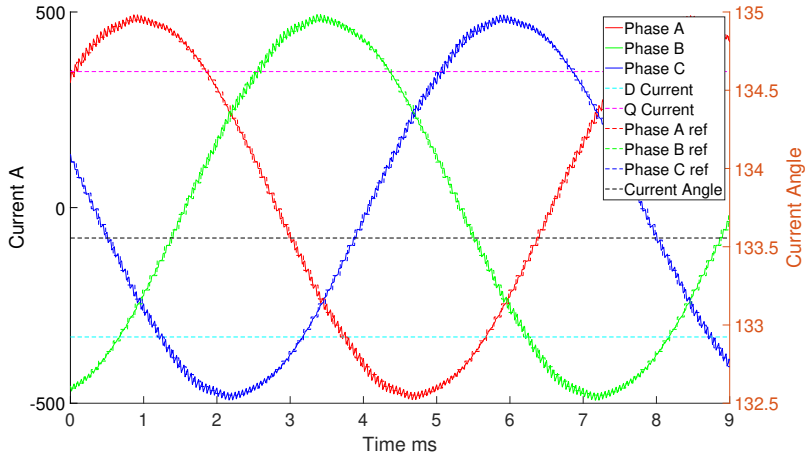


Figure 3.34: Current Harmonics with angle offset and desired length

3.6 IPMSM FEA in JMAG

As previously discussed, we use current injections with harmonics that are fed into a FEM model using JMAG. As this simulation model is for steady-state operating points, and as the torque is predominantly based on the fundamental current amplitude and current angle, we will retain the same required torque output. Now, by feeding fixed periods of the phase current data obtained from MATLAB to JMAG, we extract torque vs speed with loss maps for each modulation and control technique used. This torque output, the current map and linearity in DC and AC loss trends are checked for linearity, and if available, cross-verified with pre-existing FEM results. Having captured joule losses, iron losses and magnetic losses, a post-processing tool is used to further refine and visualise this data.

Table.3.3 contains a brief list of specifications of the IPMSM utilised during this thesis work.

Table 3.3: IPMSM Specifications & Parameter List

Parameter	Symbol	Value
Topology		Single V IPMSM
Winding Arrangement		Delta concentrated hairpin
Pole pairs	n	4
Rated operational temperature	T_{rot}	60°C
Peak Torque	T_{peak}	350 Nm
Operational DC-link voltage	U_{dc}	605 V
Peak rated current magnitude	I_{rms}	1000 A
Maximum speed	N_{peak}	10,000 RPM
Base rated speed	N_{rated}	4000 RPM

3.7 Generating performance and loss maps

Having now generated the inverter and machine loss data for the 333 points, they are post-processed using MATLAB scripts into total loss grids that help in visualising system level losses against performance to define system efficiency across the drive line's operational range for different modulation and control strategies. By analyzing these datasets using delta maps, ideal modulation methods combined with different switching frequencies are identified across the operating map. The resulting maps, analysis and conclusions are shared in the subsequent section.

4

Results and Analysis

4.1 Active clamping optimisation and mapping

As previously discussed in section 3.2, the most optimised inverter loss map is achieved by implementing the hybrid modulation map as seen in Fig.4.1. The resultant modulation technique is termed DPWM Hybrid. This is used as a custom modulation technique in all subsequent simulations and results, combined and referred to as an optimised hybrid DPWM or DPWM Hybrid as obtained from the active clamping script.

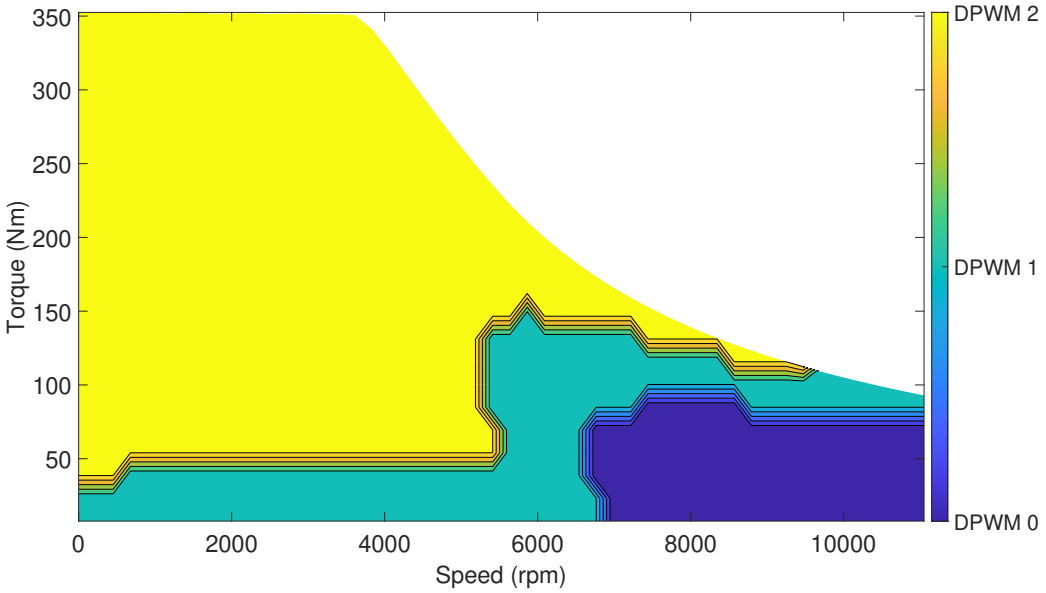


Figure 4.1: Hybrid Modulation Map

4.2 Analysis of Current Injections

Following the case setup and post-processing of the current injection waveforms detailed in section 3.5, post-validation of model convergence to the correct torque, speed, voltage and current for each operating point, and using appropriately adjusted current waveforms, an FFT of the waveforms is performed to study and compare the fundamental currents and their THD factor with changing speed and torque. The current magnitude is kept consistent across the modulation methods and is previously visualised in Fig.3.31.

4.2.1 Total harmonic distortion factor maps

An analysis is conducted on the THD factor for the different modulation methods as seen in Fig. 4.2 and 4.3 for SVPWM, 4.4 and 4.5 for DPWM Hybrid and 4.6 for NSPWM. A log scale is used to make it easier to visualise the THD factor, represented as a percentage. Across the modulation methods, a near-zero THD factor below base speed, with higher factors thereafter arising as the inverter attempts to supply maximum voltage at power factors less than 1. Conversely, with increasing loads and current magnitude, reducing harmonic factors are observed as the duty cycle increases and flux saturates.

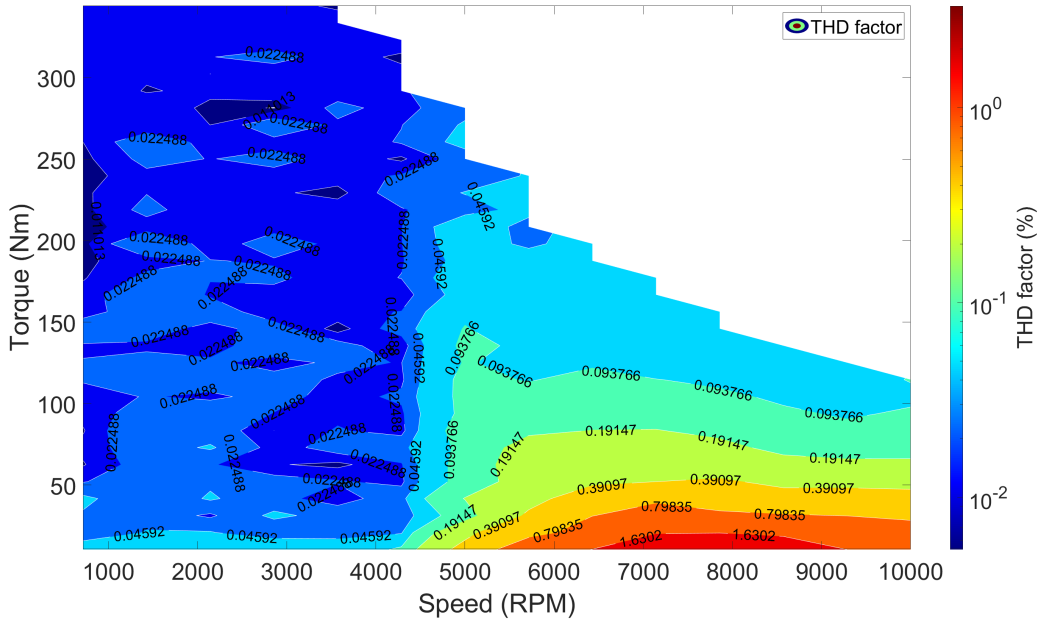


Figure 4.2: THD factor map of SVPWM 10kHz

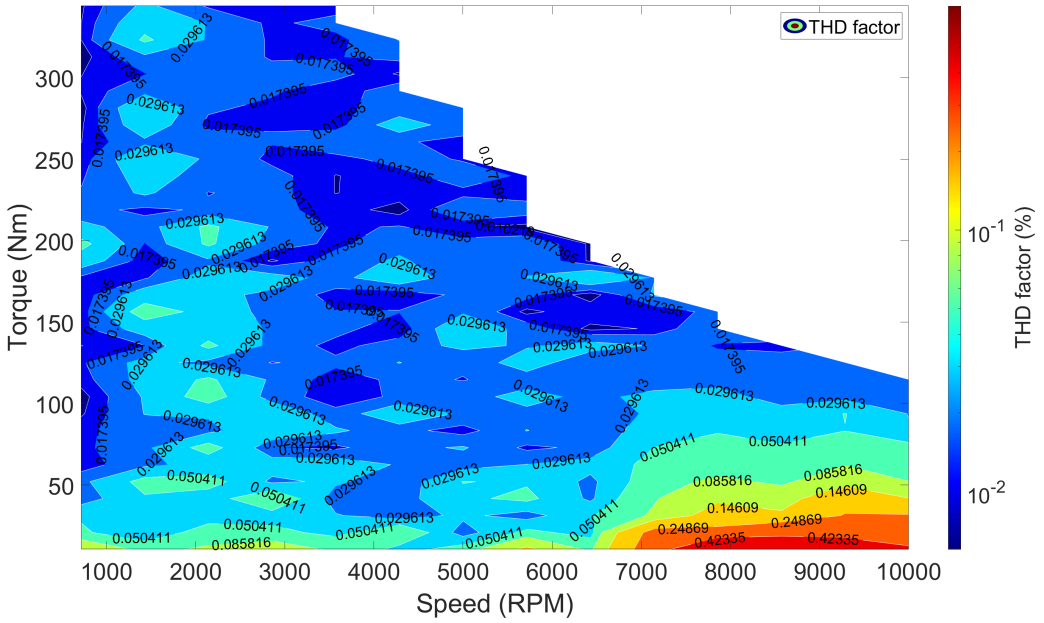


Figure 4.3: THD factor map of SVPWM 15kHz

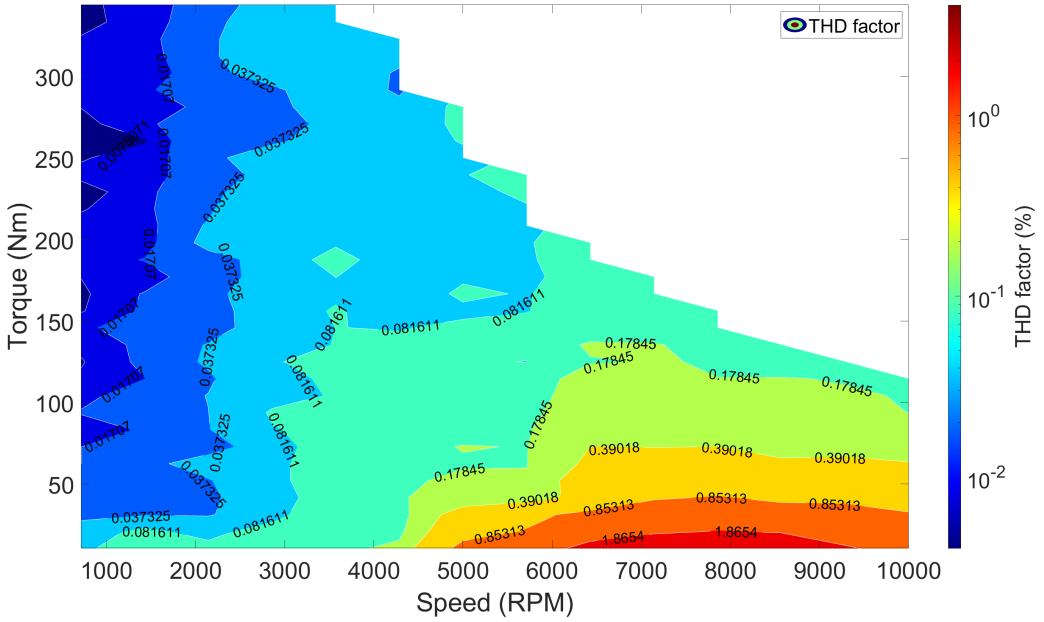


Figure 4.4: THD factor map of DPWM Hybrid 10kHz

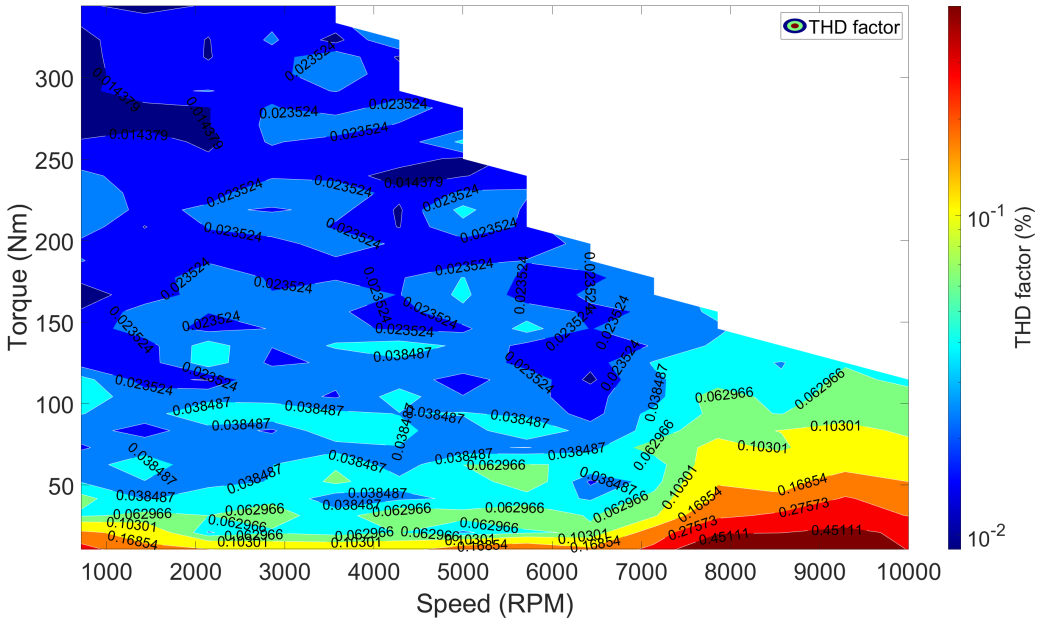


Figure 4.5: THD factor map of DPWM Hybrid 15kHz

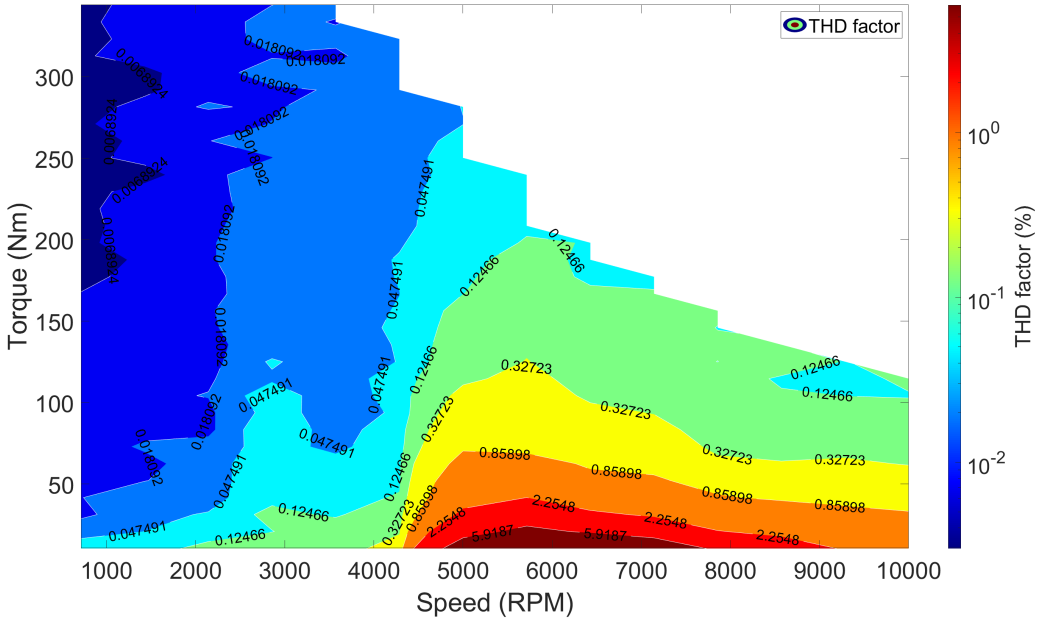


Figure 4.6: THD factor map of NSPWM 10kHz

Comparing techniques across switching frequencies, as expected, higher switching frequencies offer considerable reductions in THD factor as seen in Fig.4.7 and 4.8, especially at peaks, a result of the lower current ripple amplitude.

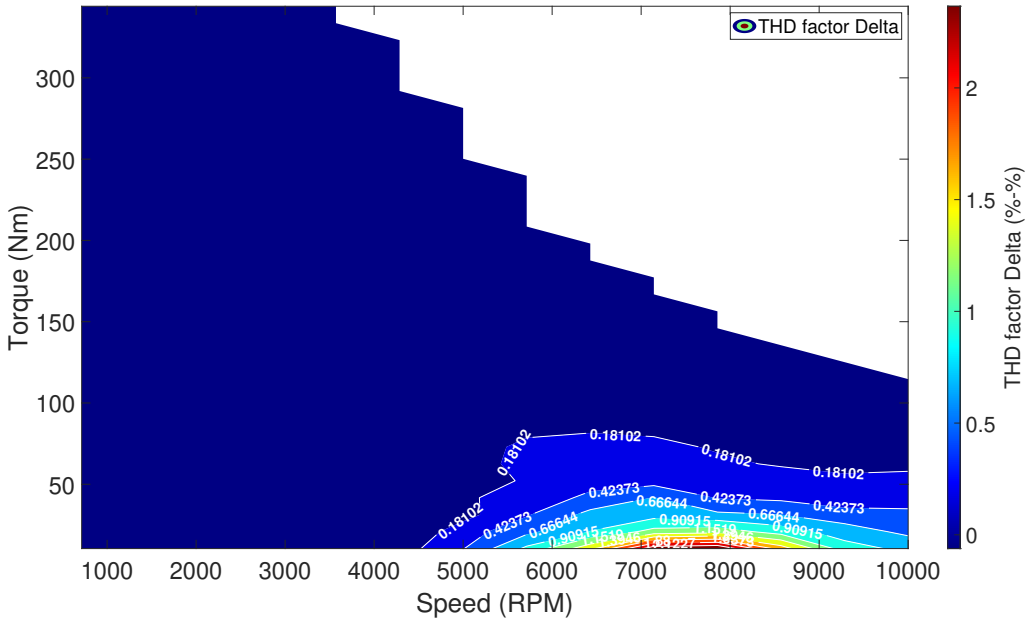


Figure 4.7: THD factor delta between SVPWM 10kHz and SVPWM 15kHz

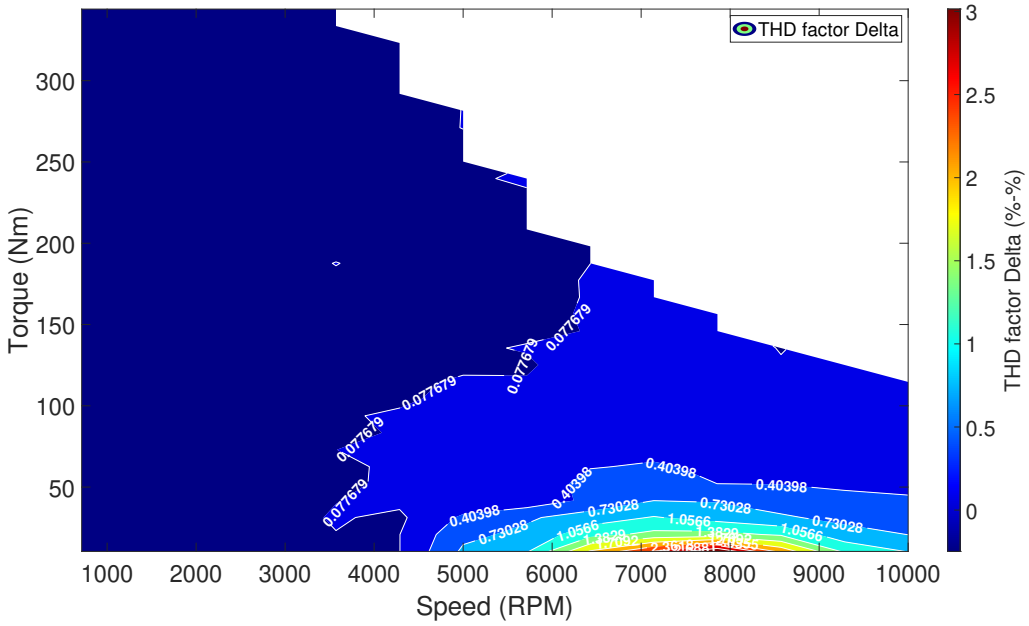


Figure 4.8: THD factor delta between DPWM Hybrid 10kHz and DPWM Hybrid 15kHz

Comparing different modulation methods using the delta maps, it is observed that SVPWM 10kHz outperforms DPWM Hybrid 10kHz by a noticeable margin as seen in Fig.4.9. On the other hand, DPWM Hybrid 15kHz is comparable, if not at times better than SVPWM 15kHz as seen in Fig.4.10.

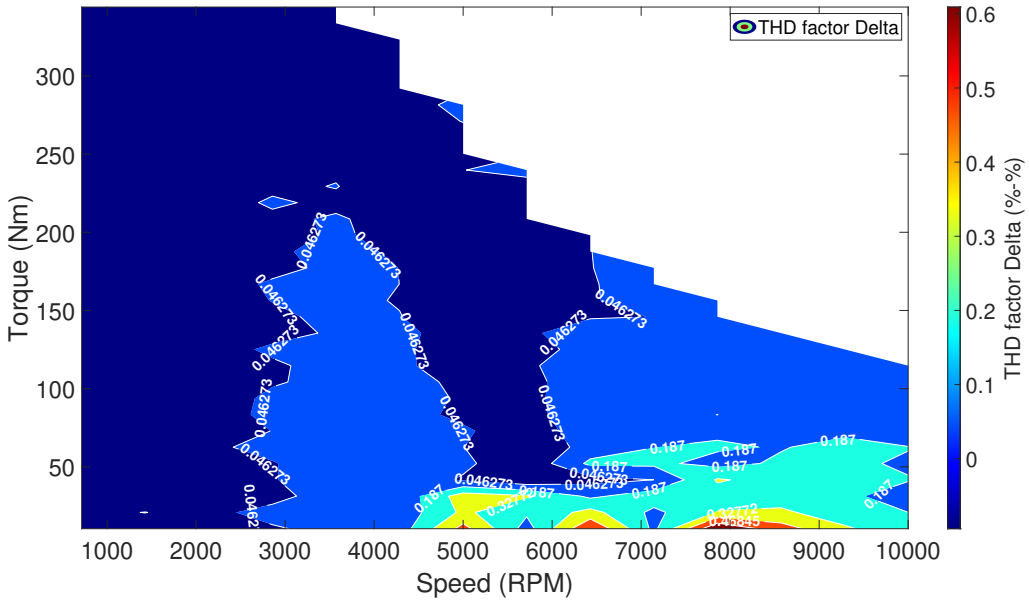


Figure 4.9: THD factor Delta between DPWM Hybrid 10kHz and SVPWM 10kHz

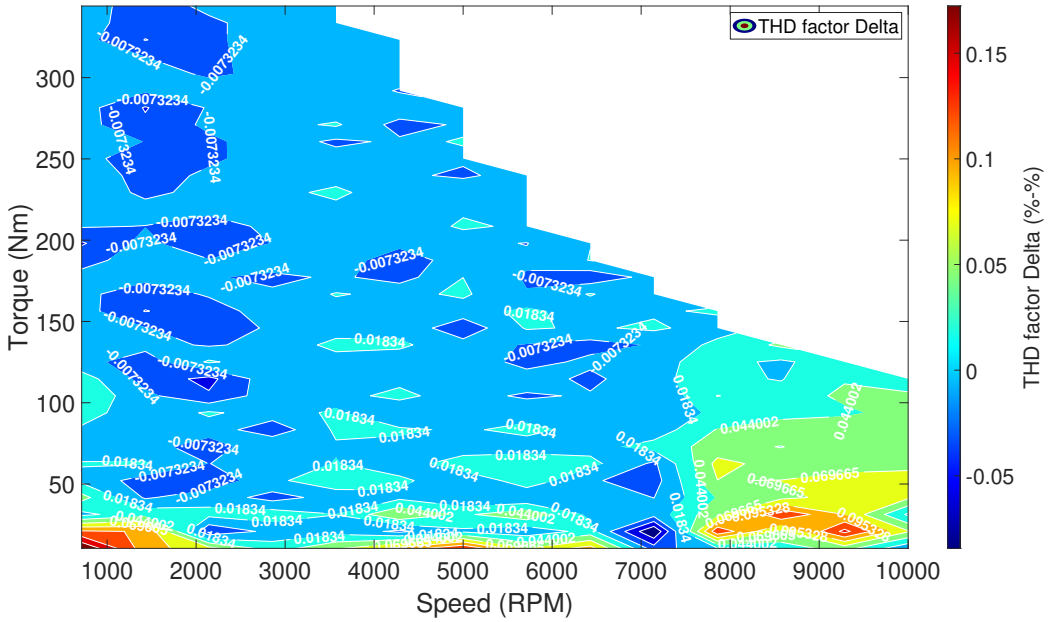


Figure 4.10: THD factor Delta between SVPWM 15kHz and DPWM Hybrid 15kHz

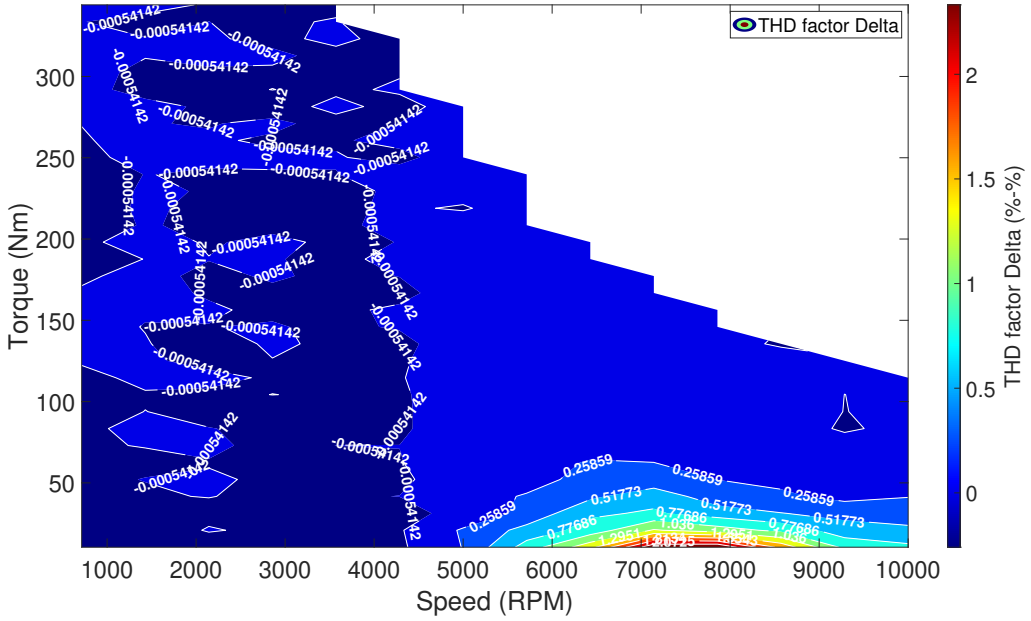


Figure 4.11: THD factor Delta between SVPWM 10kHz and DPWM Hybrid 15kHz

Comparing across frequencies and modulation methods, in Fig. 4.11, we see DPWM Hybrid 15kHz performing within margin to SVPWM 10kHz within base speed. Beyond base speed, DPWM Hybrid 15kHz offers a lower THD factor.

DPWM Hybrid 15kHz also performs better than NSPWM 10kHz, especially at medium speeds and low loads as seen in Fig.4.12.

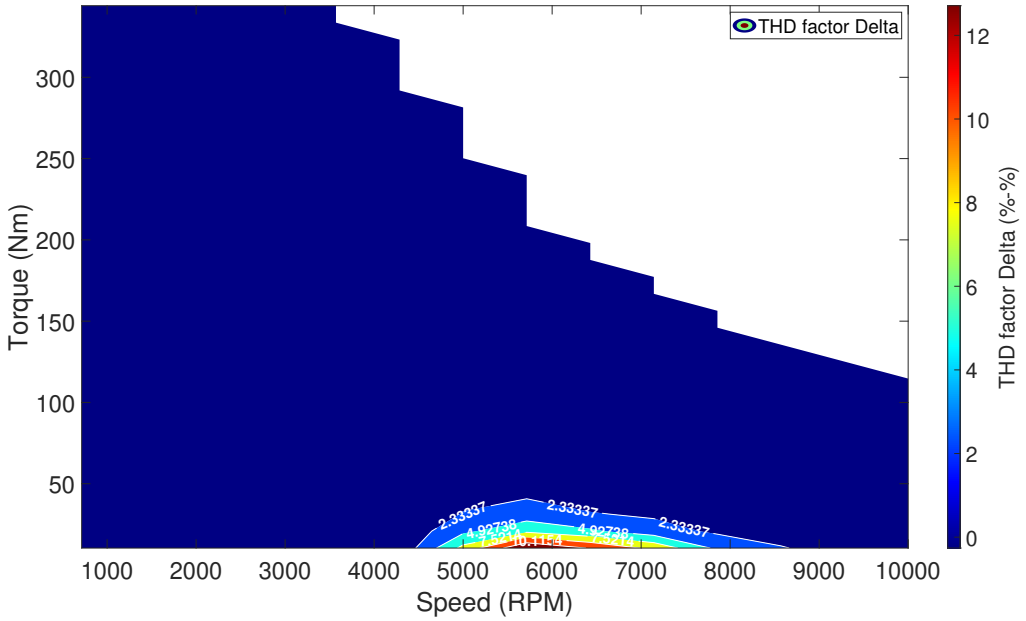


Figure 4.12: THD factor Delta between NSPWM 10kHz and DPWM Hybrid 15kHz

From this analysis, the initial conclusion is that DPWM Hybrid 15kHz does show promise, outperforming and equaling SVPWM 10kHz and SVPWM 15kHz THD factor performance respectively. The THD factor maps and their analysis are essential and are used as references when analysing the EM losses in the subsequent sections.

4.3 Inverter loss maps

The inverter loss maps are a sum of conduction and switching losses. For similar operating points, conduction losses are not affected by modulation technique and switching frequency and are thus identical. Switching losses on the other hand vary with switching frequency and modulation methods.

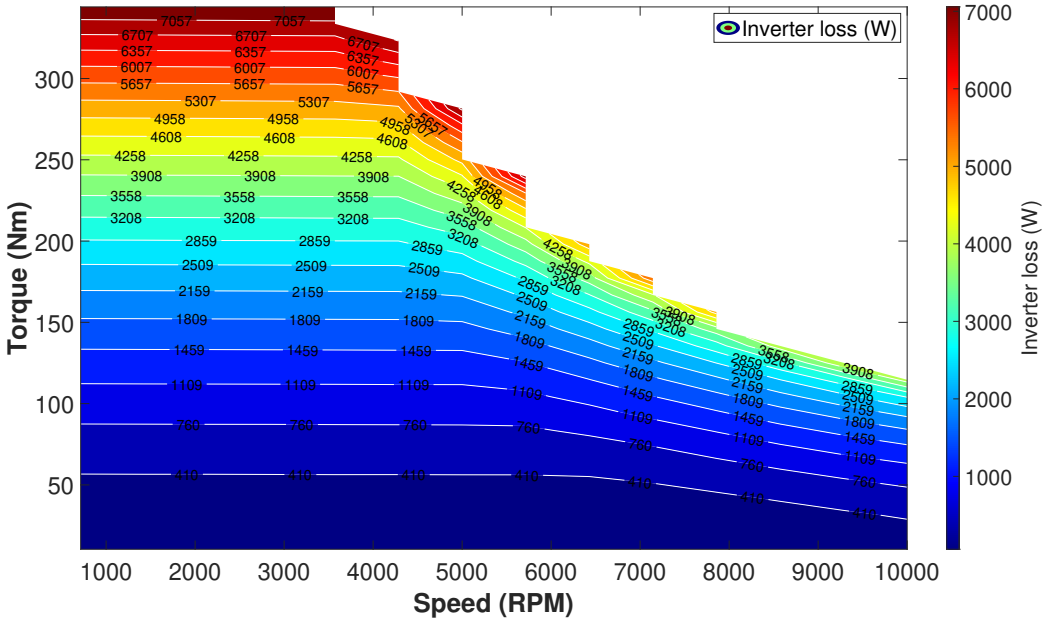


Figure 4.13: SVPWM 10 kHz Total Inverter loss

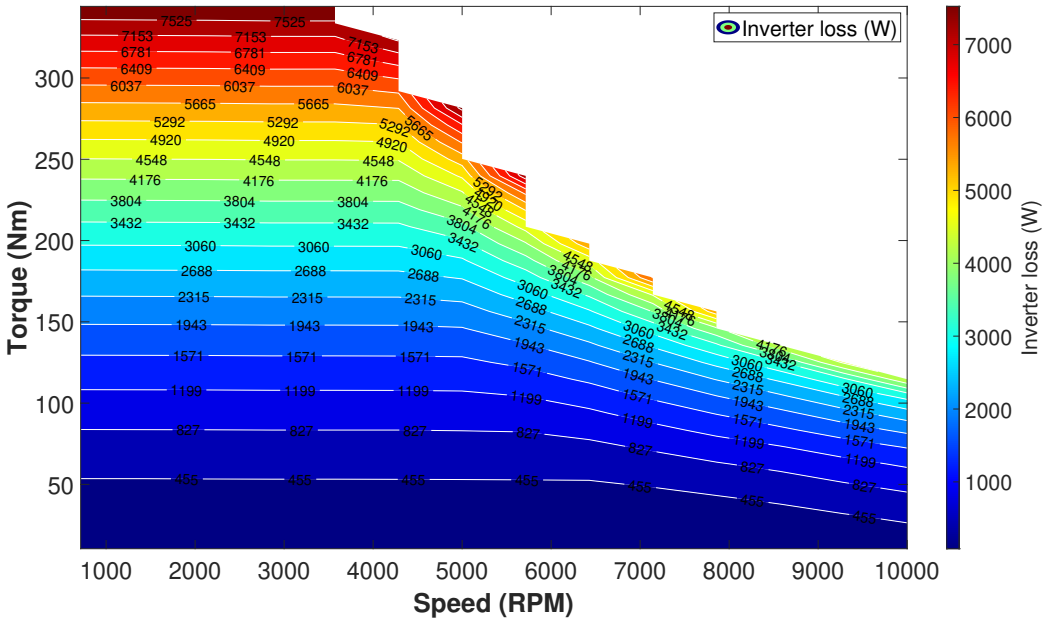


Figure 4.14: SVPWM 15 kHz Total Inverter loss

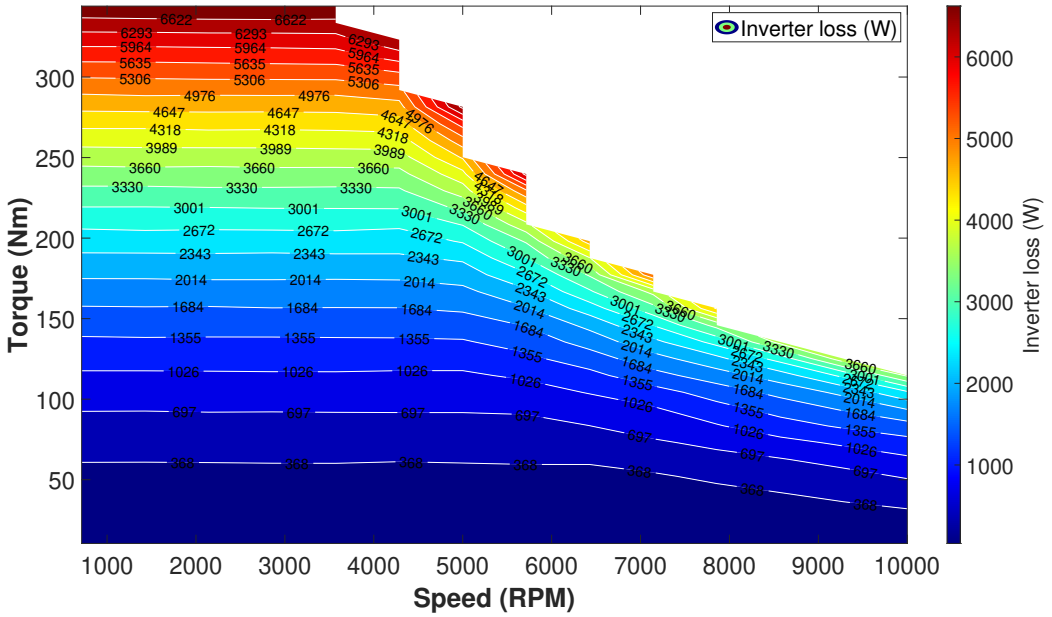


Figure 4.15: DPWM Hybrid 10 kHz Total Inverter loss

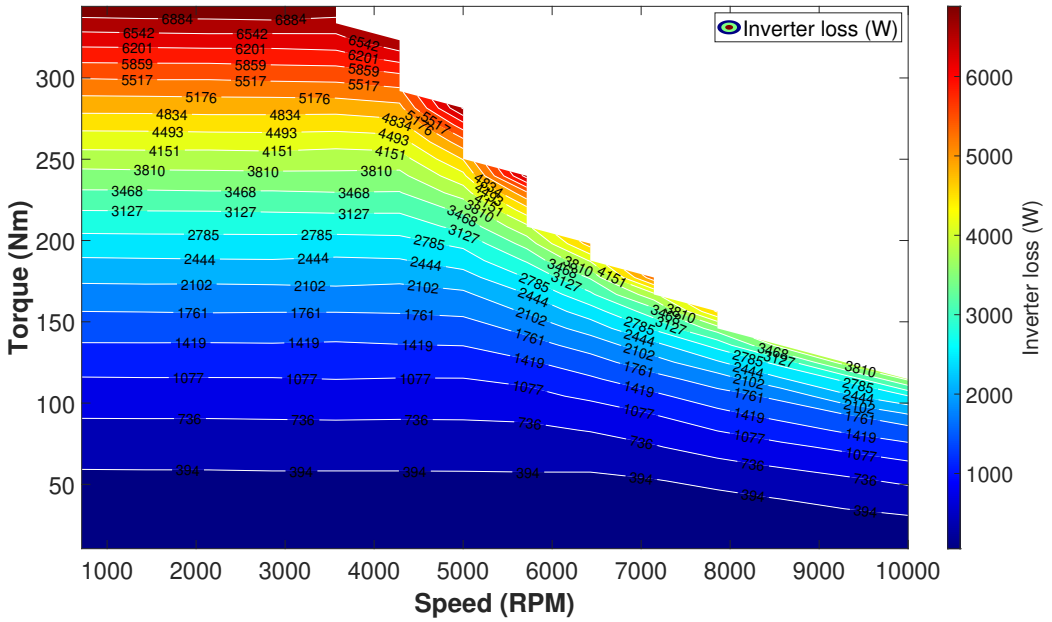


Figure 4.16: DPWM Hybrid 15 kHz Total Inverter loss

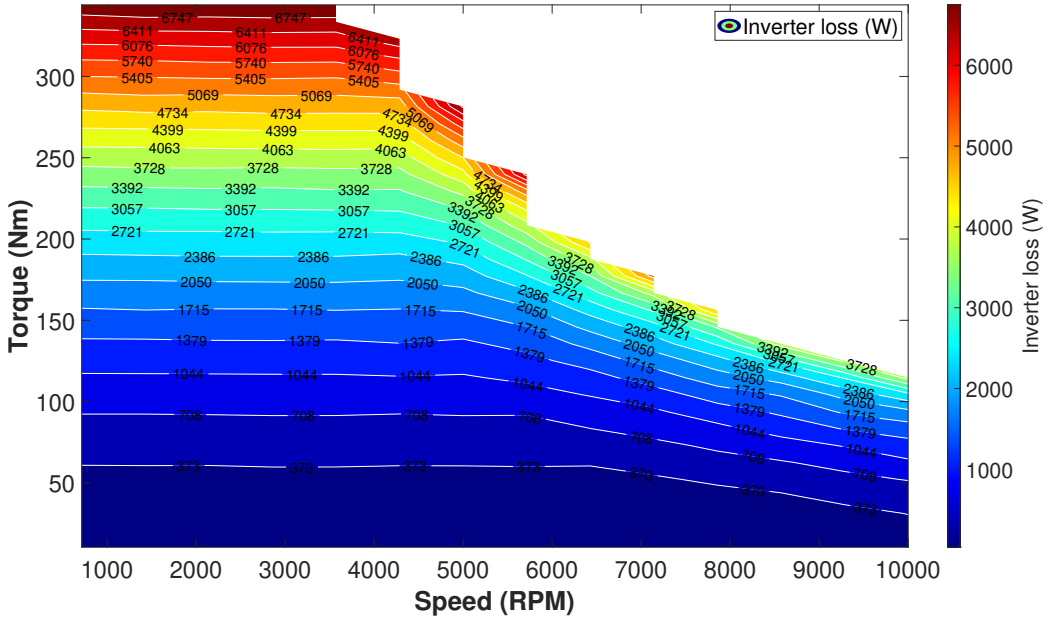


Figure 4.17: NSPWM 10 kHz Total Inverter loss

Comparing modulation methods and frequencies, we analyse the delta inverter loss maps. Negative Delta losses signify the gains of the advantage of the first technique over the second. Current trends with nonuniform distortions are visible, caused due to the variable clamping at work and from the limited torque-speed resolution.

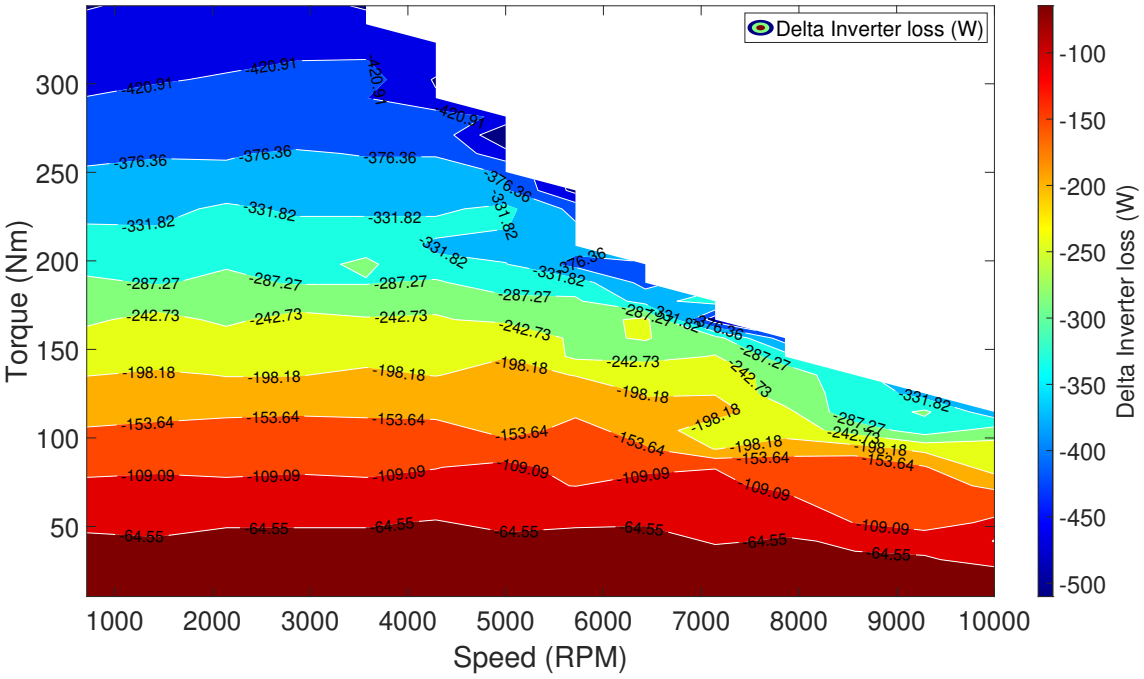


Figure 4.18: Total Inverter delta losses between DPWM 10 kHz and SVPWM 10 kHz

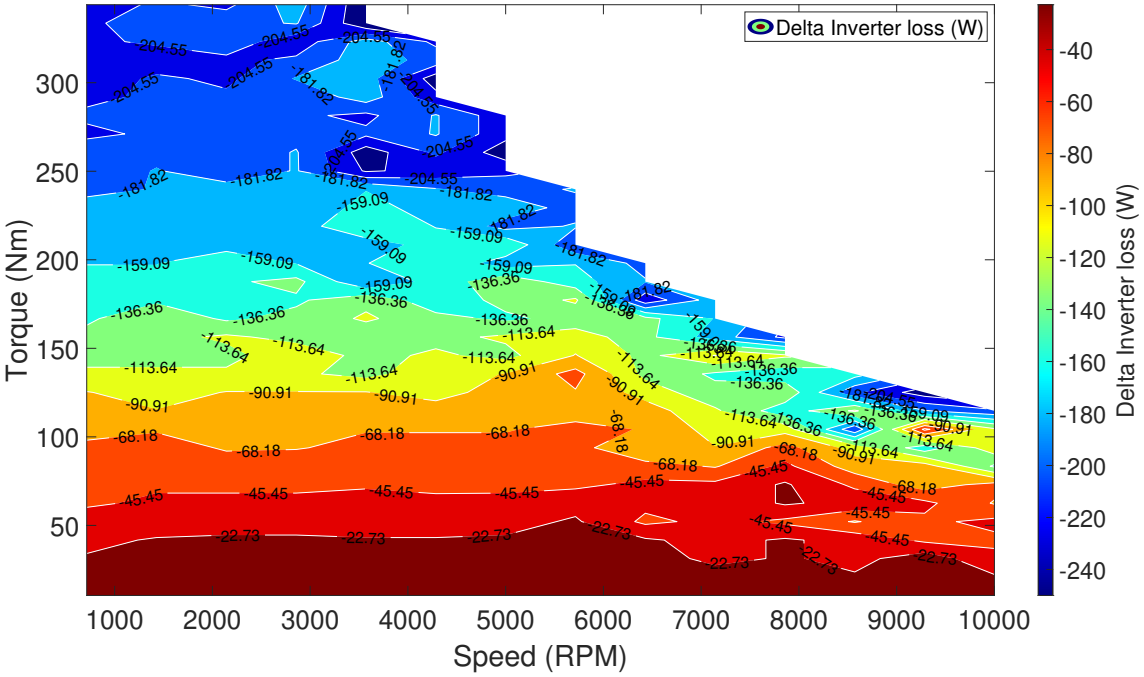


Figure 4.19: Total Inverter delta losses between DPWM 15 kHz and SVPWM 10 kHz

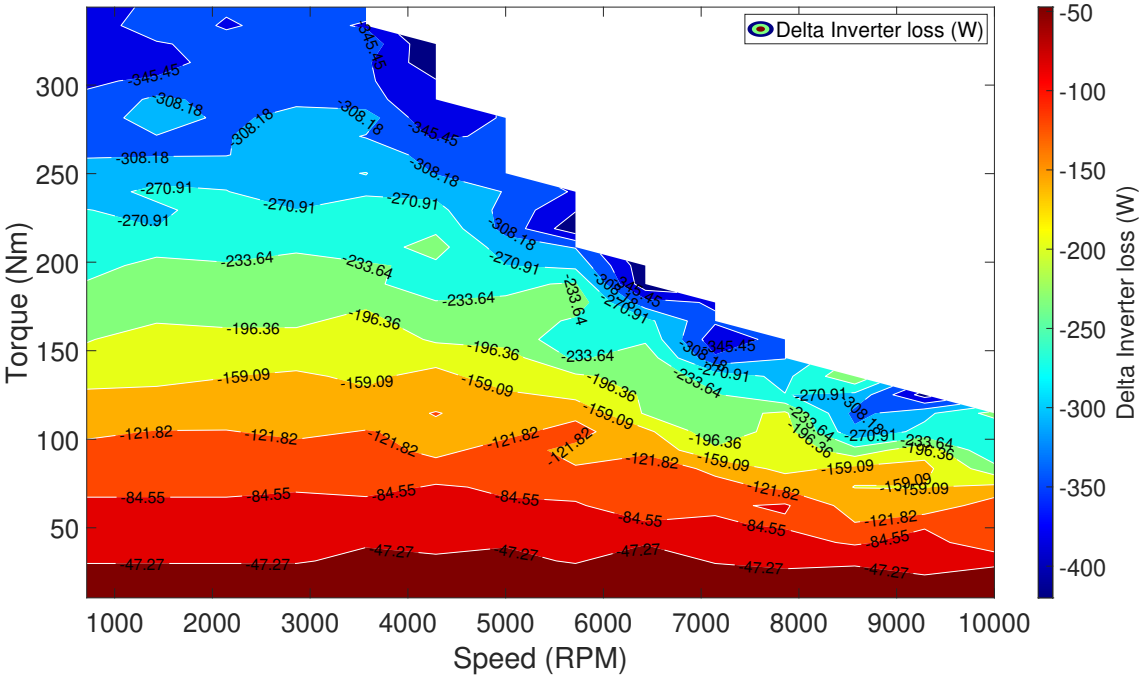


Figure 4.20: Total Inverter delta losses between NSPWM 10 kHz and SVPWM 10 kHz

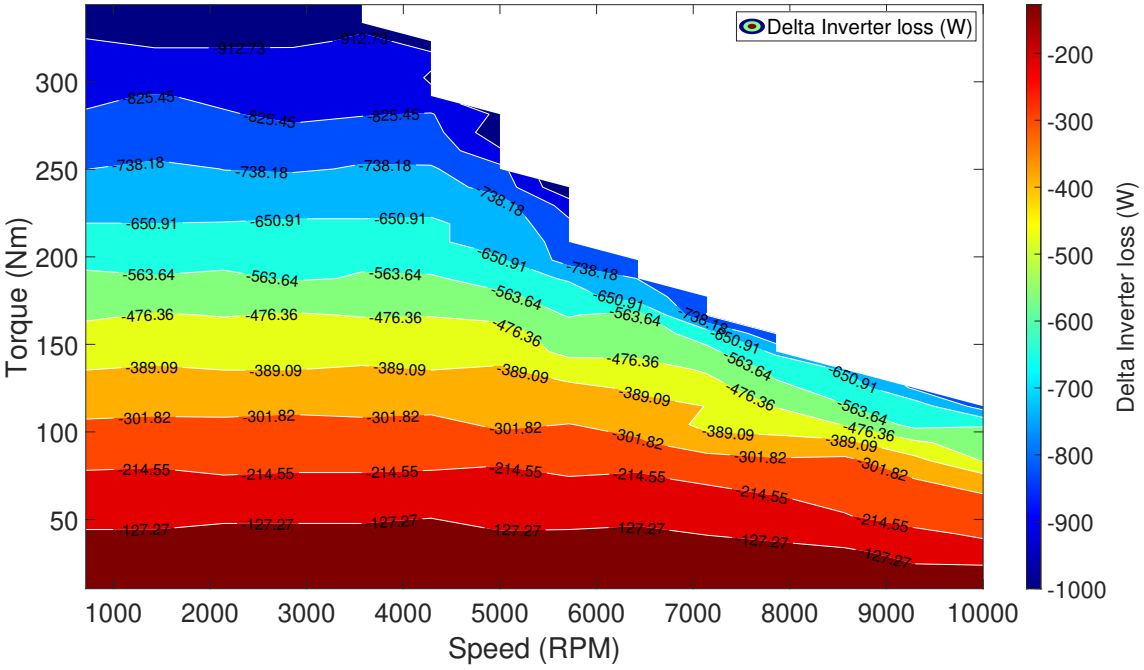


Figure 4.21: Total Inverter delta losses between DPWM 10 kHz and SVPWM 15 kHz

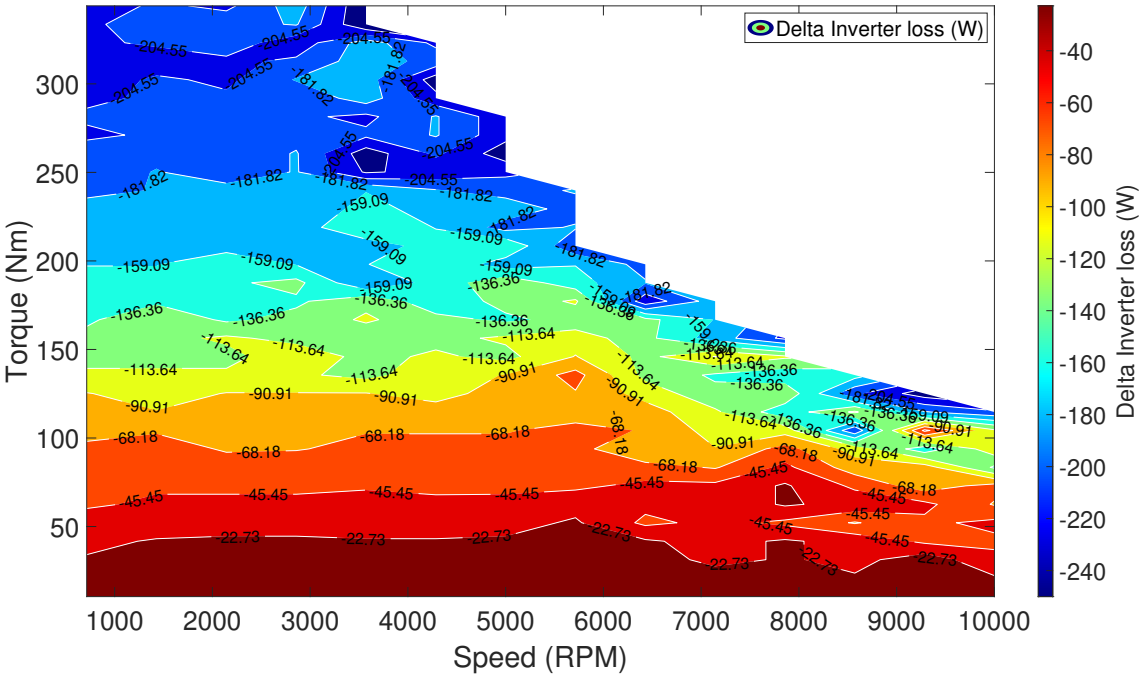


Figure 4.22: Total Inverter delta losses between DPWM 15 kHz and SVPWM 10 kHz

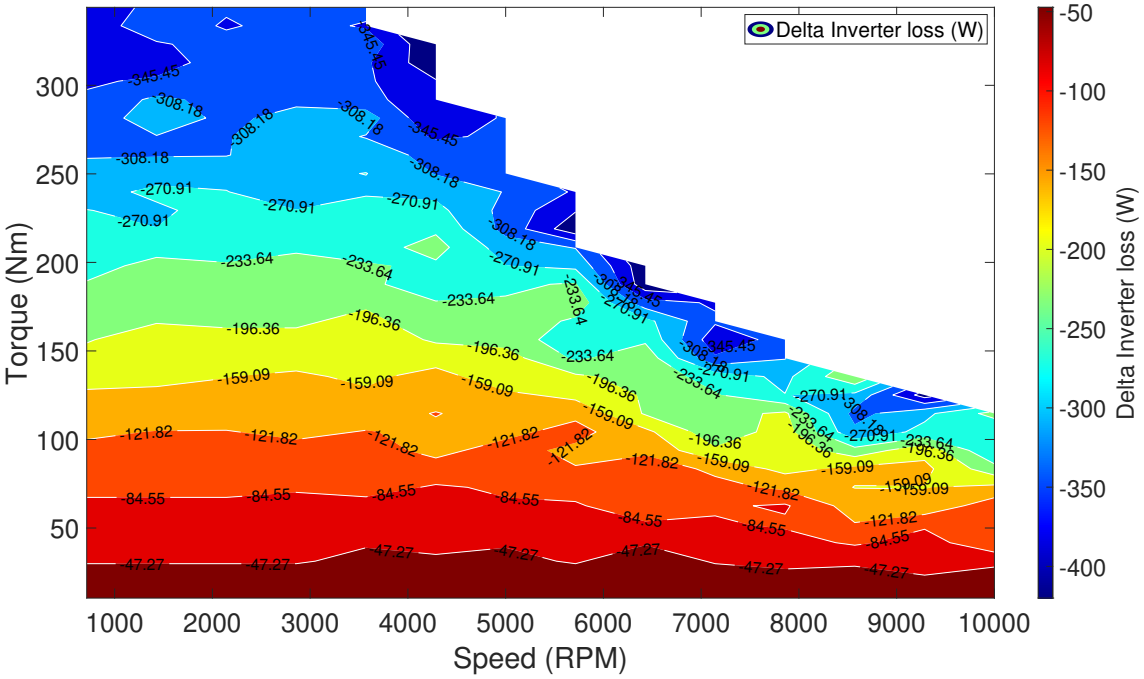


Figure 4.23: Total Inverter delta losses between NSPWM 10 kHz and SVPWM 10 kHz

The delta figures conclude that DPWM Hybrid offers lower switching losses in both 10 and 15 kHz runs compared to other modulation techniques. While DPWM Hybrid 15 kHz has higher total losses compared to DPWM Hybrid 10kHz from the higher switching frequency, it is still a viable choice and worth investigating due to its smoother current ripple and lower THD factor, which can reduce machine losses. From a switching loss perspective, DPWM techniques are the most efficient with DPWM 10 kHz yielding the least total inverter losses.

4.4 IPMSM loss maps from JMAG

The loss maps presented in this section are the sum of all Electrical Machine (EM) losses, that constitute rotor iron, stator iron, magnet losses and joule losses for all modulation techniques at 10kHz and 15 kHz switching frequencies. However, due to the material's characteristics, the AC loss component is much smaller than the Joule component. This results in a smaller difference between modulation methods and switching frequencies. Here, similar patterns are seen as that of the THD factor maps, where SVPWM performs better than both DPWM Hybrid and NSPWM modulation methods at similar switching speeds. Similarly, higher switching frequency, associated with a lower THD factor yields lower machine losses.

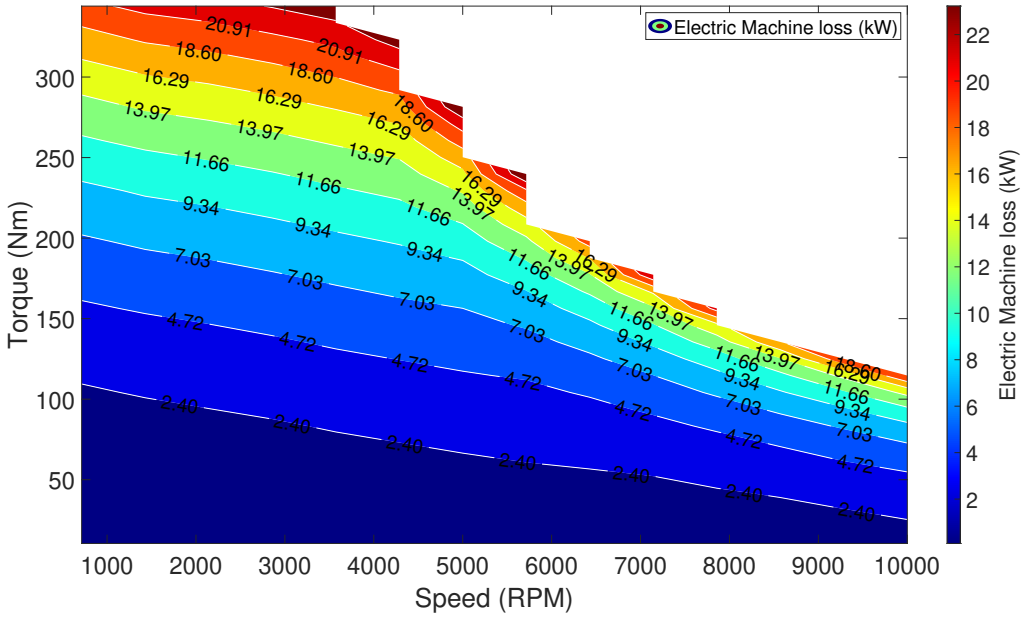


Figure 4.24: SVPWM 10 kHz Total EM loss

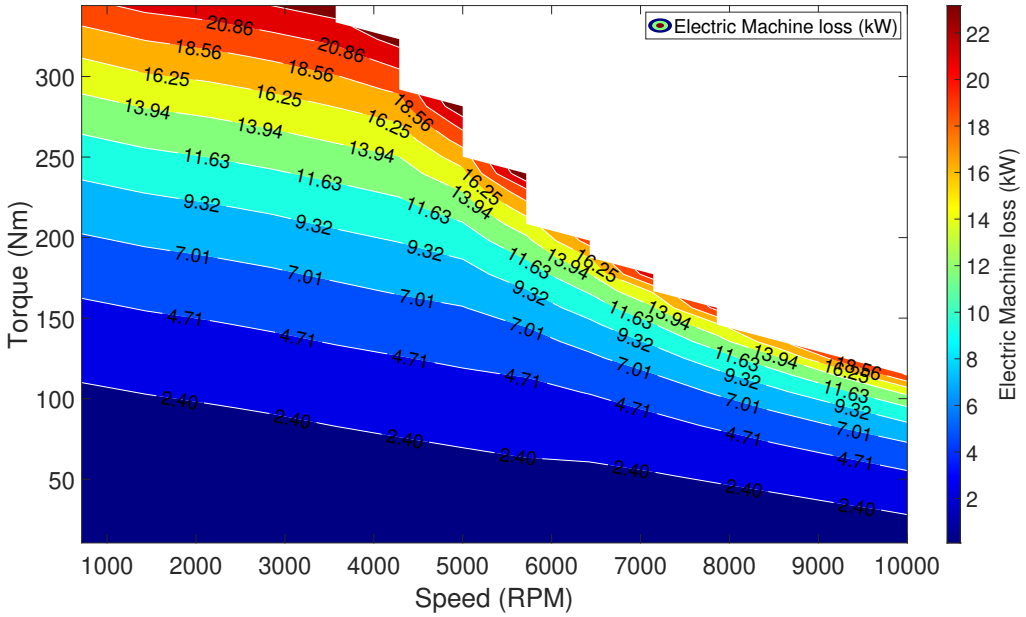


Figure 4.25: SVPWM 15 kHz Total EM loss

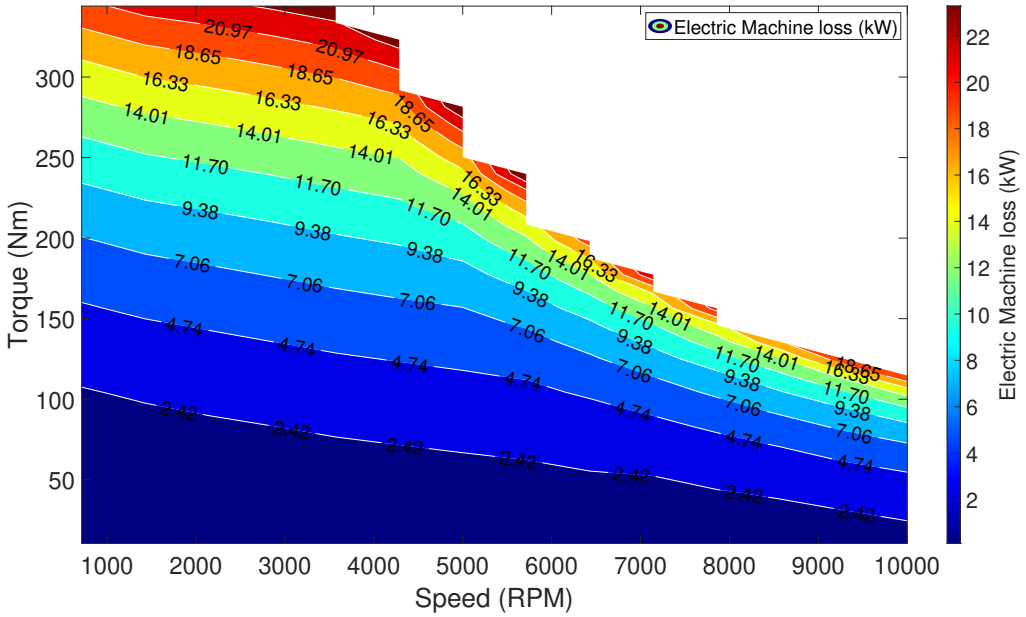


Figure 4.26: DPWM 10 kHz Total EM loss

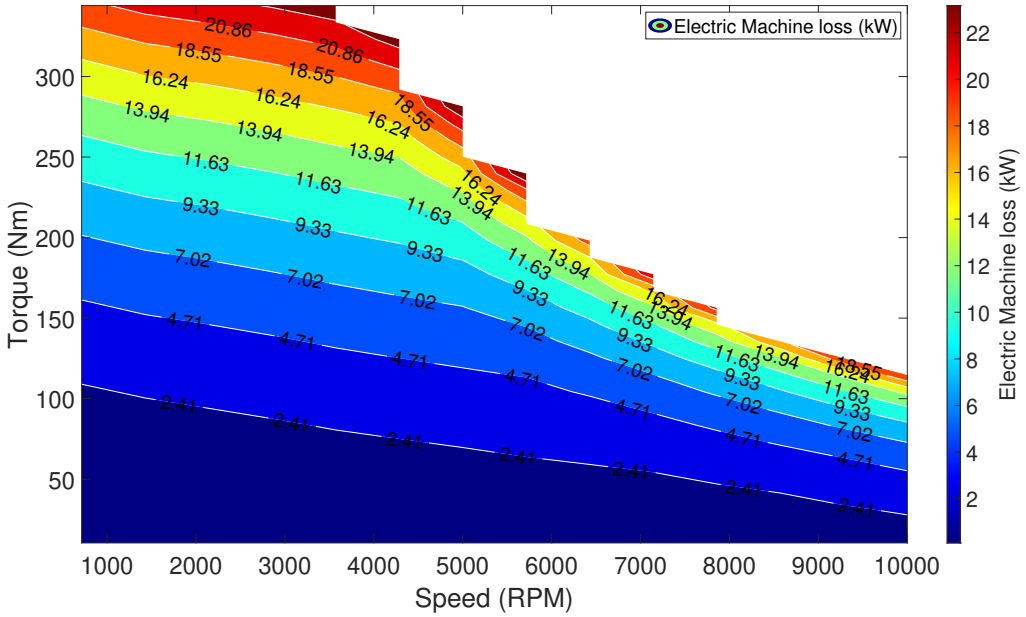


Figure 4.27: DPWM 15 kHz Total EM loss

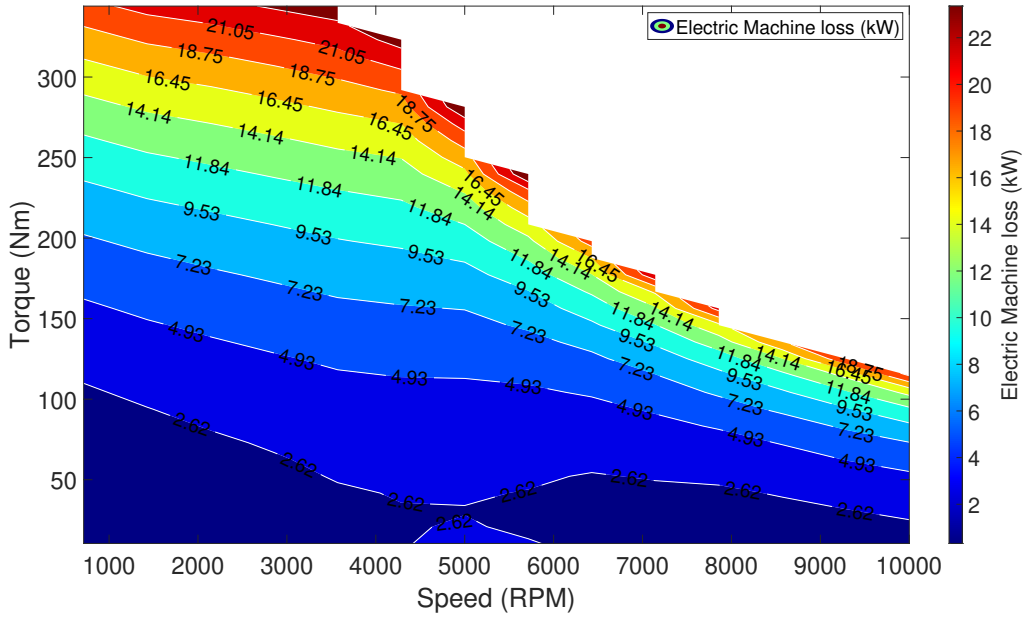


Figure 4.28: NSPWM 10 kHz Total EM loss

Taking a closer look between modulation methods at similar switching frequencies, from Fig.4.29, it is observed that while SVPWM in general does better, it is more pronounced at 10kHz and within base speed and at higher loads.

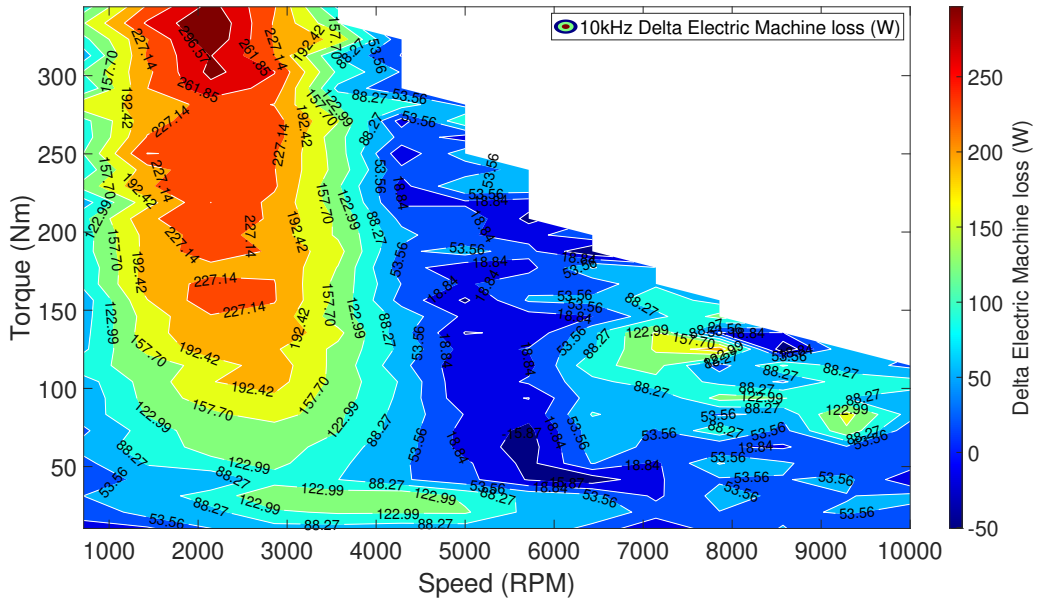


Figure 4.29: Total EM delta losses between DPWM 10 kHz and SVPWM 10kHz

In Fig.4.30, mixed trends are observed using 15 kHz. SVPWM still performs better below the base speed, albeit with a lower advantage. On the other hand, beyond base speed, DPWM hybrid remains either comparable or within margin, doing especially well at high speeds and loads. Comparing the losses between DPWM hybrid 15kHz and SVPWM 10kHz in 4.31, DPWM hybrid 15kHz in general has lower EM losses, with a majority of the map in its favour.

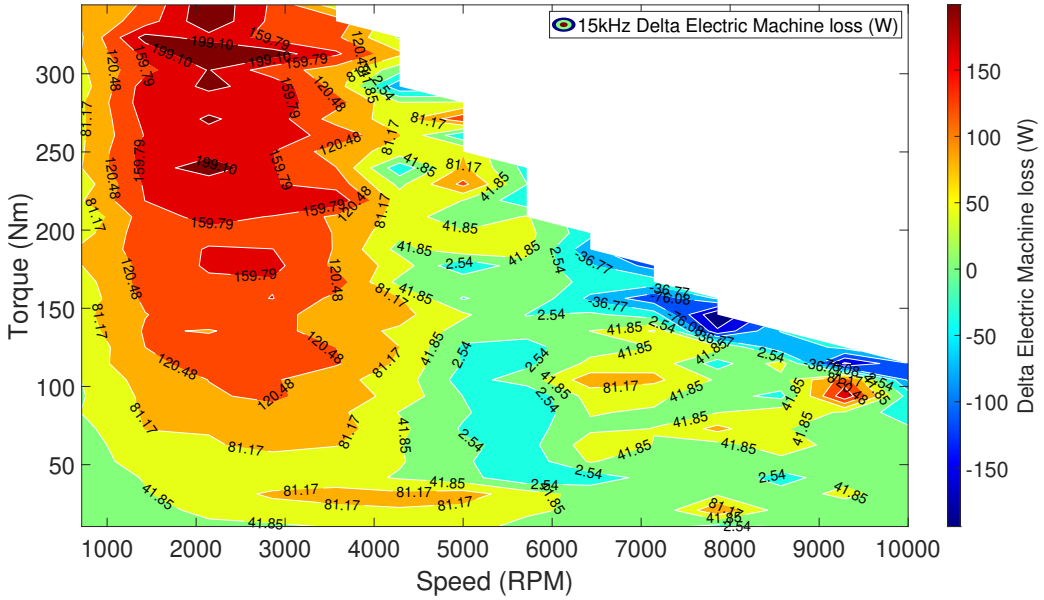


Figure 4.30: Total EM delta losses between DPWM 15 kHz and SVPWM 15kHz

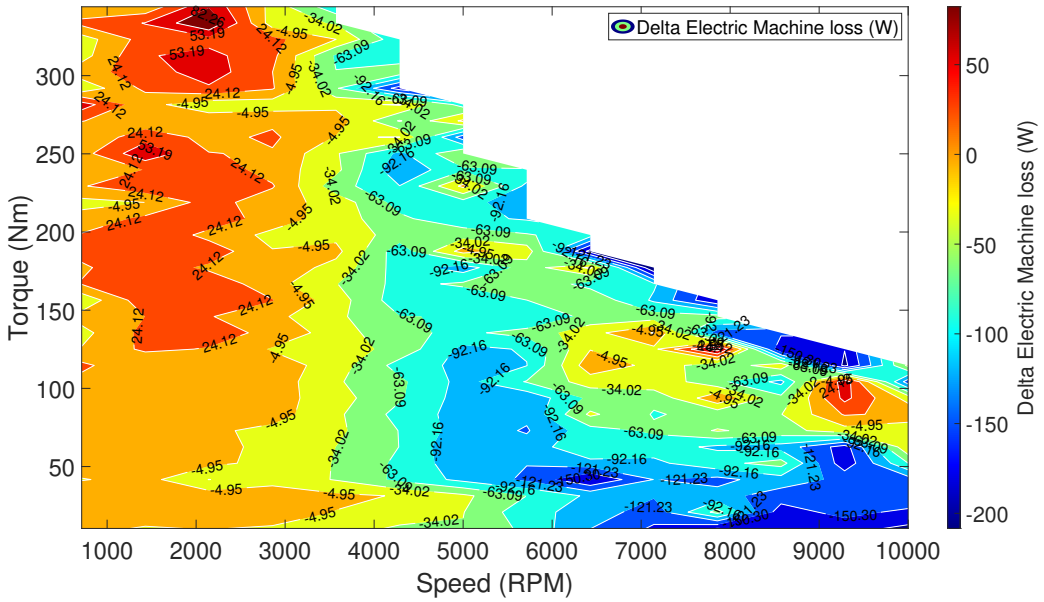


Figure 4.31: Total EM delta losses between DPWM 15 kHz and SVPWM 10kHz

4.5 Composite system loss maps

Combining the inverter and machine losses, composite system loss maps are generated. Dominating current trends throughout the maps are observed, as a result of the considerably higher contribution of EM losses for this particular EM and inverter pair.

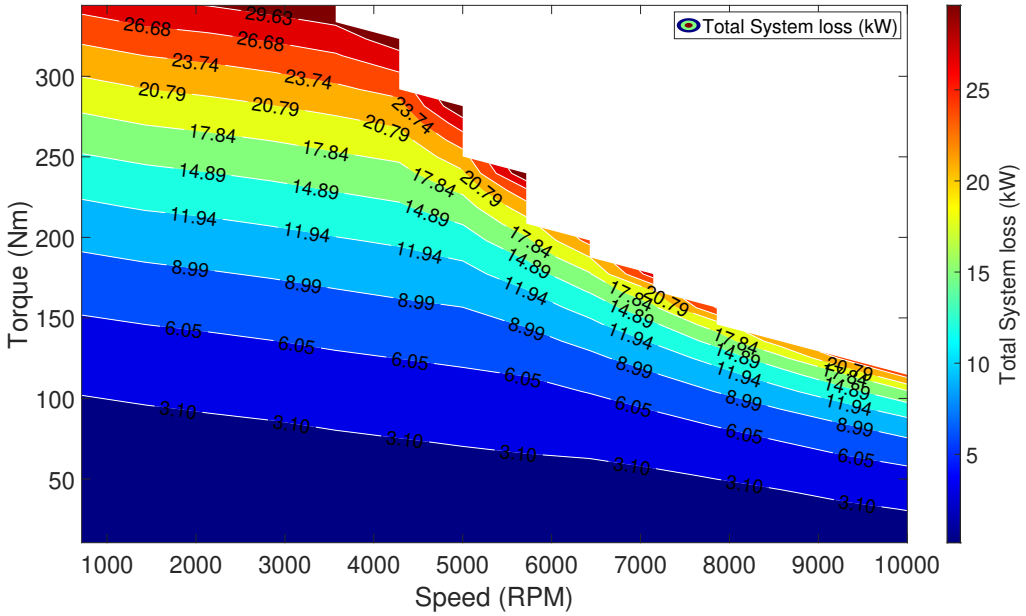


Figure 4.32: SVPWM 10 kHz Total system loss

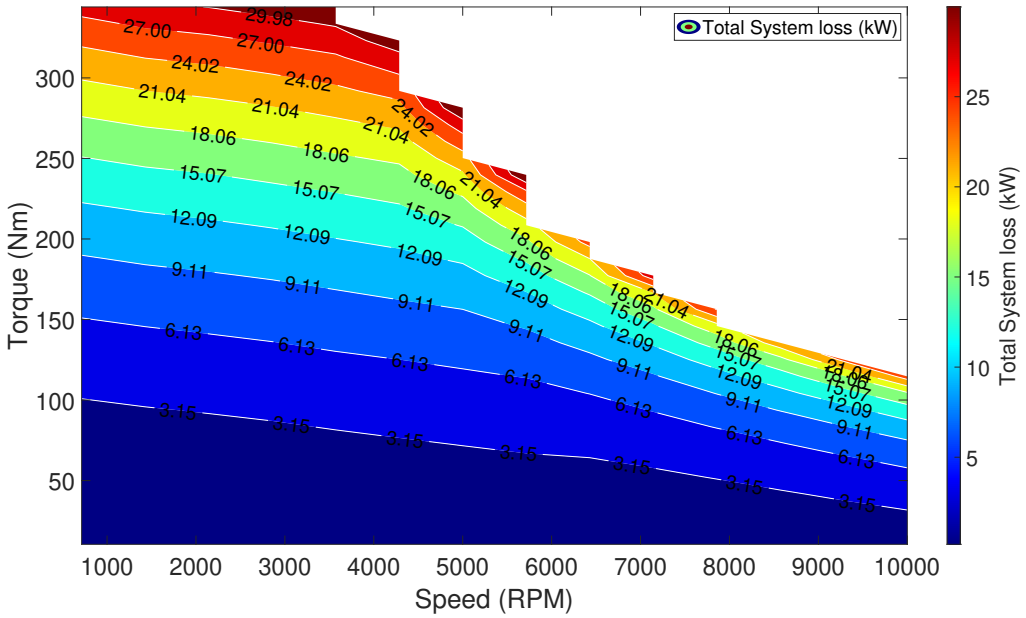


Figure 4.33: SVPWM 15 kHz Total system loss

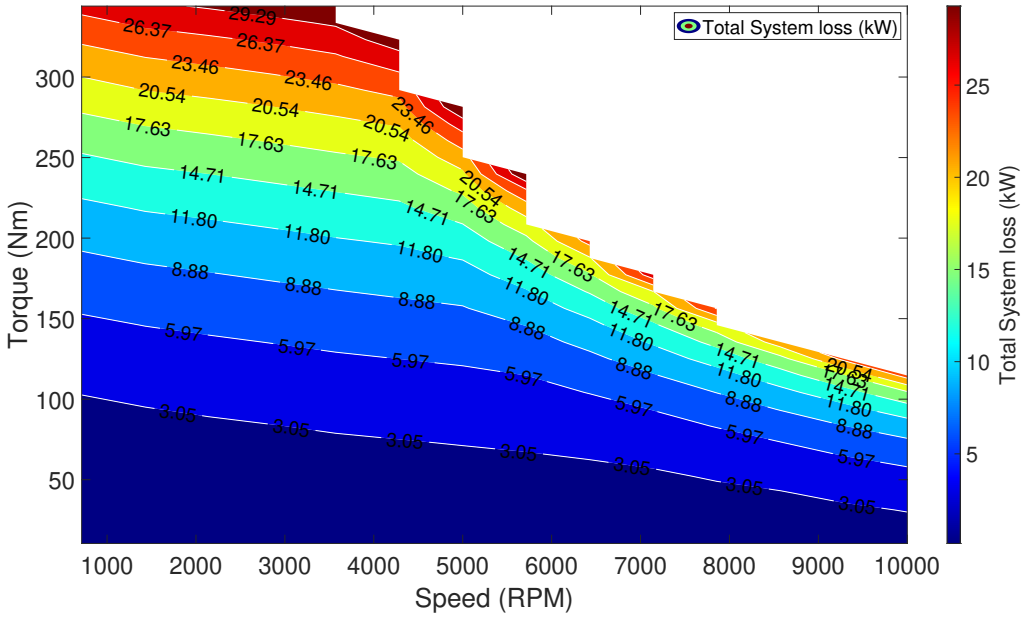


Figure 4.34: DPWM 10 kHz Total system loss

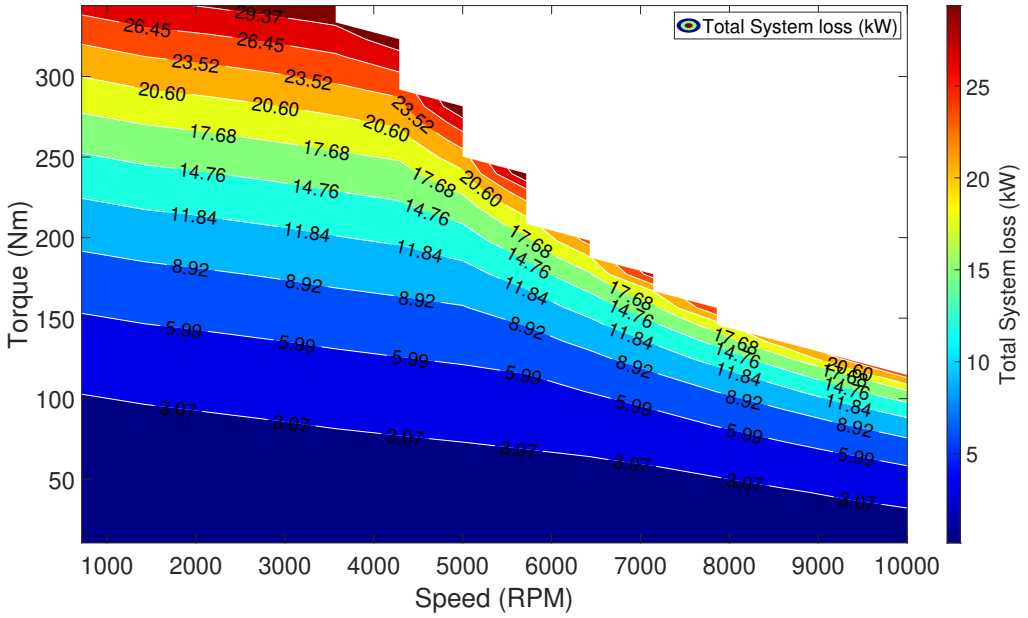


Figure 4.35: DPWM 15 kHz Total system loss

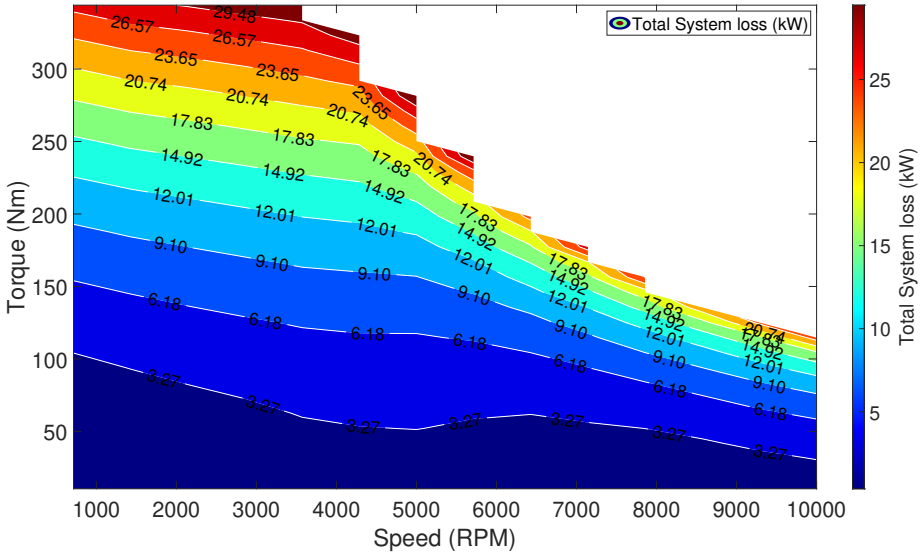


Figure 4.36: NSPWM 10 kHz Total system loss

Comparing modulation methods at the same frequencies, as seen in Fig.4.37 for 10 kHz, it is observed that DPWM hybrid 10kHz performs better at higher loads, i.e. for higher currents. SVPWM 10kHz on the other hand performs better at lower loads and speeds, where most urban drive cycle operating points reside. Here, switching losses and their contribution are small, impairing any advantage discontinuous methods may offer. Their higher general THD factor in this region results in their EM losses being larger than that of SVPWM and resulting in SVPWM's superior performance in this region.

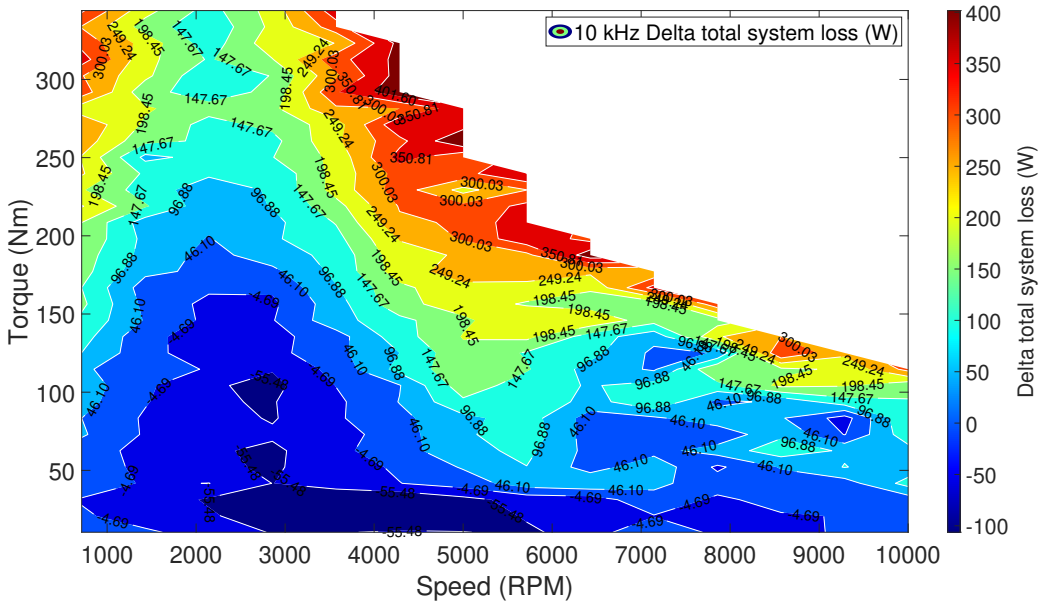


Figure 4.37: Total system delta losses between SVPWM and DPWM at 10 kHz

Performing the comparison at 15kHz, as seen in Fig.4.38, it is observed that the higher switching frequency results in lower THD factors and smaller EM loss margins between the methods. The higher switching losses of SVPWM 15kHz compared to DPWM Hybrid 15kHz and its margin is more significant, dominating any EM loss gains in favour of SVPWM, except at a small section in the torque speed map at very low loads where SVPWM is still marginally better. Overall, DPWM Hybrid 15kHz offers sizeable gains in efficiency across the rest of the map.

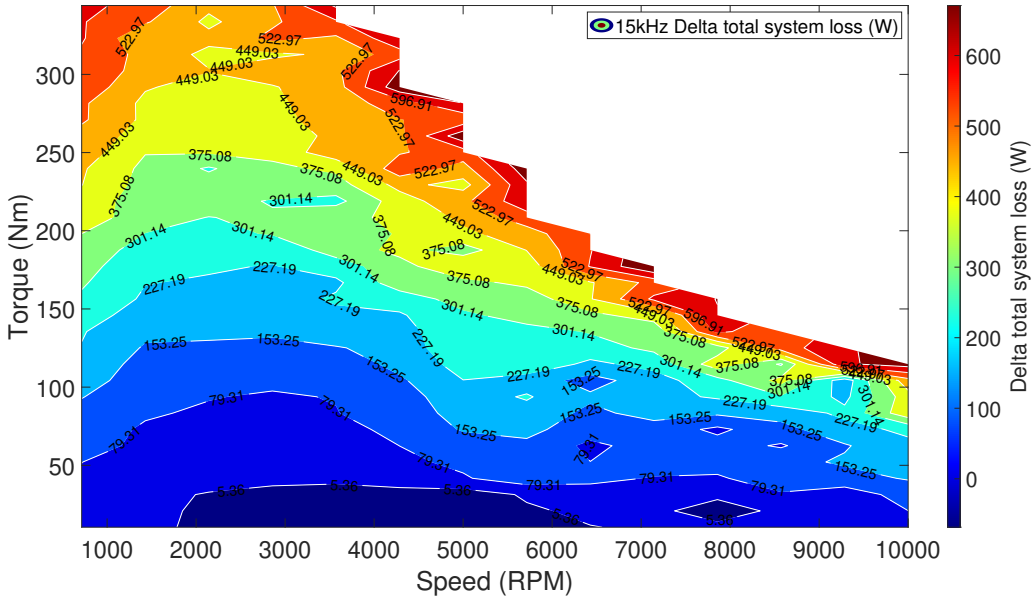


Figure 4.38: Total system delta losses between SVPWM and DPWM at 15 kHz

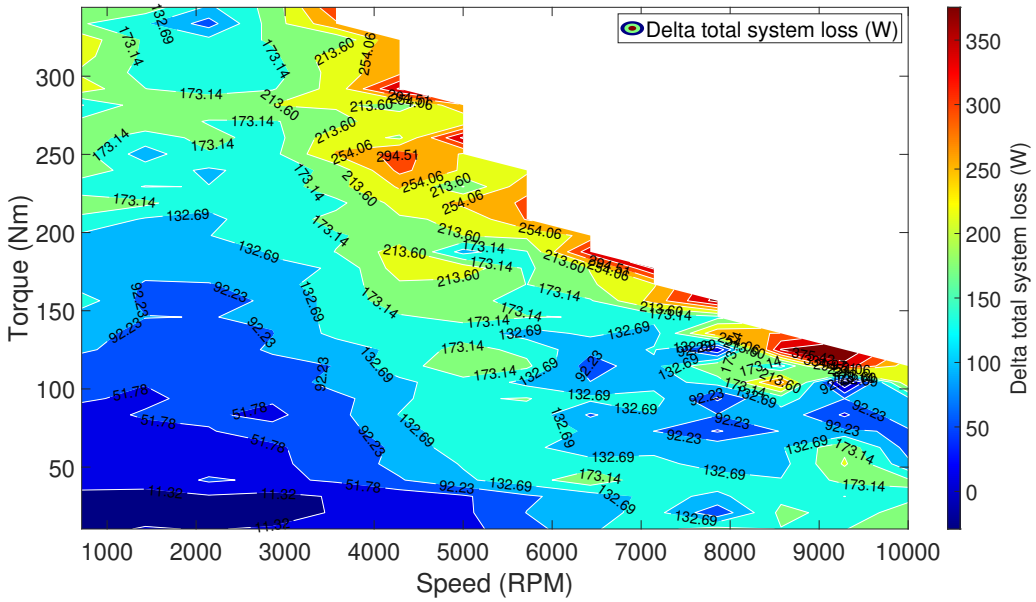


Figure 4.39: Total system delta losses for SVPWM 10kHz and DPWM 15 kHz

Finally, comparing SVPWM 10kHz and DPWM 15 kHz as seen in Fig.4.39, DPWM 15kHz consistently outperforms SVPWM 10kHz as DPWM's switching loss gains dominate any EM loss gains that SVPWM may have.

4.6 Hybrid modulation map and implementation

Comparing the system losses in the drive cycle range, the most efficient modulation strategies are now identified. This yields Fig.4.40, which is an optimised modulation map for maximum electric drive system efficiency. While DPWM's 15kHz loss advantage is evident compared to SVPWM 10kHz, SVPWM 15kHz does retain a region at low modulation index and loads. Of particular interest is the advantage of DPWM 10kHz over any other method at a high modulation index and again at very low speeds. Here, higher switching frequencies provide smaller THD factor benefits and thus lower EM delta losses. Their higher switching losses become a more dominant component and thus make a case for the implementation of not just variable modulation methods, but also variable frequency.

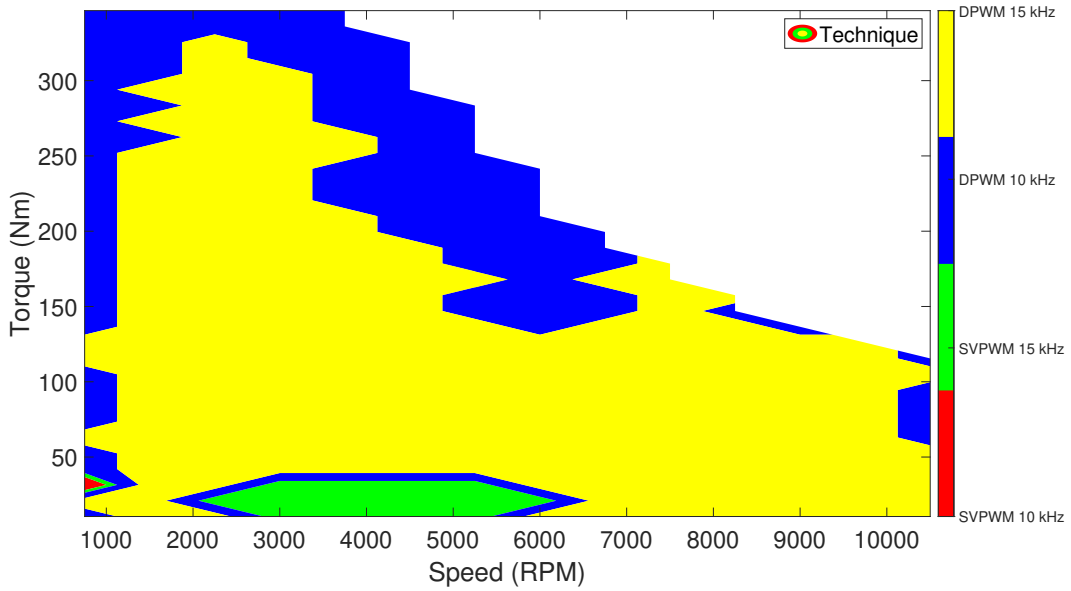


Figure 4.40: Final optimised modulation map for maximum electric drive system efficiency

4.7 Summarised Inverter delta maps

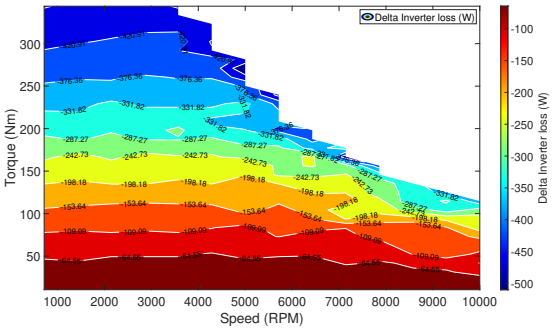


Figure 4.41: Total Inverter delta losses between DPWM 10 kHz and SVPWM 10 kHz

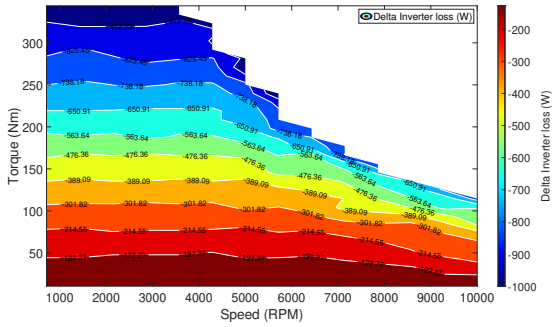


Figure 4.42: Total Inverter delta losses between DPWM 10 kHz and SVPWM 15 kHz

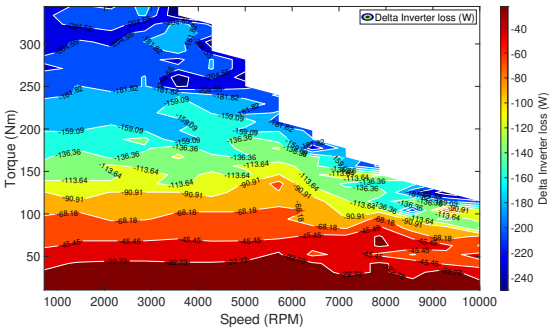


Figure 4.43: Total Inverter delta losses between DPWM 15 kHz and SVPWM 10 kHz

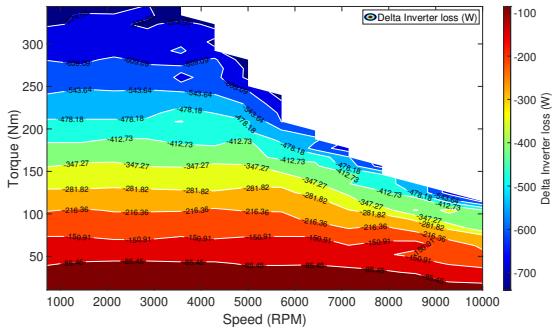


Figure 4.44: Total Inverter delta losses between DPWM 15 kHz and SVPWM 15 kHz

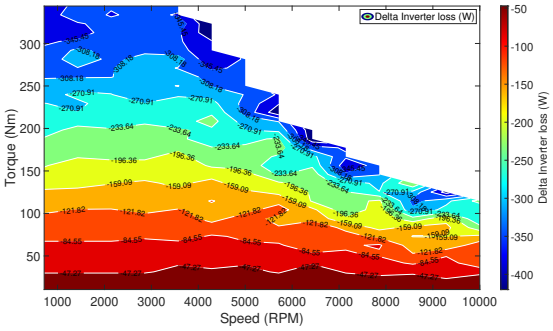


Figure 4.45: Total Inverter delta losses between NSPWM 10 kHz and SVPWM 10 kHz

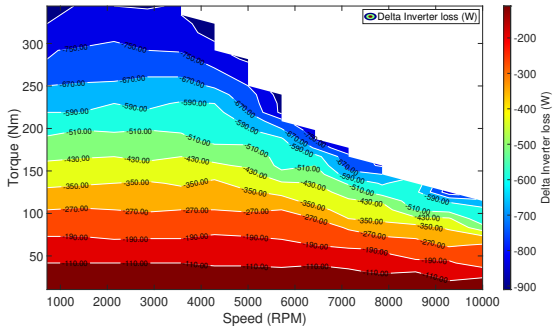


Figure 4.46: Total Inverter delta losses between NSPWM 10 kHz and SVPWM 15 kHz

Inverter losses are compared between DPWM 10 kHz, DPWM 15 kHz and NSPWM 10 kHz with SVPWM 10 kHz in the left column and SVPWM 15 kHz in the right column. A negative loss delta signifies the lower inverter losses of the alternate modulation techniques over SVPWM.

4.8 Summarised EM delta maps

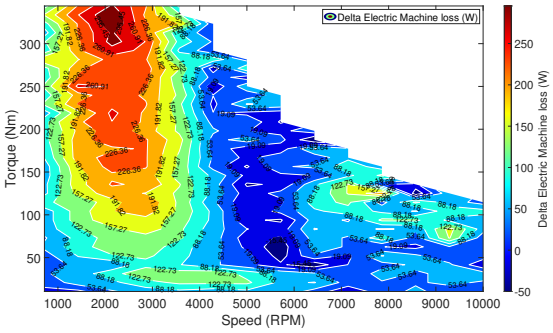


Figure 4.47: Total EM delta losses between DPWM 10 kHz and SVPWM 10 kHz

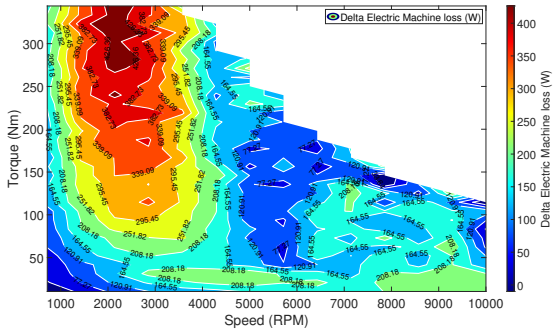


Figure 4.48: Total EM delta losses between DPWM 10 kHz and SVPWM 15 kHz

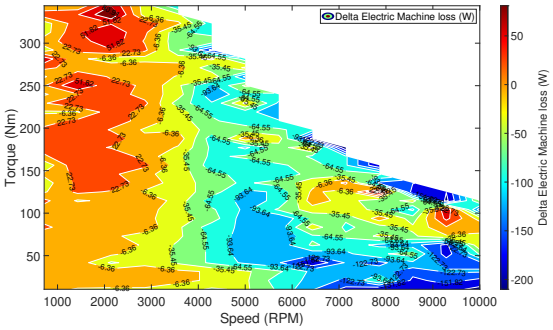


Figure 4.49: Total EM delta losses between DPWM 15 kHz and SVPWM 10 kHz

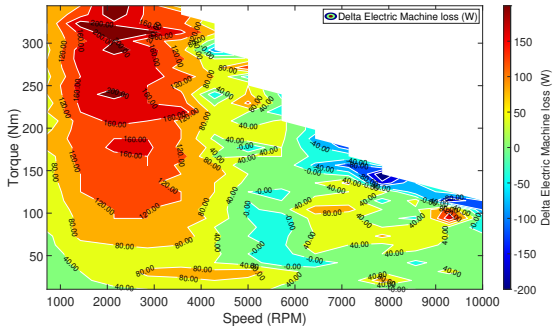


Figure 4.50: Total EM delta losses between DPWM 15 kHz and SVPWM 15 kHz

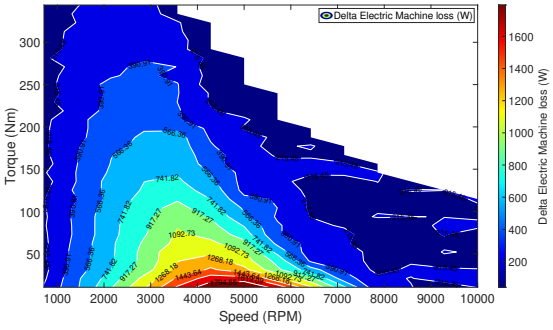


Figure 4.51: Total EM delta losses between NSPWM 10 kHz and SVPWM 10 kHz

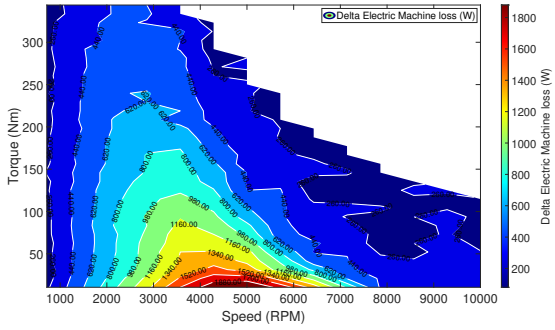


Figure 4.52: Total EM delta losses between NSPWM 10 kHz and SVPWM 15 kHz

EM losses are compared between DPWM 10 kHz, DPWM 15 kHz and NSPWM 10 kHz with SVPWM 10 kHz in the left column and SVPWM 15 kHz in the right column. A negative loss delta signifies the lower EM losses of the alternate modulation techniques over SVPWM.

4.9 Summarised System delta maps

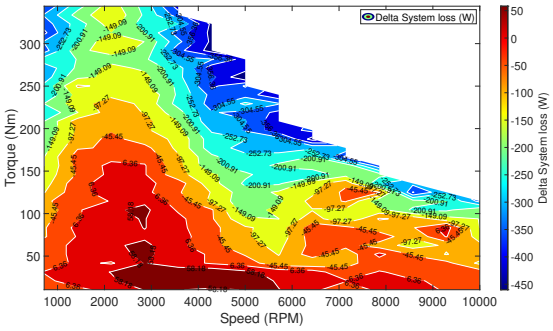


Figure 4.53: Total Inverter delta losses between DPWM 10 kHz and SVPWM 10 kHz

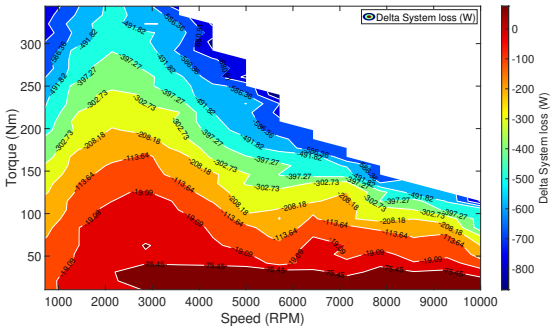


Figure 4.54: Total Inverter delta losses between DPWM 10 kHz and SVPWM 15 kHz

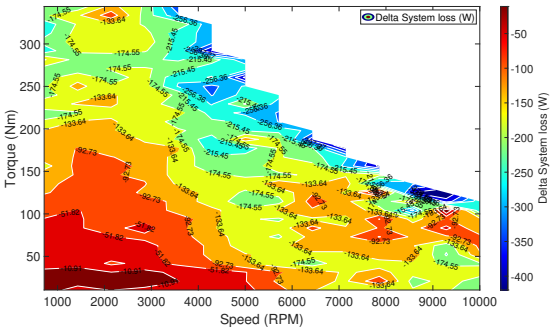


Figure 4.55: Total System delta losses between DPWM 15 kHz and SVPWM 10 kHz

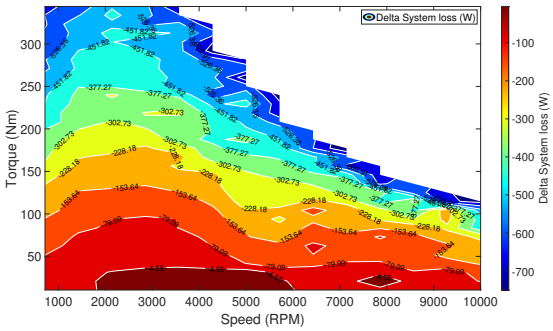


Figure 4.56: Total System delta losses between DPWM 15 kHz and SVPWM 15 kHz

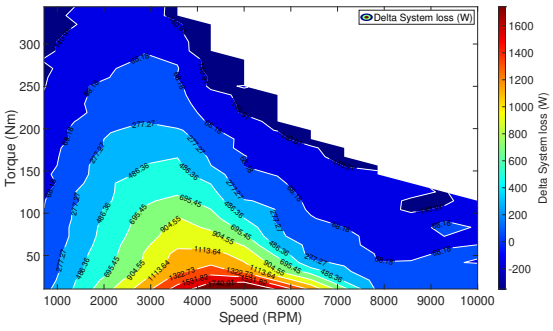


Figure 4.57: Total System delta losses between NSPWM 10 kHz and SVPWM 10 kHz

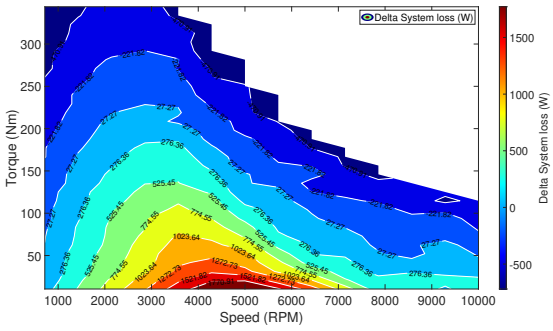


Figure 4.58: Total System delta losses between NSPWM 10 kHz and SVPWM 15 kHz

System losses are compared between DPWM 10 kHz, DPWM 15 kHz and NSPWM 10 kHz with SVPWM 10 kHz in the left column and SVPWM 15 kHz in the right column. A negative loss delta signifies the lower system losses of the alternate modulation techniques over SVPWM.

4.10 Drive cycle performance

Interpolating for the loss values when running at WLTC points as visualised in Fig. 4.59, the system losses are calculated for different modulation methods and switching ratio combinations as seen in Table. 4.1.

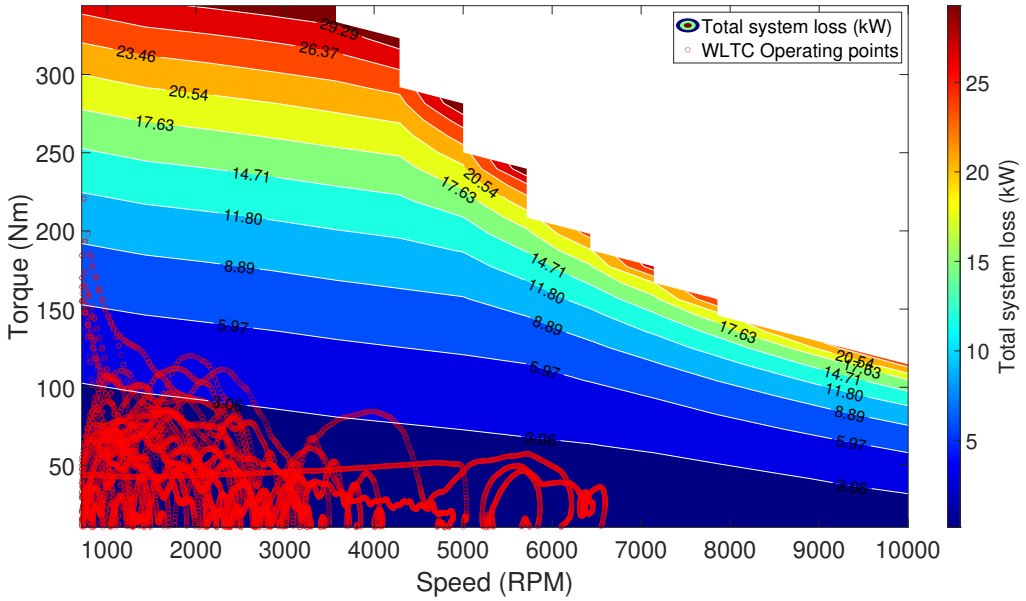


Figure 4.59: WLTC operating points marked in red on an optimised hybrid modulator system loss map

Table 4.1: Losses in various modulation methods

Modulation Method	Inverter losses (kW)	EM losses (kW)	System losses (kW)
SVPWM 10kHz	0.20	0.74	0.94
SVPWM 15kHz	0.24	0.69	0.93
DPWM 10kHz	0.16	0.81	0.97
DPWM 15kHz	0.18	0.73	0.92
NSPWM 10kHz	0.16	1.43	1.60

A small marginal gain is observed when utilising DPWM techniques at higher switching frequencies with gains predominantly from the inverter. The losses are compared and provided as a percentage in Table. 4.2 using SVPWM 10 kHz as a reference, i.e. 100%.

Table 4.2: Losses in various modulation methods (relative to SVPWM 10kHz)

Modulation Method	Inverter losses (%)	EM losses (%)	System losses (%)
SVPWM 10kHz	100	100	100
SVPWM 15kHz	120.23	92.96	98.76
DPWM 10kHz	80.69	109.16	103.08
DPWM 15kHz	91.41	98.51	97.00
NSPWM 10kHz	81.64	193.07	169.35

While Table. 4.2, offers a comparison between each modulation method and switching combination, as visualised in Fig. 4.40, implementing a hybrid modulation map can further reduce the system losses. Table. 4.3 compares the WLTC loss reduction achievable by comparing one set of modulation map combinations to another set of modulation combinations. Positive values signify a reduction in losses and thus improved efficiency.

Table 4.3: WLTC loss reduction comparison between modulation methods

Modulation Methods	WLTC Loss Reduction (%)
DPWM vs SVPWM at 10kHz	-3.08
DPWM 10/15kHz vs SVPWM 10kHz	3.17
Hybrid Switching & Modulation vs SVPWM 10kHz	3.78
DPWM vs SVPWM at 15kHz	1.77
DPWM 10/15kHz vs SVPWM 10/15kHz	1.08
Hybrid Switching & Modulation vs SVPWM 10/15kHz	1.70

5
Conclusion

5.1 Overview

In this thesis, the implementation of different modulation techniques, and their impacts on harmonic distortion, inverter losses, motor losses and system losses as a whole have been researched in detail.

The initial chapters provide an introduction to linear modulation in general, along with the various continuous and discontinuous techniques that are implemented on the modulator to vary switching effectively. Common mode voltage calculations are discussed in detail to implement SVPWM, DPWM 0, DPWM 1, DPWM 2 and DPWM 3. Additionally, the scalar implementation of the 2 dual carrier methods AZSPWM and NSPWM along with periodic switching sequences have also been discussed in detail which are otherwise complex in terms of implementation. The fundamentals of total harmonic distortion, power losses in inverters and motors along with their control have further been introduced and discussed in the context of this thesis work.

The scalar implementation of all these techniques is presented in the case setup, along with precise common mode examples. The optimised modulator technique analysis proves that no one single modulation technique is ideal. Hence, necessitating the development of a custom hybrid modulator technique. This has been implemented in the active clamping custom modulator that iterates across all possibilities and optimises for the technique that yields the least losses at each operating point, across all phase angles and modulation indices. This logic is then implemented on the Simulink control system. The custom modulator is validated with the default Simscape electrical modulator and the performance is proven to mirror the default modulator, consistent and replicable. SiC MOSFET loss modelling is then discussed with descriptions of current splits and switching instances between the 2 legs of the inverter. Currents injected with harmonics are then extracted from the control system for each technique to compare their performance on machine losses using finite element analysis on JMAG.

5.2 Observations from Results

The current injection-fed FEM analysis methodology yields converging results, with torque values that correlate to those that were requested. The model is consistent across the torque speed range but is highly sensitive to the supplied current angle and length of the current injections generated by the plant model. The THD analysis of the generated current injections shows a correlation between higher THD factors and higher motor losses. As a result, discontinuous methods that inherently possess higher harmonic content, perform more poorly than SVPWM at the electric motor but benefit from lower switching losses from the fewer switching instances at the inverter. From the analysis, it is found that the ideal modulation technique at any one point is heavily dependent on both the operating point and the hardware specifications and properties of the motor and inverter.

Among motor losses, low speed and high torque operating points result in higher harmonics, where higher switching frequencies and SVPWM yield lower motor losses. Conversely, high-speed points have lower harmonic content and thus can benefit from both lower switching frequencies and DPWM techniques. At the inverter, while conduction losses remain unchanged, DPWM is advantageous where higher currents and loads are used, i.e. high torque points. In the case of the model presented in this work, this results in DPWM 10kHz offering the lowest system losses at high torque and extremely low points, followed by DPWM 15kHz occupying the rest of the map except at very low torques and speeds where SVPWM the inverter loss benefits are inconsequential compared to those of the motors. However, as iterated before, the modulation map is sensitive to the hardware specifications. For instance, while motor losses are much more significant, utilising a lower-loss steel in the rotor and stator can significantly reduce the sensitivity to harmonics making the use of DPWM more prevalent across the torque-speed map. Simultaneously, the use of more advanced switches with lower losses can result in switching losses that are much more insignificant compared to the motor losses that instead make SVPWM more prevalent. Thus, the modulation map cannot be generalised.

Analysing the losses of this system for the WLTC drive cycle, we see small but appreciable gains of 3% when comparing DPWM 15 kHz and SVPWM 10 kHz. While DPWM 10 kHz offers a nearly 20% and 9% reduction in inverter losses to SVPWM 10 kHz and 15 kHz respectively, DPWM 10 kHz produces 9% more EM losses while DPWM 15 kHz offers a 1.5% reduction in EM losses, close to the 2% reduction of EM losses offered by SVPWM 15 kHz. Comparing across techniques, a strong case is made for the implementation of a hybrid modulation map that utilises different modulation techniques and switching combinations. While DPWM 10/15 kHz offers a 3.17% reduction in losses for WLTC compared to SVPWM 10 kHz, hybrid modulation that includes both DPWM Hybrid and SVPWM techniques at both 10 and 15 kHz can offer a 3.78% reduction in WLTC losses. This margin can potentially be increased by also implementing lower switching speeds.

In addition to the superior or at least comparable performance of DPWM tech-

niques, another significant advantage is the potential application of these techniques to either extend the operational power capability of inverters or, conversely, to facilitate downsizing. Inverters are characterized by a very short thermal time constant and relatively rigid thermal limits, which constrain the power rating of the powertrain. By substantially reducing switching losses at the same peak operating points, DPWM allows the inverter to function at higher current magnitudes while remaining within its predetermined thermal design limits. This enables the realization of enhanced power and performance. Alternatively, the inverter can be downsized and optimized for DPWM operation during peak power conditions, where efficiency is not a critical design constraint. This approach is particularly advantageous for the application of more economical or cost-sensitive EVs, which are optimized for efficiency and cost-effectiveness. By utilizing DPWM techniques, these vehicles can achieve the necessary performance levels to be perceived as viable choices for consumers, without compromising on their cost or efficiency objectives.

5.3 Future work

The methodology and approach utilised in this work prove accurate and consistent. However, certain constraints are identified that can be further worked on.

- The current model implements a 2-D partial derivative plant model of the PMSM that assumes a fixed flux map that does not vary with the rotor angle. Instead, a 4-D flux linkage plant model would add rotor angle dependence and allow factoring the varying flux of the rotor as a result of its geometry. Secondly, a finer and more detailed torque map, with a greater density of operating points at low and very high torque points is recommended. This would allow the characterisation of those operating points often used in typical drive cycles and repeated acceleration tests, as well as eliminate some of the loss and THD islands seen in the results.
- An investigation of a few more switching speeds across the modulation techniques could potentially open up a greater reduction in losses.
- This work consists of a sampling time that is too high to study the transients and harmonics that would be generated by the switching. Dead time, turn-on/off activation delays, and more are not considered in this thesis. Simulating the inverter on an electronic circuit simulator to study the micro-dynamics and resultant harmonics generated from different modulation techniques would provide invaluable insights.
- Simultaneously, a better understanding of the implementation of variable modulation is required for practical application. Real-world constraints and challenges need to be studied in its implementation.
- A better understanding of the aforementioned work would then enable a more in-depth understanding of the thermal constraints and headroom available to investigate additional performance or downsizing at the inverter.
- Finally, these modulation methods are not limited to one motor topology and should be investigated to see if they can offer improvements in efficiency or torque ripple characteristics, in specific operating points or across the map.

6
Ethics & Sustainability

6.1 Ethics

The following ethical principles were taken into account when performing this work,

- **Socially Responsible**: This work aims to enhance the efficiency of a BEV, a sustainable technology solution. The enhanced efficiency comes with the benefit of either reduced emissions or investigating alternative approaches to better drive the electric drive-train. Primarily being a simulation and digital analysis, no work was performed in test cells, on vehicles or in high-risk environments, thus posing little or no risk of harm to participants.
- **Technical accuracy, Bias and Objectivity**: Fair efforts were made to study existing literature and work to cross-reference and build on, to eliminate potential oversights. A variety of tools and methods have been used to re-verify current work, its implementation in our work, the accuracy of its results and to carefully study its limitations. The conclusions drawn in this work are supported by multiple analyses and studies and referenced work. A series of internal reviews between the examiner, supervisors and participants were used to outline the research workflow, question its methods, and results and suggest alternative outcomes and analyses to weed out potential errors.
- **Maintaining Integrity in Research**: A considerable number of journals and works have been referred to for this work. Careful efforts were made to refer to their contributions and reference their publications.
- **Protecting confidentiality and ensuring transparency**: This work does not contain any volunteer, participant, or personal data and does not compromise the confidentiality of an individual or organisation. Sensitive data pertaining to technical specifications, documents and models have been masked with care taken to not compromise the accuracy and results of this study. The methodology, approach and specifications have been transparently detailed while respecting stipulated confidentiality clauses.

6.2 Sustainability

A majority of the automotive and transport industry is striving towards sustainable mobility and carbon-neutral development. This thesis aims to enhance the efficiency of electric drive powertrain systems on a component and system level as a whole to extract more range from the pure electric vehicle. The primary contributors to

the drive system are the battery pack, power electronics, electric machine and the transmission. In comparison with internal combustion engine-driven vehicles, battery electric vehicles produce near-zero emissions during operation, contributing to the carbon neutral cause which also attracts market recognition from competitors. The European Environment Agency aims to cut carbon dioxide emissions from passenger cars by 55% and 50% from vans by the year 2030. This is a significant step towards the European Energy Commission's target of reducing energy consumption by 11% by the year 2030. Enhancing the energy efficiency of current electric vehicles is a sound pursuit in achieving these targets.

Although electric vehicles do not emit emissions during operation, the manufacturing of lithium-ion batteries and their electrodes involves questionable activities concerning sustainability, which makes the development of these components constraining. Mining of lithium to be used in battery electrodes involves the usage of heavy vehicles and equipment which are run on diesel and other heavy fuels over prolonged periods, which goes against the objective of sustainable development. Additionally, increased demand for such materials triggers unethical and illegal mining activities that also involve violation of basic human rights, as seen in various instances in Chile, China and Argentina in the race for precious metals. These activities also lead to local air pollution, and groundwater contamination in surrounding areas which impact the water supply for survival ultimately leading to health complications. Additionally, PMSMs also require rare earth magnetic materials for operation, which also involves challenges that go against the sustainable development goals of the European Union. Although dependent on these precious metals, PMSMs are highly efficient and power-dense making them a great option for vehicle propulsion sources, even in comparison to competing motor topologies.

The research conducted in this work aids in software-based enhancement to improve the efficiency of such drive systems that could potentially compensate for the emissions generated during pre-manufacturing processes to tip the scale towards being more carbon neutral across the product life cycle. Moreover, the work discussed is found to not be particularly limited to any one topology and can be deployed with potentially positive results.

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