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A Class-J Power Amplifier with Varactor Based Dynamic Load Modulation

Master's thesis in Wireless, Photonics and Space Engineering

William Hallberg

Department of Microtechnology and Nanoscience – MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2014

Thesis for the Degree of Master of Science in
Wireless, Photonics and Space Engineering

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Chalmers University of Technology
Department of Microtechnology and Nanoscience – MC2
Microwave Electronics Laboratory
SE-412 96 Gothenburg, Sweden
+ 46 (0)31-772 1000

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Abstract

In order to reach increasingly higher data rates and energy requirements in mobile networks, energy efficiency and broadband operation in power amplifiers have been driving parameter in the research of wireless transmitters. This thesis presents the theory for a broadband design of a dynamic load modulated class-J power amplifier. Calculations show that a drain efficiency higher than 70% down to an output power back off of 7.7 dB can be maintained for a fractional bandwidth of 36% by tuning the transistor load reactance during the appropriate operating conditions. The modulation of the transistor load reactance can, for example, be achieved with varactors.

The concept is demonstrated in a gallium nitride high electron mobility transistor power amplifier with silicon carbide varactors. The power amplifier achieved a power added efficiency over 50% for 1.70 to 1.80 GHz down to 5 dB output power back off, with the maximum output power of 40.4 dBm for continuous wave measurements. For modulated signals, the power amplifier showed excellent linearity and high efficiency. For a 3.84 MHz 6.6 dB peak to average power ratio W-CDMA signal at 1.75 GHz, the power amplifier achieved an adjacent channel leakage ratio of -48 dBc, an average power added efficiency of 44.9% and an average power of 33.1 dBm. The correlation between theory, simulated results and measured results is discussed to show the potential of the broadband, dynamic load modulated class-J power amplifier concept.

Keywords: Energy efficiency, Power amplifier, Dynamic load modulation, Class-J, Gallium Nitride (GaN), HEMT, Silicon Carbide (SiC), Varactor

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William Hallberg, June 2014

Notations and abbreviations

Notations

C_{ds} Drain-source capacitance.

K Rollet's stability factor – part one (K-factor).

P_{DC} DC power.

P_{out} Output power.

R_{opt} Optimum class-B load resistance.

V_{DS} Drain-source DC voltage.

V_{GS} Gate-source DC voltage.

V_{KNEE} Knee voltage.

Δ Rollet's stability factor – part two (Δ-factor).

η Drain efficiency.

f Frequency.

Abbreviations

ACLR Adjacent Channel Leakage Ratio.

AWG Arbitrary Waveform Generator.

CW Continuous Wave.

DAC Digital to Analog Converter.

DC Direct Current.

DLM Dynamic Load Modulation.

DPD Digital Pre-Distortion.

DSM Dynamic Supply Modulation.

DUT Device Under Test.

ET Envelope Tracking.

GaN Gallium Nitride.

HEMT High Electron Mobility Transistor.

IQ In-phase and Quadrature.

LSNA Large Signal Network Analyser.

NMSE Normalized Mean Square Error.

OPBO Output Power Back-Off.

PA Power Amplifier.

PAE Power Added Efficiency.

PAPR Peak to Average Power Ratio.

PCB Printed Circuit Board.

RF Radio Frequency.

Contents

Chapter 1

Introduction

1.1 Motivation

The usage of mobile communication is constantly increasing. Due to an increase of usage of services like streaming music and videos, cloud storage and cloud computing, the demand of high data rates is increasing very rapidly. By 2018, it is expected that the annual run rate of mobile network data traffic will be 190 exabytes, which is equivalent to 190 times more than all the traffic from Internet Protocol (IP), fixed line and mobile combined in 2000 [1].

In order to meet the increasing data rate demands, the network providers and operators are starting to implement different advanced solutions. One solution is to use complex modulation schemes for the signals. Increasing the order of the modulation scheme will increase the spectral efficiency, but it will also increase the Peak to Average Power Ratio (PAPR), i.e. how far the power level for the maximum value of the probability density function is from the maximum power level. For a conventional Power Amplifier (PA), the efficiency is proportional to the transistor drive level, which means that increasing the PAPR of a signal will decrease the average efficiency of the PA severely.

The available frequency spectrum for wireless networks is divided into a lot of different bands, e.g. the LTE standard utilizes 44 different bands [2]. If components with a low bandwidth is used in wireless networks, one amplifier for each band may be required. If broadband components that are able to handle more than one band is used, cost and size can be reduced. In order to reach data rate requirements, more than one band may be used for a single user (carrier aggregation), which also sets broadband demands. This is already utilized in today's standards, e.g. LTE advanced can utilize up to five 20 MHz carriers [3].

The PA consumes a lot of energy in radio base stations, e.g. in a macro radio base station, the PA is the most power consuming component, studies have shown that it is consuming 57% of all DC power at maximum load [4]. The power wasted in the PA introduces cost for the network operator and sets a carbon dioxide footprint on the environment, therefore it is necessary that the PA has a high efficiency performance. The European Union project METIS has set the requirement that the next generation mobile network system (i.e. 5G) should "fulfill the previous requirements under a similar cost and energy dissipation per area as in today's cellular systems" [5]. In addition, a too low efficiency in the PA may degrade its durability and it may cause problem with overheating.

In order to fulfill the requirements of the high data rates in the future, broadband PAs with good efficiency performance are needed. There are several ways of enhancing the efficiency performance of a PA. Due to its simplicity, the Doherty PA (with common input signal) is the most popular efficiency enhancement design [6], [7]. However, the input split needed in this Doherty PA introduces a gain loss equal to that split. For very high frequencies, the gain of the transistor is often a limiting factor, which makes it interesting to evaluate other efficiency enhancement

techniques that does not degrade the gain. Another efficiency enhancement technique is Envelope Tracking (ET) Dynamic Supply Modulation (DSM) [7]. In this technique, the envelope of the input signal controls the drain supply of the amplifier. The drain supply is controlled by an operational amplifier dissipating energy, whose efficiency may degrade the total efficiency of the whole circuit. This thesis explores a third technique: Dynamic Load Modulation (DLM). In this thesis, a novel, broadband, varactor based DLM class-J PA is described and implemented. The varactor voltage is modulated by the envelope of the input signal, amplified with an operational amplifier dissipating very little energy. Varactor based DLM enables high efficiency and in the future, such topology may be used to compensate antenna mismatch, which would improve the overall efficiency of the complete transmitter even further.

1.2 Thesis contribution

Previously, varactor based DLM class-J PAs has been implemented in for example [8], [9] and [10]. In [8], the PA achieves high efficiency performance when the transistor is backed off by dynamically tuning the reactive part of the transistor load such that it follows an optimal trajectory, found from a novel class-J performance theory derived in the same article. In this thesis, that theory is expanded such that the transistor can be operated in a way that the efficiency enhancement can be maintained over a wide bandwidth. In [9], a varactor based DLM PA is implemented from a load pull based design method, without a thorough theory as in [8]. [10] is another load pull based varactor DLM PA, where high efficiency is achieved over a wide band.

In this thesis, a power amplifier with efficiency enhancement has successfully been implemented. The center frequency is shifted and the performance is decreased from the simulated results. However, the performance at the measured center frequency is comparable to other published results of varactor based DLM PAs [8], [9], [10]. The sensitivity of this design method has been discussed in this thesis. To show the potential of the broadband class-J DLM concept, the correlation between the theory, simulated results and measured results has been discussed.

1.3 Thesis outline

This theses is initialized with a brief review of PA theory, with a focus on the class-B PA in chapter 2. Then, different efficiency enhancement techniques for the class-B PA is mentioned. The fundamental theory of the class-J PA is then discussed, together with an explanation of how a reactive tuning of the load can enhance the efficiency when the transistor is backed off over a large bandwidth. The complete design of the circuit is presented in chapter 3. A detailed description of the design of the input and output network is presented, together with motivations and simulation results. In chapter 4, measurement setups and results are presented for Continuous Wave (CW) measurements and modulated measurements. Finally, the thesis is concluded with a discussion of the presented work and suggestions of future work in chapter 5.

Chapter 2

Theory

In this chapter, the theory behind the design method of the wideband varactor tuned, DLM class-J PA will be presented. First, a brief explanation of PAs, with a focus on class-B PAs will be presented. Then, different efficiency enhancement techniques will be discussed. Finally, the class-J PA will be presented, starting with the fundamental theory and concluding with the wideband dynamic load modulated operation.

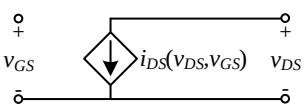
2.1 Power amplifiers

Power amplifiers can be distinguished into two different types: transconductance amplifiers and switch mode amplifiers. In a transconductance amplifier, the transistor operates as a voltage controlled current source, i.e. the current at the output is proportional to the voltage over the input. In a switch mode amplifier, the transistor is either fully turned on (maximum current) or turned off, thus acting as a switch. A schematic of a transconductance amplifier can be seen in figure 2.1a and a schematic of a switch mode amplifier can be seen in figure 2.2a.

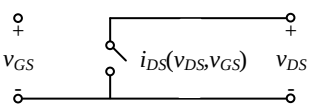
Transconductance amplifiers are usually divided in four different classes: class-A,-AB,-C and -D. The classes are distinguished by their conduction angle, i.e. the fraction of time during a full wave cycle on the input the current source is conducting. The class-B amplifier will be discussed in detail below. The class-J amplifier can be seen as variant of the class-B amplifier, but with different waveforms at the output. The class-J PA has the same maximum output power and drain efficiency as the class-B PA ($\eta = 78.5\%$).

2.2 Class-B power amplifier

The class-B PA is a transconductance amplifier biased and terminated in a way that gives half rectified sinusoidal current waveforms, i.e. the current source is conducting half of the time, and gives full sinusoidal voltage waveforms at the output of the transistor, see figure 2.3. The half rectified sinusoidal current waveform at the output of the transistor is achieved by selecting the



(a) Transconductance amplifier.



(a) Switch mode amplifier.

Figure 2.2

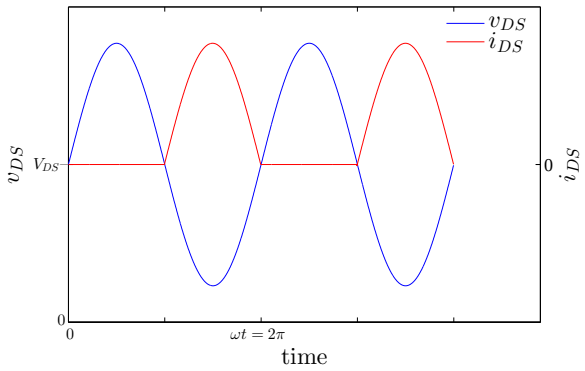


Figure 2.3: The voltage and current waveforms at the output of a class-B transistor, where V_{DS} is the bias point.

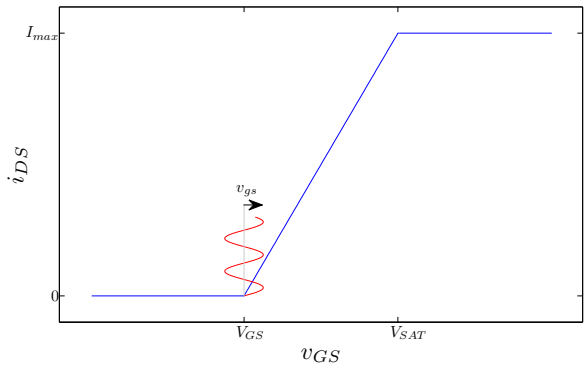


Figure 2.4: Output current as a function of input voltage of the transistor (blue), where V_{GS} is the bias point. Note how the RF-voltage (red) will turn the transistor on and off.

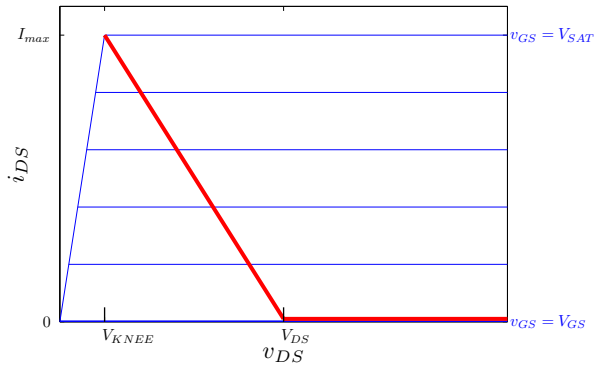


Figure 2.5: Output current as function of output voltage when DC is applied (blue lines) and when DC and RF is applied (red line) for a Class-B amplifier.

gate source bias point at the threshold voltage (V_T), i.e. $V_{GS} = V_T$, which is the point where the transistor is turned on, see figure 2.4. The full sinusoidal voltage waveform at the output of the transistor is achieved by short circuiting all voltage harmonics higher than the fundamental.

In figure 2.5, the output current is plotted as a function of the output voltage. The blue lines represents the output current function when only Direct Current (DC) is applied at the input. The red line represents the output current function when both DC and Radio Frequency (RF) is applied to the input (also called load line), when biased at the threshold voltage.

2.3 Efficiency enhancement techniques

The drain efficiency of an amplifier is defined as the ratio of the output power and DC power

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\Re(I_l^2 Z_L)/2}{V_{DC} I_{DC}} \tag{2.1}$$

where I_l is the current flowing through an attached load at the output (for a certain frequency), and Z_L is the impedance of that load. Since the DC voltage is constant and I_l and I_{DC} are

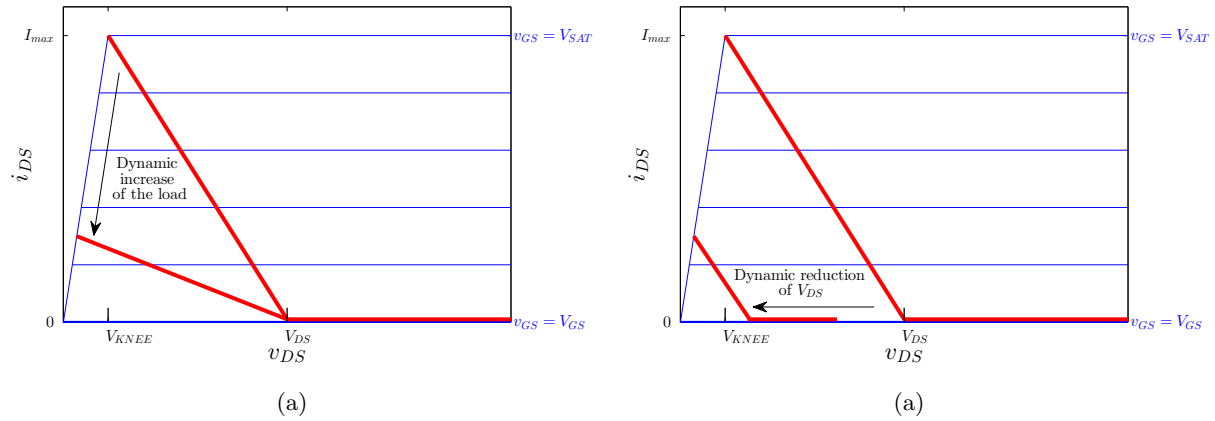


Figure 2.7: A demonstration of the load line for dynamic load modulation (a) and dynamic supply modulation (b) for a class-B PA. The direction of the arrow corresponds to backing off from maximum transistor drive level.

proportional to the transistor drive level, the drain efficiency is proportional to the drive level. Thus, the maximum drain efficiency is achieved at the maximum drive level, i.e. at maximum output current.

In order to achieve high efficiency when the transistor is backed off, an efficiency enhancement technique can be applied. There are two different categories of these techniques: DLM and DSM. In DLM, efficiency in back off is enhanced by dynamically increasing the load impedance as the transistor drive level is backed off. In equation (2.1), it can be seen that the efficiency is maintained at a high level as the transistor drive level is backed off if the load is increased at the same rate as the load current is decreased. In DSM, the efficiency in back off is enhanced by dynamically lowering the drain bias voltage as the transistor drive level is backed off. In equation (2.1), it can be seen that the efficiency is maintained at a high level as the transistor drive level is backed off if V_{DC} is decreased at the same rate as the load current is decreased. The load lines for DLM and DSM for a class-B PA are demonstrated in figure 2.7.

For modulated signals (with a PAPR larger than zero dB), the envelope of the RF signal, i.e. the baseband frequency, controls the modulation (of the load or supply), thus enhancing the average efficiency.

A popular DLM method is the Doherty PA, where the load modulation is achieved by introducing an additional current that changes the effective load the the transistor sees. This method is sometimes called active load modulation. The additional current is introduced by a second transistor, which can be controlled with a separate control signal or with the same signal as main transistor. If the second transistor is controlled with the same signal as the main transistor, the total amplifier system will be very simple (in comparison to the case with an additional control signal); the Doherty PA will be controlled in the same way as an ordinary PA. The simplicity of this Doherty PA is one of the reasons why it is so popular. There is one disadvantage though: because the input signal is splitted into two branches (usually 3 dB), there will be a gain loss (equal to the split ratio). For very high frequencies, low gain is usually a problem, which makes it interesting to evaluate other efficiency enhancement techniques.

2.4 Class-J power amplifier with dynamic load modulation

The class-B short circuiting of the harmonics higher than the fundamental can be achieved with the output capacitance of the transistor if it is large enough, meaning that the higher harmonics

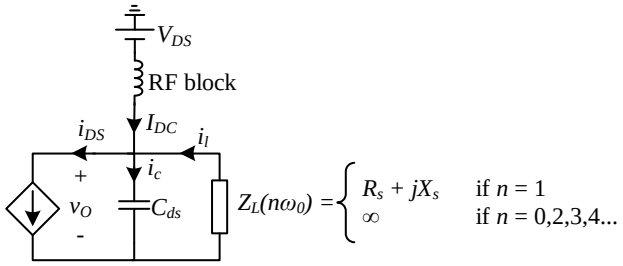


Figure 2.8: Class-J amplifier schematic.

are close to being short circuited, which gives close to ideal waveforms. In [7], it is described that if the reactance of the output capacitance fulfills $^{X_{C_{DS}}}/_{R_L} < 1$ (where R_L is the output load), classical class-B output voltage waveforms, i.e. nearly sinusoidal, can be expected. This ratio is dependent on the device technology and operating frequency. For Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs), operating at 2 GHz, this ratio can be as high as 3 [7]. Even with a high reactance, high efficiency operation can still be achieved with the correct harmonic termination. In the class-J PA, all harmonics higher than the fundamental are open circuited after the transistor output capacitance. In the ideal case, the class-J PA can be represented by a current source, the device output capacitance (drain-source capacitance, C_{ds}) and a termination that is open for harmonics higher than the fundamental and for DC. A schematic of an ideal class-J PA is shown in figure 2.8.

The transistor is biased at pinch off, resulting in a half-rectified sinusoidal current given by

$$i_{DS}(\theta) = \begin{cases} \beta I_{max} \sin\theta & \text{if } 0 < \theta < \pi \\ 0 & \text{if } \pi \leq \theta \leq 2\pi \end{cases} \tag{2.2}$$

where I_{max} is the maximum current of the transistor, β is the drive level ($0 \leq \beta \leq 1$) and θ is the phase of the input signal ($\theta = \omega t$). Since the harmonic components are open circuited, the current at the load only has one frequency component (the fundamental component) and can be written as

$$i_l = |I_l| \sin(\theta + \varphi) \tag{2.3}$$

were $|I_l|$ is the magnitude and φ is the phase shift. I_l (phasor representation) can be found by applying Kirchoff's current law to the fundamental frequency of i_{DS}

$$I_l = \frac{\beta I_{max}}{2} \frac{Z_{i,f}}{Z_L} \tag{2.4}$$

where $Z_{i,f}$ is the load presented to the current source at the fundamental frequency, which can be written as

$$Z_{i,f} = \frac{Z_L}{j\omega C_{ds} Z_L + 1}. \tag{2.5}$$

The phase shift φ can be calculated by

$$\varphi = \underline{/I_l}. \tag{2.6}$$

The current through the device output capacitor can be found by solving Kirchoff's current law

$$i_c = I_{DC} - i_{DS} - i_l \tag{2.7}$$

where the DC is given by

$$I_{DC} = \frac{\beta I_{max}}{\pi}. \tag{2.8}$$

When the DC- and load currents are known, the output power, P_{out}, DC power, P_{DC},and drain efficiency, η, can be calculated by

$$P_{out} = \Re(|I_l|^2 Z_L)/2 \tag{2.9}$$

$$P_{DC} = V_{DC} I_{DC} \tag{2.10}$$

$$\eta = \frac{P_{out}}{P_{DC}}. \tag{2.11}$$

With these derivations, η and P_{out} can be expressed as functions of R_s, X_s, $X_{C_{ds}}$ and β. However, not every combination of R_s, X_s, $X_{C_{ds}}$ and β will yield a physical solution. For a physical solution, the output voltage, v_O, must be equal or larger than zero for all values of θ. The output voltage can be calculated by

$$v_O(\theta) = \frac{1}{\omega C_{ds}} \int_0^\theta i_c \mathrm{d}\theta + V_{OFF} =$$

$$\begin{cases} \frac{1}{\omega C_{ds}} \left(\beta I_{max} \left[\frac{\theta}{\pi} + \cos\theta - 1 \right] + |I_l| \left[\cos\varphi - \cos\left(\theta + \varphi\right) \right] \right) + V_{OFF} & \text{if } 0 < \theta < \pi \\ \frac{1}{\omega C_{ds}} \left(\beta I_{max} \left[\frac{\theta}{\pi} - 2 \right] + |I_l| \left[\cos\varphi - \cos\left(\theta + \varphi\right) \right] \right) + V_{OFF} & \text{if } \pi \leq \theta \leq 2\pi \end{cases} \tag{2.12}$$

where V_{OFF} is selected such that the correct DC voltage is obtained, i.e. V_{DS}.

Finally, R_s, X_s, $X_{C_{ds}}$ and β can be swept and η and P_{out} can be calculated for all physical solutions, i.e. all combinations that fulfill $v_O(\theta) \geq 0$ for all θ. In order to generalize, R_s, X_s and $X_{C_{ds}}$ are normalized with the optimum class-B load resistance, R_{opt}, which is defined as

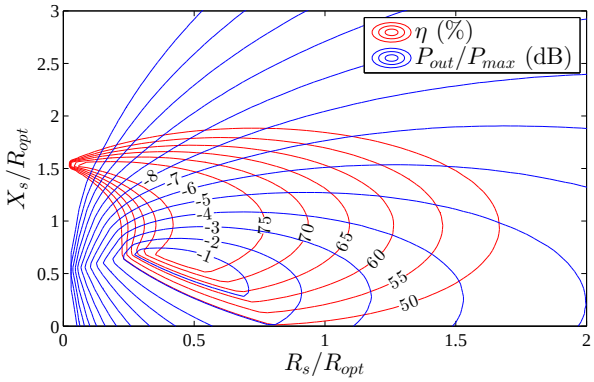
$$R_{opt} = \frac{v_{ds_{max}}}{i_{ds_{max}}} = \frac{V_{DS} - V_{KNEE}}{I_{max}/2}. \tag{2.13}$$

The results for different $X_{C_{ds}}/R_{opt}$ ratios are plotted in contours in figure 2.12. In these plots, P_{out} has been normalized to the maximum class-B output power, P_{max}, which is defined as

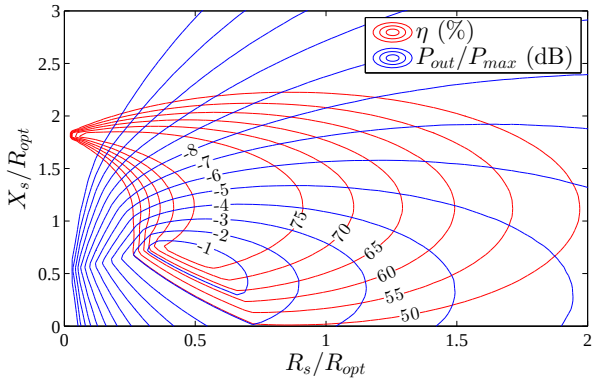
$$P_{max} = \frac{1}{2} v_{ds_{max}} i_{ds_{max}} = \frac{(V_{DS} - V_{KNEE}) I_{max}}{4}. \tag{2.14}$$

If X_s is varied while R_s is kept fixed, high drain efficiency can be obtained over a large dynamic range of output powers. It is evident that a reactively load modulated class-J architecture is a good candidate for a dynamically load modulated PA.

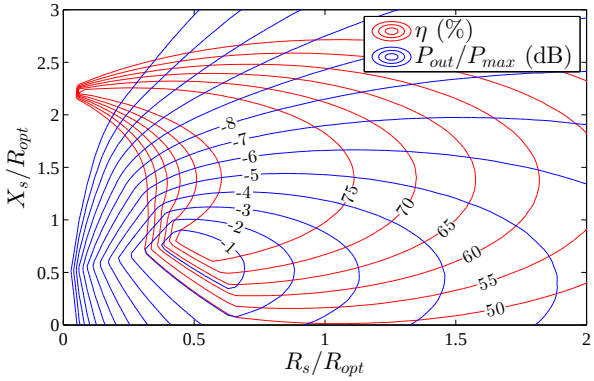
When ω increases, the ratio $X_{C_{ds}}/R_{opt}$ decreases. Figure 2.9a demonstrates η and P_{out} for a frequency 36% higher compared to the contours in figure 2.11a. If the resistive part of the load is kept fixed at $R_s/R_{opt} \approx 0.5$, high efficiency operation is possible over a wide bandwidth. The wideband operation possibilities are demonstrated in figure 2.13a and 2.14a. In 2.13a, the resistive part of the load is fixed $R_s/R_{opt} = 0.5$ and η and is plotted for different X_s/R_{opt} and $1/(X_{C_{ds}}/R_{opt})$ (which is proportional to frequency). High efficiency operation by tuning X_s is possible for $0.35 \leq 1/(X_{C_{ds}}/R_{opt}) \leq 0.95$. A cross section for different values of $1/(X_{C_{ds}}/R_{opt})$ within this span is



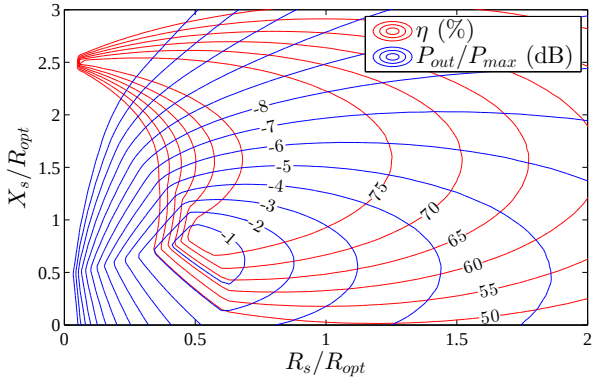
(a) $X_{C_{ds}}/R_{opt} = 1.54$



(a) $X_{C_{ds}}/R_{opt} = 1.82$

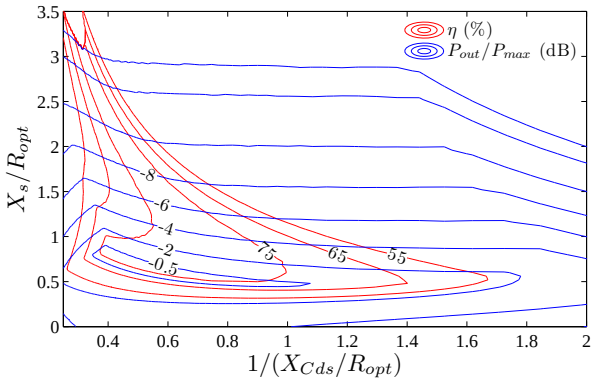


(a) $X_{C_{ds}}/R_{opt} = 2.22$

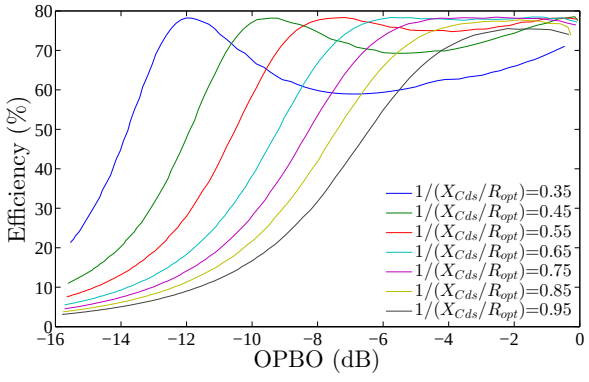


(a) $X_{C_{ds}}/R_{opt} = 2.5$

Figure 2.12: Contour plots for the drain efficiency and the normalized output power for different $X_{C_{ds}}/R_{opt}$. Later in this chapter, it will be shown that these specific ratios enables good performance.



(a)



(a)

Figure 2.14: The wideband operation possibilities. In (a), the resistive part of the load is fixed $R_s/R_{opt} = 0.5$ and η and P_{out} contours are plotted for different X_s/R_{opt} and $1/(X_{C_{ds}}/R_{opt})$ (which is proportional to frequency). In (b), the cross section for different $1/(X_{C_{ds}}/R_{opt})$ is plotted versus OPBO.

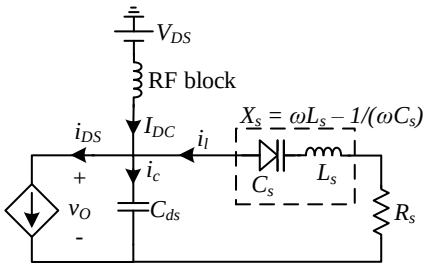


Figure 2.15: Class-J PA with a series inductor and varactor.

shown in figure 2.14a. In this figure, it can be seen that an Output Power Back-Off (OPBO) of 7.7 dB with more than 70% drain efficiency can be maintained for $1/(X_{C_{ds}}/R_{opt})$ from 0.45 to 0.65, which corresponds to a fractional bandwidth of 36% (which is equivalent to $X_{C_{ds}}/R_{opt} = 1.54$ to 2.22).

One way of implementing the tuning of X_s is by using a series inductor together with a series varactor, as in figure 2.15. The series inductor and varactor present a net reactance of

$$X_s = \omega L_s - \frac{1}{\omega C_s}. \tag{2.15}$$

The output topology in figure 2.15 also acts as a low pass filter, presenting a close to open circuit impedance for the harmonics higher than the fundamental, which enables the class-J operation.

The required varactor tuning range for achieving the wanted X_s, is dependent on the inductor reactance $X_{L_s} = \omega L_s$. A large L_s requires a small tuning range of the varactor and a small L_s requires a large tuning range of the varactor. The varactor tuning range of a real varactor is limited and therefore L_s cannot be too small. A small tuning range makes X_s more sensitive to varactor voltage and the RF voltage over the varactor, which means that L_s cannot be too large either.

In figure 2.13a, it can be seen that the required X_s tuning range for high efficiency down to 7.7 dB OPBO is 0.72 to 1.8 for $1/(X_{C_{ds}}/R_{opt}) = 0.45$ and 0.56 to 1.6 for $1/(X_{C_{ds}}/R_{opt}) = 0.65$. If L_s is

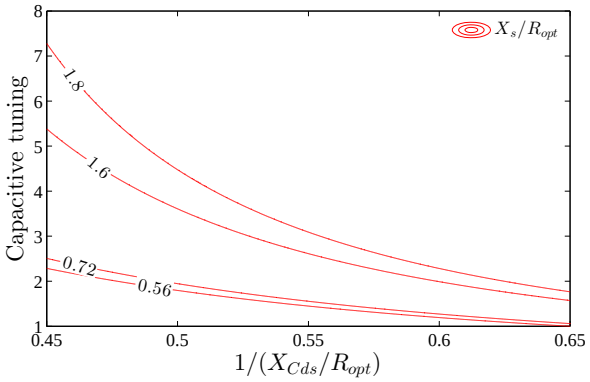


Figure 2.16: Capacitive tuning requirements for a LC series network when $X_{L_s}/R_{opt} = 3.42$ (X_{L_s} calculated when $1/(X_{C_{ds}/R_{opt}}) = 0.65$).

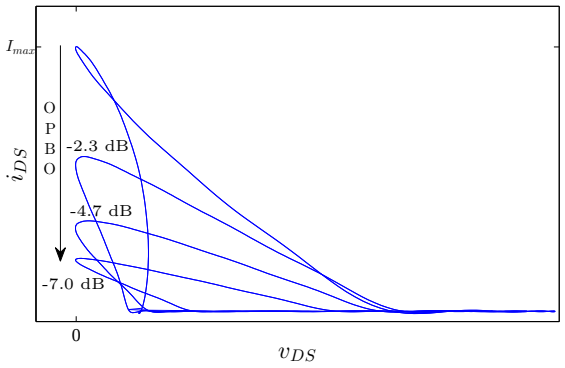


Figure 2.17: The load lines for a class-J PA that is modulated in optimum way for $1/(X_{C_{ds}/R_{opt}}) = 0.55$.

selected such that $X_{L_s}/R_{opt} = 3.42$, the required capacitive tuning will be between 1 and 1.58 for $1/(X_{C_{ds}/R_{opt}}) = 0.65$ and between 2.5 and 7.24 for $1/(X_{C_{ds}/R_{opt}}) = 0.45$ (where the ratios have been normalized with the same capacitance). This means that the varactor should have a capacitance ratio between 1 and 7.24 in order to achieve the wanted X_s range for $1/(X_{C_{ds}/R_{opt}}) = 0.45$ and $1/(X_{C_{ds}/R_{opt}}) = 0.65$. A varactor with these tuning possibilities will also achieve the wanted X_s ranges for frequencies with ratios between $1/(X_{C_{ds}/R_{opt}}) = 0.45$ and $1/(X_{C_{ds}/R_{opt}}) = 0.65$. This is demonstrated in a X_s/R_{opt} contour plot in figure 2.16, where it can been seen that the tuning behaviour for the band edges almost coincide.

The load lines for a class-J PA that is modulated in optimum way for $1/(X_{C_{ds}/R_{opt}}) = 0.55$ can be seen in figure 2.17. It can be seen that the load lines (hence also the waveforms) are quite different from the ideal class-B case above.

Since the harmonics higher than the fundamental are not completely short circuited in the design from figure 2.15, the transistor will not behave exactly as an class-J PA, which suggest that the results from the theory will not be accurate to 100%. It should also be remembered that the transistor is very simplified; the model does not consider things such that an actual transistor is bilateral and that an actual output capacitance is non-linear. However, since this model works has successfully been used in [8], it is reasonable to believe that the simple model is sufficiently accurate.

Chapter 3

Amplifier design

In this chapter, a detailed description of the design of the PA is presented. First, the specifications of the PA is presented, followed by a description of the characteristics of the selected transistor and varactors. Then, a detailed description of the design of the input and output network is described. The chapter is concluded with the simulation results and discussion of the correlation between the theory and the simulation results.

3.1 Specifications

For the amplifier, a 15 W GaN HEMT transistor by Cree (CGH60015D) was used (appendix C). The PA was implemented on Rogers 4350 Printed Circuit Board (PCB) (appendix B). The center frequency was chosen to $f_c = 2.14\,\text{GHz}$, which is at the downlink band 1 for LTE [2]. From figure 2.14a, it was shown that for high drain efficiency operation for a large OPBO over a large bandwidth, the ratio $1/(X_{C_{ds}}/R_{opt})$ should vary from 0.45 to 0.65. This suggest that the center frequency should correspond to $1/(X_{C_{ds}}/R_{opt}) = 0.55$. From the theory, η should be higher than 70% down to 7.7 dB OPBO for a fractional bandwidth of 36%, i.e. f from 1.75 GHz to 2.53 GHz.

From the figures 2.12 and 2.14, the output series resistance was chosen to $R_s = 0.5R_{opt}$. From figure 2.13a, it can be seen that X_s/R_{opt} should be tunable between 0.54 and 1.8 for high efficiency operation for all frequencies in the band. Regarding the ratio between X_{L_s} and X_{C_s}, it will be determined later by the available varactor sizes.

3.2 Transistor characteristics

The DC characteristics of the Cree transistor are shown in figure 3.1. The maximum drain current at the knee is $I_{max} = 2.6\,\text{A}$ and the corresponding voltage at that point is $V_{KNEE} = 5.2\,\text{V}$. When biased at the recommended $V_{DS} = 28\,\text{V}$, the optimum class-B load resistance will be $R_{opt} = 17.5\,\Omega$, which sets the output series resistance to $R_s = 8.75\,\Omega$.

In the transistor data sheet, the output capacitance of the transistor is approximated to $C_{ds} = 0.9\,\text{pF}$ (during the conditions $V_{DS} = 28\,\text{V}$, $V_{GS} = -8\,\text{V}$ and $f = 1\,\text{MHz}$). However, in simulations later on, when the transistor was stabilized and terminated with the intended output network, the total effective capacitance at the output of the transistor was approximated to $C_{ds} \approx 2.4\,\text{pF}$ at the maximum drive level of the transistor, see figure 3.2. It was mentioned that the center frequency should correspond to $1/(X_{C_{ds}}/R_{opt}) = 0.55$, which for $f_c = 2.14\,\text{GHz}$ means that the total output capacitance of the transistor should be $C_{ds} = 2.37\,\text{pF}$. The total capacitance is achieved with the transistor output capacitance and a shunt capacitor (if necessary).

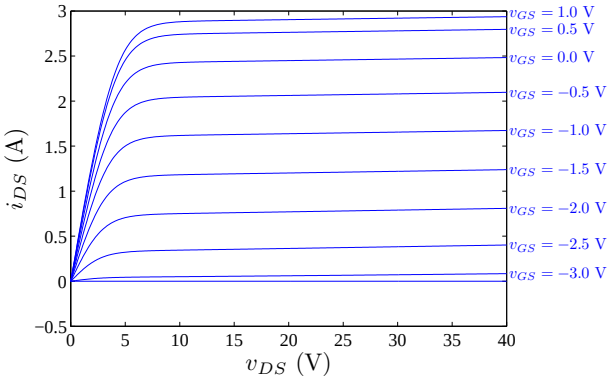


Figure 3.1: DC characteristics of the Cree transistor.

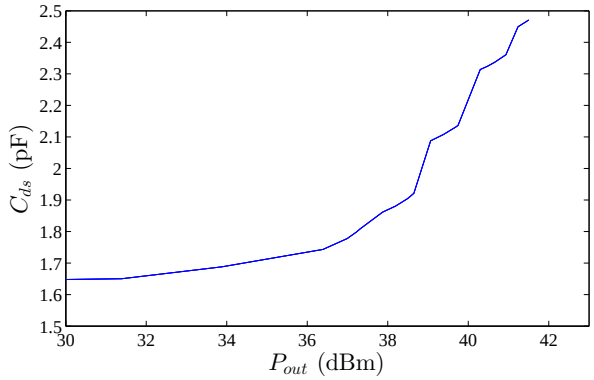


Figure 3.2: The effective C_{ds} at the output of the transistor (when stabilized and terminated with the intended output network).

The non-constant behaviour of C_{ds} implies that ${}^{X_{C_{ds}}}/_{R_{opt}}$ will not only change with frequency; it will also change with the transistor drive level. For the maximum output power at $f = 2.14\,\text{GHz}$, we have that ${}^{X_{C_{ds}}}/_{R_{opt}} = 1.77$ ($C_{ds} = 2.4\,\text{pF}$), and at 5 dB OPBO, the ratio is ${}^{X_{C_{ds}}}/_{R_{opt}} = 2.5$ ($C_{ds} = 1.7\,\text{pF}$). This means, for one frequency, that the load modulation will not be a linear curve going straight upwards in the contour plots in figure 2.12: as the output power is backed off, the contours will change.

3.3 Varactor characterisitics

For this amplifier, an in-house Chalmers SiC-varactor with a tunable capacitance between 2.5 pF – 21.0 pF, when biased with 0 – 100 V, was used (a variant of [11]). In order to achieve the wanted ${}^{X_s}/_{R_{opt}}$ ratios, the varactors were placed in anti-series. In addition, anti series varactors are desirable since they have linearity benefits compared to a single varactor [12], [13], [14]. When in anti-series, the capacitance range will be between 1.3 pF – 10.5 pF (a capacitive tuning ratio of 1 to 8.1), see figure 3.3.

When RF voltage is applied to the varactors, they will get an effective capacitance (since the RF will swing across both sides of the bias point of the varactors, where the capacitance differs). It will be shown later, in large signal simulations, that the RF-swing from the transistor is largest at the highest varactor bias points, i.e. when the capacitance of the varactors changes least abrupt. At the bias points where the capacitance of the varactors changes most abrupt, the RF-swing from the transistor will be at its lowest. This means that the effective capacitance

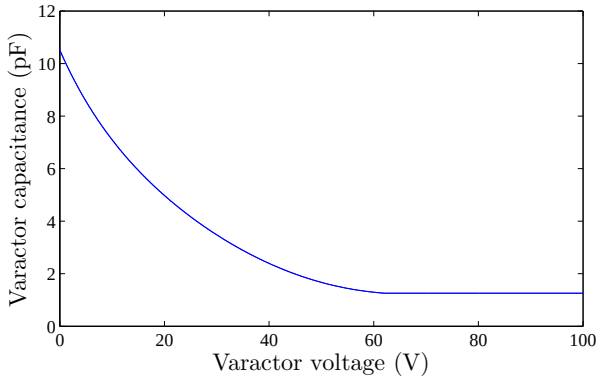


Figure 3.3: The capacitance of two anti-series Chalmers SiC-varactors.

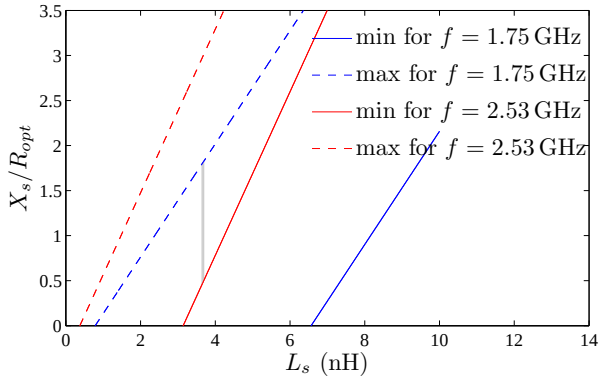


Figure 3.4: The X_s tuning possibilities for different L_s, when the varactor is tunable between 1.26 pF – 10.52 pF, for $f = 1.75$ GHz and $f = 2.53$ GHz.

versus varactor voltage, when RF is applied, will behave very similar to the behaviour without RF, i.e. like in figure 3.3.

When the effective capacitance of the varactors is known, the value of the output series inductor, L_s, can be calculated. It was mentioned that X_s/R_{opt} should be tunable between 0.54 and 1.8 in order to reach high efficiency operation for $1/X_{C_{ds}}/R_{opt} = 0.45$ to 0.65. X_s is a function of the series inductance and the capacitance of the anti-series varactors. The lower and upper frequencies in the band will set the X_s tuning possibilities. In figure 3.4, the possible maximum and minimum values of X_s/R_{opt} for $f = 1.75$ GHz and $f = 2.53$ GHz are plotted as a function of L_s. The limiting factors of the X_s tuning range will be the maximum X_s-value for $f = 1.75$ GHz and the minimum X_s-value for $f = 2.53$ GHz. If X_s/R_{opt} should be tunable between 0.54 and 1.8 for all frequencies in the band, then L_s must be between 3.65 nH and 3.7 nH. The chosen varactor configuration together with a series inductor of 3.7 nH corresponds to the tuning possibilities in figure 2.16.

3.4 Input network

3.4.1 Stability

First, the transistor was stabilized with one series and one shunt resistor, see figure 3.5. The stability of the transistor was examined for all possible bias points and X_s/R_{opt} combinations

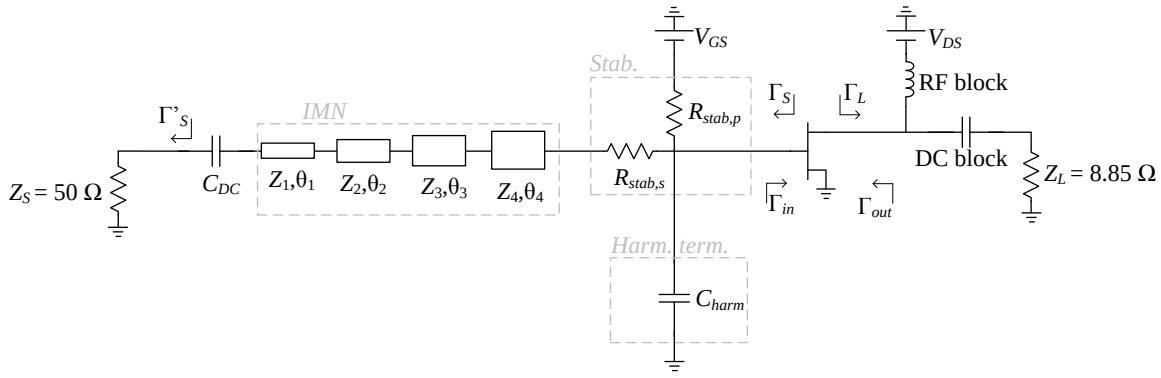


Figure 3.5: A schematic of the input network, including bias network, stabilization network and fundamental and second harmonic termination.

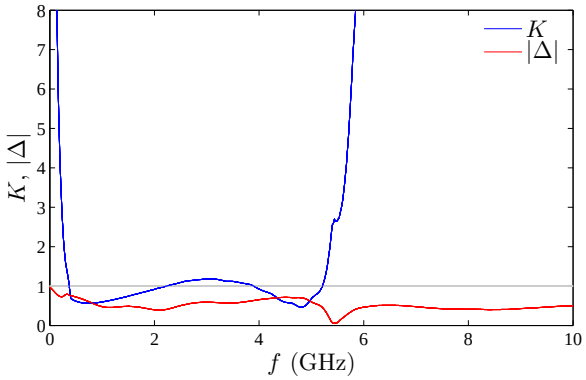
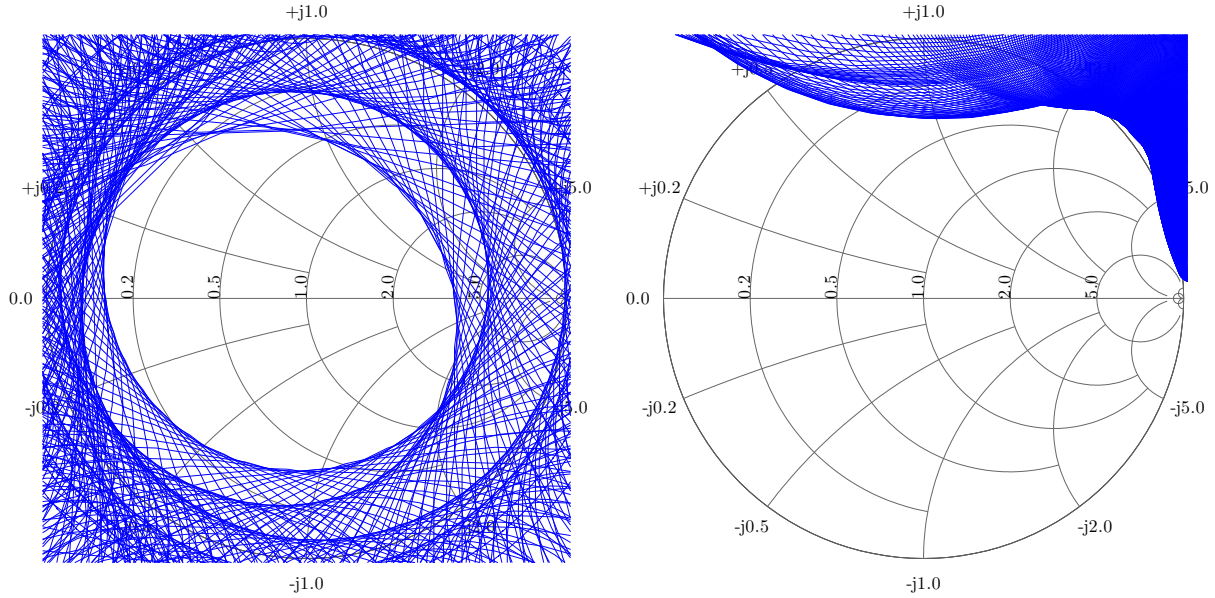


Figure 3.6: The stability factors K and $|\Delta|$.

in order to ensure stability for large signal operation. The resistors prevents low resistive and high conductive impedances ever being presented to the transistor for any frequency. The higher series resistance, the higher resistive impedances will be blocked, but it will also dissipate more power. For the shunt resistor, it is the other way around. Dissipating power is what is stabilizing the transistor, therefore it is desirable. However, the power dissipation also leads to lower gain of the transistor, which means that if the transistor is stabilized more than necessary, the gain will be lower than it has to be. This applies for in band frequencies. Outside the band, the transistor can be stable well beyond the limit between stability and instability without affecting the in band performance.

The stability factors K and $|\Delta|$ for $f = 0$ to 10 GHz, when biased with the worst case bias, i.e. $V_{gs} = -3.2$ V and $V_{ds} = 15$ V, together with the complete input network (with actual components and transmission lines) are plotted in figure 3.6. The transistor is unconditionally stable for 0 – 0.37 GHz, 2.23 – 3.89 GHz and for frequencies higher than 5.21 GHz. The transistor is conditionally stable for 0.37 – 2.23 GHz and 3.89 – 5.21 GHz, which means that if no impedances inside the unstable area of the stability circles is presented to the transistor, the transistor will be stable.

The source and load stability circles for $f = 0$ to 10 GHz, when biased with the worst case bias, together with the complete input network (with actual components and transmission lines)



(a) Source stability circles at the Γ'_s-plane, normalized to 50 Ω.

(a) Load stability circles at the Γ_L-plane, normalized to 8.85 Ω.

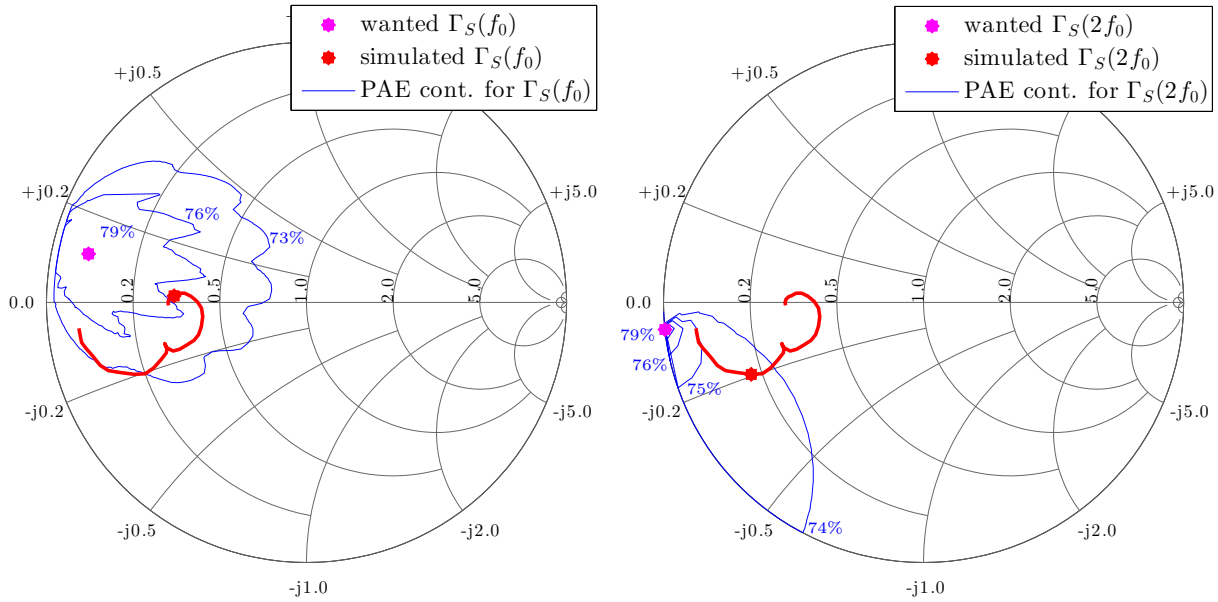
Figure 3.8: Stability circles for $f = 0$ to 10 GHz, when biased with $V_{gs} = -3.2$ V and $V_{ds} = 15$ V.

is plotted in figure 3.8. The center in both figures presents stable impedances, i.e. S_{11} and S_{22} smaller than unity, which means that the transistor will be stable as long as the reflection coefficient doesn't cross any of the stability circles (when starting from the a stable area), when changing frequency. The source stability circles are normalized with 50 Ω and the source impedance will be $Z_S = 50\,\Omega$ for all frequencies. The load stability circles are normalized with 8.75 Ω, which is the wanted resistive part of the output load (R_s). This means that, in band, with reactive tuning, the load presented to the output of the transistor will move along the upper half of the $Z/Z_0 = 1$ reactance line in figure 3.8a. Thus, the transistor will be completely stable if the output network doesn't present any load that will make the reflection coefficient cross any stability circles out of the band. It should be remembered that each stability circle represents one frequency, which means that each frequency has its own unstable area of impedances (all conditionally stable frequencies). The actual output network will be somewhat lossy and will improve stability a bit.

The shunt resistor in the stability network is a good branch to use as gate bias feed. Since, only a very small current will flow through the gate of the transistor, a resistor is good for blocking RF without introducing a voltage drop (if the resistance is not too large). After the bias resistor, a capacitor to ground and a series inductor was added. The capacitor presents low impedance for RF and inductor presents high impedance for RF, which makes the circuit independent of whatever impedance the DC feed (the power supply unit) will present.

3.4.2 Input matching

Source pull simulations were performed with the desired output network, i.e. the one in figure 2.15. Since the output load varies with both power and frequency, the source pull simulations were performed with the "average" load at the output, i.e. when $R_s = 8.85\,\Omega$, $C_{ds} = 5.5$ pF and $L_s = 3.7$ nH. First, the the optimum fundamental source load was found, when all higher



(a) Fundamental source reflections, normalized to 50 Ω.

(a) Second harmonic source reflections, normalized to 50 Ω.

Figure 3.10: The wanted and simulated source reflections, together with PAE contours. The wanted reflections almost coincide for the band frequencies, therefore only the wanted reflection for the center frequency is plotted. The simulated reflection is plotted from 1.7 GHz to 5 GHz.

harmonics were short circuited. Then, the optimum second harmonic source load was found, with the optimum fundamental source load and short circuited higher harmonics. Then, a new optimum fundamental source load was found, with the optimum second harmonic source load and all higher harmonics short circuited. This procedure was repeated until the first and second harmonic impedances had converged.

In figure 3.10, Power Added Efficiency (PAE) contours for the optimum first and second harmonic source loads are presented. The P_{out} contours were very similar to the PAE contours and were therefore excluded from the plots.

When studying the efficiency enhancement in OPBO in large signal simulations, the importance of the termination of the second input harmonic was discovered. When designing the input matching network, it appeared that it is more important to have a suitable termination for the second harmonic load than it is to have a good match for the fundamental load in order to have high efficiency when the transistor is backed off. The importance of the second harmonic source termination is discussed in [15] and [16], where it is noted that the correct second harmonic source termination gives beneficial waveforms at the output.

The actual source termination was achieved with a transmission line impedance transformer and a shunt capacitance, see figure 3.5. The reflection from the complete input network (stability network, harmonic termination and impedance transformer) can be seen in figure 3.10.

3.4.3 Input layout

The layout of the complete input network can be seen in figure 3.11. The transistor is placed on a ridge at the right side of the input network. The input network is connected to the transistor by gold bond wires. All components from the schematic of the input is connected with transmission

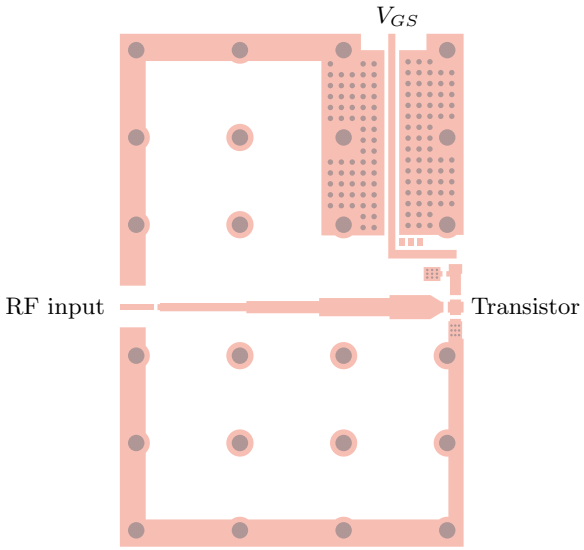


Figure 3.11: The layout of the input network of the transistor.

lines. The bond wires and transmission lines introduce unwanted impedance shifts that made the input matching more difficult, especially for the second harmonic that should be close to short circuited. The large circles represent holes for screw connections (to connect the PCB to a fixture). The other circles are via holes to ground.

3.5 Output network

3.5.1 Output matching

A schematic of the output network is presented in figure 3.12. The transistor is biased through an inductor, a shunt capacitor and another series inductor. This branch works in the same way as the DC feed discussed in section 3.4, except that a resistor cannot be used since there will be a large current flowing through the drain of the transistor. The varactors are biased with a separate DC feed. In order to introduce the same voltage over the two anti-series varactors, a DC feed with the same voltage as the drain of the transistor is placed next to the second varactor. The resistive matching is achieved with a transmission line impedance transformer.

The simulated load modulation (power sweep with the optimum varactor voltage for the complete circuit) for the center frequency and band limits can be seen in figure 3.13. From theory (figure 2.14a), the PA should have good performance for a fractional bandwidth of 36%, i.e. f from 1.75 GHz to 2.53 GHz. The final simulated circuit has efficiency enhancement for a fractional bandwidth of 21%, i.e. f from 1.92 GHz to 2.36 GHz. Thus, from here on, the band limits will be defined as 1.92 GHz and 2.36 GHz. The simulated load modulation shows that the resistive part of the output load is also modulated, and that the resistive part of the load does not start at $Rs = 0.5R_{opt}$. Even though the load modulation isn't purely reactive, the complete circuit still has high efficiency when the transistor is backed off, which will be discussed in more detail later in this chapter. The resistive part of the modulation is due to all the parasitics in all components in the output network. All components together with all the parasitics will introduce a complex load that resonates at several frequencies. The simulated load modulation and its correlation to the theory will be discussed in detail later on in this chapter.

Since the load modulation consists of both reactive and resistive tuning, it becomes harder to provide an output network that enables good performance over a large band. The farther away from the center frequency, the farther away from the optimum trajectory of the load modulation in the PAE and P_{out} contours the load modulation will be, which degrades the bandwidth

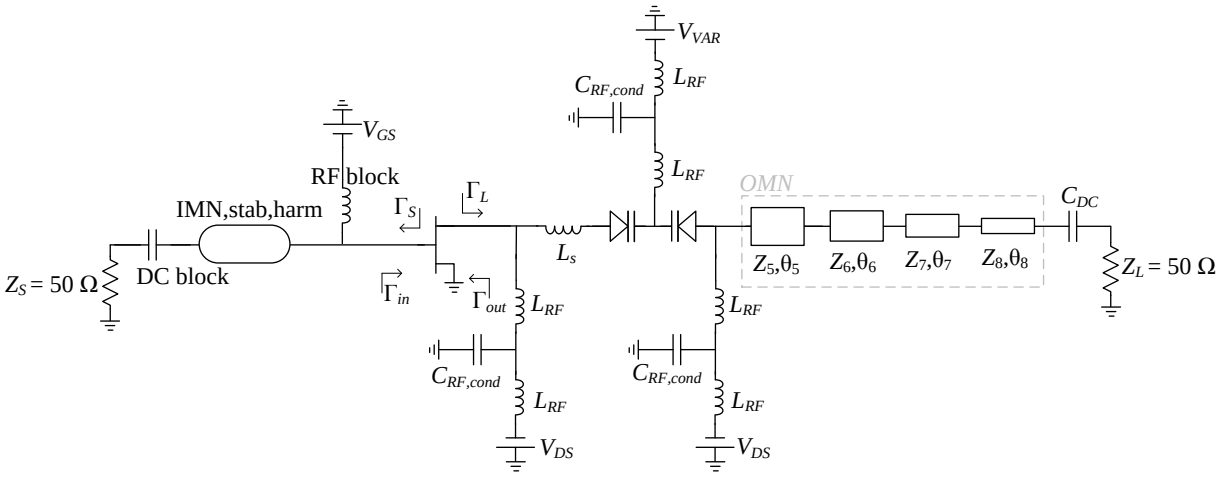


Figure 3.12: A schematic of the output network of the transistor, including biasing- and matching networks.

performance a lot.

The simulated load modulation (for the complete circuit) for the second harmonics are plotted in figure 3.13. It can be seen that higher frequencies are further away from open circuit, which also may limit the bandwidth performance.

3.5.2 Output layout

The layout of the complete output network can be seen in figure 3.14. The transistor is placed on a ridge at the left side of the output network, where the transistor is connected with gold bond wires. The varactors are also placed on ridges and are connected with gold bond wires.

3.6 Circuit simulations

A schematic of the complete circuit can be seen in figure 3.15; a detailed schematic including values can be found in appendix A.

CW simulations were made by sweeping the input power for different varactor voltages. The PAE for $f = 2.14\,\text{GHz}$ can be seen in figure 3.16. A scatter plot of all combinations is plotted in grey and the outline, i.e. the combinations that gives the best results, is plotted in blue. The PAE outlines for $f = 1.92\,\text{GHz}$, $2.14\,\text{GHz}$ and $2.36\,\text{GHz}$ can be seen in figure 3.17. The PAE is higher than 50% down to 5 dB OPBO over a 21% fractional bandwidth.

The corresponding varactor voltages during the best performance are plotted as a function of the output power in figure 3.18. The varactor voltage is tuned from 6 to 66 V over the band. The lowest value of the voltage over the varactors is 6 V in order to avoid forward bias of the varactors due to high RF swing.

The corresponding gain during the best performance is plotted in figure 3.19. The small signal gain is 14.7 dB for $f = 1.92\,\text{GHz}$, 13.4 dB for $f = 2.14\,\text{GHz}$ and 12.1 dB for $f = 2.36\,\text{GHz}$. Since the PA needs an additional control signal for the varactor voltage, Digital Pre-Distortion (DPD) that takes care of the non linear gain must be included.

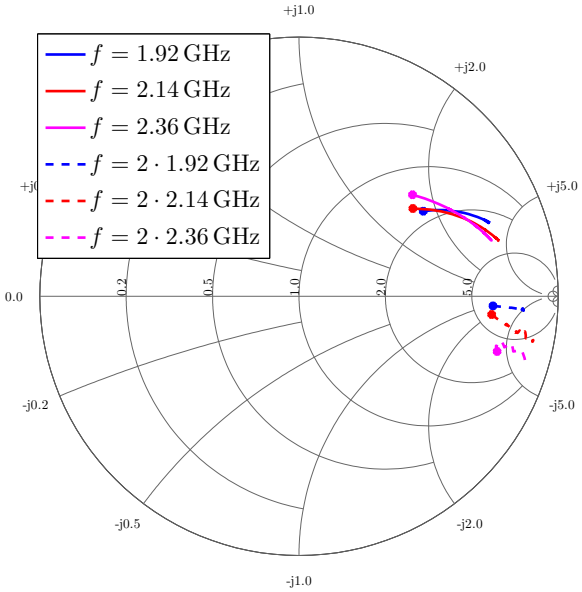


Figure 3.13: A demonstration of the load modulation for the complete circuit (a power sweep with the optimum varactor voltage). Γ_{out} for three frequencies in the band with their corresponding second harmonic, normalized to $8.75\,\Omega$ is plotted. The dot represents maximum output power, and the following line represents the load modulation when the output power is backed off.

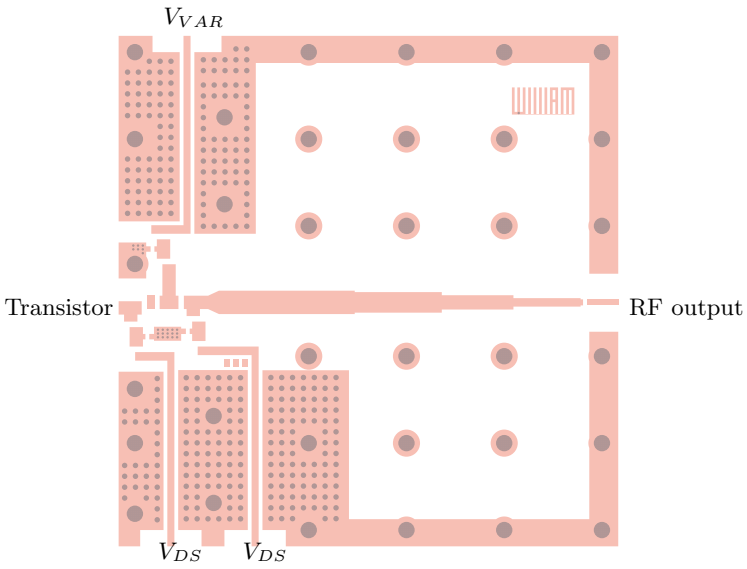


Figure 3.14: The layout of the output network of the transistor.

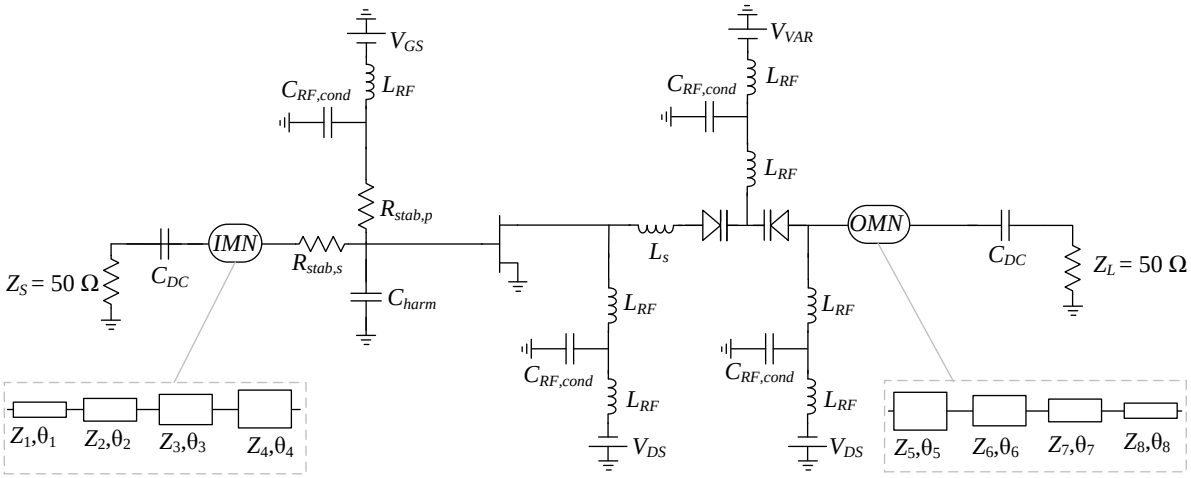


Figure 3.15: A schematic of the complete circuit.

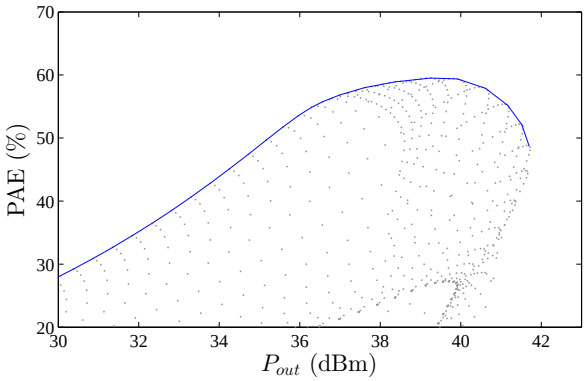


Figure 3.16: A scatter plot of all varactor and input power combinations is plotted in grey and the outline is plotted in blue for $f = 2.14\,\text{GHz}$.

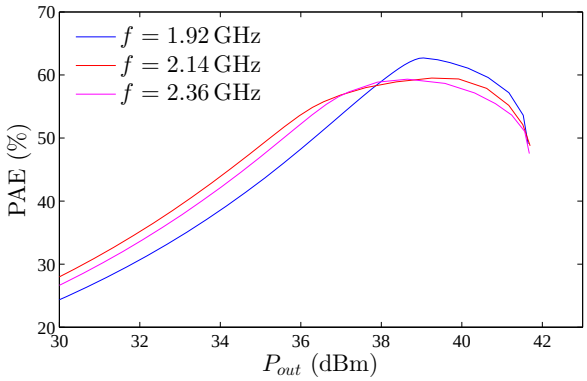


Figure 3.17: PAE as a function of output power

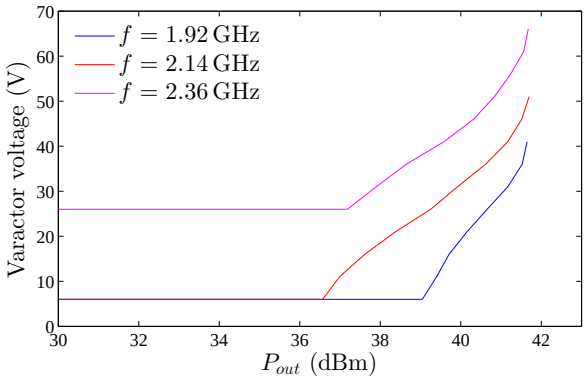


Figure 3.18: Varactor voltage as a function of output power.

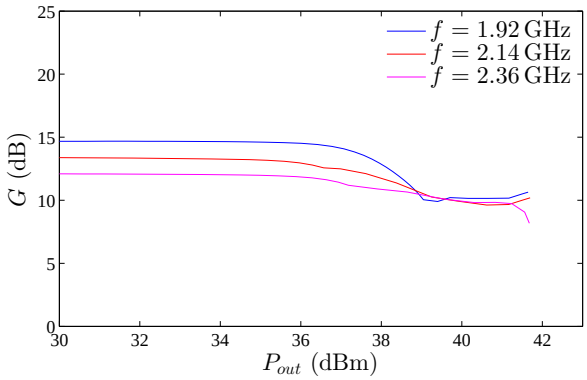
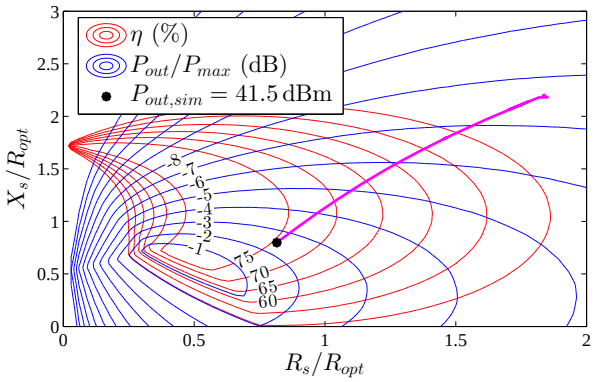


Figure 3.19: Gain as a function of output power.

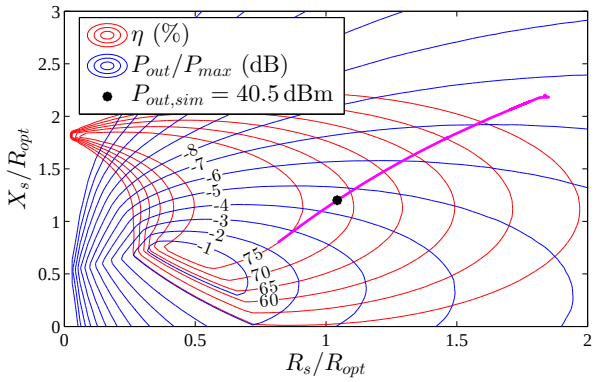
3.7 Load modulation

The correlation between the theory and the simulated results is demonstrated by comparing the simulated load modulation with the efficiency and output power contours. The simulated load modulation for $f = 2.14\,\text{GHz}$ is plotted on the theoretical PAE and P_{out} contours in figure 3.23. The load modulation is plotted for the simulated $P_{out} = 41.5$, 40.5, 38.5 and 36.5 dBm, where each power level corresponds to different ${}^{X_{C_{ds}}}/_{R_{opt}}$ ratio (since the C_{ds} is nonlinear), thus different contours. The contours suggest that the maximum simulated P_{out} is 2 dB lower than the maximum theoretical P_{out}. This is not accurate since the maximum output power of the transistor is 15 W, i.e. 41.8 dBm (from the transistor data sheet) and the maximum output power from the simulation is 41.7 dBm. The drain efficiency from the contour plots and the drain efficiency from the simulations are plotted in figure 3.24. The plots have a strong correlation, except at maximum drive level, where the transistor is compressed and presents strong non linear behaviour.

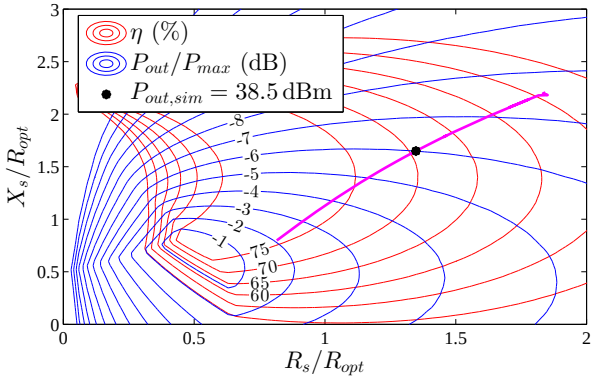
In conclusion, this design method gives enhanced efficiency performance when the transistor is backed off. The result differs somewhat from the theory: in theory, the drain efficiency is higher than 70% down to 8 dB OPBO over a fractional bandwidth of 36%, in the simulations, the PAE is higher than 50% down to 5 dB OPBO over a bandwidth of 21%. However, there is a strong correlation between the theory and the simulated results, which means that this theory and design method could be very useful.



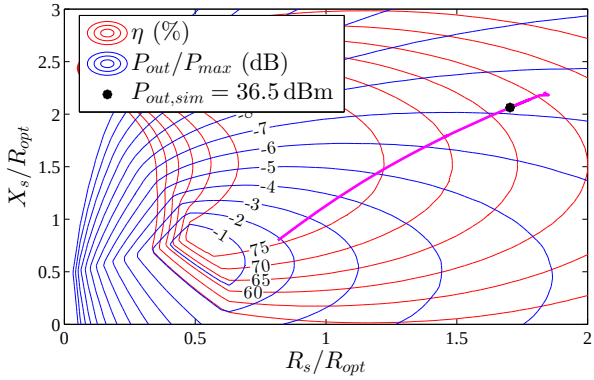
(a) $X_{C_{ds}}/R_{opt} = 1.72$.



(a) $X_{C_{ds}}/R_{opt} = 1.82$.



(a) $X_{C_{ds}}/R_{opt} = 2.23$.



(a) $X_{C_{ds}}/R_{opt} = 2.44$.

Figure 3.23: The load modulation for $f = 2.14$ GHz with corresponding contour plots for the simulated $P_{out} =$ 41.5, 40.5, 38.5 and 36.5 dBm. The black dot corresponds to the output power which $X_{C_{ds}}$ has been calculated for (which gives the contour plots). The purple line represents the load modulation.

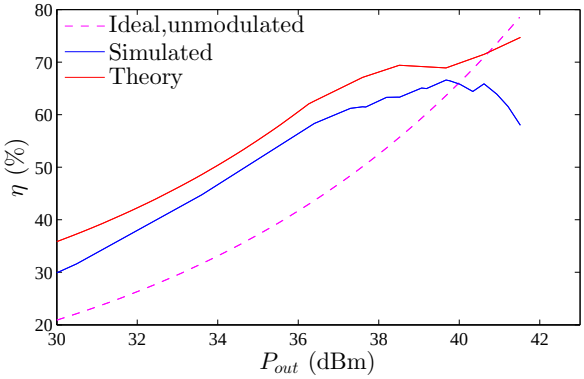


Figure 3.24: The simulated, expected from theory and unmodulated drain efficiency. The expected η corresponds to the simulated trajectory of the load in the contour plots.

Chapter 4

Measurements

A picture of the fabricated and assembled PA can be seen in figure 4.1. Measurements on the amplifier were done in two parts. First CW measurements were done, where the input power was swept for different varactor biases at different frequencies. From the CW measurements, the varactor bias control for optimum efficiency performance was extracted and then used in modulated measurements. Each measurement part, together with the obtained results, are presented in detail in this chapter.

4.1 Continuous wave measurements

The CW measurements were performed with a Large Signal Network Analyser (LSNA) (Maury Microwave Corporation MT4463), where the forward and backwards voltage waves at the input and output from the Device Under Test (DUT) were decoupled and then measured by the LSNA. In order to reach the desired input power to the DUT, a preamplfifer was added after the signal source. Before the measurements, the setup was calibrated with the SOLT (Short Open Line Through) method. A schematic of the measurement setup can be seen in figure 4.2.

The input power to the DUT was swept for a number of different varactor voltages, a scatter plot of the PAE for these sweeps can be seen in figure 4.3 for $f = 1.75\,\text{GHz}$. It can be seen that for 8 dB OPBO, the PAE has been improved from 23% to 37% for the optimum varactor voltages. Sweep measurements were done for different frequencies, the outlines of these, i.e. the best efficiency performances, for the PAE and gain are plotted in figure 4.4 and 4.5. The corresponding voltages over the varactors that enables this performance are plotted in figure 4.6. To avoid forward biasing of the varactors due to high RF swing, the voltage over the varactors was never set below 7 V (too high forward bias may break the varactors).

The center frequency for the simulated circuit is 2.14 GHz and the measured center frequency is 1.75 GHz, a frequency shift of about 0.4 GHz, i.e. an offset of about 18%. The bandwidth in the simulations is 21%, in the measurements, it has decreased to 6%. During the simulations, it was seen that the design is very sensitive to small variations. From the performance contour plots in figure 2.12, it can be seen that a slight offset the load trajectory can cause a very different performance behaviour. In figure 3.13, it was demonstrated that the load modulation differed a bit for the different design frequencies and it was discussed that it was difficult to map load trajectories that gave good performance over a wide bandwidth. It is reasonable to believe that there is an offset of the load trajectories, which is decreasing the wideband performance and the maximum output power.

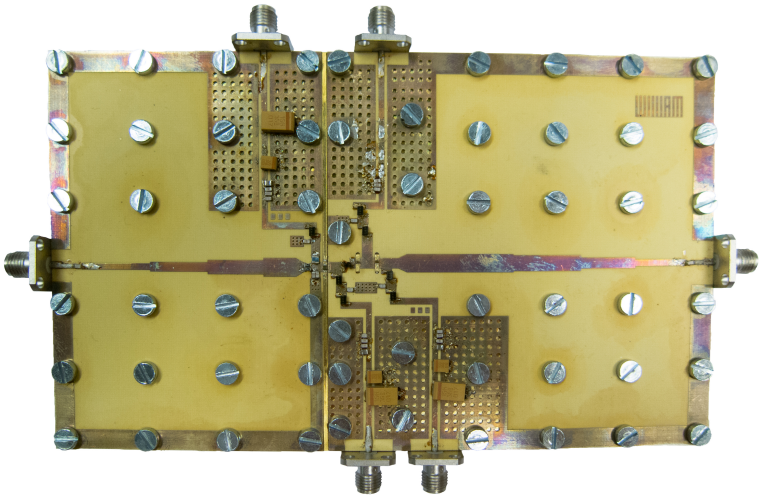


Figure 4.1: Picture of the power amplifier.

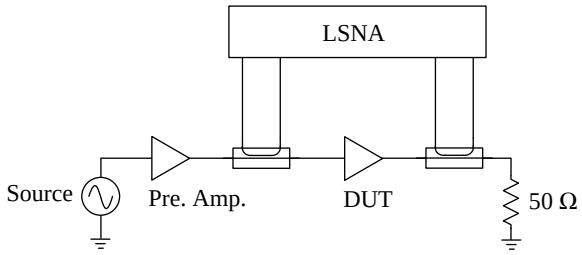


Figure 4.2: Measurement setup for CW measurements.

Furthermore, it was discussed that the second input harmonic termination was crucial for good performance. Since the second harmonics are at double the frequencies compared to the fundamentals, they are twice as sensitive to any kind of offset. An offset of the second input harmonic termination may also contribute to the difference between the simulated and measured results.

Despite the frequency offset, the PAE is over 50% for 1.70 to 1.80 GHz, a fractional bandwidth of about 6%, down to 5 dB OPBO, with the maximum output power of 40.4 dB. The small signal gain is about 13.5 dB and at maximum power it is about 10.5 dB, which is similar to the simulated gain for 2.14 GHz (the center frequency of the simulated results). The behaviour of the measured gain versus output power is also very similar to the simulated gain. The voltage over the varactors is tuned from 7 to 47 V, i.e. a total tuning of 40 V, which is close to the simulated voltage tuning range at each frequency separately. In the simulations, the lowest varactor voltage for the different frequencies varies. In the measurements, the lowest value is the same for all frequencies, which might suggest that even lower varactor voltage could be beneficial, which is equivalent to a higher effective capacitance from the varactors.

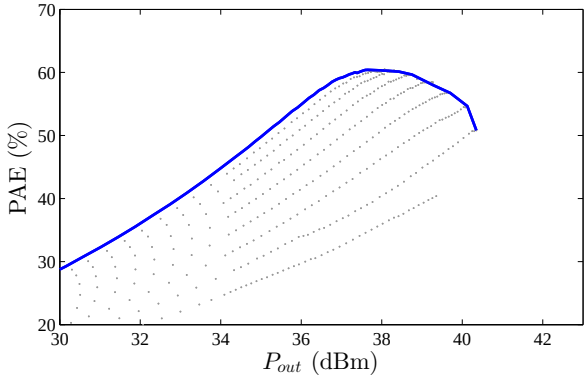


Figure 4.3: A scatter plot of the input power sweeps for different varactor voltages is plotted in grey and the outline is plotted in blue for CW measurements.

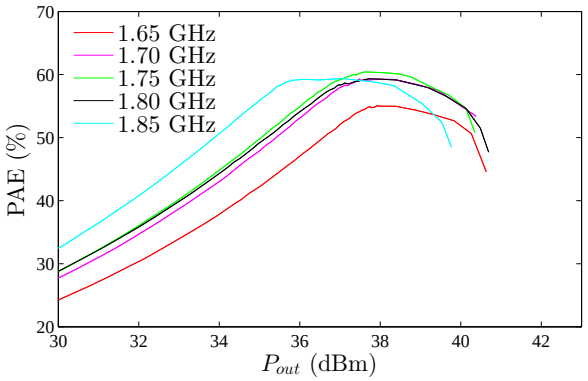


Figure 4.4: PAE as a function of output power for CW measurements.

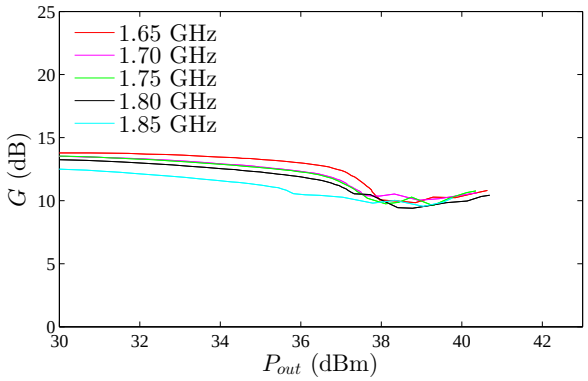


Figure 4.5: Gain as a function of output power for CW measurements.

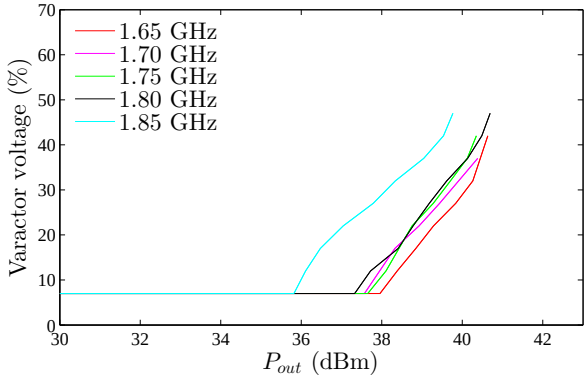


Figure 4.6: Varactor voltage as a function of output power for CW measurements.

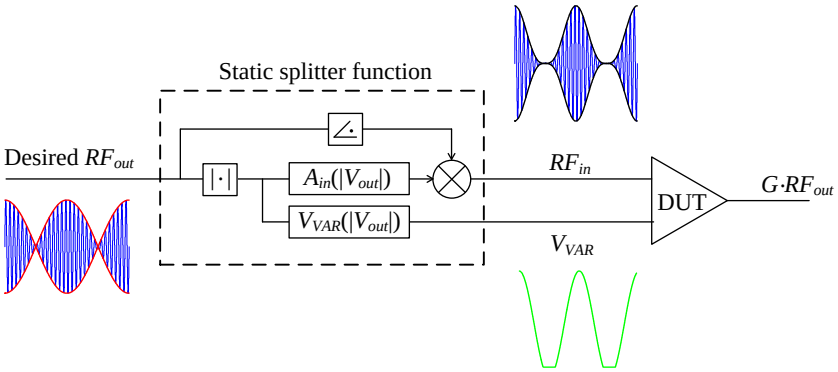


Figure 4.7: Schematic of the static spitter function.

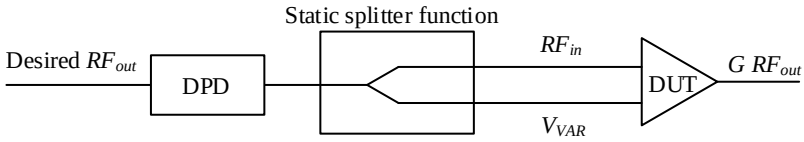


Figure 4.8: Schematic of the static spitter function together with a DPD.

4.2 Modulated measurements

At the input of the PA, a static splitter function splits the the input signal into two branches: a linearized RF signal for the RF input and a varactor control signal. The amplitude of the RF input signal is linearized by a multiplication with the inverse of the PA's output amplitude as a function of its input amplitude. The phase of the RF input remains unchanged.

From the CW measurements, the optimum varactor voltage control as a function of the output power is extracted. That relation together with the PA's output amplitude as a function of its input amplitude enables the static splitter to extract the varactor control signal from the input. A schematic of the functionality of the static spitter function can be seen in figure 4.7.

Since the linearization in the static splitter function does not compensate nonlinear phase, and due to small delay errors between the RF input to the DUT and the varactor control signal being able to cause severe nonlinearities [17], DPD is needed. With the static splitter function included as a part of the DUT, the circuit can be seen as a normal two port amplifier, which enables conventional DPD. A schematic of the setup with DPD can be seen in figure 4.8.

A schematic of the implementation of the complete measurement setup for modulated measurements can be seen in figure 4.9. The DPD and the static splitting function is implemented in MATLAB, i.e. in the digital domain. The modulated signal is generated by the pattern generator module TSW3100 by Texas Instruments, which contains Digital to Analog Converters (DACs) and In-phase and Quadrature (IQ) modulators. These modulators are driven by a external local oscillator and the TSW3100 module is clocked by an external clock. The varactor bias control is generated by an Arbitrary Waveform Generator (AWG) (Tabor Electronics WW2572A), clocked with the same external clock. The varactor control signal is amplified to the right levels with an operational (OP) amplifier. The varactor control signal and the input and output power of the DUT are monitored with an oscilloscope (Rohde Schwarz RTO1044). Before the measurements, the power level for the input and output of the DUT and the oscilloscope were

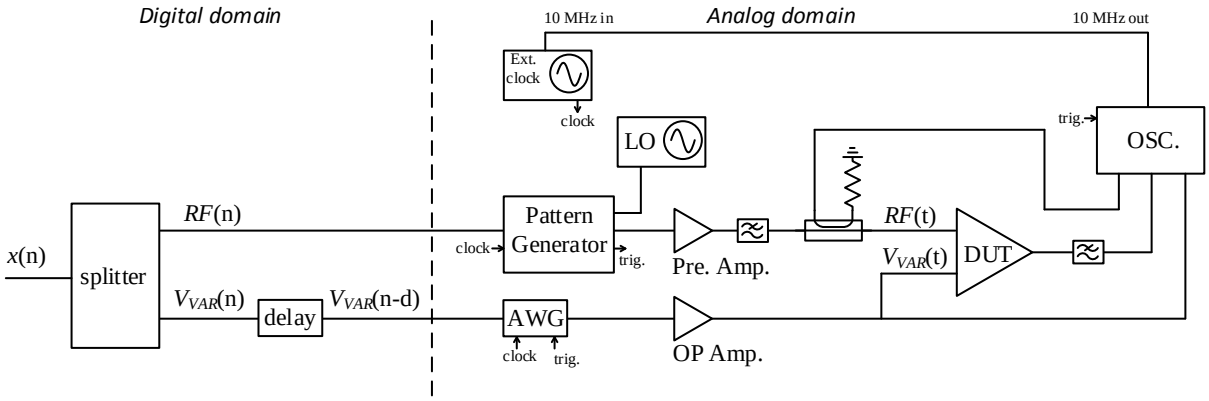


Figure 4.9: Measurement setup for modulated measurements.

calibrated with a power meter, and the RF signal and varactor control signal were synchronized by delaying one of the channels. The synchronization was measured with the oscilloscope. The DPD algorithm utilizes a vector switched generalized memory polynomial (VS-GMP) behaviour model with a nonlinear order of 3, a memory depth of 4, a lagging term of 2, for 16 regions [18].

Modulated measurements were done with a 3.84 MHz 6.6 dB PAPR W-CDMA signal at 1.75 GHz. The normalized power spectral density of the output signal of the DUT with and without DPD (i.e. with the PA and static splitter function) can be seen in figure 4.10. The DUT presents excellent linearity: an Adjacent Channel Leakage Ratio (ACLR) of -48 dB and a Normalized Mean Square Error (NMSE) of -38.3 dB for the output signal after DPD. The AM-AM and AM-PM responses of the DUT with and without DPD are shown in figure 4.12. The DUT provides an average output power of 33.1 dBm, which is a bit lower than the maximum possible in order to achieve the optimum DPD results. The DUT has an average PAE of 44.9% and an average gain of 12.7 dB, which agrees well with the CW measurements.

The results from the CW and modulated measurements are summarized in table 4.1. In the table, the results are compared with the measurement results from other published varactor based DLM PAs [8], [9], [10]. In [8], a GaN HEMT PA utlizing the a single frequency version of the theory in this work, operating at 2.08 GHz, CW measurements are presented. In [9], a varactor based DLM PA using the same transistor, operating at 2.65 GHz, CW measurements and modulated measurements for a 3.84 MHz 7 dB PAPR W-CDMA signal are presented. In [10], a varactor based DLM PA using a GaN HEMT transistor, operating at 1.0 to 1.9 GHz, CW measurements are presented.

The PA in this work achieves a bit higher PAE at 5 dB OPBO than the PA in [8]. The PA in [9] achieves a bit higher PAE at 5 dB OPBO and a bit higher average PAE, but it achieves 2.7 dB lower average output power. However, the PA in [9] utilizes a load-pull based design, while the design of this work is based on a thorough theory. The PA in [10] achieves higher efficiency over a wideband for CW measurements, this PA is also based on a load-pull based design method.

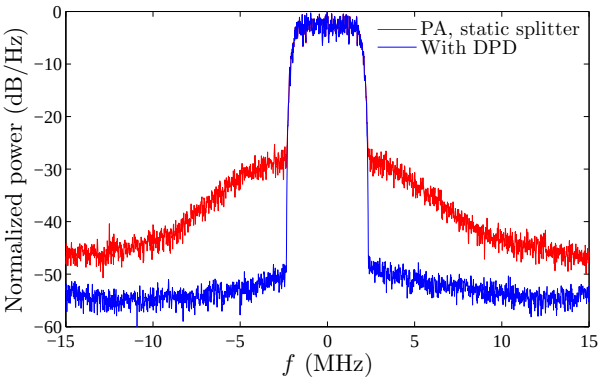
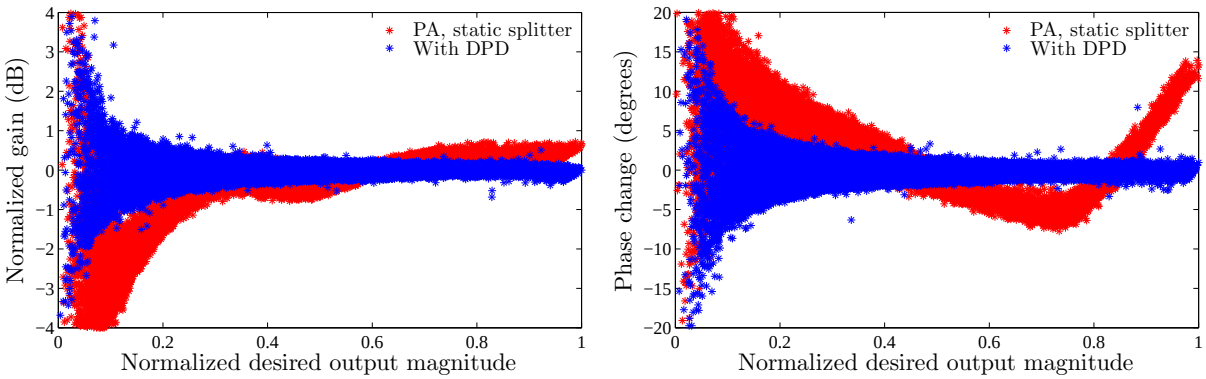


Figure 4.10: Normalized power spectral density of the output signal.



(a) AM-AM response.

(a) AM-PM response.

Figure 4.12

Table 4.1: Summary of the results from the CW and modulated measurements and a comparison with other published varactor based DLM PAs.

	[8]	[9]	[10]	This work
f (GHz)	2.08	2.65	1.0–1.9	1.7–1.8
Peak power (dBm)	38	39	39.6–40.2[a]	40.4–40.5
PAE @ 5 dB OPBO (%)	47.5 [a]	53.4[a]	45–60[a]	50.2–51.4
PAE^{b}_{avg} (%), PAPR^{b} (dB)	N/A	49, 7	N/A	44.9[c], 6.6
$P^{b}_{del,avg}$ (dBm)	N/A	30.4	N/A	33.1[c]
ACLR^{b} (dBc)	N/A	-45	N/A	-48.0[c]
NMSE^{b} (dB)	N/A	-35	N/A	-38.3[c]

[a] Read from graph.

[b] For a 3.84 MHz W-CDMA signal after DPD.

[c] For 1.75 GHz.

Chapter 5

Conclusions and future work

5.1 Conclusions

In this thesis, a theory for wideband, high efficiency class-J PAs has been presented. A demonstrator, with good simulation results that have high correlation to the theory have been presented and discussed. Furthermore, this demonstrator has been implemented in a hybrid design. The measured results are shifted in frequency and the performance is reduced compared to the simulated results.

Since the simulations agrees well with theory, it seems that this design method is useful. However, with the chosen topology for the demonstrator, it proved to be hard to achieve the theoretical optimum performance. With this topology, the simulated bandwidth is degraded from the theoretical 36% to 21%. Since the measured results differs from the simulated results, it seems like a slight offset of the load trajectories can degrade the performance a lot. The chosen topology appears to be very sensitive to small variations in the impedances of the input and output networks.

Despite the difference between simulation and measurements, the demonstrator achieved a PAE over 50% for 1.70 to 1.80 GHz (a fractional bandwidth of 6%) down to 5 dB OPBO with the maximum output power of 40.4 dBm for CW measurements. For modulated signals, the demonstrator showed excellent linearity and high efficiency. For a 3.84 MHz 6.6 dB PAPR W-CDMA signal at 1.75 GHz, the demonstrator achieved an ACLR of -48 dB, an average PAE of 44.9% and an average power of 33.1 dBm.

Even though the demonstrator did not achieve the best performance compared to other published varactor based DLM PAs, this work is the only design that is based on a thorough theory that predicts high efficiency over a wide band. Theoretically, this method should be able to achieve better performance than other published varactor based DLM PAs.

5.2 Future work

It would be interesting to review the topology of the demonstrator. Perhaps there is a less sensitive topology that is able to utilize the full performance from the theory. If the optimum load trajectories is achieved during the load modulation, a very high efficiency operation would be maintained over a wide band.

The varactors in a DLM PA may also be used to compensate antenna mismatch, making it interesting to investigate this method and other varactor based DLM methods further in the future. A varactor that both enhances efficiency and compensates antenna mismatch may enable very good overall performance for a complete transmitter.

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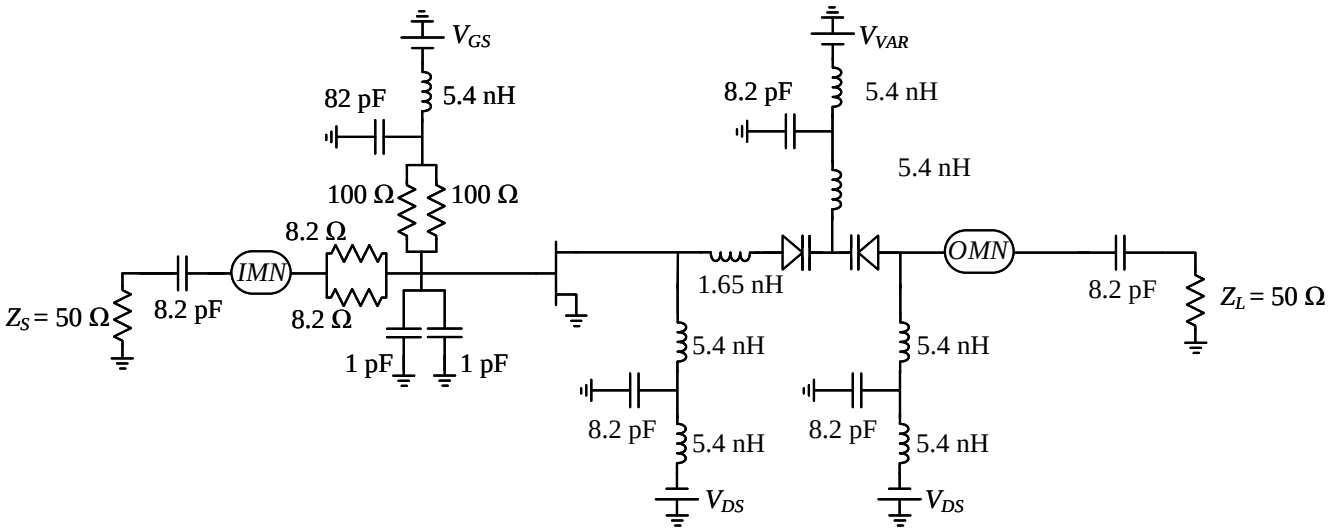
Appendix A

Detailed schematic and layout



Detailed schematic.

Appendix B

Roges 4350 data sheet

ROGERS CORPORATION

Data Sheet

Property	Typical Value		Direction	Units	Condition	Test Method
	RO4003C	RO4350B				
Dielectric Constant, ε_r Process	3.38 ± 0.05	[2]3.48 ± 0.05	Z	--	10 GHz/23°C	IPC-TM-650 2.5.5.5 Clamped Stripline
[1] Dielectric Constant, ε_r Design	3.55	3.66	Z	--	8 to 40 GHz	Differential Phase Length Method
Dissipation Factor tan, δ	0.0027 0.0021	0.0037 0.0031	Z	--	10 GHz/23°C 2.5 GHz/23°C	IPC-TM-650 2.5.5.5
Thermal Coefficient of ε_r	+40	+50	Z	ppm/°C	-50°C to 150°C	IPC-TM-650 2.5.5.5
Volume Resistivity	1.7 X 10^{10}	1.2 X 10^{10}		MΩ•cm	COND A	IPC-TM-650 2.5.17.1
Surface Resistivity	4.2 X 10^{9}	5.7 X 10^{9}		MΩ	COND A	IPC-TM-650 2.5.17.1
Electrical Strength	31.2 (780)	31.2 (780)	Z	KV/mm (V/mil)	0.51mm (0.020")	IPC-TM-650 2.5.6.2
Tensile Modulus	19,650 (2,850) 19,450 (2,821)	16,767 (2,432) 14,153, (2,053)	X Y	MPa (ksi)	RT	ASTM D638
Tensile Strength	139 (20.2) 100 (14.5)	203 (29.5) 130 (18.9)	X Y	MPa (ksi)	RT	ASTM D638
Flexural Strength	276 (40)	255 (37)		MPa (kpsi)		IPC-TM-650 2.4.4
Dimensional Stability	<0.3	<0.5	X,Y	mm/m (mils/inch)	after etch +E2/150°C	IPC-TM-650 2.4.39A
Coefficient of Thermal Expansion	11 14 46	10 12 32	X Y Z	ppm/°C	-55 to 288°C	IPC-TM-650 2.4.41
Tg	>280	>280		°C DSC	A	IPC-TM-650 2.4.24
Td	425	390		°C TGA		ASTM D3850
Thermal Conductivity	0.71	0.69		W/m/°K	80°C	ASTM C518
Moisture Absorption	0.06	0.06		%	48 hrs immersion 0.060" sample Temperature 50°C	ASTM D570
Density	1.79	1.86		gm/cm^3	23°C	ASTM D792
Copper Peel Strength	1.05 (6.0)	0.88 (5.0)		N/mm (pli)	after solder float 1 oz. EDC Foil	IPC-TM-650 2.4.8
Flammability	N/A	[3]V-0				UL 94
Lead-Free Process Compatible	Yes	Yes				

NOTES:
(1) The design Dk is an average number from several different tested lots of material and on the most common thickness/s. If more detailed information is required, please contact Rogers Corporation or refer to Rogers' technical papers in the Rogers Technology Support Hub available at http://www.rogerscorp.com/acm/technology.
(2) Dielectric constant typical value does not apply to 0.004" (0.101mm) laminates. Dielectric constant specification value for 0.004" RO4350B material is 3.33 ± 0.05.
(3) RO4350B LoPro™ laminates do not share the same UL designation as standard RO4350B laminates. A separate UL qualification may be necessary.

Typical values are a representation of an average value for the population of the property. For specification values contact Rogers Corporation.

RO4000 LoPro laminate uses a modified version of the RO4000 resin system to bond reverse treated foil. Values shown above are RO4000 laminates without the addition of the LoPro resin. For double-sided boards, the LoPro foil results in a thickness increase of approximately 0.0007" (0.018µm) and the Dk is approximately 2.4. The Dk decreases by about 0.1 as the core thickness decreases from 0.020" to 0.004.

Prolonged exposure in an oxidative environment may cause changes to the dielectric properties of hydrocarbon based materials. The rate of change increases at higher temperatures and is highly dependent on the circuit design. Although Rogers' high frequency materials have been used successfully in innumerable applications and reports of oxidation resulting in performance problems are extremely rare, Rogers recommends that the customer evaluate each material and design combination to determine fitness for use over the entire life of the end product.

Advanced Circuit Materials Division
100 S. Roosevelt Avenue, Chandler, AZ 85226
Tel: 480-961-1382 Fax: 480-961-4533 www.rogerscorp.com

ROGERS CORPORATION

Data Sheet

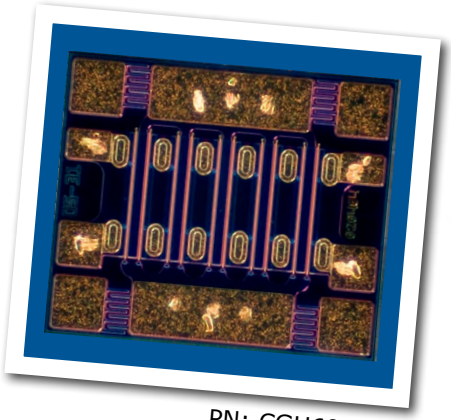
Standard Thickness	Standard Panel Size	Standard Copper Cladding
RO4003C: 0.008" (0.203mm), 0.012 (0.305mm), 0.016"(0.406mm), 0.020" (0.508mm) 0.032" (0.813mm), 0.060" (1.524mm) RO4350B: *0.004" (0.101mm), 0.0066" (0.168mm) 0.010" (0.254mm), 0.0133" (0.338mm), 0.0166" (0.422mm), 0.020"(0.508mm), 0.030" (0.762mm), 0.060"(1.524mm) Note: Material clad with LoPro foil add 0.0007" (0.018mm) to dielectric thickness	12" X 18" (305 X457 mm) 24" X 18" (610 X 457 mm) 24" X 36" (610 X 915 mm) 48" X 36" (1.224 m X 915 mm) *0. 004" (0.101mm) material in not available in panel sizes larger than 24"x18" (610 X 457mm)	½ oz. (17µm) electrodeposited copper foil (.5ED/.5ED) 1 oz. (35µm) electrodeposited copper foil (1ED/1ED) 2 oz. (70µm) electrodeposited copper foil (2ED/2ED) **PIM Sensitive Applications:** ½ oz (17µm) LoPro Reverse Treated EDC (.5TC/.5TC) 1 oz (35µm) LoPro Reverse Treated EDC (1TC/1TC) *LoPro foil is not available on 0.004" (0.101mm)thickness.

Appendix C

Cree CGH60015D data sheet

CGH60015D

15 W, 6.0 GHz, GaN HEMT Die



PN: CGH60015D

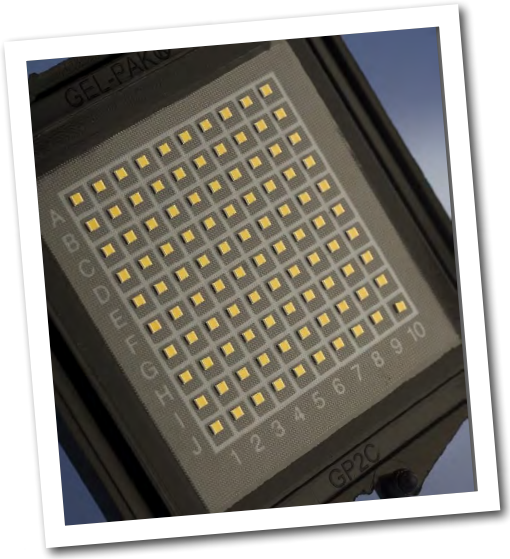
Cree's CGH60015D is a gallium nitride (GaN) High Electron Mobility Transistor (HEMT). GaN has superior properties compared to silicon or gallium arsenide, including higher breakdown voltage, higher saturated electron drift velocity, and higher thermal conductivity. GaN HEMTs offer greater power density and wider bandwidths compared to Si and GaAs transistors.

FEATURES

- 15 dB Typical Small Signal Gain at 4 GHz
- 12 dB Typical Small Signal Gain at 6 GHz
- 15 W Typical P_{SAT}
- 28 V Operation
- High Breakdown Voltage
- High Temperature Operation
- Up to 6 GHz Operation
- High Efficiency

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms



Packaging Information

RoHS COMPLIANT

- Bare die are shipped in Gel-Pak® containers.
- Non-adhesive tacky membrane immobilizes die during shipment.

Large Signal Models Available for SiC & GaN

Absolute Maximum Ratings (not simultaneous) at 25˚C

Parameter	Symbol	Rating	Units	Conditions
Drain-source Voltage	V_{DSS}	84	VDC	25˚C
Gate-source Voltage	V_{GS}	-10, +2	VDC	25˚C
Storage Temperature	T_{STG}	-65, +150	˚C	
Operating Junction Temperature	T_J	225	˚C	
Maximum Forward Gate Current	I_{GMAX}	4.0	mA	25˚C
Maximum Drain Current[1]	I_{DMAX}	1.5	A	25˚C
Thermal Resistance, Junction to Case (packaged)[2]	$R_{\theta JC}$	8.0	˚C/W	
Thermal Resistance, Junction to Case (die only)	$R_{\theta JC}$	5.1	˚C/W	85˚C
Mounting Temperature (30 seconds)	T_S	320	˚C	30 seconds

Note[1] Current limit for long term, reliable operation

Note[2] Eutectic die attach using 80/20 AuSn mounted to a 40 mil thick CuMoCu carrier.

Electrical Characteristics (Frequency = 4 GHz unless otherwise stated; T_C = 25˚C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics						
Gate Threshold Voltage	$V_{GS(TH)}$	-3.8	-3.0	–2.3	V	V_{DS} = 10 V, I_D = 3.6 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.7	–	V_{DC}	V_{DD} = 28 V, I_{DQ} = 100 mA
Drain Current	I_{DS}	2.9	3.5	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BD}	120	–	–	V	V_{GS} = -8 V, I_D = 3.6 mA
On Resistance	R_{ON}	–	1.0	–	Ω	V_{DS} = 0.1 V
Gate Forward Voltage	V_{G-ON}	–	1.9	–	V	I_{GS} = 3.6 mA
RF Characteristics						
Small Signal Gain	G_{SS}	–	15	–	dB	V_{DD} = 28 V, I_{DQ} = 100 mA
Saturated Power Output[1]	P_{SAT}	–	15	–	W	V_{DD} = 28 V, I_{DQ} = 100 mA
Drain Efficiency[2]	η	–	65	–	%	V_{DD} = 28 V, I_{DQ} = 100 mA, P_{SAT} = 15 W
Intermodulation Distortion	IM3	–	-30	–	dBc	V_{DD} = 28 V, I_{DQ} = 100 mA, P_{OUT} = 15 W PEP
Output Mismatch Stress	VSWR	–	–	10 : 1	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 100 mA, P_{OUT} = 15 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	4.1	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	0.9	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.2	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] P_{SAT} is defined as I_G = 0.4 mA.
[2] Drain Efficiency = P_{OUT} / P_{DC}

Cree, Inc.
4600 Silicon Drive
Durham, North Carolina, USA 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
www.cree.com/wireless