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Non-Isolated Battery AC Charging Using CHB Converters

Investigating Leakage Current and Short-Circuit Conditions

Master's Thesis in Sustainable Electric Power Engineering and Electromobility

ERIK BENJAMINSSON

DEPARTMENT OF ELECTRICAL ENGINEERING

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Supervisor: Alireza Norouzzadeh, Volvo Cars
Examiner: Massimo Bongiorno, Department of Electrical Engineering

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Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

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Abstract

The demand for efficient and compact electric vehicle battery chargers has sparked interest in non-isolated charging topologies that eliminate the need for a transformer. This thesis investigates the use of a 31-level grid-connected cascaded H-bridge converter for direct AC battery charging, a concept that integrates the converter into the battery itself and enables bidirectional power flow without galvanic isolation. A simulation model was developed to evaluate the system's behavior with respect to leakage current, touch current, and short-circuit conditions under various grid scenarios. The simulations showed excessive touch current compared to electric vehicle safety standards, which was especially high when using zero-sequence injection. This highlights the importance of minimizing parasitic capacitance. The leakage and touch current were found to be dependent on grid voltages, converter voltages, and modulation scheme. An analytical model was developed to describe the leakage current, yielding results consistent with the simulations. An approximate maximum limit for the total parasitic capacitance of the converter was calculated to be 120 nF. Short-circuit simulations highlighted the importance of grid impedance and R/X-ratio in determining let-through energy and protection requirements.

Keywords: Non-isolated converter, cascaded H-bridge, electric vehicle, battery charging, leakage current, touch current, short circuit, transformer-less, zero-sequence injection.

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Erik Benjaminsson, Gothenburg, September 2025

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

AC	Alternating Current
CHB	Cascaded H-bridge
CM	Common Mode
DC	Direct Current
DDSRF	Decoupled Double Synchronous Reference Frame
DUT	Device Under Test
EMI	Electromagnetic Interference
FFT	Fast Fourier Transform
Li-ion	Lithium Ion
NMC	Nickel Manganese Cobalt Oxide
OCV	Open-Circuit Voltage
PE	Protective Earth
PEN	Protective Earth and Neutral
PFC	Power Factor Correction
PI	Proportional-Integral
PLL	Phase-Locked Loop
PR	Proportional-Resonant
PSCC	Prospective Short-Circuit Current
PWM	Pulse-Width Modulation
RCD	Residual Current Device
RL	Reinforcement Learning
RMS	Root Mean Square
SoC	State of Charge
SRF	Synchronous Reference Frame
TN-C-S	Terra Neutral-Combined-Separate
ZSI	Zero-sequence Injection

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1

Introduction

Efficiency is an important aspect of power electronics that drives the development of new technologies. Higher efficiency not only reduces energy losses and operational costs, but also allows designs to be more compact, lightweight, and cost-effective. In photovoltaic (PV) systems, the transition to non-isolated topologies in grid-connected inverters increased the efficiency of such systems by 1-2% [1]. This increase comes from the exclusion of multiple stages of power conversion needed for the transformer, all of which contribute to power loss. In the electric vehicle industry, battery charging is commonly performed using isolated topologies with structures similar to the one shown in Figure 1.1. Non-isolated battery charging for electric vehicles is therefore a highly interesting topic.

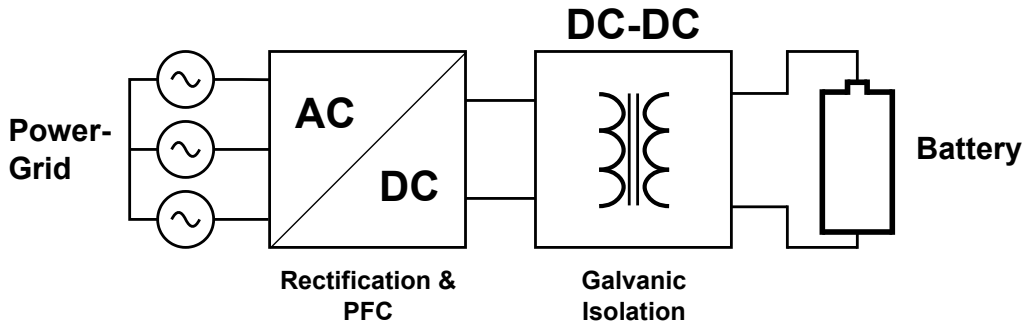


Figure 1.1: The structure of the traditional charging circuitry for electric vehicles.

A multilevel converter known as the cascaded H-bridge (CHB) converter is especially interesting for this purpose, as its modular structure allows it to be integrated into the battery. This essentially turns the car battery into a bidirectional converter that can be connected directly to the power grid during charging. Since the converter can be controlled to produce sinusoidal currents in phase with the grid voltages, the need for a separate power factor correcting (PFC) rectifier is eliminated. The battery can also be used to drive the electric motors, eliminating the need for dedicated electric drives.

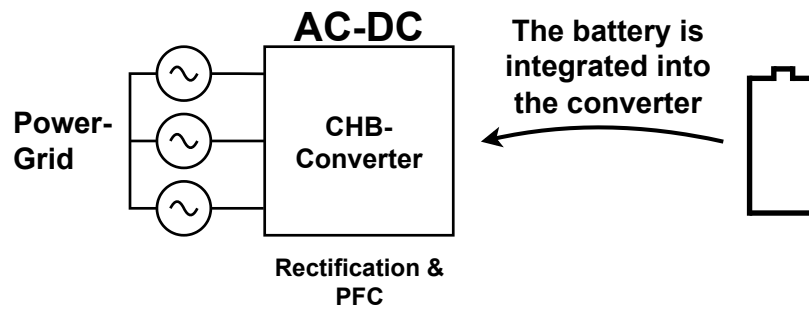


Figure 1.2: The structure of a charging concept utilizing a CHB converter.

Despite the stated benefits, the implementation of non-isolated battery charging in electric vehicles poses some problems. One such problem is that the lack of galvanic isolation in the charger provides a path for leakage current through the parasitic capacitance between the battery and the chassis. If the parasitic capacitance is too high, it can cause excessive leakage current that could trip the residual current device (RCD), or even present as harmful *touch current* if the chassis is touched.

The purpose of this thesis is to implement a model of a 31-level grid-connected CHB converter, and to simulate the leakage and touch current during charging under various power grid conditions. The results will then be compared to existing electric vehicle standards. Some short-circuit conditions will also be investigated to provide information that might be valuable when selecting protective devices.

2

Theoretical Background

This chapter provides the theoretical background necessary to understand the fundamental operating principles of CHB converters. It also explains important aspects of leakage current and short circuits.

2.1 Power Electronic Converters

Historically, transformers played an important role in power conversion as they allowed AC power from the grid to be transformed to different voltage levels. Due to the relatively low frequency of the power grid, the transformers had to be large to avoid core saturation. With the improvement of semiconductor devices, power conversion was made possible by switching at higher frequencies, which reduced the size of transformers and made it possible to use transformer-less topologies. Today, a device that converts one type of electric power to another is known as a power electronic converter. A common type of converter is the two-level converter shown in Figure 2.1, which can convert from DC to AC, and vice versa. The ability to transfer power in both directions makes it a *bidirectional* converter. The transistors are used to switch the outputs V_a , V_b and V_c between $-V_{DC}/2$ and $V_{DC}/2$ (hence the name two-level converter) at a fast rate. Through passive filtering, the voltages can be smoothed to produce any desired output voltage between $-V_{DC}/2$ and $V_{DC}/2$. The 0-volt reference is set to the midpoint of the DC voltage to correspond to the average voltage of the outputs, to act as a neutral point.

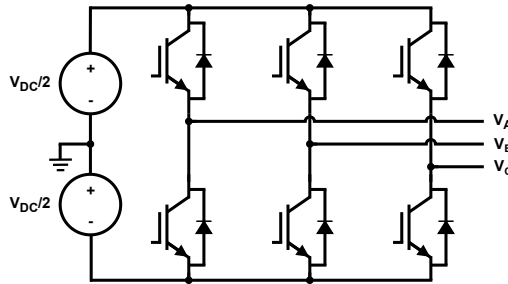


Figure 2.1: A two-level converter using IGBT transistors.

A downside of the two-level converter is that the transistors need to be rated for the full DC voltage. The converter also experiences large changes in voltage (dv/dt), which causes problems such as component stress, parasitic coupling, and electromagnetic interference (EMI). The two-level converter therefore does not scale well to higher voltages, which is desirable for efficiency. An alternative solution is the multi-level converter, which as the name implies divides the available DC voltage into multiple levels that can be switched independently. This reduces component stress and EMI by reducing dv/dt and current ripple [2].

2.2 Cascaded H-bridge Converter (CHB)

The CHB is a multilevel converter that consists of H-bridges connected in series. Each H-bridge is connected to its own DC-source, in this case a battery cell, and together they form a *module*. By using different switching states the DC sources can be selectively chained together to synthesize the desired output voltage. A schematic of the CHB converter is shown in Figure 2.2. The modular structure of the CHB converter allows an almost arbitrary number of H-bridge cells to be connected in series. This makes the converter easily scalable to higher voltages, and the switches only need to be sized in accordance with the DC-source voltage.

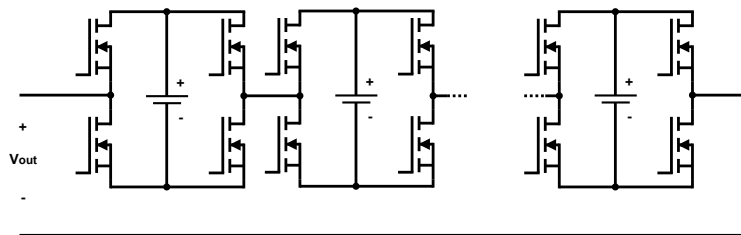


Figure 2.2: A CHB converter.

The operation of the CHB relies on the different switching states of the H-bridge. These are shown in Figure 2.3 with the conduction paths and transistor states highlighted. Each H-bridge can be in four states; positively connected (*a*), negatively connected (*b*), bypassed (*c* or *d*), or disconnected (*e*). Notice that the bypassed state can be achieved in two different ways. The disconnected state is achieved by turning off all transistors, making the entire H-bridge behave like an open switch.

2.2.1 Modulation Techniques

By utilizing the different possible switching states of each submodule, the CHB-converter can produce a set of discrete output voltages [3]. To achieve output voltages in between these values, the submodules must be switched so that the time-

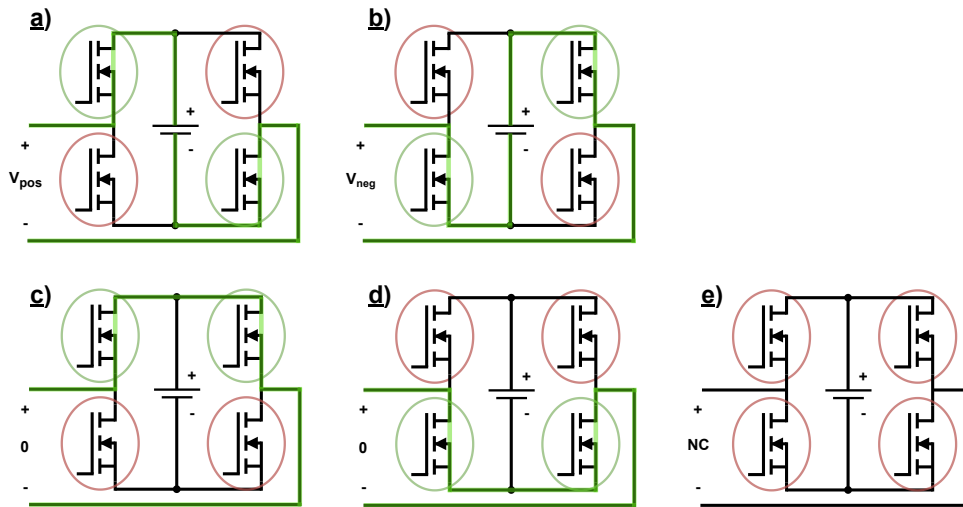


Figure 2.3: The different switching states of the H-bridge.

averaged output voltage equals the reference voltage. The process of determining when and how to switch the transistors in a converter is called modulation. Ideally, the modulator takes a reference voltage (typically from a controller) and switches the transistors in such a way that the averaged output voltage equals the reference voltage.

2.2.1.1 Pulse-Width Modulation

A key modulation technique is known as pulse-width modulation (PWM) [3]. PWM can be understood by analyzing the phase leg of a two-level inverter, shown in Figure 2.4. The reason for placing the 0 volt reference at the mid point of the DC voltage supply is to make it coincide with the average common-mode potential in a three-phase inverter driving a symmetric load. In accordance with this, the output voltage of the phase leg can be either $\frac{V_{DC}}{2}$, or $-\frac{V_{DC}}{2}$. The switching signals for the transistors in the phase leg are determined by comparing the reference voltage to a triangular carrier wave. When the reference voltage is higher than the carrier, the phase leg outputs $\frac{V_{DC}}{2}$, and $-\frac{V_{DC}}{2}$ otherwise. This is illustrated in figure 2.5, where the features have been exaggerated to make it easier to see the important details. In reality, the carrier frequency is often very high compared to the reference voltage, which renders the reference voltage approximately constant throughout a switching period. What this method achieves is an output voltage square wave in which the reference controls the duty cycle

$$D = \frac{T_{on}}{T_c}. \quad (2.1)$$

The average voltage over a switching period is approximately equal to the reference voltage. The ratio between the reference voltage and the maximum output is called

modulation index, m_a , which follows the relationship

$$\hat{v}_{\text{out},1} = m_a \cdot \frac{V_{\text{DC}}}{2}, \quad (2.2)$$

where $\hat{v}_{\text{out},1}$ is the amplitude of the fundamental frequency that the converter is producing [3]. When the voltage reference stays within the possible output range, the modulation index is between -1 and 1, otherwise the phase leg is said to be over-modulated.

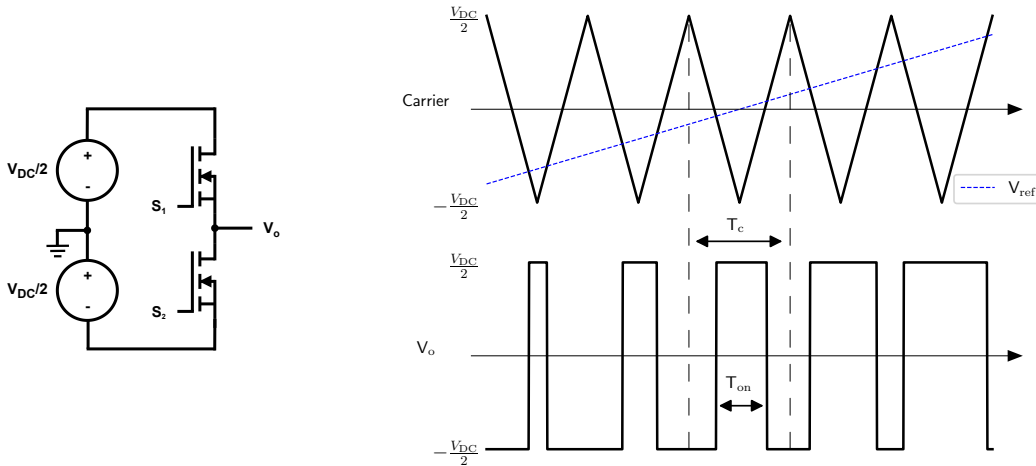


Figure 2.4: Phase leg of a two-level inverter.

Figure 2.5: Carrier- and reference signal on the top and the resulting phase leg output voltage at the bottom.

2.2.1.2 Phase-Shifted Carriers

In order to control series-connected converter modules, multiple carriers need to be generated. One way of doing this is to use phase-shifted carriers [3], where the carriers have an evenly distributed phase-shifts described by

$$\theta_i = \frac{2\pi}{N}(i - 1), \quad \{i = 1, \dots, N\}, \quad (2.3)$$

where θ_i is the phase shift of the i :th carrier, and N is the total number of carriers used. The number of output levels N_{level} of a converter dictates the necessary amount of carriers N_c according to

$$N_c = N_{\text{levels}} - 1, \quad (2.4)$$

which means that for a two-level half-bridge, one carrier is enough. In a CHB-converter however, each module can produce three levels, V_{DC} , 0, and $-V_{\text{DC}}$. Therefore, two carriers are needed per converter module. Figure 2.6 shows the waveforms of a 7-level CHB converter. Six carriers are needed for the three converter modules.

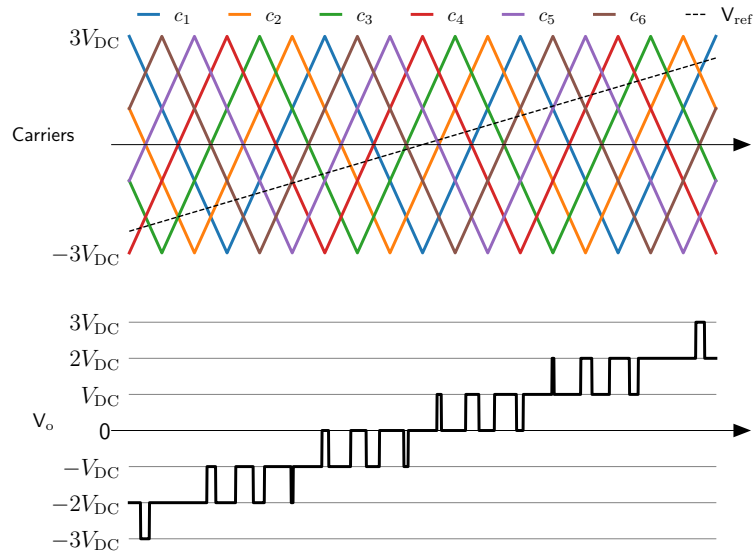


Figure 2.6: Phase-shifted carrier waveforms and corresponding output voltage for a 7-level CHB converter.

2.2.1.3 Level-Shifted Carriers

Level-shifted carrier modulation uses multiple carriers that are shifted in amplitude [3]. The carrier waveforms and the corresponding output of a 5-level converter are shown in Figure 2.7. The carriers in the positive half-plane determine when the modules switch between 0 and V_{DC} , and the carriers in the negative half-plane determine when the modules switch between 0 and $-V_{DC}$. In the carrier-based modulation strategies, the mapping from the carriers to the modules can be made arbitrarily.

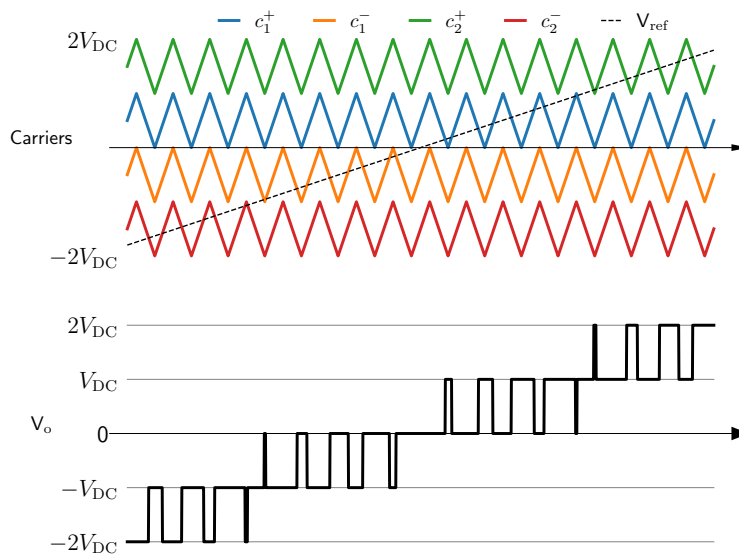


Figure 2.7: Level-shifted carrier waveforms and corresponding output voltage for a 5-level CHB converter.

2.3 Lithium Ion Batteries

The lithium-ion (Li-ion) battery is one of the most common types of rechargeable battery for portable electronics and electric vehicles [4]. The Li-ion cell stores energy through the oxidation and reduction of lithium. In a fully discharged Li-ion cell, most of the lithium exists in its reduced form as a lithium compound in the cathode (positive terminal). There are a number of different lithium compounds that can be used for the cathode, and a common choice for high-energy-density applications is nickel manganese cobalt oxide (NMC). The anode (negative terminal) most commonly consists of graphite, and as the battery charges, the lithium in the cathode oxidizes, creating lithium ions that dissolve and move through the electrolyte into the graphite. When the battery is charged, the graphite is said to be *lithiated*.

2.3.1 Equivalent Electrical Circuit

In order to do simulations with Li-ion batteries, an electrical model is needed. The model should mimic the behavior of the cell, which is largely governed by charge transfer at the electrodes, mass transport through the electrolyte, and ohmic resistance. An important phenomenon that affects the behavior of the cell is the electrical double layer that forms at the boundary between the electrodes and the electrolyte. This layer consists of ionic charges that give it capacitive properties.

The behavior of the Li-ion cell is in large part non-linear, and the cell parameters are dependent on factors such as SoC, temperature, usage pattern, and age. A simplified electrical model can be constructed using a voltage source in series with the ohmic resistance, although such a model may not adequately describe the high-frequency behavior of the cell. The reason for this is that the capacitive behavior of the electrical double layer will provide a low-impedance path for currents during fast voltage transitions. This may be important because the cell model will be used in a switching converter with fast voltage transitions. It may especially be important when performing short-circuit tests, since the short-circuit current should be higher due to capacitive effect. Therefore, an equivalent circuit with two RC networks will be used. The circuit is shown in Figure 2.8 and consists of an ohmic resistance R_0 , two RC networks, and an inductor. The RC networks describe behavior due to charge transfer and the electrical double layer, and the inductor models the inductance of the battery bus bars. The voltage source is a function that maps the battery's state of charge (SoC) to its open-circuit voltage. This function is different depending on the exact Li-ion chemistry that is used, and can also include temperature dependence.

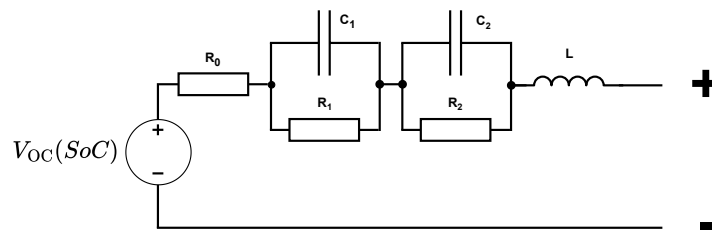


Figure 2.8: A 2RC equivalent circuit model of a Li-ion battery.

2.3.2 Battery Pack Notation

The standard way to communicate the configuration of a battery pack is to put it in the form $XSYP$ where X is the number of cells connected in series and Y is the amount of such series strings that are connected in parallel.

2.4 Power Grid

This section will discuss different configurations and characteristics of the power grid, as well as challenges of connecting it to power electronic converters.

2.4.1 Three-phase Electric Power

The most common way to transfer electric power from producers to consumers is to use a three-phase system. A three-phase transmission system has three conductors with sinusoidal phase voltages that are phase shifted 120 degrees from each other. These voltages can be mathematically expressed as

$$v_a = \hat{V}_a \sin(\omega_1 t + \phi_a) \quad (2.5)$$

$$v_b = \hat{V}_b \sin(\omega_1 t - \frac{2\pi}{3} + \phi_b) \quad (2.6)$$

$$v_c = \hat{V}_c \sin(\omega_1 t + \frac{2\pi}{3} + \phi_c) \quad (2.7)$$

where $\hat{V}_{a,b,c}$ denotes the peak voltage of each phase, ω_1 is the fundamental angular frequency of the grid, and $\phi_{a,b,c}$ is the phase shift of each phase voltage [3]. Producing these quantities is commonly done using generators with windings that are physically displaced with respect to each other, so that the rotor flux naturally induces phase voltages with the desired phase shift. A very common way to describe the three-phase quantities is to use a phasor diagram, shown in Figure 2.9, which encodes amplitude and phase in a more visible format.

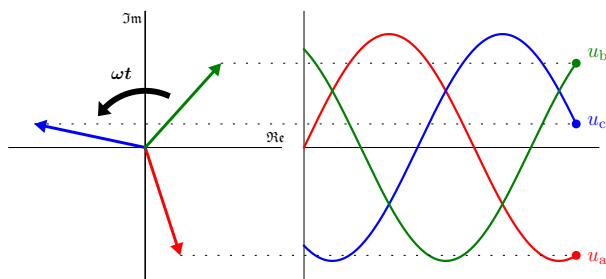


Figure 2.9: Visual interpretation of a three phase phasor diagram.

There are two main ways in which a three-phase load can be connected to a three-phase system: a Y-connection or a Δ -connection [3]. Both of these configurations are shown in Figure 2.10. A, B, and C refer to phase conductors and N is the neutral conductor at 0-volt potential. The neutral conductor is only relevant for the Y-configuration and is not necessary if the impedances are equal, such that $Z_a = Z_b = Z_c$. A load that has this characteristic is said to be balanced. If a Y-configured load is balanced, the total current flowing into the neutral node is zero, eliminating the need for a return conductor. This is one of the main benefits of three-phase electric power, as it makes efficient use of conductor material. Another

benefit is that, unlike in a single-phase system, the total power flow delivered to a balanced three-phase load is constant [5]. This is illustrated in Figure 2.11, which shows the waveforms for a purely resistive load. The power flow for a single phase has double the frequency of the phase voltages and drops to zero at its minimum. Supplying a load from a single-phase supply therefore requires energy storage in the form of large bulk capacitors, which increases cost and reduces the lifetime. In contrast, a balanced three-phase load draws power evenly over time, reducing the need for energy storage components.

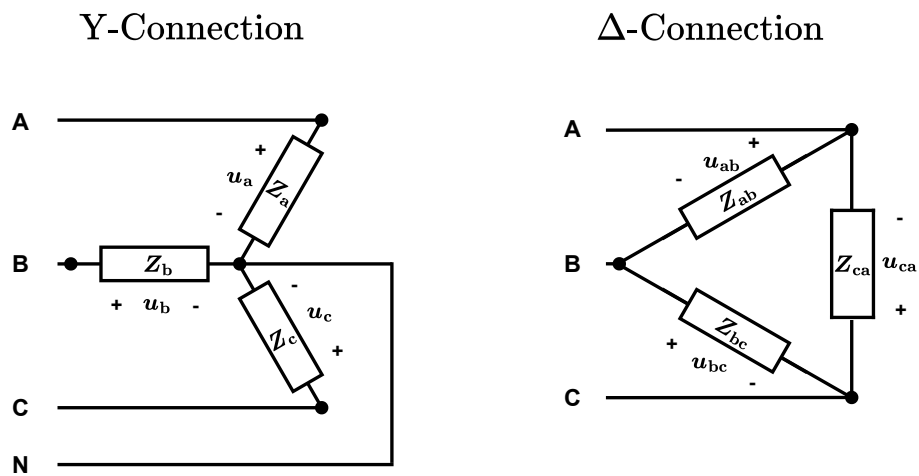


Figure 2.10: The two main load configurations for three-phase systems.

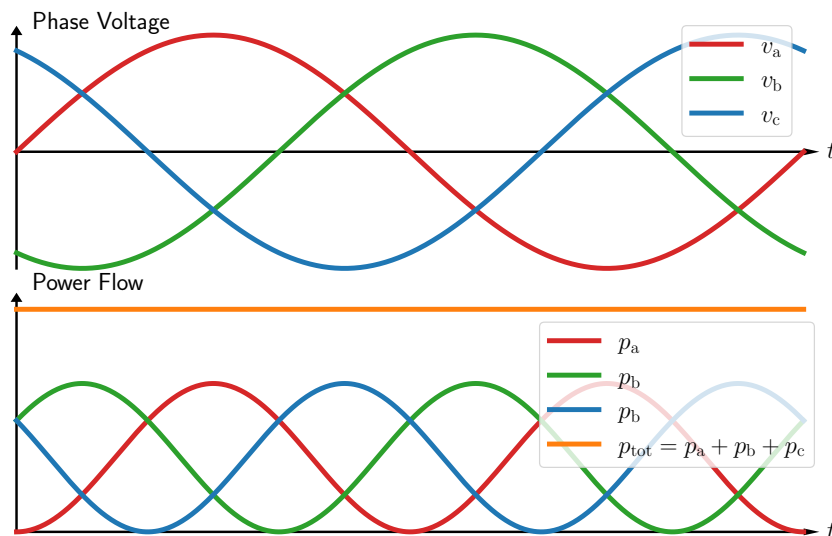


Figure 2.11: Phase voltages and power plotted for each phase in case of a balanced system with a purely resistive load. The dashed magenta line shows the total power which is constant.

2.4.2 Balanced- & Unbalanced Three-phase

Like a three-phase load, the phase voltages can also be more or less balanced. In an ideal three-phase system the phase voltages are purely sinusoidal, have the same amplitude, and are 120 degrees phase-shifted from each other. If these conditions are met, the system is balanced [3]. In reality, phase voltages can deviate from the ideal system in ways that can affect the operation of grid-connected converters. A common way to quantify the balance of a three-phase system is to analyze it in terms of symmetrical components.

2.4.2.1 Symmetrical Components

Any set of unbalanced three-phase quantities can be expressed as the sum of three sets of symmetrical components [3]. These components are called positive sequence, negative sequence, and zero sequence. The positive sequence is given by

$$v_a^+ = \hat{V}_{+1} \sin(\omega_1 t + \phi_{+1}) \quad (2.8)$$

$$v_b^+ = \hat{V}_{+1} \sin(\omega_1 t - \frac{2\pi}{3} + \phi_{+1}) \quad (2.9)$$

$$v_c^+ = \hat{V}_{+1} \sin(\omega_1 t + \frac{2\pi}{3} + \phi_{+1}), \quad (2.10)$$

where \hat{V}_{+1} and ϕ_{+1} denote the amplitude and phase shift of the positive-sequence phase voltages $v_{a,b,c}^+$. In the negative sequence, the phase shifts of the b- and c-quantities have switched places, and are thus given by

$$v_a^- = \hat{V}_{-1} \sin(\omega_1 t - \phi_{-1}) \quad (2.11)$$

$$v_b^- = \hat{V}_{-1} \sin(\omega_1 t + \frac{2\pi}{3} - \phi_{-1}) \quad (2.12)$$

$$v_c^- = \hat{V}_{-1} \sin(\omega_1 t - \frac{2\pi}{3} - \phi_{-1}), \quad (2.13)$$

where \hat{V}_{-1} and ϕ_{-1} denote the amplitude and phase shift of the negative-sequence phase voltages $v_{a,b,c}^-$.

The zero sequence consists of quantities with the same phase, and is given by

$$v_a^0 = \hat{V}_0 \sin(\omega_1 t + \phi_0) \quad (2.14)$$

$$v_b^0 = \hat{V}_0 \sin(\omega_1 t + \phi_0) \quad (2.15)$$

$$v_c^0 = \hat{V}_0 \sin(\omega_1 t + \phi_0), \quad (2.16)$$

where \hat{V}_0 and ϕ_0 denote the amplitude and phase shift of the zero-sequence phase voltages $v_{a,b,c}^0$.

An example of an unbalanced three-phase system is shown in Figure 2.12, where the symmetrical components that constitute the system are shown as phasor diagrams. The presence of negative- and zero-sequence components in the grid indicates asymmetries caused by unbalanced loads or faults. For example, a large negative sequence voltage could indicate a line-to-line short circuit, whereas a combination of negative and zero sequence voltages could indicate a short circuit from line to ground.

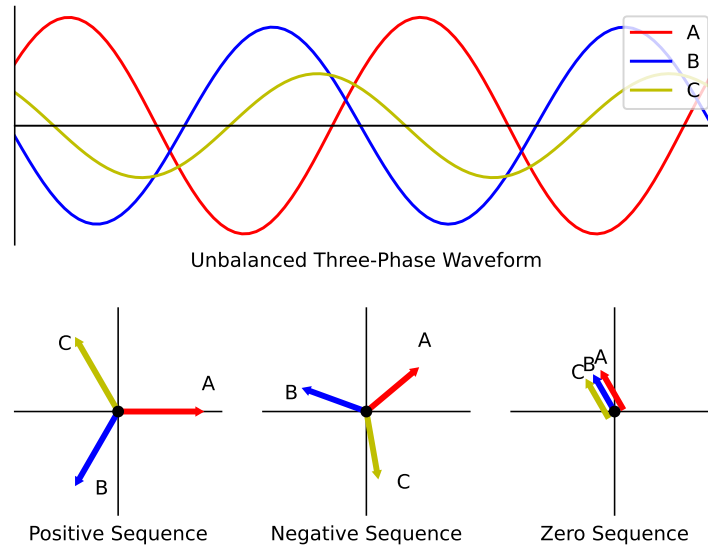


Figure 2.12: Waveforms of an unbalanced three-phase AC-system and the phasors corresponding to its symmetrical components. All phasors are spinning counterclockwise.

2.4.3 Harmonics

Power quality in a three-phase system is affected not only by voltage imbalances but also by the presence of non-linear loads. Such loads introduce frequency components higher than the fundamental frequency, which are collectively referred to as harmonics. These harmonics occur at integer multiples of the fundamental frequency and are expressed as:

$$\omega_n = n \cdot \omega_1, \quad n = 1, 2, 3, \dots \quad (2.17)$$

where n denotes the order of the harmonic. Harmonics have undesirable effects, such as power loss, heating, as well as higher peak voltages that can stress system components [6]. Harmonics that are integer multiples of three such that $n = 3, 6, 9, \dots$ are called zero-sequence harmonics, since they appear as zero-sequence components [7]. The presence of these harmonics causes current to flow through the neutral conductor (if present), which can lead to overheating. Harmonics where $n = 3k - 2$, $k \in \mathbb{N}$ such that $n = 1, 4, 7, \dots$ are called positive-sequence harmonics, which means that they rotate in the same direction as the fundamental frequency component. On the

other hand, harmonics where $n = 3k - 1$, $k \in \mathbb{N}$ such that $n = 2, 5, 8, \dots$ are called negative-sequence harmonics, which means that they rotate in the opposite direction. In electric motors, negative sequence harmonics produce flux that opposes the intended direction of rotation, which decreases efficiency [8].

2.4.4 Earthing Systems

An important aspect to consider in grid-connected converters is the earthing system, and there are different systems used depending on the country. The system used in Sweden is the TN-C-S system, which stands for *Terra-Neutral-Combined-Separate* [9], and will be the focus of this investigation. An overview of this system is given in Figure 2.13. *Terra* refers to the fact that the system is physically connected to the ground at the transformer station that supplies a residence or an industry. This is done at the star point of the transformer. *Neutral* means that any equipment supplied by the system has a direct connection to the grounding point on the transformer. *Combined* and *Separate* indicate that neutral and protective earth are combined in a single conductor, the PEN conductor. This conductor is then separated in a distribution board that provides a neutral conductor and a protective earth (PE) conductor for any connected equipment.

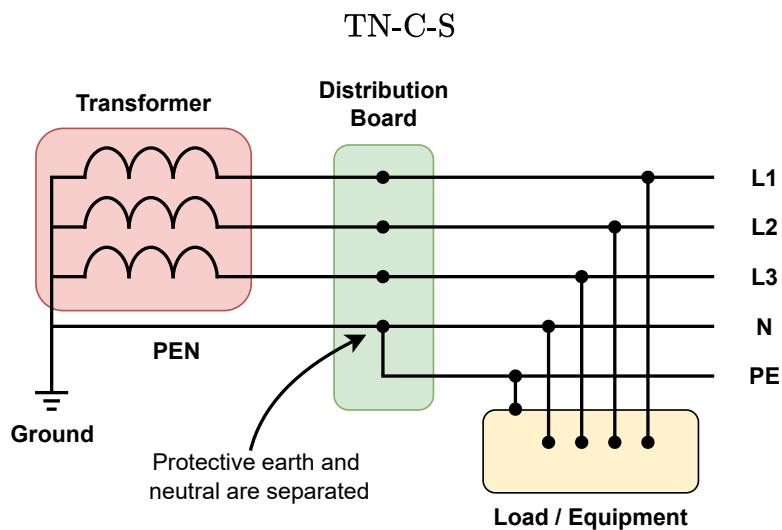


Figure 2.13: An overview of the TN-C-S system which is used in Sweden.

2.4.5 Leakage & Touch current

Although protective earthing adds safety, it also has the undesired effect of providing a path to the power supply ground through resistive and capacitive coupling between

the electronic equipment and the chassis. The capacitive coupling is caused in part by the practice of adding physical capacitors connected to the protective earth to suppress common-mode voltages. Another contributor is parasitic capacitance which arises naturally between the electronic equipment and the chassis. Any current that finds its way to the chassis and through the protective earth conductor is referred to as *leakage current*. The path of the leakage current is illustrated to the left in Figure 2.14, where it is shown how the leakage current can form a ground loop that causes EMI. If the leakage current is high enough, it can also trip the RCD. This typically happens when the leakage current exceeds 30 mA RMS.

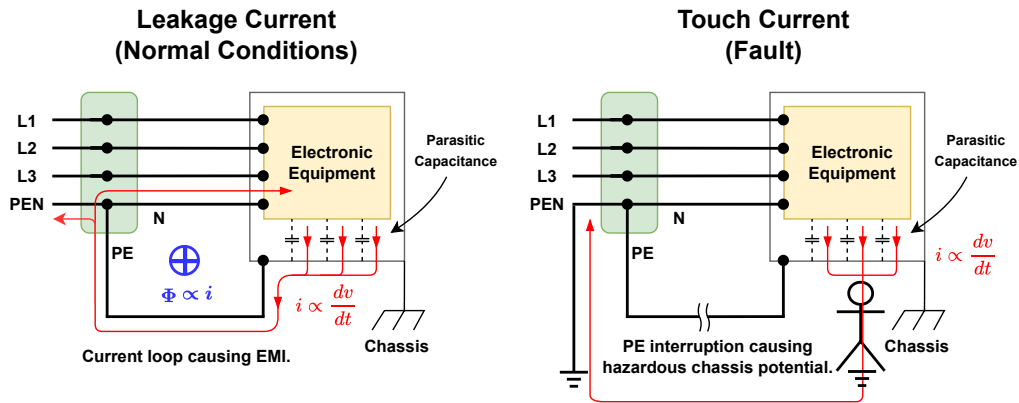


Figure 2.14: The possible paths for leakage current.

If a human or animal touches the chassis of a piece of electrical equipment, current may flow through the body back to the source. This is known as *touch current*, and is illustrated to the right in Figure 2.14. If the protective earth conductor is interrupted, the chassis is no longer clamped to neutral voltage, which poses a more serious risk of injury or death. A poorly designed piece of electrical equipment could pass enough touch current to cause injury or death to a human or animal that is touching the chassis, and there are regulations that define maximum limits.

2.4.5.1 Common-Mode Voltage

In a three-phase load, the common-mode voltage refers to the voltage between the neutral point and the ground of the power source, and can be expressed as

$$V_{CM} = \frac{1}{3} (V_a + V_b + V_c). \tag{2.18}$$

A high common-mode voltage can cause excessive leakage current, since it appears on all phases.

2.4.5.2 Capacitance

In order to understand the mechanisms behind leakage current, it is useful to study the governing equation of the capacitor

$$i(t) = C \frac{dv(t)}{dt}, \quad (2.19)$$

where C is the capacitance, $i(t)$ is the current through the capacitor, and $v(t)$ is the voltage over the capacitor. This equation shows that it is the rate of change of voltage that drives leakage current. Using the Fourier transform and rearranging gives the reactance

$$\frac{V(j\omega)}{I(j\omega)} = \frac{1}{j\omega C}, \quad (2.20)$$

where ω is the angular frequency. This shows that a capacitor can be thought of as a frequency-dependent resistor where the resistance decreases as the frequency increases. In switching applications such as converters, the high frequency content of rapidly switching transistors therefore pose a design challenge.

A useful circuit to study is the RC-circuit, which consists of a resistor and capacitor in series as shown in Figure 2.15. If a step voltage V_0 is applied to the circuit, the voltage over the capacitor will increase according to

$$v_C(t) = V_0 \left(1 - e^{-\frac{t}{RC}}\right) \quad (2.21)$$

producing an exponential waveform as shown in Figure 2.16. An important parameter of the RC-circuit is the time constant

$$\tau = RC, \quad (2.22)$$

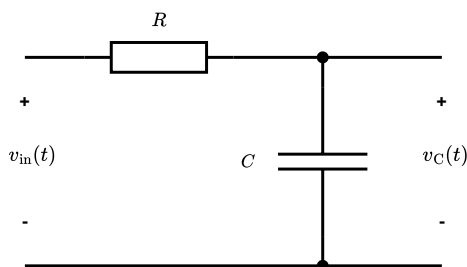


Figure 2.15: An RC-circuit.

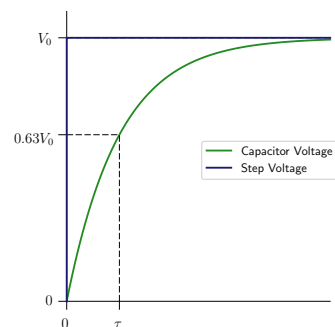


Figure 2.16: RC-circuit voltages during a voltage step.

as it characterizes how fast the capacitor charges. Substituting $t = \tau$ in Equation 2.21 shows that the capacitor voltage will have reached approximately 63% of the

step voltage after τ seconds have passed. Acquiring τ by measuring the voltage over a capacitor is therefore an effective way of measuring its capacitance, since it can easily be calculated with Equation 2.22.

2.4.5.3 Requirements & Test Procedure For Touch Current

Unlike leakage current, touch current must conform to specific legal requirements. The maximum allowable touch current for electric vehicles is defined in ISO 5474-1:2024 "General Requirements for conductive power transfer". It states the following touch current limits:

a) In normal conditions:

- 0.5 mA AC (RMS)
- 2 mA DC

b) During a protective earth interruption:

- 3.5 mA AC (RMS)
- 10 mA DC

The touch current test procedure is defined in ISO 5474-2:2024, *AC power transfer*, and involves the use of the measurement circuit shown in Figure 2.17, with the parameter values listed in Table 2.1). It contains a body model that mimics the impedance of a real human body, and is used to measure the touch current in the setup shown in Figure 2.18.

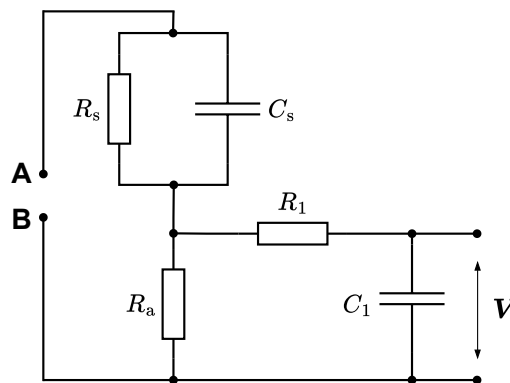


Figure 2.17: The touch current measurement circuit.

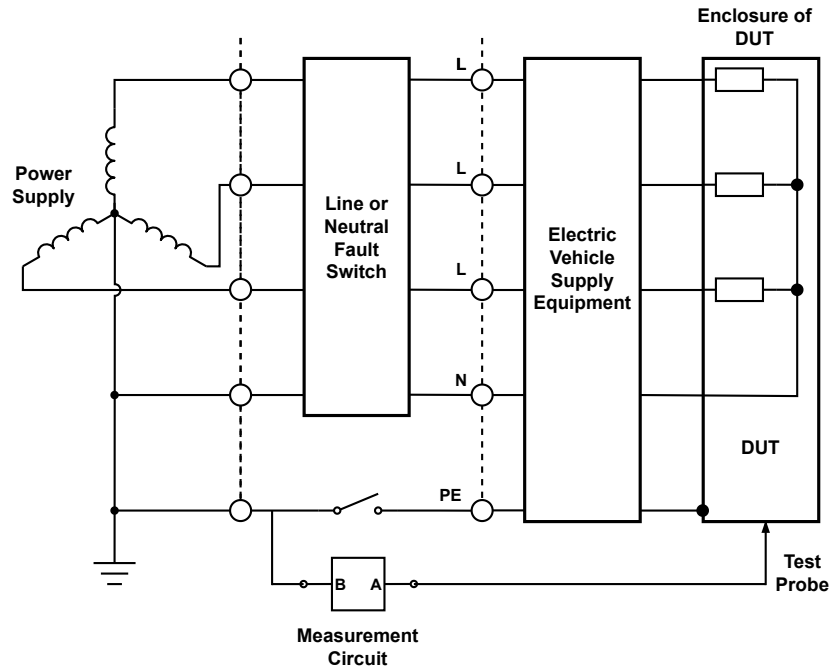


Figure 2.18: The touch current measurement setup.

Table 2.1: Measurement circuit parameter definitions.

Parameter	Value/Definition
R_s	1.5 k Ω
R_a	500 Ω
R_1	10 k Ω
C_s	0.22 μF
C_1	0.022 μF
V	Measured voltage used to calculate touch current.

2.4.6 Power Grid Modeling

The power grid is characterized by many different parameters that are of interest when creating a model for it. Two such parameters are the short-circuit power S_{SC} and the R/X -ratio. The organization Cigre provides ranges for these parameters for different grid voltages V_g in European and North American grids [10]. These parameter ranges are presented in Table 2.2 and 2.3.

Table 2.2: European grid equivalent data from Cigre.

Voltage Level	Grid Voltage, V_g [kV RMS LL]	Short-Circuit Power, S_{SC} [MVA]	R/X-ratio
Low Voltage	0.4	1 to 10	0.70 to 11.00
Medium Voltage	20	100 to 1000	0.40 to 2.00
High Voltage	220	5000 to 20000	0.07 to 0.60

Table 2.3: North American grid equivalent data from Cigre.

Voltage Level	Grid Voltage, V_g [kV RMS LL]	Short-Circuit Power, S_{SC} [MVA]	R/X-ratio
Low Voltage	0.12/0.208/0.48 †	1 to 10	0.70 to 11.00
Medium Voltage	12.47	100 to 1000	0.40 to 2.00
High Voltage	230	5000 to 20000	0.07 to 0.60

† 0.12 kV is line-to-neutral voltage of single-phase residential subnetwork;
0.208 kV is of commercial subnetwork; 0.48 kV is of industrial subnetwork.

The short-circuit power is the apparent power that flows in the case of a short circuit, and the R/X -ratio is the ratio between the resistance and the reactance of the source impedance. Using the line-to-line voltage V_{LL} , the impedance of each phase is given by

$$Z_G = \frac{V_{LL}^2}{S_{SC}}. \quad (2.23)$$

Assuming that the reactance is inductive, the resistance and inductance of Z_G can be calculated with

$$R_G = \frac{kZ_L}{\sqrt{k^2 + 1}} \quad (2.24)$$

$$L_G = \frac{Z_L}{\omega_1 \sqrt{k^2 + 1}} \quad (2.25)$$

where k is the R/X -ratio and ω_1 is the angular frequency of the grid. With these

parameters the model shown in Figure 2.19 can be constructed.

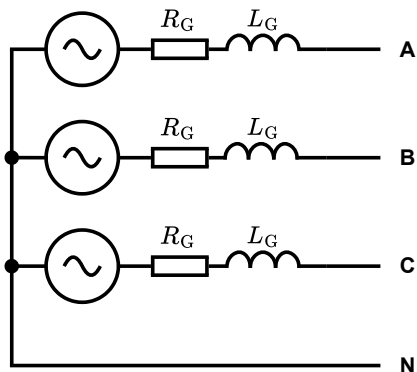


Figure 2.19: Power grid model.

2.5 Converter Control Methods

The following sections describe concepts that are relevant for the control of three-phase converters.

2.5.1 Space Vectors & The Rotating Reference Frame

A useful technique when dealing with balanced three-phase quantities, such as voltages or currents, is to represent them as equivalent two-phase quantities. The two components of the two-phase representation can be expressed as a vector in the complex plane by using the Clarke transformation

$$\mathbf{v}^s = v_\alpha + jv_\beta = \frac{2}{3}K \left(v_a + v_b e^{j2\pi/3} + v_c e^{-j2\pi/3} \right) \quad (2.26)$$

[3] where the subscripts α and β correspond to the real and imaginary components respectively. K is a scaling constant that can be chosen to encode the desired quantity in the magnitude of the vector. Choosing $K = 1$ gives the vector the same magnitude as the three-phase quantities, called amplitude-invariant scaling. Henceforth, this scaling will be used.

The amplitude invariant Clarke transformation can be expressed in matrix form with

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \quad (2.27)$$

[3] which is commonly given the symbol shown in Figure 2.20. Using this transformation reduces the number of variables to only two, which simplifies control. The alpha-beta axes form what is often called a *stationary* reference frame, since the axes themselves are fixed in time. By transforming the alpha-beta quantities further using the Park transformation

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}, \quad (2.28)$$

the reference frame is made to rotate with the phase angle θ , creating instead a *rotating* reference frame. By selecting

$$\frac{d\theta}{dt} = \omega_1, \quad (2.29)$$

all quantities of this frequency will appear as DC from the perspective of this reference frame. The Park transformation therefore makes it possible to control three-phase systems with DC-controllers.

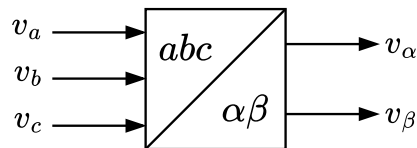


Figure 2.20: Three-phase to alpha-beta transformation symbol.

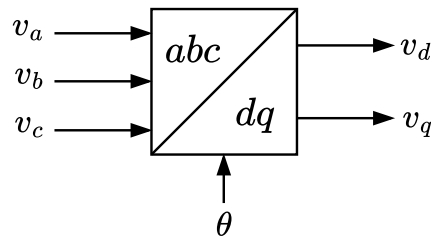


Figure 2.21: Three-phase to rotary transformation symbol.

2.5.2 Grid Synchronization

Grid synchronization is an important part in the control of grid-connected converters that deals with determining grid variables such as phase angle, frequency, and amplitude [1]. Monitoring these variables allows the converter to produce sinusoidal phase currents that are synchronized with the grid voltages at the fundamental frequency. This allows for control over the active and reactive power of the converter. Knowing the phase angle also makes it possible to transform the grid voltages and currents to

a rotational reference frame where the fundamental frequency quantities appear as DC, simplifying control. Due to the presence of harmonics and disturbances caused by other loads connected to the grid, the acquisition of grid parameters must be adequately robust. Grid synchronization is therefore a well-researched area with many different techniques.

A common grid synchronization method is to use the phase-locked loop (PLL), which consists of a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO) [1]. An overview of the structure of the PLL is shown in Figure 2.22. The objective of the PLL is to take an input signal $\mathbf{v}(t)$ and produce an output signal $\mathbf{v}'(t)$ that minimizes phase error $e_{pd}(t)$, which *locks* the phases of the input and output signals. An estimate of the phase angle of the input signal (the variable of interest) is produced internally in the VCO.

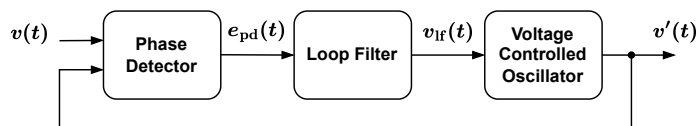


Figure 2.22: Block diagram of a phase-locked loop.

2.5.2.1 SRF-PLL

The synchronous reference frame PLL (SRF-PLL), is a three-phase PLL which uses the Park transformation to convert the grid voltages to dq-quantities [1]. The structure is shown in Figure 2.23. The low-pass filter takes v_q as an error signal and controls the frequency/phase generator (FPG) to regulate v_q to zero, aligning the voltage vector with the d-axis. This configuration conveniently makes the d-current correspond to the active power, and the q-current to the reactive power.

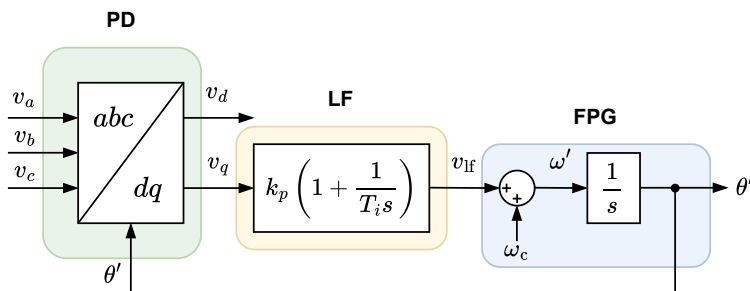


Figure 2.23: Structure of an SRF-PLL.

By supplementing the SRF-PLL with a decoupling network, a decoupled double synchronous reference PLL (DDSRF-PLL) can be formed, which unlike the SRF-PLL can produce dq-quantities for both the positive and negative sequence components of the fundamental frequency. This is useful for operating a converter under unbal-

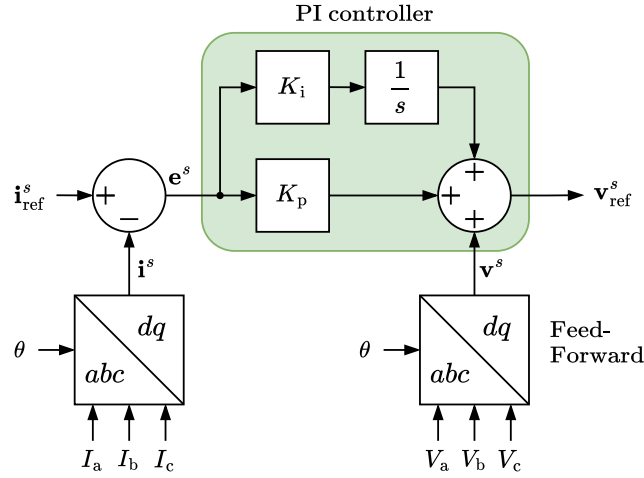


Figure 2.24: A block diagram of a PI-controller.

anced conditions.

2.5.3 PI- & PR Controllers

The PI controller is a closed-loop controller that is common in the industry [11]. The name of this controller comes from the proportional (P) and integral (I) gain that the controller applies to the error signal. The error signal is the difference between the reference signal (the desired output of the system) and the measured output. Figure 2.24 shows a block diagram representation of a PI controller, and the frequency domain transfer function is given by

$$G_C(s) = K_p + \frac{K_i}{s} \quad (2.30)$$

where K_p and K_i represent the proportional and integral gain respectively.

In order to use the PI controller for the control of AC quantities, it must be implemented in a rotating reference frame where the reference signal and the measured quantities are transformed to DC. Otherwise, the controller will produce a high steady-state error [11].

Unlike the PI controller, the proportional resonant (PR) controller can be implemented in the stationary reference frame without the need for transformations. The PR controller replaces the integral term in the PI controller with a resonant term, and has the transfer function

$$G_C(s) = K_p + \frac{2K_i s}{s^2 + \omega_0^2} \quad (2.31)$$

where ω_0 is the resonant frequency of the controller. ω_0 is the pole of the second

term, and setting it to the same frequency as the controlled quantity provides a high gain.

2.5.4 Third Harmonic Zero-sequence Injection (ZSI)

Leaving the neutral conductor of a grid converter unconnected offers the option of injecting a zero-sequence voltage. The reason for this is that any injected zero-sequence voltage appears at the Y-point, which would cause a short circuit if the neutral is connected. The benefit of ZSI might not be obvious, and it may seem counterintuitive to intentionally create an imbalance in the system. Figure 2.25 shows a phasor diagram of a converter that does not use ZSI, and its phase voltage is limited by the maximum DC voltage that a single CHB string can produce. The maximum modulation index in this case is therefore 1. In Figure 2.26 however, a zero-sequence component has been added at three times the fundamental frequency, which essentially *pushes* the center of the positive sequence arrows away from the DC limit, which accommodates a higher phase voltage. Using a third-harmonic zero-sequence injection therefore increases the maximum modulation index from 1 to $\frac{2}{\sqrt{3}}$, approximately 15% higher. This could be especially useful when charging batteries, as it would utilize the CHB modules more efficiently. In practice, ZSI can be implemented by adding the following expression to all voltage references of the converter [3]:

$$v_{\text{ZSI}} = -\frac{|\mathbf{v}_{\text{ref}}^s|}{6} \cos(3\arg(\mathbf{v}_{\text{ref}}^s)). \quad (2.32)$$

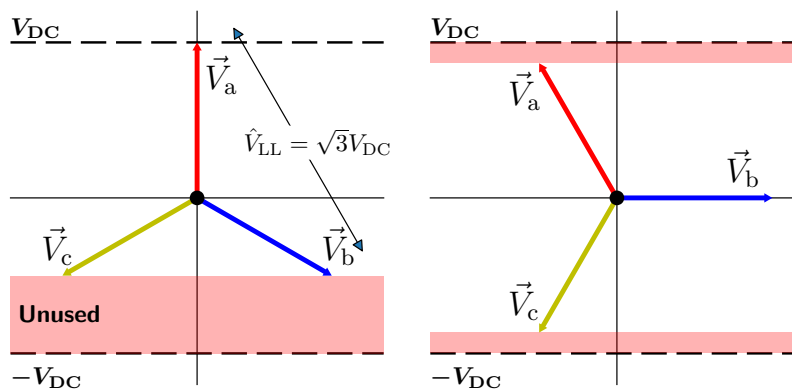


Figure 2.25: Phasor diagram showing the maximum voltage without ZSI. The red parts show the unutilized parts of the DC voltage.

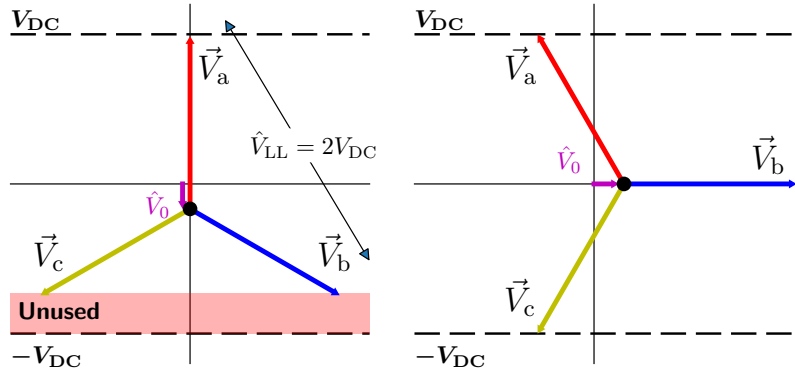


Figure 2.26: Phasor diagram showing the maximum voltage with ZSI. Here the DC voltage is fully utilized.

2.6 Short Circuit

When designing electrical applications, it is important to consider fault conditions such as short circuits. This is especially true in applications with Li-ion batteries, where excessive internal heat dissipation caused by a short circuit can lead to thermal runaway and cause fires. The magnitude of the current that flows as a result of a short circuit is dependent on the impedance at the point of the short circuit, as well as the impedance of the energy source. The maximum current that can flow in the case of a short circuit is called the prospective short-circuit current (PSCC) [12], and protective devices such as fuses and breakers should be able to protect the equipment against this current.

2.6.1 Delayed Zero Crossings

If a short-circuit occurs, it is desirable to disconnect the power source with some type of breaker. If the current is not 0 when the breaker is activated, there is a risk of arcing. Figure 2.27 shows a short-circuit model with sinusoidal voltage E , resistance R and inductance L . The short-circuit current $i(t)$ can be expressed as

$$i(t) = e^{-\frac{R}{L}t} \left\{ \frac{-\hat{E}}{\sqrt{R^2 + \omega^2 L^2}} \sin \left[\varphi - \tan^{-1} \left(\frac{\omega L}{R} \right) \right] \right\} + \left\{ \frac{-\hat{E}}{\sqrt{R^2 + \omega^2 L^2}} \sin \left[\omega t + \varphi - \tan^{-1} \left(\frac{\omega L}{R} \right) \right] \right\}, \quad (2.33)$$

where \hat{E} is the voltage amplitude, ω is the angular frequency of the voltage, and φ is the phase shift [13]. The first term is a DC component that decays at the rate determined by $e^{-\frac{R}{L}t}$, which has a time constant that is inversely proportional to the R/X -ratio. This DC-term causes the short-circuit to be asymmetric. Figure

2.28 shows how a lower R/X -ratio increases the decay time of the short-circuit DC component. For certain loads, the short-circuit current may be displaced by the DC component such that the zero crossings are delayed for more than one period. This may prevent a breaker from activating, and is therefore an important factor to consider when selecting protective devices.

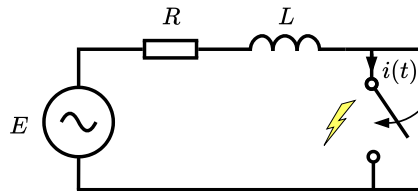


Figure 2.27: Equivalent short-circuit model.

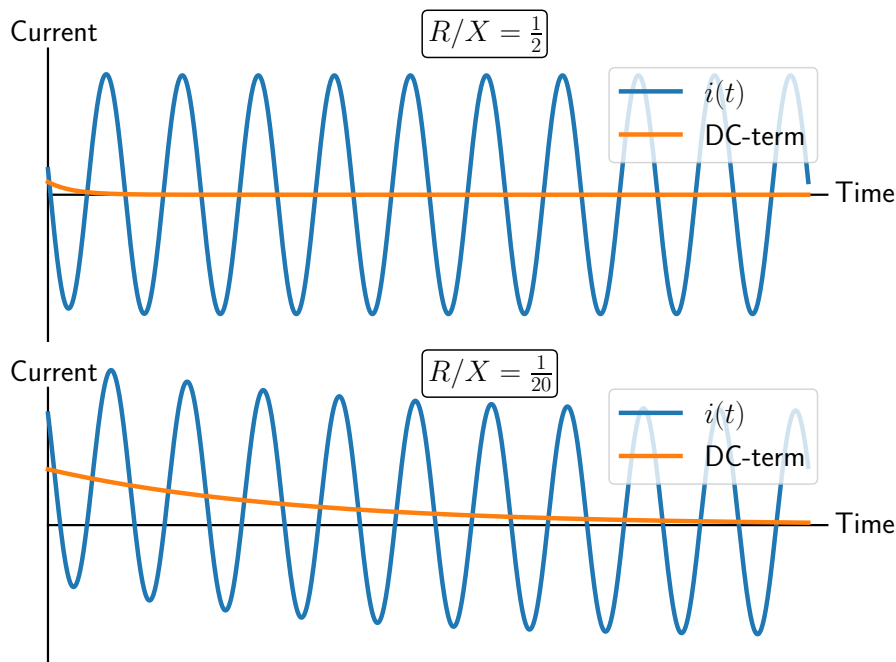


Figure 2.28: The asymmetric short-circuit current waveform for two different R/X -ratios.

2.6.2 Let-Through Energy

The high current that follows a short circuit is dissipated as heat in the affected electronic equipment. Therefore, a short circuit must be interrupted in time before the allowable temperature limits of the system components are exceeded [14]. A common metric used to dimension protective devices and wiring with respect to the

PSCC is *let-through energy*, which can be expressed as

$$\text{Let-Through Energy} = \int_{t_{sc}}^{t_{break}} i_{sc}(t)^2 dt, \quad (2.34)$$

where $i_{sc}(t)$ is the short-circuit current, t_{sc} is the time at which the short circuit occurs and t_{break} is the time at which it is interrupted. A simplified way to represent the let-through energy is given by using the RMS value of the short-circuit current instead:

$$\text{Let-Through Energy} = I_{sc}^2 t, \quad (2.35)$$

where t is the duration of the short circuit. The let-through energy represents the heat generated per unit of resistance in the short-circuit current loop, which can be realized by comparing it to the energy equation $E = \int RI^2 dt$. It can therefore be used to link the maximum thermal stress of the system to a maximum allowable time limit for protective devices to interrupt a short circuit.

3

Measurements & Simulations

This chapter presents the measurements and simulations used to evaluate the behavior of the CHB converter in terms of leakage current, touch current and let-through energy during a short circuit.

3.1 Parasitic Capacitance Measurement

The total parasitic capacitance of a prototype converter was measured by applying a voltage step between the chassis and different points in the system. A diagram of the measurement setup is shown in Figure 3.1, where the different test points are marked P_1 and P_2 . The time constant was extracted for each waveform and the total capacitance was calculated using Equation 2.22. The battery configuration for the prototype converter is shown to the left in Figure 3.2.

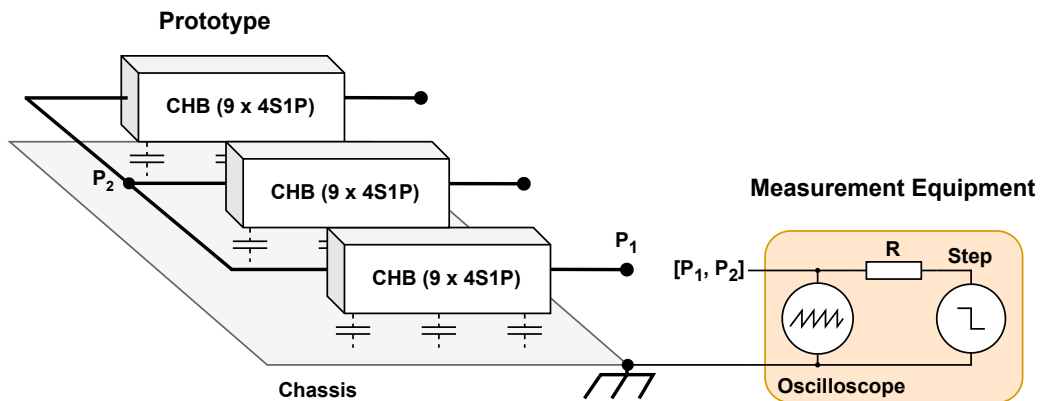


Figure 3.1: Sketch of the measurement setup.

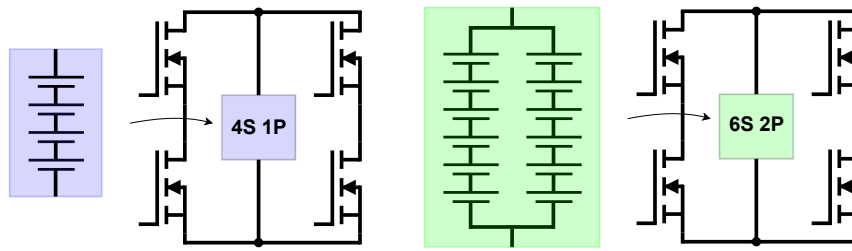


Figure 3.2: Battery cluster configurations.

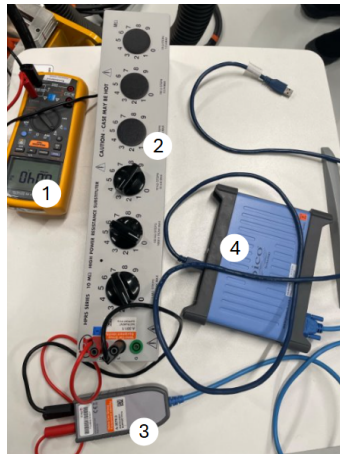


Figure 3.3: Measurement equipment. The numbered items are: 1) Multimeter; 2) Decade resistance box; 3) Differential probe; 4) Oscilloscope.

3.2 Leakage & Touch Current Simulation

The software used for modeling was PLECS 4.8.10. The simulations were run in Matlab R2023b using PLECS blockset. The solver settings used for the simulations are shown in Figure 3.8.

The H-bridges of the CHB converter were modeled using ideal switches together with a resistance of $5\text{ m}\Omega$ to model the on-state resistance of a MOSFET. The Li-ion battery cells were modeled as equivalent circuits with second-order RC circuits. The open circuit voltage was set to a constant 4.2 Volts. A CHB converter string was then modeled using 15 H-bridges, each fitted with 12 Li-ion cells in a 6S2P configuration. An overview is given in Figure 3.4. The earthing system was modeled according to the TN-C-S configuration.

3.2.1 Three-Phase Model

Three CHB-strings were arranged in a Y-configuration to form a three-phase converter. The switching frequency of the converters was set at 50 kHz. Level-shifted carrier modulation was used and the carriers were mapped to the modules so that the turn-on order goes incrementally from the phase connection to the Y-point as shown in Figure 3.5. The grid was modeled using an RL-circuit in series with each phase voltage. The converter was connected to the grid model through a filter consisting of a common mode choke and LCL-network. No Y-capacitors were used in the filter as it significantly slowed down the simulations. The angle of the grid voltages was obtained using an SRF-PLL. A PI-controller was implemented in the rotating reference frame for current control. A switch was used to change from leakage current measurement to touch current measurement. A block diagram for the complete three-phase model is shown in Figure 3.6.

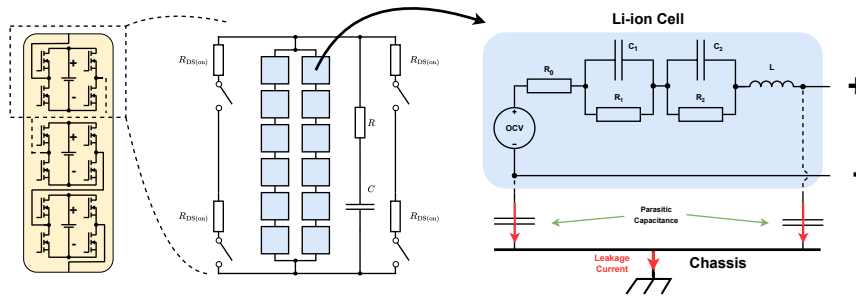


Figure 3.4: Recursive hierarchy of the CHB-converter model.

3.2.2 Single-Phase Model

In the single-phase model, the three CHB strings were connected in series, and the current controller was implemented in the stationary reference frame with a PR controller. An overview of the single-phase model is shown in Figure 3.7.

3.2.3 Simulations

The leakage current and touch current were simulated in the case of charging with 16 A per phase when connected to a European grid with a phase voltage of 230 V (RMS), 50 Hz. Five different conditions were tested:

1. Single phase.
2. Balanced grid voltages.
3. Balanced grid voltages with zero-sequence injection.

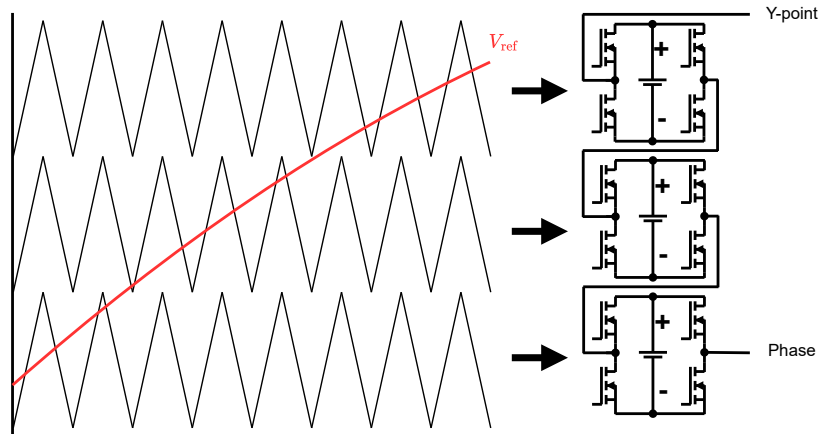


Figure 3.5: The mapping from the carriers to the CHB modules.

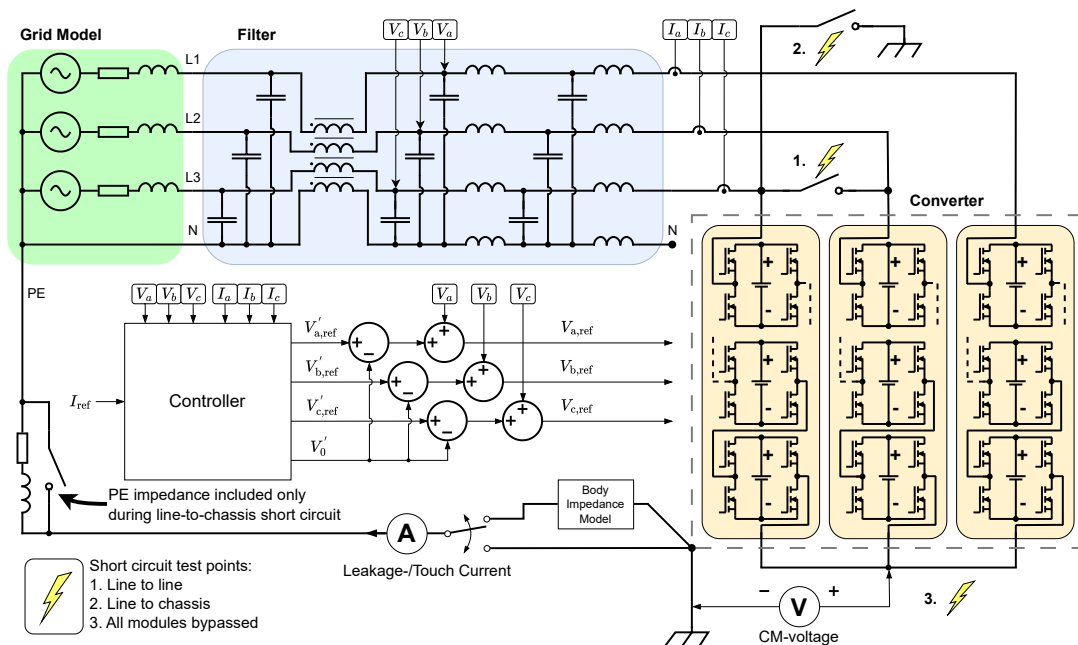


Figure 3.6: Block diagram of the three-phase model.

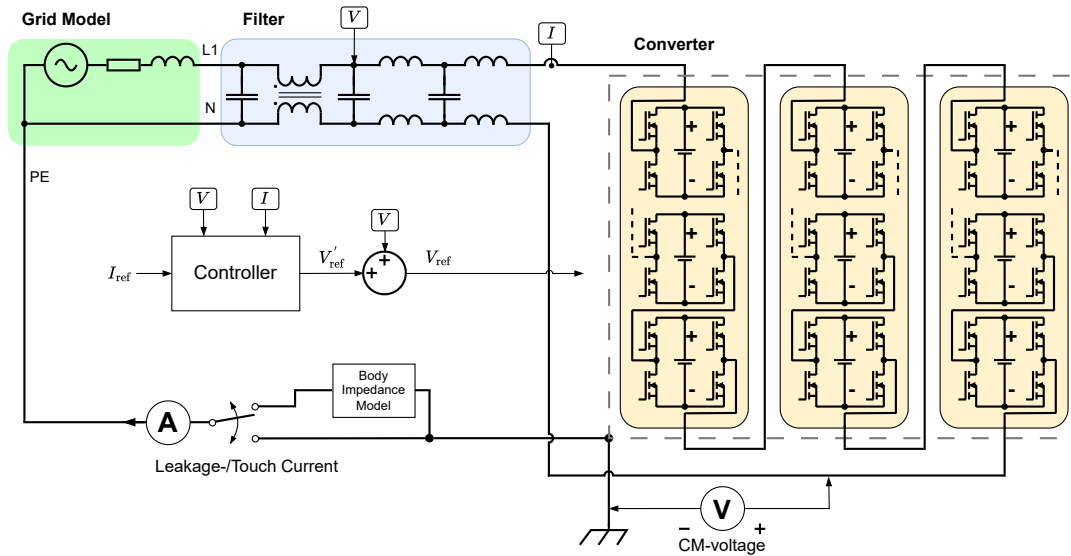


Figure 3.7: Block diagram of the single-phase model.

4. Flattened voltage peaks.
5. Voltage dip in one phase.

An FFT was performed on the leakage current and the common-mode voltage.

3.3 Short-Circuit Simulations

The three-phase model was also used for short-circuit simulations. Three different types of short circuit were simulated at the converter terminals:

1. Line-to-line.
2. Line-to-chassis.
3. All converter modules bypassed.

The different short-circuit points are marked in the model block diagram in Figure 3.6. The resistance for each short circuit was set at $5\text{ m}\Omega$. Short circuits were initiated at the peak voltage across the short-circuited points. Since the short-circuit current during a line-to-chassis short circuit flows through the protective earth conductor, an RL-circuit with the same values as in the grid model was included for this case (shown in Figure 3.6) to get a more accurate result. The impact of different short-circuit power ratings and R/X -ratios was investigated. The short-circuit

power and R/X -ratio parameters were obtained from a range provided in [10] under *European Grid Equivalent Data*. 2.34 was then used to calculate the let-through energy for a 10 ms time period after the short circuit.

The image shows the Simulink solver settings dialog box, organized into several sections:

- Simulation time:** Start time: 0.0, Stop time: 6e-2.
- Solver selection:** Type: Variable-step, Solver: ode15s (stiff/NDF).
- Solver details:**
 - Max step size: auto, Relative tolerance: 1e-4
 - Min step size: auto, Absolute tolerance: auto
 - Initial step size: auto, Auto scale absolute tolerance
 - Solver reset method: Fast, Maximum order: 5
 - Shape preservation: Disable All
 - Number of consecutive min steps: 1
 - Solver Jacobian method: auto
- Zero-crossing options:**
 - Zero-crossing control: Use local settings, Algorithm: Nonadaptive
 - Time tolerance: 10*128*eps, Signal threshold: auto
 - Number of consecutive zero crossings: 1000
- Tasking and sample time options:**
 - Automatically handle rate transition for data transfer
 - Allow multiple tasks to access inputs and outputs
 - Higher priority value indicates higher task priority

Figure 3.8: Simulink solver settings.

4

Results

This chapter presents the results from the capacitance measurements, the leakage and touch current simulations, and the short-circuit simulations.

4.1 Parasitic Capacitance Measurement

The graphs acquired from the voltage step test are shown in Figure 4.1. The parasitic capacitance was calculated using Equation 2.22, and the results are shown in Table 4.1. C_{tot} is the measured total capacitance, and C is the normalized capacitance distributed to each Li-ion cell pole. Because the metallic lid of the prototype converter was disassembled prior to measurement, the capacitance might have been lower than in a real application. To account for this, the highest measured per-pole capacitance of 0.92 nF was doubled and rounded to 2 nF when implemented in the model.

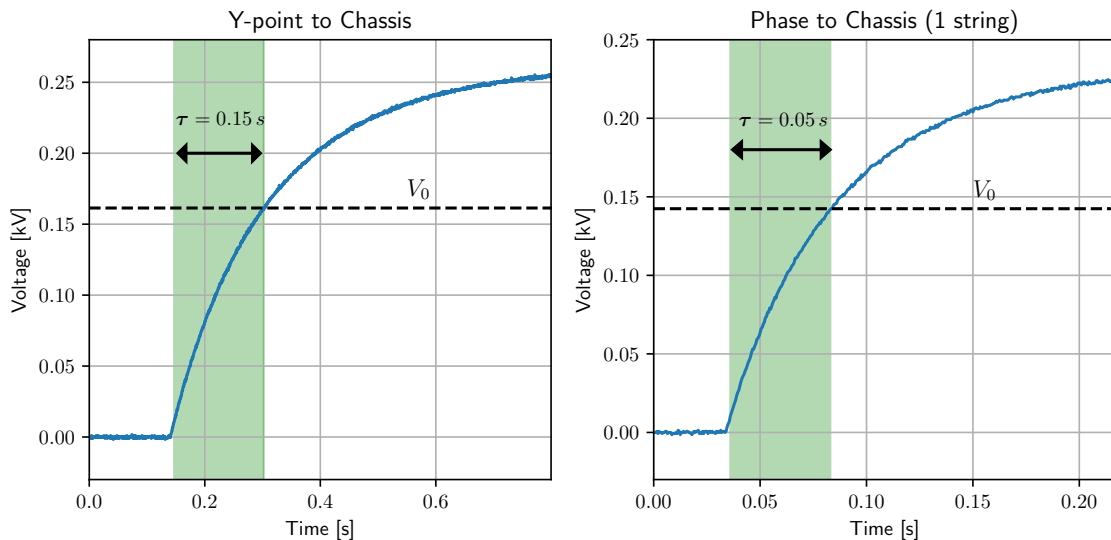


Figure 4.1: Voltage step test for capacitance extraction.

Table 4.1: Capacitance measurement results.

Measurement Point	R [M Ω]	τ [ms]	C_{tot} [nF]	C [nF]
Phase to chassis with only 1 string connected	1	66.4	66	0.92
Y-point to chassis with all three strings connected	1.05	172	164	0.76

4.2 Leakage & Touch Current Simulations

The simulations took a long time to run and therefore only one period of data was collected for each case. A distinct resonance was observed in the leakage current around 4 kHz in all simulations. A representative waveform and its FFT are shown in Figure 4.2. To improve clarity in subsequent plots, a notch filter was applied at 4 kHz to suppress this component and allow better analysis of other harmonics.

The following sections show the phase voltages, phase currents, and leakage current during charging at a peak current of 16 A. For the three-phase simulations, the common-mode voltage (the voltage between the Y-point and the chassis) is also shown. An FFT of the leakage current and common-mode voltage is included for each case to illustrate the frequency content. The leakage and touch current RMS values for the different grid conditions are presented in Table 4.2.

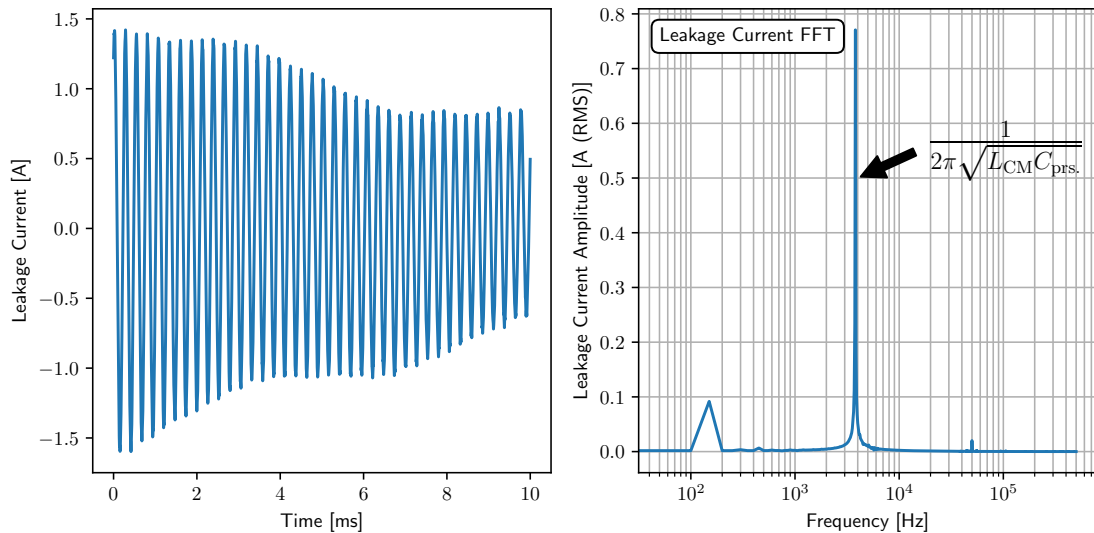


Figure 4.2: The unfiltered leakage current plot and corresponding FFT showing resonance at around 4 kHz.

4.2.1 Single-Phase Charging

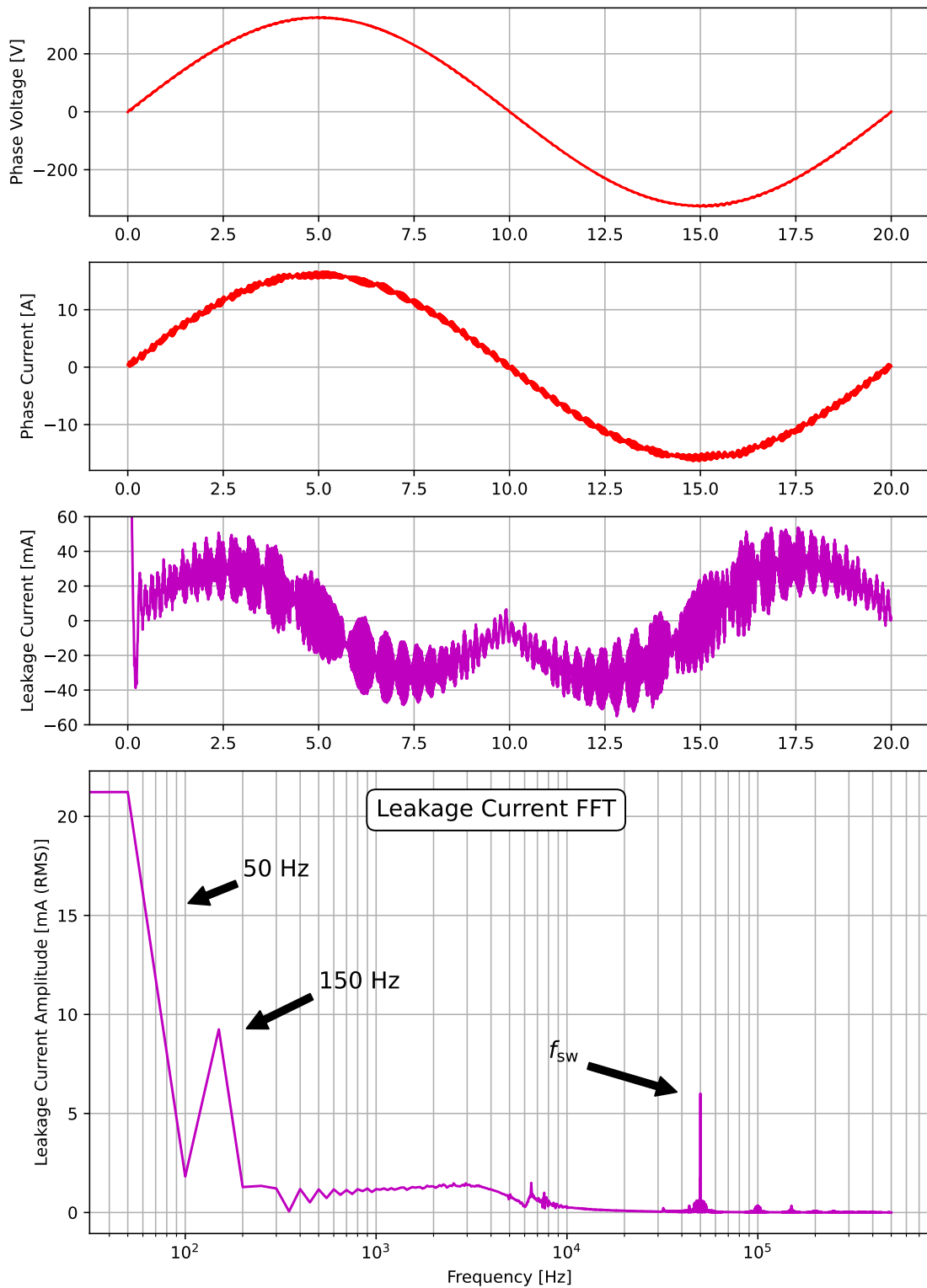


Figure 4.3: Waveform plots from the single-phase charging simulation.

4.2.2 Three-Phase Charging Without Zero-sequence Injection

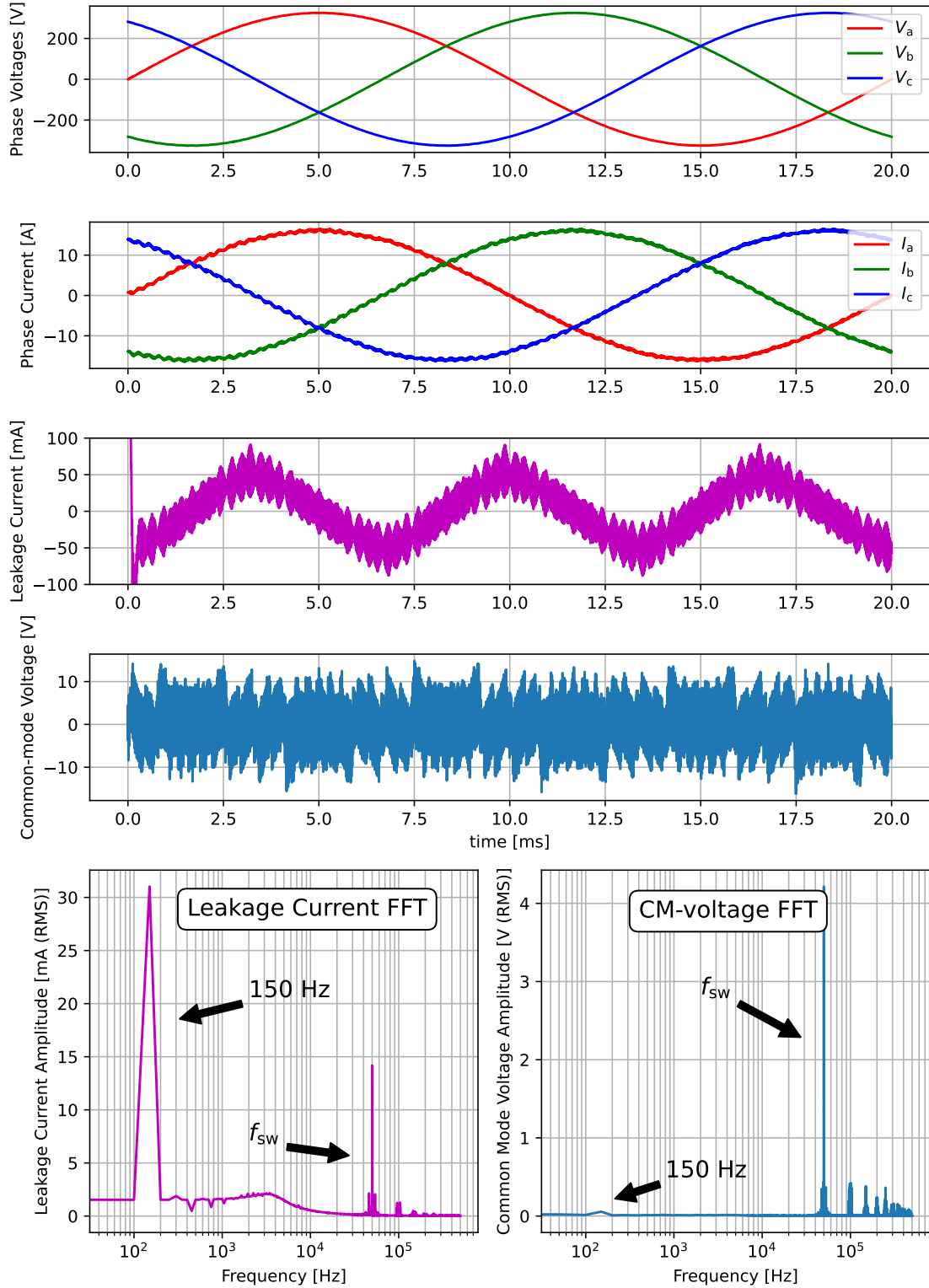


Figure 4.4: Waveform plots from the three-phase charging simulation without ZSI.

4.2.3 Three-Phase Charging With Zero-sequence Injection

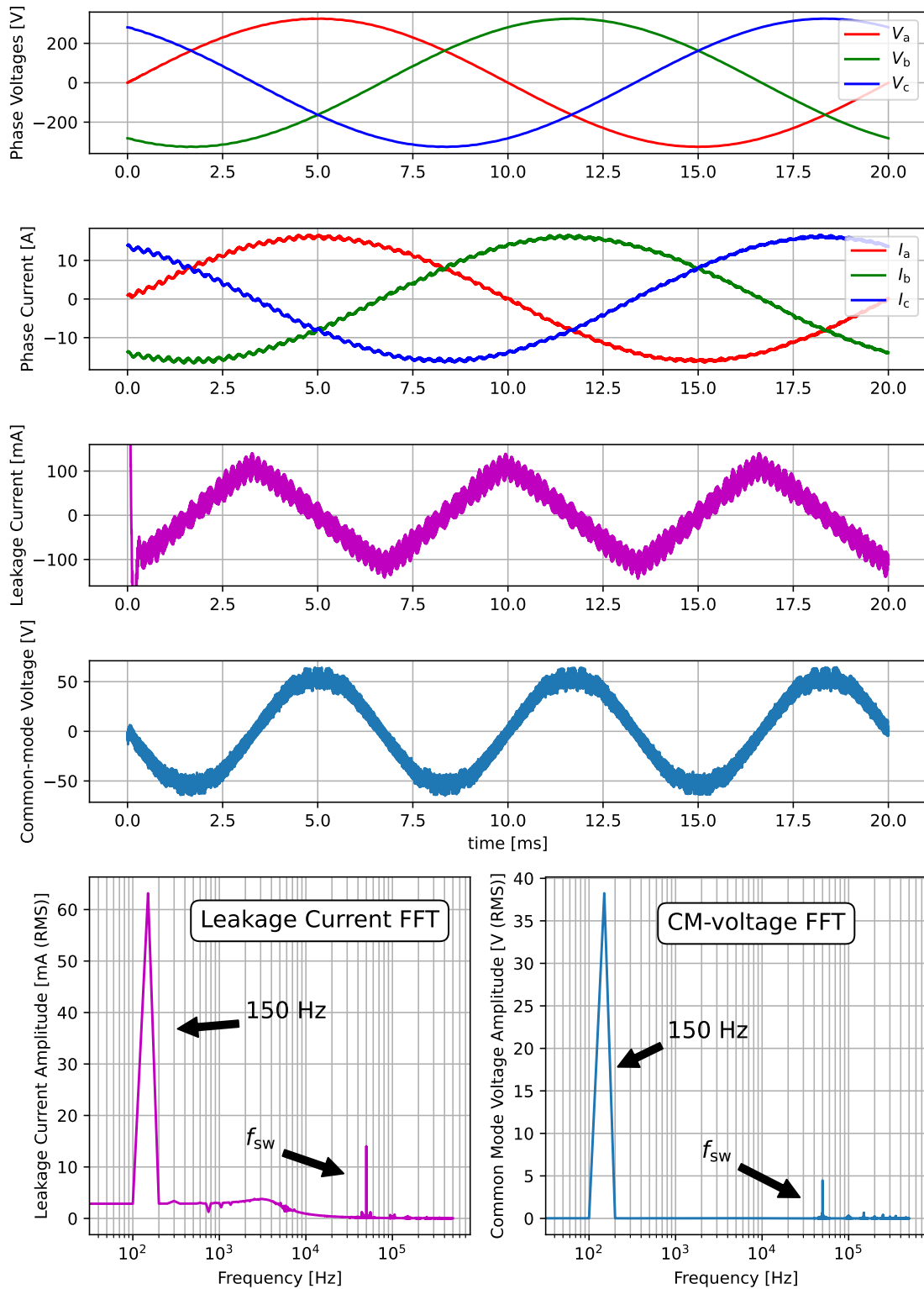


Figure 4.5: Waveform plots from the three-phase charging simulation with ZSI.

4.2.4 Three-Phase Charging With Flattened Voltage Peaks

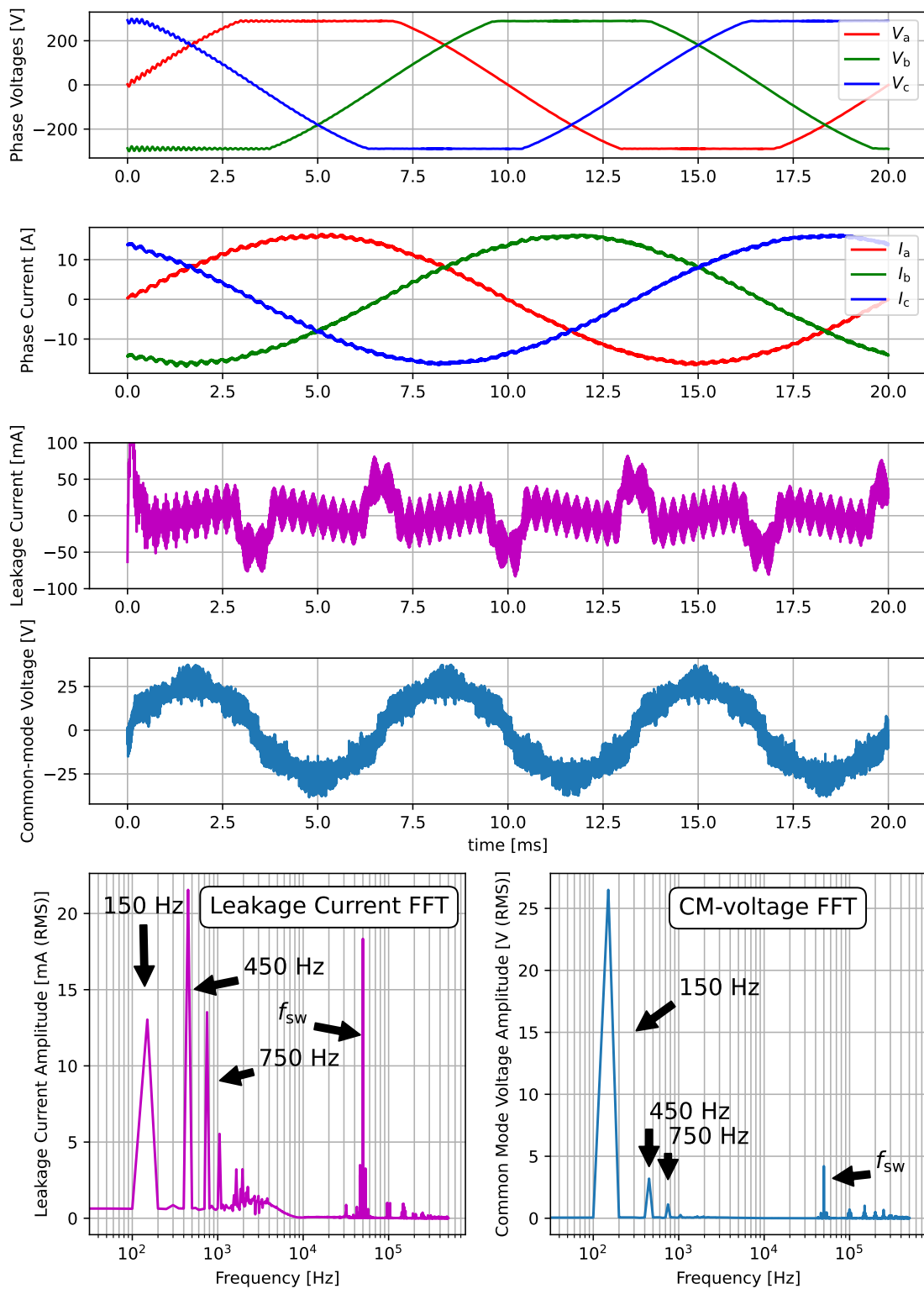


Figure 4.6: Waveform plots from the three-phase charging simulation with flattened voltage peaks.

4.2.5 Three-Phase Charging With Voltage Dip in One Phase

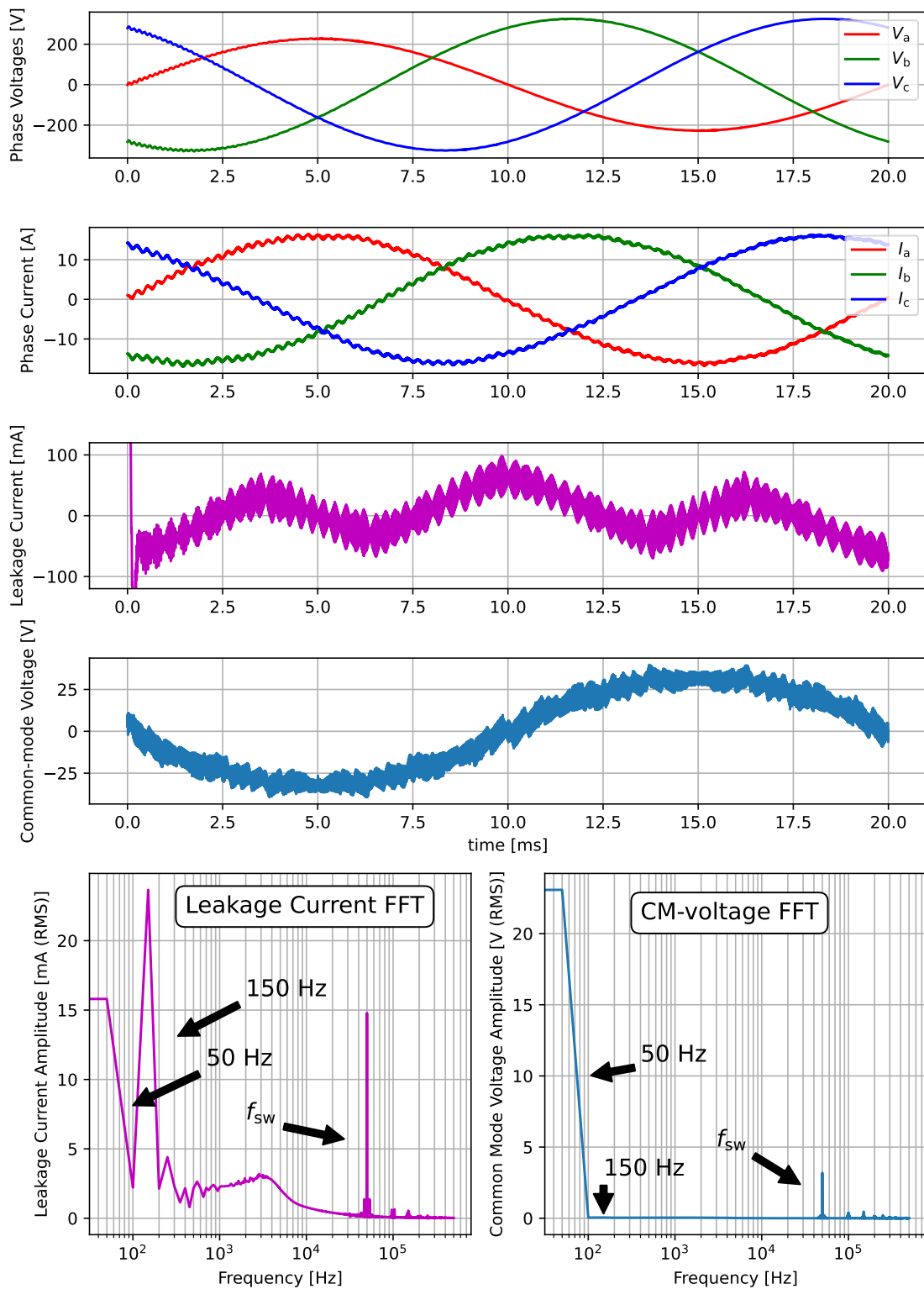


Figure 4.7: Waveform plots from the three-phase charging simulation with voltage dip in one phase.

Table 4.2: Leakage & touch current results.

Simulation	Leakage Current [mA RMS]	Touch Current [mA RMS] [†]
Single-phase	28	11
Three-phase without ZSI	40	10
Three-phase with ZSI	75	17
Three-phase with flat curve	26	13
Three-phase with voltage dip	45	14

[†] Legally required to be below 3.5 mA RMS (PE-interruption fault).

4.3 Short-Circuit Simulations

The results of short-circuit simulations are presented in the following sections. These results may be useful when selecting protective devices for a real CHB converter application.

4.3.1 Line-to-Line Short Circuit

The phase currents during the line-to-line short-circuit event are shown in Figure 4.8. Two different short-circuit power ratings were used for the grid model, $S_{SC} = 10 \text{ MV A}$ and $S_{SC} = 1 \text{ MV A}$. The corresponding let-through energy (I^2t) for each case is shown in Figure 4.9. This metric is relevant for assessing the thermal stress on components during a short circuit.

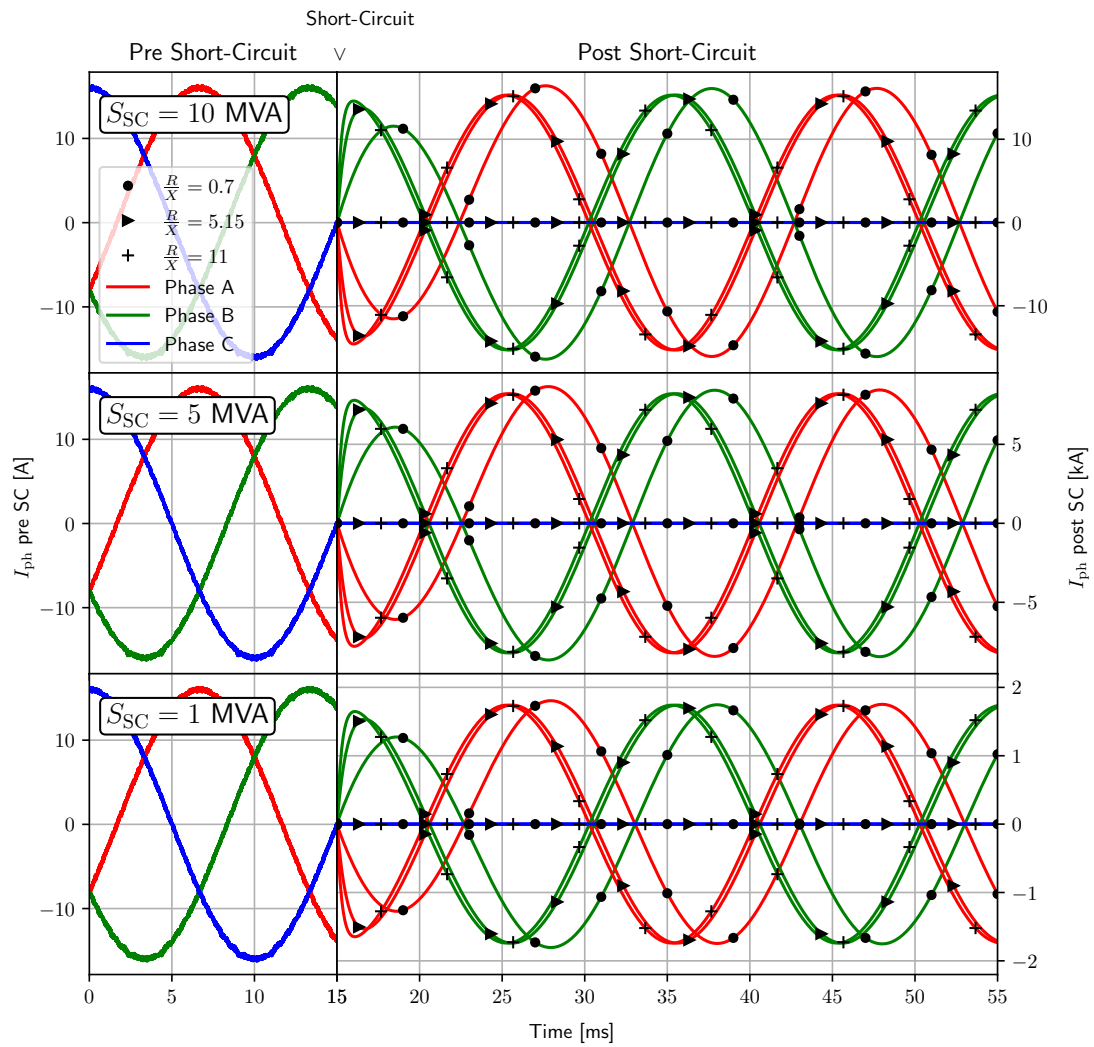


Figure 4.8: Line-to-line short-circuit simulation waveforms.

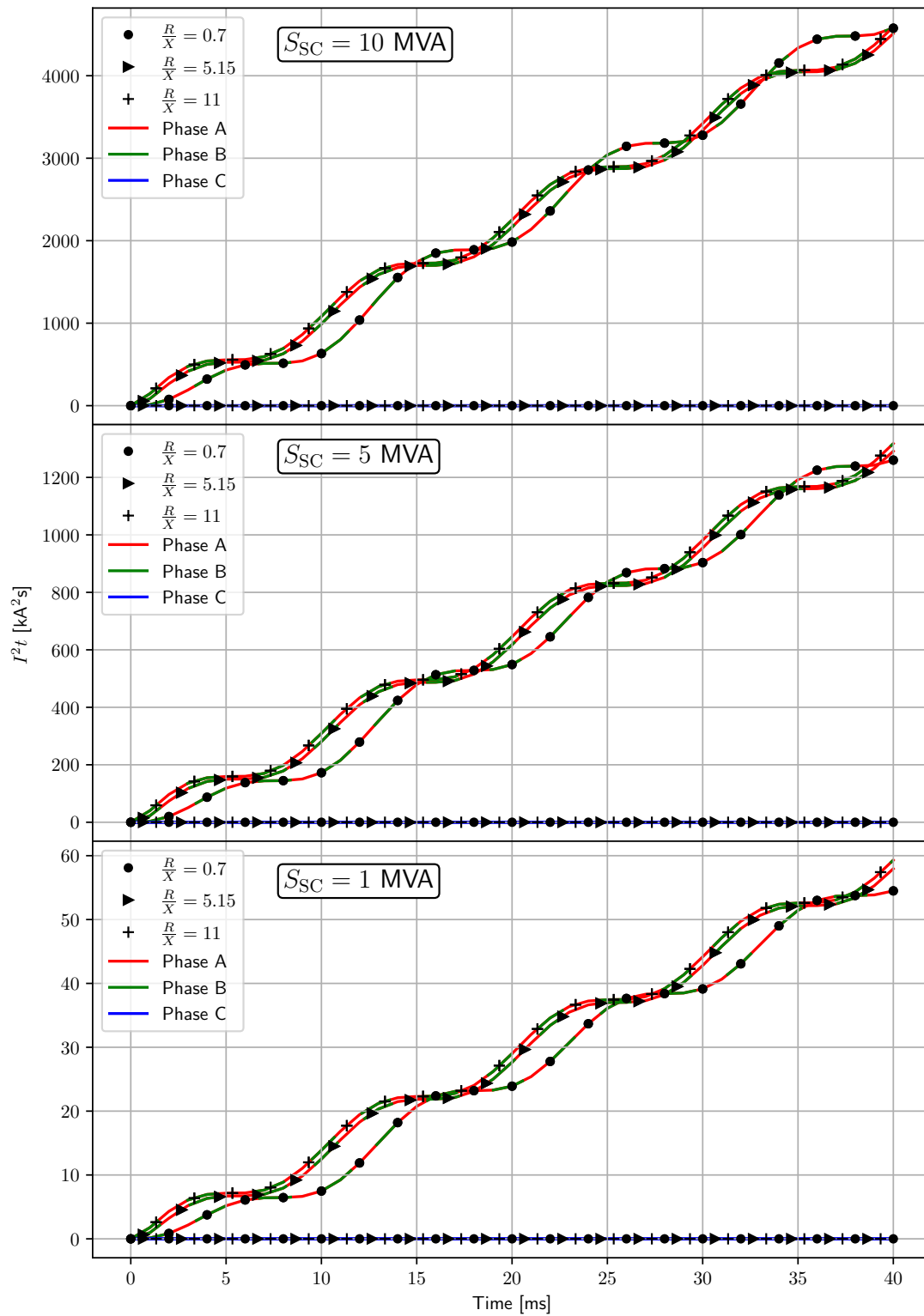


Figure 4.9: Energy let-through for different grid parameters during a line-to-line short circuit.

4.3.2 Line-to-Chassis Short Circuit

The phase currents during the line-to-chassis short-circuit event are shown in Figure 4.10. Two different short-circuit power ratings were used for the grid model, $S_{SC} = 10 \text{ MVA}$ and $S_{SC} = 1 \text{ MVA}$. The corresponding let-through energy (I^2t) for each case is shown in Figure 4.11. This metric is relevant for assessing the thermal stress on components during a short circuit

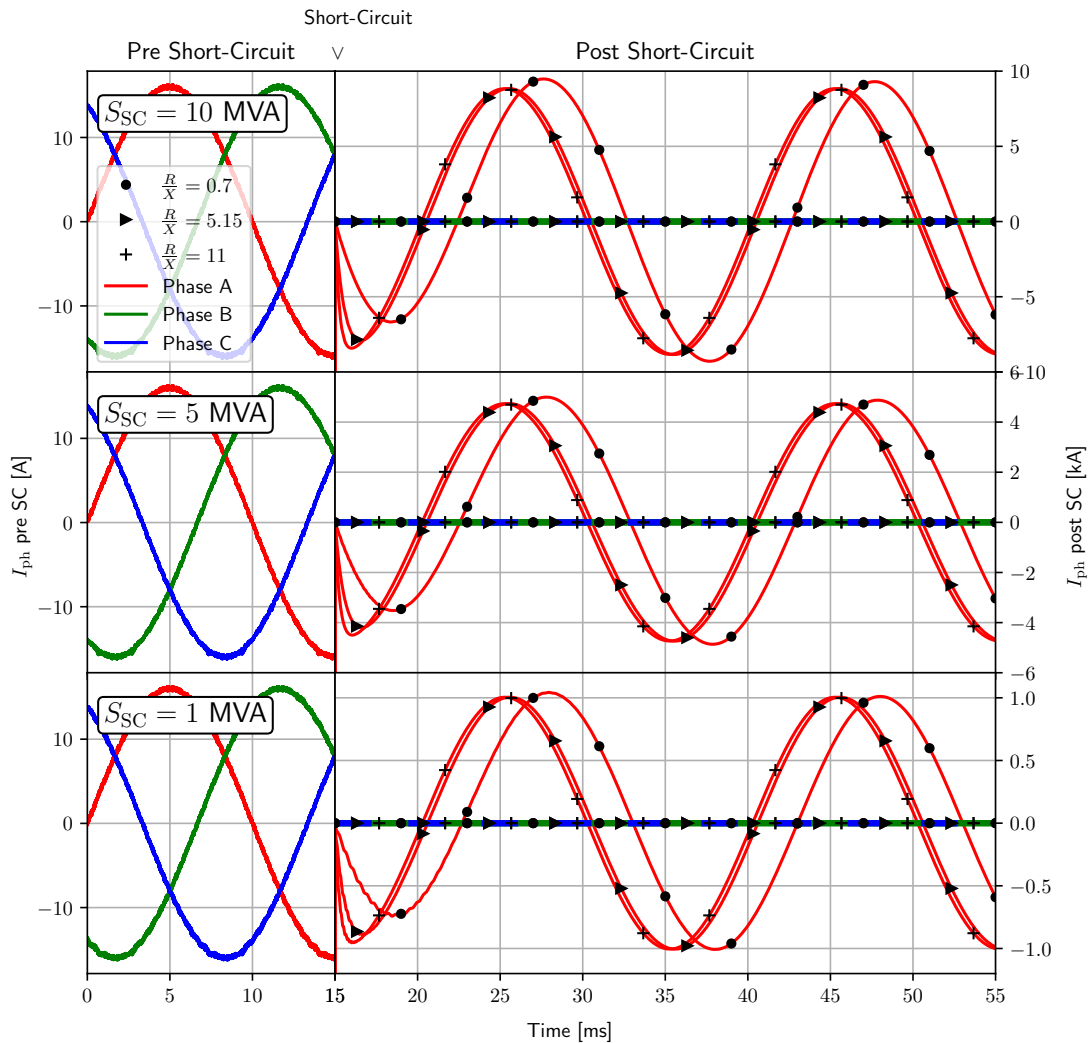


Figure 4.10: Line-to-chassis short-circuit simulation waveforms.

4. Results

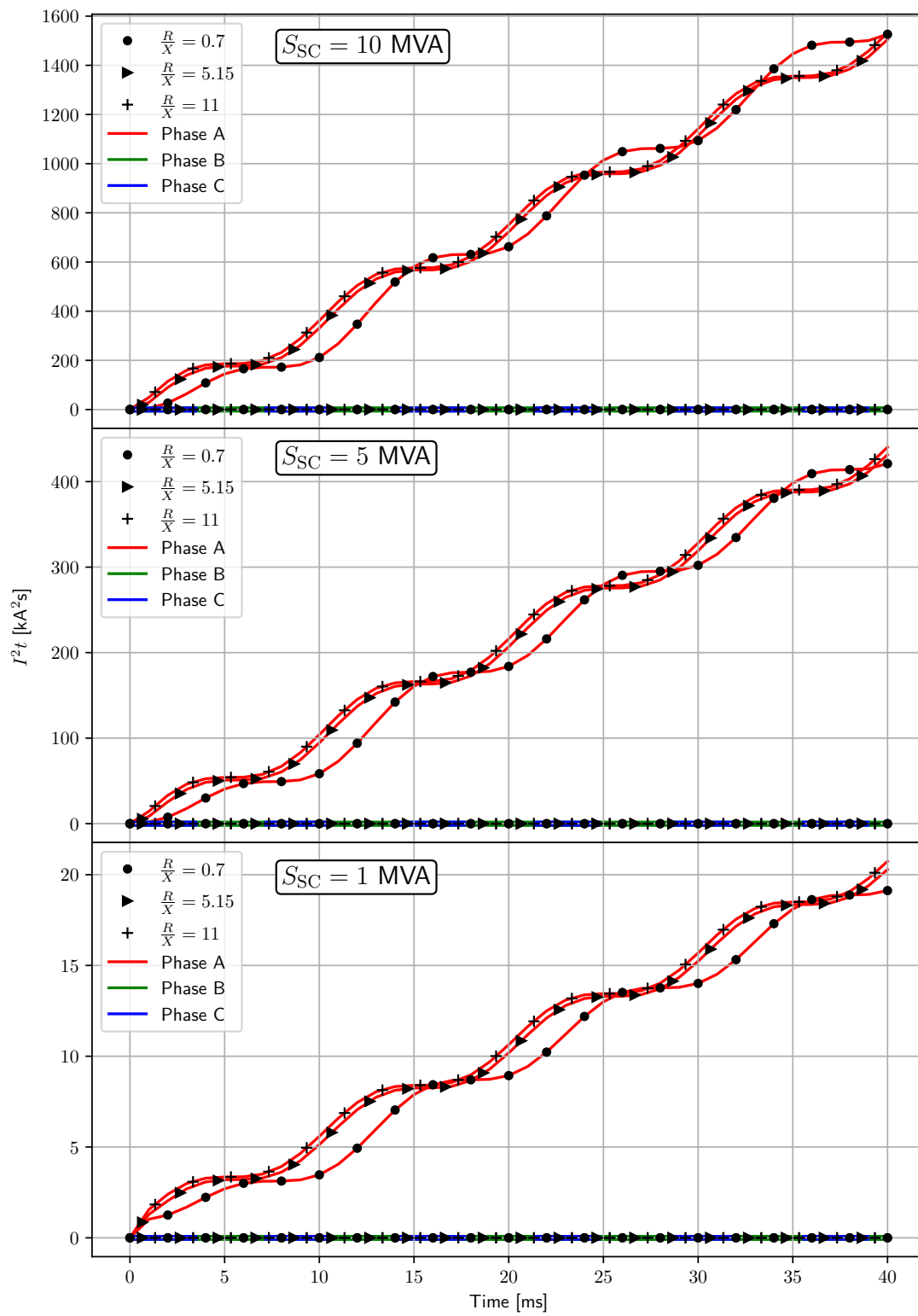


Figure 4.11: Energy let-through for different grid parameters during a line-to-chassis short circuit.

4.3.3 Bypass Short Circuit

The phase currents during the line-to-line short-circuit event are shown in Figure 4.12. Two different short-circuit power ratings were used for the grid model, $S_{SC} = 10 \text{ MVA}$ and $S_{SC} = 1 \text{ MVA}$. The corresponding let-through energy (I^2t) for each case is shown in Figure 4.13. This metric is relevant for assessing the thermal stress on components during a short circuit.

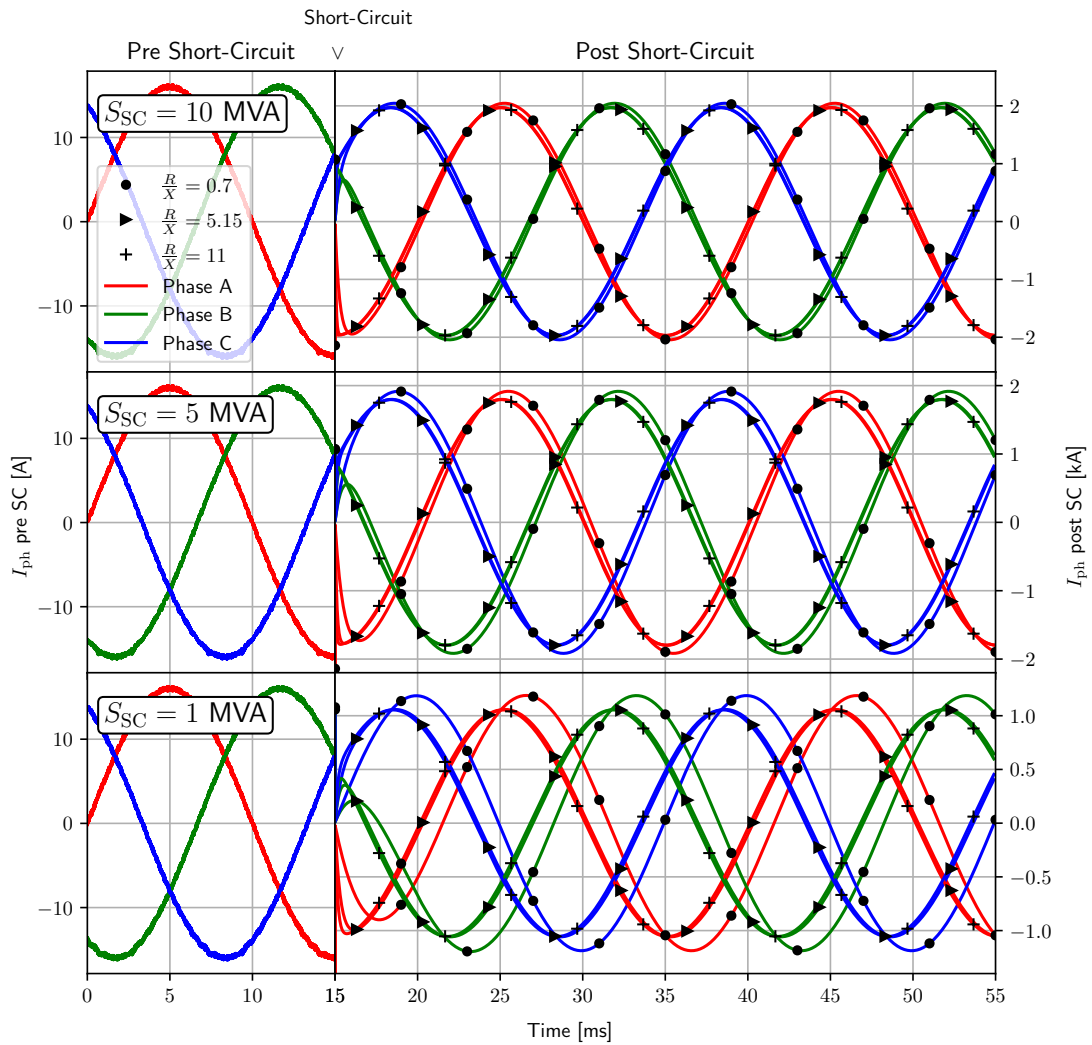


Figure 4.12: Bypass short-circuit simulation waveforms.

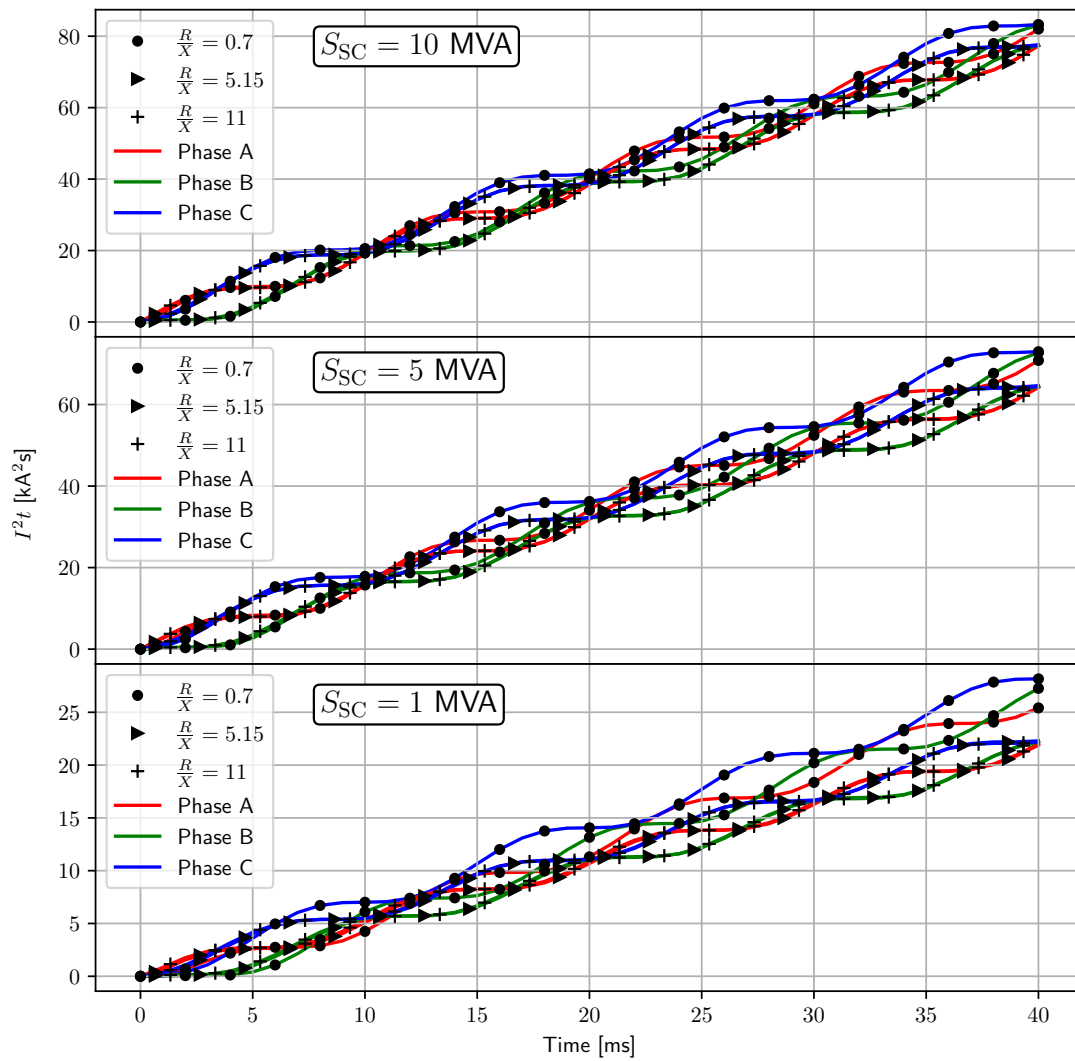


Figure 4.13: Energy let-through for different grid parameters during a bypass short circuit.

5

Discussion

This chapter analyzes the key findings from the measurements and simulations presented in the previous chapter.

5.1 Resonance

The observed resonance at 4 kHz is due to interaction between the common-mode choke and parasitic capacitance forming an LC circuit. This was verified by changing the values of the parasitic capacitance and the common-mode choke and observing that the resonant frequency was consistent with the LC-circuit equation $f_{\text{res}} = \frac{1}{2\pi\sqrt{L_{\text{CM}}C_{\text{prs.}}}}$, where L_{CM} is the common-mode choke inductance, and $C_{\text{prs.}}$ is the total parasitic capacitance of the model. Because the protective earth conductor was modeled without impedance, this resonance may be overestimated compared to a real system with impedance that damps the resonance. Nevertheless, it highlights the importance of designing the EMI filter to avoid excitation near resonant frequencies.

5.2 Leakage & Touch Current

The results in Table 4.2 show that the touch current is significantly higher than the legal limit of 3.5 mA RMS in all cases. The FFT:s show that the leakage current only consists of zero-sequence harmonics, namely multiples of the third harmonic of the grid frequency (150 Hz, 300 Hz, 450 Hz, etc.). This is intuitive since the leakage current must be caused by components in each phase that are constructively added. With ZSI the controller injects a zero-sequence voltage at 150 Hz, which is visible as a sinusoidal common-mode voltage measured at the Y-point of the converter. This explains why the leakage current during this simulation had a frequency of 150 Hz. It also explains why the simulation with ZSI gave the highest leakage current and touch current. What is interesting is that this 150 Hz leakage current still exists in the simulation without ZSI (albeit smaller in magnitude) and in the single-phase simulation, despite this frequency not being present in the grid voltages.

Since it does not originate from the grid in these simulations, the 150 Hz leakage current must therefore be caused by an imbalance in the parasitic capacitance. With flattened grid voltages, the leakage current had additional harmonics at 450 Hz, 750 Hz, and so on. The flattened voltages have a higher harmonic content because of the distortion in the sharp corners where the peaks have been flattened, and this is why there are more zero-sequence harmonics in the leakage current for this case. It is interesting that despite the high harmonic content of the flattened voltage peaks, the leakage current is lower than in the case of balanced grid voltages without ZSI. This once again hints at some type of imbalance in the parasitic capacitance.

5.3 Leakage Current Mechanisms

The behavior of the leakage current can be explained by recognizing that the CHB converter can be divided into different regions with uniform dv/dt . An example with a 9-level CHB converter using level-shifted carrier modulation is shown in Figure 5.1, where these regions are highlighted for an arbitrarily chosen point in time.

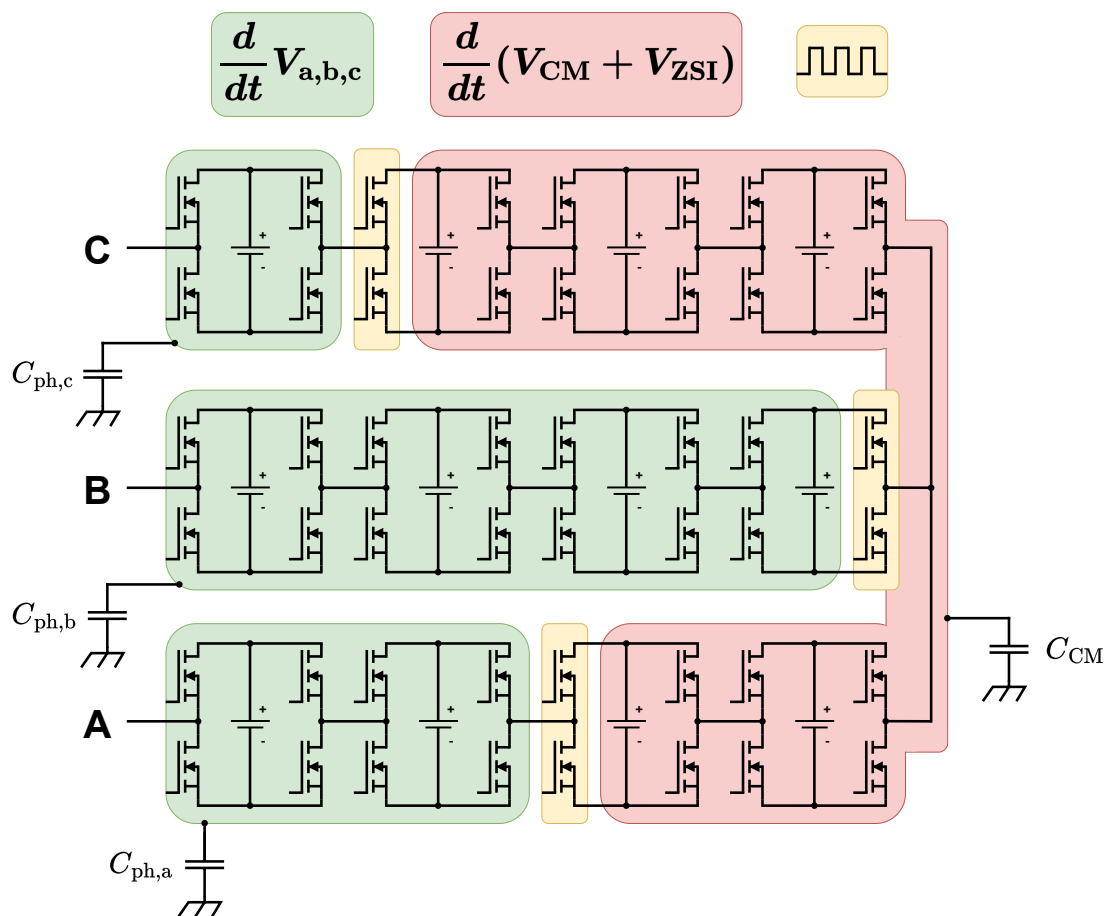


Figure 5.1: The different dv/dt -regions at a fixed point in time. The yellow regions show the location of PWM-pulsing.

The yellow regions show which half-bridge is actively switching with PWM. This *PWM-point* separates each CHB string into two regions, one that spans from the phase connection to the PWM-point (shown in green), and one that spans from the PWM-point to the Y-point (shown in red). The dv/dt of the phase voltages with respect to protective earth should be what causes leakage current to flow from the green regions. The red regions are all connected to the Y-point, and should therefore only contribute with leakage current if there is an imbalance from the grid or if the controller uses ZSI. Since the boundaries of the different regions are defined by the PWM-points, the parasitic capacitance is time dependent and nonlinear. This means that the parasitic capacitance forms an unbalanced load, in which leakage current will flow even if the grid voltages are balanced.

With the switching order used in the model, the parasitic capacitance of the green regions, $C_{\text{ph},i}$, as well as the leakage current from each region, $i_{\text{leak-ph},i}$, can be expressed as

$$C_{\text{ph},i}(t) = \frac{C_{\text{tot}}}{3N} \left| \text{floor} \left(\frac{v_i(t)}{V_{\text{bat}}} \right) \right|, \quad (5.1)$$

$$i_{\text{leak-ph},i}(t) = C_{\text{ph},i}(t) \frac{d}{dt} v_i(t) \quad (5.2)$$

where $i \in \{a, b, c\}$, C_{tot} is the total parasitic capacitance of the converter, N is the number of modules per phase, and V_{bat} is the voltage per module. The $\text{floor}()$ -function returns the largest integer that is less than or equal to the argument. An illustration of how $C_{\text{ph},i}(t)$ might change during operation is shown in Figure 5.2. The total leakage current caused by the green regions can now be expressed as the following sum

$$i_{\text{leak-ph}}(t) = \sum_{i \in \{a, b, c\}} \frac{C_{\text{tot}}}{3N} \left| \text{floor} \left(\frac{v_i(t)}{V_{\text{bat}}} \right) \right| \frac{d}{dt} v_i(t). \quad (5.3)$$

The red region should experience the common mode voltage of the grid and the zero-sequence injection from the converter. The parasitic capacitance and the leakage current of this region can therefore be expressed as

$$C_{\text{CM}} = \sum_{i \in \{a, b, c\}} \frac{C_{\text{tot}}}{3N} \left(N - \left| \text{floor} \left(\frac{v_i(t)}{V_{\text{bat}}} \right) \right| \right) \quad (5.4)$$

$$i_{\text{leak-CM}}(t) = C_{\text{CM}} \frac{d}{dt} (v_{\text{CM}}(t) - v_{\text{ZSI}}(t)). \quad (5.5)$$

The leakage of the entire converter should therefore be the sum of the leakage current from these two regions:

$$i_{\text{leak}}(t) = i_{\text{leak-ph}}(t) + i_{\text{leak-CM}}(t). \quad (5.6)$$

The equations presented were used to analyze the leakage current for the simulated cases, and a comparison is shown in Figure 5.3. The similarity is striking, and this finding means that future simulations can be run in a few seconds compared to the many hours that the current model needed. This also means that the leakage current is mostly independent of the phase current.

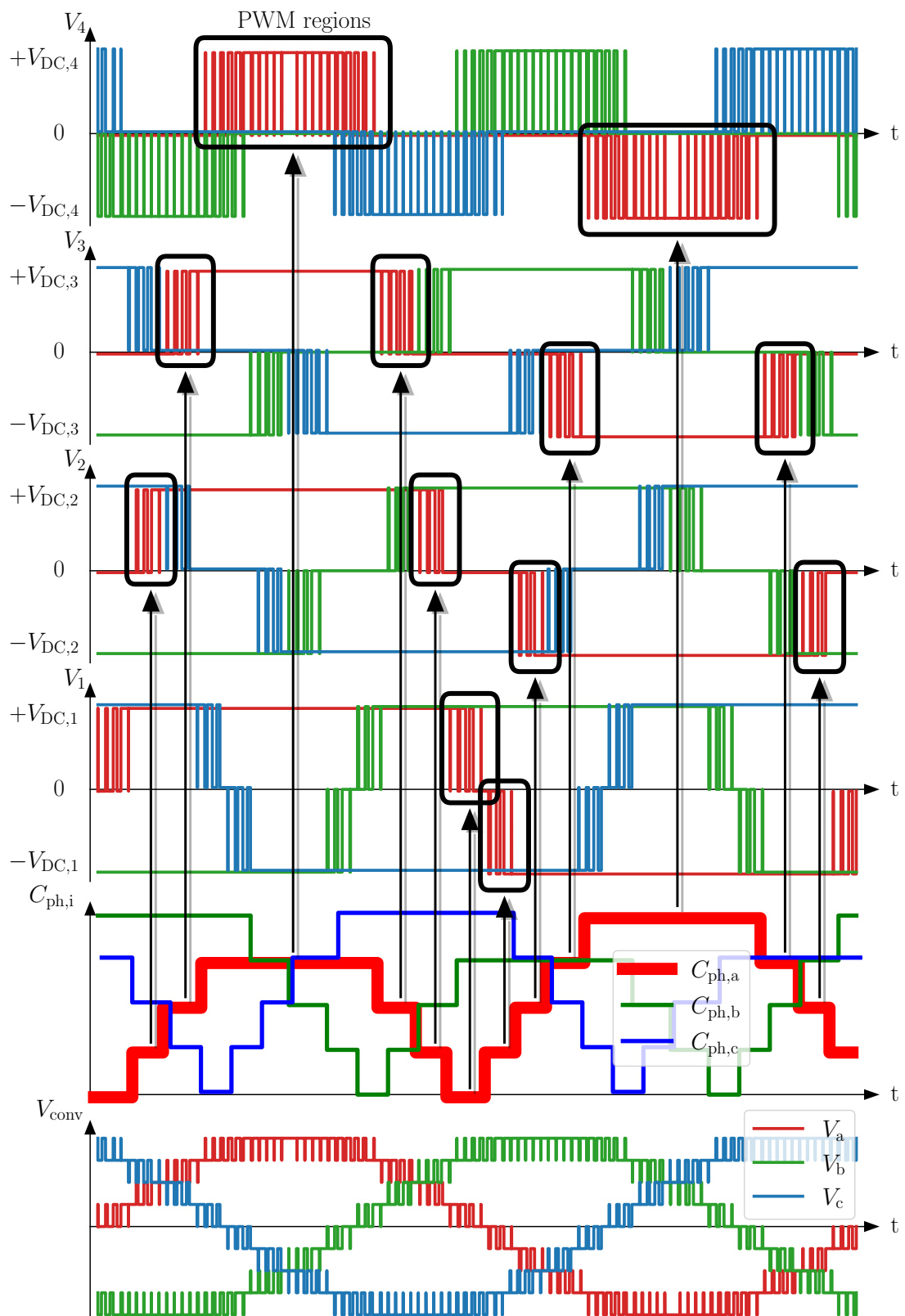


Figure 5.2: A visualization of the correlation between the PWM-regions and the effective capacitance per converter phase.

In a real application, the converter modules would need to be inserted according to a priority list to account for differences in SoC, temperature, and other parameters. Such parameters that the controller can observe can be used to form a state vector for each battery, B_{ij} , where i denotes the phase and $j \in \{1, 2, \dots, N\}$. The module that is doing PWM in phase i can then be expressed as a function of the battery states and the instantaneous phase voltage

$$s_i(t) = f(B_{i1}(t), B_{i2}(t), \dots, B_{iN}(t), v_i(t)), \quad i \in \{a, b, c\} \quad (5.7)$$

This can be used to change Equation 5.1 and 5.4 into the more general

$$C_{\text{ph},i}(t) = \frac{C_{\text{tot}}}{3N} \left(s_i(t) - \frac{q(t) \cdot \text{sign}(v_i(t)) + 1}{2} \right) \quad (5.8)$$

$$C_{\text{CM}}(t) = \sum_{i \in \{a,b,c\}} \frac{C_{\text{tot}}}{3N} \left(N - s_i(t) + \frac{q(t) \cdot \text{sign}(v_i(t)) + 1}{2} \right) = \quad (5.9)$$

$$= C_{\text{tot}} - \sum_{i \in \{a,b,c\}} C_{\text{ph},i}(t) \quad (5.10)$$

where $q(t)$ is either -1 or 1 and corresponds to whatever bypassed state the module with index $s_i(t)$ is using. The two ways to bypass a module are shown in Figure 2.3, indexed with letters c and d . $q(t) = -1$ corresponds to c being used, and $q(t) = 1$ corresponds to d being used. The reason this matters is that the bypass state determines which of the half-bridges in a module is doing the switching.

The equations given here may provide further insight into how to develop a prioritization function that also minimizes the leakage current.

5.4 Maximum Parasitic Capacitance

An approximate maximum limit to the parasitic capacitance can be formulated using the fact that the total impedance in the touch-current loop can be expressed as

$$Z_{\text{touch}} = \frac{1}{2\pi f C_{\text{prs}}} + Z_{\text{body}} \quad (5.11)$$

where C_{prs} is the total parasitic capacitance of the converter, Z_{body} is the impedance of the body model, and f is the frequency that will be set to the dominant leakage-current harmonic of 150 Hz. Since the highest simulated touch current was 17 mA RMS, and the legal limit is 3.5 mA, The minimum touch-current impedance should be

$$Z_{\text{touch,lim}} = \frac{17}{3.5} Z_{\text{touch}} \quad (5.12)$$

which gives the following equation where a maximum limit for the parasitic capacitance $C_{\text{prs,lim}}$ has been introduced:

$$\frac{1}{2\pi f C_{\text{prs,lim}}} + Z_{\text{body}} = \frac{17}{3.5} \left(\frac{1}{2\pi f C_{\text{prs}}} + Z_{\text{body}} \right). \quad (5.13)$$

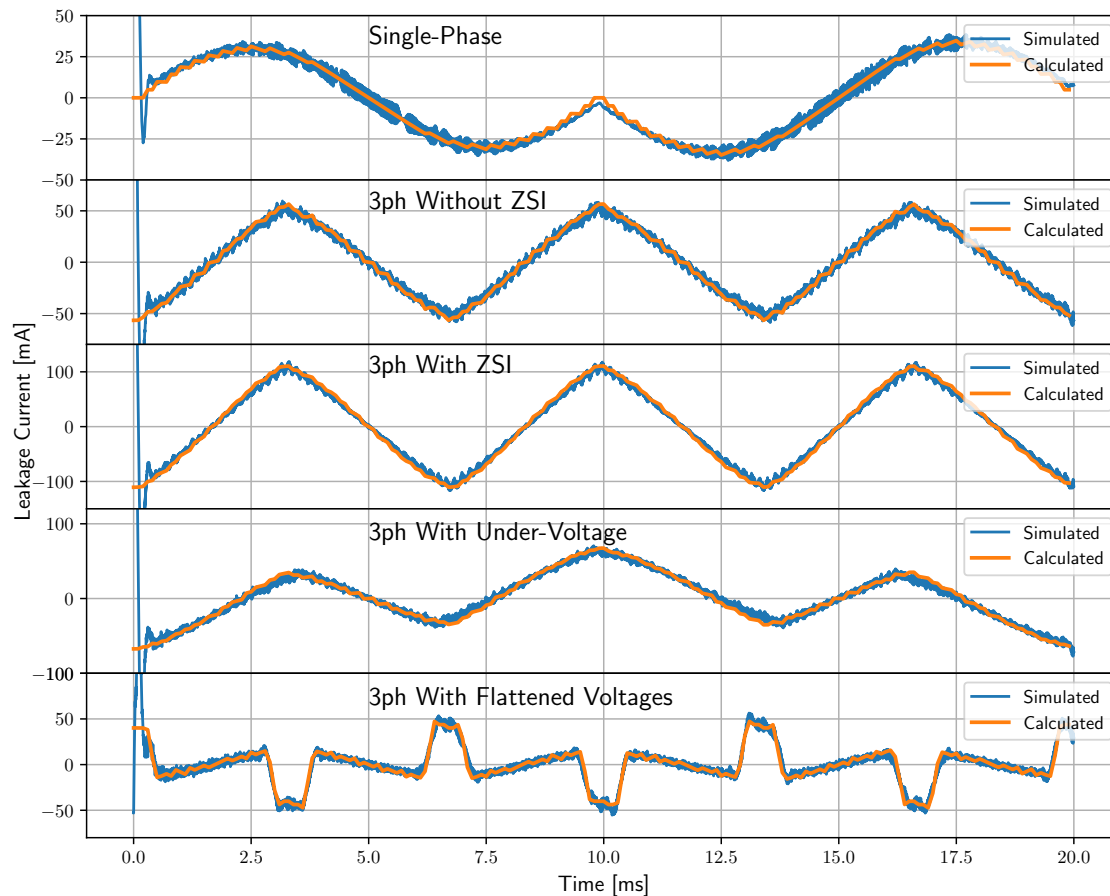


Figure 5.3: Comparison between simulations and calculations.

Solving for the maximum parasitic capacitance gives

$$C_{\text{prs,lim}} \approx 120 \text{ nF}. \quad (5.14)$$

This maximum limit assumes level-shifted carrier modulation with the same module mapping as in the simulations and is therefore not an exact number. A real application with a changing priority list will create a different frequency profile of the leakage current that goes against the assumption of the leakage current consisting only of 150 Hz. This maximum limit should therefore be seen as a rough estimate.

5.5 Resistance Imbalance

Another phenomenon, which is probably of less importance, might arise due to the difference in internal resistance of the modules as they are switching. A resistance model of a module is shown in Figure 5.4. There are always two MOSFETs conducting at the same time, each contributing with on-state resistance, $R_{\text{DS(on)}}$. When the CHB connects the battery, the ESR of the battery, R_{ESR} , is added to the converter. The internal time-averaged resistance of a converter string, R_{CHB} , can therefore be

expressed as a function of the reference voltage, V_{ref} :

$$R_{\text{CHB}}(t) = 2N R_{\text{DS(on)}} + \frac{R_{\text{ESR}}}{V_{\text{bat}}} |v_{\text{ref}}(t)|. \quad (5.15)$$

Since $v_{\text{ref}}(t) = \hat{V}_1 \sin(\omega_1 t)$, the second term is a resistance that varies proportionally to $|\sin(\omega_1 t)|$. The voltage drop caused by this resistance can therefore be expressed as a product of itself and the phase current, $\hat{I} \sin(\omega_1 t)$:

$$v_{\text{drop}}(t) = \frac{R_{\text{ESR}}}{V_{\text{bat}}} \hat{V}_1 \hat{I}_1 |\sin(\omega_1 t)| \sin(\omega_1 t). \quad (5.16)$$

The leakage current caused by this voltage drop would be

$$i_{\text{leak-R}}(t) = \frac{C_{\text{tot}}}{3} \frac{d}{dt} v_{\text{drop}}(t) \quad (5.17)$$

Due to the absolute value in the expression for the voltage drop, the leakage current caused by it should be unbalanced. Since the ESR of batteries can increase as they age (sometimes 2-3 times higher than its initial ESR), this effect should be considered during the design process. Even if the contribution is small, it might be of interest for the development of battery condition monitoring.

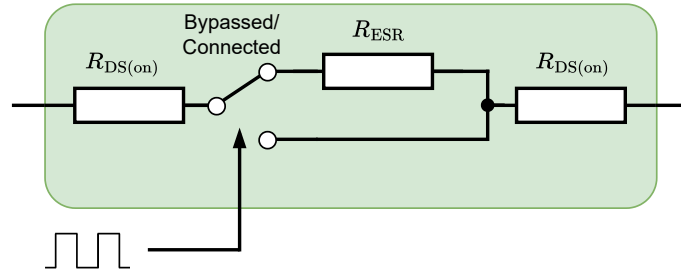


Figure 5.4: Resistance model of a CHB module.

5.6 Short Circuit

As expected, the simulated short circuits from Section 4.3 show a clear positive correlation between the short-circuit power of the grid and the let-through energy. However, it should be noted that the grid may have complex behavior that cannot be properly described by the simplified RL network that was used for the grid model. The highest short-circuit current was observed during the line-to-line short circuit. This is not surprising, as the line-to-line short circuit experiences the highest voltage drop. The most robust and safe design would therefore be achieved by dimensioning the protective devices for this type of short circuit.

None of the short-circuit currents show a visible asymmetry, and there are no delayed zero crossings, which means that the R/X -ratio is not small enough to cause problems for breakers. The impact of the R/X -ratio on the let-through energy is small

during bypass short circuit, but appears to have an increasing impact as the short-circuit power is reduced. The greatest impact of the R/X -ratio was observed in the line-to-chassis short circuit, shown in Figure 4.10. The simulations also showed a correlation between low short-circuit power and controller instability, as the phase currents started showing signs of resonance.

5.7 Future Work

The validity of the analytical model presented in Section 5.3 should be compared with real-life tests on a prototype. If valid, these equations enable fast estimation of the leakage current based on switching states, which makes it possible to explore a large number of control strategies without the need for time-consuming full-system simulations. An interesting direction for future work would therefore be the application of reinforcement learning to discover modulation and switching strategies that minimize leakage current. An example of how reinforcement learning could be performed is shown in Figure 5.5. In such an approach, the state space could be defined by observable converter and battery parameters, such as SoC, temperature, module availability, and instantaneous phase voltages. The action space would correspond to valid switching sequences or module selection strategies for each phase. A reward function can be designed to penalize high leakage current, possibly in combination with other objectives such as thermal balancing, SoC equalization, or efficiency.

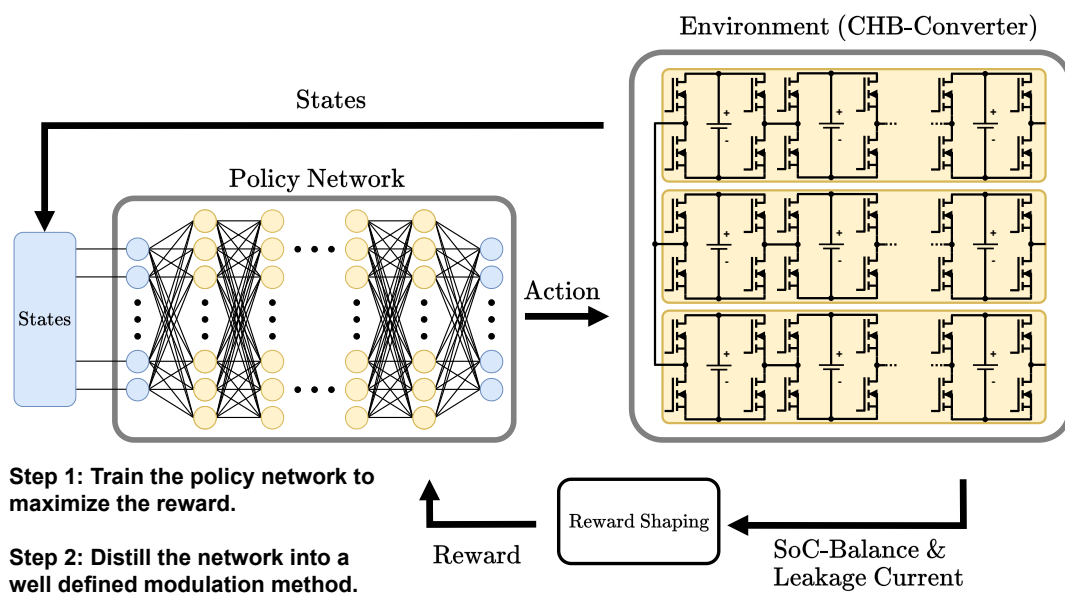


Figure 5.5: Reinforcement learning setup for minimizing leakage current. A neural network takes the states of the CHB converter (switching states, battery parameters, grid voltage/current etc.) and is trained to output the optimal action (modulation strategy).

Another line of research would be to investigate how the mapping of the CHB

modules affects the leakage current. One way of conducting such an investigation would be to use the analytical model with random mappings. This could then be used to get a better estimate of the maximum parasitic capacitance of the converter.

This work has been limited to the Swedish earthing system, which uses TN-C-S. Other earthing systems need to be explored to gain an understanding of possible region-specific challenges. An interesting line of work would be to collect time series voltage data for different power grids and run them through the analytical model.

The inconsistency in controller stability across the different grid parameters shows the need for a controller that can adapt to different power grids. An interesting line of study would therefore be to construct a more realistic grid model that can be tuned many different types of grid scenarios, and try to optimize controller stability and robustness.

6

Conclusions

This thesis has explored leakage current, touch current, and short-circuit conditions of a grid-connected CHB converter for battery charging. This was done by modeling the converter with parasitic capacitance measured from a prototype converter. The simulations revealed several interesting things, one of which being a high-frequency resonance most likely caused by parasitic capacitance in the converter and the common-mode inductor in the EMI-filter. This highlights the importance of good EMI-filter design. The simulated leakage current as well as the touch current were too high compared to electric vehicle standards, especially when using ZSI. The parasitic capacitance must therefore be kept at a minimum in a real design. An approximate maximum limit for the total parasitic capacitance of the converter was calculated to be 120 nF. Equations describing the leakage current were developed, which can be useful for developing a new modulation technique for the CHB converter that minimizes the leakage current while maintaining even charging of the cells. A powerful tool that could be used to find such a modulation technique is reinforcement learning, which would be an interesting idea for future research on the CHB converter. Simulations showed that the let-through energy was the highest during a line-to-line short circuit, and that the short-circuit power of the grid correlated positively with the short-circuit current. Changing the grid parameters appeared to affect the stability of the controller, which highlights the need for a controller that can adapt to different power grid scenarios.

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