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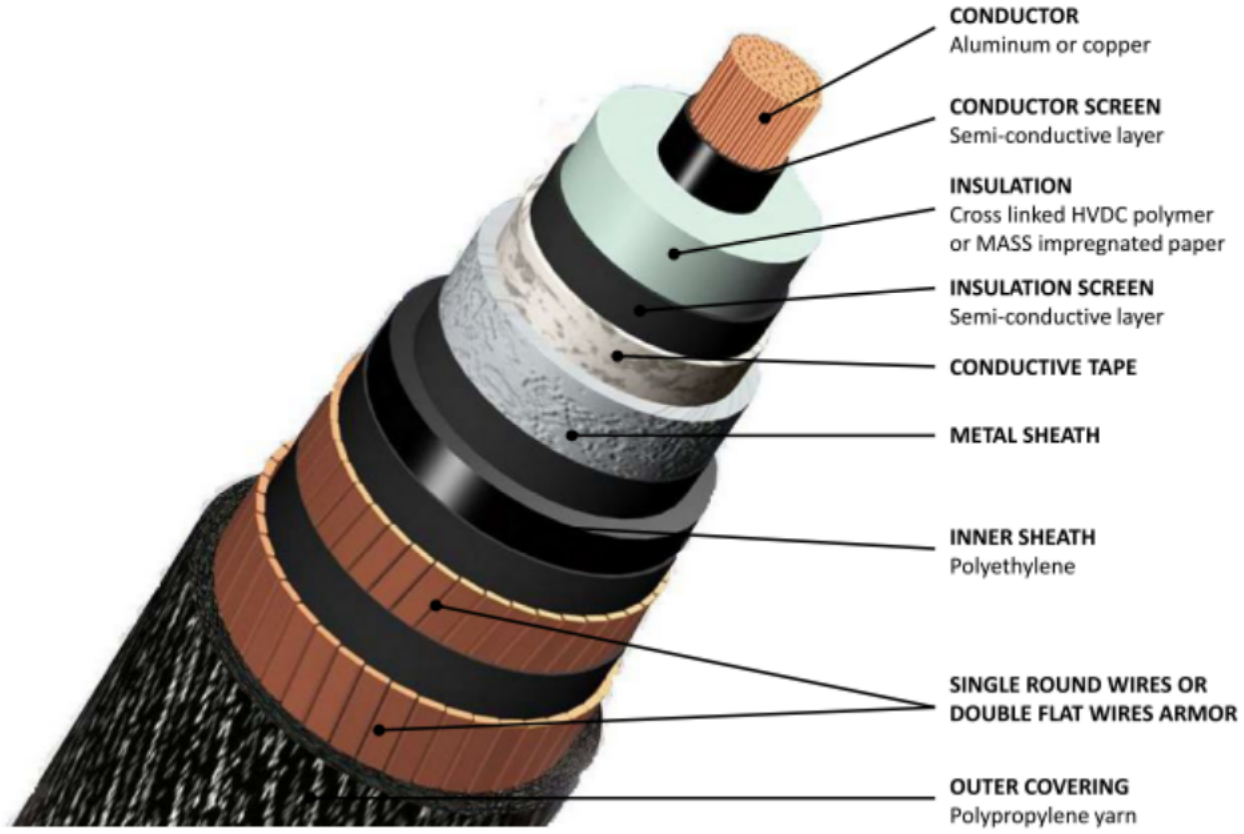

Investigating Overcurrent Stresses on 320 kV HVDC Cable Systems in a VSC-type Symmetrical Monopolar Configuration According to CIGRE Guidelines

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Department of Electrical Engineering
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Master's Thesis in Electrical Engineering

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Cover: Single core (XLPE) cable for AC or DC technology (Courtesy of Europacable).

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Abstract

In several recent High Voltage (HV) DC projects, Voltage Source Converters (VSC) have been the preferred choice of technology together with HVDC cable systems. Topologies of VSCs strongly affect performance of system components, including HVDC cable terminations, which are key elements providing connection of cable grids to external devices. Special testing procedures for HVDC cables terminations are not well defined today. Internal arc is such an exemplary special test for HVDC cable termination that simulates an internal termination fault. Different elements can be connected to the converter terminals such as DC capacitors and arm inductors, which can result in different travelling wave phenomena in the event of fault. In addition to system related stresses, HVDC cable terminations must withstand faults associated with internal arcing.

This report describes the work performed at NKT HV Cables AB in Karlskrona, Sweden, which aimed to investigate different types of faults in a 320 kV symmetrical monopolar cable system fed by a half bridge Modular Multilevel Converter (MMC) VSC. Overcurrents' profile (peak value and time duration) caused by different discharging mechanisms and grounding configurations have been analyzed by computer simulations using PSCAD software. Different types of faults have been simulated, which were permanent in nature and cleared with the help of AC breakers. The results obtained from simulations showed that the overcurrents during the fault were significantly higher at the midpoint of the cable. The peak overcurrent due to the pole-to-ground fault at the DC side of the converter terminals reached theoretical peak of discharge current defined by the ratio of the system voltage over characteristic cable impedance. Significant reflections of the fault currents were also observed during arm-to-ground faults. The performed study provided insight on the transient phenomena in HVDC cable systems during faults.

Keywords: HVDC, VSC, MMC, overcurrent, CIGRE, symmetrical monopolar, cable, PSCAD, faults.

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Last but not the least, my indebted gratitude to my parents and my sister for understanding and supporting me. Their constant encouragement proved to be a guiding path in every step of my life.

Palash Jain
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Introduction

1.1 Background

The Voltage Source Converters (VSCs) have proved to be more beneficial for the applications in High Voltage Direct Current (HVDC) transmission systems than the conventional Line Commutated Converters (LCC) [2]. The ever-increasing topologies associated with the VSCs for HVDC applications have imposed challenges in the cable systems [7]. Several short circuit requirements have been imposed on DC cable terminations for 320 kV level and beyond. However, it is not always known about an HVDC systems recommended way of requirement for testing of a HVDC cable termination. Differences at converter terminals, which consists of either DC capacitors or arm inductors, creates a difference in the travelling wave phenomena in the event of fault. In addition to such system related faults, cable systems, especially the cable terminations must withstand certain faults which might occur internally. Such internal faults in cable terminations are usually termed as "Internal Arc".

1.2 Aim

The aim of this thesis is to investigate the different types of fault that occurs on a 320 kV cable system in a symmetrical monopolar voltage source HVDC converter and thereby analyze the over-current (fault) profile caused due to different discharging mechanism and grounding.

1.3 Task

The main task of this thesis is to investigate different types of fault in 320 kV HVDC system. The main tool to execute the task has been PSCAD^{TM}/EMTDC^{TM} (hereinafter refered as PSCAD). The following are the sub-tasks:

- Modeling of HVDC converter based on CIGRE TB 604.
- Modeling the control aspects of HVDC converter to study its influence on the fault current profile.
- Various grounding configurations will be implemented to study its impact on fault currents.
- Results would then be compared with already performed tests at NKT.

1.4 Scope

This thesis will focus on fault investigation of 320 kV HVDC cable systems connected to symmetrical monopolar VSCs. Results would be achieved by modeling the HVDC system based on CIGRE parameters and definition. LCC type HVDC system configurations and bipolar topologies are beyond the scope of this thesis.

1.5 Thesis structure

In this thesis, chapter 2 describes the underlying theory of symmetrical monopolar MMC VSC-HVDC system. Chapter 3 describes the modelling methodology of symmetrical monopolar MMC VSC-HVDC system in PSCAD. Chapter 4 describes the results obtained by simulating various faults. Chapter 5 describes the sustainable and ethical aspects of the thesis. Chapter 6 concludes the thesis and discusses the future prospects.

2
Theory

This chapter discusses the background related to VSC-HVDC system. The comparision between VSC and LCC is explained in brief in section 2.1, different converter station configurations in section 2.2, components used in VSC-HVDC systems for the thesis in section 2.3 and converter topologies in section 2.4.

2.1 Voltage Sourced Converters Versus Line Commutated Converters

VSC-HVDC systems are preferred over conventional LCC-type HVDC systems as it allows the large scale integration of renewable energy sources with the Multi-Terminal DC (MTDC) grids [14]. VSCs are operated with Pulse Width Modulation (PWM) technique. This technique gives VSCs the ability to independently control both active power and reactive power [11]. Since the VSCs can control both frequency and AC voltage and can also consume and transport active power, they have the ability to assist black start [4]. VSCs also allow connection of different AC networks and large scale integration as the power flow can be changed by changing the direction of the current [17].

2.2 Converter Station Configuration for VSC-HVDC Systems

VSC-HVDC system uses three types of converter station configurations, namely asymmetrical monopolar, symmetrical monopolar and bipolar. All the three types of configurations are explained in the subsequent subsections.

2.2.1 Asymmetrical Monopolar Configuration

Figure 2.1 shows the point-to-point asymmetrical monopolar configuration. In this, a three phase AC connection is made at the midpoint of the phase legs inside the converter. There are two types of configurations possible, asymmetrical monopolar with metallic return and asymmetrical monopolar with earth return. In asymmetrical monopolar with earth return, only one insulated high voltage conductor is required and both the converters are grounded. In asymmetrical monopolar with metallic return, a return path is provided and the whole system is connected to a common ground. Metallic return configurations are provided in highly congested

areas, fresh water bed and high earth resistivity area. The symbol $\boxed{G}$ in figure 2.1 represents the possible grounding locations and the options can include bolted grounding, resistance grounding, inductive grounding, capacitive grounding or high impedance grounding [25].

From the reliability point of view, most asymmetrical monopolar systems consists of a metallic return. This is because in the event of outage or maintenance of the link, the opposite pole can be used for the transfer of power, which allows the uninterrupted supply [25].

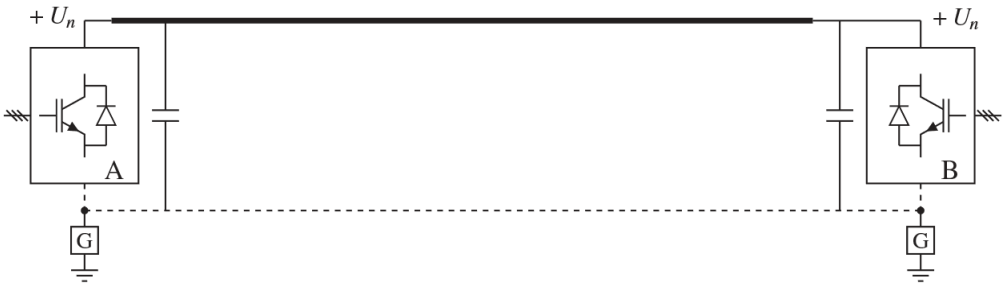

Figure 2.1: Asymmetrical monopolar configuration [13]

2.2.2 Symmetrical Monopolar Configuration

Figure 2.2 shows the point-to-point symmetrical monopolar configuration. The converters in this type of scheme consists of two DC terminals, each with positive and negative polarity. DC voltage at the converter terminals are same but have opposite polarities. If one of the converter fails, then this will result in the failure of the whole HVDC system [25]. A high impedance grounding is provided at the midpoint of the shunt capacitors. This configuration also consists of two insulated high voltage conductors. The selection of the conductors must be done according to the VSC design and it should also handle any contingencies that might occur in the system.

Figure 2.2: Symmetrical monopolar configuration [13]

2.2.3 Bipolar Configuration

Figure 2.3 shows the scheme of point-to-point bipolar configuration. It consist of two asymmetrical monopolar configurations which are connected through the common ground. At the AC side of the configuration, each of the converter has their own

transformers which are connected in parallel at their primaries. There is a possibility to use earth return or metallic return but in most of the cases, metallic return is preferred instead of earth return. This is so because, under normal operation of bipole, it must be ensured that a balanced mode is maintained by circulation of current between $+U_n$ and $-U_n$ poles, with zero current flowing through the ground. This zero current can have environmental effects if the return is through earth.

This configuration is more reliable when compared with asymmetrical monopolar and symmetrical monopolar. When there is an outage of a converter, the system can still operate at half of the transmission capacity of the configuration only when a metallic return is provided and grounding is done through earth. This configuration is also flexible as the two converter on one side can operate independently.

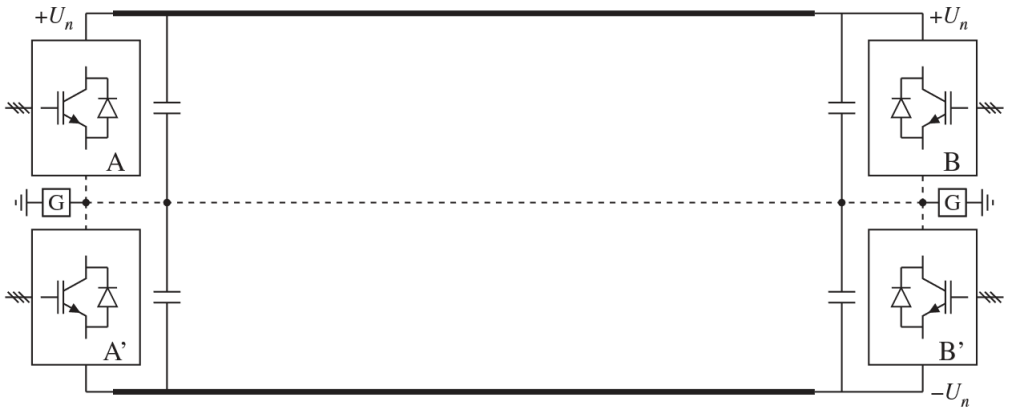

Figure 2.3: Bipolar configuration [13]

2.3 VSC-HVDC Components

VSC-HVDC scheme is represented in the figure 2.4. It consist of an AC grid, AC breaker, a transformer, star point reactor, converter station, DC capacitors and conductors (cable and transmission line). A control system is also present to be able to achieve timed switching of the valves.

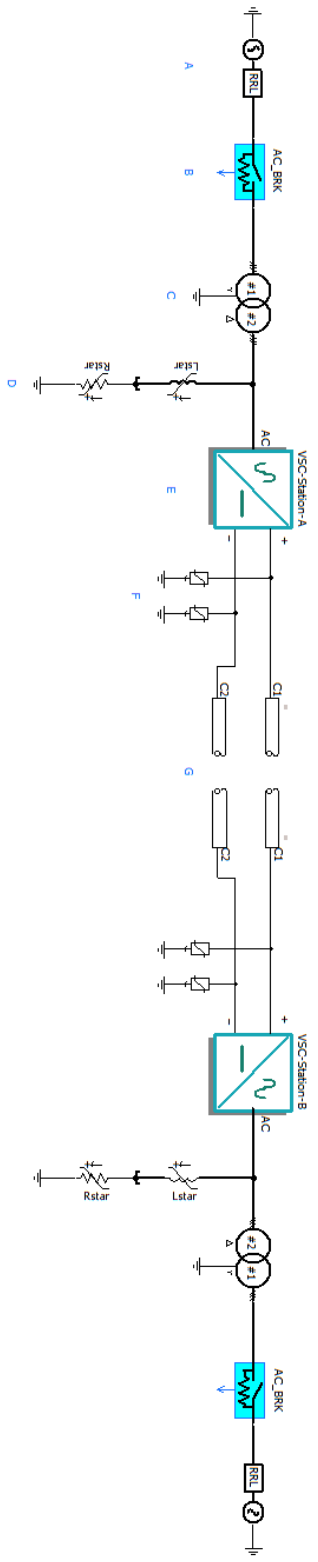

Figure 2.4: Symmetrical monopolar VSC-HVDC scheme. A) AC grid, B) AC breaker, C) transformer, D) star point reactor, E) converter station, F) DC surge arrester and G) conductors.

2.3.1 AC breaker

The component present after the busbar is an AC substation circuit breaker. This substation circuit breaker is placed between the AC transmission network and converter transmission network. These circuit breakers are used to switch the VSC substation in and out of the AC system. Special provisions are not required for the circuit breaker, however, if large filter banks are switched then the characteristics of capacitive switching needs to be taken into account [4].

2.3.2 Converter Transformer

The transformers used in the VSC substation provide reactances between the AC and VSC system, step up or step down of the AC voltage suitable for the AC system or VSC unit, increasing the number of pulse of the VSC system, connecting several VSC units having different DC voltage and not allowing the flow of zero sequence current [4]. The design of the transformers and reactors should be such that it can handle the stresses due to converter operation.

The connection configuration of three phase transformers is represented by vector groups. These groups are represented by symbols which signifies the connection of the phase type and the phase difference between high voltage (HV) and low voltage (LV) terminals of the transformers. The phase angles are represented by "clockface hour figure" [8]. For example, a Yd1 vector group represents:
Y = HV wye winding.
d = LV delta winding.
1 = clockface hour number, which signifies that LV vector is at 1 o'clock with respect to HV vector at 12 o'clock.

There are three types of winding connections, namely star/wye (Y or y), delta (Δ or D or d) and zig-zag (Z or z). Taking into account of these winding connections, different combinations can be made with respect to the phase shifts 0, 180, -30 and +30. These phase shifts can be categorized into four groups, which are given in the table 2.1.

Table 2.1: Connection combinations of different vector groups [8]

Group	**Clockface hour number Phase Shift**	**Combinations**			
Group I	0 o'clock 0^o phase shift	Yy0	Dd0	Dz0	Zd0
Group II	6 o'clock 180^o phase shift	Yy6	Dd6	Dz6	Zd6
Group III	1 o'clock -30^o phase shift	Yd1	Dy1	Yz1	Zy1
Group IV	11 o'clock $+30^o$ phase shift	Yd11	Dy11	Yz11	Zy11

2.3.3 Star Point Reactor

Star point reactors are connected between the secondary side of the transformer and the converter station. It consists of three inductors connected in wye with their neutral connected to the ground. The advantage of using a star point reactor is that it provides a low impedance path to the ground for DC so that DC current from the converter's AC side cannot flow through the transformer [10].

2.3.4 Valves

Valves are the most important component for the functioning of HVDC systems. These valves provide the capability to switch voltages and are generally connected in series.

The most commonly used switching component is Insulated Gate Bipolar Transistors (IGBT). Gate Turn Off thyristors (GTO) have also been used as a switching component but were replaced by IGBTs, since 2004 [4]. IGBTs have proved to be more advantageous than Metal Oxide Semiconductor - Field Effect Transistors (MOSFET), Bipolar Junction Transistors (BJT) and GTOs. IGBTs have the characteristics of having high value of impedance of the gate (as in MOSFETs), having small value of turn-on voltage (as in BJTs) and having the ability to block negative voltage (as in GTOs).

In VSC converters, IGBTs are equipped with a Free Wheeling Diode (FWD) which is connected in anti-parallel. These FWDs can be housed along with IGBTs or they can be connected in parallel with IGBTs in a separate housing. The function of FWD is to prevent reverse voltage and current capability in reverse direction [4].

2.3.5 DC Capacitors

The DC capacitors are connected in parallel to the converter DC terminals. These capacitors provide a stiff DC voltage (the magnitude of the source voltage is independent of the load connected to it) in order to operate the VSC unit. If there are any harmonics present after rectification then these DC capacitors will reduce them. The size of the capacitor will determine the ability to handle voltage variations which can be caused due to disturbances in the system.

In general, for MMC VSC-HVDC systems, the physical capacitor banks are not used when compared with two-level and three-level converters. Instead, the submodules contain a submodule capacitors which acts as a DC capacitor. The different submodule topologies are later explained in section 2.4.

2.3.6 Conductors

Cables and transmission lines serves as conductors for the power transfer between the converter stations. The choice of either cables or transmission lines for the VSC system depends on several factors, which are listed below:

- Transmission line contributes to the environmental impact when compared with cables.
- Unlike LCC systems, in which the power flow is determined by the DC voltage polarity, the cables for the VSC systems are not required to be designed for voltage polarity reversal.
- The exposure to lightning and pollution makes the transmission lines much more susceptible to faults when compared with cables. In transmission line, the faults are much more easy to repair and can be put again for commissioning after fault rectification.

There are different types of cables used in the HVDC systems such as mass impregnated nondraining (MIND) cables, oil-filled (OF) cables, polypropylene paper laminate (PPL, MI-PPL, PPLP) cables and polymer-insulated or extruded insulation cables [16]. Among those, polymer-insulated or extruded insulation cables, such as cross-linking polyethene (XLPE), are used in the VSC-HVDC system because they are light in weight and flexible, which in-turn provides easy installation. In addition, XLPE cables pose no risk to environment and marine life.

2.3.7 Control Systems

Control system is required for the switching of valves in VSC converters by feeding gate pulses to the valves. There are several techniques to control the HVDC systems, the most prominent being the direct control and vector control. In direct control, the parameters (modulation index and phase angles) are directly controlled whereas in vector control the parameters are adjusted by independently controlling the active and reactive power. This makes the vector control strategy more advantageous than direct control strategy. Vector control strategy has been implemented in the presented modelling work.

The control system for MMC VSC HVDC system can be divided into three types of controls namely dispatch control, upper level control and low level control. The hierarchy of the control system is shown in the figure 2.5 and different types of control in control systems are explained in the subsequent subsections.

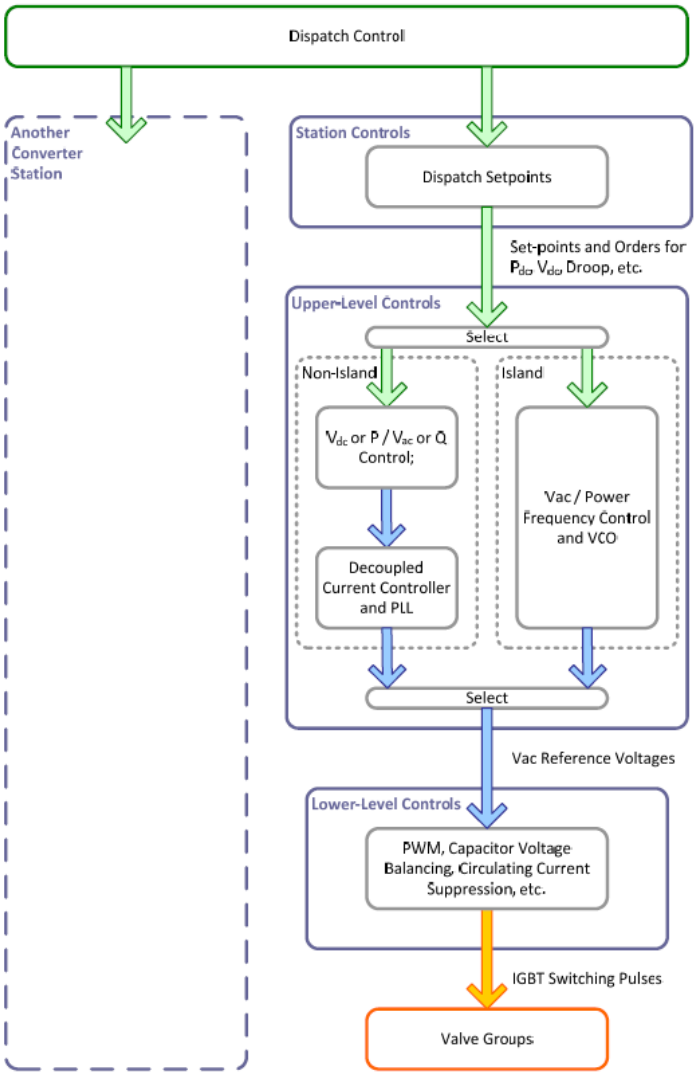

Figure 2.5: Generic control system hierarchy of VSC-HVDC converter [5]. Recommended for multi-terminal systems; indicated here for representative purposes

Dispatch control sets the reference points for the converter. Outer level control helps in generating direct axis and quadrature axis currents. Inner level control regulates these currents to generate three phase voltages. Lower level controls the firing pulse for timed switching of valves.

2.3.7.1 Dispatch Control

The dispatch control is responsible for managing the set points or the control modes which are required for the control of converter. The set points can be V_{dc}, V_{ac} etc., and the control modes can be the DC voltage (V_{DC}) control, active power (P) control, reactive power control (Q) and AC voltage control (V_{AC}). These set points and control modes are required by the upper level control as shown in figure 2.5. In real systems, the dispatch controls are coordinated by a DC grid system operator.

2.3.7.2 Upper Level Control

The reference values of P, Q, V_{AC} and V_{DC} are sent from the dispatch to the upper level control. In the upper level control, a choice is made between non-islanded and islanded mode of operation. If non-islanded mode is selected then it signifies that the control system is connected to a synchronous system. If islanded mode is selected then it signifies that the control system is connected to an asynchronous system. Since the analysis is made in steady state, the non-islanded mode of control system operation has been selected for the presented work of thesis.

The upper level controls can be further explained in two parts. These are outer control and inner control, which are described in the following sections and shown in figure 2.6.

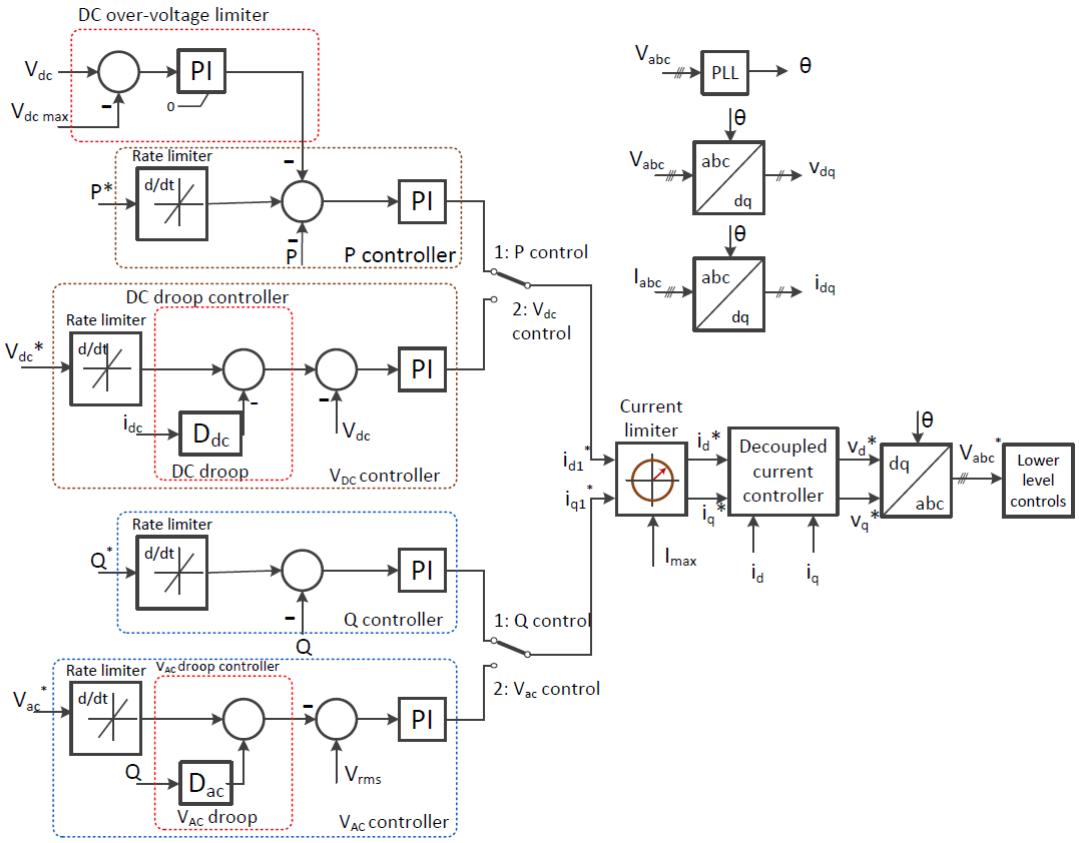

Figure 2.6: Upper level control configuration for non-islanded operation [5].

2.3.7.2.1 Outer Control In figure 2.6, the outer control consists of two types of control modes. These are direct (d) axis control and quadrature (q) axis control. The d-axis control consists of the following:

- Active power control loop:
  It consists of DC over-voltage limiter and active power controller. The DC over-voltage limiter limits the DC voltage to a pre-specified maximum value of DC voltage. The output of the DC over-voltage limiter is fed into the active power controller which gives reference d-axis current (i^*_{d1}).

- DC voltage control loop:
  It consists of a DC droop controller and DC voltage controller. The DC current (i_{dc}) is fed into the DC droop (D_{dc}) and the output is then fed into the DC voltage controller which gives i^*_{d1}.

The q-axis control consists of the following:

- Reactive power control loop:
  It consists of a reactive power controller which takes reference reactive power as an input. The output of the reactive power controller gives the reference q-axis current (i^*_{q1}).
- AC voltage control loop:
  It consists of an AC droop controller and AC voltage controller. The reactive power is fed into the AC droop (D_{ac}) and the output is then fed into the AC voltage controller which gives i^*_{q1}.

The output of outer control i.e. i^*_{d1} and i^*_{q1}, is then fed into the inner control.

2.3.7.2.2 Inner Control The inner or current control systems controls the i^*_{d1} and i^*_{q1} which is received as an output from the outer control. These outputs are fed into the current limiter which limits the current by comparing it with the maximum value of the current. The output of the current limiter i.e. i^*_d and i^*_q is fed into the decoupled current controller which allows the independent control of d and q currents and voltages. The output of this current controller gives the d and q voltages i.e. V^*_d and V^*_q. These voltages are fed into the inverse Park transformation module giving 3 phase output voltage. This output voltage is feed into the low level control.

2.3.7.3 Low Level Control

The output from the upper level control is fed into the low level control. The low level control is responsible for the generation of firing pulses which can be used as an input to the gate terminal of IGBT for timed switching of the submodules. The design of low level control depends upon the VSC configurations and the type of valves used in the converter systems. The firing control depends upon the type of mode of operation. If the mode of operation is selected as non-islanded, then phase locked loop (PLL) is used. If the mode of operation is selected as islanded, then independently locked loop is used [4].

2.4 Converter Topologies

There are two converter topologies in a symmetrical monopolar configuration. The half bridge topology is shown in figure 2.7 and full bridge or H bridge topology is shown in figure 2.9. Each of these topologies are explained in the following subsections.

2.4.1 Half Bridge Module

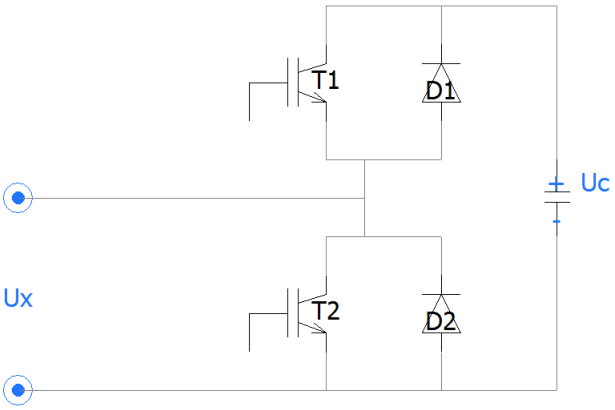

Figure 2.7: Half bridge converter topology

Half bridge module consists of two anti-parallel IGBTs and diodes. Two of these modules are then connected in series and a small capacitor is connected in parallel across the two switches. This module gives two output levels which are positive voltage and zero voltage. Positive voltage is obtained by turning on the switch T1, whereas zero voltage is obtained by turning on the switch T2 [25].

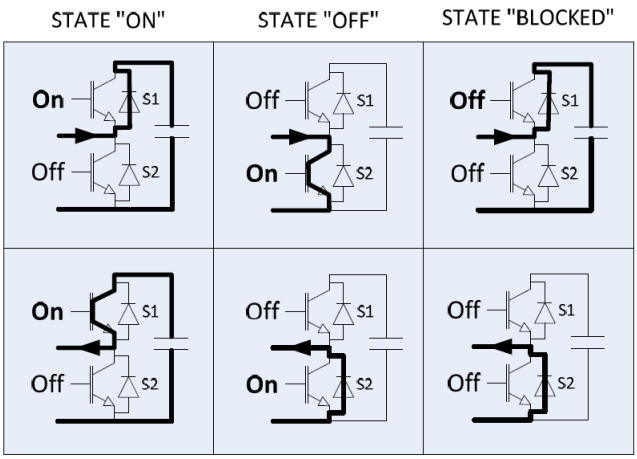

Figure 2.8: Operating state of half bridge cell [5]

Half bridge module can be operated in on, off and blocked state, which is shown in figure 2.8. When the cell is in ON state, depending on the direction of current, the current will pass through either upper diode or upper switch, charging or discharging the capacitor, respectively. When the cell is in OFF state, depending on the direction of current, the current will pass through the lower switch or lower diode, keeping the voltage across the capacitor constant. When the cell is in BLOCKED state, depending on the direction of current, it will either charge or maintain the voltage across capacitor constant.

2.4.2 Full Bridge or H-Bridge Module

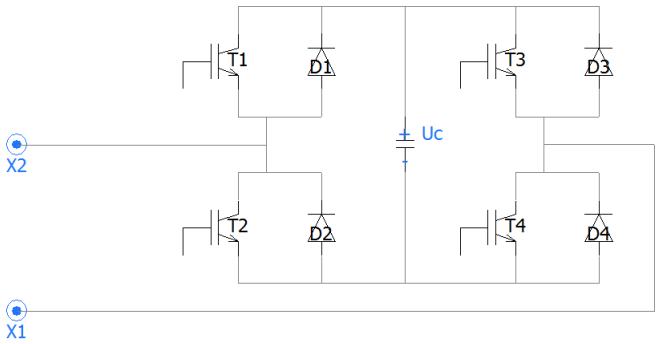

Figure 2.9: Full bridge or H bridge converter topology

Full bridge or H bridge module consist of four parallelly connected IGBTs and diode modules, altogether connected in parallel with a small capacitor. This module gives 3 output levels which are positive, negative and zero voltage. Positive and negative voltage levels are obtained by turning on T1/T4 or T2/T3 which leads to the charging of the capacitor in either direction. Zero voltage level is obtained by turning on T1/T3 or T2/T4 which results in discharge of the capacitor.

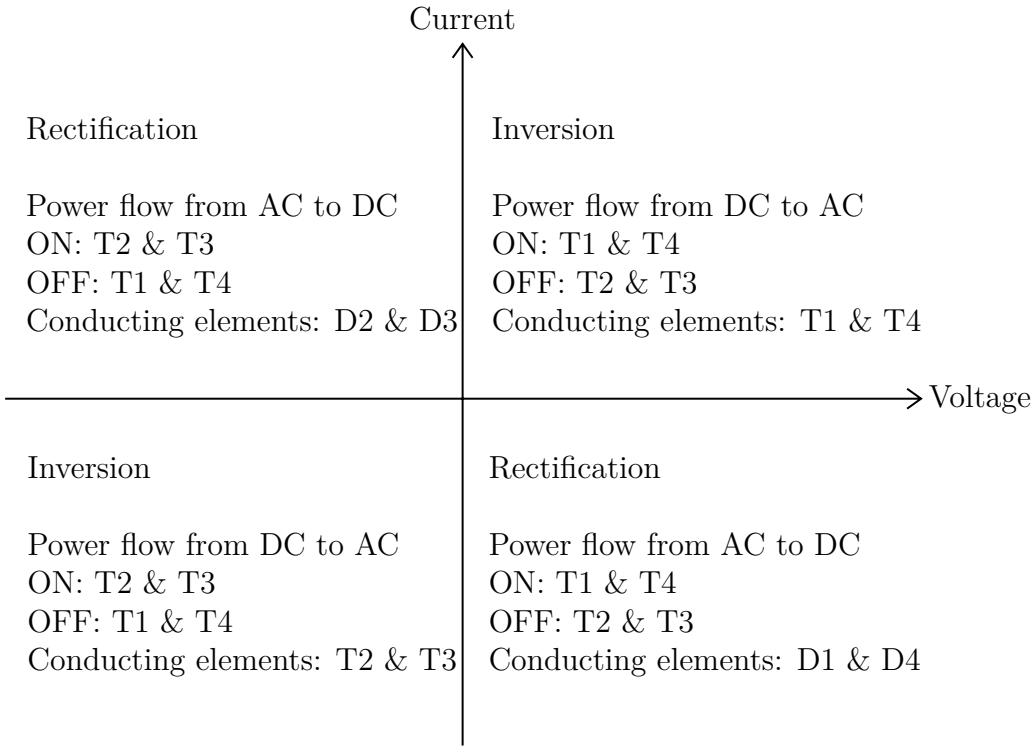

Figure 2.10: Four quadrant operation of full bridge or H bridge module

The four quadrant operation of full bridge module is shown in the figure 2.10. Rectification and inversion are the two modes of operation in the full bridge module. When the power flow is from DC to AC, then inversion operation takes place. In

this case, IGBT T1 and T4 operation results in positive output current and voltage and IGBT T2 and T3 operation results in negative output current and voltage. Similarly, when the power flow is from AC to DC, then rectification operation takes place. In this case, diodes D1 and D4 operation results in positive output voltage and negative output current and diodes D2 and D3 operation results in negative output voltage and positive output current.

3

HVDC System Modelling

This chapter discusses the methodology of symmetrical monopolar VSC-HVDC system modelling. The tool used for modelling purposes is PSCAD (Power System Computer Aided Design). PSCAD is an electromagnetic transient (EMT) simulation tool where the user can model the circuit, simulate it and analyze the results. Section 3.1 describes the modeling of AC side components which includes AC grid, AC breaker, transformer and star point reactor; section 3.2 describes the modelling of DC side components which includes MMC VSC station modelling and cable modelling.

3.1 AC side modelling

This section discusses the modelling of AC side components used in the thesis. The components includes AC grid, AC breaker, transformer and star point reactor as shown in the figure 3.1.

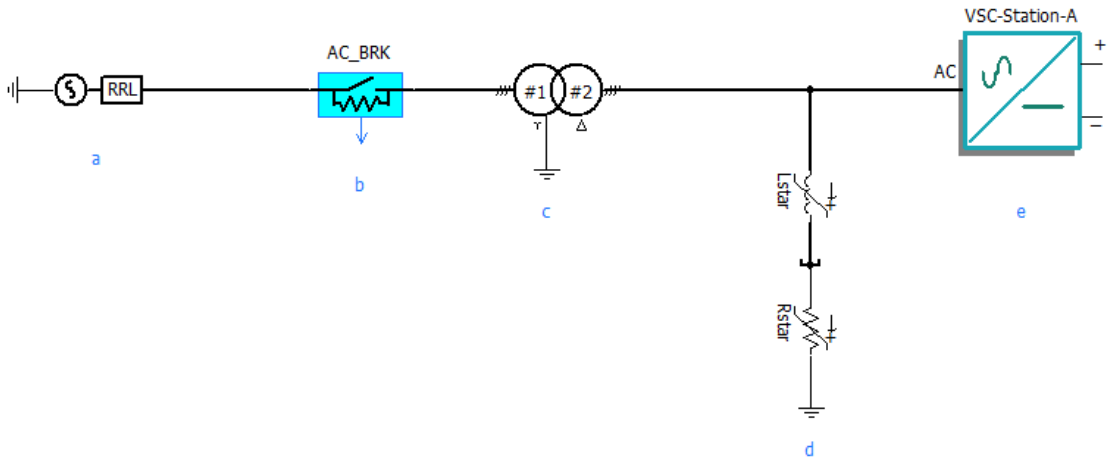

Figure 3.1: AC side model in PSCAD. a) AC grid, b) AC breaker, c) transformer, d) star point reactor and e) converter station

The modelling of the mentioned components are described in the subsequent subsections.

3.1.1 AC grid

The AC grid is modeled by an equivalent AC source impedance consisting of a source resistance and source inductance, and line to line (L-L) root mean square (RMS) value of the source voltage. To determine the value of the AC source impedance, short circuit level (SCL) is used. SCL is defined as

$$SCL = \frac{V_{L-L\_RMS}^2}{Z_{source}} \tag{3.1}$$

where,
V_{L-L_RMS} is the line to line root mean square value of the source voltage in kV, and Z_{source} is the source impedance in Ω.

To calculate the value of source resistance and source inductance, the value of X/R ratio needs to be assumed. X/R ratio is defined as the ratio of source reactance to the source resistance. Due to the nature of the AC network being highly inductive, the value of X/R ratio can be assumed as 10. The source resistance (R_{source}) and source inductance (L_{source}) can now be calculated as,

$$R_{source} = \sqrt{\frac{Z_{source}^2}{(X/R)^2 + 1}} \tag{3.2}$$

$$L_{source} = (X/R) \cdot \frac{R_{source}}{2 \cdot \pi \cdot f} \tag{3.3}$$

where,
f is the frequency of the AC gird in Hz.

The AC grid parameter for symmetrical monopolar VSC-HVDC system is given in table 3.1 [5].

Table 3.1: AC grid parameter for symmetrical monopolar VSC-HVDC system [5]

Parameter	**Value**
Short Circuit Level	30 GVA
Voltage Magnitude (L-L RMS)	400 kV
Frequency	50 Hz
X/R Ratio	10

3.1.2 AC breaker

The model of the AC breaker in PSCAD is shown in figure 3.2. It consist of a main breaker (MainBrk), auxiliary breaker (AuxBrk) and a pre-insertion resistor (preR) [5]. The main breaker is connected in parallel with the series connection of auxiliary breaker and pre-insertion resistor. The use of pre-insertion resistor is to reduce the inrush current during the start up of the VSC which results in less stress on the free wheeling diode in the converter.

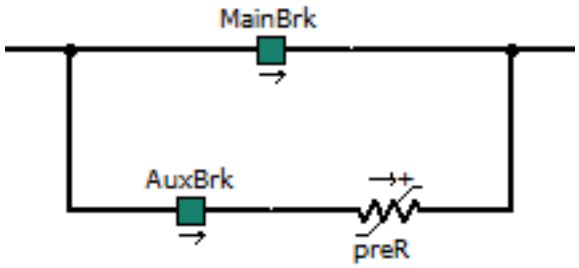

Figure 3.2: AC breaker model in PSCAD

At a certain time, the pre-insertion resistor is connected via the auxiliary breaker while the main breaker is open. After a certain delay, the pre-insertion resistor is bypassed by closing the main breaker. The auxiliary breaker is opened immediately when the main breaker is closed.

In this thesis, the pre-insertion resistors are disabled as only steady-state analysis of VSC-HVDC system are performed. The AC breaker parameters for a symmetrical monopolar VSC-HVDC system is shown in table 3.2 [5].

Table 3.2: AC breaker parameter for symmetrical monopolar VSC-HVDC system [5]

Parameter	**Value**
Breaker closing time	600 ms
Breaker opening time	100 ms

3.1.3 Transformer

Transformer parameters are shown in table 3.3. A 400/320 kV, 1060 MVA, Y/Δ transformer is considered for this thesis [5, 19]. The neutral of the primary side or the grid side of the transformer is solidly grounded. The reason for choosing this configuration of the transformer is that the secondary side voltage is shifted by 30^o with respect to the primary side voltage which reduces the lower order harmonics [3].

Table 3.3: Transformer parameter for symmetrical monopolar VSC-HVDC system [5, 19]

Parameter	Value
3 phase transformer MVA	1060 MVA
Base operation frequency	50 Hz
Nominal voltage at the grid side (L-L RMS)	400 kV
Nominal voltage at the converter side (L-L RMS)	320 kV
Vector group	YNd-11
Transformer leakage reactance	0.18 pu
No load losses	0 pu
Load losses	0.006 pu
Magnetizing current	1 %

3.1.4 Star point reactor

As discussed in section 2.3.3, a star point reactor is used to provide a low impedance path at the delta side of the transformer. It is generally a high impedance component in order to reduce the reactive power consumption. It is also equipped with a grounding resistor of a suitable value. If this value is high, then the star point reactor is considered as ungrounded. Table 3.4 shows the star point reactor parameters for symmetrical monopolar VSC-HVDC system.

Table 3.4: Star point reactor parameter for symmetrical monopolar VSC-HVDC system [5]

Parameter	Value
Inductance	5000 H
Resistance	5000 Ω

3.2 DC side modelling

This section describes the modelling of the components which are present at the DC side of the HVDC system.

3.2.1 Symmetrical monopolar MMC VSC-HVDC modelling

In order to model the symmetrical monopolar MMC VSC-HVDC converter for the transient studies, a detailed equivalent circuit model is implemented in this thesis as it reduces the time of computation by reducing the number of electrical points as well as maintain accuracy [5].

The converter is a modular multilevel converter which consisting of submodules in each phase leg. The number of submodules determines how many levels or pulses can be generated. The expression is given as

$$Number\ of\ levels = N_{arm} + 1 \tag{3.4}$$

where,
N_{arm} represents the number of submodules per arm; where arm is defined as half of each phase leg.

Each submodule can be modelled as either a half bridge cell or as a full bridge cell. For this thesis, half bridge cells are considered for each submodule. The half bridge cell consists of two anti-parallel IGBT and two free wheeling diodes connected in series and a submodule capacitor in parallel with the IGBTs. For MMC converters, physical DC link capacitor banks are not required when comparing with 2 or 3 level converters as the submodule capacitors serves the purpose of a DC link capacitors. In [18] , the submodule capacitance can be calculated from the expression:

$$C_{SM} = \frac{2 \cdot S \cdot E_{MMC}}{6 \cdot N_{arm} \cdot \nu_c^2} \tag{3.5}$$

where,
S is the rated capacity of the MMC converter in MVA,
E_{MMC} is the energy stored in MMC in kJ/MVA, and
ν_c is the individual submodule capacitor voltage in kV.

The value of the submodule capacitor should be such that the ripple voltage generated by the submodule capacitor should be in the range of $\pm 10\%$ [5].

Arm reactors are connected in series with the submodules per arm. These arm reactors are situated close to the AC node. Arm reactors plays a crucial role in the MMC VSC systems as they are helpful in controlling the circulating current and also limit the fault currents. In [5], the arm reactor value can be calculated from the expression:

$$L_{arm} = L_{arm}^{pu} \cdot \frac{Z_{ACbase}}{\omega_{ref}} \tag{3.6}$$

where,
L_{arm}^{pu} is the inductance of the arm reactor in pu,
Z_{ACbase} is the base AC impedance in Ω, and
ω_{ref} is the frequency in rad.sec^{-1}. In this thesis, 0.15 pu is considered as the value of L_{arm}^{pu}.

The parameters of the symmetrical monopolar MMC VSC-HVDC converter is given in table 3.5.

Table 3.5: Converter parameter for symmetrical monopolar VSC-HVDC system [5]

Parameter	Value
Rated AC voltage	320 kV
Rated MVA	1060 MVA
Frequency	50 Hz
Number of submodules per arm	200
Submodule capacitance	10 mF
Converter arm reactor	50 mH
Rated DC voltage	640 kV
DC output voltage (pole-pole)	640 kV

3.2.1.1 Control system

Control system plays a crucial role in the HVDC system. As already mentioned in section 2.3.7, vector control strategy is used in this thesis. Vector control allows the independent control of active and reactive power which makes this strategy a best choice over direct control method.

In dispatch control, the reference value of active power, reactive power, AC voltage and DC voltage are selected and fed as an input to the upper level control. The upper level control can be divided into two types of control which are outer control and inner control. In outer control, active power control loop and reactive power control loop is selected for VSC-Station-A (figure 2.4) and DC voltage control loop and reactive power control loop is selected for VSC-Station-B (figure 2.4). The reference values and control loop for each converter station are given in table 3.6. The parameters for inner control are given in [5].

Table 3.6: Control data for symmetrical monopolar MMC VSC-HVDC system

Converter Station	Control Mode		Dispatch Setpoints	
VSC-Station-A	P	Q	400 MW	0 MVAR
VSC-Station-B	V_{DC}	Q	640 kV	0 MVAR

In the lower level control, firing pulses are generated for each submodule. There are different modulation techniques present for generating firing pulses such as Phase Disposition Pulse Width Modulation (PD-PWM) [20], Phase Shift Pulse Width Modulation (PS-PWM) [21], Space Vector Pulse Width Modulation (SV-PWM) [4] and Selective Harmonic Elimination (SHE) [6, 23]. These modulation techniques become inefficient with the increase in the number of submodules, so nearest level control technique is used instead [5, 12]. The balancing of capacitor voltages is achieved by measuring the voltage of submodule capacitor at any instant and then the voltages are sorted. The number of submodules to be inserted is determined by the voltage and arm current magnitude.

Circulating current control is also introduced in this thesis. The circulating currents are generated due to the difference between the 3 phase generated voltage. This current is controlled by modelling a PI controller in d-q with a negative sequence, synchronized with second order harmonics [5].

Converter blocking algorithm is also introduced in this thesis. The need for this algorithm is due to the fact that VSC converters are very sensitive in detecting the DC faults as the reduction in voltage will lead to flow of currents through FWDs. The converter will act as a diode rectifier so this increases the need of blocking the converter in order to decrease this current to zero.

3.2.2 DC surge arrester modelling

The modelling of DC surge arrester is done by developing the voltage-current characteristics of the arrester. The voltage-current characteristics are shown in the table 3.7 [9]. The rated voltage of the arrester is 320 kV and number of parallel discs of metal oxide is considered as 1. These DC surge arresters are placed on each pole, at the terminals of the DC side of the converter.

Table 3.7: Voltage-current characteristics of the DC surge arrester [9]

Current [A]	**Voltage [pu]**
1.0000E-4	0.866
9.9996E-4	0.979
9.9981E-3	1.040
1.0002E-1	1.101
9.9991E-1	1.180
2.5000E+2	1.553
1.0000E+3	1.666
4.9998E+3	1.859
1.0000E+4	1.988
2.0000E+4	2.194

3.2.3 Cable modelling

The modelling of cable in PSCAD requires input parameters. These parameters are impedance matrix and admittance matrix which are given in equations [15]

$$Z(\omega) = R(\omega) + j\omega L(\omega) \tag{3.7}$$

$$Y(\omega) = G(\omega) + j\omega C(\omega) \tag{3.8}$$

where
Z is the impedance matrix, in Ω per unit length,
Y is the admittance matrix, in Ω^{-1} per unit length,
R is series resistance, in Ω per unit length,
L is the series inductance, in H per unit length,
G is the shunt conductance, in Ω^{-1} per unit length,

C is the shunt capacitance, in F per unit length, and
ω is the frequency, in rad.sec^{-1}.

The dimension of the matrix in equation 3.7 and 3.8 is represented as (n x n), where n represents the number of parallel conductors of a cable system. In order to calculate the matrices, following data must be entered:

1. Geometry
   - Location of the conductors.
   - Inner and outer radii of the conductors.
   - Burial depth of the conductors

   Except from the above mentioned parameters, one must also need to take into the consideration of representation of stranding of the core, thickness of the inner and outer semiconducting layer and sheath screen.
2. Material properties
   - Resistivity (ρ) and relative permeability (μ_r) of the conductor ($\mu_r = 1$ for non-ferrous material).
   - Resistivity (ρ) and relative permeability (μ_r) of the surrounding medium.
   - Relative permitivity (ϵ_r) of the insulation layers.

   In PSCAD, the relative permitivity (ϵ_r) of the insulation layer is assumed as real and independent of frequency. This results into the following equations [15]:

$$Z(\omega) = R(\omega) + j\omega L(\omega) \tag{3.9}$$

$$Y(\omega) = j\omega C \tag{3.10}$$

For land cable model in PSCAD, different cable layers are shown in the figure 3.3. In PSCAD, four layers are selected for land cable. These four layers are explained in the following paragraphs.

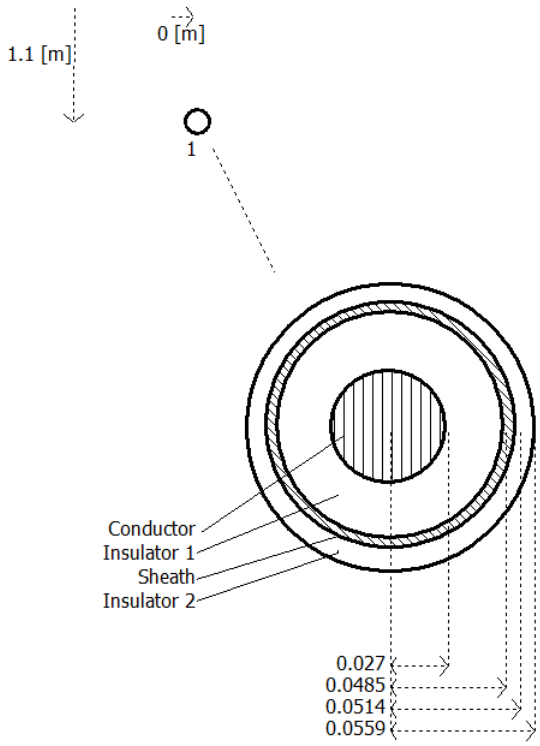

Figure 3.3: Land cable layers in PSCAD

Conductor forms the first layer in the cable. The type and the material of the cable core is a key factor for the modeling of the cable. Generally, all HVDC cables are stranded without the presence of central core. The material used is aluminium and its resistivity is considered.

Insulator 1 forms the second layer in the cable. It consists of conductor screen (inner semi-conducting layer), main insulation, insulation screen (outer semi-conducting layer) and inner water swellable tape. The material of the insulation is XLPE and its relative permitivity is considered. Radius of the conductor, thickness of both the semi-conductive layers, main insulation and inner water swellable tape constitutes the total radius of insulator 1.

Sheath forms the third layer in the cable. It comprises of screen, outer water swellable tape and metallic sheath. The material used for the screen is copper and its resistivity is considered. Radius of the insulator 1, thickness of the screen, outer water swellable tape and metallic sheath constitute the total radius of the sheath.

Insulator 2 forms the fourth and final layer in the cable. It consists of an outer sheath which is made up of polyethylene (PE) and its relative permitivity is considered. Radius of sheath and the thickness of the outer sheath constitutes the total radius of the insulator 2 as well as of the cable.

The modelling of cable in PSCAD is different than from the actual cable. So the

conversion procedure needs to be followed which are given below.

1. **Core**
   The data required in PSCAD are resistivity of the core ρ_{core} and radius of the core r_{core}. In actual cable design, the core is considered as stranded but in PSCAD, the core is represented as solid. So in order to represent the standing of the cable, in [15], the resistivity of the core is increased and can be calculated as
   $$\rho_{core} = \rho'_{core} \cdot \frac{\pi \cdot r_{core}}{A_{nom}} \tag{3.11}$$
   where,
   ρ'_{core} for copper at 20^{o}C is 1.7421*10$^{-8}\Omega \cdot m$ and for aluminium at 20^{o}C is 2.8264*10$^{-8}\Omega \cdot m$, and
   A_{nom} is the nominal cross sectional area of the core.
   If the data of DC resistance R_{DC} of the cable is available then, in [15], the resistivity can be calculated as
   $$\rho_{core} = R_{DC} \cdot \frac{\pi \cdot r_{core}}{l} \tag{3.12}$$
2. **Insulation and semiconducting layers**
   The inner and outer semi-conducting layers are not represented in PSCAD. So a conversion must be made to the relative permitivity of the insulation, which can be calculated as follows:
   (a) Calculate the radius of the core r_{core} and radius of the insulation r_{ins} which includes the thickness of inner semiconducting screen and outer semiconducting screen.
   (b) Calculate the value of relative permitivity of the insulation from the formula
   $$\epsilon_{r1} = \frac{C \cdot ln(\frac{r_{ins}}{r_{core}})}{2\pi\epsilon_o} \tag{3.13}$$
   where,
   ϵ_o is the absolute permitivity which is 8.854*10^{-12} [15].
   If the value of C is unknown then ϵ_{r1} can be calculated as
   $$\epsilon_{r1} = \epsilon_{r_{ins}} \cdot \frac{ln(\frac{r_{ins}}{r_{core}})}{ln(\frac{r_{os}}{r_{is}})} \tag{3.14}$$
   where,
   r_{os} and r_{is} represent the radius of outer and inner semi-conducting layer, respectively [15].
3. **Sheath screen**
   If the sheath screen is made up of a wire screen, then it is recommended to assume the wire screen as a tubular conductor with the cross sectional area equal to the cross sectional area of wire screen. In [15], the outer radius of the sheath screen then becomes
   $$r_{screen} = \sqrt{\frac{A_{cu}}{\pi} + r_{ins}^2} \tag{3.15}$$

The parameters of the HVDC cable for the symmetrical monopolar MMC-VSC HVDC system are given in table 3.8.

Table 3.8: HVDC cable parameters for symmetrical monopolar VSC-HVDC system

Parameter	**Value**
Length of the cable	200 km
Type of the cable	Land Cable
Rated voltage	320 kV
Metallic cross sectional area of conductor	2010 mm^2
Layer 1: Conductor	
Radius of the conductor	27 mm
Type of cable core conductor design	Stranded aluminum without central solid conductor
Resistivity of conductor	$2.826*10^{-8}$ Ωm
Layer 2: Insulation	
Radius of the insulation	48.5 mm
Relative permittivity of insulation	2.5
Layer 3: Copper screen	
Radius of the screen	51.4 mm
Resistivity of screen	$1.724*10^{-8}$ Ωm
Layer 4: Outer sheath	
Radius of outer sheath	55.9 mm
Relative permittivity of outer sheath	2.3

4

Simulation Results and Analysis

In order to perform overcurrent analysis for point to point symmetrical monopolar MMC VSC-HVDC system, fault points are placed along the system. The system energization takes place till 0.8 secs after which steady state is achieved and then after 207 ms fault inception takes place. All simulated faults are permanent in nature. Faults are cleared by the tripping action of circuit breaker on the AC side. Different simulated fault types and locations are given in the table 4.1 and figure 4.1.

Table 4.1: Fault types and location for the analysis of overcurrent stresses in a symmetrical monopolar MMC VSC-HVDC system

Sr. No.	Fault Type	Fault Location
F1	Positive pole to ground fault	DC terminal of the converter station
F2	Negative pole to ground fault	
F3	Positive pole to ground fault	Midpoint of the cable
F4	Negative pole to ground fault	
F5	Single phase to ground fault	Secondary side of the transformer
F6	Positive arm to ground fault	Top arm of phase A
F7	Negative arm to ground fault	Bottom arm of phase A

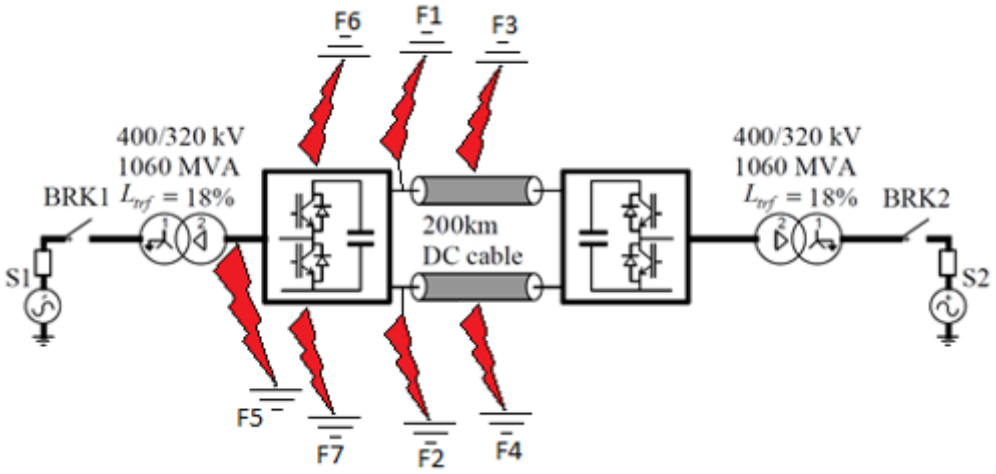

Figure 4.1: Fault location within the symmetrical monopolar MMC VSC-HVDC system

4.1 DC pole to ground fault at the DC terminal of the converter station

For simulating DC pole to ground fault at the DC terminal, two types of faults were selected. These are namely positive pole to ground fault and negative pole to ground fault. These two types of faults were simulated and presented in the following subsections.

4.1.1 Positive pole to ground fault at DC terminal of converter station

The location of positive pole to ground fault is given in the figure 4.2. Figure 4.3 shows the simulation results for positive pole to ground fault at the DC terminals.

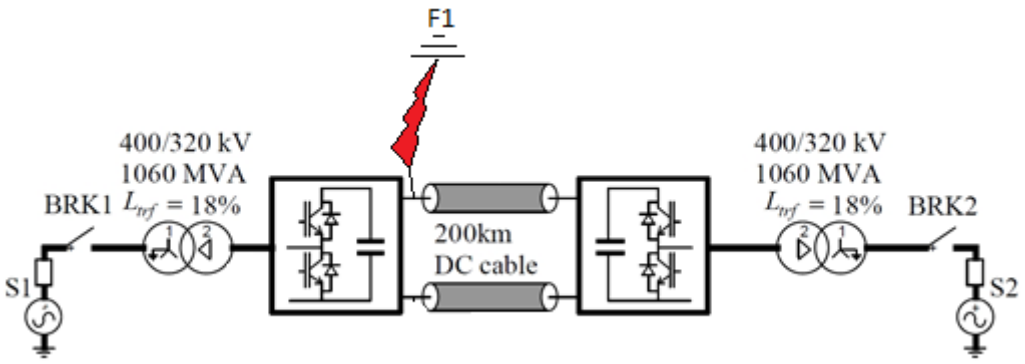

Figure 4.2: Positive pole to ground fault location in the symmetrical monopolar MMC VSC-HVDC system

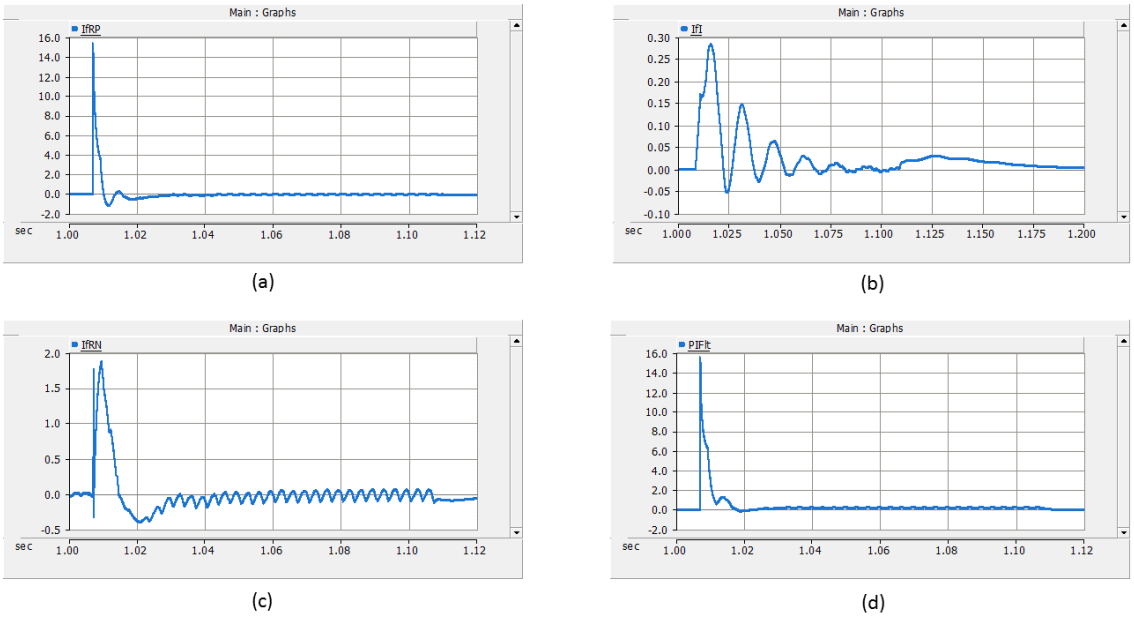

Figure 4.3: Simulation results for positive pole to ground fault at the DC terminals. (a) current through the rectifier side positive pole cable termination (peak = 15.4 kA), (b) current through the inverter side cable termination (peak = 0.28 kA), (c) current through the rectifier side negative pole cable termination (peak = 1.86 kA), (d) fault current due to positive pole to ground fault at the DC terminal of the converter station (peak = 15.5 kA).

4.1.2 Negative pole to ground fault at DC terminal of converter station

The location of negative pole to ground fault is given in figure 4.4. Figure 4.5 shows the simulation results for negative pole to ground fault at the DC terminals.

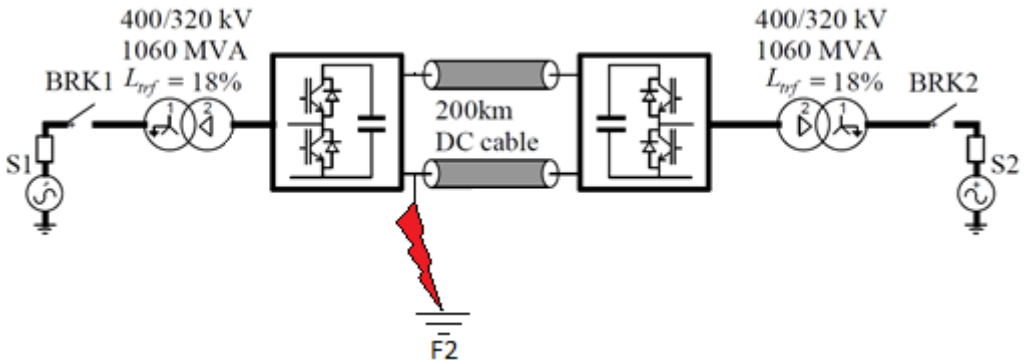

Figure 4.4: Negative pole to ground fault location in the symmetrical monopolar MMC VSC-HVDC system

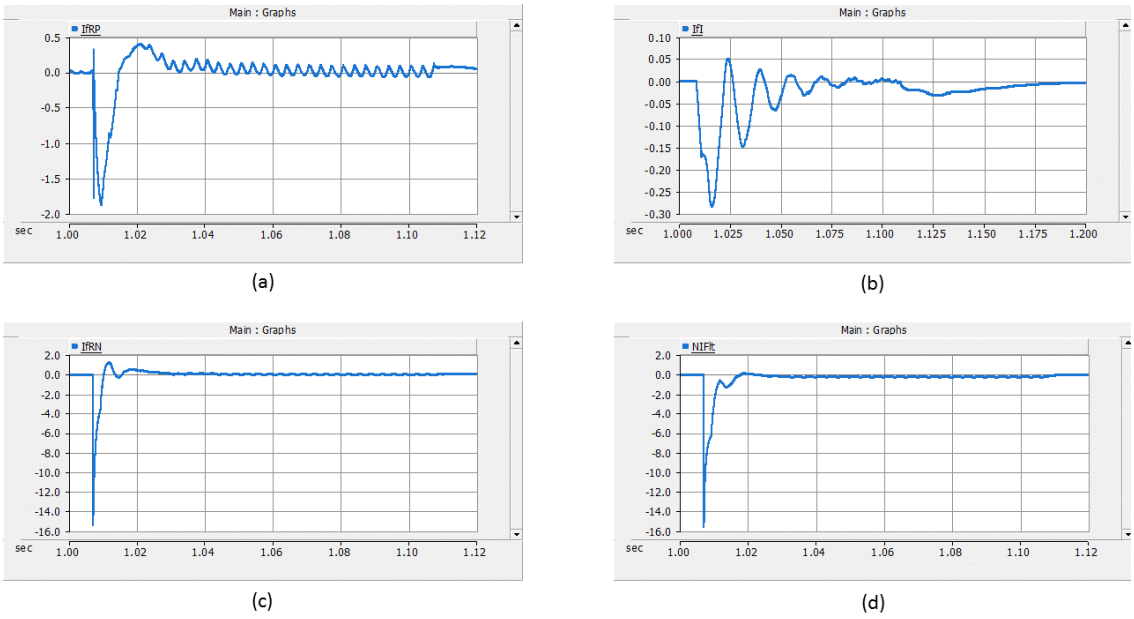

Figure 4.5: Simulation results for negative pole to ground fault at the DC terminals. (a) current through the rectifier side positive pole cable termination (peak = -1.87 kA), (b) current through the inverter side cable termination (peak = -0.28 kA), (c) current through the rectifier side negative pole cable termination (peak = -15.38 kA), (d) fault current due to negative pole to ground fault at the DC terminal of the converter station (peak = -15.5 kA).

4.1.3 Analysis

Figure 4.3 (a) shows the current through the cable termination at the positive pole, situated at the rectifier side. It is observed that the peak current is reached close to peak discharge current and then the current decreases. After the decrease in current, oscillations can be seen till 13 ms due to travelling of current wave along the cable. After 13 ms, small ripples are observed due to AC infeed until the tripping of AC breaker.

Figure 4.3 (b) shows the current through the cable termination which is located at the inverter. It is observed that the peak current reaches to 0.28 kA and then oscillations are observed due to the travelling waves along the cable until the tripping of AC breaker.

Figure 4.3 (c) shows the current through the cable termination at the negative pole, situated at the rectifier side. Two peaks are observed in this figure. First peak is due to the blocking action of the converter which is close to the fault. The fault current starts feeding the grounded cable termination which results in an increase in current till blocking of converter occurs which is situated far from the fault. After blocking, current decreases till 13 ms after which it increases and AC infeed occurs until the circuit breaker trips after 100 ms.

Figure 4.3 (d) shows the fault current at the fault location. It is observed that the peak current reaches peak discharge current which is the ratio of system voltage to the surge impedance loading of the cable. The current decreases and AC steady state infeed is observed till the tripping of AC breakers.

Figure 4.5 refers to the negative pole to ground fault at the DC terminal of the converter. Comparing this with the results obtained in figure 4.3, flipped behaviour is observed.

4.2 DC pole to ground fault at midpoint of the cable

For simulating DC pole to ground fault at the midpoint of the cable, two types of faults were selected. These are namely positive pole to ground fault and negative pole to ground fault. These two types of faults were simulated and presented in the following subsections.

4.2.1 Positive pole to ground fault at midpoint of the cable

The location of positive pole to ground fault is given in the figure 4.6. Figure 4.7 shows the simulation results for positive pole to ground fault at midpoint of the cable.

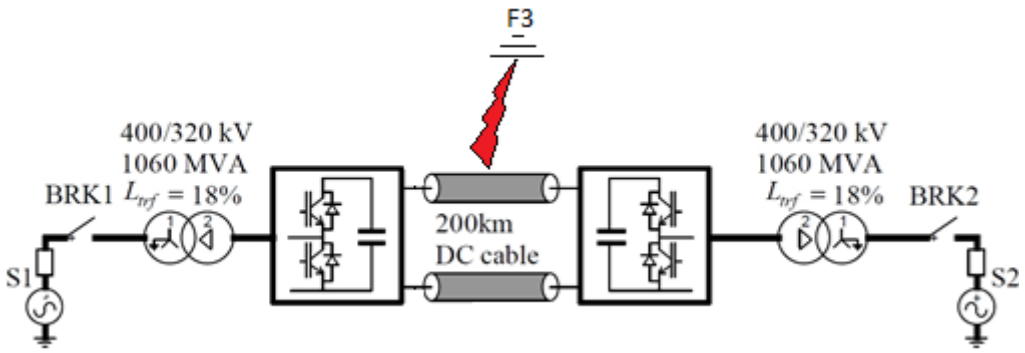

Figure 4.6: Positive pole to ground fault location in the symmetrical monopolar MMC VSC-HVDC system

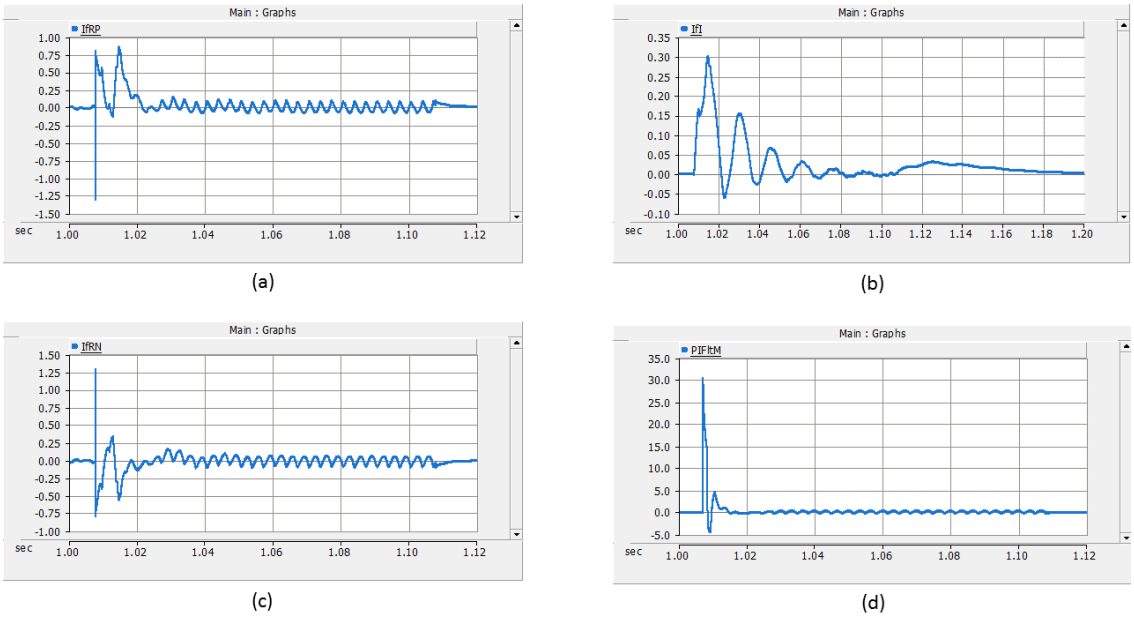

Figure 4.7: Simulation results for positive pole to ground fault at midpoint of the cable. (a) current through the rectifier side positive pole cable termination (peak = -1.29 kA), (b) current through the inverter side cable termination (peak = 0.302 kA), (c) current through the rectifier side negative pole cable termination (peak = 1.3 kA), (d) fault current due to positive pole to ground fault at midpoint of the cable (peak = 30.54 kA).

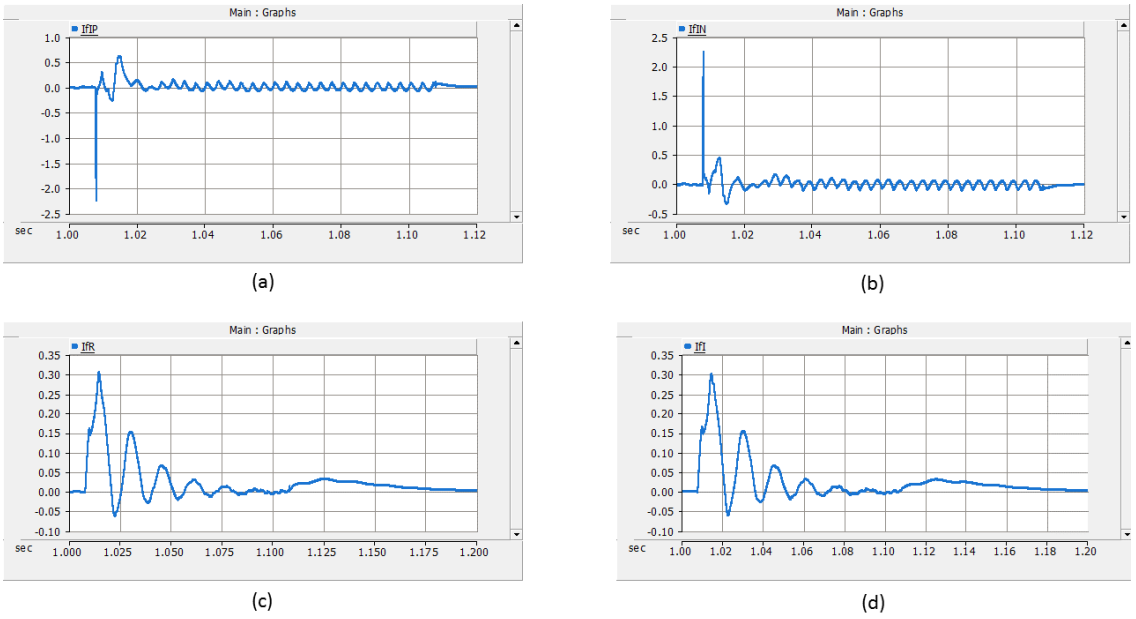

Figure 4.8: Simulation results for positive pole to ground fault at midpoint of the cable. (a) current through the inverter side positive pole cable termination (peak = -2.226 kA), (b) current through the inverter side negative pole cable termination (peak = 2.253 kA), (c) current through the rectifier side cable termination (peak = 0.305 kA), (d) current through the inverter side cable termination (peak = 0.302 kA).

4.2.2 Negative pole to ground fault at midpoint of the cable

The location of negative pole to ground fault is given in figure 4.9. Figure 4.10 shows the simulation results for negative pole to ground fault at the midpoint of the cable.

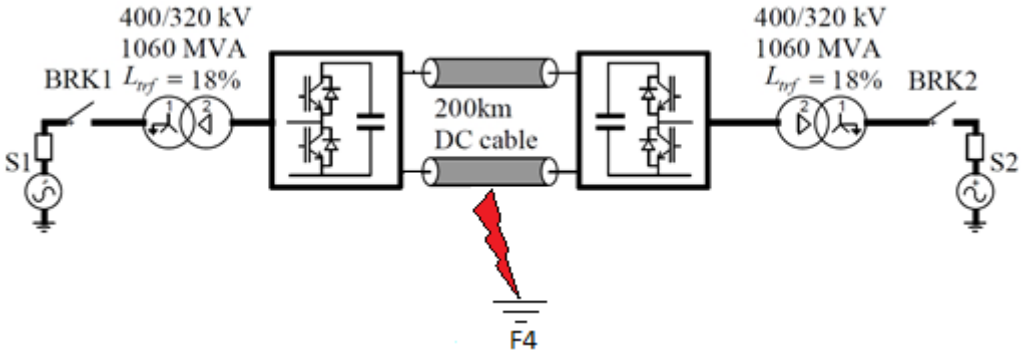

Figure 4.9: Negative pole to ground fault location in the symmetrical monopolar MMC VSC-HVDC system

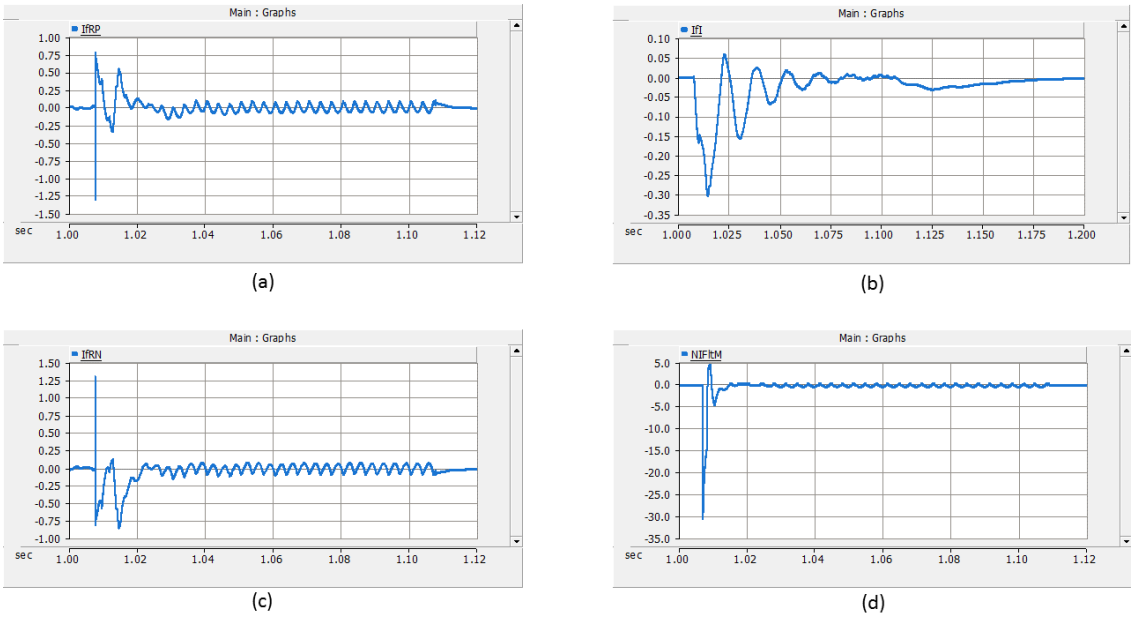

Figure 4.10: Simulation results for negative pole to ground fault at midpoint of the cable. (a) current through the rectifier side positive pole cable termination (peak = -1.3 kA), (b) current through the inverter side cable termination (peak = -0.302 kA), (c) current through the rectifier side negative pole cable termination (peak = 1.289 kA), (d) fault current due to negative pole to ground fault at midpoint of the cable (peak = -30.54 kA).

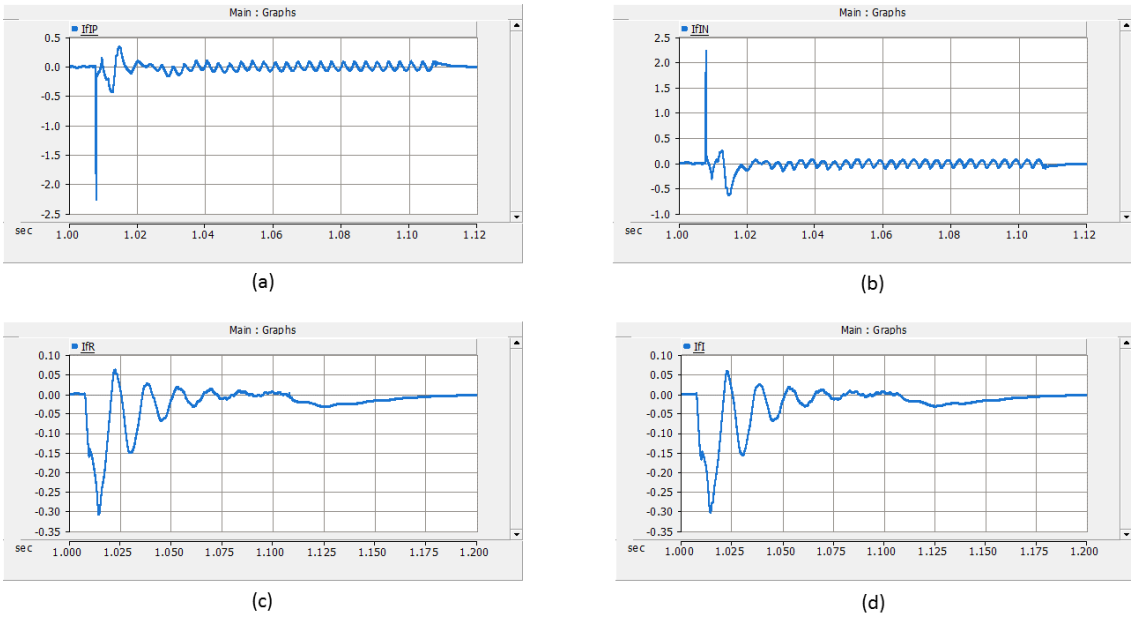

Figure 4.11: Simulation results for negative pole to ground fault at midpoint of the cable. (a) current through the inverter side positive pole cable termination (peak = -2.252 kA), (b) current through the inverter side negative pole cable termination (peak = 2.226 kA), (c) current through the rectifier side cable termination (peak = -0.307 kA), (d) current through the inverter side cable termination (peak = -0.302 kA).

4.2.3 Analysis

Figure 4.7 (a) shows the current through the cable termination at the positive pole, situated at the rectifier side. It can be seen that when the fault is applied, the current reaches a peak value of -1.29 kA and then increases to 0.75 kA. This sudden increase is due to the blocking of converters after which the current decreases. The fault current starts feeding the grounded cable termination, due to which increase in current is observed. The reduction of current occurs until 11 ms, after which AC infeed occurs until the AC circuit breaker trips after 100ms.

Figure 4.7 (b) shows the current through the cable termination situated at the inverter side. It can be observed that after fault initiation, the peak value reaches 0.302 kA, after which oscillations are observed until circuit breaker trips after 100 ms.

Figure 4.7 (c) shows the current through the cable termination at the negative pole, situated at the rectifier side. Since the fault is occuring at the midpoint of the cable and the system being symmetrical, flipped behavior is observed.

Figure 4.7 (d) shows the fault current at the fault location. Here, after the fault inception, the fault current reaches the peak value of 30.54 kA which is twice of peak discharge current observed in figure 4.3 (d). Then, a significant oscillations are observed due to travelling wave along the cable until the beginning of AC infeed.

After 11 ms, AC infeed occurs until the circuit breaker trips.

A further investigation is done to observe the behavior of cable termination situated at rectifier side and inverter side when positive pole to ground fault occurs at the midpoint of cable which is shown in the figure 4.8.

Figure 4.8 (a) and (b) refers to positive and negative pole cable termination current, respectively, situated at inverter side. By comparing it with figure 4.7 (a) and (c), it can be observed that the profile and peak values are not similar. This is because, the state of half bridge cells are unknown when the midpoint fault occurs.

Figure 4.8 (c) and (d) refers to current through rectifier side and inverter side cable termination, respectively. It can be observed that both the currents shows the same behaviour at the termination.

Figure 4.10 refers to the negative pole to ground fault at the midpoint of cable. Comparing this with the results obtained in figure 4.7, flipped behaviour is observed.

A further investigation is done to observe the behaviour of cable termination situated at rectifier side and inverter side when negative pole to ground fault occurs at the midpoint of cable, shown in the figure 4.11.

Figure 4.11 (a) and (b) refers to positive and negative pole cable termination current, respectively, situated at inverter side. By comparing it with figure 4.8 (a) and (b), similar behaviour is observed.

Figure 4.11 (c) and (d) refers to current through rectifier side and inverter side cable termination, respectively. By comparing it with figure 4.8 (c) and (d), flipped behavior is observed.

4.3 Single phase to ground fault

The location of single line to ground fault is given in the figure 4.12. Figure 4.13 shows the simulation results for single line to ground fault at secondary side of the transformer.

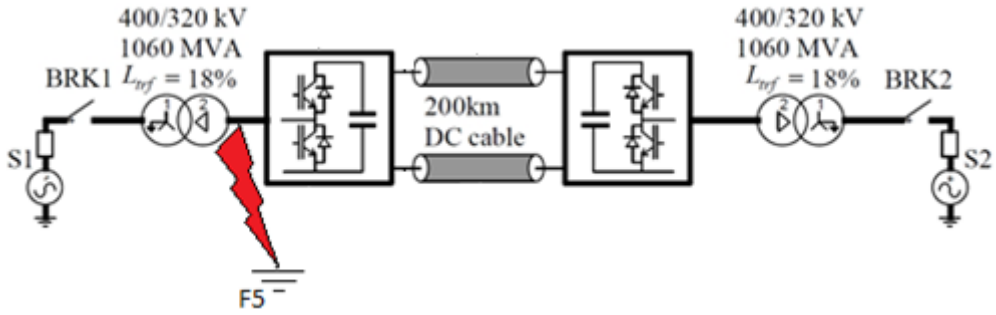

Figure 4.12: Single line to ground fault location in the symmetrical monopolar MMC VSC-HVDC system

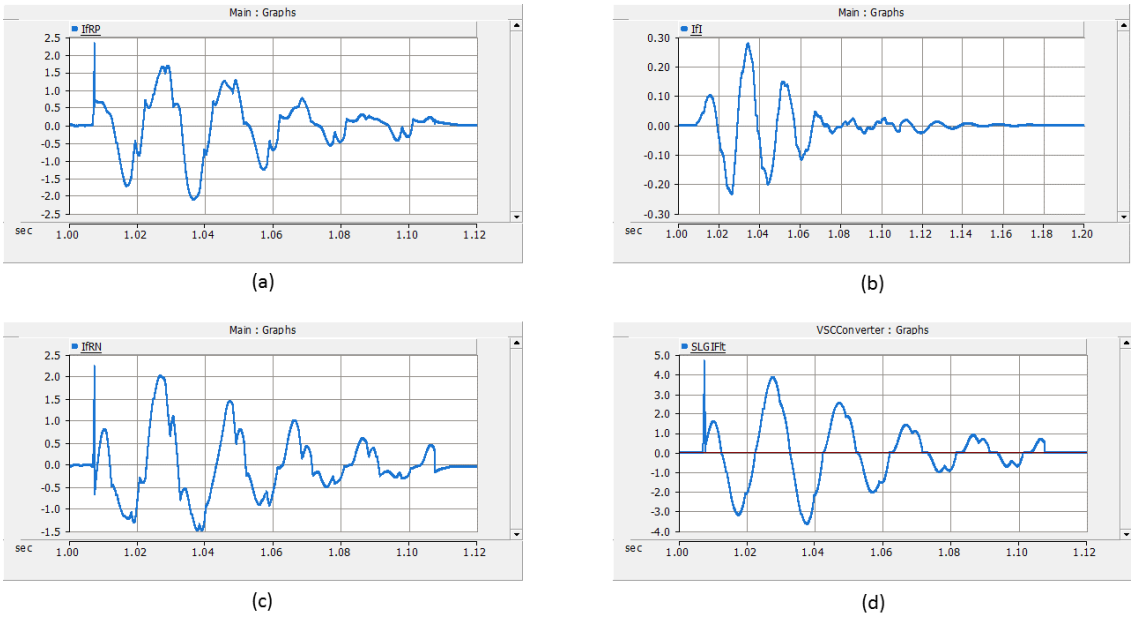

Figure 4.13: Simulation results for single line to ground fault at secondary side of the transformer. (a) current through the rectifier side positive pole cable termination (peak = 2.32 kA), (b) current through the inverter side cable termination (peak = 0.27 kA), (c) current through the rectifier side negative pole cable termination (peak = 2.24 kA), (d) fault current due to single line to ground fault at secondary side of the transformer (peak = 4.67 kA).

4.3.1 Analysis

Figure 4.13 (a) shows the current through the cable termination at the positive pole, situated at the rectifier side. When the fault occurs, blocking of rectifier takes place which results into the peak value of current reaching to 2.32 kA. This peak value is dependent on time at which the fault occurs. After blocking, due to high energy storage in the cables, rising oscillations are observed until the time when inverter is blocked after 33 ms. After the blocking of inverter, the current oscillations decreases until the tripping of AC circuit breaker after 100 ms.

Figure 4.13 (b) shows the current through the cable termination situated at the inverter side. When the fault is initiated, rising oscillations are observed until the blocking of inverter after 33 ms. After blocking of inverter, the oscillation decreases until the circuit breaker trips.

Figure 4.13 (c) shows the current through the cable termination at the negative pole, situated at the rectifier side. Here, it can be observed that after fault initiation, the peak current reaches 2.24 kA after which rising oscillations are observed until the blocking of inverter. After the blocking of inverter, the oscillations decreases until the tripping of circuit breaker.

Figure 4.13 (d) shows the fault current at the fault location. Here, the peak current reaches 4.67 kA due to blocking of rectifier after which rising oscillations are observed until the blocking of inverter. After the blocking of inverter, oscillations decreases until the tripping of circuit breaker.

4.4 Arm to ground faults

For simulating arm to ground fault at the DC terminal, two types of faults were selected. These are namely positive arm to ground fault and negative arm to ground fault. These two types of faults were simulated and presented in the following subsections.

4.4.1 Positive arm to ground fault

The location of positive arm to ground fault is given in the figure 4.14. Figure 4.15 shows the simulation results for positive arm to ground fault in top arm of phase A.

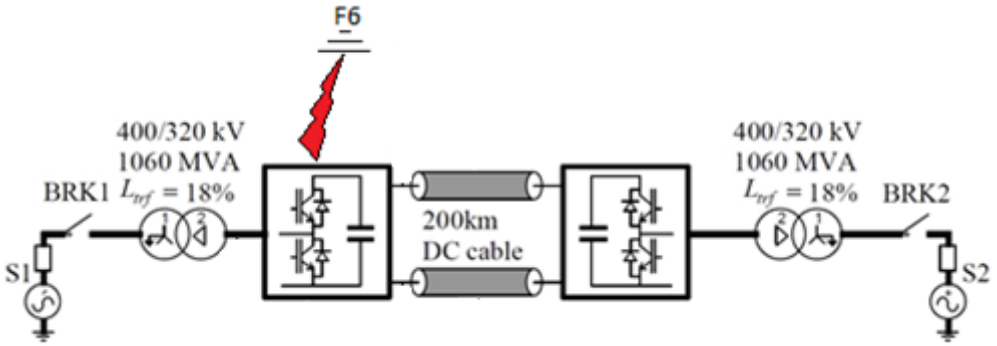

Figure 4.14: Positive arm to ground fault location in the symmetrical monopolar MMC VSC-HVDC system

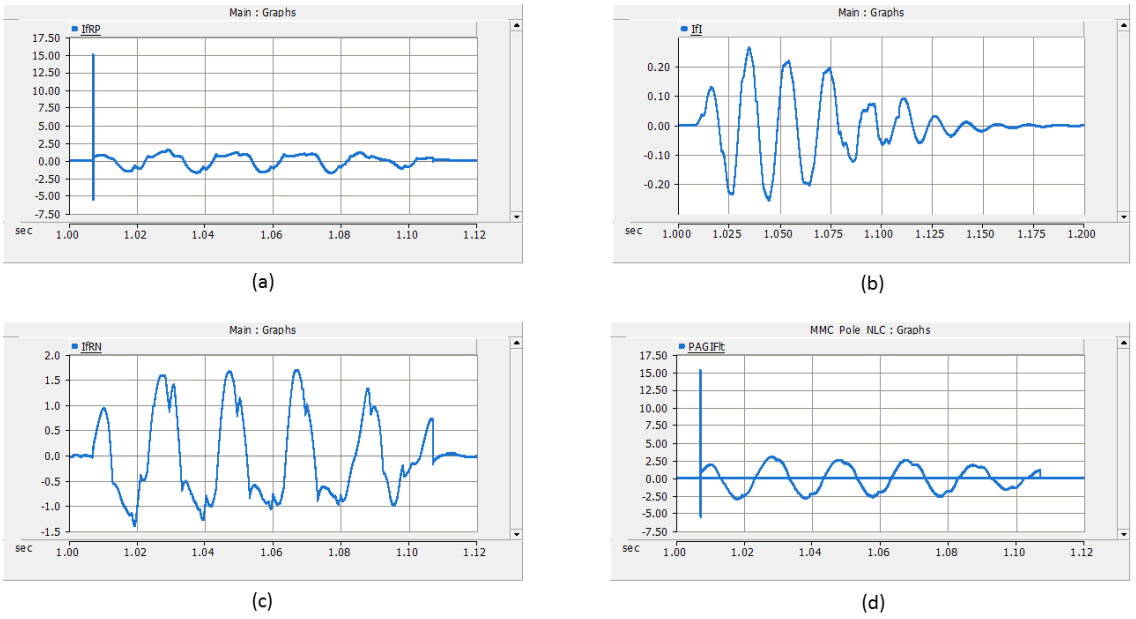

Figure 4.15: Simulation results for positive arm to ground fault at internal of the converter. (a) current through the rectifier side positive pole cable termination (peak = 15.143 kA), (b) current through the inverter side cable termination (peak = 0.26 kA), (c) current through the rectifier side negative pole cable termination (peak = 1.7 kA), (d) fault current due to positive arm to ground fault at internal of the converter (peak = 15.336 kA).

4.4.1.1 Analysis

Figure 4.15 (a) shows the current through the cable termination at the positive pole, situated at the rectifier side. When the fault occurs, the peak current reaches 15.14 kA and then the blocking of rectifier occurs. After blocking, steady current oscillations are observed until blocking of inverter after 73 ms. After the blocking of inverter, the current decreases until the tripping of circuit breaker.

Figure 4.15 (b) shows the current through the cable termination situated at the inverter side. When fault occurs, rectifier is blocked and oscillations are observed. After 73 ms, inverter is blocked and reduced oscillations are observed. After 100 ms, circuit breaker near rectifier is tripped and decaying oscillations are observed until circuit breaker near inverter is tripped.

Figure 4.15 (c) shows the current through the cable termination at the negative pole, situated at the rectifier side. After fault initiation, rectifier is blocked and oscillations are observed. After 73 ms, inverter is blocked and reduction of oscillations are observed until circuit breaker trips after 100 ms.

Figure 4.15 (d) shows the fault current at the fault location. After the fault initiation, the current reaches a peak value of 15.336 kA and rectifier blocks. After blocking, steady current oscillations are observed until blocking of inverter at 73 ms.

After the blocking of inverter, the current decreases until tripping of circuit breaker.

4.4.2 Negative arm to ground fault

The location of single line to ground fault is given in figure 4.16. Figure 4.17 shows the simulation results for negative arm to ground fault in bottom arm of phase A.

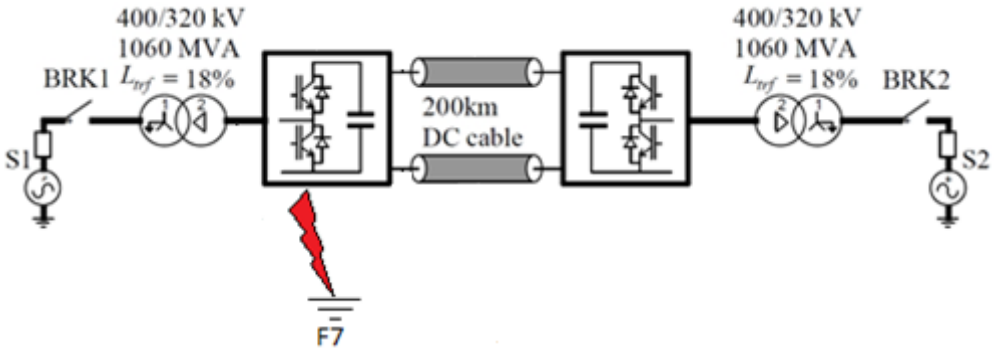

Figure 4.16: Negative arm to ground fault location in the symmetrical monopolar MMC VSC-HVDC system

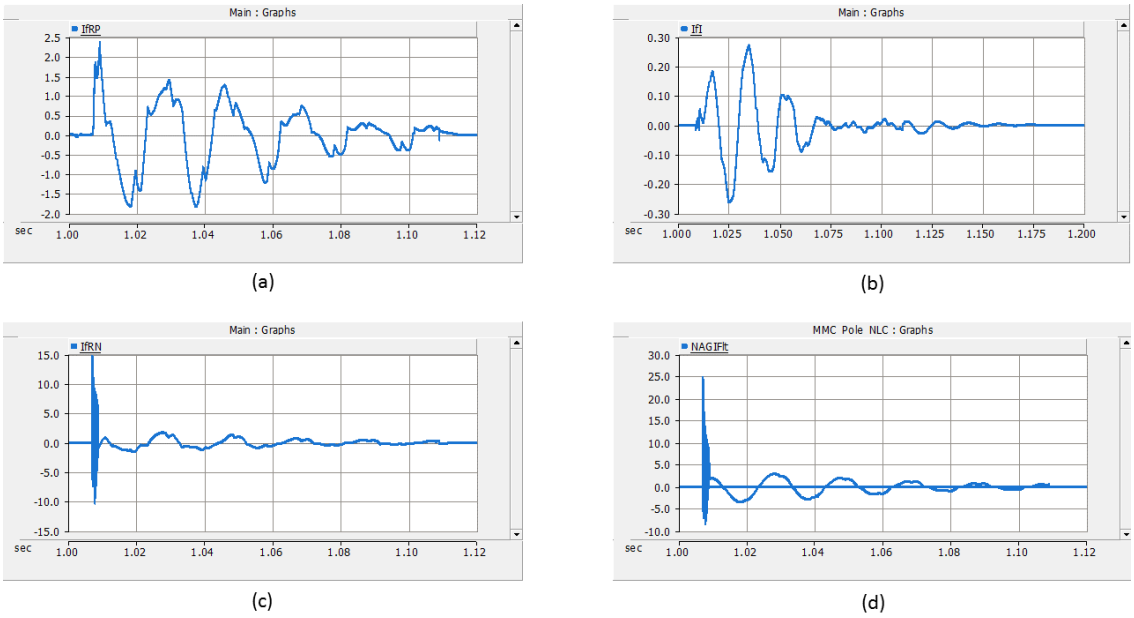

Figure 4.17: Simulation results for negative arm to ground fault at internal of the converter. (a) current through the rectifier side positive pole cable termination (peak = 2.337 kA), (b) current through the inverter side cable termination (peak = 0.27 kA), (c) current through the rectifier side negative pole cable termination (peak = 14.866 kA), (d) fault current due to negative arm to ground fault at internal of the converter (peak = 24.889 kA).

4.4.2.1 Analysis

Figure 4.17 (a) shows the current through the cable termination at the positive pole, situated at the rectifier side. When the fault occurs, the current reaches to a peak value of 2.337 kA and rectifier is blocked. After the blocking of rectifier, the current oscillates and after 33 ms, inverter is blocked. After the blocking of inverter, the current oscillations reduces until the tripping of circuit breaker.

Figure 4.17 (b) shows the current through the cable termination situated at the inverter side. When the fault occurs, the rectifier is blocked. The current oscillates and rises to a peak value of 0.27 kA. After 33 ms, the inverter is blocked and the current oscillations decreases. After 100 ms, circuit breaker near rectifier trips and decaying oscillations are observed until circuit breaker near inverter is tripped.

Figure 4.17 (c) shows the current through the cable termination at the negative pole, situated at the rectifier side. When the fault occurs, the current reaches to a peak value of 14.866 kA and oscillations are observed (in kHz range) until the blocking of rectifier. After the blocking of rectifier, steady state oscillations are observed until the blocking of inverter after 33 ms. After the blocking of inverter, the currents damps until the tripping of circuit breaker.

Figure 4.17 (d) shows the fault current at the fault location. Here, the fault current reaches to a peak of 24.889 kA and oscillations are observed (in kHz range) until the blocking of rectifier. After blocking, a steady state oscillations at system frequency is observed and after 33 ms, inverter is blocked. After the blocking of inverter, the oscillations dampens until the tripping of circuit breaker after 100 ms.

4.5 Comparative analysis

A further investigation is done by changing the length of the cable to 100 km to address the variation in peak overcurrents. The comparative analysis for the cable lengths of 200 km and 100 km cables are given in the table 4.2 and 4.3 respectively.

Table 4.2: Comparison of currents for all types of faults when cable length is 200 km

Properties	F1	F2	F3	F4	F5	F6	F7
Current at fault location	15.513 kA	-15.509 kA	30.540 kA	-30.532 kA	4.670 kA	15.336 kA	24.889 kA
Current at faulty cable termination	15.391 kA	-15.387 kA	-1.290 kA	1.289 kA	4.566 kA	15.325 kA	15.062 kA
Current transient time	13 ms	13 ms	11 ms	11 ms	100 ms	100 ms	100 ms

Table 4.3: Comparison of currents for all types of faults when cable length is 100 km

Properties	F1	F2	F3	F4	F5	F6	F7
Current at fault location	15.468 kA	-15.465 kA	30.409 kA	-30.404 kA	4.760 kA	15.259 kA	24.653 kA
Current at faulty cable termination	15.298 kA	-15.296 kA	-1.438 kA	1.437 kA	4.648 kA	15.249 kA	15.048 kA
Current transient time	8 ms	8 ms	5 ms	5 ms	100 ms	100 ms	100 ms

In both the tables, it is worth to be noted that the current transient time for the faults at DC side are same with respect to fault location i.e. at terminals and at midpoint of the cable. It is also observed that the current transient time reduces with respect to the total length of the cable. The values in both tables are plotted in figure 4.18 and 4.19.

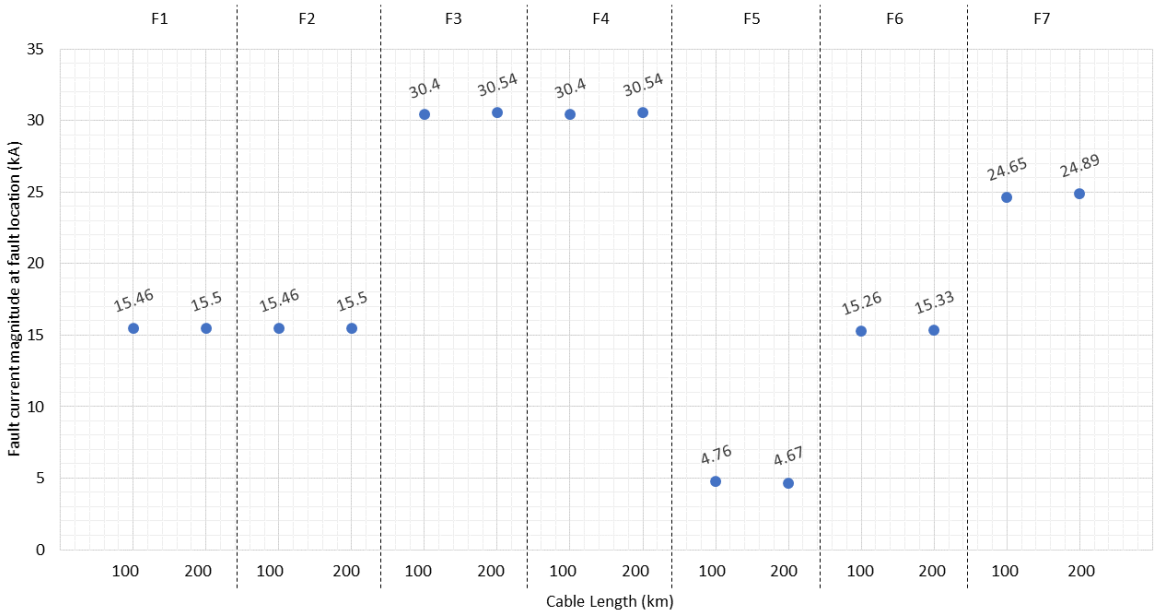

Figure 4.18: Graph showing the comparison between fault currents and cable length

Figure 4.18 shows the comparative analysis of fault currents with varying cable lengths. It can be observed that with increase in cable length, fault current increases when the fault occurs at DC side (both midpoint of the cable and terminals) and at arm. Also for the same cable length with respect to fault location at DC side i.e. at terminal and midpoint of cable, the peak current value is same. However, for single line to ground fault, the behavior is opposite as when the cable length increases, peak fault current decreases.

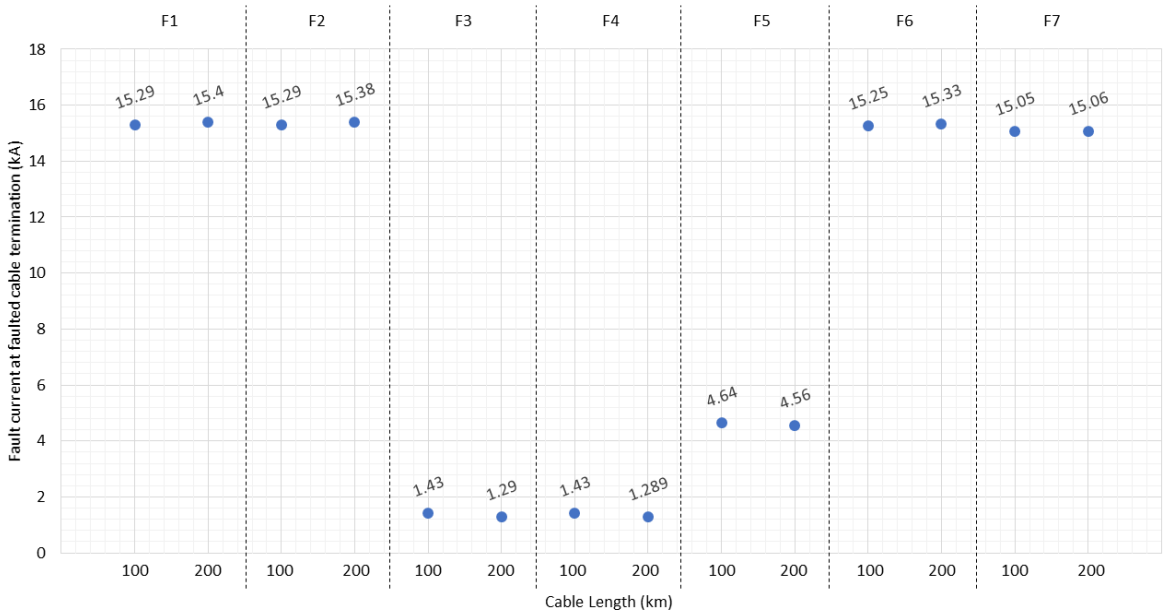

Figure 4.19: Graph showing the comparison between fault current at faulted cable termination and cable length

Figure 4.19 shows the comparative analysis of faulted cable termination currents with varying cable lengths. It can be observed that with increase in cable length, fault current at the faulted cable termination increases when the fault occurs at DC terminals and at arm. Also for the same cable length with respect to fault location at DC side i.e. at terminal and midpoint of cable, the peak current value is same. However, for single line to ground fault and cable midpoint fault, the behavior is opposite as when the cable length increases, peak fault current decreases.

5

Sustainable and Ethical Aspects

5.1 Sustainability factors

The sustainability factors are divided into 3 aspects mainly environmental, economical and social aspects [24]. Each of these aspects are explained in the following subsections between High Voltage AC (HVAC) transmission and HVDC transmission.

5.1.1 Environmental factors

The advantage of transmission of power in HVDC from an environmental view point is that the Right-of-Way (RoW) is less when compared with HVAC transmission. Right-of-way is defined as a portion of land on either side of transmission tower which are acquired by the Transmission System Operator (TSO) for operation and maintenance purposes. This land should not consist any structures which could hinder the transmission line. When compared with HVAC transmission, the number of conductors required for the transmission of same amount of power in HVDC is less. This results in less number of transmission towers and reduction of RoW. RoW is further reduced when the transmission of power is done with cables instead of overhead lines.

Inefficient grounding of HVDC system possesses a great disadvantage for the environment. Asymmetrical monopolar configuration without metallic return can not be used where there is a fresh water deposit and in areas where the resistivity of the ground is high. This can cause a threat to the animal life as well as human life.

5.1.2 Economical factors

In terms of economics, very long transmission of power through HVDC is economical compared with HVAC transmission for the same amount of transmission capacity because the number of conductors required for HVDC transmission is less compared with HVAC transmission for the same amount of power. For example, a typical bipolar HVDC system requires two conductors compared with three conductors for each phase in HVAC system. Also, when two different power systems are interconnected with HVDC, the already existing generation plant connected to the power system can operate more efficiently and economically. With this, the installation of new power plants can be adjourned.

Initial investment of HVDC system is high compared with HVAC system for the same transmission capacity. The additional cost of the converter station, transformers and HVDC cable are added, making it a non-economical option of selecting HVDC transmission. But after a certain distance, called as critical distance, total DC cost becomes less than total AC cost. Therefore, HVDC transmission is considered as a feasible option when the transmission of power is over a long distance (greater than 500 km)[1].

5.1.3 Social factors

HVDC transmission is an emerging technology. Due to its advantages, these technologies are now adopted in countries like China, India, Brazil etc [1]. This leads to the creation of job opportunities for the people especially in the developing countries.

The HVDC systems provides a good quality of power to the consumers as the existing generations are operated at high efficiency. Also the transmission losses are less when compared with HVAC systems; about 0.6 percent for HVDC Classic and below 1 percent for HVDC Light [1]. If asynchronous power systems are interconnected with the help of HVDC transmission, then in the event of an outage in one of the power system, the cascading outages do not propagate to the other power systems.

Not In My Backyard (NIMBY) plays a significant role for the choice of transmission systems. It is defined as a characteristic of the residents who only oppose an infrastructure development because of the closeness to their residence or recreational areas. Transmission of power from offshore wind farms to the consumers in the main land is generally done via HVDC. The public do not generally want these offshore wind farms located close to the main land which could hinder the scenic view of the sea.

5.2 Ethical factors

According to [22], there are some ethical aspects that need to be followed in order to carry out this thesis. Some of these ethical principles are discussed below.

For a thesis, it is important that the stated claims or the estimations made by the thesis worker need to be realistic and honest. HVDC systems have proved as a good alternative mode of transmission of power compared with HVAC systems. But there are some drawbacks which are important to be stated so that the concerned parties do not make an irrational decision.

It is also important for the thesis worker to take and accept honest criticism from their supervisors and team members. The assumptions and statements related to the technical areas made by the supervisors and engineers needs to be cited and acknowledged. For instance, the cable data provided by the manufacturers, if used in the thesis, need to be acknowledged and duly cited by the thesis worker.

Lastly, it is important for the thesis worker to treat their colleagues fairly and unbiased, irrespective of their identity. For instance, valuing the work of a manager more their colleagues should be avoided. It is best to take the comments and criticism offered by manager as well as their colleagues based on their competence area.

6
Conclusion and Future Work

6.1 Conclusion

The aim of this thesis was to investigate the different types of fault that occurs on a 320 kV cable system in a symmetrical monopolar voltage source HVDC converter and thereby analyze the over-current (fault) profile caused due to different discharging mechanism and grounding. A 320 kV point-to-point symmetrical monopolar MMC VSC-HVDC system was modelled in PSCAD. Different types of fault points were chosen in order to simulate the overcurrent profile. All the faults were permanent faults and clearing was done with the help of AC breakers.

When simulating pole to ground faults at the DC terminal, current through the fault and the current through the faulted cable termination reaches the peak value approximately equal to peak discharge current of the cable. This peak discharge current is the ratio of system voltage to the surge impedance loading of the cable. When simulating DC pole to ground faults at the midpoint of the cable, it was observed that the peak fault current at the fault location reaches twice the value of peak discharge currents. On the faulted cable termination, the effect of overcurrent was not severe compared to the terminal fault and the peak value was lowest among all other types of faults. When simulating single line to ground faults at secondary side of transformer, it was observed that the fault current at the fault location was lowest among all other types of faults. When simulating arm to ground faults at converter phase A, it was observed that the fault current at fault location as well as at cable termination was different for positive and negative arms.

A parametric analysis was conducted by decreasing the length of the cable and comparing respective fault current at fault locations and at cable termination. It was observed that the length of the cable affects the fault currents at fault location and at cable termination. Also the current transient time has an effect on cable length for the faults occurring on DC side.

Finally, it can be concluded that most severe case of fault currents at fault location was observed in the case of DC fault at midpoint of the cable. So the cable needs to be designed to handle such faults. DC faults at terminal and arm to ground faults are the most severe cases of fault current at the cable termination.

6.2 Future Work

This thesis work presented the study of overcurrent stresses on 320 kV HVDC land cable. It would be interesting to investigate for submarine cables also. Currently, most of the HVDC projects involve transmission of power from offshore wind farms to onshore substations, so a fault in the cable section could be more severe compared to fault on land cables. This work can also be extended for mixed transmission systems also which includes land cable, sea cables and overhead lines. Faults simulated on mixed transmission system can affect the travelling wave phenomena and so the behavior during faults.

Another future prospect can be proposed for this thesis work. A parametric sweep can also be performed on this work. It would be interesting to investigate the impact of overcurrents by studying the impact of short circuit level of AC grid, active and reactive power transfer and location of arm inductance.

Lastly, this thesis work can be extended for asymmetric monopolar configuration. Results obtained from asymmetrical monopolar system can be implemented to bipolar systems also as it serves as a constituent to bipolar system.

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