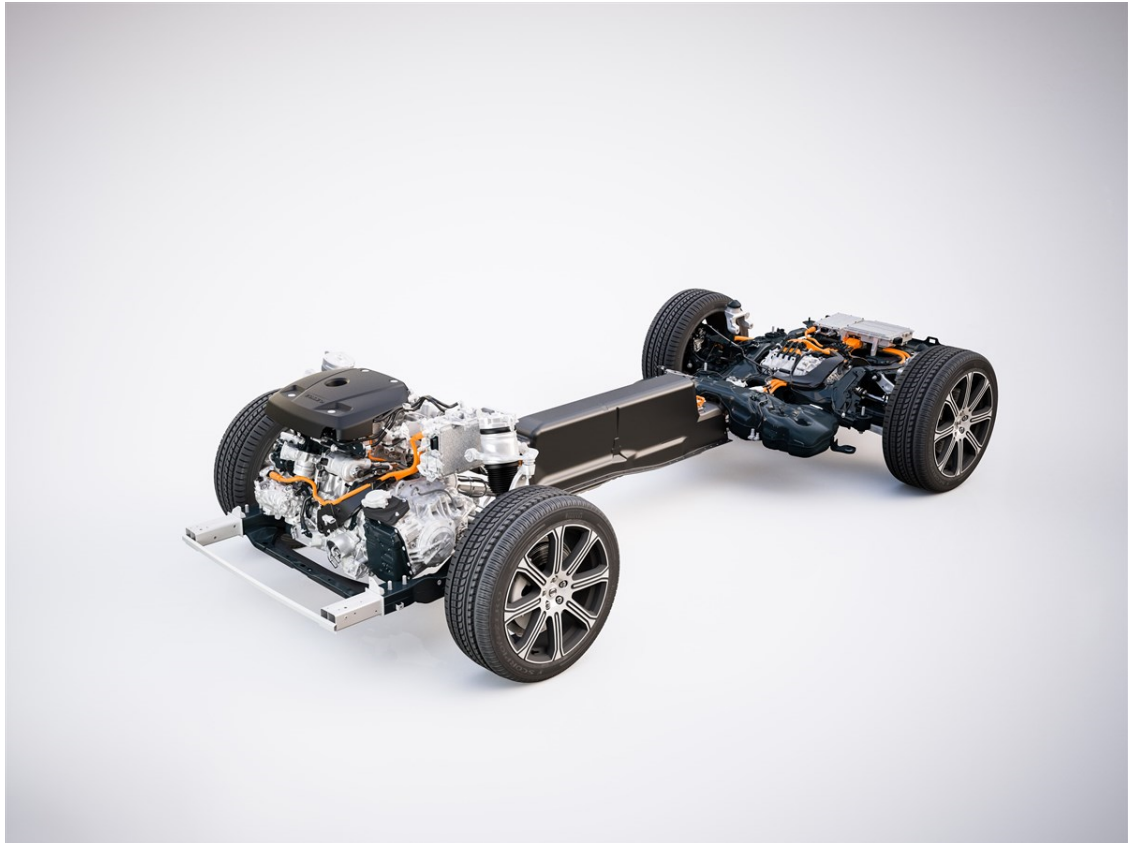




**CHALMERS**  
UNIVERSITY OF TECHNOLOGY



# Neutral point voltage of Electric motors for multilevel drives in Electric Vehicles

Masters thesis in Sustainable Electric Power Engineering and Electromobility

Rishav Dubey & Varun Prasath Kannan

---

DEPARTMENT OF SOME SUBJECT OR TECHNOLOGY

CHALMERS UNIVERSITY OF TECHNOLOGY

Gothenburg, Sweden 2024

[www.chalmers.se](http://www.chalmers.se)



MASTERS THESIS 2024

# Neutral point voltage of Electric motors for multilevel drives in Electric Vehicles

Rishav Dubey & Varun Prasath Kannan



**CHALMERS**  
UNIVERSITY OF TECHNOLOGY

Department of Electrical Engineering  
CHALMERS UNIVERSITY OF TECHNOLOGY  
Gothenburg, Sweden 2024

Neutral point voltage of Electric motors for  
multilevel drives in Electric Vehicles  
Rishav Dubey & Varun Prasath Kannan

© Rishav Dubey & Varun Prasath Kannan, 2024.

Supervisor: Dr. Georgios Mademlis, Volvo Cars Corporation & Dr. Kooros Moab-  
ber, Volvo Cars Corporation  
Examiner: : Dr. Yujing Liu, Department of Electrical Engineering

Masters Thesis 2024  
Department of Electrical Engineering  
Division of Electric Power Engineering  
Chalmers University of Technology  
SE-412 96 Gothenburg  
Sweden  
Telephone +46 31 772 1000

Neutral point voltage of Electric motors for  
multilevel drives in Electric Vehicles  
Rishav Dubey & Varun Prasath Kannan  
Department of Electrical Engineering  
Chalmers University of Technology

## Abstract

As electric vehicles (EVs) continue to gain traction as a sustainable transportation solution, the demand for efficient and reliable electric motor drives intensifies. The major components affecting these are inverters, motors, batteries, and the control system. Here we are working on inverters and the machine. Usually, in an Electric Vehicle, a high-frequency current is drawn by the electric machine from the inverter which causes conducted emissions.

In this thesis, common-mode current and voltage at the AC side of a two-level inverter and a three-level neutral point clamped inverter that are coupled to the electrical machine are estimated. This thesis also analyses the effect on the voltage at different modulation index and different load conditions. A common-mode noise filter at the inputs of the two inverters was added to check the effect of the filter on the output and validate the flow of the common mode current. Utilizing simulation tools like PLECS and LTSpice and experimental values of the electric machine, the High-Frequency current is determined in the frequency domain.

Overall, this study contributes to the advancement of neutral point voltage inverters in multilevel electric motor drives, offering valuable insights and practical solutions to optimize the performance of electric vehicles in terms of efficiency, reliability, and environmental sustainability.

Keywords: Common-mode, modulation index, frequency.



# Acknowledgements

We would like to express our deepest gratitude to Volvo Cars for providing us with the opportunity to conduct this thesis within their esteemed organization. The support and resources extended by them have been pivotal in the successful completion of this research in the dynamic domain of electric vehicles.

We are profoundly indebted to our supervisor, Georgios Mademlis and Moabber Kooros, for their exceptional guidance and invaluable insights throughout this thesis. Their expertise and mentorship have been instrumental in navigating the complexities of the thesis.

We are grateful to Chalmers University of Technology for its academic support and for fostering an environment conducive to research and learning. Also we would also like to acknowledge the contributions of our examiner Prof Yujing Liu who have provided encouragement and moral support throughout this endeavor.

Special thanks to our families for their unwavering support, patience, and encouragement during this challenging yet rewarding journey. Their belief in us has been a constant source of strength and motivation.

Thank you all for being part of this enriching journey.

Rishav Dubey, Gothenburg, June 2024

Varun Prasth, Gothenburg, June 2024



# List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

AC	Alternating Current
CM	Common Mode
CT	Current Transformers
DC	Direct Current
DM	Differential mode
EMF	Electromotive Force
EMI	Electromagnetic Interference
EV	Electric Vehicle
IGBT	Insulated gate Bipolar Transistors
$m_a$	Modulation Index
MLI	Multi Level Inverter
MOSFET	Metal Oxide Semiconductor Field Effect Transistors
NPC	Neutral Point Clamped
PMSM	Permanent Magnet Synchronous Machine
PWM	Pulse Width Modulation
S-parameter	Scattering Parameter
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
$V_{ref}$	Reference Voltage
Z-parameter	Impedance Parameter



# Nomenclature

Below is the nomenclature of indices, parameters that have been used throughout this thesis.

## Indices

$i, j$  Real and Imaginary co-efficients

## Parameters

$\Gamma$  Reflection coefficient

## Variables

$p_j$  Active power injection at bus  $j$

$p_{ji}$  Active power flow from bus  $j$  to bus  $i$

$v_i$  Square of voltage magnitude at bus  $i$



# Contents

<b>List of Acronyms</b>	<b>ix</b>
<b>Nomenclature</b>	<b>xi</b>
<b>List of Figures</b>	<b>xv</b>
<b>List of Tables</b>	<b>xvii</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Background . . . . .	1
1.1.1 <b>Battery</b> . . . . .	2
1.1.2 <b>Electric Machines</b> . . . . .	3
1.1.3 <b>Inverter</b> . . . . .	3
1.1.4 <b>Bearing Current</b> . . . . .	4
1.1.5 <b>EMI</b> . . . . .	4
1.2 Aim . . . . .	6
1.3 Scope . . . . .	6
1.4 Outline . . . . .	7
<b>2 MOSFET drivers</b>	<b>9</b>
2.1 Type of MOSFET Drivers . . . . .	9
2.1.1 Hard Switching . . . . .	9
2.1.2 Soft Switching . . . . .	10
2.2 Slew Rate Control . . . . .	10
<b>3 Modulators</b>	<b>13</b>
3.1 Pulse Width Modulation . . . . .	13
3.2 Sinusoidal Pulse Width Modulation . . . . .	14
3.3 Space Vector Modulation . . . . .	15
<b>4 Inverters</b>	<b>21</b>
4.1 Two Level Inverter . . . . .	21
4.2 Multi Level Inverter . . . . .	22
4.2.1 Neutral Point Clamped MLI . . . . .	23
4.2.1.1 Clamping Diodes . . . . .	23
4.2.1.2 Switching Devices . . . . .	24
4.2.1.3 Control Circuits . . . . .	24

4.2.1.4	DC Power Source . . . . .	24
4.2.2	Modelling . . . . .	24
4.3	CM current filter . . . . .	25
<b>5</b>	<b>Common Mode current</b>	<b>29</b>
5.1	Estimation of CM current in Bearings . . . . .	29
5.1.1	Current Transformers . . . . .	30
5.1.2	Rogowski Coils . . . . .	30
5.2	CM current Reduction . . . . .	31
<b>6</b>	<b>S-parameters</b>	<b>33</b>
6.1	Properties of S-parameter . . . . .	34
6.2	Estimation of S-parameter using VNA . . . . .	34
6.3	Estimation of Z-parameter and Current . . . . .	36
6.3.1	Machine Parameters . . . . .	37
6.4	Common Mode Current Path . . . . .	39
<b>7</b>	<b>Simulation of a single switch</b>	<b>43</b>
7.1	Double Pulse Test . . . . .	43
7.1.1	Modelling and Analysis . . . . .	44
<b>8</b>	<b>Analysis of inverters</b>	<b>47</b>
8.1	FFT comparison . . . . .	48
8.2	Effect of modulation index . . . . .	50
8.3	Effect of load conditions . . . . .	54
8.4	2 level vs 3 level . . . . .	57
<b>9</b>	<b>Conclusion</b>	<b>59</b>
<b>10</b>	<b>Future Work</b>	<b>61</b>
<b>11</b>	<b>Impact on Industries</b>	<b>63</b>
11.1	Understanding and Mitigating EMI . . . . .	63
11.2	Enhancing Efficiency . . . . .	63
11.3	Improving Power Quality . . . . .	63
11.4	Cost-Benefit Analysis . . . . .	63
11.5	Regulatory Compliance . . . . .	64
	<b>Bibliography</b>	<b>65</b>

# List of Figures

1.1	Electric Powertrain[2] . . . . .	2
1.2	Schematic representation of a typical three-level NPC traction in- verter [3] . . . . .	4
1.3	Bearing Current [4] . . . . .	5
2.1	Soft vs Hard Switching [5] . . . . .	10
2.2	Low Slew Rate . . . . .	10
2.3	High Slew Rate . . . . .	10
2.4	Driver Circuit of the Inverter . . . . .	11
3.1	PWM signal with duty cycle of 50% [6] . . . . .	13
3.2	Sinusoidal PWM technique for one phase [8] . . . . .	14
3.3	Multilevel Inverter , Single Leg [9] . . . . .	15
3.4	Large Vectors . . . . .	16
3.5	Medium Vectors . . . . .	16
3.6	Small Vectors . . . . .	16
3.7	Sector [10] . . . . .	17
3.8	Triangle inside the sector [10] . . . . .	17
3.9	Space Vector NPC [11] . . . . .	18
3.10	Switching Sequence[Region Wise] [12] . . . . .	18
4.1	Two-level Inverter model used for simulation . . . . .	22
4.2	3-level NPC [13] . . . . .	24
4.3	Schematic of 3-level NPC MLI used for simulation . . . . .	26
4.4	simple CLC filter . . . . .	26
4.5	CLC filter implemented in simulation . . . . .	26
5.1	CT construction and symbol [14] . . . . .	30
5.2	Simple Schematic of Rogowski Coil [15] . . . . .	31
6.1	2-port device [17] . . . . .	33
6.2	3-port device [18] . . . . .	33
6.3	S-parameter for EM . . . . .	35
6.4	S Parameters Magnitude and Angle . . . . .	35
6.5	Z-Parameters (Impedance) Magnitude and Angle . . . . .	36
6.6	Machine Parameters . . . . .	39
6.7	Load Capacitor Current . . . . .	39

6.8	Filter Capacitor Currents . . . . .	40
6.9	Common Mode Currents . . . . .	41
6.10	Common Mode Currents . . . . .	41
7.1	Schematic of Double Pulse Test . . . . .	43
7.2	One switch of the Inverter . . . . .	44
7.3	$V_{ds}$ and $V_{gs}$ of one Switch . . . . .	45
8.1	Single Voltage Pulse Time Domain [ $m_a = 1$ ,HTHS] . . . . .	48
8.2	(a) Rise Time (b) Ringing when pulse rises (c) Ringing when pulse begins to fall (d) Ringing when pulse falls . . . . .	49
8.3	Single Voltage Pulse FFT [ $m_a = 1$ ] . . . . .	49
8.4	L-L Plecs Voltage MLI[ $m_a = 1$ ] . . . . .	50
8.5	L-L Plecs Voltage MLI[ $m_a = 0.4$ ] . . . . .	50
8.6	Phase Current, CM Voltage and L-L voltage MLI [ $m_a=1$ ,Load= $5\Omega$ ] .	50
8.7	Phase Current, CM Voltage and L-L voltage MLI [ $m_a=0.4$ , Load= $5\Omega$ ] .	50
8.8	MLI, CM Voltage [ $m_a=1$ vs $m_a=0.4$ ], Load= $5\Omega$ . . . . .	51
8.9	MLI CM Current [ $m_a=1$ vs $m_a=0.4$ ], Load= $5\Omega$ . . . . .	51
8.10	L-L Plecs Voltage 2-Lvl [ $m_a = 1$ ] . . . . .	52
8.11	L-L Plecs Voltage 2-Lvl [ $m_a = 0.4$ ] . . . . .	52
8.12	Phase Current, CM Voltage and L-L voltage 2-Lvl[ $m_a=1$ ],Load= $5\Omega$ .	52
8.13	Phase Current, CM Voltage and L-L voltage 2-Lvl[ $m_a=0.4$ ],Load= $5\Omega$ .	52
8.14	2-Lvl Voltage [ $m_a=1$ vs $m_a=0.4$ ],Load= $5\Omega$ . . . . .	53
8.15	2-Lvl Common Mode Current [ $m_a=1$ vs $m_a=0.4$ ], Load= $5\Omega$ . . . . .	53
8.16	Phase Current, CM Voltage and L-L voltage MLI [ $m_a=1$ ,Load= $5\Omega$ ] .	54
8.17	Phase Current, CM Voltage and L-L voltage MLI [ $m_a=1$ , Load= $30\Omega$ ] .	54
8.18	MLI Load[ $5\Omega$ vs $30\Omega$ ], $m_a=1$ . . . . .	54
8.19	MLI, CM Current,Load[ $5\Omega$ vs $30\Omega$ ], $m_a=1$ . . . . .	55
8.20	Phase Current, CM Voltage and L-L voltage Two Lvl [ $m_a=1$ ,Load= $5\Omega$ ] .	55
8.21	Phase Current, CM Voltage and L-L voltage Two Lvl [ $m_a=1$ , Load= $30\Omega$ ] . . . . .	55
8.22	2-Lvl CM-Voltage,[ $m_a = 1$ ] Load:( $5\Omega$ vs $30\Omega$ ) . . . . .	56
8.23	2lvl CM Current, [ $m_a = 1$ ] Load:( $5\Omega$ vs $30\Omega$ ) . . . . .	56
8.24	L-L Plecs Voltage,MLI[ $m_a = 1$ ] . . . . .	57
8.25	L-L Plecs Voltage,2-Lvl[ $m_a = 1$ ] . . . . .	57
8.26	Phase Current, CM Voltage and L-L voltage MLI [ $m_a=1$ ,Load= $5\Omega$ ] .	57
8.27	Phase Current, CM Voltage and L-L voltage 2-Lvl[ $m_a=1$ ,Load= $5\Omega$ ] .	57
8.28	CM Voltage [MLI vs 2Lvl] , [ $m_a=1$ , Load= $5\Omega$ ] . . . . .	58
8.29	CM Current [MLI vs 2Lvl] , [ $m_a=1$ , Load= $5\Omega$ ] . . . . .	58

# List of Tables

3.1	Vector $T1/T_s$ , Vector $T2/T_s$ , and Vector $T0/T_s$ for different regions .	19
4.1	Switching state of Two-level inverter . . . . .	22



# 1

## Introduction

The adoption of electric vehicles has witnessed significant growth in recent years, driven by global efforts to mitigate climate change and reduce the usage of fossil fuels. Central to the propulsion system of EVs is the inverter, a critical component responsible for converting DC from the battery into AC to drive the electric motor. Among the various types of inverters utilized in EVs, the NPC inverter stands out for its efficiency, reliability, and performance characteristics.

In the initial phase of this thesis an extensive literature survey, delving into multiple research papers covering various topologies of inverters was done. This comprises a thorough examination of methodologies for studying currents in the frequency domain and inspecting different modulation techniques.

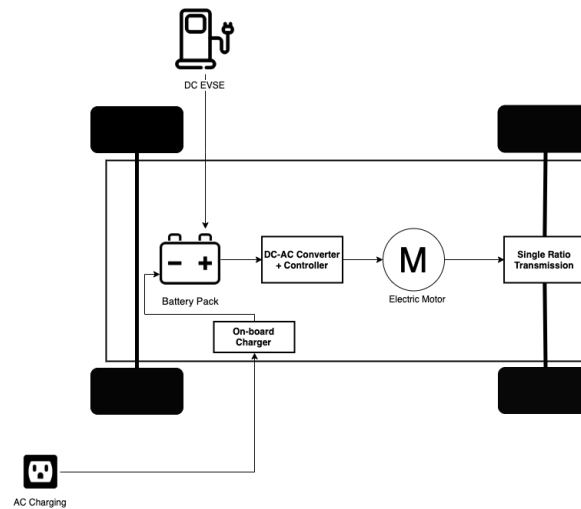
On finalizing the inverter topology for the two-level and three-level NPC the model was simulated in Ltspice. This simulation was done for different modulation indices and varying load conditions to identify the change in current at different points.

### 1.1 Background

An electric powertrain refers to the system in an electric vehicle (EV) or hybrid vehicle that converts electrical energy from the vehicle's energy storage system (such as batteries) into mechanical energy to propel the vehicle. It typically consists of several components including the electric motor, power electronics, transmission, and sometimes a gearbox.

Almost all electric vehicle manufacturing companies are presently using two-level inverter with permanent magnet synchronous machine (PMSM) for their traction application. Two-level inverter is a well-travelled field for DC-AC inverter system and PMSM provides high power density, which is one the major concern for automotive industries. However, two-level inverters have problem with high switching losses at higher switching frequencies, which is governed by the thermal limitation of the switches. This problem is more prominent when the DC-link voltage goes higher, as the device voltage ratings needs to be increased for a long-range electric vehicles.

The components included in the powertrain and effecting the operation of the vehicle are discussed below:



**Figure 1.1:** Electric Powertrain[2]

### 1.1.1 Battery

The battery pack and Battery Management System (BMS) are critical components of an electric vehicle (EV). The battery pack, typically consisting of numerous cells of different chemistry, serves as the primary energy storage unit. The cells are arranged in both series and parallel formations to reach the required voltage and capacity. The BMS supervises the battery pack, guaranteeing optimal performance, extended lifespan, and safety.

#### Battery Pack

The battery pack stores and supplies electrical energy to the vehicle's electric motor. It comprises individual cells encased in modules, which are then assembled into the battery pack. The chemistry, such as lithium-ion, is chosen for its high energy density, long cycle life, and relatively low self-discharge rate. Key parameters monitored by the BMS include cell voltage, temperature, and state of charge (SoC).

**Battery Management System (BMS)** The BMS, an electronic system that oversees the battery pack, carries out several vital functions: it monitors cell voltages to avoid overcharging and excessive discharging, balances cell charge for consistent performance, and regulates thermal conditions to prevent overheating. Additionally, the BMS communicates with the vehicle's control system to deliver real-time data and diagnostics.

However, over the vehicle's lifespan, EVs typically result in lower total emissions in comparison to internal combustion engine (ICE) vehicles. This advantage grows if the electricity used to charge EVs is sourced from renewable energy. Advances in battery recycling and second-life applications for EV batteries also promise to

mitigate some environmental impacts.

### 1.1.2 Electric Machines

Electric vehicles (EVs) rely on electric machines, or electric motors, to convert electrical energy from the battery into mechanical energy, which drives the wheels. These motors are critical for the performance, efficiency, and overall functionality of EVs. Understanding the types of electric machines used and the electromagnetic interference (EMI) emissions they produce is essential for optimizing EV design and operation.

- **Induction Motors (IMs):**

IMs operate on the principle of electromagnetic induction. The stator generates a rotating magnetic field that induces currents in the rotor, which then creates a magnetic field to produce torque.

- **Permanent Magnet Synchronous Motors (PMSM):**

PMSMs use permanent magnets embedded in the rotor to generate a constant magnetic field. The stator, which contains windings, produces a rotating magnetic field when powered.

- **Brushless DC Motors (BLDCs):**

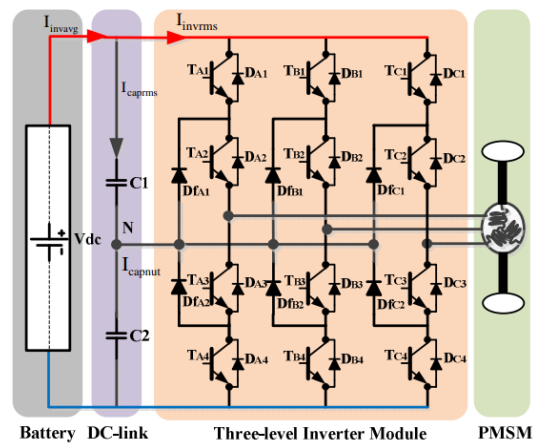
BLDC motors are similar to PMSMs but are typically controlled using a different commutation method, resulting in a simpler control scheme.

Electromagnetic interference (EMI) is a crucial aspect of electric vehicle design because it can impact the performance of both the motor and the vehicle's electronic systems. Various factors contribute to EMI emissions in electric machines:

- Harmonics
- Switching Frequencies
- Parasitic Capacitance and Inductance
- Grounding and Shielding
- High-Speed Rotating Components

### 1.1.3 Inverter

In electric vehicles (EVs), the three-phase inverter is a vital component of the powertrain system. It converts DC power from the vehicle's battery into AC power to drive the three-phase electric motor, which propels the vehicle. Understanding the types of three-phase inverters in terms of levels is essential for optimizing efficiency, performance, and cost-effectiveness in EV design.



**Figure 1.2:** Schematic representation of a typical three-level NPC traction inverter [3]

### Two-Level Inverter:

The two-level inverter is the simplest configuration, consisting of switches that connect the DC input to one of two voltage levels (positive or negative).

### Multilevel Inverters:

Multilevel inverters have more than three voltage levels, typically achieved by stacking multiple power semiconductor devices and capacitors in series.

They can generate output waveforms with higher resolution, resembling sine waves more closely than two-level or three-level inverters.

Advantages: Reduced harmonic distortion, lower electromagnetic interference (EMI), and improved motor performance. Disadvantages: Higher complexity, increased component count, and higher cost compared to simpler inverters.

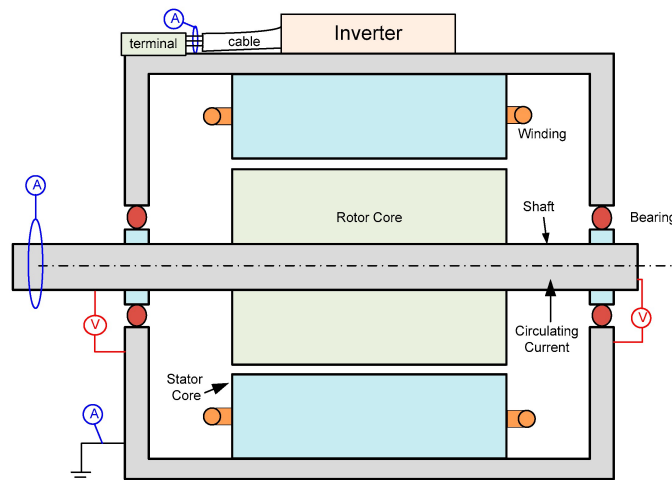
### 1.1.4 Bearing Current

When the load draws current from the fast-switching converter, High-Frequency currents flow as the output, which induces high Electromagnetic Interference which is either radiated or conducted emissions.

In an electric machine, several parasitic capacitances arise due to the separation of pairs of electrodes by an insulating medium or due to a gap in the metallic surface such as rotor-stator and stator and windings. This capacitance causes a common-mode (CM) current to flow during each inverter switching transition due to changes in the CM voltage. The CM current enters the machine through the windings, passes through to each sheet of the stator lamination stack, and exits through the grounding cable connected to the machine housing.

### 1.1.5 EMI

Electromagnetic Interference refers to the disturbance in a device due to the electrical properties or operation of another device. EMI can be categorized into two



**Figure 1.3:** Bearing Current [4]

types based on how the interference is transmitted:

- **Conducted EMI:** This type of interference travels through conductive media, such as wires and cables.
- **Radiated EMI:** This type of interference propagates through space as electromagnetic waves.

### Mitigation

- **Filters:** Filtering selectively attenuates electromagnetic signals at specific frequencies, effectively reducing the amplitude of unwanted interference. This helps in minimizing the impact of EMI on sensitive electronic devices
- **Loop Size:** In electronic circuits, adjacent conductors can induce voltages in each other through electromagnetic induction. This is particularly significant when conductors form loops. Reducing the size of loops decreases the area through which magnetic flux can intersect nearby conductors, thus reducing the amount of induced voltage and minimizing the potential for interference.
- **Grounding Shielding:** Shielding involves surrounding sensitive components or circuits with conductive materials to create a barrier that blocks or absorbs electromagnetic radiation.

Proper grounding of shielding materials is crucial to their effectiveness. By connecting shielding to ground, any intercepted electromagnetic energy can be safely diverted away from sensitive components and dissipated.

- **Separation:** When sensitive circuits are located close to sources of EMI, such as motors or power lines, electromagnetic fields from these sources can induce unwanted voltages or currents in nearby conductors. By physically separating sensitive components from sources of EMI, the likelihood of coupling decreases, reducing the potential for interference.

Due to the increased demand in the high performance and efficiency of the inverters used in EVs, three-level inverters are gaining popularity, thus to reduce these

losses there is increasing interest in the development of 800V DC bus voltage for long-range electric vehicles [1]. Thus three-level NPC inverter is considered an alternative topology for EV drives instead of the conventional two-level inverter. Efficiency is one of the significant benefits of the three-level because it enables the use of low voltage-rated devices. This thesis presents an in-depth exploration of the three-phase three-level NPC inverter and its EMC performance in connection to the electric motor that is being used.

This thesis will examine the design considerations and the EMI generated at the AC side output of the 3-level and 2-level NPC inverter, and feeding this AC side output voltage from the inverter to an electric motor to calculate the AC side common mode current flowing through and around the motor, do a comprehensive analysis on the AC side common mode current and compare the current between the two-level and three-level inverter.

### 1.2 Aim

This project aims to simulate and analyse the common mode current flowing in between the 3 phase three-level NPC inverter and the electric machine and compare it with a 2 level NPC inverter.

### 1.3 Scope

Primarily this thesis aims to measure the amount of AC side common mode current flowing from the circuit through the ground and back to the circuit. As the inverter used in the traction system is mostly two-level inverter this thesis aims to develop both a two-level and a three-level NPC inverter to showcase the usage of a three-level inverter instead of a two-level inverter. The primary focus will be on evaluating key performance metrics such as harmonic distortion under various load conditions and modulation index. Simulation data will be utilized to ensure a comprehensive and accurate comparison between the two inverters in the range of frequency 9KHz-100MHz. By exploring this aspect, the study determines the advantages and potential drawbacks of implementing a 3-level NPC inverter in EV applications.

In addition to performance metrics, this research will delve into the calculation and analysis of AC side common mode currents generated by inverters. Understanding the impact of these currents on the electromagnetic compatibility (EMC) of the electric vehicle system is crucial for optimizing design and ensuring reliable operation. The study will employ simulation tools like PLECS for generating the pulses from a modulator to be fed into the inverter switches designed in LtSpice, MATLAB/Simulink for theoretical analysis of S-parameters and LtSpice for harmonic analysis.

This thesis will include detailed discussions on the design principles, circuit dia-

grams, and control strategies for 3-level NPC inverter. The scope of this research remains focused and manageable, providing clear insights into the comparative performance of two-level inverter and a three-level NPC inverter.

## 1.4 Outline

The idea was to design two inverters, a three-level and a two-level. First, the inverter was designed in PLECS since the modulator of an inverter can be designed there. The problem with PLECS was that it gave the output but only ideal waveforms. It couldn't show any ringing in waveforms and the frequency analysis could also be not performed there. Hence, the pulses from the modulator were exported and imported in LTSpice, where again the model was constructed.

First, a single switch was made and a double pulse test was conducted to check the working of the switch with the MOSFET driver. Later single phase was constructed and the output was analysed subsequently, the entire inverter was built and the simulation was run for 1 ms, which was for 1 fundamental period of the wave.

Next, the FFT of the voltage was computed and studied for various configurations of the two inverters. The next leg of the thesis was to obtain the Z-Parameters and calculate the common mode currents in the machine. A CLC filter was also included on the DC side of the network to reduce the common mode current.



# 2

## MOSFET drivers

MOSFET gate drivers play a vital function in power electronics, effectively managing the switching of MOSFETs. They enhance control signals to match the voltage needs of MOSFET gates, guaranteeing swift switching speeds and ample drive force to surmount gate capacitance.

Moreover, gate drivers frequently offer isolation between control and power circuits to enhance safety, incorporating protective functions such as overcurrent and over-voltage protection. As we are using a multilevel 3-phase inverter, which works by the SVPWM Modulation technique, the usage of the driver circuit is essential to synchronize various switches and pulses.

In the realm of hard switching, MOSFETs rapidly alternate between fully conducting and fully non-conducting states, resulting in significant switching losses due to voltage and current overlap during this transition. To mitigate these losses and ensure efficient performance, MOSFET drivers must offer rapid rise and fall times to swiftly transition the MOSFET between these states. Moreover, they need ample current-driving capability to efficiently charge and discharge the MOSFET's gate capacitance.

Conversely, in soft switching, the objective is to diminish switching losses by ensuring that MOSFETs switch at points of zero voltage or zero current. This strategy often entails supplementary circuitry like resonant tanks or active clamps. MOSFET drivers utilized in soft switching scenarios must precisely manage switching timing to synchronize with these zero voltage or zero current conditions.

### 2.1 Type of MOSFET Drivers

#### 2.1.1 Hard Switching

In hard switching applications, MOSFET drivers with adjustable slew rates enable optimization of switching characteristics, such as reducing switching losses by minimizing voltage and current overlap during transitions. Faster slew rates facilitate quicker switching times, which can improve efficiency and reduce power dissipation.

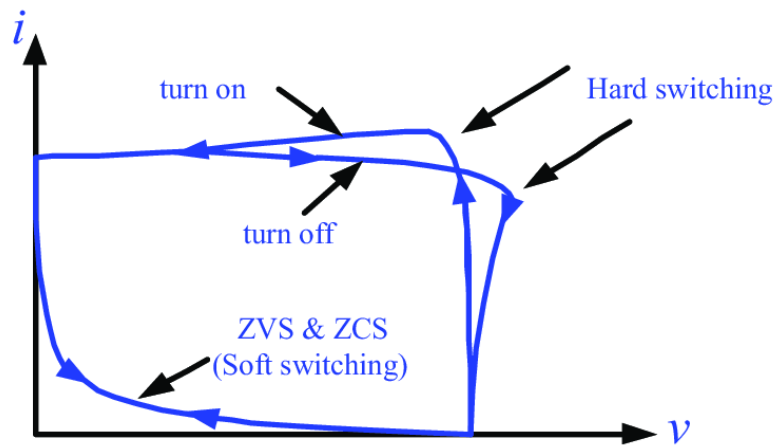


Figure 2.1: Soft vs Hard Switching [5]

### 2.1.2 Soft Switching

In soft switching configurations, MOSFET drivers with tailored slew rates play a critical role in achieving zero voltage or zero current switching conditions. By finely adjusting the slew rate, these drivers ensure precise control over the timing of the switching events, aligning them with the desired zero voltage or zero current points to minimize losses and maximize efficiency. Fig 2.1 shows a typical representation of hard switching vs soft switching.

## 2.2 Slew Rate Control

The slew rate control circuit controls inrush current. When a huge load which is capacitive in nature, is connected to the output MOSFET, quickly turning it on results in a significant current flow to charge the load. This can cause an instantaneous drop in voltage and an increase in current, potentially leading to system instability or malfunction. The slew rate control circuit limits the inrush current to ensure a stable system startup.

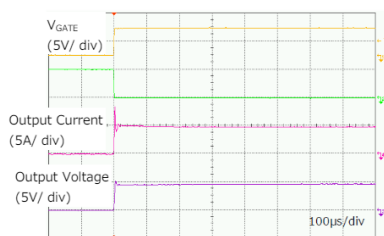


Figure 2.2: Low Slew Rate

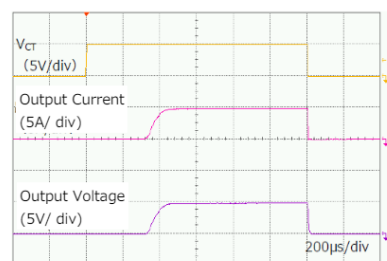


Figure 2.3: High Slew Rate

The switches in the inverter have slew rate control driver circuits. Fig 2.4 shows the driver circuit designed and implemented in LtSpice for this thesis work, the P-Channel MOSFET is responsible for the Turn-On, whereas the N-channel MOSFET





# 3

## Modulators

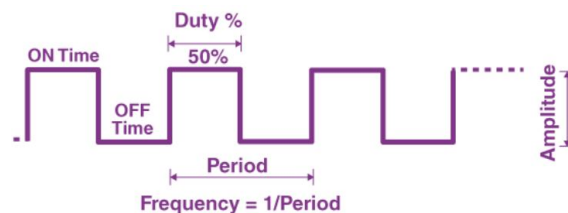
Modulators are components in inverters that control the switching of semiconductor devices (such as MOSFETs or IGBTs) to generate the desired output waveform. Inverters use modulation techniques to convert DC power to AC power efficiently and accurately. This section discusses about different modulation techniques used in inverters to control the output voltage.

### 3.1 Pulse Width Modulation

PWM is an analog modulating scheme where the duration or width or time of the pulse carrier varies proportional to the instantaneous amplitude of the message signal. A PWM is a digital uni-polar square wave signal where the duration of the ON time can be changed as intended. This way the power delivered to the load can be controlled from a micro controller. A PWM signal stays “ON” and “OFF” for a certain time. The percentage of time for which the signal remains “ON” is known as the duty cycle. If the signal is always “ON,” then the signal must have a 100% duty cycle. The formula to calculate the duty cycle(D) is given as follows:

$$D = \frac{t_{on}}{t_{on} + t_{off}} \quad (3.1)$$

The average value of the voltage depends on the duty cycle. As a result, the average value can be varied by controlling the width of the “ON” of a pulse. Using PWM



**Figure 3.1:** PWM signal with duty cycle of 50% [6]

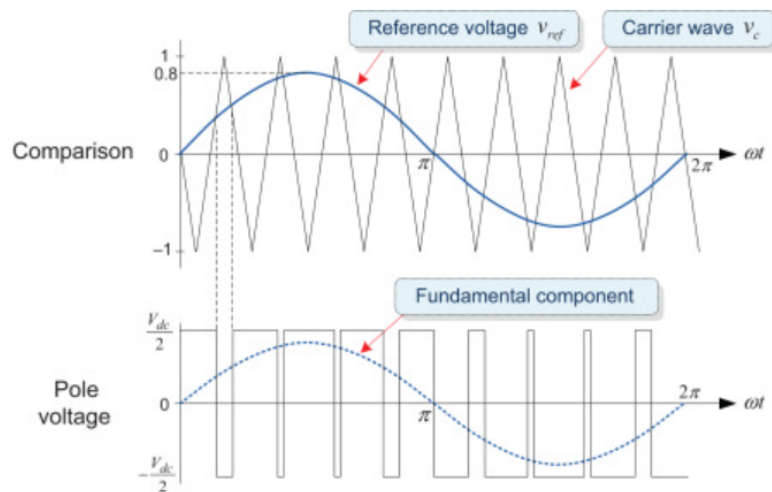
modulation techniques in an inverter reduces overheating, faster response time, and provides a high input power factor but at higher frequencies the switching losses are high[6].

## 3.2 Sinusoidal Pulse Width Modulation

In this technique, to find the switching states for each pole in the inverter, the high-frequency triangular carrier wave  $V_c$  is compared with the sinusoidal AC voltage reference  $V_{ref}$ . After comparing, the switching states is determined through the following two rules:

- Voltage reference  $v_{ref} >$  Triangular carrier  $v_c$ : upper switch is turned on (pole voltage=  $V_{dc}/2$ )
- Voltage reference  $v_{ref} <$  Triangular carrier  $v_c$ : lower switch is turned on (pole voltage=  $-V_{dc}/2$ )

The DC-link voltage  $V_c$  is the triangle carrier wave's peak-to-peak value. The requirement for linear modulation in this PWM approach is that the voltage reference  $V_{ref}$  amplitude stay below the triangle carrier  $V_c$  peak, that is,  $V_{ref} \leq \frac{V_{dc}}{2}$ . This type of PWM approach is known as a carrier-based PWM technique because it uses a high-frequency carrier wave to modulate voltage. In particular, because the reference is provided in the form of a sine wave, this carrier-based approach is known as Sinusoidal Pulse Width Modulation. This is also called the triangle-comparison PWM technique since this uses the carrier of a triangular wave. Fig 3.2 depicts the SPWM technique for one phase[7].



**Figure 3.2:** Sinusoidal PWM technique for one phase [8]

### 3.3 Space Vector Modulation

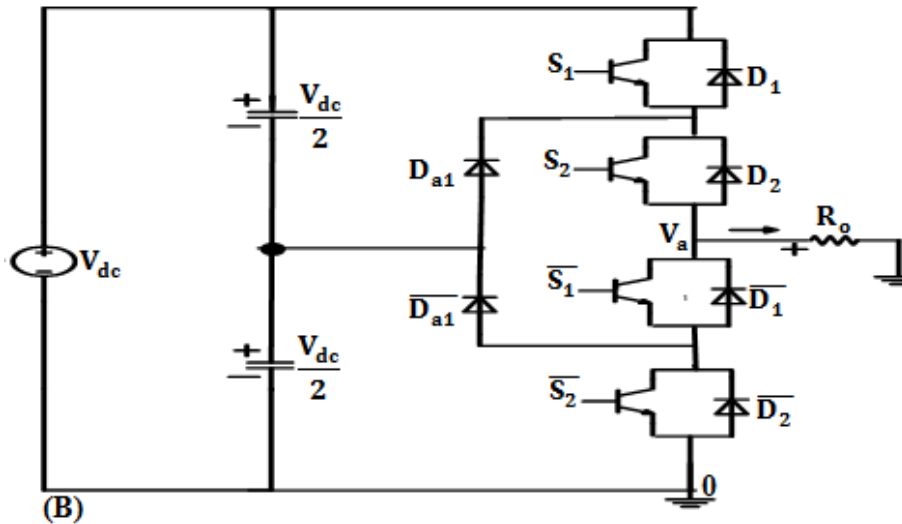


Figure 3.3: Multilevel Inverter , Single Leg [9]

S1	S2	Vdc
S1'	S2	0
S1'	S2'	-Vdc

Each leg in the above multilevel inverter corresponds to three switching states. Hence the inverter has in total  $3 \times 3 \times 3 \rightarrow 27$  switching states. These switching states can be classified into Large Vectors, Medium Vectors, and Small Vectors.

#### Large Vectors:-

- Used when the reference voltage vector lies closer to the boundaries of the modulation space.
- By using large vectors, the modulation technique aims to achieve better accuracy in approximating the reference voltage.
- These vectors trace only the non-zero vectors. here none of the output voltage is zero.

+	+	-	$\frac{2}{3} * (Vdc \angle 60)$
-	+	-	$\frac{2}{3} * (Vdc \angle 120)$
-	+	+	$\frac{2}{3} * (Vdc \angle 180)$
-	-	+	$\frac{2}{3} * (Vdc \angle -120)$
+	-	+	$\frac{2}{3} * (Vdc \angle -60)$
+	-	-	$\frac{2}{3} * (Vdc \angle 0)$

#### Medium Vectors:-

- Medium vectors are formed by combining active and zero vectors.
- They are chosen to balance between accuracy in approximating the reference voltage and minimizing switching losses.
- These vectors trace only the non-zero vectors. here none of the output voltage is zero.

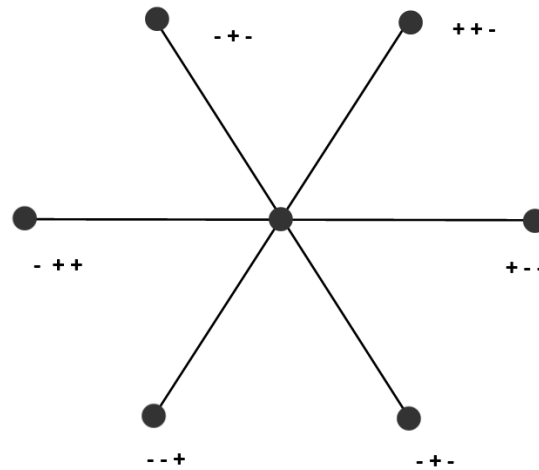


Figure 3.4: Large Vectors

++0	$\frac{2}{3} * (V_{dc}/(\sqrt{3})\angle 60)$
-+0	$\frac{2}{3} * (V_{dc}/(\sqrt{3})\angle 120)$
0+-	$\frac{2}{3} * (V_{dc}/(\sqrt{3})\angle 180)$
0-+	$\frac{2}{3} * (V_{dc}/(\sqrt{3})\angle -120)$
+0-	$\frac{2}{3} * (V_{dc}/(\sqrt{3})\angle -60)$
-0+	$\frac{2}{3} * (V_{dc}/(\sqrt{3})\angle 0)$

c

+00	0--
0+0	-0-
00+	--0
++0	00-
+0+	0-0
00+	--0

**Small Vectors:-**

- Small vectors are formed by only positives /negatives and zero
- They are a total of 12 vectors, although they occupy six positions in the space vector

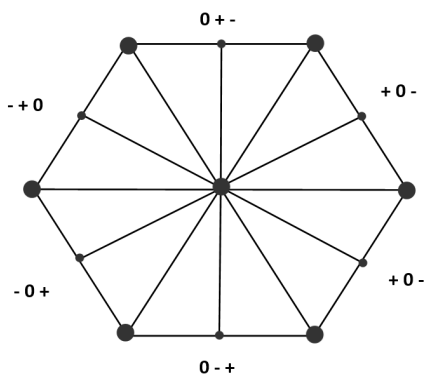


Figure 3.5: Medium Vectors

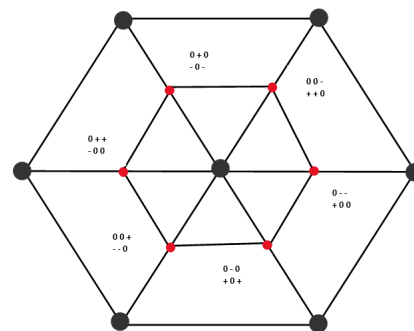


Figure 3.6: Small Vectors

The large vectors cut the hexagon into six sectors as shown in Figure 3.7. Then each sector is further divided into four triangles. A voltage vector  $V$  is used as a reference vector. This is further used to calculate the dwell time as shown in the table below

The criteria for selecting the switching pattern are akin to those for a two-level SVM.

It's preferable to have minimal or no alterations in switching when the reference vector  $V_{ref}$  transitions between sectors (regions). Transitioning from one switching state to another should ideally involve only two switches within the same leg, aiming to minimize device switching frequency.

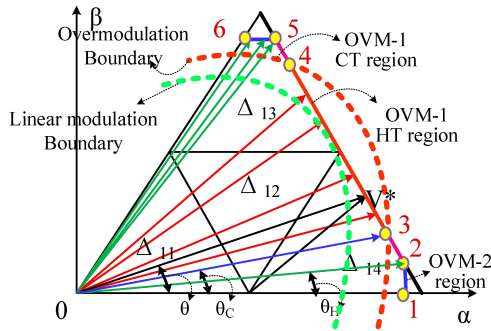


Figure 3.7: Sector [10]

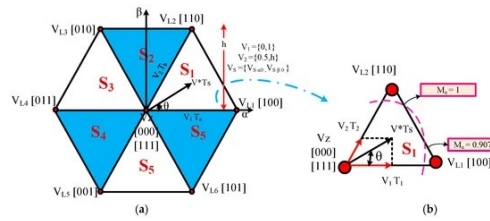


Figure 3.8: Triangle inside the sector [10]

$$V_\alpha = \frac{2}{3} \left( V_a - \frac{1}{2}V_b - \frac{1}{2}V_c \right) \quad (3.2)$$

$$V_\beta = \frac{2}{3} \left( \frac{\sqrt{3}}{2}V_b - \frac{\sqrt{3}}{2}V_c \right) \quad (3.3)$$

$$V_{ref} = V_\alpha + jV_\beta \quad (3.4)$$

After determining the reference voltage, the closest three vector positions can be identified. For any Multi-Level Inverter (MLI), an algorithm that utilizes the Volt-second balancing principle is employed to calculate the dwell time for the respective switches. According to this

$$VT_s = T_1V_1 + T_2V_2 + T_0V_0 \quad (3.5)$$

Where  $T_1$  is the dwelling time for the Voltage  $V_a$ ,  $T_2$  is the dwelling time for the Voltage  $V_b$  and  $T_0$  is the dwelling time for the Voltage  $V_c$ .

Below is the dwell time calculation for a sector in all the four regions.

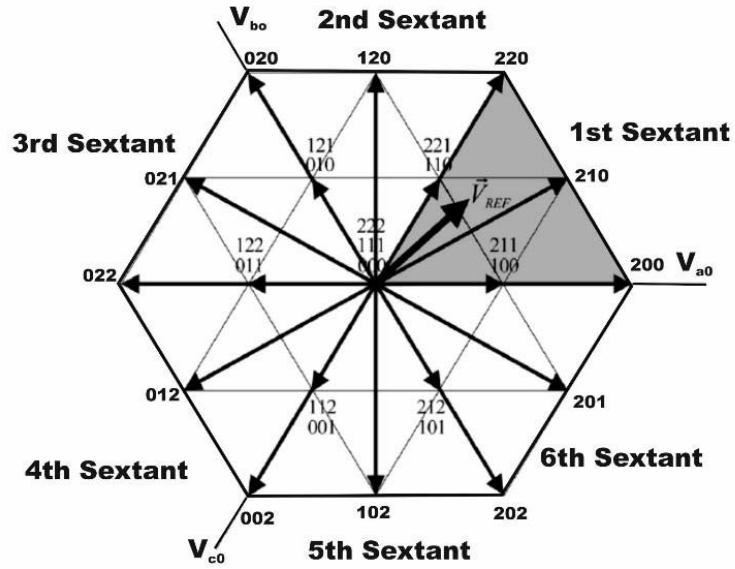


Figure 3.9: Space Vector NPC [11]

Region							
1	V0	V1	V2	V19	V2	V1	V0
	[OOO]	[POO]	[PPO]	[PPP]	[PPO]	[POO]	[OOO]
2	V1	V7	V21	V20	V21	V7	V1
	[POO]	[PON]	[OON]	[ONN]	[OON]	[PON]	[POO]
3	V1	V7	V13	V20	V13	V7	V1
	[POO]	[PON]	[PNN]	[ONN]	[PNN]	[PON]	[POO]
4	V2	V14	V7	V21	V7	V14	V2
	[PPO]	[PPN]	[PON]	[OON]	[PON]	[PPN]	[PPO]

Figure 3.10: Switching Sequence[Region Wise] [12]

Region	Vector $T_a/T_s$	Vector $T_b/T_s$	Vector $T_c/T_s$
1	$2ma \sin\left(\frac{\pi}{3} - \theta\right)$	$1 - 2ma \sin\left(\frac{\pi}{3} + \theta\right)$	$[2ma \sin(\theta)]$
2	$[1 - 2ma \sin(\theta)]$	$2ma \sin\left(\frac{\pi}{3} + \theta\right) - 1$	$1 - 2ma \sin\left(\frac{\pi}{3} - \theta\right)$
3	$2 - 2ma \sin\left(\frac{\pi}{3} + \theta\right)$	$[2ma \sin(\theta)]$	$2ma \sin\left(\frac{\pi}{3} - \theta\right) - 1$
4	$[2ma \sin(\theta) - 1]$	$2ma \sin\left(\frac{\pi}{3} - \theta\right)$	$2 - 2ma \sin\left(\frac{\pi}{3} + \theta\right)$

**Table 3.1:** Vector  $T_1/T_s$ , Vector  $T_2/T_s$ , and Vector  $T_0/T_s$  for different regions



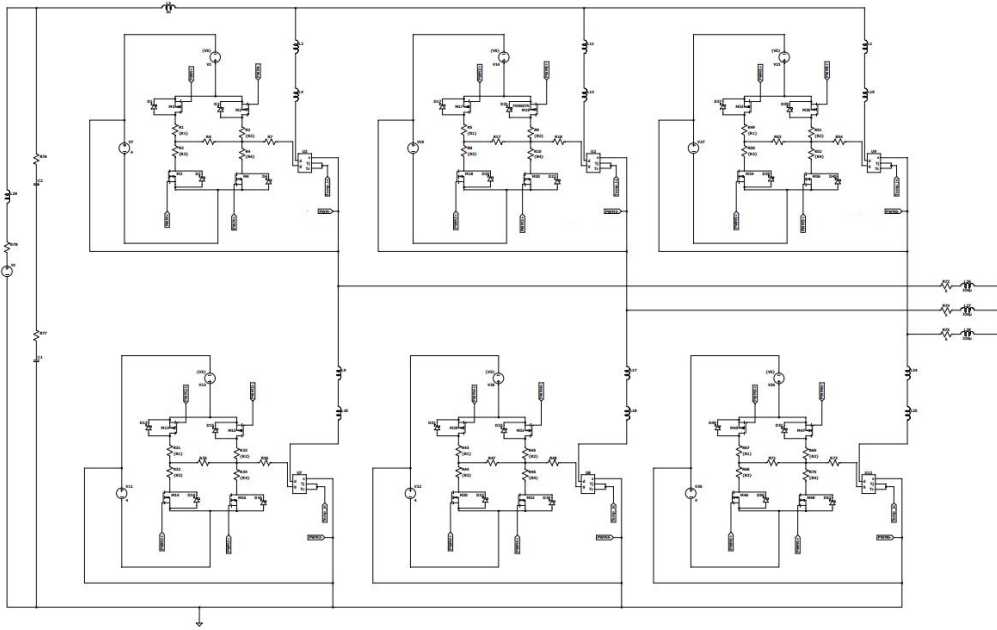
# 4

## Inverters

An inverter is a device that converts DC power to the AC power used in an electric vehicle motor. The inverter can change the speed at which the motor rotates by adjusting the frequency of the alternating current. It can also increase or decrease the power or torque of the motor by adjusting the amplitude of the signal. There are current source inverters and voltage source inverters, in Current Source Inverter the input DC source is connected to the inverter through a current source, and the output voltage waveform is controlled by varying the switching of the power electronic devices such as IGBTs in the inverter circuit and in Voltage Source Inverter the input DC source is connected to the inverter through a voltage source, the output voltage waveform is controlled by varying the switching of the power electronic devices such as IGBT's in the inverter circuit. A multilevel voltage source inverters is used in this thesis because of the unique structure that allows them to reach high voltages and power levels without the use of transformers. They are especially suited to high-voltage vehicle drives where low output voltage total harmonic distortion (THD) and electromagnetic interference (EMI) are needed.

### 4.1 Two Level Inverter

A two-level inverter is a type of voltage source inverter (VSI) that converts DC power into AC power with two voltage levels: positive and negative. The two-level inverters remain widely used in various industrial and commercial applications due to their simplicity and reliability. These inverters offer a relatively simple and cost-effective solution for many medium to high-power applications. However, they may have limitations compared to a MLI in terms of efficiency, harmonic distortion, and voltage levels. A topology of a 2-level inverter designed in Ltspice is shown in figure 4.1. The inverter consists of six switches, two for each leg, and the switching state for the six switches is shown in table 4.1.



**Figure 4.1:** Two-level Inverter model used for simulation

Switches	Phase A	Phase B	Phase C
S1	ON	OFF	OFF
S2	OFF	ON	OFF
S3	OFF	OFF	ON
S4	OFF	OFF	OFF
S5	ON	OFF	ON
S6	OFF	ON	OFF

**Table 4.1:** Switching state of Two-level inverter

## 4.2 Multi Level Inverter

Multilevel Inverter generates a desired output voltage from several DC voltage levels at its input. The input side voltage levels are usually obtained from renewable energy sources, capacitor voltage sources, fuel cells etc. Multilevel inverters nowadays are used for medium voltage and high power applications. In the concept of MLI topology, several DC voltage levels are added together to create a smooth output waveform. The obtained output waveform have lower  $\frac{dv}{dt}$  and harmonic distortions. The different field of applications include its use as UPS, High voltage DC transmission, Variable Frequency Drives, in pumps, conveyors etc.

The major issue of moving from a two level inverter to a multi-level inverter in a traction system is their  $\frac{dv}{dt}$  issues. High-frequency transitions inside an multi-level inverter are unavoidable due to the faster switching transition of

the MOSFET's/IGBT's. Due to these fast transitions and the existence of parasitic inductances and capacitances, EMI issues emerge in both conducted and transmitted emissions. These EMI noises in an inverter are emitted mainly through the cable. So, these high frequency noises at the inverter output causes voltage spikes that reduce the motor lifetime by damaging the windings, insulation and bearing ball.

### 4.2.1 Neutral Point Clamped MLI

A Neutral Point Clamped MLI is used to convert DC power to AC power with multiple voltage levels. In an NPC MLI, the DC input power is converted into an AC output waveform with several discrete voltage levels, which enables higher quality output voltage compared to traditional two-level inverters. NPC MLIs are commonly used in high-power applications such as motor drives and electric vehicle propulsion due to their ability to generate high-quality output waveforms with relatively simple circuit topologies. Considering the advantages of an NPC compared to the above two MLI, a three-level Neutral Point Clamped is implemented in this thesis. A typical schematic of a three level NPC is shown in fig 4.2.

#### Advantages :

- Reduced  $dv/dt$  and harmonics due to its five-level line-to-line voltage, offering lower stress on motor or transformer windings compared to the two-level inverter, which typically has higher  $dv/dt$  and harmonics. This reduction in stress benefits the longevity of the equipment.
- The NPC's topology ensures that switches endure only half of the DC bus voltage during commutation between certain states, minimizing switching stresses during transitions.
- The input current exhibits minimal distortion, contributing to smoother operation.

#### Disadvantage :

- Increased complexity in controlling and modulating the system, posing challenges in implementation and maintenance.
- Uneven load distribution on switches, where certain switches are consistently more active than others. For instance, S2 is always on in one state, and S3 is always on in another. This issue has been addressed by replacing clamping diodes with switches to balance the load distribution.

The main components and their operation are listed below:

#### 4.2.1.1 Clamping Diodes

The clamping diodes are connected between the DC bus and the midpoint of each phase. These diodes ensure that the midpoint voltage remains clamped at a reference voltage, usually half of the DC bus voltage. This placement of the diodes reduces the voltage stress on the switching devices and allows for the generation of multiple voltage levels in the output waveform.

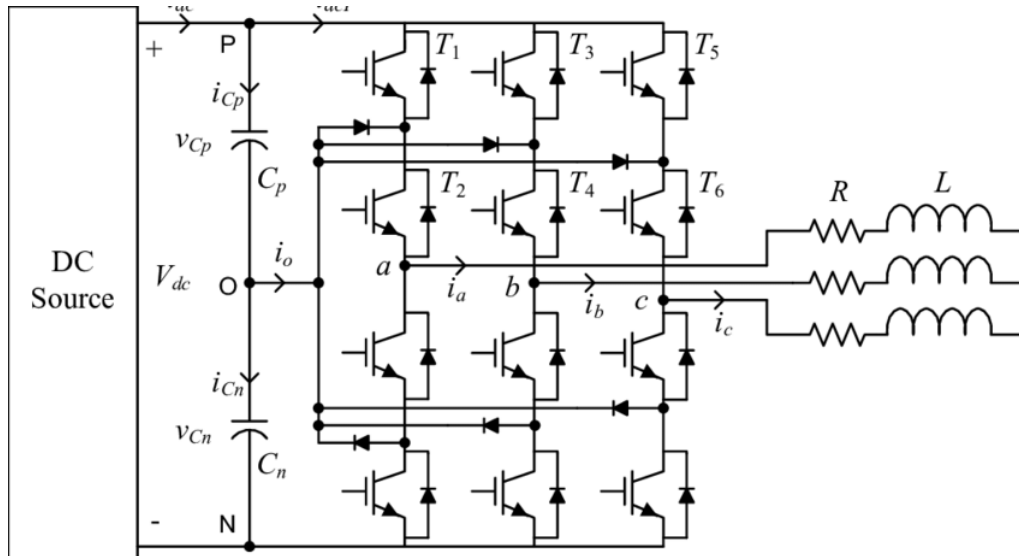


Figure 4.2: 3-level NPC [13]

#### 4.2.1.2 Switching Devices

Each phase of the NPC MLI contains a set of switching devices, such as insulated gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs). These devices are controlled to connect the phase to either the positive or negative DC bus or to the midpoint, depending on the desired output voltage level.

#### 4.2.1.3 Control Circuits

The control circuits of an NPC MLI is responsible for generating the switching signals for the switching devices to produce the desired output voltage waveform. The control algorithm typically involves modulation techniques such as PWM to achieve the desired voltage levels and minimize harmonic distortion in the output waveform.

#### 4.2.1.4 DC Power Source

An NPC MLI requires a DC power source, such as a battery pack or a DC bus derived from a rectifier, to supply power to the inverter. The voltage level of the DC source determines the maximum amplitude of the output voltage waveform.

### 4.2.2 Modelling

The 3-level inverter for this thesis was developed using the switch used from the double pulse test. The below figure 4.3 shows the schematic of 3-level NPC MLI designed and simulated in LTspice. The input of the inverter is a 800V DC source, the positive terminal is connected to the drain of the power MOSFET and the negative is connected to the source of the power MOSFET.

The 3-level inverter consists of 12 switches these switches help in regulating the output multilevel voltage. Diodes  $D_{18}$  and  $D_{19}$  are used as clamping diodes and they clamp the voltages to half the DC bus voltage. Capacitors  $C_1$  and  $C_2$  are connected to neutral point of the topology and ensures the voltage between the upper and lower switching devices are balanced to minimize the voltage stress on the device. Each switch consists of four driver MOSFET's whose gate signal is controlled by the SVPWM pulse generated. The SVPWM pulse is imported from an ideal three-phase three-level neutral point-clamped MLI designed in PLECS software.

Parasitic elements such as inductors and resistors are introduced in the inverter to replicate non-ideal conditions. The parasitic inductance is caused by the wires and PCB traces that connect the components of the inverter. This inductance can cause voltage spikes and ringing during switching. The parasitic capacitance is between two adjacent traces and the inherent capacitances of the switches. The value for the parasitic inductance is 10nH and the capacitance is  $300\mu\text{F}$

An RL load has been considered for the inverter, the value of the inductor was taken as  $320\mu\text{H}$  and a higher resistance value varying from  $5\Omega$  to  $30\Omega$  is taken, the higher value of the resistance is taken considering the back EMF of the machine.

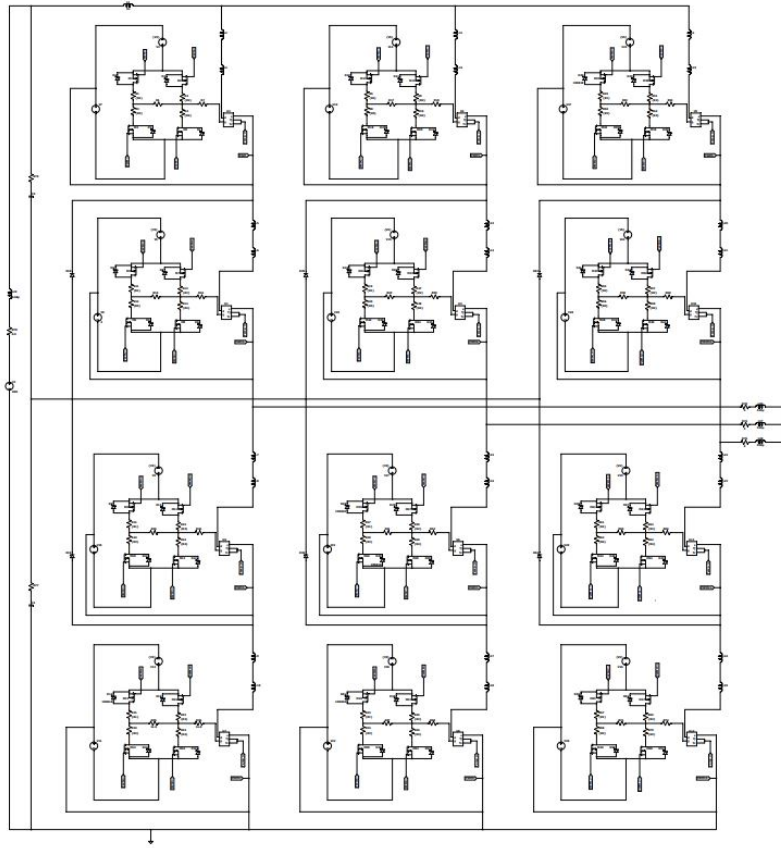
### 4.3 CM current filter

Common mode currents are caused by coupling between the cables and the ground due to parasitic capacitance or EMI. Even though they are comparatively small, when compared to differential mode currents, they cause large radiated electric fields since they flow in a large loop. So, the main cause of emission noise in a circuit is common mode currents.

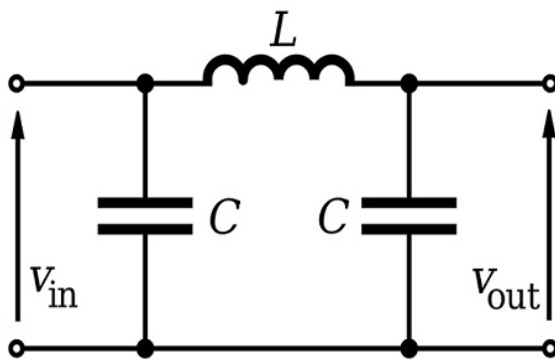
To reduce the CM currents flowing in the circuit a CLC filter is introduced at the input of the inverter in the LtSpice model. A simple schematic of a CLC filter is shown in figure 4.4 and the filter implemented in the thesis is shown in figure 4.5.

CLC is derived from the order of arrangement of the components in the circuit ie., the input voltage source is connected to a Capacitor then an inductor and the output of the inductor is connected another capacitor as seen from fig 4.5. The capacitor implemented in the thesis is a Y-type capacitor, Y capacitors, sometimes referred to as safety capacitors, are a kind of capacitor that is frequently employed in electrical circuits to offer safety insulating and for electromagnetic compatibility (EMC). Below is a brief overview of each component of a CLC filter shown in fig 4.5,

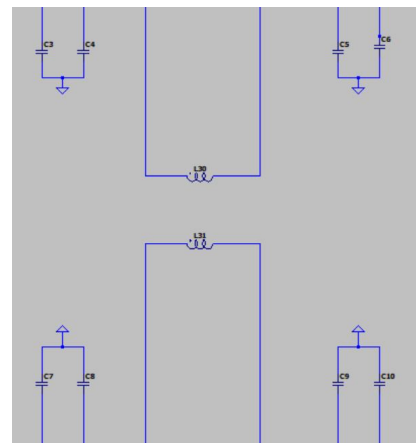
- **Capacitor 1** - The first Y capacitors are used in the circuit to reduce ra-



**Figure 4.3:** Schematic of 3-level NPC MLI used for simulation



**Figure 4.4:** simple CLC filter



**Figure 4.5:** CLC filter implemented in simulation

radio frequency interference (RFI) and electromagnetic interference (EMI). They lessen conducted and radiated emissions, which helps to filter out noise and ensure that the equipment conforms with EMC regulations.

- **Inductor** - The inductor is positioned in between the two capacitors, it aids in eliminating the harmonics and high-frequency interference from the input signal. By attenuating high-frequency components, it functions as a low-pass filter, permitting only low-frequency components to pass through.
- **Capacitor 2** - The second capacitor is positioned at the output of the inductor to further filter out high-frequency noise and smooth down the voltage waveform. Additionally, it improves in output voltage stabilization.



# 5

## Common Mode current

There are basically two types of current flowing through the circuits namely Differential mode currents and Common mode currents,

**Differential Mode Currents:** Differential Mode Currents flow through a circuit's conductors in opposite directions, creating a voltage difference between them. These currents are typically the intended signals or power that is transmitted through the circuit. In power electronics, for example, the main power flow from a source to a load is usually considered differential mode current.

**Common Mode Currents:** Common mode currents flow through a circuit's conductors in the same direction. They are usually the unwanted or undesirable currents that can result from various sources such as electromagnetic interference (EMI) or ground loops.[19] Common mode currents can introduce noise into the circuit and may interfere with the proper operation of sensitive electronic equipment. In electrical systems, common mode currents often flow along unintended paths, such as through the ground or chassis of the equipment. This thesis will focus on the estimation the common mode currents flowing through the machine and the ground.

### 5.1 Estimation of CM current in Bearings

The voltage induced over the bearings causes the bearing currents in electric machine. In large motor uneven flux distribution causes high frequency bearing currents to be induced in the motor shaft. Voltage pulses fed by the inverter contain high frequencies and the leakage capacitances of the motor winding provide paths for currents to flow to the earth. This induces a voltage between the shaft ends. If the induced voltage is high enough to overcome the impedance of the oil film of the bearings, a circulating type of high frequency bearing current occurs which is the undesirable common-mode currents.

Common-mode currents can have several effects in inverters as well as electric machines. Here are some of the key effects:

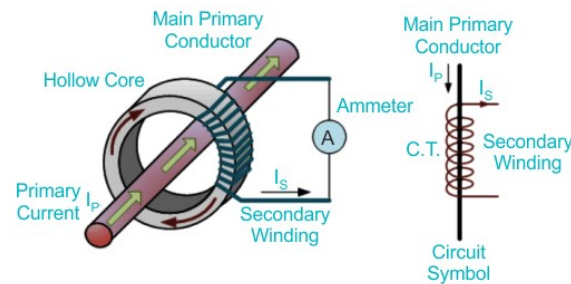
- **Electromagnetic Interference (EMI)** : Common-mode currents can generate electromagnetic fields that may interfere with other nearby electronic devices or communication systems. This interference can manifest as noise or malfunctions in sensitive electronic equipment.

- **Grounding Issues** : Common-mode currents flowing through ground paths can lead to ground loop problems, where there are multiple paths for current flow between different ground points. Ground loops can introduce noise, voltage fluctuations, and potential safety hazards in the electrical system.

There are many principle methods for measuring the current, by using Current transformers, Rogowski Coils and current shunts and S-parameters. A small brief on their principle is mentioned below:

### 5.1.1 Current Transformers

A current transformer (CT) is a type of instrument transformer used in electrical power systems. Its primary function is to measure alternating current (AC) by transforming high currents into a proportionally lower, safer, and measurable value that can be utilized by instruments and meters. Fig 5.1 shows the construction of CT.



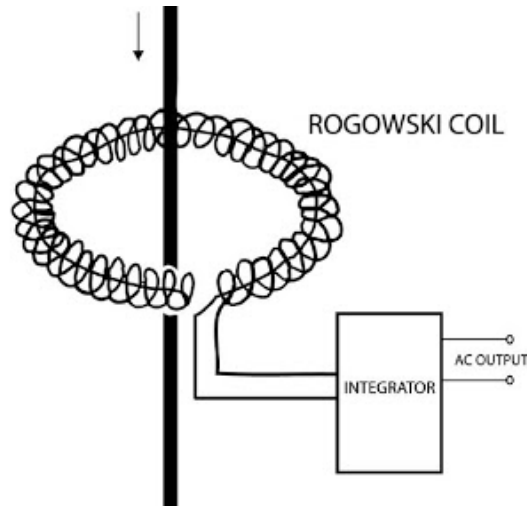
**Figure 5.1:** CT construction and symbol [14]

AC is induced within the secondary winding. Whenever AC is supplied throughout the primary winding, an alternating magnetic flux is produced. The load impedance for this kind is relatively low. As a result, this transformer operates in a short circuit. Consequently, the secondary winding's current depends on the main winding's current but is independent of the load impedance.

### 5.1.2 Rogowski Coils

The Rogowski coil is defined as an electrical device that is used to measure alternating current (AC). It is also used to measure the high-speed transient, pulsed current or sinusoidal current. Fig 5.2 shows a simple construction of a Rogowski Coil.

Rogowski coils work on the principle of Faraday's law. It is similar to AC current transformers (CTs). In current transformers, the voltage induced in a secondary coil is proportional to the current flow through the conductor. The difference between Rogowski coils and AC current transformers is in the core. In Rogowski coils, an air core is used and in the current transformer, a steel core is used. When current passes through the conductor, it will create a magnetic field. Due to an intersection with a magnetic field, a voltage is



**Figure 5.2:** Simple Schematic of Rogowski Coil [15]

induced between the terminals of the Rogowski coil. The magnitude of voltage is proportional to the current passes through the conductor. Rogowski coils are close pathed. Generally, the output of Rogowski coils is connected with the integrator circuit. So, the coil voltage is then integrated to provide an output voltage that is proportional to the input current signal.

## 5.2 CM current Reduction

When Variable Frequency Drives utilize inverters, high common-mode voltages are developed. The resulting common-mode voltage will have a high frequency and high amplitude depending on the pulse-width modulation. The motor's rotor side experiences shaft voltage as a result of this common-mode voltage. There is a current flow in the bearings if the voltage induced in the motor shaft is greater than the breakdown voltage of the lubricant in the bearings. This is bad for the motor and eventually causes it to break down or stop working properly. In addition to damaging the motor bearings, current flow in the bearings ruins the output terminals and the electrical parts that are attached to the motor.

Below are some common techniques to reduce the CM currents:

- Isolation Transformers
- Passive and Active Filters
- CLC Filters

In this thesis a CLC filter is introduced at the input of the inverter as shown in the previous section fig 4.5.

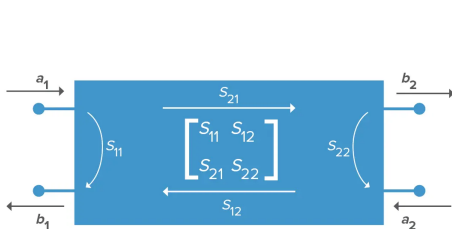


# 6

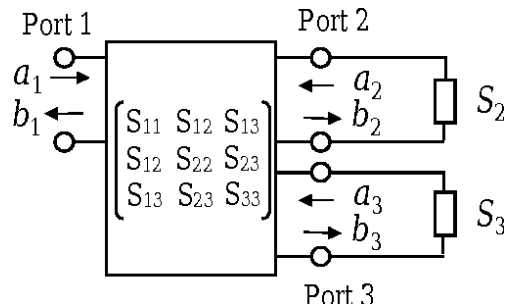
## S-parameters

This thesis involves working with higher frequencies so the above methods cannot be precise in estimating the high frequency currents in the machine, in order to get precise measurements of current, the S-parameter method is used in this thesis. This method can be used to measure the currents across a wide range of frequency and when the measurements are done with a calibrated VNA the measurements can be of very high accuracy and precision. Another reason for using the S-parameter is, the estimation methods used above can't measure the stray and parasitic elements present in the system. In order to utilize these parasitic elements to measure the current the S-parameter method is used in this thesis work.

S-Parameter describes the electrical behavior of linear electrical networks. S-parameters are used to help characterize how signals are transmitted and reflected in a network. These parameters are important in high frequency applications including radio frequency.[16]



**Figure 6.1:** 2-port device [17]



**Figure 6.2:** 3-port device [18]

For example, let's consider a 2 port circuit. From Fig 6.1 let's excite a power wave of some frequency, " $a_1$ " and " $a_2$ " is the incident wave from ports 1 and 2, " $b_1$ " is the transmitted wave, and " $b_2$ " is the reflected wave. Due to these excited power waves, the energy is scattered along the ports of the network and these scattered energies are the 'scattered parameters' the number of parameters in a s-matrix is decided by the number of ports in a circuit. The number of parameters is equal to the square of the number of ports, for a 2-port device the number of parameters in a matrix is 4. The physical meaning of  $S_{11}$  is the input reflection coefficient with the output of the network terminated by a matched load ( $a_2 = 0$ ).  $S_{21}$  is the forward transmission (from port 1 to port

2),  $S_{12}$  the reverse transmission (from port 2 to port 1) and  $S_{22}$  the output reflection coefficient. In this project the focus will be on the diagonal element of the matrix, the input and the output reflection coefficient.

In this project a 3-port device (electric machine) is taken for getting the s-matrix data. Since, a three-port device is taken the number of elements would be 9, below is a sample 3X3 matrix: 
$$\begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix}$$

## 6.1 Properties of S-parameter

The properties of S-parameters are essential in the characterizing of linear electrical networks, such as filters and amplifiers. These properties can help understand how signals propagate through these networks and how they interact with different components. Below are some property of the S-parameter:

- **Matched** : This property is taken if the characteristic impedance of all the three ports are same, then the diagonal elements of the matrix would become,  $S_{11} = S_{22} = S_{33} = 0$
- **Reciprocity** : This property states that the transmission port from a to b is equal to the transmission port from b to a for all  $a \neq b$  for example,  $S_{12} = S_{21}$

By applying the above two property the S- matrix becomes : 
$$\begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{12} & 0 & S_{23} \\ S_{13} & S_{23} & 0 \end{bmatrix}$$

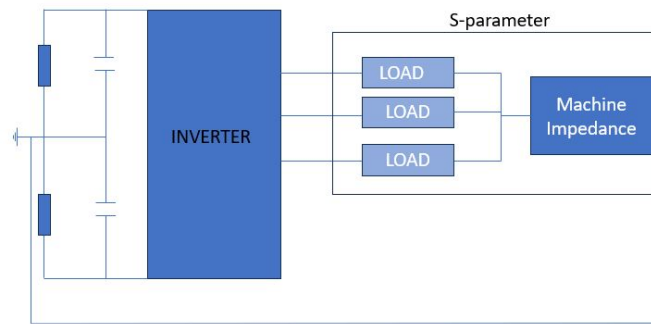
- **Lossless** : The lossless property states that the sum of the power reflected and transmitted from a port equals 1, indicating conservation of power. This property is crucial for maintaining signal integrity and efficiency in various applications. This can be expressed as:  $|S_{11}|^2 + |S_{12}|^2 = 1$ .

## 6.2 Estimation of S-parameter using VNA

In reality device called Vector Network Analyser(VNA) is used to calculate s-parameter. The Vector Network Analyser uses the transmission-reflection measurement method and reports the results in the form of a s-parameter matrix. For this project, a 3 port device, an electric machine will be used as shown in fig 6.2.

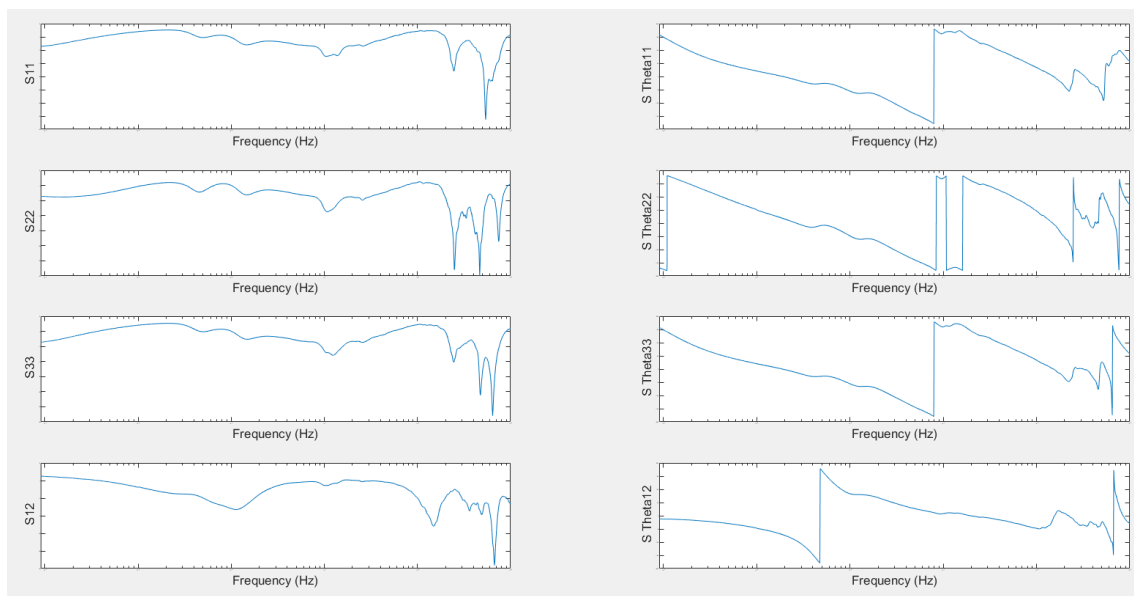
Here is the overview on how the VNA estimates the S-parameter of the electric machine:

- At first, the VNA generates electric signals at various frequencies, these frequencies can swept over a various range.



**Figure 6.3:** S-parameter for EM

- The generated signals are transmitted into the electric machine through the probes. The VNA typically has multiple ports for transmitting and receiving signals, since we are using a 3-port device three ports of the VNA is used and each of these port has a termination impedance  $50\Omega$  allowing for measurements of reflection and transmission properties at different points in the circuit.
- Once the signals have been transmitted, the VNA receives the signals that have been reflected back by the electric machine. It then measures the magnitude and angle of these reflected signals.



**Figure 6.4:** S Parameters Magnitude and Angle

The fig 6.4, shows the magnitude on the left side and angle of the diagonal element of the S-parameter matrix of the electric machine varying over a frequency range between 9KHz - 100MHz. For the frequency greater than 100 Mhz , a 3D Simulation would have been required the parasitic elements and

the resonance, hence this frequency range was covered.

### 6.3 Estimation of Z-parameter and Current

Similar to S-parameter the Z-parameters are used to describe the electrical behaviour of a linear network. The value of the Reflection coefficient( $\Gamma$ ) is needed to find the impedance value. The reflection coefficient is a parameter that describes how much of a wave is reflected by an impedance discontinuity in the transmission medium. It is equal to the ratio of the amplitude of the reflected wave to the incident wave, with each expressed as phasors.

In order to calculate the Z-parameter, the S-parameter has to be transformed to Z-parameter and the following equations are used to find the real and imaginary part of  $\Gamma$  and the Z-parameter,

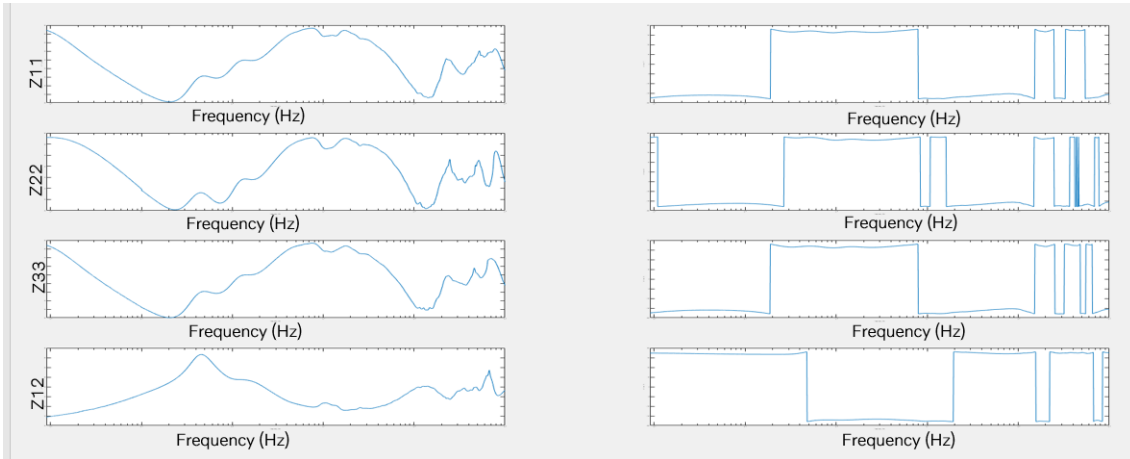
$$\Gamma_{real} = \cos\theta * S - parameter_{magnitude} \quad (6.1)$$

$$\Gamma_{imaginary} = \sin\theta * S - parameter_{magnitude} \quad (6.2)$$

$$\Gamma_{total} = \Gamma_{real} + \Gamma_{imaginary} \quad (6.3)$$

$$Z = Z_0 * ((1 + \Gamma)/(1 - \Gamma)) \quad (6.4)$$

$Z_0$  is the termination impedance at the measurement port that is  $50\Omega$ .



**Figure 6.5:** Z-Parameters (Impedance) Magnitude and Angle

Fig 6.5, shows the diagonal elements of the Z-Matrix [Impedance Matrix] converted from the S-parameter matrix.

To calculate the common mode current from the electric machine a simple schematic of Fig 6.3 is used in the thesis, the input for the electric machine will be the high-frequency output voltage from the inverter. The output voltage from the inverter will be converted to the frequency domain to be fed as an input to the machine (The output voltage from the inverter is converted

to the frequency domain because the VNA samples the S-parameter matrix in the frequency domain).

The three-phase voltages of the inverter from the simulation are measured with respect to ground and the S-parameter is converted to Z-parameter(impedance) and the following equation-6.5(in linear form) is converted to logarithmic form, as the voltage and the Z-parameter are in the frequency domain, to calculate the current equation-6.7 used,

$$I = \frac{V}{Z} \quad (6.5)$$

$$\log(I) = \log\left(\frac{V}{Z}\right) \quad (6.6)$$

$$\log(I) = \log(V) - \log(Z) \quad (6.7)$$

### 6.3.1 Machine Parameters

As the impedance of the machine was computed from the S Parameters, the machine parameters were estimated.

$$\omega = 2\pi f$$

Inductive Reactance ( $X_L$ ):

$$X_L = \omega L$$

Capacitive Reactance ( $X_C$ ):

$$X_C = \frac{1}{\omega C}$$

Now, for high frequencies, as the frequency increases, Impedance can be seen increasing, which implies that in this region the Inductance is Dominant as  $X_L$  is directly proportional to frequency.

Whereas for lower frequency as the frequency increases impedance decreases, which shows its capacitance behavior, as  $X_C$  is inversely proportional to frequency.

The impedance curve with reflective parameter was used for the estimation of machine parameter ranging from frequency 9KHz to 100 MHz.

As seen in 6.6, the impedance curve has two valleys. Considering a single valley, which is shown inside the dashed box. Each valley corresponds to one L-C network. The valley can be divided into low frequency and high frequency region. In the low frequency region the impedance drops as the frequency increases. Hence, in this region the capacitive element is dominant and we estimate the capacitance by assuming the impedance in the low-frequency region as a straight line and calculating the slope of the line.

The equation of a straight line is  $y=mx$ , where  $y$  and  $x$  are the respective coordinates on the straight line and  $m$  is the slope of the line.

The impedance  $Z$  of a capacitor is given by:

$$Z = \frac{1}{2\pi fC}$$

Given the points  $(10^4, 63)$  and  $(10^5, 23)$ , we need to calculate the slope of the line in a semilog plot (logarithmic scale on the  $x$ -axis and linear scale on the  $y$ -axis).

First, we transform the  $x$ -values to their logarithmic form:

$$\log_{10}(10^4) = 4 \quad \text{and} \quad \log_{10}(10^5) = 5$$

Next, we use the formula for the slope  $m$  of a line in a semilog plot:

$$m = \frac{y_2 - y_1}{\log_{10}(x_2) - \log_{10}(x_1)}$$

The slope  $m$  is:

$$m = \frac{23 - 63}{5 - 4} = \frac{-40}{1} = -40$$

To convert this slope to Farad we use the equation ;

$$C = 10^{\frac{\text{dB}}{20}}$$

$$C = 10^{\frac{-40 \cdot 2\pi}{20}}$$

Hence the Capacitance value comes to around , 23nF .

Simplifying:

$$C = \frac{1}{2\pi \cdot 630000} \approx \frac{1}{3958400} \approx 2.53 \times 10^{-7} \text{ F} \approx 253 \text{ nF}$$

Checking for one coordinate the value of capacitance Using the point  $(10^4, 63)$ :

$$63 = \frac{1}{2\pi(10^4)C}$$

Solving for  $C$ :

$$C = \frac{1}{2\pi(10^4) \cdot 63}$$

Thus, the capacitance is approximately 253 nF.

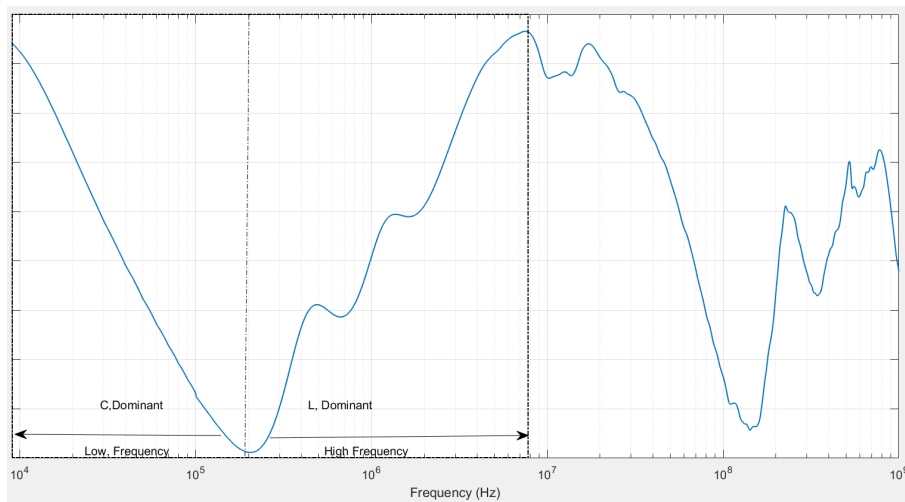


Figure 6.6: Machine Parameters

## 6.4 Common Mode Current Path

CM current is the current that flows in an electric machine's capacitive coupling elements through the ground and back to the inverter causing Electro-magnetic Interference. The fig 6.7 shows the common mode current flowing through the capacitor at the load of the inverter.

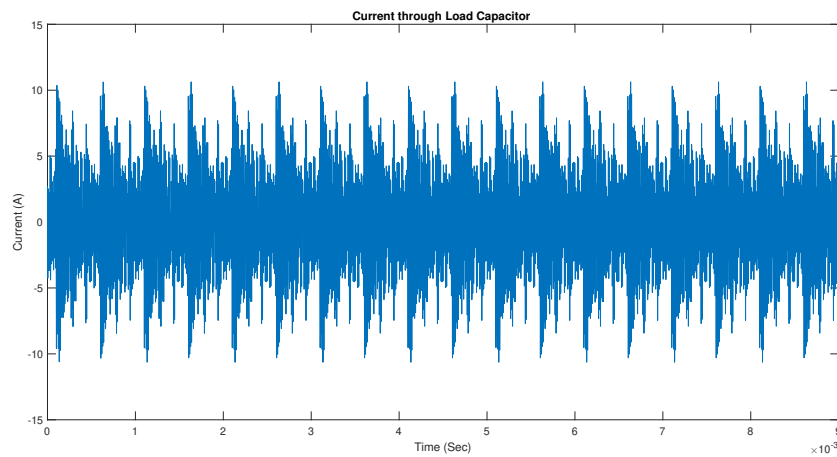
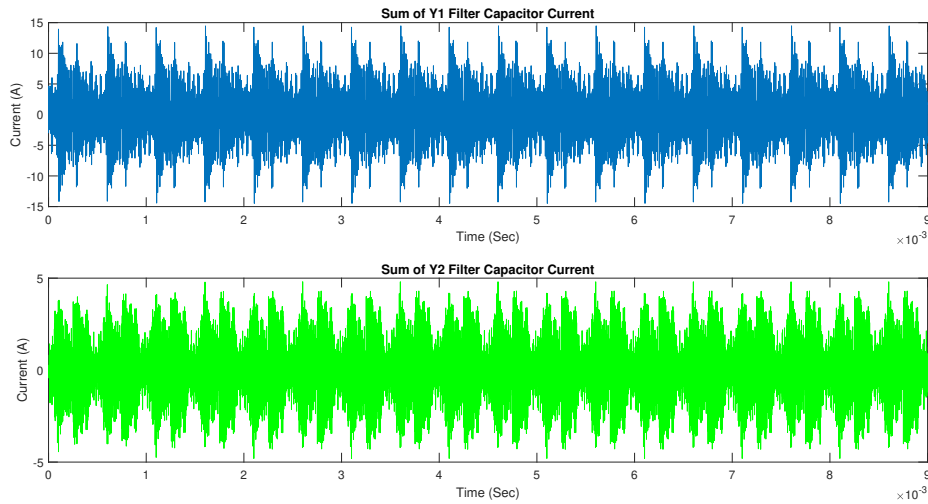


Figure 6.7: Load Capacitor Current



**Figure 6.8:** Filter Capacitor Currents

The fig 6.8 shows the currents flowing through the filter capacitors, the first plot of fig 6.8 shows the current flowing through the four capacitors in the input of the filter and the second plot of fig 6.8 shows the current flowing through the four capacitors in the output of the filter.

The fig 6.9 shows the CM current from the output load capacitor and is compared with the summation of current flowing through all the eight capacitors in the CLC filter.

It can be seen both the currents are equal and opposite in magnitude confirming the CM current flowing back to the circuit through the ground. From the fig 6.10 it is seen that the magnitude of CM current has reduced significantly after adding the filter.

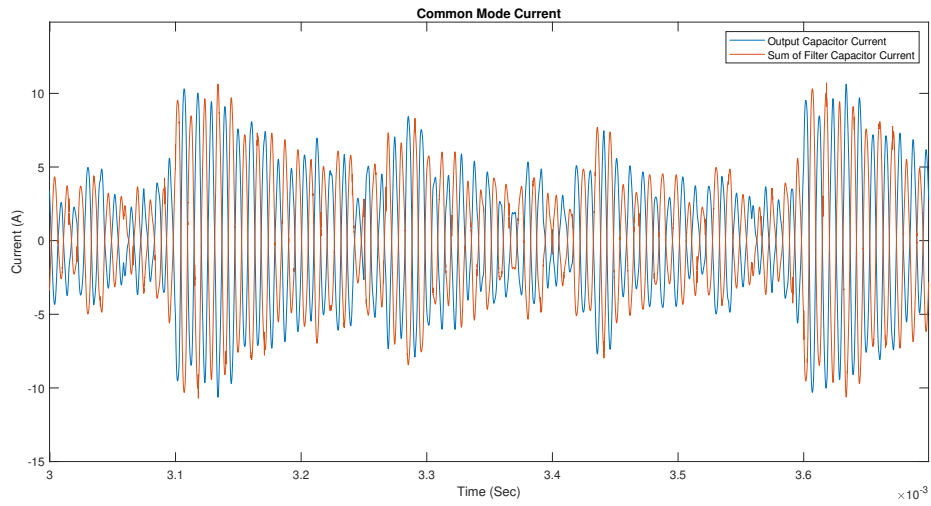


Figure 6.9: Common Mode Currents

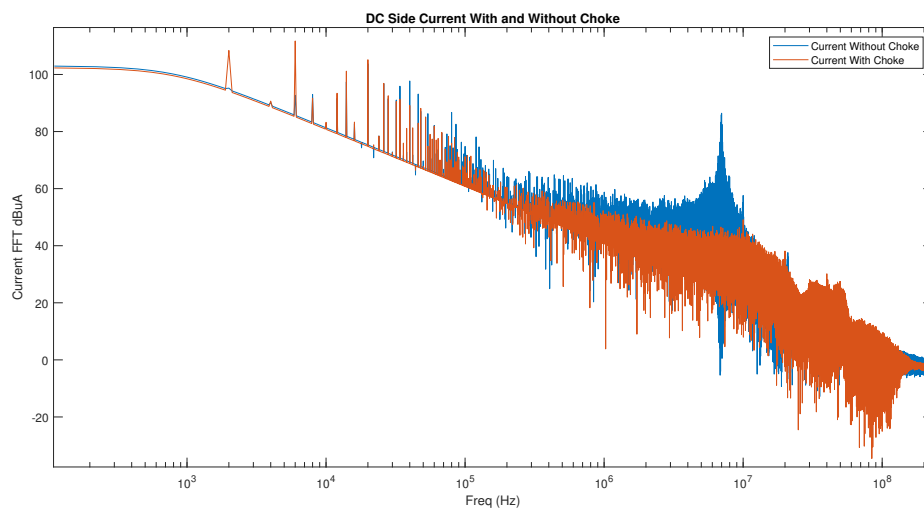


Figure 6.10: Common Mode Currents



# 7

## Simulation of a single switch

The simulation analysis of the switch and the inverter was done in software Ltspice.

### 7.1 Double Pulse Test

Double Pulse Test is used to evaluate the switching characteristics of a MOSFET during the transition time of turn-ON and turn-OFF. This double pulse test was performed in Ltspice. The figure ?? shows the circuit for a Double Pulse test of a single-power MOSFET used for the analysis. It consists of one n-channel power MOSFET driven by four driver MOSFET's, two n-channel and two p-channel.

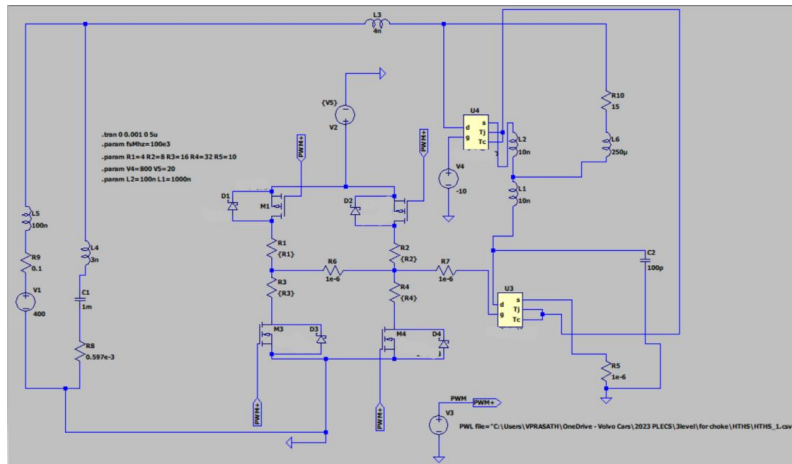
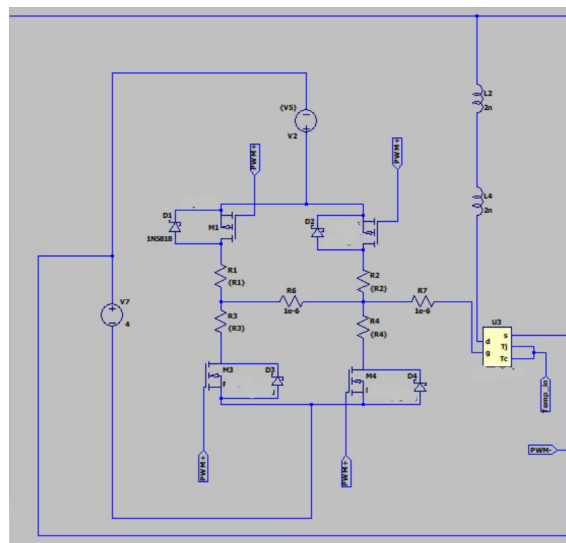


Figure 7.1: Schematic of Double Pulse Test

The drain of the power MOSFET is directly connected to a DC source of 800V and turn-ON and turn-OFF of the power MOSFET is controlled by the pulses provided to the two p-channel MOSFET(the top two MOSFET's) and the two n-channel MOSFET(the bottom two MOSFET's). The Gate Resistance R7 limits the peak current provided by the driver, and is responsible for an increase or decrease of MOSFET turn-on and turn-off times. The inductor L1 is responsible for fast turn-OFF of the drain-source voltage.

### 7.1.1 Modelling and Analysis

Fig 7.2 shows a connection of one switch of the inverter. The drain of the power MOSFET is connected to the positive port of the DC supply and the source is connected to the drain of immediate bottom power MOSFET. As the  $V_{gs}$  of the power MOSFET has to switch between +15V and -4V, the driver MOSFET's source of the p-channel is connected to a +20V DC supply, and the source of the n-channel is connected to a -4V DC supply. The negative 20V is connected to the positive 4V of the DC supply and to measure the potential between them the reference is connected with respect to the source of the power MOSFET.



**Figure 7.2:** One switch of the Inverter

Fig 7.3 shows the drain-source and gate-source voltage of the power MOSFET. The ringing in  $V_{gs}$  during turn-ON is due to the presence of parasitic elements such as inductors. These inductors are introduced in the circuit to represent the stray inductance. During turn-OFF there is spike in  $V_{ds}$ , that's because during that instance  $\frac{di}{dt} < 0$  across the parasitic inductance.

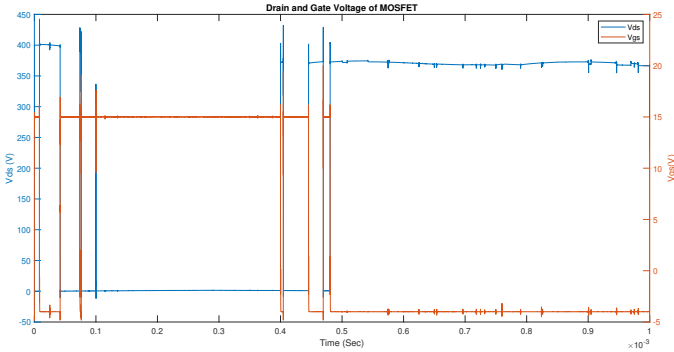


Figure 7.3:  $V_{ds}$  and  $V_{gs}$  of one Switch



# 8

## Analysis of inverters

After completing the modeling and simulation, we processed our data on Matlab and did comparisons as mentioned below.

### Output Voltage

#### Effect of Modulation Index on the Voltage

##### Three Level Inverter (MLI)

- $ma = 1$ , Load = 5 Ohms
- $ma = 0.4$ , Load = 5 Ohms

##### Two Level Inverter

- $ma = 1$ , Load = 5 Ohms
- $ma = 0.4$ , Load = 5 Ohms

#### Effect of Load on the Voltage

##### Three Level Inverter

- High Torque,  $ma = 1$
- Low Torque,  $ma = 1$

##### Two Level Inverter

- High Torque,  $ma = 1$
- Low Torque,  $ma = 1$

#### Effect of Type of Inverter on Voltage

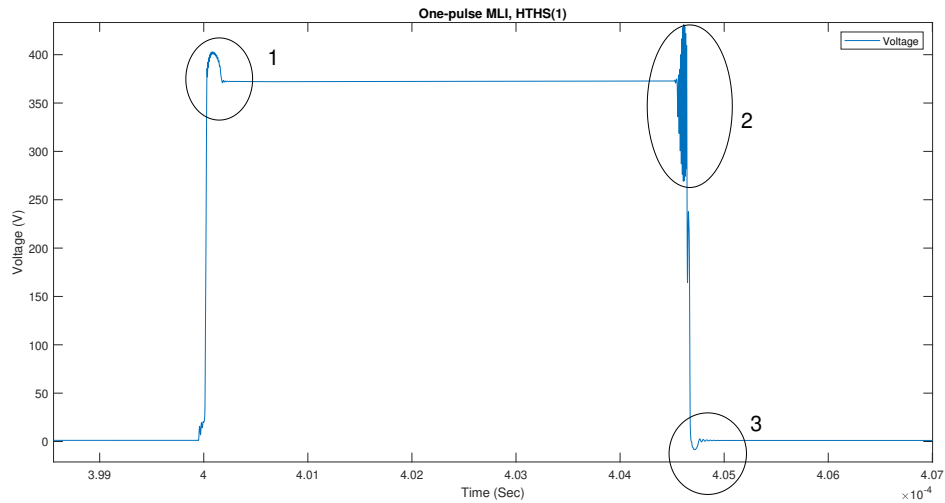
- Three Level Inverter, Load = 5 Ohms
- Two Level Inverter,  $ma = 1$ , Load = 5 Ohms

## 8.1 FFT comparison

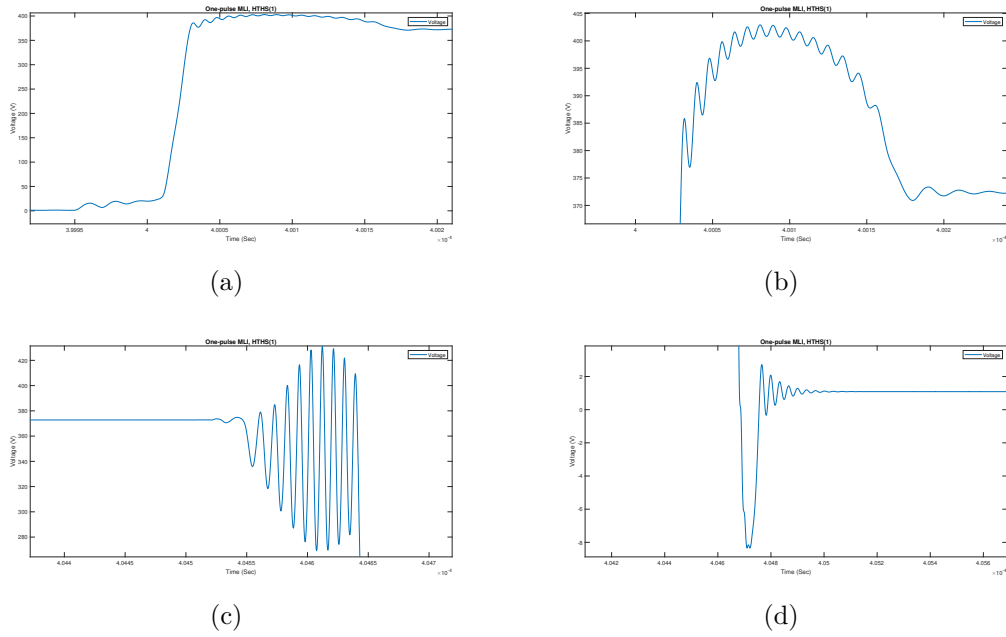
In this section, a single pulse of Voltage at Load =5 Ohms and a  $\mu = 1$ , is analyzed . The time domain graph and its various transients are compared with its Frequency domain plot.

In ,8.1, it can be seen that , there are three significant areas marked by 1, 2 and 3 where ringing can be seen. Figure 8.2, shows the zoomed area where ringing happens as well as the rise time.

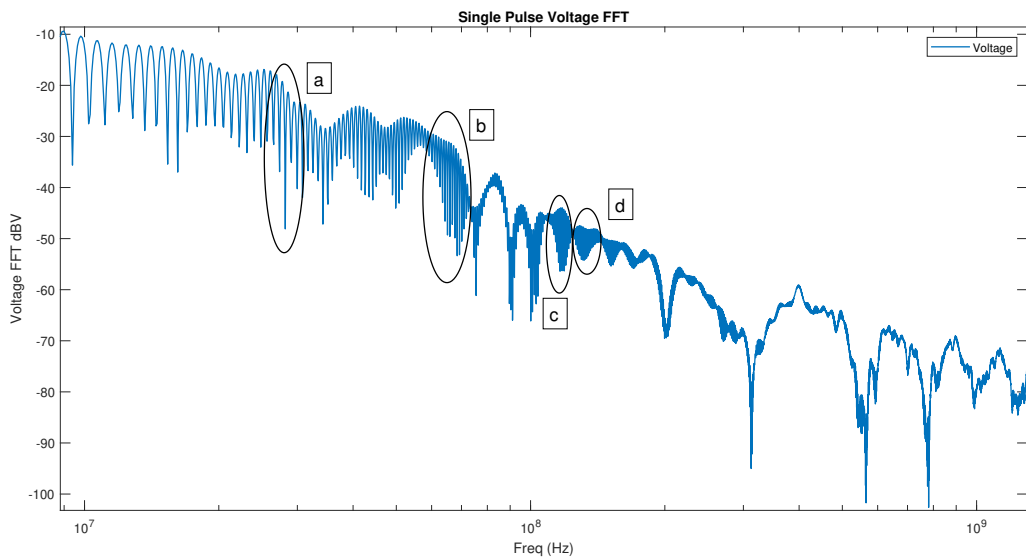
Next, the FFT analysis of the plot is done and the frequencies corresponding to the time domain plots mentioned are marked by circles in 8.3



**Figure 8.1:** Single Voltage Pulse Time Domain [ $m_a = 1, \text{HTHS}$ ]



**Figure 8.2:** (a) Rise Time (b) Ringing when pulse rises (c) Ringing when pulse begins to fall (d) Ringing when pulse falls



**Figure 8.3:** Single Voltage Pulse FFT [ $m_a = 1$ ]

## 8.2 Effect of modulation index

Here the effect of the modulation index on the output voltage and common mode current is observed, both in the time domain and the frequency domain for the three-level and two-level inverters.

### Three Level Inverter

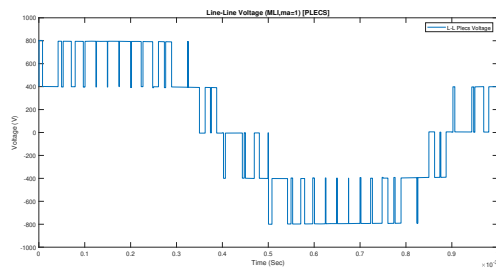


Figure 8.4: L-L Plecs Voltage MLI $[m_a = 1]$

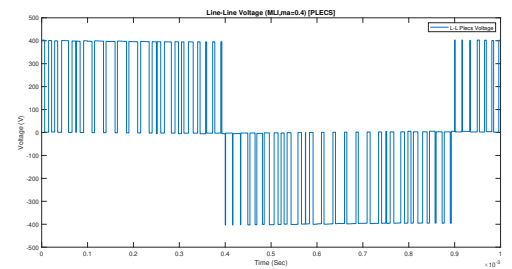


Figure 8.5: L-L Plecs Voltage MLI $[m_a = 0.4]$

Figures 8.4 and 8.5 depict the Line to Line voltage of the Three Level Inverter. The three level inverter shows higher voltage amplitudes, and with multiple levels, whereas for lower modulation, due to under modulation a lower voltage with lesser levels can be seen. This leads to lower utilization of the DC bus voltage, resulting in less efficient use of the available power supply.

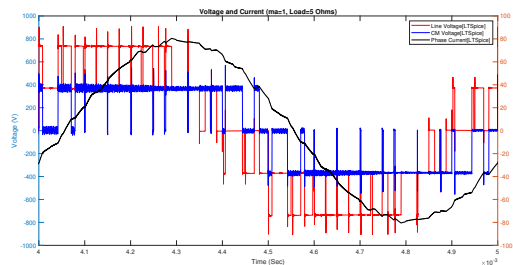


Figure 8.6: Phase Current, CM Voltage and L-L voltage MLI  $[m_a=1, \text{Load}=5\Omega]$

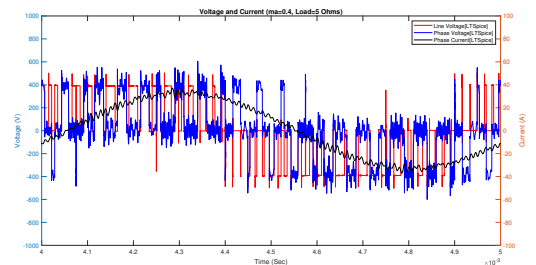
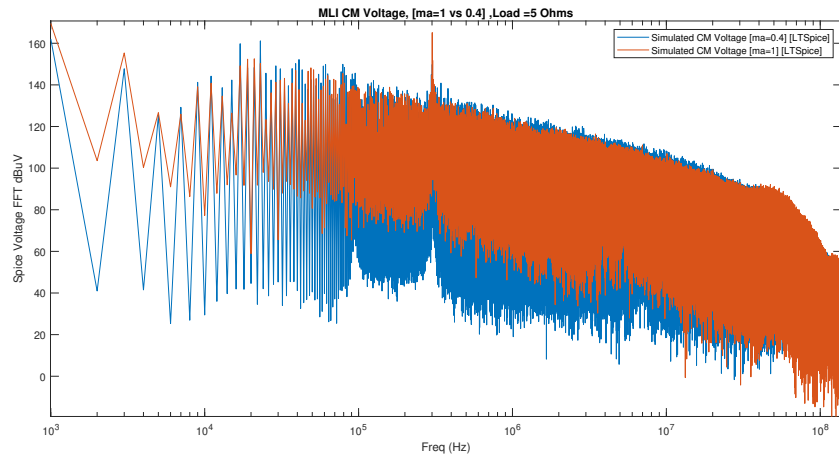


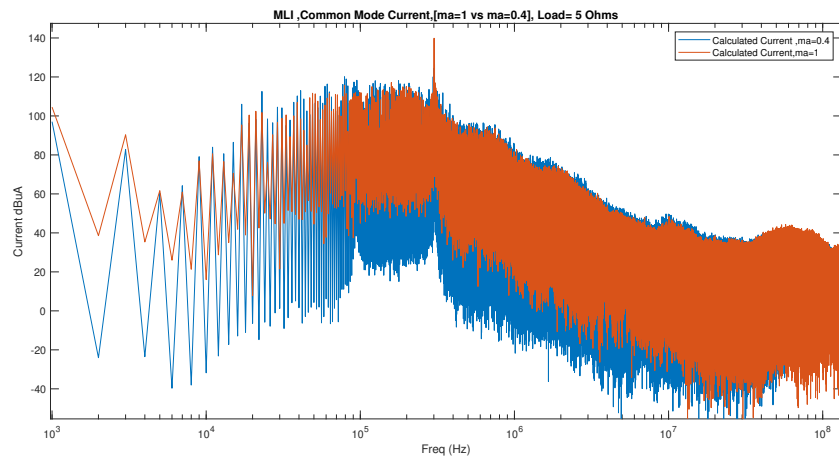
Figure 8.7: Phase Current, CM Voltage and L-L voltage MLI  $[m_a=0.4, \text{Load}=5\Omega]$

First, the time domain analysis was done, Figure 8.6 shows the line and common mode voltage and phase current for modulation index 1 while figure 8.7 shows the same for modulation index 0.4.

It can be seen that, at a higher modulation index, the switching is not so frequent and we obtain much thicker pulses, i.e. pulses which are on or off for a long time. This leads to higher output voltage. Also, it can be seen that the voltage has three levels. For higher modulation, the 3 voltage has levels and for lower modulation index it has 2. The current at higher modulation index 1 is around two times higher than at 0.4.



**Figure 8.8:** MLI, CM Voltage [ $m_a=1$  vs  $m_a=0.4$ ], Load=  $5\Omega$



**Figure 8.9:** MLI CM Current [ $m_a=1$  vs  $m_a=0.4$ ], Load=  $5\Omega$

## 8. Analysis of inverters

The graphs depict the comparison of the Voltage of a 3-level inverter in the frequency domain at modulation index 1 and 0.4. It was seen that the voltage FFT of the two voltages were almost similar in magnitude and had variations due to simulations. It is evident that since the lower limit of the waveform with modulation index 1 is higher than that of 0.4, the RF emissions at  $m_a=1$  is higher than  $m_a=0.4$ . This also shows the time dependency of the FFT and that there are many iterations in a single pulse.

At lower [10K Hz - 100 KHz] frequencies each voltage peak corresponds to the fundamental frequencies and after that, the voltage peaks correspond to the switching frequencies. 8.9 shows the common mode current, which was calculated from the CM Voltage and the Z11, of the Impedance frequency graph. Similar to 8.8, it looks unstable, and the current at  $m_a = 1$  seems to produce somewhat more emissions than at  $m_a = 0.4$ .

### Two Level Inverter:

Similar to the three-level inverter in the two level the same sequence was followed. 8.12 and 8.13 shows the voltage and current in time domain with modulation index 1 and 0.4 respectively. Here, only two voltage levels can be seen and the higher modulation index had greater magnitude of current.

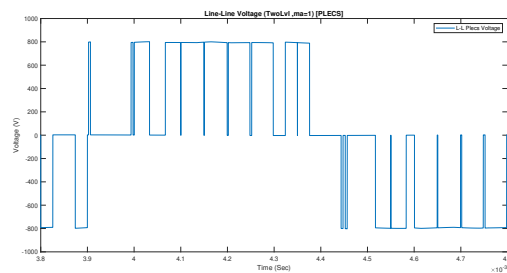


Figure 8.10: L-L Plecs Voltage 2-Lvl [ $m_a = 1$ ]

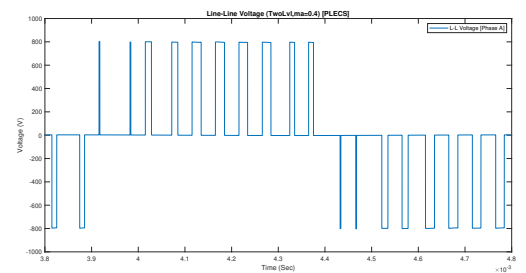


Figure 8.11: L-L Plecs Voltage 2-Lvl [ $m_a = 0.4$ ]

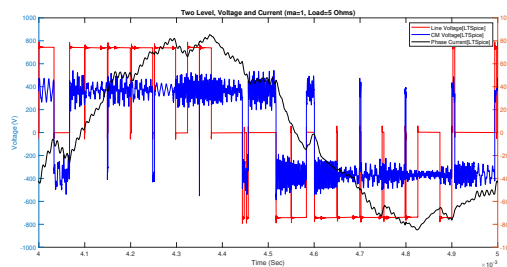


Figure 8.12: Phase Current, CM Voltage and L-L voltage 2-Lvl [ $m_a=1$ ], Load=5 $\Omega$

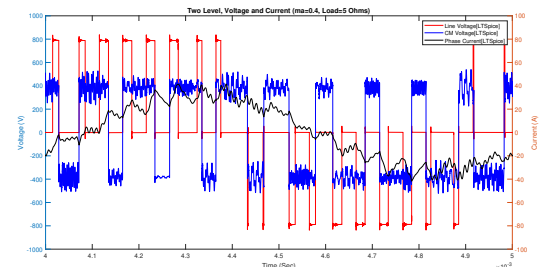


Figure 8.13: Phase Current, CM Voltage and L-L voltage 2-Lvl [ $m_a=0.4$ ], Load=5 $\Omega$

Figure 8.14 and 8.15 show the common mode voltage and the current. Similar to three level, in two level also there is high variations due to simulation, while the voltages and current at both the modulation index looks similar, emissions at  $m_a=1$  look more while instability in  $m_a=0.4$  looks more.

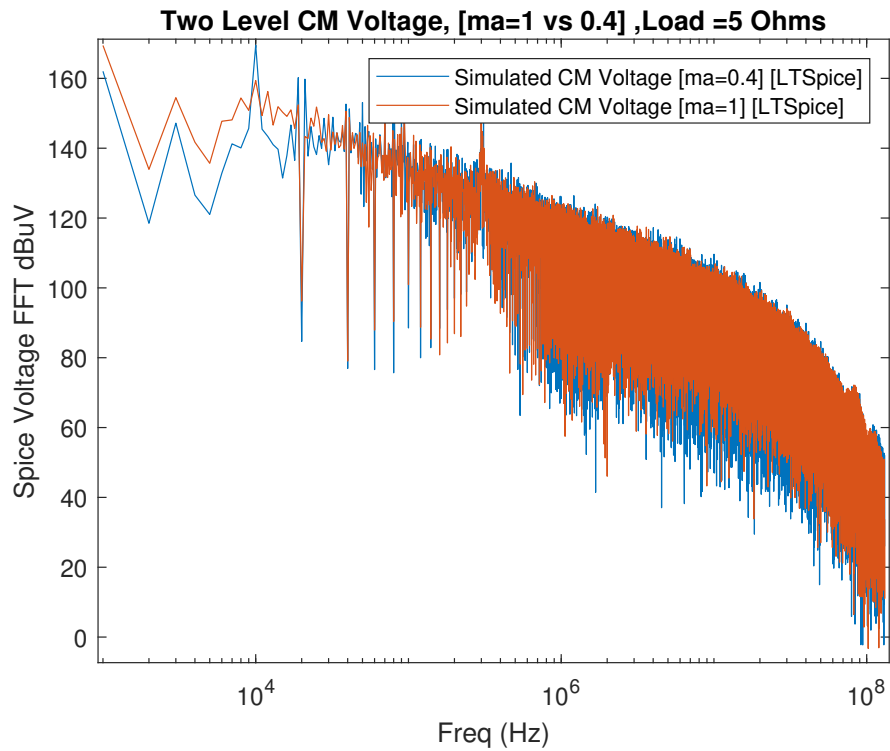


Figure 8.14: 2-Lvl Voltage [ $m_a=1$  vs  $m_a=0.4$ ], Load= $5\Omega$

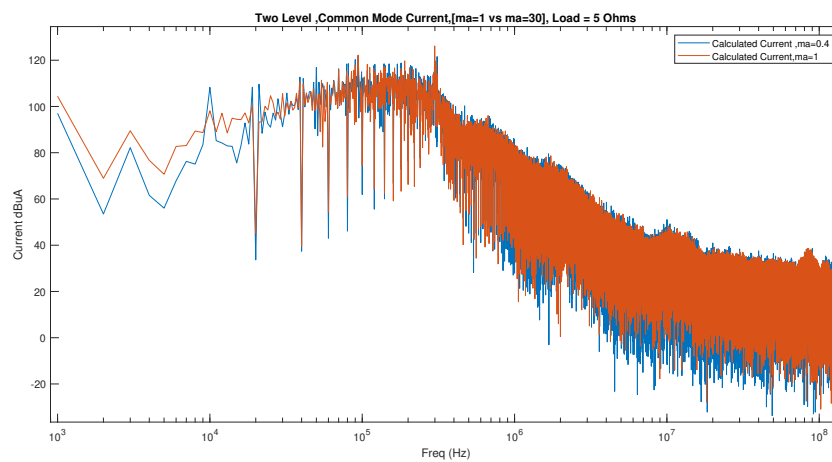


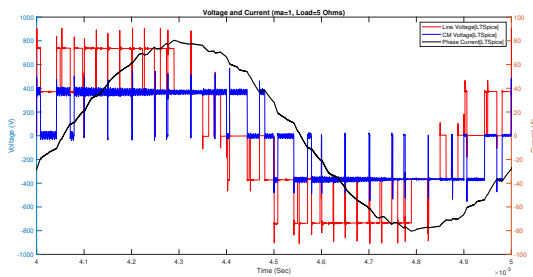
Figure 8.15: 2-Lvl Common Mode Current [ $m_a=1$  vs  $m_a=0.4$ ], Load= $5\Omega$

### 8.3 Effect of load conditions

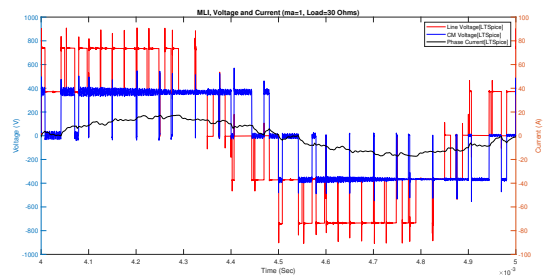
In this, the load resistance has been increased from  $5\ \Omega$  and  $30\ \Omega$  to analyze the effect of load on the inverter current emissions in the two inverters respectively.

#### Three Level Inverter

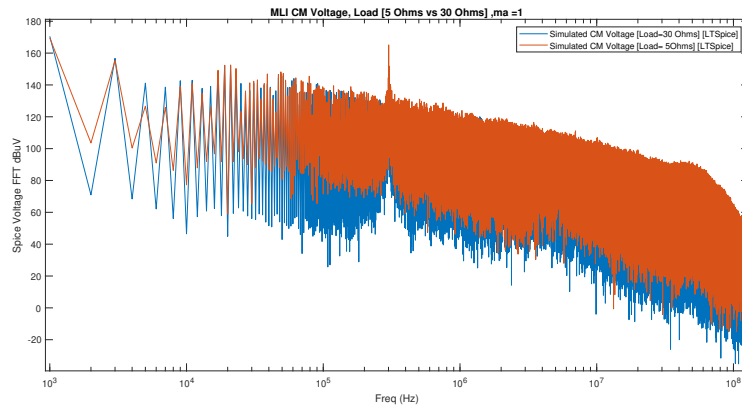
The figures 8.16 and 8.17 below depict the time domain graph of line and CM voltage and Phase current of the three-level inverter with different loads [ $5\ \Omega$  and  $30\ \Omega$ ] at  $m_a=1$ . It can be seen that low resistance the current at Load  $5\ \Omega$  is much higher than at  $30\ \Omega$ , while the voltage remains the same, as it was expected.



**Figure 8.16:** Phase Current, CM Voltage and L-L voltage MLI [ $m_a=1, Load=5\ \Omega$ ]



**Figure 8.17:** Phase Current, CM Voltage and L-L voltage MLI [ $m_a=1, Load= 30\ \Omega$ ]



**Figure 8.18:** MLI Load [ $5\ \Omega$  vs  $30\ \Omega$  ],  $m_a=1$

Figures, 8.18, 8.19, depicts the comparison of common mode voltage and common mode current in the frequency domain at different load conditions [ $5\ \Omega$  and  $30\ \Omega$ ]. It can be seen that at higher loads there seems to be more energy [Noise] than at lower loads.

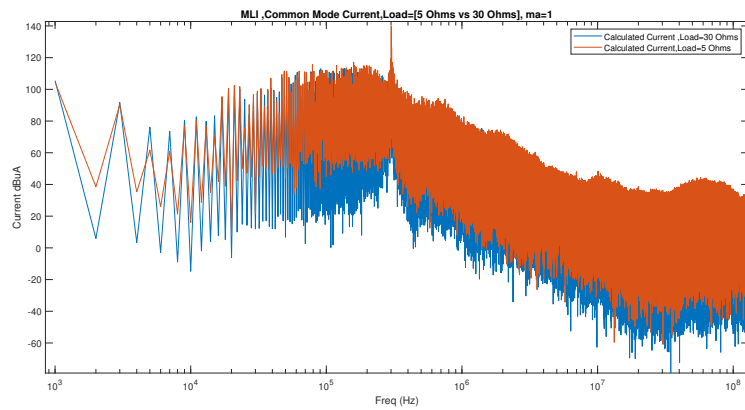


Figure 8.19: MLI, CM Current, Load [ $5\Omega$  vs  $30\Omega$  ],  $m_a=1$

### Two Level Inverter

The figures 8.20 and 8.21 below depicts the time domain graph of line and CM voltage and Phase current of the two-level inverter with different loads [ $5\Omega$  and  $30\Omega$ ] at  $m_a=1$ . It can be seen that low resistance the current at Load  $5\Omega$  is much higher than at  $30\Omega$ , while the voltage remains the same.

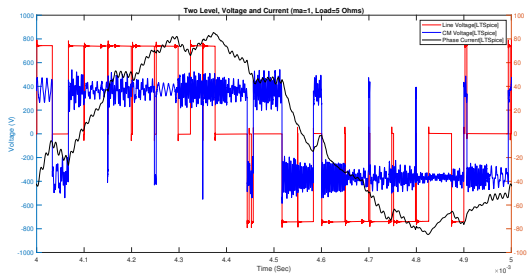


Figure 8.20: Phase Current, CM Voltage and L-L voltage Two Lvl [ $m_a=1$ , Load= $5\Omega$ ]

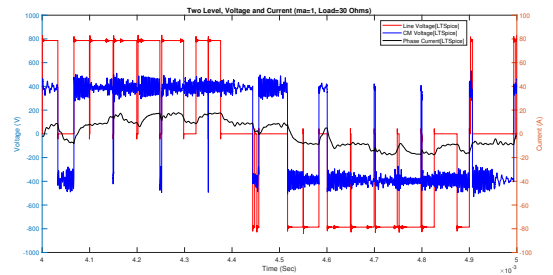


Figure 8.21: Phase Current, CM Voltage and L-L voltage Two Lvl [ $m_a=1$ , Load= $30\Omega$ ]

Figures, 8.22, 8.23, depict the comparison of common mode voltage and current in the frequency domain at different load conditions [ $5\Omega$  and  $30\Omega$ ]. It can be seen that at higher load there seems to be more energy [Noise] than at lower loads as seen in the three level inverter.

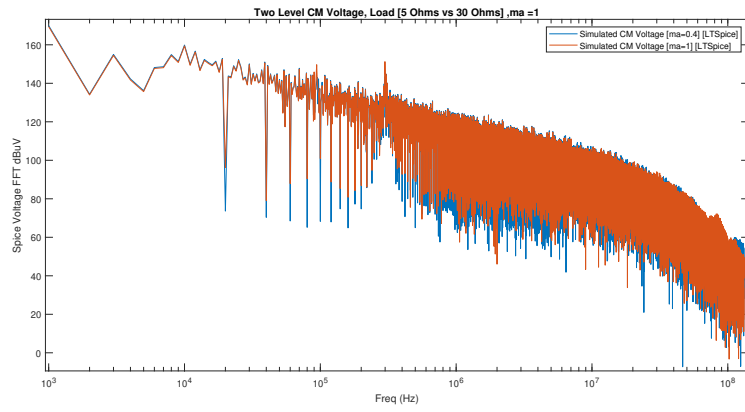


Figure 8.22: 2-Lvl CM-Voltage,  $[m_a = 1]$  Load:  $(5\Omega$  vs  $30\Omega)$

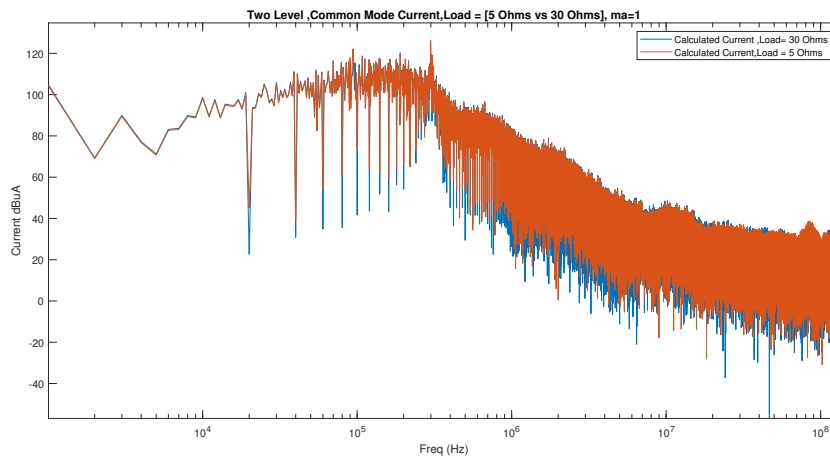


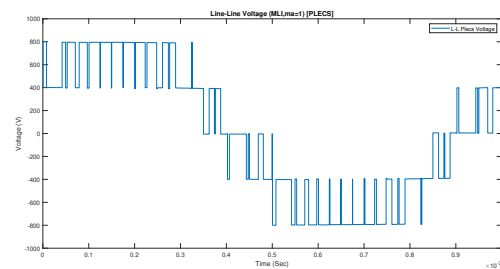
Figure 8.23: 2lvl CM Current,  $[m_a = 1]$  Load:  $(5\Omega$  vs  $30\Omega)$

## 8.4 2 level vs 3 level

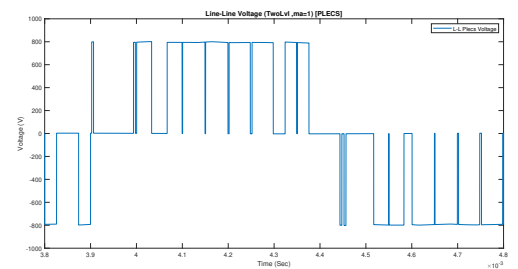
This section compared and analyzed the outputs of the three-level and the two-level inverter.

**MLI vs 2 Lvl [ $m_a=1$ , Load =5 Ohms]**

Figures , 8.24 and 8.25, shows the line-to-line voltage of MLI and 2Lvl Inverters.

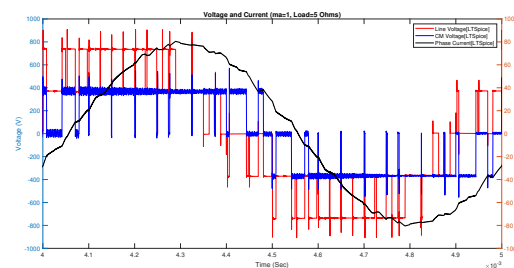


**Figure 8.24:** L-L Plecs Voltage,MLI [ $m_a = 1$ ]

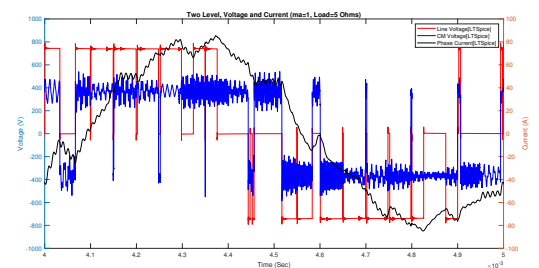


**Figure 8.25:** L-L Plecs Voltage,2-Lvl [ $m_a = 1$ ]

Next , figures and 8.26 and 8.27, depict the line and CM voltage and the phase currents of the three-level and the two-level inverters. It can be seen that in three level the sin waveform is much smoother than in the case of the two level.This is due to the fact that due to three levels of voltages , the current estimation is more accurate in MLI than in Two Level.



**Figure 8.26:** Phase Current, CM Voltage and L-L voltage MLI [ $m_a=1$ ,Load=5 $\Omega$ ]



**Figure 8.27:** Phase Current, CM Voltage and L-L voltage 2-Lvl [ $m_a=1$ ,Load=5 $\Omega$ ]

Then finally in figures 8.28 and 8.29 , it is proved that the emissions created by the two level inverter is greater than the three-level inverter.

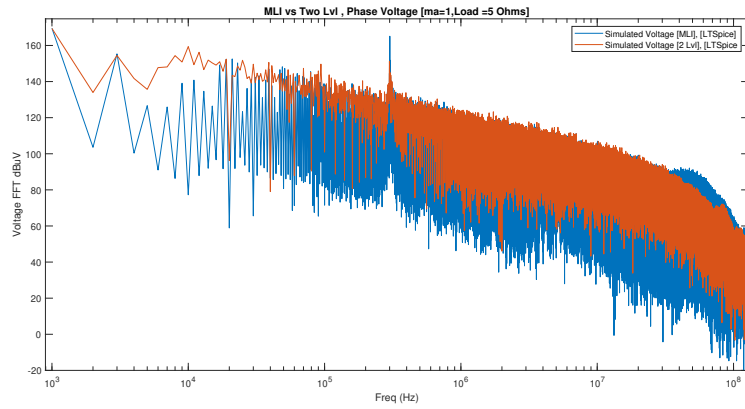


Figure 8.28: CM Voltage [MLI vs 2Lvl] , [ $m_a=1$ , Load= $5\Omega$ ]

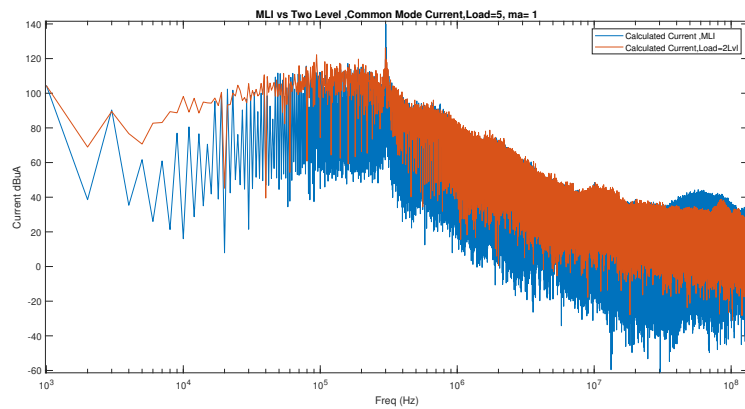


Figure 8.29: CM Current [MLI vs 2Lvl] , [ $m_a=1$ , Load= $5\Omega$ ]

# 9

## Conclusion

Two-level and three-level NPC inverter and modulator is designed and simulated in PLECS under ideal conditions to extract the SVPWM pulses, to be fed to the switches in Ltspice model. The same model of the two-level and three-level NPC inverter coupled to the RL load with some parasitic components is designed and simulated in Ltspice.

Common mode current is the undesirable current flowing in an electric system. The CM voltage from the inverter model in Ltspice and the impedance value from the S-parameter were used in the following formula to identify the amount of CM current flowing in the circuit. Where I-CM current, V-CM voltage and Z-impedance.

$$I = \frac{V}{Z} \quad (9.1)$$

The voltage is analysed in both time and frequency domain for different modulation index and load conditions to identify the cause of the noise in frequency domain.

Similarly the CM current was compared between the two inverters in frequency domain to analyse the EMI emission and the current magnitude at each frequency. The CM current analysis was also done at different modulation index and at different load conditions.

In conclusion, analysing these common current and the voltages gives us idea of moving from two level to a three level NPC inverter in electric vehicles. It also enables us to see the amount of EMI emissions from the inverter at different load conditions and design the inverter to operate at a higher performance with better a efficiency.



# 10

## Future Work

Future work for this thesis comes down to four major aspects. First analyzing the effect emission for different modulation indices and for different load conditions. In this thesis work the effect of emission was done only for two different modulation index ( $m_a = 0.4$  and  $m_a = 1$ ) and two different load conditions ( $5\Omega$  and  $30\Omega$ ). Analyzing the modulation index from 0.1 to 1 would give an more in depth analysis in studying the change in emission from one modulation index to another.

Second, tuning the common mode filter at the input of the inverter. In this thesis work the parameter values for the components have been chosen through some reference work. Setting up the correct parameter values for the choke would give a more accurate filtering of the high frequencies.

Third, modelling of the machine. This thesis uses a RL load for the inverter. For the future work modelling a machine with appropriate parasitic values to couple with the inverter would produce an even accurate measurements of the currents flowing through it.

Fourth, analysing the effect of slew rate  $\frac{dv}{dt}$  on FFT. Slew rate of a signal determines it's high frequency components, so faster the slew rate higher the harmonics content. Due to this it is important to analyse the slew rate for high frequency application.



# 11

## Impact on Industries

### 11.1 Understanding and Mitigating EMI

Common mode currents are a major source of electromagnetic interference (EMI).

- Determine which inverter design generates less EMI, leading to fewer issues with interference in vehicle electronics and communications systems.
- Optimize inverter designs to minimize CMC

### 11.2 Enhancing Efficiency

Three-level inverters typically offer better efficiency and lower switching losses compared to two-level inverters. The analysis can help:

- **Select Components:** Guide the selection of inverter technology that optimizes efficiency and performance
- **Thermal Management:** Reduce heat generation due to lower switching losses

### 11.3 Improving Power Quality

Inverter design affects the quality of power delivered to the motor.

- **Reducing Harmonics:** A three-level inverter generally produces lower harmonic distortion, improving the power quality and reducing motor heating and losses.
- **Smoother Operation:** More the voltage levels increased, the better the probability of results.

### 11.4 Cost-Benefit Analysis

The comparison provides data for a cost-benefit analysis between the two inverter types:

- **Initial Cost vs. Lifetime Cost:** Help in understanding the trade-offs between higher initial costs of three-level inverters versus potential savings in operational efficiency and maintenance.
- **Component Lifetime:** Braring Lifetime increase and there can be less number of filters on the driveshaft.

## 11.5 Regulatory Compliance

Understanding CMC and its implications on EMI can help in:

- **Meeting Standards:** Ensure the EVs meet stringent EMC regulations, avoiding potential recalls or compliance issues.
- **Future Proofing:** Stay ahead of evolving regulatory requirements by adopting advanced inverter designs that minimize EMC-related risks.

# Bibliography

- [1] S. Satpathy, S. Bhattacharya and V. Veliadis, *Comprehensive Loss Analysis of Two-level and Three-Level Inverter for Electric Vehicle Using Drive Cycle Models*, 2020.
- [2] EVreporter. *EV - Powertrain Components - Basics*. <https://evreporter.com/ev-powertrain-components/>, 2024.
- [3] Choudhury, Abhijit and Pragasen Pillay. *A DC-Link Voltage Balancing Algorithm for Three-Level Neutral Point Clamped (NPC) Traction Inverter Drive in Field Weakening Region*, 2015.
- [4] Tawfiq, K.B.; Güleç, M.; Sergeant, P. Bearing Current and Shaft Voltage in Electrical Machines: A Comprehensive Research Review, 2023.
- [5] Khaled, Usama & Hussein Farh, Hassan M. & Alissa, Salman & Abanmi, Abdulrhman & Aldrainli, Omar. *Efficient Solution of the DC-link Hard Switching Inverter of the PV System*, 2018.
- [6] BYJUS. *Pulse Width Modulation - Definition, Terminologies, Types, Applications*. <https://byjus.com/physics/pulse-width-modulation/>, 2022.
- [7] Sang-Hoon Kim, *Chapter 7 - Pulse width modulation inverters*, Editor(s): Sang-Hoon Kim, Electric Motor Control, Elsevier, 2017.
- [8] Ranaweera, Narmada & Donato, Giulio. *Development and Experimental Testing of a Speed Controlled PMSM Drive Using PSIM Visual Programming Environment*, 2019.
- [9] Diyoke, Gerald & Onwuka, Ifeanyichukwu & Okoye, O. *Design And Simulation of Three-Phase Diode Clamped And Improved Inverter Fed Asynchronous Motor Drive With Three-Level Configurations*, 2015.

- [10] Madasamy, P.; Pongiannan, R.K.; Ravichandran, S.; Padmanaban, S.; Chokkalingam, B.; Hossain, E.; Adedayo, Y. *A Simple Multilevel Space Vector Modulation Technique and MATLAB System Generator Built FPGA Implementation for Three-Level Neutral-Point Clamped Inverter*, 2019.
- [11] Ali, Irfan & Sharma, Virendra & Kumar, Prabhat. *A Comparison of Different Control Techniques for Active Power Filter for Harmonic Elimination and Enhancement of Power Quality*, 2018.
- [12] M. Sajitha and R. Ramchand, *Space Vector PWM Scheme for Three Phase Three Level T-type NPC Inverter*, 2019.
- [13] I. Pereira and A. Martins, *Multicarrier and space vector modulation for three-phase NPC converters: A comparative analysis*, 2009.
- [14] Guolei, X., Yan, S., Juwei, Y., Chengcong, L., Binfeng, W., Feng, J., & Weidong, J. *Research on the principle of residual current protection technology based on transient waveform criterion*, 2020.
- [15] File:Rogowskis coil.png - Wikimedia Commons.  
[https://commons.wikimedia.org/wiki/File:Rogowskis\\_coil.png](https://commons.wikimedia.org/wiki/File:Rogowskis_coil.png), 2006.
- [16] V. Rajamani, J. C. West and C. F. Bunting, *Measurement and Simulation of the Induced Current on a Wire Using S-Parameter Method*, 2014.
- [17] Zedníček, T. *What Filter S-Parameters Are Good For. Passive Components Blog*. <https://passive-components.eu/what-are-filter-s-parameters/>, 2023.
- [18] Maeda, Noboru et al. *An estimation method for the 3 port S-parameters with 1 port measurements*, 2013.
- [19] C. R. Paul, *A comparison of the contributions of common-mode and differential-mode currents in radiated emissions*, 1989.
- [20] Tawfiq, K.B.; Güleç, M.; Sergeant, P. *Bearing Current and Shaft Voltage in Electrical Machines: A Comprehensive Research Review*, 2023.
- [21] S. S. Ahmad and G. Narayanan, *Double pulse test based switching characterization of SiC MOSFET*, 2017.
- [22] Pereira, I. & Martins, Antonio. *Multicarrier and space vector modulation for three-phase NPC converters: A comparative analysis*, 2009.

DEPARTMENT OF ELECTRICAL ENGINEERING  
CHALMERS UNIVERSITY OF TECHNOLOGY  
Gothenburg, Sweden  
[www.chalmers.se](http://www.chalmers.se)



**CHALMERS**  
UNIVERSITY OF TECHNOLOGY