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EMI Reduction Using Symmetrical Switching in an Application with an Unshielded Wire between the Power Electronic Converter and the Load

Master of Science Thesis

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Abstract

An EMI reduction technique using two MOSFETs instead of a single MOSFET in a Buck converter has been investigated in this thesis. A circuit that implements this technique was designed, constructed on a surface-mounted technology printed circuit board and tested.

The designed circuit is made up of an IRF 7307 consisting of a p-channel and an n-channel MOSFETs; plus the input circuit for the MOSFETs and a “error-handling” circuit containing a p-regulator responsible for approximating the turn-on and turn-off times of the p-channel MOSFET and n-channel MOSFET, and also correct the effect of differences in the threshold voltages between the two MOSFETs.

The analyses of simulations and measurements results show that the symmetrical switching (or double MOSFET switching) technique may successfully be applied to reduce the RF emission in the low frequency and medium frequency range when compared to the single MOSFET switching.

Keywords: double MOSFET, EMI, EMC, FFT.

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List of Abbreviations

BJT	Bipolar Junction Transistor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FFT	Fast Fourier Transform
MOSFET	Metal Oxide Semiconductor Field Effect Transistors
N-MOS	n-channel MOSFET
P-MOS	p-channel MOSFET
PCB	Printed Circuit Board
RF	Radio Frequency
SPICE	Simulation Program with Integrated Circuit Emphasis

Introduction

Following the increased number of power electronic objects in many applications, such as houses, vehicles, etc, the concern for electromagnetic interference (EMI) is increasing. If an electrical equipment is an unintended source of interference in the RF range, there is a substantial risk that it will interfere with other equipment such as radio receivers.

One particular situation of an unintended RF interference source is a single switch Buck converter located distant from the load. In this situation, the wires between the converter and the load act as an antenna radiating electromagnetic waves due to the variation of the electric filed. One way to reduce the emission in this case is to transform the switching signal into two signals that are symmetrical to each other and cancel out the antenna effect by eliminating the variations in the electric field. This could be accomplished by utilizing two MOSFET instead of one in the Buck converter, in a configuration called Double MOSFET Switching (or Symmetrical Switching).

A previous thesis work [6] has been done in order to implement and verify the symmetrical Switching principle. The aim of this thesis is to design a circuit and construct a printed circuit board that implement the symmetrical switching technique and that operates with higher switching frequencies and with shorter turn-on/turn-off times, when compared to the previous work. Also investigations if the circuit is really able to reduce the RF emissions when compared to a single switch Buck converter are intended.

The first part of this thesis is an introduction to EMC, EMI and other concepts that lead to a better comprehension of the problem and the existing solutions. The following part will in detail explain the symmetrical switching idea and how to implement it. Further on, the design of each part of the circuit will be described in detail. The implementation of the designed circuit in a PCB will be briefly explained and the most important SPICE simulations and measurements, as well as the comparison between them, will be exposed in the section about the results. Finally, the comparison between the double MOSFET switching and single MOSFET switching regarding the reduction of emissions will be done and the final conclusions will be draw.

1 EMI / EMC Fundamentals

Designing electronic systems means producing system and circuit boards that not only work at the development department and in the testing laboratory, but also work in their application environment. This could be an industrial environment, a medical environment, a vehicle, etc.

To guarantee a problem-free operation of the designed system in its application environment and satisfied customers, the manufacturer must take into account a very important issue: the electromagnetic compatibility (EMC).

In order to understand the meaning of EMC, it is necessary to introduce the concept of electromagnetic interference (EMI). EMI is any electromagnetic disturbance (a noise, an unwanted signal, or a change in the propagation medium itself), that degrades or limits the effective performance of electronic or electrical equipment [1]. Although the meanings of disturbance and EMI are considered different by many authors, in this report, as is common in practice, the terms disturbance, interference and EMI are used interchangeably.

EMC is defined according to [1] as: (1) The capability of electrical and electronic systems, equipments, and devices to operate in their intended electromagnetic environment within a defined margin of safety, and at design levels of performance without suffering or causing unacceptable degradation as a result of electromagnetic interference. (NATO) (2) The ability of a device, equipment, or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment. (IEEE Std 100-1996)

The manufacturer must therefore produce a system that:

1. is not susceptible to interference from other systems,

2. is not susceptible to interference from itself, and

3. is not a source of interference to other systems,

The limits of electromagnetic emissions that characterize EMI for each kind of equipment and system can be determined in standards, regulation or in special agreement between the manufacturer and the purchaser. Even though the equipment or system is designed according to standards, regulations and agreements, this does not guarantee that it will not be susceptible to or interfere with some current or future equipment.

1.1 Characterization of EMI

The EMI can be classified, according to [2], by its source, frequency content and transmission mode. It is not unusual to classify them also in terms of energy content, waveform, etc, but the most important characterizations are the ones exposed below.

1.1.1 Source

Sources of EMI can be divided into natural and manmade [9]. The natural sources of disturbances exist at much lower level than the manmade. Two existing natural sources are the electrical discharges occurring during thunderstorms that produce atmospheric noise and planets, stars that produce cosmic noise.

Some typical manmade sources of electromagnetic emissions are transmitters, pulse generators, oscillators, digital logic circuits, switching power supplies and converters, relays, motors, and line drivers. One can conclude that all manmade systems that involve quick voltage and current transitions are potential sources of EMI.

1.1.2 Frequency content

The frequency spectrum of all electromagnetic waves is commonly divided as illustrated in Figure 1 [8]. The radio frequency band, which is the disturbance band of interest in this thesis is highlighted in Figure 1 and detailed bellow.

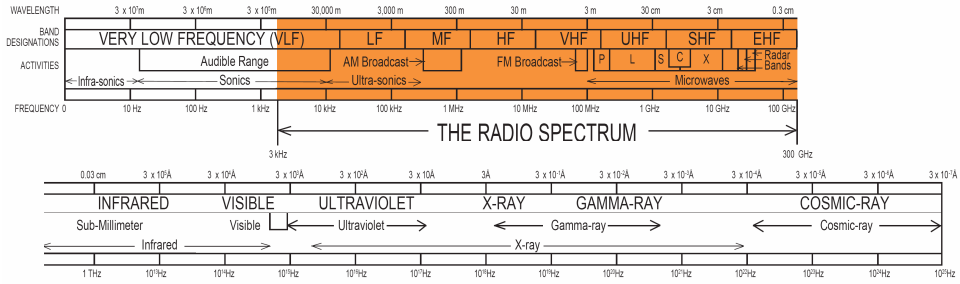

Figure 1: Frequency spectrum of electromagnetic waves [8]

Where:

- LF – low frequency – f < 300 kHz
- MF – medium frequency – 300 kHz < f < 3 MHz
- HF – high frequency – 3 MHz < f < 30 MHz
- VHF – very high frequency – 30 MHz < f < 300 MHz
- UHF– ultra high frequency – 300 MHz < f < 3 GHz
- SHF – super high frequency – 3 GHz < f < 30 GHz
- EHF – extra high frequency – 30 GHz < f < 300 GHz

1.1.3 Transmission mode

Electromagnetic disturbances travel by conduction on wiring and by radiation in space. Disturbances below approximately 10MHz spread primarily by conduction; at higher frequencies, radiation becomes dominant. For radiated emissions, if the victim and source are about a wavelength or more apart, the interference is referred to as far-field or just radiated interference. If the victim and source are electrically close, the interference is referred to as near-field interference or crosstalk. More specifically, there are four ways that the disturbances can be passed from the source to the victim [3].

1. Via conductive and common impedance coupling (i.e., shared conductor)

2. via near-field electric coupling (i.e., capacitance coupling)

3. via near-field magnetic field coupling (i.e., mutual inductance)

4. via far-field coupling (i.e., radiation)

The disturbances enter the victim receiver through the front door or the back door. Access through the front door means that the disturbances enter through the receiver's input terminal used by the desired signal, while access through the back door means that the disturbances enter through any other path, such as being conducted into primary power lines inputs, induced into interconnecting signal and control cables, and radiated directly through equipment case. Figure 2 illustrates the means of entry by disturbances [10].

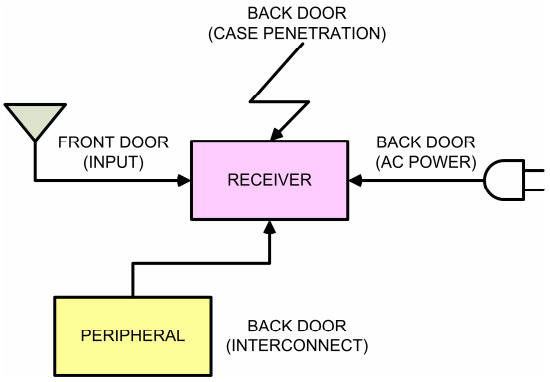

Figure 2: Means of entry by disturbances

1.2 Interference mitigation

There are many approaches to be applied over the source, path, and receiver of the entire system in order to increase its EMC. The following list enumerates most methods [3]:

- shield the source and victim
- balance the source and victim

- separate physically the source and victim
- isolate electrically the source and victim
- reorient the source and victim
- reduce the length of conductors in the source and victim
- reduce the strength of the source (cancellation technique)
- decrease (or change) the frequency of the source
- increase the rise and fall time of the source
- ground properly the source and victim
- filter the source and victim
- select the appropriate cables at the source and victim
- match the loads at the source and victim

The implementation of any method depends, of course, on the accessibility of each part of the system and must be considered preferably early on in the design stage to increase the possibility of success.

1.3 RF Interferences in a volume

A common type of interference in a volume is an EMI source interfering with the volume's radio receiver. A volume could be, for example, a car, a boat, or any other equipment containing an EMI source and a radio receiver.

There are several routes that the interference to the radio may enter. These routes are listed bellow and they are illustrated in Figure 2.

1. through the "front door", via the antenna or antenna's transmission line

2. through the "back door", via the power leads

3. through the speakers' leads (and other inputs or outputs)

4. through the radio's chassis

In this thesis, the goal is to design a solution to reduce RF emissions created by switching power electronic equipment, such as DC/DC converters existing inside the volume.

It is known that the level of radiated emissions from the secondary of the converters is dependent on the geometry of the wiring between the output of the converter and the load [9]. If inside the volume there are long wires between the switching equipment and the load, the wires might behave as an unintended antenna that emits electromagnetic waves in the frequency range of the switching signal to the load, increasing the level of radiated emissions. In this case, it is not possible to apply simple solutions such as shielding (due to the long distance) and twisting the wires would just cancel out the variations in the magnetic field.

2 Double MOSFET switching idea

2.1 Cancellation Technique

In order to reduce the RF emissions from the wires between the switching equipment and the load inside a volume, a cancellation technique is proposed. The cancellation technique consists in splitting the switching voltage into two paths with 180^o phase difference and equal magnitude. The split signal is intended to cancel out the variation in the electric field and consequently, reduce the electromagnetic emission.

2.2 Proposed Setup

One way to apply the cancellation technique is by having two controlled switching devices switching symmetrically against each other instead of having one single switching device in the converter to drive the load.

The chosen switching device is the MOSFET and the reason why the MOSFET is chosen over other controlled switching devices is explained in 3.2.1.

The proposed setup of the MOSFETs and the load is shown in Figure 3.

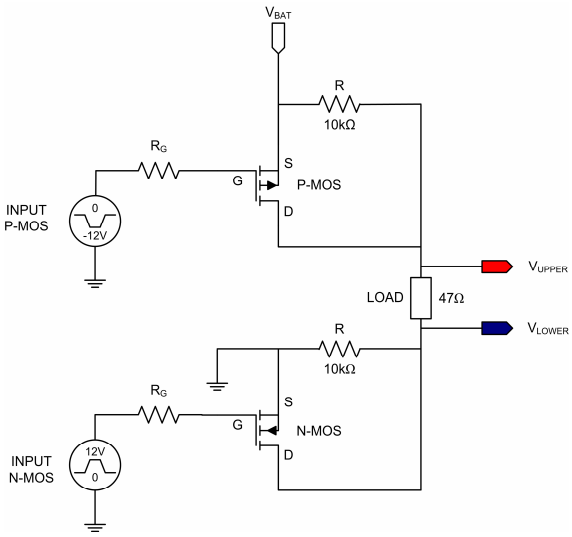

Figure 3: MOSFET setup

The working principle is: the upper MOSFET produces the upper voltage V_{UPPER} while the lower MOSFET produces the lower voltage V_{LOWER}. When the upper and lower MOSFETs are ON, V_{UPPER} and V_{LOWER} are respectively V_{BAT} and zero, and the voltage over the load is V_{BAT}. When the upper and lower MOSFETs are OFF, V_{UPPER} and V_{LOWER} are approximately $V_{BAT}/2$, and the voltage over the load is approximately zero. Figure 4 shows the working principle and dynamics of the double MOSFET switching by illustrating the current paths during the ON and OFF states of the MOSFETs.

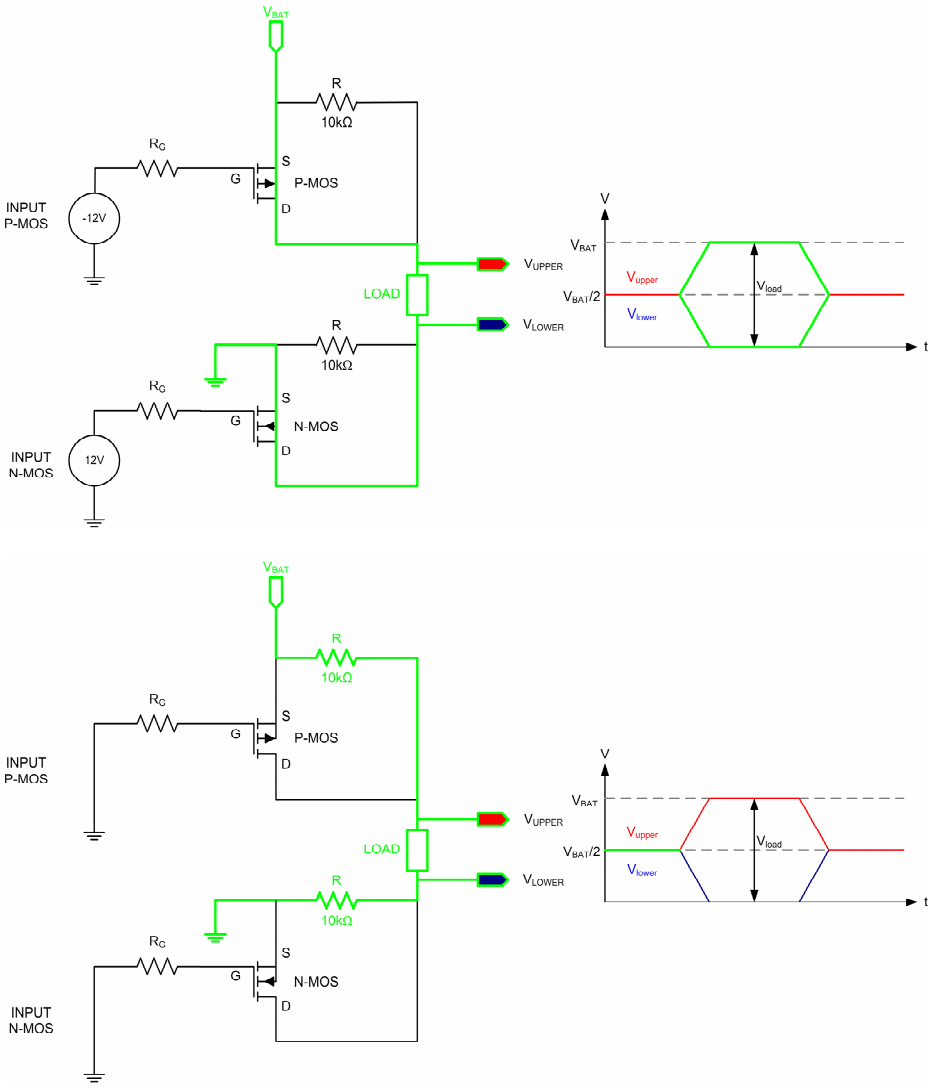

Figure 4: MOSFET setup - working principle

Through this technique, the voltage over the load switches between zero and V_{BAT}, similarly to a single switching. The most important difference between double and single switching is that, in the double switching, the sum of V_{UPPER} and V_{LOWER} equals V_{BAT} at all times, consequently a DC signal is seen from the outside and this means that there will be a reduction in the high frequency disturbances.

As the sum of V_{UPPER} and V_{LOWER} should equal V_{BAT} at all times, it is essential that V_{UPPER} and V_{LOWER} are as symmetrical as possible. The way to implement this is to define one MOSFET as a master and the other as a slave. The MOSFET that acts as the slave will have the switching signal added with a regulated feedback signal from the load as its input.

2.3 Non-symmetrical V_{UPPER} and V_{LOWER}

A very common problem is to not have V_{UPPER} and V_{LOWER} as perfect mirror images of each other. Consequently, the summation of V_{UPPER} and V_{LOWER} will not correspond to a constant DC signal and disturbances will exist. The following sections describe two kinds of problems that results in deviations from a constant DC level.

2.3.1 Different slew rates between the upper and lower MOSFETs

Considering the input signal to the MOSFET absolutely symmetric, there could be a non-symmetrical switching caused by the differences in the slew rates between the upper and lower MOSFETs.

It is known that the MOSFET's switching behaviour is dependant on the charge and discharge of its internal capacitances (further on Section 3.2.1, the internal characteristics of the MOSFET will be explained in detail). The difference in the values of the MOSFETs internal capacitances in addition with the value of their gate resistance could cause difference in the slew rates between the upper and lower MOSFETs and, consequently, generate a non-symmetrical switching.

There are four kinds of differences in the slew rates between the upper and lower MOSFET, which cause the following transients in the summation of V_{UPPER} and V_{LOWER}:

1. Upper MOSFET turns on faster

Figure 5: V_{UPPER}, V_{LOWER} during turn-on - Summation of V_{UPPER} and V_{LOWER}

2. Upper MOSFET turns off faster

Figure 6: V_{UPPER}, V_{LOWER} during turn-off - Summation of V_{UPPER} and V_{LOWER}

3. Lower MOSFET turns on faster

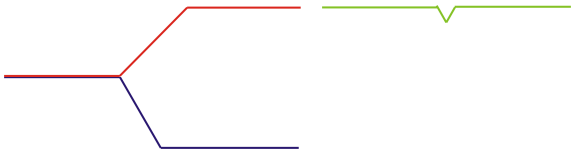

Figure 7: V_{UPPER}, V_{LOWER} during turn-on - Summation of V_{UPPER} and V_{LOWER}

4. Lower MOSFET turns off faster

Figure 8: V_{UPPER}, V_{LOWER} during turn-off - Summation of V_{UPPER} and V_{LOWER}

2.3.2 Time-shift between the upper and lower MOSFETs

Considering the input signal to the MOSFET absolutely symmetric and identical slew rates of the lower and upper MOSFETs, there could be a time-shift between the upper and lower MOSFETs, also caused by the internal characteristics of the MOSFETs.

The reason for the time-delay could be explained by the difference in threshold voltage between the upper and lower MOSFETs (further on Section 3.2.1, the internal characteristics of the MOSFET will be explained in detail).

Similarly to the previous section, the different time-shifts cause the following transients in the summation of V_{UPPER} and V_{LOWER}:

1 Upper MOSFER turns on earlier

Figure 9: V_{UPPER}, V_{LOWER} during turn-on - Summation of V_{UPPER} and V_{LOWER}

2 Upper MOSFER turns off earlier

Figure 10: V_{UPPER}, V_{LOWER} during turn-off - Summation of V_{UPPER} and V_{LOWER}

3 Lower MOSFER turns on earlier

Figure 11: V_{UPPER}, V_{LOWER} during turn-on - Summation of V_{UPPER} and V_{LOWER}

4 Lower MOSFET turns off earlier

Figure 12: V_{UPPER}, V_{LOWER} during turn-off - Summation of V_{UPPER} and V_{LOWER}

3 Design of the Circuit

3.1 Circuit's parts

Figure 13 shows a block diagram with proposed parts for the implementation of the double MOSFET switching.

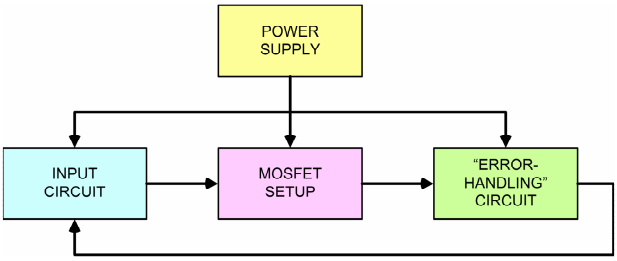

Figure 13: Block diagram of the circuit parts

The design of each part and the choice of components are done according to the following considerations and limitations:

- In order to not introduce more sources of EMI in the circuit (such as DC/DC converters) and facilitate the design, the considered power supply for the electronic devices and the load is the battery available in the volume. The main voltage in this battery is considered to be+12V, although the instantaneous voltage level can vary from +10V to +16V. The voltage level and its variation are the only restrictions related to the power supply. No current limitation is considered.

- The circuit should be constructed in a printed circuit board (PCB) using surface mounted devices in order to reduce the impact of non-ideal wring.

- The circuit should be designed to drive a resistive load of approximately 47Ω with a switching frequency of minimum 5 kHz.

In the following items, the design of each part is explained in detail.

3.2 The MOSFET Setup

3.2.1 MOSFET Overview

The metal oxide field effect transistor (MOSFET) is based on the original field-effect transistor introduced in the 70s. The invention of the MOSFET was partly driven by the limitations of bipolar junction transistors (BJTs) in power electronics applications. It is not possible to absolutely define the operation boundaries of a power device; [4] defines a power device as any device that can switch at least 1A.

Some of the limitations of the bipolar transistors for this application are:

- The bipolar power transistor is a current controlled device. A large base drive current as high as one-fifth of the collector current is required to keep the device in the ON state.
- Higher reverse base drive currents are required to obtain fast turn-off.
- They are inferior to the MOSFET in high frequency application were the switching power loss are important.

The above limitations make the base circuit design of the bipolar transistor more complicated and hence more expensive than the MOSFET. For these reasons the MOSFET was the chosen switch device for this project, and its basic function is to control the drain current by the gate voltage.

Figure 14 shows the n-channel and p-channel MOSFET device symbol, transfer characteristics and output (i_D - v_{DS}).

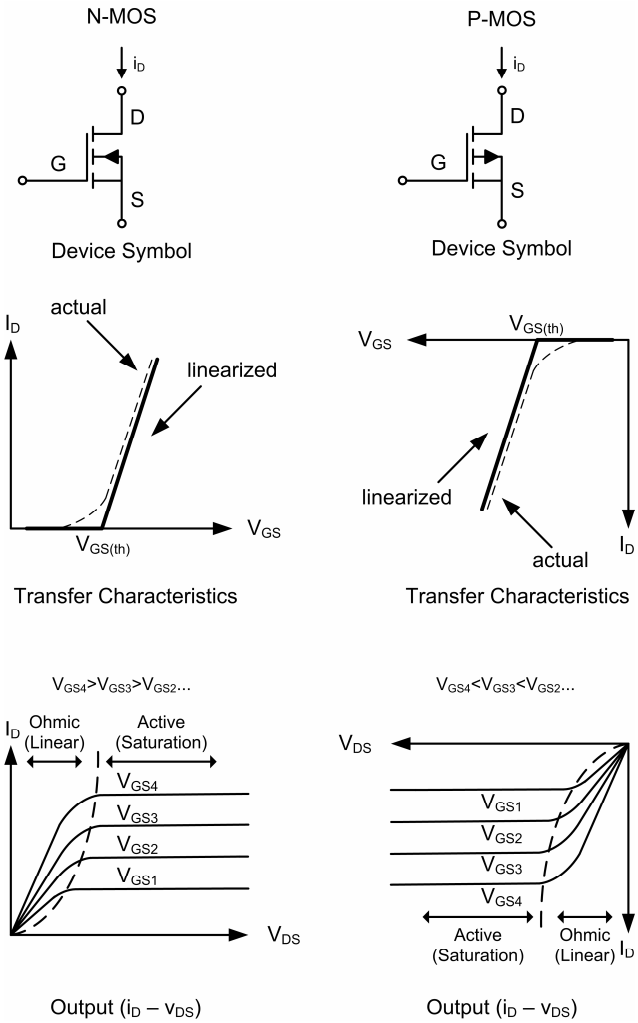

Figure 14: N-MOS and P-MOS device symbol, transfer characteristics and output (i_D - v_{DS})

3.2.1.1 MOSFET equivalent circuit model

From the physical configuration of the MOSFET presented in Figure 15, it is possible to identify the existence of parasitic components in its structure. Some of the parasitic components have substantial effect on the MOSFET switching performance and, therefore they are used in the MOSFET's circuit model for transient analysis shown in Figure 16.

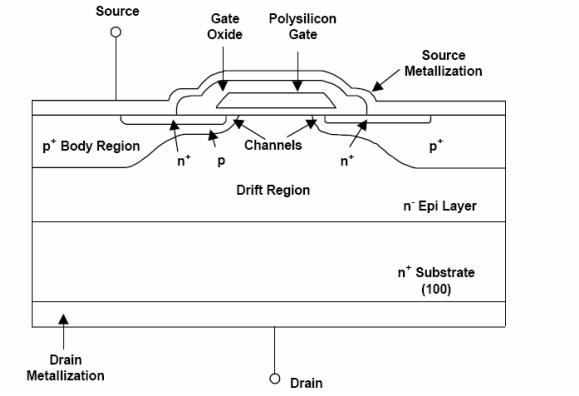

Figure 15: Schematic diagram for an n-channel MOSFET

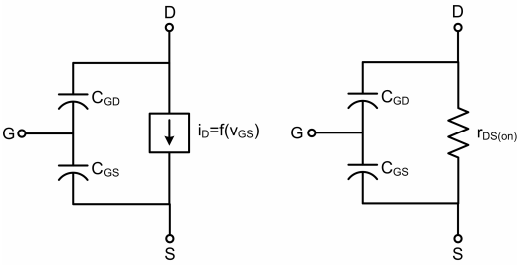

Figure 16: MOSFET model for transient analysis - Active region model and ohmic region model

C_{GS} is the capacitance due to the overlap of the source and the channel regions by the polysilicon gate and is independent of the applied voltage.

C_{GD} consists of two parts, the first is the capacitance associated with the overlap of the polysilicon gate and the silicon underneath in the JFET region. The second part is the capacitance associated with the depletion region immediately under the gate. As shown in Figure 17, C_{GD} is a nonlinear function of the drain-source voltage and is the most important parameter because it provides a feedback loop between the output and the input of the MOSFET's circuit model. It is also called Miller capacitance.

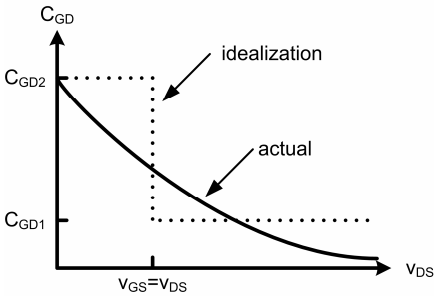

Figure 17: Variation of the gate-drain capacitance as function of the drain-source voltage

C_{DS} is the capacitance associated with the body-drift diode and varies inversely with the square root of the drain-source bias. This capacitance does not substantially affect the switching characteristics or waveform, so it is not considered in the MOSFET model for transient analysis. However, it should be considered when designing snubbers [5].

$R_{DS(on)}$ is the on-state resistance.

3.2.1.2 Switching dynamic characteristics

Based on the circuit model, it is possible to examine the switching behaviour of the power MOSFET. The switching performance is determined by the time required to establish voltages changes across the MOSFET capacitances.

A suitable example to verify the dynamic characteristics of the MOSFET is to analyze the voltage and current waveforms of an n-channel MOSFET embedded in a step-down DC/DC converter [5]. In this step-down DC/DC converter, the inductive load is modelled as a constant current source I0 in parallel with a diode D_f (modelled as an ideal diode). The gate is driven by an ideal voltage source, which is assumed to be a voltage pulse between zero and V_{GG} in series with an external gate resistance R_G as shown in Figure 18.

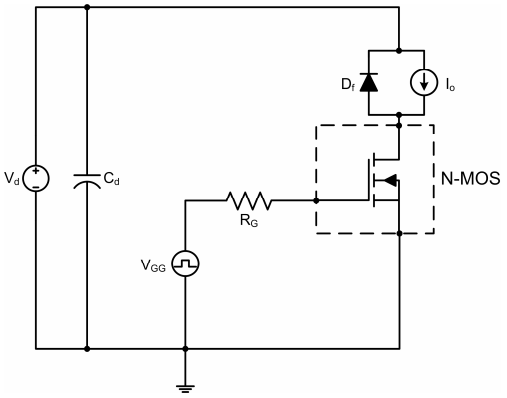

Figure 18: MOSFET embedded in a buck converter

3.2.1.2.1 Turn on

Figure 19 shows the voltage and current waveforms of the MOSFET circuit model embedded in a Buck converter. The dynamics of each time interval represented in Figure 19 is explained bellow.

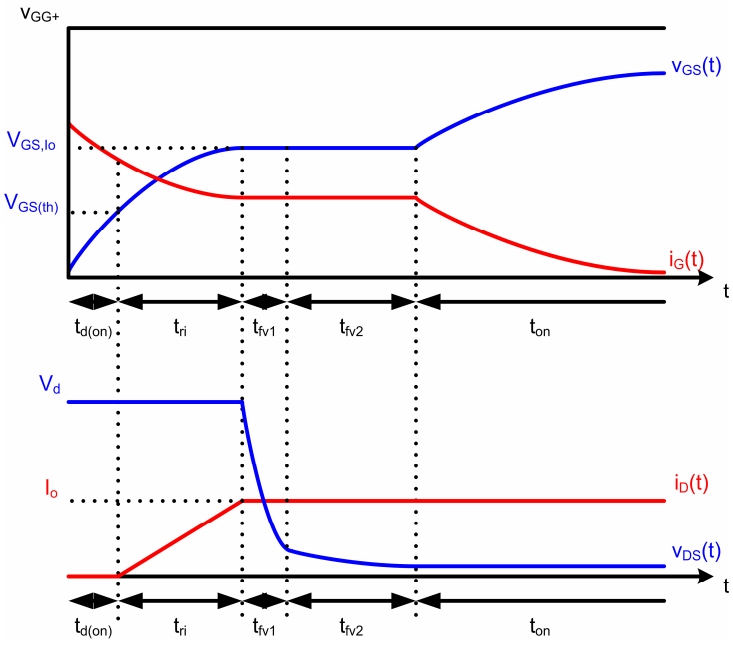

Figure 19: MOSFET dynamics - turn-on

-$t_{d(on)}$: when a voltage step from zero to V_{GG} is applied in the gate (Note: V_{GG}>>$V_{GS(th)}$), the gate-source voltage v_{GS} rises from zero to $V_{GS(th)}$. This dynamic corresponds to charge of the C_{GS} and C_{GD} capacitor, as is shown in the equivalent circuit in Figure 20. The v_{GS} voltage during this interval corresponds to the equation:

$$v_{GS}(t) = V_{GG}\left(1 - e^{\frac{-t}{R_G (C_{GS}+C_{GD1})}}\right) \quad (3.1)$$

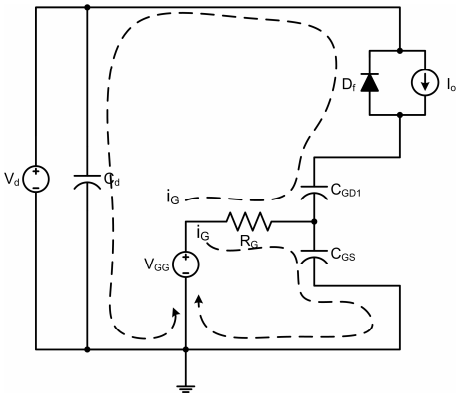

Figure 20: Equivalent circuit during $t_{d(on)}$

-t_{ri}: beyond $V_{GS(th)}$, v_{GS} continues to rise as before, and the drain current i_D begins to increase. The drain-source voltage remains at V_d as long as i_D is lower than the load current Io and the free-wheeling diode is conducting. The equivalent circuit representing this dynamic behaviour is shown in Figure 21.

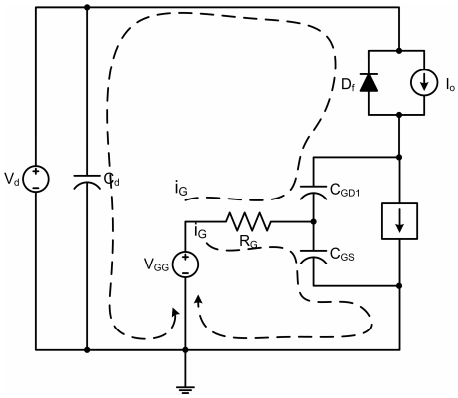

Figure 21: Equivalent circuit during t_{ri}

-t_{fv1}: when i_D reaches the load current I_o, but the MOSFET is still in the active region, the gate-source voltage v_{GS} becomes temporarily clamped at $V_{GS,Io}$, which is the gate-source voltage needed to maintain $i_D = I_o$.

$$i_G(t) = \frac{V_{GG} - V_{GS,I_o}}{R_G} \tag{3.2}$$

$$\frac{dv_{DG}}{dt} = \frac{dv_{DS}}{dt} = \frac{i_G}{c_{GD}} = \frac{V_{GG} - V_{GS,I_o}}{R_G C_{GD}} \tag{3.3}$$

The entire gate current i_G, given by (3.2), flows through C_{GD}, which in this interval is equivalent to C_{GD1}, causing the drain-source voltage v_{DS} to drop at a rate given by (3.3). The equivalent circuit representing this dynamic is shown in Figure 22.

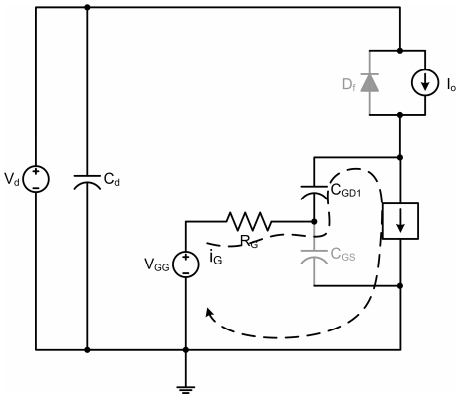

Figure 22: Equivalent circuit during t_{fv1}

-t_{fv2}: during this time interval, the voltage v_{GS} is still clamped at $V_{GS,lo}$ and the drain-source voltage v_{DS} continues to decrease similarly to t_{fv1}. The main differences are that the MOSFET is in it transient operation between the active and ohmic region and the C_{GD} is equivalent to C_{GD2}. The correspondent equivalent circuit is shown in Figure 23.

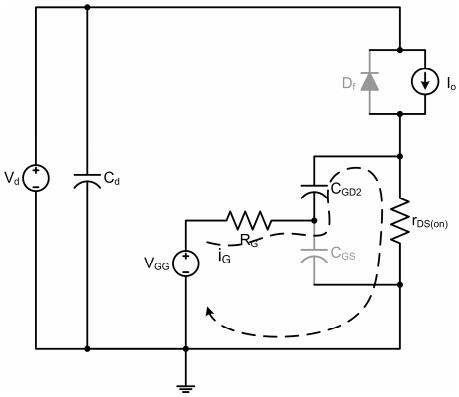

Figure 23: Equivalent circuit during t_{fv2}

-t_{on}: once the drain-source voltage v_{DS} has completed its drop to the on-state value of $I_o r_{DS(on)}$, the gate-source voltage v_{GS} becomes unclamped and continues its growth towards V_{GG} according to Figure 24.

$$v_{GS}(t) = V_{GG}(1 - e^{\frac{-t}{R_G(C_{GS}+C_{GD2})}}) \tag{3.4}$$

The increase of v_{GS} is described by (3.4). The gate current decays toward zero with the same time constant ($R_G(C_{GS}+C_{GD2})$)of (3.4).

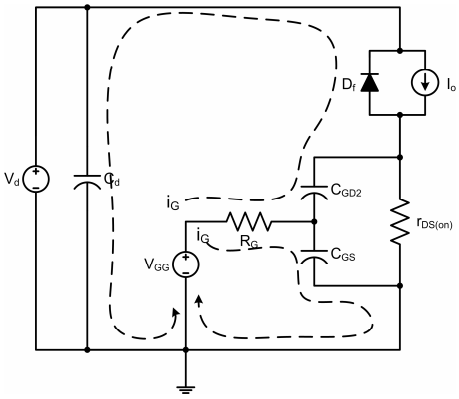

Figure 24: Equivalent circuit during t_{on}

3.2.1.2.2 Turn off

Figure 25 shows the voltage and current waveforms of the MOSFET embedded in a buck converter during turn-off. The turn-off characteristic is an inverse sequence of the turn-on events.

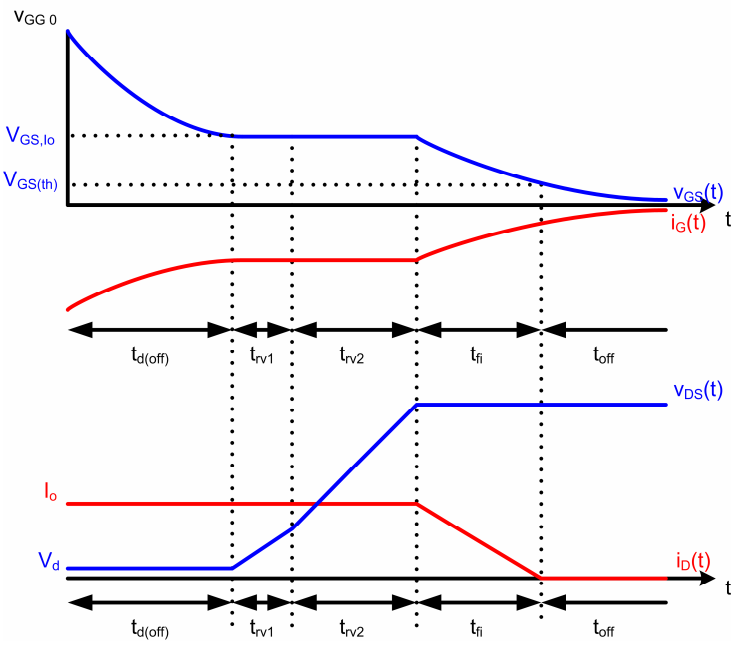

Figure 25: MOSFET dynamics - turn-off

3.2.2 The IRF 7307

When choosing the MOSFETs to implement the double MOSFET switching, there are some issues to be considered. They are:

1. The MOSFETs must be able handle the power requirements (see Section 3.1).

2. The MOSFETs should be available in surface mounted technology (see Section 3.1).

3. In order to verify the designed circuit through simulations, the MOSFETs should have some reliable equivalent SPICE model to be simulated in OrCAD Capture.

4. The N-MOS and P-MOS should have very similar turn-on and turn-off times in order to avoid non-symmetrical switching.

The device that matches these requirements and presents some particular advantages is the IRF7307 from International Rectifier. The IRF7307 contains an N-MOS and a P-MOS in the same surface mounted package and a very low on-state resistance which implies in low on-state losses.

3.2.2.1 MOSFET SPICE model

The SPICE model for the IRF7307 N-MOS and P-MOS is the model available in the device manufacturer's webpage and is the same model found in the internal library of OrCAD Capture. The models' files are presented in Appendix – IRF 7307 SPICE model. Each MOSFET model consists in a MOSFET type *level 1* with some external components to adjust the model *level 1* to the real IRF7307.

The model type *level 1* is a MOSFET model based on the physical properties of the MOSFET and equations that corresponds to its electrical behaviour (for more detail about the equations, see ref [13]). According to [12], this model has a relatively accuracy of C_{GD}, constant value of C_{GS} and omits the reverse recovery for the body diode. The suggested applications of this model are general power electronic circuit simulations where v_{GS} is always above zero, and the body diode is not used.

Figure 26 shows the circuit correspondent to the translation of the IRF 7307 N-MOS model presented in APPENDIX 1.

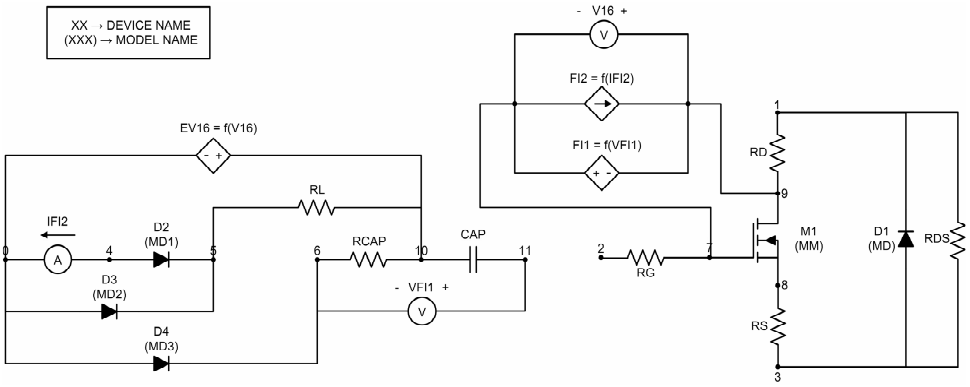

Figure 26: IRF 7307 N-MOS model

Figure 27 shows the results of some basic simulations made in order to certify the reliability of the available MOSFETs models. The N-MOS and P-MOS output characteristics are very similar to the output characteristics shown in the IRF7307 datasheet [14], which confirms the similarity of the models when compared to the real device.

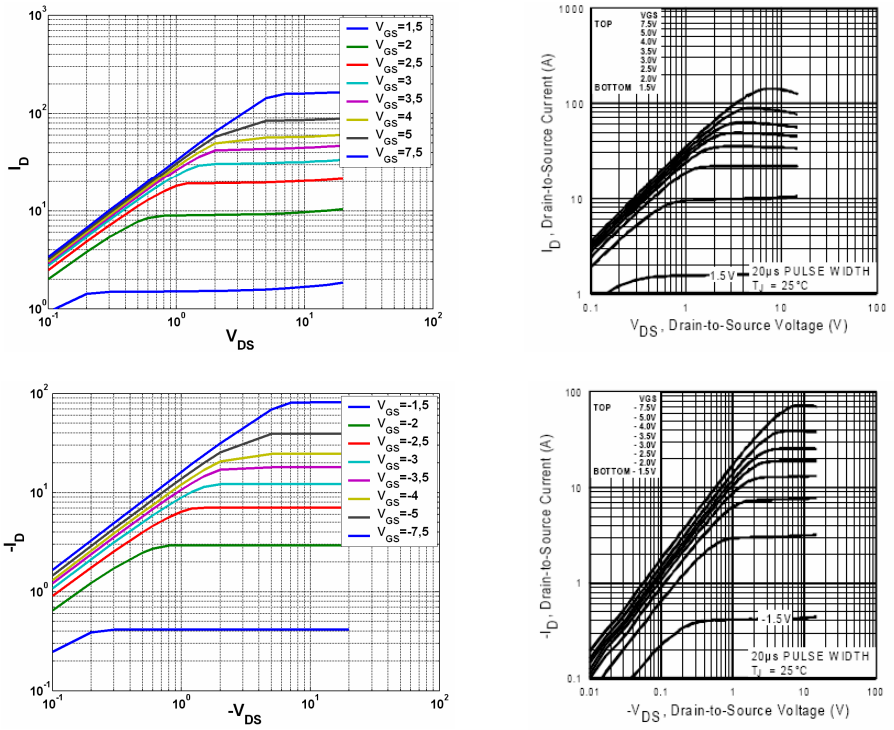

Figure 27: N-MOS and P-MOS output characteristics - simulated and datasheet [14]

3.3 The input circuit

The proposed input circuit for the P-MOS and N-MOS consists in a positive square-wave generator followed by an integrator as shown in Figure 28. The purpose of this configuration is to generate a pulse train with controlled frequency and slew rate, which facilitates the control of the MOSFET's switching dynamics.

$$v_{INT}(t) = \frac{1}{R_{INT}C_{INT}}\int_0^t \left(\frac{V_{BAT}}{2} - v_{SQW}(t)\right)dt + v_{INT}(0) \qquad (3.5)$$

The integrator has its performance represented by (3.5). By varying the resistor, it is possible to change the slew rate of the pulse train.

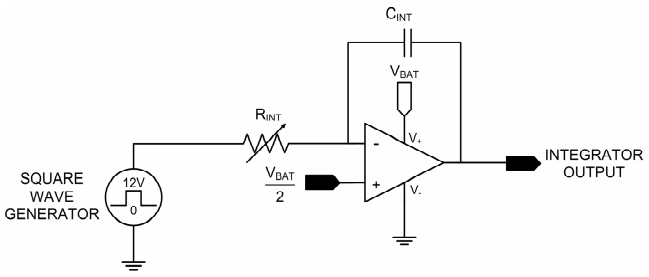

Figure 28: Square-wave generator followed by an integrator

The previous configuration creates a pulse train with an amplitude varying between zero and V_{BAT}, which is the desired v_{GG} voltage for the N-MOS input. In order to generate the right v_{GG} pulse train for the P-MOS input, an inverter circuit with an offset voltage is connected to the output of the integrator. Figure 29 shows the proposed input circuit for the P-MOS and N-MOS.

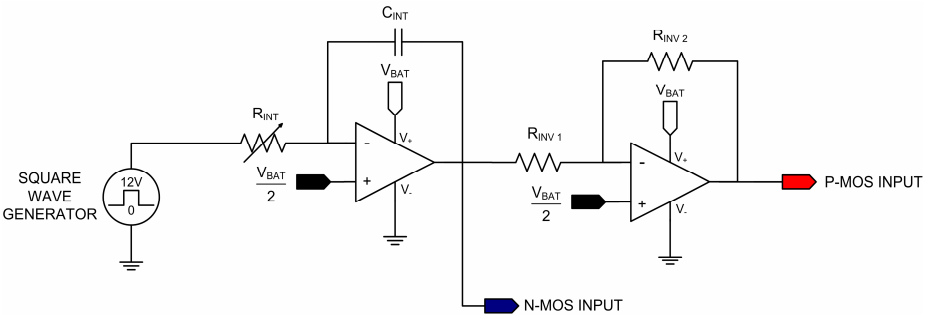

Figure 29: P-MOS and N-MOS input circuit

3.3.1 Compensation of time constants with polarized resistance set-up

The P-MOS and N-MOS have different internal capacitances, consequently, the charging/discharging time constants are different and the switching waveforms become different, resulting in non-symmetrical switching as discussed in 2.3.

Basically, there are two ways to change the MOSFETs time constants. One way is to change the external resistance R_G connected to the gate, and the other way is to connect an external capacitance between the gate and drain or gate and source. The second option is not desirable because it implies an increase of the time constants, so the focus is to control the time constants by varying R_G.

The proposed solution is to compensate the difference of time constants between the P-MOS and N-MOS through the configuration of Figure 30. This configuration consists in having, for each MOSFET, one value of external gate resistance for the turn-on and a different value of gate resistance for the turn-off, which approximates to maximum the turn-on/off time constants for the P-MOS and N-MOS.

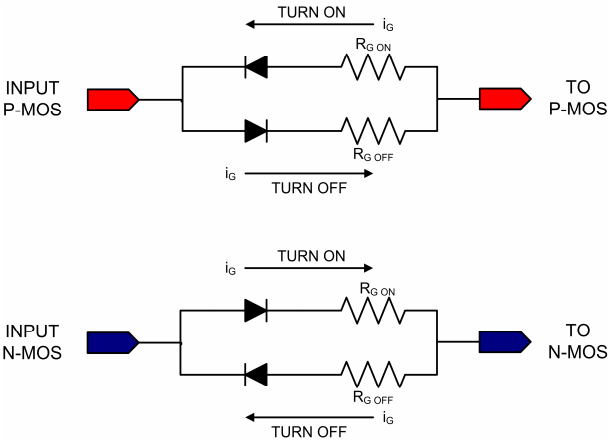

Figure 30: Polarized resistance set-up

The values of gate resistance should be as low as possible to result in fast dynamics. In order not to modify the waveforms from the input circuit, the diodes should be fast diodes, with very short reverse recovery time, low reverse recovery current, and low forward voltage drop. For these reasons, the best option found is to use the Schottky diode 10BQ040 from International Rectifier.

3.3.2 Operational amplifiers

Similarly to the MOSFET, when choosing the operational amplifiers for the input circuit as well as for other parts of the circuit, there are certain needs to be fulfilled. They are:

1. The operational amplifier should have the available battery as its power supply (see Section 3.1).

2. The operational amplifier should be available in surface mounted technology (see Section 3.1).

3. The operational amplifier should have a good SPICE model to be simulated in OrCAD Capture.

4. The operational amplifier should have a large slew rate to avoid time delay in the circuit dynamics.

5. Since the input of the MOSFETs needs to be as low as possible to make sure that they are turned-off, the operational amplifier must have rail-to-rail output.

The device that matches these requirements is the LM6144 from National Semiconductor, which contains four operational amplifiers in the same package.

3.4 The "error-handling" circuit

Even adjusting the time constants of the P-MOS and N-MOS in the input circuit, there could be some other kind of error that results in a non-symmetrical switching. As stated in Section 2.2, the way to solve this problem is to define one MOSFET as a master and the other as a slave. The MOSFET that acts as the slave will have the previously designed input signal added with a regulated signal from the load as its input.

The IRF7307 P-MOS has larger C_{GD} capacitance than the N-MOS [14] and it has a longer input circuit with one more stage using operational amplifier. These characteristics probably make the dynamics of the P-MOS slower than the N-MOS, and, for that reason, the P-MOS is defined as the master MOSFET.

3.4.1 Regulator design

When the sum of the outputs of the MOSFETs V_{UPPER} and V_{LOWER} are not equal to V_{BAT} at all times, it means that there is a non-symmetrical switching. In that case, the reference signal is defined as V_{BAT} and the error signal is defined as:

$$E = V_{BAT} - (V_{UPPER} + V_{LOWER}) \tag{3.6}$$

There are several kinds of regulators that results in different actions to the error signal. The following item contain the principle of the chosen regulator and how to implement it.

3.4.1.1 The P regulator

A regulator with a proportional control action has the following relation between the output of the controller U and the error signal E:

$$U = K_P.E \tag{3.7}$$

Even though there are many ways to implement a P regulator, the selected configuration for this application is a non-inverting operational amplifier configuration as shown in Figure 31.

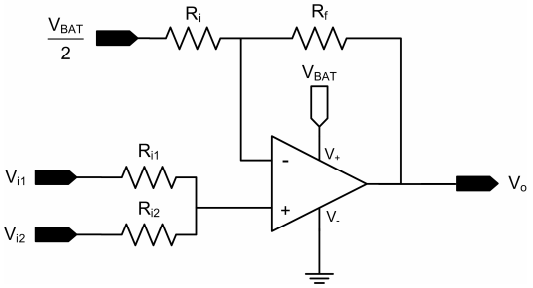

Figure 31: Non-inverting operational amplifier configuration

The relation between the output of the regulator V_o and the regulator's inputs V_{i1} and V_{i2} is given by:

$$V_0 = V_{i1}(\frac{R_{i2}}{R_{i1}+R_{i2}})(\frac{R_f}{R_i}+1) + V_{i2}(\frac{R_{i1}}{R_{i1}+R_{i2}})(\frac{R_f}{R_i}+1) - \frac{V_{BAT}}{2}(\frac{R_f}{R_i}) \quad (3.8)$$

Having R_{i1}equal to R_{i2} and substituting V_{i1} and V_{i2} for V_{UPPER} and V_{LOWER} respectively, the equation above becomes:

$$V_0 = \frac{1}{2}(V_{UPPER} + V_{LOWER})(\frac{R_f}{R_i}+1) - \frac{V_{BAT}}{2}(\frac{R_f}{R_i}) \quad (3.9)$$

Rearranging the terms and using the error definition described by (3.6), the regulator's output V_o is then:

$$V_0 = \left[-\frac{1}{2}(\frac{R_f}{R_i}+1)\right]E + \frac{V_{BAT}}{2} \quad (3.10)$$

This corresponds to the relation that describes the P regulator (3.7), but with a voltage offset of $V_{BAT}/2$.

3.4.2 Adding the regulator output to the input signal

In order to add the regulator output to the previously designed N-MOS input signal; the same non-inverting operation amplifier configuration of Figure 31 is used. In this case, the inputs V_{i1} and V_{i2} correspond to the previously designed N-MOS input, $V_{IN\ N\text{-}MOS}$, and the regulator output, V_o. Having R_{i1} equal to R_{i2} and R_f equal to R_i, the resulting signal of this configuration, V_o' is then:

$$V_0' = (V_{IN\,N\text{-}MOS} + V_o) - \frac{V_{BAT}}{2} \quad (3.11)$$

It is important to observe that, depending on the summation of V_o and $V_{IN\ N\text{-}MOS}$; V_o' can have a negative value. However, once the operational amplifier that implements this function is fed with zero and V_{BAT}, this configuration will not be able to deliver the right negative output V_o' that would be limited downwards to zero volt.

The proposed solution for this problem is supply the operational amplifier with a negative voltage source, which is achieved by adding a charge-pump voltage converter that delivers -10V in its output. The chosen charge-pump converter is the MAXIM MAX680 and the 5V regulator used as the converter's input is the LM2936-05 from National Semiconductor.

The final layout of the circuit including the input circuit, MOSFET setup and the "error-handling" configuration is presented in Figure 32.

Prepared (also subject responsible if other)		No.		
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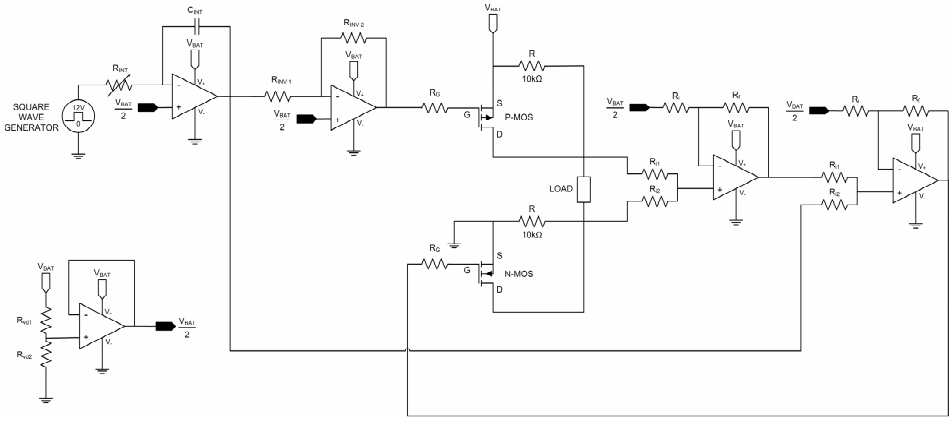

Figure 32: Circuit schematics

4 Printed Circuit Board (PCB)

4.1 Non-ideal behavior of components

The final circuit schematics presented in Figure 32 was implemented in a surface-mounted printed circuit board (PCB). The main motivation for the construction of the designed circuit in a PCB was the desire to reduce the effect of the internal inductances of the wires in the circuit, which is the component that probably affects the behaviour of the circuit in the most negative way.

A wire has an internal inductance that is frequency-dependent [7], since it is due to magnetic flux internal to the wire. The dc internal inductance $l_{i,dc}$ and the high-frequency internal inductance $l_{i,hf}$, where the current tend to crowd toward the wire surface due to skin effect are derived as

$$l_{i,dc} = \frac{\mu_0}{8\pi} = 50\text{nH/m}; \qquad \text{for } r_w << \delta \tag{4.1}$$

and,

$$l_{i,hf} = \frac{1}{4\pi\pi_w}\sqrt{\frac{\mu_0}{\pi\sigma}}\frac{1}{\sqrt{f}}; \qquad \text{for } r_w >> \delta \tag{4.2}$$

where

r_w is the radius of the wire,

σ is the wire's conductivity,

μ_0 is permeability in free space, and

δ is the skin depth of the wire (decreases with the frequency increase)

The aim was to build a small, clean and flexible board that reduces the possible sources of errors during the measurement tests and correspond very close to the simulation conditions.

4.2 OrCAD Layout

The used software for the PCB designing was the OrCAD Layout. The main advantages of OrCAD Layout over other PCB designing software's were its simplicity and the possibility to communicate with the software for schematics design and simulation, OrCAD Capture.

The design of the PCB was done according to the following steps:

1. The circuit schematics was designed and simulated in OrCAD Capture.

2. In OrCAD Capture, all the components and devices were linked to the right footprint in the common footprint library for OrCAD Capture and Layout.

3. A netlist containing all the connections between components was created in OrCAD Capture.

4. The schematic information, such as netlist and components footprints, was exported to OrCAD Layout and the pads of the components, as well as their interconnections, were generated automatically.

5. In OrCAD Layout, the PCB characteristics, such as number of layers, location of components, thickness of the PCB tracks, board outline and the track routing were set and finally the files for the board manufacturer were generated.

4.3 Designed PCB

Figure 33 shows the picture of the constructed PCB with all the components soldered for the double MOSFET switching and Figure 34 shows the same PCB, but with single MOSFET switching configuration.

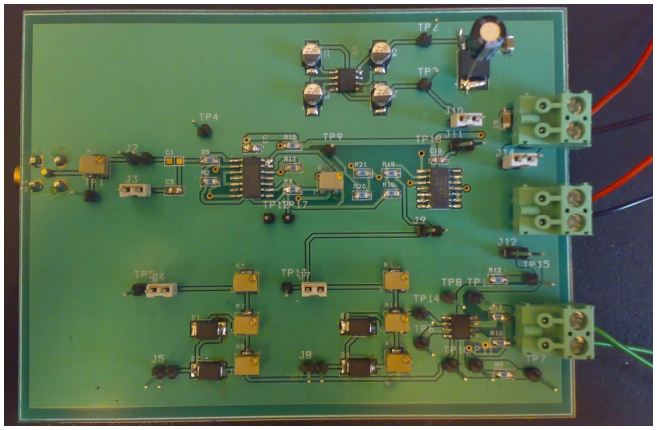

Figure 33: Double MOSFET Switching PCB

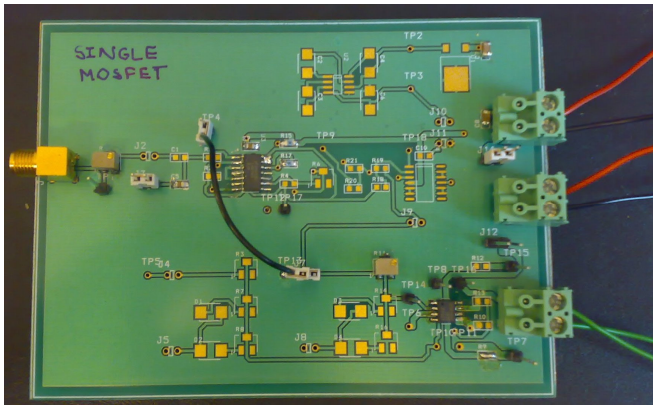

Figure 34: Single MOSFET Switching PCB

In Figure 35, the main devices of the circuit are identified in the board.

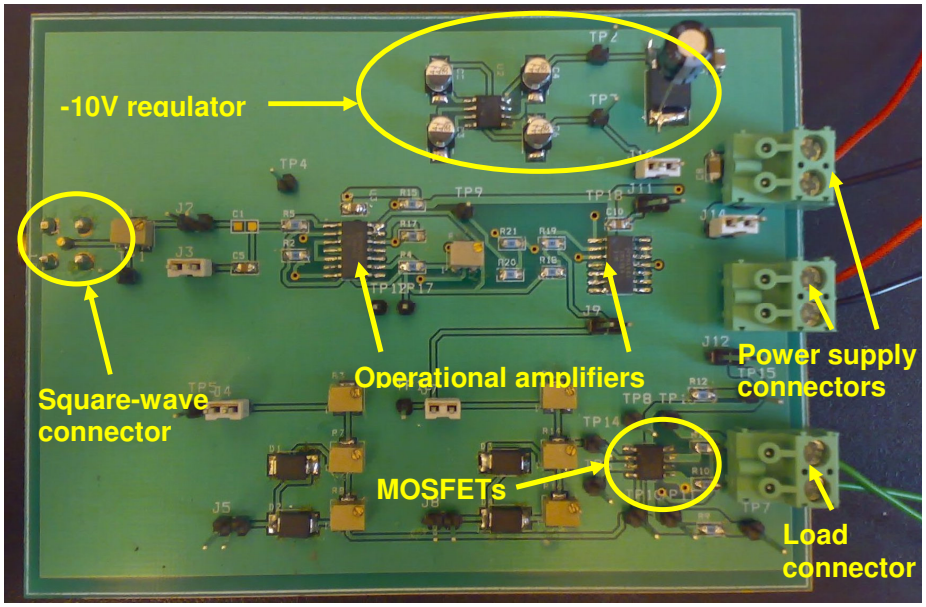

Figure 35: PCB with the main devices identified

5 Results

In order to verify the reliability of the circuit parts and facilitate the choice of parameters such as resistors and capacitors values, several simulations were done during the design of the double MOSFET switching circuit. After achieving a good performance in the simulation, the same parameters were used in the PCB and the measurements were performed.

The way to really certify that the double MOSFET switching solution reduces the emissions in the wires between converter and the load is to compare with the single MOSFET switching. For that reason, the single MOSFET switching was simulated and implemented in the same PCB layout as the double MOSFET switching according to the scheme shown in Figure 36 below.

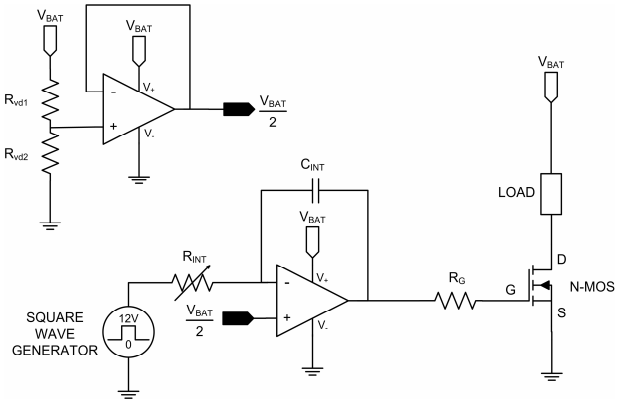

Figure 36: Single MOSFET switching scheme

The following items show the most important results of simulations and measurements of the designed circuit, including the output of each circuit's part.

5.1 Simulations

5.1.1 Single MOSFET switching

The simulation results correspond to the circuit presented in Figure 36 under the following parameters:

- V_{SQW}=12V;
- F_{SQW}=10kHz, duty cycle =0.5;
- V_{BAT}=12V;
- R_{INT}=2987Ω;
- C_{INT}=4.7nF

- R_{LOAD}=47Ω;
- R_G=100Ω.

Figure 37 presents the output voltage of the integrator circuit. In this figure, it is possible to observe a small overshoot during a few microseconds after the square-wave transients and before it starts to de-integrate. The expected output voltage would not have any overshoot and the slew would start in the same instant of the square-wave transient.

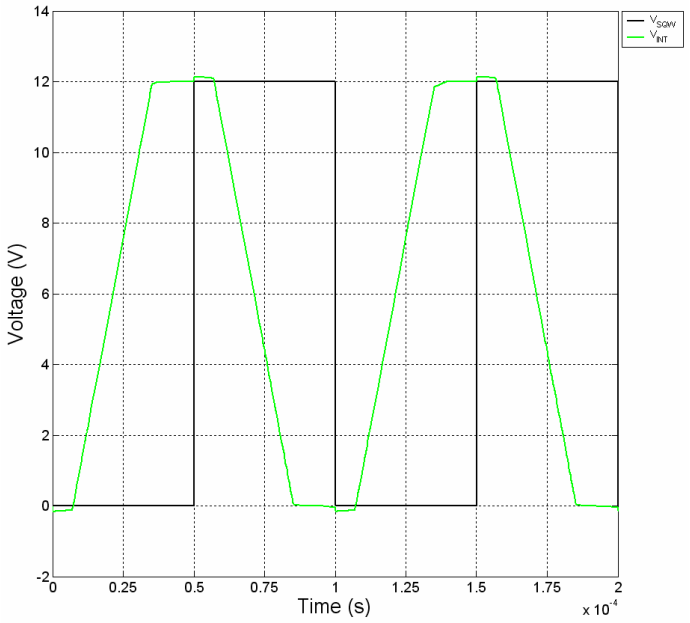

Figure 37: Simulation - Single MOSFET switching - V_{SQW} and V_{INT}

The origin of this overshoot is related to the saturation of the operational amplifier when the voltage over the integrator capacitor is higher (in module) than $\pm V_{BAT}/2$. The solution to this problem is to introduce two zener diodes in parallel to the integrator capacitor, according to the configuration of Figure 38. By choosing the right values of forward voltage drop and reverse voltage for the zener diodes, the voltage over the capacitor would vary between $\pm V_{BAT}/2$ and the integrator will behave as expected.

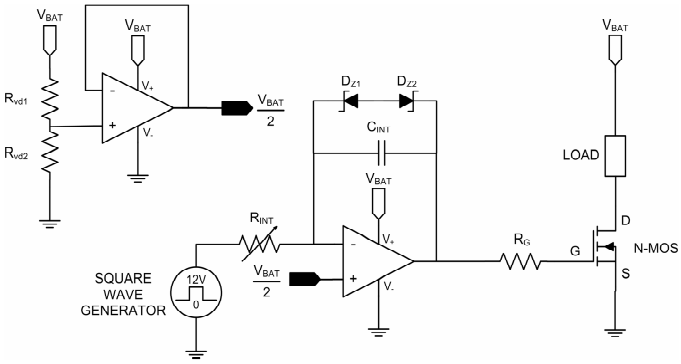

Figure 38: Single MOSFET switching scheme with zener diodes in parallel to the integrator capacitor

Figure 39 shows the output of the integrator circuit V_{INT} with the zener diode configuration in parallel to the integrator capacitor. Comparing Figure 37 with Figure 39, it is possible to observe that the zener diode configuration removes the overshoot in the integrator voltage as expected. Although the solution behave as expected, it does not show any influence (except for a time shift) in the switching dynamics of the MOSFET, so the overshoot in the integrator is not a reason of concern and the zener diode configuration can be ignored.

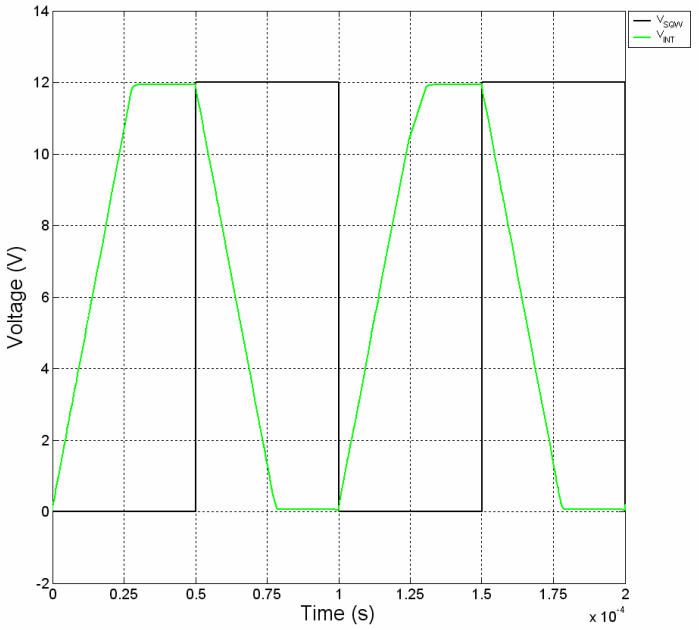

Figure 39: Simulation - Single MOSFET switching with zener diode configuration - V_{SQW} and V_{INT}

Figure 40, Figure 41 and Figure 42 show the gate-source and drain-source voltages, gate current and drain current respectively. From these curves, it is possible to observe that the MOSFET dynamic differs from the MOSFET embedded in a Buck converter seen in Section 3.2.1.2. In this case, the V_{GG} voltage is a ramp and the load is resistive. Even thought the circuit presents different dynamic characteristics, it is still possible to briefly analyse the switching behaviour.

During the turn-on, when v_{GS} starts to grow with a constant rate, the gate current i_G assumes a fixed value according to the equation:

$$I_G = (C_{GS} + C_{GD1})\frac{dv_{GS}}{dt} \tag{5.1}$$

When the v_{GS} voltage reaches the threshold value $V_{GS(th)}$, v_{DS} decreases and the drain current i_D increases with a rate dependant on the correspondent gate-drain capacitance.

When v_{GS} is equal to V_{DS}, it can be said that the Miller capacitance is changing from C_{GD1} to C_{GD2}, for that reason, it is observed a small variation in the v_{GS} voltage ramp and a large peak in the gate current.

After this region, v_{GS} continues to grow and the current i_G assumes a fixed value according to the equation:

$$I_G = (C_{GS} + C_{GD2})\frac{dv_{GS}}{dt} \tag{5.2}$$

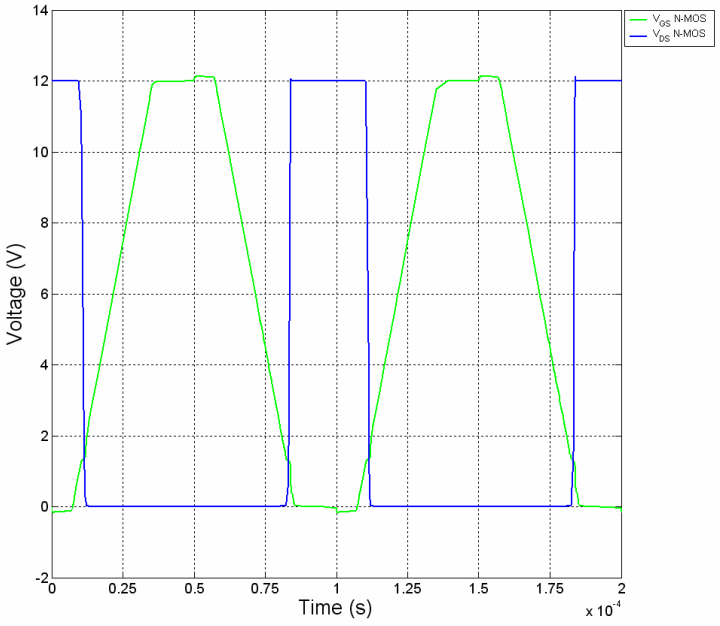

Figure 40: Simulation - Single MOSFET switching - V_{GS} and V_{DS}

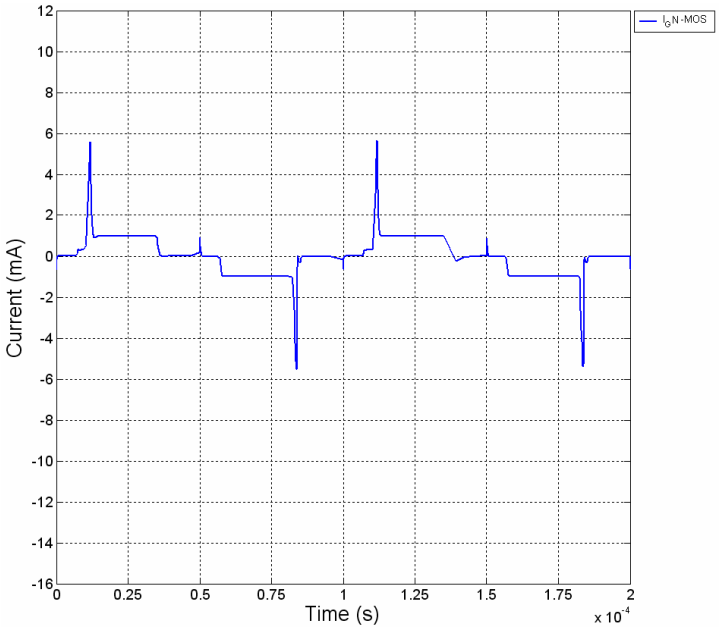

Figure 41: Simulation - Single MOSFET switching - I_G

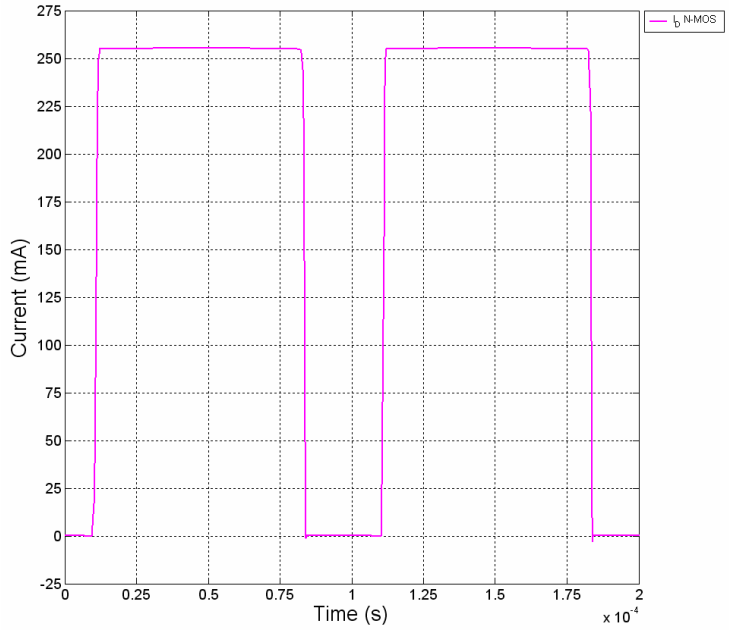

Figure 42: Simulation - Single MOSFET switching - I_D

Similarly to the double MOSFET switching, V_{UPPPER} and V_{LOWER} are defined as the upper and lower voltages over the load. Figure 43 shows the voltages over the load and the summation of them.

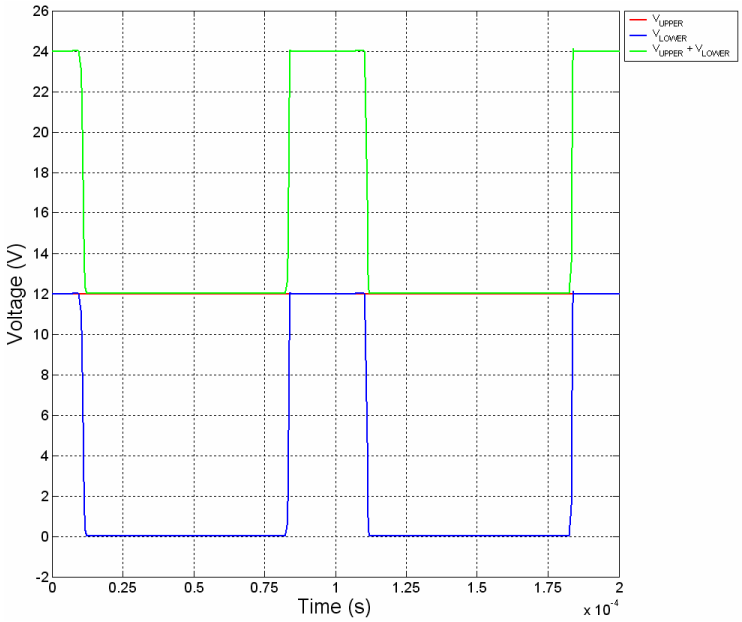

Figure 43: Simulation - Single MOSFET switching - V_{UPPER}, V_{LOWER} and V_{UPPER}+ V_{LOWER}

5.1.2 Double MOSFET switching without regulator

5.1.2.1 Single gate resistance - 5Ω

The next simulation results correspond to the circuit presented in Figure 44 under the following parameters:

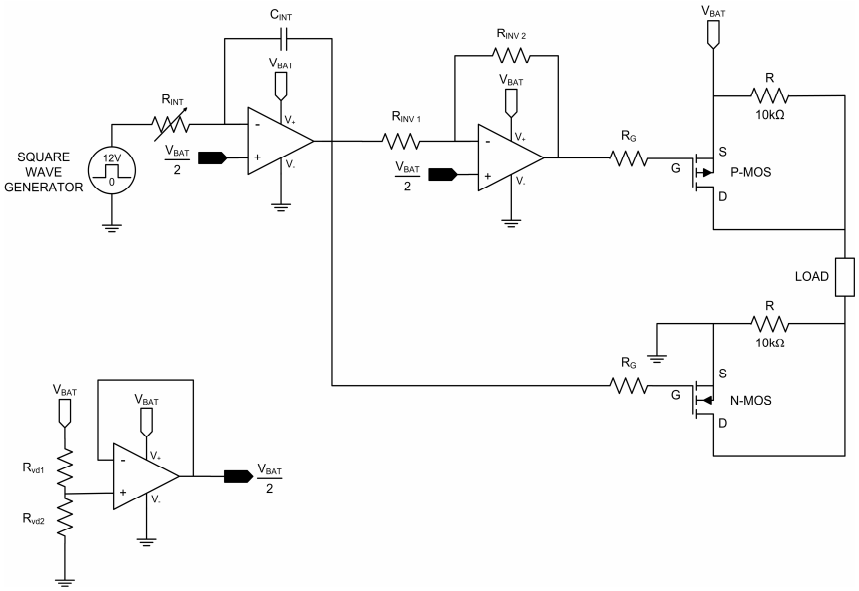

Figure 44: Double MOSFET switching without regulator

- V_{SQW}=12V;
- F_{SQW}=10kHz, duty cycle =0.5;
- V_{BAT}=12V;
- R_{INT}=3810Ω;
- C_{INT}=4.7nF
- $R_{INV\ 1}$=$R_{INV\ 2}$=10kΩ
- R_{LOAD}=47Ω;
- P-MOS R_G=5Ω;
- N-MOS R_G=5Ω.

The simulation result presented in Figure 45 corresponds to the expected performance of the integrator and inverter circuits, except for some oscillations indicated in Figure 45.

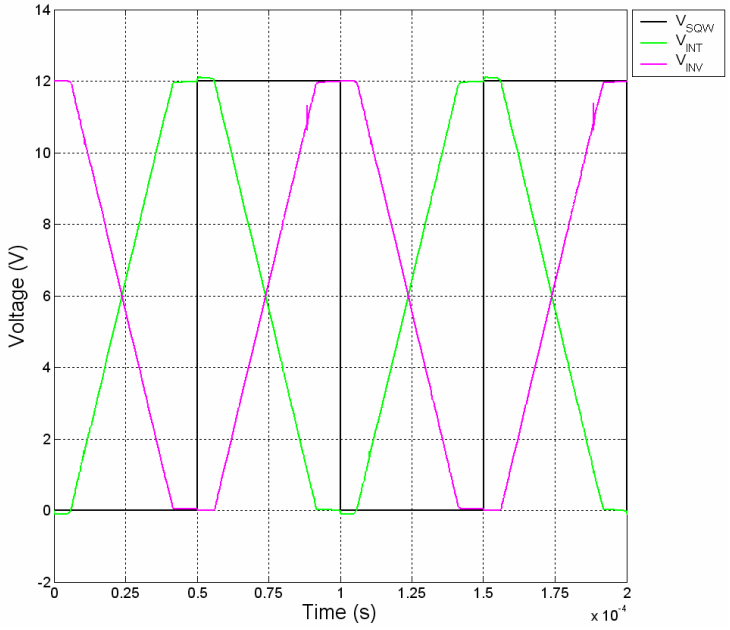

Figure 45: Simulation - Double MOSFET switching without regulator and with single gate resistance 5Ω – V_{SQW}, V_{INT} and V_{INV}

Figure 46, Figure 47 and Figure 48 show the gate-source and drain-source voltages for both MOSFETs; gate current; and load voltages V_{UPPER} and V_{LOWER}.

By observing the drain-source voltages of the two MOSFETs in Figure 46 together with the sum of V_{UPPER} and V_{LOWER} in Figure 48, it is possible to notice that this configuration generates non-symmetrical switching. The sum of V_{UPPER} and V_{LOWER} differs very much from a DC level because the turn-off of the P-MOS is faster than the turn-off of the N-MOS and the turn-on of the N-MOS is faster than the turn-on of the P-MOS.

In Figure 47 the simulation of the gate currents also presents odd oscillations as noticed previously in the inverter output of Figure 45. Figure 49 clearly shows the oscillatory behaviour during the turn-off region of the gate currents. The origin of these oscillation may be related to the inability of the operational amplifier in the inverter circuit to deliver sufficient current in the gate to drive the MOSFET with such a small gate resistor (R_G=5Ω). A solution for this problem would be to increase the gate resistances in such a way that would not affect the turn-on and turn-off time of the MOSFETs very much.

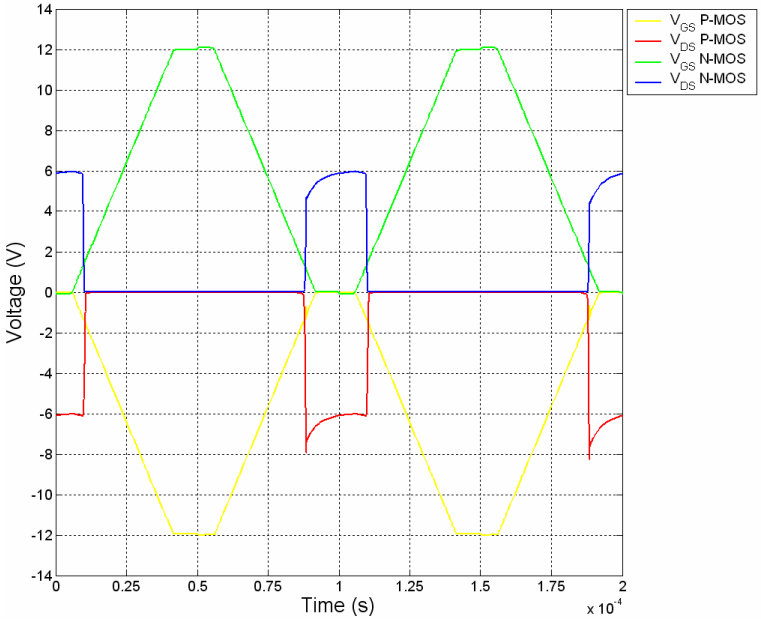

Figure 46: Simulation - Double MOSFET switching without regulator and with single gate resistance 5Ω – V_{GS} P-MOS, V_{DS} P-MOS, V_{GS} N-MOS and V_{DS} N-MOS

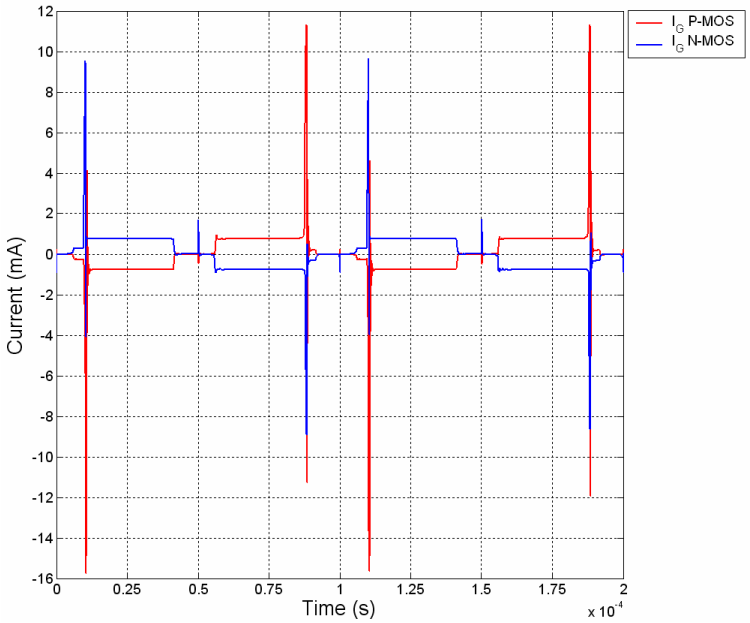

Figure 47: Simulation - Double MOSFET switching without regulator and with single gate resistance 5Ω – I_G P-MOS and I_G N-MOS

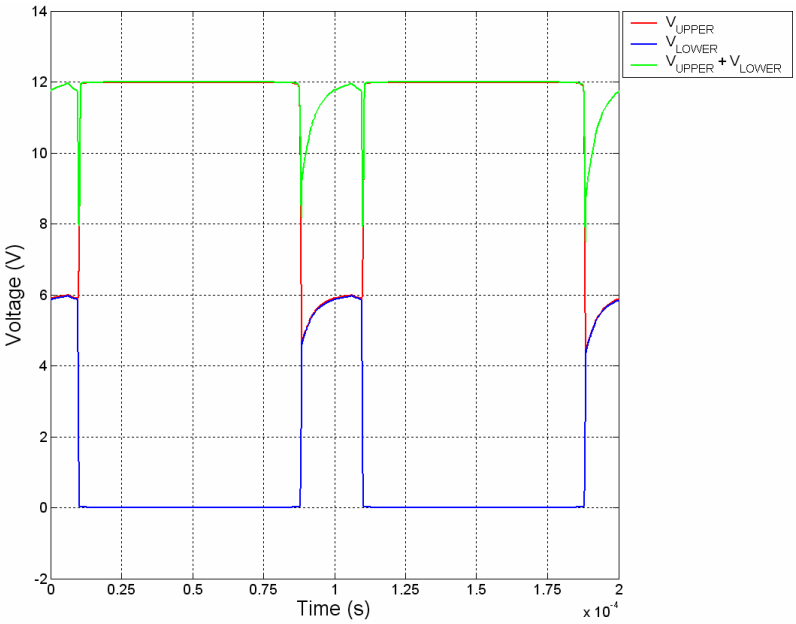

Figure 48: Simulation - Double MOSFET switching without regulator and with single gate resistance 5Ω - V_{UPPER}, V_{LOWER} and V_{UPPER}+ V_{LOWER}

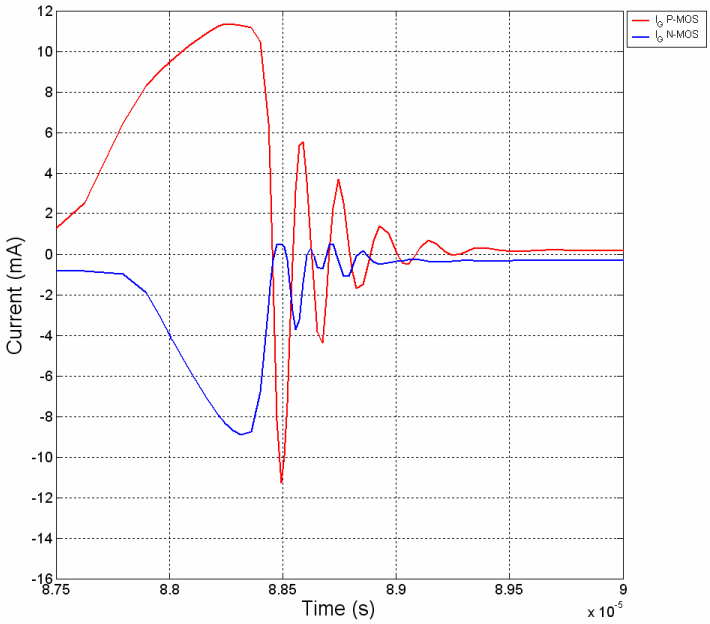

Figure 49: Simulation - Double MOSFET switching without regulator and with single gate resistance 5Ω – Zoom of I_G P-MOS and I_G N-MOS in the oscillation region of turn-off

5.1.2.2 Single gate resistance - 100Ω

In order to verify that the increase of the gate resistances do not saturate the operational amplifier, the circuit of Figure 44 was simulated with the same previous parameters, except for the gate-resistances which was changed for 100 Ω.

From Figure 50 to Figure 52, it is possible to observe the absence of oscillations. The gate current in Figure 52 presents much nicer shape and lower peak, when compared to Figure 47, which reinforce the supposition that the operational amplifier is not able to deliver enough current in the previous case.

Figure 53 shows that the sum of V_{UPPER} and V_{LOWER} still differs substantially from a constant DC level, however, with 100Ω as gate-resistance, the turn-on and turn-off of the N-MOS are faster than the P-MOS.

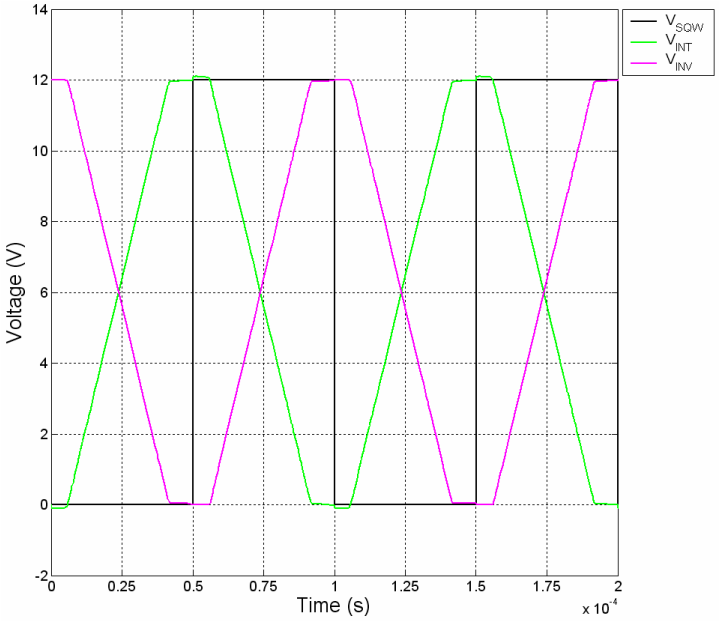

Figure 50: Simulation - Double MOSFET switching without regulator and with single gate resistance 100Ω – V_{SQW}, V_{INT} and V_{INV}

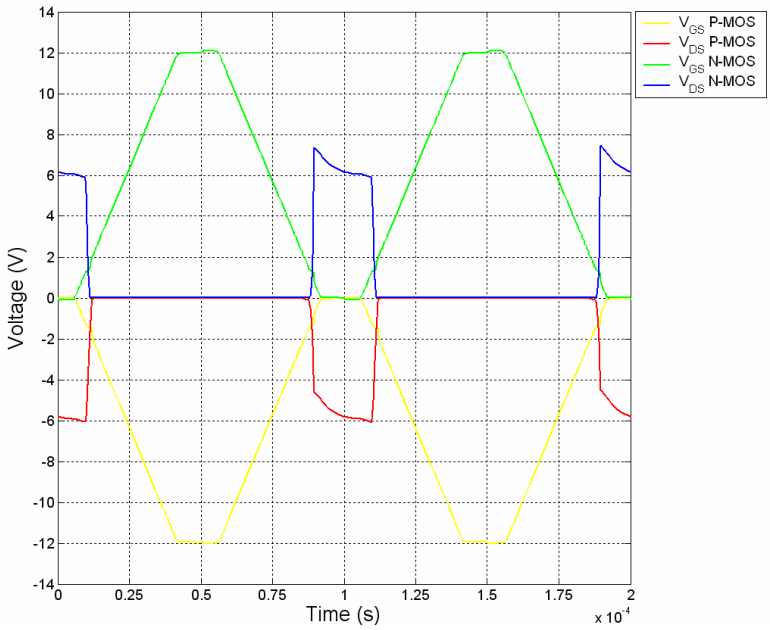

Figure 51: Simulation - Double MOSFET switching without regulator and with single gate resistance 100Ω – V_{GS} P-MOS, V_{DS} P-MOS, V_{GS} N-MOS and V_{DS} N-MOS

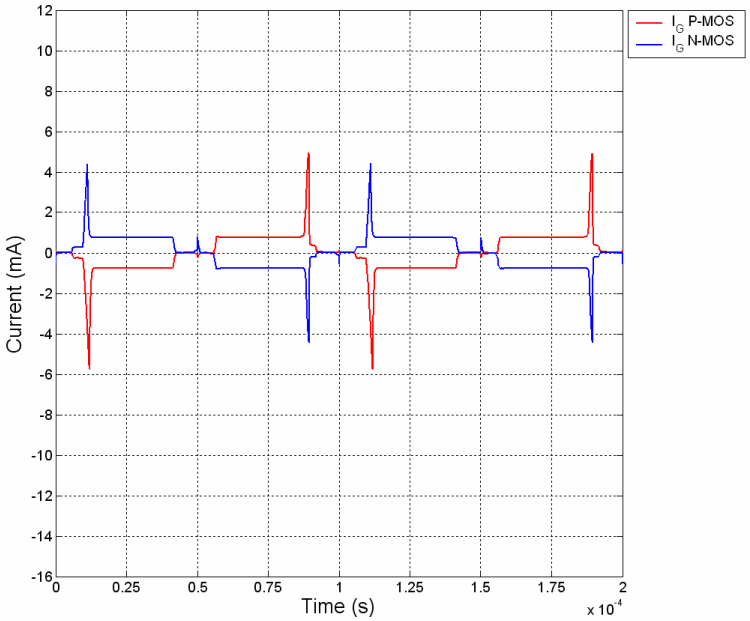

Figure 52: Simulation - Double MOSFET switching without regulator and with single gate resistance 100Ω – I_G P-MOS and I_G N-MOS

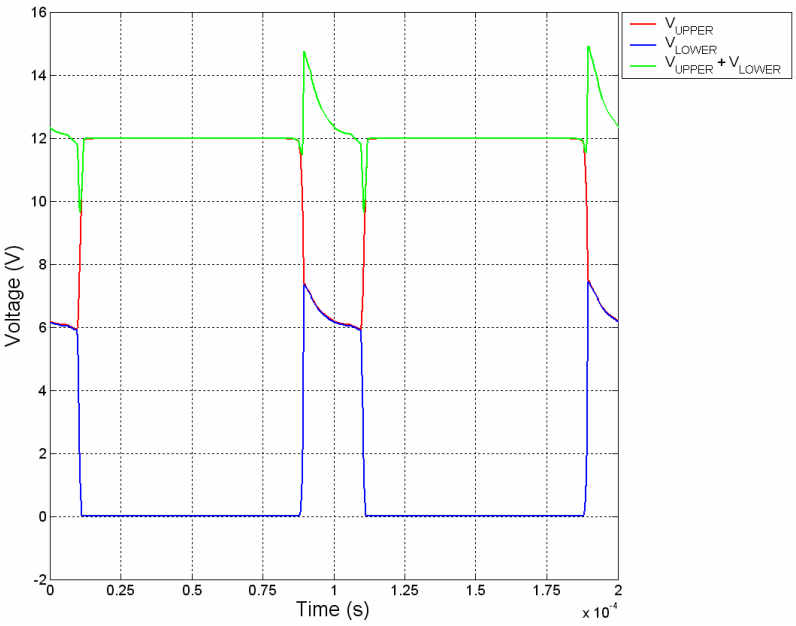

Figure 53: Simulation - Double MOSFET switching without regulator and with single gate resistance 100Ω - V_{UPPER}, V_{LOWER} and V_{UPPER}+ V_{LOWER}

5.1.2.3 Polarized resistance set-up in the gate

The next simulation results correspond to the circuit presented in Figure 54 with the following parameters:

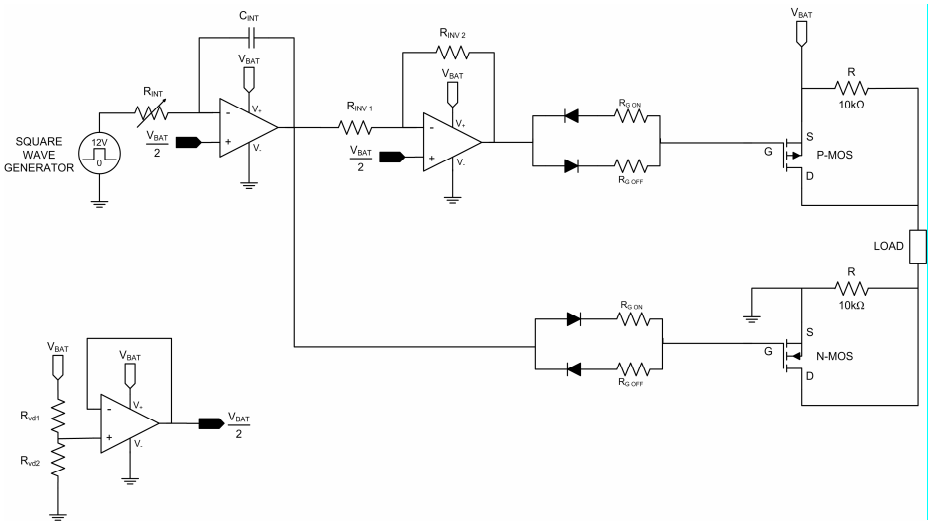

Figure 54: Double MOSFET switching without regulator and with polarized resistance set-up in the gate

- V_{SQW}=12V;
- F_{SQW}=10kHz, duty cycle =0.5;
- V_{BAT}=12V;
- R_{INT}=3810Ω;
- C_{INT}=4.7nF;
- $R_{INV\ 1}$=$R_{INV\ 2}$=10kΩ;
- R_{LOAD}=47Ω;
- P-MOS: $R_{G\ ON}$=$R_{G\ OFF}$=100Ω;
- N-MOS: $R_{G\ ON}$=200Ω, $R_{G\ OFF}$=130Ω.

In this simulation the polarized resistance set-up was introduced to reduce the difference in turn-on and turn-off when comparing the N-MOS with the P-MOS. The choice of the gate resistance was made by fixing the values of gate resistance for the P-MOS, once it is the master MOSFET, and changing the values of gate resistances for the N-MOS until the circuit simulation gives the best results.

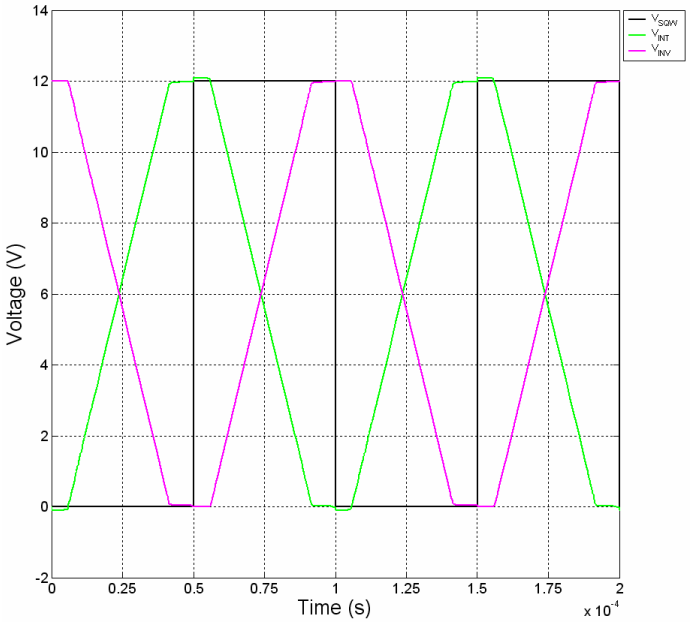

Figure 55: Simulation - Double MOSFET switching without regulator and with polarized resistance set-up – V_{SQW}, V_{INT} and V_{INV}

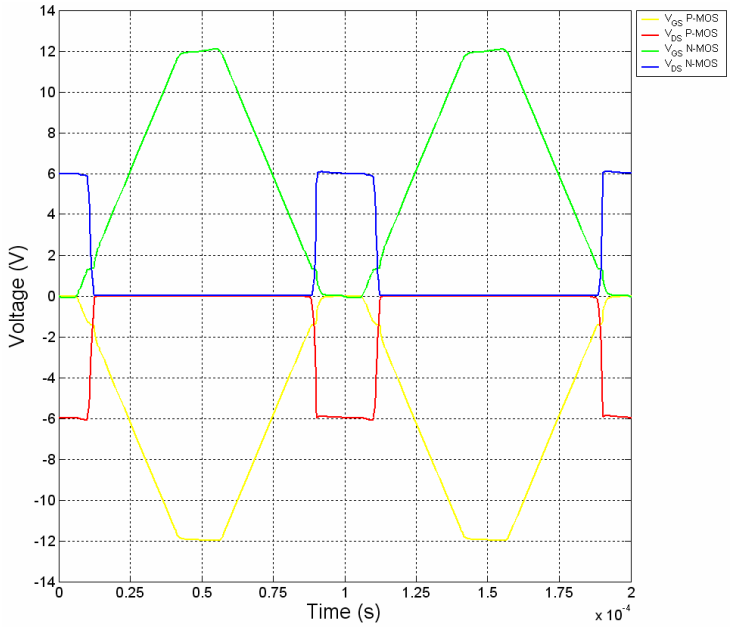

Figure 56: Simulation - Double MOSFET switching without regulator and with polarized resistance set-up – V_{GS} P-MOS, V_{DS} P-MOS, V_{GS} N-MOS and V_{DS} N-MOS

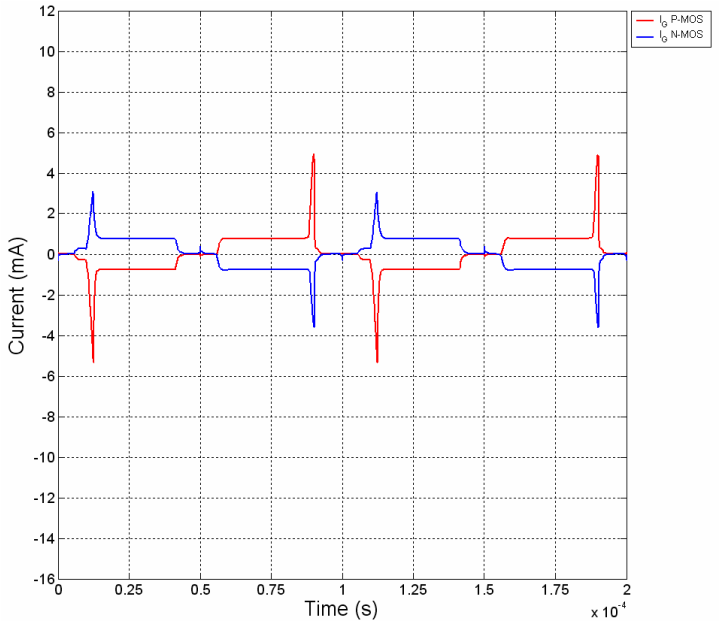

Figure 57: Simulation - Double MOSFET switching without regulator and with polarized resistance set-up – I_G P-MOS and I_G N-MOS

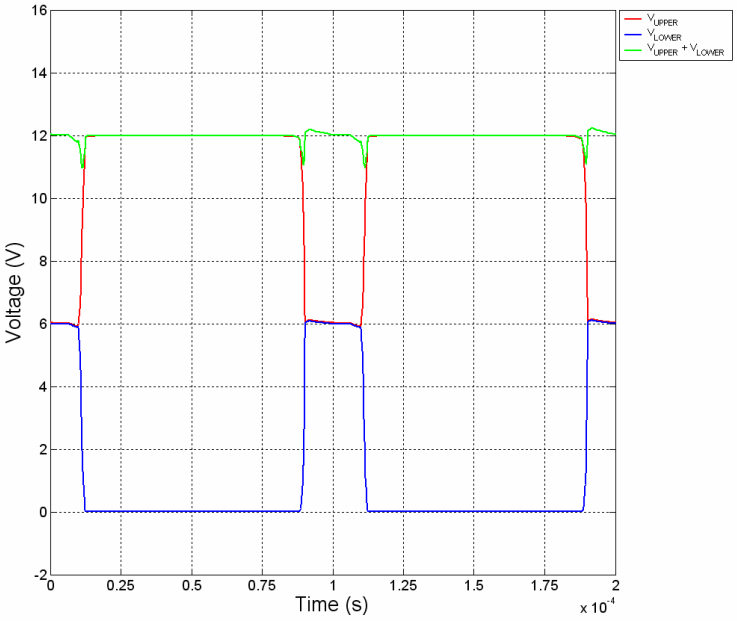

Figure 58: Simulation - Double MOSFET switching without regulator and with polarized resistance set-up - V_{UPPER}, V_{LOWER} and V_{UPPER}+ V_{LOWER}

5.1.3 Double MOSFET switching with regulator

5.1.3.1 Single gate resistance - 100Ω

The purpose of the following simulations is to verify how well the circuit with regulator performs with a single resistance in the gate. The simulated circuit is presented in Figure 59 with the parameters:

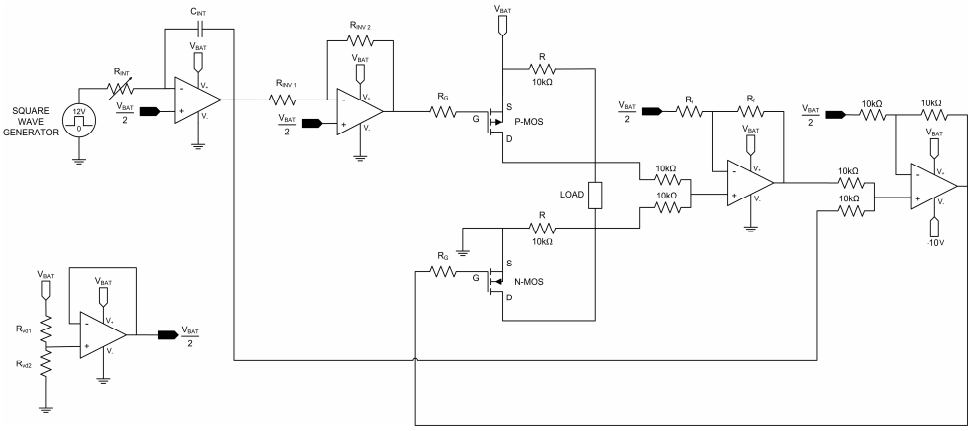

Figure 59: Double MOSFET switching with regulator

- V_{SQW}=12V;
- F_{SQW}=10kHz, duty cycle =0.5;
- V_{BAT}=12V;
- R_{INT}=3810Ω;
- C_{INT}=4.7nF;
- $R_{INV\ 1}$=$R_{INV\ 2}$=10kΩ;
- R_{LOAD}=47Ω;
- P-MOS R_G=100Ω;
- N-MOS R_G=100Ω;
- R_i=10kΩ;
- R_f=4890Ω.

The value of the P-regulator resistance R_f that is responsible for the gain of the regulator was adjusted observing the simulation that gave lowest error.

Similarly to the previous simulations, the following figures show the outputs of the integrator circuit and inverter circuit, the gate-source and drain-source voltages for both MOSFETS, the gate currents and the voltages over the load.

In Figure 61 and Figure 62 is important to observe that gate-source voltage and the gate current for the N-MOS have shapes that show the effect of the feedback regulation, by presenting small variations and oscillations when compared to the double MOSFET switching without regulator.

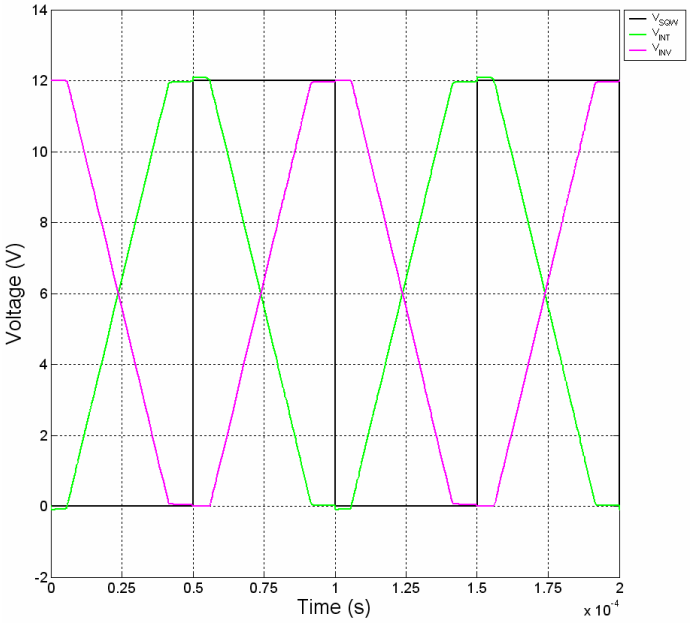

Figure 60: Simulation - Double MOSFET switching with regulator and with single gate resistance 100Ω – V_{SQW}, V_{INT} and V_{INV}

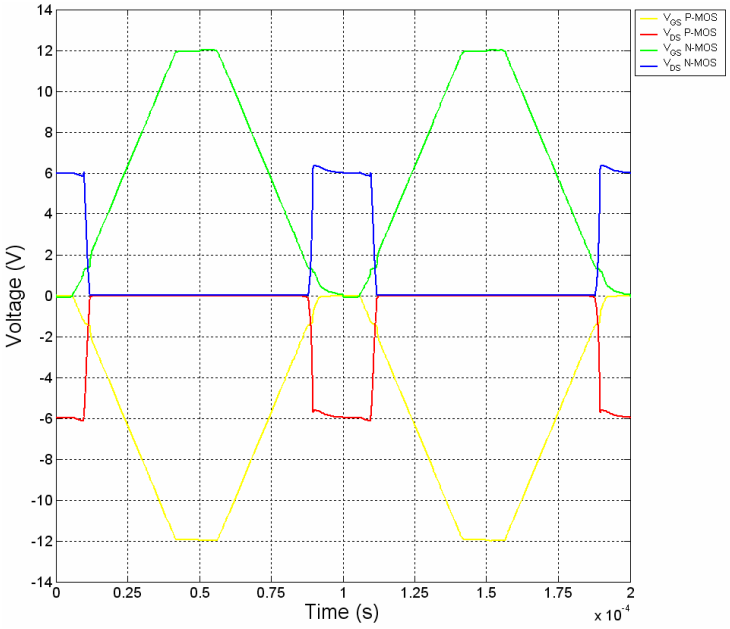

Figure 61: Simulation - Double MOSFET switching with regulator and with single gate resistance 100Ω – V_{GS} P-MOS, V_{DS} P-MOS, V_{GS} N-MOS and V_{DS} N-MOS

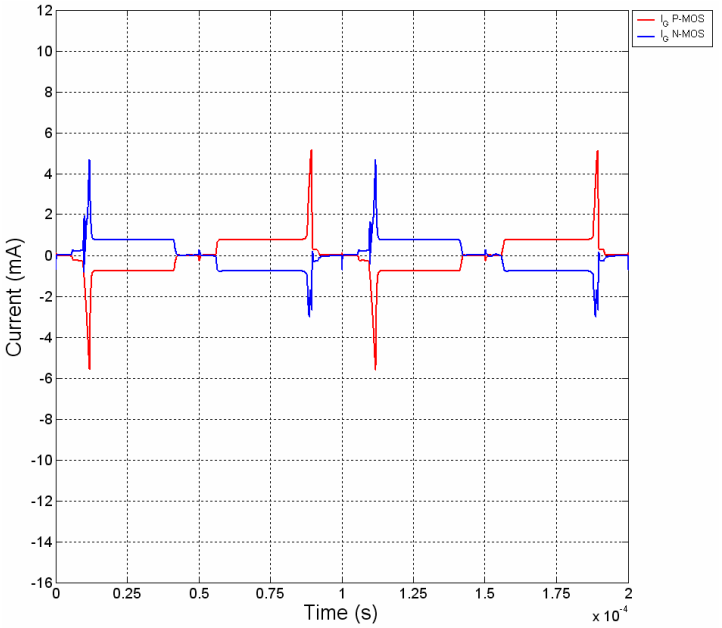

Figure 62: Simulation - Double MOSFET switching with regulator and with single gate resistance 100Ω – I_G P-MOS and I_G N-MOS

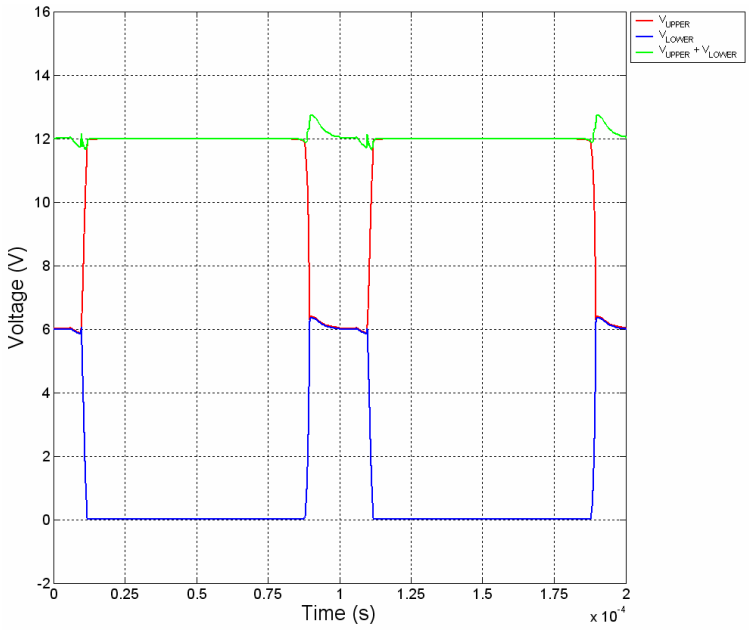

Figure 63: Simulation - Double MOSFET switching with regulator and with single gate resistance 100Ω - V_{UPPER}, V_{LOWER} and V_{UPPER}+ V_{LOWER}

5.1.3.2 Polarized resistance set-up in the gate

The next simulation results correspond to the circuit presented in Figure 64 with the following parameters:

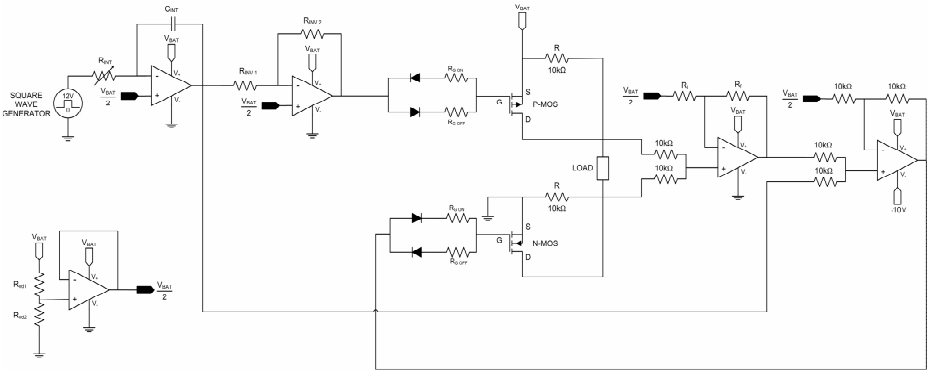

Figure 64: Double MOSFET switching with regulator and with polarized resistance set-up in the gate

- V_{SQW}=12V;
- F_{SQW}=10kHz, duty cycle =0.5;
- V_{BAT}=12V;
- R_{INT}=3810Ω;
- C_{INT}=4.7nF;
- $R_{INV\ 1}$=$R_{INV\ 2}$=10kΩ;
- R_{LOAD}=47Ω;
- P-MOS: $R_{G\ ON}$=$R_{G\ OFF}$=100Ω;
- N-MOS: $R_{G\ ON}$=200Ω, $R_{G\ OFF}$=130Ω;
- R_i=10kΩ;
- R_f=4890Ω.

The purpose of this simulation is to check if the addition of the polarized resistance set-up makes some considerable improvement in the double MOSFET switching circuit with regulator.

Similarly to the previous simulations, the following figures show square wave signal, the outputs of the integrator circuit and inverter circuit, the gate-source and drain-source voltages for both MOSFETS, the gate currents and the voltages over the load.

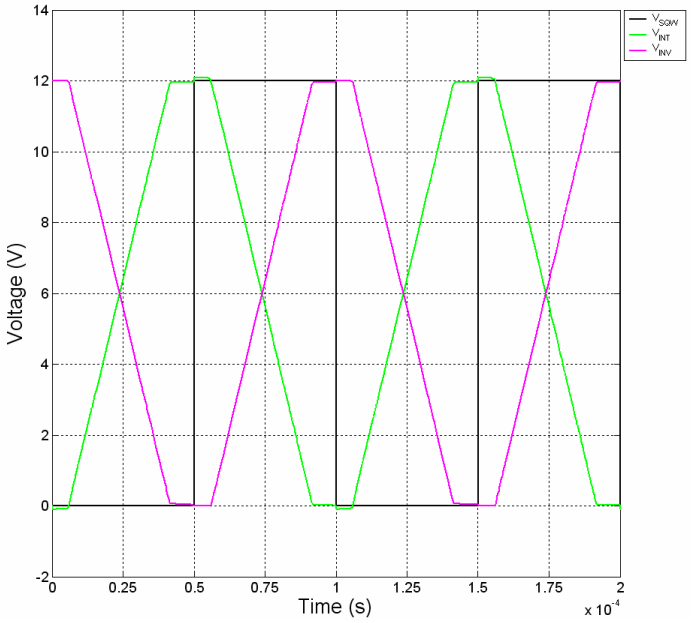

Figure 65: Simulation - Double MOSFET switching with regulator and with polarized resistance set-up – V_{SQW}, V_{INT} and V_{INV}

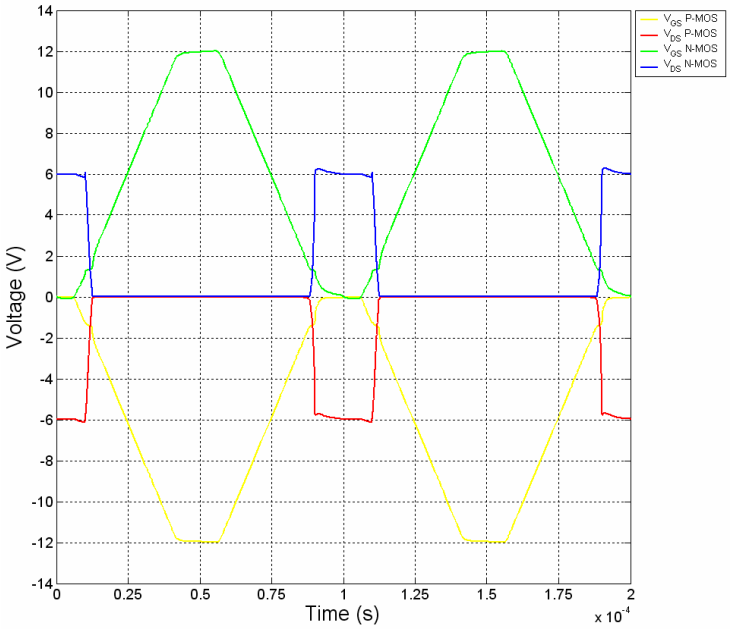

Figure 66: Simulation - Double MOSFET switching with regulator and with polarized resistance set-up – V_{GS} P-MOS, V_{DS} P-MOS, V_{GS} N-MOS and V_{DS} N-MOS

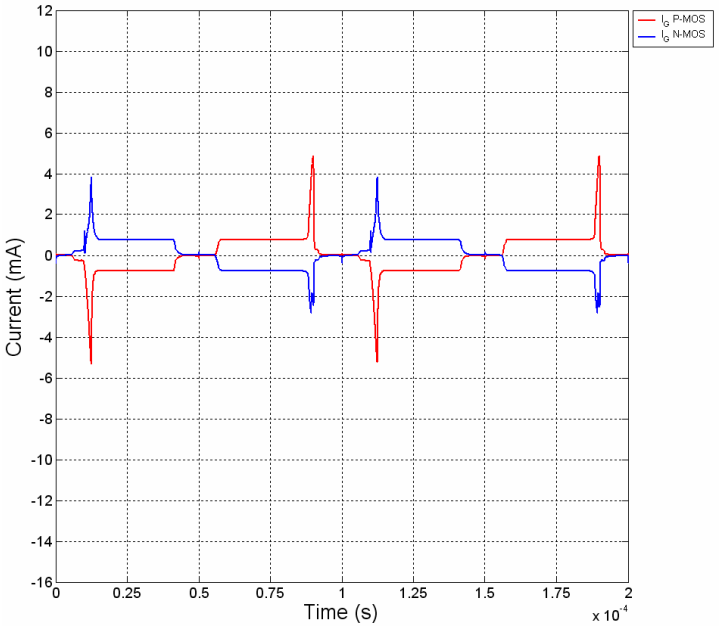

Figure 67: Simulation - Double MOSFET switching with regulator and with polarized resistance set-up – I_G P-MOS and I_G N-MOS

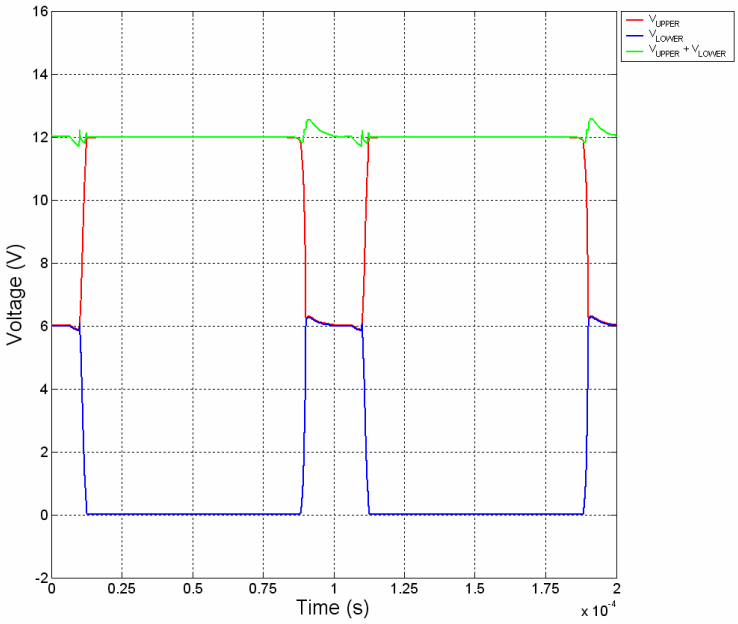

Figure 68: Simulation - Double MOSFET switching with regulator and with polarized resistance set-up - V_{UPPER}, V_{LOWER} and V_{UPPER}+ V_{LOWER}

5.1.4 Comparison between the simulated circuits

Figure 69 shows the comparison of the sum of V_{UPPER} and V_{LOWER} for all previously simulated circuits (except the circuit without regulator and with 5Ω as gate resistance).

In this figure it is possible to observe that the insertion of the polarized resistance set-up and the regulator greatly improves the behaviour of the circuit, by approximating the sum of V_{UPPER} and V_{LOWER} to a DC level.

As expected, the best circuit setup is the one containing both the polarized resistance set-up and the regulator, although it does not differ significantly from the configuration with single gate resistance and regulator.

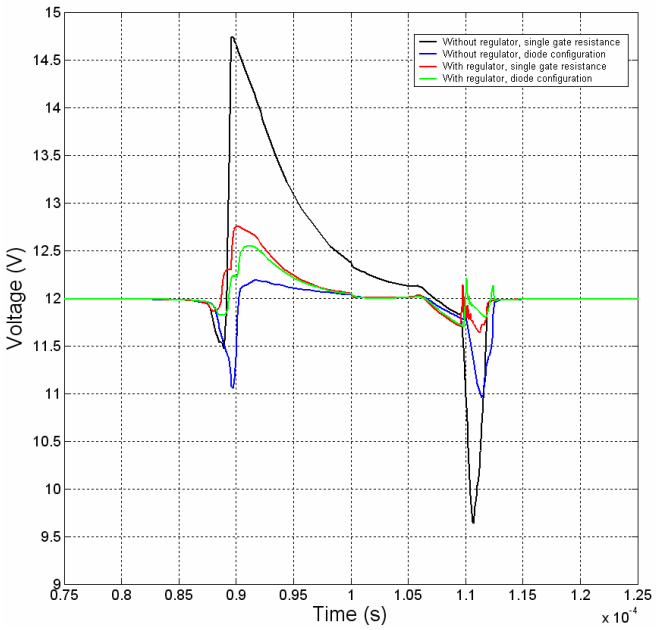

Figure 69: Comparison between the simulated circuits, zoom of V_{UPPER}+V_{LOWER}

5.2 Measurements

For comparison purposes, the measurements performed in the PCBs were done with the same parameters of the simulations. Figure 70 shows the arrangement of the equipment used for the measurements. The measurements results were taken from the oscilloscope as a “csv” file and were plotted using MATLAB for further analysis.

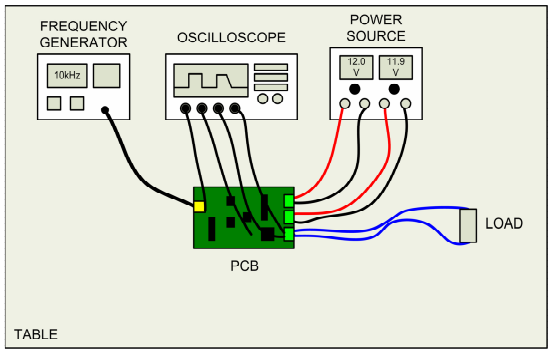

Figure 70: Arrangement of the equipment for the measurements

The following items present the measurement results of the single MOSFET switching circuit and the double MOSFET switching circuit with polarized resistance set-up and with regulator, which is the circuit that shows the best simulation results.

5.2.1 Single MOSFET switching

Similarly to the simulations, the following figures show the square wave, the output of the integrator circuit, the gate-source and drain-source voltages; the voltages over the load and the summation of them. The gate-current was measured by taking the voltage across the gate resistance, but, as its value was too low, with the same amplitude of the usual noise present in oscilloscope measurements, it was excluded from the measurements results

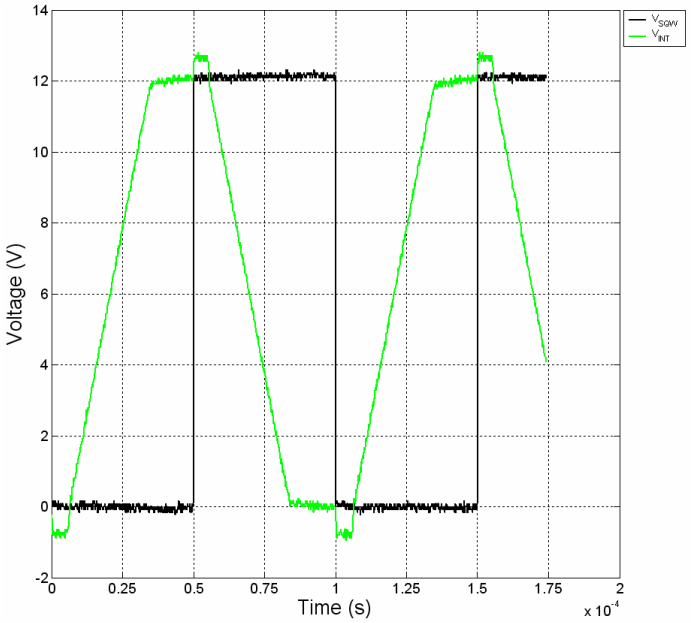

Figure 71: Measurement - Single MOSFET switching - V_{SQW} and V_{INT}

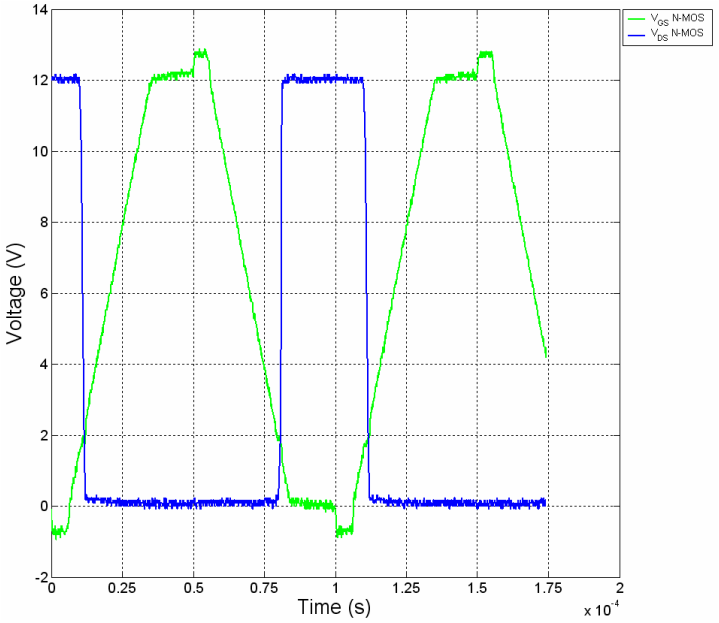

Figure 72: Measurement - Single MOSFET switching - V_{GS} and V_{DS}

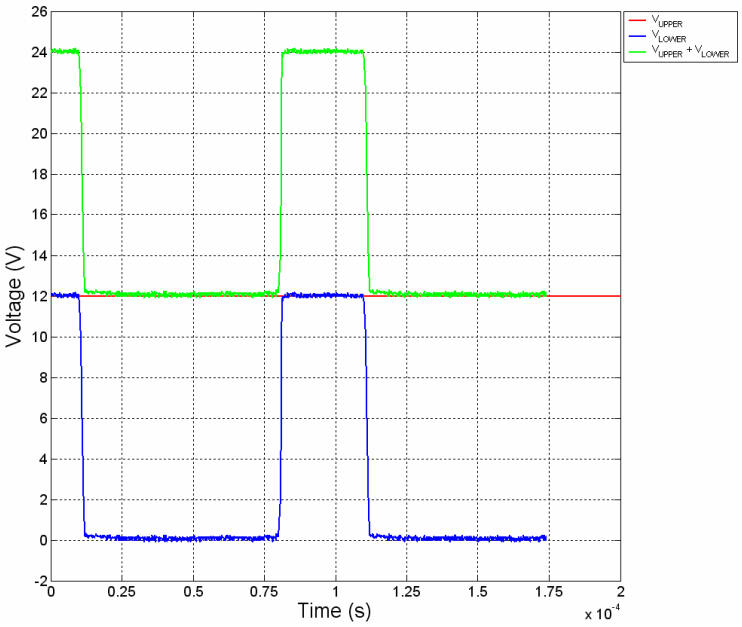

Figure 73: Measurement - Single MOSFET switching - V_{UPPER}, V_{LOWER} and V_{UPPER}+V_{LOWER}

5.2.2 Double MOSFET switching with regulator and polarized resistance set-up in the gate

The following figures show the measured square wave signal, the outputs of the integrator circuit and inverter circuit, the gate-source and drain-source voltages for both MOSFETS, the voltages over the load and the summation of them. For the same reason as exposed in the previous section, the gate-current was excluded from the measurements.

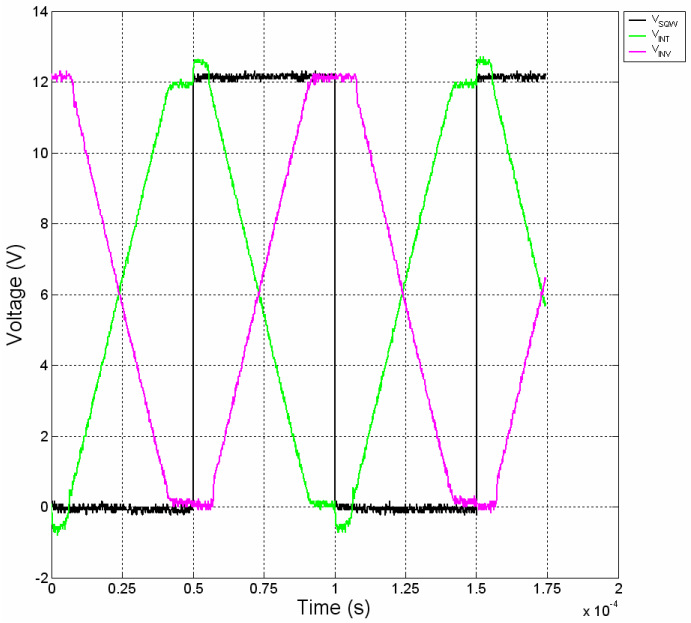

Figure 74: Measurement - Double MOSFET switching with regulator and with polarized resistance set-up – V_{SQW}, V_{INT} and V_{INV}

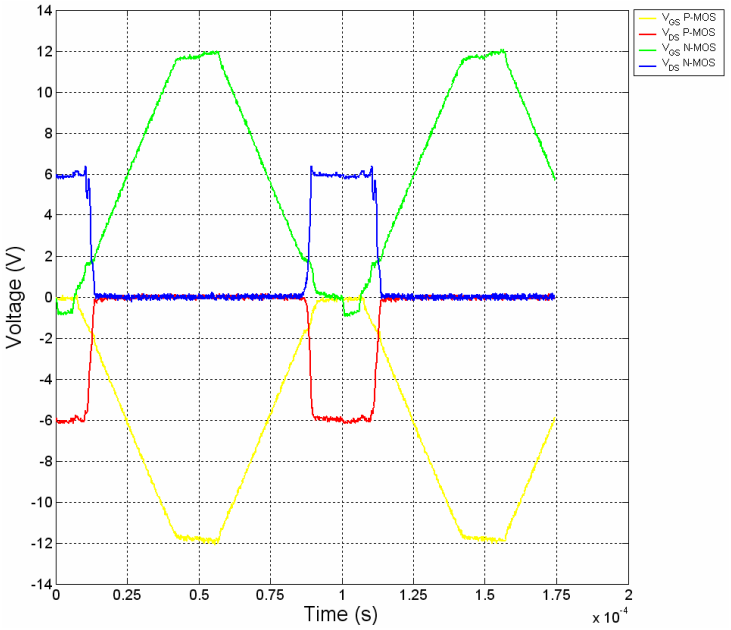

Figure 75: Measurement - Double MOSFET switching with regulator and with polarized resistance set-up – V_{GS} P-MOS, V_{DS} P-MOS, V_{GS} N-MOS and V_{DS} N-MOS

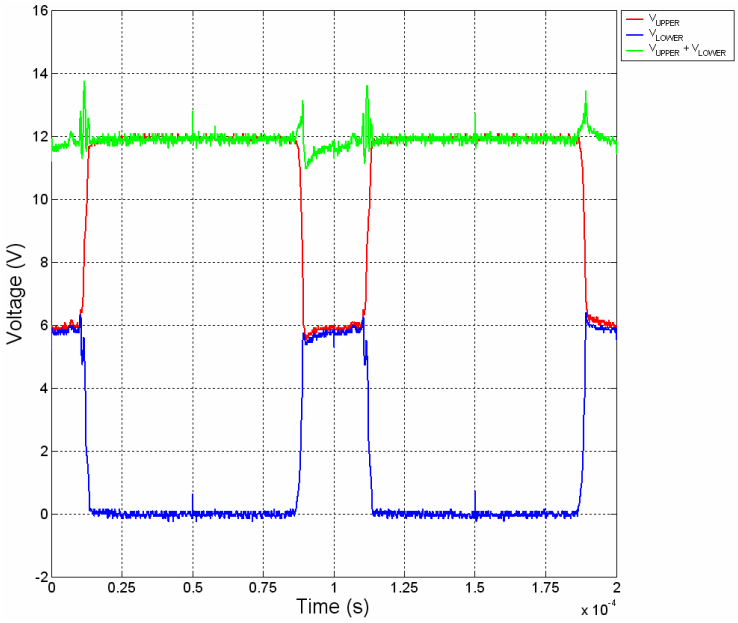

Figure 76: Measurement - Double MOSFET switching with regulator and with polarized resistance set-up - V_{UPPER}, V_{LOWER} and V_{UPPER}+ V_{LOWER}

5.3 Comparison between measured and simulated results

As stated before, the simulation and measurements were done using the same parameters such as resistors, capacitors values, switching frequency, etc.

In order to verify how well the simulation model of the single MOSFET switching and double MOSFET switching with regulator and with polarized resistance set-up in the gate correspond to the real circuit (and vice-versa), both measurements and simulations, were plotted together, with the same time scale.

The way to adjust both measurements and simulations to the same time scale was to define the square-wave input as a reference signal and apply a time-delay in the measured values that superimpose perfectly the measured square-wave to the simulated one.

In the following plots, the “noisy” curves correspond to the measurement results and the “clean” curves; obviously correspond to the simulation results.

5.3.1 Single MOSFET switching

The following figures show the measured and simulated square wave signals, the output of the integrator circuits, the gate-source and drain-source voltages, the voltages over the load and the summation of them.

In Figure 77, one can observe a larger undershoot in the measured integrator output voltage and a small time delay, of approximately 1µs, between the measured and simulated integrator output voltage. These differences are probably due to small differences between the operational amplifier SPICE model and the real operational amplifier.

In Figure 78, there is a much larger time delay during turn-off between the measured and simulated drain-source voltage, which obviously reflects in the same time delay in V_{LOWER} and $V_{UPPER}+V_{LOWER}$, as seen in Figure 79.

Taking a closer look at the turn-off region of Figure 78, it is possible to notice that, in the measured curves, the drain-source voltage starts to rise when the gate-source voltage has a higher value, compared to the simulated curves. Then, one can assume that the reason for the time delay is related to difference in the gate-source threshold voltage between the real MOSFET and the SPICE MOSFET model.

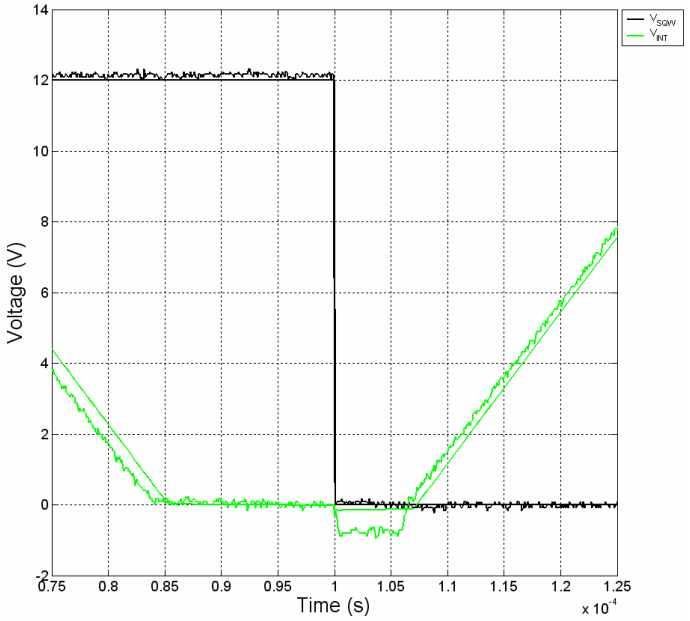

Figure 77: Comparison - Single MOSFET switching - V_{SQW} and V_{INT}

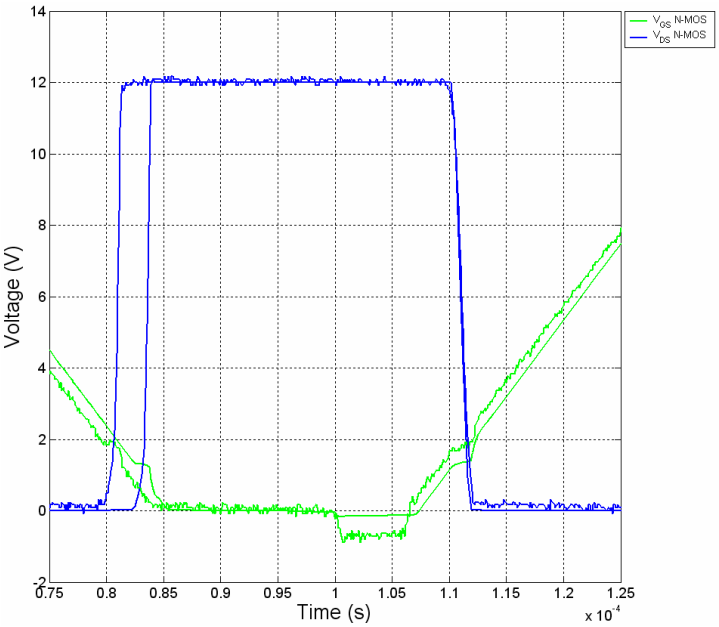

Figure 78: Comparison - Single MOSFET switching - V_{GS} and V_{DS}

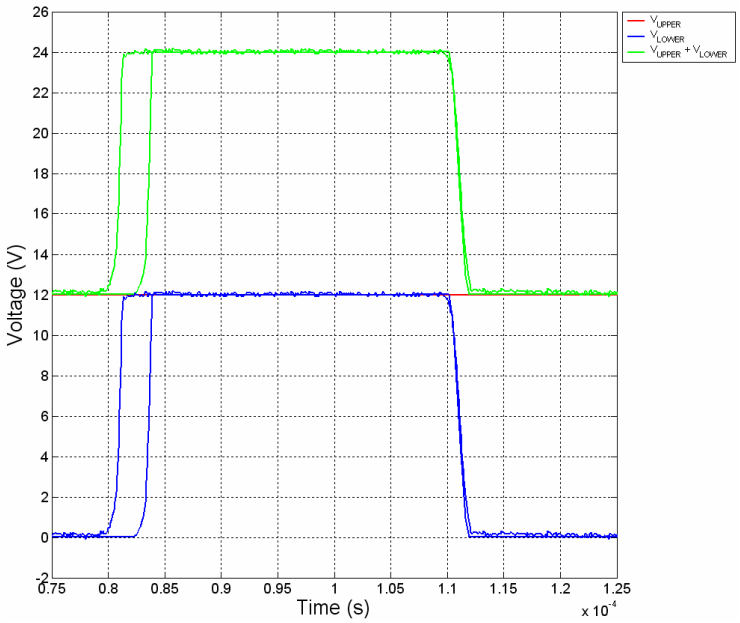

Figure 79: Comparison - Single MOSFET switching - V_{UPPER}, V_{LOWER} and V_{UPPER}+V_{LOWER}

5.3.2 Double MOSFET switching with regulator and polarized resistance set-up in the gate

Similarly to the single MOSFET switching, the following figures show the measured and simulated square wave signals, the output of the integrator and inverter circuits, the gate-source and drain-source voltages of both MOSFETs, the voltages over the load and the summation of them.

As seen in single MOSFET switching case, the integrator circuit output presents a larger undershoot in the measured values and there is also a time delay between the simulated and measured curves.

The most important observation is, in Figure 82, the measured summation of V_{UPPER} and V_{LOWER}, has a much stronger oscillatory behaviour than the simulation. These oscillations are probably related to the differences between the regulator's operational amplifiers SPICE model and real regulator's operational amplifier.

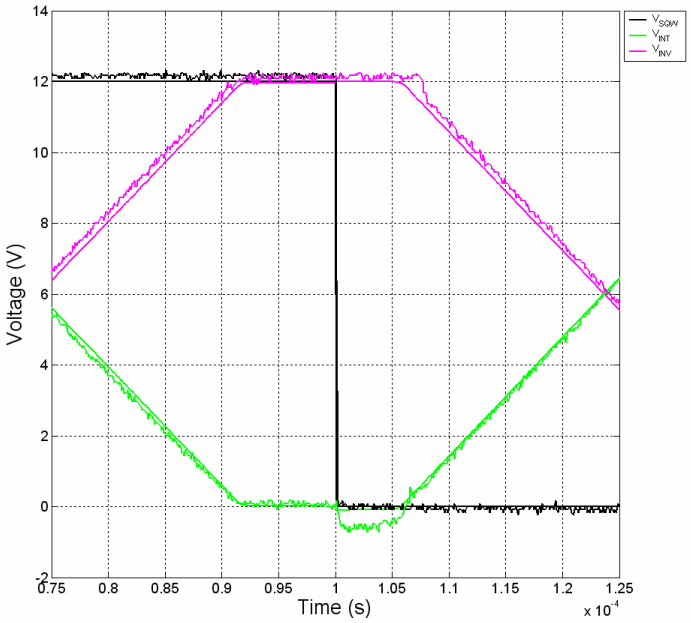

Figure 80: Comparison - Double MOSFET switching with regulator and with polarized resistance set-up – V_{SQW}, V_{INT} and V_{INV}

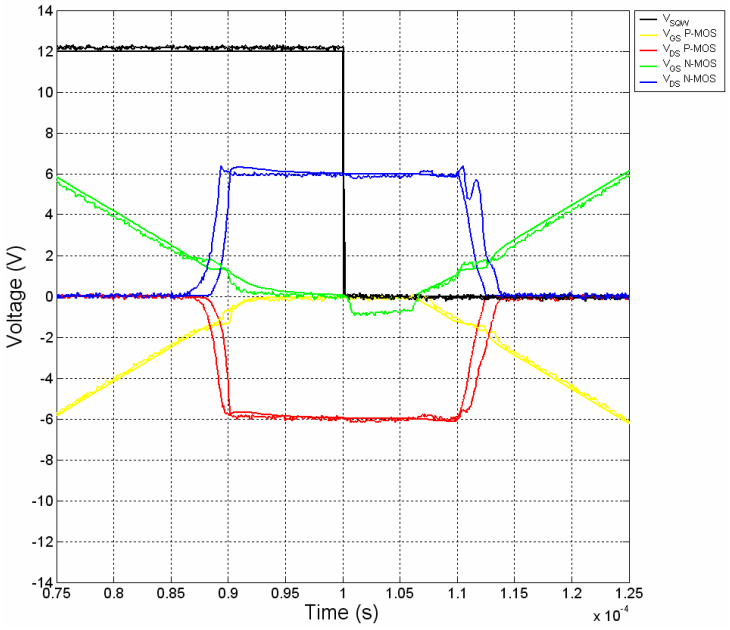

Figure 81: Comparison - Double MOSFET switching with regulator and with polarized resistance set-up – V_{GS} P-MOS, V_{DS} P-MOS, V_{GS} N-MOS and V_{DS} N-MOS

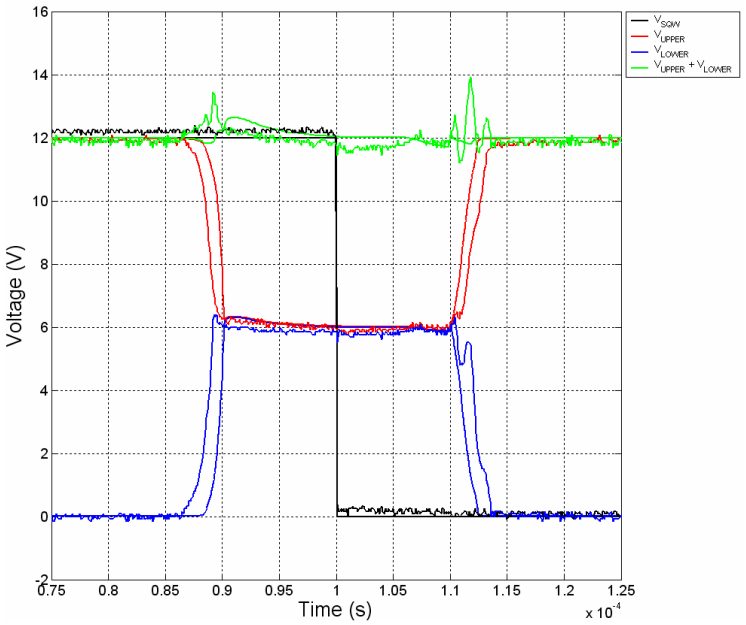

Figure 82: Comparison - Double MOSFET switching with regulator and with polarized resistance set-up - V_{UPPER}, V_{LOWER} and V_{UPPER}+ V_{LOWER}

5.4 Comparison between the emission levels

In order to verify the expected frequency content of the radiated emissions in the wires when comparing the double MOSFET switching and the single MOSFET switching configuration, the FFT of the sum of V_{UPPER} and V_{LOWER} for the measured and simulated configuration were calculated in MATLAB and plotted in the figures bellow.

Figure 83 and Figure 84 show the magnitude of the calculated FFT components expressed in volts while Figure 85 and Figure 86 shows the magnitude of the FFT components expressed in dBV.

As expected, the double MOSFET switching presents lower magnitudes in the FFT components in the frequency range from 10 kHz up to 0.5 MHz, compared to the single MOSFET switching, indicating that the double MOSFET switching is a viable alternative to reduce radiated emissions on the wires between DC/DC converter and the load when they are distant from each other.

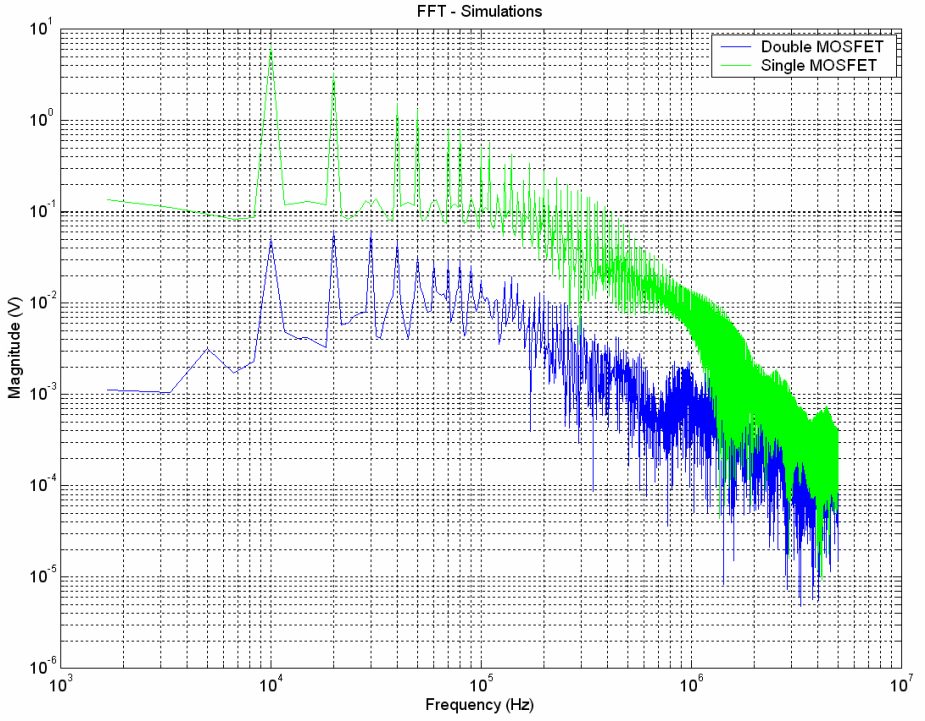

Figure 83: $V_{UPPER}+V_{LOWER}$ FFT magnitude expressed in volts - Simulations

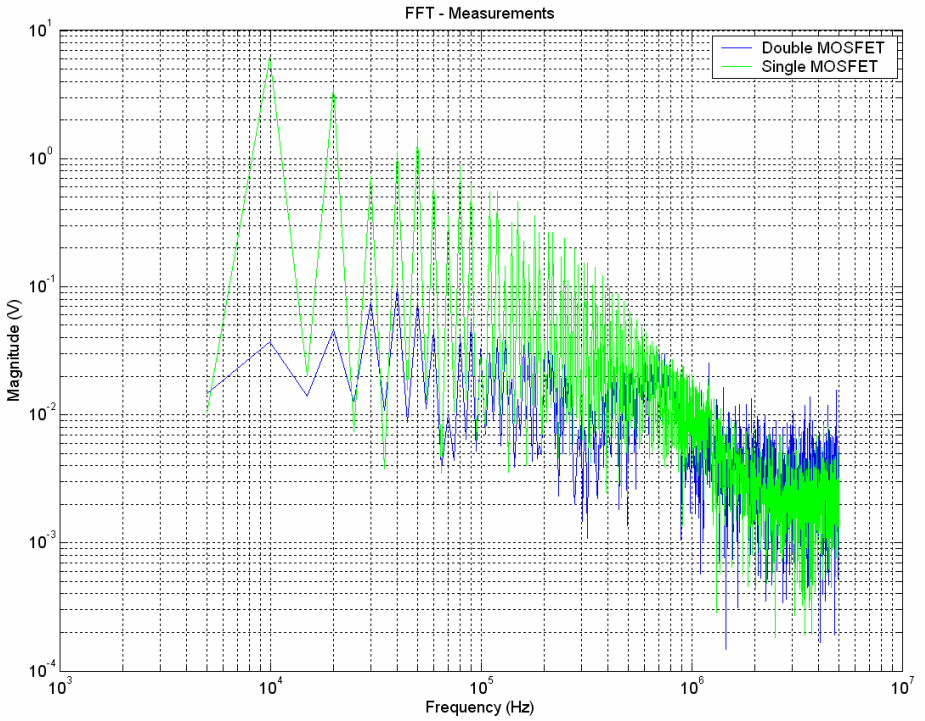

Figure 84: $V_{UPPER}+V_{LOWER}$ FFT expressed in volts - Measurements

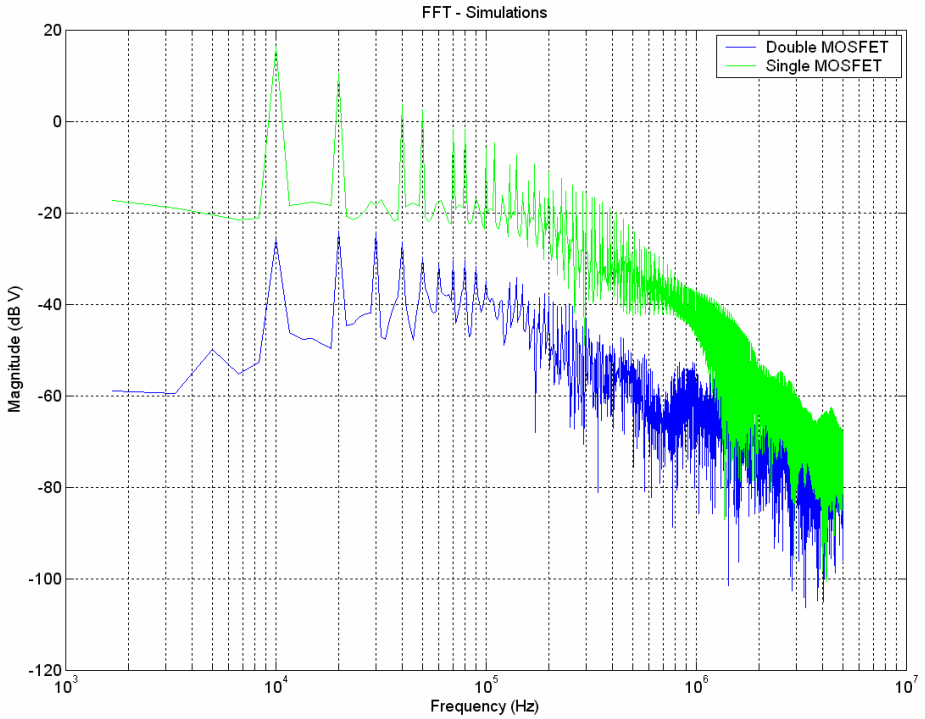

Figure 85: $V_{UPPER}+V_{LOWER}$ FFT magnitude expressed in dBV - Simulations

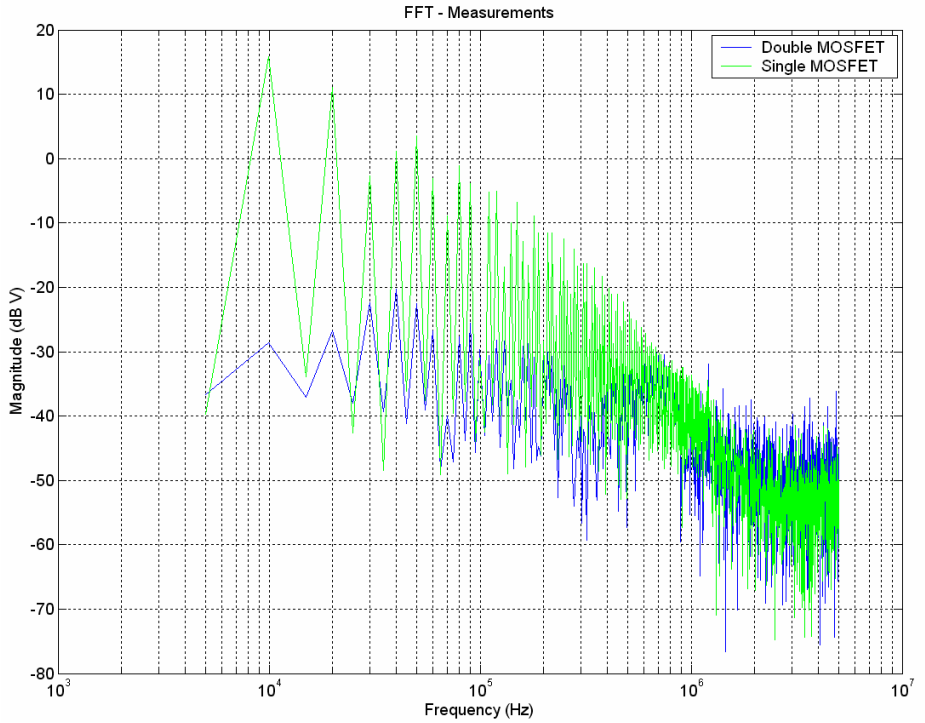

Figure 86: $V_{UPPER}+V_{LOWER}$ FFT magnitude expressed in dBV - Measurements

6 Conclusions

In this thesis work, the principle that it is possible to reduce the radiated emission from the wires between the DC/DC converter and the load by applying the double MOSFET switching technique was verified, giving satisfactory results.

From the simulation results in the double MOSFET switching design process, it was possible to draw several conclusions. The use of a too small gate resistance introduces oscillations in the input signal for the MOSFET, leading to a deteriorated performance of the circuit. This problem could be solved by simply increasing the gate resistance, but then the turn-on and turn-off times of the MOSFETs became slower. The introduction of the polarized resistance set-up in the gate, as well as the introduction of the P-regulator, contributes enormously to a good performance of the circuit, although the combination of polarized resistance set-up and regulator does not improve very much when compared to the configuration with single resistance and regulator.

After achieving good simulation results, a surface-mounted printed circuit board was constructed in such a way that several configurations of the circuit could be tested with different parameters. The board seemed to be well designed, except for one problem, which was that the PCB's copper traces from the MOSFETs to the load connector should be thicker, so the PCB would be able to handle currents higher than 1A.

There are some observations regarding the comparison between measurements in the PCB and simulations. During the circuit design, there was an important concern in choosing a MOSFET that had a SPICE model matching the real device; however, the measurements proved that the limited device for the chosen operation conditions was not the MOSFET, but the operational amplifier. The chosen operational amplifier was the cause of most discrepancies between the measurements and simulation results. As a further improvement, an operational amplifier that has a model that corresponds better to the reality should be used.

Finally, when comparing the FFT results of the sum of voltage over the load for the double MOSFET switching and single MOSFET switching, it is possible to conclude that the double MOSFET switching might emit in lower levels than the single MOSFET especially in the frequency range of 10 kHz to 0.5 MHz. Even though the designed circuit presents a much better behaviour when compared to the single MOSFET switching, there are several limitations to be considered and improvements to be done. Other configuration of regulator could be tested, and analysis regarding to the variation of load and voltage levels should be done.

7 References and list of literature

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8 Appendix – IRF 7307 SPICE model

```
.SUBCKT irf7307n 1 2 3
**************************************
*      Model Generated by MODPEX     *
*Copyright(c) Symmetry Design Systems*
*         All Rights Reserved        *
*    UNPUBLISHED LICENSED SOFTWARE   *
*   Contains Proprietary Information *
*      Which is The Property of      *
*     SYMMETRY OR ITS LICENSORS      *
*Commercial Use or Resale Restricted *
*   by Symmetry License Agreement    *
**************************************
* Model generated on May  7, 01
* MODEL FORMAT: SPICE3
* Symmetry POWER MOS Model (Version 1.0)
* External Node Designations
* Node 1 -> Drain
* Node 2 -> Gate
* Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM NMOS LEVEL=1 IS=1e-32
+VTO=1.24972 LAMBDA=0.0183892 KP=65.9883
+CGSO=5.48064e-06 CGDO=1.00043e-11
RS 8 3 0.0259771
D1 3 1 MD
.MODEL MD D IS=2.49819e-08 RS=0.0736216 N=1.5 BV=20
+IBV=0.00025 EG=1 XTI=4 TT=0.0001
+CJO=5.40605e-10 VJ=0.5 M=0.373666 FC=0.5
RDS 3 1 1e+06
RD 9 1 0.00117609
RG 2 7 9.36243
D2 4 5 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=8.05104e-10 VJ=0.5 M=0.523292 FC=1e-08
D3 0 5 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.4 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 1.72861e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
* Default values used in MD3:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.4
.ENDS irf7307n
```

```
.SUBCKT irf7307p 1 2 3
**************************************
*      Model Generated by MODPEX     *
*Copyright(c) Symmetry Design Systems*
*         All Rights Reserved        *
*    UNPUBLISHED LICENSED SOFTWARE   *
*   Contains Proprietary Information *
*      Which is The Property of      *
*     SYMMETRY OR ITS LICENSORS      *
*Commercial Use or Resale Restricted *
*   by Symmetry License Agreement    *
**************************************
* Model generated on May  7, 01
* MODEL FORMAT: SPICE3
* Symmetry POWER MOS Model (Version 1.0)
* External Node Designations
* Node 1 -> Drain
* Node 2 -> Gate
* Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM PMOS LEVEL=1 IS=1e-32
+VTO=-1.2365 LAMBDA=0 KP=13.3782
+CGSO=4.57456e-06 CGDO=1e-11
RS 8 3 0.0342305
D1 1 3 MD
.MODEL MD D IS=7.42493e-09 RS=0.0344217 N=1.5 BV=20
+IBV=0.00025 EG=1.2 XTI=1.64903 TT=3.31943e-14
+CJO=6.52964e-10 VJ=0.5 M=0.457429 FC=0.5
RDS 3 1 1e+06
RD 9 1 0.0141686
RG 2 7 5.48635
D2 5 4 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=1.79577e-09 VJ=1.09807 M=0.9 FC=9.99999e-09
D3 5 0 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=1 RS=2.99895e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 1.79577e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 6 0 MD3
* Default values used in MD3:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=1
.ENDS irf7307p
```