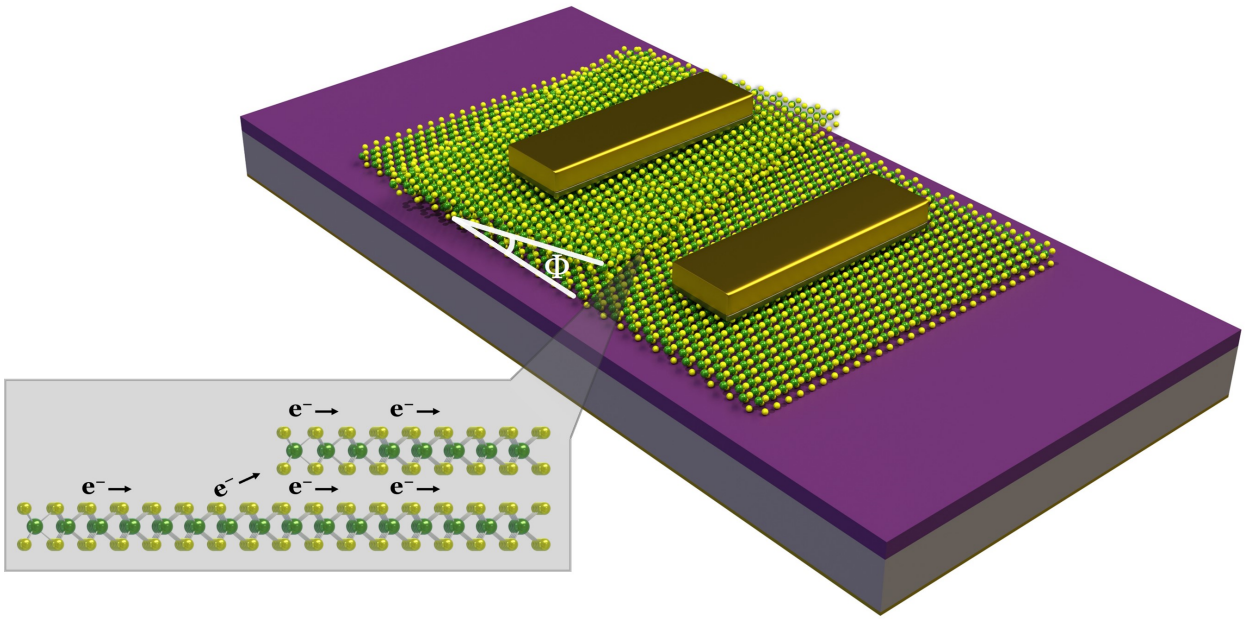
CHALMERS
UNIVERSITY OF TECHNOLOGY



Electronic Transport Measurements of Two-Dimensional Semiconductor Homostructures

Charge Transport Across Twisted Monolayer-Bilayer WS_2-Homojunctions

Master's thesis in Nanotechnology

JONATHAN BLOMQVIST

DEPARTMENT OF MICROTECHNOLOGY AND NANOSCIENCE
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2024
www.chalmers.se

Master's thesis 2024

Electronic Transport Measurements of Two-Dimensional Semiconductor Homostructures

Charge Transport Across Twisted Monolayer-Bilayer WS_2-Homojunctions

JONATHAN BLOMQVIST

CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Microtechnology and Nanoscience
Quantum Device Physics Laboratory
Chalmers University of Technology
Gothenburg, Sweden 2024

Electronic Transport Measurements of Two-Dimensional Semiconductor Homostructures
Charge Transport Across Twisted Monolayer-Bilayer WS_2-Homojunctions
JONATHAN BLOMQVIST

Examiner & Supervisor: Saroj Prasad Dash, Department of Microtechnology and Nanoscience

Master's Thesis 2024
Department of Microtechnology and Nanoscience
Quantum Device Physics Laboratory
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover: Twisted 2D WS_2 field-effect transistor containing a bilayer-monolayer homojunction.

Typeset in LaTeX
Printed by Chalmers Reproservice
Gothenburg, Sweden 2024

Electronic Transport Measurements of Two-Dimensional Semiconductor Homostructures
Charge Transport Across Twisted Monolayer-Bilayer WS_2-Homojunctions
JONATHAN BLOMQVIST
Department of Microtechnology and Nanoscience
Chalmers University of Technology

Abstract

The ever-increasing demand for emerging technologies requires advancements in semiconductor devices beyond what is hitherto envisaged. Two-dimensional (2D) semiconductors have recently gained considerable attention for field-effect transistor technologies. However, there are various challenges regarding the growth of 2D semiconductors and the optimisation of their channel properties.

Specifically, the growth of 2D semiconductors by chemical vapour deposition (CVD) can result in bilayer patches and twisted layered structures, leading to the formation of homojunctions. These homojunctions may exhibit non-uniform charge transport due to various growth-related defects. Therefore, it is imperative to investigate charge transport across such homojunctions in 2D semiconductor field-effect transistor devices.

In this thesis, charge transport across monolayer-bilayer homojunctions in twisted 2D WS_2-homostructures is demonstrated. Devices were fabricated from WS_2 flakes containing monolayer-bilayer junctions with twist angles of 0° and 60°. Transport measurements conducted at room temperature revealed rectifying behaviour across monolayer-bilayer WS_2-homojunctions. This rectifying behaviour is attributed to the different band gaps and work functions of monolayer WS_2 and bilayer WS_2. Additionally, it is likely that intrinsic defects around the nucleation site, originating from the CVD growth, increased the doping concentration in the bilayer region. Together, these factors affect the charge transport across the homojunctions and result in the observed diodic behaviour.

These findings contribute to a deeper understanding of the physics of 2D semiconductor devices, thereby highlighting the pivotal role of these devices in shaping future technological developments.

Keywords: Transport measurements, Charge transport, Twistronics, WS_2, CVD, 2D TMD FET.

Acknowledgements

The work presented in this thesis has been made possible by the continuous guidance and help that I have received from so many people. Thanking each one of them as fully as they deserve would require more pages than what is written below. Nonetheless, I want to extend my sincerest gratitude and appreciation to these brilliant people without whom this thesis could not have been completed.

First and foremost, my deepest thanks to my examiner and supervisor, Professor Saroj Prasad Dash. Your door was always open for me when I had questions, and you answered each one of them in a way that demonstrated your vast knowledge and calmness, providing me with constant reassurance throughout my thesis work. Despite your numerous responsibilities, you always found time for me and continuously showed me unwavering support and patience. Thank you for that Saroj. I truly could not have asked for a better supervisor.

Secondly, I want to thank my practical supervisors, Roselle Ngaloy and Dr. Md Anamul Hoque. I appreciate your help during the fabrication process, with measurements, and for teaching me how to make fancy figures in Blender. I also want to thank Lars Sjöström and the other postdocs and PhD students in the department for your input and assistance.

I wish you all good luck and continued success in your academic careers.

Thank you to the other master's students in the open office landscape of QDP: Marcus, Enling and in particular my fellow 2D TMD investigators, Patrik and Krishna. Writing my thesis alongside you has been a pleasure. I value our productive discussions, and perhaps slightly more, our fun and non-productive conversations as we took breaks from desperately trying to produce good results.

Lastly, I want to thank my family and friends, especially my lovely Nindya, for always supporting me and for being by my side throughout these past months.

Tack till er alla!

Jonathan Blomqvist, Gothenburg, June 2024

Contents

1

Introduction

The rapid increase of smartphones, laptops, tablets, and similar devices serves as a hallmark of our technological achievement in recent decades. These devices have been seamlessly integrated into our daily lives and completely reshaped the way we communicate and interact with the world. A cornerstone of such innovations is the field-effect transistor (FET). Advancements in semiconducting technology, materials science, and fabrication techniques have been essential to downscale the size of transistors, in order to increase their capacity.

This downscaling is described by Moore's law, which predicts that the amount of transistors on a microchip doubles every two years, resulting in an increase in computation power [1]. It has held true for over half a century, enabling continuous development of electronic devices. Although transistor channel lengths have currently reached the nanoscale, attempts to further downscale the channel are met with challenges collectively termed short-channel effects (SCEs) [2]. Due to SCEs, devices demonstrate larger leakage currents, resulting in increased heat dissipation and ensuing energy losses [3].

Therefore, the research community has needed to expand its understanding and look for ways of combating these challenges. One such way is the use of two-dimensional (2D) materials [4, 5]. Graphene, transition metal dichalcogenides (TMDs), phosphorene, silicene and other 2D materials all possess ultrathin atomic structures. This unique characteristic confines charge carriers within a single layer and has been utilised in 2D transistors. The confinement of charge carriers to one layer effectively eliminates leakage currents, meaning that 2D transistors can be considered immune to SCEs present in conventional transistors [6]. This opens up for the possibility of continued downscaling of transistors, ultimately increasing capacity without any SCEs.

Regarding 2D materials, 2D TMDs, such as MoS_2, WSe_2 and WS_2, are of particular interest due to having a desirable bandgap, planar structures lacking dangling bonds, as well as mobilities comparable to Si [7–11]. Thus far, MoS_2 has received the most attention among 2D TMDs, with the first monolayer MoS_2 demonstrating an impressive I_{ON}/I_{OFF} of 10^8, mobility values of approx. 200 $cm^2\ V^{-1}\ s^{-1}$ (although this was revised downwards [12]) as well as a subthreshold swing (SS) close to the theoretical value of 60 mV dec^{-1} [5, 13]. This showcase of potential sparked an interest in conducting further research on 2D TMD transistors.

In addition to the inherent properties of 2D TMDs, emerging research has explored twistronics, which involves stacking layers of 2D materials with a twist angle between them [14]. Manipulating the relative orientation or twist angle between two or more layers induces a lattice mismatch, resulting in the formation of an interference pattern known as a moiré superlattice [15]. The presence of this superlattice has been found to significantly alter the electronic band structure of the stacked layers. Thus, by stacking layers with a twist angle, it becomes possible to tune the electronic properties of the structure and enhance its performance [11, 16–19].

The possibility of leveraging this to develop high-performance devices, in line with the historical trend of Moore's law, has recently sparked significant research interest [14, 20]. A critical aspect of this exploration involves understanding the impact of twist angles on the transport properties and behaviour of 2D TMD structures. However, several challenges accompany this pursuit. For instance, defects arising from the fabrication process may severely impact device performance and behaviour.

Addressing these challenges requires careful attention to the fabrication process to ensure good quality of the structure. Up until now, exfoliation has been widely used for fabricating TMDs [13, 21–23]. In contrast, chemical vapour deposition (CVD) has recently emerged as a promising alternative to obtain high-quality 2D TMD structures [24–26]. Although, the CVD growth of TMDs necessitates transferring the material from the growth substrate to a target substrate after fabrication. During this process, various extrinsic defects and contaminants from the external environment can affect device performance [27, 28]. Furthermore, during CVD growth, bilayer regions might naturally form at the nucleation site, resulting in a homojunction. Different intrinsic defects can occur during this process, potentially affecting the doping polarities of the different regions [29, 30]. Therefore, investigating the charge transport across CVD-grown homojunctions is of particular interest.

Thereby, this research aims to provide a foundation for further advancements in the field of nanoelectronics, by pursuing the following objectives: i) Fabricating angle-dependent 2D homostructures of CVD-grown WS_2, ii) Measuring the transport properties of the structure, and iii) Investigating charge transport across homojunctions. By addressing these aims, this master's thesis contributes to an increased understanding of the physics of angle-dependent 2D TMD homostructures and their electronic properties.

This thesis is structured accordingly: Chapter 2 provides an overview of the FET, explores 2D semiconductors, and delves into the field of twistronics, as well as the mechanisms of charge transport across homojunctions. Chapter 3 briefly explains the fabrication and measurement processes, with Chapter 4 presenting the results of transport measurements of WS_2-homostructures performed at room temperature. The results are followed by a summary and conclusions in Chapter 5. Lastly, detailed descriptions of the fabrication and measurement processes are provided in Appendices A and B respectively.

2

Theory

The physics of angle-dependent homostructures has recently gained considerable attention. Understanding its significance and potential for future applications requires a historical perspective on the field and its predecessors. This section aims to provide a foundational understanding of charge transport across homojunctions and twistronics. It will also explore the current state of the art upon which this thesis will build. First, the basic structure of a conventional enhancement-type Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is presented, together with key parameters of performance. Subsequently, short-channel effects associated with the downscaling of modern MOSFET technology are explained. Thereafter, two-dimensional (2D) semiconductors are introduced, with an emphasis on transition metal dichalcogenides (TMDs) and their desirable properties as well as challenges. Additionally, the field of twistronics is presented. An exploration of how properties change with a twist angle is provided alongside the current state of the art. Lastly, this section brings up charge transport across homojunctions, explaining how these junctions are formed during chemical vapour deposition (CVD) growth, as well as how various defects can impact charge transport across different layer regions.

2.1 Field-Effect Transistor

A conventional MOSFET, illustrated in Figure 2.1, consists of three terminals: source, drain, and gate [9, 31]. The gate terminal is isolated from the other two by an insulating layer. The source- and drain electrodes are highly doped with the same dopant type, while the body of the transistor has the opposite dopant type. Applying a voltage, denoted as V_g, to the gate terminal, generates an electric field that attracts minority carriers in the body. Eventually, these will accumulate at the interface between the body and the insulator, forming a channel between the source and the drain. A current, I_D, will start to flow along this channel when a voltage, denoted V_{ds}, is applied across the source- and drain terminals.

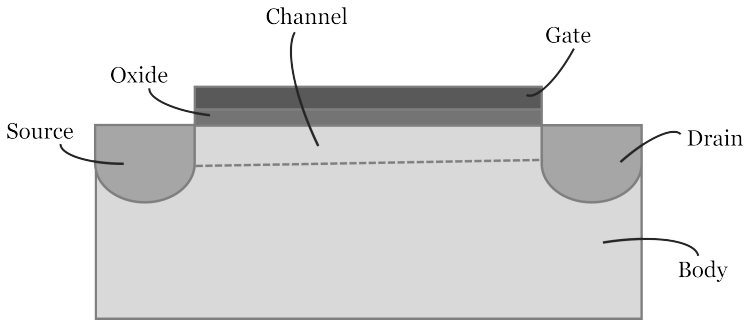


Figure 2.1: A schematic illustrating the structure of a conventional enhancement-type MOSFET.

2.1.1 Characteristics and Parameters of Performance

The performance and behaviour of a MOSFET can be understood through its I-V characteristics, namely output and transfer characteristics [32, 33]. Output characteristics involve measuring I_D over a range of V_{ds} sweeps for different V_g. Transfer characteristics are obtained by instead sweeping V_g at various V_{ds} while measuring I_D. Here, V_g is increased until a specific threshold voltage, V_{th}, is reached, after which the transistor turns on and starts to conduct current. The two ideal I-V curves are illustrated in Figure 2.2.

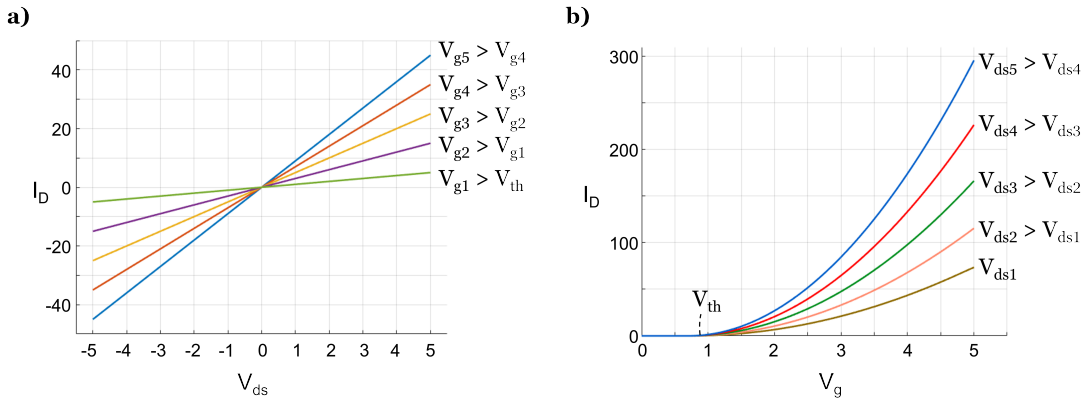


Figure 2.2: Ideal I-V characteristics of a MOSFET plotted in a linear scale. **a)** Output characteristics. Current increases linearly with V_{ds} for a specific V_g. Increasing the value of V_g results in an increasing flow of I_D. **b)** Transfer characteristics. V_g is increased until V_{th} is reached. The transistor then turns on and current starts to flow. Increasing V_{ds} also increases I_D at a specific V_g.

Several key parameters reflect the performance of the MOSFET, most of which can be acquired through the I-V characteristics above [33]. A parameter of great importance is the carrier mobility of the channel. The field-effect mobility, μ_{FE}, is a commonly used form of mobility and is calculated using the formula:

$$\mu_{FE} = \frac{L_{ch} \cdot g_m}{W_{ch} \cdot C_{ox} \cdot V_{ds}} \tag{2.1}$$

where L_{ch} is the channel length, g_m is the transconductance, W_{ch} is the channel

width, and C_{ox} is the capacitance of the oxide. The latter is calculated using the formula:

$$C_{ox} = \frac{\varepsilon_r \cdot \varepsilon_0}{t_{ox}} \tag{2.2}$$

where ε_r is the relative permittivity of the oxide, ε_0 is the permittivity of free space and t_{ox} is the thickness of the oxide [34].

Additionally, subthreshold swing (SS) relates to how fast the transistor switches between the on- and off-states [33]. More specifically, it represents the amount of voltage required to increase the current by one order of magnitude during the turn-on process. SS is obtained through the logarithmic scale of the transfer characteristics. By taking the derivative of I_D with respect to V_g followed by the inverse of this value, the minimum SS is acquired. Thereby, SS can be expressed using the following formula:

$$SS = \left(\frac{\partial(\log_{10} I_D)}{V_g} \right)^{-1} \tag{2.3}$$

I_{ON}/I_{OFF} is a ratio relating currents in the on- and off-states and indicates the modulation ability of V_g [33]. I_{ON} is determined as the highest current value of the transfer characteristics plotted in a logarithmic scale, while I_{OFF} is acquired by the mean value of the noise floor of the curve. Together, these currents give the I_{ON}/I_{OFF}. Lastly, V_{th} is the minimum amount of voltage required to turn on the transistor and can be extracted by identifying the tangent to the linear region of the transfer characteristics. The intersection of this tangent with the X-axis gives V_{th}.

2.1.2 Short-Channel Effects

The performance of MOSFETs is significantly affected by short-channel effects (SCEs) [3, 9, 35, 36]. The different doping polarities between the source and drain, compared to the body, create a pn-junction. For instance, in a MOSFET with a p-type substrate, where holes are the majority carriers and electrons are minority carriers, a pn-junction forms between the p-type substrate and the heavily doped n-type drain- and source electrodes. As electrons diffuse across the junction and recombine with holes, positive and negative ions are generated on the n- and p-sides, respectively. This leads to the formation of a depletion region, where no mobile charges exist due to the induced electric field in this region.

When scaling down the MOSFET to the point where the channel length becomes comparable to the widths of the depletion regions, these regions will begin to influence the behaviour of the channel, alongside the gate [35, 37]. Consequently, SCEs begin to manifest. Charge carriers are then affected not only by the field-effect of the gate but also by that of the depletion region at the drain terminal. As a result of this reduced gate control, the threshold voltage, V_{th}, of the device decreases, while subthreshold slopes increase, leading to larger currents when the transistor is in its off-state. Additionally, SCEs intensify surface scattering effects, which degrades carrier mobility [35]. Moreover, tunnelling between the source and drain occurs, leading to increased leakage currents and higher power dissipation [38].

2.2 Two-Dimensional Semiconductors

To enable continued shrinking of transistor sizes, the research community turned to two-dimensional (2D) semiconductors, with transition metal dichalcogenides (TMDs) gaining particular interest [39–41]. 2D TMDs are compounds represented by the chemical formula MX_2, where M denotes a transition metal element such as tungsten (W) or molybdenum (Mo), and X represents a chalcogen atom such as sulphur (S) or selenium (Se). These materials consist of atomic layers bonded together through covalent forces, while van der Waals interactions enable the stacking of multiple layers to form hetero- and homostructures [42]. Given the challenges faced by traditional MOSFETs due to SCEs, resulting in degraded mobilities and increased tunnelling and leakage currents, 2D TMDs have been deemed suitable as potential solutions for enhancing transistor performance [36].

The atomic thickness and pristine surface, free from dangling bonds, inherent in these materials, prevent charge carriers from tunnelling and scattering [3, 5, 6, 43–50]. Hence, they remain unaffected by SCEs, enabling the downscaling of channel lengths and widths, all while maintaining a high carrier mobility and keeping leakage currents at a minimum. Research within the TMD family has almost solely focused on MoS_2 [5, 51]. However, WS_2 has attracted recent attention due to exhibiting desirable electronic properties, including the demonstration of higher mobility values than any other TMD including MoS_2 [52–56]. It is therefore compelling to investigate WS_2 and its electronic properties for transistor applications.

2.2.1 2D TMD-Based FET

In a 2D TMD-based FET, depicted in Figure 2.3c), the TMD serves as the channel. To induce a field-effect, a back-gate can be employed to drive charge carriers along the TMD channel. A highly doped body then acts as a gate. By applying V_g the conductivity of the channel increases [50]. Applying V_{ds} will then establish a current flow between the drain and the source, similar to conventional MOSFETs.

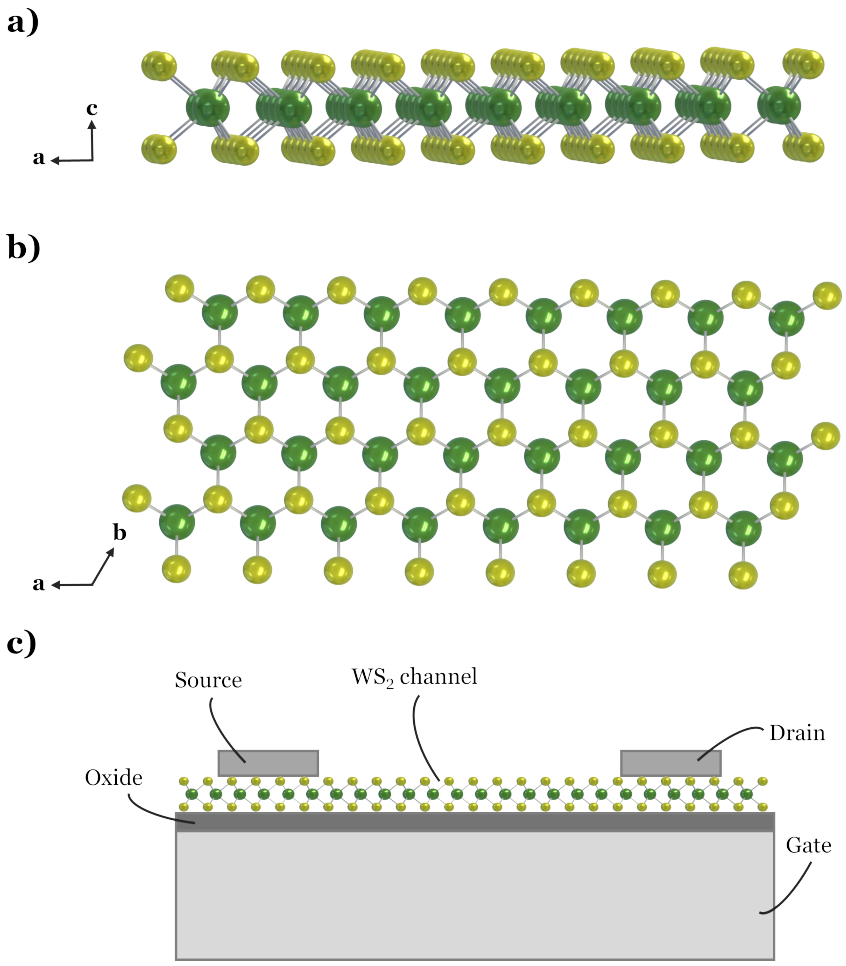


Figure 2.3: Atomic structure and orientation of a WS_2 monolayer (ML) alongside a 2D FET with WS_2 as the channel material. **a)** Side view of a WS_2 ML. **b)** Top view of a WS_2 ML. **c)** Illustration of a 2D TMD-based FET with the channel material being WS_2. The figure is not to scale.

2.2.1.1 Transfer Process

When fabricating 2D FETs using CVD-grown TMD samples, the material first needs to be transferred to a target substrate, as the high temperatures of the growth process heavily disrupt the quality of the growth substrate [27, 28]. A wet transfer method is often employed for its speed and ease in transferring CVD-grown samples [57–60]. However, this method can easily introduce unwanted impurities such as bubbles, wrinkles, polymer residue, water molecules, and other contaminants. These extrinsic defects can degrade overall device performance, emphasising the importance of being aware of them.

2.2.1.2 Contact Resistance

Despite the advantage of possessing a pristine surface free from dangling bonds, 2D TMDs also face challenges in forming a good interface with metal contacts [61–63]. This limitation restricts parameters such as SS, I_D, I_{ON}/I_{OFF} and mobility, thereby

also hindering overall device performance [64–67]. It is therefore crucial to assess the quality of the contact, by characterising the contact resistance, R_C, and the Schottky barrier height [50]. The Schottky barrier height, Φ_b, is determined by subtracting the electron affinity, χ of the semiconductor from the work function, Φ_m of the metal. This is called the Schottky-Mott rule and is shown here for electrons:

$$e\Phi_b = e\Phi_m - e\chi \tag{2.4}$$

2.2.1.2.1 Metal-Semiconductor Interface at the 2D Scale In the interface between a metal and a 2D TMD semiconductor, various factors come into play, as seen in Figure 2.4. Solely considering the work function of the contact metal is therefore not enough. Due to the pristine surface of 2D TMDs, establishing contacts with metals often relies on a van der Waals gap. This creates an additional tunnel barrier, which increases R_C [62, 63]. To form stronger bonds, disruption of the 2D surface is necessary, leading to the introduction of defects, represented by gap states in the interface of the materials [50]. Consequently, Fermi level pinning occurs, further increasing R_C [50, 62, 63, 67–70]. In other words, several factors affect the quality of a metal-2D TMD contact, and it is necessary to consider more factors beyond the metal work function [62, 67, 71–74].

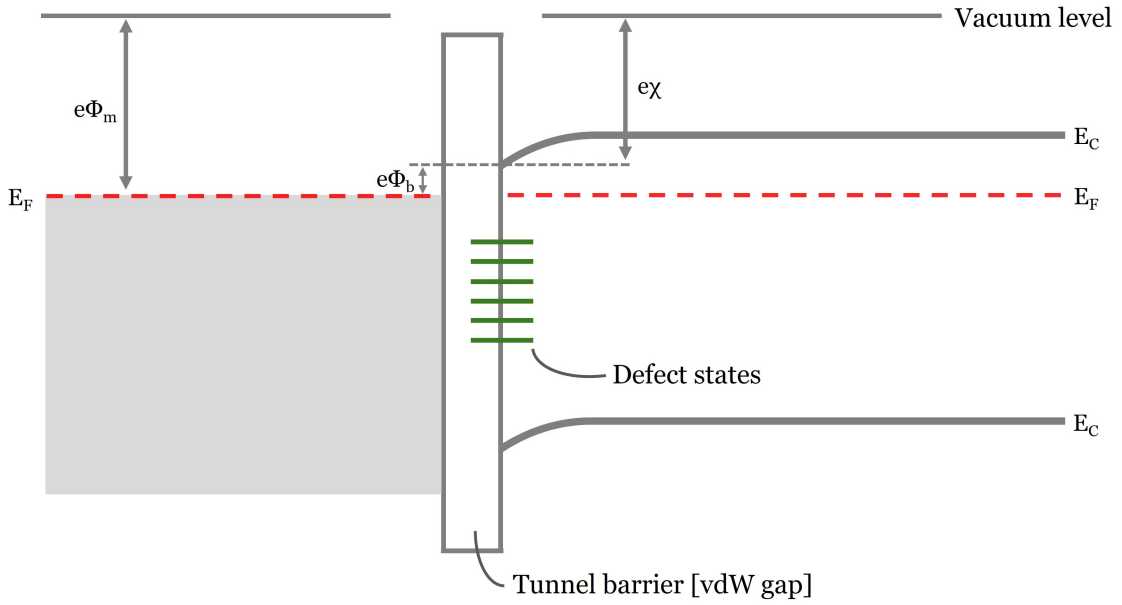


Figure 2.4: The interface between a metal and a 2D semiconductor after contact has been made. Before contact, $e\Phi_m > e\chi$. When the metal and semiconductor are placed in contact with each other, electrons are transferred from the metal to the semiconductor, causing band bending in the semiconductor, as the Fermi levels align. A Schottky barrier, $e\Phi_b$, is formed, symbolising the barrier that charge carriers need to overcome. In this scenario, $e\Phi_m$ is only slightly higher than $e\chi$, resulting in a relatively small $e\Phi_b$ compared to a metal with a high $e\Phi_m$. Due to the vdW gap between the metal and semiconductor, a tunnel barrier is created. Defect states in the interface, caused by the disruption of the 2D surface, are also present.

It is worth noting that calculating the R_C and Schottky barrier height requires the use of various methods and measurement techniques, which falls outside the scope of this thesis. Nonetheless, it is important to recognise that these parameters can significantly hinder device performance, which is important to understand when measuring and characterising the performance of 2D devices.

2.3 Twistronics

In a crystalline material, a periodic potential is created by its crystal structure. As electrons move through this potential, the electronic band structure of the material is formed [75]. Moreover, the repeating arrangement of atoms in the crystal structure is referred to as the atomic lattice. When stacking two or more materials, it can be done in two ways: AA-stacking, where the lattice constants perfectly align, or with a deliberate lattice mismatch [15]. These two ways are illustrated in Figure 2.5.

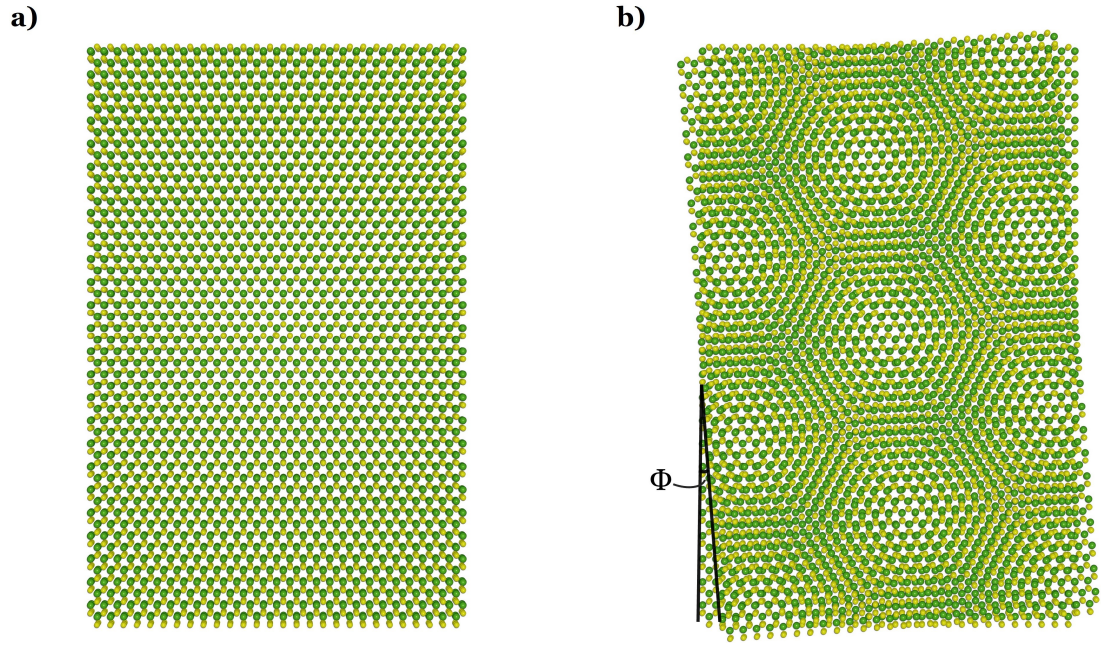


Figure 2.5: Different stacking orientations of 2D homostructures. **a)** AA-stacking with perfect lattice alignment. **b)** Stacking with a twist angle, Φ, between the layers, forming a moiré pattern.

For the latter case, the periodic potential is altered and a moiré pattern is formed [76]. This moiré pattern is the result of the interference between the periodicities of the respective stacked layers and introduces an additional periodicity which changes the band structure [77, 78]. Additionally, the interaction between the layers varies depending on their alignment along different lattice sites [79]. Certain regions of the stacked layers may exhibit stronger interlayer interactions than others, due to how the layers are aligned. As a result, the transfer of electrons between the layers is altered, leading to variations in the electronic properties of the material [75, 80–92].

This has promoted the field of twistronics to gain significant traction as of late [17, 93]. The forming of angle-dependent vdW-structures has proven to be a good way of tuning the properties of the structure and introducing different phenomena. Twist-dependent superconductivity and insulating behaviour were discovered in twisted bilayer graphene, occurring at a magic angle of $\approx 1.1^\circ$ [79, 91, 92]. Subsequently, much attention has been directed at 2D TMDs, which possess a broader spectrum of twist angles, highlighting the superior tunability of these materials [14, 75, 94].

Up until now, previous work has mostly revolved around exfoliated samples. While exfoliation is an established fabrication technique ensuring good quality material, [95, 96], it is hindered by low yield and small flake sizes, limiting scalable production of 2D materials [22, 97]. Recent advancements have shown that employing CVD serves as a solid alternative to exfoliation, promoting high yield and industrial compatibility and allowing for the fabrication of high-quality 2D TMD heterostructures [24–26, 98]. Moreover, prior research on twisted 2D TMD structures has had a significant emphasis on optics [99–103] and correlated electron physics [78, 94, 104–106]. Conducting transport measurements using CVD-grown TMD-flakes is therefore important to also investigate the electronic transport of these materials.

2.4 Charge Transport Across Homojunctions

During CVD growth of TMDs, natural bilayer (BL) regions might grow from the nucleation site, forming a homojunction between two different layer regions, as seen in Figure 2.6. Previously, such homojunctions have been reported in both graphene and 2D semiconductor materials [107, 108].

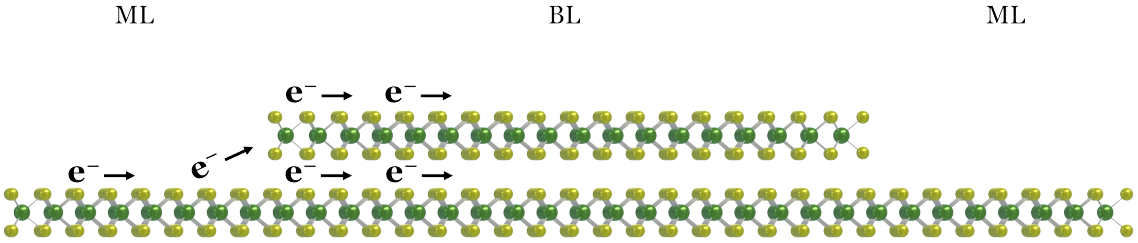


Figure 2.6: Illustration of charge transport across a ML-BL-ML homojunction, with electron movement between the TMD layers being shown.

These homojunctions can form with different twist angles and stacking orientations of the ML and BL regions. Due to being more energetically favourable, AA-stacking, where the layers are perfectly aligned, and AB-stacking, where the BL region is twisted 60° relative to the ML, are more common for the growth of the BL [109–117]. Despite the potential of CVD-grown TMDs, defects can easily form during the growth process and disrupt the quality of the sample [29, 30]. These defects are intrinsic in nature, originating from the processes involved in growing the sample.

Different defects can affect the doping polarities of the regions at the homojunction. Generally, the thinner ML region is more susceptible to defects, potentially result-

ing in a higher doping concentration of this region [118, 119]. In some instances, however, BL regions may contain more intrinsic defects, leading to a higher doping concentration of these regions.

Previous studies have employed Raman spectroscopy to investigate defects in a CVD-grown ML WSe_2 flake with naturally grown BL regions [120]. Raman was conducted to characterise a BL region located at the centre of the flake, as well as BL regions situated at the edges of the flake. It was observed that the Raman intensity of the E_{2g} peak was lower for the BL region at the centre compared to those at the edges. A lower intensity of this peak is typically associated with a higher amount of defects, which, in this case, can be attributed to more intrinsic defects originating from the nucleation site at the centre. Moreover, photoluminescence (PL) has previously been used to investigate defects, as crystal defects are found to also weaken the intensity of PL emission [121–123].

Effectively, these factors can potentially influence charge transport across homojunctions, representing an important aspect in the exploration of twisted 2D TMD devices. Thus, in utilising the concepts presented in this section, this thesis aims to widen the knowledge base of 2D TMD homostructures and how their electronic properties and behaviour are affected by a twist angle.

3

Experimental

The experimental part of this thesis consisted of two processes: device fabrication and measurements. Twisted WS_2-homostructures were fabricated using various microfabrication techniques. Measurements were then performed to characterise the devices and investigate their behaviour. This chapter gives an overview of the experimental procedures, the results of which are presented in Chapter 4. For a more detailed version of the fabrication, see Appendix A. Similarly, the measurement process is explained more thoroughly in Appendix B.

3.1 Device Fabrication

Layers of CVD-grown WS_2 were transferred onto a Si/SiO_2 substrate using a wet transfer process, in an attempt to stack layers with a twist angle. A schematic illustration for this is depicted in Figure 3.1. Subsequently, the Si/SiO_2 substrate now containing twisted WS_2-homostructures was spin coated and patterned using electron beam lithography (EBL). Thereafter, development and etching were performed to reveal desirable areas and allow for contact placement. An additional spin coating process ensued, followed by a second iteration of EBL, with contact areas being exposed through development of the chip. Metal contacts of Ti/Au were deposited using electron beam evaporation, after which lift-off was performed to remove deposited metals from everywhere apart from the contact areas themselves. This procedure thus ensured that only the contact regions remained covered with Ti/Au. Finally, the chip underwent annealing to improve its crystallinity, reduce defects and enhance electronic properties as well as the WS_2-electrode interface [124].

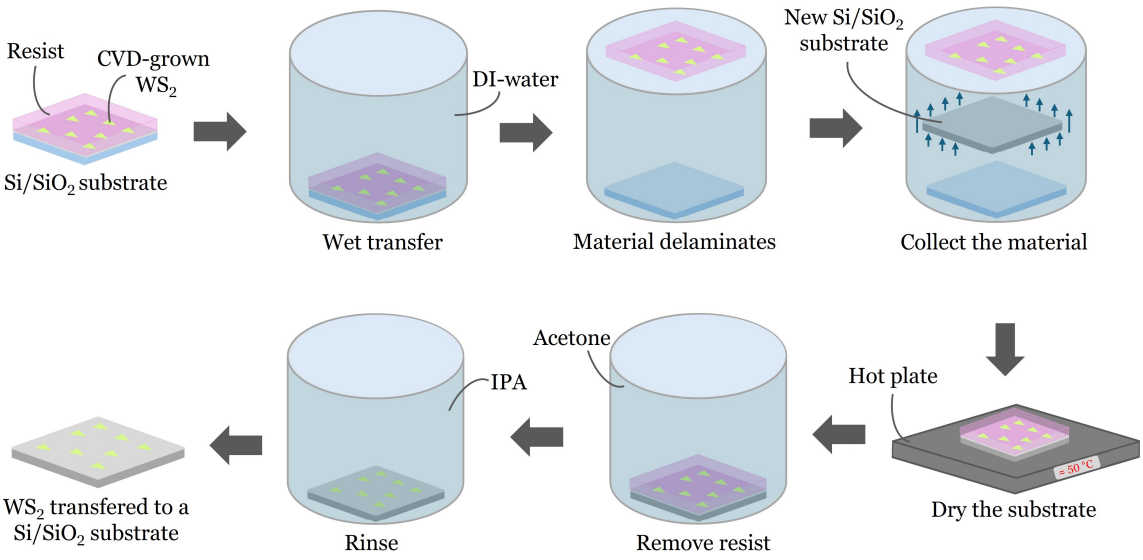


Figure 3.1: Wet transfer process used to transfer WS_2 to a target substrate. A growth substrate of Si/SiO_2 coated with CVD-grown WS_2 flakes and a layer of resist was submerged in a beaker of DI-water. This immersion caused the material to delaminate and float towards the surface. Subsequently, the target substrate was submerged in the same beaker and raised upwards to collect the detached material. The assembled structure was then put on a hot plate for drying. Once dried, acetone was used to remove the layer of resist from the substrate, isolating the WS_2. Lastly, the substrate was rinsed with IPA to remove any residue.

One of the successfully fabricated devices is seen in Figure 3.2.

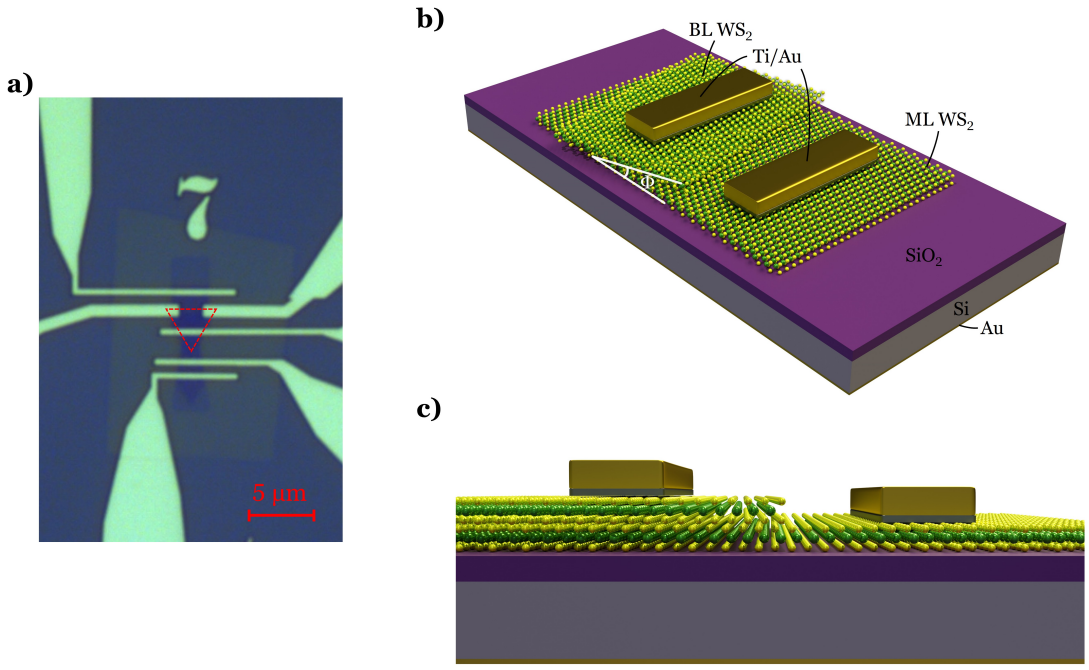


Figure 3.2: Twisted WS_2-based FET. **a)** Image of a successfully fabricated device taken with an optical microscope. The dashed red triangle indicates the BL region grown on top of a ML region. **b)** Schematic representing the structure of a twisted WS_2 FET. ML- and BL regions of WS_2 are twisted relative to each other at an angle, Φ, and placed on a Si/SiO_2 substrate containing a thin layer of gold at the bottom, with Ti/Au contacts being deposited onto the homostructure. **c)** Cross-section illustration of a twisted WS_2 FET.

3.2 Device Measurements

After a successful fabrication, the chip was securely placed in a chip holder. Devices designated for measurements were first bonded using a wire bonding machine. Thin wires were connected between the contacts of the devices and terminals located on the chip holder. The chip was then placed in a microstat under high vacuum. Thereafter, Labview software was utilised to perform various measurements. First, a small voltage was applied between each of the contacts to ensure that they were working properly. Subsequently, I-V characteristics were investigated. Both output- and transfer characteristics were acquired. For the former, I_D was measured over a V_{ds} range of -5 V to 5 V or -10 V to 10 V depending on which device was measured, while V_g was varied between -70 V and 70 V. Transfer characteristics were obtained by measuring I_D across a sweep range of V_g between -70 V and 70 V, with V_{ds} varying between -5 V and 5 V. The procedure was repeated for every device on the chip that was measured. All measurements were performed at room temperature.

3.2.1 Measurement Analysis

Upon having measured the fabricated devices, results were analysed using OriginLab software. Data saved from each measurement set was processed, and the software

was used to plot graphs and visualise the behaviour of the devices. Through analysis of the I-V curves, various parameters were extracted to accurately characterise device performance.

V_{th} was obtained by identifying the tangent along the linear region of the transfer characteristics at maximum V_g. This process was performed manually in OriginLab, with the linear region and tangent placement visually estimated. V_{th} was found at the point where the tangent intersects the X-axis.

I_{ON} and I_{OFF} were both determined from the transfer characteristics plotted in a logarithmic scale and at maximum V_{ds}. I_{ON} corresponds to the highest value of the curve, while OriginLab was used to calculate the mean value of the noise floor of the curve to obtain I_{OFF}. The appropriate region for mean value calculation was again determined through visual estimation.

The SS parameter was derived by first noting which V_g corresponded to the minimum SS in the transfer characteristics plotted in a logarithmic scale. Subsequently, the derivative of the logarithmic values of I_D at maximum V_{ds} was calculated using OriginLab. The inverse of these values was then taken and placed in a column. Lastly, the value of I_D at the previously noted V_g, was noted as the minimum SS.

The μ_{FE} was obtained using equation 2.1. L_{ch} and W_{ch} of each device configuration were measured on an optical image inserted in AutoCAD software. Additionally, C_{ox} was calculated using equation 2.2. The transconductance, g_m, was derived by plotting V_g with the derivative of I_D, followed by calculating the mean value of the linear region of the curve. This allowed for the μ_{FE} of the investigated devices to be calculated.

4

Results

In this master's thesis, twisted 2D TMD homostructures were fabricated using CVD-grown WS_2. Transport measurements were then conducted to investigate angle-dependent physics and charge transport across homojunctions. Herein, the results of these measurements are presented. The three devices that were fabricated are first shown. Subsequently, I-V curves are demonstrated in linear and logarithmic scales for the three devices. Lastly, a comparison is made between the devices, discussing their overall behaviour and performance.

4.1 Transport Measurements of CVD-Grown WS_2-Homostructures at Room Temperature

Transport measurements are important to study the electronic characteristics of a device, with output- and transfer characteristics being two common I-V curves to investigate performance [50, 125]. Such measurements were performed on the fabricated devices of CVD-grown WS_2. Figure 4.1 illustrates the three devices that were measured, along with schematics detailing contact placements and clarifications of the distinction between different layer regions, such as monolayer (ML), bilayer (BL) or multilayer (Multi).

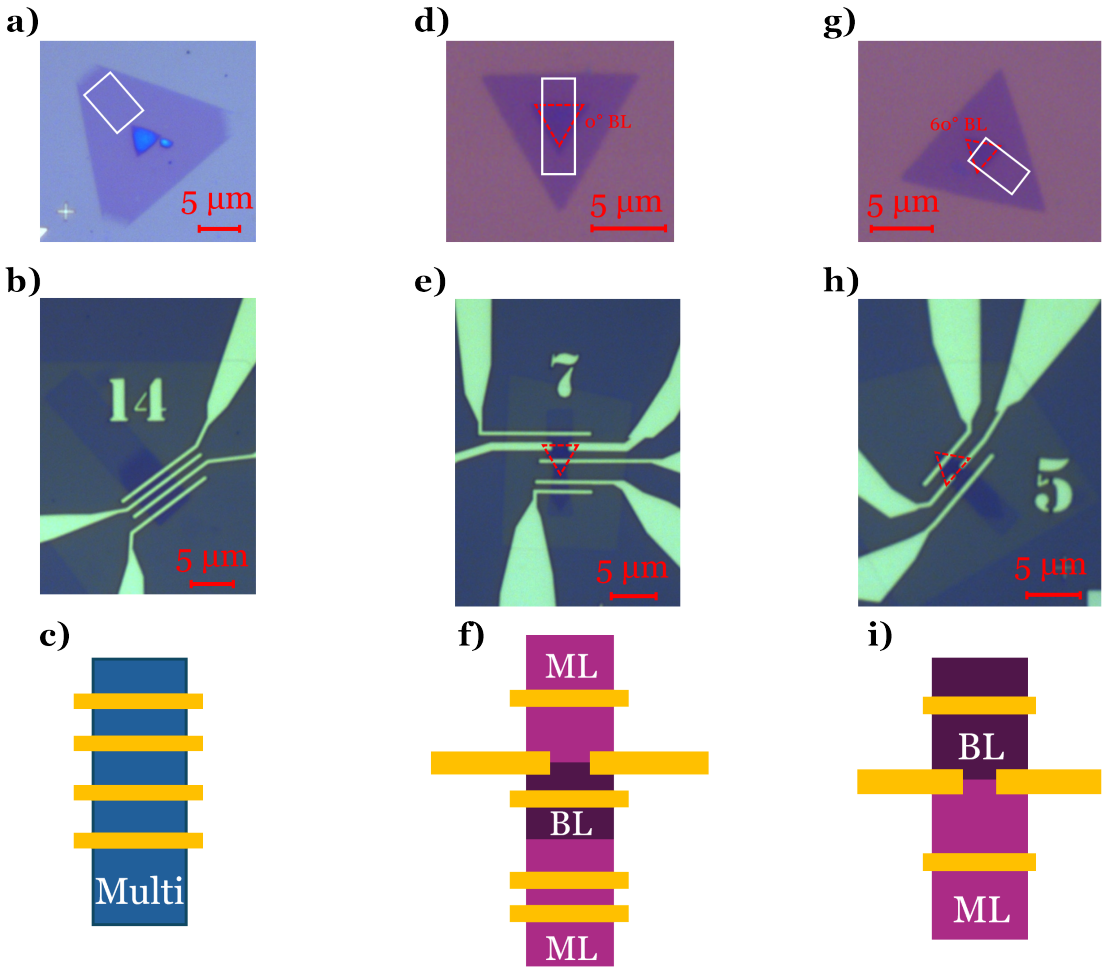


Figure 4.1: The three devices, their contact placements and different layer regions. **a)** The CVD-grown multilayer WS_2 flake used for fabrication of the device without a twist angle. The contact area, represented by the white rectangle, contains the same amount of layers. **b)** Optical image of the device and its contacts. **c)** An illustration of the fabricated device. The gold stripes symbolise the Ti/Au contacts. **d)** The flake used for fabricating the 0°-device, with the white rectangular shape indicating the contact area, and the dashed red triangle highlighting the 0°-BL region. **e)** An image of the 0°-device taken with an optical microscope. **f)** Clarification of contact placements and different layer regions of the 0°-device. **g)** The WS_2 flake used for fabrication of the 60°-device, with the white rectangle again indicating the contact area of the device, while the red triangle highlights the 60°-BL region. **h)** An optical image of the 60°-device. **i)** An illustration of contact placements and distinctions between different layer regions of the 60°-device.

The three devices encompass different layer regions and twist angles. Devices 7 and 5 are BL flakes with angles of 0° and 60° respectively, while device 14 consists of several layers without a twist angle. No junction is present in this device, as the contact area is comprised of the same amount of layers everywhere. As such, this device acts as a reference. In contrast, devices 7 and 5 both feature ML-BL junctions. Ti/Au contacts were deposited along both ML- and BL regions, allowing for multiple different measurement configurations across these regions.

4.1.1 I-V Characteristics

I-V characteristics of the three devices were obtained for different measurement configurations and sets of contacts, thus ensuring a thorough understanding of the behaviour of the devices. For every set of measurements performed, output- and transfer characteristics were measured and their respective curves were plotted.

Regardless of the device or measurement configuration, V_g was consistently set to vary between -70 V and 70 V in steps of 10 V when obtaining both output- and transfer characteristics. However, the range of V_{ds} underwent minor adjustments, specifically for obtaining the output characteristics. In some measurement sets, V_{ds} ranged from -5 V to 5 V, while in others, it varied from -10 V to 10 V. Additionally, due to the relatively low voltage levels of these intervals, the step size of V_{ds} also varied and was not always 1 V, particularly as V_{ds} approached 0 V. Consequently, V_g was swept for several values of V_{ds} close to 0 V.

Upon measuring, the output- and transfer characteristics were initially plotted in a linear scale to illustrate the behaviour of the devices. Subsequently, the same plots were visualised in a logarithmic scale to provide further insight into device performance. Plotting the transfer characteristics in a logarithmic scale indicates how the transistor operates in the subthreshold region with more accuracy than the linear scale. Similarly, the logarithmic version of the output curve can reveal more detailed information, especially in the low-current region, as small changes become more apparent in a logarithmic scale. In some instances, curves corresponding to certain voltages were excluded from the plot due to substantial noise.

4.1.1.1 No Twist Angle (Device 14)

It is appropriate to first analyse device 14 and observe the behaviour of a device with the same amount of layers and without a twist angle. Unfortunately, performance was found to be lacking, as the device displayed low current levels and undesirable I-V characteristics. In total, four sets of measurements were conducted on the device. Of these four, the one with the most acceptable current levels and I-V characteristics was chosen for further analysis. It is depicted in Figure 4.2, where the two I-V characteristics are plotted in both linear and logarithmic scales.

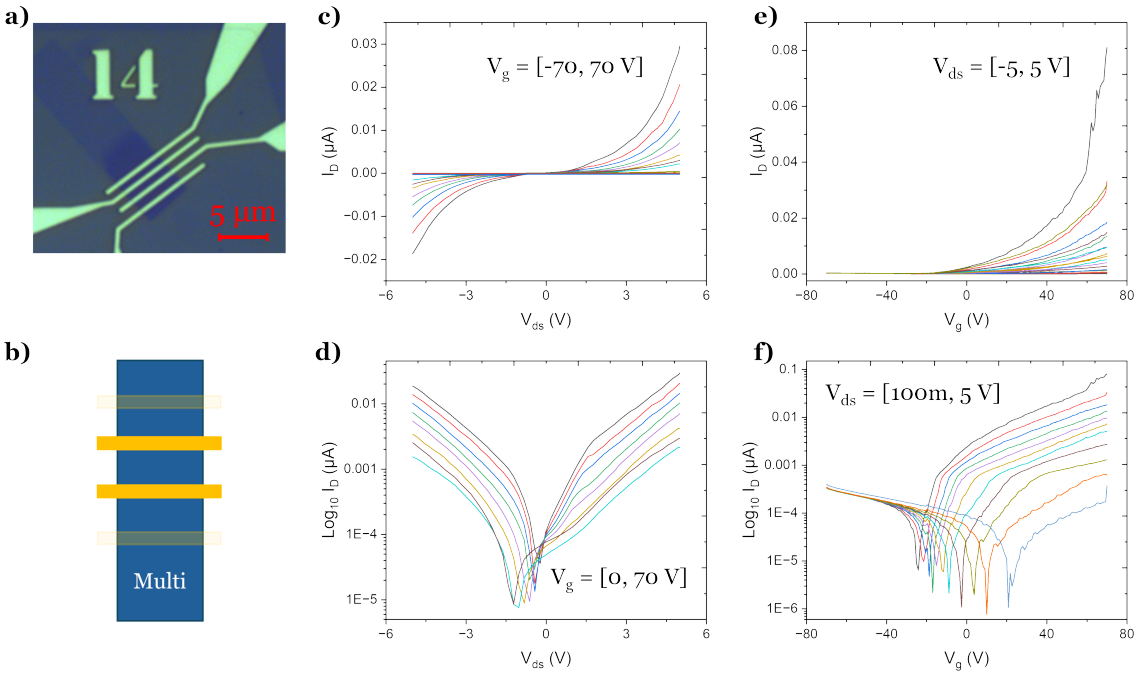


Figure 4.2: I-V characteristics of the device without a twist angle. **a)** Optical image of the device. **b)** An illustration of the device and its contacts. The two contacts between which the measurement was performed are highlighted. **c)** Output characteristics in a linear scale. V_{ds} ranges from -5 V to 5 V for every V_g, which ranges from -70 V to 70 V in steps of 10 V. **d)** Output characteristics for positive values of V_g. Plotted in a logarithmic scale. **e)** Transfer characteristics in a linear scale, with V_{ds} ranging from -5 V to 5 V and V_g from -70 V to 70 V. **f)** Transfer characteristics plotted in a logarithmic scale and for positive values of V_{ds}.

The linear output characteristics in Fig. 4.2c) display a rather symmetric behaviour, indicating a uniform charge transport. Since the device has the same number of layers everywhere, this is expected. This uniformity is also observed in the output characteristics plotted in a logarithmic scale in Fig. 4.2d), where current levels are similar for both negative and positive values of V_{ds}. Various slope changes are also observed in the same plot, which are believed to be due to the effect of two simultaneous transport mechanisms. Considering that the device does not possess any junctions or different layer regions, these changes are most likely caused by the contacts. Atoms from the contacts may diffuse into the channel, resulting in these slope changes. Residue and other factors originating from the wet transfer process might also contribute to this effect.

Moreover, Fig. 4.2d) demonstrates slight shifts of the individual curves in the plot, as they do not originate from the same position. These shifts are markedly larger in the transfer characteristics plotted in a logarithmic scale in Fig. 4.2f). Pinpointing the exact reason for this is challenging, as various factors can contribute. One major factor is believed to be trapped charges at the oxide-channel interface. This is supported by the fact that the shifts are more pronounced in Fig. 4.2f), where V_g

is a determining factor.

Using equation 2.1, the μ_{FE} of the channel is obtained. The transconductance, g_m, is calculated to be $3.38 \cdot 10^{-8}$ F/cm while the L_{ch} and W_{ch} are 0.63 µm and 5 µm respectively. C_{ox} is calculated through equation 2.2 to a value of $1.21 \cdot 10^{-8}$ F/cm. As all devices were fabricated on the same Si/SiO_2, this value is valid for all devices and will hereafter be used for all mobility calculations. The obtained μ_{FE} is 0.007 $cm^2/V{\cdot}s$. Furhtermore, V_{th} is 46.9 V. I_{ON} is noted to be 0.08 µA, while I_{OFF} is $6.4 \cdot 10^{-6}$ µA, resulting in an I_{ON}/I_{OFF} of 10^4. The SS parameter of the device is 2.17 V/dec.

4.1.1.2 0° Twist Angle (Device 7)

After observing the behaviour of the device without a twist angle, it is interesting to analyse the two twisted devices in order to investigate any twist-dependent effects as well as charge transport across the different layer regions. Device 7 possesses a BL region with a 0° twist angle and the contact area of this device spans across a ML-BL-ML region. Various contact configurations were measured to properly characterise the device. Figure 4.3 illustrates a set of measurements between the first ML-BL junction, with output- and transfer characteristics plotted.

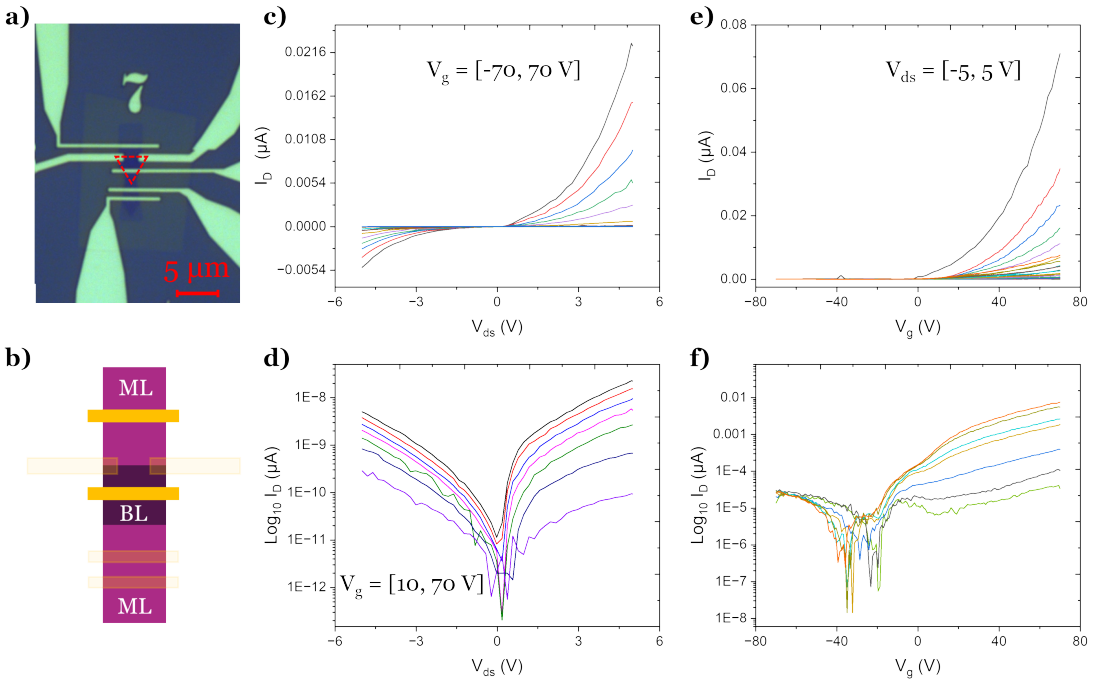


Figure 4.3: I-V characteristics of the 0°-device, with measurements performed over the first ML-BL junction. **a)** Optical image of the 0°-device. **b)** Illustration of layer regions and contact placements of the device, with the two contacts used for measurements over the first ML-BL junction being highlighted. **c)** Output characteristics in a linear scale, with V_{ds} ranging from -5 V to 5 V and V_g from -70 V to 70 V. **d)** Output characteristics, plotted in a logarithmic scale and for values of V_g between 10 V and 70 V. **e)** Linear transfer characteristics. V_{ds} ranges from -5 V to 5 V and V_g from -70 V to 70 V. **f)** Transfer characteristics plotted in a logarithmic scale.

The output characteristics presented in Fig. 4.3c) demonstrate a clear asymmetry, with current levels being elevated for positive values of V_{ds} compared to negative values. Unlike Fig. 4.2c), which exhibits uniform charge transport, this asymmetry indicates rectifying behaviour across the ML-BL junction. This is further evident in Fig. 4.3d), where a higher current is noted for positive voltages. Furthermore, shifts in the curves are again observed in the same plot. Additionally, in the logarithmic version of the transfer characteristics shown in Fig. 4.3f), instead of the curves collectively contributing to one valley, two valleys can be seen. The reason for this is difficult to pinpoint but it is believed to occur due to residue from the wet transfer.

Due to the triangular shape of the bilayer region, the contact area was adjusted accordingly. As a result, the channel width of device 7 is not constant. Instead, different channel widths, corresponding to the two contact placements of the measurement set, are considered and an average W_{ch} of 2.7 µm is acquired. L_{ch} is 2.6 µm. With g_m calculated to be $1.95 \cdot 10^{-9}$ F/cm, a μ_{FE} of 0.03 $cm^2/V{\cdot}s$ is obtained. V_{th} is noted to be 37.6 V. Additionally, I_{ON} and I_{OFF} is 0.07 µA and $1.04 \cdot 10^{-5}$ µA respectively, and an I_{ON}/I_{OFF} of 10^3 is acquired. Finally, SS is 3.28 V/dec.

After measuring over the first ML-BL junction, measurements were then performed over the second junction, to further investigate the charge transport across different layer regions.

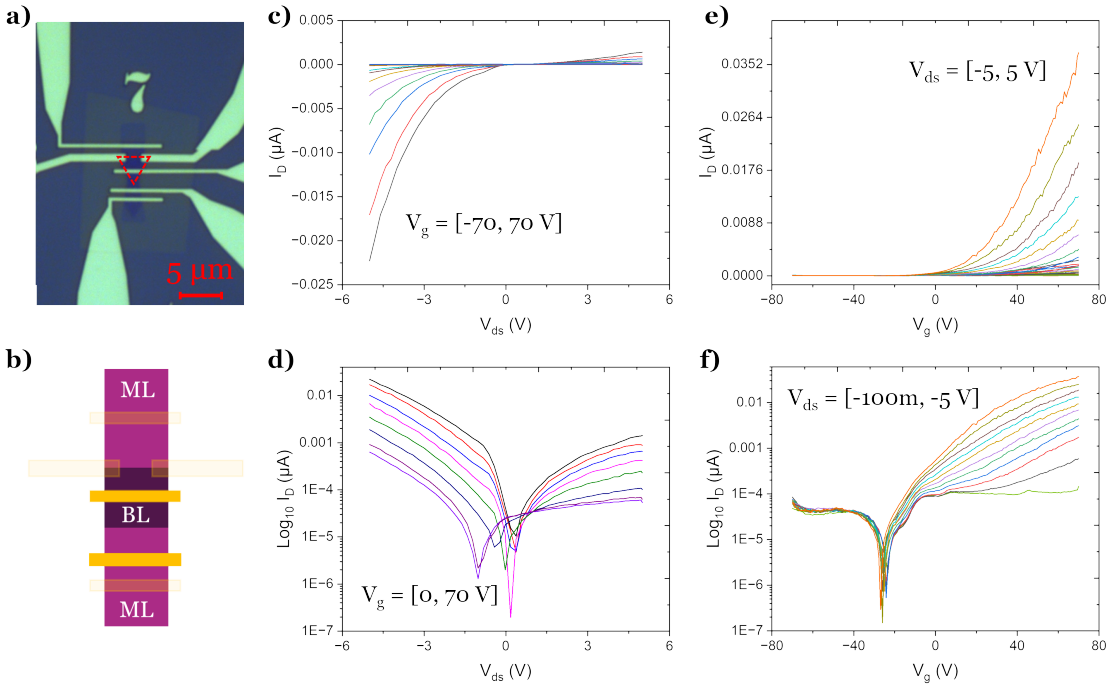


Figure 4.4: I-V characteristics of the second junction of the 0°-device. **a)** Optical image of the device. **b)** Schematic of layer regions and contact placements, clarifying that measurements were performed over the second ML-BL junction. **c)** Output characteristics plotted in a linear scale. The sweep range is from -5 V to 5 V for V_{ds} and -70 V to 70 V for V_g. **d)** Output characteristics in a logarithmic scale plotted for positive V_g. **e)** Transfer characteristics plotted in a linear scale. V_g is swept from -70 V to 70 V for V_{ds} values between -5 V and 5 V. **f)** Transfer characteristics plotted in a logarithmic scale and for negative values of V_{ds}.

The asymmetry of the output characteristics observed in Fig. 4.4c) points to a similar phenomenon noted in Fig. 4.3c), with a clear rectifying behaviour being observed. This time the device displays a substantial negative current and a low positive current, which is reflected by the larger negative current values in the output characteristics plotted in a logarithmic scale in Fig. 4.4d). Further analysis of the non-uniformity of the charge transport over the two junctions is illustrated in Figure 4.5.

As in the previous case, the channel width across the two contacts is not constant. The average W_{ch} of this measurement set is 2.35 µm, while L_{ch} is 1.86 µm. With a g_m of $5 \cdot 10^{-11}$ F/cm, this results in a μ_{FE} of 0.0007 $cm^2/V{\cdot}s$. Moreover, SS is noted to be 8.6 V/dec, I_{ON} 0.002 µA, I_{OFF} $1.6 \cdot 10^{-4}$ µA and a rather low I_{ON}/I_{OFF} of 10^1 is obtained. V_{th} is noted to be 23.8 V.

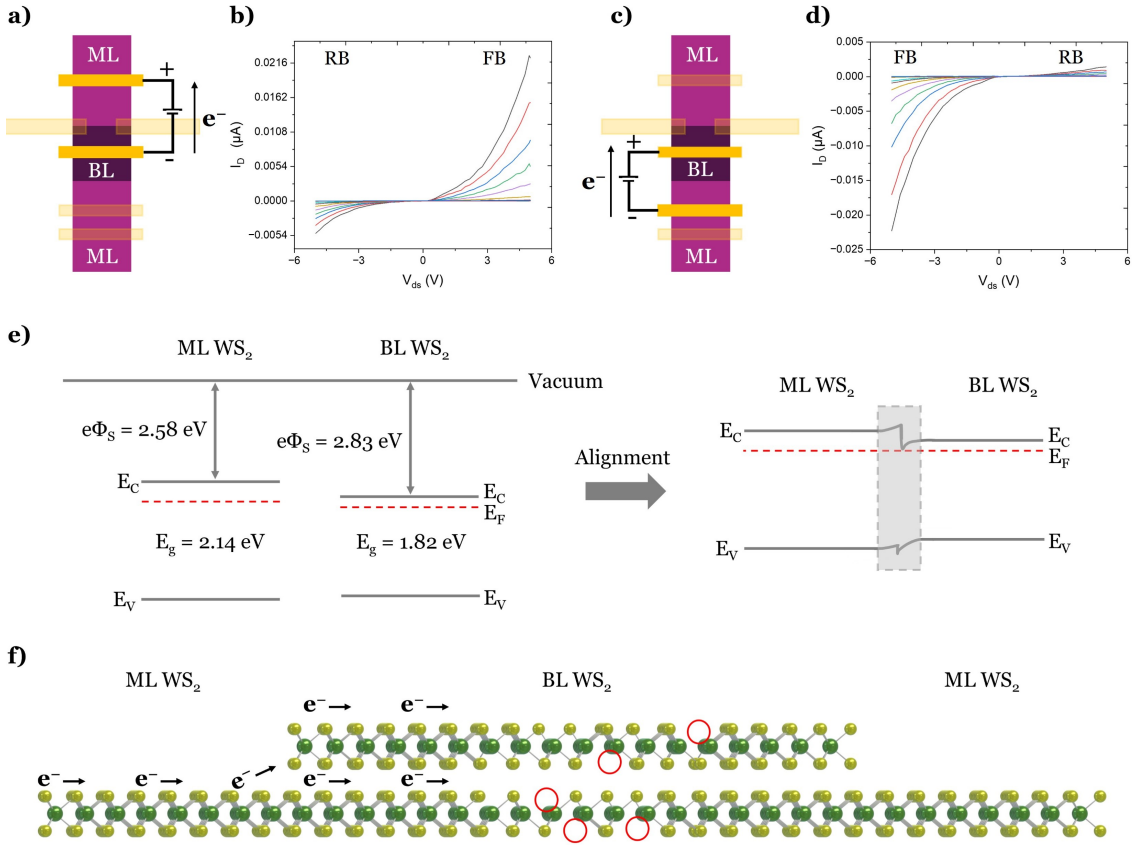


Figure 4.5: Comparison of charge transport across homojunctions. **a)** Illustration of how measurements were performed over the first junction. **b)** Output characteristics of the first junction, with reverse bias (RB) and forward bias (FB) marked. **c)** Illustration of measurements being performed over the second junction. **d)** Output characteristics corresponding to the second junction. **e)** Band structure before and after alignment, with the dashed grey rectangle emphasising the homojunction. **f)** Illustration of charge transport over a ML-BL homojunction. The BL region is believed to contain more defects, with red circles showcasing sulphur vacancies.

As indicated in Fig. 4.5a), plus was connected to the ML and minus to the BL, causing electrons to flow from BL to ML. This resulted in a positive current at forward bias. Conversely, when measuring over the second junction, as illustrated in Fig. 4.5c), plus was instead connected to BL and minus to ML. Electron flow was then established from ML to BL and resulted in a large negative current at forward bias. Thus, rectifying behaviour is observed in the device, which is illustrated by the band structure in Fig. 4.5e). Band gaps and work functions of ML WS_2 and BL WS_2 were obtained from previous literature, [126–128], and the band structure before and after contact are visualised in Fig. 4.5e). As the Fermi levels align, electrons flow from the ML to BL, causing the ML bands to bend upward. The BL bands bend down, symbolising the increased electron concentration at the interface.

It is evident that the different band gaps and work functions of ML WS_2 and BL WS_2 cause rectifying behaviour to emerge and potential barriers to form in the junc-

tion. This behaviour can be enhanced if the band gaps and work functions differ further between the two regions, indicating that these factors significantly affect the rectifying behaviour across the homojunctions. Moreover, the contact between the metal and the semiconductor differs, as contacts are deposited on two different layer regions in the device. Thus, this could lead to different Schottky barrier heights and different R_C for the respective regions in the device.

Additionally, from the I-V curves, it appears that the two layer regions have different doping polarities, with the BL possessing a higher doping concentration than the ML, consistent with previous works [120]. The increased doping concentration in the BL region is most likely due to intrinsic defects. It is possible that defects, such as sulphur vacancies, are introduced near the nucleation site during the CVD growth, as illustrated in Fig. 4.5f). These vacancies effectively contribute to an increasing concentration of free electrons, leading to a higher doping concentration in the BL region near the nucleation site. Consequently, this results in the formation of an n-n^+ junction between the ML and BL regions. Together, the different band gaps and work functions, as well as these intrinsic defects, collectively contribute to the rectifying behaviour in the device.

Subsequently, measurements were performed across the first junction, to investigate the behaviour precisely at the junction.

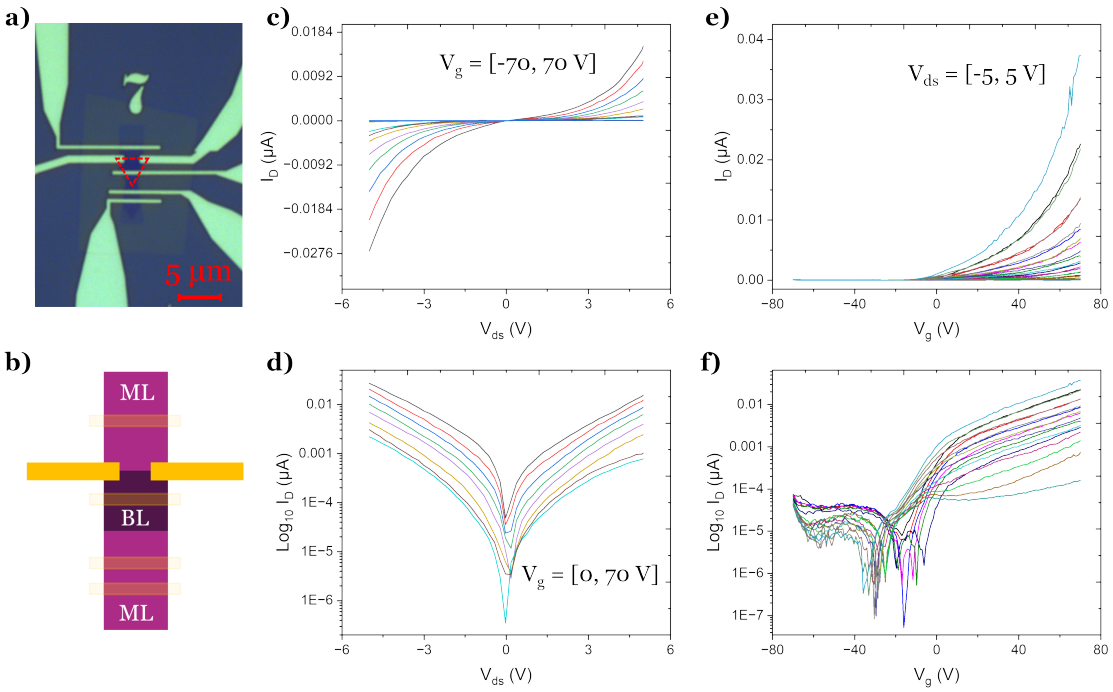


Figure 4.6: I-V characteristics across the ML-BL junction of the 0°-device. **a)** Optical image of the 0°-device. **b)** Schematic illustration of the layer regions and contacts of the device. Measurements were performed across the ML-BL junction, as indicated by the two highlighted contacts. **c)** Output characteristics in a linear scale. V_{ds} ranges from -5 V to 5 V and V_g ranges from -70 V to 70 V. **d)** Output characteristics plotted in a logarithmic scale for positive values of V_g. **e)** Transfer characteristics plotted in a linear scale and with V_g being swept from -70 V to 70 V for values of V_{ds} between -5 V and 5 V. **f)** Transfer characteristics plotted in a logarithmic scale.

While the linear output characteristics in Fig. 4.6c) display some asymmetry, it is not as pronounced as the measurements over the two junctions. Also, the output characteristics plotted in a logarithmic scale in Fig. 4.6d) exhibit clear symmetric behaviour. It is worth mentioning that it can be rather challenging to fully capture the behaviour of the junction, especially given the smaller channel length and width of this measurement configuration. L_{ch} is the distance between the contacts, which is 1.8 µm, while W_{ch} is 1 µm, which is the width of the contacts themselves. g_m is $5.9 \cdot 10^{-10}$ F/cm, and a μ_{FE} of 0.02 $cm^2/V{\cdot}s$ is calculated. With an I_{ON} of 0.026 µA and I_{OFF} of $6.82 \cdot 10^{-5}$ µA, the I_{ON}/I_{OFF} is 10^3. V_{th} is 36.3 V and SS 8.3 V/dec.

A final set of measurements were performed over both junctions and over the whole BL region.

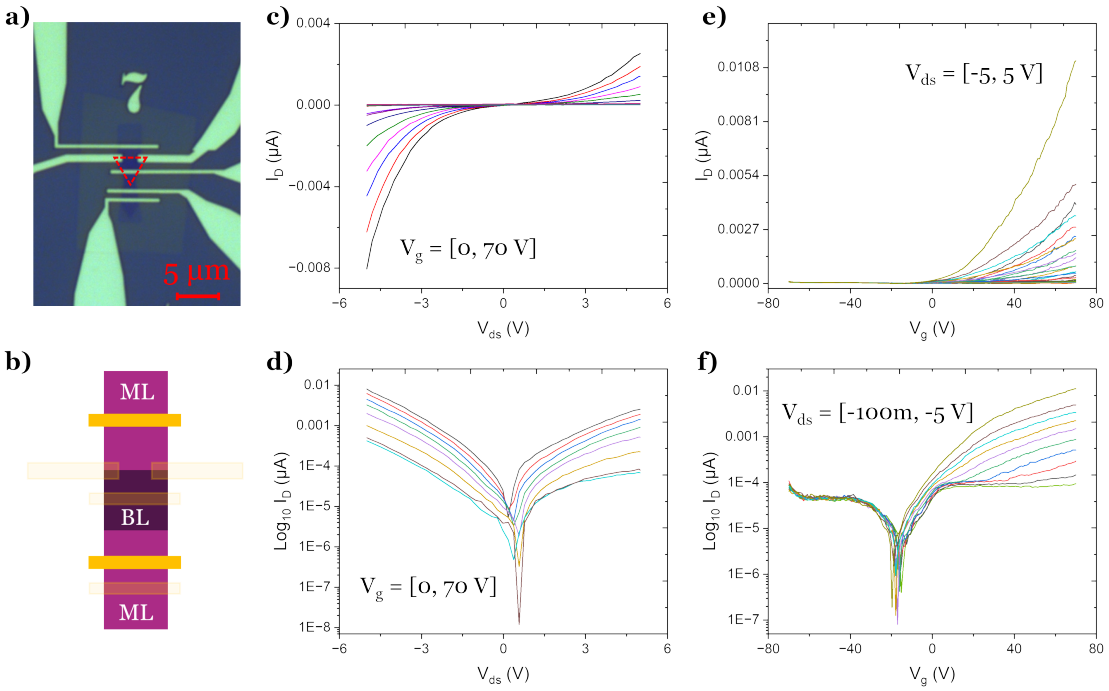


Figure 4.7: I-V characteristics of the 0°-device, measured over both ML-BL junctions. **a)** Optical image of the device. **b)** Illustration of the 0°-device, with highlighted contacts indicating measurements between the two ML regions, over the BL region. **c)** Output characteristics in a linear scale. V_{ds} ranges from -5 V to 5 V while V_g ranges from -70 V to 70 V. **d)** Output characteristics plotted in a logarithmic scale and for positive values of V_g. **e)** Transfer characteristics plotted for voltage intervals of -70 V to 70 V for V_g and -5 V to 5 V for V_{ds}. Plotted in a linear scale. **f)** Transfer characteristics plotted in a logarithmic scale and for negative values of V_{ds}.

Similar asymmetric behaviour, as previously observed, is demonstrated in the output characteristics plotted both in linear and logarithmic scales. Fig. 4.7c) indicates a higher negative current, which is reflected by elevated current levels at negative values in Fig. 4.7d). While this further showcases the rectifying behaviour observed in the 0°-device, it might be difficult to fully capture this behaviour, as measurements are performed over both ML-BL junctions simultaneously.

With a g_m of $1 \cdot 10^{-10}$ F/cm, L_{ch} and W_{ch} of 15 µm and 2.7 µm respectively, μ_{FE} is calculated to be 0.009 $cm^2/V{\cdot}s$. V_{th} is noted to be 37.2 V and the SS is 15.9 V/dec. Lastly, I_{ON} is 0.004 µA and I_{OFF} is $7.46 \cdot 10^{-5}$ µA, resulting in an I_{ON}/I_{OFF} of 10^2.

4.1.1.3 60° Twist Angle (Device 5)

Lastly, device 5 with a BL region twisted 60° was analysed. The contact area of this device spans across a BL and ML region. Measurements were performed over the BL-ML junction as well as across the junction. I-V characteristics of measurements conducted over the BL-ML junction are illustrated in Figure 4.8.

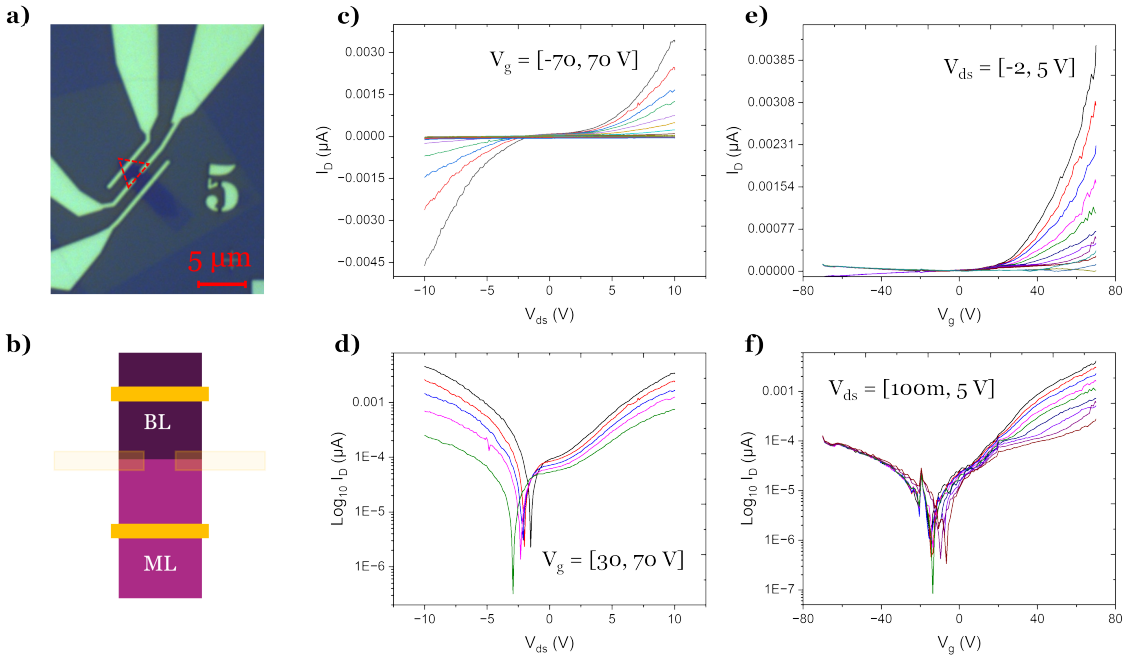


Figure 4.8: I-V characteristics of the 60°-device, measured over the BL-ML junction. **a)** Optical image of the 60°-device. **b)** Schematic illustration of layer regions and contact placements of the device, with the two highlighted contacts indicating that measurements were performed over the BL-ML junction. **c)** Output characteristics plotted in a linear scale, with V_{ds} ranging from -10 V to 10 V and V_g ranging from -70 V to 70 V. **d)** Output characteristics plotted in a logarithmic scale for values of V_g between 30 V and 70 V. **e)** Transfer characteristics in a linear scale. V_g is swept from -70 V to 70 V for V_{ds} values between -2 V and 5 V. **f)** Transfer characteristics plotted for positive V_{ds} values. Logarithmic scale.

Fig. 4.8c) shows symmetric output characteristics, which does imply uniform charge transport. Although, the slope changes seen in Fig. 4.8d), particularly at lower voltages, suggest that there might be rectifying behaviour over the junction, as higher current values are observed for negative voltages compared to positive voltages. However, these slope changes could also be due to contact atoms diffusing into the channel, as previously explained. Therefore, while there are some indications of rectifying behaviour, it is challenging to pinpoint an exact cause for the observed behaviour, as various factors can play a role.

Moreover, the linear transfer characteristics in Fig. 4.8e) show a non-zero current at negative V_g. This indicates that there might be some leakage in the device. Alternatively, it might be due to trapped charges in the interface between the oxide and the channel.

For this configuration, L_{ch} is 2.5 µm and W_{ch} 2.6 µm. μ_{FE} was calculated to be 0.003 $cm^2/V{\cdot}s$. The obtained V_{th} is 42.5 V and the SS 2V/dec. I_{ON} is 0.004 µA and I_{OFF} is $1.2 \cdot 10^{-4}$ µA and the I_{ON}/I_{OFF} is 10^1.

Finally, measurements were performed across the BL-ML junction.

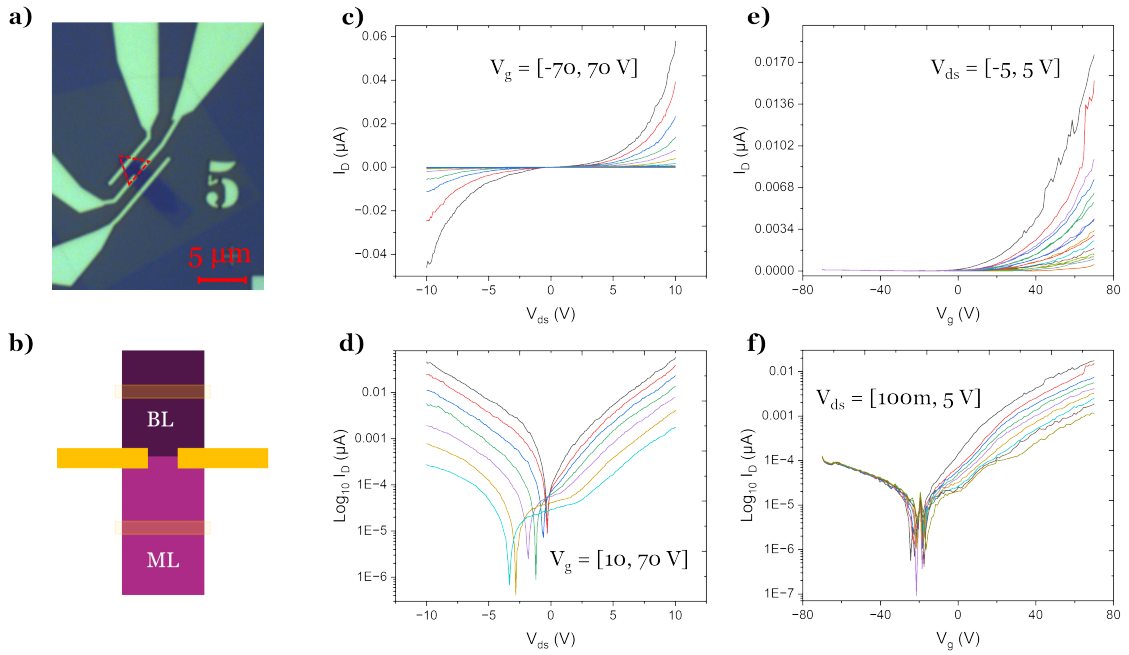


Figure 4.9: I-V characteristics of the 60°-device, measured across the BL-ML junction. **a)** Optical image of the device. **b)** Schematic illustration of the device, showing its layer regions and contact placements. Measurements were performed across the BL-ML junction, as indicated by the two highlighted contacts. **c)** Output characteristics plotted in a linear scale. The sweep range of V_{ds} is from -10 V to 10 V while V_g ranges from -70 V to 70 V. **d)** Output characteristics in a logarithmic scale. Plotted for values of V_g between 10 V and 70 V. **e)** Transfer characteristics in a linear scale. V_g ranges from -70 V to 70 V for V_{ds} values between -5 V and 5 V. **f)** Transfer characteristics plotted in a logarithmic scale and for positive V_{ds}.

Overall, Fig. 4.9c) demonstrates symmetric output characteristics, which again indicates a uniform charge transport. The output characteristics plotted in a logarithmic scale in Fig. 4.9d) show symmetry at some voltages, while slope changes are present at other voltages. Similarly to the measurements over the BL-ML junction in Fig. 4.8, pinpointing the exact reason for this is challenging. There may be rectifying behaviour as a result of intrinsic defects from the CVD growth, but considering that the linear output characteristics display symmetry, it is less obvious to conclude for this device.

Furthermore, pronounced shifts are visible in Fig. 4.9d), again suggesting trapped charges at the oxide-channel interface. Additionally, similarly to the configuration in figure 4.6, L_{ch} is determined as the distance between the contacts, while W_{ch} is the width of the contacts. They are found to be 0.87 µm and 0.5 µm respectively. Further, a μ_{FE} of 0.017 $cm^2/V{\cdot}s$ is obtained, while V_{th} is 39.9 V. The SS is 19.8 V/dec, I_{ON} 0.018 µA and I_{OFF} $1.18 \cdot 10^{-4}$ µA. Thus, an I_{ON}/I_{OFF} of 10^2 is acquired.

4.1.1.4 Comparison

The three measured devices exhibit various defect-induced phenomena, affecting their performance. Despite generally demonstrating good transistor behaviour, overall device performance is lacking. This is evidenced by the extracted parameters and observations such as slope changes, shifts, and other similar behaviour. Extrinsic defects, primarily introduced during the wet transfer process, are believed to be the main cause of such phenomena.

Moreover, the main finding of this thesis is the rectifying behaviour observed across ML-BL homojunctions. It is most pronounced in the 0°-device, where clear asymmetric behaviour in both the linear and logarithmic representations of the output characteristics indicates non-uniform charge transport. In contrast, the 60°-device, shows less obvious rectifying behaviour, as the linear output characteristics remain rather symmetric. Asymmetric behaviour is observed in the output characteristics of this device when plotted in a logarithmic scale, but such behaviour may be caused by diffusion of contact atoms, similar to the case of the multilayer device which does not possess a homojunction.

In other words, rectifying behaviour is more noticeable in the 0°-device, while it is difficult to conclude similar behaviour with certainty in the 60°-device. The rectifying behaviour is mainly attributed to the different band gaps and work functions of ML WS_2 and BL WS_2. Another contributing factor is believed to be defects, with intrinsic defects from the CVD growth being the likely cause, resulting in different doping polarities in the two layer regions. All in all, these three factors contribute to the rectifying behaviour observed in the 0°-device.

5

Summary and Conclusions

This master's thesis aimed to fabricate twisted 2D WS_2-homostructures, perform transport measurements, and investigate charge transport across homojunctions. Using a wet transfer process, CVD-grown WS_2 flakes were transferred onto a Si/SiO_2 target substrate. Through various microfabrication techniques, devices with different twist angles and homojunctions were fabricated. Transport measurements were conducted at room temperature and in a high vacuum environment. However, the performance of the devices was hindered by the presence of extrinsic defects such as residue, air, and other contaminants, thereby overshadowing possible twist-dependent performance enhancements. Furthermore, intrinsic defects originating from the CVD growth, particularly present at the nucleation site, are believed to have resulted in different doping densities in the ML and BL regions. These defects, along with different band gaps and work functions of ML WS_2 and BL WS_2, led to the observation of rectifying behaviour across homojunctions. This rectifying behaviour is the main finding of this thesis.

To address the observed performance limitations, an alternative approach could have involved utilising the tear-and-stack method. This method vastly minimises the unreliability associated with the wet transfer and reduces the likelihood of defect-induced performance degradation. Simultaneously, it allows for precise stacking of flakes with a specific twist angle. It is possible that such an approach could have revealed more apparent twist-dependent effects. Although, it is important to note that, despite its drawbacks, the wet transfer method offered fast and easy fabrication at an early stage of the project. Using a tear-and-stack method is more time-consuming and thus, would mean a longer time before measurements could be conducted. It is therefore suggested that future work in this field can focus on the tear-and-stack method or other similar approaches to further investigate twist-dependent transport properties.

Regarding the rectifying behaviour, it is believed that the intrinsic defects from the CVD growth increased the doping concentration of the BL region. To further investigate and confirm this assumption, Raman spectroscopy could be utilised to visualise the sample and examine the presence of defects in the BL region. However, as this thesis primarily focused on transport measurements rather than optical characterisation, conducting Raman spectroscopy was deemed beyond the scope of the study. Alternatively, carrier concentrations could be extracted and a comparison could be made between the ML and BL regions to confirm the observations. However, this approach requires two contacts deposited over the same layer region.

Since both the 0°- and 60°-devices only had one contact on the BL region, this examination is not possible. Instead, it is also suggested for future work. Investigation of CVD-grown TMDs requires an awareness of these intrinsic defects. By incorporating multiple contacts on each layer region, combined with Raman spectroscopy, PL, and other methods, defects can be thoroughly examined and better understood.

Thus, it can be concluded that this thesis has contributed to a deeper understanding of the physics of 2D TMDs and the influence that defects and other factors can have on charge transport across homojunctions, which helps widen the knowledge base of 2D semiconductor devices. This contribution represents a small step forward and emphasises the importance of continued research in semiconductor technology, in order to meet the growing demand for technological innovations. As smartphones, laptops, and other devices continue to proliferate, commitment to further research allows us to harness the potential of technology for the betterment of humanity.

Bibliography

[1] G. E. Moore. "Cramming more components onto integrated circuits". In: *Electronics* 38 (1965), pp. 114–177.

[2] R.K. Ratnesh et al. "Advancement and challenges in MOSFET scaling". In: *Materials Science in Semiconductor Processing* 134 (2021). DOI: 10.1016/j.mssp.2021.106002.

[3] T. Wei et al. "Two dimensional semiconducting materials for ultimately scaled transistors". In: *iScience* 25.10 (2022). DOI: 10.1016/j.isci.2022.105160.

[4] G. Fiori et al. "Electronics based on two-dimensional materials". In: *Nature Nanotech* 9 (2014), pp. 768–779. DOI: 10.1038/nnano.2014.207.

[5] M. Chhowalla, D. Jena, and H. Zhang. "Two-dimensional semiconductors for transistors". In: *Nature Reviews Materials* 1.16052 (2016). DOI: 10.1038/natrevmats.2016.52.

[6] Q. Zhang, C. Liu, and P. Zhou. "2D materials readiness for the transistor performance breakthrough". In: *iScience* 26.5 (2023). DOI: 10.1016/j.isci.2023.106673.

[7] Q. H. Wang et al. "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides". In: *Nature Nanotechnology* 7 (2012), pp. 699–712. DOI: 10.1038/nnano.2012.193.

[8] R. Fivaz and E. Mooser. "Mobility of Charge Carriers in Semiconducting Layer Structures". In: *Phys. Rev.* 163.3 (1967), pp. 743–755. DOI: 10.1103/PhysRev.163.743.

[9] W. Cao et al. "The future transistors". In: *Nature* 620 (2023), pp. 501–515. DOI: 10.1038/s41586-023-06145-x.

[10] M-Y. Li et al. "How 2D semiconductors could extend Moore's law". In: *Nature* 567 (2019), pp. 169–170. DOI: 10.1038/d41586-019-00793-8.

[11] G. Iannaccone et al. "Quantum engineering of transistors based on 2D materials heterostructures". In: *Nature Nanotechnology* 13 (2018), pp. 183–191. DOI: 10.1038/s41565-018-0082-6.

[12] M. S. Fuhrer and J. Hone. "Measurement of mobility in dual-gated MoS_2 transistors". In: *Nature Nanotechnology* 8 (2013), pp. 146–147. DOI: 10.1038/nnano.2013.30.

[13] B. Radisavljevic et al. "Single-layer MoS_2 transistors". In: *Nature nanotechnology* 6.3 (2011), pp. 147–150. DOI: 10.1038/nnano.2010.279.

[14] "Making a case for moiré semiconductors". In: *Nat. Nanotechnol.* 17.673 (2022). DOI: 10.1038/s41565-022-01184-3.

[15] S. K. Behura et al. “Moiré physics in twisted van der Waals heterostructures of 2D materials”. In: *Emergent Mat.* 4 (2021), pp. 813–826. DOI: 10.1007/s42247-021-00270-x.

[16] S. Fang and E. Kaxiras. “Electronic structure theory of weakly interacting bilayers”. In: *Phys. Rev. B* 93 (23 2016), p. 235153. DOI: 10.1103/PhysRevB.93.235153.

[17] S. Carr et al. “Twistronics: Manipulating the electronic properties of two-dimensional layered structures through their twist angle”. In: *Phys. Rev. B* 95.7 (2017), p. 075420. DOI: 10.1103/PhysRevB.95.075420.

[18] G. W. Burg et al. “Coherent Interlayer Tunneling and Negative Differential Resistance with High Current Density in Double Bilayer Graphene–WSe_2 Heterostructures”. In: *Nano Letters* 17.6 (2017), pp. 3919–3925. DOI: 10.1021/acs.nanolett.7b01505.

[19] S. Kar et al. “Twist-assisted optoelectronic phase control in two-dimensional (2D) Janus heterostructures”. In: *Scientific Reports* 13.13696 (2023). DOI: 10.1038/s41598-023-39993-8.

[20] N. Gupta et al. “Twistronics in two-dimensional transition metal dichalcogenide (TMD)-based van der Waals interface”. In: *RSC advances* 14.5 (2024), pp. 2878–2888. DOI: 10.1039/d3ra06559f.

[21] A. S. Sarkar and E. Stratakis. “Recent Advances in 2D Metal Monochalcogenides”. In: *Advanced science (Weinheim, Baden-Wurttemberg, Germany)* 7.21 (2020), p. 2001655. DOI: 10.1002/advs.202001655.

[22] K. S. Novoselov et al. “Electric Field Effect in Atomically Thin Carbon Films”. In: *SCIENCE* 306.5696 (2004), pp. 666–669. DOI: 10.1126/science.1102.

[23] H. Li et al. “Preparation and Applications of Mechanically Exfoliated Single-Layer and Multilayer MoS_2 and WSe_2 Nanosheets”. In: *Accounts of Chemical Research* 47.4 (2014), pp. 1067–1075. DOI: 10.1021/ar4002312.

[24] H. Zeng et al. “Recent developments in CVD growth and applications of 2D transition metal dichalcogenides”. In: *Frontiers of Physics* 18.5 (2023), p. 53603. DOI: 10.1007/s11467-023-1286-2.

[25] Y. Shi, H. Li, and L-J. Ji. “Recent advances in controlled synthesis of two-dimensional transition metal dichalcogenides via vapour deposition techniques”. In: *Chem. Soc. Rev.* 44 (2015), pp. 2744–2756. DOI: 10.1039/C4CS00256C.

[26] Y. Zhang et al. “Recent Progress in CVD Growth of 2D Transition Metal Dichalcogenides and Related Heterostructures”. In: *Advanced Materials* 31.41 (2019). DOI: 10.1002/adma.201901694.

[27] A. J. Watson et al. “Transfer of large-scale two-dimensional semiconductors: challenges and developments”. In: *2D Mater.* 8.3 (2021). DOI: 10.1088/2053-1583/abf234.

[28] D. Ma et al. “A universal etching-free transfer of MoS_2 films for applications in photodetectors”. In: *Nano Res.* 8 (2015), pp. 3662–3672. DOI: 10.1007/s12274-015-0866-z.

[29] W. Wang et al. “Defect Passivation and Photoluminescence Enhancement of Monolayer MoS_2 Crystals through Sodium Halide-Assisted Chemical Vapor

Deposition Growth". In: *ACS Applied Materials & Interfaces* 12.8 (2020), pp. 9563–9571. DOI: 10.1021/acsami.9b19224.

[30] Q. Wang et al. "Recent progress on kinetic control of chemical vapor deposition growth of high-quality wafer-scale transition metal dichalcogenides". In: *Nanoscale Adv.* 3 (2021), pp. 3430–3440. DOI: 10.1039/D1NA00171J.

[31] J.C. Tsang and Ph. Avouris. "5.10 - Electronic and Optoelectronic Properties and Applications of Carbon Nanotubes". In: *Comprehensive Semiconductor Science and Technology* 5 (2011), pp. 480–498. DOI: 10.1016/B978-0-44-453153-7.00030-4.

[32] W. Zhang. "The Performance of Enhancement MOSFET—The trade-off on Transfer and Output Characteristics". In: *Mater. Sci. Eng.* 729.012001 (2020). DOI: 10.1088/1757-899X/729/1/012001.

[33] Z. Cheng et al. "How to report and benchmark emerging field-effect transistors". In: *Nature Electronics* 5 (2022), pp. 416–423. DOI: 10.1038/s41928-022-00798-8.

[34] D. A. Neamen. *SEMICONDUCTOR PHYSICS & DEVICES: BASIC PRINCIPLES, FOURTH EDITION*. McGraw-Hill, 2012. ISBN: 978-0-07-352958-5.

[35] V. K. Khanna. "Short-Channel Effects in MOSFETs". In: *Integrated Nanoelectronics* (2016), pp. 73–93. DOI: 10.1007/978-81-322-3625-2_5.

[36] G. Arutchelvan et al. "Impact of device scaling on the electrical properties of MoS_2 field-effect transistors". In: *Scientific Reports* 11.6610 (2021). DOI: 10.1038/s41598-021-85968-y.

[37] I. Ferain, C. A. Colinge, and J-P Colinge. "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors". In: *Nature* 479 (2011), pp. 310–316. DOI: 10.1038/nature10676.

[38] H. Ilatikhameneh et al. "Saving Moore's Law Down To 1nm Channels With Anisotropic Effective Mass". In: *Scientific Reports* 6.31501 (2016). DOI: 10.1038/srep31501.

[39] X. Huang, C. Liu, and P. Zhou. "2D semiconductors for specific electronic applications: from device to system". In: *npj 2D Materials and Applications volume* 6.51 (2022). DOI: 10.1038/s41699-022-00327-3.

[40] S. Manzeli et al. "2D transition metal dichalcogenides". In: *Nature Reviews Materials* 2.17033 (2017). DOI: 10.1038/natrevmats.2017.33.

[41] N. H. Patoary et al. "Improvements in 2D p-type WSe_2 transistors towards ultimate CMOS scaling". In: *Sci Rep* 13.3304 (2023). DOI: 10.1038/s41598-023-30317-4.

[42] A. K. Geim and I. V. Grigorieva. "Van der Waals heterostructures". In: *Nature* 499 (2013), pp. 419–425. DOI: 10.1038/nature12385.

[43] V. Podzorov et al. "High-mobility field-effect transistors based on transition metal dichalcogenides". In: *Appl. Phys. Lett.* 84.17 (2004), pp. 3301–3303. DOI: 10.1063/1.1723695.

[44] X. Tang et al. "Distorted Janus Transition Metal Dichalcogenides: Stable Two-Dimensional Materials with Sizable Band Gap and Ultrahigh Carrier Mobility". In: *The Journal of Physical Chemistry* 122.33 (2018), pp. 19153–19160. DOI: 10.1021/acs.jpcc.8b04161.

[45] A-S. Chou et al. “Antimony Semimetal Contact with Enhanced Thermal Stability for High Performance 2D Electronics”. In: (2021), pp. 7.2.1–7.2.4. DOI: 10.1109/IEDM19574.2021.9720608.

[46] S. Das et al. “Transistors based on two-dimensional materials for future integrated circuits”. In: *Nat Electron* 4 (2021), pp. 786–799. DOI: 10.1038/s41928-021-00670-1.

[47] Q. Guo et al. “Strain engineering and mechanical assembly of silicon/germanium nanomembranes”. In: *Materials Science and Engineering: R: Reports* 128 (2018), pp. 1–31. DOI: 10.1016/j.mser.2018.02.002.

[48] H. Nan et al. “Soft hydrogen plasma induced phase transition in monolayer and few-layer $MoTe_2$”. In: *Nanotechnology* 30 (2019). DOI: 10.1088/1361-6528/aaebc5.

[49] S. Kanungo et al. “2D materials-based nanoscale tunneling field effect transistors: current developments and future prospects”. In: *npj 2D Materials and Applications* 6.83 (2022). DOI: 10.1038/s41699-022-00352-2.

[50] S. B. Mitta et al. “Electrical characterization of 2D materials-based field-effect transistors”. In: *2D Mater.* 8.1 (2020), p. 012002. DOI: 10.1088/2053-1583/abc187.

[51] A. Sharma1 et al. “Large area, patterned growth of 2D MoS_2 and lateral MoS_2–WS_2 heterostructures for nano- and opto-electronic applications”. In: *Nanotechnology* 31.25 (2020). DOI: 10.1088/1361-6528/ab7593.

[52] U.T. Uthappa et al. “Trends and prospects of 2-D tungsten disulphide (WS_2) hybrid nanosystems for environmental and biomedical applications”. In: *Advances in Colloid and Interface Science* 322.103024 (2023). DOI: 10.1016/j.cis.2023.103024.

[53] S-K. Su et al. “Layered Semiconducting 2D Materials for Future Transistor Applications”. In: *Small Structures* 2.5 (2021), p. 2000103. DOI: 10.1002/sstr.202000103.

[54] K-T. Chen and S-T. Chang. “How high can the mobility of monolayer tungsten disulfide be?” In: *Vacuum* 140 (2017), pp. 172–175. DOI: 10.1016/j.vacuum.2016.11.006.

[55] Z. Jin et al. “Intrinsic transport properties of electrons and holes in monolayer transition-metal dichalcogenides”. In: *Phys. Rev. B* 90.4 (2014).

[56] A. Sebastian et al. “Benchmarking monolayer MoS_2 and WS_2 field-effect transistors”. In: *Nat Commun* 12.693 (2021). DOI: 10.1038/s41467-020-20732-w.

[57] J. T. Mlack et al. “Transfer of monolayer TMD WS_2 and Raman study of substrate effects”. In: *Scientific Reports* 7.43037 (2017). DOI: 10.1038/srep43037.

[58] M. Mupparapu, T. Bucher, and I. Staude. “Integration of two-dimensional transition metal dichalcogenides with Mie-resonant dielectric nanostructures”. In: *Advances in Physics: X* 5 (2020), p. 1734083. DOI: 10.1080/23746149.2020.1734083.

[59] M. Sharma et al. “Large-Area Transfer of 2D TMDCs Assisted by a Water-Soluble Layer for Potential Device Applications”. In: *ACS Omega* 7.14 (2022), pp. 11731–11741. DOI: 10.1021/acsomega.1c06855.

[60] A. Md. Hoque et al. "Spin-valley coupling and spin-relaxation anisotropy in all-CVD Graphene-MoS_2 van der Waals heterostructure". In: *Phys. Rev. Mater.* 7.4 (2023), p. 044005. DOI: 10.1103/PhysRevMaterials.7.044005.

[61] D. Jena, K. Banerjee, and G. H. Xing. "Intimate contacts". In: *Nature Materials* 13 (2014), pp. 1076–1078. DOI: 10.1038/nmat4121.

[62] A. Allain et al. "Electrical contacts to two-dimensional semiconductors". In: *Nature Materials* 14 (2015), pp. 1195–1205. DOI: 10.1038/nmat4452.

[63] J. Kang et al. "Computational Study of Metal Contacts to Monolayer Transition-Metal Dichalcogenide Semiconductors". In: *Phys. Rev. X* 4.3 (2014), p. 031005. DOI: 10.1103/PhysRevX.4.031005.

[64] S. Das et al. "High Performance Multilayer MoS_2 Transistors with Scandium Contacts". In: *Nano Letters* 13.1 (2013), pp. 100–105. DOI: 10.1021/nl303583v.

[65] H. Liu, A. T. Neal, and P. D. Ye. "Channel Length Scaling of MoS_2 MOSFETs". In: *ACS Nano* 6.10 (2012), pp. 8563–8569. DOI: 10.1021/nn303513c.

[66] H. Liu et al. "Statistical Study of Deep Submicron Dual-Gated Field-Effect Transistors on Monolayer Chemical Vapor Deposition Molybdenum Disulfide Films". In: *Nano Letters* 13.6 (2013), pp. 2640–2646. DOI: 10.1021/nl400778q.

[67] Y. Wang and M. Chhowalla. "Making clean electrical contacts on 2D transition metal dichalcogenides". In: *Nat Rev Phys* 4 (2022), pp. 101–112. DOI: 10.1038/s42254-021-00389-0.

[68] C. Kim et al. "Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides". In: *ACS Nano* 11.2 (2017), pp. 1588–1596. DOI: 10.1021/acsnano.6b07159.

[69] D. Rhodes et al. "Disorder in van der Waals heterostructures of 2D materials". In: *Nat. Mater.* 18 (2019), pp. 541–549. DOI: 10.1038/s41563-019-0366-8.

[70] S. McDonnell et al. "Defect-Dominated Doping and Contact Resistance in MoS_2". In: *ACS Nano* 8.3 (2014), pp. 2880–2888. DOI: 10.1021/nn500044q.

[71] M-H. Lee et al. "Two-Dimensional Materials Inserted at the Metal/Semiconductor Interface: Attractive Candidates for Semiconductor Device Contacts". In: *Nano Letters* 18.8 (2018), pp. 4878–4884. DOI: 10.1021/acs.nanolett.8b01509.

[72] J. H. Werner and H. H. Güttler. "Temperature dependence of Schottky barrier heights on silicon". In: *J. Appl. Phys.* 73.3 (1993), pp. 1315–1319. DOI: 10.1063/1.353249.

[73] A. Toriumi et al. "Opportunities and challenges for Ge CMOS – Control of interfacing field on Ge is a key". In: *Microelectronic Engineering* 86.7–9 (2009), pp. 1571–1576. DOI: 10.1016/j.mee.2009.03.052.

[74] D. E. Eastman and J. L. Freeouf. "Photoemission Partial Yield Measurements of Unoccupied Intrinsic Surface States for Ge(111) and GaAs(110)". In: *Phys. Rev. Lett.* 33.27 (1974), pp. 1601–1605. DOI: 10.1103/PhysRevLett.33.1601.

[75] Z. Zhang et al. "Flat bands in twisted bilayer transition metal dichalcogenides". In: *Nature Physics* 16 (2020), pp. 1093–1096. DOI: 10.1038/s41567-020-0958-x.

[76] G. Abbas et al. “Recent Advances in Twisted Structures of Flatland Materials and Crafting Moiré Superlattices”. In: *Adv. Funct. Mater.* 30.36 (2020), p. 2000878. DOI: 10.1002/adfm.202000878.

[77] S. Carr, S. Fang, and E. Kaxiras. “Electronic-structure methods for twisted moiré layers”. In: *Nat Rev Mater* 5 (2020), pp. 748–763. DOI: 10.1038/s41578-020-0214-0.

[78] L. Wang et al. “Correlated electronic phases in twisted bilayer transition metal dichalcogenides”. In: *Nat. Mater.* 19 (2020), pp. 861–866. DOI: 10.1038/s41563-020-0708-6.

[79] A. Jorio. “Twistronics and the small-angle magic”. In: *Nature Materials* 21 (2022), pp. 844–845. DOI: 10.1038/s41563-022-01290-6.

[80] M. Yankowitz et al. “Emergence of superlattice Dirac points in graphene on hexagonal boron nitride”. In: *Nature Phys* 8 (2012), pp. 382–386. DOI: 10.1038/nphys2272.

[81] K. Kim et al. “Tunable moiré bands and strong correlations in small-twist-angle bilayer graphene”. In: 114.13 (2017), pp. 3364–3369. DOI: 10.1073/pnas.16201401.

[82] Y. Pan et al. “Quantum-Confined Electronic States Arising from the Moiré Pattern of MoS_2–WSe_2 Heterobilayers”. In: *Nano Letters* 18.3 (2018), pp. 1849–1855. DOI: 10.1021/acs.nanolett.7b05125.

[83] H. Yoo et al. “Atomic and electronic reconstruction at the van der Waals interface in twisted bilayer graphene”. In: *Nat. Mater.* 18 (2019), pp. 448–453. DOI: 10.1038/s41563-019-0346-z.

[84] Y. Choi et al. “Electronic correlations in twisted bilayer graphene near the magic angle”. In: *Nat. Phys.* 15 (2019), pp. 1174–1180. DOI: 10.1038/s41567-019-0606-5.

[85] A. Kerelsky et al. “Maximized electron interactions at the magic angle in twisted bilayer graphene”. In: *Nature* 572 (2019), pp. 95–100. DOI: 10.1038/s41586-019-1431-9.

[86] Y. Jiang et al. “Charge order and broken rotational symmetry in magic-angle twisted bilayer graphene”. In: *Nature* 573 (2019), pp. 91–95. DOI: 10.1038/s41586-019-1460-4.

[87] Y. Xie et al. “Spectroscopic signatures of many-body correlations in magic-angle twisted bilayer graphene”. In: *Nature* 572 (2019), pp. 101–105. DOI: 10.1038/s41586-019-1422-x.

[88] B. Hunt et al. “Massive Dirac Fermions and Hofstadter Butterfly in a van der Waals Heterostructure”. In: *SCIENCE* 340.6139 (2013), pp. 1427–1430. DOI: 10.1126/science.12372.

[89] C. R. Dean et al. “Hofstadter’s butterfly and the fractal quantum Hall effect in moiré superlattices”. In: *Nature* 497 (2013), pp. 598–602. DOI: 10.1038/nature12186.

[90] L. A. Ponomarenko et al. “Cloning of Dirac fermions in graphene superlattices”. In: *Nature* 497 (2013), pp. 594–597. DOI: 10.1038/nature12187.

[91] Y. Cao et al. “Correlated insulator behaviour at half-filling in magic-angle graphene superlattices”. In: *Nature* 556 (2018), pp. 80–84. DOI: 10.1038/nature26154.

[92] Y. Cao et al. “Unconventional superconductivity in magic-angle graphene superlattices”. In: *Nature* 556 (2018), pp. 43–50. DOI: 10.1038/nature26160.

[93] H. Li et al. “Twisted moiré conductive thermal metasurface”. In: *Nat Commun* 15.2169 (2024). DOI: 10.1038/s41467-024-46247-2.

[94] T. Devakul et al. “Magic in twisted transition metal dichalcogenide bilayers”. In: *Nature Communications* 12.6730 (2021). DOI: 10.1038/s41467-021-27042-9.

[95] Y. Li et al. “Recent progress on the mechanical exfoliation of 2D transition metal dichalcogenides”. In: *Mater. Res. Express* 9.12 (2022). DOI: 10.1088/2053-1591/aca6c6.

[96] E. Gao et al. “Mechanical exfoliation of two-dimensional materials”. In: *Journal of the Mechanics and Physics of Solids* 115 (2018), pp. 248–262. DOI: 10.1016/j.jmps.2018.03.014.

[97] Y. Huang et al. “Universal mechanical exfoliation of large-area 2D crystals”. In: *Nat Commun* 11.2453 (2020). DOI: 10.1038/s41467-020-16266-w.

[98] K. H. Ruiz et al. “Chemical Vapor Deposition Mediated Phase Engineering for 2D Transition Metal Dichalcogenides: Strategies and Applications”. In: *Small Science* 2.1 (2022). DOI: 10.1002/smsc.202100047.

[99] Y. Yuan et al. “Probing the Twist-Controlled Interlayer Coupling in Artificially Stacked Transition Metal Dichalcogenide Bilayers by Second-Harmonic Generation”. In: *ACS Nano* 17.18 (2023), pp. 17897–17907. DOI: 10.1021/acsnano.3c03795.

[100] T. Zhang et al. “One-Step CVD Growth and Interlayer Coupling Characteristics of Twisted MoS_2/MoS_2/MoS_2 Homotrilayers”. In: *The Journal of Physical Chemistry C* 127.48 (2023), pp. 23420–23427. DOI: 10.1021/acs.jpcc.3c05832.

[101] M. Xu et al. “Reconfiguring nucleation for CVD growth of twisted bilayer MoS_2 with a wide range of twist angles”. In: *Nat Commun* 15.562 (2024). DOI: 10.1038/s41467-023-44598-w.

[102] H. G. Ji et al. “Stacking Orientation-Dependent Photoluminescence Pathways in Artificially Stacked Bilayer WS_2 Nanosheets Grown by Chemical Vapor Deposition: Implications for Spintronics and Valleytronics”. In: *ACS Applied Nano Materials* 4.4 (2021), pp. 3717–3724. DOI: 10.1021/acsanm.1c00192.

[103] S. K. Mallik et al. “Polarized Moiré Phonon and Strain-Coupled Phonon Renormalization in Twisted Bilayer MoS_2”. In: *The Journal of Physical Chemistry C* 126.37 (2022), pp. 15788–15794. DOI: 10.1021/acs.jpcc.2c04201.

[104] Y. Xu et al. “A tunable bilayer Hubbard model in twisted WSe_2”. In: *Nat. Nanotechnol.* 17 (2022), pp. 934–939. DOI: 10.1038/s41565-022-01180-7.

[105] J. Cai et al. “Signatures of fractional quantum anomalous Hall states in twisted $MoTe_2$”. In: *Nature* 622 (2023), pp. 63–68. DOI: 10.1038/s41586-023-06289-w.

[106] D. Pei et al. “Twist-Induced Modification in the Electronic Structure of Bilayer WSe_2”. In: *Nano Letters* 23.15 (2023), pp. 7008–7013. DOI: 10.1021/acs.nanolett.3c01672.

[107] S. Kim et al. “Thickness-controlled black phosphorus tunnel field-effect transistor for low-power switches”. In: *Nat. Nanotechnol.* 15 (2020), pp. 203–206. DOI: 10.1038/s41565-019-0623-7.

[108] D. Khokhriakov et al. “Robust Spin Interconnect with Isotropic Spin Dynamics in Chemical Vapor Deposited Graphene Layers and Boundaries”. In: *ACS Nano* 14.11 (2020), pp. 15864–15873. DOI: 10.1021/acsnano.0c07163.

[109] A. Chaves et al. “Bandgap engineering of two-dimensional semiconductor materials”. In: *npj 2D Mater Appl* 4.29 (2020). DOI: 10.1038/s41699-020-00162-4.

[110] H. Yang et al. “Identification and Structural Characterization of Twisted Atomically Thin Bilayer Materials by Deep Learning”. In: *Nano Letters* 24.9 (2024), pp. 2789–2797. DOI: 10.1021/acs.nanolett.3c04815.

[111] X. Zhang et al. “Transition metal dichalcogenides bilayer single crystals by reverse-flow chemical vapor epitaxy”. In: *Nat Commun* 10.598 (2019). DOI: 10.1038/s41467-019-08468-8.

[112] D. Dumcenco et al. “Large-Area Epitaxial Monolayer MoS_2”. In: *ACS Nano* 9.4 (2015), pp. 4611–4620. DOI: 10.1021/acsnano.5b01281.

[113] Z. Gao et al. “Recent advances in the properties and synthesis of bilayer graphene and transition metal dichalcogenides”. In: *J. Phys. Mater.* 3.4 (2020). DOI: 10.1088/2515-7639/abb58d.

[114] M. Xia et al. “Spectroscopic Signatures of AA’ and AB Stacking of Chemical Vapor Deposited Bilayer MoS_2”. In: *ACS Nano* 9.12 (2015), pp. 12246–12254. DOI: 10.1021/acsnano.5b05474.

[115] S. V. Mandyam et al. “Controlled Growth of Large-Area Bilayer Tungsten Diselenides with Lateral P–N Junctions”. In: *ACS Nano* 13.9 (2019), pp. 10490–10498. DOI: 10.1021/acsnano.9b04453.

[116] Q. Zhang et al. “Two-Dimensional Layered Heterostructures Synthesized from Core–Shell Nanowires”. In: *Angew. Chem. Int. Ed.* 54 (2015), pp. 8957–8960. DOI: 10.1002/anie.201502461.

[117] J. Zhang et al. “Observation of Strong Interlayer Coupling in MoS_2/WS_2 Heterostructures”. In: *Adv. Mater.* 28 (2015), pp. 1950–1956. DOI: 10.1002/adma.201504631.

[118] S. M. T-S. Afrid. “Defect engineered magnetism induction and electronic structure modulation in monolayer MoS_2”. In: *Heliyon* 10.1 (2024), e23384. DOI: 10.1016/j.heliyon.2023.e23384.

[119] I. S. Kim et al. “Influence of Stoichiometry on the Optical and Electrical Properties of Chemical Vapor Deposition Derived MoS_2”. In: *ACS Nano* 8.10 (2014), pp. 10551–10558. DOI: 10.1021/nn503988x.

[120] L. Fang et al. “Direct bilayer growth: a new growth principle for a novel WSe_2 homo-junction and bilayer WSe_2 growth”. In: *Nanoscale* 12 (2020), pp. 3715–3722. DOI: 10.1039/C9NR09874G.

[121] L. Fang et al. “Quick Optical Identification of the Defect Formation in Monolayer WSe_2 for Growth Optimization”. In: *Nanoscale Res Lett* 14.274 (2019). DOI: 10.1186/s11671-019-3110-z.

[122] P. K. Chow et al. “Defect-Induced Photoluminescence in Monolayer Semiconducting Transition Metal Dichalcogenides”. In: *ACS Nano* 9.2 (2015), pp. 1520–1527. DOI: 10.1021/nn5073495.

[123] S. Zhao et al. “Strong room-temperature emission from defect states in CVD-grown WSe_2 nanosheets”. In: *Nano Res.* 11 (2018), pp. 3922–3930. DOI: 10.1007/s12274-018-1970-7.

[124] R. Ko, D. H. Lee, and H. Yoo. “Annealing and Doping Effects on Transition Metal Dichalcogenides—Based Devices: A Review”. In: *Coatings* 13.8 (2023), p. 1364. DOI: 10.3390/coatings13081364.

[125] M. W. Iqbal et al. “Tailoring the electrical and photo-electrical properties of a WS_2 field effect transistor by selective n-type chemical doping”. In: *RSC Adv.* 6 (2016), pp. 24675–24682. DOI: 10.1039/C6RA02390H.

[126] S Jo et al. “Mono- and Bilayer WS2 Light-Emitting Transistors”. In: *Nano Letters* 14.4 (2014), pp. 2019–2025. DOI: 10.1021/nl500171v.

[127] C. Zhou et al. “Interfacial properties of 2D WS2 on SiO2 substrate from X-ray photoelectron spectroscopy and first-principles calculations”. In: *Front. Phys.* 17.53500 (2022). DOI: 10.1007/s11467-022-1167-0.

[128] D. Thakur et al. “Layer number dependent optical and electrical properties of CVD grown two-dimensional anisotropic WS2”. In: *Surfaces and Interfaces* 26.101308 (2021). DOI: 10.1016/j.surfin.2021.101308.

[129] M. Khan et al. “Investigation of the annealing temperature for few-layer MoS_2 and ion-beam induced athermal annealing/purification behaviour by in-situ XRD”. In: *Applied Surface Science* 639.158106 (2023). DOI: 10.1016/j.apsusc.2023.158106..

[130] J. Cai et al. “Atomic Layer Deposition of Two-Dimensional Layered Materials: Processes, Growth Mechanisms, and Characteristics”. In: *Matter* 2.3 (2020), pp. 587–630. DOI: 10.1016/j.matt.2019.12.026.

[131] M. Ji and W. Choi. “Performance enhancement of WS_2 transistors via double annealing”. In: *Microelectronic Engineering* 255.111709 (2022). DOI: 10.1016/j.mee.2022.111709.

A
Fabrication

This appendix offers a more detailed explanation of the fabrication process conducted for this thesis. All of the steps were performed in the Nanofabrication laboratory at Chalmers University of Technology.

A.1 Fabrication of WS_2-Homostructures

In this master's thesis, devices were produced from twisted 2D structures of CVD-grown WS_2, with Ti/Au used as the contact material. The complete fabrication recipe is presented below, with Figure A.1 illustrating the complete process.

A.1.1 Chip Preparation

A 7 mm x 7 mm Si/SiO_2 chip was used in this fabrication. First, the substrate was cleaned with acetone at 50 °C for $\approx$ 5 minutes followed by room-temperature IPA for an additional $\approx$ 5 minutes. Subsequently, N_2 was used to dry the substrate. It was then put under an optical microscope to verify proper cleaning and ensure the absence of damage or contamination.

A.1.2 Transfer of WS_2

The transfer of WS_2 to the Si/SiO_2 substrate was achieved using a wet transfer process. First, the Si/SiO_2 substrate was cleaned using acetone and IPA, as described above. Then, the edges of a substrate coated with CVD-grown WS_2 were lightly scratched with a scalpel and placed in a beaker of deionised (DI) water. The scratches on the substrate allowed for DI-water to flow in between the substrate and the layer of WS_2, causing the latter to detach from the substrate and float to the surface. The Si/SiO_2 substrate was then submerged in the DI-water and carefully raised towards the surface to collect the material. Thus, the WS_2 had been placed on the Si/SiO_2 substrate. The substrate was placed on a hot plate to dry as well as to improve the uniformity of the material. During the transfer process, a layer of resist covering the WS_2 was also transferred. To remove this layer, the substrate was cleaned with acetone and IPA, thereby isolating the WS_2. The same procedure was performed several times in an attempt to stack multiple layers of WS_2 with an angle. Due to the random nature of such a transfer, it was difficult to know how to correctly place the material with a relative orientation. Following each transfer attempt, the substrate was examined under an optical microscope to assess the

success of the transfer. After the third attempt, several multilayer overlaps were observed and WS_2-homostructures had formed with a clear twist angle. Images of these structures were captured.

A.1.3 Spin Coating

The Si/SiO_2 substrate containing WS_2-homostructures was spin coated with two positive resists. First, MMA 8.5 EL8 was applied with a spin coating duration of 60 seconds and a rotation speed of 6000 rpm. The substrate was then put on a hot plate for curing at 135 °C for 10 minutes. Thereafter, ARP 6200 was applied and spin coated for 60 seconds at 6000 rpm, followed by curing on the hot plate for 10 minutes at 135 °C.

A.1.4 Mask Design

Mask designs were created using AutoCAD software. Images taken of the WS_2-homostructures were properly aligned and regions of interest on the chip for making devices were identified and marked accordingly. Afterwards, the substrate was patterned using electron beam lithography and developed to dissolve the exposed part of the resists. During the development, the chip was placed in a small beaker containing Amyl acetate for $\approx$ 45 seconds. Immediately after, it was placed in another beaker containing MIBK:IPA 1:1 for $\approx$ 1 minute and 15 seconds, followed by drying with N_2 to ensure complete removal of any residual solvent. Finally, the desired device structure was defined through CHF_3 plasma etching for $\approx$ 40 seconds, after which the chip was cleaned with acetone and IPA.

Subsequently, a second spin coating process, identical to the prior one, ensued to allow for contact placement. AutoCAD software was once again utilised to draw two types of contacts: for high and low currents. The polyline function improved the otherwise high aspect ratio between these two types. The drawn contacts were marked with numbers and letters to easily distinguish between different contacts and devices. A second cycle of EBL was performed to expose the areas where contacts were to be deposited. Lastly, these exposed areas were dissolved through development, using the same development process as described above.

A.1.5 Contact Deposition

After development, the chip underwent a physical vapour deposition (PVD) process in which contact materials were deposited onto the exposed areas. 20 nm of Ti followed by 80 nm of Au was deposited via electron beam evaporation at a high vacuum. Following this deposition, lift-off was performed to remove the resists and deposited metals everywhere else than the designated contact areas. For this, the chip was placed in acetone and subsequently IPA, through the same procedure as described previously.

A.1.6 Low-Temperature Annealing

Annealing has been found to improve the crystallinity of a sample and enhance electronic properties [124]. A particular advantage of annealing TMDs is the elimination of defects, which will enhance overall device performance. With contacts deposited, the chip was annealed in an environment of H_2 and Ar gas, at 180 °C for 120 minutes.

A.1.7 Second Annealing Procedure

After low-temperature annealing, devices on the chip were measured. Overall, the results of the measurements demonstrated lacking device performance. In an attempt to improve the crystallinity and electronic properties of the chip, annealing was performed for a second time, this time at a temperature of 250 °C. The second annealing procedure lasted 6 hours in a H_2 and Ar environment.

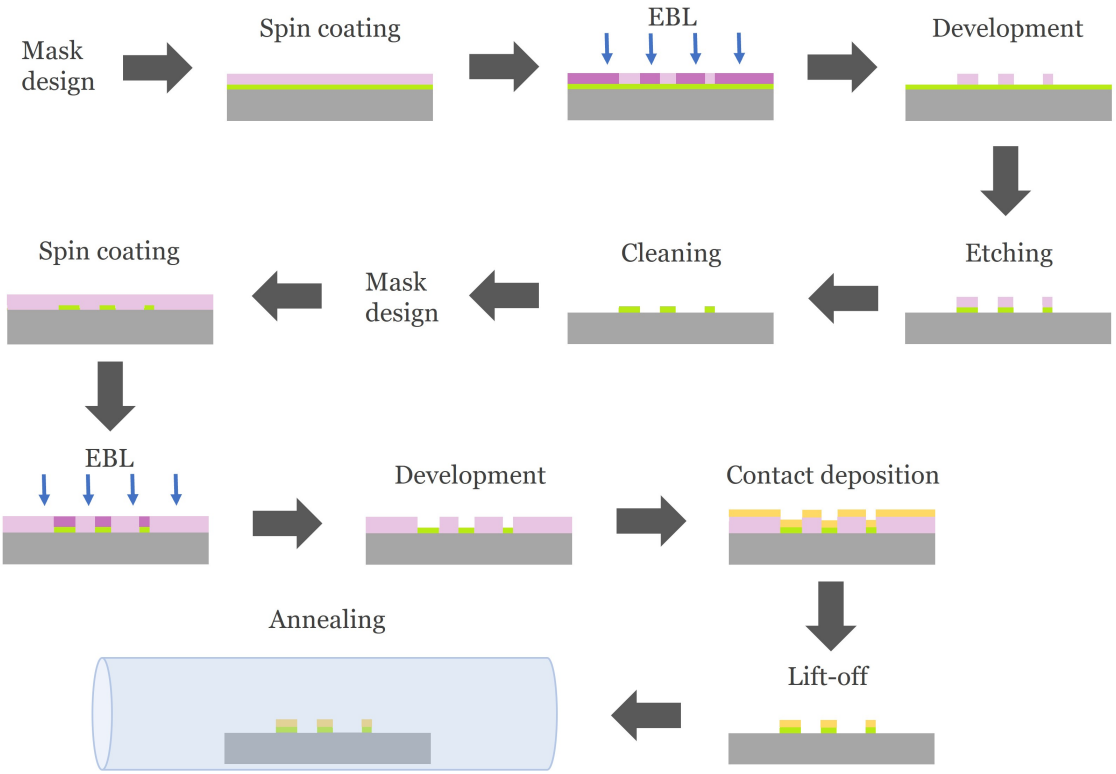


Figure A.1: Illustration of the complete fabrication process. After the mask design, the substrate was spin coated and exposed with EBL. Development and etching removed unwanted material before the chip was cleaned and resists were removed. A second mask design was performed for the contacts before the chip was spin coated and exposed with EBL for a second time. After development, Ti/Au contacts were deposited. After lift-off, the substrate was annealed.

B

Measurements

Herein follows a detailed view of the measurement process. All measurements were performed in spintronics laboratories at Chalmers.

B.1 Measuring Fabricated Devices of WS_2-Homostructures with Ti/Au Contacts

In this thesis work, devices of WS_2-homostructures with Ti/Au contacts were successfully fabricated and measurements were performed. A detailed version of the steps taken in this process is seen below.

B.1.1 Device Bonding

The Si/SiO_2 substrate containing WS_2-homostructures with deposited Ti/Au contacts was placed in a chip holder. Silver paste was applied on the surface of this chip holder, with the chip being placed and gently pressed to ensure secure placement. Of the fabricated devices on the chip, three were selected for measurements. A wire bonding machine was then used to bond these three devices. With a 10 µm gold wire, the machine created electrical connections between them and the terminals on the chip holder.

B.1.2 Measurement Setup

With devices bonded, the chip was placed in a microstat wherein the high vacuum environment prevented contamination and interference with the measurements. Labview software was solely utilised to devise different measurement processes, allowing for various transistor parameters to be measured. To verify that the contacts were working properly and to get a glimpse of the behaviour of the devices, a series of basic tests were conducted between each of the contacts and for each device. Thereafter, output- and transfer characteristics were measured systematically.

Output characteristics were acquired by measuring I_D at a fixed V_g while varying V_{ds} between either -5 V and 5 V, or -10 V and -10 V. After measuring these parameters across the sweep range, V_g was changed, and the same measurement was conducted once again. I_D was first measured at a V_g of -70 V, after which this was changed to -60 V, then -50 V all the way to 70 V. Transfer characteristics were acquired by instead measuring I_D at a fixed V_{ds}, while V_g was swept between -70

V and 70 V. The interval of V_{ds} was from -5 V to 5 V. In conducting these measurements, a comprehensive view of the parameters of the device could be acquired. After completing measurements on bonded devices, new devices were selected and the process was repeated.

C

Excluded Measurements

As a result of the overall low performance of the fabricated devices, not all measurements are presented in this research. Those devices which were excluded from the main part of the thesis are instead presented here. I-V characteristics of some measurement sets are presented below.

C.0.1 Transport Measurements of CVD-Grown WS_2-Homostructures at Room Temperature

C.0.1.1 0° Twist Angle (Device 7)

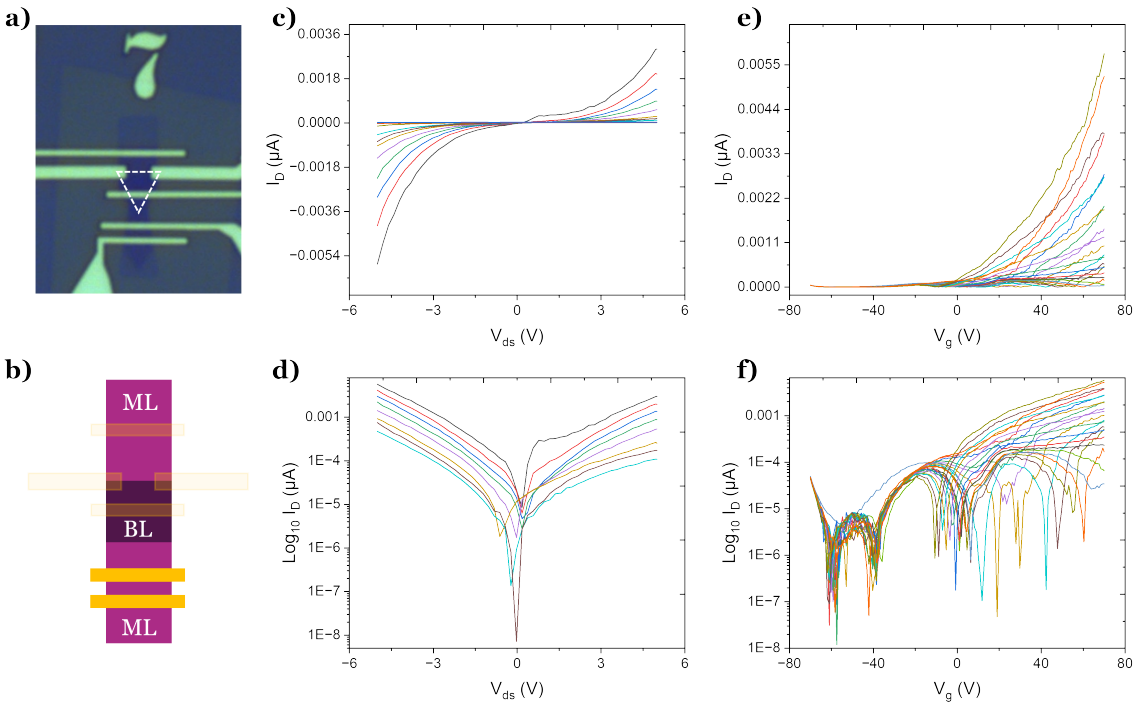


Figure C.1: I-V characteristics of a ML region of the 0°-device. **a)** Optical image of the device. **b)** Illustration of the device. **c)** Output characteristics in a linear scale. **d)** Output characteristics in a logarithmic scale. **e)** Transfer characteristics in a linear scale. **f)** Transfer characteristics in a logarithmic scale.

C.0.2 Transport Measurements of CVD-Grown WS_2-Homostructures After Second Annealing

Due to the overall lack of performance observed after the first set of transport measurements, annealing was performed on the chip for a second time, in an attempt to improve its performance. The first annealing iteration was conducted at a relatively low temperature of 180 °C for 2 hours. Previous research has indicated that improvements in the crystallinity of 2D TMD samples are observed at temperatures of several hundred degrees, suggesting that a temperature of 180 °C may be too low [129, 130]. Furthermore, in some instances, a double annealing procedure was performed, which resulted in considerably higher mobility than if annealing was performed once [124, 131].

As a result, the chip was annealed again, this time at 250 °C for a duration of 6 hours. Subsequently, identical measurements as those presented in section 4.1 were performed for the same devices to investigate whether or not a second annealing procedure would improve device performance. Unfortunately, a second annealing had the opposite effect, and device performance worsened even further.

C.0.2.1 No Twist Angle (Device 14)

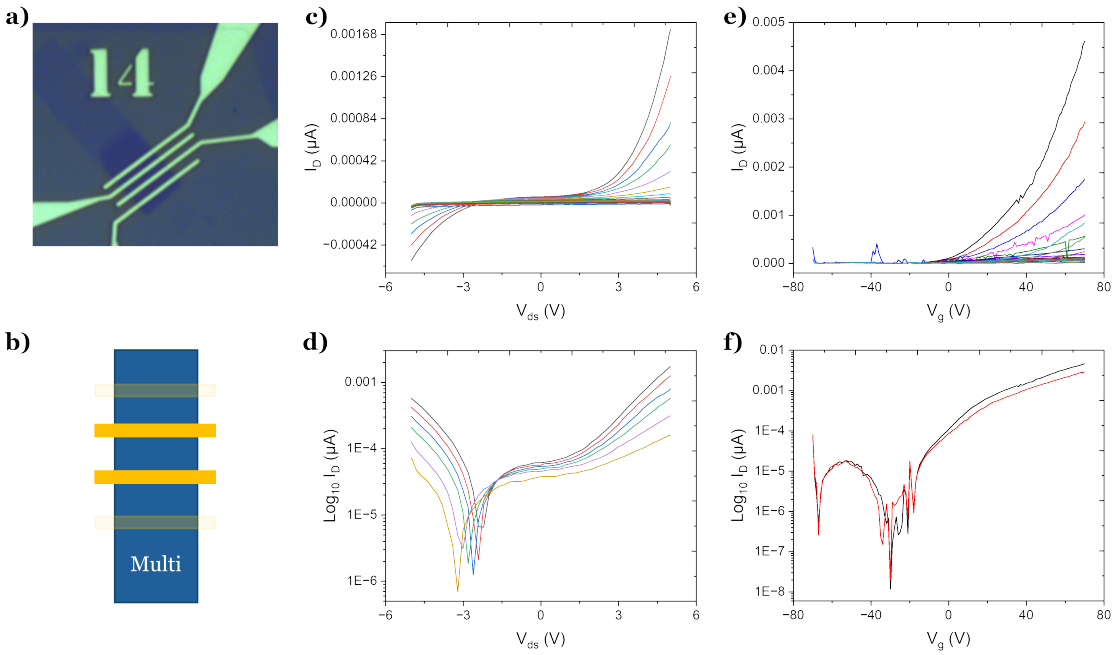


Figure C.2: I-V characteristics of the device without a twist angle. **a)** Optical image of the device. **b)** Illustration of the device. **c)** Output characteristics in a linear scale. **d)** Output characteristics in a logarithmic scale. **e)** Transfer characteristics in a linear scale. **f)** Transfer characteristics in a logarithmic scale.

C.0.2.2 0° Twist Angle (Device 7)

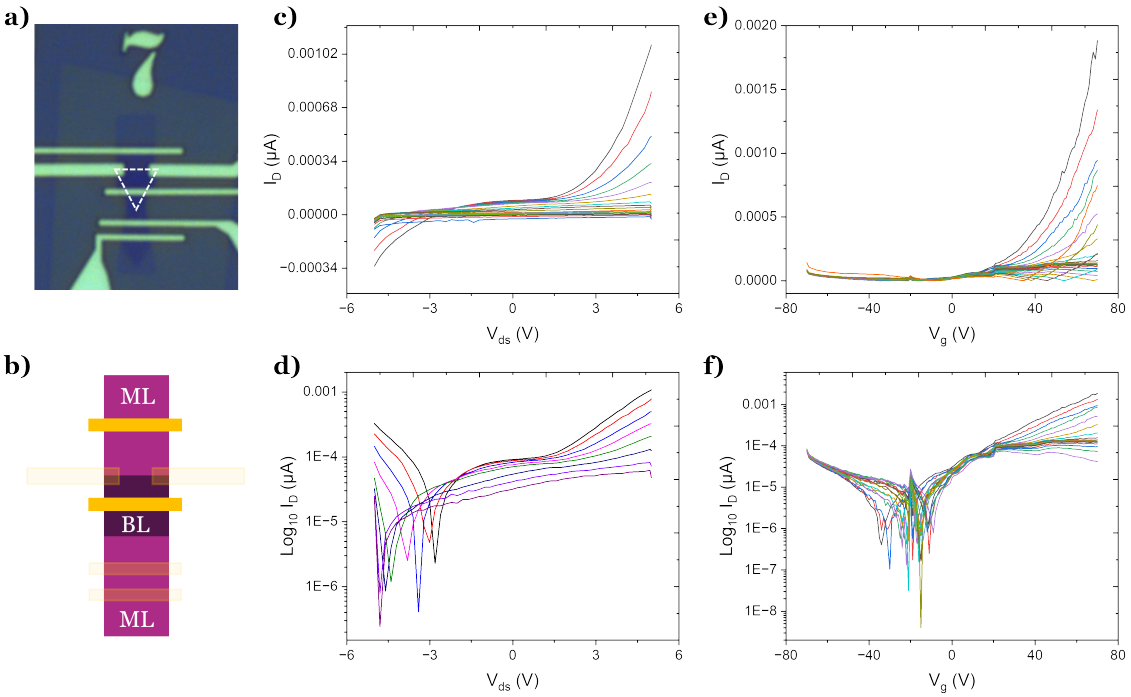


Figure C.3: I-V characteristics of the 0°-device with measurements performed over the first ML-BL junction. **a)** Optical image of the device. **b)** Illustration of the device. **c)** Output characteristics in a linear scale. **d)** Output characteristics in a logarithmic scale. **e)** Transfer characteristics in a linear scale. **f)** Transfer characteristics in a logarithmic scale.

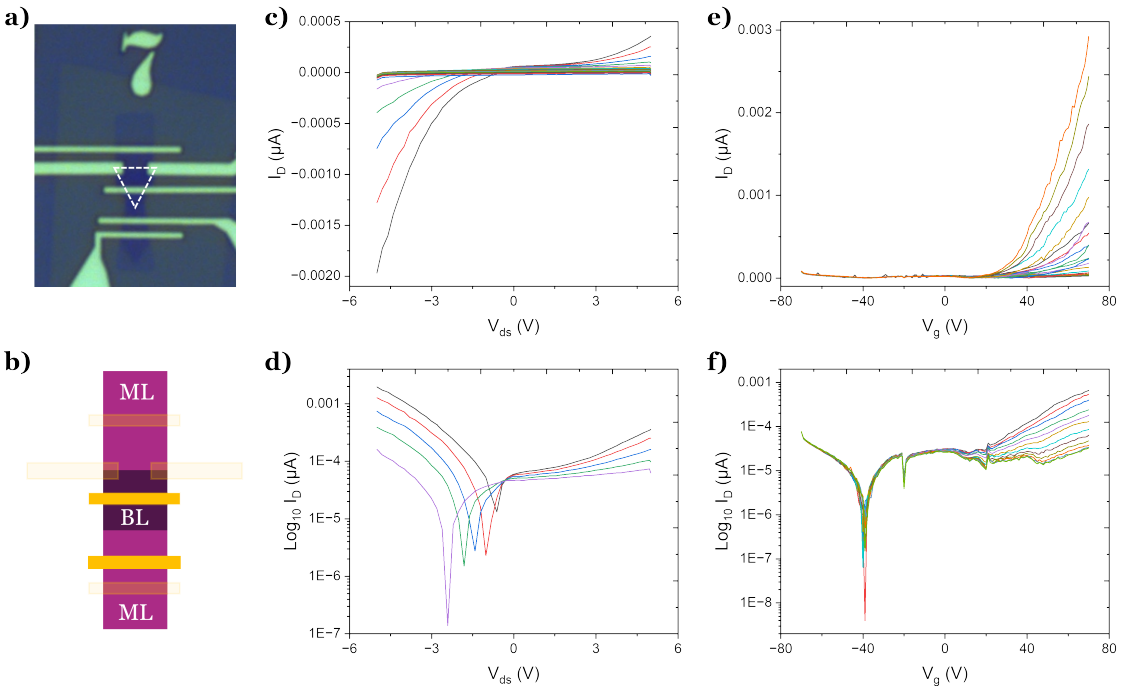


Figure C.4: I-V characteristics of the second junction of the 0°-device. **a)** Optical image of the device. **b)** Illustration of the device. **c)** Output characteristics in a linear scale. **d)** Output characteristics in a logarithmic scale. **e)** Transfer characteristics in a linear scale. **f)** Transfer characteristics in a logarithmic scale.

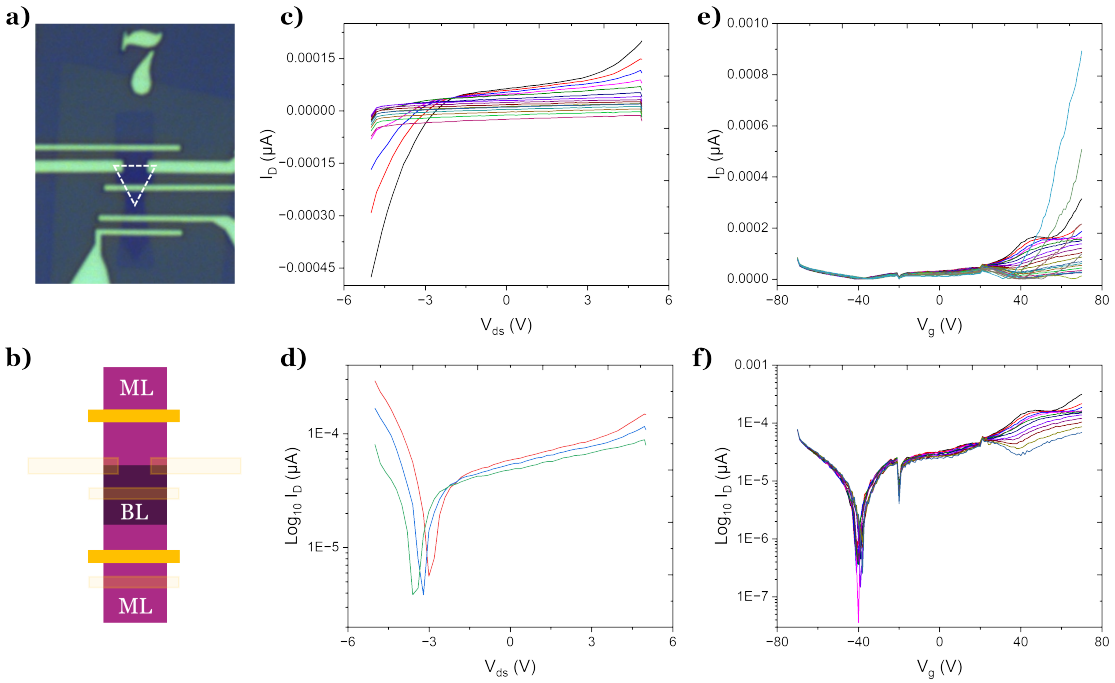


Figure C.5: I-V characteristics of the 0°-device, measured over both ML-BL junctions. **a)** Optical image of the device. **b)** Illustration of the device. **c)** Output characteristics in a linear scale. **d)** Output characteristics in a logarithmic scale. **e)** Transfer characteristics in a linear scale. **f)** Transfer characteristics in a logarithmic scale.

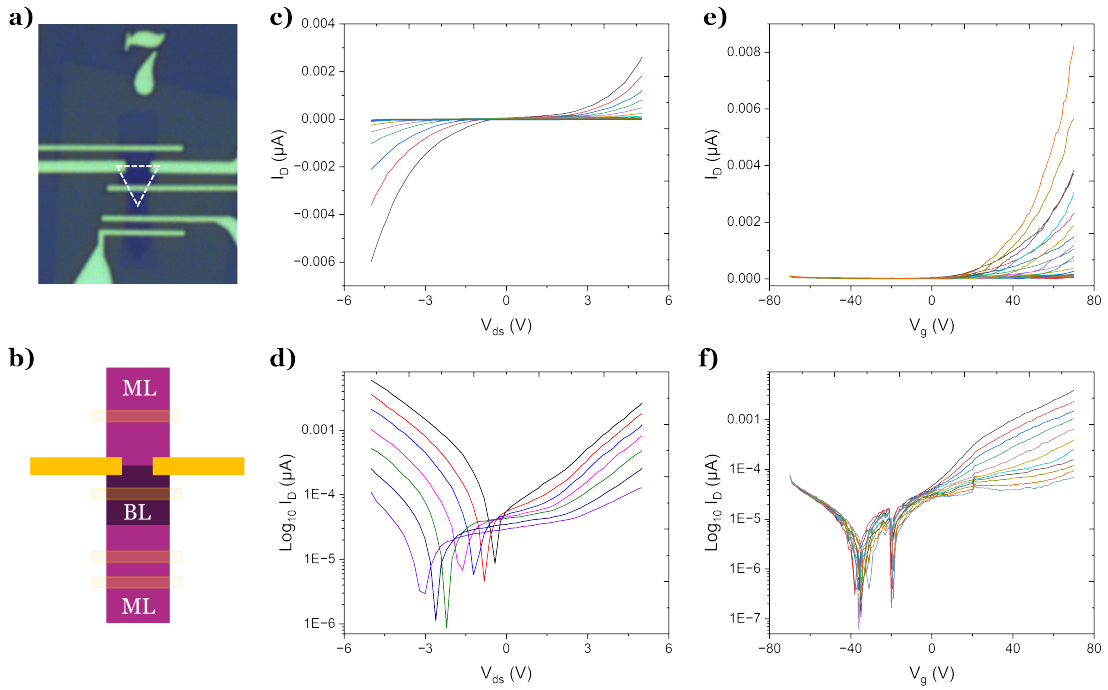


Figure C.6: I-V characteristics across the ML-BL junction of the 0°-device. **a)** Optical image of the device. **b)** Illustration of the device. **c)** Output characteristics in a linear scale. **d)** Output characteristics in a logarithmic scale. **e)** Transfer characteristics in a linear scale. **f)** Transfer characteristics in a logarithmic scale.

C.0.2.3 60° Twist Angle (Device 5)

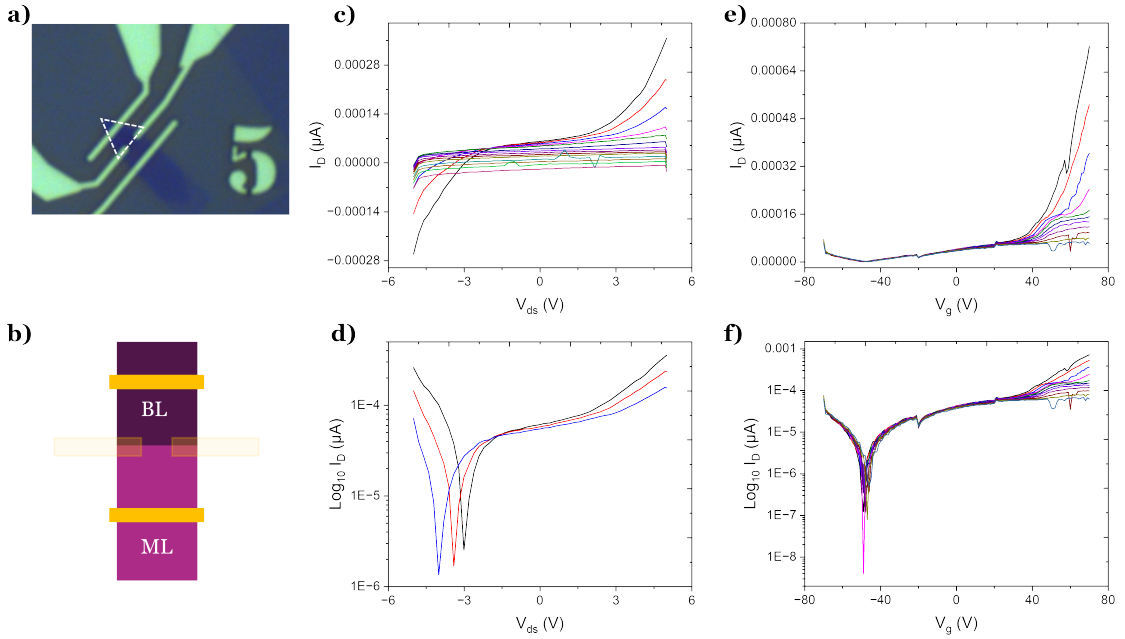


Figure C.7: I-V characteristics of the 60°-device, measured over the ML-BL junction. **a)** Optical image of the device. **b)** Illustration of the device. **c)** Output characteristics in a linear scale. **d)** Output characteristics in a logarithmic scale. **e)** Transfer characteristics in a linear scale. **f)** Transfer characteristics in a logarithmic scale.

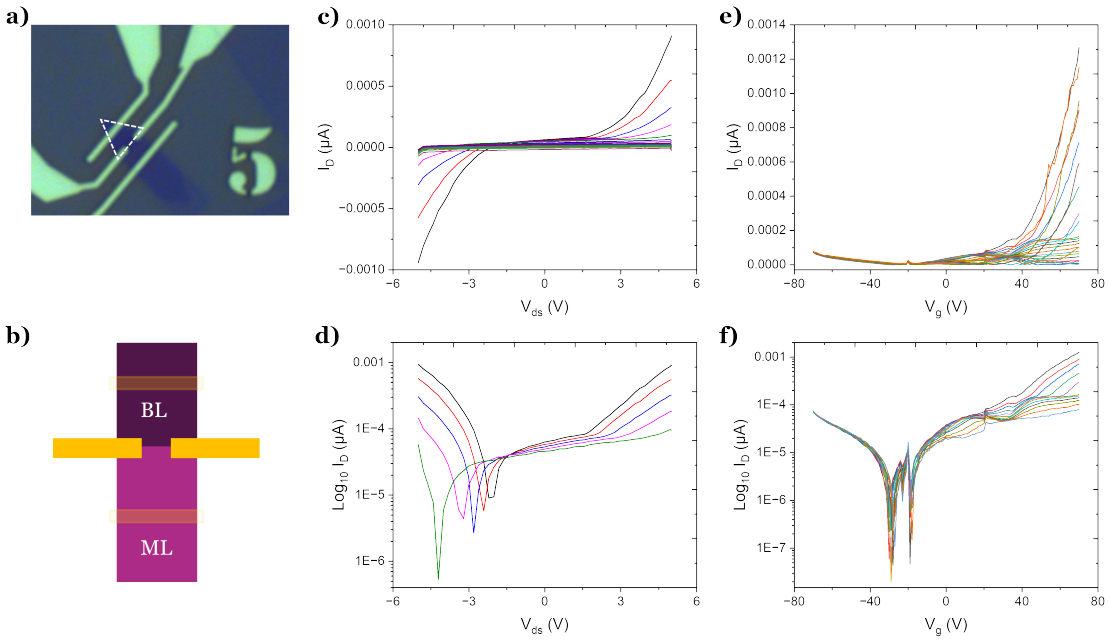


Figure C.8: I-V characteristics of the 60°-device, measured across the ML-BL junction. **a)** Optical image of the device. **b)** Illustration of the device. **c)** Output characteristics in a linear scale. **d)** Output characteristics in a logarithmic scale. **e)** Transfer characteristics in a linear scale. **f)** Transfer characteristics in a logarithmic scale.

D

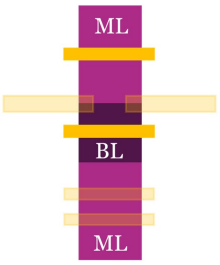
Compilation of Parameters

Herein follows a complete compilation of the extracted parameters. Figure D.1 presents each measurement configuration alongside a table of the extracted parameters for this configuration.

a)

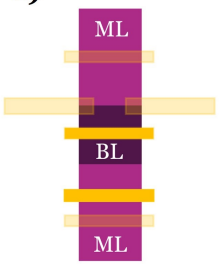
On/Off	$1*10^4$
SS	2.17 V/dec
$W_{channel}$	5 µm
$L_{channel}$	0.63 µm
μ_{FE}	0.007 $cm^2/V*s$
V_{th}	46.9 V

b)



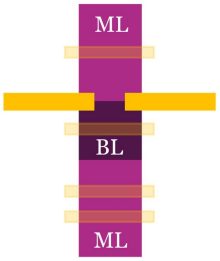
On/Off	$1*10^3$
SS	3.28 V/dec
$W_{channel}$	2.7 µm
$L_{channel}$	2.6 µm
μ_{FE}	0.03 $cm^2/V*s$
V_{th}	37.6 V

c)



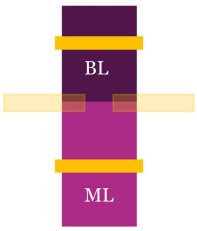
On/Off	$1*10^1$
SS	8.6 V/dec
$W_{channel}$	2.35 µm
$L_{channel}$	1.86 µm
μ_{FE}	0.0007 $cm^2/V*s$
V_{th}	23.8 V

d)



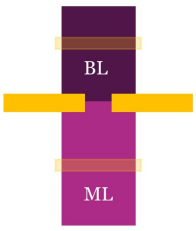
On/Off	$1*10^3$
SS	8.3 V/dec
$W_{channel}$	1 µm
$L_{channel}$	1.8 µm
μ_{FE}	0.02 $cm^2/V*s$
V_{th}	36.3 V

e)



On/Off	$1*10^1$
SS	2 V/dec
$W_{channel}$	2.6 µm
$L_{channel}$	2.5 µm
μ_{FE}	0.003 $cm^2/V*s$
V_{th}	42.5 V

f)



On/Off	$1*10^2$
SS	19.8 V/dec
$W_{channel}$	0.5 µm
$L_{channel}$	0.87 µm
μ_{FE}	0.017 $cm^2/V•s$
V_{th}	39.9 V

Figure D.1: Paramaters for each of the measurement configuration **a)** The device without a twist angle. **b)** Over the first ML-BL junction of the 0°-device. **c)** Over the second junction of the 0°-device. **d)** Across the first ML-BL junction of the 0°-device. **e)** Over the BL-ML junction of the 60°-device. **f)** Across the BL-ML junction of the 60°-device.

DEPARTMENT OF SOME SUBJECT OR TECHNOLOGY
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden
www.chalmers.se

CHALMERS
UNIVERSITY OF TECHNOLOGY