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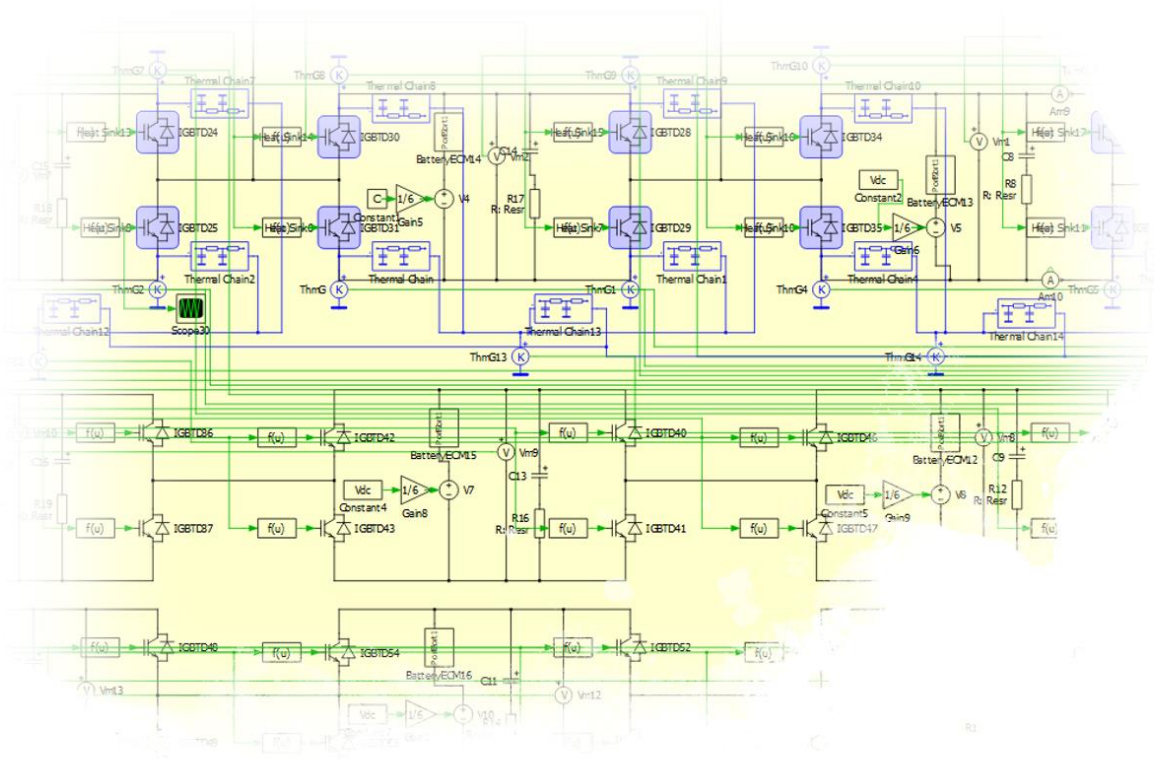

Output Voltage Modulation for Cascaded H-Bridge Inverters including Thermal and Battery SoC Balancing in Vehicle Traction Applications

Master's thesis in Electrical Power Engineering

LUKAS BAUM

DEPARTMENT OF ELECTRICAL ENGINEERING
Division of Electrical Power Engineering

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Cover:
Screenshot of a PLECS simulation model of the 7-level-3-phase cascaded H-bridge inverter including thermal LPNs used for the assessment of a thermal balancing algorithm in this work.

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Abstract

In traction applications, two-level inverters are commonly used. Multilevel inverters can provide benefits in efficiency and output voltage quality, as known for power system applications. This work analyzes different aspects of cascaded H-bridge multilevel inverters especially for traction applications. The inverter is simulated, considering efficiency and harmonic distortions, for the whole operating region of a permanent magnet synchronous machine. The findings are verified using a representative laboratory setup. Compared to a two-level inverter, the analyzed cascaded H-bridge multilevel inverter allows for significant increases in efficiency as inverter losses are approximately halved. Different switching strategies are analyzed, such as pulse width modulated switching and fundamental frequency switching with selective harmonic elimination. A strategy is developed, combining the advantages of both switching techniques. Additionally, a thermal balancing strategy is proposed, resulting in a reduction of the temperature differences between switches with up to 67 %. Furthermore, cascaded H-bridge multilevel inverters allow for novel possibilities of balancing the individual battery packs. Here, different state of charge balancing strategies are proposed and experimentally validated.

Keywords: Conduction Losses, Electric Vehicle, Efficiency, Multilevel Converters, Multilevel Inverters, SoC Balancing, Switching Losses, Thermal Balancing

Contents

1 Introduction

1.1 Problem Background and Previous Work

Slowing down and reducing the effects of a changing climate due to massive greenhouse emissions already is and will be the challenge of the twenty-first century. One aspect is reducing or, in the best case, avoiding greenhouse emissions caused by individual transport. Besides making public transport more attractive, the change from fossil fuel-powered to electric vehicles is a matter that manufacturers and the public highly focuses on. A significant challenge is to increase the range of electric vehicles enough to allow for a similar use as with fossil-fuel-powered vehicles.

Thus, electric vehicle drive systems require highly efficient power electronics, especially for the drive train inverters. Due to their low component count and maturity, two-level inverters are widely used [1–5]. To further reduce harmonic distortion [6], electromagnetic emissions [7] and switching losses [8, 9], as well as allowing the use of low voltage MOSFETs, multilevel inverters became an interesting option [10–12]. Furthermore, multilevel inverters allow for a fault tolerant operation of the drive train [13]. Different topologies and switching techniques are used to obtain optimal performance and minimal losses for different operation regions [14–16]. While multilevel inverters are well known for applications in power systems, they are not yet commonly used for traction applications.

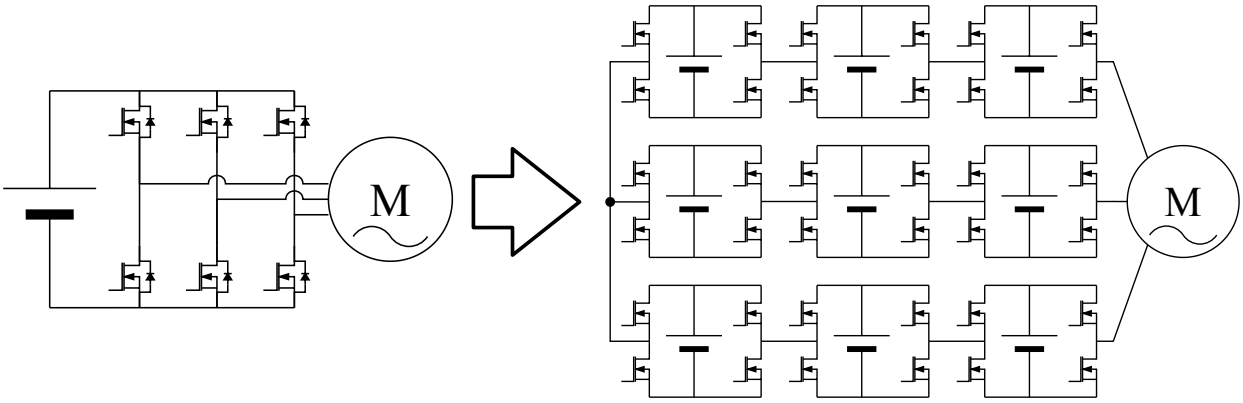


Figure 1.1.1: *Inverter topologies: From a two-level to a cascaded H-bridge 7-level inverter*

The general function of the inverter in a drive application is to synthesize the desired output voltage wave shape to drive the electric machine, mainly three-phase and possibly of pure sinusoidal voltage of variable frequency. While one goal is to avoid distortion of the output from the desired waveform (reducing total harmonic distortion (THD)), another, in most cases contradicting, goal is to reduce switching losses by reducing the switching frequency. Here the first part of the thesis links in and investigates the performance and efficiency of different switching techniques for different operation regions of the traction machine.

Another central aspect of the development of battery electric vehicles (BEV) is energy storage. Commonly used lithium-based batteries are usually considered to be the most critical

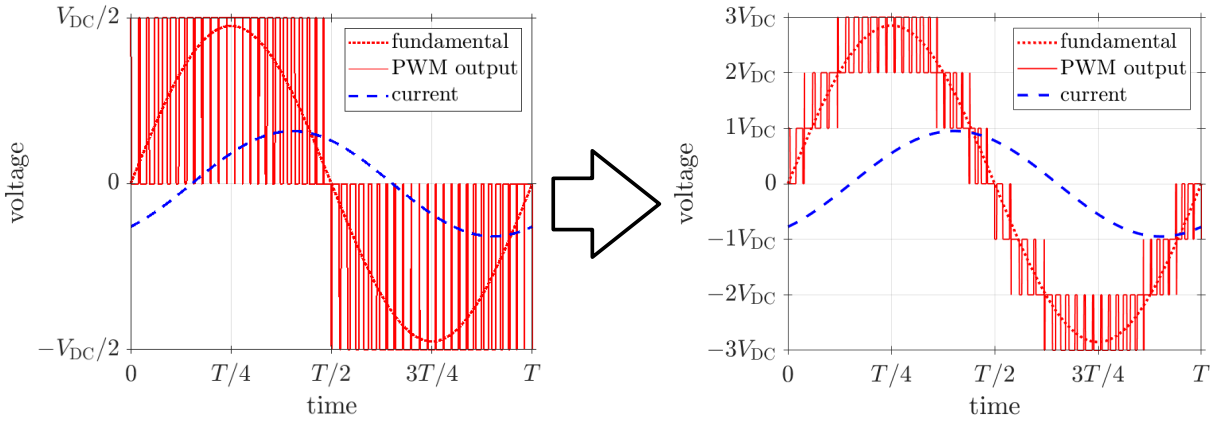


Figure 1.1.2: *Output voltage: From a two-level to a cascaded H-bridge 7-level inverter*

component concerning lifetime but as well in terms of sustainability. Considering the three pillars of sustainability, ecologic, economic and social aspects, it is important to use the battery in the best possible way. The extraction of the raw materials might impose geopolitical concerns, as the majority of the lithium extraction takes place in politically unstable or questionable regions as Argentina, Bolivia, Chile, and China. As well, the lithium extraction from salt lake brines imposes ecological and social challenges, as it lowers ground water levels, which instead imposes challenges for agriculture and the general access to fresh water for the local population. The extraction from sea water is technically possible but very challenging as very large volumes of water are required [17]. Furthermore the social risks imposed by the supply of cobalt are a concern, as production conditions in high-risk countries such as D.R. Congo are not appropriate [18]. These aspects of the production of Li-ion batteries directly affect the United Nations Sustainable Development Goals as, among others, aiming for good health, clean water, and reduced inequalities [19].

An important aspect of their operation is to ensure that each cell is operated only inside its safe operation area (SOA). Boundaries of the SOA are lower and upper voltage, current and temperature limits [20, 21]. To allow for maximum use of the battery capacity, the cells must reach their SOA boundaries simultaneously. For this reason, it is necessary to balance the state of charge (SoC) of series-connected cells. Thus, the different techniques used to balance SoC of series-connected battery cells are a major factor of battery management. Two-level inverters require external balancing and battery management solutions, which allow for lossy passive or active balancing. With passive balancing, cells that have a higher voltage than the cell with the lowest voltage, are discharged over a bleeding resistor until all cells have the same voltage [22]. This method results in a complete loss of the unbalanced charges and energy. To partly avoid these losses, unbalanced cells can be connected in parallel for balancing, using suitable switches and current limiting resistors. This method, by principle, results in losses of at least 50% [23]. For a further increase of efficiency and flexibility, DC-DC converters or transformers can be used to control a current from cells with high cell voltage to cells with lower cell voltage, known as active balancing [22]. Depending on the balancing converter topology, high efficiencies can be achieved, but a separated balancing module is required. CHB multilevel inverter topologies directly enable battery balancing with the existing inverter hardware and in a proactive manner during regular operation. The switching techniques are adapted to prioritize the discharging of modules with higher SoC or respectively prioritize the charging of

modules with lower than average SoC [24]. This technique, in principle, could avoid balancing losses completely. Here, the second part of this thesis links in and aims to develop a balancing technique for multi-phase, multi-level cascaded H-bridge inverter systems.

Furthermore, it is necessary to balance the electrical stresses, both conduction and switching losses over all switches of the converter. Doing so will reduce temperature levels, on-state resistance and thus conduction losses, as well as generally prolonging the lifetime of the semiconductors [25] .

1.2 Purpose

The goal of this work is to analyze different control and switching techniques and strategies for multilevel inverters, especially cascaded H-bridge inverters. The aim is to assess different output voltage modulation strategies like pulse width modulation and fundamental frequency switching with selective harmonic elimination, considering efficiency, total harmonic distortion and weighted total harmonic distortion. The inverter is modeled, simulated and analyzed and an optimal control strategy, possibly using different modulation techniques for different operation points, is suggested. Furthermore, battery state of charge balancing between the inverter modules is investigated in different aspects as a proof of concept. Also, a proposal for battery balancing techniques for balancing unbalanced battery modules in one phase as well as between phases at standstill and during regular operation is a target. Finally, a concept for balancing thermal effects is simulated and validated.

1.3 Limitations

The thesis focuses on cascaded H-bridge multilevel inverters and the possibilities and challenges they create. Other inverter or multilevel inverter topologies are not assessed or discussed in detail. While in traction applications the inverter is combined with an electric machine in a drive system, the control of the electric machine is not discussed in detail. When verification is done with an experimental setup, the electric machine is substituted by a simple RL-load.

2 Concepts and Theory Background

2.1 Multilevel Inverter

In general, multilevel inverters have certain advantages like allowing a staircase output voltage waveform and lower dv/dt at switching compared to conventional two-level converters [11, 26]. This is desirable since high dv/dt during switching can cause motor bearing failure and stator winding insulation breakdown, as well as electromagnetic interference (EMI) [27]. Cascaded H-bridge multilevel inverters (CHB) use a series connection of H-bridge converters (Figure 2.1.2) to achieve the desired number of voltage levels [28]. This allows for a modular layout while keeping a low component count compared to other multilevel inverter topologies with the same number of voltage levels [29].

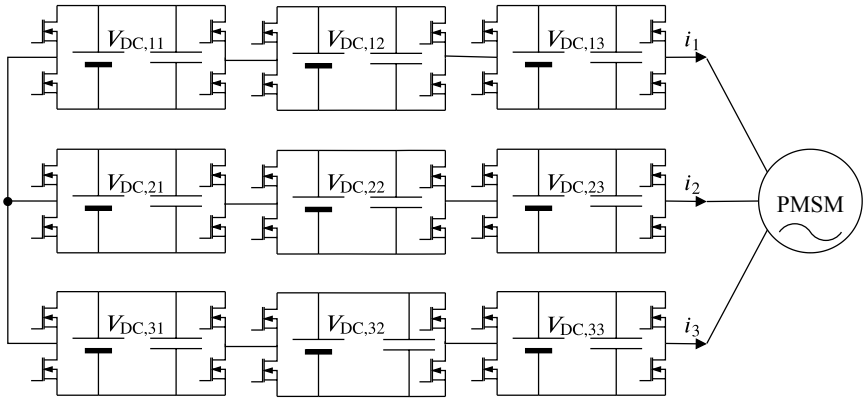
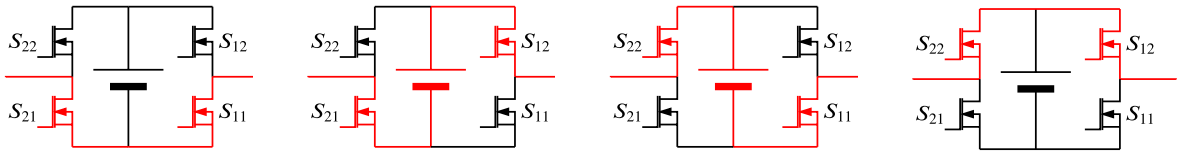


Figure 2.1.1: *7-Level-3-Phase cascaded H-bridge inverter*

CHB inverters allow the generation of high voltage outputs using a series connection of multiple low or medium voltage sources. Pushing the concept of CHB inverters to the extreme, using a series connection of single-cell DC-sources, completely eliminates the need for an external cell balancing, as will be discussed later. While multilevel inverters, in general, require a larger number of semiconductor devices and, thus, an increased amount of gate drivers, they allow for the use of cheaper lower-voltage MOSFETs [30].



(a) $V_{\text{out}} = 0\,\text{V}$ (b) $V_{\text{out}} = V_{\text{DC}}$ (c) $V_{\text{out}} = -V_{\text{DC}}$ (d) $V_{\text{out}} = 0\,\text{V}$

Figure 2.1.2: *H-bridge switching states where red color indicates the on and black the off state*

2.1.1 Switching Techniques for Multilevel Inverters

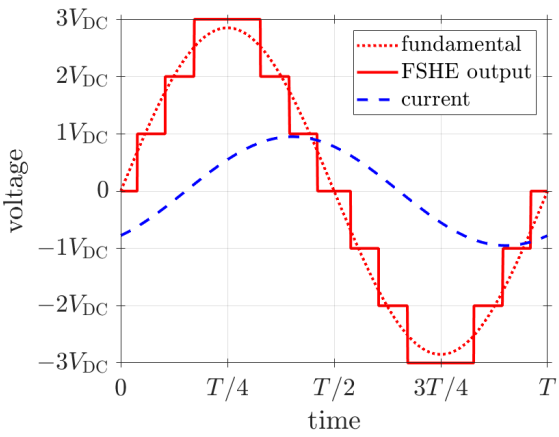


Figure 2.1.3: *FSHE modulation per phase output for a 7-level-inverter with equal DC voltages and* $M = 0.95$

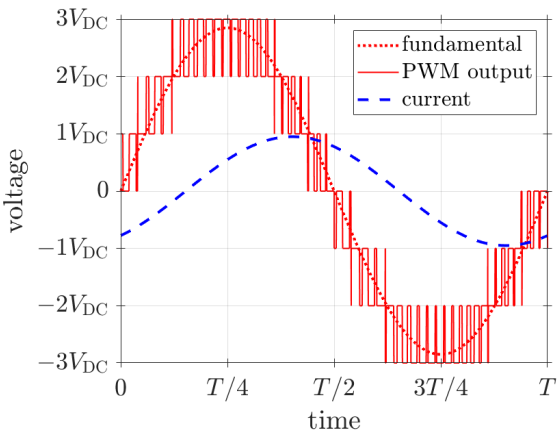


Figure 2.1.4: *PWM modulation per phase output for a 7-level-inverter with equal DC voltages and* $M = 0.95$, $f_1/f_{sw} = 0.035$

The output voltage of a cascaded H-bridge multilevel inverter is generated as a superposition of the output voltages of the respective H-bridge modules of each phase. Each H-bridge module has a DC voltage source that is connected to the output terminals in different ways. Apart from all switches being open, thus the H-bridge acting as an open circuit connection, there are four valid switching states shown in Figure 2.1.2. Figures 2.1.2a and 2.1.2d show the two redundant switching states with the H-bridge acting as a short circuit connection with an output voltage of zero. In terms of equalizing the losses over all switches, both, the upper and the lower, current paths should be equally used. Figure 2.1.2b shows the switching states with $V_{out} = V_{DC}$. Figure 2.1.2c shows the switching states with $V_{out} = -V_{DC}$. To generate the desired output voltage waveform, one has to cycle all modules between the four switching states in a useful way. Here, two switching techniques, fundamental frequency switching with selective harmonic elimination (FSHE) and pulse width modulation (PWM), appear to be the most commonly used approaches.

FSHE utilizes a staircase switching pattern as a superposition of fundamental frequency square waves by each H-bridge, as illustrated in Figure 2.1.3. Here, the so called firing angle is given as the delay by which the square wave is switched on and off, compared to a pure square wave. By adjusting the firing angles of every H-bridge, the output waveform can be controlled. The firing angles are commonly controlled to eliminate lower order harmonics. As shown by [31], for an 11-level inverter, the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic can be eliminated using this method. This modulation technique results in the lowest possible switching frequency. It is possible to be computed offline and recalled from lookup-tables. [31, 32]

PWM utilizes high-frequency square pulses with a modulated width, which is usually determined by comparing the (sinusoidal) modulation signal to a triangular carrier signal (SPWM). Each level of PWM output is added to the total voltage output, as illustrated in Figure 2.1.4.

Both switching techniques can be modulated using pre-calculated lookup tables, comparison with a carrier signal, or Space Vector Modulation (SVM). SVM uses the representation of the three-phase output voltages as a single vector in the $\alpha\beta$-plane to control the switching. Each

switching state is represented as a state variable for the voltage vector in the $\alpha\beta$-plane, which results in a hexagon for a two-level inverter. The output is now modulated by switching either in a fundamental frequency 6-step pattern from state to state or in a pulse width modulated manner between the adjacent states as Space Vector Modulated PWM (SVPWM). [33]

For a multilevel inverter, additional hexagonal layers of equilateral triangles, which surround the outermost hexagon, are formed with an increasing number of levels and the number of switching states increases cubic with the number of levels. This highly increases computational complexity [34]. Since the Park transformation from *abc* to $\alpha\beta$-frame is not uniquely reversible, third-order harmonics or a zero sequence can be added to increase the output voltages to a modulation index up to 1.15, without introducing low order harmonics at the output [33]. This can also be achieved using optimal zero sequence injection with SPWM.

While increasing the component count and complexity, more series-connected H-bridge modules allow for more voltage levels, a finer output voltage control and lower EMI. The same can also be achieved by an asymmetric CHB multilevel inverter with varying DC-voltage levels, e.g. V_{DC}, $2^1 \cdot V_{\mathrm{DC}}$, $2^2 \cdot V_{\mathrm{DC}}$,..., $2^n \cdot V_{\mathrm{DC}}$. This allows for $2^{n+1} - 1$ voltage levels, compared to the $2n + 1$ voltage levels possible for a multilevel inverter with n-series-connected H-bridges with equal DC-voltages [14]. For symmetrical/equal DC-voltages, the hexagonal structure of a five-level 3-phase inverter is symmetric and with 64 states, of which 37 states are unique/non-redundant, rather simple. It is therefore, even if computationally challenging, manageable. For non-equal DC-voltages of a 7-level-3-phase inverter instead, the structure is no longer symmetric, has up to 512 states of which 259 states being unique/non-redundant.

2.2 Harmonic Distortions

Due to the switching nature of a switched-mode converter, the output is always distorted relative to its (sinusoidal) reference. As a measurement for the quality of the output voltage, the ratio between the fundamental component of the output and the sum of all undesired higher harmonic components is defined as the voltage Total Harmonic Distortion ($\mathrm{THD_V}$) as

$$\mathrm{THD_V} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \quad . \tag{2.2.1}$$

With the quality of the output current as the primary interest, the Current Harmonic Distortion can be defined similarly as

$$\mathrm{THD_I} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} = \sqrt{\left(\frac{I^{\mathrm{RMS}}}{I_1^{\mathrm{RMS}}}\right)^2 - 1} \quad . \tag{2.2.2}$$

With the non-fundamental harmonic current components through an inductance approximated as $I_{\mathrm{n}} \approx V_{\mathrm{n}}/(n\omega_1 L)$ and normalized with $V_1/(\omega_1 L)$, the voltage Weighted Total Harmonic Distortion ($\mathrm{WTHD_V}$) can be defined as in [35] as

$$\mathrm{WTHD_V} = \frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{V_n}{n}\right)^2}}{V_1} \quad . \tag{2.2.3}$$

Compared to using the voltage $\mathrm{THD_V}$, the use of the voltage $\mathrm{WTHD_V}$ allows for a direct estimation of the current quality, as the weighting represents the fact that higher order current harmonics have less impact on the current quality trough an inductance.

2.2.1 Computation of the Fourier Spectrum

For the computation of the harmonic distortions, first, the measured or simulated waveforms have to be transformed from time to frequency domain using Fourier transform. Since both, the measured, as well as the simulated signals are sampled, a Discrete Fourier transform (DFT) has to be applied. The Matlab function fft(X) computes the Discrete Fourier transform of X using a Fast Fourier Transform (FFT) algorithm. If the signal is not equally sampled, it has to be re-sampled to a constant sampling rate. Then, a zero padded DFT is performed and evaluated at multiples of the fundamental frequency. From this data, the $\mathrm{THD_I}$ or $\mathrm{WHTD_V}$ can be computed, as in (2.2.2) and (2.2.3). A corresponding Matlab code is shown in Figure 2.2.1.

```
%% zero padded DFT
N_frame=4;
span=1/frequency*N_frame;
idx=find(time >= (time(end)-span),1);

T_sampling=diff(Time(idx:end);
T_sampling=T_sampling(1);
f_sampling=1/T_sampling;

L=size(Signal(idx:end),1);
L_padded=100*L;

FFT=fft(Signal(idx:end),L_padded);
FFT_freq=(0:L_padded-1)*(f_sampling/L_padded);
FFT=abs(FFT)/L*2;

fn=(f:f:1e6/2);
Hn=interp1(FFT_freq,FFT,fn);

THD=sqrt(sum(Hn(2:end).^2))/Hn(1);
WTHD=sqrt(sum((Hn(2:end)./(fn(2:end)./f)).^2))/Hn(1);
```

Figure 2.2.1: *Matlab code for zero padded DFT and THD/WHTD calculation*

2.3 Thermal Lumped Parameter Networks

To estimate and simulate the temperatures of components and systems, they can be described as lumped parameter nodes in thermal networks. In analogy to electric networks, the heat transfer rate or power $\dot{Q}$ [W] corresponds to the electric current, while the temperature T [K] corresponds to the electric potential. Thermal conductivity and capacity can be defined in analogy to electric conductivity and capacity. Similar to electric networks, the parameters can be lumped to represent whole components. A basic example of a thermal lumped parameter network is shown in Figure 2.3.1.

The thermal resistance between two components and the thermal capacitance of a component are then defined as

$$R_{\mathrm{th}} = \frac{T}{\dot{Q}} \quad [\mathrm{K\,W^{-1}}] \quad , \tag{2.3.1}$$

and

$$C_{\mathrm{th}} = \frac{dQ}{dT} \quad [\mathrm{J\,K^{-1}}] \quad , \tag{2.3.2}$$

with the electric loss power resulting in heat being represented as the heat power $\dot{Q}$ [W].

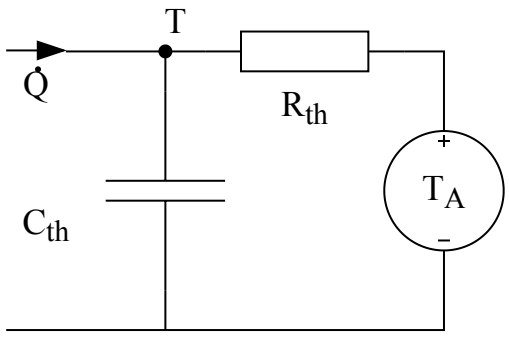


Figure 2.3.1: *Basic thermal LPN*

2.4 Battery Modeling

The battery, being the energy storage on-board a BEV, plays a major role in the development of drive systems. To properly take the dynamic behavior of battery cells and packs into consideration when analyzing drivetrain components, a model representation of the battery is required.

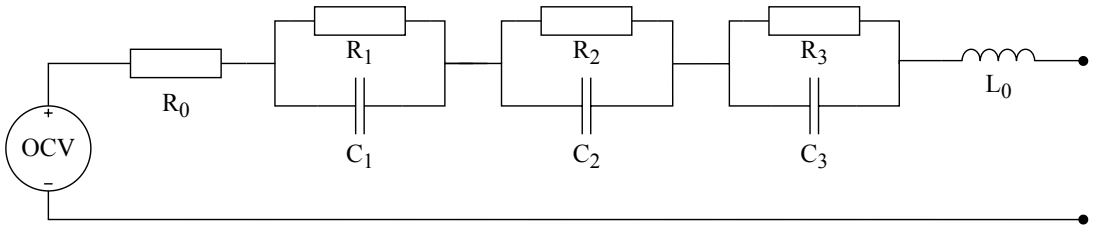


Figure 2.4.1: *Battery OCV-R-3RC-model*

For simulation purposes, each battery cell can be represented by an equivalent electric circuit model (ECM). Here it is possible to use a physics based ECM, with the components representing the physical and chemical processes inside the battery cell. If no knowledge about the cells construction is available, electrochemical impedance spectroscopy (EIS) can be performed

and the parameters of a mathematical model extracted. Here, the battery impedance can be modeled using a three time constant model with a series inductance and resistance as shown in Figure 2.4.1. Though, apart from the series resistance R_0, the components of the ECM do not represent specific physical or chemical processes in the cell. This model representation can be easily parameterized using EIS data as done in [8,36] and does represent the dynamic behavior of the battery cell sufficiently good.

2.5 PMSM Modeling and Control

In an electric vehicle, an electric machine is used to convert the stored electric energy to mechanical energy to propel the vehicle. Here, permanent magnet synchronous machines (PMSMs) are very popular due to their high efficiency, simplicity and ease of control [37].

In its basic principle, torque is produced by the alignment force between the field of an electromagnet (stator) and the field of a permanent magnet (rotor), rotating synchronously. The torque is thus, among other factors, dependent on the angle between the two fields, the load angle δ [38]. Since there are no excitation currents in the rotor, there are also no resistive losses in the rotor, which improves the motor's efficiency. The performance is highly dependent on the magnetic flux caused by the permanent magnets, thus by their size and materials. Unfortunately, materials like Neodymium, that high performance magnets are made of, are ethically and environmentally problematic. For example, in production regions in China the mining pollutes rivers being the primary water source for 150 million people. Also work conditions, even including exposure to radioactive material, are a concern [37]. [37] compared PMSM to rare earth free induction machines (IM), stating a global warming potential [kgCO2, eq] of 48.9 for a PMSM compared to 42 for a IM with conventional aluminum rotor bars. Here an evaluation of the benefits in sustainability of the IM versus the benefits in efficiency of the PMSM would have to be performed, but is not part of this work.

Using the Park transformation, the three-phase machine can be described in the rotating dq-frame. Here, the d-axis is aligned with the rotating magnetic flux. An equivalent circuit model of the PMSM in the dq-frame is shown in Figure 2.5.1, with the stator resistance R_s, the d- and q-axis inductance L_sd and L_sq, the electric rotational speed ω_r and the magnetic flux linkage Ψ_m.

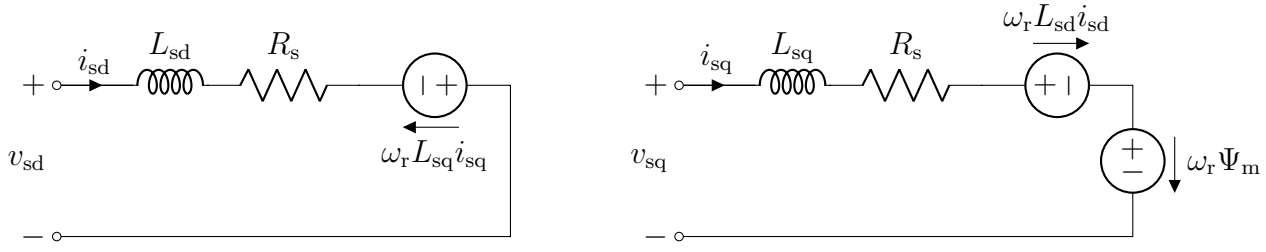


Figure 2.5.1: *PMSM equivalent circuit in direct-quadrature-frame*

With θ as the current angle, the current vector of magnitude I_s is expressed in the dq-plane as

$$\begin{aligned} i_\mathrm{sd} =& I_\mathrm{s}\cos(\theta) \\ i_\mathrm{sq} =& I_\mathrm{s}\sin(\theta) \quad . \end{aligned} \tag{2.5.1}$$

With the load angle δ as the angle between rotor and stator field, the voltage equations can be established as

$$\begin{aligned} v_\mathrm{sd} =& R_\mathrm{s} i_\mathrm{sd} + L_\mathrm{sd}\frac{di_\mathrm{sd}}{dt} - \omega_\mathrm{r} L_\mathrm{sq} i_\mathrm{sq} = V_\mathrm{s}\cos(\delta) \\ v_\mathrm{sq} =& R_\mathrm{s} i_\mathrm{sq} + L_\mathrm{sq}\frac{di_\mathrm{sq}}{dt} + \omega_\mathrm{r} L_\mathrm{sd} i_\mathrm{sd} + \omega_\mathrm{r}\Psi_\mathrm{m} = V_\mathrm{s}\sin(\delta) \quad . \end{aligned} \tag{2.5.2}$$

The torque is then derived as

$$T_e = \frac{3n_\mathrm{p}}{2}(\Psi_\mathrm{m} i_\mathrm{sq} + (L_\mathrm{sd} - L_\mathrm{sq}) i_\mathrm{sd} i_\mathrm{sq}) \quad . \tag{2.5.3}$$

Below base speed, the machine operation is restricted by the maximum current magnitude

$$I_\mathrm{s} = \sqrt{i_\mathrm{sd}^2 + i_\mathrm{sq}^2} \leq I_\mathrm{s,max} \quad , \tag{2.5.4}$$

and, thus, the maximum torque is restricted. This region is known as constant torque region. The torque can be maximized with respect to the current angle θ for a given current, using a maximum torque per current (MTPA) control strategy. Setting the derivative of (2.5.3) with respect to θ to zero and inserting (2.5.1), while assuming constant parameters, one can obtain

$$i_\mathrm{sd,MTPA}(i_\mathrm{sq}) = \frac{\Psi_\mathrm{m}}{2(L_\mathrm{sd} - L_\mathrm{sq})} - \sqrt{\left(\frac{\Psi_\mathrm{m}}{2(L_\mathrm{sd} - L_\mathrm{sq})}\right)^2 + i_\mathrm{sq}^2} \quad . \tag{2.5.5}$$

One can then derive $i_\mathrm{sq,MTPA}(T_e)$ by inserting (2.5.5) into (2.5.3) and solving numerically for i_sq [39].

Above base speed, the machine operation is restricted by the maximum voltage magnitude

$$V_\mathrm{s} = \sqrt{v_\mathrm{sd}^2 + v_\mathrm{sq}^2} \leq V_\mathrm{s,max} \quad . \tag{2.5.6}$$

Thus, the flux has to be weakened by injection of a negative d-axis current so that the back-EMF does not get higher than the supply voltage. This region is thus known as the field weakening or constant power region. For steady state, if the stator resistance is neglected, one can obtain

$$i_\mathrm{sd,FW}(i_\mathrm{sq}, \omega_\mathrm{r}, V_\mathrm{s,max}) = -\frac{\Psi_\mathrm{m}}{L_\mathrm{sd}} + \frac{1}{L_\mathrm{sd}}\sqrt{\left(\frac{V_\mathrm{s,max}}{\omega_\mathrm{r}}\right)^2 - (L_\mathrm{sq} i_\mathrm{sq})^2} \tag{2.5.7}$$

by inserting (2.5.2) into (2.5.6). One can then derive $i_\mathrm{sq,FW}(T_e, \omega_\mathrm{r}, V_\mathrm{s,max})$ by inserting (2.5.7) into (2.5.3) and solving numerically for i_sq [39].

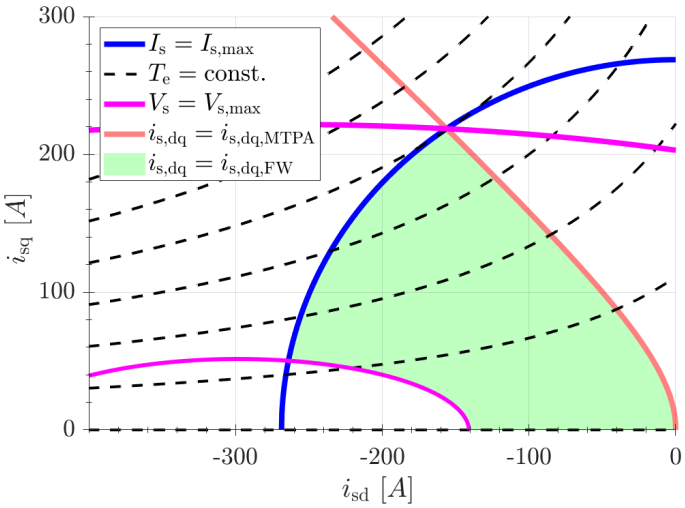


Figure 2.5.2: *dq-currents for the PMSM operation region*

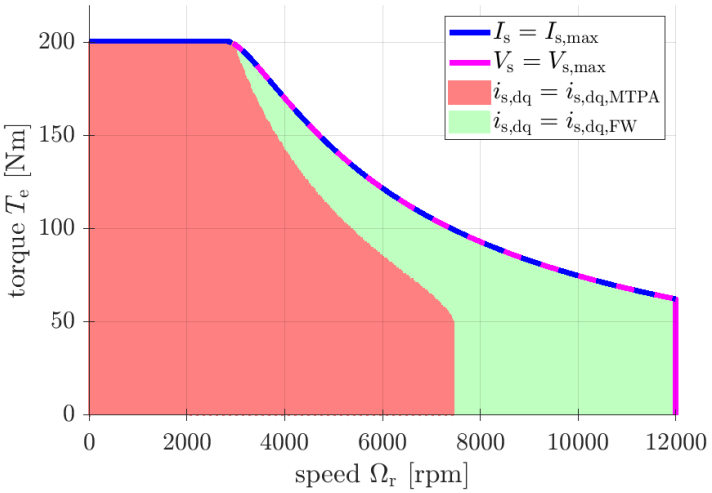


Figure 2.5.3: *PMSM operation region*

Figure 2.5.2 shows the resulting current trajectories for the MTPA control approach, as well as the circle formed by the maximum current magnitude and the maximum voltage ellipse, which shrinks with increasing speed. As long as the shrinking voltage ellipse does not cross the MTPA trajectory inside the current maximum, MTPA currents as given by (2.5.5) can be applied. This region corresponds with the indicated region shown in Figure 2.5.3. Above base speed, field weakening currents, as given by (2.5.7), have to be applied, as maximum torque and speed are limited by the maximum current magnitude and the voltage magnitude as indicated in Figures 2.5.2 and 2.5.3.

3 Simulation Model and Test Setup

The central part of this work is a set of simulations using MathWorks Simulink and Plexim PLECS. Here a simulation model of an electric drivetrain with a focus on the CHB multilevel inverter, the battery and thermal aspects, was used. The model is used to simulate different cases with the focus on different aspects. A model with the focus on the inverter losses is used to assess the efficiency and quality (THD_I, $WTHD_V$) of different output voltage modulation techniques like PWM and FSHE. A model with the focus on the thermal aspects is used to assess aspects of switching between current paths to equalize the loss distribution, while a model that incorporates a detailed battery model is used to evaluate SoC balancing aspects. The obtained simulation results are then verified with an experimental setup. To simplify the setup, only open loop control of sinusoidal voltages using an RL-load is realized for different converter configurations depending on the desired experiment. The results of the simulation and the experiments are then compared and a proposal for an optimal switching strategy as well as for the possibility of different balancing strategies is made.

3.1 Simulation Model

The simulation model in Simulink/PLECS is separated into several parts: A control system, including the PMSM field oriented control, the PWM and FSHE modulator, as well as the processing of the hi/low switching signals is implemented in Simulink. An additional PLECS subsystem contains the models of all electrical components, such as all inverter modules, battery models, a model of the PMSM and also the thermal LPNs.

A current controller was implemented in Simulink using the same PMSM model to design a closed-loop PI control, feed-forward of the back-EMF and active damping [40]. The current reference calculation from the speed and reference torque is realized via lookup tables for the pre-calculated MTPA and FW dq-currents. The reference voltages are then forwarded to the switching signal processors, where the PWM or FSHE signals, as well as the hi/lo switching signals for the switches are generated.

Implementation of PWM

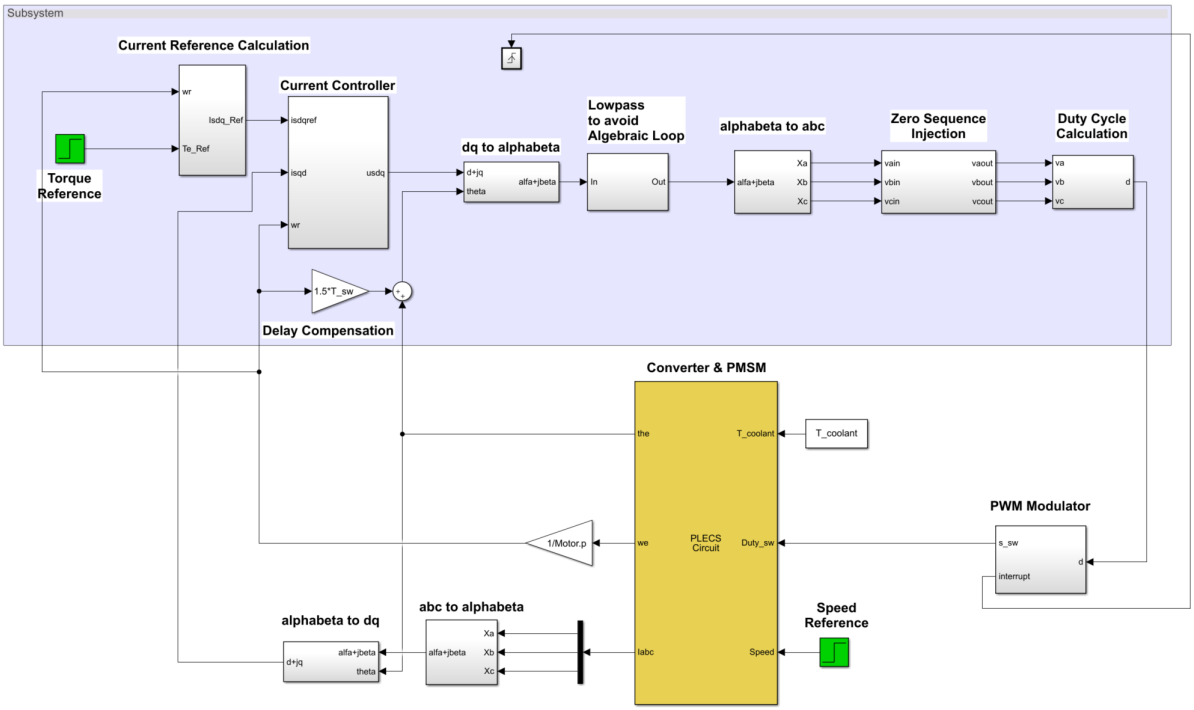


Figure 3.1.1: *Simulink/PLECS model with PWM modulator*

A block diagram of the simulation model is shown in Figure 3.1.1. To generate the hi/lo switching signals for the semiconductor switches from the reference voltage signals, several steps are performed. A zero-sequence signal is injected into all three phases, such that a modulation index of up to $M = 1.15$ becomes possible without changing the sinusoidal shape of the line-to-line output voltage. For each phase, the duty cycles for each module are obtained by comparing the reference signal to the different voltage levels of the modules. By comparing the duty cycle signals to a switching frequency triangular carrier wave, the switching signals are obtained. To avoid aliasing, the processing is triggered by interrupt pulses, synchronized with the carrier peaks. The computational time delays together with the PWM delay, create 1.5 cycles delay, which is compensated in the transformation angle of the dq to $\alpha\beta$ transformation of the current controller.

Implementation of FSHE

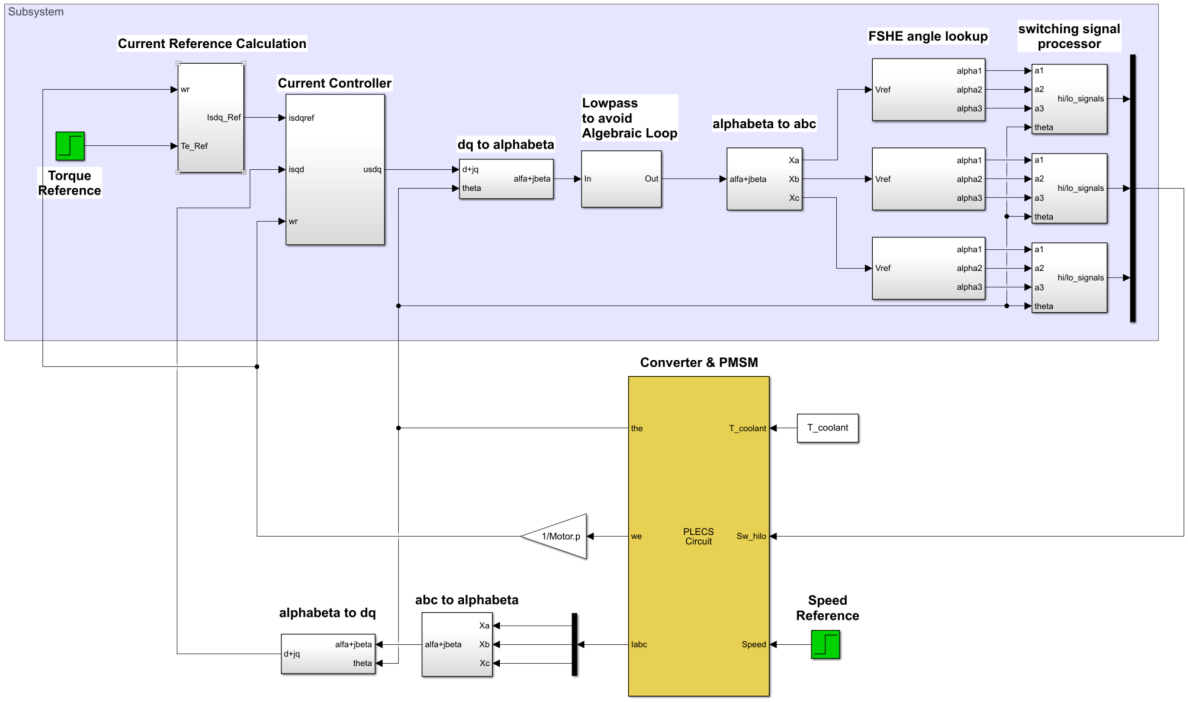


Figure 3.1.2: *Simulink/PLECS model with FSHE lookup*

A block diagram of the simulation model using FSHE switching is shown in Figure 3.1.2. For the implementation of the fundamental frequency switching with selective harmonic elimination, the switching angles are computed offline by an optimization algorithm and stored in lookup tables. To compute the switching angles, the phase voltage output waveform can be expressed by Fourier Series as

$$V_{\mathrm{ph}}(\omega t) = \frac{a_0}{2} + \sum_{h=1}^{\infty}[a_h \sin(h\omega t) + b_h \cos(h\omega t)] \quad . \tag{3.1.1}$$

Since the described staircase waveform for N series modules and $L = 2N + 1$ levels is quarter-wave symmetrical with no DC component ($a_0 = 0$), the coefficients can be found as

$$\begin{cases} a_h = \dfrac{4}{h\pi}[V_{\mathrm{dc,1}} \cos(h\alpha_1) + V_{\mathrm{dc,2}} \cos(h\alpha_2) + ... + V_{\mathrm{dc,N}} \cos(h\alpha_{\mathrm{N}})] & \text{for odd } h \\ a_h = 0 & \text{for even } h \\ b_h = 0 & \text{for all } h \end{cases} \tag{3.1.2}$$

with the modulation index

$$M = \frac{a_1}{\sum_{\mathrm{i}=1}^{N} V_{\mathrm{dc,i}}} \tag{3.1.3}$$

with a_1 as the desired output voltage. $V_{\mathrm{dc,i}}$ are the measured module voltage levels.

For N firing angles, N independent equations can be set up that can be used to eliminate $(N-1)$ harmonics for an adjustable modulation index M [41]. With the triple harmonics canceled due to the balanced three-phase system and $N = 3$, the 5^{th} and 7^{th} harmonic can be minimized by minimizing the cost function

$$f(\alpha) = 7 \cdot |a_5(\alpha)| + 5 \cdot |a_7(\alpha)| \tag{3.1.4}$$

with the equality constraint of the fundamental component being as desired with

$$a_1 = \frac{4}{\pi}[V_{\mathrm{dc},1}\cos(\alpha_1) + V_{\mathrm{dc},2}\cos(\alpha_2) + V_{\mathrm{dc},3}\cos(\alpha_3)] = M \cdot (V_{\mathrm{dc},1} + V_{\mathrm{dc},2} + V_{\mathrm{dc},3}) \quad , \tag{3.1.5}$$

and maintaining staircase shape with

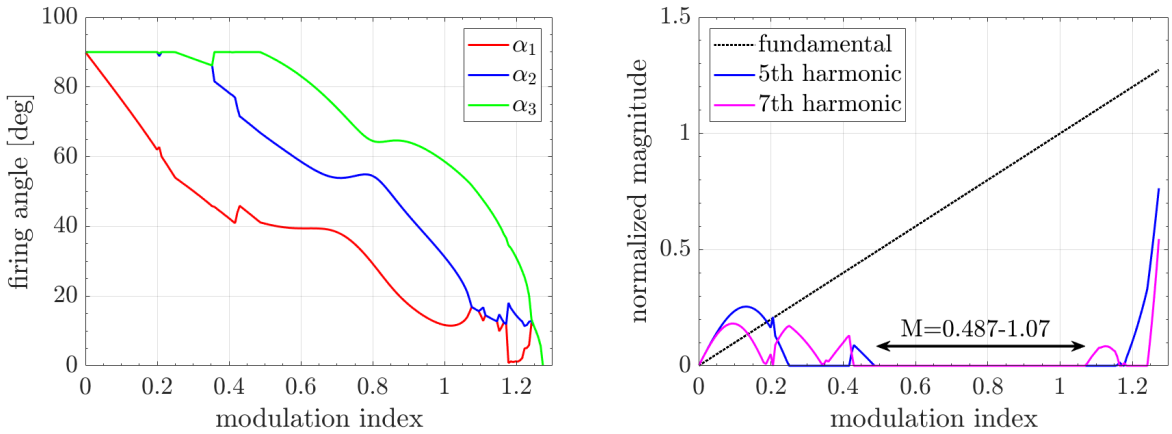
$$0 \leq \alpha_1 \leq \alpha_2 \leq \alpha_3 \leq \frac{\pi}{2} \quad . \tag{3.1.6}$$

For the case of equal DC voltages (3.1.2) simplify to

$$a_h = \frac{4V_{\mathrm{dc}}}{h\pi}[\cos(h\alpha_1) + \cos(h\alpha_2) + \cos(h\alpha_3)] \text{ for } h = 1, 5, 7, \ldots \quad , \tag{3.1.7}$$

and (3.1.5) simplifies to

$$a_1 = \frac{4V_{\mathrm{dc}}}{\pi}[\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3)] = M3V_{\mathrm{dc}} \quad . \tag{3.1.8}$$



(a) *optimal angles* (b) *harmonic content*

Figure 3.1.3: *Solution for equal DC voltages*

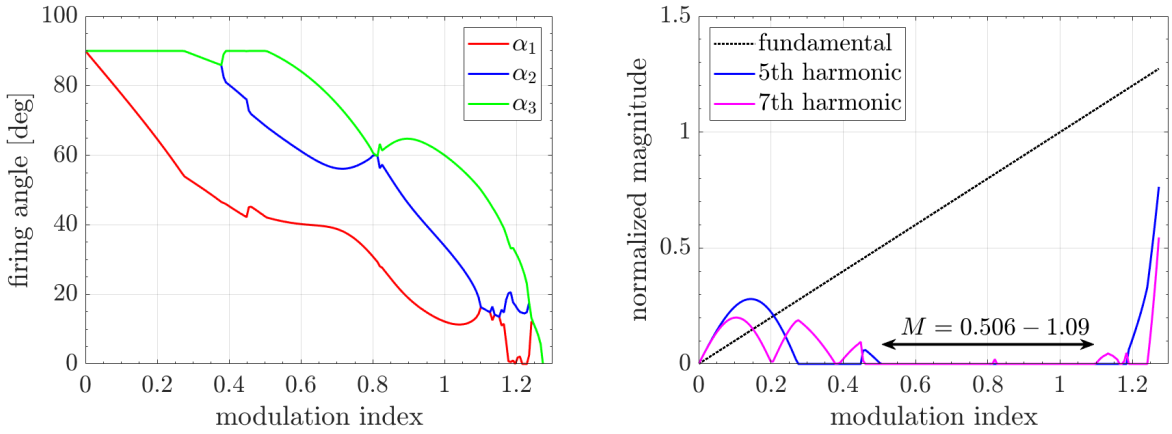
Figure 3.1.3a shows the resulting switching angles after the optimization. Figure 3.1.3b shows the resulting harmonic contents. As shown, the 5^{th} or 7^{th} harmonic can be eliminated between $M = 0.25$ and $M = 0.487$. The 5^{th} and 7^{th} harmonic can be eliminated between $M = 0.487$ and $M = 1.07$. An operation using FSHE outside of the range of $M = 0.25$ and $M = 1.07$ most likely results in high distortions.

For the case of symmetric unequal DC voltages with average voltage $V_{\mathrm{dc},2} = \bar{V}_{\mathrm{dc}}$ and $V_{\mathrm{dc},1} = 1.1\bar{V}_{\mathrm{dc}}$ and $V_{\mathrm{dc}_3} = 0.9\bar{V}_{\mathrm{dc}}$, (3.1.2) simplify to

$$a_h = \frac{4\bar{V}_{\mathrm{dc}}}{h\pi}[1.1\cos(h\alpha_1) + \cos(h\alpha_2) + 0.9\cos(h\alpha_3)] \text{ for } h = 1, 5, 7, \ldots \quad , \tag{3.1.9}$$

and (3.1.5) simplifies to

$$a_1 = \frac{4\bar{V}_{\mathrm{dc}}}{\pi}[1.1\cos(\alpha_1) + \cos(\alpha_2) + 0.9\cos(\alpha_3)] = M3\bar{V}_{\mathrm{dc}} \quad . \tag{3.1.10}$$



(a) *optimal angles* (b) *harmonic content*

Figure 3.1.4: *Solution for symmetric unequal (±10%) DC voltages*

Figure 3.1.4a shows the resulting switching angles after the optimization. Figure 3.1.4b shows the resulting harmonic contents. Since the minimization of the harmonics is independent of the average DC voltage, the switching angles can be computed offline for the equal as well as the unequal case and stored in lookup tables.

As shown by [31], voltage THD is changed less than 5%, when using the switching angles calculated for balanced DC voltages, even if the actual DC voltages vary by ±10%. Since DC voltage level variations of more than ±10% are not expected when using balancing during normal operation, the use of switching angles derived for the balanced case is sufficient.

State of Charge Balancing Control

Even though all simulations but the ones comparing FSHE to PWM switching incorporate a dynamic model of a battery pack instead of an ideal voltage source, a constant open-circuit voltage (OCV), independent of the SoC, was assumed for all simulations. All simulations on thermal or SoC balancing thus focused on equalizing currents through all switches or creating an active power flow between modules independent of the OCV.

To ensure an equal use of all modules in one phase and thus balancing the SoC between the modules of one phase during normal operation, a separate control module sorts the modules by their terminal voltage and assigns the different duty cycles such that, during motor operation, the module with the highest voltage and thus highest OCV gets assigned to the longest duty cycle and vice versa. In the case of FSHE, the smallest firing angle is assigned to the module with the highest voltage. Since constant OCVs are assumed for all simulations, this is only implemented in the laboratory setup.

To allow for balancing between different phases during normal operation, the active power provided by each phase must be altered to allow for a balancing flow of active power between phases, as introduced by [42] for the balancing of DC-link capacitors in multilevel inverters for STATCOM applications. The reference voltage is increased, if the phase current is positive and decreased, if the phase current is negative, which increases the reference voltage magnitude whenever current and voltage are in phase and, thus, increases active power from the batteries. The resulting principal waveforms are shown in Figure 3.1.5. As shown, the changed reference

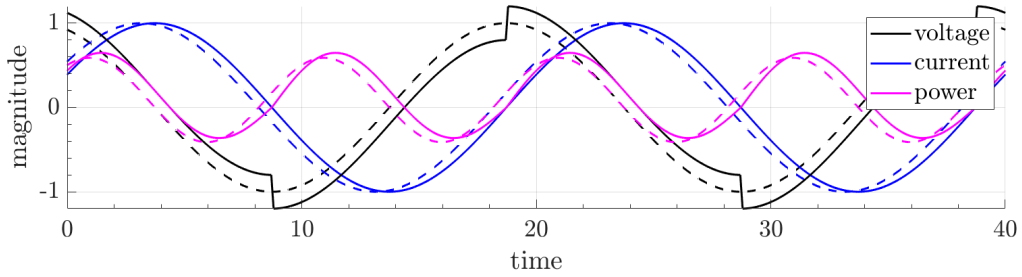


Figure 3.1.5: *Ideal waveforms with AC balancing (solid) and without (dashed)*

voltage also implies a phase shift, which will introduce torque ripples. For this reason, balancing between phases during regular operation should be avoided or performed only slightly.

When the vehicle is not under operation or at standstill, different balancing techniques can be applied, using the modules as DC/DC-converter-half-bridges with the motor inductance, as shown in Figure 3.1.6. This can both be applied between two modules in the same phase, as well as between three modules in three different phases. For the simulation of the DC-balancing, a manual input of duty-cycles is implemented.

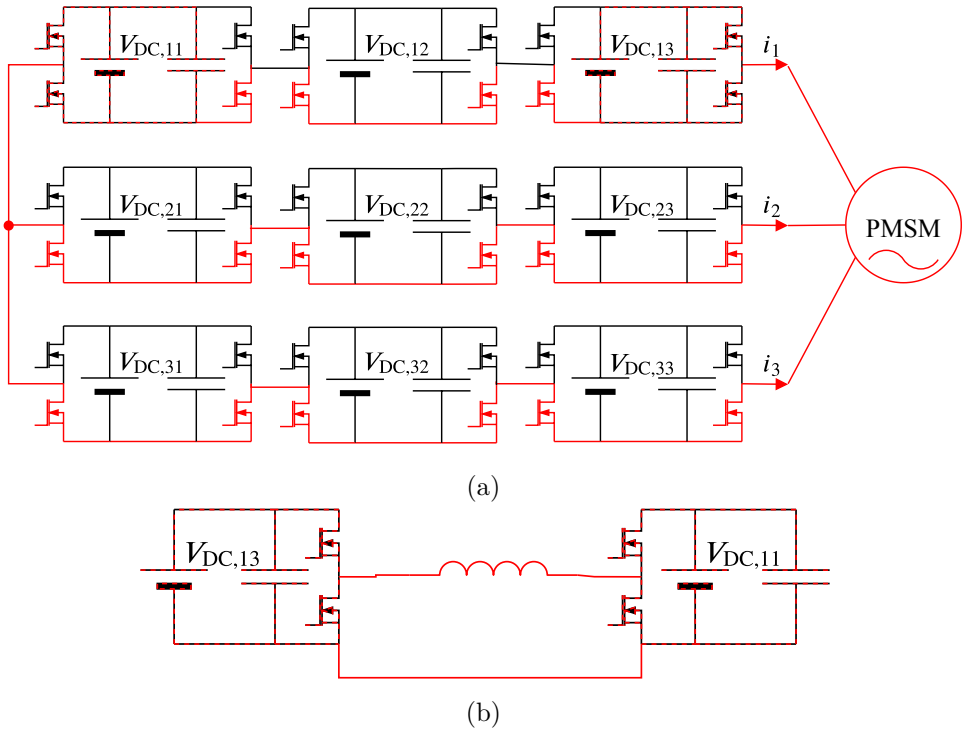


Figure 3.1.6: *DC balancing between two modules (a) and the same configuration simplified (b): current carrying paths marked in red, switched components dashed*

Thermal Balancing Control

Especially for the low-speed region, there is the necessity to regularly switch current paths to avoid overheating of switches, mainly due to conduction losses. For this purpose, a separate module is implemented, regularly switching, with a frequency of 100 Hz, between the upper and lower current path of each H-bridge (compare Figure 2.1.2), as well as, for lower voltage operation, switching between the modules of one phase. This is necessary to avoid overheating of the lower current path's MOSFETs and single modules. Of course, this is not compatible with the controlled SoC balancing between modules, while still ensuring an equal discharging of all modules.

3.1.1 Inverter, Battery and Machine Model

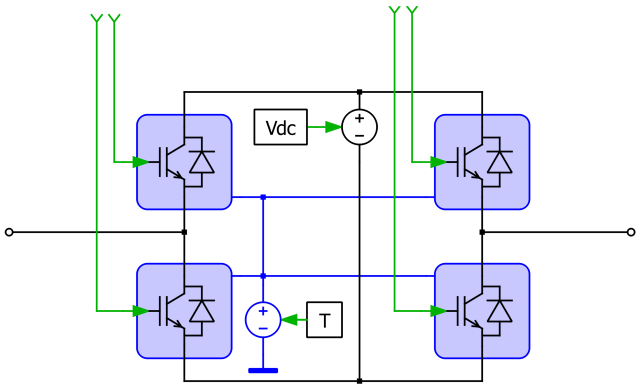


Figure 3.1.7: *Simple PLECS circuit model of one inverter module with signals in green and thermal network in blue*

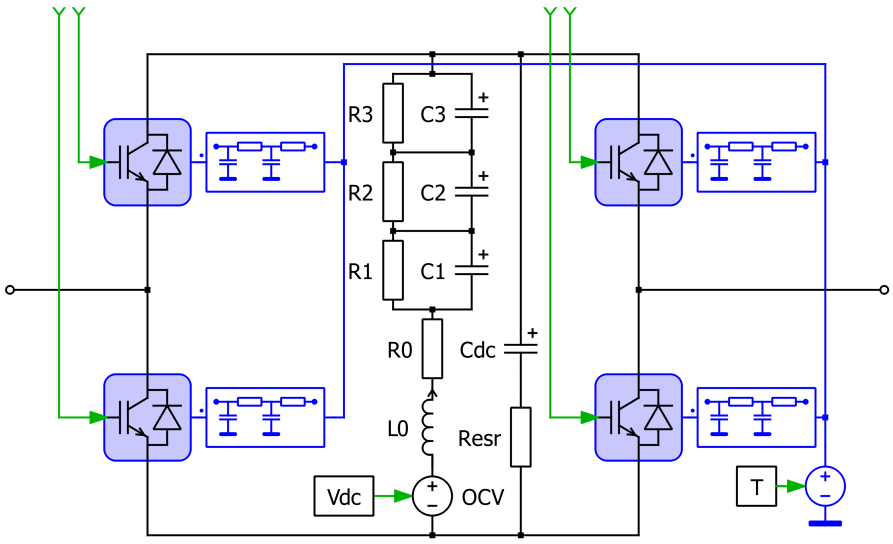


Figure 3.1.8: *Extended PLECS circuit model of one inverter module with signals in green and thermal network in blue*

The inverter, as shown in Figure 2.1.1, is implemented in a PLECS subsystem. While the switches act as ideal switches, switching and conduction loss data is stored in lookup tables as done in [8]. For the simulations, data of an Infinion OptiMOS™-5 Power-Transistor

IAUT300N10S5N015 with $V_{DS} = 100\,V$, $R_{ds,on} = 1.5\,m\Omega$, $I_D = 300\,A$, $T_{max} = 175\,°C$ and $R_{th,JC} = 0.4\,K\,W^{-1}$ was used.

The temperature of the MOSFETs was either defined as constant, as shown in Figure 3.1.7, with $T_{initial} = T_{coolant} = 70\,°C$. Or, a thermal lumped parameter network was implemented, modeling the heat flow from junction to coolant, to asses the efficiency of the proposed thermal balancing methods, as shown in Figure 3.1.8. Here, the parameter of the thermal LPN were assumed to be as listed in Table 3.1.1. Since only the thermal resistance $R_{th,junction-case}$ of the MOSFET is known from datasheets, while the other parameters are a matter of a not yet designed cooling system, the unknown thermal resistance parameters were chosen to result in reasonable steady-state temperatures for regular operation. The thermal capacitance values were chosen such that a near steady-state is reached in a manageable simulation time.

The DC-link was either modeled as an ideal voltage source, or by a battery equivalent circuit model in parallel to the DC-link capacitor. The ECM's parameters are set for a 15s100p configuration of LG Chem ICR18650 C2 2800 mAh li-ion cells as measured in [8] and listed in Table 3.1.2. The DC-link capacitor is parameterized with $C_{DC} = 50\,mF$ and $R_{ESR} = 2.4\,m\Omega$. The PMSM was modeled as presented in section 2.5, with the generated 3-phase voltage and rotational speed as input and torque and 3-phase currents as output. The machine parameters are defined as listed in Table 3.1.3, representing a 84 kW machine, as done in [3].

Table 3.1.1: Thermal LPN parameters

parameter	value
$R_{th,junction-case}$	$0.4\,K\,W^{-1}$
$R_{th,case-heatsink}$	$0.4\,K\,W^{-1}$
$R_{th,heatsink-coolant}$	$0.6\,K\,W^{-1}$
$C_{th,junction}$	$0.005\,J\,K^{-1}$
$C_{th,case}$	$0.5\,J\,K^{-1}$
$C_{th,heatsink}$	$2\,J\,K^{-1}$
$T_{initial}$	$70\,°C$
$T_{coolant}$	$30\,°C$

Table 3.1.2: LG Chem ICR18650 cell parameters

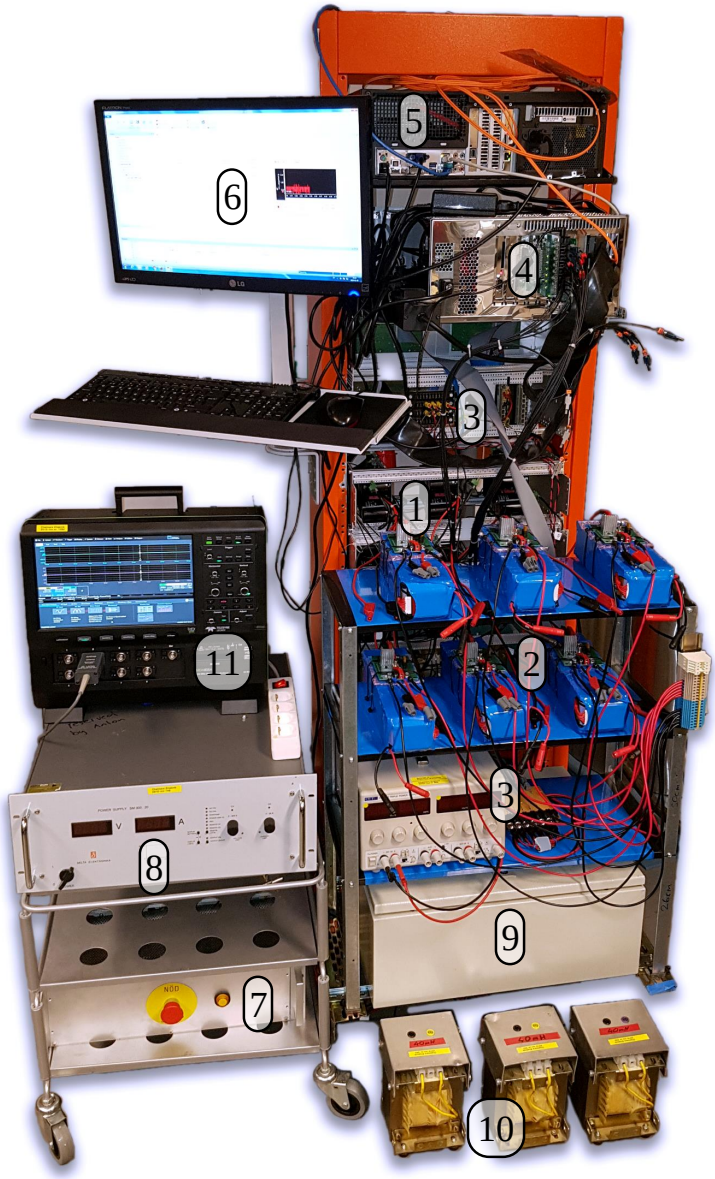
parameter	value
R_0	$41.53\,m\Omega$
L_0	590.8 nH
R_1	$5.02\,m\Omega$
C_1	75.44 mF
R_2	$7.32\,m\Omega$
C_2	339.5 mF
R_3	$3.23\,m\Omega$
C_3	3.625 F
scaling factor for 15s100p	0.15

Table 3.1.3: PMSM model parameters

parameter	value
stator resistance R_s	$20\,m\Omega$
d-axis inductance L_{sd}	250 µH
q-axis inductance L_{sq}	750 µH
magnetic flux Ψ_m	75 mWb
number of pole pairs n_p	4
max. phase voltage U_{max}	200 V
max. rated current I_{rated}^{RMS}	190 A
max. speed $\Omega_{r,max}$	12 000 rpm
nominal torque T_n	170 Nm

3.2 Laboratory Setup for Validation

The verification of the simulations was done using an experimental laboratory setup. To reduce the complexity, the experimental setup facilitated inverter topologies, like a 5-level-3-phase and a 7-level-two-phase inverter with separate DC-sources. The CHB inverter was composed using six full-bridge converters, each supplied by an own DC-link capacitor connected to custom made Li-ion battery packs via a soft-start circuit. The machine control strategy was not verified with an electric machine. The electric machine was substituted with an RL-load consisting of three 40 mH inductors with a resistance of 1.8 Ω each. The converters were controlled via fiber-optical connections and a dSPACE-system. The full setup is shown in Figure 3.2.1.



(1) H-bridge modules
(2) Battery modules
(3) Auxiliary power supply
(4) dSPACE HIL-system
(5) Computer
(6) Control desk
(7) Emergency stop
(8) Battery charger
(9) Current measurements
(10) RL-load
(11) Oscilloscope

Figure 3.2.1: *Lab-Setup*

The used inverter modules were developed by Aalborg University. Each module contains an IGBT H-bridge, as well as the complete control and power supply circuitry. The modules receive a hi/lo-signal for each half-bridge via optical receivers. The control logic includes blanking time, overcurrent protection, as well as other protection mechanisms. The voltage measurement of the DC-link is available as a PWM signal at an optical transmitter. The H-Bridge module is shown in Figure 3.2.2.

The DC-link capacitor bank with four 1 mF capacitors is directly bolted to the H-Bridge board and connected in parallel to a battery pack. The custom made 13s4p battery packs, assembled from Samsung ICR 18650 22P - 2200 mAh cells, contain a battery management system (BMS) with passive balancing, over and under-voltage protection as well as overcurrent protection. To avoid high inrush currents when connecting the battery packs to the capacitor banks, a soft start circuit using a MOSFET to short-circuit a current limiting resistor as well as a thermal overcurrent fuse was designed, manufactured and used for each battery pack. The battery pack, including the BMS and the inrush current limiter, is shown in Figure 3.2.3. The battery packs with a nominal capacity of 8800 mAh and a nominal voltage of 48 V can be charged in parallel via diodes with CC-CV-charging using a laboratory power supply.

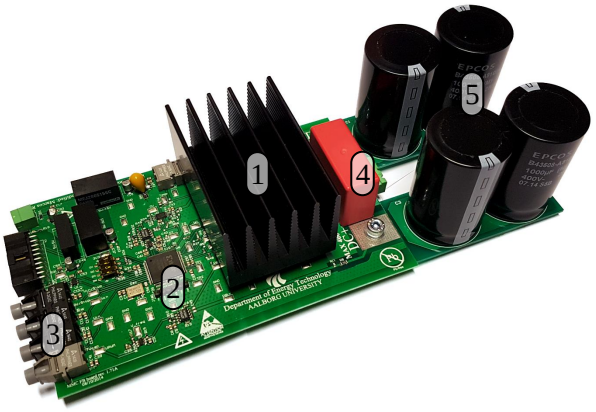


Figure 3.2.2: *H-Bridge module with (1) IGBTs with heat sink, (2) integrated FPGA, (3) optical transceivers, (4) output with filter, (5) DC-link capacitors*

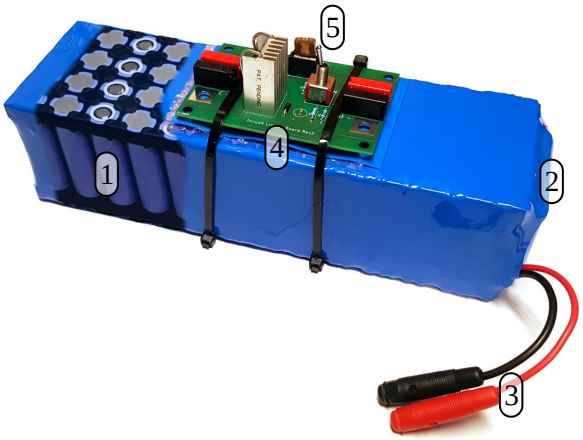


Figure 3.2.3: *Battery module with (1) 13s4p cell pack, (2) BMS, (3) connectors, (4) DC-link inrush current limiter, (5) overcurrent thermal fuse*

The H-bridge modules are controlled via a HIL-dSPACE system with a DS1006 processor board and a DS5101 digital waveform output board connected to optical transmitters. The processor board is programmed from Simulink via a Real-Time Interface (RTI) using the adapted simulation models and controlled with Control-Desk software. DS2004 high-speed A/D boards were used for data capturing from the voltage sensors on the inverter boards, as well as from current transducers, used to measure the phase currents. Additionally, a Teledyne Lecroy MDA810A 8-channel oscilloscope with differential voltage and current probes was used to capture the different voltage and current waveforms, as well as switching patterns.

Due to limited number of H-Bridge modules, as well as PWM outputs, only six modules could be used in either a 2-Phase-7-Level, as shown in Figure 3.2.4, or a 3-phase-5-level arrangement, as shown in Figure 3.2.5.

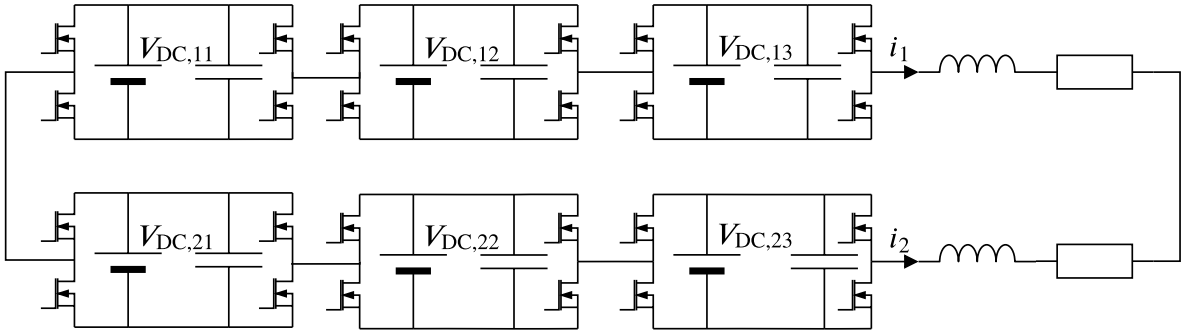


Figure 3.2.4: *2-Phase-7-Level cascaded H-bridge inverter*

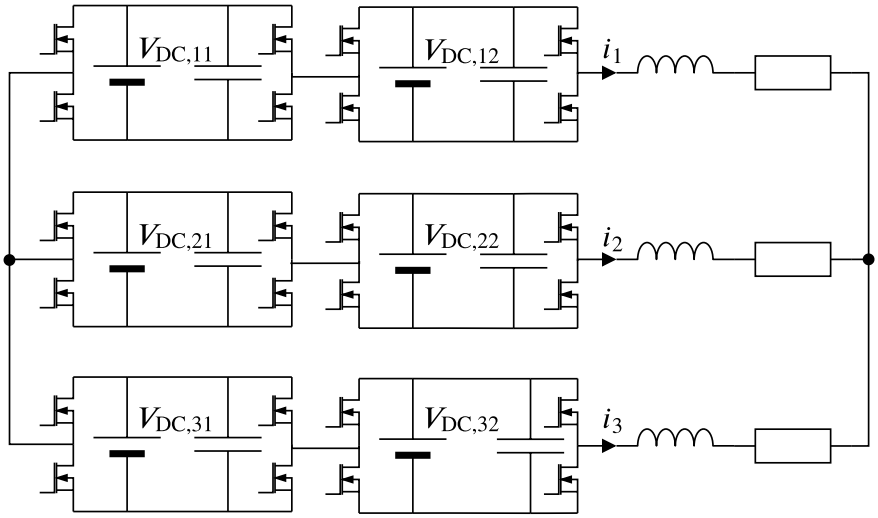


Figure 3.2.5: *3-Phase-5-Level cascaded H-bridge inverter*

4 Simulations and Measurements

The analysis of the multilevel inverter is divided into several parts. First, different switching strategies, such as PWM and FSHE, are compared using simulations. Next, the results are experimentally verified for selected operation points. Then, a simulation of a thermal balancing algorithm is performed as a proof of concept, but not verified using the laboratory setup. Finally, different battery balancing strategies are simulated and tested with the laboratory setup as a proof of concept.

4.1 Comparison of Switching Techniques

This section deals with the simulation and experimental results comparing PWM and FSHE switching for a 7-level cascaded H-bridge inverter. The simulations were performed with the previously introduced simulation model, using fixed temperatures and ideal voltage sources. Simulations were performed for various torque and speed operating points to provide mappings over the whole operation range. Figures 4.1.1 and 4.1.2 show the voltage and current

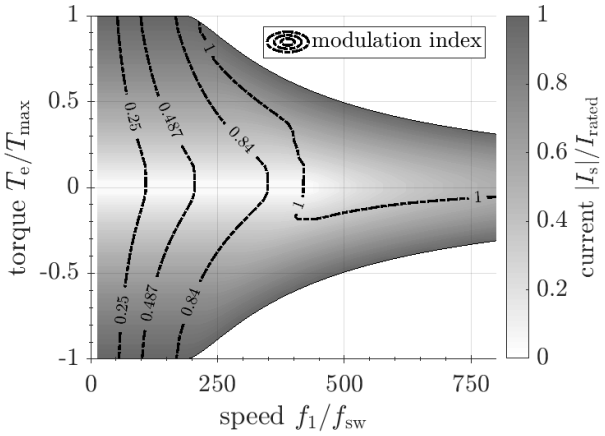


Figure 4.1.1: *Modulation index and current magnitude over the operation range of the chosen electric machine*

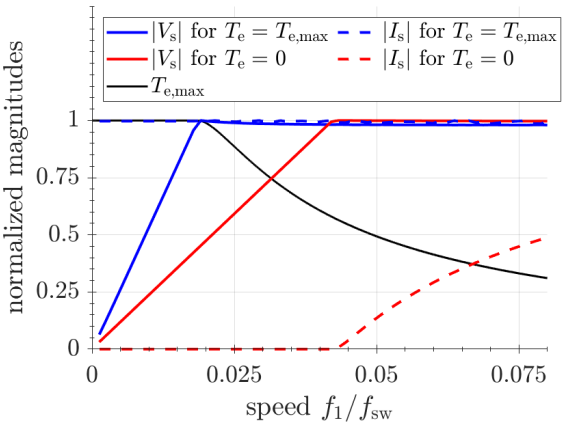


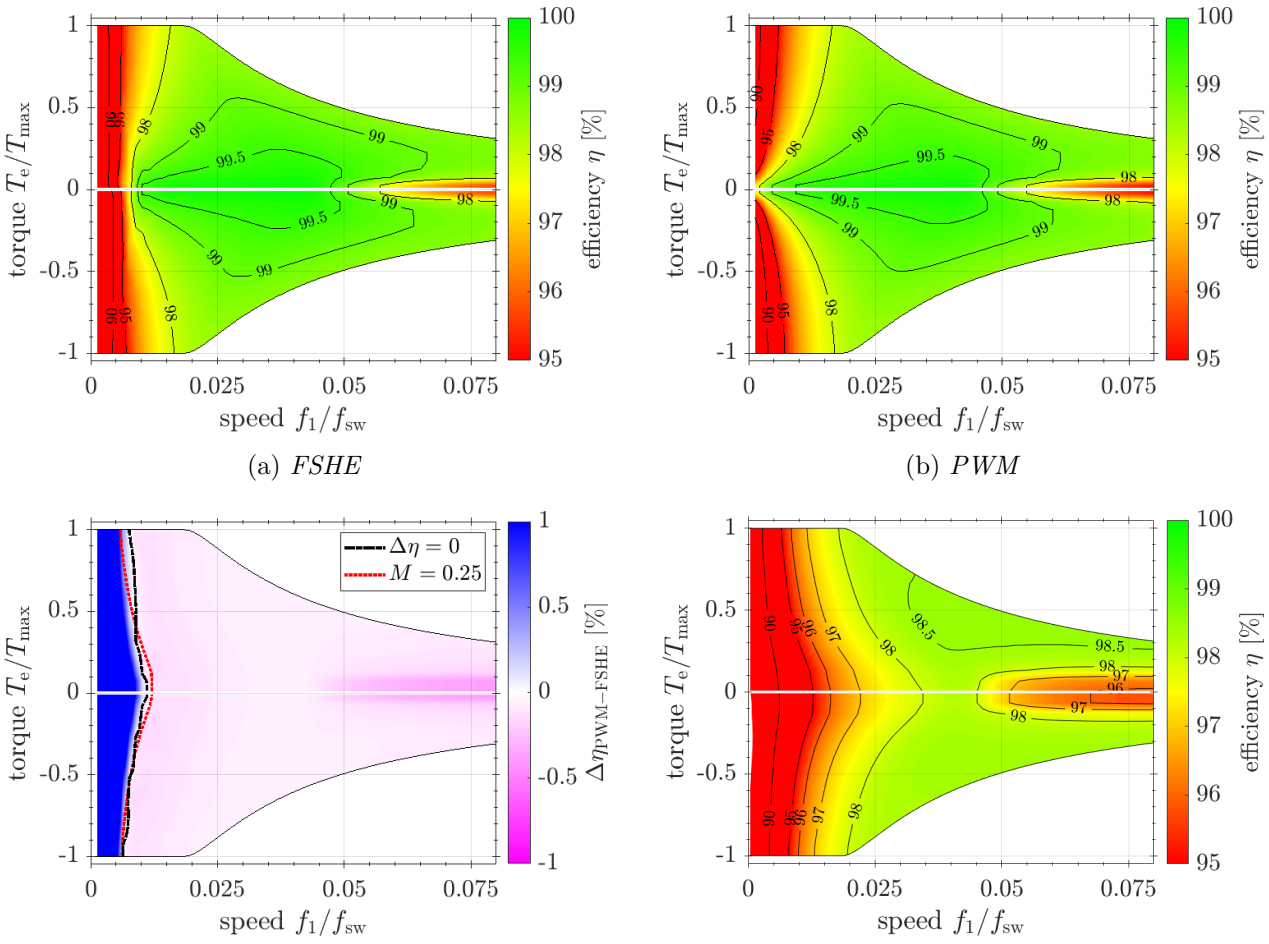
Figure 4.1.2: *Voltage and current magnitudes for zero and maximum torque vs. machine speed*

magnitude distribution over the operation range of the chosen electric machine. Here it can be already observed what has been derived in section 2.5: The current magnitude increases with the torque magnitude, as well as for field weakening in high-speed regions and for zero torque, when the voltage limit is reached. Furthermore, it is visible that the voltage magnitude predominantly rises with increasing machine speed to compensate for the increasing back-EMF. Once the voltage maximum is reached, the modulation index is kept at 1, and maximum torque can no longer be provided since an increasing negative d-axis-current has to be injected to weaken the rotor field and control the back-EMF.

Figures 4.1.3a and 4.1.3b show the different inverter efficiencies extracted from the simulation results for FSHE and PWM. From the derivation of the FSHE switching angles, it was expected to achieve good results in the range of $M = 0.25$ to $M = 0.487$, where the 5^{th} or 7^{th} harmonic can be eliminated, and between $M = 0.487$ and $M = 1.07$, where the 5^{th} and 7^{th} harmonic can be eliminated. Figures 4.1.4a and 4.1.5a clearly show high WTHD_V and THD_I for the region of low modulation index smaller than $M = 0.25$. A high THD_I means a low ratio of

the torque producing fundamental component versus the higher harmonic components. This leads to low inverter efficiency for regions of low modulation index (compare Figure 4.1.3a) as the low-speed region, as expected. Since $\mathrm{WTHD_V}$ and $\mathrm{THD_I}$ do not significantly change over the operation range for PWM switching, and $\mathrm{THD_I}$ is very low in the low-speed region (compare Figure 4.1.5b), the inverter efficiency is significantly better using PWM switching for the low-speed region as shown in Figure 4.1.3c.

Only comparing the resulting inverter efficiency for the different switching techniques, as shown in Figure 4.1.3c, it can be observed, that, apart from the low-speed region, the general efficiency level is slightly higher for FSHE switching. Assumable, this is due to less frequent switching and thus lower switching losses. It is thus preferable to apply FSHE switching above modulation indices of $M = 0.25$, if only the inverter efficiency is a concern.



(a) *FSHE* (b) *PWM*

(c) *Difference: PWM-FSHE* (d) *2-level IGBT inverter analyzed in [3]*

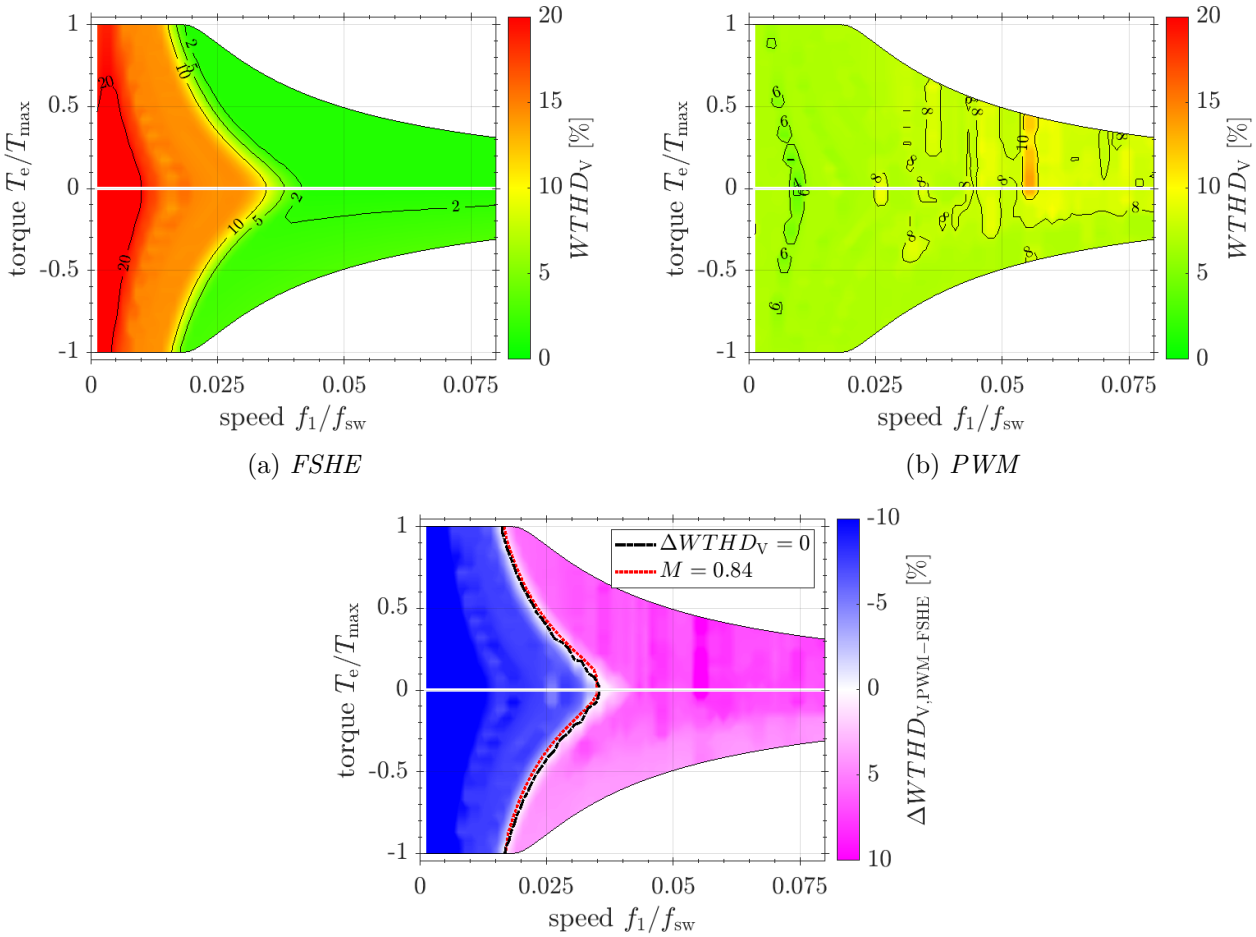
Figure 4.1.3: *Inverter efficiency*

[3] compares a standard two-level inverter with a three-level and a five-level active neutral point clamped inverter for the very same vehicle traction application as assumed in this work. It shows a high potential increase in efficiency for the multilevel inverter compared to the two-level inverter. Comparing the simulated efficiencies of the two-level-inverter from [3], shown in Figure 4.1.3d, to the efficiencies simulated in this work, shown in Figure 4.1.3b, a significant improvement in inverter efficiency is observable. Over the whole operation region, efficiency is improved by 0.5 to 1 % and by more than 2 % for the low torque regions.

Analyzing the results evaluated with respect to voltage $\mathrm{WTHD_V}$, as shown in Figure 4.1.4, a slightly different picture is shown. From Figure 4.1.4b it can be observed that voltage $\mathrm{WTHD_V}$ for PWM switching is at a level between 5 and 10 % over nearly the whole operation region. For PWM, $\mathrm{WTHD_V}$ increases towards higher speed regions as the ratio of fundamental to switching frequency decreases, which leads to a higher weighting of the harmonic components caused by the PWM switching.

Considering voltage $\mathrm{WTHD_V}$ for FSHE switching, as shown in Figure 4.1.4a, one can observe, as discussed earlier, that $\mathrm{WTHD_V}$ is very high for low speed or low modulation index below 0.25. Above a modulation index of about $M = 0.84$, $\mathrm{WTHD_V}$ significantly drops to lower levels than for PWM switching, since only high modulation index sinusoidal waveforms can be properly approximated by the staircase waveforms. Even though not separately shown, it is likely that the $\mathrm{WTHD_V}$ correlates with the modulation index instead of the fundamental frequency, for FSHE switching.

If only the quality of the output voltage is a concern, a strategy as indicated by Figure 4.1.4c, utilizing PWM switching for modulation indices below $M = 0.84$ and FSHE switching above, should be applied.

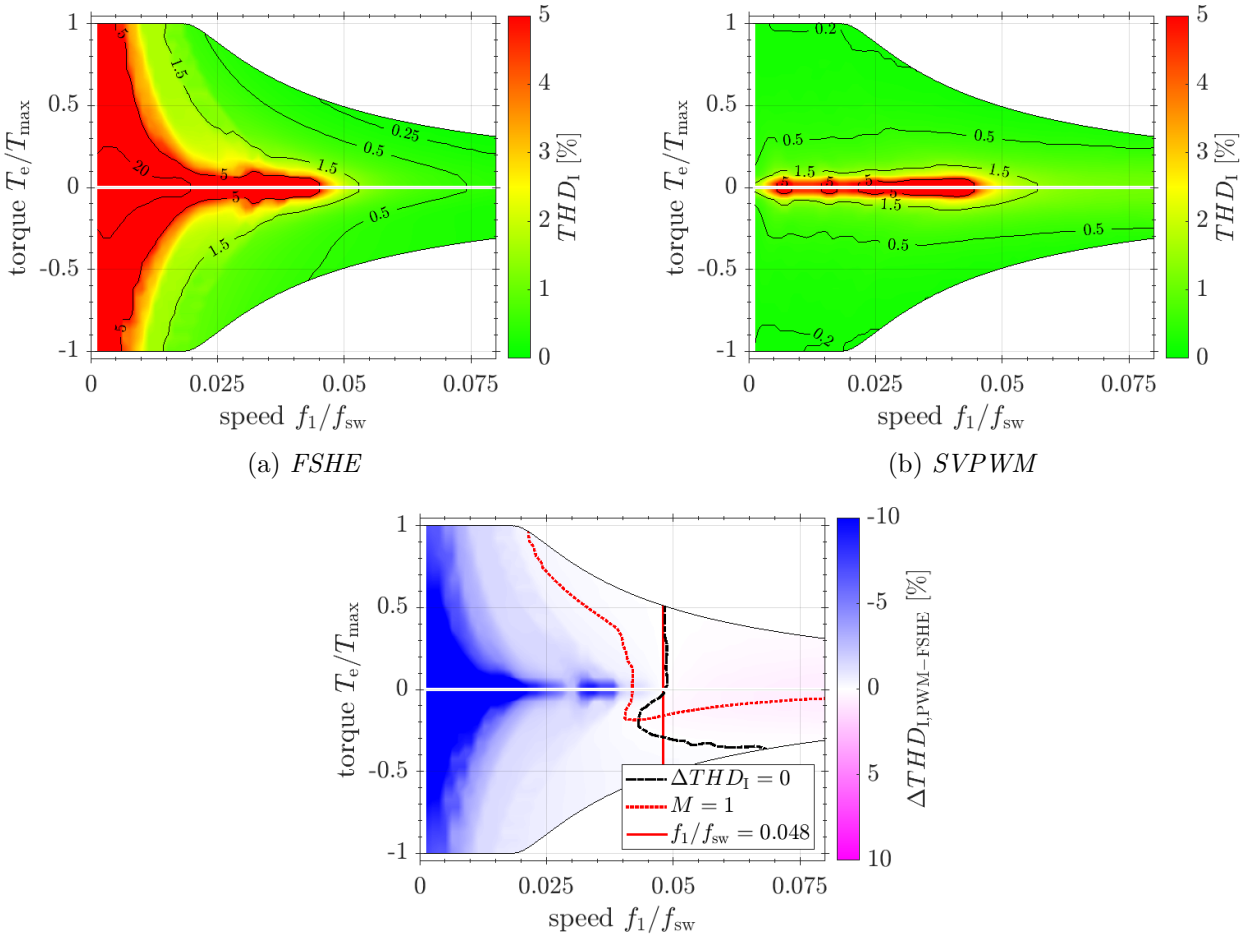


(a) *FSHE* (b) *PWM*

(c) *Difference*

Figure 4.1.4: *Voltage* $WTHD_V$

Considering current $\mathrm{THD_I}$ in the simulation results, by principle, a very similar picture as for the $\mathrm{WTHD_V}$ is shown. $\mathrm{THD_I}$ is high for FSHE switching in low modulation index regions, as shown in Figure 4.1.5a. This was to be expected, as $\mathrm{WTHD_V}$ is high for these regions. On the other hand, $\mathrm{THD_I}$ for PWM switching is the lowest in the low-speed region, as shown in Figure 4.1.5b, as the switching frequency is high compared to the fundamental frequency. Consequently, considering the current quality (compare Figure 4.1.5c), a similar strategy to the one proposed considering voltage quality should be applied.



(a) *FSHE* (b) *SVPWM*

(c) *Difference*

Figure 4.1.5: *Current THD_I*

Considering all aspects, the machine's operation region can be divided into three regions. Below modulation indices of $M = 0.25$, PWM switching is superior in all aspects. In the region above, up to modulation indices of $M = 0.84$ PWM switching is still superior considering voltage and current quality, as well as torque ripple, but due to less frequent switching, FSHE switching shows to be superior in terms of inverter efficiency. In higher speed regions and modulation indices above $M = 0.84$, FSHE switching shows to be superior, both in terms of inverter efficiency, as well as in terms of voltage quality and, above speeds of $f_1/f_{sw} = 0.048$, also in terms of current quality.

In a subsequent step, the simulation results were verified using the laboratory setup. For this purpose four operation points were chosen to represent four different regions of the operation region: 100 Hz and $M = 0.2$ representing the low-speed region where FSHE switching is not applicable, 200 Hz and $M = 0.6$ representing the medium-speed region, where FSHE appears to be more efficient, but PWM should result in lower distortions, 350 Hz and $M = 0.95$ representing a small region where $\mathrm{WTHD_V}$ should be less for FSHE, but $\mathrm{THD_I}$ less for PWM switching. 700 Hz and $M = 1$ represents the high-speed region, where FSHE switching appears to be superior in all aspects. Since the efficiency is not evaluated in the laboratory setup, only verification of the $\mathrm{THD_I}$ and $\mathrm{WTHD_V}$ results may be done. Line voltage and phase current is measured in a 2-phase-7-level setup, as illustrated in Figure 3.2.4 connected to an RL-load. Zero-padded discrete Fourier transforms (DFT) are computed to asses voltage $\mathrm{WTHD_V}$ and current $\mathrm{THD_I}$ of the measured signals.

Figure 4.1.6 shows the measurement data for the low-speed operation region. It is clearly visible that, compared to the PWM waveforms, the FSHE waveforms are far from a sinusoidal shape, which results in the indicated difference in $\mathrm{WTHD_V}$ and $\mathrm{THD_I}$ between PWM and FSHE of about factor 2 and underlines the findings from the simulations. It also can be observed that due to the low voltage magnitudes, only 3-level switching takes place. The change of current direction is visible, causing a voltage drop, as it is not compensated for in the control. In the Fourier spectrum, it can be observed, that while the FSHE waveforms contain significant low order harmonic components, the waveforms generated with PWM switching, mainly contain high order harmonics with a significant component at about switching frequency of 10 kHz. For FSHE, the 5^{th} and 7^{th} order harmonics are not canceled. This was to be expected from Figure 3.1.3a.

Figure 4.1.7 with 200 Hz and $M = 0.6$ shows a more sinusoidal output voltage waveform, especially for FSHE switching. As well, already 7 level switching takes place, and the 5^{th} and 7^{th} order harmonics are significantly reduced for FSHE switching. $\mathrm{WTHD_V}$ is at a similar level for both switching techniques, while lower than expected. The $\mathrm{THD_I}$ is close to the expected level for FSHE while being significantly higher than expected for PWM switching.

Figure 4.1.8 with 350 Hz and $M = 0.95$ shows a further decrease in $\mathrm{WTHD_V}$ and $\mathrm{THD_I}$ levels for the increased speed. Both $\mathrm{WTHD_V}$ and $\mathrm{THD_I}$ are slightly lower for PWM switching compared to FHSE switching, with the general levels as expected for $\mathrm{THD_I}$ but significantly lower than expected for $\mathrm{WTHD_V}$. As well, it can be observed that the line voltage now shows 11 switching levels as expected.

Figure 4.1.9 shows the results for the high speed region with 700 Hz and $M = 1$. With $\mathrm{THD_I}$ levels slightly higher than expected and $\mathrm{WTHD_V}$ levels lower than expected. Here, FSHE switching performs better both in terms of $\mathrm{THD_I}$ and $\mathrm{WTHD_V}$.

The general discrepancies between simulation and measurements can possibly be explained with measurement errors as well as an incomplete simulation of the switching, simulating the transistors as ideal switches not accounting for the voltage drop across the IGBTs and diodes.

The measurements support the main findings from the simulations. FSHE shows to not be applicable for low modulation indices and being superior in terms of $\mathrm{THD_I}$ and $\mathrm{WTHD_V}$ for high speed and modulation index regions. For the intermediate region, differences in voltage and current quality are shown to be small as expected, and it thus appears to be a valid strategy to apply FSHE switching for modulation indices where all available switching levels are utilized.

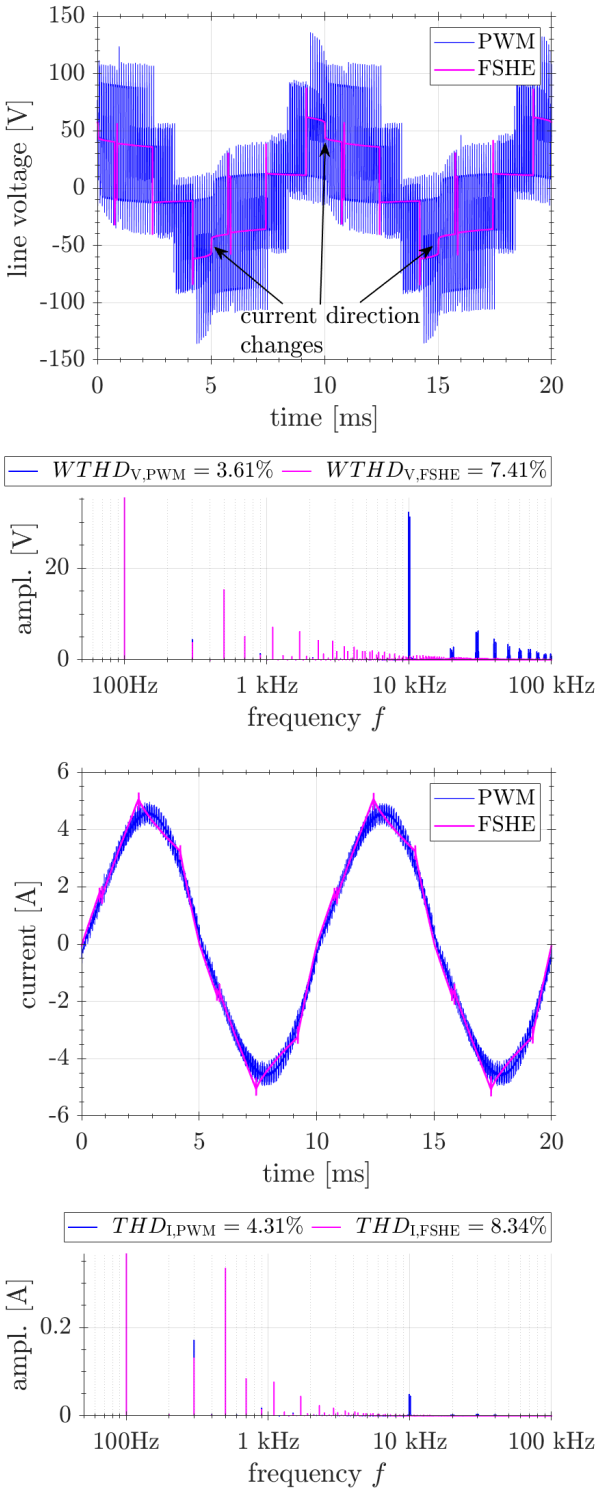


Figure 4.1.6: *Line voltage and current measurements and their zero padded DFTs for PWM and FSHE at* 100 Hz *and* $M = 0.2$

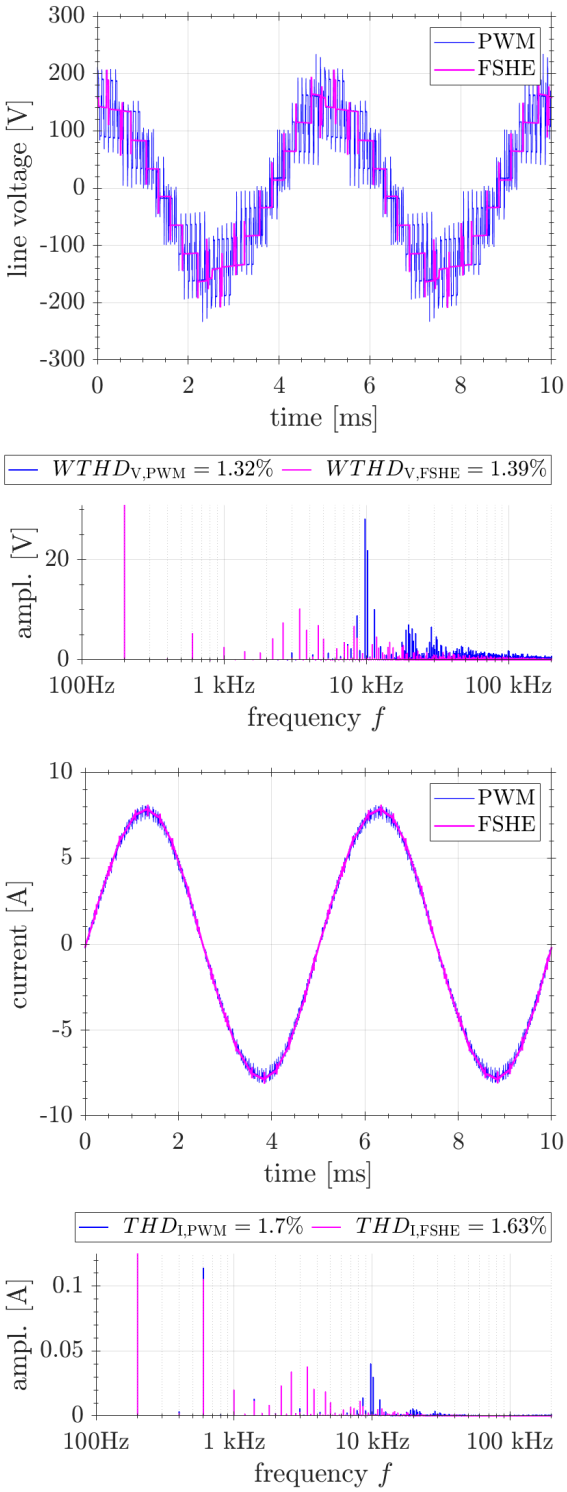
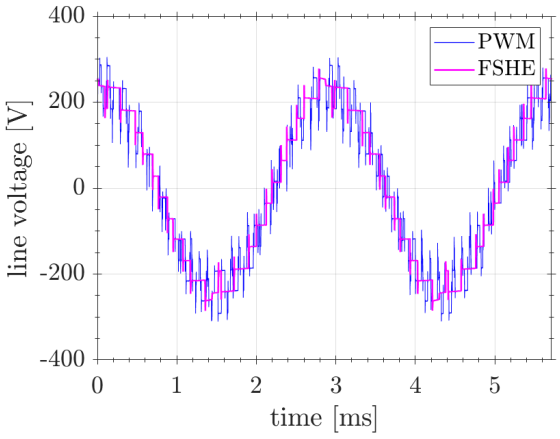
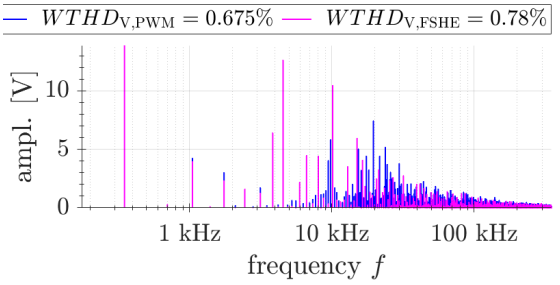
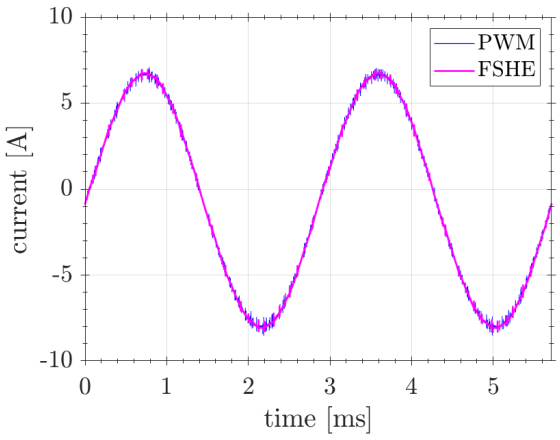


Figure 4.1.7: *Line voltage and current measurements and their zero padded DFTs for PWM and FSHE at* 200 Hz *and* $M = 0.6$







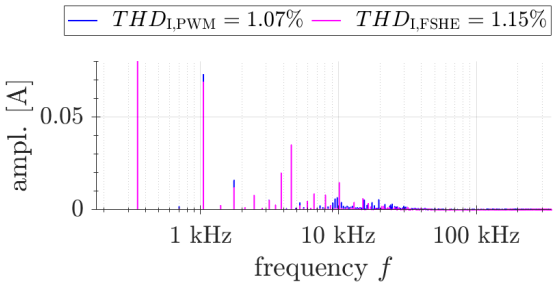
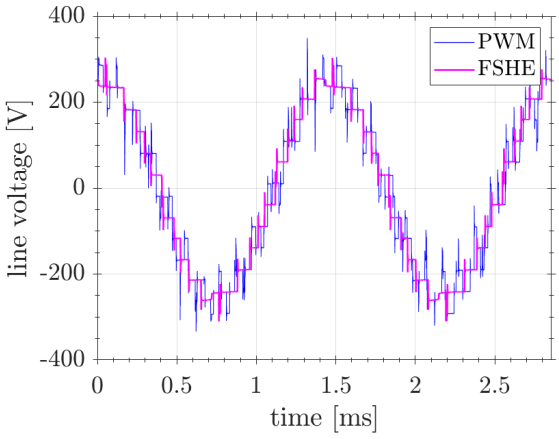
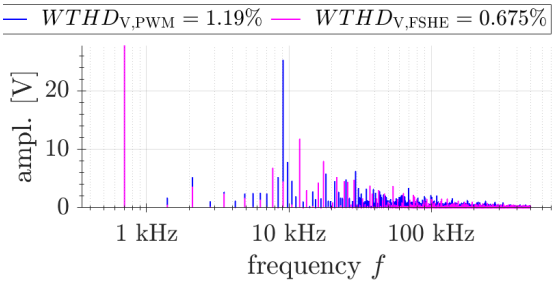
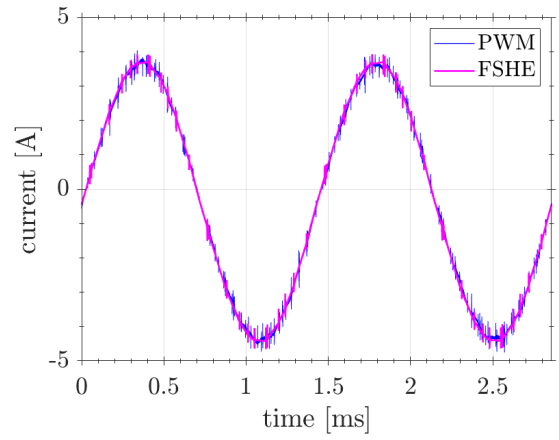


Figure 4.1.8: *Line voltage and current measurements and their zero padded DFTs for PWM and FSHE at* 350 Hz *and* $M = 0.95$







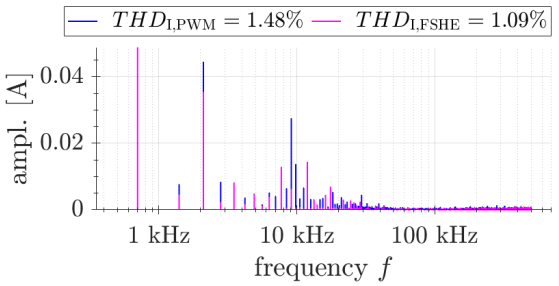
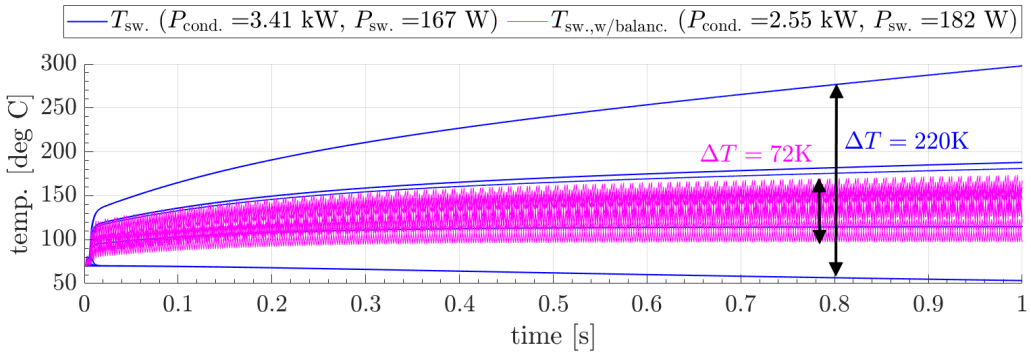


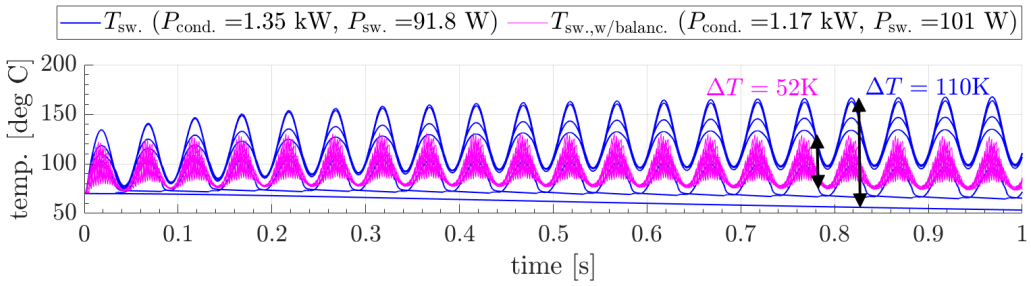
Figure 4.1.9: *Line voltage and current measurements and their zero padded DFTs for PWM and FSHE at* 700 Hz *and* $M = 1$

4.2 Thermal Balancing

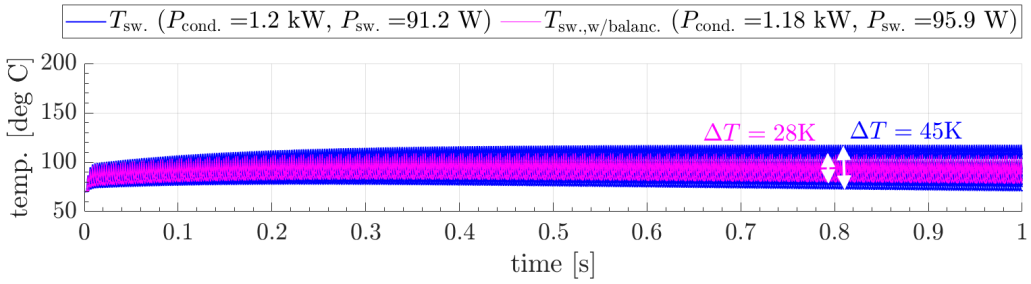
The described thermal balancing controller, regularly switching between current paths and between modules in one phase, is simulated for maximum torque at different speeds. Especially challenging are situations of very low or zero rotational speed, where the phases are unequally stressed. Also, these situations are rather constant over time. The extreme situation with zero speed but maximum torque is simulated in case (a) and shown in Figure 4.2.1a. The rotor position is chosen such that the shown phase is the highest stressed phase.



(a) 0 Hz,200 Nm



(b) 10 Hz, 200 Nm



(c) 200 Hz,200 Nm

Figure 4.2.1: *Transistor junction temperatures for all transistors of one phase during different driving situations with and without thermal balancing*

Without thermal balancing, single switches reach too high temperatures, resulting in high conduction losses and possible damage, while other switches do not carry any current and, thus, cool down. Incorporating thermal balancing, all switches are stressed more equally, and the temperatures of all switches oscillate in a reasonable range. The temperature delta between the hottest and coldest switch can be reduced by about 67 % at the selected time instance indicated in Figure 4.2.1. Even though the switching losses consequently increase, the total conduction losses are significantly lower due to the lower temperature levels, as $R_{\text{DS,on}}$ is lower.

Figure 4.2.1b shows the simulation results for slow rotation at maximum torque. In this situation, the phases are stressed equally on average. However, without thermal balancing, significant low frequency oscillations in temperature occur, and individual switches/current paths are not utilized. Facilitating the proposed thermal balancing controller, temperature oscillations can be reduced, and all switches stressed more equally. The temperature delta between the hottest and coldest switch can be reduced by over 50 %. This, again, leads to a slight increase in switching losses but, again, to a significant reduction of conduction losses due to the generally lower temperature levels.

Even in a situation occurring for longer time periods during regular operation as shown in Figure 4.2.1c, thermal balancing does reduce oscillations in temperature, and it reduces the general temperature level which still reduces conduction losses more than the switching losses are increased. The temperature delta between the hottest and coldest switch can be reduced by about 37 %.

It can be seen that already the proposed thermal balancing of regular (100 Hz) switching between current paths and modules, without a more elaborated control algorithm, does distribute the conduction losses significantly more equal, while still not increasing switching losses too much. Above the medium speed range, switching between the different modules of one phase should no longer be necessary and stands in conflict with SoC balancing of the modules in one phase. Switching between the upper and lower current path of the modules will still be beneficial. Using a more elaborated control strategy, switching losses caused by the thermal balancing could be further reduced.

4.3 SoC Balancing

SoC balancing was simulated and tested for two relevant cases. First, the operation of the H-bridges as DC/DC converters, utilizing the motor inductance at standstill, was simulated. Then, regular operation with the selective use of modules of one phase, as well as modifying the phases' active power to transfer charges between phases, was simulated. Figure 4.3.1 shows the simulation results for the balancing between two modules at standstill.

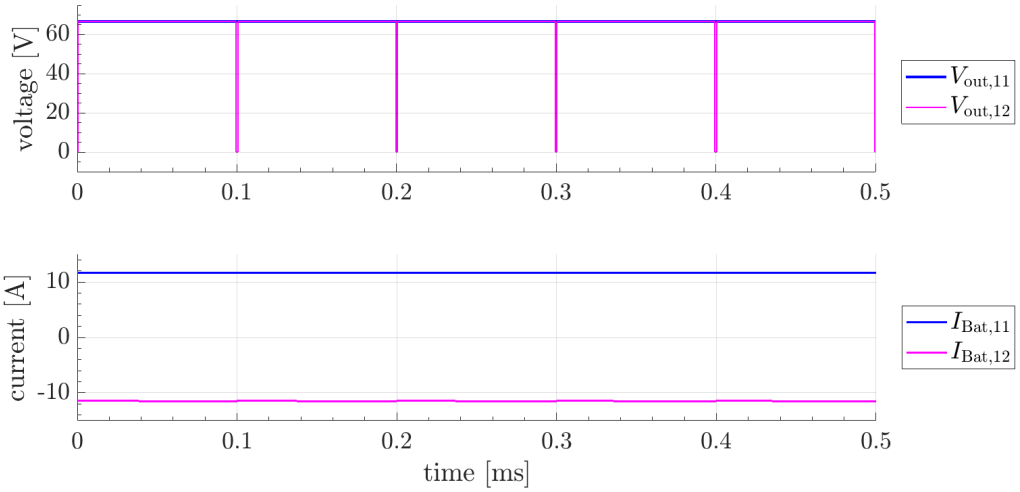


Figure 4.3.1: *DC balancing simulation results between two modules,* $d_{11} = 1$*,* $d_{12} = 0.99$*,* $\eta = 98.4\,\%$

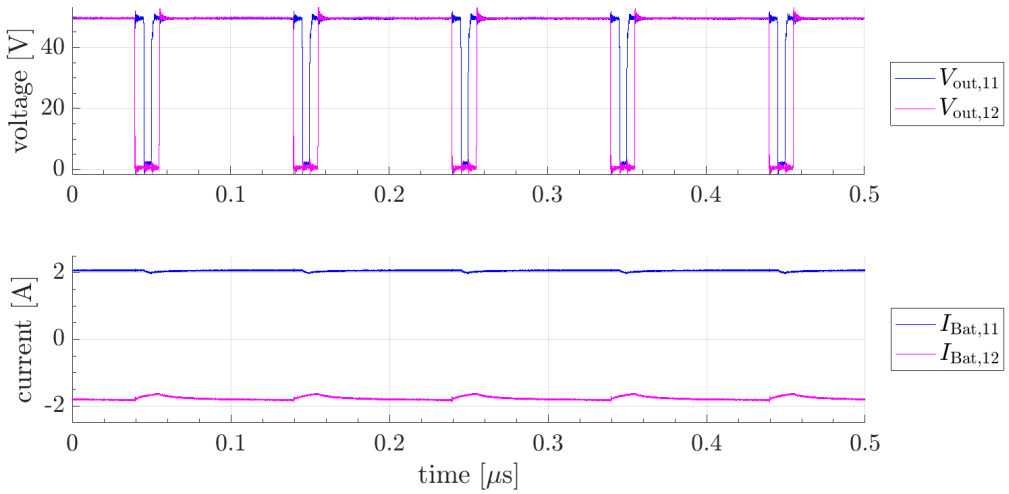


Figure 4.3.2: *DC balancing between two modules,* $d_{11} = 0.95$*,* $d_{12} = 0.9$*,* $L = 13.33\,\mathrm{mH}$*,* $R = 0.6\,\Omega$*,* $\eta = 86.2\,\%$

The electric machine's inductance is used as energy storage, while the current is adjusted via the voltage difference between modules, which is controlled by the duty cycle. Simulating with ideal switches and the motor inductance, as given in Table 3.1.3, charge transfer is possible with an inverter efficiency of $\eta = 98.4\,\%$ between arbitrary modules of one phase. If balancing between modules in different phases is needed, a module in the third phase needs to be set to an appropriate duty cycle to avoid an unwanted current flow.

The concept was then verified using the laboratory setup with a 3-phase-5-level configuration. Unfortunately, due to unknown reasons, the H-bridge inverter board does not allow switching the DC-source constantly to the output terminals. Thus a duty cycle of 1 is not possible in the laboratory setup. Figure 4.3.2 shows the measured module voltages and battery currents for balancing between two modules of one phase. Since a duty cycle of 1 is not possible, and the resistance of the used RL-load is rather high, only efficiency of 86.2 % is achieved.

Figure 4.3.3 shows the resulting DC-link voltages as measured during balancing of the unbalanced module voltages using a simple proportional control, driving the error from average voltage to zero. Even with the simple proportional control, the dc-link voltages and thus the SoC of the battery packs can be balanced in a reasonable time.

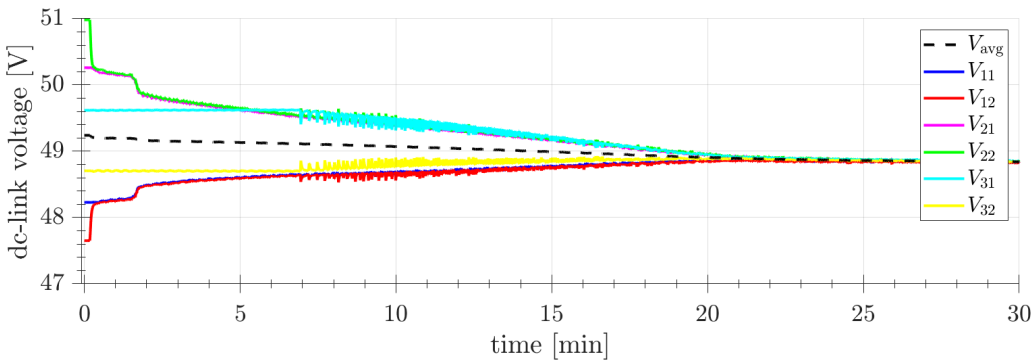
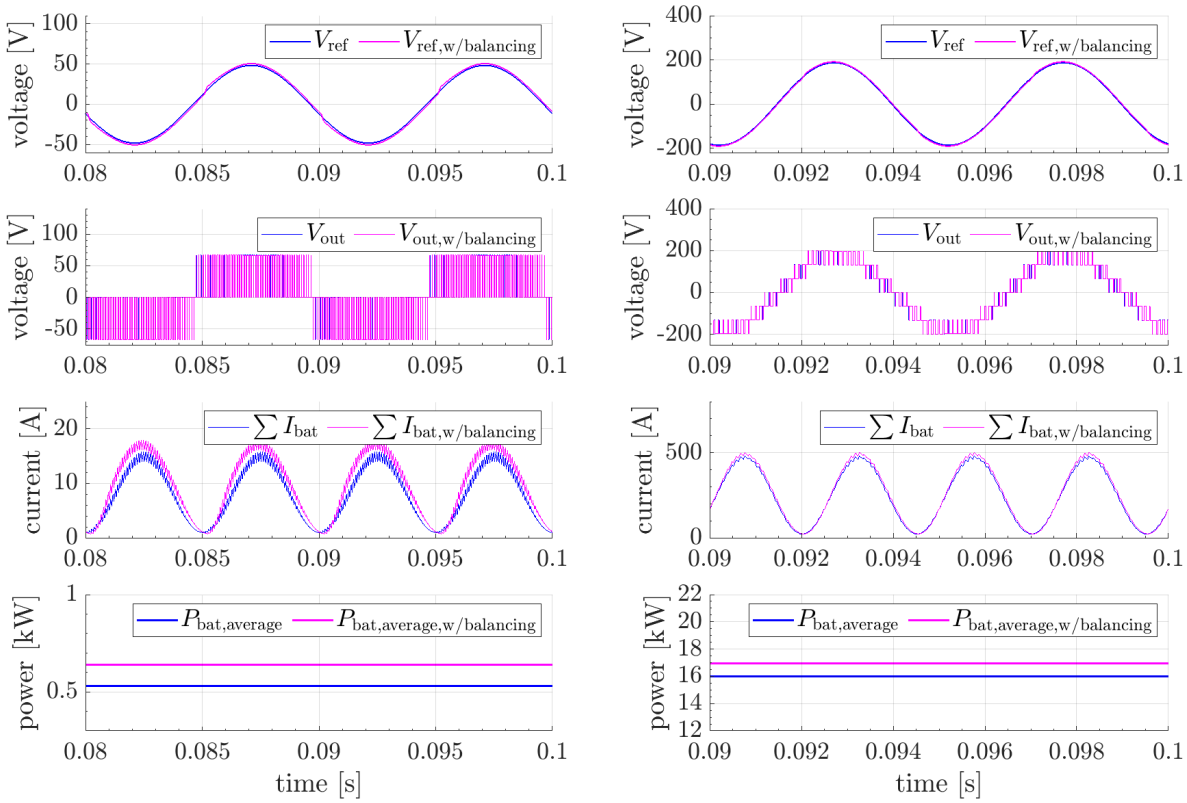


Figure 4.3.3: *DC balancing in 3-phase-5-level system*

For balancing during regular operation, a different strategy, modifying the reference voltage to change the active power output, was proposed and simulated. The results are shown in Figure 4.3.4. The first case, shown in Figure 4.3.4a, shows balancing at low speed. Here, only 3-level inverter operation is performed. It can be observed that the battery currents are shifted upwards, which correlates with the increased active power output of the batteries. As to be expected, current $\mathrm{THD_I}$ is significantly worse. Even though, efficiency is not changed significantly.

Figure 4.3.4b shows the simulation results for balancing during operation at medium speed and high torque. Here, again, a significant change in active power can be observed. Current $\mathrm{THD_I}$ is not worsened to the same extent as for low speed and low torque operation. This would reduce the introduced torque ripples.

The simulations show that the proposed principle is working without decreasing inverter efficiency too much. In terms of introduced torque ripples, is seems to be beneficial to apply as less balancing as possible in low-speed regions.

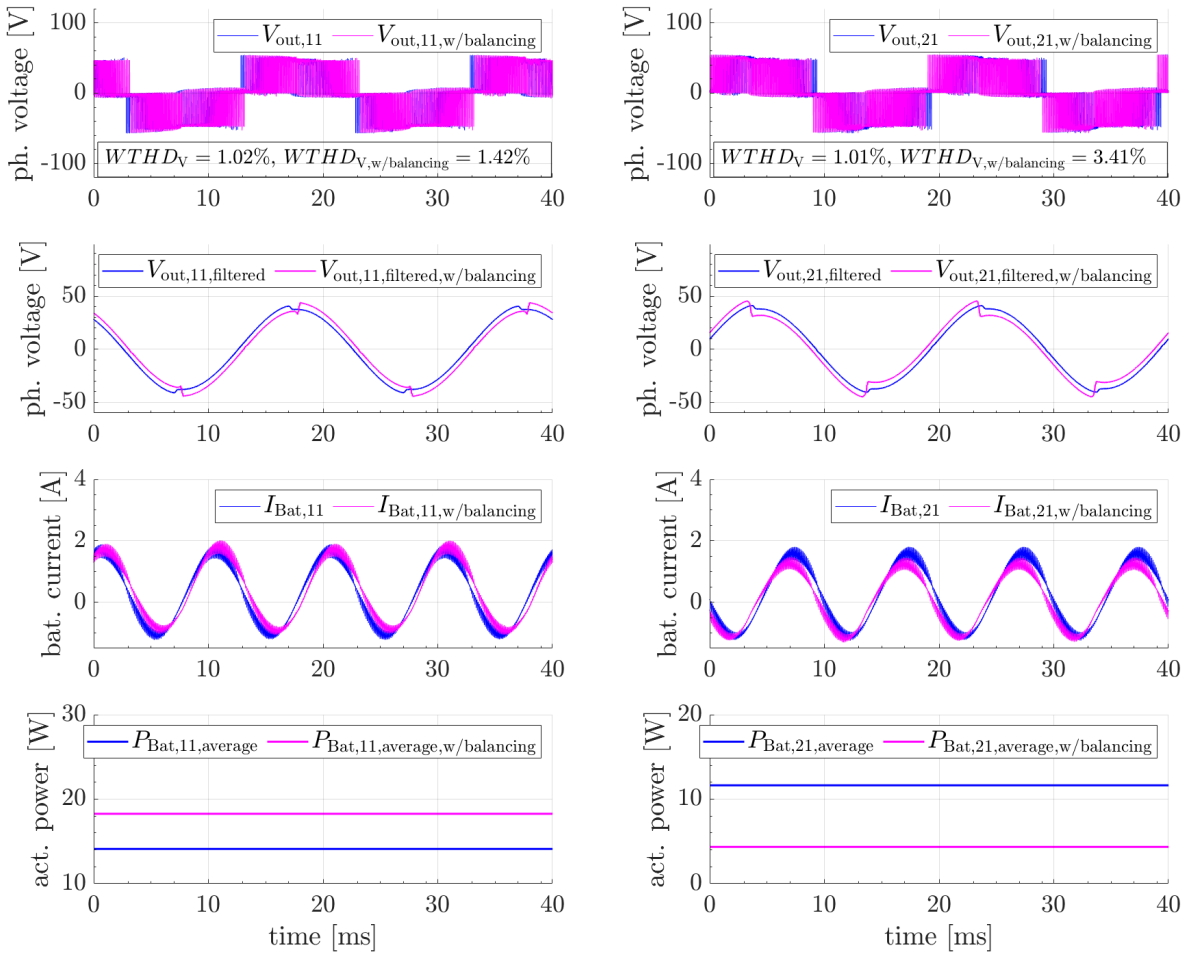


(a) *3-phase-3-level,* 100 Hz, 10 Nm,
$\eta = 98.40\,\%$, $THD_I = 3.89\,\%$, $WTHD_V = 0.74\,\%$
w/o balancing vs.
$\eta = 98.24\,\%$, $THD_I = 13.76\,\%$, $WTHD_V = 1.07\,\%$
w/ balancing

(b) *3-phase-7-level,* 200 Hz, 150 Nm,
$\eta = 98.40\,\%$, $THD_I = 0.81\,\%$, $WTHD_V = 0.38\,\%$
w/o balancing vs.
$\eta = 98.34\,\%$, $THD_I = 2.29\,\%$, $WTHD_V = 0.78\,\%$
w/ balancing

Figure 4.3.4: *Simulated waveforms for active balancing during operation*

To provide a verification for the simulations, the balancing between phases during regular operation was also tested using the laboratory setup. Figure 4.3.5 shows the measured waveforms for the phase with pushed active power and for the corresponding phase with suppressed active power output. The change in active power output is clearly visible, but also the introduction of an additional phase shift.



(a) *Phase A with pushed active power* (b) *Phase B with suppressed active power*

Figure 4.3.5: *Measured waveforms for active balancing during operation in 3-phase-3-level system*

Finally, the proposed setup was tested balancing unbalanced battery packs under regular operation. Both, balancing between modules of one phase, as well as between phases, was implemented. As described, this is achieved by switching between modules of one phase and a simple proportional control of the reference voltage offset for the balancing between phases. Figure 4.3.6 shows the measured module DC-link voltages. Because the degree of unbalance is high, and the battery capacity is high compared to the used energy, the balancing process is rather slow. Balancing between modules of one phase is relatively faster than balancing between phases. A significant reduction of unbalance is possible even with the simple proportional control.

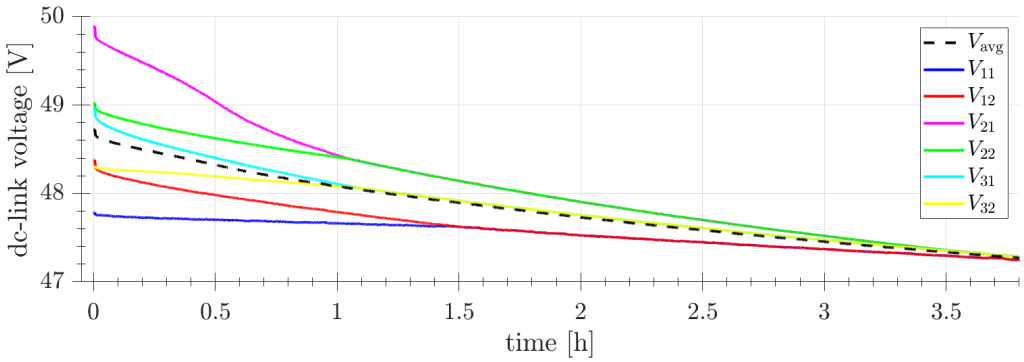


Figure 4.3.6: *Resulting equalization of the dc-link voltages due to active balancing during operation in a 3-phase-5-level system*

5 Conclusions

5.1 Results from the Present Work

This work analyzed different switching strategies for CHB multilevel inverters. PWM switching was compared to FSHE switching in terms of inverter efficiency, $\mathrm{WTHD_V}$, and $\mathrm{THD_I}$. The inverter efficiencies were also compared to a commonly used two-level inverter for the same traction application. It was shown that the analyzed multilevel inverter is about 2 % more efficient over most of the operation region. While this figure might not sound like a significant improvement, it corresponds to a rough halving of the inverter losses.

Comparing PWM and FSHE switching for the CHB multilevel inverter in terms of efficiency, a slight improvement in efficiency for FSHE switching could be observed. Apart from a region below a modulation index of 0.25, where FSHE switching is not applicable, FSHE switching results, on average, in a 0.087 % better efficiency, due to the reduced switching losses. Since the general efficiency level is at about 99 to 99.5 %, even this small increase in efficiency is significant. It was shown, that PWM switching results in lower $\mathrm{WTHD_V}$ levels below modulation indices of 0.84, which results in lower $\mathrm{THD_I}$ levels as well. Only from the medium-high speed region, FSHE switching was superior in all analyzed aspects. The experimental verification using the laboratory setup supported the findings from the simulations. Whenever all inverter levels are used, FSHE switching showed to have similar or lower $\mathrm{WHTD_V}$ and $\mathrm{THD_I}$ levels. Since efficiency is most likely the most important consideration for traction applications, it was proposed to apply FSHE switching wherever possible, thus above modulation indices of 0.25, and PWM switching below. This was shown to be a valid assumption.

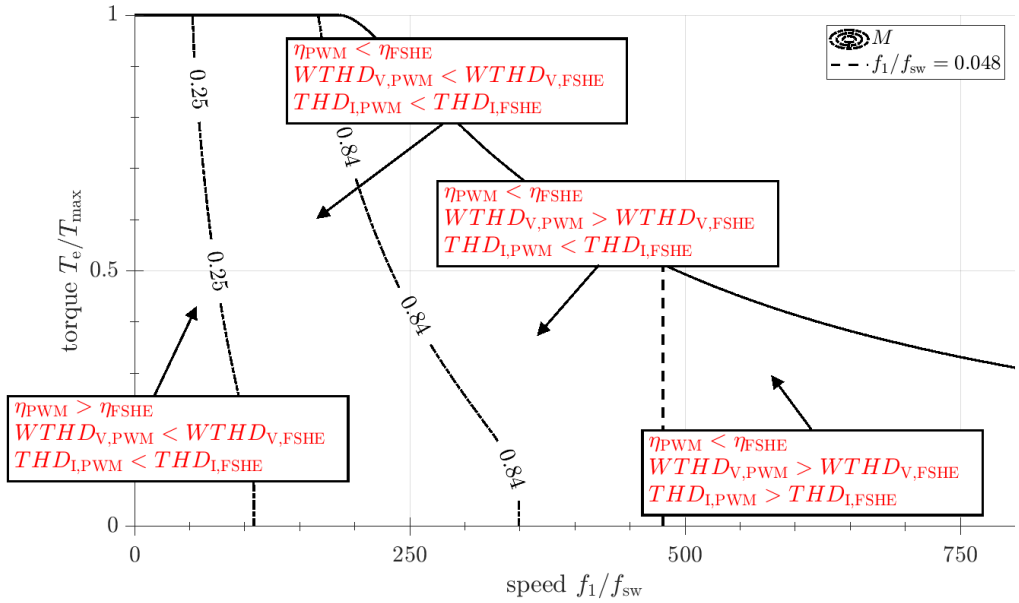


Figure 5.1.1: *Resulting subregions over the PMSM's operation region.*

Subsequently, an algorithm for thermal balancing between the upper and lower current path, as well as for distribution of the switching losses, was proposed and verified using simulations. It was shown, that during regular operation, the temperature differences between switches

could be reduced by about 30 %. The conduction losses were significantly reduced, while the switching losses were only slightly increased. Especially, for the extreme case of maximum torque at zero speed, the temperature differences could be reduced by about 67 %. In this situation, without thermal balancing, an overheating of single switches is very likely.

A CHB multilevel inverter provides the option of balancing the module's DC-links during regular operation or at standstill without further hardware. Two balancing techniques were introduced, simulated, and tested. For the situation that the vehicle is at standstill, thus speed and torque are zero, an arbitrary pair of modules can be operated as a DC/DC converter using the motor's inductance. This method shows to be very flexible and efficient and shows to be a working concept to balance between the modules. For balancing during regular operation, a different concept was proposed and tested. The modules of a phase were used, such that the highest duty cycle is assigned to the module with the highest SoC. The different phases were balanced by altering the active power output of the phases. This concept proved to be working, both in simulations, as well as in the laboratory. It was shown by experiments to be possible to balance an unbalanced CHB inverter using both concepts, even without an elaborated control strategy. Using the proposed balancing concepts, the battery, as a critical component in terms of sustainability, can be facilitated best, and unnecessary impacts on environment and society be avoided, without the need for additional hardware.

5.2 Future Work

This work compared FSHE and PWM switching for CHB multilevel inverters mainly by simulations. Verification was done for a few operation points using a basic laboratory setup, substituting the PMSM with an RL-load. A proper comparison of FSHE and PWM switching using a full three-phase laboratory setup including an electric machine would provide further insights. Also the efficiency should be analyzed using measurement data.

In this work, the different balancing strategies, both thermal and SoC balancing, were only simulated and tested using the laboratory setup as a proof of concept. Here, the development of more elaborated control strategies is required to increase the efficiency and speed of the balancing.

From a systems perspective, testing the whole setup, including a PMSM, the FSHE/PWM switching strategy, as well as the balancing strategies, possibly over standardized or real-world driving cycles appears as a interesting round up of the project.

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