Design and evaluation of a 1kW DC/DC - converter for contactless power transfer

DC/DC-converter utilizing a rotating transformer in an environment demanding high duty cycle and low voltage drops

Master of Science Thesis

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Abstract

The concept of contactless transfer of power to rotating sensors have long been a desired feature. Today the technology relied upon to supply such moving parts with power is slip rings. While being a well proven technology, slip rings are subject to wear and this in turn results in a relatively high maintenence frequency.

This master thesis deals with the design and evaluation of a 1kW DC/DC-converter. The purpose of this DC/DC-converter is to be used together with a rotating transformer in order to attain a contactless transfer of power for rotating sensors. The inverter part of the converter uses a full bridge topology. For the rectifier side, two different aspects are investigated and evaluated, diode rectifier bridges versus synchronous MOSFET rectifier bridges as well as the use of center-tap configuration of the transformer versus a single secondary winding.

The resulting DC/DC-converter is a full bridge inverter with n-channel MOSFETs paralleled two and two. The transformer is connected with a single secondary winding (2:4 turns ratio) resulting in a total leakage inductance of 140nH and an effective maximum duty cycle of 97% at a switching frequency of 55kHz. The final rectifier used is a full bridge self-driven synchronous MOSFET rectifier, utilizing the secondary side of the transformer for gate signals. With an input of 450W at 28V the converter reaches an efficiency of 94,4%, with the majority of the loss originating in the MOSFET's switching and conduction of the inverter.

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Contents

1 Introduction 1
- 1.1 Problem background . . . 1
- 1.2 Previous work . . . 1
- 1.3 Purpose . . . 2
- 1.4 Delimitations . . . 2

2 Technical background 3
- 2.1 Inverter . . . 3
  - 2.1.1 Switching . . . 3
  - 2.1.2 Switching scheme . . . 4
  - 2.1.3 Duty cycle loss of the inverter . . . 7
- 2.2 Rotating transformer . . . 8
  - 2.2.1 Core loss - Hysteresis loss . . . 8
  - 2.2.2 Magnetizing inductance . . . 10
  - 2.2.3 Leakage inductance . . . 10
  - 2.2.4 Winding resistance considerations . . . 11
- 2.3 Rectifier . . . 11
  - 2.3.1 Full wave diode rectifier - Single secondary winding . . . 12
  - 2.3.2 Full wave diode rectifier - Center-tap on secondary winding . . . 13
  - 2.3.3 Self-driven synchronous rectifier - Center-tap on secondary winding . . . 14
  - 2.3.4 Self-driven synchronous rectifier - Single secondary winding (H-bridge rectifier) . . . 15
- 2.4 Snubber . . . 16
- 2.5 MOSFET theory . . . 19
  - 2.5.1 MOSFET intrinsic body diode . . . 19
  - 2.5.2 MOSFET switching characteristic . . . 20
  - 2.5.3 MOSFET power losses . . . 23

3 Measurements and calculations 24
- 3.1 Measured duty cycle loss . . . 26
  - 3.1.1 Influence on the total leakage inductance caused by conductors . . . 27
  - 3.1.2 Synchronous rectification and effective duty cycle . . . 29
- 3.2 Full bridge inverter losses . . . 30
  - 3.2.1 Original full bridge inverter - Old MOSFETs . . . 30
  - 3.2.2 Improved full bridge inverter - New MOSFETs . . . 33
- 3.3 RotatingTransformer effects . . . 36

3.4 Rectifier voltage - and power loss 38
3.4.1 Measurements on the full wave diode rectifier - Single secondary winding 38
3.4.2 Measurements on the full wave diode rectifier - Center-tap on secondary winding 39
3.4.3 Measurements on the self-driven synchronous rectifier - center-tap on secondary transformer winding 40
3.4.4 Measurements on the self-driven synchronous rectifier - single secondary transformer winding 41
3.5 Snubber design 43
3.6 Output filter design 43

4 Conclusion **46**
4.1 Results and discussion 46
4.1.1 Inverter 46
4.1.2 Transformer 47
4.1.3 Center-tap 47
4.1.4 Rectifier 48
4.1.5 Influence on the leakage inductance caused by the switching frequency 49
4.2 Future work 50

5 References **51**

1 Introduction

1.1 Problem background

In today's radar systems the rotating antenna is provided with power via slip rings and rotating joints. Due to extreme demands on electro magnetic compatibility, EMC, introduced by radio communication etc, around the antenna, these mechanical parts are highly complex and prone to be in need of maintenance. The major issue with this solution is, apart from being a complex piece of mechanics which demands very specific knowledge, the fact that the wear lead to a relatively high maintenance frequency. An alternate method of transfering power could be using an inductive coupling via a rotating transformer which then provde a contactless and thus friction-less solution. In the system in question the antenna electronics requires a bus voltage of 56V DC which could potentially be supplied from the already available 28V DC in static parts of the radar system, if DC-transformation was applied.

1.2 Previous work

A great deal of research in this subject, with different solution of the problems evolving from this scenario. The main issues of this research being to keep the losses as well as the EMI low, e.g. (Papastergiou and Macpherson 2007). A common conclusion is that a fairly high frequency should be used in order to reduce the filter losses, however few texts deal with the issue of high duty cycle demand. In order to keep frequency high the switching usually has to be done in a low loss and low electro magnetic interference, EMI, manner. There are two aspects involved in this process. First the switching losses, introduced by the current through the switch and the voltage over the switch being non-zero simultaneously during the switching, should be reduced. This is normally done by forcing the switching to occur during zero-voltage (ZVS) or zero-current (ZCS) conditions. A great number of papers have been published in this field and the number of solutions to the problem is steadily growing. The main idea however is to cleverly use the different paths of the circuit in order to use the natural commutations of for instance diodes to perform the switching at appropriate times or by using a controlled resonance and time the switching according to that. While doing this the EMI should be limited by either shielding or limiting the di/dt- and dv/dt- properties of elements in the circuit.

1.3 Purpose

The purpose of this thesis is to design and evaluate a building block, prototype of a complete DC/DC converter, using partly already available converter parts.

The main purpose is to perform an analysis of the feasibility of using the rotating transformer in this type of system and to construct a technical specification of the requirements for such a system. The DC/DC converter should have a working range of 500W to 1000W and give an output voltage of between 48V and 60V, keeping as close to 56V as possible and at the same time attain a high efficiency.

1.4 Delimitations

The only aspect of the transformer investigated in this thesis is the use of different winding configurations. The converter should utilize hard switching, i.e. not purposely working towards soft-switching. The output voltage waveform, pre-filter may not rise above 60V. This adds a limitation on the transformer winding ratio that is possible to use for the transformer. Since the average output voltage desired (56V) is fairly close to this maximum allowed value (60V), this also means that a high duty ratio, as close to 100% as possible, is required. This, due to the fact that a lower current would lead to a reduction of inductive duty cycle loss, result in an unexpected duty cycle increase. The converter should ideally not require any control signals from external systems in order to operate efficiently. The thesis should work with a predetermined transformer, with 4 turns on primary and secondary side, giving a very limited number of winding configuration options. The 56V DC on the secondary side can be allowed to vary slightly, meaning that the converter does not need to have a primary to secondary side feedback control.

2 Technical background

2.1 Inverter

One of the main factors regarding the use of a rotating transformer compared to the conventional systems is the low magnetizing inductance introduced by the existence of a substantial air gap. This air gap has to be there in order to allow rotation of the transformer with little or close to zero friction. The resulting magnetizing current, that will always flow through the primary side regardless of the loading level, will result in increased conduction losses.

In situations like this, where the primary side current is of high importance, a common inverter is the phase-shifted full bridge inverter, PSFB. In the PSFB an auxiliary circuit is used in order to introduce the necessary energy needed to discharge a parallel capacitance and by the use of that attain zero-voltage transitions of the switches.

At these kinds of power levels, full bridge configurations are popular for several reasons but mostly due to their bidirectional quality, meaning it provides the full input voltage in both positive and negative direction, as opposed to half the input voltage, which would be the case of a unidirectional inverter. Having higher voltage means lower current and thus decreased conduction losses.

When it comes to the choice of switch type, in this thesis MOSFETs are considered. Greatly due to good high-frequency characteristics and possibility of low conduction losses but also due to the unacceptable voltage drop of for instance IGBTs, which otherwise might have been considered as an alternative.

2.1.1 Switching

Using fixed duty cycle, allows for an optimization of the drive circuit components for this specific duty cycle. Due to certain degrees of freedom introduced by the application specification (there is a high performance DC/DC converter on the input of the load) there is no need for feedback control, i.e. the converter should provide a fix ratio between input and output, regardless of variation in load- and input- voltage. To reduce output ripple one can either increase the size of the output filter or increase the frequency. Commonly one would prefer to increase the frequency to minimize losses. In order to maintain a fairly high frequency it becomes highly relevant that the losses involved with this do not go out of hand and the benefits of the higher frequency does not get outweighed.

Traditionally this might be achieved by performing soft-switching and thus removing most of the switching losses, however the aim of this thesis is to provide a working model and not to add extra complexity.

2.1.2 Switching scheme

The inverter considered in this thesis is a full bridge inverter, based on an existing PSFB inverter, where the phase shift is driven to be as close to 100% as possible. This inverter is designed for a higher voltage and power level but approximately the same load current, resulting in similar demands on cooling and thus mounting, making it a suitable starting point. The term phase shifted full bridge relates to a control scheme where both legs are separately driven to a duty ratio very close to 50% and then phase shifted against each other (Andreycak 1997). Other than the 180 degrees shift between the two legs' waveforms there is also a delay between the turn off of one transistor and the turn on of the other one in the same leg. Primarily this ensure that the full bridge doesn't suffer from current shoot through, which it otherwise would have issues with at time periods where both the upper and the lower transistor in the same leg are open, i.e. the supply is short circuited. The main point about phase shifted control in comparison with using conventional pulse width modulation (pwm) waveforms is the possibility to not only control the duty cycle but also add some degree of control of the switching losses. In the proposed full bridge, it is not possible to reach quite 100% phase shift, but one can get very close, around 99%. The basic switching waveforms are shown in Figure 2.1.

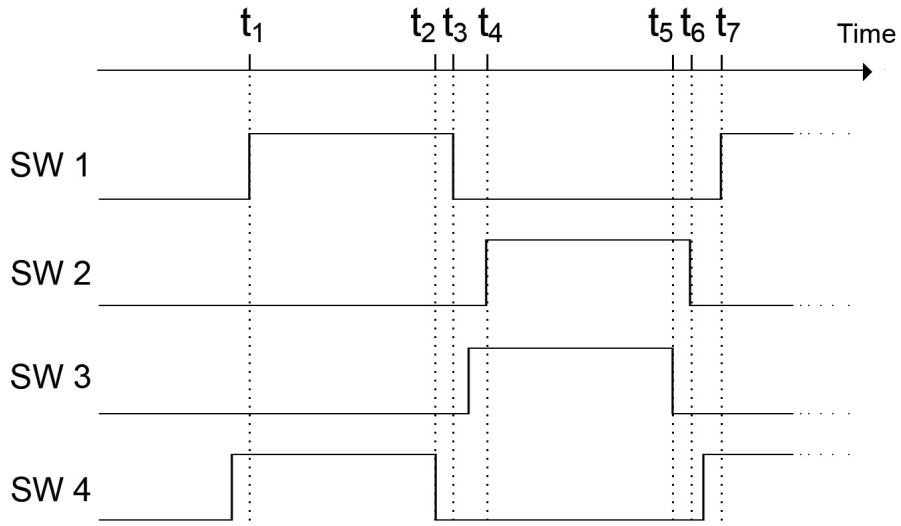
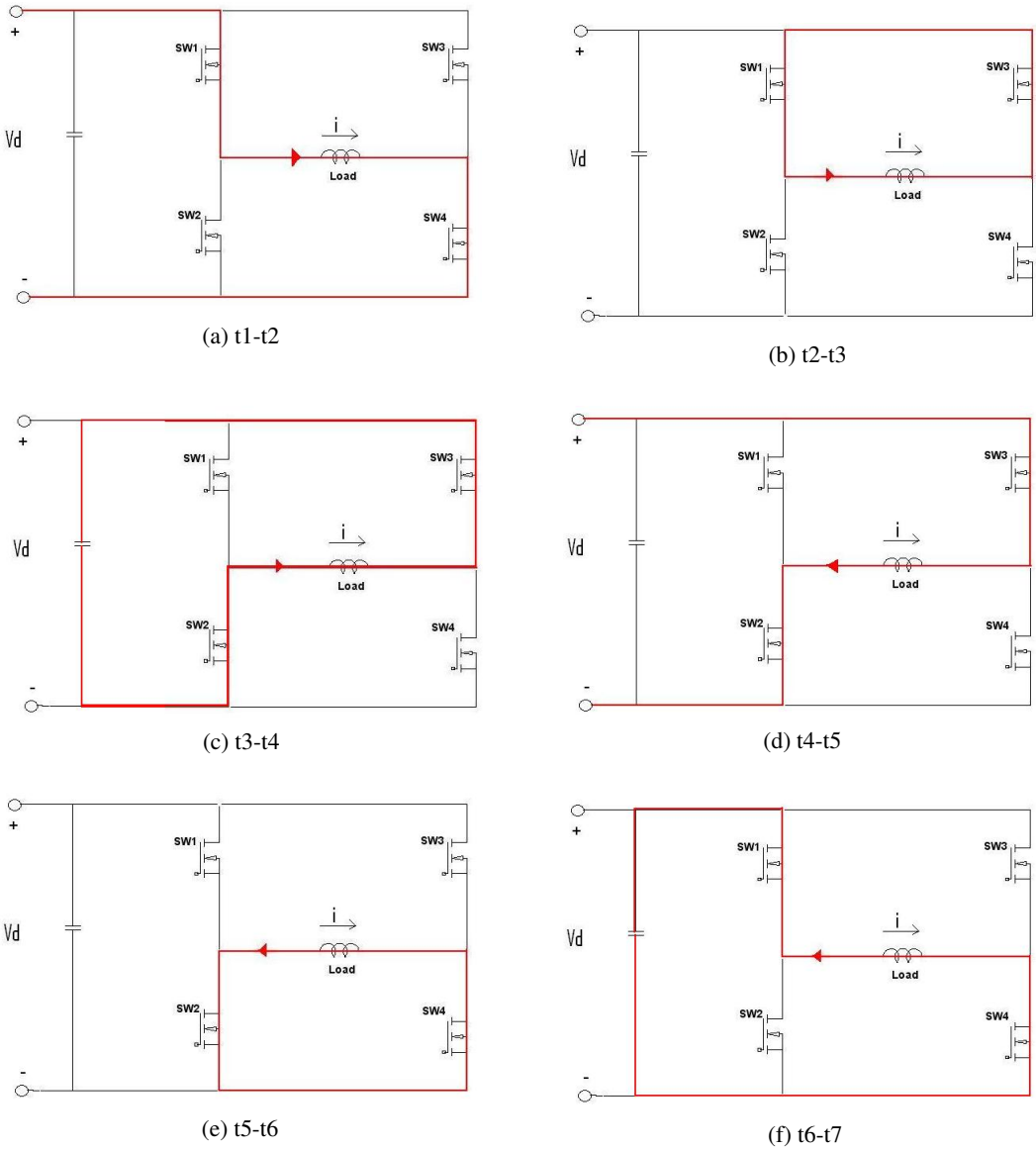


Figure 2.1: Switching waveforms of the proposed phase shifted full bridge inverter (Gate-source signals).

The resulting switching scheme is described in Figure 2.2.



(a) t1-t2

(b) t2-t3

(c) t3-t4

(d) t4-t5

(e) t5-t6

(f) t6-t7

Figure 2.2: Switching schedule of the phase shifted full bridge inverter.

The switching schedule illustrated in Figure 2.2 is broken down into time intervals and explained below.

t1-t2 At this point, the load current flows in the positive reference direction through SW1 and SW4, as shown in Figure 2.2a. Power is being delivered to the the load and the overall full bridge is in an on-state. At t2, SW4 is turned off.

t2-t3 The case of Figure 2.2b. During the turn-off of SW4, its current commutates to the body diode of SW3. This interval is the part of the dead-time controlled by the phase shifted gate-pulse control and often referred to as the freewheeling interval. With the control used in this thesis, the freewheeling intervals last for approximately 40 ns, according to Figure 2.3 below.

t3-t4 At t3 SW1 is turned off and the decreasing current through it, if any, commutates to the body diode of SW2, Figure 2.2c. The description of this stage depends on the load condition and the inductance of the converter circuit. If the full load current reaches zero within the 40 ns of period t2-t3, the current will simply be zero until t4. If not, the time between t3 and t4 is set by the time it takes for the current to reach zero at full, reversed supply voltage.

t4-t5 At t4 the case of Figure 2.2d starts as the current has reversed and is actively driven in the negative reference direction through SW2 and SW3, which are turned on (SW2 40ns after SW3). Similar to period t1-t2 this goes on until t5 where SW3 is turned off.

t5-t6 As in the other half period, the current previously in the right leg MOSFET commutates to the body diode of the opposite transistor in the same leg, in this case the current through SW3 commutates to the body diode of SW4, as shown in Figure 2.2e. After another 40 ns delay t6 is reached.

t6-t7 At t6 SW2 is turned off, while SW2 is turned on and the current through SW2 commutates to the body diode of SW1. This stage ends at t7, where the case of Figure 2.2f has begun. The current reversal is completed and SW1 and SW4 is turned on (SW1 40 ns after SW4) as the switching scheme is repeated from t1.

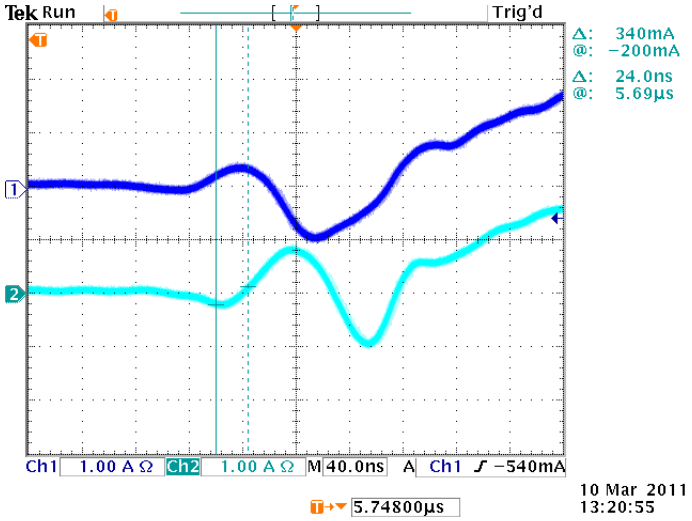


Figure 2.3: Channel 1(Dark blue): Drain current of SW4, Channel 2(Light blue): Drain current of SW1. The current waveforms are shown for the instance of turn-on for the SW1 and SW4 path. When the current goes from zero to a negative value is when the current commutates to the MOSFETs body diode. The 40 ns delay between the two diode turn-ons is the controlled dead-time where the freewheeling goes on, 2.2e.

2.1.3 Duty cycle loss of the inverter

As mentioned in previous chapters an important part of the evaluation of the DC/DC-converter is the losses in power within it, but another fairly important part is the loss of duty cycle. In general this is due to the resulting current ripple that a decreased duty ratio entails. However, in this application the most relevant factor is the need for a specific voltage output with a very narrow limit on pre-filter voltage amplitude (i.e. the average voltage must not vary much from the unfiltered voltage maximum).

$$U_{inductor} = L_{inductor} \cdot \frac{\Delta i}{\Delta t} \tag{2.1}$$

A rough estimate of the induced voltage over the output filter inductor is given by 2.1. Assuming a fairly constant output voltage the inductor voltage is known to be the difference between the instantaneous rectifier output voltage and its average, i.e. the output voltage. For a given frequency, the ratio time Δt is given by the duty cycle, where an increased duty cycle loss results in a longer dead time and thus longer Δt. As the ratio $\frac{\Delta i}{\Delta t}$ is fixed for a given inductance and induced voltage, an increased duty cycle loss means a greater inductance is needed to keep the current ripple at the same level. Larger inductors means problems in several areas. First of all, the core losses of the inductors, depending a little on the choice of core type, increases with the volume of the inductor core (assuming the same material) (Schade). While the energy loss per core volume decreases with an increased cross section area, the total volume would increase slightly more in most cases.

The other factor is slightly more obvious, the size and weight of the complete converter. For the sake of this thesis the duty cycle is, as mentioned, not only important due to the increased filter losses a poor duty cycle ratio would entail, but also by the fact that the application it is meant for requires a specific range of voltage input/output ratios.

2.2 Rotating transformer

There are three factors of the transformer needed to be investigated for this thesis. First the magnetizing inductance of the transformer, as this determines the amount of core loss to be expected and secondly the leakage inductance of the transformer and finally the winding resistance. The fact that the transformer is a rotating transformer does not actually affect this thesis very much since the choice of transformer is one of the already available delimitations and thus no design apart from the choice of winding configuration is possible. One factor needed to be considered, however, is the effect of the transformer's air gap. In an optimized none-moving transformer, the air gap would be reduced, but in this case it is needed to allow for friction free movement.

2.2.1 Core loss - Hysteresis loss

When looking at the losses of a transformer there are, as mentioned above, several aspects that should be considered. First there is the obvious part of resistive losses, caused by traditional resistive heating by current in the conductor windings. While this has a frequency dependence introduced by the induced eddy currents, the electric power loss is still caused by simply conduction heating. The second and in this case more important part is the magnetizing losses within the core.

Every time the magnetic flux is reversed within the core, the magnetic dipoles of the material align themselves with the field causing a certain amount of loss equal to the energy required to move the dipoles. This is often illustrated by a hysteresis, like the one in Figure 2.4, thus explaining the name, hysteresis loss.

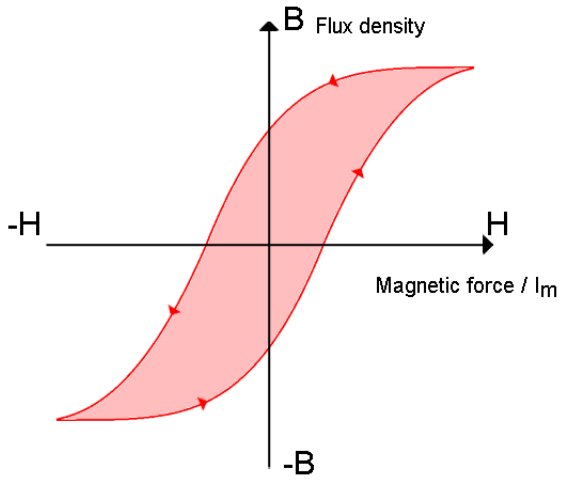


Figure 2.4: Magnetic hysteresis, depicting the energy loss involved in reversing the polarity of a certain magnetic material.

The figure shows the magnetic flux density, B, inside the core versus the magnetic field applied, i.e. the magnetizing current. If a magnetic field is applied and then removed, the energy used to align the dipoles within the core material is stored and must be removed in order to return the flux to zero. Every time the polarity of the current in the transformer changes, this stored energy is removed at the cost of the curve shifting, as extra magnetic force is required to change the magnetic flux. The energy loss involved in every switching period is illustrated by the area enclosed by this hysteresis.

2.2.2 Magnetizing inductance

In the prestudy of the rotating transformer, the magnetizing inductance has been measured under certain conditions with the use of no-load tests. At 50.3kHz, the magnetizing inductance is found to be approximately 20.25µH in a 1:4 winding ratio connection. In this thesis, both center-tap configuration, where two seperate windings with a common center-point is used on the secondary, as well as single secondary winding is to be considered. The values should therefore be known for a winding ratio of 1:2:2 and 2:4. Depending on how good an approximation of the inductance one needs, complicated formulas to calculate more or less accurate values, depending on form factors etc can be used. However in this case, due to the limitations at hand, the only thing interesting is the approximate ratio between these two cases. As such, an adequate approximation can be found by simply stating that the magnetizing inductance is proportional to the number of primary windings, squared. I.e. if the primary windings change from 1 to 2, the magnetizing inductance increases approximately with a factor of 4. Further, in the prestudy, the core losses are found to be approximately 27.3W for the 1:2:2 configuration and 2.73W for the 2:4 configuration in theory. The approximated values are presented in Table 2.1.

2.2.3 Leakage inductance

An other important factor is, as mentioned above, the leakage inductance of the transformer and the rest of the circuit. This is not so much related to losses as in the case of the magnetizing inductance but in current reversal speed. The speed at which the current can be reversed is directly related to how high switching frequency can be used in order to achieve an adequate duty ratio. The time it takes to reverse the current results in a forced dead-time and the higher the frequency, the more it affects the possible duty ratio. In the same prestudy of the transformer, measurements of the transformer leakage inductance at 52kHz can be found to be approximately 500nH at four primary turns. With the same reasoning as with the magnetizing inductance, the leakage inductance values at ratios of 1:2:2 and 2:4 becomes 31.25nH and 125nH respectively. The assumption here is that changing the winding configuration does not affect form factors as well as mutual inductance between the two secondary windings. These result are also shown in Table 2.1.

Table 2.1: Theoretical transformer parameters. These are extrapolated using known values at different winding configuration and very similar frequencies.

	Center-tap	Single secondary winding
	1:2:2	2:4
Magnetizing inductance	$20.25\mu H$	$81\mu H$
Leakage inductance	$31.25nH$	$125nH$
Core loss	$27.3W$	$2.73W$

An easy way, to measure total leakage inductance of a circuit like this one, is to look at the current induced dead time at the input of the rectifier part. With the current and voltage known, all that is needed is the dead time, in order to calculate the inductance according to:

$$V_{in} = L_{leakage}\frac{2 \cdot I_{in}}{T_{dead-time}} \Rightarrow L_{leakage} = \frac{V_{in} \cdot T_{dead-time}}{2 \cdot I_{in}} \tag{2.2}$$

2.2.4 Winding resistance considerations

The transformer is designed in such a way that the winding resistance should be a very small part of the total impedance seen by the primary side, however it has not been completely optimized. As the resistance is subject to the skin effect at alternating currents, the skin depth is what limits the resistance. In a final winding design this would be accounted for to make sure, at the frequency you want to use, the skin dept take up as big part of the complete winding cross-section as possible, but no more.

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{2.3}$$

where:
δ =the skin depth
ρ = resistivity of the conductor
ω = angular frequency of the alternating current
μ = absolute magnetic permeability of the conductor
In this transformer this fact is, however, merely pointed out but not designed for.

2.3 Rectifier

When it comes to the rectification part of the converter, there are two aspects investigated in this thesis. First the option to use a center-tap on the transformer secondary winding should be investigated in terms of voltage drop, duty cycle and efficiency, where the positive aspects should be weighted against the negative. Secondly the possible benefits of using synchronous rectification should be investigated for two cases with and without a center-tap configuration on the transformer secondary winding. As there is only a factor of two between the voltage on the primary and secondary side, the voltage drop over the active components must still be kept well below that of for instance IGBTs and also here MOSFETs are chosen as active components, i.e. for the synchronous rectifiers.

2.3.1 Full wave diode rectifier - Single secondary winding

The single winding diode rectifier bridge is one of the most commonly used rectifiers in electronic equipment. It is a full-wave rectifier, using four diodes to rectify alternating current and its set-up is illustrated in Figure 2.5.

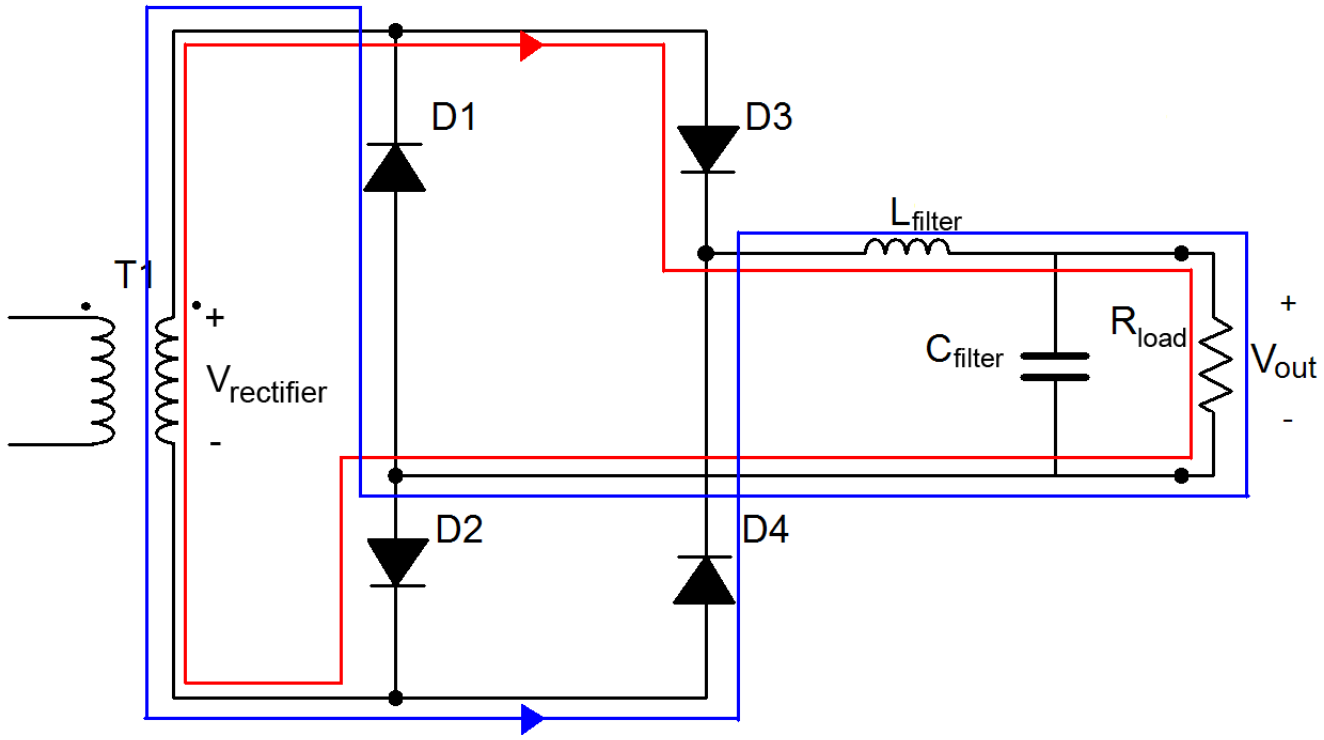


Figure 2.5: Traditional four diode full wave diode rectifier for a single secondary transformer winding. The blue and red lines/arrows show the two different current paths of the rectifier.

When $V_{rectifier}$ is positive, D3 and D2 are forward biased and the current starts to conduct through them. At the same time, D1 and D4 becomes reversed biased, thus preventing the current to flow through them. When $V_{rectifier}$ changes polarity, it is the other way around. The current then flows through D1 and D4 while D2 and D3 are blocking and the output voltage will keep the same polarity.

The main benefits using a diode bridge are its simplicity and the low design costs. The big disadvantage is on the other hand the voltage drops over each diode and the conduction losses that will arise.

2.3.2 Full wave diode rectifier - Center-tap on secondary winding

The center-tapped full wave rectifier utilizes the two secondary windings of a transformer in a way that only two diodes are needed in the rectifier (Figure 2.6).

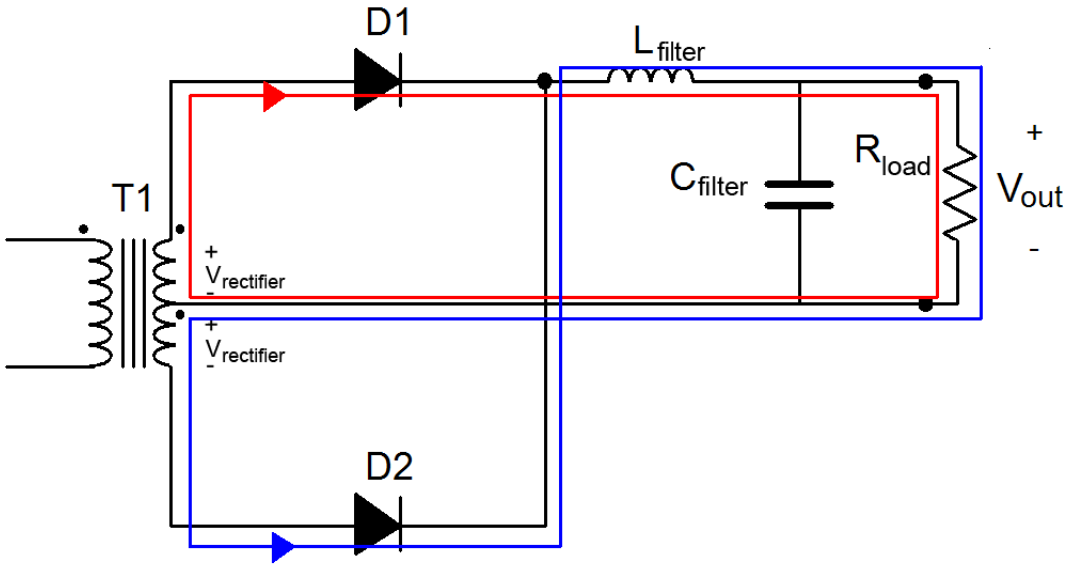


Figure 2.6: Full wave diode rectifier with a center-tap on the secondary transformer winding. The blue and red lines/arrows show the two different current paths of the rectifier.

The number of turns for both windings on the secondary side is the same and the voltage across each winding will thereby be the same. When $V_{rectifier}$ is positive, D1 will be forward biased while D2 is blocking and the current will flow out from the dot on the first winding on the secondary side. When the input voltage change polarity, D2 will be forward biased while D1 is blocking, and the current will flow into the dot of the second winding on the secondary side. Since this center-tapped full wave rectifier uses only two diodes, the voltage drop and conducting losses are lower than for the diode bridge, making it more suitable for low voltage and high current systems.

2.3.3 Self-driven synchronous rectifier - Center-tap on secondary winding

If the voltage drop over the rectifier is of great importance, a rectifier which is self driven and synchronous can be obtained by utilizing the secondary winding of a center-tapped transformer in a way that is showed in Figure 2.7.

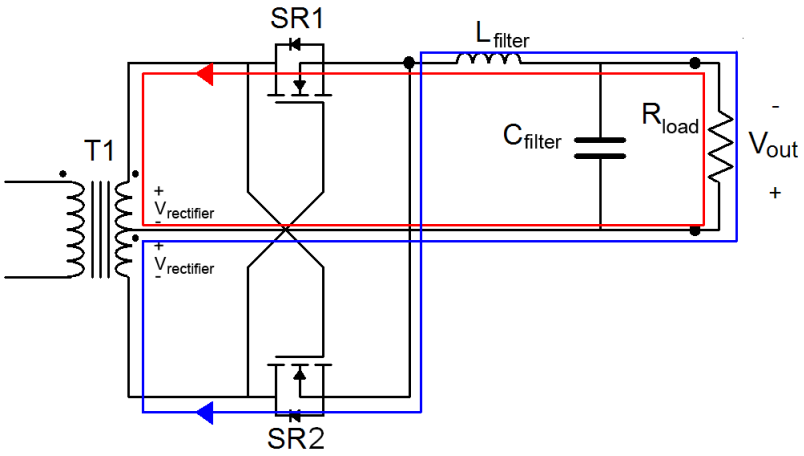


Figure 2.7: Full wave self-driven synchronous MOSFET rectifier, with a center-tap on the secondary transformer winding. The blue and red lines/arrows show the two different current paths of the rectifier.

This design is a step taken further from the previous center-tapped full wave rectifier, in which two diodes were used for rectification. The diodes have now been replaced with transistors which have a lower on-state resistance and the voltage drop over the rectifier will thereby be reduced. To turn the transistors on and off, the gates are driven directly by the pulsating voltage on the two secondary windings of the transformer. Seen from the output of the rectifier, the center-tap is the positive polarity while the negative polarity is taken from either upper or lower part of the transformer output in accordance to the voltage polarity of $V_{rectifier}$. Figure 2.7 shows the current path for the first and second half cycle of $V_{rectifier}$. At the first half cycle when $V_{rectifier}$ is positive, $V_{gs,SR1}$ is negative and transistor SR1 will be in a blocking state. Since SR2 now becomes reversed biased the current will start to flow from source to drain through the body diode. However, due to the resulting positive $V_{gs.SR2}$, SR2 is turned on and the current flows through the conducting channel. At the second half cycle when $V_{rectifier}$is negative, it will be the other way around. SR2 will be turned off and the current flows from source to drain inside the turned on SR1.

A possible disadvantage of this rectifier design is that if the duty cycle is not high enough, there will be a period where the transformer voltage will be zero. As a result, the gate signals become zero and the transistors conduct through their body diodes (described in section 2.5.1), which leads to increased losses. Another obvious shortcoming of the circuit shown in Figure 2.7 is that the gate source voltages need to be clamped below the maximum allowed voltage, in this case below 30V, in order to not break the transistors.

2.3.4 Self-driven synchronous rectifier - Single secondary winding (H-bridge rectifier)

If a center-tapped transformer is hard to achieve, the synchronous H-bridge rectifier is a good choice when the voltage drop of a diode is unacceptable. This rectifier can be seen as a four diode rectifier bridge, but with its diodes replaced with transistors. Due to the internal body diode of the MOSFET the transistor can only prevent current flowing in one direction (drain to source). Hence, to prevent a possible short circuit in one of the legs of the H-bridge, it is of great importance that the transistors are oriented in the correct direction, see Figure 2.8.

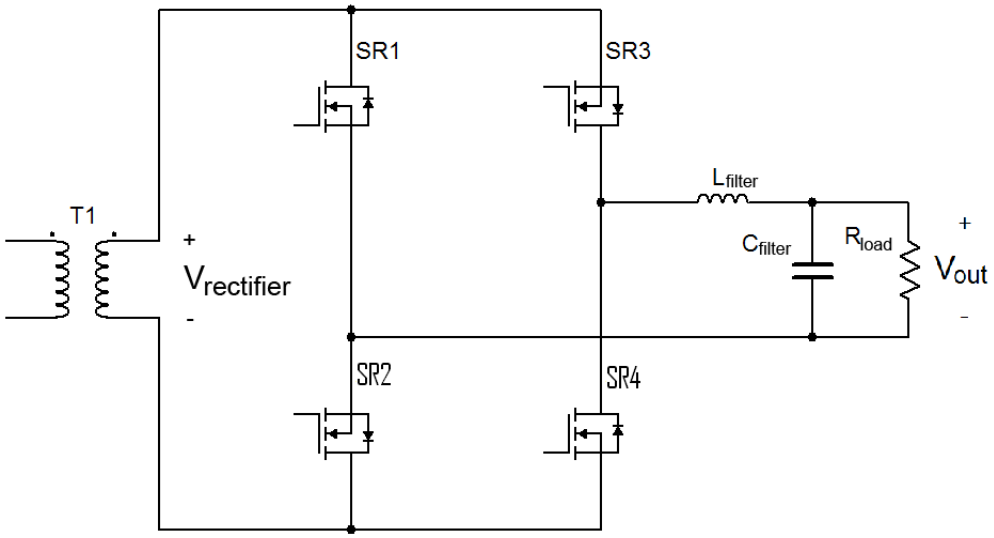


Figure 2.8: Full wave self driven synchronous MOSFET rectifier, with a single secondary transformer winding.

One of the differences between this one and the synchronous rectifier with a center-tap is that it is not quite as easy to drive by directly using the transformer secondary winding, so it usually requires a special connection in order to acquire gate drive signals.

The transistors here are N-channel enhancement MOSFETs and they have been connected in such a way that they may only conduct in the reverse direction. This means that without gate driver the rectifier would have the same operation as that of a diode bridge. However, turning the transistors on by applying synchronous gate pulses to the transistor gates will allow the majority of the current to start flowing through enhanced low resistance n-channel instead of the intrinsic body diode. When $V_{rectifier}$ is positive, the current will flow through SR3 and SR2 or SR1 and SR4 if $V_{rectifier}$ is negative.

2.4 Snubber

There are many different types of snubbers, used for different situations. In the types of application regarded in this thesis, there are basically two groups of snubbers considered:

- Turn-off snubbers - Used to decrease the $\delta V/\delta t$ of the voltage between the drain and the source of transistors in order to reduce the losses at turn-off of these transistors, through zero - or lower than nominal voltage transition.
- Damping snubbers - Similar to the turn-off snubber but more focus on the damping coefficient, in order to reduce ringing effects at inductive turn-off of currents through semiconductor devices.

There is a certain issue regarding the time it takes to perform a switching, though for the MOSFETs considered in this thesis with a switching time of approximately 50ns, this is not the greatest source of power loss. A much greater issue at turn off comes from a phenomenon called voltage ringing. This effect is shown in Figure 2.9 and is cause by current, going through an inductance, being forced to change almost momentarily by a semiconductor device. Basically the voltage oscillates between the leakage inductance and the leakage capacitance of the circuit.

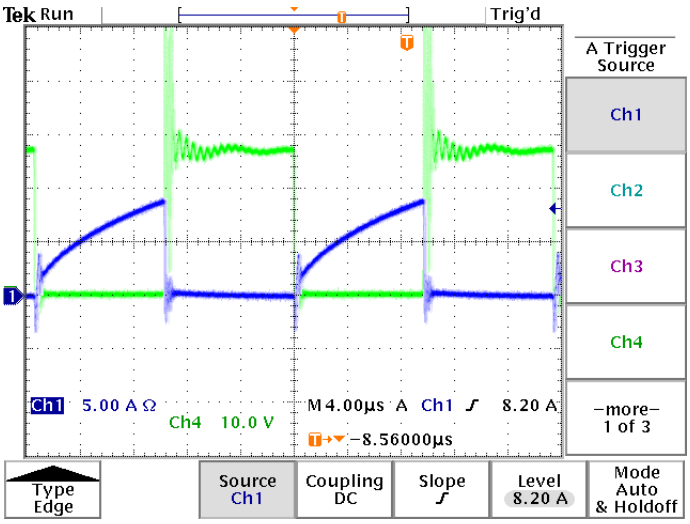


Figure 2.9: Oscilloscope plot of the drain-source voltage (green) and the drain current (blue) of a primary side inverter MOSFET. As seen in the picture, when the current is turned off and the voltage rises, the voltage continues far beyond the off-state value only to later on be slowly damped over time.

Two common methods of dealing with this is to either provide an alternate path for the current to go and thus not interupt it instantaneously or to more directly reduce the $\delta I/\delta t$ by the use of snubbers. Also here, there are many complex alternatives but the most common snubber is the RC snubber in which a resistor and a capacitor is put in parallel with the device being protected.

To further simplify the situation an even simpler, purely resistive snubber can be used to explain the situation and derive a solution.

Breaking down the situation of the semiconductor device during turn-off, the equivalent simplified resonant tank described in Figure 2.10 can be used to illustrate the ringing effect, where the charge up of the capacitance induces a current in the inductance, which in turn discharges the capacitor and so on.

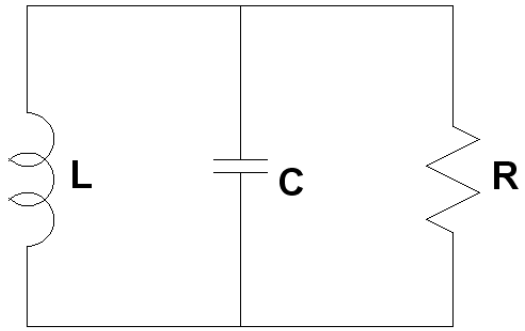


Figure 2.10: Very simple resonant tank depicting the equivalent situation of the drain-source of the semi conductor device at turn-off.

With simple voltage division, a transfer function from input to output can be found as in (Hagerman 1995):

$$H(s) = \frac{\left(\frac{R_s \cdot \frac{1}{sC}}{R_s + \frac{1}{sC}}\right)}{\left(\frac{R_s \cdot \frac{1}{sC}}{R_s + \frac{1}{sC}}\right) + sL} = \frac{\left(\frac{1}{LC}\right)}{s^2 + s\left(\frac{1}{R_s C}\right) + \left(\frac{1}{LC}\right)} \tag{2.4}$$

Where in the general second order response

$$2\zeta\omega_n = \frac{1}{R_s C}$$

and

$$\omega_n^2 = \frac{1}{LC}$$

with ω_n being the natural oscillation frequency of the circuit in radians and ζ being the damping coefficient. Thus the transfer function can be put in the general form

$$T(s) = \frac{\omega_n^2}{s^2 + s(2\zeta\omega_n) + \omega_n^2} \tag{2.5}$$

.

Finally the value of the snubber can be solved as

$$\boxed{R_s = \frac{1}{2\zeta\omega_n C} = \left(\frac{1}{2\zeta}\right)\sqrt{\frac{L}{C}}} \tag{2.6}$$

In Figure 2.11 the response is shown for different values of the damping coefficient. The goal is to use enough damping to get the oscillations down, but not too much, since excessive damping leads to unnecessary resistive loss. A common approach is to choose a damping coefficient of 0.5 resulting in

$$R_s = \sqrt{\frac{L}{C}}$$

or as it is commonly referred to, the characteristic impedance of the circuit.

Regarding the shape of the waveform this snubber would do a very effective job, however the power dissipation of this snubber would be very high. Here the second part of the snubber design takes in. After choosing a desired value of R_s to achieve the desired ζ a capacitor is connected in series with it to greatly increase the DC-resistance of the snubber.

Replacing R_s in equation 2.4 with $\left(R_s + \frac{1}{sC_s}\right)$ the -3dB cutoff frequency is found and given by

$$f_o = \frac{1}{2\pi R_s C_s}$$

To make sure the cut off frequency really passes through the snubber effortlessly a slightly lower frequency should be designed for, in order to achieve the damping desired. By choosing to design for a factor 2π lower frequency the capacitor value is given by

$$\boxed{C_s \approx \frac{1}{R_s f_{ringing}}} \tag{2.7}$$

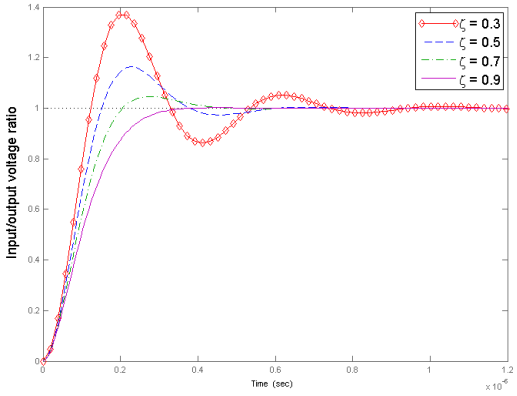


Figure 2.11: Step response of a general second order transfer function at different dampening coefficients ζ. At ζ=0.5 a good degree of dampening occurs without decreasing the speed of the system very much.

2.5 MOSFET theory

The metal-oxide-semiconductor field effect transistor (MOSFET) is a gate charge controlled transistor (Undeland 2003). It requires a positive gate-source voltage in order to charge up the gate to turn it on. It then creates a channel between its drain and source which can conduct current in either direction, depending on the drain-source voltage polarity. Since the MOSFET is a charge controlled device it is easy to control the speed at which it switches by adding gate driving circuits to control the current that flows into and out of the gate. It also has a relatively high possible switching speed, making it the preferred choice of transistor in many high frequency applications.

The MOSFET transistor has a positive temperature coefficient which means that several units can be placed in parallel and thus decrease the total drain-source resistance $R_{ds,on}$. When one unit is conducting more current than the others, its temperature increases and thereby also the channel resistance, thus making the current divide it self evenly among the transistors. However, with increased voltage blocking capabilities of the MOSFET, the conduction channel has to be longer, thus increasing its resistance (due to increased drain/drift region thickness). Therefore it is often considered less suitable for high voltage applications, than other alternatives, such as IGBTs.

2.5.1 MOSFET intrinsic body diode

One important parasitic component in a MOSFET transistor is the BJT that emerges across the drain and source contacts. With the body, drain and source of the MOSFET serving as base, collector and emitter respectively, the BJT might turn on if the voltage across the body and source is high enough. Since this will destroy the device, the source and body are connected together as a protection. As a result, there is instead an intrinsic diode formed inside the body-drain p-n junction of the MOSFET.

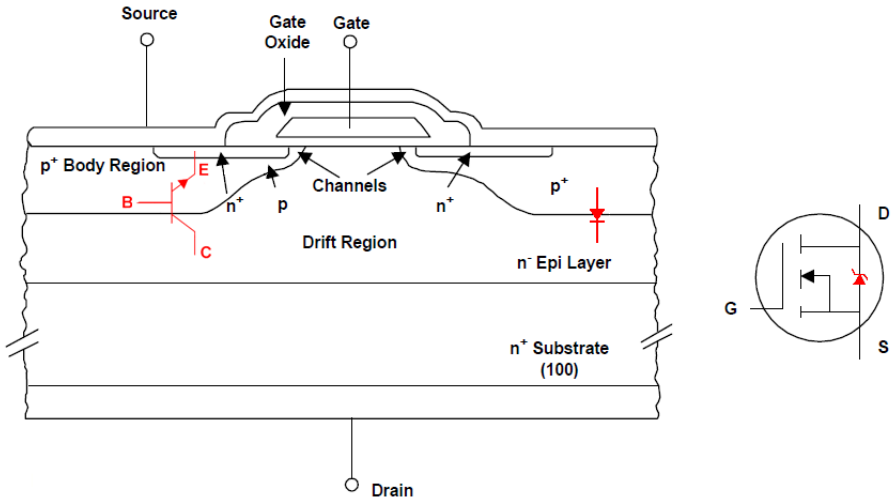


Figure 2.12: Schematic picture of a MOSFET transistor.

The diode can be observed in Figure 2.12 where it is connected between the drain and source, (in red) making it useful as a freewheeling diode in half- and full-bridge converters. On the left side of Figure 2.12, the possible BJT transistor formed across the drain and source contacts is shown in red.

2.5.2 MOSFET switching characteristic

The switching characteristics of a MOSFET transistor can be explained in four steps where each step relates to a certain time interval of the total switch-on/off time. Starting with the turn-on sequence, the graphs in Figure 2.13 are theoretical representations of the gate current i_G, gate-source voltage V_{GS}, drain-source voltage V_{DS} and drain current i_D, in these time intervals.

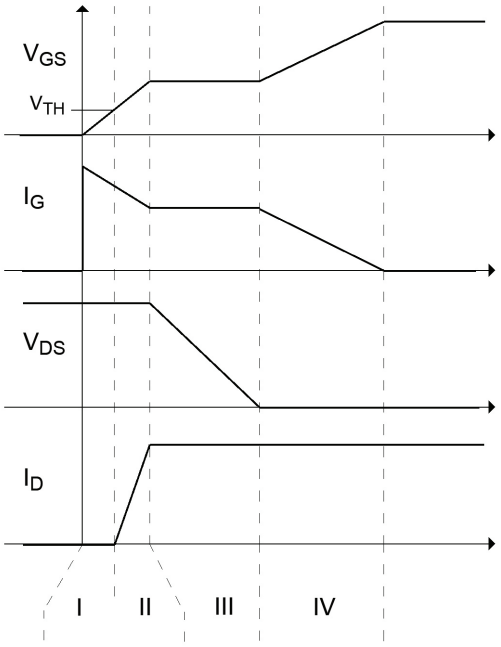
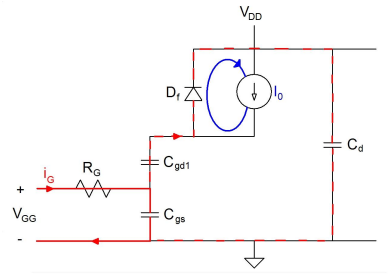
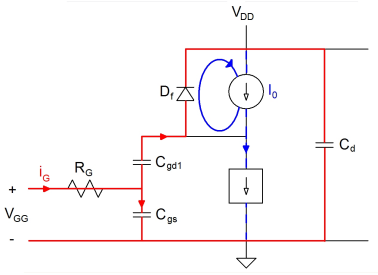


Figure 2.13: Switching waveforms of a MOSFET transistor during an ideal turn-on.

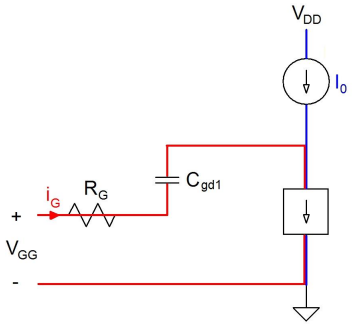
The transistor can be modeled with equivalent circuits, which correspond to each interval, as shown in Figure 2.14. The current source with the parallel diode is the model of an inductive load and R_g is an external gate resistance. The four steps during the turn-on are described below:



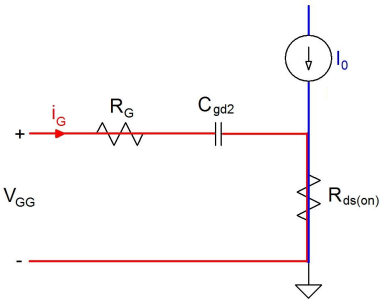
(a) Equivalent model of the MOSFET transistor during time interval 1. The time interval corresponds to the time it takes to charge the gate up to the threshold gate-source voltage.



(b) Equivalent model of the MOSFET transistor during time interval 2. This interval is the interval during which the drain current rises from zero to the load the full load current.



(c) Equivalent model of the MOSFET transistor during time interval 3. The interval during which the drain-source voltage falls to zero after the drain current has turned fully on.



(d) Equivalent model of the MOSFET transistor during time interval 4. This interval corresponds to the time where the conduction channel further enhances to reduce the resistance. Parallel to this, the gate gate-source voltage rises to the full gate-source voltage of the gate drive circuit.

Figure 2.14: Equivalent models of the MOSFET during the different stages of its turn-on process.

1. The first interval (2.14a) is called the turn-on delay. The name is given due to that both V_{DS} and i_D, are remaining unchanged. During this stage i_G is primarily charging the gate-source capacitance C_{gs}, but there is also a small current flowing into the gate-drain capacitance C_{gd}, (also called the miller capacitance). V_{GS} now appears to increase linearly from zero to $V_{GS(th)}$, although it is in reality a part of an exponential curve with time constant $\tau_1 = R_G(C_{gd1} + C_{gs})$.

2. In the next interval (2.14b) i_G continues to charge C_{gd} and C_{gs}, causing V_{GS} to increase above $V_{GS(th)}$. At the same time, i_D has started to increase and is doing so linearly with V_{GS}. V_{DS} remains constant until the current i_D consist of the whole load current I_0. When this occurs, the free wheeling diode D_f is no longer forward biased, thus not conducting, and V_{DS} starts to decrease.

3. During the third interval (2.14c) V_{GS} is clamped to V_{GS,I_0}.The resulting plateau is characterized as the "Miller plateau". With the drain current i_D now being equal to I_0 and the MOSFET operating in the active region, the gate current can do nothing other than discharging C_{gd} and thus decrease V_{GD}. As a result, V_{DS} will eventually drop to zero, as V_{DS} is the sum of V_{GS} and V_{GD}.

4. When both capacitances C_{gs} and C_{gd} are fully charged (2.14d), V_{GS} will grow exponentially, with time constant $\tau_2 = R_g(C_{gd2} + C_{gs})$, until it reaches the supplied gate voltage V_{GG}.

A similar analytical approach which was used above for finding the turn-on switching waveforms can be used when finding the turn-off waveforms. The sequence in this case is the inverse of the stages during turn-on. However, the times during each interval may be different since the applied gate voltage at turn-off can sometimes be set to minus V_{GG} instead of zero. This is done in an effort to speed up the turn-off and is the case used for this thesis.

2.5.3 MOSFET power losses

With the use of MOSFETs there are two different kinds of transistor power losses to consider. Switching losses and conduction losses. These are illustrated in Figure 2.15, where the switching losses are split in two parts, turn-on losses and turn-off losses. Due to the switching characteristics described in the previous subsection, without external influence, the drain current will rise before the drain-source voltage drops and vice versa, leading to both current through and voltage over the drain source channel being present at the same time, at every turn-on and turn-off occasion.

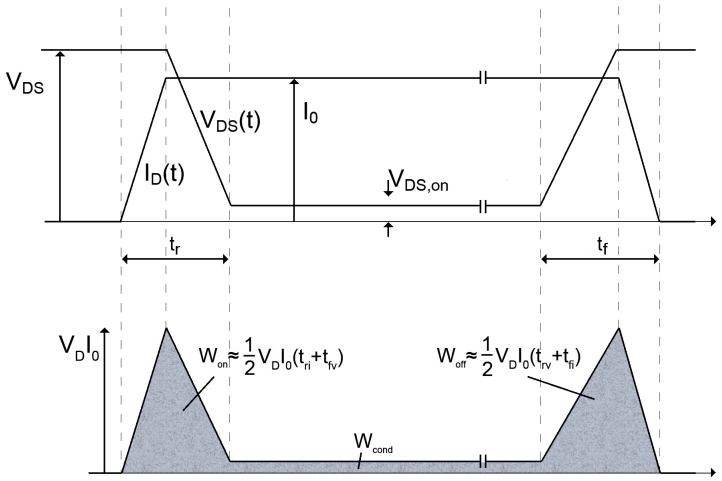


Figure 2.15: Picture illustrating the source of switching - and conduction losses.

$$P_{turn-on} = \frac{I_d \cdot V_d \cdot t_r}{2} \cdot f_{sw} \tag{2.8}$$

$$P_{turn-off} = \frac{I_d \cdot V_d \cdot t_f}{2} \cdot f_{sw} \tag{2.9}$$

$$R_{DSon} = \frac{V_{DSon}}{I_d}$$

$$P_{conduction} \approx \left(T_{sw} - t_r - t_f\right) \cdot D \cdot I^2 R_{DSon} \tag{2.10}$$

Where I_d is the drain current, V_d is the DC-supply voltage, t_r is the rise time, t_f is the fall time, f_{sw} is the switching frequency, T_{sw} is the switching period, D is the duty cycle and R_{DSon} is the on-state resistance of the full-bridge MOSFETs. The turn-on and turn-off power losses can be found with 2.8 and 2.9. As for the conduction loss; This is a simple resistive loss, caused by the drain current flowing through the n-channel of the MOSFET which has a certain resistance at a given load situation.

3 Measurements and calculations

In the first part of the thesis upto the point where the second rectifier is applied (the center-tap 2-diode rectifier bridge) the measurement euipment used is presented in Measurement setup 1:

- TDS220 - Oscilloscope, 2 channel digital
- Tektronix TCP202 - DC to 50MHz current probe
- Tektronix 1103 TekProbe Power Supply - Power supply for current probes when used together with TDS220 (to prevent saturation of probe at DC-currents)
- Oltronix B40-1 - DC Power supply
- 2 x Isolation transformer

The connection setup is presented in Figure 3.1.

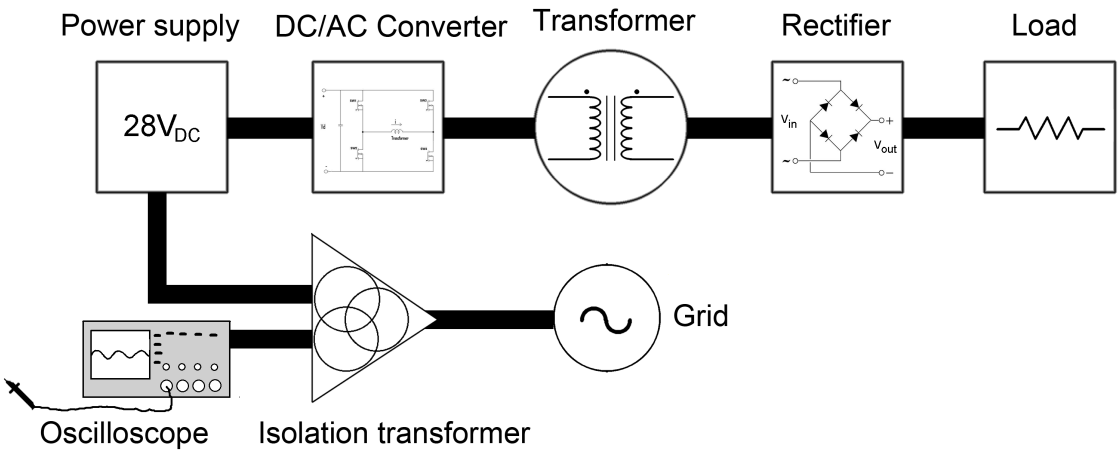


Figure 3.1: Blockdiagram of measurement setup, for the whole converter.

As can be seen in the picture, both the oscilloscope and the power supply is connected to the grid via isolation transformers. This is done to solve issues with circulating ground signals (primarily 50Hz noise) and common mode disturbances, by providing separate ground potentials.

After the point where the inverter has stopped being considered, the equipment used is presented in Measurement setup 2:

- TDS 3014B - Oscilloscope, 4channel digital
- Tektronix TCP202 - DC to 50MHz current probe
- Delta electronica SM7020-D - DC - Power supply
- 2 x Isolation transformer

In Figure 3.2 the actual connection set-up is shown.

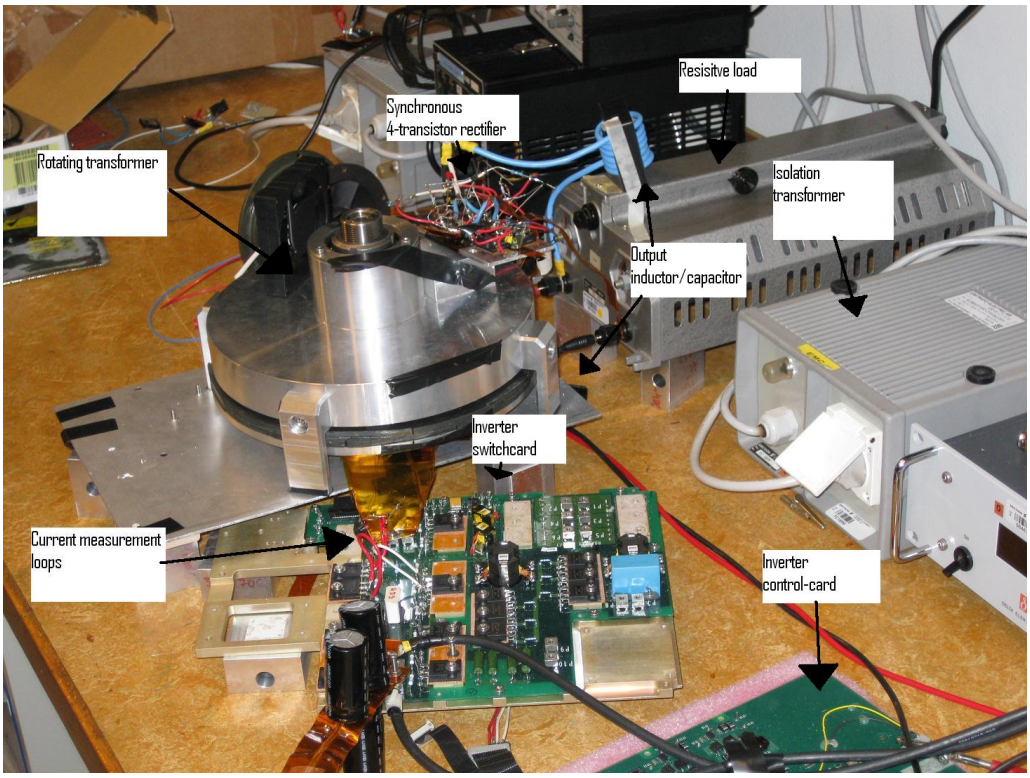


Figure 3.2: Photograph of the actual converter.

3.1 Measured duty cycle loss

There are many sources of duty cycle loss in this circuit, but the single greatest one is the one caused by the commutation time, due to the circuit inductance. When a reverse voltage is applied at the output of the full bridge the current takes some time to change in the full circuit. This phenomenon is shown in Figure 3.3.

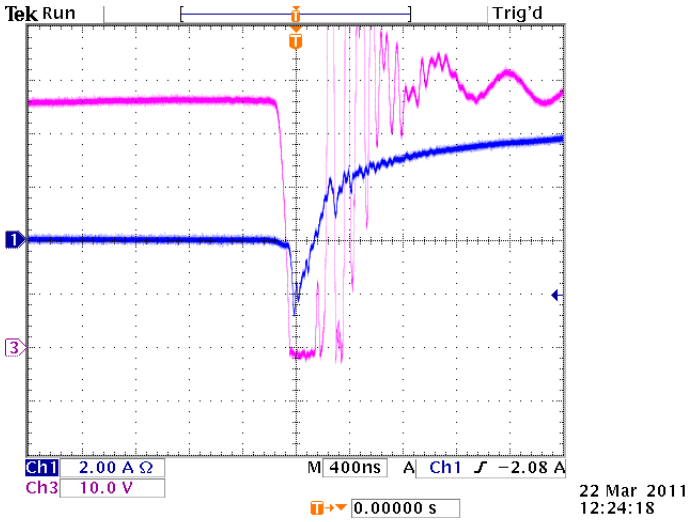


Figure 3.3: Ch1 (Blue) is here the drain current of one of 4 parallel MOSFETs, i.e. a forth of the total primary side drain current. Ch3 (purple) is the output of the full wave diode rectifier. While the current rises linearly (due to the inductance) the output experiences a voltage dead time. With the full current of 18A applied here, the dead time, caused by the circuit inductance is approximately 300ns (compared to the 50ns switching time, this is a lot).

With the current, voltage and time known, the inductance can be found with the relation :

$$L = \frac{U}{\Delta i / \Delta t} \tag{3.1}$$

At the input of the rectifier, during the current reversal, the voltage is now zero, since the full applied voltage will be over the inductance, as seen in Figure 3.3. The negative effect of the leakage inductance mentioned, brings a huge flaw in the design since if the voltage is zero for a significant amount of time, the effective duty cycle will be reduced and so will the output voltage. Therefore, with a transformer ratio of 1:2, it is of great importance to achieve a duty cycle as close to 100% as possible to achieve a doubled output voltage. The factors that can at this moment be optimized to decrease this phenomenon's effect on the effective duty cycle are the leakage inductance and the switching frequency. Other causes of duty cycle loss for this converter include the switching times of semiconductor devices and gate driving errors.

3.1.1 Influence on the total leakage inductance caused by conductors

During the earlier design stages of the complete DC/DC converter system (including full bridge, transformer with a single secondary winding and a diode bridge rectifier), a pair of 50cm twisted wires were used for connecting the full bridge and the rectifier with the transformer. At an input voltage and current of the DC/DC converter equal to 28V and 20A, the rectifier output voltage were measured and its waveform showing the dead time is shown in Figure 3.4a. It can be seen that the dead time during zero voltage is approximately $1\mu s$.

The relation between dead time and effective duty cycle is given by:

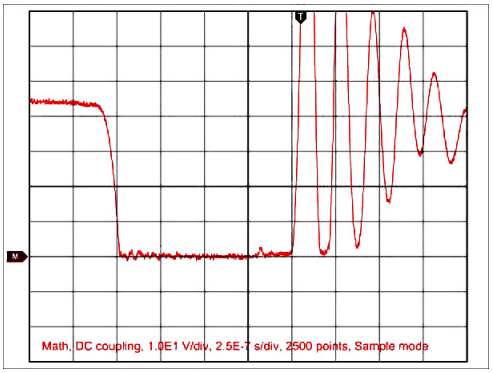
$$Duty - cycle_{effective} \approx \frac{T_s/2 - T_{dead-time}}{T_s/2} \tag{3.2}$$

where $T_{dead-time}$ is the length of the dead time for each switching occasion, which happens once every half switching period $(T_s/2)$.

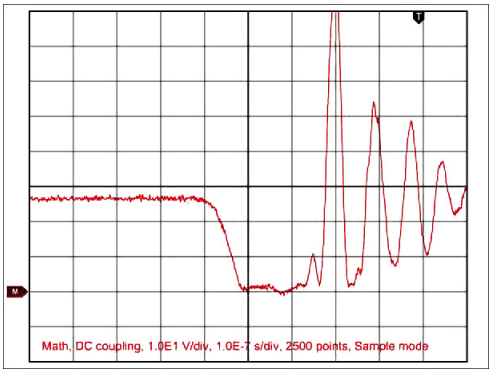
Ignoring the rest of the dead time, originating from semi conductor devices switching time etc, $1\mu s$ of dead time translates, at a frequency of 55kHz, to an effective duty cycle of 89%.

To illustrate the effect of the conductors, the transformer was disconnected and one of the old wires were used to connect the inverter and rectifier directly. The resulting dead time is shown in Figure 3.4b. The resulting dead time was 180ns translating to an effective duty cycle of approximately 98% (once again ignoring all duty cycle related effects not related to the inductance of the circuit). The next thing to try was to replace the 50cm twisted wires with 10cm wires, twisted as tightly as possible. The result is shown in Figure 3.4c, where the dead time is now reduced to 120ns.

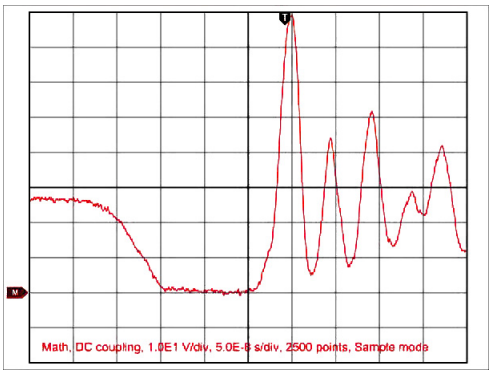
To lower the inductance of the conductors, which was currently unacceptably high, the wires were replaced by flat copper bands. These bands were mounted tightly on top of each other and shortened to the minimum possible length physically possible. Figure 3.4d shows the result, at an input voltage of 28V and an input current of 10A with all conductors and transformers once again connected. Total dead time at this power level is now 100ns and the effective duty cycle loss = 1.1%.



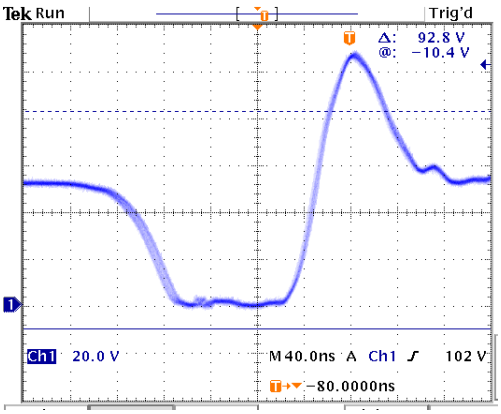
(a) Rectifier output at 28V, 20A. Inverter and rectifier is connected to the transformer with 50cm, twisted wire conductors.



(b) Rectifier output at 28V, 20A. Inverter and rectifier is connected directly (no transformer) with a 50cm, twisted wire conductor.



(c) Rectifier output at 28V, 20A. Inverter and rectifier is connected directly (no transformer) with a 10cm, twisted wire conductor.



(d) Rectifier output at 28V, 10A. Inverter and rectifier is connected with transformer with short tightly paralleled, flat aluminum bands.

Figure 3.4: Rectifier outputs with different conductors between inverter and rectifier.

The relations might not be obvious since different power levels had to be used for various equipment related reasons, but transforming the values into inductances put them all in the same scale.

Using the relation in (3.4) the final leakage inductance can be calculated to approximately 140nH, while the original one is 700nH, with the difference being introduced by the change of conductors.

$$T_{dead-time} = {}^{L \cdot 2 \cdot I_{in}}/_{V_{in}} \tag{3.3}$$

Using relation (3.3) and (3.2), the resulting effective duty cycle is found to be 97.8%. Once again this is only valid assuming the switching times of semi conductor devices and other time factors are negligible in comparison with the commutation time, which they after these improvements, are not.

Another factor worth mentioning is that the new conductors also lead to a situation where the outer circuit is not affected much by the setup used, i.e. the circuit inductance is the same no matter how the converter is twisted and pulled.

3.1.2 Synchronous rectification and effective duty cycle

When using the synchronous method of rectification the most important factor to set, in order to keep up the effective duty cycle, is found in the gate driving circuit. The dead time due to circuit inductance is the same as before, but now there is also a risk of dead time induced by faulty gate driving.

Without gate control the gate voltage and current will become much to high and simply short circuit and most likely break the MOSFETs. To keep this in check a gate driver needs to be implemented. The scope of this driver is to make sure, enough charge is delivered to the gate as fast as the MOSFET switching time allows, but not faster.

Due to low gate current, one transistor might turn on, "long" before the other one turns off, resulting in a short circuit loop for a short time. This can be seen as the spikes in the drain current of Figure 3.5 and is often referred to as cross conduction. With a perfect gate driver and appropriate delay times the spikes seen in Figure 3.5 will not be visible at all.

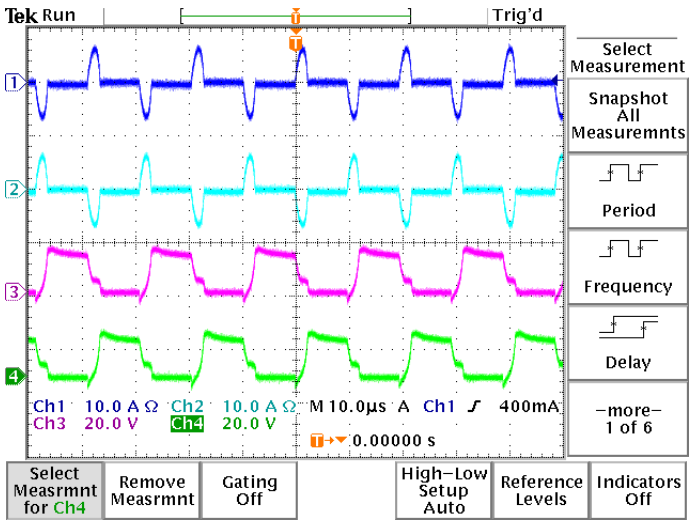


Figure 3.5: Channel 1(Dark blue) drain current transistor 1, Channel 2 (Light blue) drain current transistor 2, Channel 3 (purple) V_{gs} transistor 1, Channel 4 (green) V_{gs} transistor 2

Achieving a perfectly synchronized switching without adding unwanted delay is not an easy task but was improved greatly by the gate drives described in later section 3.4.4.

3.2 Full bridge inverter losses

Due to certain initial constraints on easily available lab equipment, the initial power loss measurements and calculations are performed at a load level corresponding to 28V and 6A input. A fairly substantial degree of linearity is assumed at this point, which gives an adequate approximation of reality. The only source of power loss considered in the inverter, is the one located in the MOSFET transistors. There is also resistive loss in the conduction paths on the circuit board, but these are negligible in comparison. In this section, the MOSFETs originally used in the inverter worked with, IRFP460LC, are compared with another choice of MOSFETs, IRFP044NPbF, that according to theory should work a lot better. The performance of these new transistors is evaluated and put into context. The major difference between these two models of MOSFET transistors is the on-state resistance. The old transistors have a resistance of 0,27Ω, while the new ones only have one of 21mΩ. Important to notice regarding the resistance of the MOSFETs, is that the old one were paralleled four and four while the new ones were used two and two, resulting in $0,27\Omega/4$ and $21m\Omega/2$ respectively.

3.2.1 Original full bridge inverter - Old MOSFETs

The first thing to measure is the switching losses of the old transistors. This was as mentioned performed at an input voltage of 28V and an input current of 6A, resulting in the losses presented in Table 3.1.

Table 3.1: Calculated theoretical and measured actual switching losses of the original full bridge, at 28V and 6A input. Three different switching frequencies are tested: 55kHz, 121kHz and 173kHz. Using a single secondary winding on the transformer (i.e. 2:4 turns ratio)

Calculated	Turn-on losses[W]	Turn-off losses[W]	Switching losses[W]	Perc. of P_{in}
55 kHz	1.66	1.55	3.22	1.92 %
121 kHz	3.66	3.42	7.07	4.21 %
173 kHz	5.23	4.88	10.11	6.02 %
Measured				
55 kHz	≈0	1.56	1.56	0.93 %
121 kHz	≈0	3.19	3.19	1.9 %
173 kHz	≈0	4.41	4.41	2.63 %

When the actual measurements are performed it appears that the great commutation time, due the inductance in the circuit, is greater than the turn-on time as can be seen in Figure 3.6.

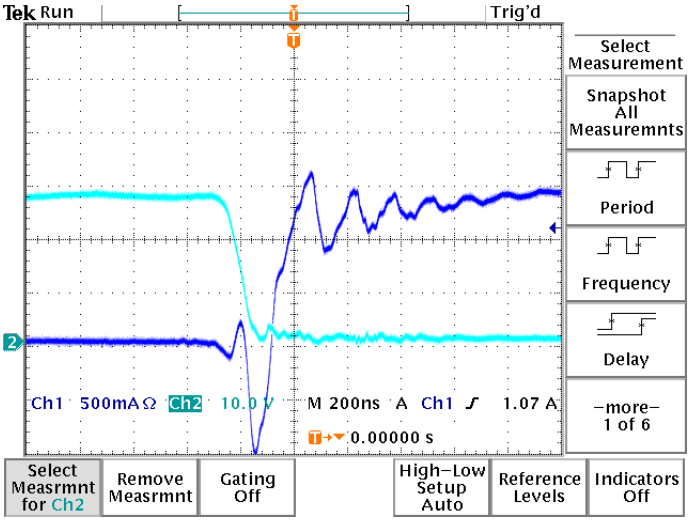


Figure 3.6: Drain current (dark blue) and drain-source voltage (light blue) during a turn-on occasion for one of the MOSFETs in the inverter. The voltage reaches zero before the current goes starts to increase (approximately)

The normal assumption when calculating turn-on losses is that the current goes up at the same time as the voltage goes down, but as can be seen, the voltage goes down to $V_{DS(on)}$ long before the current reaches its high value. In effect, soft turn-on switching is applied. In this situation, a fairly high amount of current is to be conducted, resulting in a great dependence on the circuit inductance, which in turn is tricky to keep constant from setup to setup.

Another factor affecting the turn-off losses is the derivative of the drain current during the on-state. At 55kHz the current varies with 2A over the on-state period in the case without the center-tap (2:4 winding ratio). This in effect means that the current at the moment of turn-off is higher than the average current and lower than the average at turn-on. Fortunately this is an absolute effect, and not a proportional one, so that at higher load currents this effect has a smaller impact on the turn-off losses.

The other loss to consider is the on-state conduction losses. These were measured at the same voltage and current levels as the switching losses and presented in Table 3.2.

Table 3.2: Calculated theoretical and measured actual conduction losses of the original full bridge, at 28V and 6A. The measured values illustrates the point, but are due to measuring errors at the time of the measuring not possible to use as a verification.

Calculated	Conduction loss [W]	Percentage of input power
55 kHz	4.46	2.65 %
121 kHz	4.41	2.63 %
173 kHz	4.36	2.60 %
Measured		
55 kHz	8.32	4.95 %
121 kHz	8.23	4.90 %
173 kHz	8.15	4.85 %

At the time these measurements were performed, measurement errors due to the very big ratio between high and low values in an oscilloscope were not yet known. This ratio leads to saturation in a part of the amplifier within the oscilloscope when trying to zoom in, in a way resulting in a big part of the waveform being outside the screen, (Calmels 2004). After the measurement error was discovered, the voltage clamp described in Figure 3.7 was used to get a more accurate value of $V_{ds,on}$. Fortunately the error is a proportional one and therefore by comparing the values attained before the use of the voltage clamp and the ones after for the new MOSFETs, the measurement error of the on-state voltages of the old MOSFETs is found to be approximately 40%. As a result, the conduction losses measured are a factor $(1,4)^2$ larger than they ought to be.

3.2.2 Improved full bridge inverter - New MOSFETs

In Table 3.3 the theoretical switching losses for the new MOSFETs are shown. Assuming a case with an unchanged external circuit inductance the turn-on losses will in reality still be very low (more or less zero) with the use of the new MOSFETs.

Table 3.3: Calculated and measured switching losses, using the new 55V MOSFETs, at 28V and 6A. The transformer winding configuration used here is the case with a single secondary winding.

Calculated	Turn-on losses[W]	Turn-off losses[W]	Switching losses[W]	Perc. of P_{in}
55 kHz	1.48	0.96	2.44	1.45%
121 kHz	3.25	2.11	5.37	3.20%
173 kHz	4.65	3.02	7.67	4.57%
Measured				
55 kHz	0.0422	4.36	4.4022	2.62%
121 kHz	0.155	4.18	4.335	2.58%
173 kHz	0.22	3.6	3.82	2.27%

As the table shows, the values measured for the turn-off losses are not quite the same as the ones calculated. This is mainly due to two facts. First, the magnetizing inductance of the transformer affects the current derivative during the turn-on time, the same way as in section 3.2.1. Secondly it has to do with excessive overshoot of the voltage at the moment of turn-off. This is due to that the new transistors switch faster and thus allow a higher $\delta i/\delta t$ within the transistor. If disregarding all the overshoots and odd ringing, the switching times of the new transistors can still be found to be approximately 50ns at both turn-on and turn-off. As this is roughly the same as the old ones, the switching losses ought to be roughly the same as for the old ones as well.

At a later point the circuit was stable enough and the lab equipment required was available to measure the switching losses at a higher power level.

To find the overall loss in voltage as well as the conduction loss of the full bridge, the on-state voltage drop needed to be measured, which was done according to Figure 3.7.

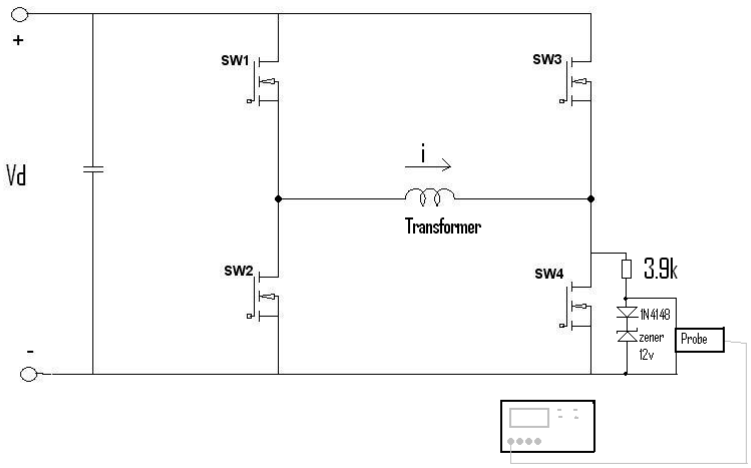


Figure 3.7: Connection used in order to measure the on-state voltage of SW4 with an acceptably small error.

In order to get realistic and accurate results, a voltage clamp is needed to keep the ratio between the on-state and the off-state voltage down. A simple voltage clamp, using a 12V zener diode, a 1N4148 diode and a $3.9k\Omega$ was used. The exact value of the resistance is not important, the only thing considered is that the current in the parallel path is kept negligibly low while the resistance is still kept well below the value of the non-conducting diodes (i.e. when the diodes are not conducting, more or less the whole voltage should be over the diodes). The resulting conduction losses measured with this setup, as well as the theoretical one calculated from the data sheet, are presented in Table 3.4.

Table 3.4: Calculated and measured conduction losses, using proposed choice of MOSFETs, at 28V and 6A.

Calculated	Cond. loss	Perc. of P_{in}
55 kHz	0.72 W	0.43 %
121 kHz	0.71 W	0.42 %
173 kHz	0.7 W	0.42 %
Measured		
55 kHz	$\approx$ 0.96W	0.57%
121 kHz	$\approx$ 0.96W	0.57%
173 kHz	$\approx$ 0.96W	0.57%

The low power parameters found for the new mosfets are not quite as good as the data sheets claim, however despite the difficulties in getting stable and nice waveforms, they still show an over all large difference from the old ones, as seen in Figure 3.8. In the graph of Figure 3.8, only the conduction losses are shown, however these are very important as they, unlike the linearly increasing switching losses, increases with the square of the current.

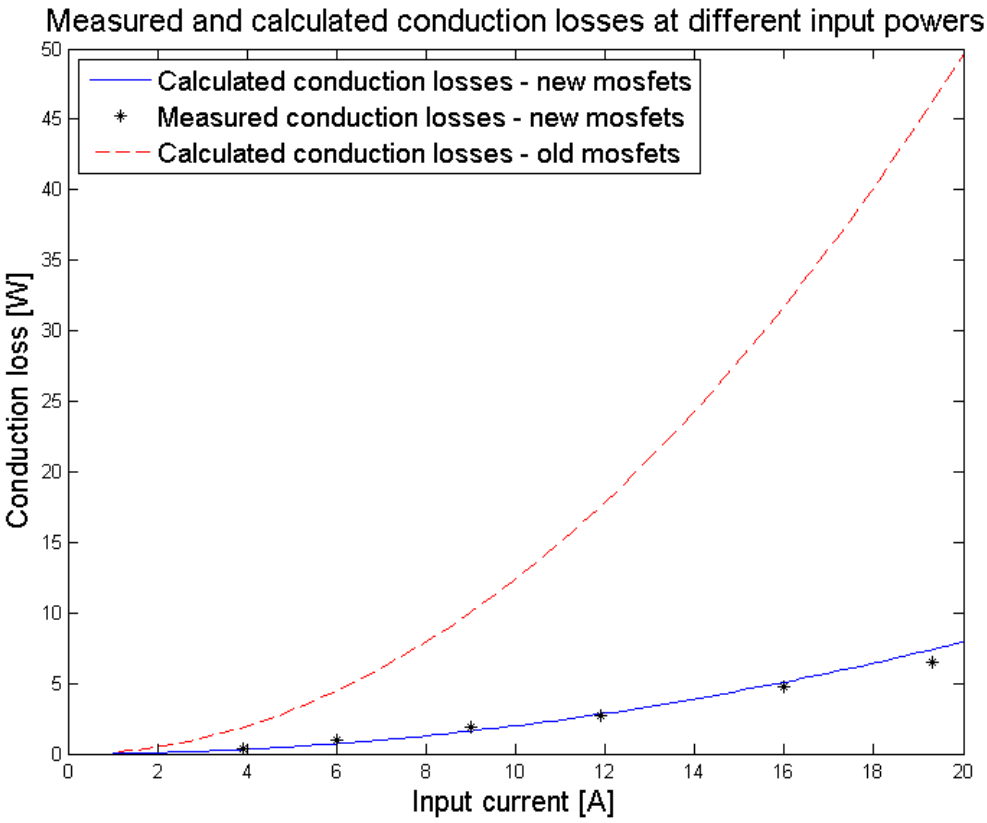


Figure 3.8: Conduction losses of the old and the new MOSFETs at different input powers.

Finally, with a stable rectifier, the losses of the inverter were measured again at a higher power level. At 55kHz, 27.9V input voltage and 16.1A input current, the final values presented in Table 3.5were acquired. As can be seen, at this higher power level the switching losses have leveled out to be approximately 1% just as for the old MOSFETs at the lower power level.

Table 3.5: Summarized final losses of the inverter, at an input power of 450W.

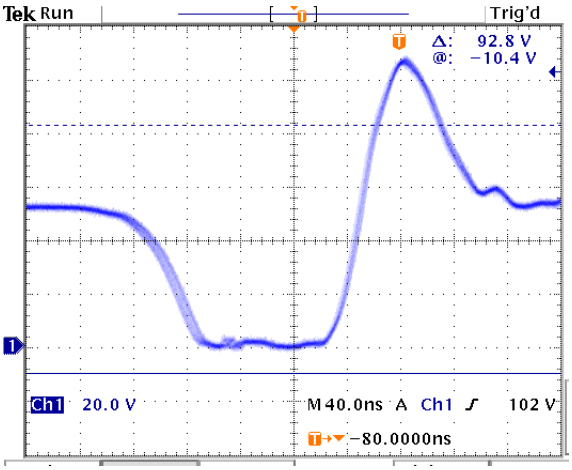
	Loss relative to input power (450W)
Switching loss [Percent of input power]	1.15 %
Conduction loss [Percent of input power]	2.18 %
$V_{ds,on}$ [V]	0.16 V

3.3 RotatingTransformer effects

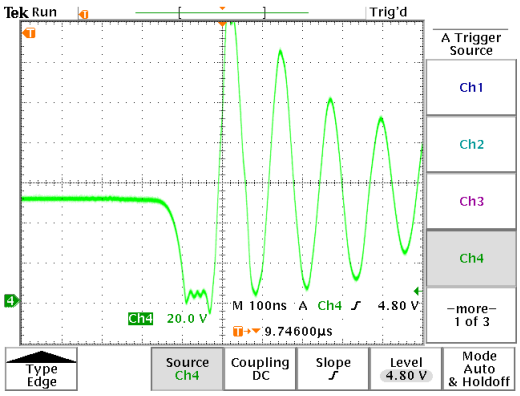
For the cases of synchronous rectification, without the center-tap, the total leakage inductance of the system before the output filter is found with the relation:

$$L_{leakage} = \frac{V_{in} \cdot T_{dead-time}}{2 \cdot I_{in}} \tag{3.4}$$

Here it is found to be approximately 140nH while in the case for the center-tap the total leakage inductance is approximately 66nH. This is found by looking at the time of zero voltage in Figure 3.9b and Figure 3.9a, in which the dead-time of the two different configurations, measured right before the output filter are shown.



(a) Single secondary winding. Output of the rectifier at one switching occasion at 28V and 10A input.



(b) Center-tap configuration. Output of the rectifier at one switching occasion at 28V and 20A input.

Figure 3.9: Dead-times found with and without the use of center-tap. The plots depict a switching occasion of the voltage over the rectifier output.

Looking back at the theoretical values of the leakage inductances found in Table 2.1 for the transformer, the leakage inductance for the case with the center-tap appears to be about 20nH larger than the theory. Considering that the theoretical values did not at all consider the differences between the cases, namely that with a center-tap configuration there will always be a more complicated connection (inductance wise), this is not very odd. In any case there is about twice as much leakage inductance with the single secondary winding case compared to the center-tap case, resulting in a longer dead time for each switching occasion.

As for the effect of the magnetizing inductance, a no load test reveals a magnetizing current of 1.1A and 0.1A for the center-tap configuration and the single secondary winding configuration respectively. At an input voltage of 27.9V this translates to a core loss of 30.7W with the center-tap and 2.8W with the single secondary winding. All the resulting measured transformer parameters are shown summarized in Table 3.6.

Table 3.6: Transformer parameters. One thing important to notice in this table is that the leakage inductance mentioned is not just the internal leakage inductance of the transformer, but the whole part of the circuit leakage inductance affected by the choice of transformer configuration.

	Center-tap	Single secondary winding
	1:2:2	2:4
Magnetizing current	$1.1A$	$0.1A$
Leakage inductance	$\approx 31.25nH + 20nH = 51.25nH$	$125nH$
Total circuit leakage inductance	66nH	140nH
Core loss	$30.7W$	$2.8W$

3.4 Rectifier voltage - and power loss

In chapter 2, the different rectifiers evaluated in this thesis are presented:

- Full wave diode rectifier - Single secondary transformer winding
- Full wave diode rectifier - Center-tap on secondary transformer winding
- Self-driven synchronous rectifier - Center-tap on secondary transformer winding
- Self-driven synchronous rectifier - Single secondary transformer winding

In this section, these are investigated with regards to voltage loss, power loss, effective duty cycle as well as complexity of components and control of components. This is performed in order to provide arguments for reasonable tradeoffs between different solutions. From this part and on, a switching frequency of 55kHz is used, since this currently is the only option that allows for decent duty cycles.

3.4.1 Measurements on the full wave diode rectifier - Single secondary winding

The single phase diode bridge was never meant to be the rectifier used in the end due to the relatively large voltage drop across the four diodes compared with transistors. However, it was a solution that was good enough at the starting point. Its main purpose was simply to rectify and provide the load a DC-voltage and complete the system to see if everything worked as intended. It also provided a first evaluation of the aspects of the rectifier needed to be worked with. For simplicity, the preferred diode package was TO-247 since it could easily be mounted into the already existing empty slots on the full bridge chassis that were used for cooling. This package can provide a low thermal resistance and with a cooling fan temperatures could be kept within normal operation limits.

The blocking voltage of the rectifier needed to be larger than the output voltage of the transformer but also with respect to the possible voltage ringing, that will occur due to the interaction of the circuits leakage inductance and the parasitic junction capacitance of the diodes.

The ultra fast switching diode, STTH6002CW, specified as suitable for switch mode power supplies, SMPS, and high frequency DC/DC-converters was chosen. It has a maximum RMS forward current of 50 A and a blocking voltage of 200V.

Measurements were made at Vin = 28V, an input current of 15 A and a switching frequency of 55kHz. The obtained waveforms of the diode output voltage (pink) and the output voltage after the output filter (green) are shown in Figure 3.10. It can be seen that the largest spike of the voltage ringing is slightly more than 140V. This unwanted ripple causes excessive power loss of the diode bridge and put high stress on the diodes.

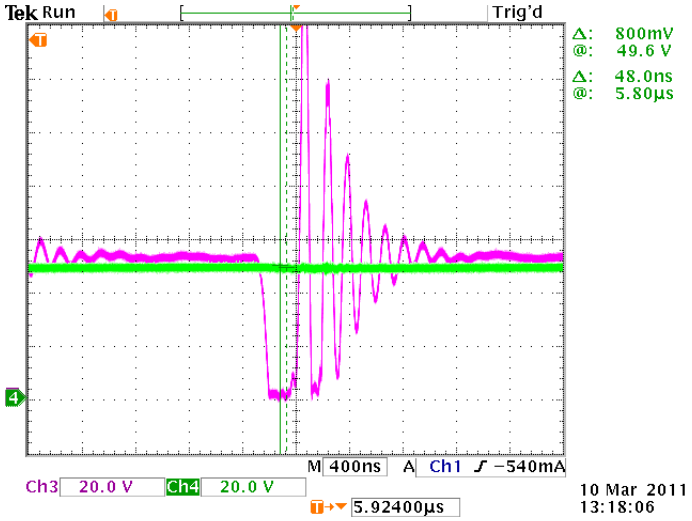


Figure 3.10: Picture of a switching occasion at the rectifier output. The purple channel is the pre-filter voltage and the green one is the resulting average output voltage.

The voltage drop across each diode was measured to 0.8V which leads to a total drop of 1.6V across the whole bridge. Due to the transformer design with a ratio of 1:2, this large drop is not acceptable if the aim is an output voltage twice that of the input.

3.4.2 Measurements on the full wave diode rectifier - Center-tap on secondary winding

For this rectifier setup, two diodes of the same type that was used in the previous rectifier were also used here. During all measurements, the wires had been replaced with flat aluminum bands connected between the full bridge converter, transformer and the rectifier. The wires were made as short as possible in order to minimize their inductance and the conductors were bundled as tightly as possible. The obtained values of the currents below were taken from the internal ampere meter of the power supply at 55kHz switching frequency and V_{in} and V_{out} were measured using the oscilloscope. With the load adjusted to give the input characteristic below:

$$U_{in} = 28V$$

$$I_{in} = 18A$$

$$P_{in} = 28V \cdot 18A = 504W$$

the output voltage was measured to 52.43V.

To find the efficiency, the output power needs to be known. As there at this moment were no accurate current probes easily available, the output power was instead found by measuring the DC-resistance of the load with a simple FLUKE multimeter. The load resistance at this power level was found to be approximately 6.75Ω, resulting in an output power of:

$$P_{out} = \frac{U_{out}^2}{R_{load}} = \frac{52.43^2}{6.75} = 407.25W$$

This results in a total efficiency of:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{407.25}{504} = 80.8\% \tag{3.5}$$

While there were losses all over the converter, extreme heat dissipation made it obvious without measurements that a great part of it came from the rectifier diodes. A lot of further work could be done with the voltage ringing and efficiency here, but a decision was made to start investigating synchronous rectification instead.

3.4.3 Measurements on the self-driven synchronous rectifier - center-tap on secondary transformer winding

The main aspect to look at when choosing a rectifier transistor is its on-state resistance, $R_{ds,on}$, since it will determine the size of the voltage drop across each unit when conducting. The transistors chosen for this rectifier are IRFP4227PbF which have an $R_{ds,on}$ of 21mΩ and a switching speed of approximately 30ns. They are capable of blocking voltages up to 200V and can conduct a maximum continuous drain current of 65A. The switching speed is not that important as long as it is higher than that of the primary side inverter switches, since these directly pull the secondary side's gate voltages.

In the center tapped synchronous rectifier, the voltage across each secondary winding is $V_{rectifier}$. If the setup in Figure 2.7 is used, the transistor gates must be able to withstand twice the output voltage of the transformer. In this case, at full voltage, there would be around 114V and therefore this setup is initially only tested at input voltages of up to 7V, resulting in a 28V gate-source voltage. To be able to pull the voltage up, a resistive/capacitive voltage divider as shown in Figure 3.11 was connected between the gate and source on each transistor.

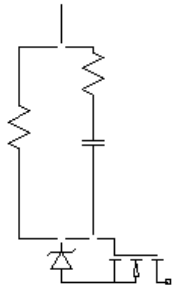


Figure 3.11: Voltage divider used in order to not expose the MOSFET gates to over voltages. The zener-diode clamps the voltage over the gate-source nodes to its maximum reverse voltage, in this case 12V.

At a drain current of 4A the resulting on-state voltage drop was measured to be approximately 80mV, verifying that this way of using the transistors instead of diodes, indeed works. When the function of the transistors was verified, it was concluded that the high core loss of the transformer (1.1A*27.9V) with the center-tap configuration was not worth the gain of using one less transistor and therefore the single secondary winding solution was carried on with.

3.4.4 Measurements on the self-driven synchronous rectifier - single secondary transformer winding

To achieve synchronous switching, without endangering the transistors, the transistor gates were driven in pairs using two pulse transformers, each having two secondary windings. The pulse transformers' primary windings were connected across one turn of the rotating transformer's secondary windings, hence a gate voltage of 56/4= 14V was attained, see Figure 3.12.

To provide the MOSFET gates with a controlled amount of current, a gate resistor, R_g, was connected in series with the input of the pulse transformer. According to the data sheet, at V_{gs} = 10V, a gate resistor of 2,5Ω was used to attain the switching times of approximately 30ns, associated with this transistor. However, due to the gate pulse voltage of 14V, a 40% larger resistor would in theory be necessary. The switching speed of the primary side inverter transistors is limited to approximately 50ns and since the pulse transformer is connected directly to the secondary side of the transformer, so are the rectifier transistors. Therefore, there is no need to use a smaller resistor than what would lead to a switching speed of 50ns. A gate resistor of 7,8Ohm resistor was chosen as an appropriate value.

The measured drain-source voltage of the transistors in the rectifier contained large amount of ripple, resulting in the need of a snubber in order to prevent damaging of the components. The snubbing procedure is described in section 3.5.

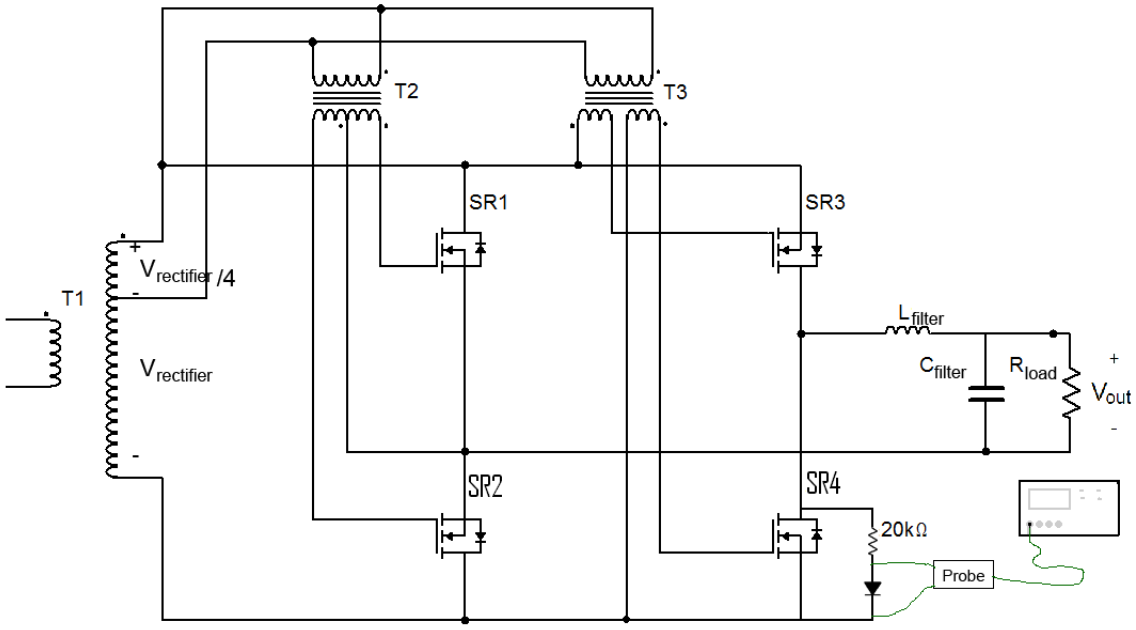


Figure 3.12: Connection used to acquire a voltage clamp for the off-state voltage level. When the drain-source voltage goes high, the probe sees only the forward voltage of the 1N4148 diode. T2 and T3 are the pulse transformers used to deliver gate pulses from the secondary winding of the transformer to the rectifier MOSFETs.

In order to get a more accurate measurement of $V_{ds,on}$ a voltage clamp similar to the one used on the inverter, was applied, according to Figure 3.12.

After snubbing the rectifier MOSFETs according to section 3.5, the final resulting voltage drops and power losses of the rectifier was measured, using the measuring procedures presented earlier (voltage clamps between the drain and source of transistors). These values are shown in Table 3.7.

Table 3.7: Rectifier losses, measured at 55kHz, 27,9V input voltage and 16,1A input current.

	Percentage of input power
Switching loss [Percent of input power]	0.55 %
Conduction loss [Percent of input power]	0.57 %
Loss in rectifier snubbers [Percent of input power]	0.21 %
$V_{ds,on}$ [V]	0.155 V

3.5 Snubber design

In section 2.4 the basic idea behind the snubber design is described. In reality measuring both the effective capacitance and the total leakage inductance of the circuit is often hard. In (Ridley 2005) a simpler approach is described in which the characteristic impedance is approximated with the use of the undampened ringing frequency and just one of these two parameters. At 450W the ringing frequency is directly measured over the drain to source voltage of the rectifier transistors to be 25MHz with the use of an oscilloscope. The leakage inductance was presented in Table 3.6 to be 140nH. With these values the snubber resistor can be calculated as:

$$R_s = Z_0 = 2 \cdot \pi \cdot f_{ringing} \cdot L = 2 \cdot \pi \cdot 16e6 \cdot 140e-9 = 14\Omega \tag{3.6}$$

when the snubber resistor value is known the next thing to calculate is the snubber capacitor.

$$C_s = \frac{1}{R_s \cdot f_{ringing}} = 4nF \tag{3.7}$$

However, using this snubber capacitor led to much more dampening than needed and greatly affected the system, making it much too slow and greatly reducing the efficiency. A compromise that worked well was to instead use a 100Ω resistor and with the same reasoning a resulting 0.7nF capacitance.

$$\boxed{R_s = 100\Omega}$$

$$\boxed{C_s = 0.7nF}$$

Important to note here is that this is not the ideal snubber, it is simply as mentioned, an acceptable compromise.

3.6 Output filter design

In order to aquire the desired output voltage a simple output filter was designed. A simple approach to this design procedure can be summarized with:

$$U_{inductor} = L_{inductor} \cdot \frac{\Delta i}{\Delta t} \Rightarrow L_{inductor} = U_{inductor} \cdot \frac{\Delta t}{\Delta i} \tag{3.8}$$

With some exaggeration the worst case scenario dead time can be approximated to 10%. With a desired average output voltage of 56V that means we have a peak voltage of $56/0.9 \approx 62V$ and a conduction time of approximately $9\mu s$ for each half period. The voltage $U_{inductor}$ in (3.8) refers to the voltage over the inductor, i.e. the difference between the output voltage of the rectifier and the average voltage. Looking at, for instance, the conducting part of the half periods, the interesting area, $U_{inductor} \cdot \Delta t$, becomes the area covered by the red grid in Figure 3.13.

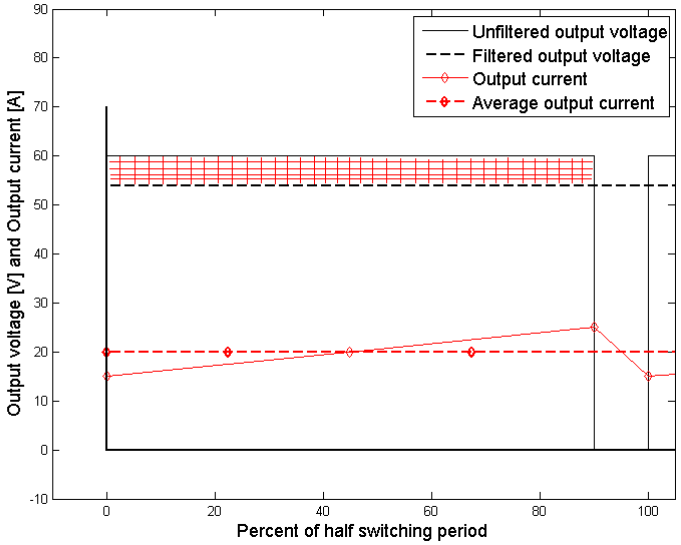


Figure 3.13: Schematic picture illustrating the output of the rectifier pre-filter, contra the average voltage output obtained after the filter.

Approximating the allowed current ripple through the inductor to 1A, for simplicity, leads via (3.8) to an inductance:

$$\boxed{L_{filter} = \frac{(62-56)V \cdot \frac{1}{110kHz} \cdot 0.9}{1A} = 49\mu H} \tag{3.9}$$

Looking at the current-waveform through the inductor, Figure 3.13, the charge needed to be absorbed and released by the output capacitor every half period can be found using simple relations. The charge consists of the difference between the actual current through the inductor and the output average current, which would ideally be fully DC.

$$Q_C = \frac{{}^{\Delta i}/_{2} \cdot {}^{T_{sw}}/_{(2\cdot 2)}}{2} = \frac{{}^{1A}/_{2} \cdot {}^{18.2\mu s}/_{4}}{2} = 1.14\mu As \tag{3.10}$$

Accepting a voltage ripple of 0.5V, the capacitance value can be found with the relation:

$$\boxed{C_{filter} = \frac{Q_C}{V_{ripple}} = \frac{1.14\mu As}{0.25V} = 4.56\mu F} \tag{3.11}$$

The -3dB cut-off frequency of this LC-filter becomes

$$f_{cut-off} = \frac{1}{(2\pi)\sqrt{L_{filter} \cdot C_{filter}}} \approx 10.7kHz$$

which is well below the 100kHz output of the rectifier considered.

After the desired values of the inductor and capacitor of the filter has been found, the design of the inductor begins.

Going one step further from the relation in (3.8) another known relation can be applied:

$$U_{inductor} = L_{inductor} \cdot \frac{\Delta i}{\Delta t} = \frac{\Delta B}{\Delta t} \cdot A_{Fe} \cdot N_{inductor} \tag{3.12}$$

where B is the magnetic flux density and A_{Fe} is the cross section area of the core

$$L_{inductor} = \frac{\hat{B} \cdot A_{Fe} \cdot N_{inductor}}{\hat{i}} \tag{3.13}$$

At the time this inductor was designed the peak of the current worked with was about 5A and the inductor was thus designed for that area in order to get started with the rectifier. The exact core used is unknown, as it is an old component being reused, however it is a ferrite E-core. To stay well below saturation levels of the ferrite core, a maximum magnetic flux density of 0.2T is assumed.

$$\boxed{N_{inductor} = \frac{L_{inductor} \cdot \hat{i}}{\hat{B} \cdot A_{Fe}} = \frac{49\mu H \cdot 5A}{0.2T \cdot 340\mu m^2} = 3.6 turns} \tag{3.14}$$

Since later on a greater current is desired, the number of turns are slightly exaggerated into the number of turns there happen to be room for, namely seven. An additional reason for this action is that filling the available area with extra turns makes acquiring a tight and well coupled winding easier. Finally to make sure the magnetic flux density within the core is kept down below saturation levels, an air gap is introduced.

Using the relation of (3.13) once again in combination with Ampere's law gives:

$$N\hat{i} = \hat{B}\left(\frac{l_{core}}{\mu_{core}} + \frac{l_g}{\mu_0}\right) \approx \hat{B}\frac{l_g}{\mu_0} \tag{3.15}$$

$$\hat{B} \approx \frac{N^2 \hat{i} \mu_0}{l_g} \tag{3.16}$$

$$\boxed{l_g \approx \frac{A_{Fe}\mu_0}{L_{inductor}/N^2} = \frac{340\mu m^2 \cdot 4\pi 10^{-7}}{49\mu H/7^2} \approx 0.4mm} \tag{3.17}$$

4 Conclusion

4.1 Results and discussion

4.1.1 Inverter

Measurements and simulations of the losses and performance of the simple full bridge inverter proposed in Chapter 2 verify that this topology is indeed adequate for the voltage - and power-interval considered. With the use of the two parallel IRFP044NPbF MOSFET transistors , the efficiency reaches 94.4% at 450W. The majority of the losses originates from the inverter and a possible source of concern is the conduction losses, which would increase exponentially in case of an increased power level, as seen in Figure 3.8. This could however easily be improved further with the use of either better transistors with a lower R_{DSon} or simply a greater number of parallel connected transistors. In Table 4.1 the different sources of loss in the converter are shown.

Table 4.1: Losses of the resulting converter at an input power of 450W.

Source of power loss	Losses [Percent of 450W input power]
Inverter conduction	1.15%
Inverter switching	2.18%
Transformer magnetization and resistive	≈0.97%
Rectifier conduction	0.55%
Rectifier switching	0.57%
Rectifier snubbers	0.21%
Complete DC/DC-converter	**5.63%**

As can be deduced from the table, the inverter conduction is the only major issue at this moment. If the input power was to be doubled, closing in on the 1000W load that was originally considered, the inverter conduction would be the single greatest source of power loss of the converter and would be in need of reduction. The switching losses are what they are and will not be affected by load level, since the switching loss relation is linear with current.

4.1.2 Transformer

For the sake of the rest of the converter the use of a center-tap configuration of the transformer windings would be ideal, however with the specific transformer worked with in this thesis, it is simply not viable, due to the low number of turns and thus low magnetization inductance. At 500W the different power losses of center-tap and single secondary winding configurations are approximately 30.7W and 2.8W respectively. In fact, the low magnetic inductance has a double negative impact on the converter since the inverter turn-off losses is the single greatest source of power loss in the system and this increases further with a lower magnetizing inductance and thus higher drain current at the moment of turn-off, although this is mostly an issue at low power levels. Apart from not being able to use the center-tap, the drawback of using the single secondary winding configuration is that it results in a higher leakage inductance, as well as the desired higher magnetic inductance. The resulting leakage inductance of the transformer comes to 125nH out of a total of 140nH for the entire converter.

4.1.3 Center-tap

To achieve a center-tap connection and a 1:2 ratio with the transformer with only 4 winding turns available on primary and secondary, a winding ratio of 1:2:2 must be used. Apart from performing its task of supplying two windings on the secondary side this also greatly affects the magnetizing inductance of the transformer. As mentioned in Section 2.2.2, the inductance is proportional to N_1^2. With a single secondary winding, a turns ratio of 2:4 can be used for the transformer. Due to this, the magnetizing inductance is reduced with a factor $2^2 = 4$. The effect of this is that the magnetizing current needed to magnetize, i.e. charge up the transformer is greatly increased. The resulting magnetizing current for the center-tap connection is approximately 1,1A. With an input voltage of 28V the power loss of the magnetizing comes up to an unacceptable level of 30,8W.

4.1.4 Rectifier

The most beneficial rectifier topology was found to be the four transistor self-driven synchronous rectifier shown in Figure 2.8, with the gate signals taken from the transformer secondary via small pulse transformers. With the switches consisting of two IRFP4227PBF MOSFETs in parallel, the rectifier losses could be kept at about 1% at an input power of 450W. With these transistors basically working as enhancement diodes, a non-negligible voltage ringing is introduced that needs to be snubbed, in order to protect the transistors as well as reduce losses. The snubbers used are designed to dampen no more than needed; keep the turn-off voltage peaks below 130V and introduces an extra loss of approximately 1W total in the rectifier. The maximum duty cycle achievable at 450W is 97% where 1% of the loss of duty cycle comes from the switching times of the rectifier transistors (and indirectly the switching times of the inverter transistors). At 28V and 15A input, this in combination with the various voltage drops within the circuit leads to an output voltage of 52.9V.

In Figure 4.1, a rough approximation of the input - and output- voltage relation is shown. The plot is derived from known voltage drops and causes of duty-cycle loss with a slight approximation regarding the input current, in order to find the duty-cycle for each condition. This approximation is that the input current is approximately 95% of the output current multiplied with two (from the transformer).

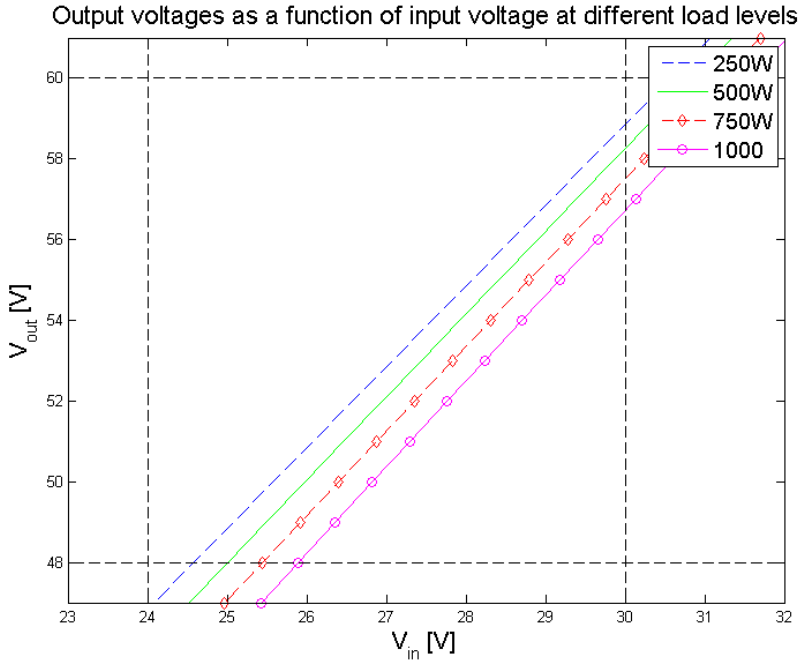


Figure 4.1: Graph of relation between input voltage and output voltage of the full converter. The previously determined acceptable voltage input (24-30 V) - and output (48-60 V)-levels are illustrated by the black dashed lines.

The way to interpret Figure 4.1 is that the point at which the plotted lines cross the vertical dashed lines sets the limit for which input voltages are acceptable in order to achieve an output voltage within the desired interval. From this plot, some application limitations can be found. The most interesting one is the fact that the interval of acceptable input voltage variations in order to get an output voltage within the accepted interval is moved to the right (higher values) with increased power level. This effectively sets a higher demand on the input voltage with increased load.

4.1.5 Influence on the leakage inductance caused by the switching frequency

Since the absolute dead time is unrelated to the frequency used for switching, the effective duty cycle would be less affected by this dead time, with a longer switching period. A lower switching frequency is therefore strongly preferred if the dead time is of considerable size. The lowest switching frequency possible with the inverter control used is 55kHz, which is therefore chosen.

The possible advantage of having a high switching frequency is the ease of canceling the output current ripple. Smaller filter can be used, hence the size and cost can be reduced. However, the loss of duty cycle due to a higher switching frequency is of far more concern in this design in order to achieve the desired output voltage.

4.2 Future work

- A factor of great importance for this converter is the air gap of the transformer. Due to certain imperfections in physical design of the current transformer the air gap can not be reduced below approximately 3mm without compromising the transformers ability to rotate without friction. If the iron parts of the transformer was further processed and greatly smoothed the air gap could theoretically be greatly reduced. If for instance the air gap could be reduced with a factor 4, the magnetizing inductance of the case with the center-tap would be approximately that of the current case without the center-tap. This could potentially allow for the use of the center-tap configuration, which would greatly reduce the leakage inductance and thus the dead-time associated with it as well as slightly reduce the power losses and voltage drops of the rectifier MOSFETs.
  - In the transformer today there is also a lot of unused space, which with a redesign could allow for more windings => more primary turns => more magnetizing inductance.
- Another partly mentioned point of interest could be the turns ratio of the transformer. The limitation is set so that the output voltage of the rectifier, pre-filter (excluding spikes) must not exceed 60V. With a maximum input voltage of around 28V this would allow for a turns ratio of up to 1:(2,14). With this ratio, voltages even slightly above 56V would be possible, which in turn would allow for an additional control feature. Since the dead time is a function of the input current, the phase shift control could be used in order to increased the dead time when the input current and thus the dead time decreases.
- Worth mentioning is also the fact that the inverter used in this thesis is originally designed to have phase shifting capability to allow resonant soft-switching. If a brand new inverter was designed, where this capability was not introduced, as would be the case for the current application, the inverter could be snubbed in order to lag the turn-off voltages and greatly reduce the turn-off losses.
- If implementing this converter in reality an active snubber that could handle dampening of the voltage without decreasing the speed characteristics of the converter too much would be a great improvement. This could possibly increase the efficiency by another percent, putting the switching losses of the inverter closer to that of the theoretical response, where overshoot was not considered.
- In the next version of the transformer; Optimize connections for the transformer windings. Currently the winding configuration is controlled by physical windings sticking out from the transformer, leading to extra stray inductance and degradation of the form factors affecting the leakage - and magnetic - inductance.

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