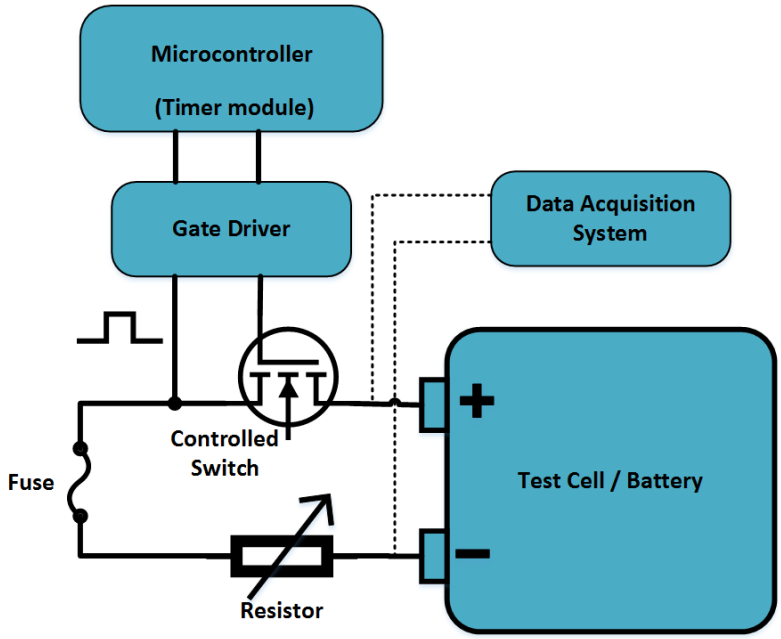
CHALMERS
UNIVERSITY OF TECHNOLOGY



Battery Modelling For Large Current Pulses

ENMX04 - Master Thesis in Energy and Environment

PremKumar *Ayyadurai*

Navya *Kundaranahalli Renukaiah*

Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2017

Master Thesis Report 2017

Battery Modelling for Large Current Pulses

PremKumar *Ayyadurai*

Navya *Kundaranahalli Renukaiah*

CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
Gothenburg, Sweden 2017

Battery modelling for large current pulses

PREMKUMAR *AYYADURAI*
NAVYA *KUNDARANAHALLI RENUKAIAH*

Supervisors : Torbjörn *Thiringer*, Chalmers
Johan *Lektenius*, Volvo Cars
Examiner : Torbjörn *Thiringer*, Electrical Engineering.

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover : Current pulse generation circuit
Typeset in LaTeX
Chalmers Bibliotek, Reproservice
Gothenburg, Sweden 2017

Battery modelling for large current pulses

PREMKUMAR *AYYADURAI*
NAVYA *KUNDARANAHALLI RENUKAIAH*
Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology

Abstract

Non-linearity due to high current pulses and frequency should be accounted for and included in the electrical equivalent circuit model of a battery cell; apart from its dependence on state of charge (SOC) and temperature. In order to obtain a large current pulse characterisation of a given cell, a current pulse testing circuit with both the high current and high frequency range capabilities is designed. The test circuit is built in a printed circuit board with the controlled switches and a provision to set the current pulse width using a microcontroller. The desired current magnitude is obtained by using a resistor designed from a copper sheet. Also, pretests are carried out on the given cell to determine state of charge (SOC) vs. open circuit voltage (OCV) characteristics at different temperatures. The cell is tested with the current pulses of different magnitude and time duration at a selected SOC level and temperature. Impedance behaviour over current magnitude and time duration respectively are deduced and mathematically fitted to the piecewise parameterised models. The obtained model parameters are in accordance with the Electrochemical Impedance Spectroscopy (EIS) results. Hence, the developed test circuit used for the battery modelling is validated.

Keywords: Test cell, State of charge (SOC), Electrochemical impedance spectroscopy (EIS), Large current pulse, Electrical equivalent model.

Acknowledgement

First and foremost, we would like to express our sincere gratitude to our supervisor and also examiner at Chalmers, Torbjorn Thiringer, for all the encouragement, technical guidance and continuous feedback on our thesis work. We also like to thank our supervisor at Volvo Cars, Johan Lektenius, for providing us an opportunity to embark on this thesis and his continuous support during the thesis. Furthermore, we would like to take this opportunity to thank Robert Karlsson, Daniel Pehrman, Evelina Wikner, Andreas Henriksson and Peter Berggren (Volvo Cars) for their help, kindness and support.

Premkumar Ayyadurai,
Navya Kundaranahalli Renukaiah,
Gothenburg, August 2017.

Contents

Chapter 1

Introduction

1.1 Background

Electrification of vehicles is a significant step towards sustainability and environment friendly technology in the automotive industry [1]. Those vehicles are either completely or partially electrified by introducing electrical components in the powertrain of the vehicle [2]. Batteries are an integral part of the powertrain and act as a energy source [3]. Thus the performance of the battery is critical at the powertrain level and also at the vehicle level as a whole [4].

To analyse the electric powertrain performance, an electrical equivalent battery model is required. There are various models available for the battery with various complexities [5]. The existing models does not depict the operation of the battery in all driving conditions of the vehicle. Generally the battery model in the low frequency range is modelled by testing the battery with sinusoidal sweeps of very low current in the frequency range 0.1 Hz to 100 kHz [6].

However during driving conditions like acceleration of the vehicle, the battery in the powertrain needs to supply a high magnitude current pulse for short duration. Hence the battery model developed with low current sinusoidal sweeps for a range of frequencies cant accurately predict the above driving conditions. This calls for the modelling of the battery that also includes the performance of the battery for high current pulses. But the available battery testing instruments don't have a high current and high frequency range capabilities.

1.2 Aim

The aim of the thesis is to design and develop a current pulse testing circuit to test a battery. Another objective is to develop an electrical equivalent circuit model of a battery accounting for the non-linearity of the high current pulses in the frequency range from 0.1 Hz to 100 kHz with a focus on the high frequency range. This model is obtained on a battery cell level.

1.3 Scope

Initially, testing is done on a single battery cell and can then be extended to module level and finally to a battery pack level. Ageing of the battery is not considered in the battery modelling for high current pulses. The tests are conducted at selected temperature

and SOC level for accurate modelling. Relaxation of the battery is also studied but not included in the models. In addition to that, tests are conducted only on a given lithium ion battery not for all cell chemistry's.

1.4 Ethical and sustainable aspects

Electric vehicles are sustainable if the source of electric power produced to charge the batteries are from renewable resources like hydro, solar, wind etc [7]. In contrary, they are not a sustainable option if the electric power produced is from the non renewable resources like fossil fuels etc [8].

Moreover electric vehicles are zero emission technology and hence environment friendly [9]. But as mentioned above, this is questionable if the electric power is produced by burning fossil fuels. Availability of raw materials to manufacture the battery is another area that has to be addressed if the electric vehicles increase in future because of the various benefits it offers. The above can be overcome if the life of the battery is enhanced for many years and hi-tech recycling technologies are adopted [10]. Still certain batteries like lead acid battery still pose a threat to environment and humans after their life cycle.

There are various ethical aspects that will be considered during the course of this work. IEEE code of ethics will be followed in this thesis work. The apt code of ethics that can be applied for this project are listed here. First, to be honest and realistic in stating claims and assumptions of the battery model with available measurement data. Second is to improve the understanding of the battery response for large current pulses from the vehicle application point of view.

1.5 Contributions

A current flowing in a cell has a significant impact on the operation of the cell. Hence, such a non-linearity introduced by the current magnitude has to be included in the mathematical modelling of a cell. Earlier methods of mathematical modelling generally includes the impact of the following factors: state of charge (SOC), temperature and frequency [11][12]. To an extent, the large current dependency is studied and included in the battery cell modelling but focused only in the low frequency region because of the test setup limitations [13][14]. In order to include the frequency dependence in the mathematical modelling, the existing works use only the small signal method results i.e. results from Electrochemical Impedance Spectroscopy (EIS) [12][14]. This thesis aims at the mathematical modelling of the cell by obtaining the impedance behaviour over frequency and current magnitude simultaneously. Hence, a current pulse testing circuit with both the high current and high frequency range capabilities is designed and developed to test and model a battery cell. The procedure to test, measure and analyse the results is explained in detail with the assumptions.

The previous published works represents the mathematical modelling of the cell as a complex electrical network with high accuracy [13]. Instead, in this thesis, models are represented as a less accurate but simple networks [15] for different frequencies and current magnitudes at selected temperature and state of charge(SOC). The existing research works are used to explain and validate the behaviour of the cell for different operating conditions during the course of this thesis.

1.6 Thesis Outline

A short introduction about the thesis and its objectives are discussed in this chapter. Further a brief theory with respect to cell modelling is discussed and the requirements for large current pulse testing are listed. Pretests are carried out on the selected cell to obtain its impedance behaviour over state of charge (SOC) and temperature. Based on the given requirements, the large current pulse test setup is designed and built. Simple mathematical models are derived from the measured data and parameters in the cell model are analysed along with visualisations of the measurement results. Finally, the thesis is concluded with important observations and scope for possible future work.

Chapter 2

Theory

A battery is an electrochemical component and it delivers electrical energy during discharge and stores energy in the form of chemical bondings during charge. A Battery is comprised of one or more modules in series or/and parallel combinations based on the given specifications like nominal voltage and Amperehour capacity of the battery. The individual module is also comprised of many cells in series or/and parallel combinations with an effective cooling mechanism provided for the cells. Even though the battery is not a pure electrical component, electrical represenation is required to analyse the operation of the battery at a system level in electrical applications. Hence, this calls for a mathematical modelling of the battery.

A single cell is also referred to as a battery in certain applications. A simple cell model is shown in Figure 2.1 where E is open circuit voltage (OCV) of the battery; Z is internal impedance of the battery and V_t is the terminal voltage of the battery [15]. I is the current flowing in the battery when it is loaded externally. The parameters OCV and Z has a strong dependency on the state of charge (SOC) and operating temperature of the battery.

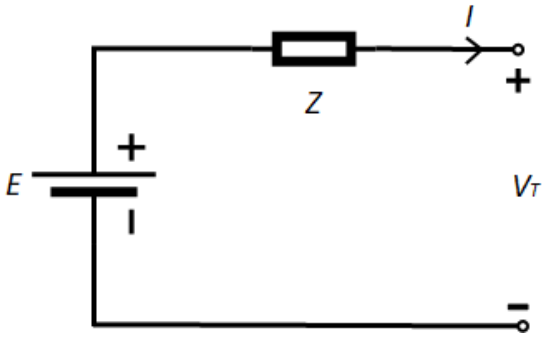


Figure 2.1: Simple cell model

For a constant current flow either during charging or discharging of the battery, the impedance Z is equal to a resistance. In case of a small sinusoidal currents or a pulse current operations, Z is not equal to a resistance and it shows a strong dependency on the frequency. The impedance of a cell is capacitive for lower frequencies and inductive for higher frequencies at a given SOC and temperature [14]. Hence, a piece-wise cell modelling can be carried out depending on the frequency. In order to avoid complexity in the electrical circuit representation of the cell, a simple inductive and capacitive equivalent

impedance of the cell is shown in Figures 2.2 and 2.3 respectively [15]. The impedance in the high frequency region is represented as a series RL element. The transfer function of this circuit is derived and represented by the parameters of the model as shown in 2.1. The transfer function contains one pole and no zero.

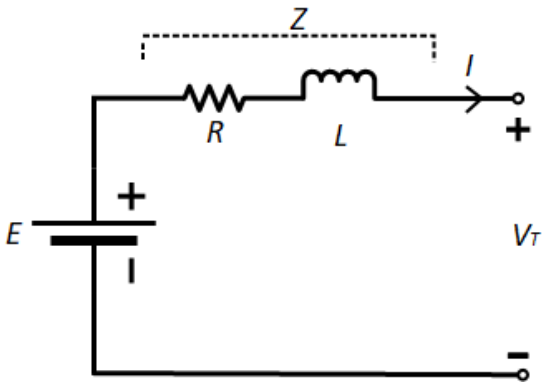


Figure 2.2: Simple cell model for high frequency region

$$H(s) = \frac{I(s)}{E(s) - V_T(s)} = \frac{1}{Z(s)} = \frac{\frac{1}{L}}{s + \frac{R}{L}} \tag{2.1}$$

For the low frequency region, the equivalent impedance of the cell is represented as capacitive as shown in Figure 2.3. Unlike the series RL circuit representation for the high frequency region, the impedance here is a series connection of R with a RC parallel branch. The transfer function of this circuit is derived and represented by the parameters of the model as shown in 2.2 giving a one pole and one zero system.

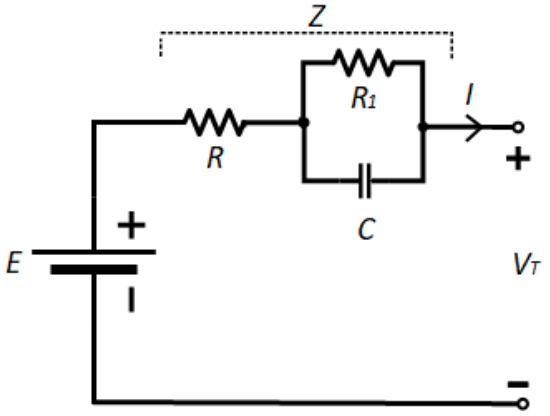


Figure 2.3: Simple cell model for low frequency region

$$H(s) = \frac{I(s)}{E(s) - V_T(s)} = \frac{1}{Z(s)} = \frac{\frac{1}{R}s + \frac{1}{RR_1C}}{s + \frac{R+R_1}{RR_1C}} \tag{2.2}$$

In this thesis, a large current pulse testing circuit is built and tested with a cell to analyse the dependence of impedance Z on the magnitude of the current. The block diagram of the proposed test setup with the cell is shown in Figure 2.4. As discussed in

the introduction chapter, the thesis objective is to study the dependency of Z on frequency and current magnitude. Hence the other two dependency factors, SOC and temperature has to be maintained at the same operating point throughout the large current pulse study. The SOC and temperature curves are not available for the given cell. Hence, in order to obtain those curves, pretesting on the cell is carried out and discussed in chapter 3. A relaxation study on the cell at a selected SOC level is conducted and analysed in chapter 4. The design of a test circuit board comprising a controlled switch and driver circuit along with the frequency control by a microcontroller are explained in chapter 5. The design of a resistor which determines the current magnitude of the pulse during testing is discussed in chapter 6. And in the same chapter, the selection and purpose of the fuse is discussed. In chapter 7, a physical connection layout of the test setup is described. And in chapter 8, measurements are carried out for different pulse durations and current magnitudes at a selected SOC and temperature. The measured results are then processed and the piecewise cell modelling is completed.

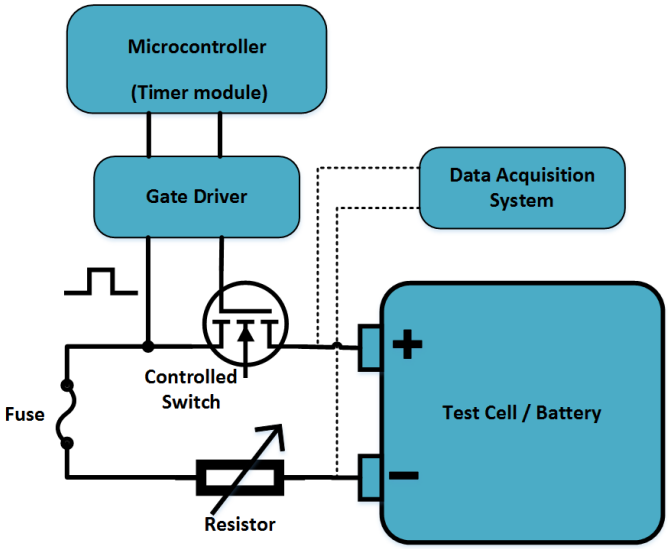


Figure 2.4: Block diagram of the current pulse testing circuit connected with the cell

Chapter 3

OCV Curve Determination

The experimental setup used for the determination of the SOC - OCV curve of a test cell used in this thesis work is as shown in Figure 3.1. The chemical composition of the test cell is lithium with an operating voltage range of 2.8 V to 4.15 V and a current capacity of 26 Ah. As shown in Figure 3.1, the instrument : a Gamry Reference 3000 [16] is used to determine the SOC - OCV curve. Since the test is performed at different temperatures, the test cell along with the connection wires from the instrument Gamry is placed inside the temperature chamber. Cables with the white and red termination are used for sensing the test cell voltage and cables with the green and blue termination are used for injecting the current to a test cell. A temperature sensor is used to measure the cell temperature. The test cell is placed inside a battery holder and the positive and negative leads are pressed under the bolted termination for a proper contact during connection.

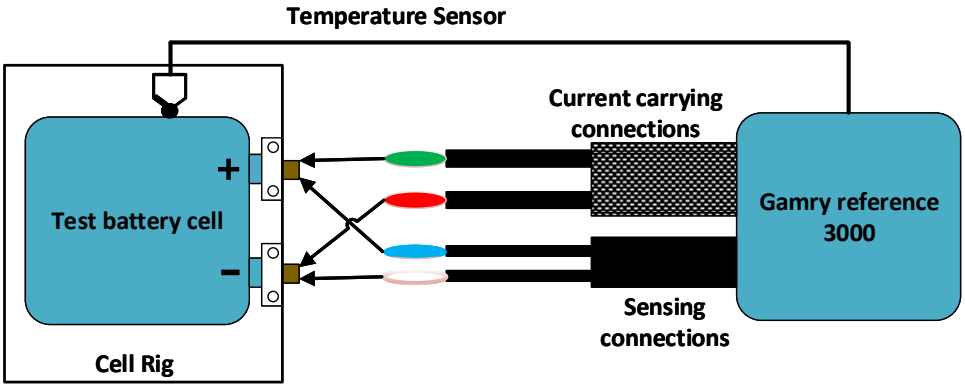


Figure 3.1: Experimental setup to determine the SOC-OCV curve using the instrument Gamry

The sequence of the test performed to determine the SOC - OCV using the instrument Gamry is shown as a flowchart in Figure 3.2 and represented graphically in Figure 3.3 (voltage and time axes are not drawn according to the scale). The test sequence uses two modes of operation defined using the Gamry Framework software. The two operating modes are : the Galvanostat mode and the Potentiostat mode. The test sequence starts with a Potentiostat mode by allowing the test cell to stay at its nominal low voltage (2.8 V) for 48 h. Then it goes to the galvanostat mode where the cell is charged from its nominal low voltage (2.8 V) to its nominal high voltage (4.15 V) continuously with a constant current amplitude. After this phase, the cell is again operated in potentiostat

mode at its nominal high voltage for 48 h. After 48 h, the cell is discharged from 4.15 V to 2.8 V continuously with the same current magnitude as the charging current. Finally, the cell is again kept in the potentiostat mode at 2.8 V for 48 h. Ideally the two galvanostat modes for the charging and the discharging would be sufficient for the determination of the SOC - OCV curve. But when the continuous charging of the cell is stopped, the cell voltage might tend to drop by a few mV. The voltage which the cell reaches after this drop might not be the exactly required voltage for the next phase of the test. Hence the potentiostat modes are added to make sure that the cell voltage has reached exactly the required point by allowing it to stay at that voltage for a long period of time.

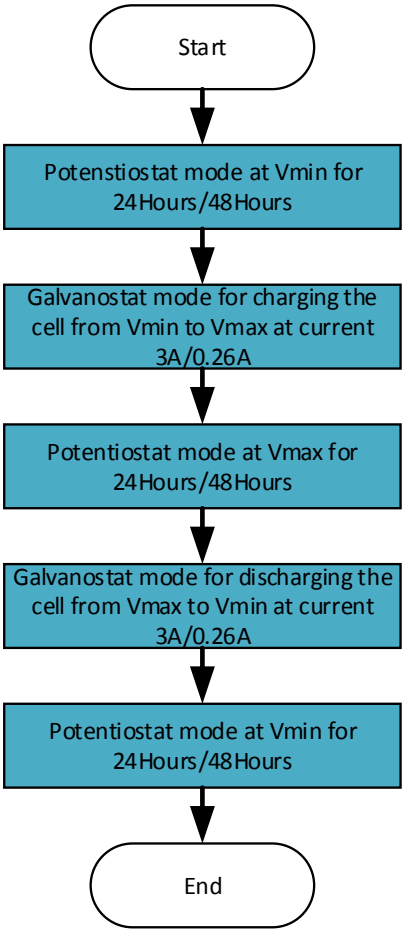


Figure 3.2: Flow chart of the test sequence used in the determination of the SOC-OCV curve

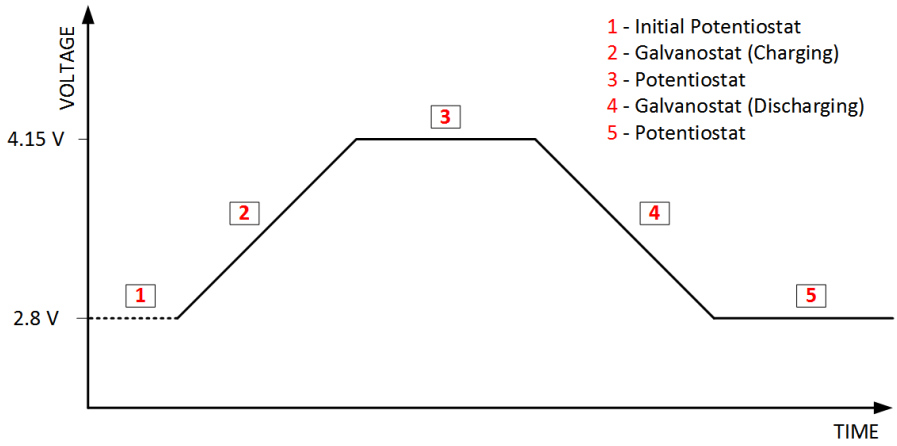


Figure 3.3: Graphical representation of the test sequence used in the determination of the SOC - OCV curve

Using the test sequence shown in Figure 3.3, the SOC - OCV curves are obtained for the test cell at two different constant currents 0.26 A and 3 A at 20 °C. The charge and discharge cycles for the two currents are shown in Figure 3.4. For a low charging and discharging current value, the resistive drop in the cell could be very low and the terminal voltage read would be very close to the cell open circuit voltage (OCV) of the cell. To observe this phenomenon, low current magnitudes like 0.26 A and 3 A is chosen for the SOC - OCV curve determination.

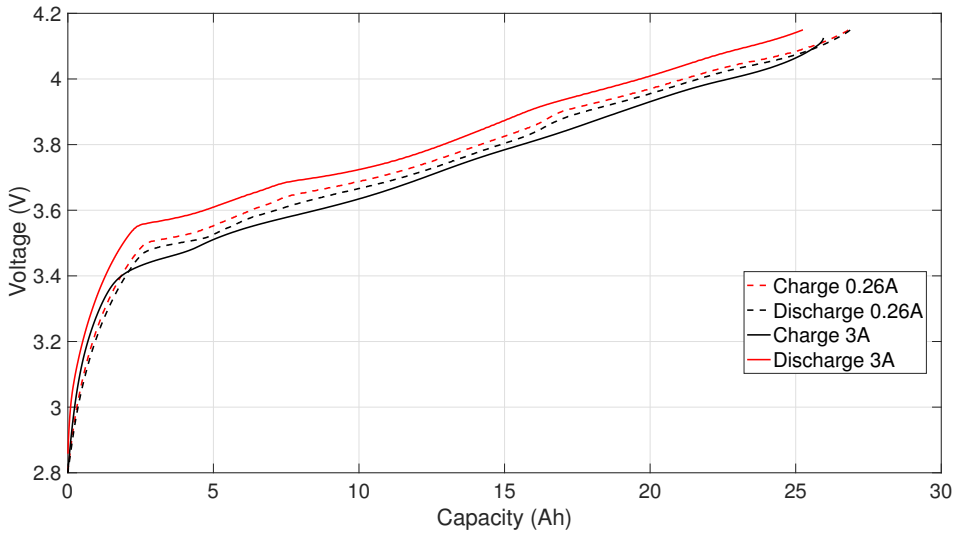


Figure 3.4: Charge and discharge curves for the test cell at 0.26 A, 3 A at 20 °C using Method 1

The curves in Figure 3.4 are plotted by taking into account the amperehours (Ah) obtained from the two galvanostat modes (which will be referred as Method 1 in the continuity). Using Method 1, the end points reached for the two currents are not similar and also the total Ah at the end of the two galvanostat modes is more than the known battery capacity of 26 Ah. Due to these discrepancies in the result, charge and discharge cycles are redrawn adding the Ah from the potentiostat mode to the Ah from the galvanostat

mode (which will be referred as Method 2 in the continuity). The charge and discharge curves for the Method 2 is shown in Figure 3.5. The total Ah from the two modes is listed in Table 3.1. It is observed that the total Ah reached at the end of charging and discharging cycle using Method 2 for the two currents is quiet similar and the capacity of the cell is close to 27 Ah. The difference in the end points reached using Method 1 and Method 2 is shown in Figure 3.6 which shows the comparison for 3 A curves at 20 °C.

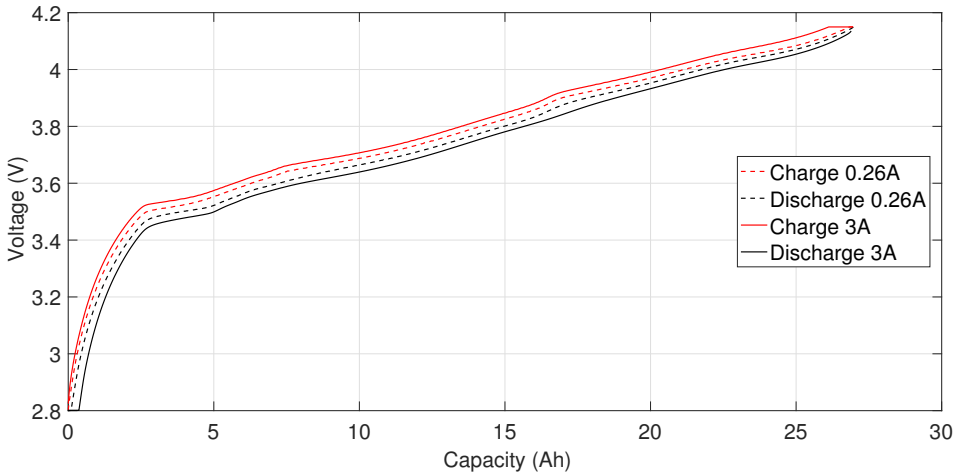


Figure 3.5: Charge and discharge curves for the cell at 0.26 A, 3 A at 20 °C using Method 2

Table 3.1: Number of Ah considering both the galvanostat mode and the potentiostat mode for 0.26 A and 3 A at 20 °C

Modes Of Operation	**0.26 A**	**3 A**
Galvanostat (Charging) + Potentiostat at 4.15 V	27.05	26.95
Galvanostat (Discharging) + Potentiostat at 2.8 V	27.06	26.89

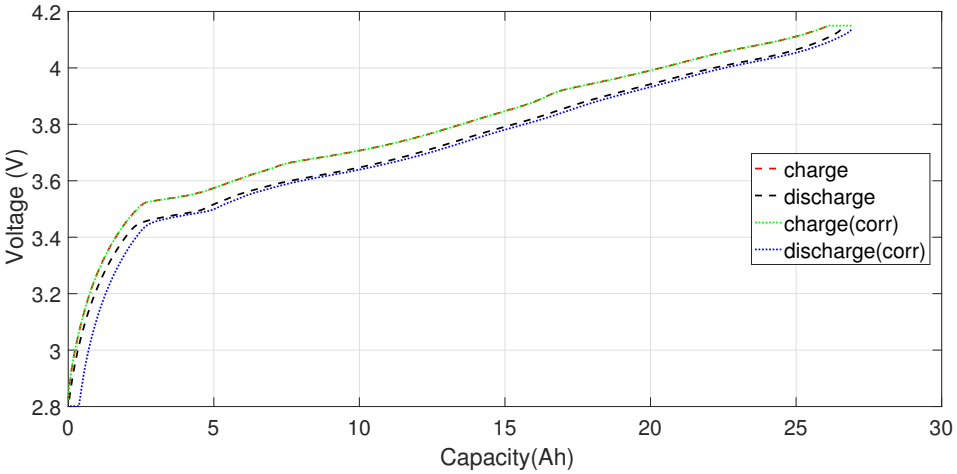


Figure 3.6: Charge and discharge curves of the cell for 3 A at 20 °C using Method 1 and 2

The test sequence shown in Figure 3.3 is also performed on the test cell for different temperatures at 3 A charging and discharging current. The results are plotted in Figure 3.7 using Method 2. It is observed that, the resistance of the cell varies with the temperature and so as the state of charge levels [17]. In support of this, the variation of ΔV for 3 A current at different temperatures is shown in Figure 3.8 and average resistance of the cell at different currents and temperatures is listed in Table 3.2. It is also observed that the internal resistance of the cell has decreased with the increasing current and the temperature.

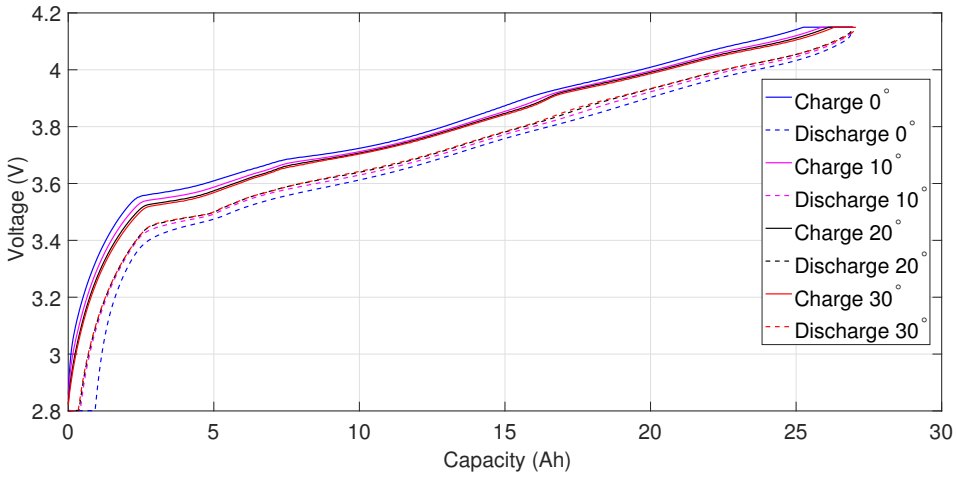


Figure 3.7: Charge and discharge curves of the cell for 3 A at different temperature using Method 2

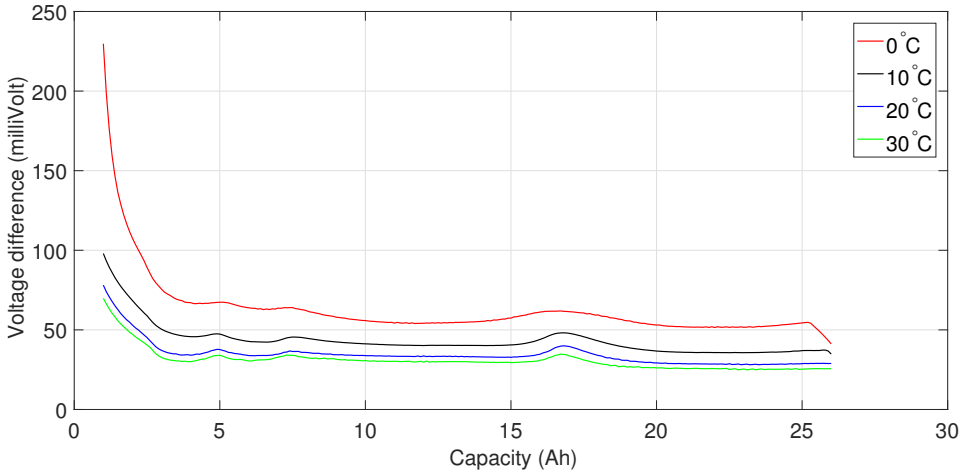


Figure 3.8: Variation of ΔV between 3 A charge and discharge curves at different temperatures for using Method 2

Table 3.2: Average resistance of the cell at different currents and temperatures

Charging and discharging current of the cell (A)	0.26	1.3	3			
Temperature of the cell (°C)	20		0	10	20	30
Resistance of the cell (mΩ)	42.1	15.7	19.1	13.6	10.9	9.8

Table 3.3: Total Ah for charge and discharge cycles for 3 A current at different temperatures

Modes Of Operation	**0 deg**	**10 deg**	**20 deg**	**30 deg**
Galvanostat (Charging) + Potentiostat at 4.15 V	26.92	26.97	26.95	27.04
Galvanostat (Discharging) + Potentiostat at 2.8 V	26.87	26.88	26.88	26.96

Table 3.3 shows the total Ah at the end of charging and discharging cycles for 3 A current at different temperatures. It is also confirmed from these tests that the capacity of the test cell is close to 27 Ah. At 20 °C, the average voltage drop in the cell is calculated for different currents and plotted in Figure 3.9. From the figure, there is an offset voltage of 10 mV in the cell.

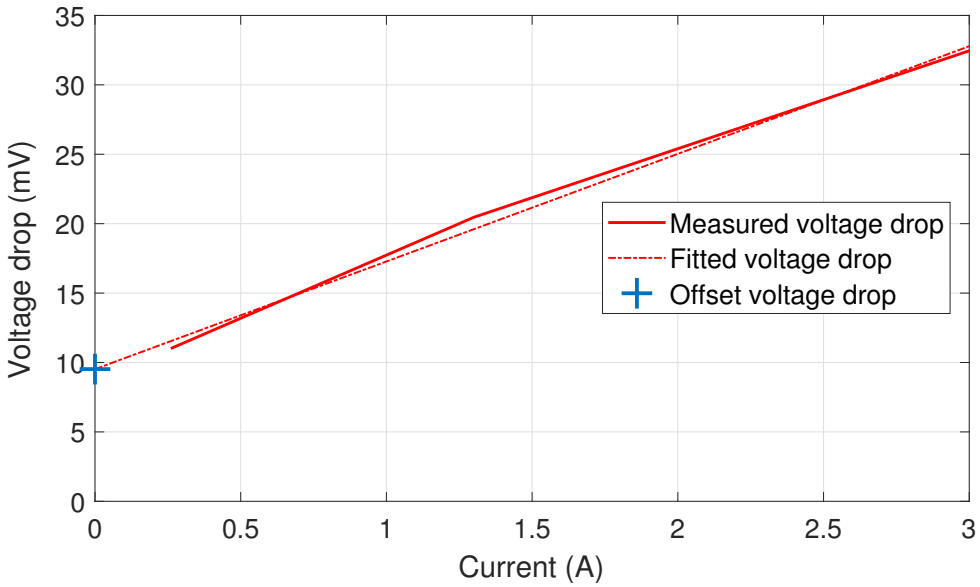


Figure 3.9: Average voltage drop in the cell for different currents at 20 °C using Method 2

Chapter 4

Relaxation Tests

This chapter describes the test procedure used to observe the relaxation behaviour of the test cell. Electrochemical Impedance Spectroscopy (EIS) is carried out to analyze the change in impedance of the test cell after charging and discharging cycles.

In this relaxation test, the test cell is charged from 0 % SOC to 50% SOC and EIS measurements are taken at every ten minutes (for initial half an hour) and at every one hour until 24 hour [18]. To compare the results with the discharging cycle, the same procedure is repeated after the test cell is discharged from 100% to 50% SOC. EIS for both the charging and discharging cycles is performed from 0.1 Hz to 1 kHz. The results of the EIS tests are shown in Figure 4.1. As it can be seen, the EIS measurement is different at different intervals of time. Also the test cell is taking a longer time to relax that even after 24 hour, it has not reached an equilibrium point.

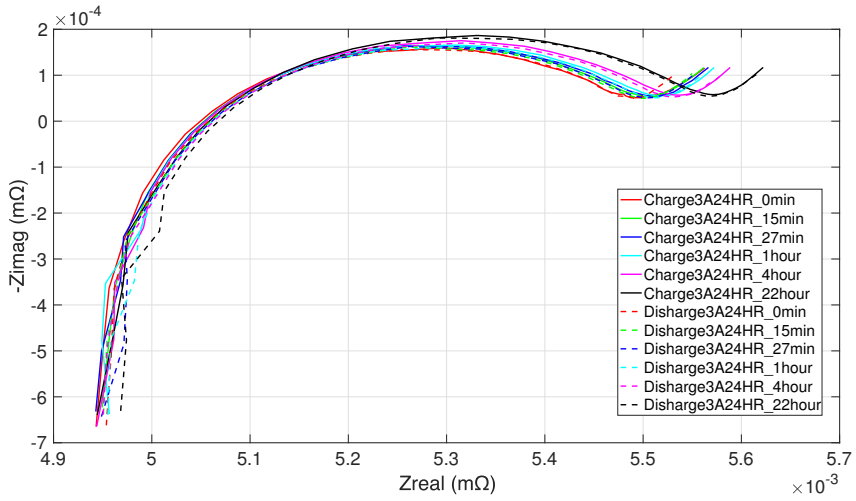


Figure 4.1: EIS test performed on the test cell at different intervals of time for 3 A current at 20 °C

The test procedure followed to perform the EIS test is shown in Figure 4.2 as a flowchart. The EIS measurement is performed using the instrument Gamry Reference 3000 and the test procedure is written using the Gamry Framework software. The test setup used is the same as in Figure 3.1. The current injected by the instrument Gamry to perform the EIS test is a maximum of 3 A for a frequency sweep from 0.1 Hz to 1 kHz.

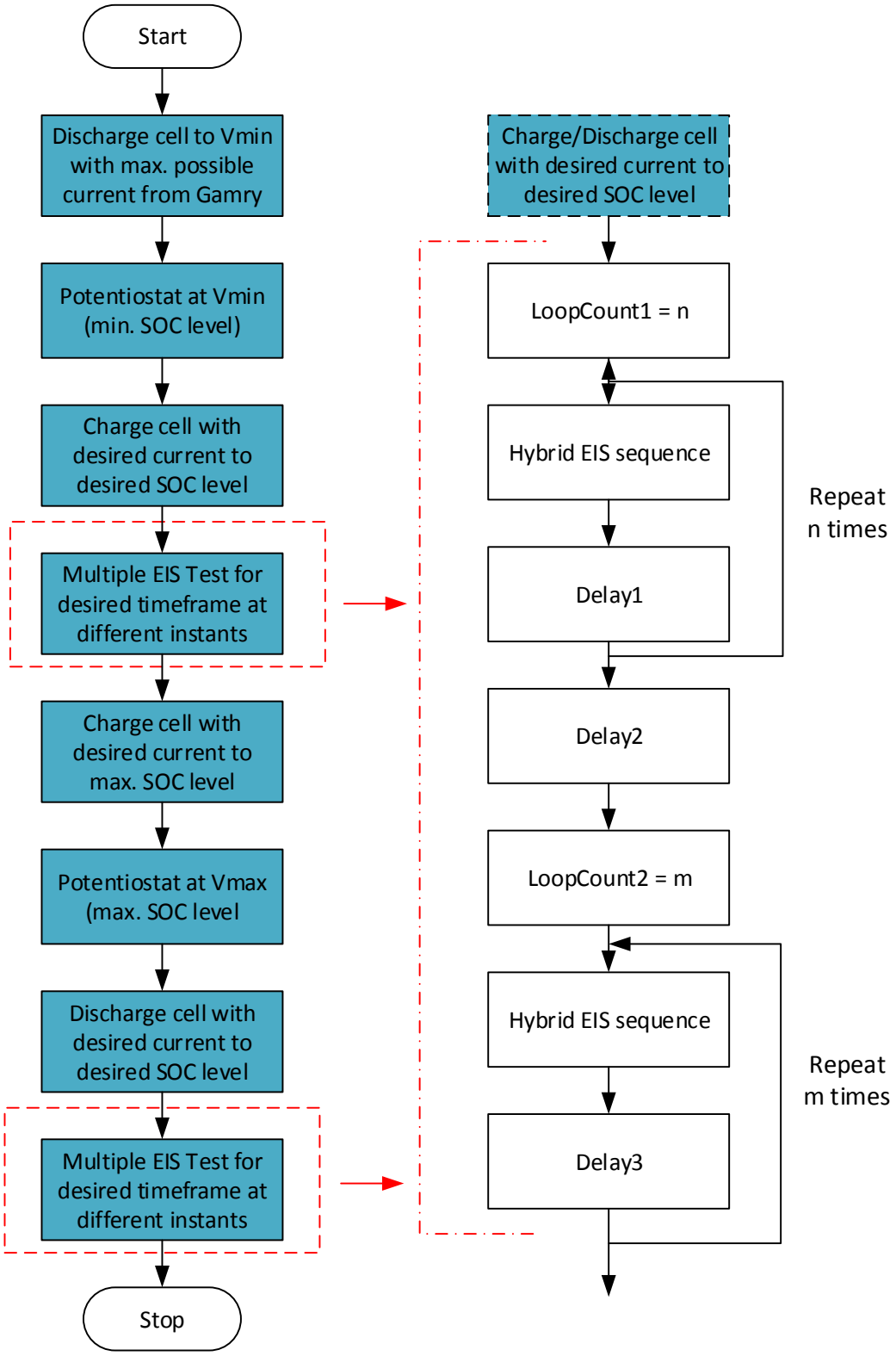


Figure 4.2: Testing Sequence implemented using the instrument Gamry 3000 to study relaxation of the cell at desired SOC level

Here also the galvanostat and the potentiostat modes are used in the test procedure. The test procedure starts by making sure that the test cell is at its nominal low voltage or at 0% SOC. Using the galvanostat mode, the test cell is charged to 50% SOC and a loop is initiated to perform EIS at a regular interval of time. After the charging cycle, the same procedure is repeated by starting the test from 100% SOC and discharging the test cell to 50% SOC.

From Figure 4.1, another important observation made is that the Z_{real} of the test cell is 4.95 mΩ. The conventional Z_{real} of the test cell used in this thesis work seems to be around 1.4 mΩ. Considering this, the Z_{real} obtained in the EIS measurement is bit higher. Regarding this, the experimental setup in Figure 3.1 is rechecked for the connection settings. It is observed that the voltage sensing connections were place after the bolted connection. Since it is not connected before that, the voltage drop across the bolted connection is added to the EIS measurement as well. Hence, changes in connection is made to the experimental setup as shown in Figure 4.3. since the space between the cell leads and the bolted connection is very less it was hard to connect the sensing and the current injecting wires close enough to each other.

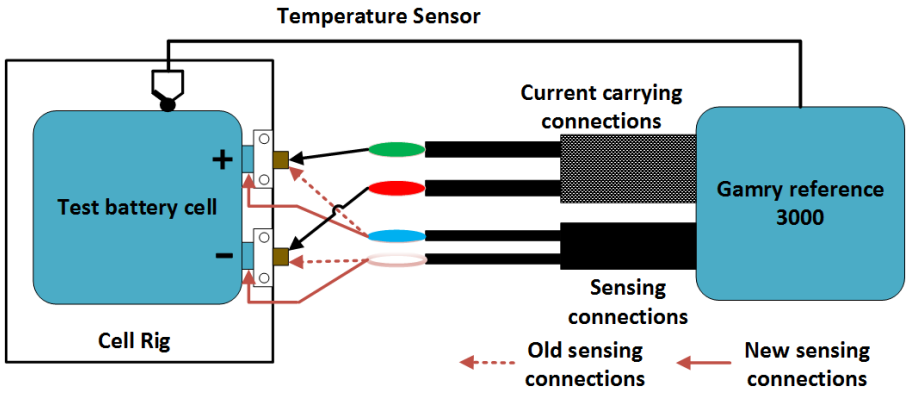


Figure 4.3: Experimental setup with modified sensing connections to determine the SOC-OCV curve of the test cell

After the modification shown in Figure 4.3, the SOC - OCV curve is repeated at 3 A current for 20 °C. There was a change in the SOC points compared to Figure 3.5. This is shown in Figure 4.4. Along with the SOC test, another relaxation test is performed using the new connection setup and the results are shown in Figure 4.5 and Figure 4.6. It is observed from Figure 4.5, that the cell Z_{real} has reduced to 1.7 mΩ. But the charging and the discharging EIS measurements are shifted more during different time intervals. To observe this, the EIS measurement is repeated on the test cell keeping it under the same experimental setup. The test result is shown in Figure 4.6. Again the curves are shifted and also the resistance has increased to 2.1 mΩ. When few more EIS measurements were repeated under the same test conditions, it is observed that the resistance started varying each time. It was not possible to get the consistent and repetitive results.

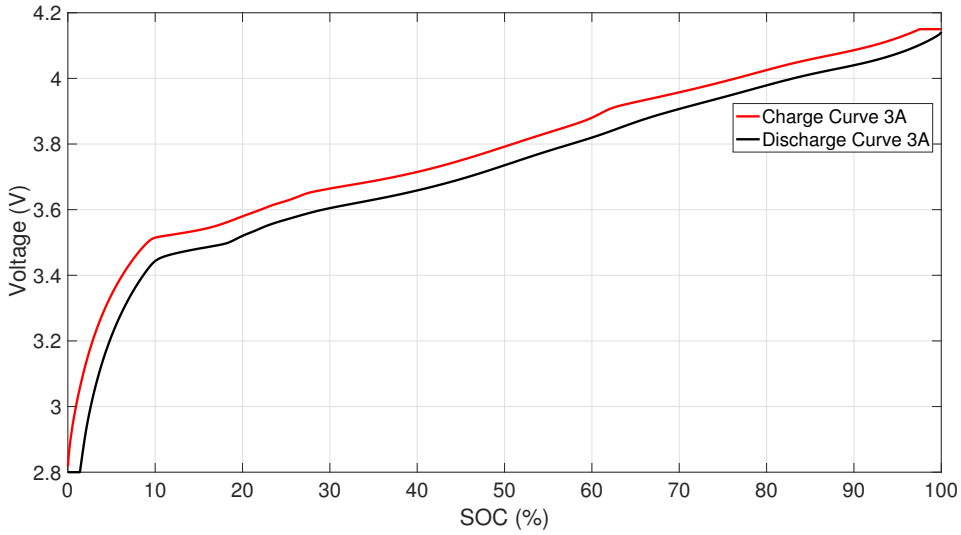


Figure 4.4: Modified charge and discharge curve for the cell at 3 A current at 20 °C

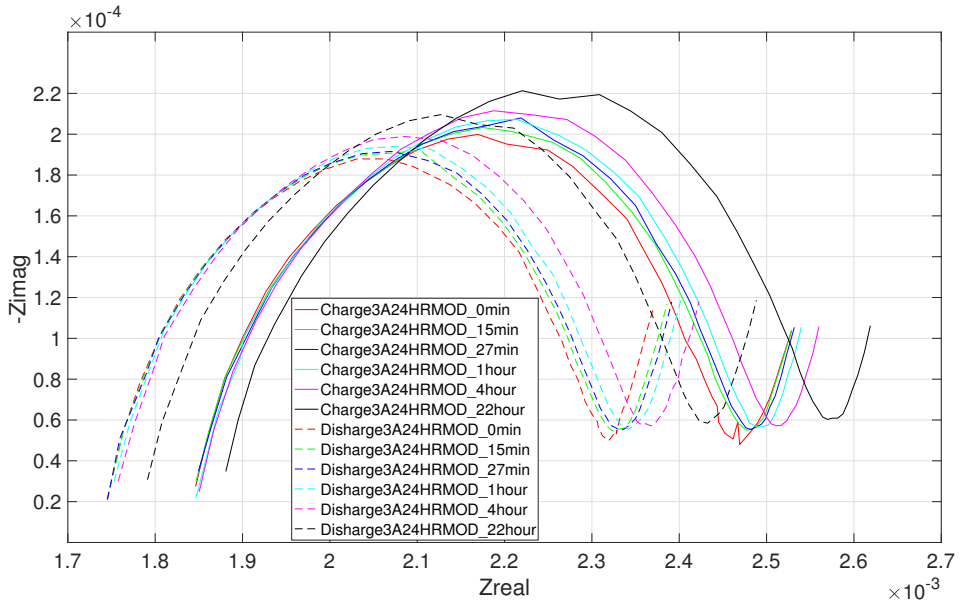


Figure 4.5: EIS test performed on the test cell at different intervals of time for 3 A current at 20 °C

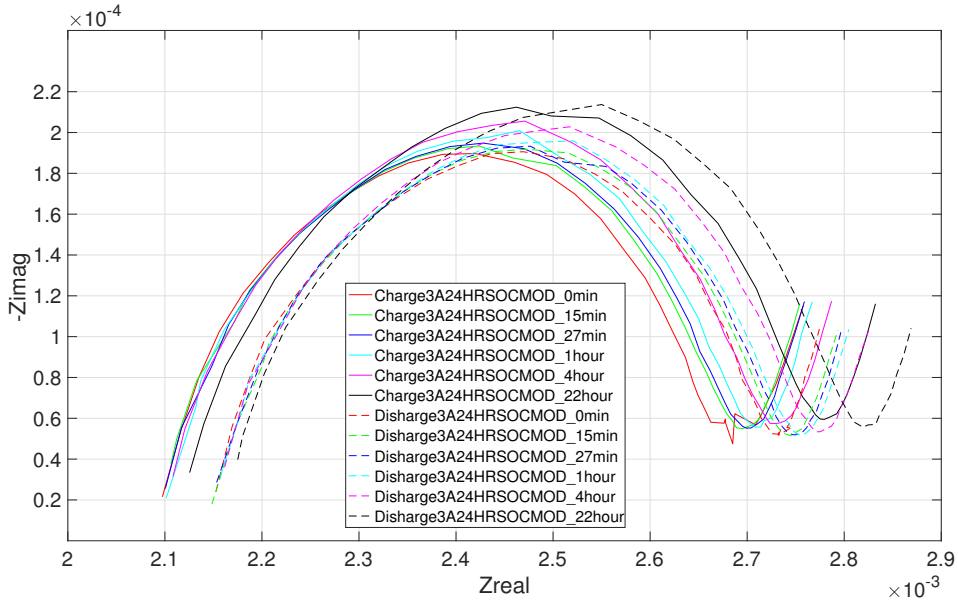


Figure 4.6: EIS test performed on the test cell at different intervals of time for 3 A current at 20 °C

Since the results were not repetitive, the working condition of the test cell is analyzed using an algorithm (explanation of the algorithm is out of the scope of this thesis work). It is found that the state of health of the test cell is in the beginning of life phase and the cell is not damaged. The result of the test performed using the algorithm is shown in Figure 4.7 [19]. To analyze the reason for the varying cell resistance further tests are performed by changing the way of connecting sensing connections of the instrument. It is found that the instrument Gamry is very sensitive to the way the sensing and the current injecting cables are connected and also the impedance of the test cell varied for different connections. Since more emphasis has to be given on the design of current pulse generation circuit in this thesis work, the relaxation and SOC tests were not continued further.

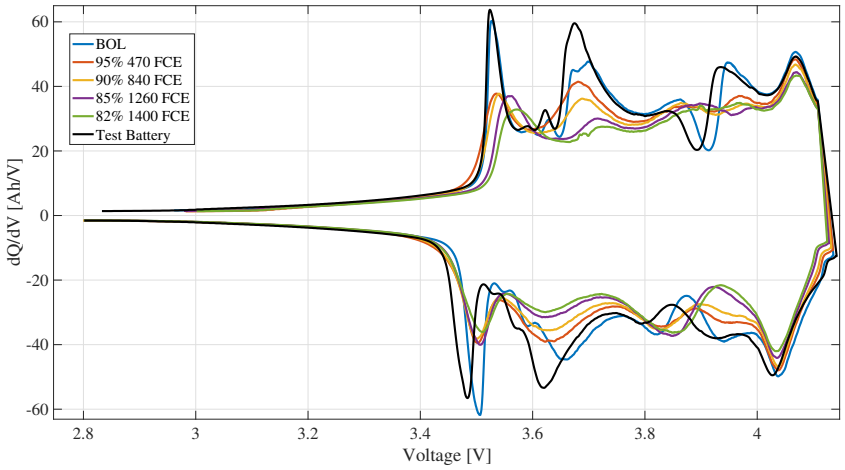


Figure 4.7: Test results performed to analyze the state of health of the test cell [19].

Chapter 5

Design Of The Current Pulse Generation Circuit

This chapter describes the design of an electrical circuit that generates the current pulses of large magnitude and small pulse widths. The main objective of this electrical circuit is to generate current pulses of varying magnitude from 1 C-rate to 10 C-rate and of different pulse widths. Even though the circuit is used to perform characterization of a single test cell, it is built with a capability of testing on a battery module. This test circuit can handle the voltage magnitudes up to 650 V and a current magnitude up to 420 A.

The block diagram of the current pulse generation circuit with all the components is shown in Figure 5.1. The main components used are : Arduino with a micro-controller, an Optocoupler, Driver IC's, MOSFET switch and Heat sink. An Arduino is equipped with a microcontroller ATmega328 sets the variable pulse width for the current pulses. Since it is easy to obtain the pulses of different time periods using the timers of the microcontroller and there is no need for any external hardware circuit, the arduino board is used for the pulse width variation.

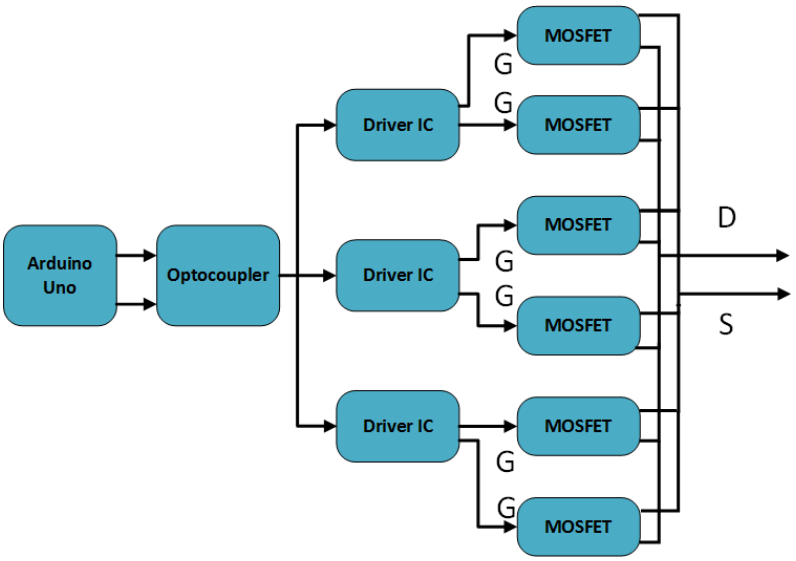


Figure 5.1: Block Diagram for Current Pulse Generation Circuit (G = Gate, D = Drain, S = Source)

The generated pulse is fed as the input signal to the opto-coupler ACPL-P349, whichis mainly used for an electrical isolation between the micro-controller and the MOSFET-driver circuit. The output from the opto-coupler to the MOSFET switches is stepped up using the MOSFET Driver IC IXDD604PI. Since it is a dual output gate driver, one driver IC is used to drive two MOSFET switches. Three driver circuits are used to turn on the six parallel connected MOSFFET's. These are silicon carbide power MOSFET's, where each switch has a rated drain-source voltage of 650 V and a rated drain current of 70 A. Even though nominal high voltage of the the test cell used in thesis work is 4.15 V, the current pulse generation is circuit is designed to test for voltage upto 650 V thinking that the same circuit can be used to perform tests for a battery module.

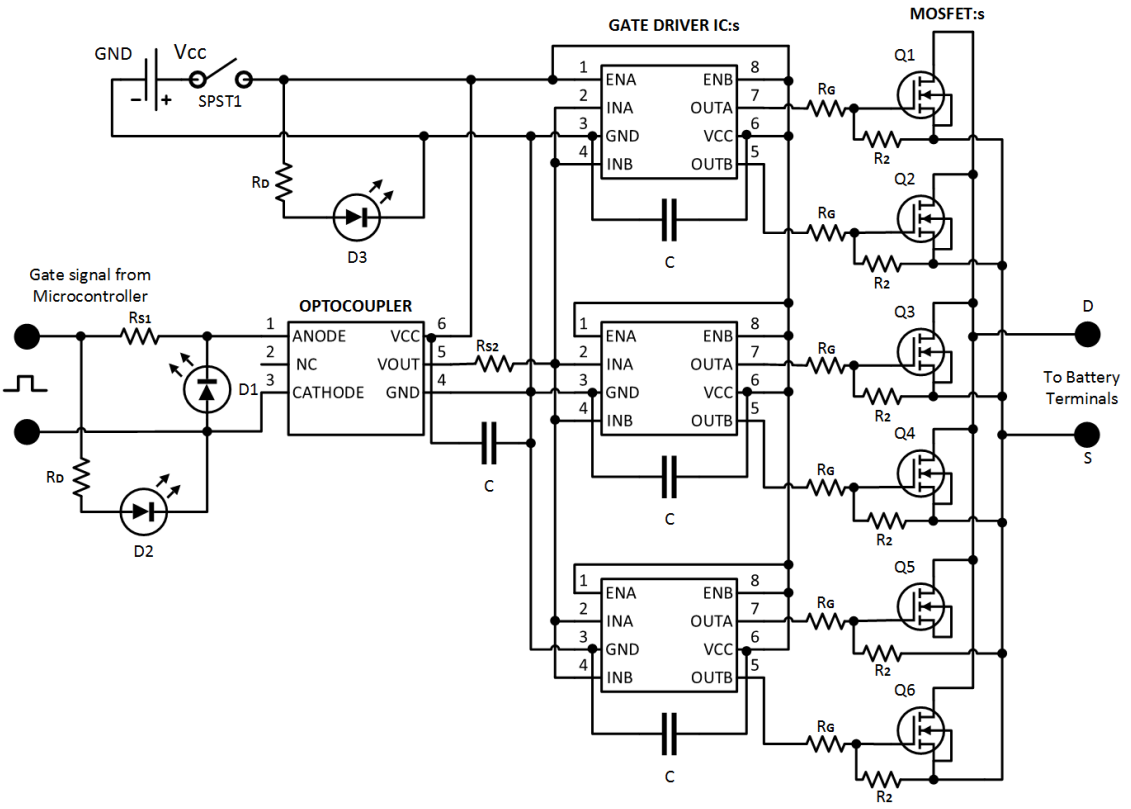


Figure 5.2: Circuit diagram for current pulse generation circuit

As the main objective of the circuit is to generate short timed pulses, it is very important to have as little stray inductance as possible. Minimizing the stray inductance is necessary in order to have shorter rise time of the pulse and to avoid a voltage over shoot during the turn-off of the switch. In order to achieve this, the MOSFET switch with a R_{DSon} of 30 mΩ with fast switching characteristics is chosen and a two layer electronic circuit board (PCB board) is designed providing anti-parallel paths for the current. The electronic circuit board is designed using a software *DesignSpark PCB* by creating a library for all the components used. The circuit diagram of the current pulse generation circuit is shown in Figure 5.2. After the design of the circuit board, it is tested by providing a pulse from the arduino. Figure 5.3 shows the pulse train of pulse width of 16 µs. Figure 5.4 and Figure 5.5 show the rise time and fall time of approximately 25 ns.

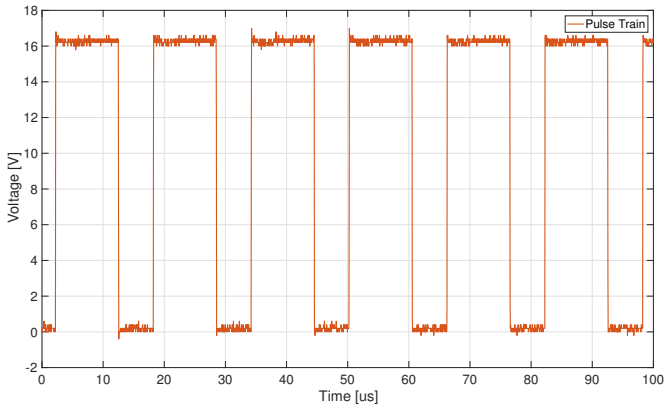


Figure 5.3: Sample pulse train output in current pulse generation circuit

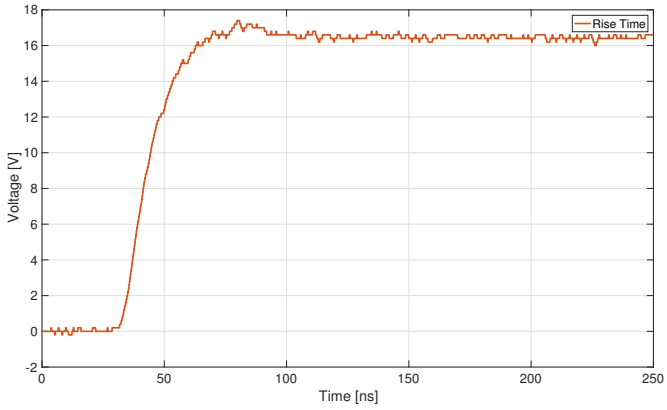


Figure 5.4: Rise time of the sample pulse train output

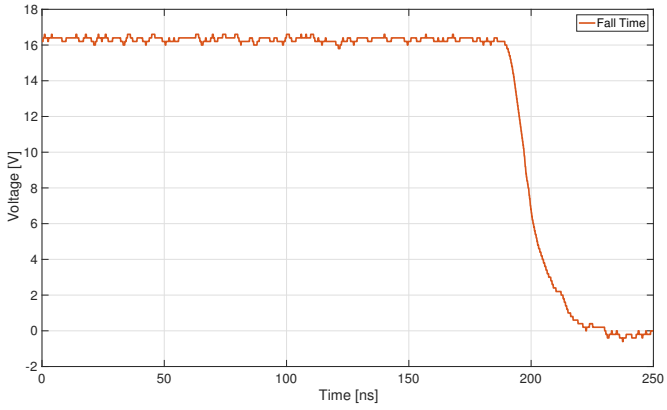


Figure 5.5: Fall time of the sample pulse train output

Chapter 6

Resistor Design and Circuit Protection

This chapter describes the design of a resistor element for the generation of the current pulse. This resistor element connected between the battery terminals and the MOSFET switches, sets the magnitude of the current pulse generated. It explains about the two different resistor elements used in the circuit to obtain the current pulses of different magnitude. This chapter also describes about the fuse used for the circuit protection.

As described in the previous section, the major objective in designing the test circuit for the pulse generation was to have as little inductance as possible in the complete circuit. For this reason a resistor element with little inductance is needed for this thesis work. Two resistors elements are used to obtain the current pulses of magnitude approximately 1 C-rate and 10 C-rate. To obtain 1 C-rate of current pulse, an aluminum housed heat sink resistor from the manufacturer *arcol resistor* is used. For the current magnitude of 10 C-rate, it was difficult to obtain a resistor element having a low inductance from any other manufacturer. Hence, the resistor element is designed using a copper sheet.

Figure 6.1: Proposed resistor element design using a copper sheet

In order to get approximately 1 C-rate magnitude of the current pulse, a 0.1 Ω resistor is chosen out of the Arcol manufactured resistors. Since it was not possible to find another resistor element from which a 10 C-rate of current magnitude can be obtained, a resistor is designed using a copper sheet. A copper sheet of the dimension (0.1 mm∗ 100 mm∗2 m) is used to make the resistor element. In order to have a low inductance path for the current, the copper sheet is bent in loops as shown in Figure 6.1. These loops provide an opposite path for the current through them and reduces the inductance. Before physically designing the copper sheet, the same module is built in COMSOL Multiphysics as shown in Figure 6.2 and the inductance is calculated. The inductance value estimated for the resistor element in COMSOL is found to be 7.421 nH.

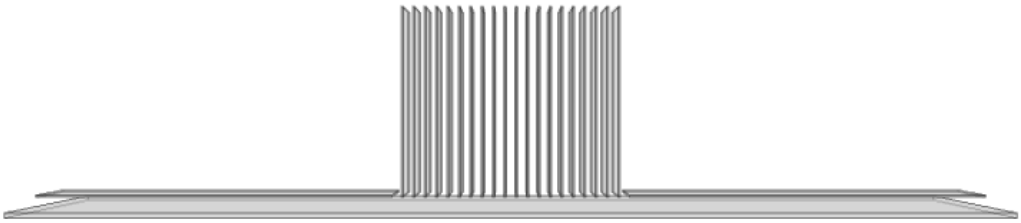


Figure 6.2: Estimation of inductance for the resistor element in COMSOL

Circuit Protection

In order to provide protection to the current pulse generation circuit from any short circuit currents from the test cell, a fuse is used as a short circuit protection device and it prevents the test setup from fire hazards. Fuse 0298060 manufactured by the *Littlefuse Inc.* is used in the testing. The specifications of the fuse are: 60A current carrying capability at normal operating conditions and fast short circuit current interrupting capability. Six fuses in parallel (360A) are used in the testing circuit in order to handle at least 10C current magnitude in the testing circuit without any interruption.

Chapter 7

Complete Test Circuit

This chapter describes the integration of the complete test circuit designed for the generation of the current pulses of varying pulse width and magnitude.

After the design of the electronic circuit board and selection of all the necessary components, the complete test circuit is organized as shown in Figure 7.1. The components from arduino to the MOSFET switches makes the printed circuit board. In the next stage the drain of the six parallel MOSFET's is connected to the resistor element (in this case it is the one made from the copper sheet). The other end of the resistor element is connected to the fuse and then to the positive terminal of the test cell. The source of the MOSFET's is connected to another copper sheet and then to the negative terminals of the test cell. When the test setup shown in Figure 7.1 is used, the pulse obtained contained a lot of disturbance because of the stray inductance. Hence the copper sheet connected to the source terminal is extended over the resistor element as shown in Figure 7.2. This arrangement considerably reduced the disturbance and the oscillations in the current pulse. Finally an oscilloscope is used for the data acquisition.

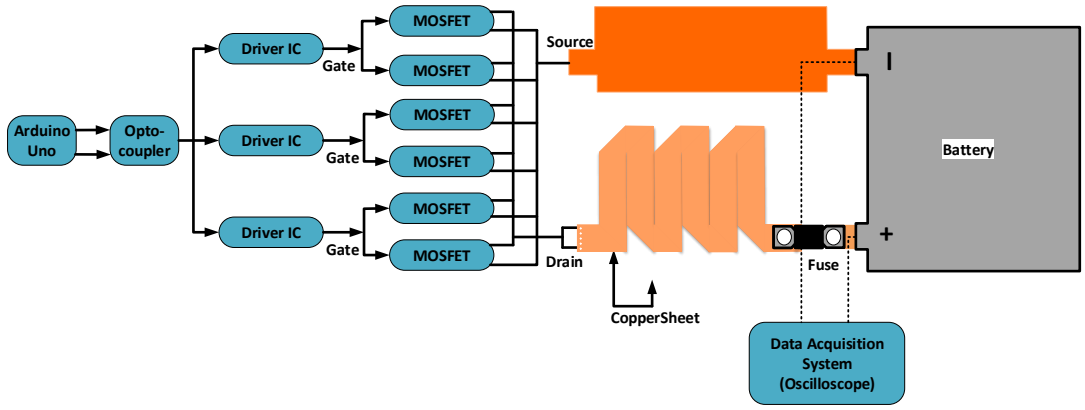


Figure 7.1: Complete test circuit for the generation of the current pulses

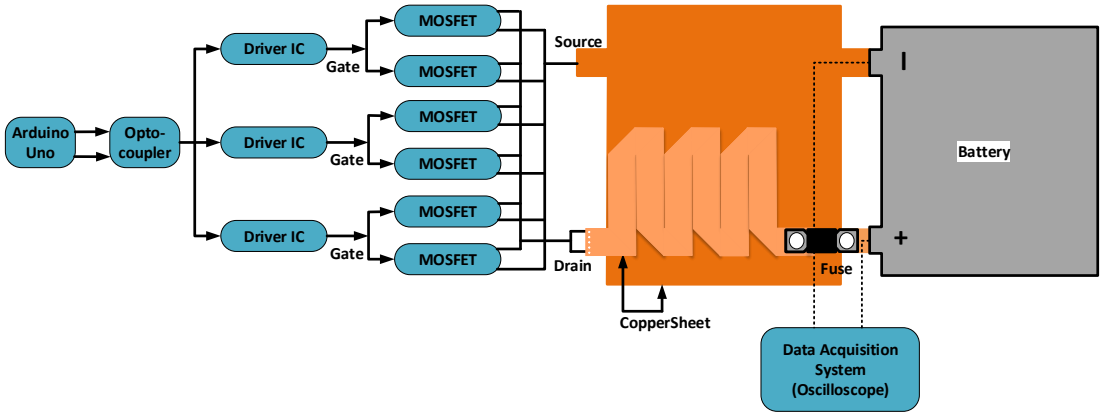


Figure 7.2: Improved complete test circuit for the generation of the current pulses

Using this test setup, the current pulses of varying pulse width and magnitude are generated for discharge current pulses of the cell. To do the same for charge pulses it would require an another test cell in the loop which would make the test circuit complex and require an effective control mechanism to obtain the desired current magnitude. After assembling the complete test setup, a sample pulse for 1 ms is obtained as shown in Figure 7.3. As the test cell is connected in the loop and it is the source of the discharge pulse, once the discharge starts, the capacity of the test cell reduces and so does the voltage. Since there is no other source that feeds the constant current to the system, the voltage response of the test cell reduces gradually as the discharge happens.

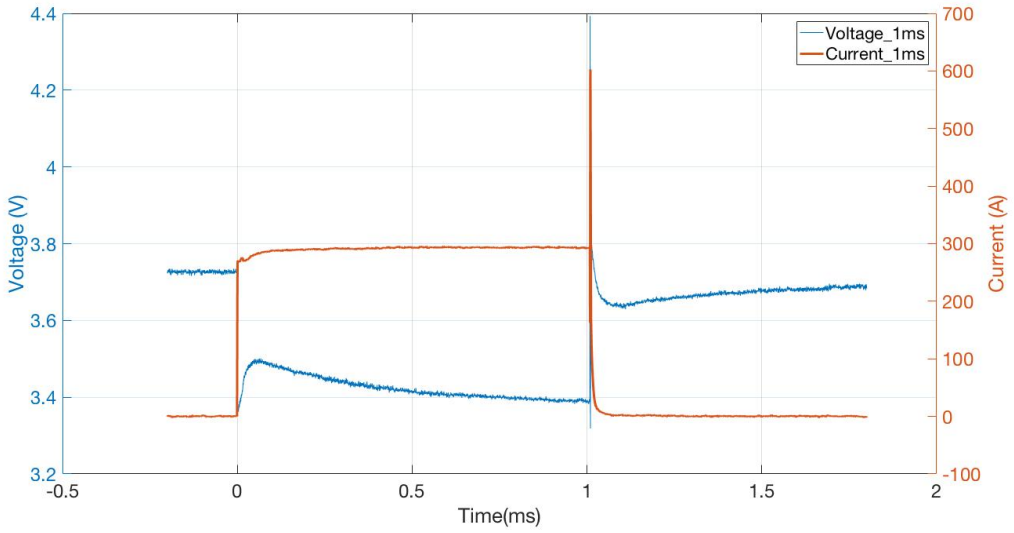


Figure 7.3: Sample pulse output from the complete test circuit for the generation of the current pulses

Chapter 8

Battery Modelling

This chapter describes the testing of the cell with the developed test circuit; and modelling of the cell for large current pulses with different magnitudes and pulse duration respectively.

Testing the pretested battery cell with the developed test circuit is shown in the Figure 11.1. The test is carried out at a room temperature and the SOC in the cell is set to approximately 50% using the Gamry instrument. The resistor element designed using the copper sheet to give approximately 10C current magnitude is used in this testing. The cell is allowed to discharge as a pulse with varying time widths and the selected pulse width duration are 10 µs, 100 µs, 1 ms and 10 ms respectively. The measured quantities are cell terminal voltage (V_t) and current (I) in the cell. The current (I) is indirectly computed by measuring the voltage across the resistor element (V_R). The measured terminal voltage of the cell (V_t) for a current pulse with 10C magnitude and varying pulse duration of 10 µs, 100 µs, 1 ms and 10 ms are shown in Figures 8.1, 8.2, 8.3 and 8.4 respectively.

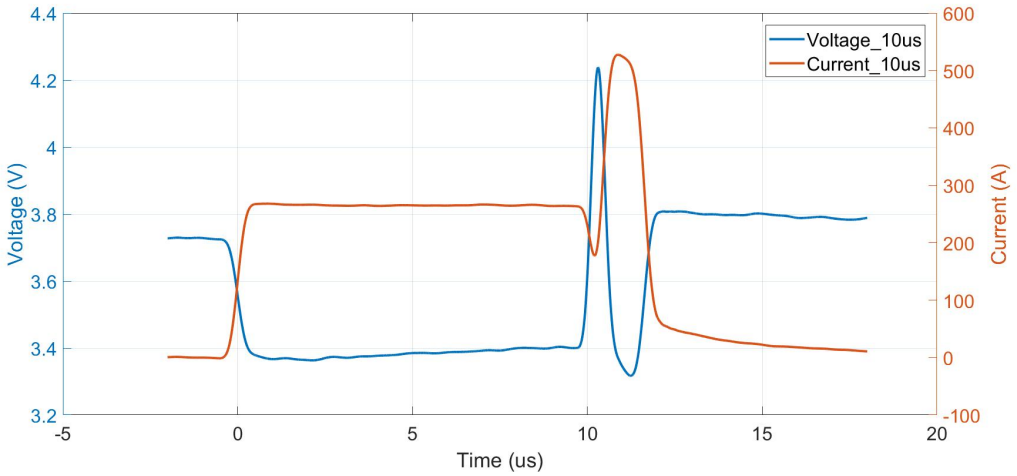


Figure 8.1: Cell terminal voltage and current pulse with 10C magnitude and 10 µs duration.

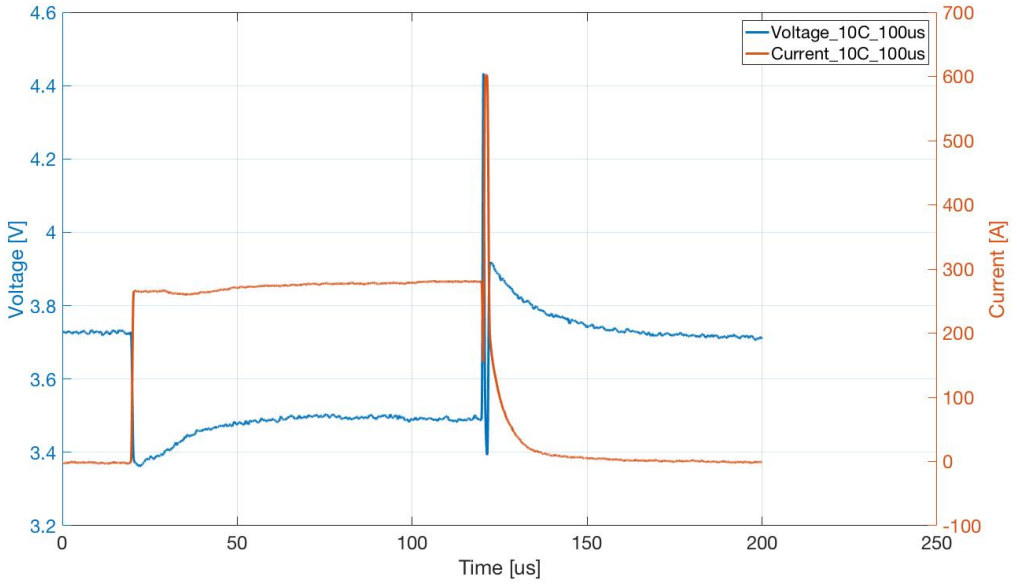


Figure 8.2: Cell terminal voltage and current pulse with 10C magnitude and 100 µs duration.

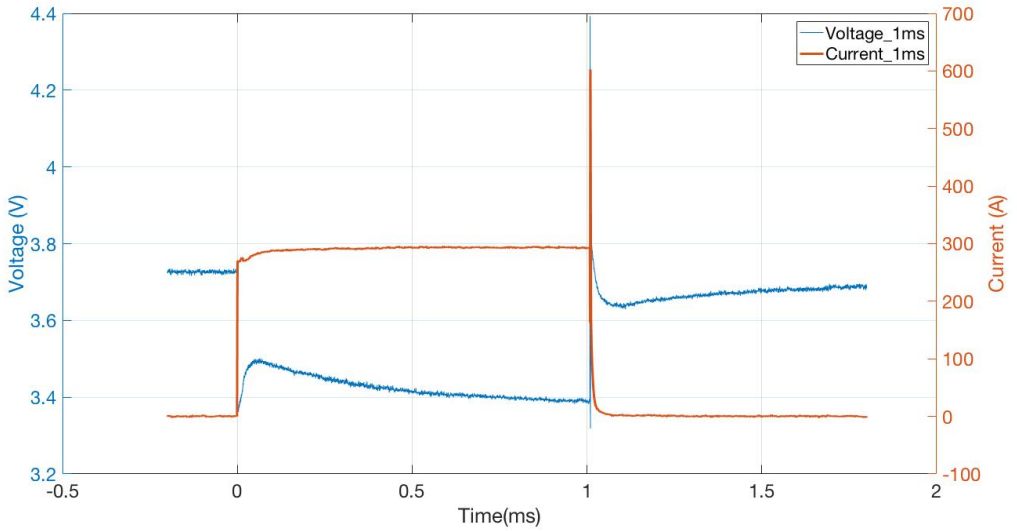


Figure 8.3: Cell terminal voltage and current pulse with 10C magnitude and 1 ms duration.

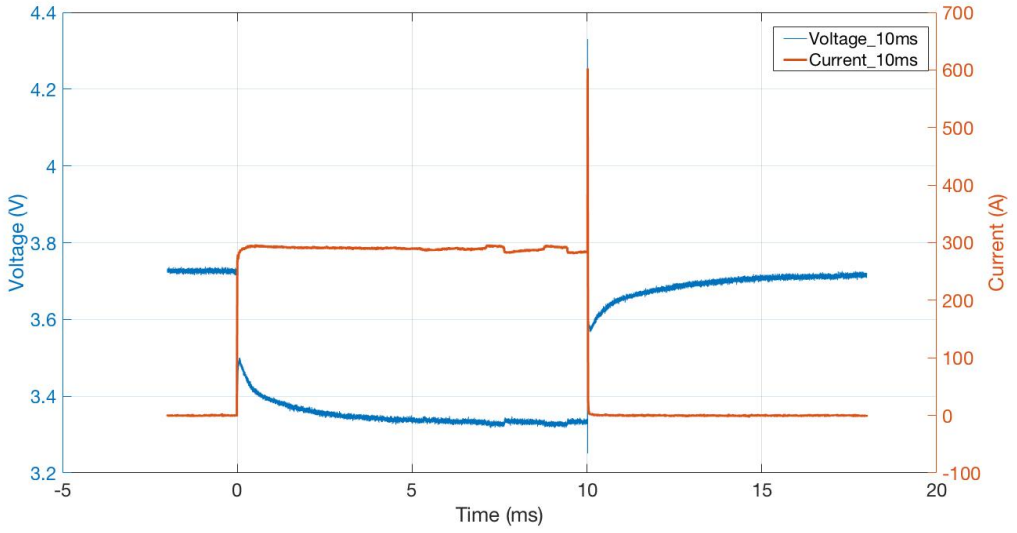


Figure 8.4: Cell terminal voltage and current pulse with 10C magnitude and 10 ms duration.

The resistor element in the test setup is replaced by the commercially available Arcol manufactured resistor 0.1 Ω and the test setup is shown in appendix Figure 11.2. This results in approximately 1C current magnitude in the circuit during discharge. The test is repeated for the same time duration like in 10C case. The repetition of the tests for 1C current is to compare and analyse the modelling of 10C with 1C for various time duration. The measured terminal voltage of the cell (V_t) for a current pulse with 1C magnitude and varying pulse duration of 10 µs, 100 µs, 1 ms and 10 ms are shown in Figures 8.5, 8.6, 8.7 and 8.8 respectively.

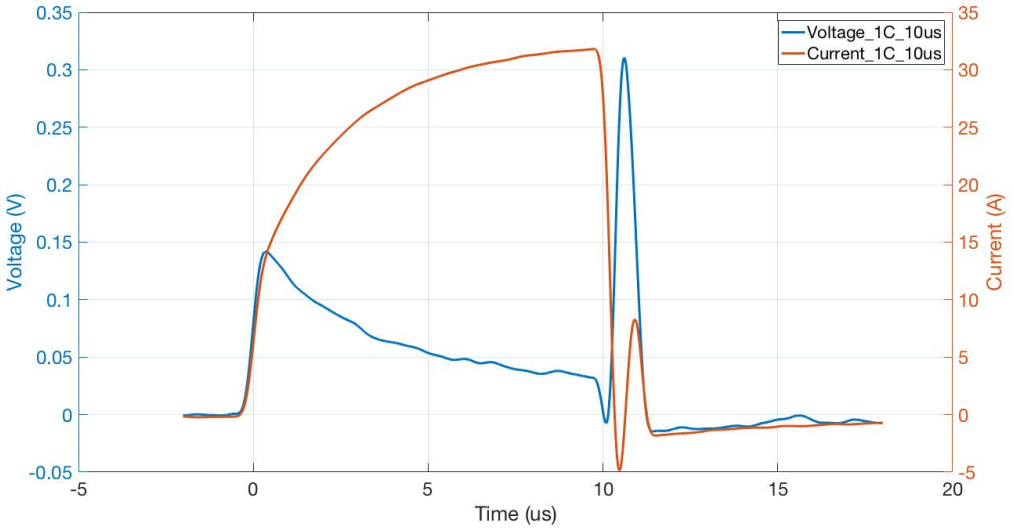


Figure 8.5: Cell terminal voltage and current pulse with 1C magnitude and 10 µs duration

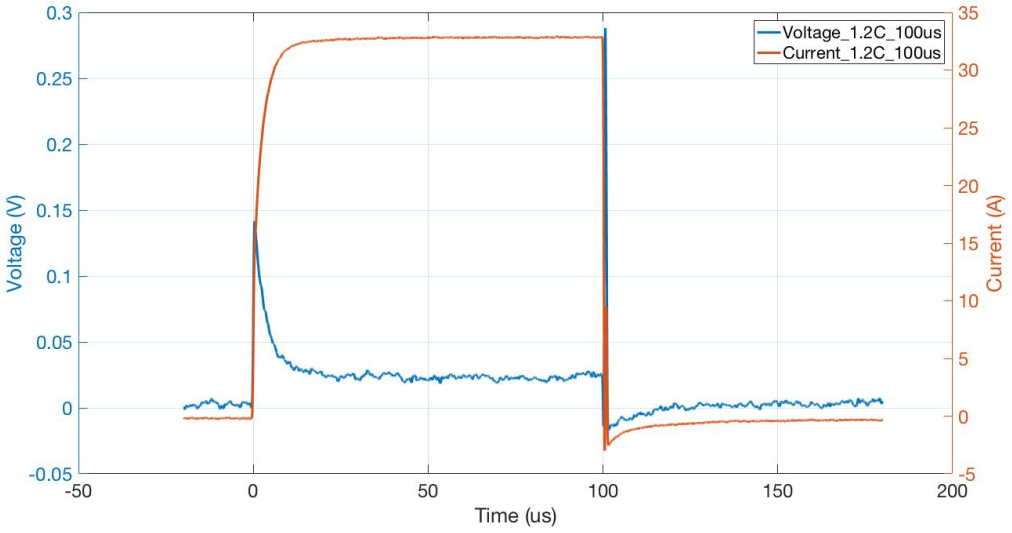


Figure 8.6: Cell terminal voltage and current pulse with 1C magnitude and 100 µs duration

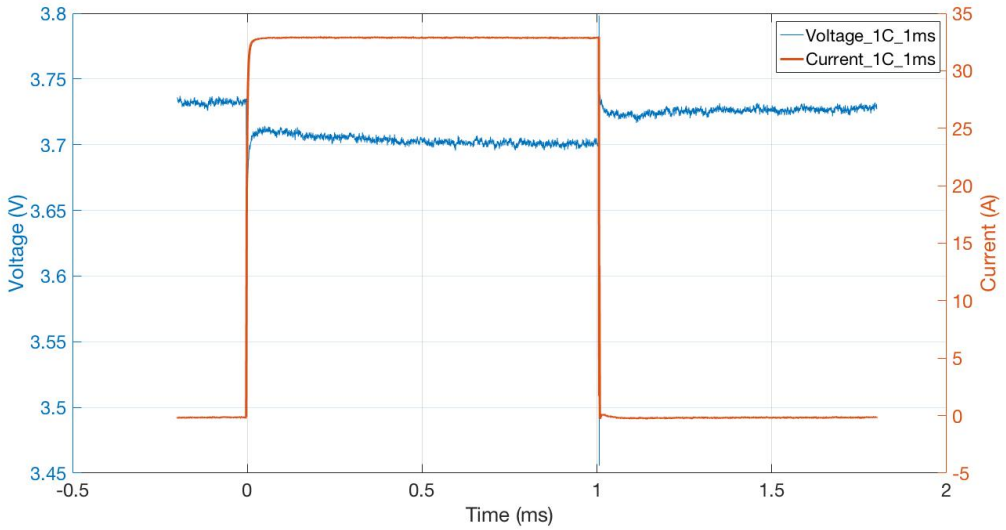


Figure 8.7: Cell terminal voltage and current pulse with 1C magnitude and 1 ms duration

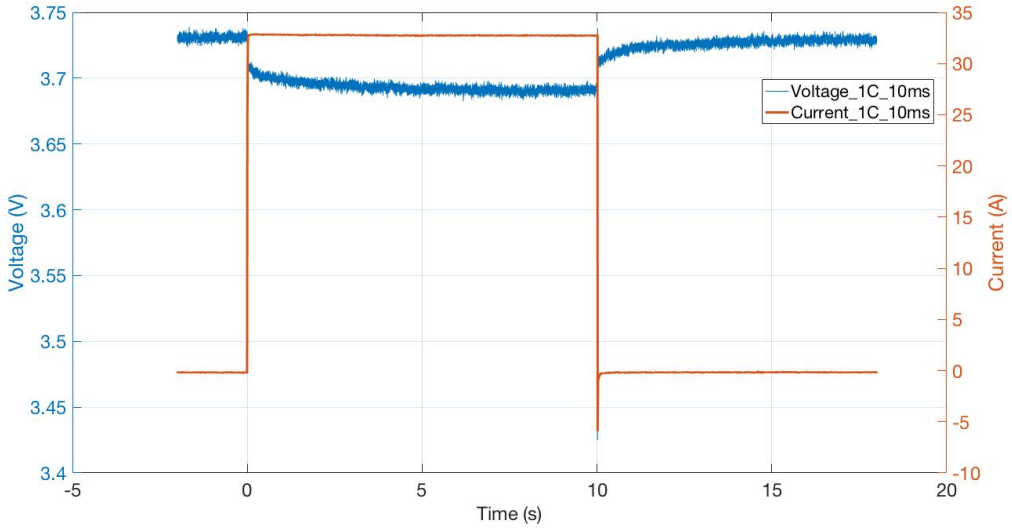


Figure 8.8: Cell terminal voltage and current pulse with 1C magnitude and 10 ms duration

From the Figures 8.1 - 8.8, the open circuit voltage (E) of the cell can be assumed to be battery terminal voltage just before the discharge pulse initiation (i.e. V_t at t=t_{on}^-). The internal voltage drop (E-V_t) in the cell is the difference between the open circuit voltage (E) and the cell terminal voltage (V_t). The two parameters (E-V_t) and I are fed into the System Identification application in MATLAB as input and output respectively [20]. By mentioning the number of zeros and poles, the transfer function can be obtained. The reciprocal of the transfer function gives the equivalent internal impedance (Z) in the cell. In order to compare the cell modelling for different current magnitudes, it is preferred to have minimum zeros and poles in the transfer function. This will be an advantage to realise the transfer function into a simple electrical circuit without much complexity as discussed in chapter 2.

Since the tested pulse widths are in µs and ms for both the current magnitudes, the transfer function is obtained to have one pole and no zero resembling like a series RL circuit as shown in Figure 2.2. This assumption is also valid from the observation during the relaxation study in chapter 4, the cell impedance is inductive for higher frequencies. Obtaining the transfer functions from system identification, the resulting R and L parameters in the cell for both the current magnitudes and for the time duration 10 µs, 100 µs and 1 ms respectively has been tabulated in Table 8.1. The results for 10 ms failed to fit in a RL circuit and the modelling of it will be discussed later this chapter.

Table 8.1: Value of R and L for different pulse duration and current magnitude

Pulse width	**Current = 10C**		**Current = 1.2C**	
	R (mΩ)	L (nH)	R (mΩ)	L (nH)
1ms	0.9697	8.65	1.083	5.4
100us	0.86258	9.8088	0.89061	11.512
10us	1.1	2.8969	3.2	18.688

An electrical circuit with the obtained parameters R and L from the table has been created in the Simulink. The corresponding (E-V_t) for different current magnitudes and

time duration respectively are fed as the input to the electrical circuit and the resulting current responses are obtained. Those responses are plotted against the respective measured current waveform and compared to validate the fitting of the model. The current responses of the models and measured responses for two current magnitudes (10C and 1C) for the time duration of 10 µs, 100 µs and 1 ms are shown in Figures 8.9 - 8.14 respectively.

The estimated resistance values in Table 8.1 is found to be approximately 1 mΩ. The deviation in the value of resistance for 1C and 10 µs case is due to the poor fitting of the measured results to the model as shown in Figure 8.12. Similarly the deviation in the inductance value for 1C and 10 µs case is evident from the measured current in which the current is rising during the discharge and hardly settling to a value. In general, the inductance values are in nH and the deviation in the 1C case is evident from the test setups in which the commercial resistor with the connection wires (1C case) contributed more stray inductance compared to the resistor made from the copper sheet (10C case).

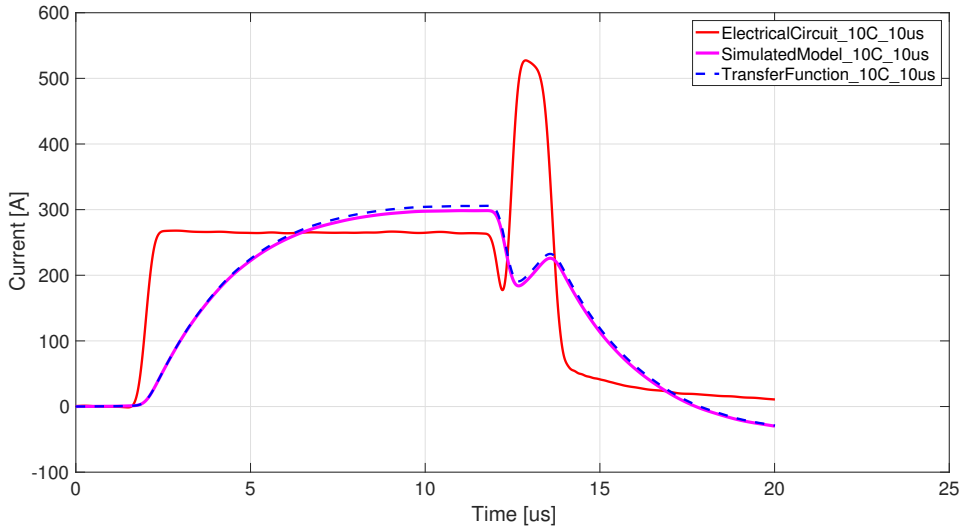


Figure 8.9: Measured current and response of the model for 10C current magnitude and 10us duration

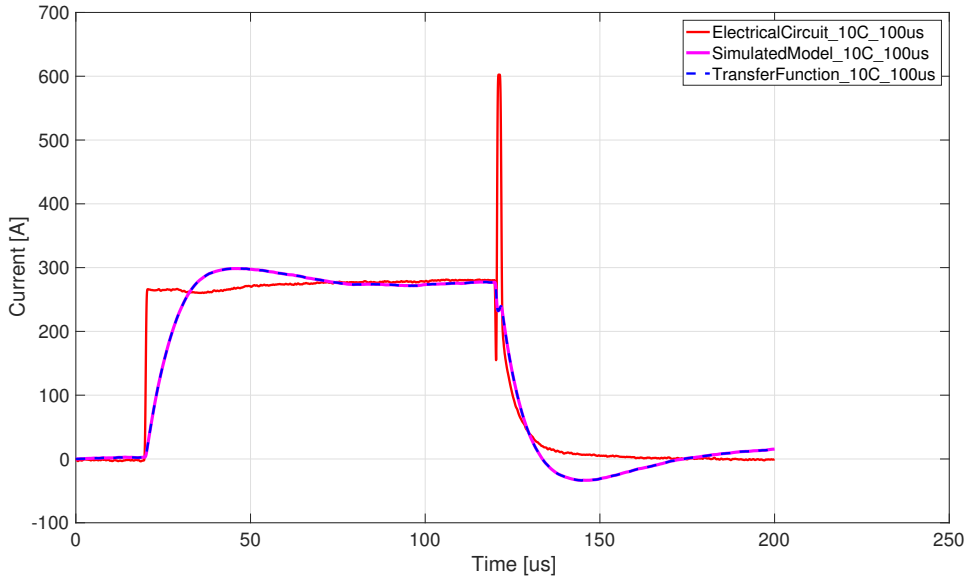


Figure 8.10: Measured current and response of the model for 10C current magnitude and 100us duration

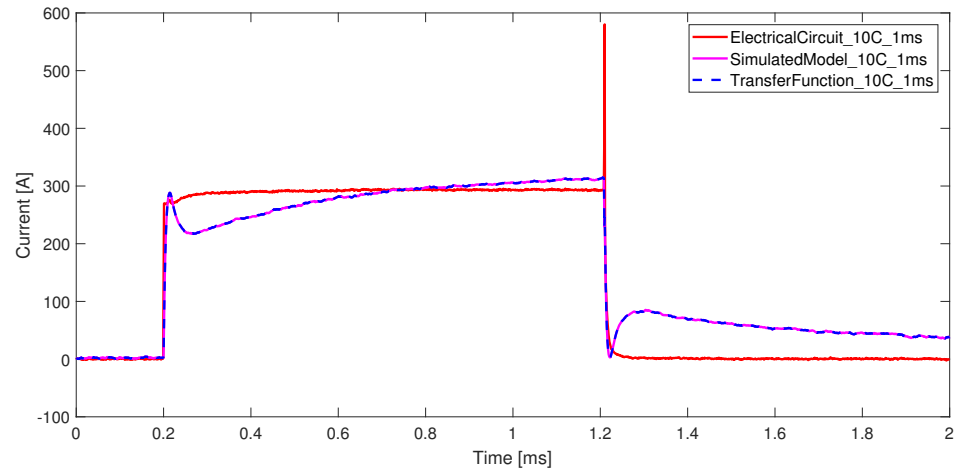


Figure 8.11: Measured current and response of the model for 10C current magnitude and 1ms duration

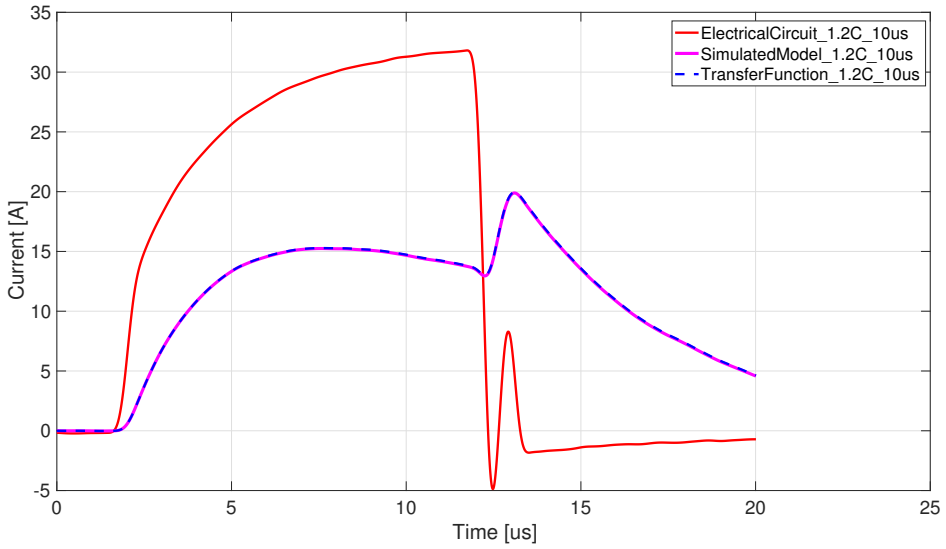


Figure 8.12: Measured current and response of the model for 1C current magnitude and 10us duration

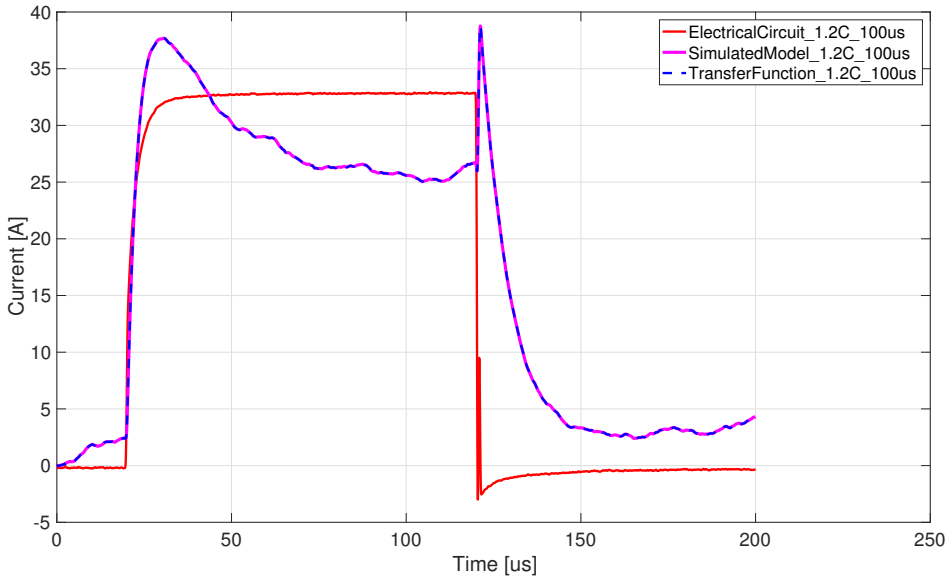


Figure 8.13: Measured current and response of the model for 1C current magnitude and 100us duration

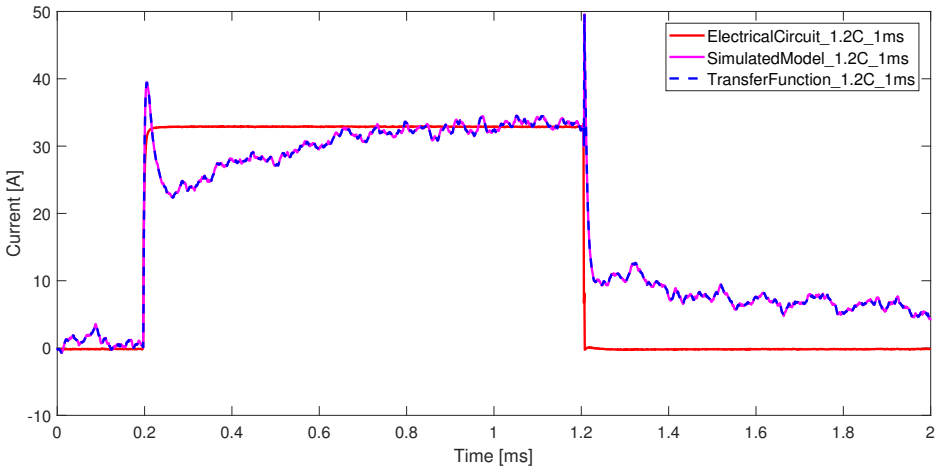


Figure 8.14: Measured current and response of the model for 1C current magnitude and 1ms duration

For 10ms case shown in Figures 8.4 and 8.8, fitting the data to a series RL circuit model failed in the system identification application. Instead, the data are fitted to a capacitive circuit model as shown in Figure 2.3. This is achieved by specifying the number of poles and zeros in transfer function to be one. The parameters R, R_1 and C are computed from the transfer function and has been tabulated in Table 8.2 for both the cases. An electrical circuit has been modelled along with the obtained parameters in the Simulink. The current response of the model is plotted against the measured current for both the current magnitude cases as shown in Figures 8.15 and 8.16 respectively.

The estimated resistance value R in the table is found to be approximately 1 mΩ. There is also an additional resistance R_1, hence Z_{real} in the modelled circuit increases. This is in accordance with the EIS study, as the frequency decreases further in the low frequency region, Z_{real} increases. Since the heat sink used in the developed test circuit could not handle the heat generated in switches due to 10C current magnitude for time duration greater than 10ms, the above phenomenon of Z_{real} increase could not be studied further in detail.

Table 8.2: Value of R, R_1 and C for 10ms pulse width and different current magnitudes

Pulse width	**Current = 10C**			**Current = 1.2C**		
	R (mΩ)	R_1 (mΩ)	C (F)	R (mΩ)	R_1 (mΩ)	C (F)
10ms	0.99	0.41	5.77	0.93	0.30	11.49

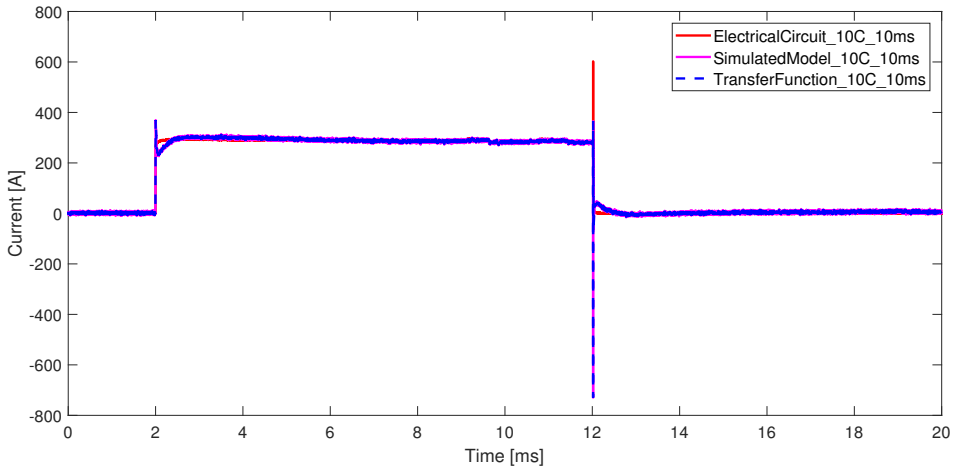


Figure 8.15: Measured current and response of the model for 10C current magnitude and 10ms duration

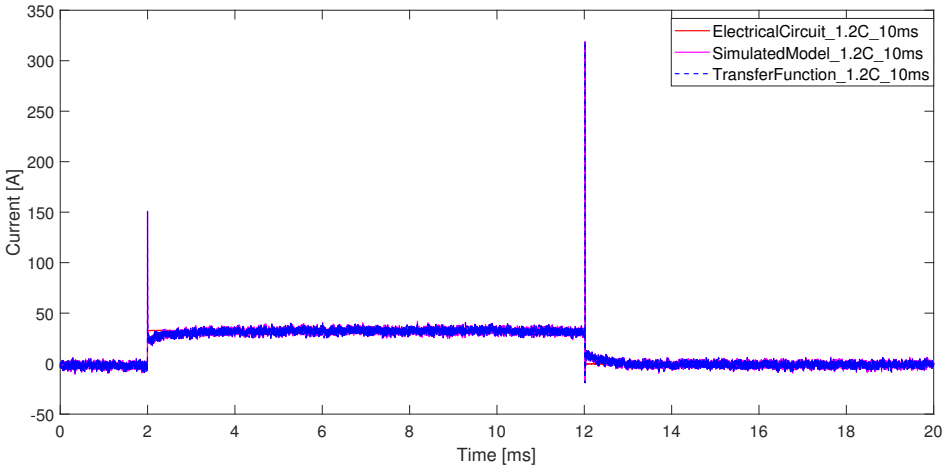


Figure 8.16: Measured current and response of the model for 1C current magnitude and 10ms duration

Chapter 9

Conclusion

The work was aimed at developing a large current pulse testing circuit according to the requirements. The designed test circuit has a high current range capability (up to 420 A) and a high frequency range capability (up to 100 kHz). The test circuit comprising MOSFETs and gate driver ICs along with an isolation between power and gate circuit was built in a printed circuit board (PCB). The current pulse width is set using an Arduino microcontroller. For the desired current magnitude, a resistor was designed using a copper sheet. The PCB, resistor and the complete test circuit connection was ensured to have as little inductance as possible.

The given cell was tested with different current magnitudes and time durations at a selected SOC and temperature; and the obtained measurements were parameterised accordingly to simple piecewise electrical equivalent circuit models. For the tested current magnitude cases, the cell internal impedance is inductive for current pulses with time duration less than or equal to 1 ms and capacitive for time duration greater than 1 ms. This is in accordance with the EIS results in which the impedance is inductive for higher frequencies and capacitive for lower frequencies. Hence, the developed test circuit can be used for the battery modelling of large current pulses.

9.1 Future work

Eventhough the pretests carried out in this thesis produced erroneous results because of misplacement of sensing probes in the test setup, the testing methods can be readily repeated to get accurate results. In the developed circuit board, there is a scope to improve the thermal cooling which will extend the circuit capability to test with time duration greater than 10 ms and also with a pulse train similar to EIS. Modelling can be further extended by conducting current pulse tests at different SOC levels and temperature. After the detailed and accurate cell modelling, the same test circuit can be used to test at module level.

Chapter 10

Bibliography

[1] Eurelectric, *Eurelectric-the benefits of electrification.* `http://www.eurelectric.org/media/189332/electrification_report_final-2015-030-0437-01-e.pdf`: Eurelectric, 2015.

[2] D. Helmersson, "Nationalencyklopedin, Hybridbil." `http://www.ne.se/uppslagsverk/encyklopedi/l%C3%A5ng/hybridbil`, 2016. Online: accessed 2016-11-10.

[3] M. Alaküla, *Hybrid Drive Systems for Vehicles: part 1 System Design and Traction Concepts.* Compendium, Lunds University of Technology, Lund, Sverige, 2006. Online: accessed 2016-11-17.

[4] several authors, *Systems perspecitve on electromobility.* Gothenburg, Sweden: Chalmers University of Technology, 2014.

[5] G. Park, B. Son, D. Kum, S. Lee, and S. Kwak, "Dynamic Modeling and Simulation for Battery Electric Vehicles under Inverter Fault Condition," *Scientific.net*, vol. 110-116, pp. 3007–3015, 2011.

[6] T. Doersam, S. Schoerle, E. Hoene, K. Lang, C. Spieker, and T. Waldmann, "High frequency impedance of li-ion batteries," *IEEE*, 2015.

[7] S. Casten, "How hard is it to integrate renewables into the grid?," *Grist*, 2013.

[8] Goals and visions, ""Energy Policy in Sweden"."

[9] A. Faiz, C. S. Weaver, and M. P. Walsh, *Air pollution from motor vehicles: standards and technologies for controlling emission.* Washington DC, USA: World Bank Publications, 1996.

[10] D.Larcher and J. Tarascon, "Towards greener and more sustainable batteries for electrical energy storage," *nature.com*, vol. Nature Chemistry 7, pp. 19–29, 2015.

[11] J. Gomez, R. Nelson, E. E. Kalu, M. H. Weatherspoon, and J. P. Zheng, "Equivalent circuit model parameters of a high-power li-ion battery: Thermal and state of charge effects," *Journal of Power Sources*, vol. 196, no. 10, p. 4826–4831, 2011.

[12] D. Andre, K. S. M. Meiler, H. Walz, T. Soczka-Guth, and D. Sauer, "Characterization of high-power lithium-ion batteries by electrochemical impedance spectroscopy. ii: Modelling," *Journal of Power Sources*, vol. 196, no. 12, pp. 5349–5356, 2011.

[13] S. Bullar, "Impedance based simulation models for energy storage devices in advanced automotive power systems," *publication-RWTH*, 2002.

[14] S. David, "Pulse power characterisation for lithium ion cells in automotive applications: Small and large signal cell impedance analysis," 2016.

[15] A. Rahmoun and H. Biechl, "Modelling of li-ion batteries using equivalent circuit diagrams," *Electrical review*, no. ISSN, pp. 0033–2097, 2012.

[16] Gamry, *Gamry Instruments Reference 3000 Potentiostat/Galvanostat/ZRA Operators manual.* `http://www.gamry.com/assets/Uploads/Reference-3000-Operators-Manual.pdf`: Gamry instruments, 2015.

[17] Y. Xing, W. He, M. Pecht, and K. L. Tsui, *State of charge estimation of lithium-ion batteries using the open-circuit voltage at various ambient temperatures.* 2013.

[18] Z. Geng and C. Savvidis, "On-board impedance diagnostics method of Li-ion traction batteries using pseudo-random binary sequences. Method evaluation and feasibility study of concept," 2015.

[19] J. Groot, "State-of-health estimation of li-ion batteries: Cycle life test methods," 2012.

[20] MATLAB, *System identification toolbox.* `https://se.mathworks.com/help/ident/?requestedDomain=www.mathworks.com`: Mathworks, 2017.

Chapter 11

Appendix

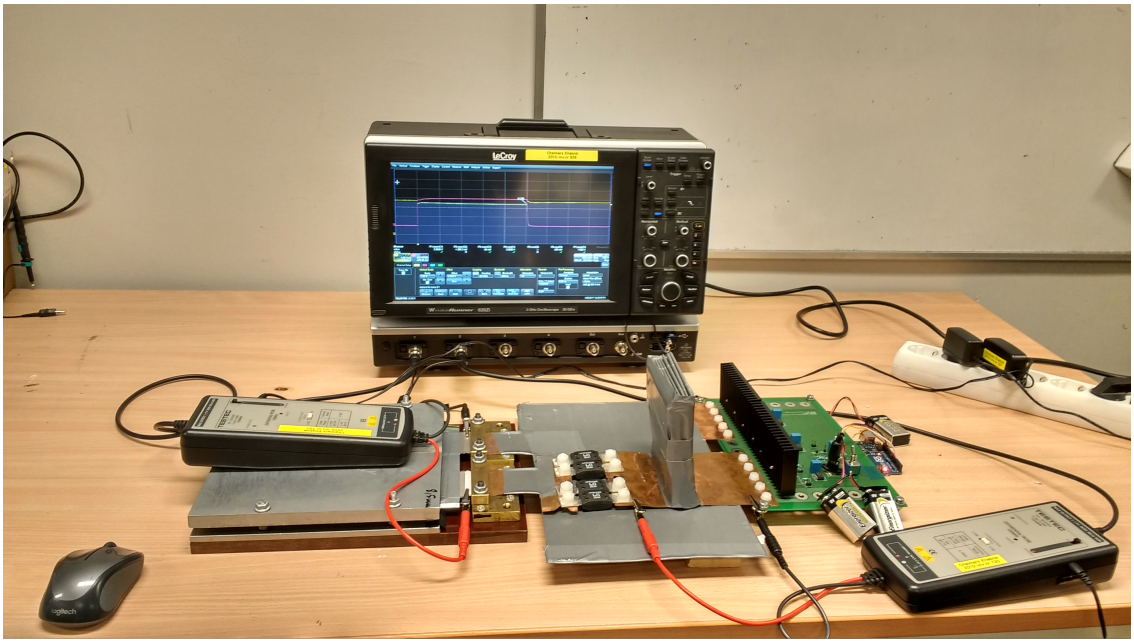


Figure 11.1: Current pulse testing circuit with a resistor that generates current pulse of 10C magnitude

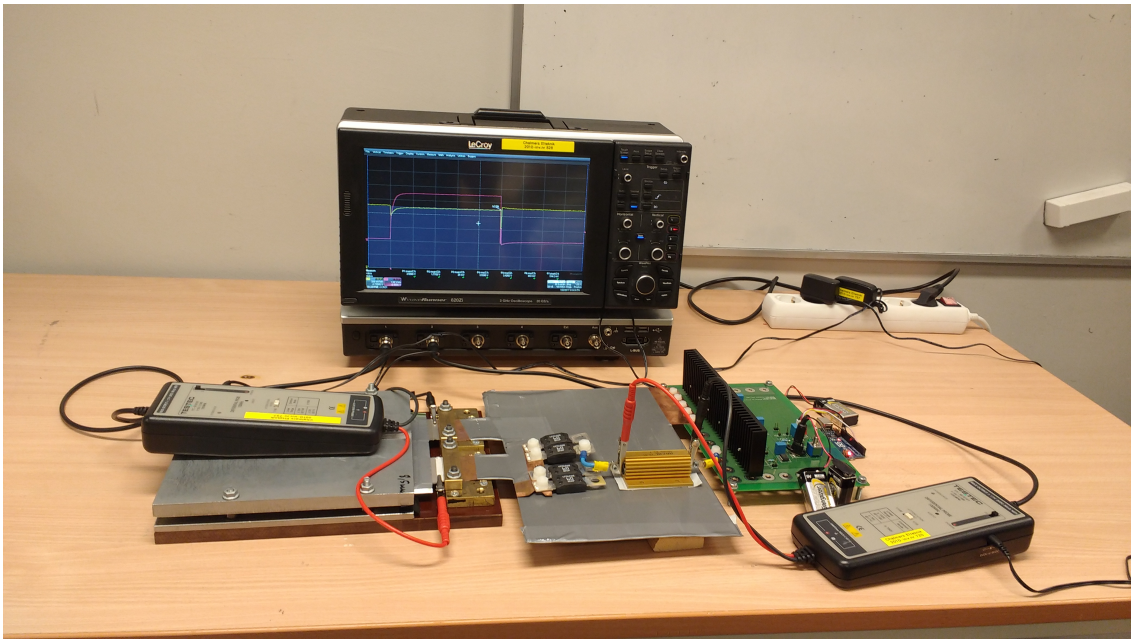


Figure 11.2: Current pulse testing circuit with a resistor that generates current pulse of 1C magnitude