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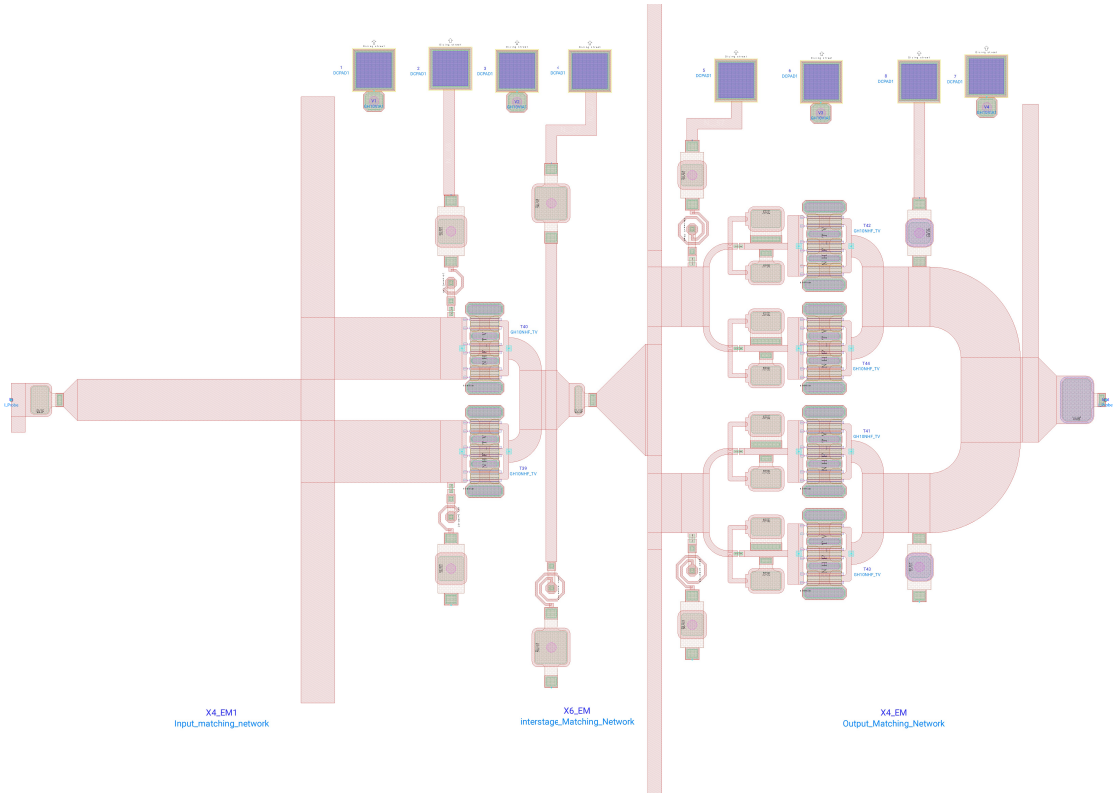

Design and Evaluation of Efficient Power Amplifier Architectures for Millimeter-Wave 5G Backhaul Applications

Master's thesis in Embedded Electronic System Design

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Cover: Final layout of MMIC power amplifier presentted in this thesis.

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Abstract

The rapid global rollout of 5G mobile communications has put a great strain on millimeter-wave backhaul infrastructure, requiring power amplifiers (PAs) with high output power, high efficiency, and wide bandwidth. This thesis presents the design and simulation evaluation of an efficient Class AB power amplifier for 5G point-to-point backhaul links in the 37–40 GHz band. The design is implemented using the United Monolithic Semiconductors GH10-10 Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) process design kit in the Keysight Advanced Design System simulation environment.

The methodology makes use of a two-stage cascaded architecture with a driver stage and a four-transistor parallel power amplifier stage. To bridge the gap between the theoretical performance and physical realization, the design incorporates the electromagnetic (EM) model-based layouts for the input, interstage, and output matching networks. The integrated *RC* stabilization networks were also optimized to suppress low-frequency and out-of-band instabilities, which are common in high-gain GaN devices.

The final EM-realized MMIC simulation results show a saturated output power of 34.6 dBm (2.9 W) at 37 GHz and 33.15 dBm at 40 GHz. The design exhibited a peak Power Added efficiency (PAE) of 25.93% and 10 dB output power back-off PAE of $\sim$ 5%. The small-signal performance shows gain (S_{21}) ranges between 11.3 dB and 12.1 dB over the bandwidth and an input return loss (S_{11}) better than 13.6 dB. The final MMIC is found conditionally stable from 1 to 50 GHz with Rollett stability factor also using advanced stability verification with Ohtomo loop gains and Kurokawa driving-point admittance. The results validate the effectiveness of GaN HEMT technology to construct robust and energy efficient transmitter front-ends for next-generation 5G backhaul infrastructure. These results are lower than the design goal and can be improved in future work by adding an additional driver stage or by increasing the total gate periphery of the driver-stage transistors to provide a higher drive capability. Such changes would require re-design of the matching networks to compensate for increased device parasitics.

Keywords: Power Amplifier, GaN HEMT, Class AB, MMIC, Keysight ADS, EM Co-Simulation, PAE, Impedance Matching, Power Combiner, Microstrip, Stability.

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1

Introduction

The rollout of 5G mobile communications has significantly increased data traffic in backhaul microwave and millimeter wave (mmW) networks. The increased number of units needed to cover this traffic at mmW puts a requirement of cost-effective solutions on the whole product and with high focus on the specific component generating the Radio Frequency (RF) power in the transmitter, the Power Amplifier (PA). The PA is an important part of the system. This is due to its direct impact on power consumption and environmental impact. Advances in Gallium Nitride (GaN) transistor technology for the PA has the possibility together with the design technique of PA to reduce system footprint and operating costs in future products to transport 5G and 6G data traffic.

The purpose of the thesis is to identify critical blocks needed to design an efficient PA for mmW frequencies. Key specifications for a PA in a point-to-point link are a high saturated output power, high DC-to-RF power efficiency both at peak power and when the power is backed-off, high gain, and low cost. At mmW frequencies, fulfilling these requirements becomes challenging since most commercially available semiconductor integrated circuit processes at these frequencies either offer low gain or operate only at low voltages. This necessitates either large power combining networks or many amplifier stages, both of which increase chip size and, therefore, the cost, while incurring power losses that limit the output power and efficiency. However, several foundries have high-frequency GaN processes in development that offer higher voltage operation combined with high gain at mmW frequencies.

Although many foundries have high frequency GaN processes under development, the United Monolithic Semiconductors (UMS) GH10-10 GaN HEMT process is being used in this project, which was already selected for this design by Ericsson before the start of this thesis. The goal of the project is to leverage this new process in combination with design techniques for high efficiency PAs to enable improved output power in point-to-point links with similar or lower power consumption compared to today's products. Although this problem is relevant throughout the mmW range from 18 GHz to 86 GHz, the plan for this project is to focus on designing a PA for the bands from 37 GHz to 40 GHz.

1.1 Related Work

Recent developments in mmW GaN PAs have shown optimistic results for 5G and evolving 6G systems. Wang et al. pointed out the high dynamic range and multi-Watt-level PAs enabled by innovative mmWave PA concepts[1]. Additionally, Giofrè et al. demonstrated a 28 GHz GaN Doherty MMIC with good load-modulated efficiency, applicable to multi-band/ multimode base stations [2]. Furthermore, Quaglia et al. have shown that associated GaN MMIC amplifiers can linearize and increase the output power for microwave backhaul links [3]. Recently, Sweeney et al. reported a wideband Watt-level GaN PA with high-efficiency performance throughout the band, thus proving that GaN is a strong candidate for robust and cost-effective 5G front ends [4]. Despite these significant efforts, some major challenges remain, including broadband matching, thermal issues, and power combining efficiency. Conventional methods such as Doherty and outphasing are more challenging to implement at mmW frequencies due to higher loss and complexity. In this context, we motivate the study of transistor selection, matching networks, and power combining strategies for simulation-generated tradeoffs to refine next generation PA performance.

1.2 Purpose and Goal

The overall goal is to design, evaluate and optimize key PA building blocks that enable efficient Watt-level output power at millimeter-wave frequencies for 37-40 GHz for 5G backhaul links using UMS GH10-10 GaN HEMT process. This project aims to contribute to energy-efficient, high-capacity mmW backhaul. The output of the project will enable more economical and sustainable network roll-outs in 5G and beyond.

The specific objective is to use proven GaN models and circuit-plus-EM simulation to design, assess, and optimize three important PA sub-blocks: device selection/sizing, input/output matching, and compact power combiners. The target of this project is to achieve following goals for the selected frequency band:

1. Small-signal gain $>$ 20 dB.
2. Power added efficiency $>$ 15% At 10 dB output power back-off.
3. Output power $>=$ 5 W (37 dBm).

1.3 Thesis Outline

The thesis is structured in six chapters, which lead from the theoretical basis to the final electromagnetic realization and evaluation of the power amplifier.

- Chapter 1 presents the infrastructure requirements for 5G backhaul point to point links and defines the technical performance targets for the power amplifier design.

- Chapter 2 presents the technical background covering the physics of GaN HEMT technology, operating classes, impedance matching theory and distributed transmission line principles for millimetre-wave design.
- Chapter 3 details the methodology used for the simulation. The Keysight Advanced Design System (ADS) environment, UMS GH10-10 Process Design Kit (PDK) transistor model and DCIV characterization and load-pull analysis procedures are presented.
- Chapter 4 discusses the design and realization of the power amplifier. It describes the two-stage cascaded architecture, with the driver stage built of two parallel HEMTs, and the final power stage based on a parallel four-transistor topology. In this chapter the synthesis of the input (IMN), interstage (ISMN) and output (OMN) matching networks is discussed starting from ideal schematic stubs and going towards physical EM-model integrated top-level layouts.
- Chapter 5 describes the complete results of the simulations. This chapter reports load-pull characterization for the driver and power stages, small-signal parameters (S-parameters, gain, and Rollett stability), large-signal performance (output power, PAE, and gain compression), and advanced stability analysis using Ohtomo loop gains and Kurokawa driving-point admittance.
- Chapter 6 conclude and summarizes the performance indicators obtained, reviews the findings on conditional instability, and outlines the future improvements for further improvement in gain and power added efficiency and design optimization.

2

Technical Background

The theoretical background and technical principles required for the design and analysis of high-frequency power amplifiers are presented in this chapter. The chapter begins with an overview of GaN HEMT technology, highlighting its high power density, wide bandgap, and suitability for millimeter-wave applications. It then introduces the various power amplifier operating classes, with particular emphasis on the efficiency, linearity trade-offs of Class AB operation, which forms the basis of this work.

The chapter further discusses the fundamentals of impedance matching, including the Bode-Fano bandwidth limit and the practical use of the Smith chart for impedance matching network synthesis. The analytical framework required to transform target impedances into physical matching networks is presented alongside essential microwave engineering concepts, including scattering parameters (S-parameters), distributed transmission-line theory, and large-signal load-pull analysis.

Finally, the chapter addresses microstrip discontinuities and parasitic effects to ensure that the transition from ideal schematic design to physical layout accounts for the electromagnetic complexities inherent to 40 GHz.

2.1 Radio Frequency Power Amplifiers

An RF power amplifier is an active two-port electronic circuit that takes a low-power RF input signal and sends a much stronger version of that signal to a load, which is usually a 50 Ω antenna or transmission system. PAs are made to work close to or in the nonlinear saturation region of the transistor so that they can get the most output power with the least amount of energy used. The behavior of a PA is determined by both small-signal linear network theory and large-signal nonlinear device physics. This makes PA design one of the most technically challenging fields in RF and microwave engineering.

There are a few key figures of merit that are important to know for the power amplifier. These figures show how well the amplifier works. P_{out} (output power) is the total RF power sent to the load at the fundamental frequency. It is usually measured in dBm or Watts. In decibels, power gain (G) is the ratio of output power to input power. Power Added Efficiency (PAE) shows how well DC power is converted to RF output power. The 1dB compression point ($P1dB$) is the input power level at which the output power gain of a device is 1 dB less than the linear

(small-signal) gain, which is also the start of nonlinear behavior where the device starts to saturate. These parameters are interdependent; enhancing one frequently compromises another, and it is the designer's responsibility to identify the optimal trade-off considering the transistor technology and system specifications [5].

The following basic equations show how these important parameters are related to each other. The power gain of a transducer is defined as:

$$G_T = \frac{P_{\text{out}}}{P_{\text{available,source}}} \tag{2.1}$$

In decibels it is $G_{T,dB} = P_{\text{out,dBm}} - P_{\text{in,dBm}}$. The Power Added Efficiency is calculated as:

$$PAE = \frac{P_{\text{out,RF}} - P_{\text{in,RF}}}{P_{DC}} \times 100\% \tag{2.2}$$

where $P_{DC} = V_{DD} \times I_{DD}$ is the total DC power drawn from the supply.

2.2 GaN High Electron Mobility Transistor (HEMT) Technology

GaN semiconductor devices, especially GaN high-electron-mobility transistor (HEMT) devices, are widely used in high frequency integrated circuits for transmission and reception due to their excellent properties of electron mobility characteristics. These circuits can be stable at high frequencies and high power operation, responding to the growing demands of radio and telecommunication applications. This field is actively researched In particular, GaN semiconductor devices are emerging as the only high-frequency power semiconductors suitable for use in semiconductor-based solid-state power amplifiers (SSPAs) replacing the vacuum tube-type traveling wave tube amplifiers (TWTAs) used in the past for military applications [6]. It is also the active device used in this design through the UMS-GH10-10 process [7].

The HEMT is a type of field-effect transistor that has a channel that forms at the interface between two semiconductor materials with different band-gap energies; in this case between an AlGaN (aluminum gallium nitride) barrier layer and a GaN buffer layer. Because of the piezoelectric and spontaneous polarization effects at this heterojunction, a high concentration of electrons builds up at the interface, even without intentional doping. This creates a two-dimensional electron gas (2DEG) [8].

This 2DEG acts as the conducting channel and possesses:

- Very high electron mobility: typically $1500\,\text{cm}^2/\text{V}\cdot\text{s}$ to $2000\,\text{cm}^2/\text{V}\cdot\text{s}$.
- High sheet charge density: typically $10^{13}\,\text{cm}^{-2}$.

Together, these two properties give GaN HEMTs high-frequency and high-power performance. The main material properties that make GaN HEMTs superior to other transistor technologies for power amplifier applications include:

- Wide band gap energy: 3.4 eV (compared to 1.1 eV for Si and 1.42 eV for GaAs).
- High critical breakdown field: approximately 3.3 MV/cm.
- High electron saturation velocity: approximately 2.5×10^7 cm s^{-1}.

The wide band-gap allows for operating voltages much higher than those for GaAs-based devices. For example, the UMS GH10-10 process utilizes drain bias voltages (V_{DD}) of 13 V to 15 V. Higher voltage operation leads to higher output power density because the maximum output power is directly related to the product of voltage and current swing.

Table 2.1: Power Density Comparison

Technology	**Power Density (W/mm)**
GaN HEMT	4 – 10
GaAs pHEMT	0.5 – 1

Power density is the RF output power generated per unit total gate width of the transistor and is expressed in W/mm.

From table 2.1, GaN HEMTs have much higher power density (4–10 W/mm) compared to GaAs pHEMTs (0.5–1 W/mm). This makes GaN a good candidate for high-power Millimeter-wave applications.

To understand how to design a matching network, it is important to know how to use a small-signal equivalent circuit model of a HEMT. The gate-source capacitance (C_{gs}) stores charge in the channel below the gate; the gate-drain capacitance (C_{gd}) gives internal feedback from output to input; the drain-source resistance (R_{ds}) models the finite output conductance; and the transconductance (g_m) relates the drain current to gate voltage as below:

$$i_D = g_m \cdot v_{gs} \tag{2.3}$$

The current gain cutoff frequency (f_T) and the highest frequency of oscillation (f_{max}) are the two most important high-frequency figures of merit:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2.4}$$

$$f_{max} = \frac{f_T}{2\sqrt{(R_g + R_s + R_i) \cdot g_{ds} + 2\pi f_T \cdot R_g \cdot C_{gd}}} \tag{2.5}$$

For the UMS GH10-10 process, the frequency (f_T) is usually around 40 GHz, and the frequency (f_{max}) is more than 100 GHz. This is why this process can give useful gain at 37–40 GHz. The gate length of 0.1 μm in GH10 is very important to obtain these frequency figures of merit because (f_T) scales roughly inversely with the gate length.

2.3 Power Amplifier Operating Classes

The conduction angle of a transistor, which indicates which portion of the RF cycle the transistor conducts drain current, determines the operating class of a power amplifier (Class A, AB, B, C). This classification is fundamental for understanding the trade-off between efficiency and linearity in PA design [9]. It also establishes the DC bias point from which the amplifier operates. Conduction angles for each class are shown in figure 2.1 [10].

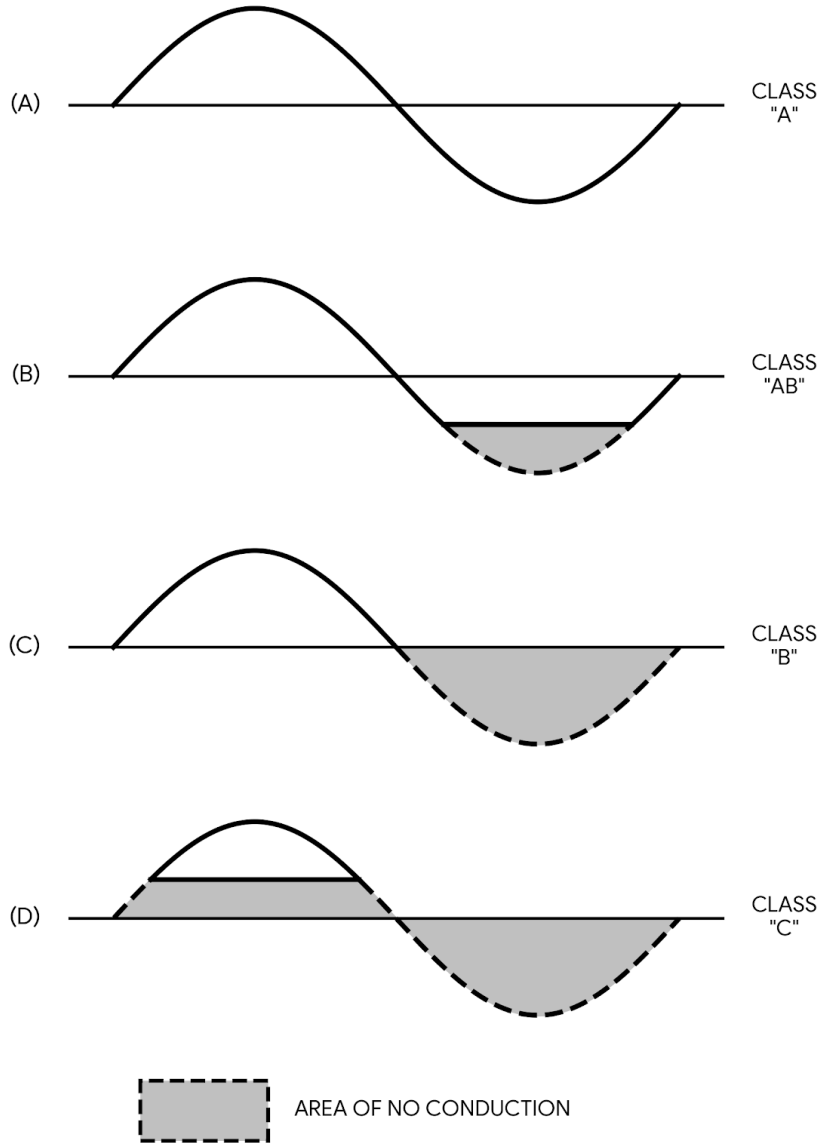


Figure 2.1: PA operating classes with conduction angles

2.3.1 Class A and Class B Operation

A conduction angle of 360° defines the Class A operation as shown in figure 2.1. In this mode, the transistor conducts a drain current for the entire RF cycle. The DC

bias point is set in the middle of the load line, between pinch-off and saturation. Class A amplifiers are naturally linear because the transistor remains in its active region; however, they achieve a theoretical maximum drain efficiency (η_D) of only 50 %. In practical GaN PA applications, efficiencies typically range between 30 % and 40 %.

In Class B operation, the DC bias is set at the pinch-off threshold, resulting in a conduction angle of 180° (half the cycle) as shown in figure 2.1. In ideal Class B amplifiers, the drain current is half-wave rectified (multiple harmonics), but the output matching network shorts all harmonics (odd and even) so only the fundamental is presented to the load as a perfect sine wave. In fact, real transistors have gradual (not sharp) pinch-off characteristics and matching networks cannot completely eliminate all harmonics, resulting in some residual distortion and an efficiency slightly below the theoretical 78.5% maximum drain efficiency.

2.3.2 Class AB Operation

The conduction angle for Class AB is between 180° and 360° as shown in figure 2.1. The DC bias is set slightly higher than the pinch-off voltage, typically at a drain current (I_D) that is 10 % to 20 % of the maximum saturation current (I_{DSS}).

Class AB is the most widely used operating class for communication systems because it is more efficient than Class A (with a theoretical maximum between 50 % and 78.5 %) while maintaining better linearity than Class B [11].

2.3.3 Class C Operation

In a Class C amplifier, the DC bias point is set below the pinch-off threshold, resulting in a conduction angle of less than 180° (typically between 90° and 150°) as shown in figure 2.1. Consequently, the transistor conducts for less than half of the RF input cycle, producing a drain current waveform consisting of narrow current pulses with significant high-order harmonic content.

Due to this highly non-linear operation, a high-Q resonant tank circuit is required at the output to suppress harmonics and reconstruct the desired sinusoidal waveform. As the conduction angle decreases, the overlap between the drain voltage and drain current is reduced, thereby minimizing power dissipation within the transistor.

In theory, the drain efficiency (η_D) of a Class C amplifier approaches 100% as the conduction angle approaches zero. However, this improvement in efficiency is accompanied by a substantial reduction in gain and output power capability, making Class C amplifiers most suitable for applications involving constant-envelope signals, such as RF transmitters, where high efficiency is a primary requirement.

2.4 Impedance Matching and Network Design

Impedance matching is the process of designing a reactive network to transform the impedance of a source or load to a target value. In PA design, impedance matching serves two primary goals:

- Input Matching Network (IMN): Transforms the 50 Ω source impedance into the complex conjugate of the transistor's input impedance to maximize power delivery.
- Inter-stage Matching Network: To maximize power transfer between stages and increase the gain.
- Output Matching Network (OMN): Transforms the optimal load impedance (Z_{opt}) determined by Load-Pull simulation into the 50 Ω load impedance to connect outside blocks of PAs [12].

2.4.1 Maximum Power Transfer and Reflection

The Maximum Power Transfer Theorem states that maximum power is delivered from a source with impedance Z_S to a load Z_L when:

$$Z_L = Z_S^* \tag{2.6}$$

where the asterisk indicates the complex conjugate. The reflection coefficient (Γ) in any port is defined as:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.7}$$

where Z_0 is the reference impedance (typically 50 Ω). Return Loss (RL) expressed in decibels is:

$$RL = -20 \log_{10} |\Gamma| \quad \text{dB} \tag{2.8}$$

For example, if $S_{11} = -21.83\,\text{dB}$ at 37.5 GHz, the reflection coefficient magnitude is:

$$|\Gamma| = 10^{\frac{-21.83}{20}} \approx 0.081 \tag{2.9}$$

This indicates that only 0.65 % ($|\Gamma|^2 \times 100\%$) of the incident power is reflected.

2.4.2 The Bode-Fano Limit

The **Bode-Fano limit** establishes a fundamental theoretical bound on the bandwidth of an impedance matching network [13]. For a parallel RC load, the limit is expressed as:

$$\int_0^\infty \ln \frac{1}{|\Gamma(\omega)|} d\omega \leq \frac{\pi}{R_s C_p} \tag{2.10}$$

This limit demonstrates that for a given load Q-factor, the matching bandwidth and the minimum reflection coefficient are inversely related. Consequently, achieving broadband matching with low reflection requires complex matching topologies with multiple reactive sections. At millimeter-wave frequencies, lumped-element networks are impractical; therefore, this design utilizes distributed microstrip transmission line sections for all matching stages.

2.4.3 Smith Chart

The Smith chart is used to match circuit designs and it provides a graphical representation of the consecutive matching design procedure. The Smith chart can be used for matching using either lumped elements or transmission lines [14]. The Smith chart shown in the shown in figure 2.2 is especially useful for matching circuit designs that use transmission lines, as the analytical calculation becomes very complicated in this case [15]. In addition, the complete Smith chart can be utilized to directly calculate all the circuit parameters such as VSWR, reflection coefficient, return loss or losses in the transmission line.

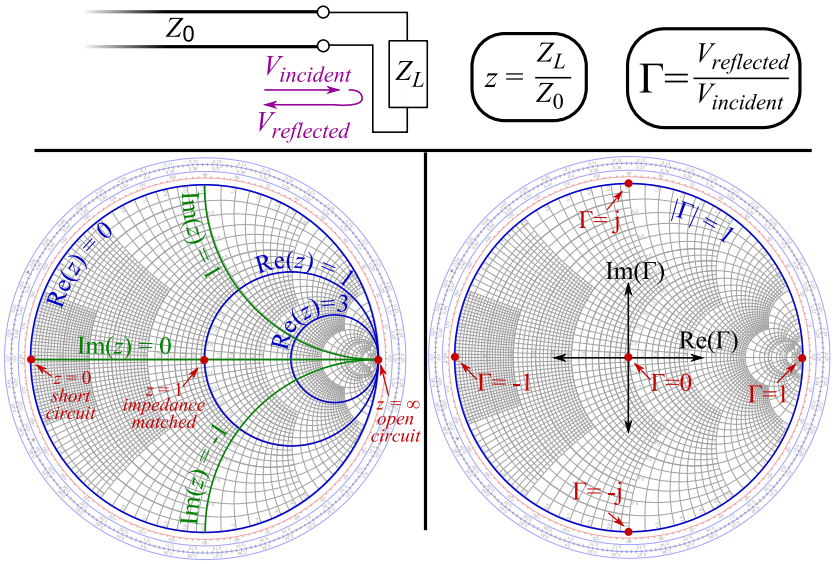


Figure 2.2: Smith chart

The Smith chart is a graph of the relationship between the load impedance Z and the reflection coefficient given by eq. 2.7.

2.5 Scattering Parameters (S-parameters)

At RF and microwave frequencies, Scattering parameters (S-parameters) are the standard method for describing linear two-port and multi-port networks [16]. Unlike the Impedance (Z) and the Admittance (Y) parameters, which require open-circuit or short-circuit terminations that are difficult to achieve at high frequencies, the S-parameters are measured with all ports terminated in a reference impedance (typically 50 Ω). This makes them easily measurable using a Vector Network Analyzer (VNA).

The S-parameter matrix relates the complex amplitudes of the incident waves (a) and the reflected/outgoing waves (b) at each port:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.11}$$

The physical definitions of the parameters are as follows:

- S_{11}: Input reflection coefficient (Input return loss).
- S_{21}: Forward transmission coefficient (Gain).
- S_{12}: Reverse transmission coefficient (Isolation).
- S_{22}: Output reflection coefficient (Output return loss).

2.5.1 Impedance Transformation and Power Gain

The bilinear transformation is used to convert the measured reflection coefficient into the input impedance:

$$Z_{\text{in}} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{2.12}$$

Power quantities are also derived directly from these parameters. The available power gain (G_A) is defined as:

$$G_A = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)}{1 - |S_{11}|^2} \tag{2.13}$$

Under perfectly matched conditions, the transducer gain (G_T) simplifies to:

$$G_T = |S_{21}|^2 \tag{2.14}$$

In this design, an S_{21} of approximately 10 dB corresponds to a power amplification factor of:

$$|S_{21}|^2 = 10^{\frac{10}{10}} = 10 \tag{2.15}$$

This represents a ten-fold increase in power. The S-parameters also allow for direct stability analysis [5].

2.6 Network Stability in High-Frequency Circuits

In RF and microwave engineering, network stability signifies that an active circuit, such as a transistor power amplifier, performs its intended function without breaking into parasitic or unintended oscillations. When the net resistance of a system is negative, the system oscillates, and transient signals grow exponentially instead of decaying. The stability of a typical two-port network connected to the source impedance (Z_S) and load impedance (Z_L) is determined by evaluating the input and output reflection coefficients, Γ_{in} and Γ_{out}. The network is globally stable if the absolute values of these coefficients are strictly less than one:

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2.16}$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{2.17}$$

If these conditions are satisfied for all geometrically allowed passive terminations ($|\Gamma_S| \leq 1$ and $|\Gamma_L| \leq 1$), the network is said to be unconditionally stable. If these conditions are met only in some regions of the Smith chart, the network is conditionally stable.

The classical Rollett stability criterion, as defined by the K-factor, along with the auxiliary delta metric (Δ), is used to globally evaluate traditional linear, two-port unconditional stability. It can be rigorously proved that a two-port network is unconditionally stable if the following simultaneous conditions are satisfied:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.18}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.19}$$

Alternatively, this can be summarized in a single mathematically rigorous parameter, the Edwards-Sinsky parameter (μ), for which unconditional stability requires $\mu > 1$:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \tag{2.20}$$

The K-factor is a great mathematically sound binary measure for simple isolated two-port systems, but it is a complete black box. It does not illustrate internal node oscillations, multi-stage transistor interactions, or non-linear behaviors under large-signal driven states [17].

To overcome these basic limitations in nonlinear active circuits, the Kurokawa stability check is used to examine the dynamic driving-point admittance (Y) or impedance (Z) of the network. Kurokawa's theory, originally developed to model microwave power combiners and solid-state oscillators, determines whether a dynamic operating point (or orbital limit cycle) is able to successfully recover from small amplitude (δA) and frequency ($\delta\omega$) perturbations. The complex interface between the active device impedance, $Z_D(A,\omega) = R_D(A,\omega) + jX_D(A,\omega)$, and the passive load impedance, $Z_L(\omega) = R_L(\omega) + jX_L(\omega)$, must be matched ($Z_D + Z_L = 0$). For a steady-state operating point to be stable to transient noise, Kurokawa's formulation requires that the cross-product derivative inequality be satisfied:

$$\frac{\partial R_D}{\partial A}\frac{\partial (X_D + X_L)}{\partial \omega} - \frac{\partial X_D}{\partial A}\frac{\partial (R_D + R_L)}{\partial \omega} > 0 \tag{2.21}$$

If this inequality is applicable at the crossing point then any sudden increase of the signal amplitude will necessarily drive the system back to the damped, stable state rather than trigger an increasing oscillation [18].

Complex multi-stage or multi-transistor topologies with internal feedback loops bypassing the external ports require advanced frameworks such as the Ohtomo stability test and the modern Winslow probe (WS-Probe). The Ohtomo test is an extension of the traditional Nyquist principles achieved by extracting the determinant of the multi-port characteristic matrix. It counts the clockwise encirclements of the origin for a denominator of the open-loop transfer function:

$$H(s) = \det |\mathbf{I} - \mathbf{S}_{active}(s)\mathbf{\Gamma}_{passive}(s)| = 0 \tag{2.22}$$

Additionally, the Winslow probe greatly simplifies the current linear and non-linear multi-loop validation process by inserting a non-invasive, localized ideal probe in key internal circuit branches. The probe is able to identify the Return Ratio (RR) matrix or the generalized loop gain $G_L(\omega)$ without disturbing the operating point of the circuit. The actual multi-loop stability margin is verified by checking that the poles of the closed loop transfer function are strictly contained in the open left-half of the complex s-plane ($s = \sigma + j\omega$):

$$1 - G_L(s) \neq 0 \quad \text{for all } \Re(s) \geq 0 \tag{2.23}$$

By unifying what historically required dozens of discrete, fragmented ideal-ideal-node simulations into a structured, unified return-ratio workflow, the Winslow probe enables engineers to precisely target the transistor node or branch responsible for instability [18].

2.7 Distributed Transmission Line Theory

At microwave frequencies, the physical dimensions of the circuit components in an MMIC become comparable to the wavelength of RF signal, and classical lumped-element circuit theory loses accuracy. To accurately describe interconnects and matching elements, distributed transmission line theory must be used. A transmission line is a two-conductor structure that supports a guided electromagnetic wave, characterized by its characteristic impedance (Z_0), electrical length (θ), and propagation constant:

$$\gamma = \alpha + j\beta \tag{2.24}$$

where α is the attenuation constant and β is the phase constant [19].

2.7.1 Transmission Line Parameters

For a lossless transmission line, the distributed inductance per unit length (L') and capacitance per unit length (C') determine the characteristic impedance and phase constant:

$$Z_0 = \sqrt{\frac{L'}{C'}} \tag{2.25}$$

$$\beta = \omega\sqrt{L'C'} = \frac{2\pi}{\lambda_g} \tag{2.26}$$

where $\lambda_g = \lambda_0/\sqrt{\epsilon_{\text{eff}}}$ is the guided wavelength in the medium and ϵ_{eff} is the effective permittivity [20].

The input impedance (Z_{in}) of a transmission line of length ℓ terminated by a load impedance Z_L is given by the fundamental equation:

$$Z_{\text{in}} = Z_0 \frac{Z_L + jZ_0 \tan(\beta\ell)}{Z_0 + jZ_L \tan(\beta\ell)} \tag{2.27}$$

For a line with an electrical length $\theta = \beta\ell = 90°$ (a quarter-wave transformer), this simplifies to the impedance inversion property:

$$Z_{\text{in}} = \frac{Z_0^2}{Z_L} \tag{2.28}$$

2.7.2 Microstrip Realization

The microstrip is the most common planar transmission line for MMIC design, consisting of a conducting strip on a dielectric substrate with a continuous ground plane [21]. The UMS-GH10-10 process utilizes a SiC (Silicon Carbide) substrate. The characteristic impedance Z_0 depends on the ratio between the strip width (W) to substrate height (H).

For $W/H \leq 1$:

$$Z_0 = \frac{60}{\sqrt{\epsilon_{\text{eff}}}} \ln\left(\frac{8H}{W} + \frac{W}{4H}\right) \tag{2.29}$$

For $W/H \geq 1$:

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_{\text{eff}}}\left[\frac{W}{H} + 1.393 + 0.667 \ln\left(\frac{W}{H} + 1.444\right)\right]} \tag{2.30}$$

The effective permittivity ϵ_{eff} is calculated as:

$$\epsilon_{\text{eff}} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left(1 + 12\frac{H}{W}\right)^{-1/2} \tag{2.31}$$

These formulas are used within Keysight ADS (Follow section 3.1 to know more about Keysight ADS) to design series microstrip lines (MLIN elements), where the width W and length L are optimized to achieve the required impedance transformation at the design frequency [5].

2.8 Large-Signal Characterization and Load-Pull Analysis

The Load-Pull analysis is one of the method used in power amplifier design to characterize the large signal performance of a transistor. This technique identifies the optimal source and load impedances required to maximize output power and efficiency. The process involves systematically varying the complex load impedance presented to the transistor output. Performance metrics such as output power (P_{out}) and PAE are recorded at each point to generate Power Contours and PAE Contours.

The reason for employing load-pull analysis rather than simple conjugate matching is that power transistors operating near saturation are nonlinear. Consequently, the optimal large-signal load impedance (Z_{opt}) typically deviates from the conjugate of the small-signal output impedance (Z_{out}^*) [11].

2.8.1 Load-Line Theory and Optimal Resistance

The Load-line theory provides an initial estimate of the optimal load resistance (R_{opt}) based on the transistor's DC characteristics:

$$R_{\text{opt}} = \frac{V_{DD} - V_{\text{knee}}}{I_{\text{max}}/2} \tag{2.32}$$

where:

- V_{DD} is the drain supply voltage (15 V for the UMS-GH10-10 process).
- V_{knee} is the knee voltage (approximately 2 V).
- I_{max} is the maximum drain current (1.2 A/mm of gate width).

The theoretical maximum output power ($P_{\text{out,max}}$) for a single transistor is given by:

$$P_{\text{out,max}} = \frac{(V_{DD} - V_{\text{knee}}) \cdot I_{\text{max}}}{8} \tag{2.33}$$

2.9 Microstrip Discontinuities and Parasitic Effects

At millimeter-wave frequencies, every geometric variation in a microstrip circuit introduces parasitic electromagnetic effects that deviate from ideal transmission line theory. Common examples of these discontinuities include T-junctions (three-line intersections), corners (bends), open-circuit stubs, and step changes in line width. For an accurate simulation between 37 GHz to 40 GHz, these must be modeled using PDK-specific elements such as MTEE (T-junction), MCORN (corner) and MLOC (open-circuit stub) [22].

2.9.1 T-Junction Modeling (MTEE)

The MTEE element models the T-junction discontinuity, which is critical in corporate feed networks designed to distribute RF signals equally among parallel transistors. Fringing fields at the junction introduce parasitic capacitance, which the model represents as equivalent lumped elements. Neglecting this junction capacitance leads to phase errors in signal distribution, which reduces the effectiveness of coherent power combining.

The parasitic capacitance of a microstrip T-junction is approximately:

$$C_{\text{junction}} \approx \frac{\epsilon_{\text{eff}} \epsilon_0 W_1 W_2}{H} \tag{2.34}$$

where W_1 and W_2 are the widths of the intersecting lines and H is the substrate height.

2.9.2 Open-Circuit Stub End-Effects (MLOC)

The open-circuit stub discontinuity MLOC exhibits fringing capacitance at its termination, causing the effective electrical length to appear longer than the physical length by an end-effect correction $\Delta\ell$:

$$\Delta\ell = 0.412H\frac{(\epsilon_{\text{eff}} + 0.3)(\frac{W}{H} + 0.264)}{(\epsilon_{\text{eff}} - 0.258)(\frac{W}{H} + 0.8)} \tag{2.35}$$

In ADS MLOC models, this correction is applied automatically. Failure to account for $\Delta\ell$ would cause the stub to resonate at a frequency slightly lower than the design target, potentially shifting the matching or filtering response of the amplifier [23].

2.9.3 Short-Circuit Stubs End Effects (MLSC)

A short-circuit stub is terminated in a low-impedance connection to ground, typically via a via or a grounding structure. Unlike an open-circuit stub, it has no large fringing-field capacitance at its termination. However, the physical shorting structure introduces parasitic inductance and capacitance that cause the effective electrical length to differ slightly from the physical length.

Thus, the short-circuit stub can be represented by an effective electrical length.

$$\ell_{\text{eff}} = \ell + \delta\ell$$

where $\Delta\ell$ is the equivalent length correction for the via, ground connection and local discontinuity. The electrical effects of the short-circuit termination are included in the MSHORT model in ADS. Neglecting these parasitic effects can change the resonant frequency of the stub and thus lead to errors in the desired impedance transformation and matching performance of the amplifier [23].

2.10 Electromagnetic Simulations

MMIC design electromagnetic (EM) simulators are classified into 2D, 2.5D, and 3D solvers, depending on the physical detail they simulate. 2D planar EM simulators analyze the cross-section of strip-type transmission lines under the assumption of transverse electromagnetic (TEM) or quasi-TEM wave propagation [24]. They determine parameters such as effective permeability, per-unit-length capacitance, inductance and S-parameters for finite transmission lines, with current flowing only along the width and length of the conductors. Examples of these simulators are ANsoft Designer SV Integrated 2D find solver and LINMIC quasi-TEM and full-wave simulator [25, 26]. 2.5D simulators such as Momentum extend this capability to model current flow in the vertical direction, thus enabling accurate modeling of through-substrate vias and multilayer planar structures [27]. 3D planar simulators also take into account conductor thickness and resistivity for more realistic predictions of conductor losses.

The most comprehensive method is 3D arbitrary geometry EM simulators. These simulators model the whole structure volumetrically and do not restrict current or field directions. These simulators accurately model conductor thickness, resistivity and the complex electromagnetic interactions but require significantly longer simulation times than planar methods [28]. With these EM solvers, MMIC designers can predict coupling between nearby components, wavelength effects and higher order propagation modes that cannot be represented with conventional S-parameter models. Full-chip EM simulation is usually done as a final verification step before manufacturing the circuit whereas EM-simulation of critical parts is done earlier in the design process to check coupling or parasitic effects that could impact circuit performance [29].

In nonlinear simulations when EM-generated models are used, it is important that EM data are generated with sufficient frequency sampling. In harmonic-balance analysis, the solved frequency points should include all required harmonic frequencies, while time-domain simulations require frequency samples at multiples of the minimum time step. Correct sampling in frequency ensures numerical convergence and accuracy of the combined EM and circuit-level simulation results[30].

3

Method

This chapter presents the systematic methodology of designing and optimizing the millimeter-wave power amplifier using the UMS GH10-10 GaN HEMT process in the Keysight ADS environment. The workflow started with a DCIV characterization for the optimum Class AB quiescent bias point, followed by extensive load-pull simulations at 40 GHz to obtain the peak load impedances for maximum power and efficiency. The methodology described the design of the matching networks, outlining the transition from ideal microstrip stubs to a high-fidelity EM-circuit co-simulation framework. Finally, a multi-layered stability verification workflow was established, using Winslow probes and localized loop-gain analysis along with driving point admittance to ensure that the amplifier is robust against self-oscillations across the entire 1–50 GHz spectrum.

3.1 Simulation Environment

The PA MMIC is synthesized and optimized using the industry-standard Keysight ADS software. For both nonlinear harmonic balance simulations and linear S-parameter analysis can be done easily with Keysight ADS. To ensure that matching networks satisfy the requirements for both the large-signal power supply and small-signal gain flatness, this dual capability is essential.

We simulated bandwidth/efficiency/linearity trade-offs for class AB power amplifier and provide suggestions for incorporation into mmW transmitter front ends. Keysight ADS was for both the design and verification of the system and the layout.

3.2 Transistor Model

For the accurate ADS simulation, the use of PDKs provided by the manufacturer is crucial. In this PA design, UMS GH10-10 PDK is used [7]. This PDK consists of nonlinear HEMT models and the particular material characteristics of the SiC substrate. The electrical length of Metal–Insulator–Metal (MIM) capacitors, the current-carrying constraints of microstrip lines, and the parasitic effects of substrate vias can all be taken into account by using PDK components. In the 37–40 GHz spectrum, nonlinear modeling is necessary to predict PAE and saturation output power. Gain compression and harmonic generation that occur close to saturation cannot be predicted by linear models, despite the fact that they are quicker and

more helpful for initial topology selection. In actual large-signal situations, matching networks can be iteratively optimized using the ADS Harmonic Balance engine. All these criteria are satisfied with the PDK nonlinear Hot FET model GH10NHF_TV.

3.3 DCIV Simulations and Bias Point

To find the ideal quiescent bias point (Q-point), HEMT cells are first characterized using DCIV sweeps, as shown in figure 3.1. A bias point for the PA design for the nonlinear hot FET model GH10NHF_TV is observed at a gate-source voltage (V_{GS}) of -2.5 V and a drain-source voltage (V_{DS}) of 15 V. This bias value strikes a compromise between the power management needed to satisfy the 5 W requirements and the strong transconductance for gain.

The transconductance (g_m) and internal capacitances specifying the input and output impedances of the transistor are determined by the quiescent conditions. For the synthesis of a matching network, these values are crucial. While supplying the current swing needed for high-power operation, a constant quiescent current guaranties that the transistor stays within the safe working range of its IV characteristics.

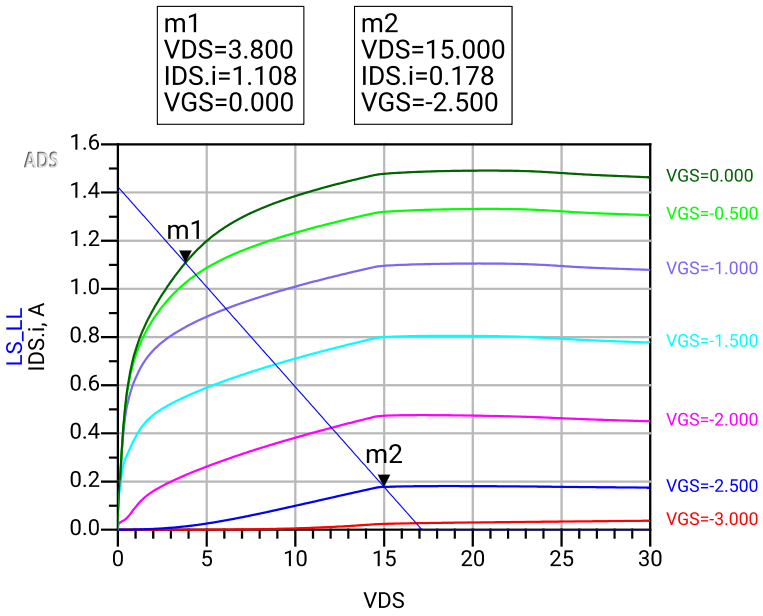


Figure 3.1: DCIV characteristics

3.4 Load Pull Simulations

To obtain the ideal load reflection coefficient (Γ_L) for a certain performance objective, the Load-Pull approach is used [1]. To determine the impedances that optimize power or PAE, simulated tuners are swept across the Smith chart in the ADS environment. In this PA design, this methodology is applied to the 37–40 GHz range, where optimal Γ_L is significantly more sensitive to parasitics. A parallel RC net-

work (Rp, Cp) that simulates the transistor's output under saturated conditions is created once the ideal Γ_L has been found.

3.5 Matching Network

The output matching network is synthesized using the load-pull data throughout the frequency range 37–40 GHz. The network guarantees maximal power transfer from the transistor to the 50 Ω load by displaying the conjugate of the parallel RC model [31]. Matching networks convert Z_{source} (Source impedance) and Z_{load} (Load impedance) to standard 50 50 Ω termination with limited bandwidth [32]. To obtain the desired maximum power, gain, or PAE, these Z_{source} and Z_{load} values are crucial. Consequently, it's important to identify these ideal values using load pull simulations.

3.6 Stability Network

A stability network provides unconditional stability ($K > 1$, $|\Delta| < 1$) at DC and out-of-band frequencies while maintaining in-band performance. Due to the internal feedback and the high out-of-band gain, high-frequency transistors are conditionally stable[33]. The stability network is realized using resistive RC networks and low frequency decoupling circuits at the input and the interstage sections. It provides controlled loss at self-oscillation frequencies with minimal attenuation in the 37–40 GHz operating band without degrading PAE, gain or output power.

Multi-stage stability check was characterized using WS probe at gate and drain terminals of the driver stage (two transistors) and the final stage (four transistors). Kurokawa's driving point admittance analysis included impedance at each transistor node, taking into account parasitic coupling and inter-transistor interactions. Ohtomo loop-gain measurements revealed local feedback paths and instability mechanisms not captured by global S-parameter analysis. This multi-point approach detects device level oscillations (gate to drain coupling, drain-source feedback) and confirms that stability networks suppress out-of-band resonances.

4

Design

This chapter presents the design and physical implementation of a Class AB PA for 5G backhaul applications in the 37–40 GHz millimeter-wave band using the UMS GH10-10 GaN HEMT process design kit. The cascaded two-stage architecture consists of a driver stage with two parallel transistors and a final power stage with four parallel transistors targeting 37 dBm output power. The design flow is systematic, where first the IMN, ISMN and OMN are synthesized with ideal microstrip stubs, then converted to layout-realizable schematics and verified by electromagnetic simulation. It then moves to EM-circuit simulation to capture high-frequency parasitics, radiation losses and substrate effects. Parallel *RC* stabilization networks and Winslow probes guarantee multi stage stability against self-oscillations. The chapter ends with the final layout design ready for fabrication.

4.1 Ideal Microstrip Two-Stage PA Schematic

The UMS GH10-10 GaN HEMT process design kit provides foundry verified nonlinear models necessary for accurate large signal design. The gate-source bias is $-2.5\,\mathrm{V}$ and the drain-source bias is 15 V determined with DCIV simulations ((section 3.3)) for Class AB operation. The load impedance for final PA stage is $R_p \parallel C_p$ ($15\,\Omega \parallel 0.6\,\mathrm{pF}$) and at driver stage is $R_{\mathrm{pd}} \parallel C_{\mathrm{pd}}$ ($40\,\Omega \parallel 0.4\,\mathrm{pF}$) obtained from load-pull simulations (section 5.1). Impedances at the gate of driver stage and final PA stage has been determined using S-parameter simulations, as these impedances required in matching networks. The load-pull simulations also determined optimal transistor geometries of $80\,\mu$m per gate finger and 6 fingers per transistor, giving 31 dBm output power per transistor. In an effort to achieve the target output power of 37 dBm, four transistors were connected in parallel (31 dBm output power for one, 34 dBm for two and 37 dBm for four, since each doubling adds 3 dB), with a total gate width of $1920\,\mu\mathrm{m}$ ($4 \times 6 \times 80\,\mu\mathrm{m}$) which is well within the $2\,\mathrm{mm}^2$ chip-area constraint.

DC-blocking capacitors separate bias networks from RF signals. The gate bias is composed of a V_{GS} voltage source and an inductor to establish the proper quiescent drain current and the class of the amplifier, while preventing RF leakage to the supply. The drain bias feed is to keep RF from getting to the power supply. The current probe measures the current for PAE, output power and current limits.

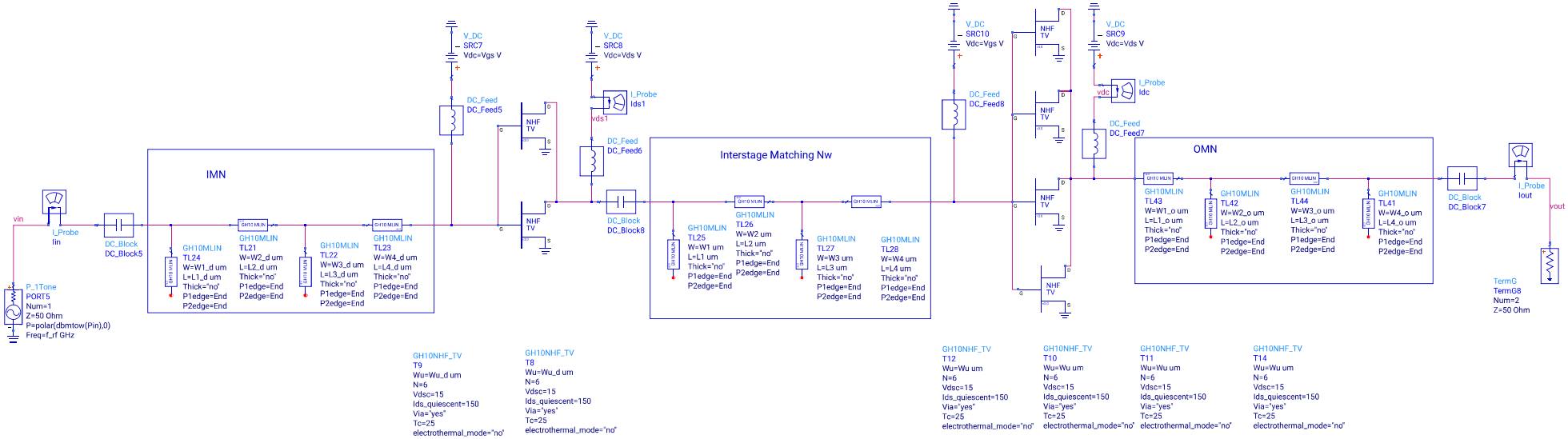


Figure 4.1: Schematic design with ideal stub matching network

Figure 4.1 shows the complete top-level schematic of the ideal two-stage RF PA topology. The two-stage cascade provides 37 dBm output power at 37–40 GHz by using three matching networks: IMN, ISMN, and OMN. The signal travels from the 50 Ω input port, through the IMN to the driver stage (two GaN transistor cells in parallel), and then via the ISMN to the four-transistor parallel power stage. The OMN provides the simultaneous matching of output impedance to 50 Ω termination and the DC feed path.

4.1.1 Output Matching Network

The OMN is the final stage of the amplifier, which is shown in figure 4.2. It transforms the standard 50 Ω system impedance (TermG12) into the optimum load impedance for the four-transistor power stage ($R_p \parallel C_p$, where $R_p = 15\,\Omega$ and $C_p = -0.6\,\text{pF}$), derived from load-pull simulations (Section 5.1) to achieve maximum output power of +37 dBm (5 W).

The negative capacitance cancels the transistor output capacitance but can be realized with physical components only over a limited bandwidth. To find an OMN that achieves this, we used small signal simulations to optimize the matching between the conjugate of the optimum load $R_p \parallel C_p$ and the 50 Ohm system impedance as shown in figure 4.2. We use complex conjugate matching because the maximum power transfer occurs when the OMN input impedance is equal to the complex conjugate of the transistor output impedance. That is, if the transistor output impedance is $Z_{\text{out}} = R_{\text{out}} - jX_{\text{out}}$, the OMN input impedance should be $Z_{\text{in}} = R_{\text{out}} + jX_{\text{out}}$. Such conjugate matching removes the reactive components and delivers the maximum real power to the load.

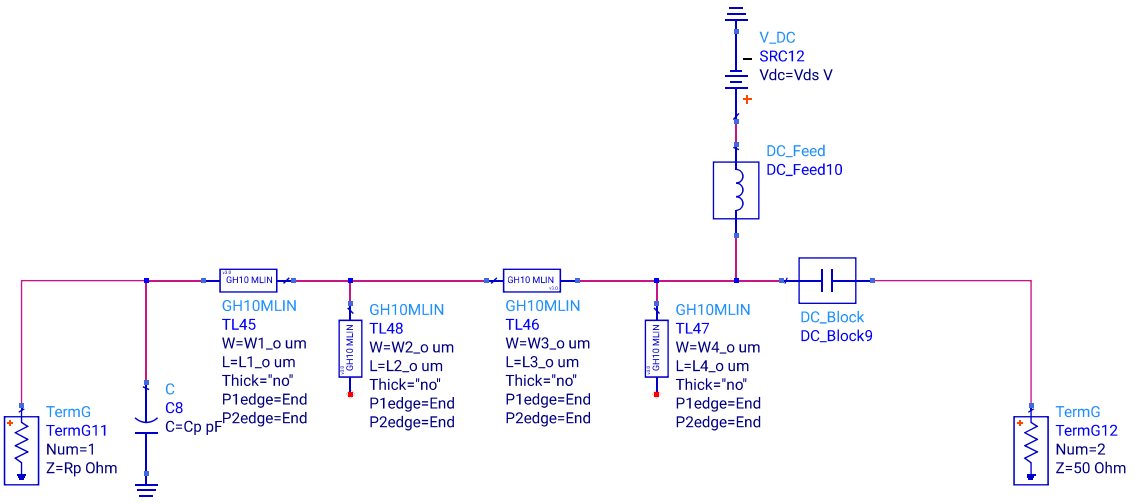


Figure 4.2: Output matching network schematic

The OMN should match the 50 Ω reference impedance to the optimal load impedance of 15 Ω. This means a transformation ratio of 3.33 : 1 is needed. Although the ratio

is moderate, the most challenging aspect is that the 0.6 pF output capacitance presents an impedance of only -j*6.6 Ohm at 40 GHz, which is quite small relative to 50 Ohm. The relative high optimum load resistance ($R_p = 15\,\Omega$) is attributed to the operation at high drain source voltages that intrinsically limits the bandwidth due to the Bode-Fano limit but also an Rp closer to 50 Ohms makes a wideband matching network easier to realize in practice. To overcome these limitation, the OMN utilizes a multi-section microstrip transmission line topology (TL45–TL48) where the impedance transformation is performed in discrete steps rather than a single abrupt transition shown in figure 4.2. This distributed approach leads to a dual-resonant bandpass response, which extends the usable bandwidth in the 37–40 GHz band, while maintaining efficient power delivery and low insertion loss.

4.1.2 Interstage Matching Network

The impedance transformation between the two-transistor driver stage and the four-transistor final power stage is performed by the ISMN. It matches the output of the two-transistor driver stage to the input of the final four-transistor power stage as shown in figure 4.3. Following are the impedance values obtained from load pull simulations (Section 5.1) for ISMN, the input impedance of the ISMN is the complex conjugate of output impedance of the driver, which is $R_{pd} \parallel C_{pd}$ ($40\ \Omega \parallel -0.4$ pF) which was determined from load-pull simulations and the input impedance determined at the gate of four parallel transistors which was $1 - j2.4\,\Omega$ (simulated with S parameter). The ISMN uses cascaded microstrip transmission lines (TL20 to TL3) to transform the $40\,\Omega$ driver impedance to a $1 - j2.4\,\Omega$ reactive load, compensating for both drain and gate capacitances.

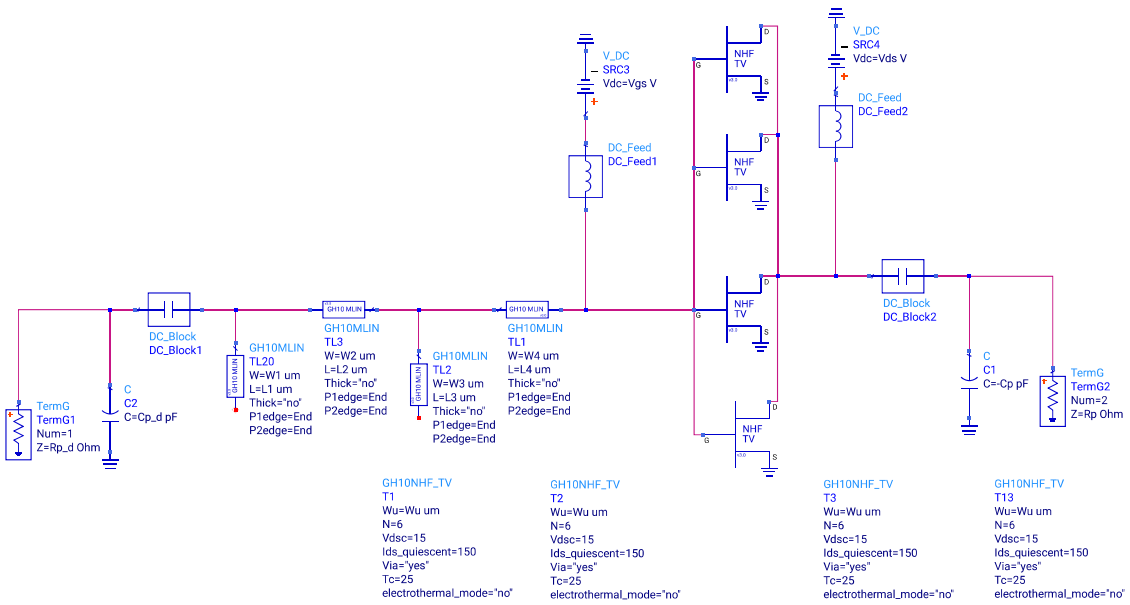


Figure 4.3: Interstage matching network

Here, to check gain of final stage including ISMN, four parallel transistors and the optimum load impedance ($R_p \parallel C_p$ (15 Ω ∥ 0.6 pF)) is added to the design.

4.1.3 Input Matching Network- Driver amplifiers

The IMN, shown in figure 4.4 is designed primarily to provide an optimum impedance matching between the standard 50 Ω RF source generator (TermG3) and the complex conjugate of the gate impedance of the driver stage (which was $1.86 + j1.28\,\Omega$ obtained with S-parameters).

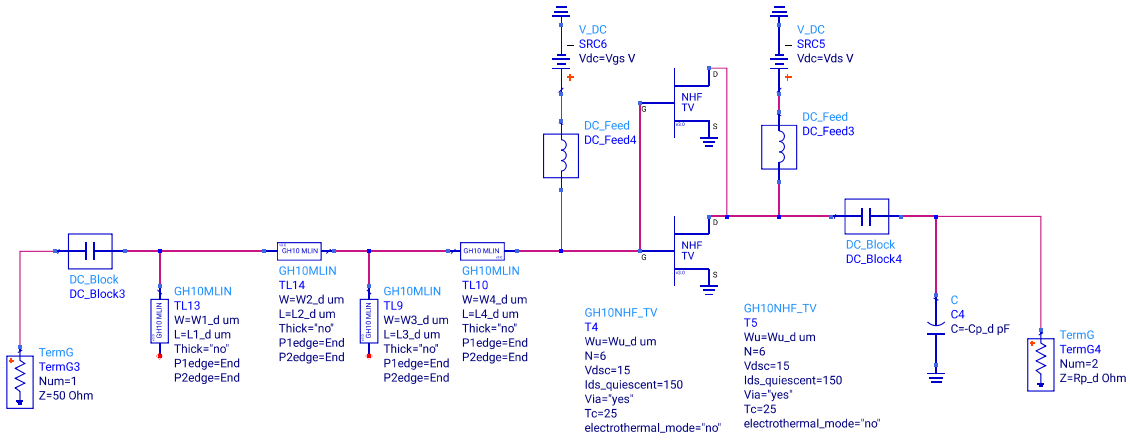


Figure 4.4: Input matching network

To achieve this impedance matching at 40 GHz, the IMN is synthesized with distributed microstrip transmission lines (GH10MLIN elements TL24, TL21, TL22, and TL23). Here, to check gain of driver stage including IMN, two parallel transistors and the optimum load impedance ($R_{pd} \parallel C_{pd}$ (15 Ω ∥ 0.6 pF)) is added to the design

4.2 Layout-Realizable Schematic Design of Two-Stage PA

Although, the ideal microstrip transmission line design provides accurate impedance transformation and performance prediction, it cannot be directly transferred to the physical layout due to practical implementation constraints. Ideal transmission line models do not include the connection discontinuities such as T-junctions (MTEE), corners (MCORN), and via transitions that are inherent in fabricated layouts. Furthermore, biasing networks cannot be added to the idealized schematic without decreasing the accuracy of electromagnetic simulation.

Hence, the PA architecture is redesigned as a layout-realizable schematic by replacing ideal microstrip stubs with parameterized distributed elements accounting for practical discontinuities, junction effects and parasitic coupling to bridge the gap between theoretical design and manufacturable implementation. The resulting schematic is cleaner and has explicit biasing components, decoupling networks, via placements and transmission line segments with realistic dimensions and routing topologies. This layout-realizable design methodology ensures the electromagnetic performance is preserved from schematic simulation to physical mask layout, while maintaining the impedance matching, gain flatness and stability over the operational band.

4.2.1 Output Matching Network Schematic

An ideal OMN design (figure 4.2) based only on microstrip transmission line stubs cannot be directly realized in physical layout as junction points, corner connections along with biasing networks are missing which are crucial in layout design. The redesigned layout-ready OMN implements a symmetrical 4-to-1 corporate power combiner with input impedance $15\,\Omega \parallel -0.6\,\text{pF}$ and $50\,\Omega$ output, implementing a series DC blocking capacitor close to the output to prevent supply current from the $50\,\Omega$ load. Here, we replaced each circuit element from the ideal OMN with foundry-provided components in a systematic fashion as shown in figure 4.5. The first short stub is replaced by a short microstrip line and the first open stub is replaced by MTEE and shunt capacitor. The second short stub is substituted by a short microstrip line and the second open stub is a shunt capacitive element. After each replacement the circuit is re-tuned and re-optimized to recover the ideal frequency response by tuning the component values as closely as possible. The curved 'trombone' structure is used to reduce overall length of the network [34].

The RF signal at each transistor drain has to be coherently combined into one $50\,\Omega$ output. The matching network is first divided into two parallel traces and then four traces to connect the output load to the four parallel transistors. The network is designed to be exactly symmetric such that the load impedance seen by each transistor drain is the same, and hence the phases are added coherently to combine the power. Whenever the network splits into two parallel branches, impedance scaling is applied. All series inductances in each trace are doubled, all shunt capacitances are halved. As we have split the network again into four traces the inductances are multiplied by four and the capacitances divided by four compared to the original ideal design. This scaling keeps the electrical characteristics of the original ideal two-port matching network, so that the four-way corporate combiner presents the correct efficiency-tuned impedance to each transistor output over 37–40 GHz and transforms to $50\,\Omega$ at the RF output connector.

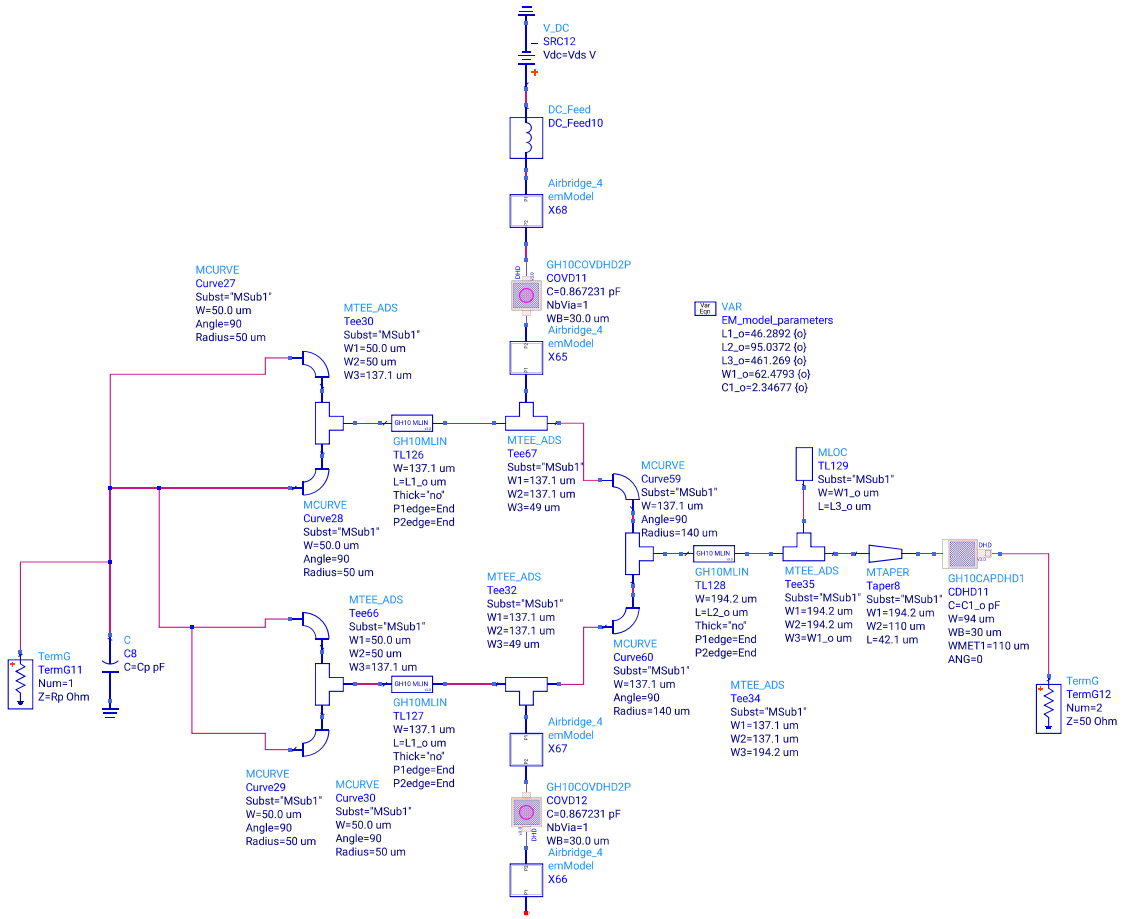


Figure 4.5: Output matching network schematic

An alternative topology was tested to optimize the OMN layout shown in figure 4.6. The ideal schematic simulation indicated the original and revised OMN topologies had identical performance, but the electromagnetic (EM) co-simulation showed a significant performance degradation at 40 GHz. In particular, the new structure showed a 5% decrease of PAE and a 2 dB degradation of transducer gain. The degradation is attributed to unmodeled layout parasitics, destructive electromagnetic coupling, and local field discontinuities introduced by the additional MTEE junction at high mm-wave frequencies. The change turned out counterproductive so the design went back to the original OMN architecture.

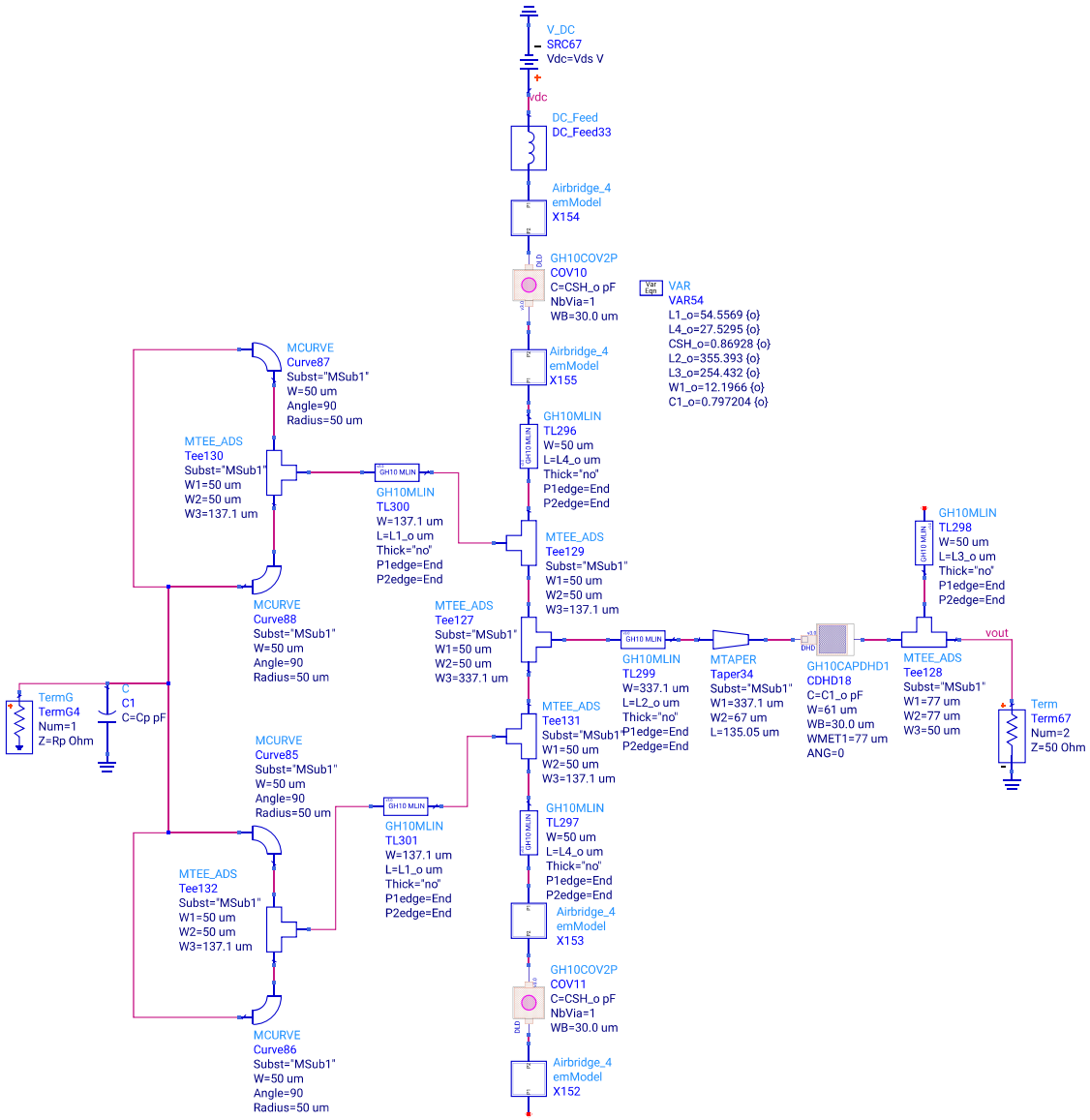
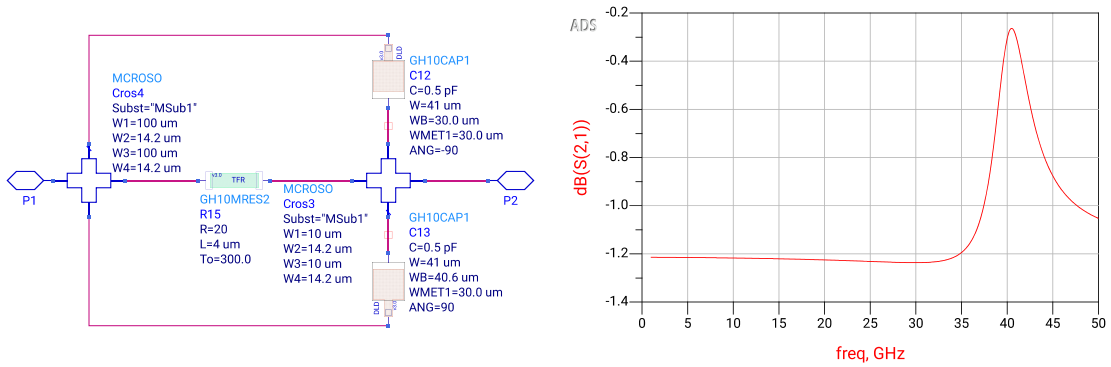


Figure 4.6: Alternate output matching network topology schematic

Parallel RC Stabilization Network

We noticed the instability near operating band frequencies (at 32.5 GHz) as per stability analysis performed in figure 5.18. To ensure stability across the millimeter-wave active devices, a parallel *RC* lossy bandpass stabilization network (figure 4.7a) was introduced. This network supresses the positive reflection caused by OMN where design have a negative return loss ($|S_{11}| < 0\,\text{dB}$) near 32.5 GHz. While this response peak is outside the desired 37–40 GHz passband, the stabilization network provides resistive loading at these frequencies to selectively suppress positive feedback and spurious self-oscillations without degrading in-band PAE.

This is a very symmetrical corporate schematic with microstrip crosses (MCROSO



(a) Stability network.

(b) Insertion loss response of stability network.

Figure 4.7: Parallel RC stabilization network.

elements Cros4 and Cros3) used to split and recombine the RF signal. The network comprises two parallel signal paths:

1. **The resistive path:** The middle lane is a thin-film resistor R15 (GH10MRES2). It's resistance is 20 Ω.
2. **The capacitive bypass path:** The top and bottom lanes contain series (MIM) capacitors C12 and C13 (GH10CAP1), each with a capacitance of 0.5 pF, giving a total parallel capacitance of 1.0 pF.

At low frequencies (from DC to approximately 30 GHz), the capacitors exhibit a very high reactive impedance,

$$X_C = \frac{1}{\omega C},$$

and therefore they can be approximated as open circuits. This forces the RF signal to pass through the 20 Ω resistor R15, resulting in a controlled insertion loss of approximately 1.2 dB. Transistors are naturally very sensitive to out-of-band self-oscillations because of their very high intrinsic gain at lower frequencies. This targeted low-frequency attenuation suppresses the excess gain, thereby maintaining the amplifier in stable condition.

Figure 4.7b is a plot of the simulated forward transmission coefficient (dB(S_{21})) clearly shows the frequency-selective behaviour of this stabilization network. As the frequency is swept above 35 GHz, the desired operating band is approached, and

the impedance of the bypass capacitors C12 and C13 becomes much smaller. Consequently, the RF signal naturally bypasses the lossy 20 Ω resistor and propagates through the low-loss capacitive paths. This results in a sharp transmission peak at approximately 40 GHz with an insertion loss as low as 0.26 dB.

This frequency-dependent response is particularly useful for millimeter-wave PAs, as it provides strong lossy damping to suppress low-frequency instabilities while introducing only a small signal loss within the desired 40 GHz operating band. This block is EM simulated and EM model of this stability network is used for impedance matching in following sections.

4.2.2 Interstage Matching Network Schematic

The ISMN is the most complicated passive network in the multistage PA. Its primary objective is to achieve a complex-to-complex impedance matching of the output of the two-transistor driver stage and the input of the four-transistor final power stage. Following same procedure used for designing the OMN, a microstrip implementation of the ISMN was done and optimized from ideal microstrip ISMN shown in figure 4.3 to the layout ready ISMN shown in figure 4.8. The ISMN is implemented as a highly symmetrical 2-to-4 splitter network to distribute RF power uniformly from the two driver drains to the four power-stage gates. To get correct S parameters (gain and return loss) OMN is also added along with the ISMN.

Impedance scaling is applied when the network splits in two where inductances in each trace are doubled and the capacitances halved in order to preserve same electrical characteristics as the original two-port matching network in figure 4.3. Additional stabilization blocks are connected in series with the gates of each of the four final-stage transistors to ensure stable operation under all operating conditions.

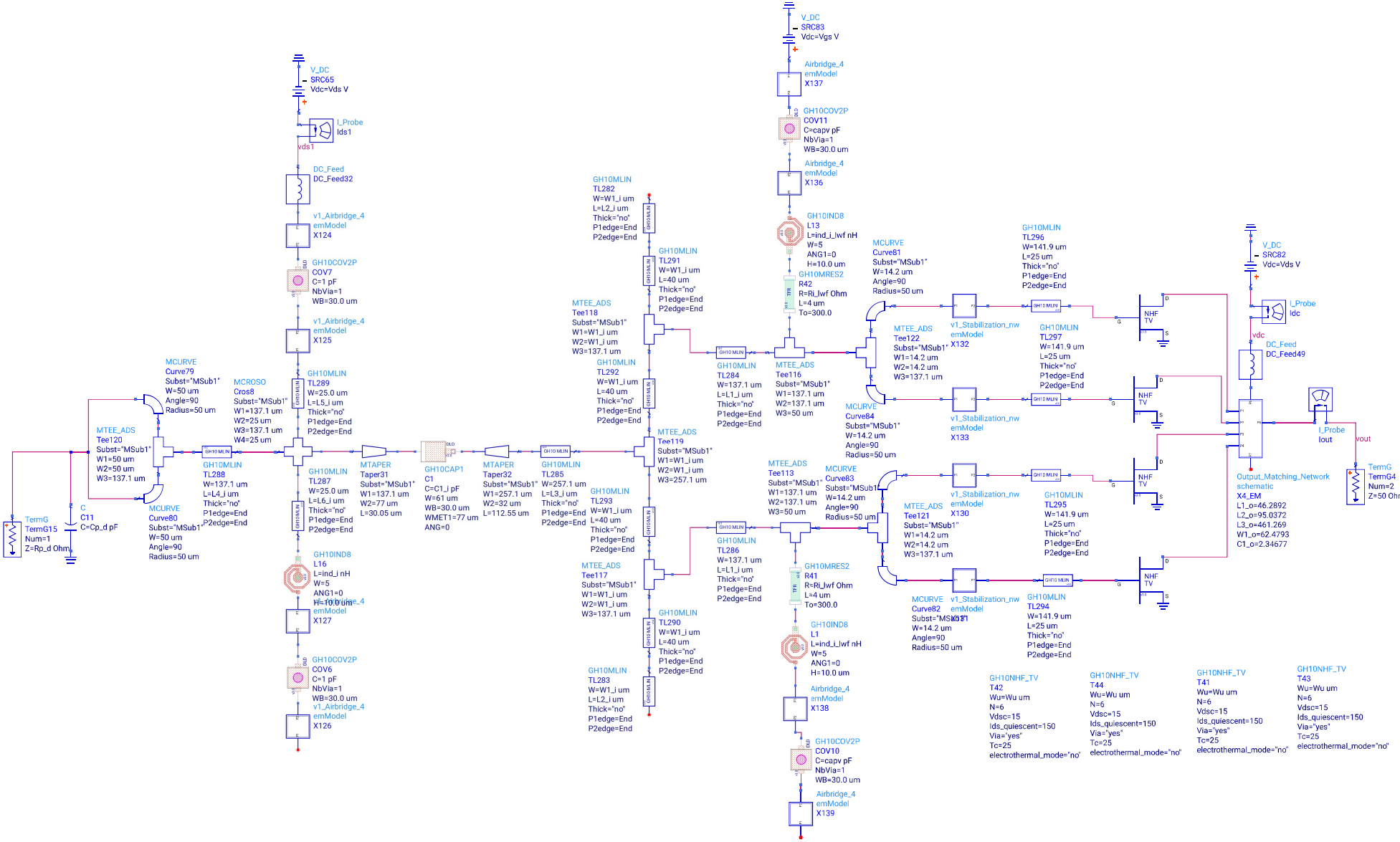


Figure 4.8: Interstage matching network schematic

4.2.3 Input Matching Network Schematic

In accordance with the procedure used for the other networks, a microstrip realization of the circuit was developed from the ideal microstrip IMN shown in figure 4.4 to the layout ready IMN shown in figure 4.9. It is designed to convert the standard 50 Ω source impedance (TermG3) to the optimum input impedance of the driver stage, which is $1.86 + j1.28\,\Omega$ obtained with S-parameters. To accomplish this transformation and simultaneously split the input signal to feed the two parallel driver transistors, the IMN is arranged as a symmetrical 1-to-2 corporate power divider. To get correct S parameters (gain and return loss) OMN along with ISMN is also added with the IMN which makes figure 4.9 a complete PA schematic.

The network feeds the gate bias voltage to the first-stage transistors and does the required division of the input signal. Like interstage network, the input network is also commonly employed to compensate for gain slope versus frequency and provide amplifier stabilization through the intentional introduction of loss.

Airbridges (Airbridge_4 X140 to X143) are used here, as The MIM cap-on-via layout uses the top metal layer for the RF signal trace and the bottom layer (metal 1) for ground. They thus require airbridges to connect to the surrounding metal 1 structures to not short circuit the signal to ground, preventing electrical short circuits.

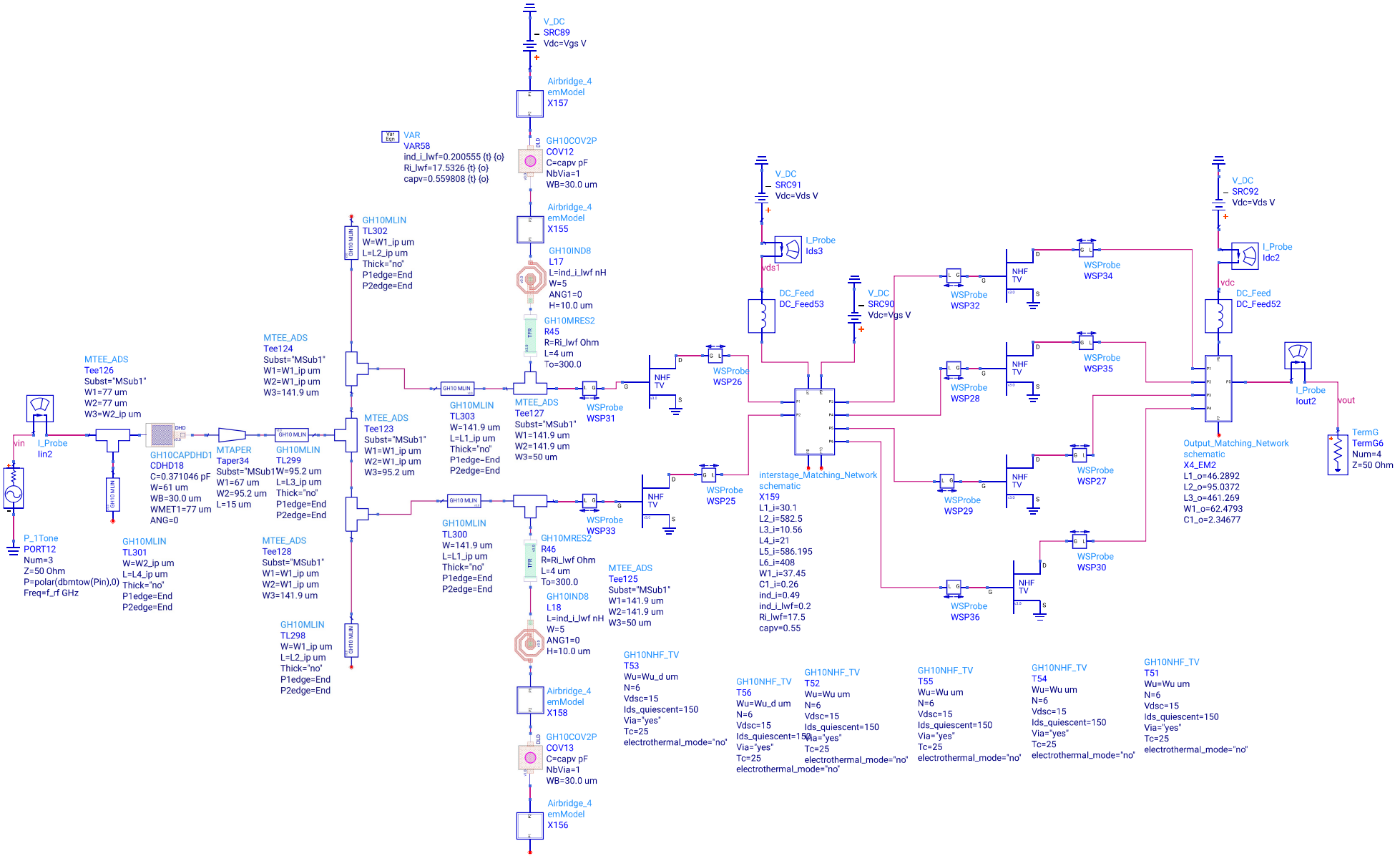


Figure 4.9: Two-stage PA schematic with detailed IMN schematic

4.3 Realization of PA Design Based on EM-Model Integrated Top-Level Layout

The operation of a PA is dominated by the electromagnetic fields produced by the real metal geometry, not the ideal elements used in a schematic explained in section 4.2. Microstrip bends, T-junctions, tapers, air-bridges and MIM capacitors all add frequency-dependent loss, phase shift and mutual coupling which change the intended impedance transforms of the IMN/ISMN/OMN. These effects also create unintended feedback paths and negative resistance regions that are not in the schematic, so a design that appears well matched, efficient and stable in schematic can shift in frequency, lose gain/PAE, or even oscillate after layout. Converting the matching networks to EM models captures these distributed effects, the real Q of resonators, current crowding around corners, ground-return inductance, and layout-to-layout coupling, giving tape-out-level predictions and allowing stability to be engineered rather than hoped for.

EM-model PA shown in figure 4.10 does this by replacing each passive network by an EM block taken from its schematic: the IMN matches the $50\,\Omega$ source to the two driver gates, the ISMN transforms the two driver drains to the four power-stage gates, and the OMN transforms the low parallel drain impedance of the four power devices to $50\,\Omega$.

To simulate the circuit with EM-simulated blocks, a layout of each passive subcircuit was generated and EM-simulated with ADS momentum. These EM-simulations were then compared to the original schematic models and discrepancies compensated for in an iterative process. The whole amplifier circuit was then simulated with EM-simulated sub-blocks.

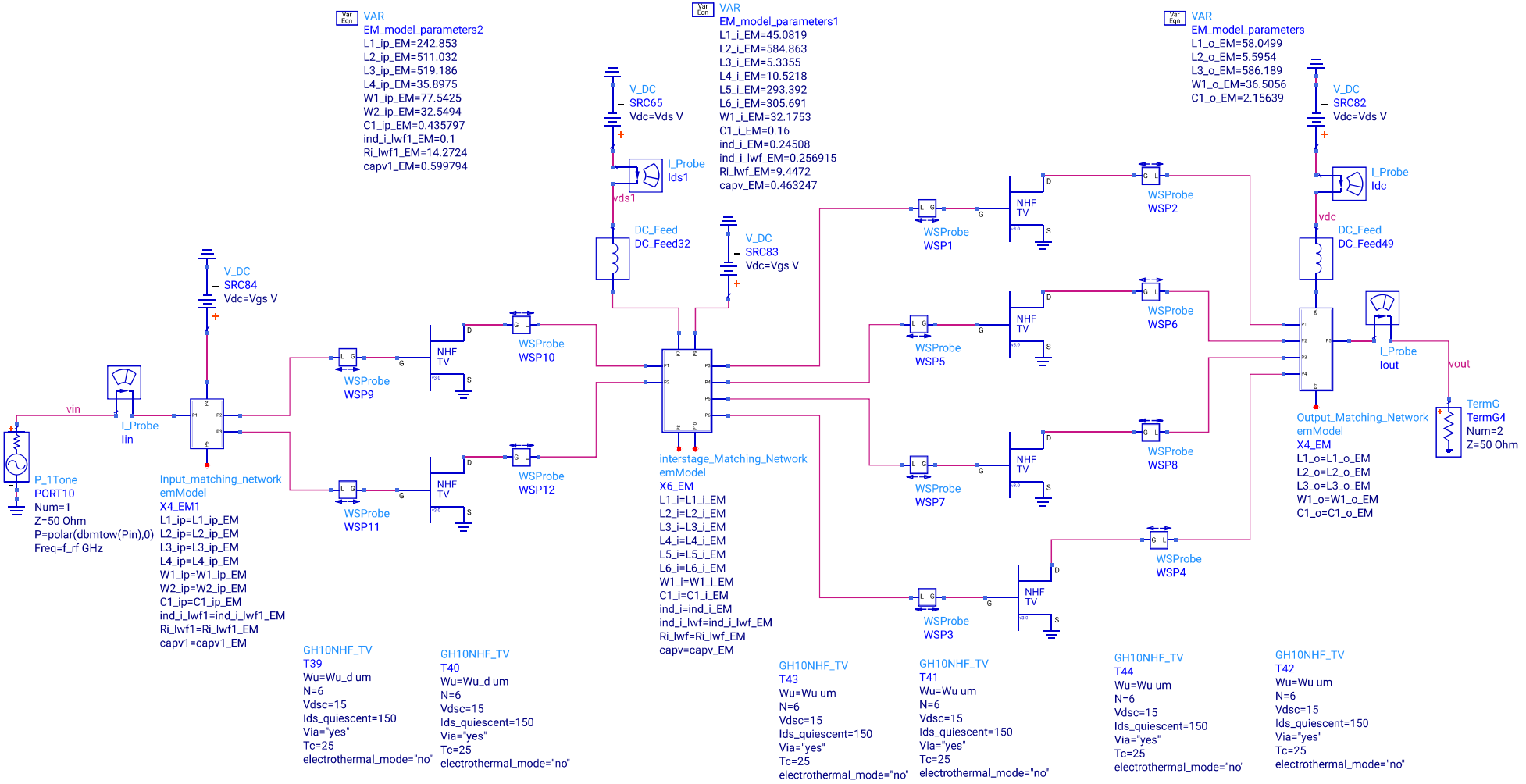


Figure 4.10: Layout-realized PA with stability and EM-model integration

4.4 Final MMIC PA Layout

The final physical layout of the MMIC PA for high-power and high-efficiency operation at 37–40 GHz is shown in figure 4.11. The layout shows a corporate-feed architecture that flows from the single input pad on the far left to the single output pad on the far right. The layout employs a 1-to-2 corporate splitter in the IMN, a 2-to-4 corporate splitter/combiner in the ISMN, and a 4-to-1 corporate combiner in the OMN to split and combine the RF signals across the multi-device active cores. The size of this layout is 3 mm × 2 mm..

Here, driver stage transistors are smaller than final PA stage as the first stage transistors do not contribute to the overall output power of the amplifier, but they do consume DC power. If these devices are too large, the power-added efficiency of the amplifier will be adversely affected. If the first stage FETs are too small, then there will not be enough power to drive the output stage to 3 dB of compression, and both output power and PAE will be affected negatively. This latter case is much worse, and it is recommended to err on the side of over-sizing the first stage transistors and living with a few points of lower efficiency.

The layout replaces sharp 90° corners with smooth, constant-width microstrip curves to avoid current crowding at inner edges and to reduce radiation and parasitic capacitive losses. As the RF signals travel towards the output, the microstrip transmission lines in the OMN are physically widened to accommodate the high combined RF current. These wide transmission lines reduce losses.

The vertical periphery of the layout is dedicated to the DC biasing, low-frequency decoupling, and stabilization networks, which are physically isolated from the main horizontal RF signal path. The gate and drain bias voltages are routed vertically and terminate in large square MIM bypass capacitors connected directly to ground through low-inductance substrate vias. These large bypass capacitors provide a very solid RF short-to-ground, preventing high-frequency RF leakage from coupling into the DC power rails and causing interstage feedback. Additionally, the previously described parallel RC stabilization networks, which consist of the microstrip crosses, series capacitors, and thin-film resistors, are physically integrated directly before the gate terminals of the active devices. This placement brings the lossy low-frequency damping mechanism as close as possible to the transistor gates, successfully absorbing out-of-band gain and ensuring the stability of the whole cascaded amplifier under all operating conditions.

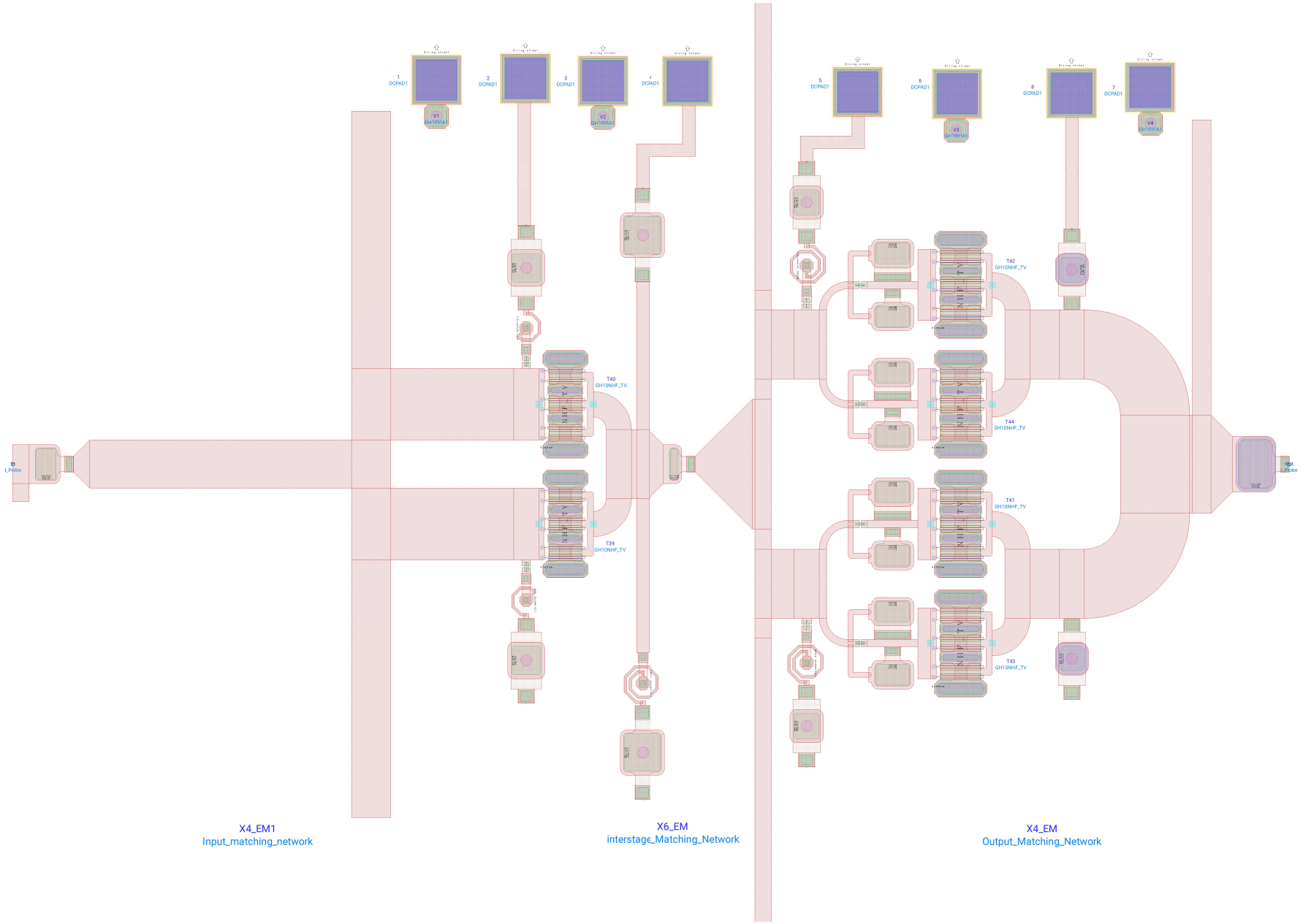


Figure 4.11: Final MMIC PA layout

5

Results

The complete simulation results of the proposed two-stage PA are presented in this chapter, covering linear, non-linear, and stability performances of two-stage PA. The analysis begins with driver and final-stage load-pull simulations, where output power and PAE contours are evaluated to find the optimum load impedance for each stage.

The amplifier performance is then characterized through small-signal S-parameter simulations, demonstrating the achieved transducer gain and input return loss. Large-signal harmonic balance simulations are subsequently performed to evaluate the saturated output power, AM–AM compression characteristics, and peak PAE.

Finally, a comprehensive stability analysis is presented, confirming that the final EM-realized layout achieves unconditional stability ($K > 1$) for operating band frequencies. The stability of the design is ensured through the integration of RC stabilization networks and is further validated using Ohtomo loop-gain analysis and Kurokawa driving-point admittance criteria.

5.1 Load-Pull Simulations

Load-pull simulations allow the designer to find optimum load impedance that balances the trade-off between maximum power delivery and efficiency without over driving the transistor into breakdown.

The fundamental frequency used for these simulations is 40 GHz. The input of the transistors were conjugate matched for these simulations to transfer maximum power. To find out optimum load impedance, parallel load capacitance (C_p) and load resistance (R_p) swept. $-C_p$ used to compensate transistor parasitics, R_p works as to load line to transfer maximum power.

5.1.1 Final PA Stage

Following are the results of the Load-Pull simulations done for the final PA stage which consist of 4 parallel transistors topology. These results are with 4 dB compression. The input power used is 30 dBm

Power Contours

Results of load-pull simulation on a Cartesian plane (R_p vs. C_p) are shown in figure 5.1. The output power contours are plotted with a step resolution of 0.2 dB. Closed oval contours connect load impedance combinations that provide equal fundamental output power, with the power value decreasing outwards from the center. The optimal point, marked by m_7 at the center of the innermost contour, provides a parallel load impedance $R_p = 15\,\Omega$ and $C_p = 0.6\,\text{pF}$ which results in the maximum output power of 37 dBm (5 W). This key result verifies the project target output power is achieved with the transistor working into this particular load impedance.

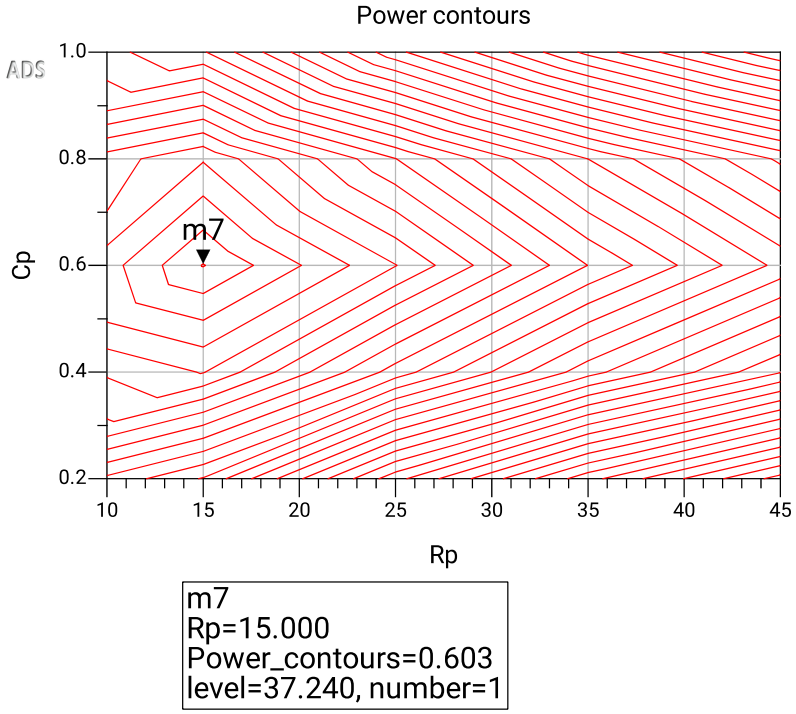


Figure 5.1: Power contours

Power Added Efficiency Contours

Load-Pull contours of constant PAE is defined as PAE $= \frac{P_{\text{RF,out}} - P_{\text{RF,in}}}{P_{\text{DC}}} \times 100\%$ are shown in figure 5.2 on the same R_p vs C_p plane. the power-added efficiency (PAE) contours are plotted in discrete 2% decrement, where center contour has highest efficiency. The PAE is a measure of how effectively the DC supply power is converted into useful RF output power, which is desired to reduce power consumption and heat generation in 5G backhaul systems. Marker m_5 points out a peak efficiency of 47.5% at $R_p = 16.6\,\Omega$ (close to $15\,\Omega$) and $C_p = 0.6\,\text{pF}$.

The load impedance values were chosen near the peak power contour to meet the high power requirement, trading off maximum efficiency for higher RF output power.

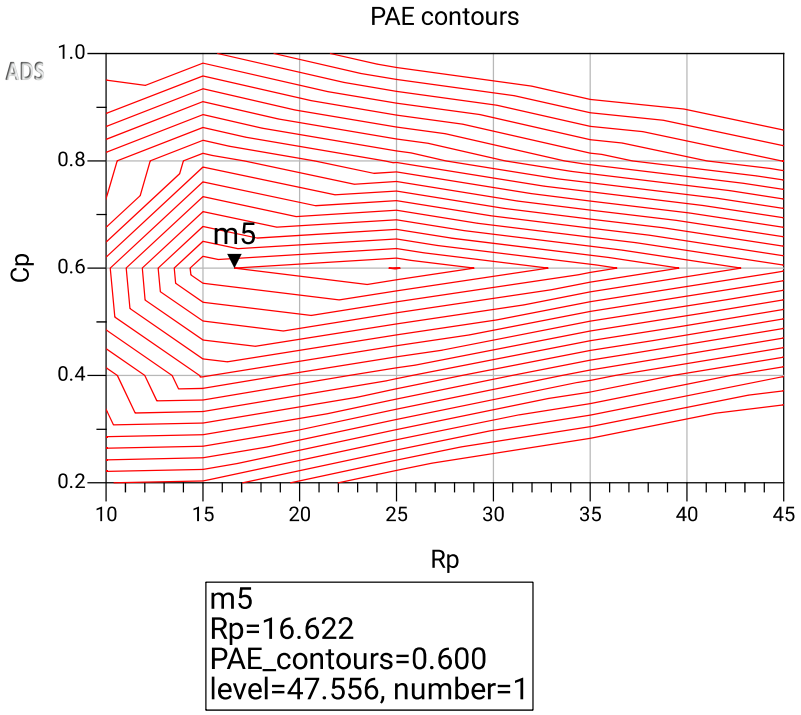


Figure 5.2: PAE contours

Power Added Efficiency Vs Output Power

Figure 5.3 shows the PAE as a function of the fundamental P_{out} for different load impedances evaluated in the load-pull sweep.

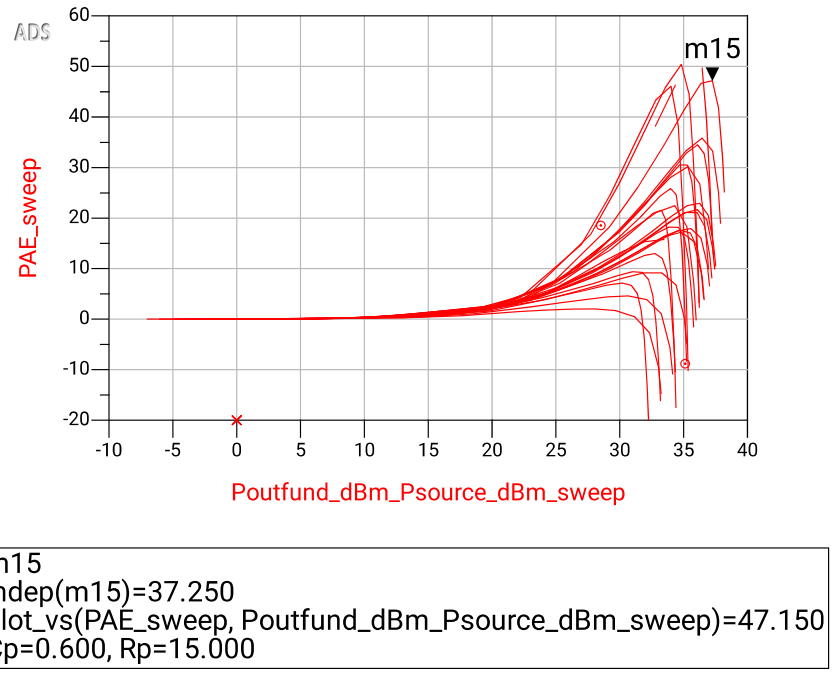


Figure 5.3: Power added efficiency vs output power

Here, the different traces are for different R_p-C_p combinations and that the trace with the marker is for the chosen $15\,\Omega \parallel -0.6\,\text{pF}$.

As expected for a PA, the PAE remains relatively low in the small-signal region and increases rapidly with output power as the amplifier is driven into the large-signal regime. Figure 5.3 shows that the amplifier achieves a peak PAE of 47% at an output power of 37 dBm for the selected optimum load impedance of $R_p = 15\ \Omega$ and $C_p = 0.6$ pF, as indicated by marker m_{15}. Also at 27 dBm output power (10 dB back-off) efficiency is approximately 16%. This PAE can achieve the project's design target of $> 15\%$ PAE at 10 dB output power back-off. This confirms that the selected load impedance provides an excellent compromise between the required maximum output power of approximately 5 W and high efficiency.

Gain Vs Output Power

Figure 5.4 shows the gain of the amplifier as a function of the fundamental output power (AM–AM characteristic). It demonstrates the transition from linear operation to nonlinear saturation for the optimal load impedance. The small-signal linear gain is ($\sim$ 10 dB) at an output power of 0 dBm at low power levels, as indicated by marker m_{13}. As the transistor is driven into the saturation region, the gain begins to compress. At marker m_{14}, the output power reaches 36.4 dBm, while the gain decreases to 7.4 dB, corresponding to approximately 2.5 dB of gain compression. This performance indicates operation near the 3 dB compression point $P_{3\text{dB}}$, which closely corresponds to the saturated output power capability of the device.

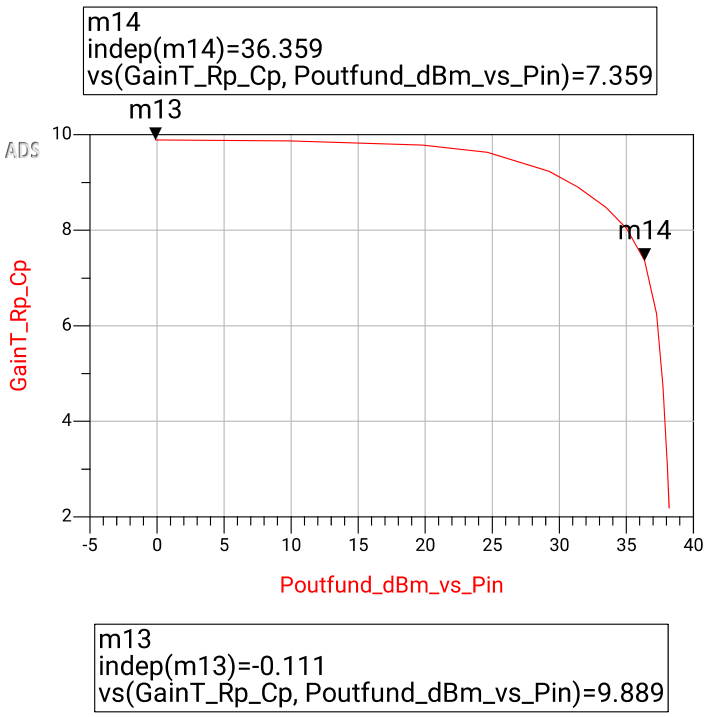


Figure 5.4: Gain vs output power

Highest achieved gain for final PA stage is ($\sim$ 10 dB) and the target gain (20 dB),

hence driver stage needs to be added. The power stage has a gain of 8 dB with an output power of 30 dBm at approximately 2 dB of gain compression as shown in figure 5.4. Therefore, the driver stage should be designed to provide a driving output power of at least 30 dBm. To achieve this, a load-pull analysis was performed for the driver stage, and the results are presented in the following section.

5.1.2 Driver Stage

Following are the results of the Load-Pull simulations done for the driver amplifier design which is added here to increase the overall gain, which consist of two parallel transistors topology, where gate width of each finger is 65 μm and number of gate fingers used in each transistors are six (total gate periphery of 780 μm). The fundamental frequency used for these simulations is 40 GHz and the input power is 15 dBm. All below results are with 2 dB compression.

Power Contours

The driver stage power contours plot (figure 5.5) shows the output power levels on a Cartesian plane versus R_p and C_p at 40 GHz. Marker m_7 indicates the optimum load impedance for maximum power transfer at $R_p = 40\ \Omega$ and $C_p = 0.4$ pF, resulting in a peak output power of 26 dBm at this load-pull input drive level.

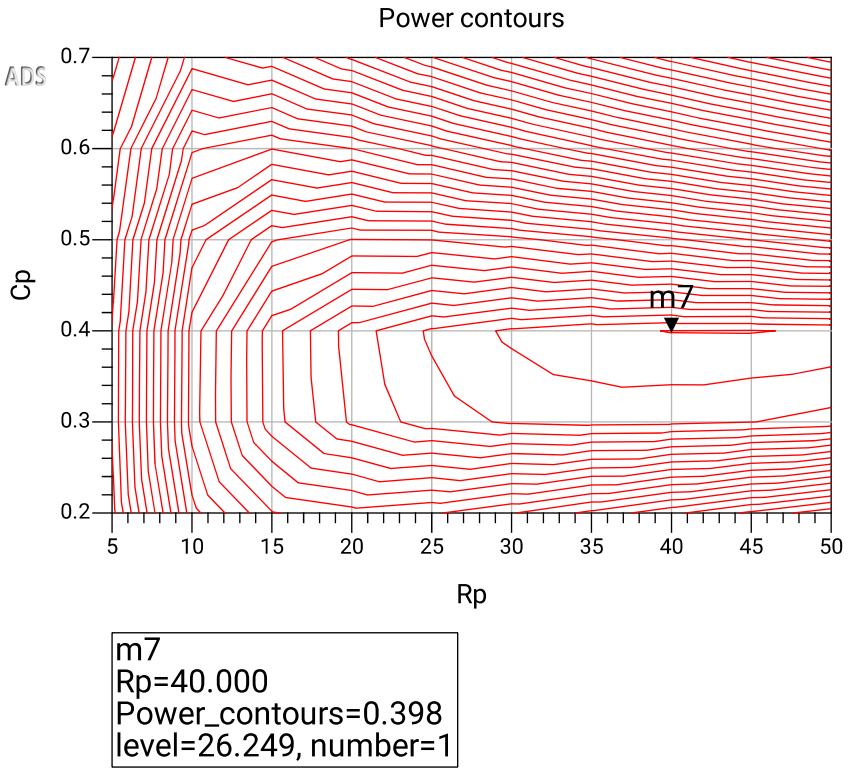


Figure 5.5: Driver power contours

Compared to the optimum power impedance of the primary PA ($R_p = 15\ \Omega$ and $C_p = 0.6$ pF), the driver stage needs a much larger load resistance (40 Ω versus

15 Ω). This is a direct result of the reduced transistor sizing used in the driver stage (two parallel transistors with 6×65 μm fingers, for a total gate periphery of 780 μm, compared to four parallel transistors in the primary stage with 6×80 μm fingers, for 1920 μm). It has lower maximum drain current capability ($I_{\max}$) due to the smaller total gate periphery of the driver stage. This is in accordance to load-line theory where the optimum load resistance is inversely proportional to $I_{\max}$ mentioned in eqn. 2.32.

As a result, the lower driver stage requires a significantly higher load resistance in order to swing its voltage efficiently. In addition, the optimal parallel capacitance for the driver stage is considerably smaller (0.4 pF vs. 0.6 pF). This is due to the smaller physical size of the driver HEMTs and thus much smaller intrinsic output parasitic capacitance (C_{DS}). Therefore, the matching network has to resonate out a much smaller capacitive reactance. This facilitates the physical design of the ISMN and helps to preserve a wider operating bandwidth.

Power Added Efficiency Contours

Figure 5.6 shows the PAE contours of the driver stage in the R_p–C_p plane. The maximum efficiency is 19.5% at $R_p = 45$ Ω and $C_p = 0.3$ pF. This overall efficiency is lower than that of the main stage, which achieves 47.5%, as expected since the driver stage is primarily designed to provide higher gain rather than maximize power conversion efficiency. Higher load resistances naturally limit the current swing.

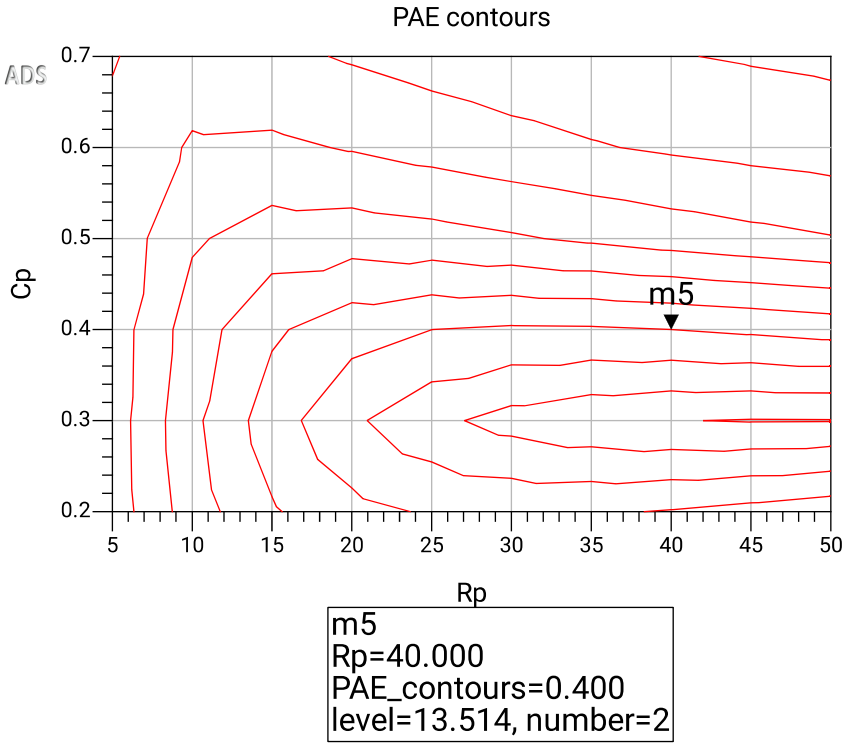


Figure 5.6: Driver power added efficiency

To maximize the power gain, a load impedance of $R_p = 40\ \Omega$ and $C_p = 0.4$ pF, indicated by marker m_5, was intentionally selected. At this load impedance, the driver stage achieves an efficiency of 13.5%, representing a trade-off between peak efficiency and gain.

Power Added Efficiency Vs Output Power

The PAE as a function of the fundamental P_{out} for the driver stage at the swept load impedances is shown in figure 5.7. Although, the other load terminations can provide higher peak efficiencies, reaching approximately 45%, the driver stage was designed to prioritize maximum power delivery rather than peak efficiency, ensuring sufficient drive power for the main amplifier stage. For the selected optimum load impedance of $R_p = 40\ \Omega$ and $C_p = 0.4$ pF, indicated by marker m_{15}, the driver stage achieves an output power of 30 dBm with a corresponding PAE of approx. 20%. This satisfies the required driver output power of approximately 30 dBm needed to drive the final PA stage to the desired operating condition.

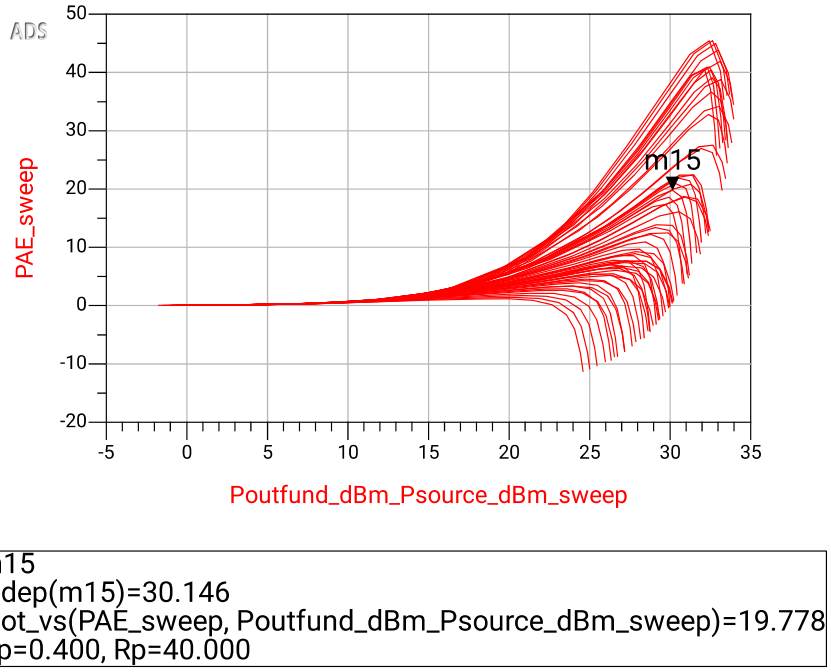


Figure 5.7: Driver PAE vs Pout

Gain Vs Output Power

The nonlinear AM–AM compression characteristic of the driver stage is shown in figure 5.8. Marker m_{13} indicates a linear small-signal transducer gain of 13 dB at an output power of 3.2 dBm. At an output power of 26 dBm, marker m_{14} indicates a gain of 11 dB, corresponding to approximately 2 dB of gain compression. The plot also confirms that, at a compressed gain of 8 dB, the driver delivers an output power of 30 dBm, which is the required input drive level for the final PA stage.

The gain of the driver stage is significantly higher than that of the main stage (13 dB versus 10 dB). This improvement is attributed to the smaller transistor dimensions, with gate width of 65 μm for driver stage versus 80 μm for final PA stage. The reduced transistor dimensions result in lower parasitic gate-to-source capacitance (C_{GS}), thereby improving the high-frequency performance at 40 GHz. Cascading the driver stage with the main stage results in an overall small-signal gain of more than 23 dB, providing sufficient margin to compensate for the insertion losses of the matching network and comfortably meeting the 20 dB system gain requirement.

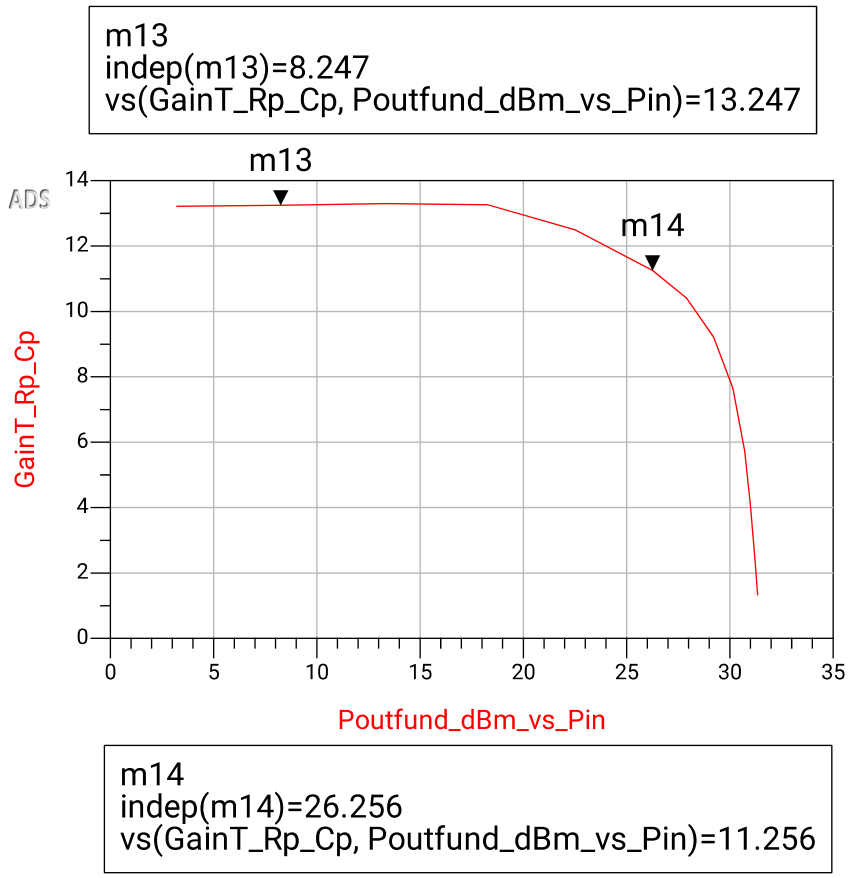


Figure 5.8: Driver gain vs power efficiency

One thing to note, for 30 dBm output power, driver transistors are in 5 dB compression. Due to this for higher frequencies gain and efficiency dropped, which we will see in section 5.3.2.

5.2 Simulations Results for Ideal Microstrip Two-Stage PA

The small signal parameters and large signal parameters (harmonic balance) simulation results for Ideal Microstrip Two-Stage PA design mentioned in Section 4.1

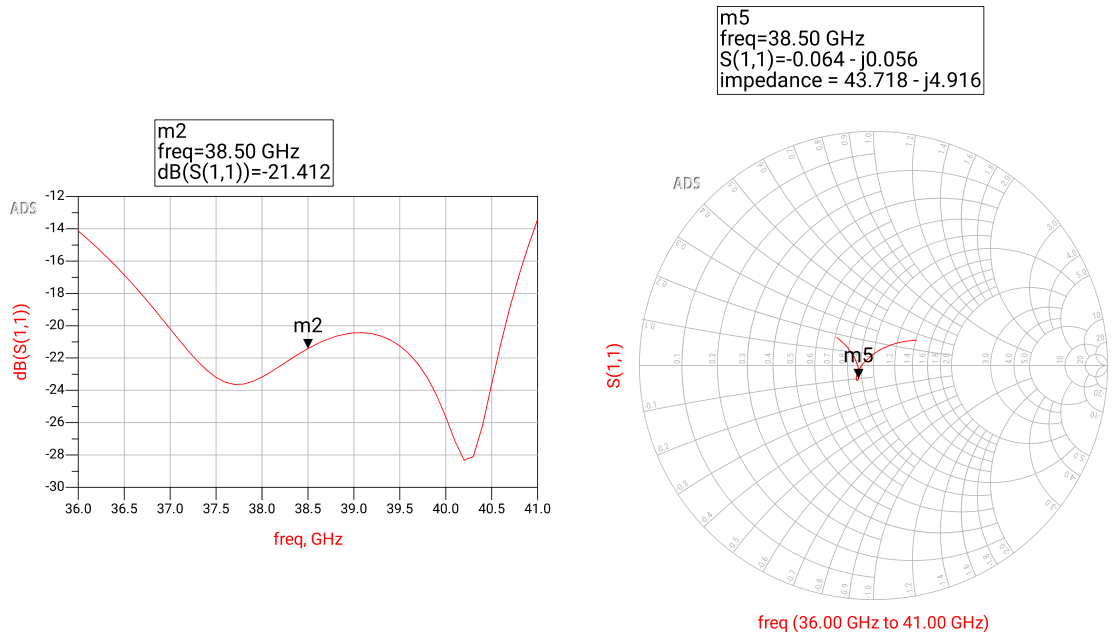
are discussed below.

5.2.1 Small Signal Parameters for Ideal Microstrip Two-Stage PA

Small signal parameters such as input return loss, impedance matching with Smith chart, gain and stability factor (K-factor) for OMN, ISMN and IMN are discussed below for frequency range 36 GHz to 41 GHz which is 1 GHz more than lower and higher frequency band limit.

Output Matching Network simulation results

The simulated small signal parameter of the OMN design in figure 4.2 is shown in figure 5.9.



(a) Return loss S_{11} of the OMN

(b) OMN reflection coefficient with Smith chart

Figure 5.9: OMN simulation results

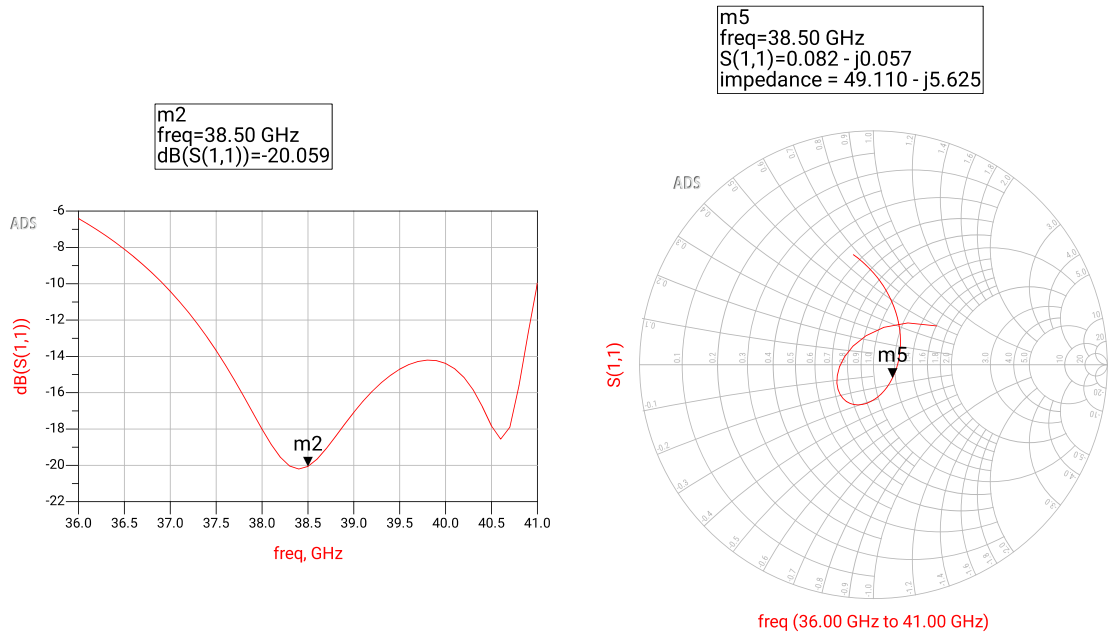
This is the return loss relative to the desired $R_p \parallel -C_p$ (15 Ω ∥ 0.6 pF) that the PA wants to see at the drain of the four parallel transistors. Hence, it shows how well the matching network transforms the 50 Ω port impedance to the desired load. The simulated input return loss, dB(S_{11}), and reflection coefficient of the OMN are shown in figure 5.9a and figure 5.9b. The network exhibits a broadband dual-resonant behavior. This behavior creates a tight loop on the Smith chart, resulting in a stable, low-reflection match across the entire 5 GHz operating bandwidth.

In general, the OMN provides a return loss better than 20 dB across the operating band. The excellent impedance match minimizes power reflection and is therefore

expected to result in transistor performance close to the optimum values predicted by the load-pull simulations.

Interstage Matching Network simulation results

The simulated small signal parameter for the ISMN design in figure 4.3 is shown in figures 5.10 and 5.11. To get correct output gain OMN is also added together with ISMN.

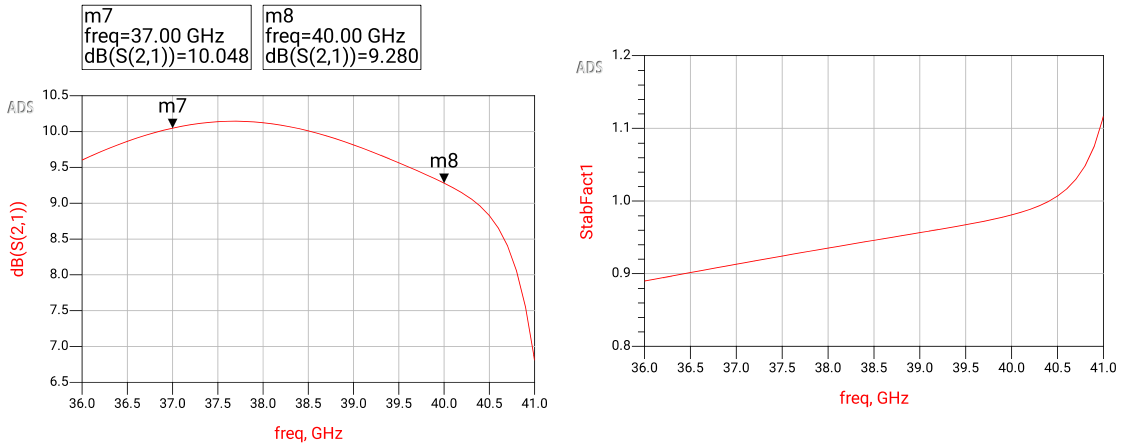


(a) Interstage return loss **(b)** Interstage S_{11} Smith chart

Figure 5.10: S11 simulation results of interstage matching network

This parameters are relative to the desired $R_{pd} \parallel -C_{pd}$ ($40\ \Omega \parallel -0.4$ pF) that the PA wants to see at the output of the driver stage. Hence, it shows how well the matching network transforms the $40\,\Omega$ driver impedance to a $1 - j2.4\,\Omega$ (Gate impedance at the 4 parallel transistors)inductive load.

The S_{11} response plotted in figure 5.10a in exhibits a dual-resonant behavior with a centered trajectory on the Smith chart and a return loss better than 14 dB over the 37.5–40.5 GHz range, reaching 20 dB at 38.5 GHz, corresponding to the impedance plotted in figure 5.10b. The Smith chart of the ISMN is normalized to 40 Ω instead of the standard 50 Ω system reference. The decision is based on the real output load impedance ($R_{pd} = 40\ \Omega$) seen by the driver stage, which reflects the true interstage transformation. The ISMN effectively compensates for the large gate capacitance of the four parallel output transistors, allowing the driver stage to see the desired optimum load impedance at its output.



(a) Interstage gain (S_{21})

(b) Interstage stability factor

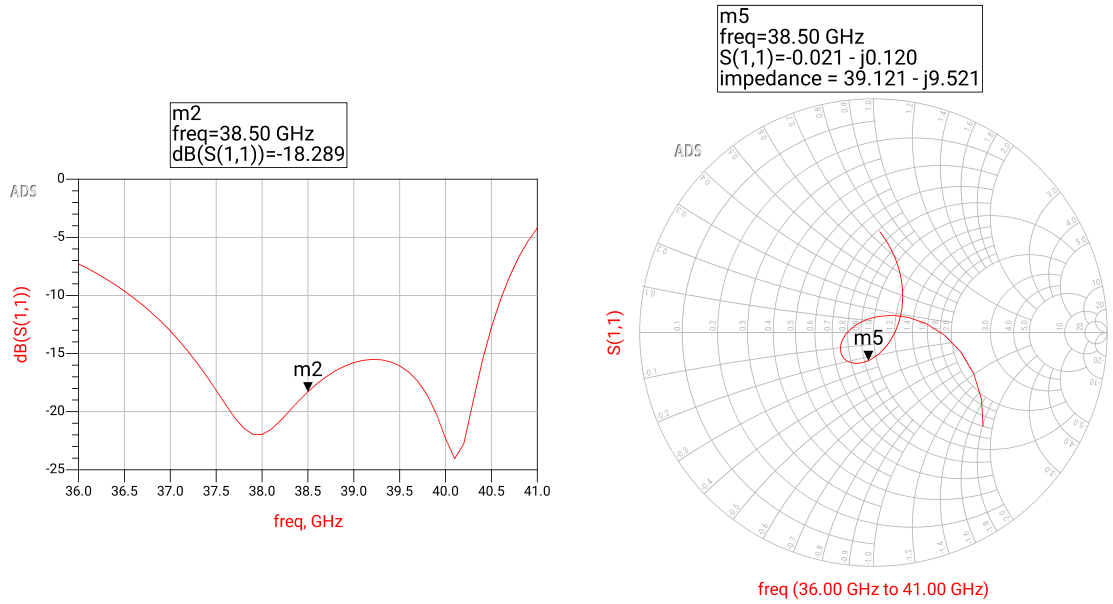
Figure 5.11: Gain and stability factor simulation results of interstage matching network

The S_{21} forward transmission exhibits a flat bandpass characteristic, with approximately 9.5 dB gain in operating band with less than 0.77 dB variation. The S_{21} response ensures that the ISMN provides sufficient power gain, consistent with the drive levels obtained from the load-pull simulations, to drive the final power stage into full saturation and achieve maximum output power.

Finally, the stability factor remains slightly above unity for operating frequency band due to the active transistor feedback capacitance and becomes unconditionally stable ($K > 1$).

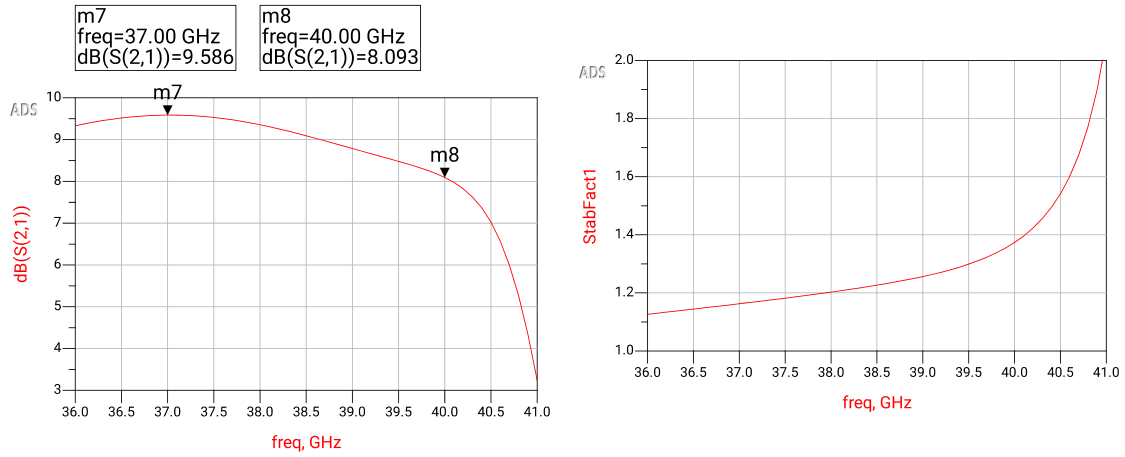
Input Matching Network (Driver Stage) simulation results

The simulated small signal parameter for the IMN design in figure 4.4 is shown in figures 5.12 and 5.13. To get correct output gain along with IMN, ISMN is also added in the design. This parameters are relative to the desired input impedance of (50 Ω) that the PA wants to see at the input port. Hence, it shows how well the matching network transforms the 50 Ω input impedance to a $1.86 + j1.28\,\Omega$ (Gate impedance at the driver stage transistors).



(a) IMN return loss **(b)** IMNS_{11} Smith chart

Figure 5.12: S11 simulation results of input matching network



(a) IMN gain (S_{21}) **(b)** IMN stability factor

Figure 5.13: Gain and stability factor simulation results of input matching network

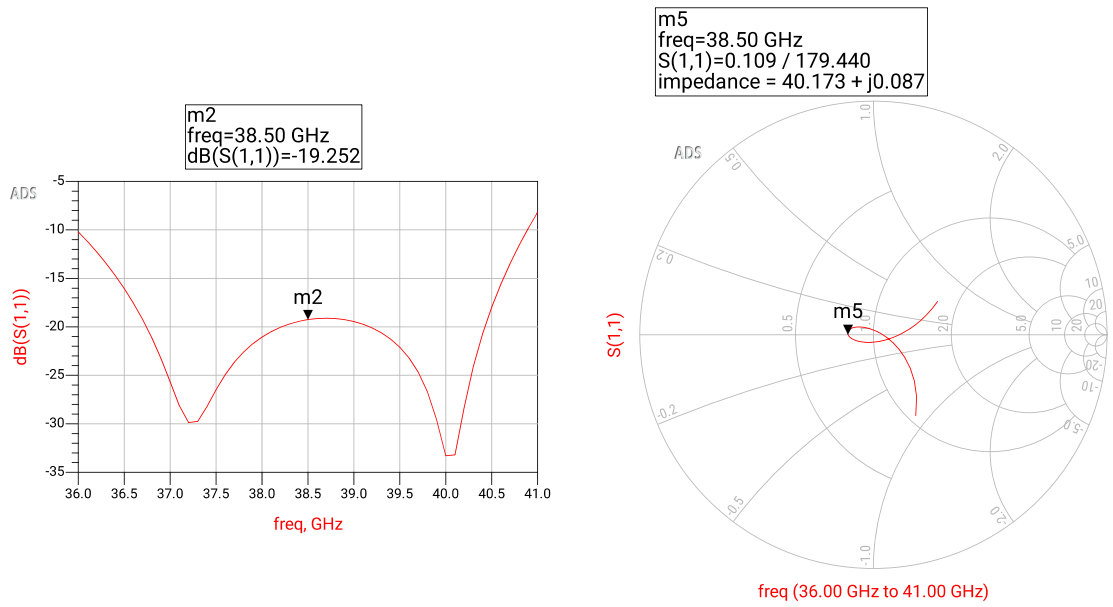
Here, the IMN and ISMN are simulated together to find the gain of driver stage. The S_{11} response plotted in figure 5.12a in relation to the 50 Ω source shows a wide band dual-resonant behavior with a return loss of above 15 dB at operating band with impedance $Z = 39 - j9.5$ Ω at 38.5 GHz the Smith chart (figure 5.12b)).

The results are overall very good. The forward gain S_{21} plotted in figure 5.13a shows $\sim$ 10 dB is precisely the sort of gain one expects from a single-stage driver at 40 GHz. Also, the K-factor is well above unity over the entire 36–41 GHz sweep (1.1 to 2), verifying unconditional stability of the driver stage.

One important point to note in interpreting these results is that to properly load the driver transistor and realize this $\sim$ 10 dB gain, it is necessary to include the ISMN in addition to the IMN. This robust single stage design ensures the entire multi stage amplifier will fulfill the target system gain which is 20 dB and power requirements when cascaded with the final PA stage.

Complete Ideal Microstrip Two-Stage PA simulation results

Figures 5.14 and 5.14 show the small-signal parameters for the complete basic PA design shown in figure 4.1 in relation to its primary design goals (20 dB gain, 20 dB return loss, centered Smith chart match and $K > 1$).



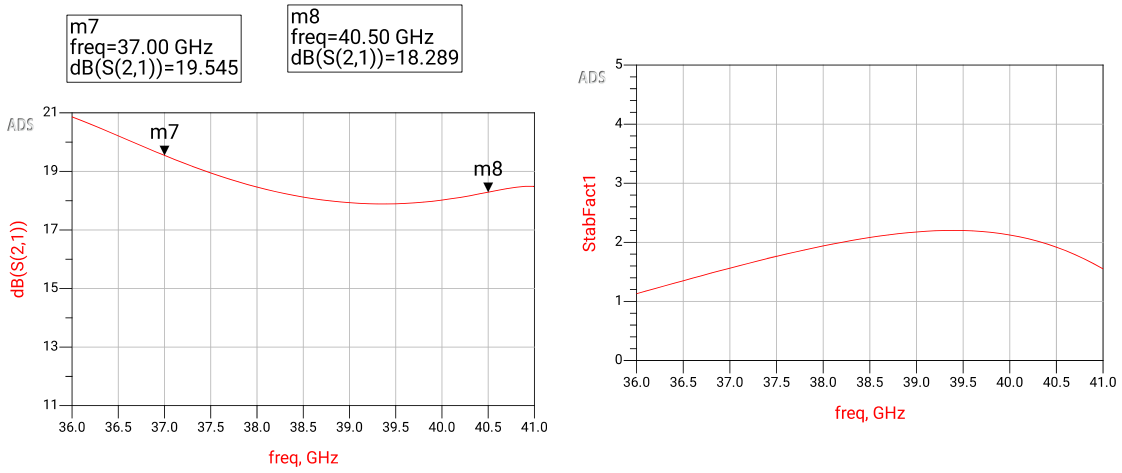
(a) Basic PA return loss

(b) Basic PA S_{11} Smith chart

Figure 5.14: S11 simulation results of basic PA

Overall, these results are very good as they are very close to all mentioned design goals. The small-signal gain ($\sim$ 19.5 dB) at lower pass-band frequency plotted in figure 5.15a is near the 20 dB target and the return loss (19 dB) plotted in figure. 5.14a and Smith chart trajectory match the ideal center match with less than 1.2% reflected power shown in figure 5.14b. Pass-band stability plotted in figure 5.15b where $K > 1$. However, because this plot is limited to the high-frequency range, it does not show the severe low-frequency instabilities that occur out-of-band and ultimately determine the need to incorporate parallel RC stabilization networks.

More thorough analysis of stability for wide-band from 1 to 50 GHz is done in Section 5.2.3.

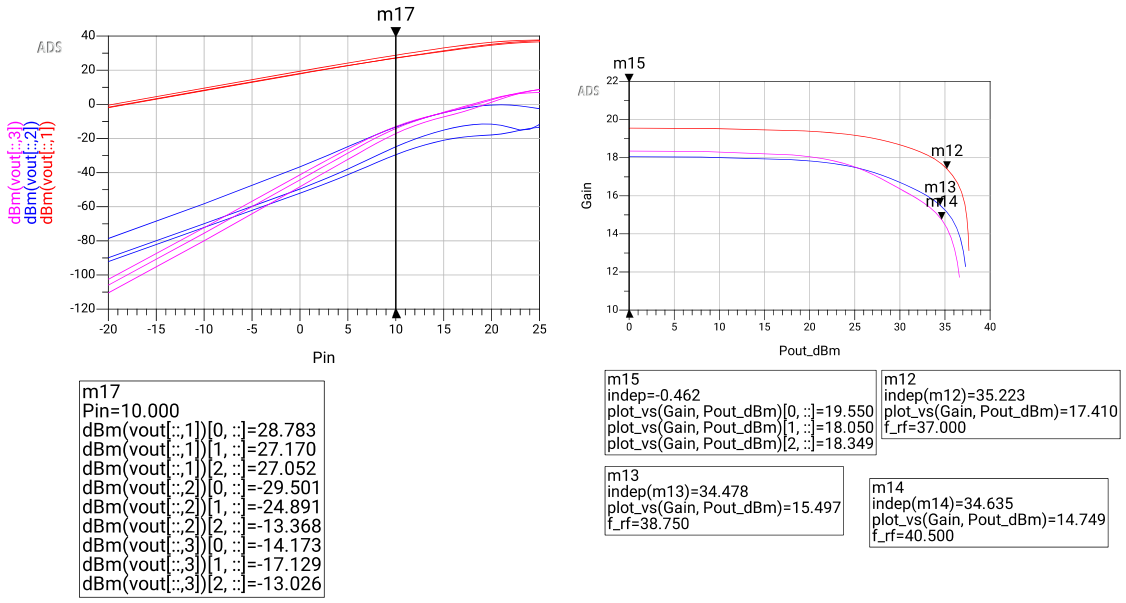


(a) Basic PA gain (S_{21}) **(b)** Basic PA stability factor

Figure 5.15: Gain and stability factor simulation results of basic PA

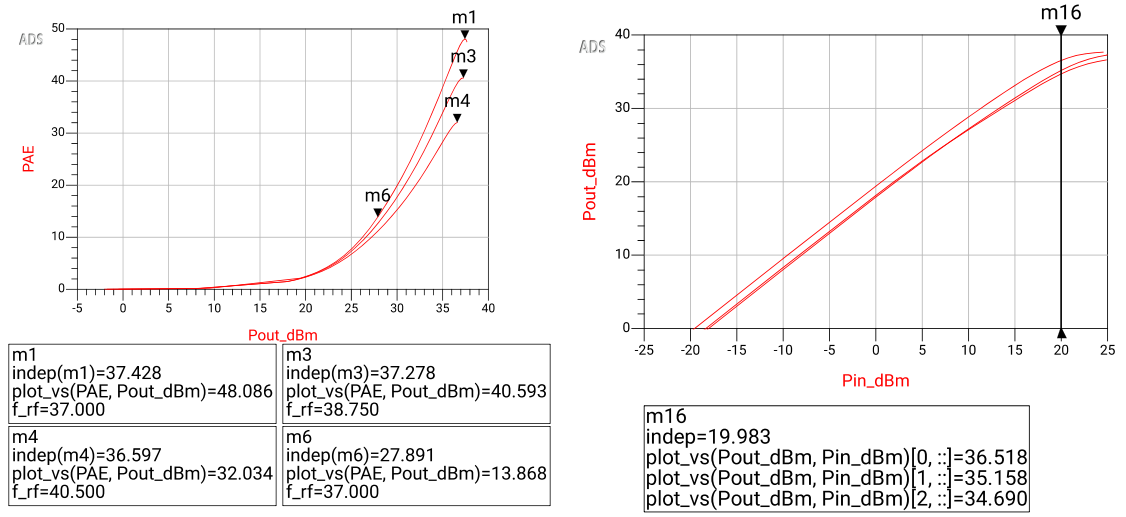
5.2.2 Large Signal Parameters for Ideal Microstrip Two-Stage PA Schematic

Figures 5.16 and 5.17 evaluate the large-signal performance, power distribution, compression behavior, and efficiency of the complete basic PA shown in figure 4.1 across three key frequencies (37 GHz, 38.75 GHz, and 40.5 GHz). At $P_{\text{in}} = -10$ dBm (marker m_{17}) shown in figure 5.16a, the internal power levels remain tightly grouped (27 dBm across branches), demonstrating strong corporate splitter amplitude balance that avoids branch overdrive and maximizes combining efficiency. Here, fundamental output power is well above second and third harmonics. The AM–AM gain compression curves plotted in figure 5.24b reflect a smooth transition into saturation at $P_{\text{out}} \sim 34\,\text{dBm}$, gain compresses by 2 dB is above 16 dB for all key three frequencies with highest around 20 dB. This gradual roll-off is ideal for minimizing spectral regrowth with high-PAPR signals.



(a) Basic PA output power spectrum **(b)** Basic PA gain compression curve

Figure 5.16: Basic PA schematic large signal simulation results 1



(a) Basic PA power added efficiency vs output power **(b)** Basic PA transfer characteristics

Figure 5.17: Basic PA schematic large signal simulation results 2

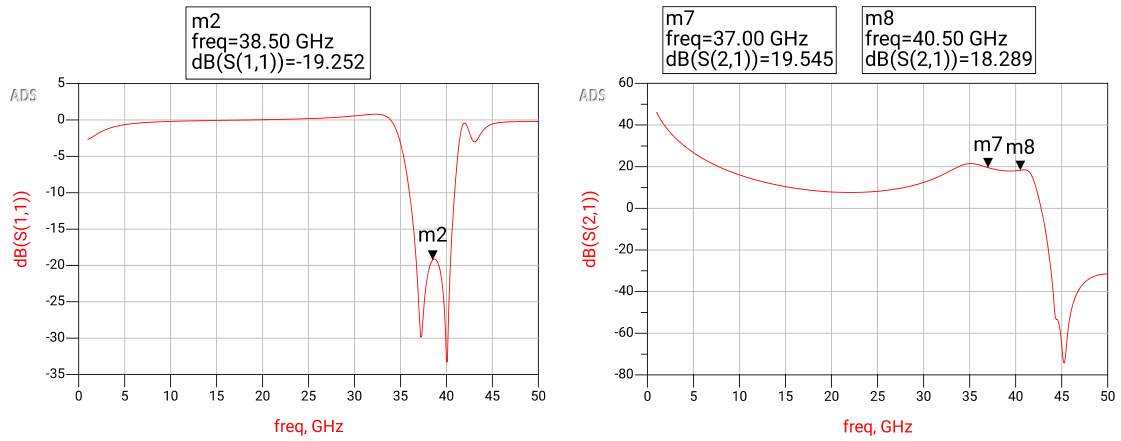
Concurrently, the PAE plotted in figure 5.17a achieves exceptional peaks above 32% across the band properly accounting for high-frequency parasitic roll-off and Maximum 10 dB P_{out} back-off PAE is $\sim$ 14%. The linear transfer curves plotted in

figure 5.17b begin bending past +15 dBm drive, delivering saturated output power approximately 35 dBm across the band and achieving ∼ 37 dBm at 37 GHz.

Overall, these results are good when measured against system design goals. Combined with balanced corporate power splitting, smooth large-signal compression, and high peak PAE (>40% over the majority of the pass-band), these findings confirm that the open/short stub networks and four-transistor parallel architecture are thoroughly optimized for 40 GHz operation.

5.2.3 Wideband Instability Analysis of Basic PA Design

A wideband S-parameter analysis of the basis PA design shown in figure 4.1, synthesized by open and short-circuited microstrip stubs, reveals critical out-of-band instability outside the target 37–40 GHz band.



(a) Return loss S_{11} for 1 GHz to 50 GHz frequency band

(b) Small signal gain for 1 GHz to 50 GHz frequency band

Figure 5.18: Return loss and small signal gain for 1 GHz to 50 GHz frequency band

Figure 5.18a shows the dB(S_{11}) response which reveals a severe anomaly between 30 and 34 GHz having a maximum return loss of ∼ +1 dB at ∼ 32.5 GHz although the return loss in-band is below 19 dB. Since dB(S_{11}) > 0 dB means $|S_{11}| > 1$, the amplifier has a negative input resistance and can reflect more RF power than is incident. This shows a clear potential for self-oscillation under non-ideal source terminations. This instability is associated with a severe low frequency gain expansion as shown in figure 5.18b. The in-band transducer gain is 19.5 dB at 37 GHz and ∼ 18 dB at 40.5 GHz (marker m_8), but the gain increases more than

+45 dB close to 1 GHz. This phenomenon is caused by the intrinsic low frequency gain of the GaN HEMTs where the gate-to-source capacitance (C_{gs}) has a high impedance and does not adequately shunt the input signal. The matching stubs are optimized for approximately 40 GHz and become very reactive at lower frequencies, thus providing a high-Q feedback path which can trigger low frequency oscillations.

To suppress such instabilities, a custom parallel RC stabilization network shown in figure 4.7a has been added in ISMN to remove positive reflection caused by OMN. Without stabilization, the PA can self-oscillate directly after biasing, at low frequencies (1–5 GHz) or near the band edge close to (27–33 GHz), which can affect circuit operation and device reliability. The lossy parallel RC bypass network, implemented with thin-film resistors and MIM bypass capacitors, provides a frequency-selective damping path. It presents about 1.2 dB of desired attenuation in low frequencies and band edges, so that the +45 dB out-of-band gain is suppressed and dB(S_{11}) is reduced below 0 dB. At the same time, the network provides a low loss bypass path with only about 0.26 dB loss at 40 GHz while maintaining the required in-band gain and return-loss performance.

5.3 Simulations Results for Layout-Realizable Schematic Design of Two Stage PA

The small signal parameters and large signal parameters (harmonic balance) simulation results for layout-realizable schematic design of two stage PA mentioned in Section 4.2 are discussed below.

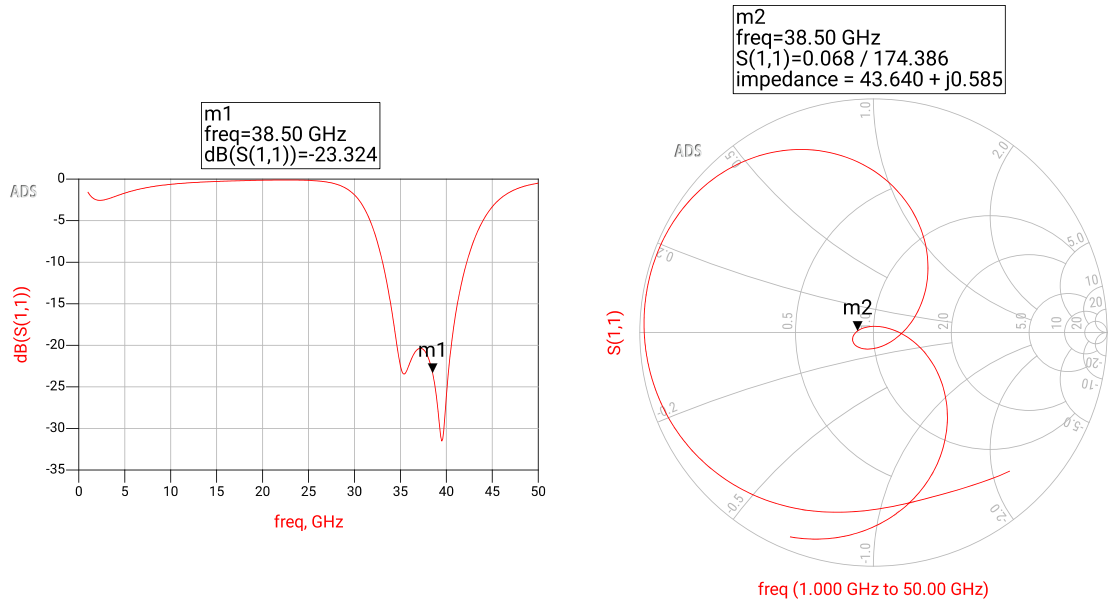
5.3.1 Small Signal Parameters for Layout-Realizable Schematic Design of the Matching Networks

Small signal parameters such as input return loss, impedance matching with Smith chart, gain and stability factor for OMN, ISMN and IMN for layout-realizable schematic design are discussed below for frequency range 1 GHz to 50 GHz.

Output Matching Network Schematic Simulation Results

The simulated small signal parameter of OMN design in figure 4.5 is shown in figure 5.19. This is the return loss relative to the optimum impedance $R_p \parallel -C_p$ (15 Ω ∥ 0.6 pF) that the PA wants to see at the drain of the four parallel transistors. Hence, it shows how well the matching network transforms the 50 Ω port impedance to the desired load. Impedance matching is same as the OMN section mentioned in Section 5.2.1 with Layout-Realizable Schematic of OMN network.

Figure 4.5 shows the simulated return loss (dB(S_{11})) plotted in figure 5.19a and Smith chart reflection trajectory for the layout-realizable OMN schematic plotted in figure 5.19b over 1–50 GHz. Overall, these results show an excellent agreement with ideal expectations, maintains the main dual-resonant profile with the return loss more than 20 dB across the pass-band shown in figure 5.9a and impedance



(a) OMN schematic return loss S11

(b) OMN schematic reflection coefficient with Smith chart

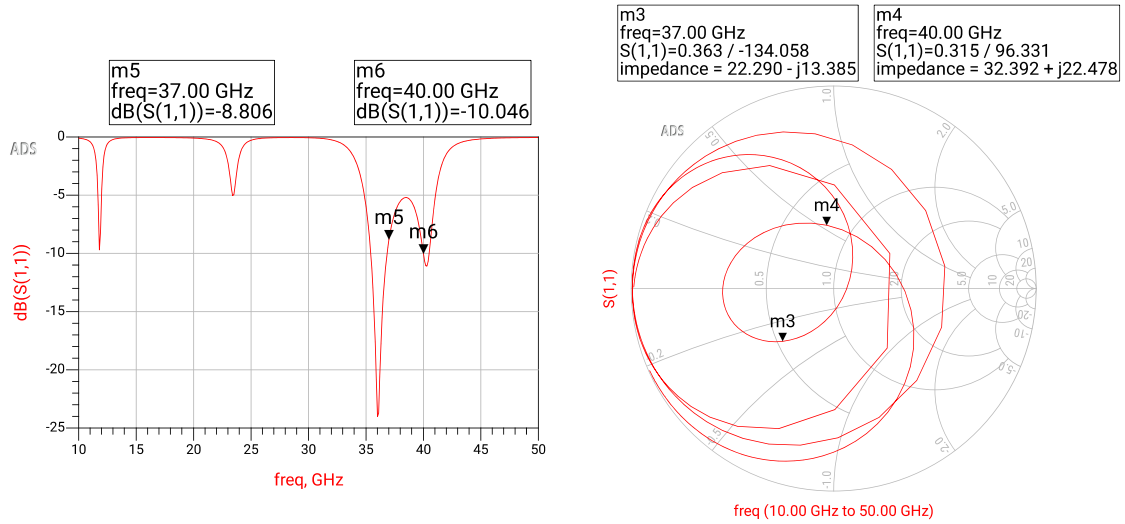
Figure 5.19: Output matching network schematic simulation results

matching is close to 50 Ω as shown in figure 5.19b; these results are more or less same as the results of ideal OMN shown in figure 5.9a.

Interstage Matching Network simulation results

Figure 5.20 and figure 5.21 shows the performance simulation of the layout-realizable ISMN schematic design shown in figure 4.8 with integrated parallel RC stabilization network. The transition from the ideal ISMN to a physical layout model introduces parasitic effects that may cause out-of-band positive reflection (oscillation risks) around 27–34 GHz shown in figure 5.18a of section 5.2.3. The parallel RC network shown in figure 4.7a suppresses these resonances, ensures the return loss above 0 dB in the 10–50 GHz frequency range, and stabilizes the network without significantly degrading the pass-band power transfer.

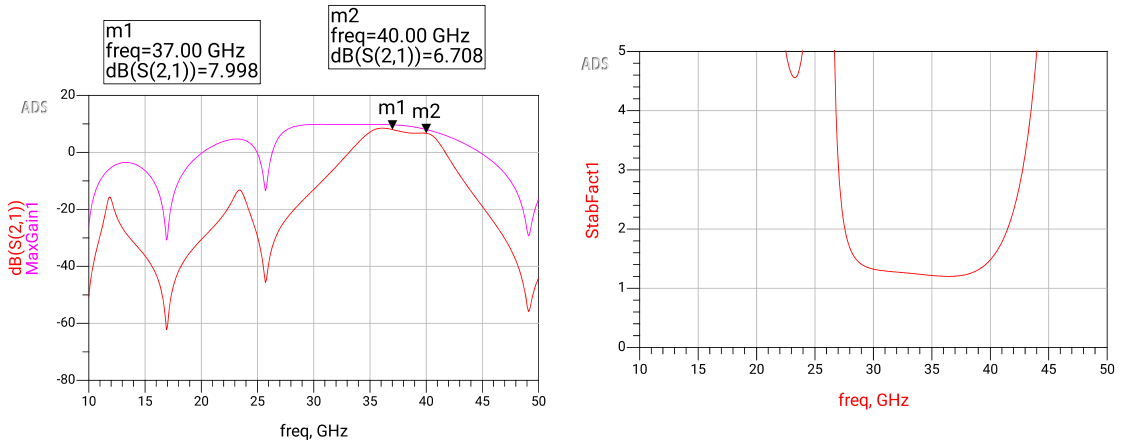
Return loss plotted in figure 5.20a is better than 5 dB across the operating band. The Smith chart plotted in figure 5.20b shows impedance matching close to 40 Ω (optimum load impedance). The ideal ISMN produced a deeper S_{11} notch (< -20 dB) shown in figure 5.10a close to 38.5 GHz, but the layout model trades some match depth for strong wideband damping to safely match the driver output to the low gate impedance of the final stage.



(a) ISMN schematic return loss S11

(b) ISMN schematic reflection coefficient with Smith chart

Figure 5.20: Interstage matching network schematic S11 simulation results



(a) ISMN schematic S21 gain

(b) ISMN schematic stability factor

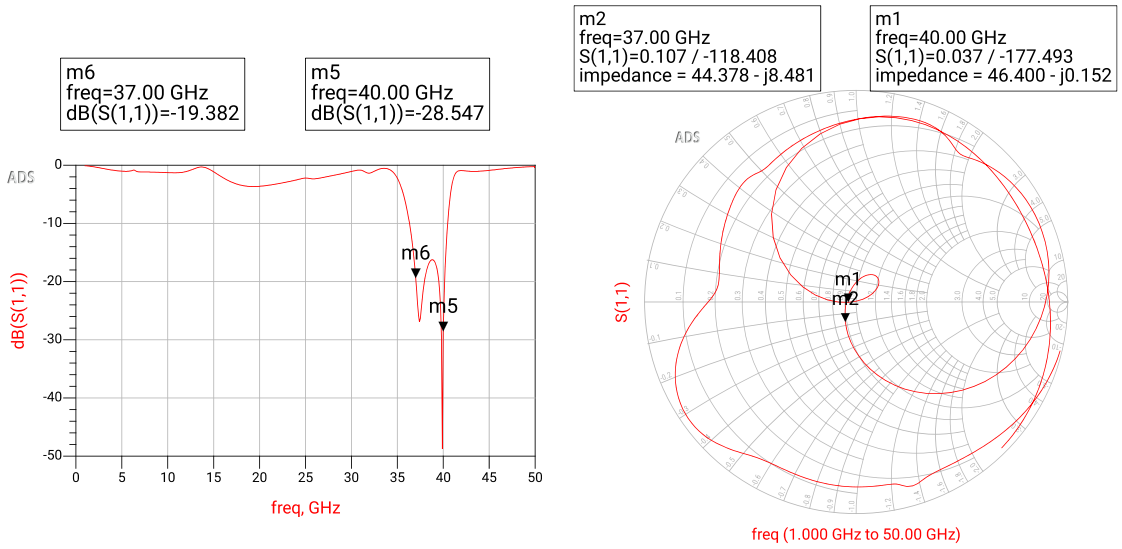
Figure 5.21: Interstage matching network schematic gain and K-factor simulation results

The forward gain (S_{21}) plotted in figure 5.21a and the stability factor plotted in

figure 5.21b confirms the overall effectiveness of the network. S_{21} offers approx 7 dB gain in the operating band with highest is around 8 dB at 37 GHz to provide enough drive power to the final stage. This is lower than ideal ISMN gain Shown in figure 5.11a (above 9 dB gain in the operating band) due to addition of stability network. Importantly, the K-factor is strictly above 1 across the whole 10–50 GHz, which proves the efficacy of the RC network in eliminating out-of-band instability and guaranteeing unconditional stability.

Complete PA Schematic simulation Results

As IMN schematic along with ISMN and OMN shown in figure 4.9 is nothing but schematic of layout-Realizable two-stage PA. Small signal simulation result for PA schematic (figure 4.9) is shown in figure 5.22 and figure 5.23 over 1–50 GHz.



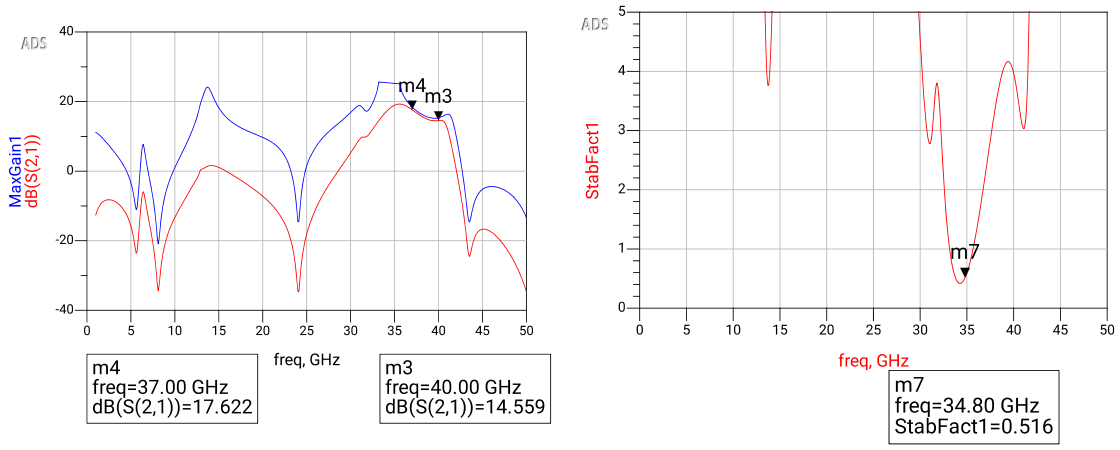
(a) PA schematic return loss S11

(b) PA schematic reflection coefficient with Smith chart

Figure 5.22: PA schematic S11 simulation results

The layout schematic fulfills the design goals in the following way: the input return loss is $>$ 16 dB for operating frequency band shown in figure 5.22a , the input impedance is directly mapped in the middle of the Smith chart (46 Ω with almost zero reactance) shown in the figure 5.22b , and the pass-band stability is preserved completely also as mentioned in Section 3.6 K-factor stability is not accurate for the Multistage- PA, we added WS probe to check stability of the transistors. The gain is approximately over 15 dB for the operating band shown in the figure 5.23a. The expected gain drop as compared to figure 5.15a ($\sim$ 18–19.5 dB) is due to addition of stability network also changes in interstage network to suppress out-of-band instability, make it layout-realizable and allow driver biasing made it difficult to achieve

same performance. These results provide a good and realistic baseline before the final EM co-simulation.

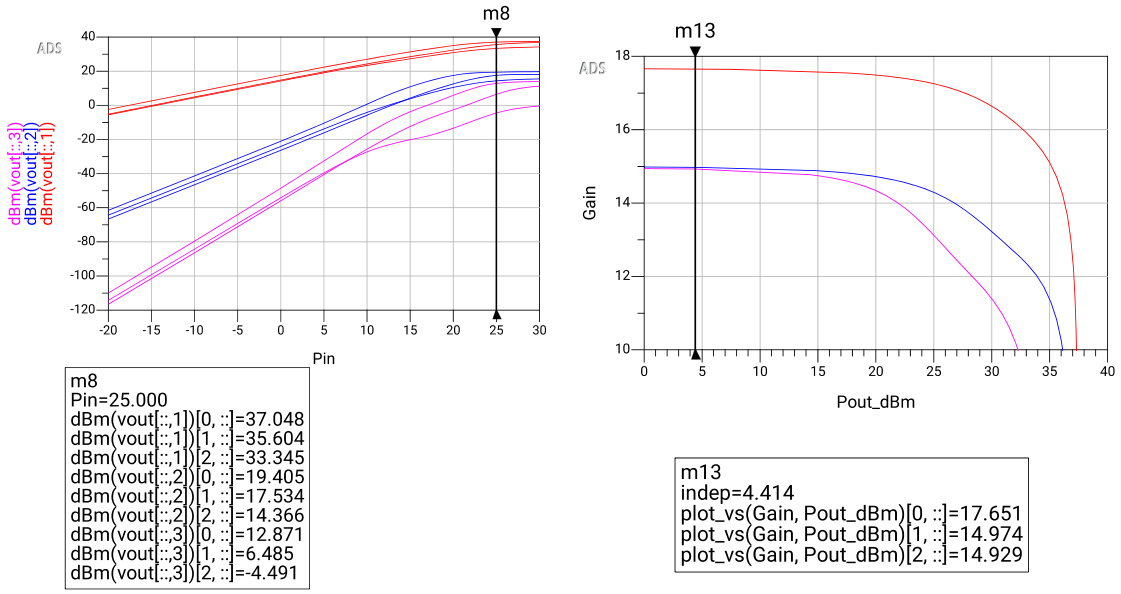


(a) PA schematic S21 gain **(b)** PA schematic stability factor

Figure 5.23: PA schematic gain and K-factor simulation results

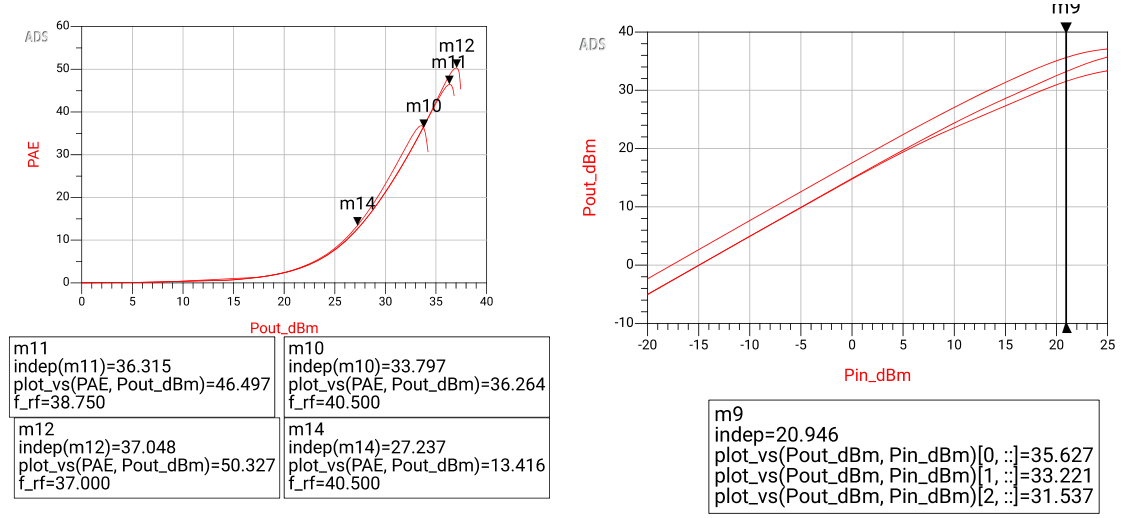
5.3.2 Large Signal Parameters for Layout-Realizable Two-Stage PA Schematic

The large-signal performance, gain compression, PAE and transfer characteristics of the layout-realizable PA schematic design (figure 4.9) are shown in figures 5.24 and 5.25. The maximum output power is 37 dBm at the lower end of the band but drops to around 34 dBm at the high end the output spectrum plotted in figure 5.24a. In the linear small-signal regime plotted in figure 5.24b the large-signal gain is above $\sim$ 15 dB for operating frequency band. It can also be observed from figure 5.24b that there is approximately a 5 dB reduction in output power from the lower to the higher frequencies. This reduction is due to the driver stage entering compression earlier at higher frequencies, which limits its ability to deliver sufficient output power to the final PA stage (section 5.1.2). Transfer curves plotted in figure 5.25b show output powers is above of 31.5 dBm for operating frequency band.



(a) PA schematic output power spectrum **(b)** PA schematic gain compression curve

Figure 5.24: PA schematic large signal simulation results 1



(a) PA schematic power added efficiency **(b)** PA schematic transfer characteristics vs output power

Figure 5.25: PA schematic large signal simulation results 2

As shown in the PAE plots (figure 5.25a), the efficiency performance is still robust over the pass-band, achieving PAE above 36% for all operating frequencies and 10 dB P_{out} back-off PAE is $\sim$ 14%. The layout-realizable schematic has slightly

lower gain and efficiency compared with the ideal PA (peak PAE reduced from 48% to 45% and power gain reduced from 17 dB to 15 dB (figures 5.16 and 5.17)). The reduction is mainly due to losses in the physical microstrip lines (conductor and dielectric), insertion losses of T-junctions and cross-junctions, parasitic step-discontinuities and interstage loading/mismatch effects, which are present in the layout-realizable schematic but not in the ideal component model.

Overall these results are positive. The output power is lower at the higher part of the band. This is because the interstage networks gives non-optimal load impedance to the driver stage causing it to saturate before the final stage. This could be remedied by choosing larger transistors or different load impedance for the driver stage. This design achieves an output power close to $\sim$ 37 dBm (close to the $\sim$ 5 W target) as shown in figure 5.24a, maintains good gain (15–17.6 dB) and provides excellent peak PAE (>36%). The AM-AM compression curves exhibit a smooth roll-off, indicating good linearity properties and confirming that the use of realizable microstrip topologies instead of ideal matching networks maintains a strong large-signal performance and offers a reliable baseline for the final EM simulation.

5.3.3 Stability Analysis Results Layout-Realizable Two-Stage PA Schematic

Stability analysis results using Ohtomo loop gain and kurokawa driving point admittance for layout-Realizable two-Stage PA schematic are explained in below section. For Ohtomo loop gain and kurokawa driving point admittance analysis WS probe is used at input and output of the transistors. Input power used for this stability analysis is -10 dBm RF power. This stability analysis is done for $50\,\Omega$ load impedance.

Ohtomo Loop Gains:

The encirclement plot, which is the plot of the number of clockwise encirclements of the critical $1 + j0$ point as a function of frequency, is obtained by applying the Nyquist stability criterion to the multi-node Ohtomo loop gains.

For a closed loop system to be stable, the total number of encirclements must be zero. In practical, the total number of encirclements should be below one. This plot gives the mathematically rigorous single-trace validation of the internal stability of the amplifier, thereby simplifying the analysis of the complicated 12-port active core. As shown in figure 5.26 the encirclements are near zero, which means that the system is stable [18].

The open-loop transfer functions for each individual transistor are plotted on polar S-plane charts using virtual non-invasive probes at the gate and drain terminals of all six transistors ('WSP1' to 'WSP12'). According to Nyquist stability criterion, if any of these loop gains encircle the critical point $1 + j0$ in clockwise direction, the system is unstable and will oscillate. The loop gain polar plots are plotted in figure 5.27, where polar plots have large, wide sweeping loops. There is no encirclement at the critical point $1 + j0$, This indicate that the design is stable.

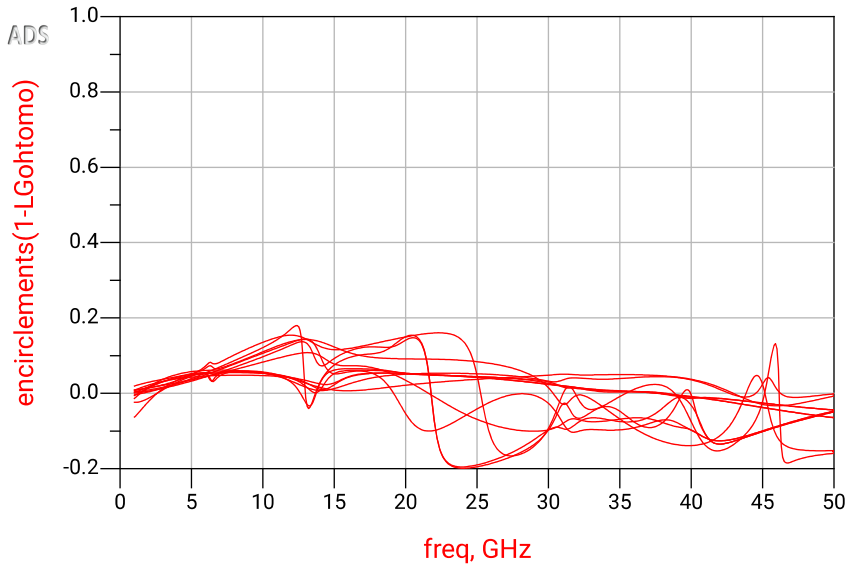


Figure 5.26: PA schematic encirclement plot

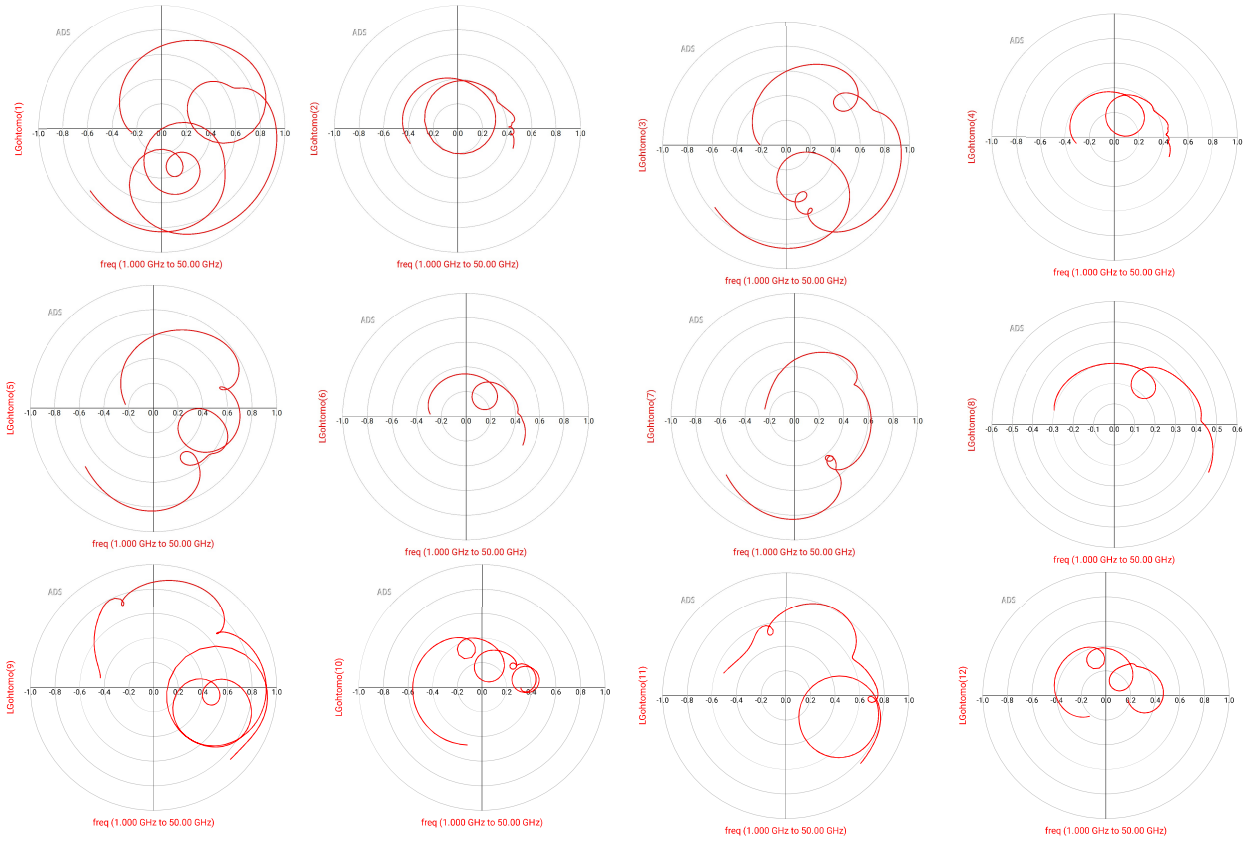


Figure 5.27: PA schematic Ohtomo loop gain polar plots

Kurokawa Driving Point Admittance:

The Kurokawa driving point admittance curves represent the real and imaginary parts of the input/output admittances at all active device terminals.

The circuit is stable throughout the frequency spectrum as shown in figure 5.28 for which the real part of the driving-point admittance satisfies $\mathrm{Re}\{Y_{in}(\omega)\} > 0$ for all traces and the network is thus fully dissipative, i.e., is not equipped with the required net negative conductance, $\mathrm{Re}\{Y_{in}\} \leq 0$, to initiate or sustain regeneration. Thus, there are no zero-crossings where an oscillation equilibrium point could exist ($\mathrm{Re}\{Y_{in}\} = 0$ and $\mathrm{Im}\{Y_{in}\} = 0$) and Kurokawa's dynamic derivative stability condition, $\frac{\partial G_d}{\partial V}\frac{\partial B_l}{\partial \omega} - \frac{\partial B_d}{\partial V}\frac{\partial G_l}{\partial \omega} > 0$, is inherently bypassed; without a physical locus intersection between the active device and the load, a perturbation cannot trigger a runaway feedback loop, ensuring absolute linear stability. This analysis is also supported by table 5.29, where there is no instability for any of the twelve check points [18]

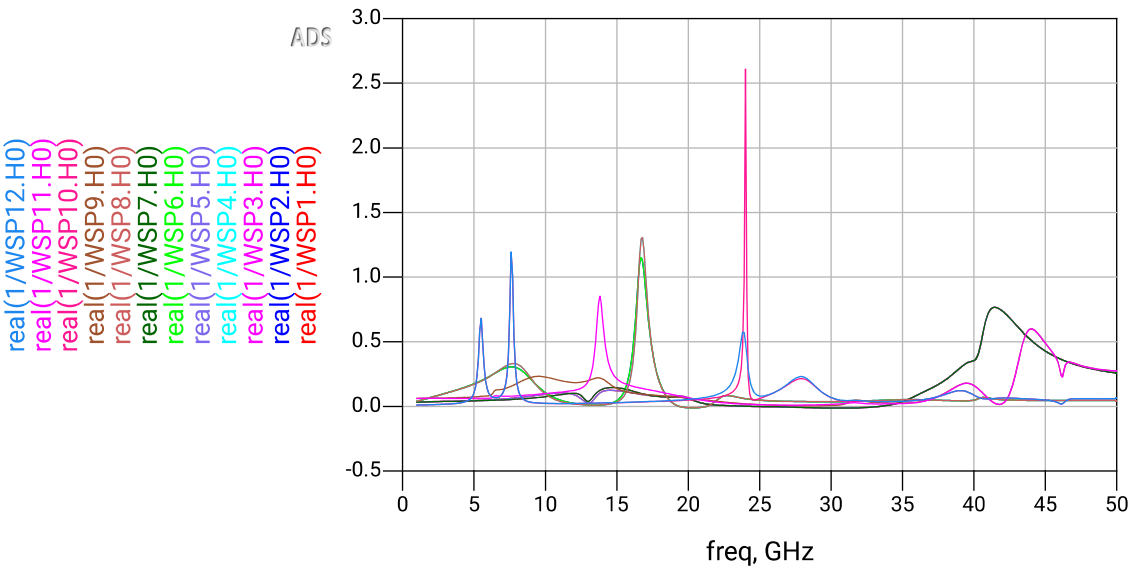


Figure 5.28: PA schematic Kurokawa driving point admittance

Kurokawa_D1	Kurokawa_D2	Kurokawa_D3	Kurokawa_D4	Kurokawa_D5	Kurokawa_D6	Kurokawa_G1	Kurokawa_G2	Kurokawa_G3	Kurokawa_G4	Kurokawa_G5	Kurokawa_G6
0	0	0	0	0	0	0	0	0	0	0	0

Figure 5.29: PA schematic Kurokawa frequency counter

5.4 Simulations Results for Realization of PA Design Based on EM-Model Integrated Top-Level Layout

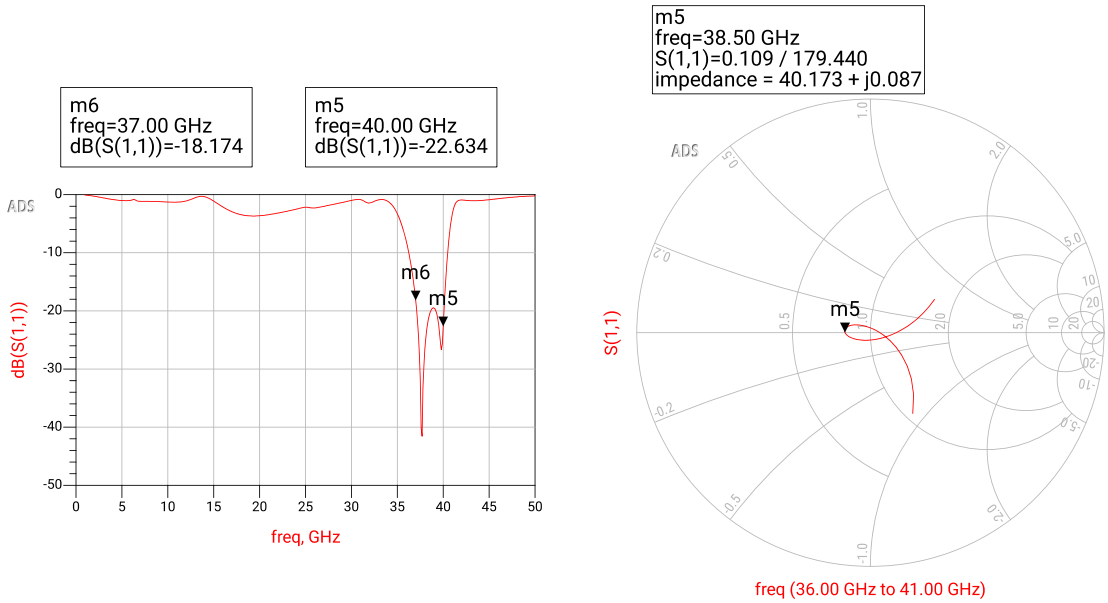
The small signal parameters and large signal parameters (harmonic balance) along with stability analysis simulation results for EM model of OMN, ISMN and IMN in final PA design are discussed below.

5.4.1 Small Signal Parameters Simulation Results for PA EM model

In this case, with reference to figure 4.9 each matching network is successively converted into an electromagnetic (EM) model to evaluate its small-signal performance. First, only the OMN is converted into an EM model while ISMN and IMN are preserved as schematics. Then, both OMN and ISMN are simulated as EM models together with the schematic IMN. Finally, all three matching networks are transformed into full EM models as shown in figure 4.10 and the complete cascaded results are recorded.

Output Matching Network EM Simulation Results for PA EM model

The simulated small signal performance of the PA using the EM-modeled OMN with the schematic IMN and ISMN is shown in figures 5.30 and 5.30.



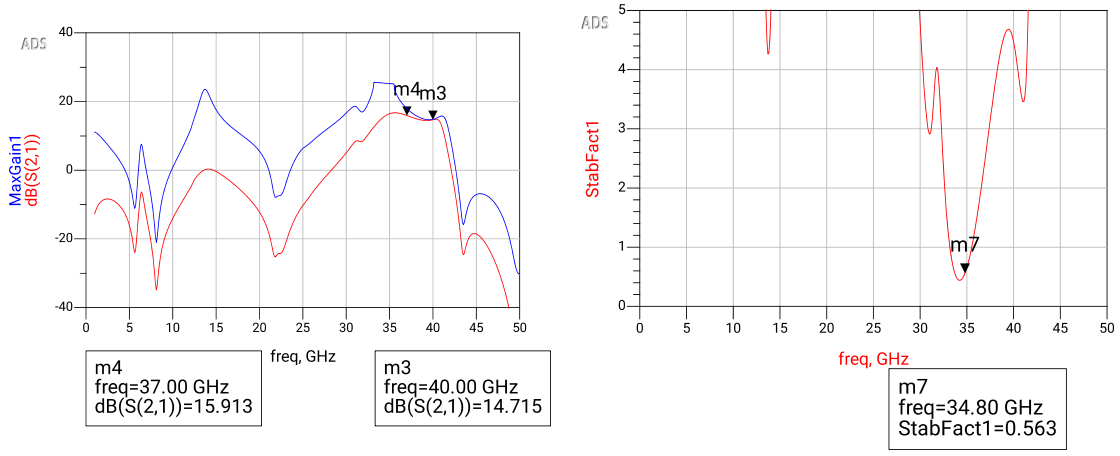
(a) OMN EM model return loss **(b)** OMN EM model S_{11} Smith chart

Figure 5.30: OMN EM Model with ISMN and IMN schematic model S11 simulation results

The input matching performance is similar to the OMN schematic (above > 18 dB return loss for operating band frequencies) as shown in figure 5.30a

Transducer gain (S_{21}) shown in figure 5.31a is approximately 15 dB across the operating band with highest achieved gain of $\sim$ 16 dB. This gain is slightly lower than the ideal PA design ($\sim$ 18–20 dB) and the layout-realizable schematic PA ($\sim$ 15–18 dB). The expected gain drop is due to physical EM attenuation, intentional RC stabilization loading and fixed layout geometries (e.g. MTEE, MCROSS) limiting further matching optimization.

Overall, the results validate the proper operation of the EM-modeled OMN and its robust and stable wide-band matching. The K-factor in figure 5.31b is stable in the operating band. further stability analysis for non linearity is done in section 5.4.3.

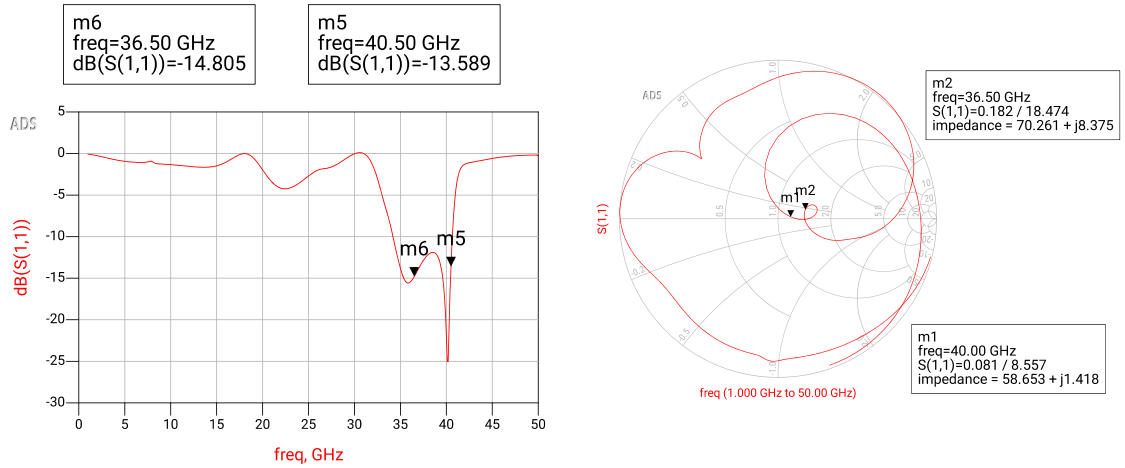


(a) OMN EM model gain (S_{21}) **(b)** OMN EM model stability factor

Figure 5.31: OMN EM Model with ISMN and IMN schematic model gain and K-factor simulation results

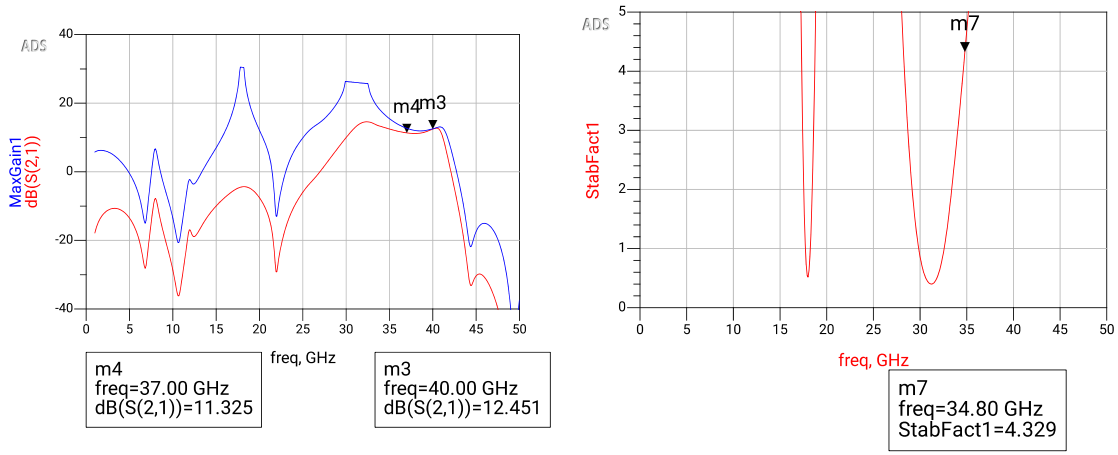
Output and Interstage Matching Network EM Model with schematic IMN model Simulation Results for PA EM model

The small signal simulation performance of the PA with EM models for both OMN and ISMN together with a schematic IMN are presented in figures 5.32 and 5.33.



(a) OMN ISMN EM model return loss **(b)** OMN ISMN EM Model S_{11} Smith chart

Figure 5.32: OMN ISMN EM model with IMN schematic model S11 simulation results



(a) OMN ISMN EM model gain (S_{21}) **(b)** OMN ISMN EM model stability factor

Figure 5.33: OMN ISMN EM model with IMN schematic model Gain and K-factor simulation results

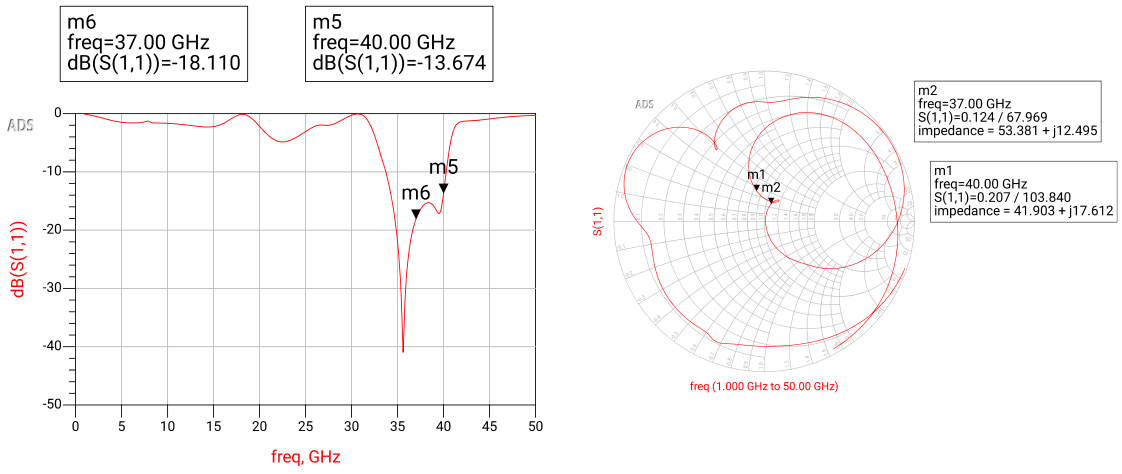
The input return loss plotted in figure 5.32a is above 13dB in the operating band. This dual-EM setup shows a clear gain loss ($\sim$ 11.5–12.5, dB gain) as shown in figure 5.33a compared to the ideal PA ($\sim$ 18–19.5, dB gain), the layout realizable schematic PA ($\sim$ 15–18, dB gain), and the OMN-only EM model ($\sim$ 15–16, dB gain). This is because ISMN is highly susceptible to small model inaccuracies which

reduce the gain and increase the out-of-band instability. A significant contributor to this difference between the schematic and EM results is also the fixed microstrip layout elements (e.g. MTEE, MCROSS, MCURVE and corner junctions) cannot be dynamically varied or re-optimized within the EM model and therefore the interstage impedance transformations cannot be fine-tuned. The K-factor in figure 5.33b is stable in the operating band.

Output, Interstage and Input Matching Network EM Model Simulation Results for PA EM model

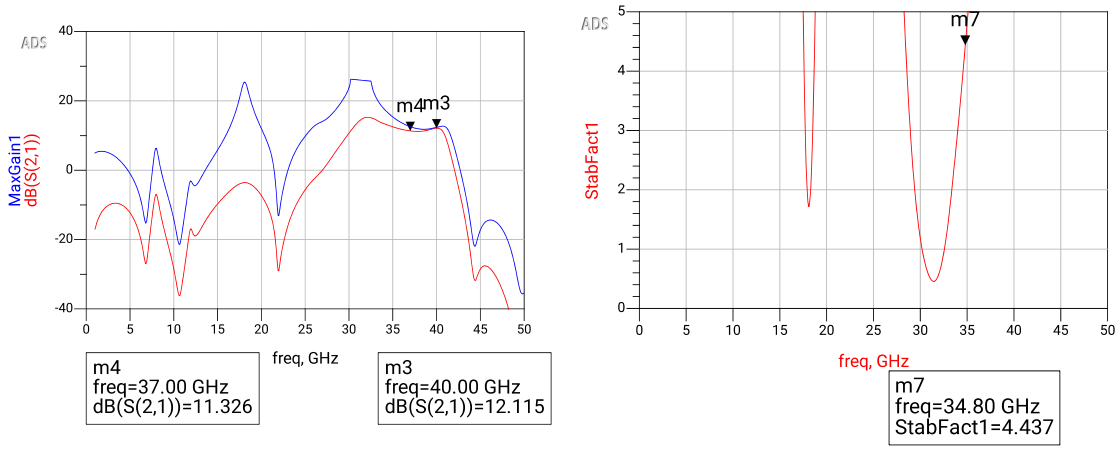
The performance of the complete multi-stage PA with the full EM simulation of all three matching networks i.e., IMN, ISMN, and OMN (figure 4.10) is shown in figures 5.34 and 5.34.

Overall, these results are very good for a full 3D EM model of a millimeter-wave PA. The input return loss (S_{11}) plotted in figure 5.34a exhibits a dual-resonant band-pass shape with above 16 dB at operating band, while the Smith chart trajectory (figure 5.34b) shows a tight double-tuned loop around the center.



(a) Final PA output return loss **(b)** Final PA output S_{11} Smith chart

Figure 5.34: Final PA output with all matching network EM models S11 simulation results



(a) Final PA output gain (S_{21}) **(b)** Final PA output stability factor

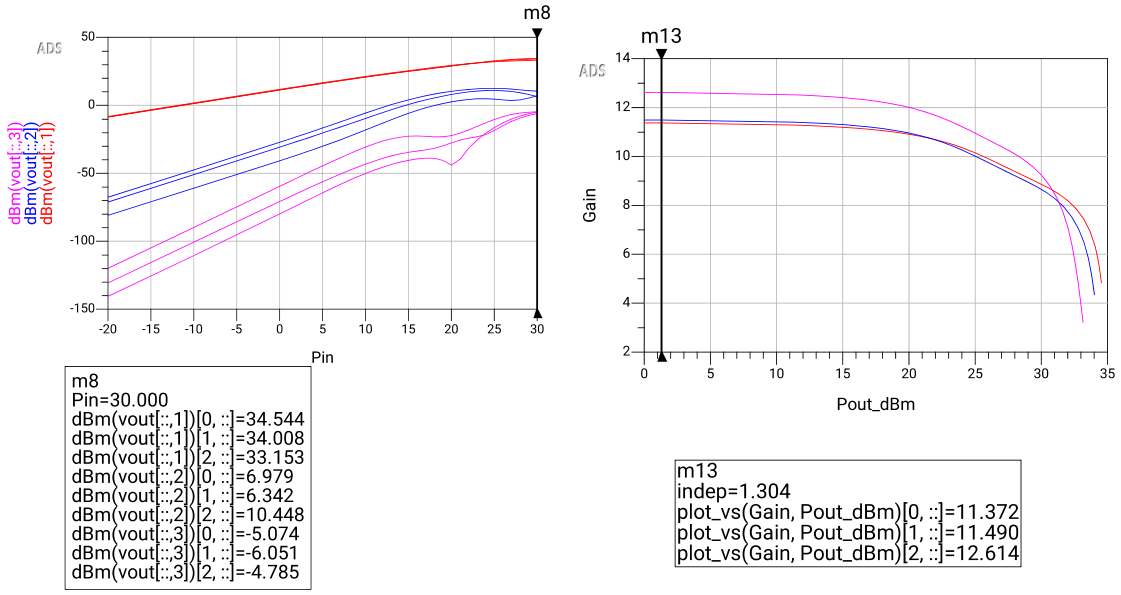
Figure 5.35: Final PA output with all matching network EM models gain and K-factor simulation results

The full EM gain ($\sim$ 11–12 dB) shown in figure 5.35a naturally falls below the 20 dB small-signal target when comparing across design iterations, from the ideal PA ($\sim$ 18–20 dB gain), layout-realizable schematic PA ($\sim$ 15–18 dB gain). The anticipated reduction is due to sensitive interstage network and also the fixed microstrip layout geometries (MTEE, MCROSS, MCURVE).

5.4.2 Large Signal Parameters Simulation Results for PA EM model

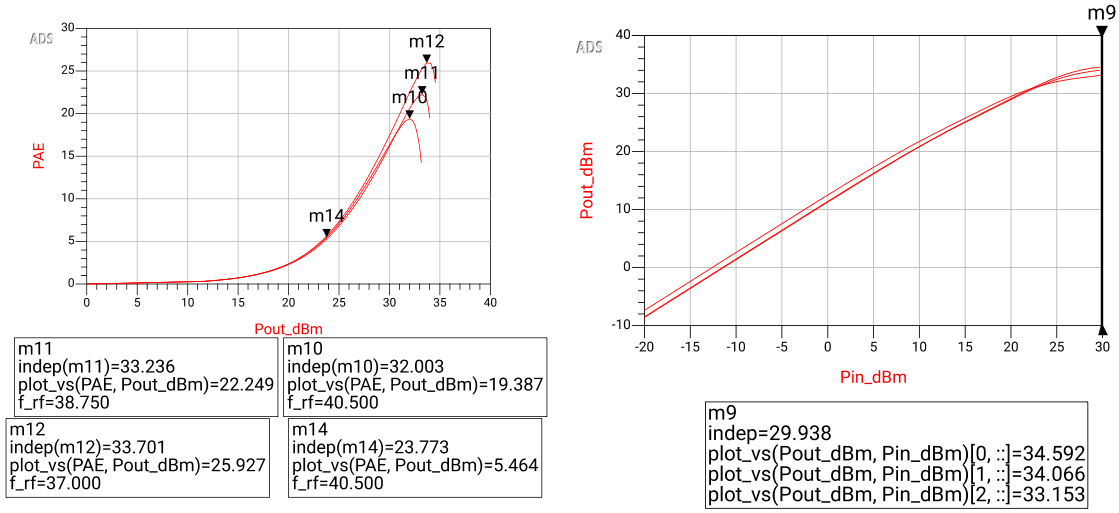
Figures 5.36 and 5.37 evaluate the full EM-simulated PA large-signal performance, compression behavior and efficiency. The fundamental output power shown if figure 5.36a is approximately 35 dBm at $P_{\text{in}} = +30$ dBm. The linear small-signal gains plotted in the figure 5.36b are above 11 dB across the operating band with a smooth compression past $P_{\text{out}} \approx +25$ dBm. The PAE shown in figure 5.37a attains a peak of approx. 26% at 37 GHz and for 10 dB Output power back-off PAE was $\sim$ 5%. The transfer curve shown in figure 5.37b yields a saturated output power (P_{sat}) of maximum approx. 35 dBm (2.9 W) at 37 GHz.

The full EM results suggest a large performance degradation compared to previous iterations: (i) the ideal PA: $P_{\text{sat}} \sim$ 37 dBm, PAE $\sim$ 48%, Gain $\sim$ 18–19.5 dB; (ii) the layout schematic PA: $P_{\text{sat}} \sim$ 37 dBm, PAE $\sim$ 45%, Gain $\sim$ 15–17.6 dB. Therefore, the complete EM model does not satisfy important 5G backhaul design goals: it does not meet the 37 dBm (5 W) output power objective, only providing approx. 35 dBm (2.9 W). This difference is due to mismatch especially in the interstage network since it is highly susceptible to small model inaccuracies.



(a) Final PA output power spectrum **(b)** Final PA gain compression curve

Figure 5.36: Final PA large-signal simulation results: output power spectrum and gain compression



(a) Final PA PAE vs output power **(b)** Final PA transfer characteristics

Figure 5.37: Final PA large-signal simulation results: PAE and transfer characteristics

5.4.3 Stability Analysis results for PA EM model

This section provides a full stability assessment of two-stage PA, using Ohtomo loop gains (encirclement plots) to apply Nyquist stability principles to internal feedback paths, and Kurokawa driving point admittance to confirm the absence of negative resistance at the active device terminals. All these results confirm the effectiveness of the integrated RC stabilization networks to ensure a stable operation environment in the whole frequency spectrum.

Ohtomo Loop Gains:

The Ohtomo test uses Nyquist stability principles for internal nodes by placing virtual probes at the gate and drain of each transistor. The Ohtomo loop gains (encirclement plot) shown in figure 5.38 is near zero over the frequency sweep, and the corresponding polar plots shown in figure 5.39 do not show any clockwise encirclements of the critical $1 + j0$ point. This is a check that all internal feedback loops are stable and that no oscillations will be propagated in the parallel amplifier branches.

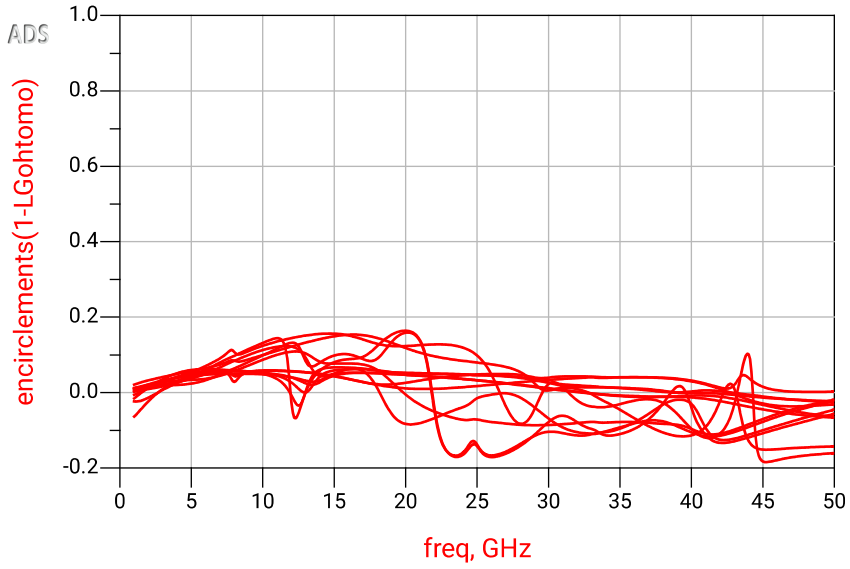


Figure 5.38: Encirclement plot for final PA design

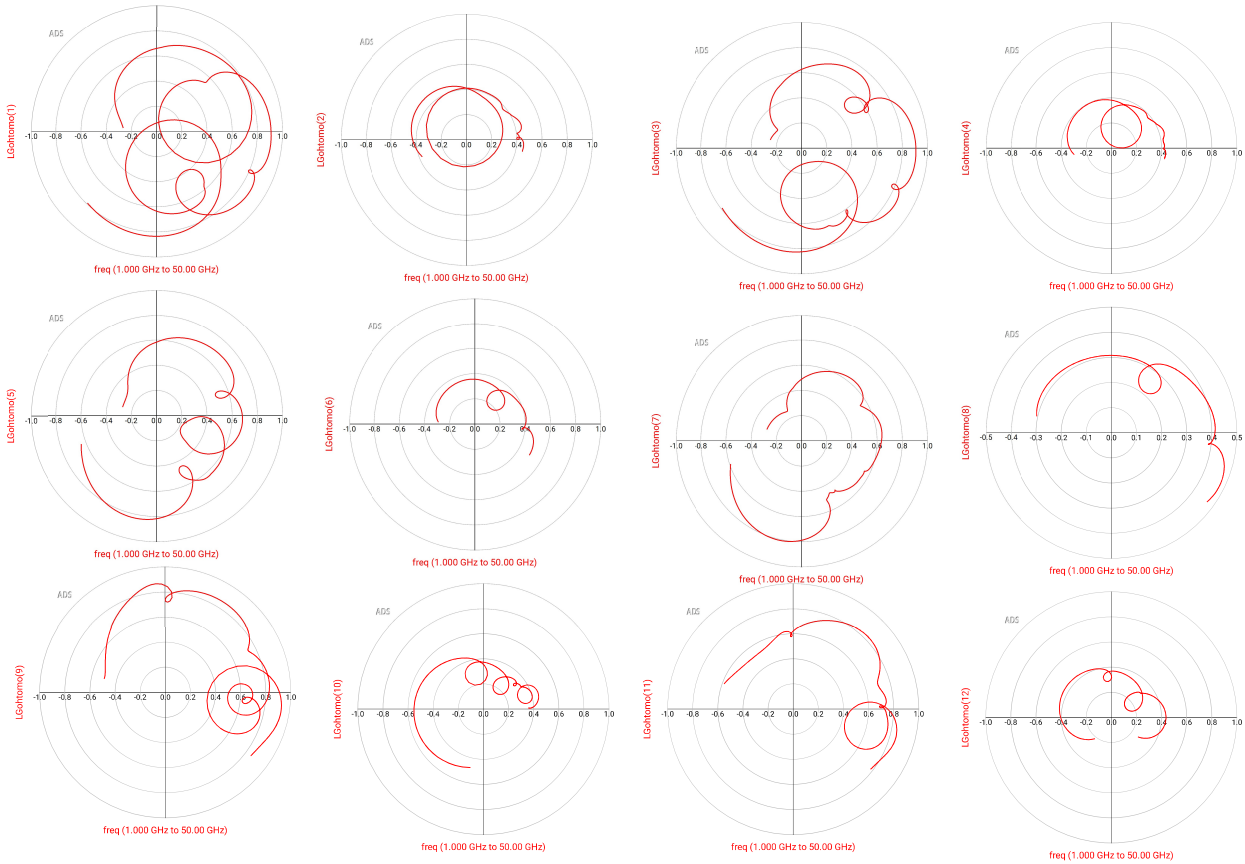


Figure 5.39: Ohtomo loop gain polar plots for final PA design

Kurokawa Driving Point Admittance:

As explained stbility conditions for Kurokawa driving point admittance in section 5.3.3, the Kurokawa driving point admittance plot shown in figure 5.40 shows that there are no zero-crossings where an oscillation equilibrium point could exist ($\mathrm{Re}\{Y_{in}\} = 0$ and $\mathrm{Im}\{Y_{in}\} = 0$) and Kurokawa's dynamic derivative stability condition, $\frac{\partial G_d}{\partial V}\frac{\partial B_l}{\partial \omega} - \frac{\partial B_d}{\partial V}\frac{\partial G_l}{\partial \omega} > 0$, is inherently bypassed; ensuring absolute linear stability. Simulation results confirm that the gate and drain admittances of all six transistors are positive, so that there is no negative resistance to excite catastrophic self-oscillations at any frequency.

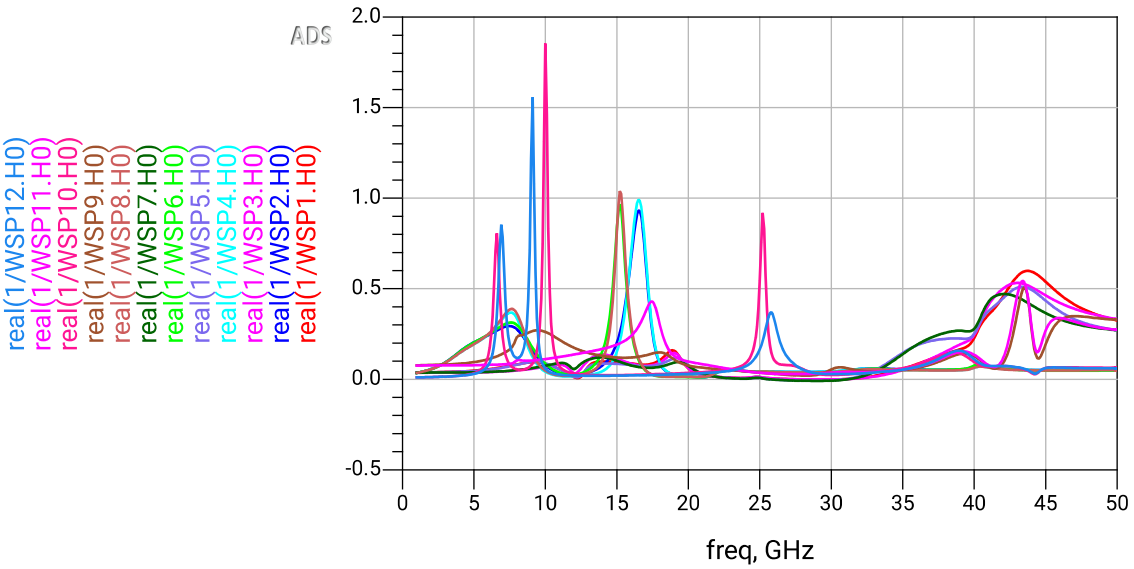


Figure 5.40: Kurokawa driving point admittance for final PA design

6

Conclusion

Summary of Performance and Iterative Comparison

This thesis documents the systematic design of a two-stage GaN HEMT Class AB power amplifier for 5G Millimeter-wave backhaul in the 37–40 GHz band. One of the main goals was to assess the translation from the theoretical models to a physically, electromagnetically (EM) realized MMIC. The results show a clear performance trajectory as design complexity increased to account for physical reality.

The table 6.1 below gives a full comparison of the three main design phases:

Table 6.1: Performance comparison between the ideal power amplifier, schematic co-simulation, and full 3D EM model across the 37–40 GHz operating band.

Metric	**Ideal PA**	**PA Schematic**	**Full EM Model**
P_{sat}	37.4 dBm (5.5 W)	37 dBm (5 W)	34.6 dBm (2.9 W)
Small-Signal Gain	19.5 dB	15–17.6 dB	11.3–12.1 dB
Peak PAE	48%	45.3%	26%
10 dB P_{out} Back-off PAE	14%	14%	5%
Return Loss (S_{11})	19.2 dB	23.3 dB	13.6 to 18 dB

Ideal Microstrip Design: Used simple lossy stubs giving a "best-case" baseline that fulfills all project objectives including >37 dBm output power saturated and almost 50% PAE.

Layout-Realizable Schematic: Added physical discontinuities (MTEEs, MCROSSes) and bias networks. The power was still around 37 dBm but the gain and efficiency started to drop off because of the junction insertion loss and the stabilization loading which was added.

Full EM Model: 3D electromagnetic effects were taken into account including conductor skin effect, substrate dielectric absorption and radiation losses from the corporate combiners. The EM simulated MMIC PA shows the practical performance with achieved P_{sat} of $\sim 35\,\text{dBm}$ and 10 dB Output power back-off PAE was $\sim 5\%$, where the fixed layout geometries cannot be re-optimized dynamically as the same as in schematic environments.

Future Outlook

The full 3D EM simulation has confirmed conditional stability and validated the overall circuit topology, while losses in the physical layout (conductor skin depth attenuation, substrate absorption, and junction discontinuities) caused drops in performance. The final EM model did not meet the target specifications with producing $\sim$ 37 dBm instead of 37 dBm (5 W) output power, gain degradation and only achieved $\sim$ 5% PAE at 10 dB backoff versus the target of 15%. In future design iterations, three primary structural improvements are proposed to address this gap.

1.Driver Stage Transistor Up-Sizing with Load-Pull Optimization: Load pull optimization and up-sizing the driver stage transistors will eliminate driver starvation issues. Increasing the total gate width (W_g) of the driver stage provides more output power headroom ($P_{1\text{dB}}$ and P_{sat}) to keep the driver linear and force the 4-transistor output stage into full saturation (37 dBm).

2. Transitioning to a 3-Stage PA Design: Moving to a 3 stage PA topology (e.g. 1-transistor $\rightarrow$ 2-transistor $\rightarrow$ 4-transistor ratio) provides an additional 8–12 dB of small-signal gain, easily compensating for the physical EM layout losses ($\sim$ 6–8 dB). Power scaling tapers off so that each stage has enough drive headroom to drive the last stage into saturation without compressing too soon. Importantly, pushing the output stage harder takes full advantage of the Class-AB efficiency profile, allowing dynamic biasing techniques on the additional driver stages to significantly reduce low power DC consumption and boost the 10 dB backoff PAE from $\sim$ 5% to the required 15% target.

3. Re-design of the interstage matching network (ISMN): the interstage matching network design was very challenging and that further optimizations and investigations of different topologies could lead to better trade-off between stability, matching, loss, sensitivity and being realizable in a practical and compact layout.

Societal, Ethical and Ecological Considerations

Design and optimization of high efficiency GaN HEMT PAs for mmW frequencies contribute to the development of more energy efficient communication infrastructure. From an ecological aspect, the PA is a critical component as its efficiency directly influences the power consumed and the ecological footprint of the network transmission units. The design work presented in this thesis is in line with "Green IT" principles, with emphasis on Class AB architectures and optimized matching networks, aiming at minimizing the energy waste in future high-capacity backhaul links.

In accordance with the IEEE Code of Ethics, this project corresponds to the professional responsibility to provide honest and realistic technical claims based on the available data. This is demonstrated by the transparent reporting of the performance gap between the ideal schematic results and the final EM-simulated models, noting that the simulated saturated output power was below the initial design target. In the final stages of this thesis, generative AI was applied to linguistic refinement and

structural optimization, especially in the conclusion and the summary of results.

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Appendix 1

Table A.1: List of Abbreviations

S. No.	Abbreviation	Long Form
1	**ADS**	Advanced Design System
2	**AlGaN**	Aluminum Gallium Nitride
3	**AM-AM**	Amplitude Modulation to Amplitude Modulation
4	**AM-PM**	Amplitude Modulation to Phase Modulation
5	**BW**	Bandwidth
6	**CAD**	Computer-Aided Design
7	C_{gd}	Gate-Drain Capacitance
8	C_{gs}	Gate-Source Capacitance
9	**CW**	Continuous Wave
10	**DC**	Direct Current
11	**DPD**	Digital Predistortion
12	**EM**	Electromagnetic
13	**FET**	Field Effect Transistor
14	**GaN**	Gallium Nitride
15	**HEMT**	High Electron Mobility Transistor
16	**IMN**	Input Matching Network
17	**ISMN**	Interstage Matching Network
18	**LDMOS**	Laterally Diffused Metal Oxide Semiconductor
19	**MIM**	Metal-Insulator-Metal (Capacitor)
20	**MMIC**	Monolithic Microwave Integrated Circuit
21	**OMN**	Output Matching Network
22	**PA**	Power Amplifier
23	**PAE**	Power Added Efficiency
24	**PDK**	Process Design Kit
25	P_{in}	Input Power
26	P_{out}	Output Power
27	P_{sat}	Saturated Output Power
28	**RF**	Radio Frequency
29	**SiC**	Silicon Carbide
30	S_{11}	Input Reflection Coefficient / Return Loss
31	S_{21}	Forward Transmission Coefficient / Transducer Gain
32	**UMS**	United Monolithic Semiconductors
33	V_{DS}	Drain-Source Voltage
34	V_{GS}	Gate-Source Voltage
35	**mmW**	Millimeter Wave