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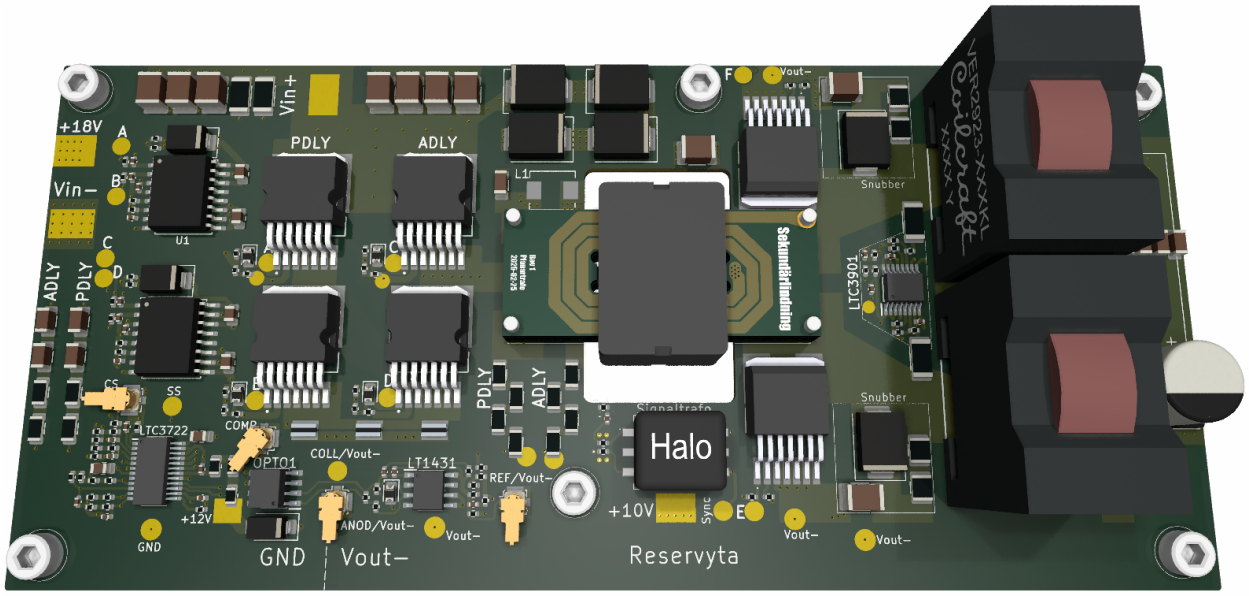

Development and Optimization of a Phase-Shifted Full-Bridge Converter

Exploring high-frequency planar magnetics in aerospace power electronics

Master's Thesis in Electric Power Engineering

David Prytz Arcombe & Lowe Blank

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David Prytz Arcombe & Lowe Blank

Supervisor: Simon Larsson, Saab AB
Supervisor: Johannes Karlsson, Saab AB
Examiner: Torbjörn Thiringer, Department of Electrical Engineering at Chalmers University of Technology

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Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Göteborg
Telefon +46 31 772 1000

Cover image: **3D model of converter from KiCad.**

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David Prytz Arcombe & Lowe Blank
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Abstract

Power electronic converters have become an essential part of modern-day electronics. Switching converters dominate the industry, with switching speeds going up while physical dimensions are shrinking. Out of all available converter topologies, the phase-shifted full-bridge converter has emerged as a promising option when dealing with higher power levels, partly due to its ability to perform zero voltage switching to increase efficiency. This thesis explores the development of such a converter at a power level of 500 W, with a focus on small form factor and the use of discrete components to ensure full design freedom. In order to decrease the size of the magnetics the switching frequency has been greatly increased. The magnetics includes the transformer, which has been constructed as a planar transformer to better suit the high frequency operation of the converter and enable good thermal management. After designing the converter and sourcing components, the converter was assembled and put through a series of tests. Full output power was achieved at a total system efficiency of 90 %, while maximum regulated output power reached 300 W due to instability in the control loop. The transformer worked and proved the possibility to decrease total converter size, but parasitics caused ringing which ended up thermally limiting the converter. A thermal model of the converter and mainly the transformer was implemented and used successfully to predict real-life temperature under load.

Keywords: converter, phase-shifted full-bridge, planar transformer, high-frequency.

Acknowledgements

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David Prytz Arcombe & Lowe Blank, Gothenburg, June 2025.

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

PSFB	Phase-Shifted Full-Bridge
PCB	Printed Circuit Board
ZVS	Zero Voltage Switching
PCMC	Peak Mode Current Control
TRM	Thermal Risk Management
CDR	Current Doubler Rectifier

Contents

1
Introduction

In recent decades, power electronics has seen a rapid proliferation within different parts of society. Everything from the smallest LED driver to Gigawatt HVDC transformers is in some way the same idea, applied at different sizes and power levels. The relationship between these two factors, size and power level, has also changed drastically since the birth of power electronics. Where once large and slow thyristors were needed to handle high power requirements, small SiC MOSFETs are now up the task, reducing the size while maintaining efficiency and increasing flexibility.

This miniaturization has enabled different types of power electronics such as DCDC converters to be applied in areas where size and weight are critical aspects, such as in different aerospace products offered by Saab. While converters with high performance can be bought off the shelf, they are seldom able to match a converter that has been tailor-made for the application. For this reason, Saab has requested the development of a high-power isolated DCDC converter with a small physical footprint. One suitable topology for higher power levels is the full-bridge converter, more specifically the phase-shifted full-bridge (PSFB) converter. The possibility of utilising Zero Voltage Switching (ZVS) allows this topology to achieve high efficiency while still remaining easier to implement compared to its close relative, the full bridge LLC resonant converter.

In order to achieve the main objective of minimizing board area while maintaining full functionality, multiple different methods can be used but one key parameter that affects component sizes in switched power applications is switching frequency. The size of some of the largest components such as transformers and other inductors have a strong dependency on the switching frequency and for this reason, increasing the frequency is an important tool when creating a small converter. Going this route brings its own set of challenges, such as increasing switching and core losses as the frequency increases. The potential use for a planar transformer, something mainly found within higher frequency designs, is another possibility that can be investigated in order to reach desired performance.

1.1 Purpose

The purpose of this thesis is to design and develop an isolated, high power DCDC converter based on the PSFB topology with a large focus on decreasing physical size. The key methods to enable the size decrease will be higher switching frequency

as well as selecting space-efficient components. The potential use of a planar transformer and its design will be investigated as a step in this process. In order to assess the final prototype and its merits, an off-the-shelf converter module made by Vicor and currently used by Saab will be used as a benchmark. The two converters shall be analysed and compared. Lastly, different types of secondary sides of the PSFB such as current doubler, center-tapped and passive/active rectification shall be dissected and compared.

1.2 Goals

A number of different goals are set out for the project:

Design a phase-shifted full-bridge DCDC converter: Using LTspice and other simulation software, a realistic electrical model of the converter will be created and used to test various functions before the PCB is manufactured. The circuit schematic will be made concurrently with the model.

Design a PCB and minimize converter size: An attempt will be made to create a layout for the PCB design. Compact size will be a high priority.

Design and construct a planar transformer: A custom transformer which implements planar technology will be designed and constructed. As with the PCB, a small physical footprint will be a high priority.

Verify converter performance: Once the PCB has been manufactured and all components have been assembled on the board, validation of all functionality will be carried out. Other criteria such as EMI and thermal performance shall also be evaluated.

Comparison with Vicor's converter: The final product will be compared to the currently used third-party converter, to assert if the customization has provided any signs of possible benefits in terms of performance.

1.3 Scope

A number of limitations have been set in order to make the project feasible:

Disturbances on the supply voltage will not be considered: While the input voltage will be varied across the defined range, disturbances such as voltage spikes and similar events will not be tested.

Only one controller will be considered: The LTC3722-1 IC from Analog Devices will be the only controller used and investigated in the project, as specified by Saab. Previous Master's thesis at the company have used this controller and

therefore there exists a good understanding of its benefits but also its challenges. This will be valuable for the project in order to develop a functioning prototype.

Cost will not be studied: A cost estimate will not be made. On the same topic, no carbon footprint will be calculated either in order to limit the workload of the project.

Auxiliary power will not be supplied internally: In order to simplify circuitry and the number of potential error sources, auxiliary power will be supplied externally.

1.4 Societal, Ethical and Ecological Aspects

The main ethical aspect that must be addressed regarding the project is the application of the converter. Saab is defence company and thus its products may be used in armed conflicts which could bring harm to civilians and society. With that said, Swedish law regulates how these products are sold in order to prevent them from falling in the wrong hands. Democracies should be able to defend themselves from external threats which requires a defence industry to provide the necessary equipment to do so.

Other aspects to consider include the ecological impact of the project. As with all physical products, material and energy use during manufacturing comes with a climate impact, as well as the waste generated when the product reaches its end of life. Some materials such as lead could be harmful to workers dealing with the recycling if proper care is not taken.

2
Theory

The following chapter describes theory behind the phase-shifted full-bridge converter, planar transformers, control strategy, component selection and PCB layout.

2.1 PSFB

The phase-shifted full-bridge is composed of four transistors, isolating transformer and a rectifying stage in the secondary as seen in Figure 2.1. It is optimal for high power and when efficiency is desired, enabling soft switching utilizing parasitics present in the transformer and transistors [1]. The power transfer of the PSFB is different from the regular full bridge. Each transistor is always conducting close to 50% of the time, where the top and bottom transistors of a leg are switched opposite to each other with a delay in-between to prevent shoot-through. The way in which the two legs, the Active leg and the Passive leg, are switched in relation to each other is what drives the power transfer, this is the phase-shifting operation of the converter. During no load the two legs will be in complete sync where transistors T1 and T3 will be conducting at the same time, freewheeling and thus no voltage will be present over the transformer. For power transfer, the phase of the Passive leg will increase causing an overlap of T1 and T4 as seen in Figure 2.2. The output voltage of the PFSB is as follows,

$$V_O = \frac{V_{in} \cdot D}{2 \cdot N} \tag{2.1}$$

where V_{in} is input voltage, D is the phase shift between the legs and N is the turns ratio of the transformer from primary to secondary. The factor of 2 originates from the current doubler rectification.

The whole switching cycle involves a series of steps. Assuming a starting point of T1 and T4 conducting, the first stage in the switching cycle is power transfer. The time T4 is conducting is determined by the phase-shift. After T4 is turned off the second stage starts, providing zero-voltage condition for T3. The energy stored in the inductance is used to discharge the output capacitance of T4 while charging up output capacitance of T3. The body diode of T3 will start conducting and the zero-voltage turn-on condition has been provided for T3. Turning on of T3 begins the third stage where T1 and T3 are "freewheeling" and there is no voltage over the transformer. This transitional stage will be repeated for the turn off of T1 and turn on of T2. After, the converter will once again enter the power transfer stage and

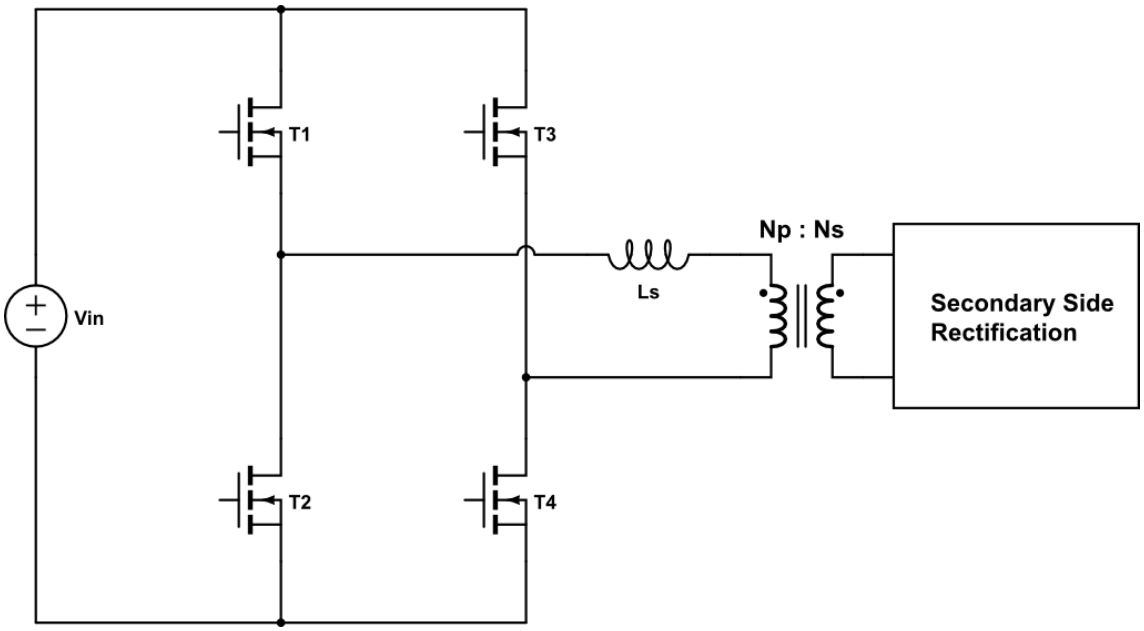


Figure 2.1: Full-bridge circuit diagram, including leakage inductance L_s and the secondary side.

the whole process from the first stage will be mirrored for the pair, T2 and T3, to get back to T1 and T4 conducting.

2.2 ZVS Condition

Energy in the parasitic elements of transformer leakage inductance and MOSFETs capacitance causes resonance which can be utilized to force the drain-source voltage of the FETs to zero before turn on. To allow the voltage to drop to zero over the MOSFET following criterium needs to be fulfilled [1], [2].

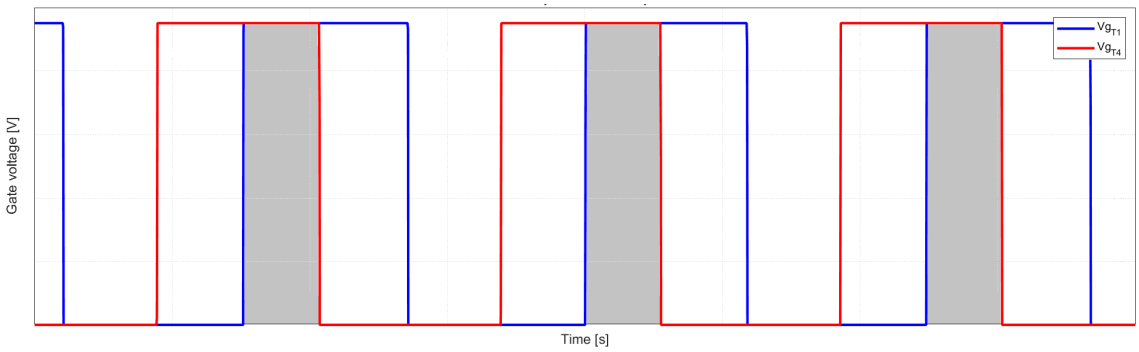
$$E_C = \frac{4 \cdot (C_{oss} + C_{xmfr}) \cdot V_p^2}{3} \tag{2.2}$$

$$E_L = \frac{(L_{lkg} + L_s) \cdot I_p^2}{2} \tag{2.3}$$

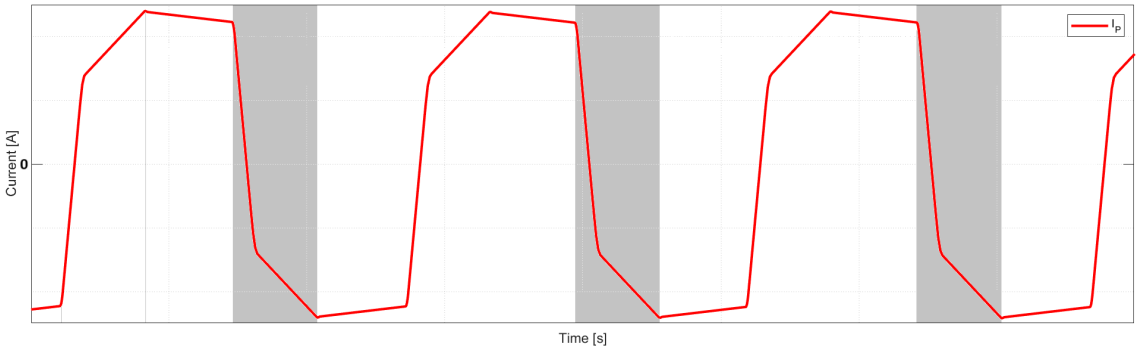
$$E_L \geq E_C \tag{2.4}$$

The output capacitance, C_{oss} of the MOSFETs will have the largest effect on the capacitive energy present when charged to the voltage, V_p. L_{lkg} is the leakage inductance of the transformer and will often not be sufficient to satisfy the condition of (2.4) throughout the load range as I_p is the maximum current flowing through the primary and is dependent on the output current. The additional inductor, L_s, increases the total energy available.

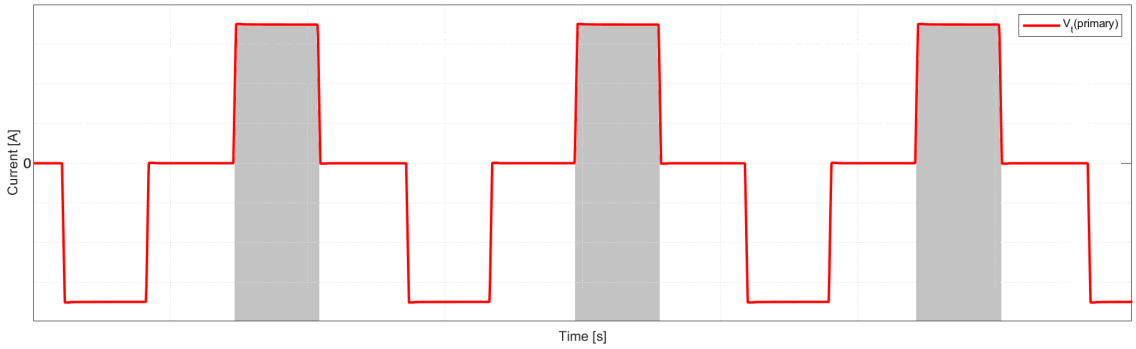
The next condition for ZVS is to ensure proper dead time for the switch event to be sure the voltage across the FETs are near zero. The timing required is reliant on



(a) Gate voltages for T1 and T4



(b) Current flowing through the primary side transformer.



(c) Transformer voltage as a result of the switching

Figure 2.2: Theoretical PSFB waveforms where shaded areas are matched between the graphs. Each shaded area consist of the duty cycle loss, during which the transformer current is reversed and quickly rising until it matches the reflected current from the secondary and the following power delivery phase.

the resonance frequency of the parasitic elements.

$$f_r = \frac{1}{2\pi \cdot \sqrt{(L_{lkg} + L_s) \cdot (2 \cdot C_{oss} + C_{xfmr})}} \tag{2.5}$$

f_r is the resonance frequency of the parasitic elements in the circuit leading to a dead time between each transition according to the expression

$$T_D = \frac{1}{4 \cdot f_r} \tag{2.6}$$

where T_D is the time it takes the resonance to swing the voltage to zero, as seen in delay between the two gate voltages in Figure 2.3. Increasing inductance in the circuit to increase the ZVS range will lead to a longer required dead time and increased loss in duty cycle. However, a longer dead time means a lower maximum overlapping conduction time. If a wider ZVS range is required, reducing circuit capacitance is more beneficial.

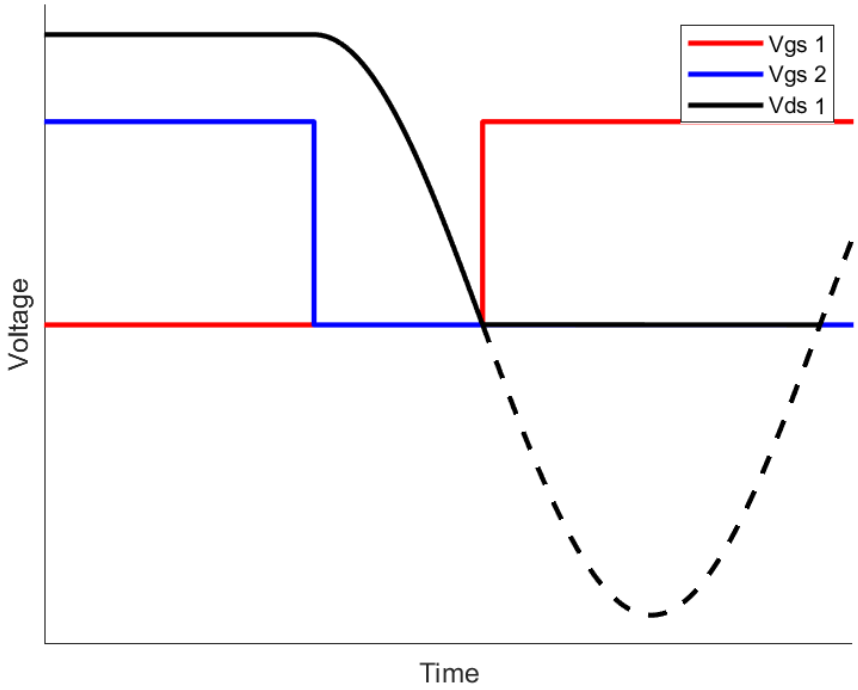


Figure 2.3: Parasitic resonance of the drain-source voltage of a transistor. Removing overlap of voltage and current eliminates or at least decreases switching losses.

2.3 Secondary side rectifying

The topology chosen on the secondary side has a large impact on the design and dimensioning of secondary side components. A current doubler rectifier (CDR) has two output inductors and two rectification diodes, see Figure 2.4.

The power transfer, freewheeling and reflected current matching is the three stages determining current flow for the CDR secondary, see currents in Figure 2.5 and

2.6. When the dot marking is positive, D_2 is conducting, the current increasing in L_{out1} and decreasing in L_{out2} until the freewheeling period start on the primary side. Then there will be no voltage over the transformer causing both inductor currents to decrease, still only D_2 conducting. During the moment the primary current is reversed and rising to match the reflected current, D_1 starts to conduct while both inductor currents are decreasing. After the current is matched the voltage on the dot marking is now negative and D_2 will stop conducting completing a half cycle, a mirrored operation finishes the whole cycle.

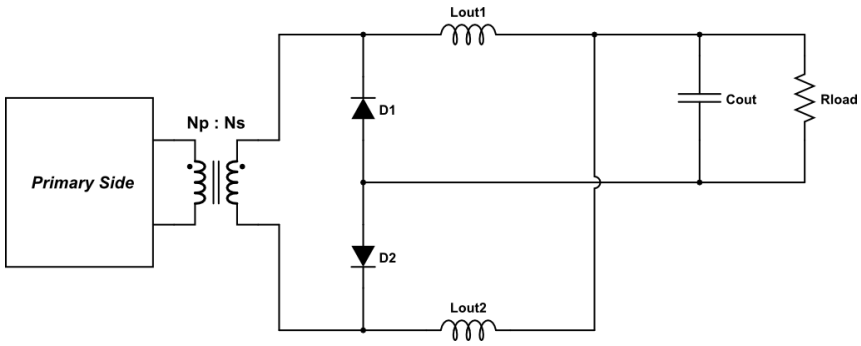


Figure 2.4: Current doubler rectification circuit diagram. While decreasing the current stress on the transformer compared to the center-tapped approach, the CDR implementation requires twice as many output inductors.

Reducing diode losses can be done at the cost of increased complexity by replacing the diodes with actively controlled MOSFETs. These will require to be driven correctly and synchronized to the primary side switching to ensure no current reversal into the MOSFETs and to ensure they are conducting during their correct state. The separate diode current can be seen in Figure 2.5, while the inductor currents and the output current can be seen in Figure 2.6.

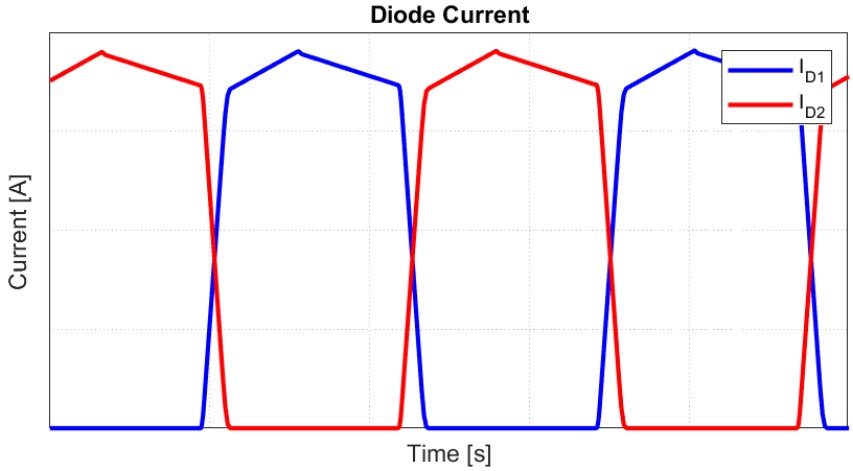


Figure 2.5: Rectifying diode current in a CDR circuit.

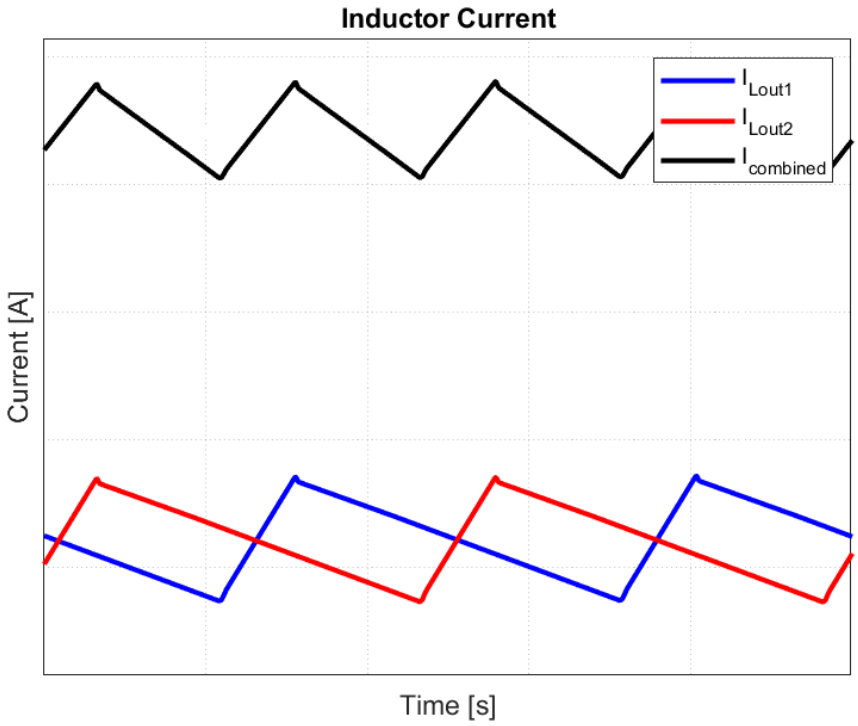


Figure 2.6: Inductor and output current in a CDR.

2.4 Transformer Design

Due to its size and impact on the operation of the converter as a whole, the transformer may be the single most important component. There is a lot of freedom in how one designs a transformer, starting with choosing what type to use and then dimensioning core and windings to suit the demands placed on it.

2.4.1 Planar vs wound transformer

The two most commonly used types of transformers used in power electronics are the wound transformer and the planar transformer. The main difference lies in the windings, which for wound transformer tends to be some wire like litz wire, while planar transformer use traces on PCB laminates. The PCB laminates can be part of the main converter board or their own small boards, with the first alternative allowing for tighter vertical packaging while the latter one gives the designer more freedom in terms of stack-up. The choice of which type of transformer to use depends on the use case. Planar transformers excel at high-frequency applications where thermal management can be an issue. The large surface area provided by the laminates provide increased cooling of the windings, hence the improved thermal management. The advantage at higher frequencies lies partly in the use of thin copper traces which reduce eddy current and skin effect. Lastly, the use of PCBs instead of wires result in great production consistency and repeatability. Wound transformers come with other advantages instead, such as higher fill factor and lower interwinding capacitance. [3]

2.4.2 Dimensioning

When going for minimal size, heat management will be the main concern for the transformer. The sources of heat generation are iron losses in the transformer core as well as resistive losses in the copper windings. Both increase as size decreases, since smaller components result in higher current and flux densities which in turn lead to increased losses. Once a core size has been chosen, the copper windings/traces should be made as wide as possible to minimize resistance, with limitations such as creepage distance and manufacturing tolerances taken into account. Due to the specific materials and processes needed to create magnetic cores that are suitable for high-frequency applications, it is preferable to purchase a core off the shelf rather than trying to dimensions a custom one. In order to find an optimal core, a sweep of different available cores in the suitable range can quickly give a good estimation of what size is most appropriate. For each core, the expected losses is calculated from the core material and core dimensions which is then used as the basis for evaluation.

2.4.3 Parasitic capacitance

Since a minimal amount of parasitic capacitance is desired in order to achieve ZVS, it is of interest to calculate the expected interplane capacitance between the windings of the transformer. In principle, it is a quite simple ordeal since the windings form parallel planes at a certain distance from each other. The standard capacitor equation, $C = \epsilon_0 \epsilon_r \frac{A}{d}$, can therefore be utilized where A is the winding surface, d is the distance to another winding, ϵ_0 is the permittivity of free space, ϵ_r is the dielectric constant of the material in-between the windings. Assuming the PCBs used have windings on both sides, each winding will consist of two parallel surfaces that are connected but at a distance from each other. The parasitic capacitance between layers can then be calculated as the sum of many contributions of capacitance between different sets of windings.

2.5 Control

The following section describes the basis of how the converter is regulated and what models are used to implement said regulation.

2.5.1 Peak Current Mode Control

In peak current mode control the control voltage determining the duty cycle is compared to a ramp waveform taken from the current flowing through the output inductors. The control voltage, in turn, is the amplified difference between the output voltage and a reference[4]. A feedback circuit can be implemented along the error amplifier to provide better regulation. A challenge appears when isolation is required and the controlling IC is located on the primary side. The control voltage can be opto-coupled to primary side while the current measurement can be exchanged with a measurement of the primary side current as they will be related to each other according to

$$I_P(PEAK) = \frac{I_O}{2 \cdot N \cdot EFF} + \frac{V_{in} \cdot D}{L_{MAG} \cdot f_{sw} \cdot 2} + \frac{V_O \cdot (1 - D)}{L_{OUT} \cdot f_{sw} \cdot N} \tag{2.7}$$

where $I_P(PEAK)$ is the peak current in the primary, I_O is the maximum output current, N is transformer turns ratio, EFF is the efficiency of the transformer, V_{in} is input voltage, D is the phase shift for the associated input voltage, L_{MAG} is the magnetizing inductance, f_{sw} is the controller switching frequency and V_O is the nominal output voltage [5].

The voltage loop controls how high the current can go while the current loop is responsible for determining the duty cycle. Because of this current limiting is automagically implemented as any irregular behaviour will be sensed and the duty cycle will be adjusted accordingly.

2.5.2 Small signal model of PCMC PSFB

The control to output transfer function derived in [6] provides a theoretical open-loop transfer function:

$$G_{vc}(s) = \left.\frac{\hat{v}_o(s)}{\hat{i}_c(s)}\right|_{\hat{v}_i(s)=0} = \frac{T_c G_{vd}(s)}{1 + M_o G_{vd}(s) + T_L G_M(s)} \tag{2.8}$$

The open-loop transfer function will be used to determine positions of poles and zeros of the compensation network.

2.5.3 TYPE II, TYPE III

Then name Type 2 and 3 regulation describes how many poles a feedback loop contains [7]. The amount of poles will increase performance and response times, but is more complex to design and contains more parts [4].

2.6 Component Selection

The following section describes the theory behind the selection of the main components on the converter.

2.6.1 Gate drivers

The choice of gate drivers has a large impact on the implementation of the converter and has a large impact on the PCB layout and care should thus be put into this process. For one, the drivers must be capable of delivering the currents needed to charge and discharge the MOSFET gate, referred to as sink and source current. The required current will mainly depend on the gate charge of the MOSFETs and the switching frequency of the converter. Given the high switching speeds this project aims for, the demands on the drivers will be high. Apart from simply turning on and off the gates, internal logic such as programmable dead time to avoid shoot-through

adds a layer of protection since the input signals to the drivers might be distorted on its way from the main controller.

2.6.2 MOSFETs

Selection of MOSFETs for the converter must take a number of parameters into account. As always with power electronics, low $R_{ds,on}$ and gate drive requirements help increase efficiency, while a small physical footprint decreases total converter area which is especially important in this project. A requirement more specific to the PSFB topology is the need for low output capacitance, C_{oss}, since it heavily affects the amount of energy needed to achieve ZVS and thus further increase efficiency. Due to the non-linear relationship between V_{ds} and C_{oss} for MOSFETs, it is the most challenging parameter to compare between different switches [8].

2.6.3 Inductors

In general when designing power electronics, the magnetics tend to be the physically largest components which is very much true for the PSFB topology. Because of the current doubler, two output inductors are needed instead of one. Similar to the transformer, decreasing the inductor size is a fight against losses that need to fit within the power budget. The losses are copper losses in the conductors as well as core losses, just like the transformer. An approach to reduce inductor size that has become more common recently is the use of moulded inductors due to their compactness but they tend to generate substantial core losses at higher frequencies such as in this project. Still, their size advantage make them suitable for applications where board area is of importance. The other main option is flat wire inductors which are noticeably larger but can handle high currents while maintaining low core losses even at higher frequencies. Lastly, regardless of inductor type, there is the question of using shielded or non-shielded inductors. Shielded inductors decrease radiated EMI which could disturb nearby components and circuits but generally showcase sightly lower current density compared to their non-shielded counterparts [9]. If the inductors are placed close to sensitive circuits, it could be advantageous to use shielding and accept the small loss in current density.

2.7 Layout

Given the schematic and chosen components, a lot of potential problems can arise from poor PCB layout. These can range from more manageable difficulties such as high conduction resistance and the associated losses to EMI which prevents the operation of the converter completely. In order to minimize the risk of such problems, a couple of specific areas can be looked at:

- **Switch nodes:** Since the switch nodes rapidly change voltage level between ground and the input voltage, they can be the origin of strong radiated EMI which might interfere with other parts of the circuit. Minimizing their area counters this effect to a large degree, but can cause higher switch temperatures

since the MOSFETs rely on all connected copper shapes to act as heat sinks.

- **Trace inductance:** All traces will come with some amount of parasitic inductance. Generally speaking, the longer the trace the more inductance you will have. For signal traces especially, this can become problematic as the inductance slows down and distorts signals. One example where this can become problematic is for the gate drive. Once the signal for a given switch leaves the main controller, it must make its way first to the gate driver and then from the gate driver to the MOSFET. If one gate signal is delayed more than another one due to a longer trace and therefore more inductance, the risk for mistiming and possibly shoot-through increases. Higher switching frequencies such as in this project can exasperate the problem unless one takes good core to keep the trace lengths to a minimum.[10]

- **Copper losses and heat management:** Given a power electronics PCB where minimal size is an aim, dealing with the heat generated can be challenging. Thinner traces and smaller shapes leads to more resistance and less area to dissipate heat which will lead to higher component temperatures. Utilizing trace width calculators and current density simulations can help the designer achieve more uniform heat spread and lower maximum temperatures by adding or removing copper where needed. The use of vias and the bottom layer can be beneficial in many cases, especially if a heat sink is mounted to the bottom side of the PCB.

- **Creepage distance:** When dealing with higher voltages, it is crucial to maintain adequate creepage distance in order to prevent discharges that could damage equipment or harm people. All components but mainly copper shapes and traces that carry high voltage should therefore be spaced apart from each other at a distance specified by the IPC-2221 standard. The exact distance required depends on if it is inner or outer layers, whether coating is used or not etc. [11]

3
Case set-up

The execution of the project is heavily centred on design and practical work in a lab setting. Based on technical aspirations and a corresponding power budget, a circuit will be simulated which will lay the foundation for the converters schematic. Next, component selection will take place in tandem with the PCB design, with some thermal simulation to evaluate the design.

3.1 Technical Aspirations

The criteria for the converter have been set beforehand by Saab in order to be compatible with the existing product range and system requirements.

- Power output of 500 W.
- Input voltage range from 270-420 V.
- Output voltage of 28 V.
- Voltage ripple below 2 %.
- Minimal board size.
- Increased switching frequency, around 800 kHz.
- Galvanically isolated.
- Based around planar transformer technology.

The output voltage of 28 V is industry-standard for aerospace application, while the rest are more custom to this specific project. The increase in switching frequency must not necessarily end up at exactly 800 kHz, but said value has been estimated as an approximate level to aim for in order to achieve the other aspiration of minimal board size. The explicit request to implement a planar transformer is based on a desire to increase knowledge within the company around said technology and what benefits it might bring for future power electronic projects. Lastly, efficiency should of course be as high as possible, with at least 90 % being expected in order to make the converter viable.

3.2 Power Budget

The target efficiency for the converter is set at 92.5 % which is in line with the value given in the datasheet for the LTC3722. Given a maximum output power of 500 W, 40 W of losses can be distributed across the different components according to the power budget:

Table 3.1: Power/loss budget of the converter, featuring the main sources of losses.

Component	Losses
Output	500 W
Transformer	10 W
MOSFETs	20 W
Inductors	4 W
Snubbers	4 W
Misc	2 W

The values in the power budget have been estimated from calculations of what losses one can expect from the different components at full load, given that roughly equal time is spent across the board on optimization. MOSFET losses will largely be dependent on to what degree ZVS is achieved, while inductor losses are quite stable and predictable as long as one knows the output current.

3.3 Circuit Simulation & Schematics

The development phase starts with the schematics and their implementation in simulation software. The foundation for how the circuit should be routed will be the datasheet for the LTC3722-1 controller, since it is the centrepiece of the converter and is the most complex part. Since Analog Devices, the manufacturer of the controller, also distribute the simulation software LTspice, there exists a model of a fully implemented converter in said program based on this controller. Some modifications have to be made in order to better suit the project, the main one being replacing the LTC4440 gate drivers from Analog Devices with faster UCC21520 drivers from Texas Instruments. The feedback loop is implemented with the isolated error amplifier ADUM4190 from Analog Devices.

Simulations were performed to evaluate the efficiency and compare with the physical prototype. The tests were performed unregulated to replicate similar behaviour along with input and output matched as closely as possible to the measured values from the prototype in Table 4.3 found in section 4.4.9.

3.4 Component Selection

In order to make appropriate component selections, multiple simulation programs will be used in order to cover all relevant aspects. While LTspice provides the

electrical requirements for the components, it will be supplier programs like K-SIM, Simsurfing and Coilcraft Design Tools that provide the framework needed to take things such as derating and operating conditions into mind. Given the goal of decreasing size and weight, a considerable amount of effort will be put into finding small and space-efficient components that enable the converter to become as compact as possible, should a production-ready version be constructed.

3.5 Layout and PCB Design

When the schematic is finished, a layout will be designed in order to manufacture the PCB. Challenges such as efficiency, thermal management, EMI and most importantly size will be taken into account during the design. Since the PCB is a prototype there will be features added that would not be present on a production-ready board such as measuring points, micro coaxial connectors, extra resistor footprints etc.

3.6 Control

The presented control-to-output transfer function presented in (2.8) gave rise to the transfer function showcased in Figure 3.1 which provided a starting point for selecting components for the feedback loop. An example of how the feedback loop is implemented in LTspice can be seen in Figure 3.2, where the ADuM4190 from Analog Devices is being evaluated in simulations.

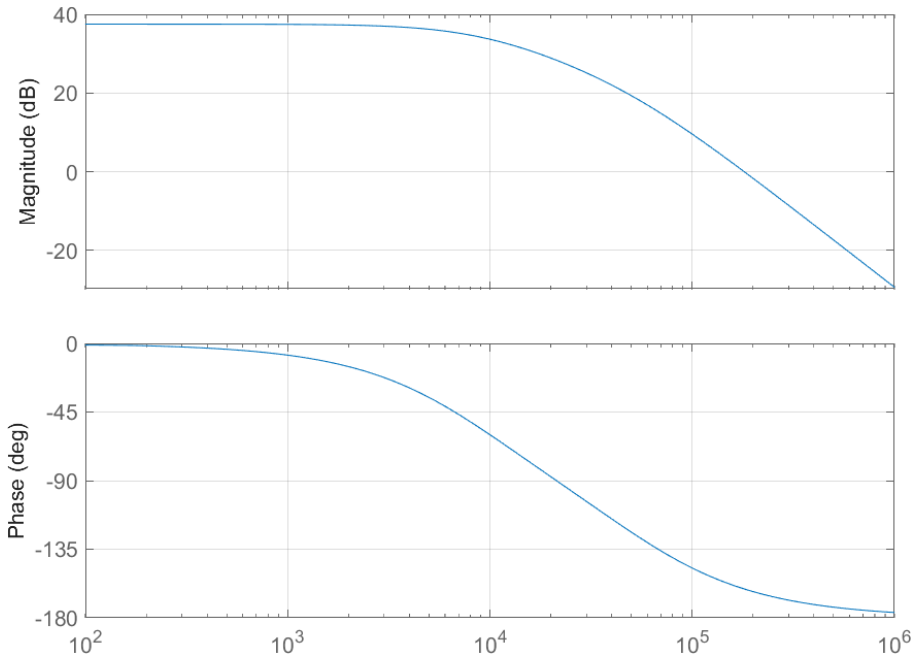


Figure 3.1: Bode plot of transfer function for CDR PSFB, showcasing the amplitude and phase margin of the system.

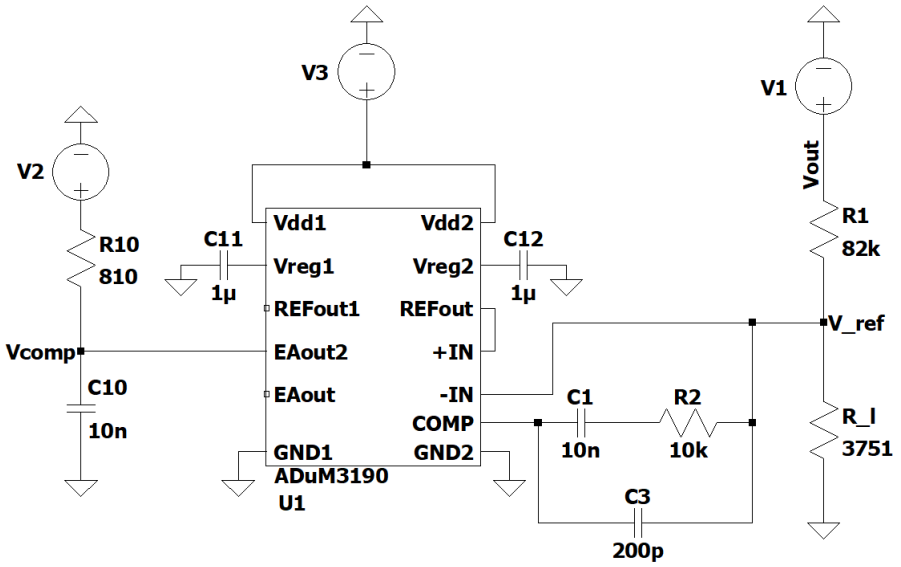


Figure 3.2: LTspice circuit evaluating transfer function of the feedback loop, based on an alternative error amplifier known as ADuM4190/ADuM3190 from Analog Devices.

3.7 Assembly

Once the PCB has been manufactured and supplied by a PCB manufacturer, the process of assembling the components will begin. In order to save lead time, components will be ordered separately and soldered on in-house using a reflow oven. This also gives more hands-on experience which will be valuable during the debugging phase.

3.8 Verification

After the board has been assembled, the verification process can start. All functions of the board will be tested with stable power delivery being the main focus. The following section describe these tests in more detail.

3.8.1 Start-up

Multiple different functions occur during start-up of the device which protect the device and supply voltage in different ways.

- **Soft-start:** The controller should slowly ramp up according to the time constant set by a capacitive circuit.
- **Inrush current:** The peak inrush-current should be limited to a safe value.
- **Delay until switching starts:** The delay until the top power MOSFETs start to switch should not be needlessly long.

3.8.2 Power delivery

Being the main function of the converter, it is essential that power delivery works as intended over the entire defined working range.

- **Output power:** The converter should be able of delivering 500 W of power continuously.
- **Input voltage range:** Rated power delivery should be possible within the entire defined input voltage range.
- **Slew rate/Transient behaviour:** To handle dynamic loads, the slew rate should be high enough to keep up with rapid load increases/decreases.

3.8.3 Thermal management

Since the aim of the project is to increase the power density of the converter, high temperature will likely be present and must not exceed the rating of different components.

- **MOSFETs:** The switches are likely to run hot due to turn-on and turn-off as well as conduction losses. Their operating temperatures must not be too high in order to ensue adequate lifetime and to minimize losses.
- **Transformer:** The largest of the components used will be the transformer, which will therefore be made as small as possible. The lack of active cooling presents additional challenges, requiring good thermal design.
- **Snubbers:** The protective snubbers may conduct a substantial amount of current which would result in large amounts of heat generation.

3.9 TRM

With the use of the simulation software TRM, short for *Thermal Risk Management*, the thermal behaviour of the transformer windings will be evaluated. The basis for each simulation is the Gerber and drill files for the PCB. These are mainly used for the manufacturing of the PCB and describes where copper should be kept or removed on each layer in the board, as well as where vias are placed. The main user input that is needed is defining the currents in different nets, as well as any heat flux from components generating substantial amounts of heat such as MOSFETs or inductors. Given a complete PCB, this can be quite a tedious task to complete, especially if accuracy is wanted, but for the example of PCB windings it is a matter of a single net with one current running through it. At the moment, only DC currents are supported but for a thermal analysis, setting the DC current equal to the AC RMS current will suffice. The simulation results will later be verified to an extent using thermal imagery.

3.10 Comparison with Vicor's converter

In order to compare the developed converter to alternatives on the market, the currently used converter will act as a benchmark for performance and packaging. Since both converters are used for the same application, they will be compared at rated operation of 500 W on metrics such as size, efficiency, output ripple and more.

3.11 Measurement Setup

The following section describes the measurement setup, with the main components being visualized in Figure 3.3. Two power supply units will be used, one for supplying the high voltage input at 350 V and one for the auxiliary low voltages at 12 V and 5 V. In order to load the 28 V output of the converter, a digital resistive load from Chroma will be used. This setup makes it possible to test a wide range of operating points since both input voltage and load can be adjusted independently of each other.

On the converter from Vicor, the probing capabilities will be limited since it's a production version without dedicated measuring points or similar features. Input and output voltage as well as current can of course still be measured which will give estimations of efficiency, dynamic performance and more. For the converter that this project results in however, there will be several measurement and debugging features in order to aid the validation. Measurement points will be one such feature, allowing voltage measurements across critical components such as the power switches and the main transformer. Debugging LEDs will ease troubleshooting by indicating if voltage is present at different nodes. Lastly, current will be measured using clamp-on current probes in order to minimize any disturbance on the circuit.

Figure 3.3: The measurement setup of the converter with the PSUs and DC load.

3.12 Component Selection

The following section describes the selection of the main components.

3.12.1 Gate drivers

For the primary side, the UCC21520 gate driver from Texas Instruments was chosen. It is an isolated gate driver which handles both the top and bottom switch in a half-bridge. Some benefits include low propagation delay of around 33 ns, built in dead time control and powerful gate drive capability with 4 A peak source current and 6 A peak sink current which is helpful for high frequency operation.

For the secondary side, the LTC3901 controller from Analog Devices was chosen. This driver was developed specifically to work in conjunction with the LTC3722 and was thus the optimal choice in terms of ease of implementation. The maximum voltage of 11 V made the choice of secondary side MOSFETs more challenging but this was eventually solved. Should one require MOSFETs with higher gate voltage, this driver would either need replacing or some sort of amplification would be needed for the gate driver signals.

3.12.2 MOSFETS

For the primary side of the converter, the ROHM SCT3060AW7L are the MOSFETs of choice due to their low output capacitance, see Figure 3.4, combined with their low on-state resistance of 60 mΩ. The D2PAK package is advantageous for thermal management because of the large tab surface, making them capable of 160 W of power dissipation at 25 °C case temperature.

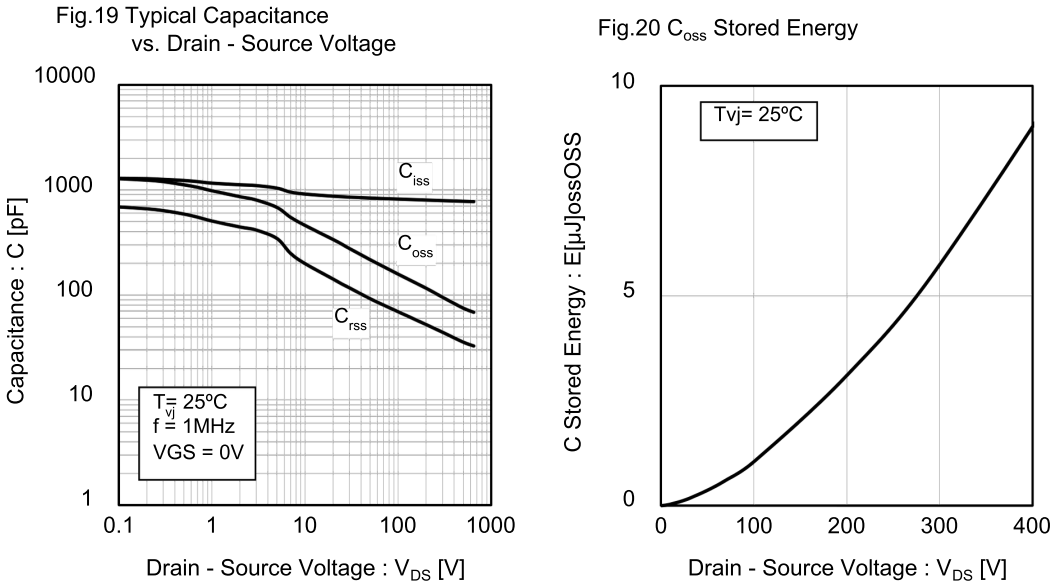


Figure 3.4: Output capacitance and energy stored in said capacitance as a function of voltage for the primary side MOSFETs.

On the secondary side, the UJ4SC075011B7S was chosen instead. It shares the package and many of the benefits that made the primary side MOSFETs attractive, with the main difference being their internal structure and gate drive requirements. The secondary side MOSFETs are of the Cascode type, meaning they combine

MOSFET and JFET technology to achieve a device with low on-state resistance while still being normally-off (unlike pure JFETs). In this case, a gate drive voltage of just 12 V was needed to achieve 11 mΩ of on-state resistance, meaning the 11 V from the LTC3901 driver used on the secondary side would suffice. The trade-off was higher C_{oss} than the MOSFETs used on the primary side.

3.12.3 Inductors

In order to keep losses down, VER2923-223 flat wire inductors with and inductance of 22 μH from Coilcraft where chosen, see Figure 3.5. With a DC resistance of 2.3 mΩ and estimated total losses of 1.42 W per inductor at full load operation, this choice favoured efficiency over size somewhat. These inductors are through-hole mounted and take up space vertically instead of horizontally which was favourable.

Figure 3.5: The Coilcraft VER2923-223 inductor was chosen for the output inductors. While physically large, the flat wire design keeps DC resistance to a minimum while the shielding prevents radiated EMI. Image used courtesy of Coilcraft.

3.12.4 Error amplifier

Initially, the LT1431 error amplifier from Analog Devices was used but due to difficulties in achieving stable regulation, it was swapped out for the ADuM4190. One advantage with this new amplifier, apart from the easier implementation, is the built-in isolation which removes the need for a separate optocoupler. The result is a smaller board area, had one used it from the start. In this case the opposite was true, as the ADuM had to be soldered to a separate PCB and strapped onto the main PCB with soldered jumper cables. The inductance added to the compensation network by the cables was thought to be small enough to not cause any major problems.

4

Results

Once assembled, the converter was put through a swath of different tests and many days of de-bugging. This work lead to the results presented in the following chapter. Starting with the finalized circuit design and schematic, the chapter then moves on to PCB layout and transformer design which showcase the properties of all physical products made during the project. Lastly, the electrical and thermal characteristics of the converter is measured, compared with simulation and lastly compared to the competitors converter.

4.1 Circuit Design and Schematics

The basis of the whole convert is of course the circuit design, which will determine the operation and characteristics of the whole system. The first draft of the semi-complete circuit design has been implemented in LTspice as can be seen in Figure 4.1. Due to problems with the different SPICE models for the gate drivers, they have been omitted in this model in order to be able to run the simulations. With that said, the drivers have still been put through simulations as well, but in smaller models which did not feature the entire circuit. The main reason for this approach was the inherent problems with the models provided by the manufacturer, for example Texas Instrument for the UCC21520 primary side gate drivers. The simulation immediately went up to the highest defcon level which slowed down simulation time substantially. Should these drivers be implemented in some other work where LTspice is used as the simulation software, work should preferably be put into finding the problems with these models and dealing with them so that complete simulations of the converter can be performed. Still, despite these challenges, the models did give good insight into the expected behaviour of the converter and problems with it, such as ringing on the secondary side of the transformer.

As for the schematic which was implemented on the physical PCB, it can be found in Appendix A in its complete form. The individual parts which make up the schematic are dissected in Figures 4.2 to 4.5, which each focus on a different IC and the surrounding components. The schematic is largely based on the example design for the LTC3722, with the main exception of course being the primary side gate drivers. As mentioned before, more footprints than strictly necessary has been added in order to ease tuning and modification of the PCB during the testing phase.

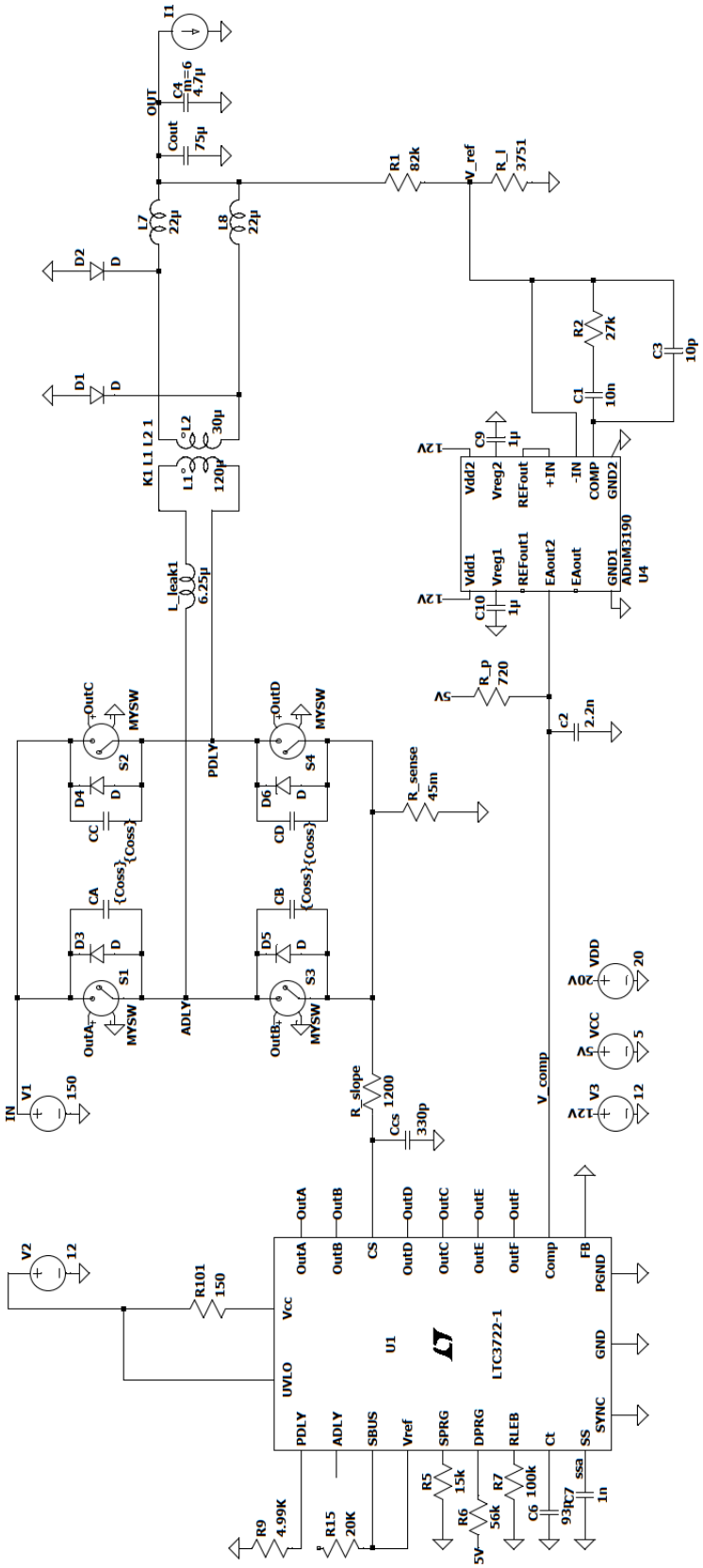


Figure 4.1: LTspice model of the preliminary circuit for the converter. Focus has been placed on the control loop, hence why the only ICs included are the LTC3722 and LT1431.

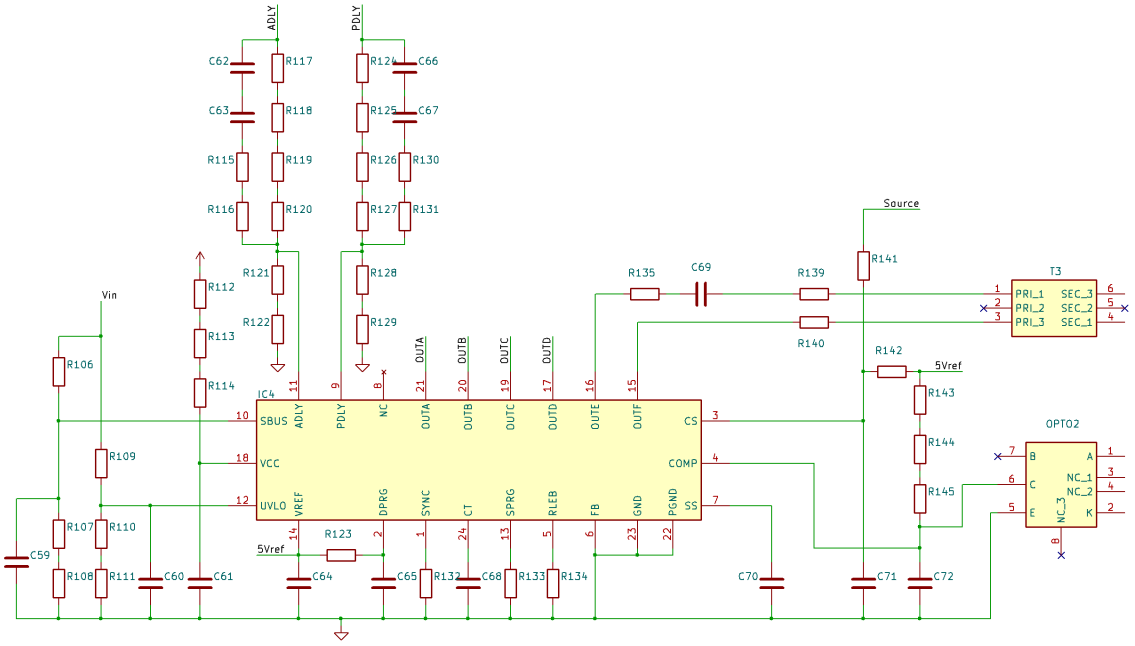


Figure 4.2: The LTC3722-1 and surrounding components. This IC is the brain of the converter and handles the task of providing signals to the gate drivers for all MOSFETs on the PCB, which are timed depending on sensed current and output voltage. The large voltage dividers connecting to pin 9 and 11 will handle high voltage and need to be fine-tuned, therefore the large amount of resistors. The parallel RC dividers add feed-forward to the control, which should improve the response according to Analog Devices.

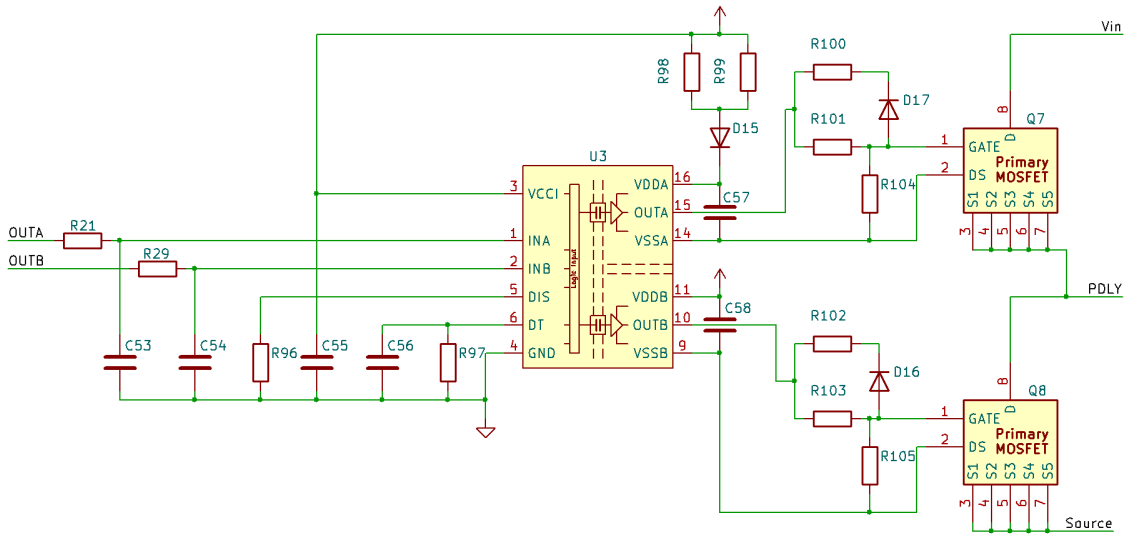


Figure 4.3: Gate drive and the corresponding half-bridge. The input signals, labeled as $OUTA$ and $OUTB$, come from the LTC3722 and are fed through an RC-filter to mitigate the effect from any EMI picked up on the way. For the physical prototype, the turn-off resistors and diodes (R100, D17 etc) were not used.

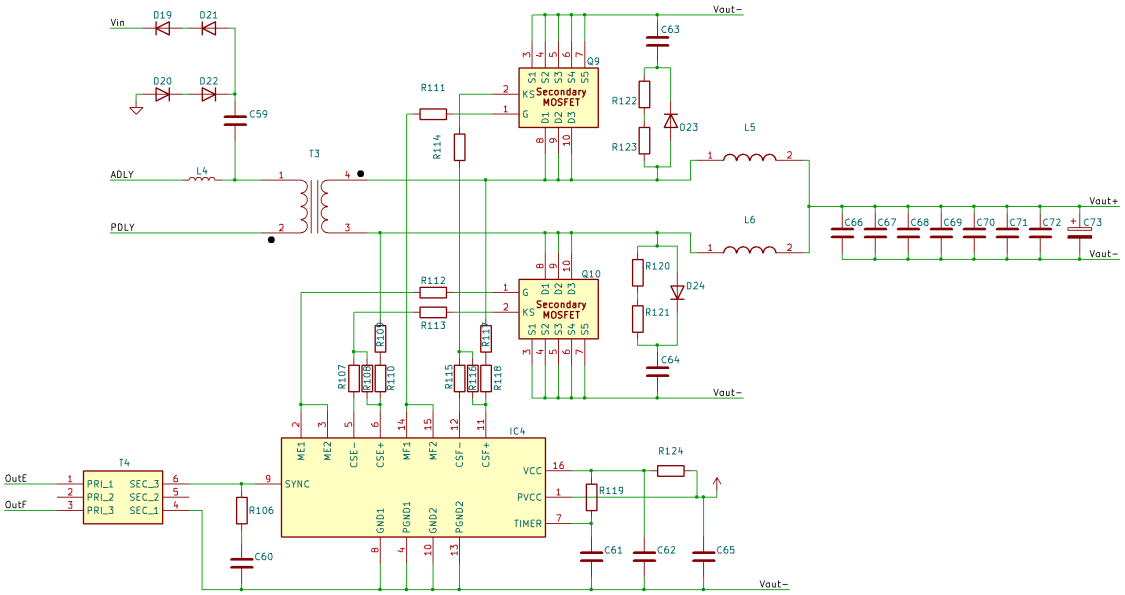


Figure 4.4: Secondary side of the converter. Two MOSFETs are used for rectification, either passively through their body diodes or actively by normal means of MOSFET conduction. The control of the MOSFETs is handled by the LTC3901 secondary side gate driver in the bottom of the figure. It receives input from the LTC3722 through a signal transformer, in order to maintain galvanic isolation.

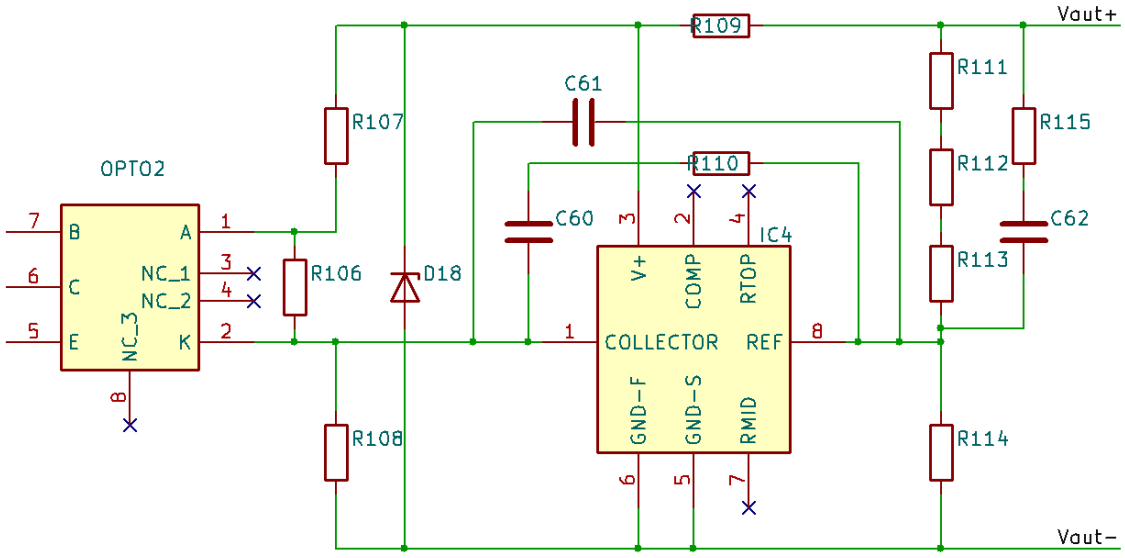


Figure 4.5: Voltage feedback and compensation network, based around the LT1431 programmable reference. By tuning the values of the passive components, the transient behaviour of the converter can be modified to suit applicable requirements. The output is fed back to the LTC3722 through and optocoupler to maintain galvanic isolation.

4.2 Layout

The layout for the PCB was designed in KiCad and required multiple iterations before being sent of to production. The following figures show all the layers of the board as well as 3D renderings depicting the components.

Some general comments about the layout:

- It is not fully optimized. In order to not lose valuable lab time, changes that were not considered critical for functionality were discarded in order to get the PCB sent of for production. An improved version has been in the works since then.
- Due to the requirement for galvanic isolation, a divide can be seen between primary and secondary side of the board (left side primary, right side secondary).
- Copper fill underneath switch nodes have been intentionally avoided, since parasitic capacitance is a problem for PSFB converters.
- The spacing which can be seen between some components, mainly on the primary side, is due to creepage which sets 2.5 mm of distance for the given input voltages the converter will operate at. The use of coating or some other method to prevent discharges could greatly decrease this distance and further reduce the size of the board, at the cost of safe possibilities to test the converter in a lab setting while also being able to easily modify the board as needed.

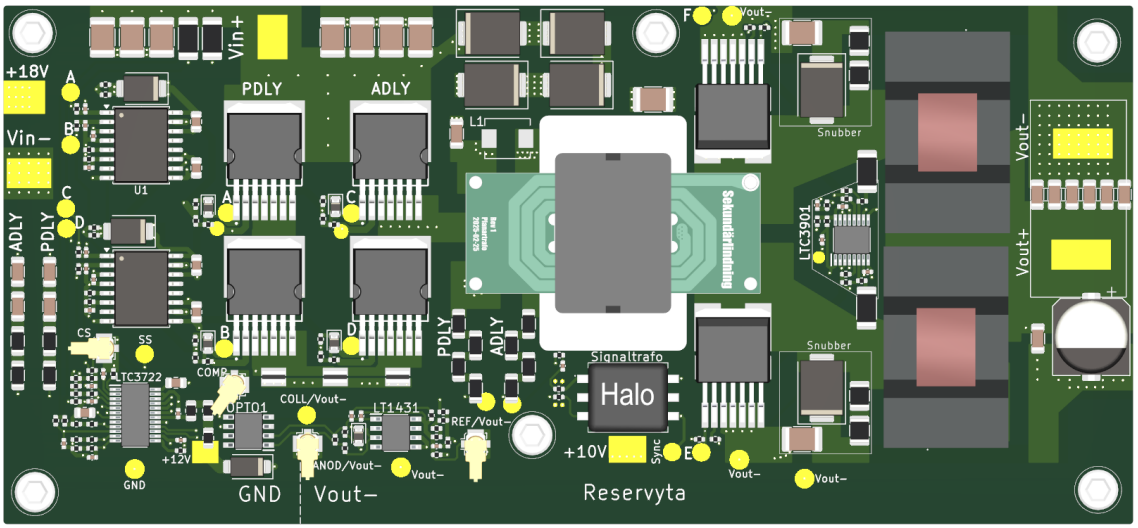


Figure 4.6: Orthographic top view of the PCB. Some main components, left to right: Gate drivers, full bridge, planar transformer, secondary side rectifying MOSFETs, series inductors and lastly output capacitors. Control and feedback has mainly been placed along the lower broad side of the board, with the exception of the secondary side gate driver next to the series inductors.

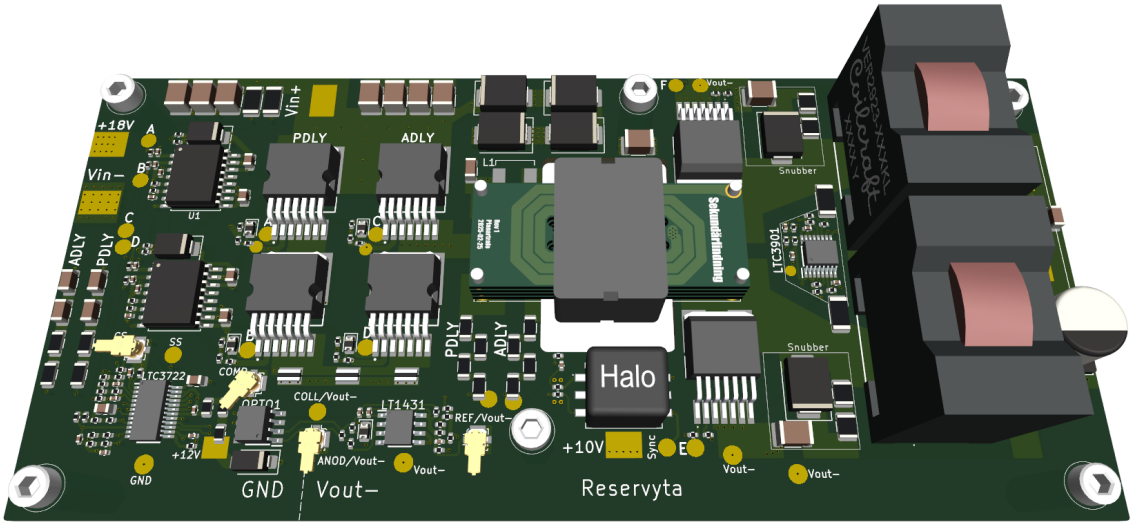


Figure 4.7: Angled top view of the PCB. The tallest components are the magnetics: Planar power transformer, signal transformer (marked *Halo)* and the series inductors. The planar transformer is placed high up for convenience in the lab and will be lowered into the PCB for the final version. The series inductors are quite large due to their current capacity requirements, but will be replaced as well to decrease their height as well as footprint.

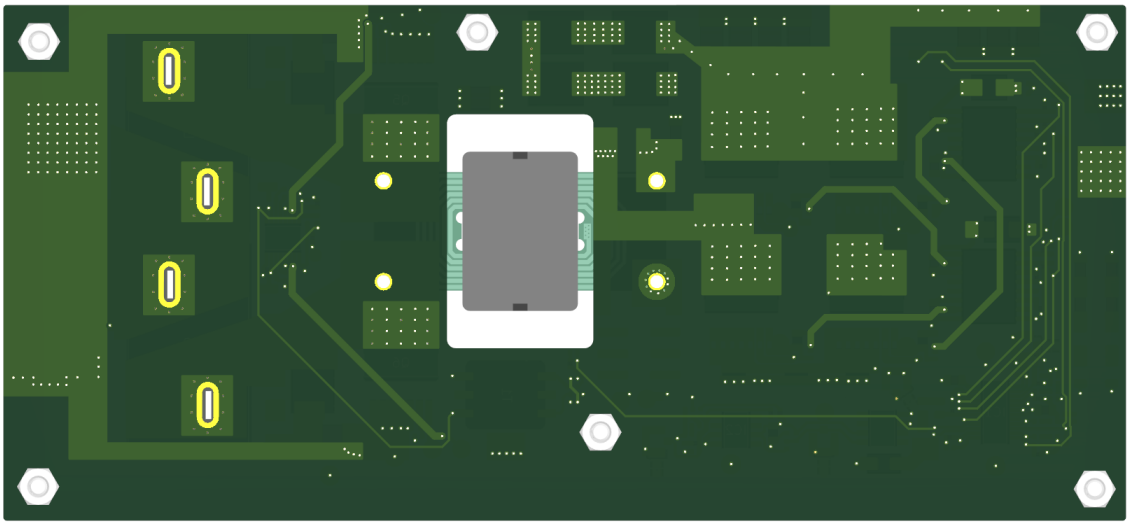


Figure 4.8: Orthographic bottom view of the PCB. Apart from routing signals for gate drive and other critical inputs, this side of the PCB is used for thermal management by conducting heat away from the top side components through vias which is then spread across large copper areas. The main components that are cooled are the MOSFETs as well as the snubber diode. The through-hole pins for the series inductors can be seen to the left in the picture.

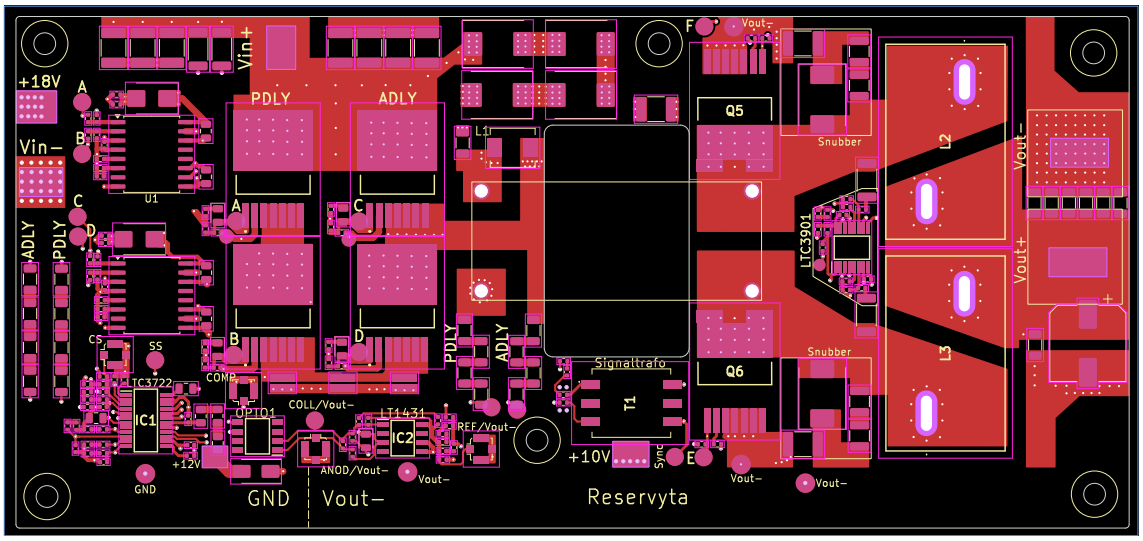


Figure 4.9: Top layer of the board where all the components are placed. Large copper areas have been favoured around the power components in order to increase current carrying capability and to enable more heat dissipation. For the signal traces, the trace widths have been chosen depending on current but overall kept small. A spare area (*Reservyta*) has been left empty at the lower side of the board in case components need to be added afterwards.

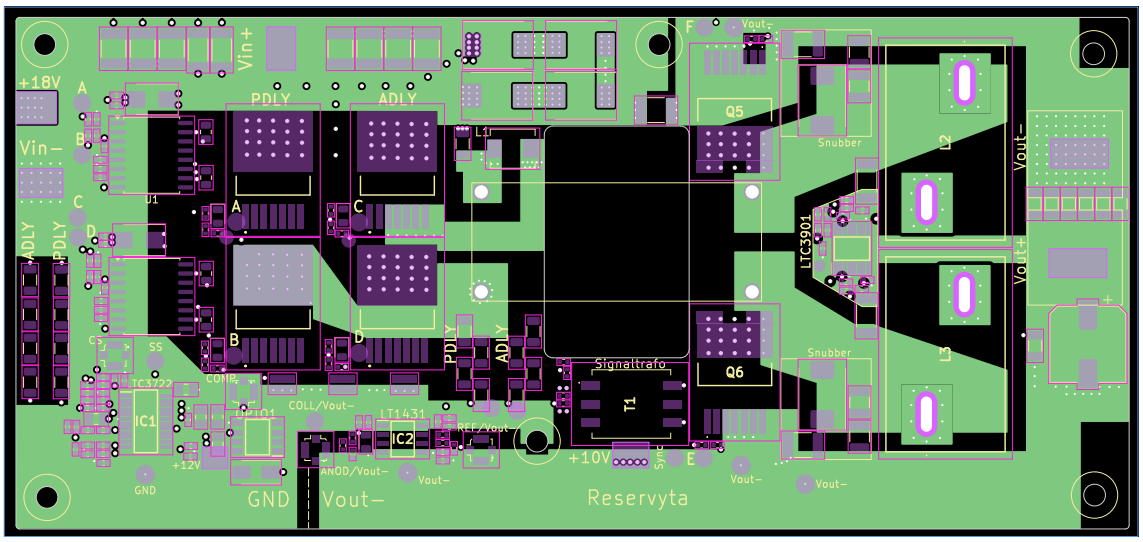


Figure 4.10: First (internal) layer. On the primary side the layer is used as a ground plane, with copper removed below the switch nodes and ADLY/PDLY feed forward components in order to reduce parasitic capacitance. It is also used for carrying current from the left leg of the full bridge to the transformer in order to decrease total resistance. The situation is very much the same on the secondary side, with one zone being the ground plane $V_{out}-$ and the other ones aiding in carrying current from the transformer to the series inductors.

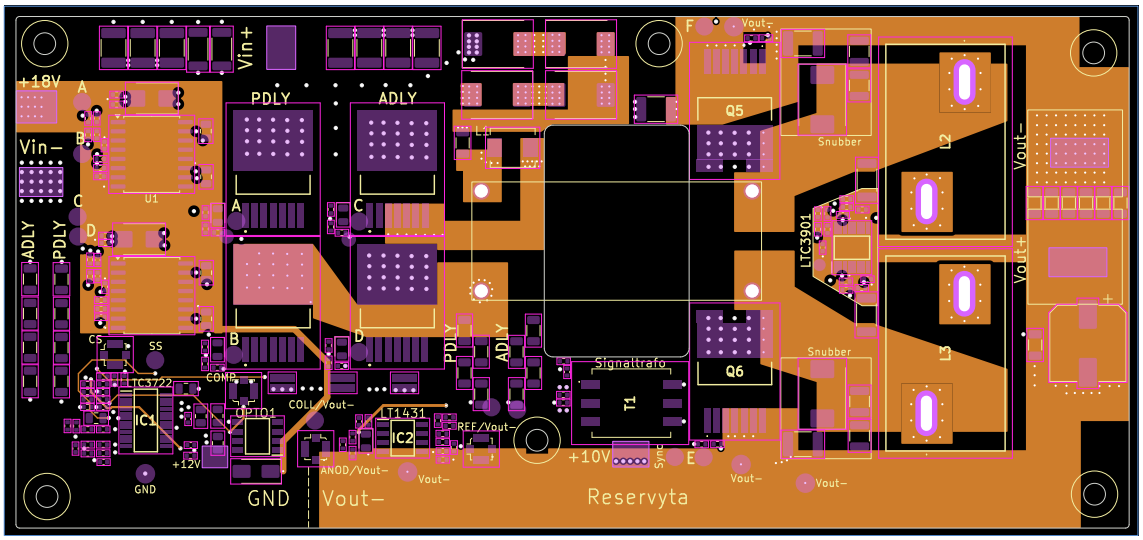


Figure 4.11: Second internal layer. The primary side has replaced the ground plane with an 18 V zone to feed the gate drivers. Further down, a couple of sensitive analogue signals have been routed on this plane in order to shield them by means of having ground planes above and below. These signals include current sense (CS), voltage compensation input (COMP) and the 5 V internally generated reference. The secondary side is the same as the first internal layer.

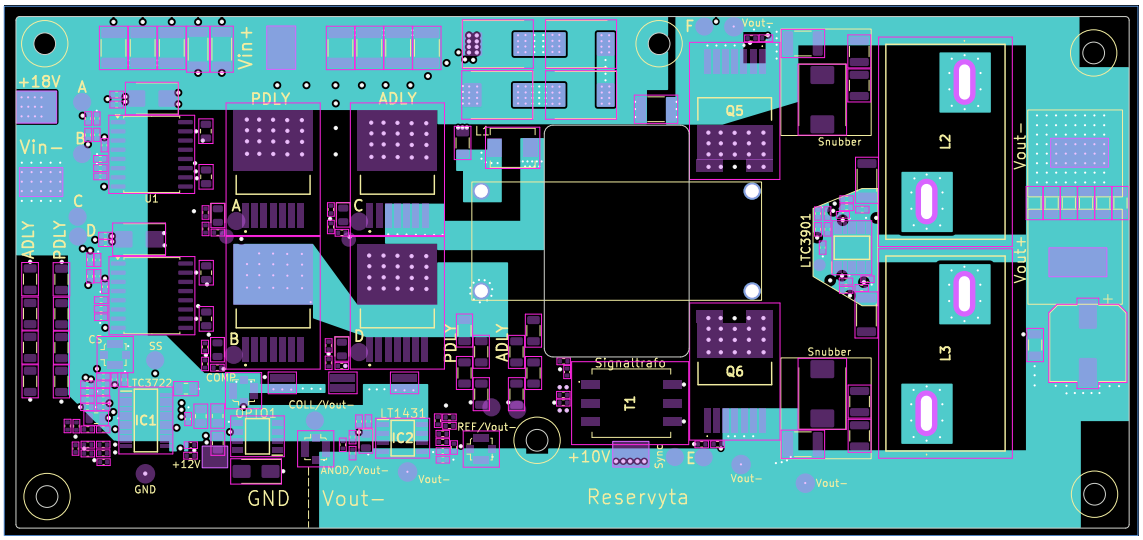


Figure 4.12: Third internal layer, direct copy of the first internal layer. In a more common 6-layer stack-up, this would be a signal layer and not a power plane. The reason for this change is explained in the Figure 4.13.

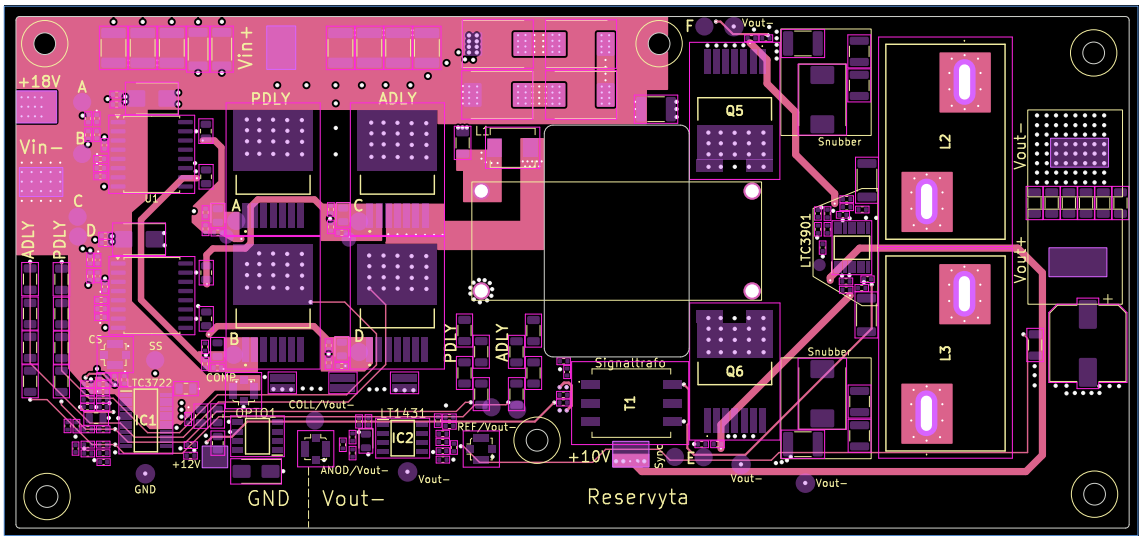


Figure 4.13: Fourth internal layer, signal layer. The wide traces connect the gate drivers with the MOSFET gates and their resistors. Since all MOSFETs have dedicated gate source pins in order to minimize noise, they have dedicated traces returning to the drivers which forms differential pairs with the other gate trace. The routing method which grants the best coupling between the traces is so-called *broadside* differential routing, where the traces are separated vertically on two adjacent layers. The traces are 0.9 mm wide with a 0.12 mm laminate separating them, guaranteeing good coupling. In order to route signals this way, two adjacent signal layers were needed which motivated a change away from the normal stack-up mentioned in Figure 4.12.

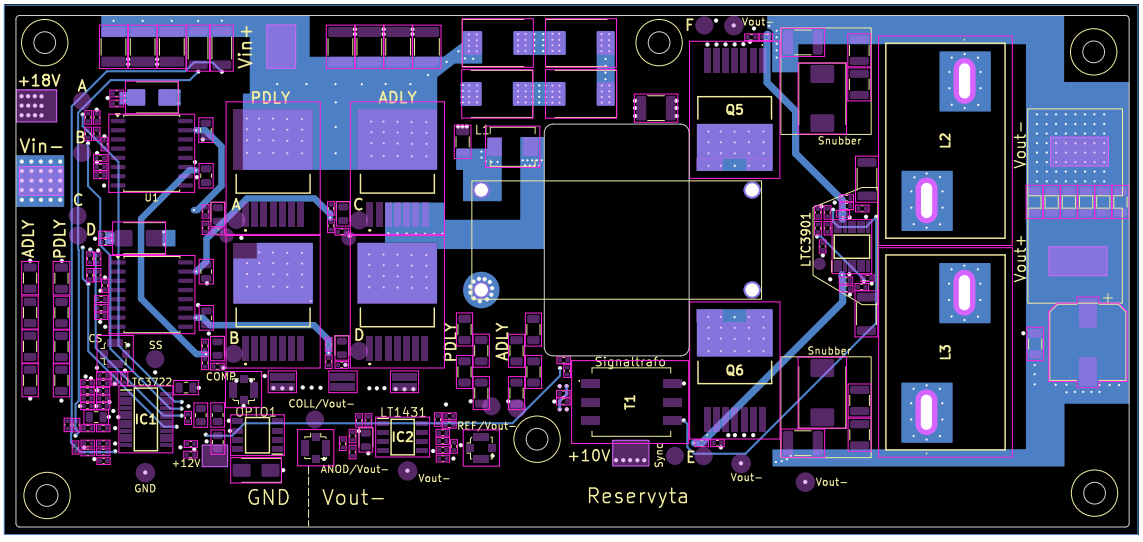


Figure 4.14: Bottom layer of the board. Some signals including gate driver outputs are routed on this layer, which otherwise is used for thermal management for the main heat generating components such as the MOSFETs. Because of isolation requirements, routing of the gate drive outputs for the top switches was somewhat troublesome.

4.3 Transformer design

Several considerations went into the transformer design, from core material to winding size and number. Firstly, choosing an appropriate core material would be the starting point since it would determine the available core sizes. After said core size has been decided on, the winding number and design is calculated to optimize for minimal losses.

4.3.1 Core material

A number of different core materials where considered for the transformer. The requirements included good performance at higher frequencies and relatively high saturation magnetization in order to decrease size, as well as low power loss. In the end, the choice came down to two candidates: 3F36 and 3F46 from FerroxCube. Both materials are developed for high-frequency, but 3F36 is best suited for frequencies below 600 kHz while 3F46 can go up to 3 MHz. Since the transformer operates at half the oscillator frequency, that equates to 400 kHz which is within the span of what 3F36 can handle. Furthermore, 3F36 can handle high flux densities and has a higher resistivity than 3F46 which helps minimizing eddy currents. Their attributes are summarized in Table 4.1.

Table 4.1: Material properties of 3F36 and 3F46

Material	3F36	3F46
Initial permeability at 25°C	1600	750
Recommended max frequency	1 MHz	3 MHz
Resistivity	12 Ωm	5 Ωm
Power loss at 50 mT, 1 MHz, 100 °C	90 kW/m^3	150 kW/m^3
Density	4750 kg/m^3	4750 kg/m^3
Curie temperature	230 °C	280 °C

One more benefit of 3F36 is the tolerance to low temperatures as can be seen in Figure 4.15. If the converter is to be used in harsh environments, it will still maintain a high initial permeability and can keep operating as intended. By comparison, 3F46 exhibits a less linear dependence on temperature and does not seem suited for low temperatures, as shown in Figure 4.16.

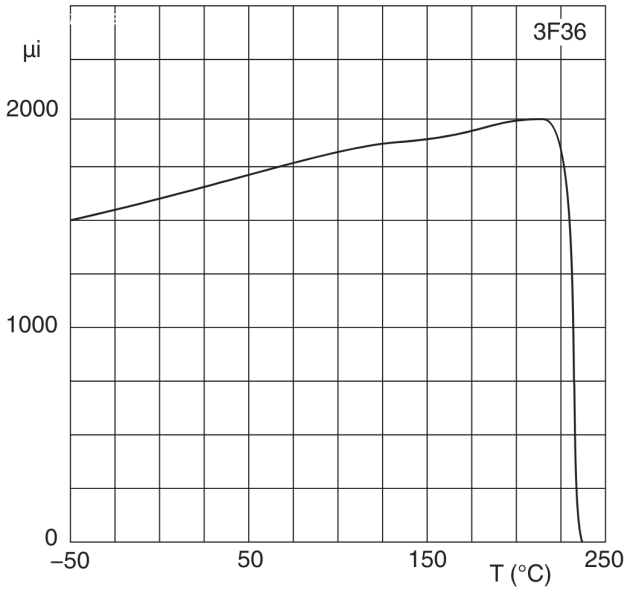


Figure 4.15: Permeability as a function of temperature for the 3F36 material. The material maintains relatively high permeability in colder conditions, making it suitable for applications in harsh environments.

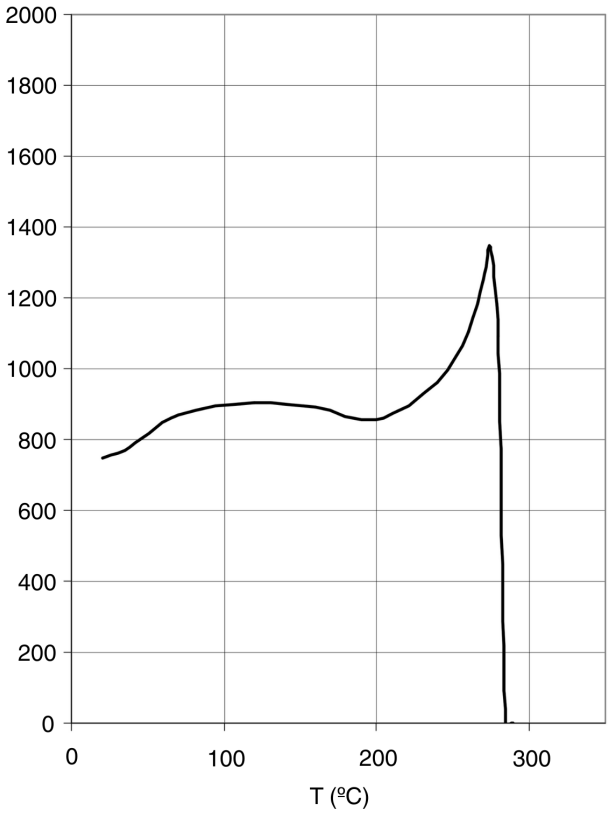


Figure 4.16: Permeability as a function of temperature for the 3F46 material. The curve is stable across higher temperatures where the transformer will usually be operating, but no data is provided for the lower temperature range where functionality of the transformer must still be ensured.

4.3.2 Core size

With the core material selected, the next task was to pick the core shape and size. For planar transformers, planar E cores are well suited and will therefore be used. For a given material, the cores come in certain predefined sizes with similar proportions that range in length from 14 mm to 64 mm. Since a smaller core would result in higher losses, the goals was to find the smallest core with losses that still fit within the transformer power budget. The top four alternatives are presented in Table 4.2, with power loss breakdown and dimensions listed. While the actual spreadsheet used to calculate all the losses is quite a bit longer, all main differences are included here.

Table 4.2: Comparison of different core sizes and their associated losses.

Parameter	**E18**	**E22 a**	**E22 b**	**E32**
Dimensions [mm]	18/4/10	22/6/16	22/6/16	32/6/20
Turns ratio	2	2	3	3
Primary turns	16	12	18	12
A_{eff} [mm^2]	39,5	78,5	78,5	130
Flux density [mT]	111	74	74	67
Core loss [W]	1.66	1.26	1.26	2.05
Copper loss [W]	7.78	3.86	4.52	1.67
Total loss [W]	9.44	5.12	5.78	3.72

Apart from the number of turns and ratio between primary and secondary, the effective area A_{eff} that the flux travels through and the resulting flux density give an indication of how stressed the core is from a magnetic point of view. Once the flux density goes beyond the intended range, saturation causes the core losses to grow at a rapid pace which quickly dwarfes the copper losses. Due to the relatively low number of turns, there is not a lot of freedom in fine-tuning the number of turns to get the split between core and copper losses to an optimal point. The choice landed on the E22 a, which struck a good trade-off between small size and low losses.

For the transformer windings, two parallel PCBs for each side was used in order to lessen the current stress and thus heat generation on any single board, see Figure 4.18a and Figure 4.18b. The PCBs are all two layer in order to maximise cooling and also enable the relative movement of PCBs in relation to each other vertically. This allows one to achieve different levels of parasitic interwinding capacitance, since the vertical distance has a large impact on this parameter. Copper thickness of 105 µm was used in order to enable more current carrying capability while keeping losses within the power budget.

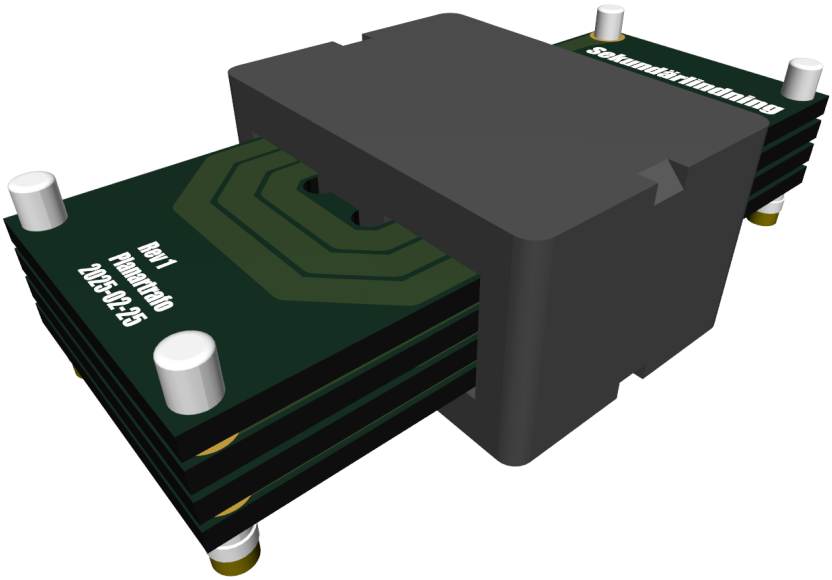
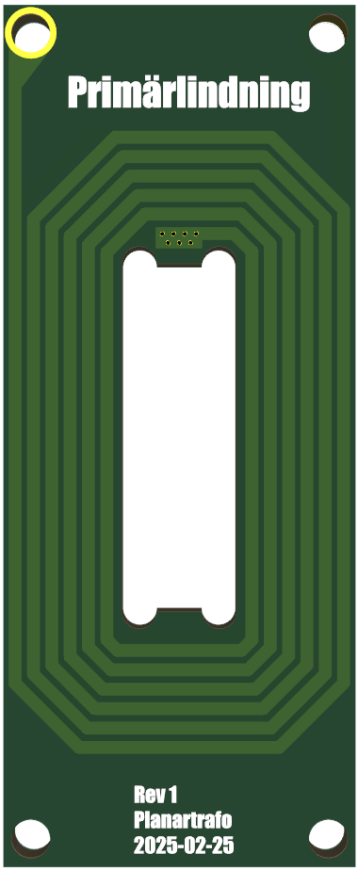
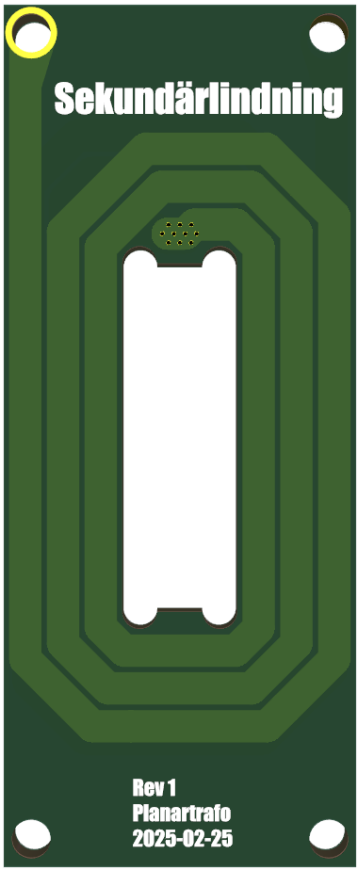


Figure 4.17: 3D model of the planar transformer created in KiCad. Insulation has been omitted from the model in order to decrease time spent on modelling.



(a) Primary side winding for the planar transformer with 12 turns in total, 6 on each side.



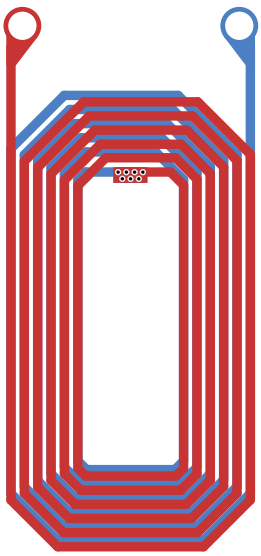
(b) Secondary side winding for the planar transformer with 6 turns in total, 3 on each side.

4.3.3 Parasitic capacitance

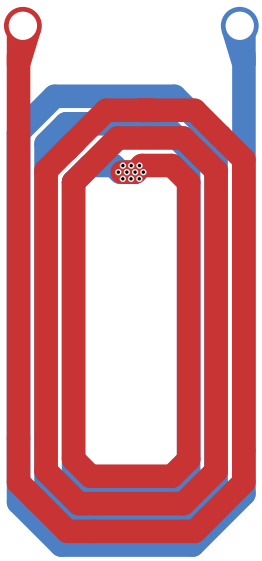
Given the chosen stackup, the parasitic capacitance was calculated as described previously using the stated assumptions. The three sets of windings facing each other were assumed to make up the vast majority of all capacitance and others were neglected. The winding area was measured in KiCad to be 234 mm^2 for one layer. The vertical space within the core is 6.4 mm and four PCBs with a thickness of 1.11 mm leave room for about 0.65 mm of separation between them. The space in-between is occupied by air and Kapton tape, but the thickness of the tape is normally 0.07 mm and it will therefore be ignored. With these values, an estimate can be calculated,

$$C_{transformer} = 3 \cdot \epsilon_0 \frac{234\,\text{mm}^2}{0.65\,\text{mm}} = 9.65\,\text{pF}, \tag{4.1}$$

which is an order of magnitude lower than the output capacitance of the MOSFETs on both sides of the transformer. However, when measuring the primary-to-secondary capacitance of the assembled transformer, the readings showed 40.9 pF, about four times as much as the theoretical value. Measurement errors may in part contribute to this difference, but the choice to neglect capacitive coupling between more distant windings may also have played a part. As can be seen in Figure 4.19a and 4.19b, the windings on the PCBs have nearly complete overlap and should therefore shield each other, prohibiting good coupling between for example the lower winding and other windings above the top winding. The results indicate that such is not the case, assuming the measurement is roughly correct.



(a) Windings on the primary side, top layer in red and bottom layer in blue.



(b) Windings on the secondary side, top layer in red and bottom layer in blue.

4.4 PSFB Measurements

Documentation of all tests, measurements and simulations performed on the converter.

4.4.1 Gate drive

Being one of the major deviations in the design with regards to the recommendation in the LTC3722 datasheet, the UCC21520 gate drivers and their importance are interesting to evaluate. Figures 4.20 to 4.22 show the input signal to the gate drivers and the corresponding gate voltages. The gates were fed 18 V and have a total gate charge of 58 nC. The datasheet claims a typical propagation delay of 33 ns which is clearly met during both turn-on and turn-off. An external gate turn-on resistance of 10 Ω has been added to remove ringing, while a similar resistance for the turn-off event was found to be unnecessary. The small overshoot on the input signal to the gate driver features a small overshoot on both events which could be fine-tuned with the input filter but seems to have no significant impact on the gate driver operation.

Figure 4.20: Measured gate driver propagation delays from the UCC21520 driver. Overall, the response is quite rapid and exhibits low amounts of distortion.

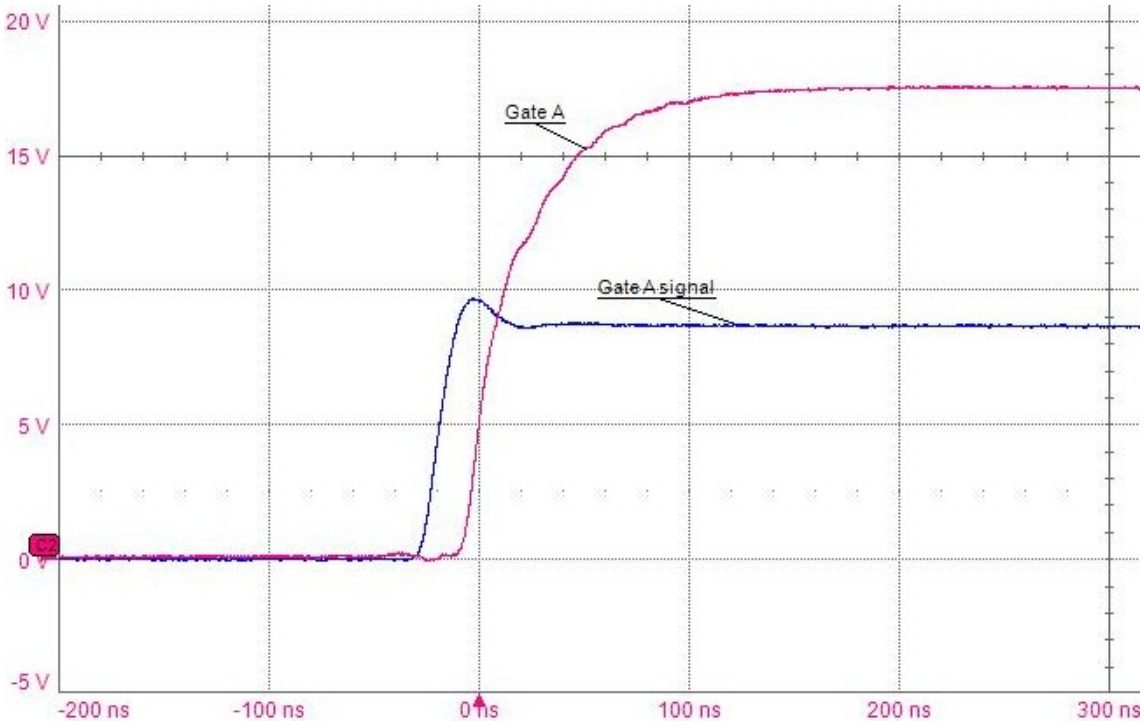


Figure 4.21: Measured gate driver propagation delay from the UCC21520 driver, rising edge. A 10 Ω turn-on resistor limits the rise of the gate voltage in order to handle ringing.

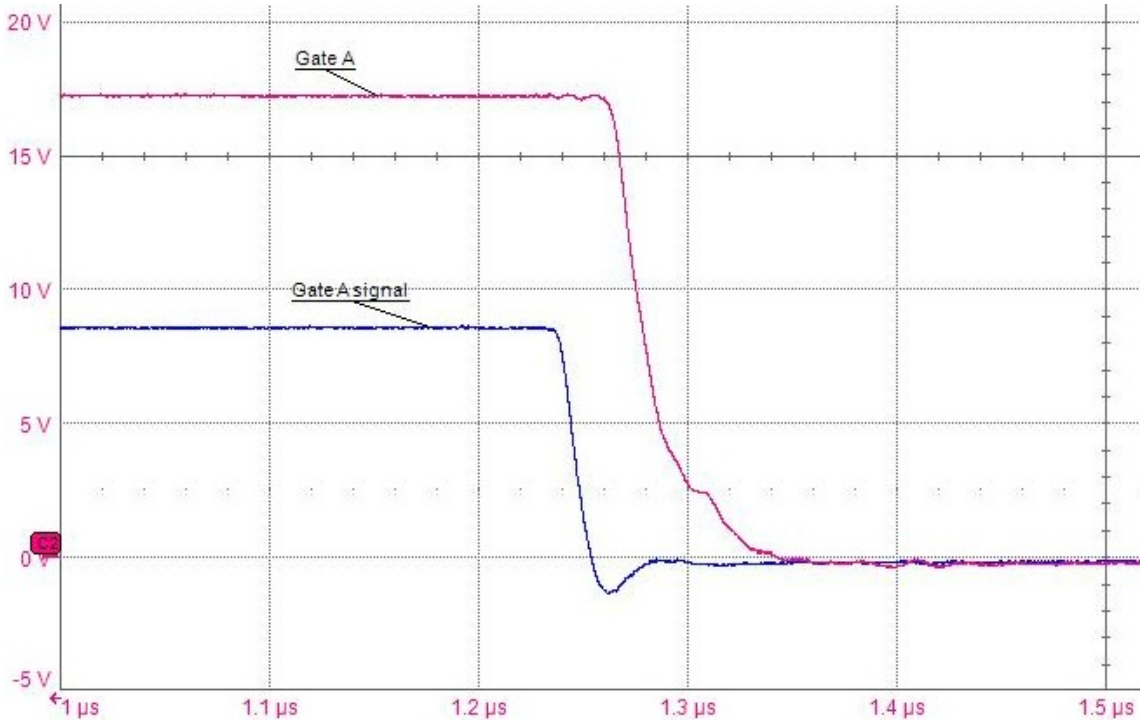


Figure 4.22: Measured gate driver propagation delay from the UCC21520 driver, falling edge. No turn-off resistor was added as it was deemed not necessary, the slope is therefore steeper compared to the turn-on event.

4.4.2 MOSFETs

Given the well-behaved gate signals displayed in the previous section for the full-bridge, one would expect to see equally well-behaved MOSFET waveforms during normal operation. That was however not the result, as can be seen in Figure 4.23. When the gate is turned either on or off, the drain-to-source voltage across the MOSFET does not simply change from high to low or vice versa. Instead, there is a clear dip on both slopes where the voltage initially bounces back before rapidly changing to the opposite state. When including the gate signal from the corresponding MOSFET from the opposite leg, it becomes clear that the dip occurs when the opposite conducting pair of MOSFETs turns off.

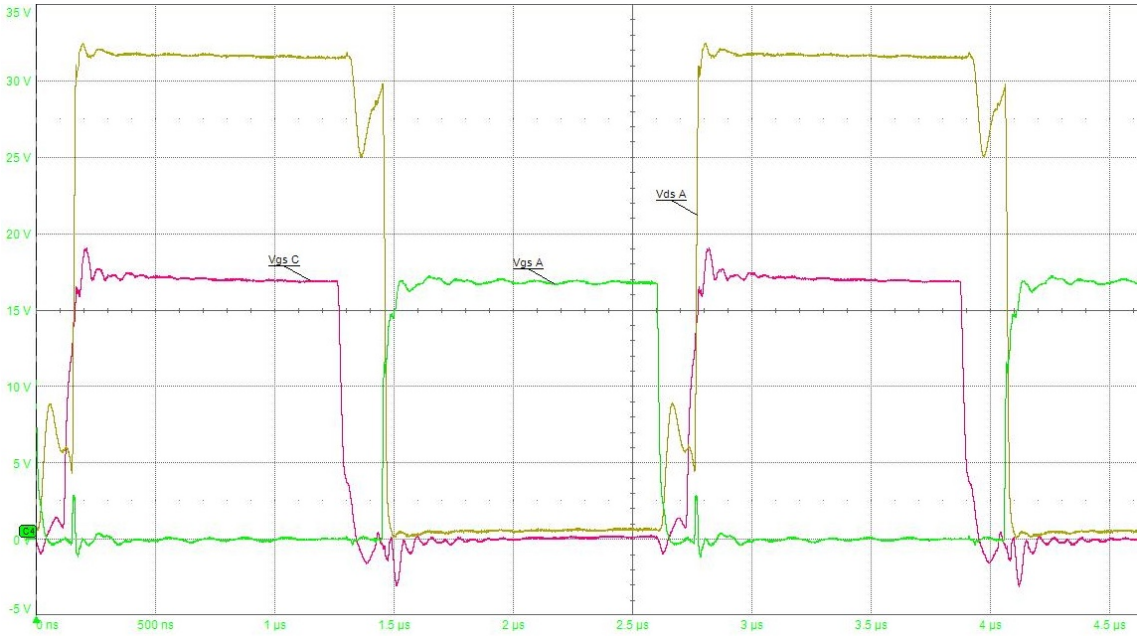


Figure 4.23: Measured waveforms of gate signals for the two top-side MOSFETs in the full-bridge (green and pink) and the drain-to-source voltage for one of them (yellow). The dip appears to be correlated to the period when both FETs are turned off.

4.4.3 Start-up

One of the more common transients the converter is subjected to is the start-up sequence. For this measurement, auxiliary voltages and a load corresponding to half of full power have been applied before the input voltage. The waveform in Figure 4.24 shows the response of the converter which shows a controlled start-up with a slight overshoot.

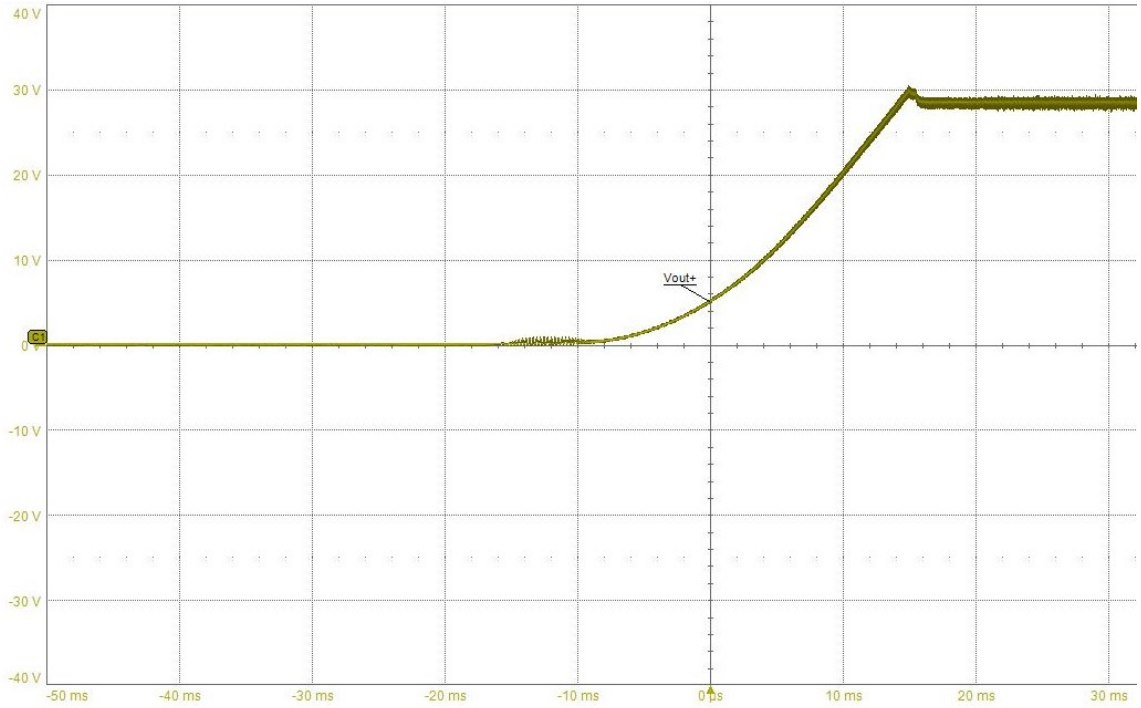


Figure 4.24: Output voltage during start-up of the converter at 250 W output power and 150 V input voltage. A controlled rise is followed by a slight overshoot and then a stable output.

4.4.4 Transformer waveforms

In order to see how the converter is operating at any moment, the single waveform which gives the most insight is the transformer waveform. Nearly all implemented control loops serve the purpose of manipulating this waveform to achieve the desired output from the converter, with the exception of the active rectification.

When no regulation is taking place, such as for lower input voltages, the transformer will transmit a simple square wave with the amplitude of the input voltage. The main point of interest here is the ringing, which was quite noticeable on the secondary side. The implementation of RC snubbers across the secondary side MOSFETs decreased the ringing to a point where full output power could be achieved without overheating said MOSFETs. The waveforms are presented in Figure 4.25, which shows that quite a bit of ringing is still present despite the snubbers. One possible cause could be oscillation between the transformer leakage inductance and the output capacitance of the secondary side MOSFETs.

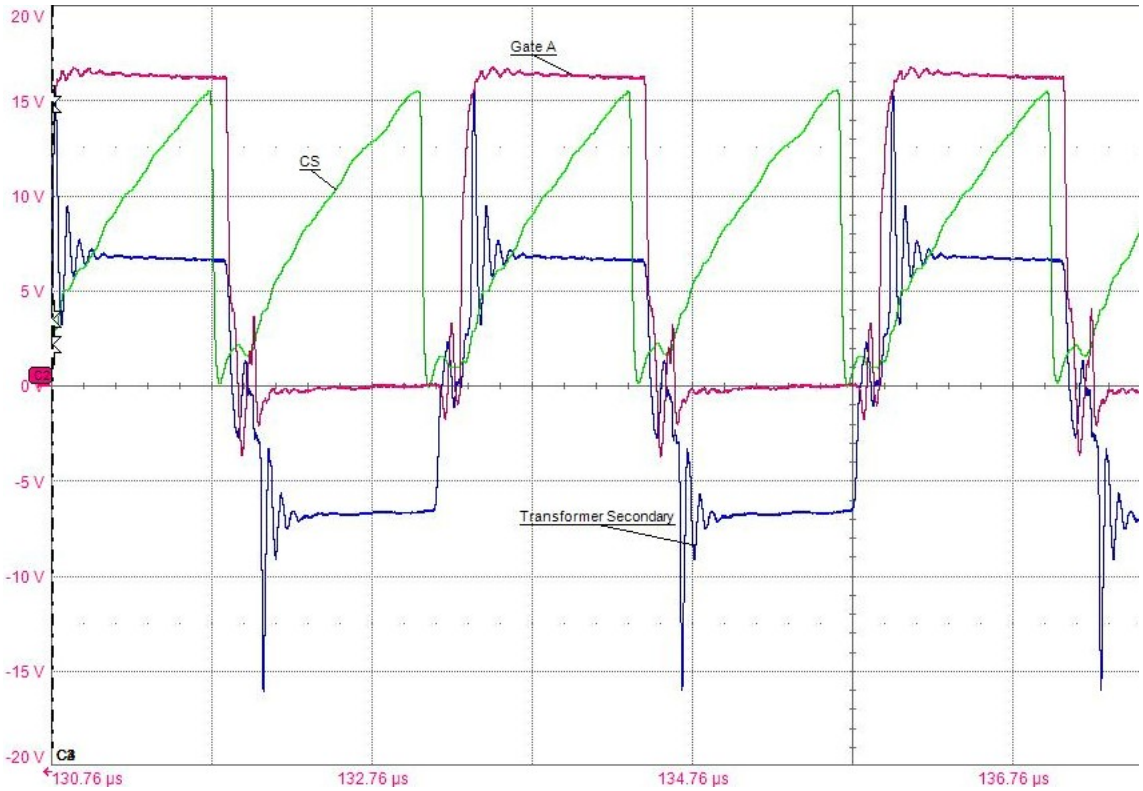


Figure 4.25: Waveforms at unregulated full power, featuring the transformer secondary side (blue) along with the gate signal for switch A (pink) and current sense (green). Input voltage was set at 137 V in order to reach the target 28 V output voltage with no regulation.

Once regulation kicks in at higher input voltage, the transformer waveform changes shape as it starts to freewheel for parts of the switching cycle. As discussed in previous chapters, the output voltage is fed back through an error amplifier which controls the COMP signal, which in turn regulates how high the current sense signal can rise and how long the conduction phases are. Figure 4.26 shows the transformer typical waveform, with distinct plateaus that correspond to the freewheeling periods. The transformer is was probed on the primary side for this measurement, hence the lower ringing compared to Figure 4.25. One phenomenon which can be observed in Figure 4.26 is the difference in width for the two transformer peaks, where the left peak is visibly shorter. The reason is likely some missing fine-tuning of the voltage dividers from the two switch nodes ADLY and PDLY, since they play an important role in how the switching legs operate in regards to each other.

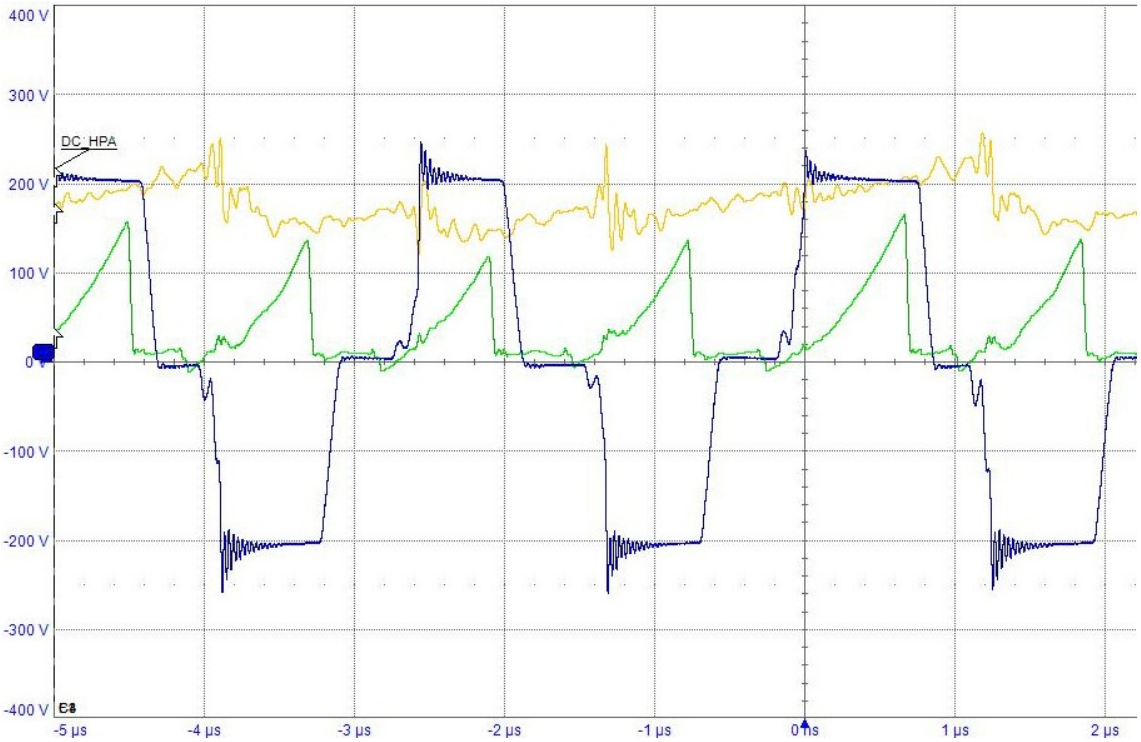


Figure 4.26: Waveforms at regulated partial power. The transformer primary side waveform (blue) showcases the freewheeling part of the converter operation when voltage plateaus at zero, as a result of the current sense signal (green) reaching its maximum set by the COMP signal (yellow).

4.4.5 Active rectification

In order to increase total converter efficiency, active rectification using the secondary side MOSFETs was attempted. While an input signal with the desired shape was transmitted to the LTC3901 secondary side gate driver from the LTC3722 via the signal transformer, the desired gate drive output was not achieved. One MOSFET was turned on for the entire duration it was supposed to, while the other one was only given a high gate voltage input for half the intended duration. It seemed as if the gate driver sensed an incorrect voltage difference over its sense resistors and shut of the MOSFET, incorrectly assuming that current was conducted the wrong way. Measurements with probes showed that radiated EMI seemed to be the issue, with random voltage fluctuations which were larger than the built-in threshold in the gate driver which protected against current being conducted in the wrong direction.

4.4.6 Output characteristics

One design specification dictated that the output voltage ripple should be limited to 2%, which corresponds to 560 mV given the specified output voltage. Figure 4.27 shows the output voltage at full power but limited input voltage of 137 V due to lack of regulation. The ripple is clearly correlated to the switching events that cause a maximum ripple of about 400 mV, within margin of the specified 560 mV.

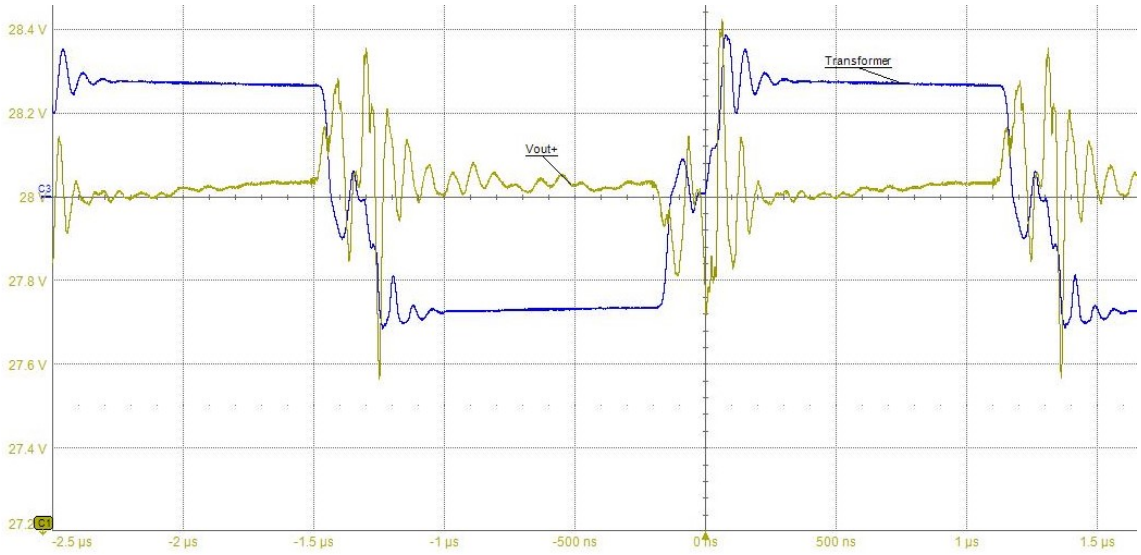


Figure 4.27: Output voltage (yellow) and transformer waveform (blue) at full load of 500 W and 137 V input voltage.

When enabling regulation, an oscillatory behaviour can be seen on the output voltage. The voltage reference on the controller was set to 28.5 V which the controller maintained quite stable. Figure 4.28 shows the faster oscillation of around 4 MHz and Figure 4.29 shows the slower oscillation at around 100 kHz. Suboptimal component values in the compensation network is likely the cause of the unstable behaviour.

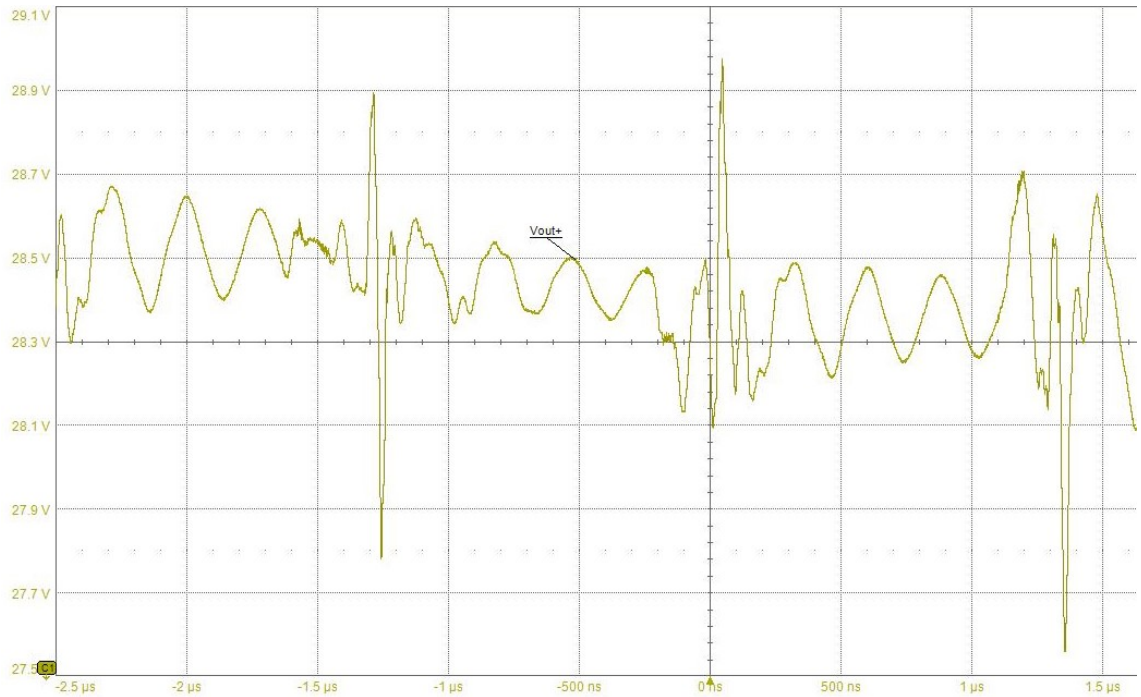


Figure 4.28: Regulated output voltage set to 28.5 V at 300W power and 150 V input voltage. The waveform exhibits high-frequency oscillations which are likely caused by control loop instability.

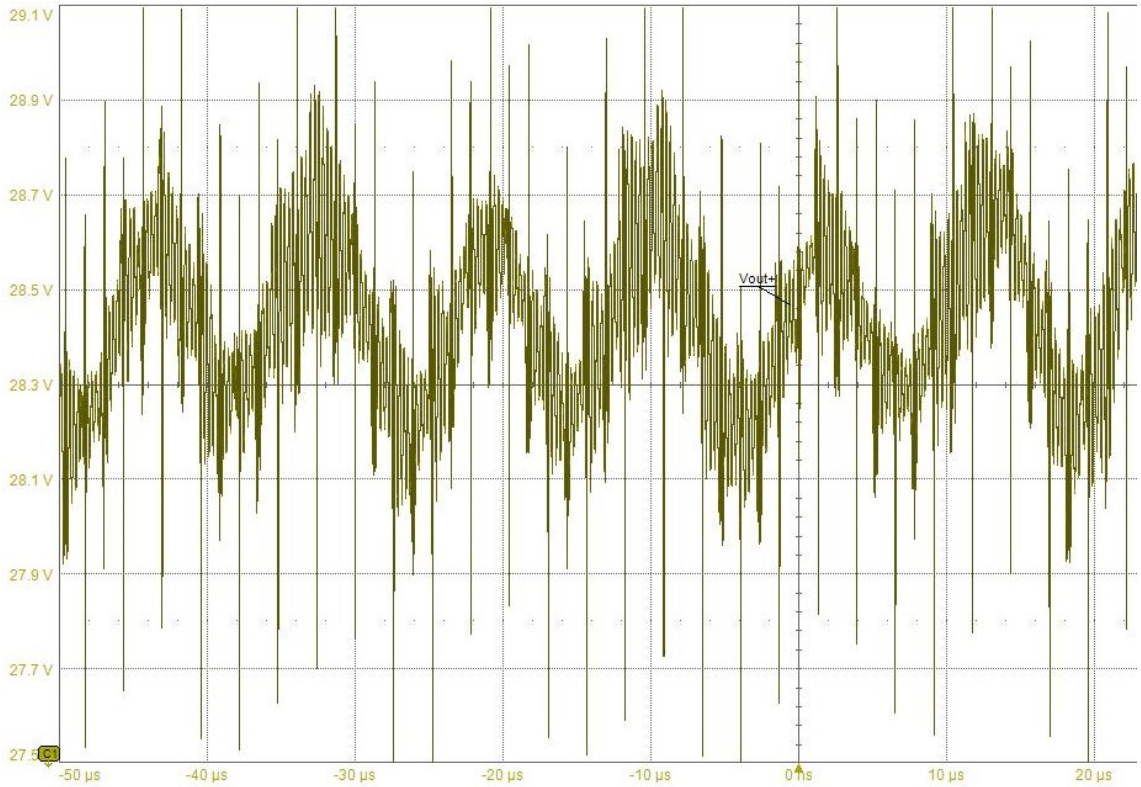


Figure 4.29: Regulated output voltage set to 28.5 V at 300W power and 150 V input voltage. Longer duration oscillations are clearly visible with a frequency of about 100 kHz.

4.4.7 Thermal imagery

In order to assess the temperature rise the transformer windings would experience in the lab once the converter was set up, a measurement was done beforehand where a DC current equal to the expected AC RMS current was fed through one winding at a time. A thermal camera was used to measure the temperature across the windings, which can be seen in Figure 4.30 and Figure 4.31. The primary side winding reaches the higher maximum temperature, 63 °C compared to 51 °C on the secondary side winding. The cause for the difference is attributed to the difference in trace width which is much lower on the primary.

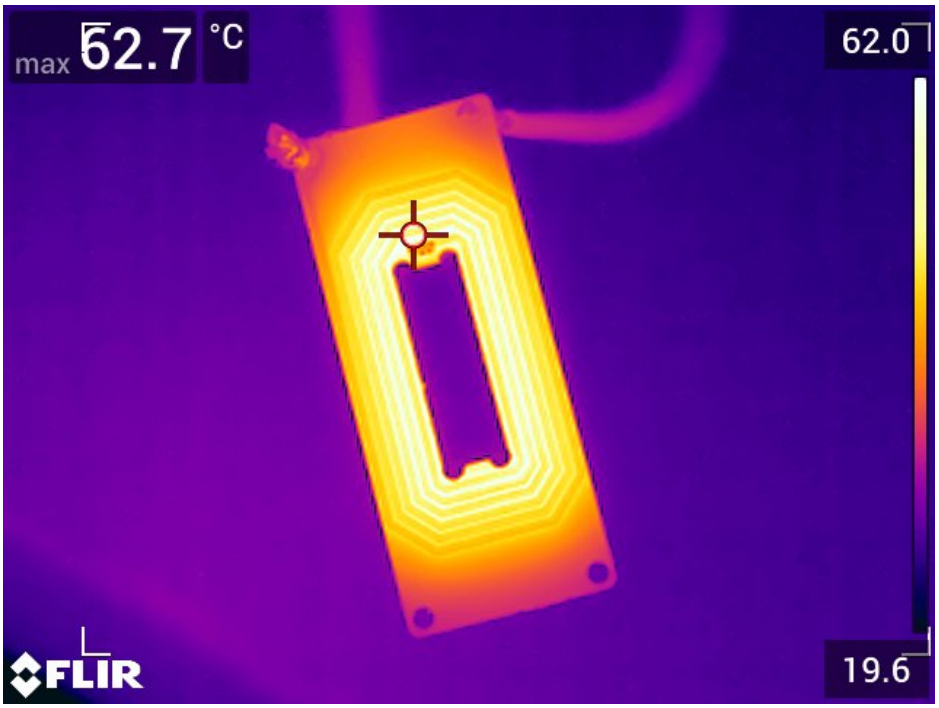


Figure 4.30: Thermal image of the primary side transformer winding conducting a DC current of 2.05 A, equal to the RMS value of the AC current. The temperature reached steady state at 62.7 °C, ambient temperature of 21 °C.

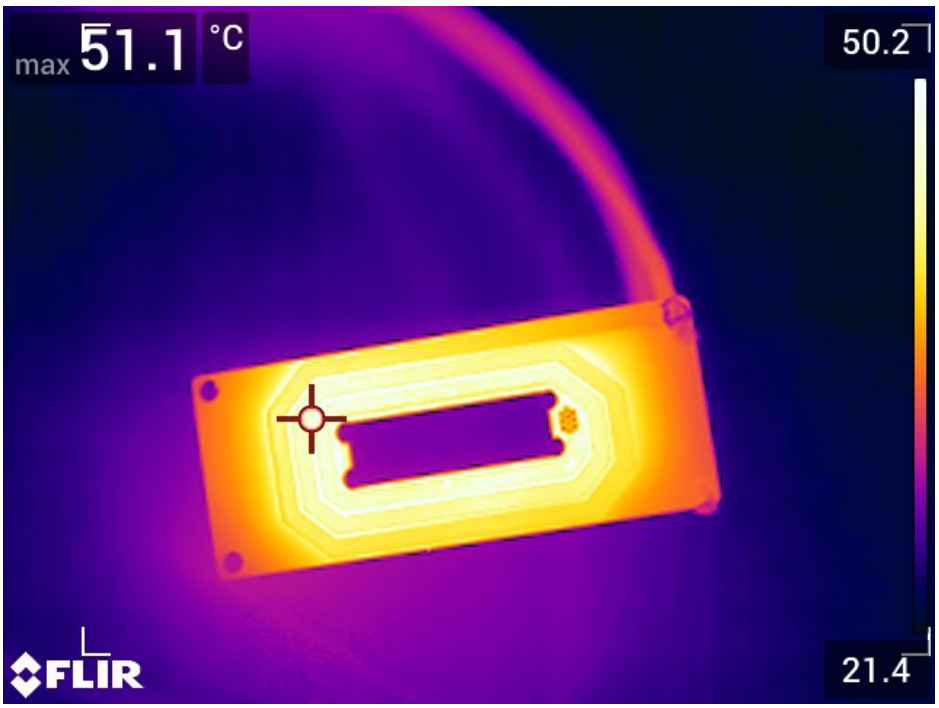


Figure 4.31: Thermal image of the primary side transformer winding conducting a DC current of 4.1 A, equal to the RMS value of the AC current. The temperature reached steady state at 51.1 °C, ambient temperature of 21 °C.

When running the converter at full load and unregulated, it was the secondary side that reached the highest temperatures as can be seen in Figure 4.32. The previously discussed ringing on the secondary side were dealt with by the use of snubbers that dissipated the energy in the ringing as heat. As a result, the snubbers reached the highest temperature of just below 100 °C. A fan was used to provide moderate air speed in order to not overheat the components. One can note the relatively low temperature of the series inductors which is an indicator that smaller, possibly moulded inductors could be used instead to save on board area. The transformer temperature ended up being similar to the temperature reached by the windings in the DC load test above, despite the addition of a fan. The tight packaging of the laminates, combined with the insulation tape used to prevent short-circuit, likely impeded the airflow and thus cooling capability. Lastly, the primary side full-bridge ran at a quite moderate and even temperature, despite the lack of ZVS switching. Since regulation was not used for this test, due to control loop instability and full load, the input voltage was restricted to 137 V in order to not exceed the nominal voltage on the output. The lower-than-intended voltage meant that switching losses were lower than they would have been during normal operation, which helped keep the MOSFETs cool. The large thermal contact between the drain tabs and copper likely also helped quite a bit.

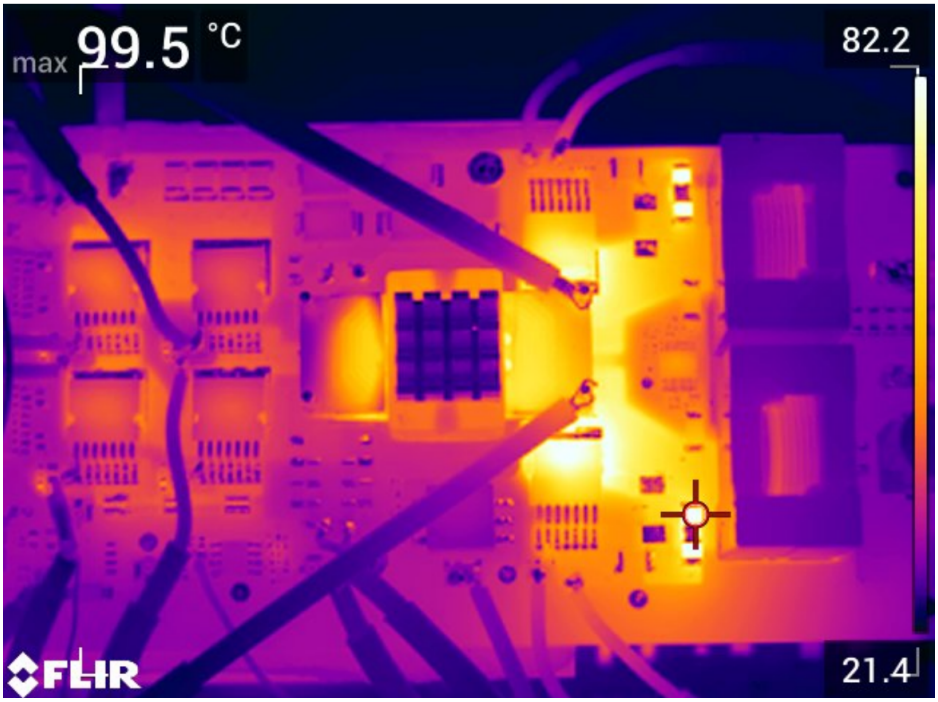
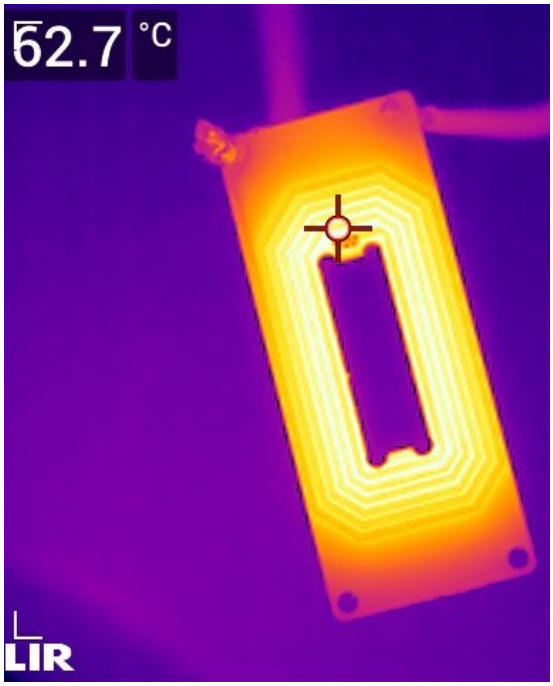


Figure 4.32: Thermal image of the converter running at full load. Due to ringing on the secondary side, the snubbers ran the hottest at 99.5 °C.

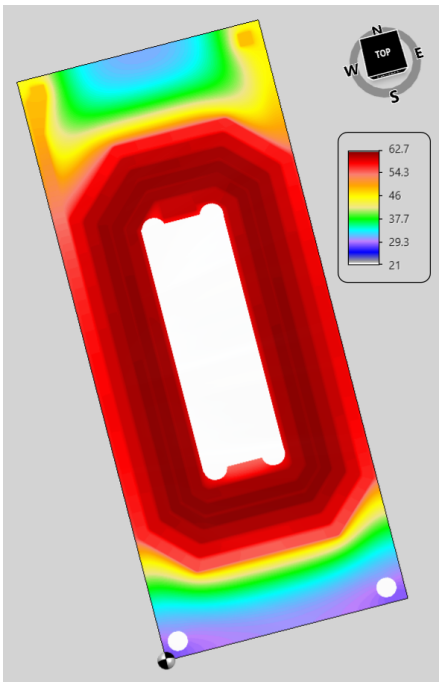
4.4.8 Planar transformer thermals: Model vs measurement

Since the transformer has a high probability of becoming the component which thermally limits the converter, it is of great interest to validate the TRM model against the lab measurements. An accurate model could allow designers to get a good grasp of maximum temperatures before even sending the product of for prototype manufacturing, saving both time and resources.

The results from the simulation of the primary side PCB is compared to lab measurements using a thermal camera in Figures 4.33a and 4.33b. Both are based on a 2.1 A DC current fed through them at an ambient temperature of 21 °C and are steady-state. The heat distribution shows good correlation between simulation and measurements. For absolute temperature, some tuning had to be done in software to the thermal conductivity from the PCB to air. This value will depend on factors such as the solder mask thermal conductivity, its thickness etc. In the end, a value of 32.95 $W/m^2 \cdot K$ yielded the most accurate results with both boards, simulated and real life, reaching a maximum temperature of 63 °C.

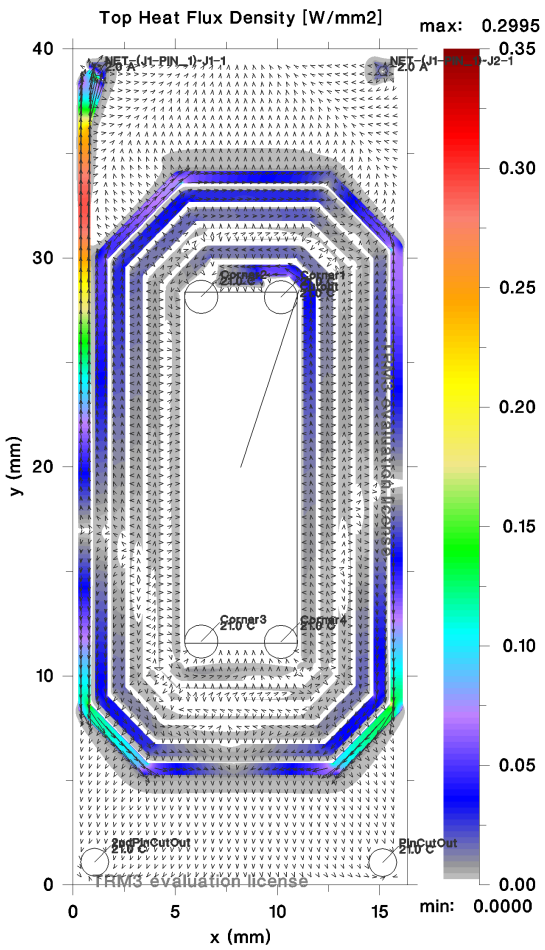


(a) Primary side winding at equivalent full load current of 2.1 A viewed through a thermal camera.

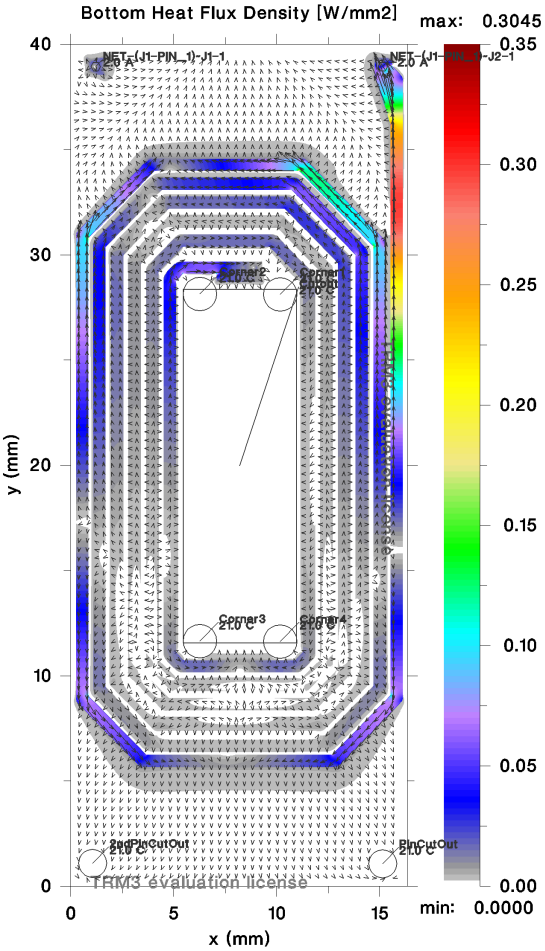


(b) Primary side winding at equivalent full load current of 2.1 A simulated in TRM.

Since the model proved capable of producing realistic temperature distributions, it can be of interest to see how the simulation predicts that heat will flow in the windings. The results in Figure 4.34a and 4.34b show a not entirely intuitive result. The flux seems to be greatly more pronounced at the outer parts of the PCB and especially near the corner where the trace meets the copper pin that connects the transformer laminates to each other and the main PCB.

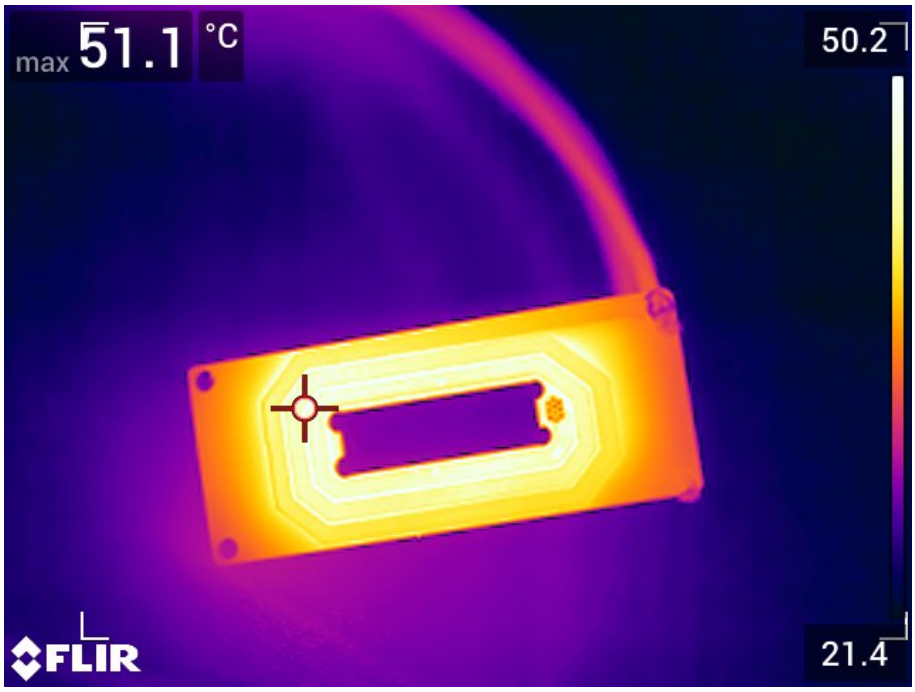


(a) Simulated heat flux on the top layer of the primary side winding.

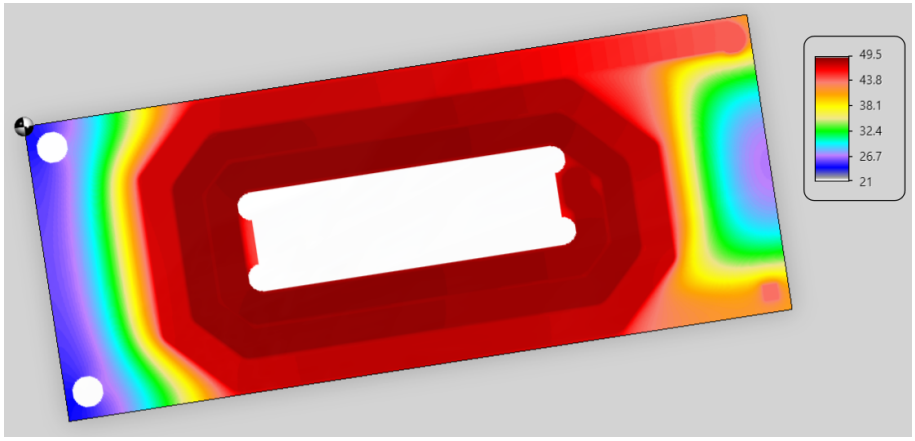


(b) Simulated heat flux on the bottom layer of the primary side winding.

Moving on to the secondary side PCB, which will show if the simulation can reliably produce accurate results or not. Given that the thermal conductivity parameter was tuned to match the measurement on the primary side PCB, one cannot truly tell if the program is correct from said measurement alone since it was tweaked in order to match real life measurements. However, if the simulation for the secondary side PCB shows accurate results with the same thermal conductivity, that would indicate that the model works. The thermal imagery and simulation result are shown in Figures 4.35a and 4.35b. At a DC current of 4.1 A and ambient temperature of 21 °C, the peak trace temperatures reached 51.1 °C for the measurement and 49.5 °C for the simulation. Just like for the primary side windings, the innermost traces on the board reach the highest temperatures. The absence of an adjacent colder surface, such as the bare laminate at the short ends of the board, is a probable reason for this phenomenon. Given this result, it could be of interest to look into varying trace width along the winding to achieve a more even temperature distribution.

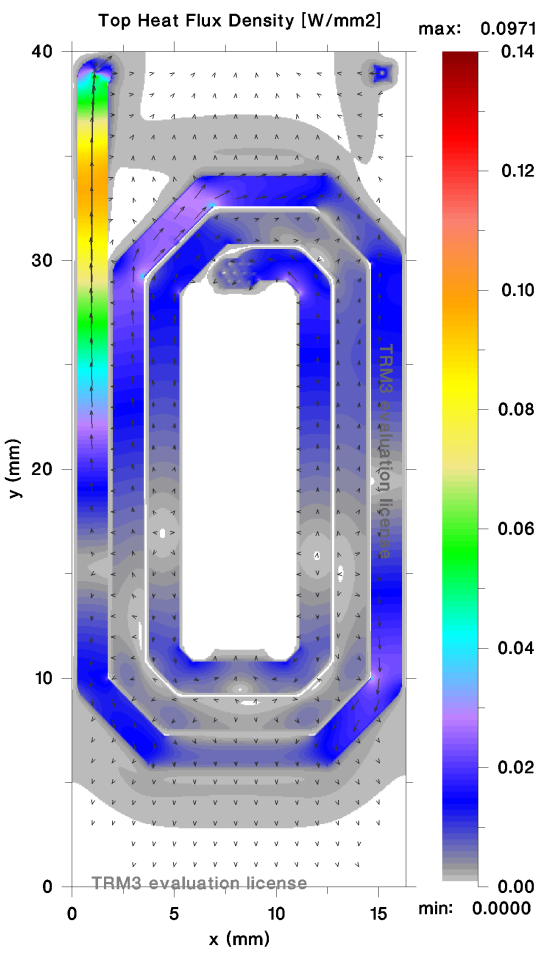


(a) Secondary side winding at equivalent full load current of 4.1 A viewed through a thermal camera.

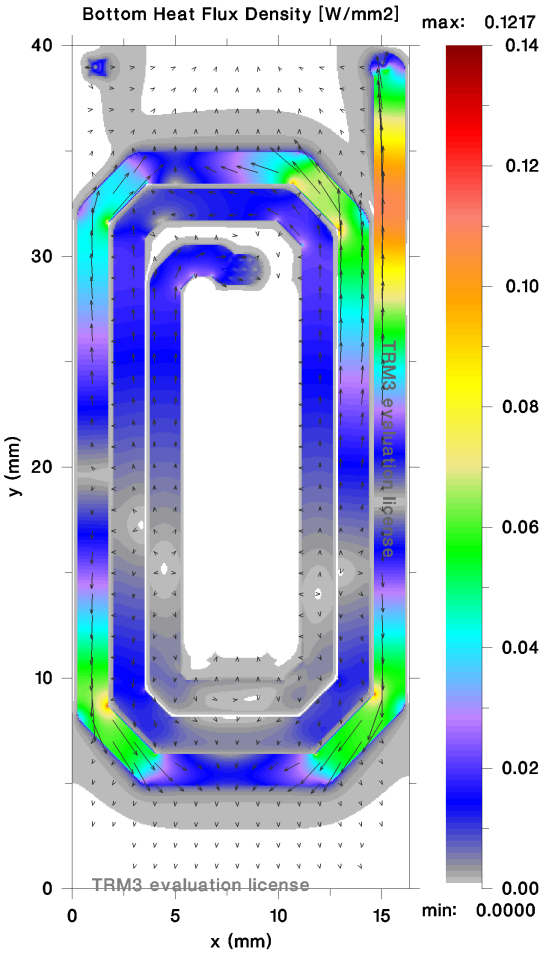


(b) Secondary side winding at equivalent full load current of 4.1 A simulated in TRM.

Returning to the heat flux, the results for the secondary side came out slightly different than those on the primary side. As shown in Figure 4.36a and 4.36b, the heat flux is more evenly spread across the windings compared to the primary side. The wider traces likely play a part in the difference in distribution, but the seemingly random gaps on the inner traces are more difficult to explain. It might be due to the way the algorithm solves the heat equations locally in the mesh, but that is outside the scope of this report.



(a) Simulated heat flux on the top layer of the secondary side winding.



(b) Simulated heat flux on the bottom layer of the secondary side winding.

4.4.9 Efficiency

As the last measurement on the converter, the total system efficiency was measured. This included power provided by the auxiliary power supplies in order to get an idea for what efficiency numbers that can be expected, should they have been supplied directly by the PCB. Due to the control loop instability, the test was done with no regulation in order to test the entire output power range. Measurements were done at 100 W intervals, with the data stated in Table 4.3 and visualized in Figure 4.37. As with most switched power electronic converters, the efficiency increases as load increases. This is partly because some losses are quite invariant to load, making low load scenarios less efficient compared to full load. A maximum efficiency of about 90 % is reached at around 300 W and stays at that level all the way to 500 W. It should be noted that the simulations showed a decreasing total efficiency at higher power levels, which seemed to be due to auxiliary power to gate drivers and such consuming more energy than in reality. Future iterations of the simulation could address this problem in order to create a more accurate model.

Table 4.3: Input and output measurements for attaining converter efficiency over load range with maximum phase-shift, no ZVS and without active rectification.

Input					Output			
Voltage	**Current**	**Power**	**Auxiliary**	**Total Power**	**Voltage**	**Current**	**Power**	**Efficiency**
129	0.9	116.1	1.3	117.4	28.1	3.6	100.1	0.853
132	1.7	225.1	1.3	226.3	28.1	7.1	200.7	0.887
134	2.5	334.8	1.3	336.1	28.0	10.8	301.8	0.898
135	3.2	436.1	1.3	437.3	28.0	14.1	393.7	0.900
137	3.9	529.2	1.3	530.5	28.1	17.0	478.9	0.903

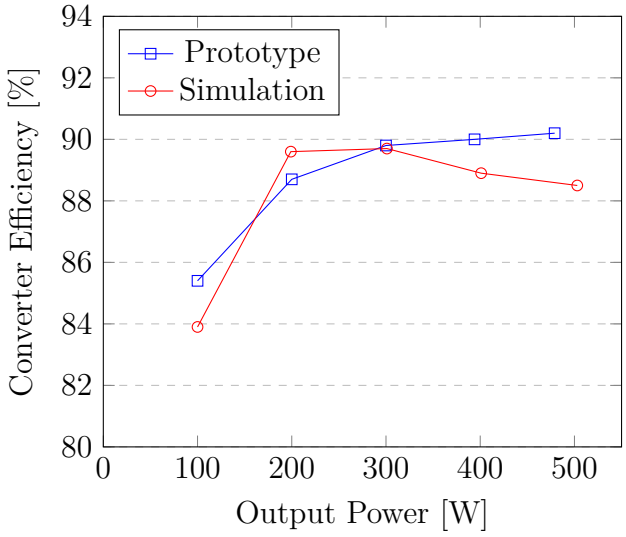


Figure 4.37: Efficiency of the converter when not in regulation.

4.5 Competitor Measurements

The Vicor module's efficiency and output voltage ripple from its datasheet are presented below in Figures 4.38 and 4.39. A peak efficiency of 94 % can be noted at a input voltage similar to the one used for this projects test, though it does decrease for higher input voltages at low to medium load. The output voltage ripple falls well within the set voltage ripple requirement of 2 %. Overall, the PSFB converter did not beat the Vicor module on these two criteria, though the differences were not vast.

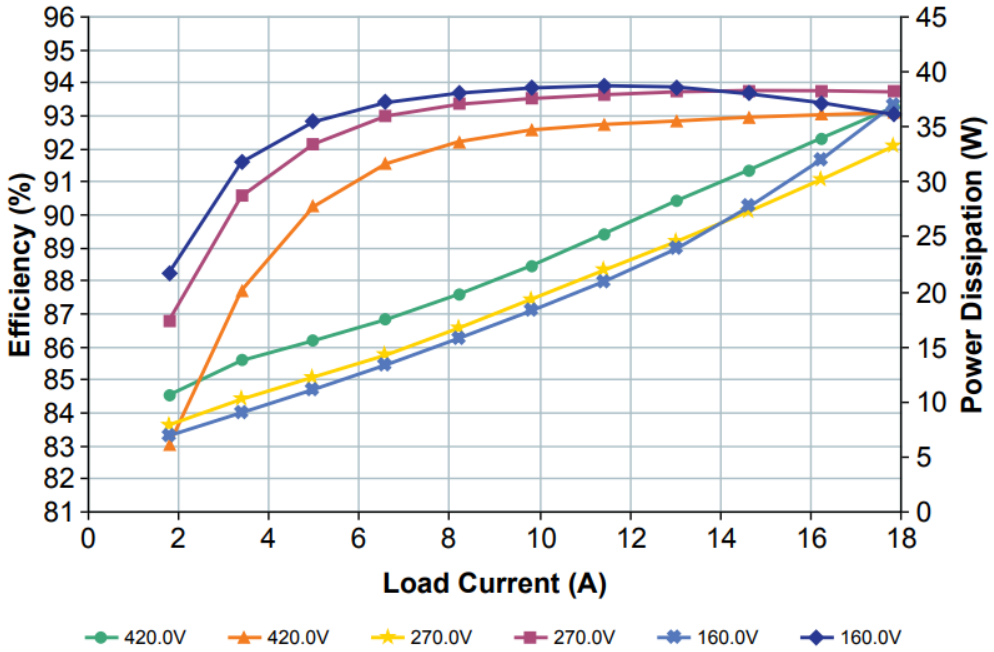


Figure 4.38: Vicor modules efficiency and power dissipation at a case temperature of 25 °C, as a function of output current.

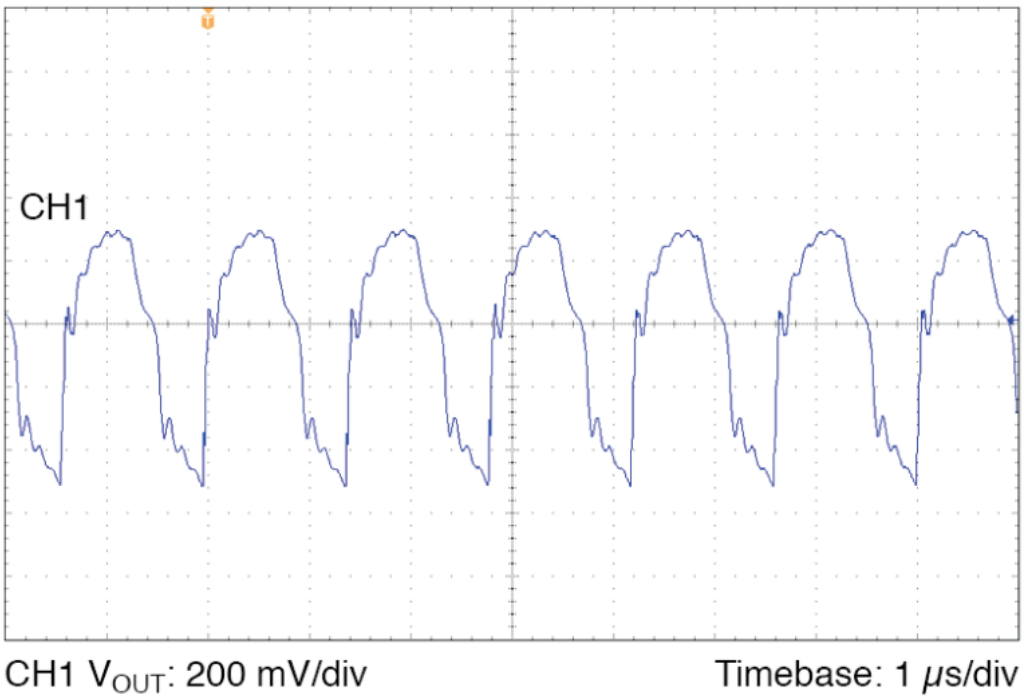


Figure 4.39: Vicor modules output voltage ripple at 500 W output power. Peak-to-peak ripple amplitude is measured at 800 mV.

5
Discussion

This chapter presents discussions about the test results from the PSFB converter and the Vicor measurements obtained in Chapter 4.

5.1 Performance

The converter as a whole and the thermal model reached some of the performance targets while others fell short, which is summarized in the following section.

5.1.1 Converter

The converter yielded some mixed results during the various tests performed on it. The most successful one was the full power test, which showed no apparent problems on the more crucial components such as the transformer and MOSFETs. The low input voltage and use of a fan for cooling does mean that true field environment was not possible to achieve, but the problems seemed to arise from areas which were not the main focus of this report, such as EMI and unstable control loop. Aspects which were seen as the main focus, such as the high frequency operation and implementation of the planar transformer, worked to a satisfactory degree.

5.1.2 TRM thermal model

The models generated in TRM generated accurate results after some tuning, most notably for the transformer winding PCBs. The difference between simulation and lab measurement for the secondary side winding came down to less than 2 °C, which for most power electronics use cases is enough accuracy. Combined with the simplicity and low skill requirements to use, the use of TRM can be an important tool for any power electronics engineer attempting to bring down board size.

5.2 Competitor comparison

The efficiency of the PSFB converter did not reach the same value as the Vicor module, but with some more work one could make ZVS and active rectification work which would bring up the efficiency by a couple of percentage points. Also, the PCB size ended up being larger than than the module but ideas to change this are presented further down in this chapter. In all cases of regulation, steady-state and transients, the competitor is performing better but not out of reach.

5.3 Future improvements

In order to reach and potentially surpass the goals set out at the start, a couple of improvements could be made to the current converted design.

5.3.1 Power level

One of the main goals of the project was to keep board area to a minimum. One of the main challenges with this goal is the large quantity of components needed to create a functioning PSFB converter, but also the size of some components such as the primary side MOSFETs due to the high voltage ratings. The easiest ways to increase the space efficiency would be to increase the desired power output from the current 500 W to instead 1 kW or even more. Only the transformer would requite a size increase and most active components would see a higher degree of utilization.

5.3.2 Layout

The current layout has some inherent flaws which can be dealt with in updated designs. Improvements such as a more clear divide between high and low voltage, shorter distances from gate drivers to MOSFETs, increased noise protection and fewer components make the converter more attractive and likely less error prone. A sketch of what such an layout could potentially look like can be seen in Figure 5.1, but here dimensioned for 1 kW as discussed previously.

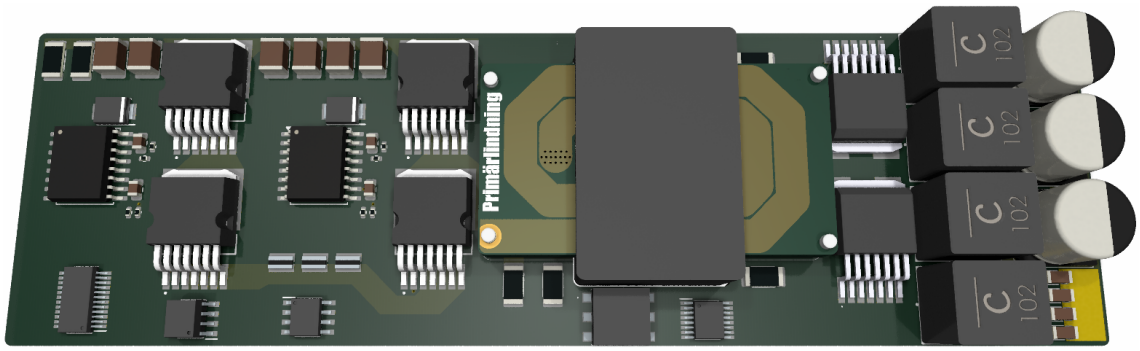


Figure 5.1: Sketch of improved layout with 1 kW output power and smaller size.

5.3.3 Transformer

Since the transformer largely worked as intended, there aren't any fundamental changes which would need to be done on it. However, even if the current power output is kept, the number of turns in the windings could be decreased in order to widen the traces and thus shift power loss from the windings to the core. The motivation for this change is the way the transformer would be cooled in a field environment: A cold plate mounted to the transformer core. Also, the way in which the insulation tape is mounted would need improvement in order to prevent the suspected partial discharges that could be heard at higher voltage levels.

6
Conclusion

Conclusions from the project and future work in presented in the following chapter.

6.1 Results from present work

The transformer design and dimensioning showed good results, being able to transmit over 500 W of power with a total volume of less than 4 cm^3. The thermals showed manageable temperatures in both windings and core. For a field-ready product, the number of turns would be decreased in order to shift losses from the copper to the core which would handle the majority of the transformer cooling via a cold plate.

The parasitic capacitance of the transformer ended up higher than expected at 40.9 pF, showcasing one of the challenges when using planar transformers. Said capacitance may have played a part in the large ringing on the secondary side of the transformer which had to be dealt with by the use of snubbers. These snubbers in turn ran the hottest at 99.5 °C during full power tests, thermally limiting the converter had active cooling with a fan not been used.

Lastly, partial discharges where suspected to occur in the transformer at higher voltage levels, likely caused by improperly applied insulation. The small size of the transformer comes with an inherent downside for manufacturability, which should be taken into account when considering the use of smaller, custom-made magnetics.

The converter delivered full output power and exhibited no fundamental issues whilst doing so. Problems with the control and compensation network prohibited the full output power from being transmitted while under active regulation, which in turn meant that limited input voltage had to be applied during tests. A maximum of 300 W could be output during regulation, which can be seen as a partial success.

The system efficiency ended up at 90 % during full load, below the ambition of 92.5 %. The discrepancy between these two values stem from a couple of factors: Lack of consistent zero voltage switching on the primary side, the use of body diode rectification and ringing which had to be dealt with by snubbers. Had these issues been dealt with, the efficiency would have risen by a few percentage points.

The attempt at higher frequency operation of the converter at 800 kHz was successful. Waveforms looked stable and the LTC3722 showed no difficulties keeping

up, assuming that the control issues were not caused by the high frequency. This increase enabled large reductions in component size such as the magnetics, with the transformer being a prime example. The output inductors could also be downsized, even though the ones chosen for the project ended up on the larger side. There is a clear potential for replacing the flat wire inductors with moulded inductors, bringing the size down further.

While the PCB size was kept low at 153.7 by 64.5 mm, the phase-shifted full-bridge topology is one with a high component count. Due to voltage ratings, MOSFETs required large packages which in turn brought up the total converter size. The 500 W power level is on the lower side of what is suitable for a PSFB converter due to these reasons. If the power level had been increased up to 1 kW or more, the power-to-size ratio would've greatly increased as only the magnetics need to be scaled up.

Use of the software TRM for thermal modelling showed good accuracy in predicting steady-state temperature of the transformer winding PCBs and the main PCB of the converter. As a design tool, TRM and other thermal modelling software can be important tools for dimensioning traces and other copper shapes on PCBs. Instead of finding out a certain part runs too hot once the prototype board shows up, the problem can be dealt with during the design phase, saving both time and money.

Lastly, the Vicor module which the project aims to replace was not outcompeted in terms of either size or efficiency. If the power level had been increased by a factor of two or more, that might change, especially with optimizations to the PSFB that have been proposed. Either way, a discrete in-house converter will always grant more design freedom and flexibility than an off-the-shelf product.

6.2 Future work

Further work should be put into solving the problems of the control loop to enable full operation of the converter. While the control loop is not of major interest in this case, the converter as a whole cannot be fully tested without functioning regulation.

A more thorough model of the transformer and especially the main PCB could be done using TRM in order to get a consistent temperature across all power carrying copper shapes, mainly to save on board space but also to keep maximum temperature as low as possible. Further work to validate the temperature on inner layers would be interesting but likely challenging to execute.

Continuing on the simulation trend, a magnetics model of the transformer would add understanding of the flux distribution which could potentially enable even further size reduction and optimization. The parasitic capacitance in particular would be advantageous to model in order to find the optimal spacing between transformer winding PCBs, without increasing the vertical footprint too much. The use of other laminates with different dielectric constant as compared to FR-4 could be explored in order to bring the capacitance down.

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A

Appendix 1

The complete schematic from KiCad can be seen in Figure A.1.

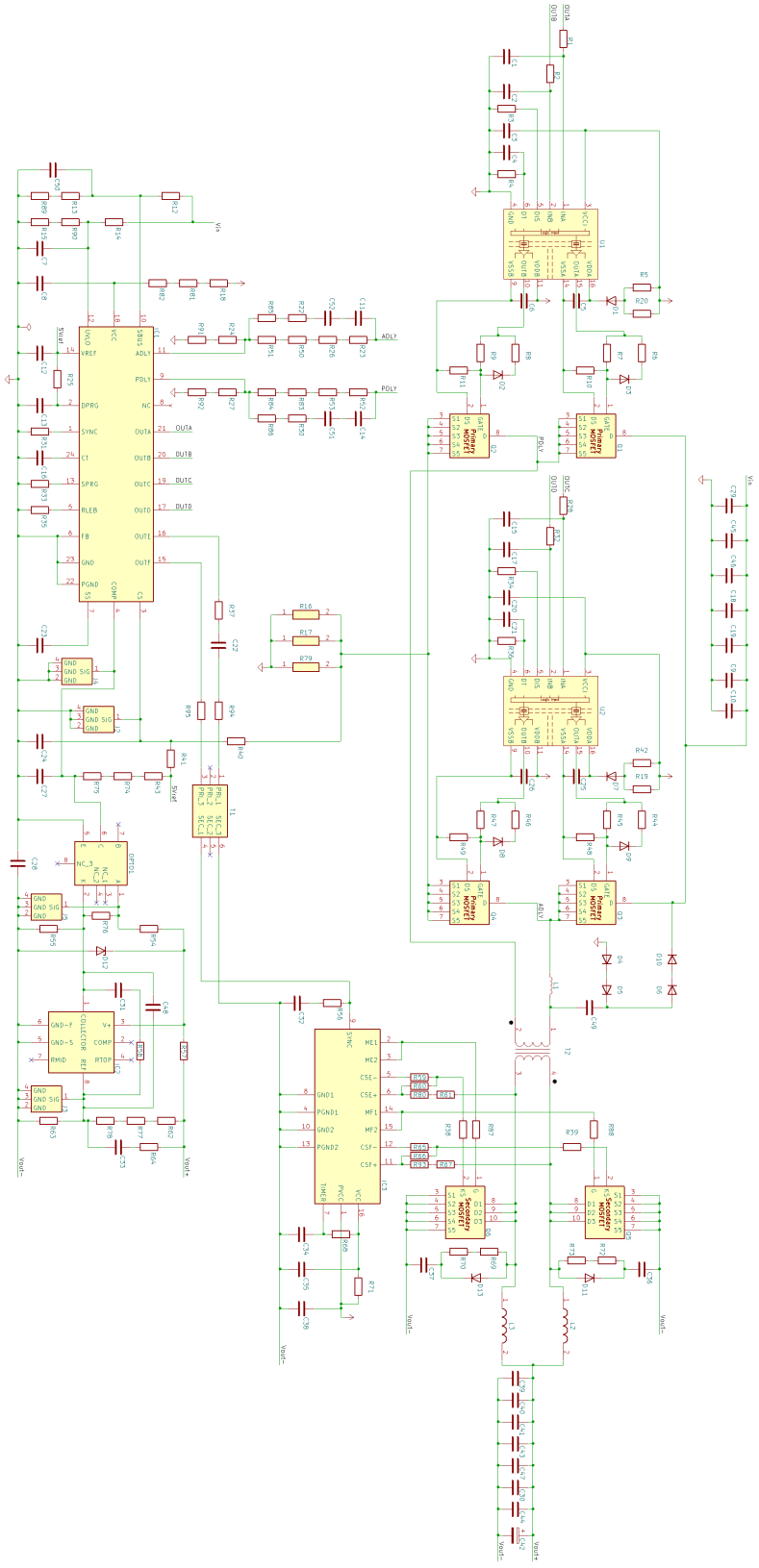

Figure A.1: The full converter schematic from KiCad.

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