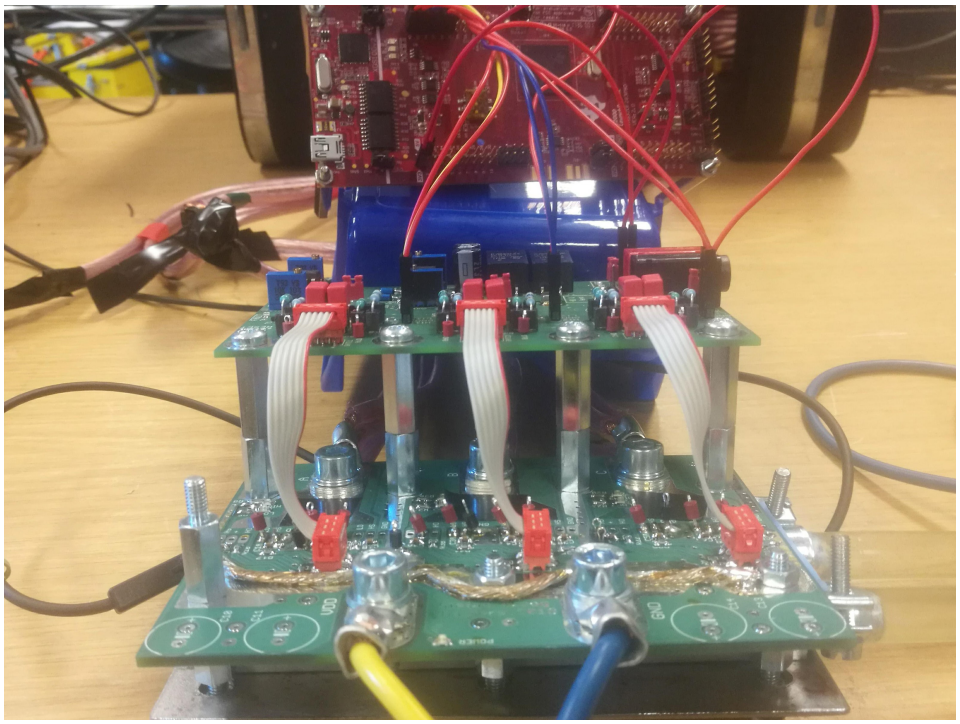
CHALMERS
UNIVERSITY OF TECHNOLOGY



Design, construction and evaluation of a distributed 48 V inverter for a mild hybrid vehicle

Master's thesis in Electric Power Engineering

Carl Tisell
Usman Tariq

Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2018

Master's thesis 2018

Design, construction and evaluation of a distributed 48 V inverter for a mild hybrid vehicle

Carl Tisell
Usman Tariq



CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
Gothenburg, Sweden 2018

Design, construction and evaluation of a distributed
48 V inverter for a mild hybrid vehicle
Carl Tisell & Usman Tariq

© Carl Tisell & Usman Tariq, 2018.

Supervisors:
Stefan Skoog, Chalmers University of Technology
Torbjörn Larsson, Volvo Cars Corporation
Alexander Robertsson, Volvo Cars Corporation

Examiner:
Torbjörn Thiringer, Chalmers University of Technology

Master's Thesis 2018
Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 (0)31-772 10 00

Gothenburg, Sweden 2018

Design, construction and evaluation of a distributed
48 V inverter for a mild hybrid vehicle
Carl Tisell & Usman Tariq
Department of Electrical Engineering
Chalmers University of Technology

Abstract

This thesis deal with the design, construction and evaluation of a prototype of an integrated inverter intended for integrated modular motor drive in a 48 V mild hybrid vehicle in order to reduce the overall volume of the inverter. The prototype is developed for a crankshaft integrated starter generator. Different semiconductor devices are evaluated theoretically with regards to performance, losses and thermal development. Moreover, different topologies for an integrated inverter are analyzed and PPB-II is selected as the platform to build the prototype of. Two prototypes are built, the first is a single phase half bridge which is used to verify and investigate different circuit designs. The second one is a three phase half bridge inverter which represents one module of eight integrated inverters. This second prototype is designed on a PCB and will have water cooling integrated. How to design and optimized a DC capacitor bank is studied. By implementing ceramic capacitors on the second prototype the size of the DC capacitor bank is reduced. Furthermore, an optimization program is used to present the optimal combination of capacitors with regards to cost, volume and losses. A switching frequency of 100 kHz is achieved.

Keywords: Integrated Modular Motor Drive, Crankshaft Integrated Starter Generator, Semiconductor, PPB-II, DC capacitor bank.

Acknowledgements

This thesis was carried out at the Unit of Electric Machine & Power Electronics, Electrical engineering, Chalmers University of Technology and has been supported by Volvo Cars Corporation.

We would like to express our deepest appreciation for those who helped us in completing this master's thesis report. Firstly a special recognition to our supervisor Stefan Skoog for helping us throughout this project. Despite his high work load and busy schedule he would always answer the questions we had and he invested a lot of his time and energy into making this project a success. Without his help this project would have been an arduous task. Secondly we also want to express our gratification towards Torbjörn Larsson, who was our supervisor from Volvo Cars, for his help with the report but also for his mentorship throughout the project as well as give a big thanks to Volvo Cars for sponsoring this project. Thirdly, we would like to express our humble appreciation towards our examiner Torbjörn Thiringer for guiding us in writing the report. Lastly, a sincere thanks to Robert Karlsson for taking the time to aid us in the lab, offering design solutions and answering questions regarding our inverter.

Furthermore, we would also like to extend a special thanks to Daniel Pehrman for his knowledge with the microcontroller and helping us understand and code it. Another recognition and person we would like to thank is our classmate Charlie Jägerhag for helping us implement the code in GAMS when optimizing the DC capacitor bank. Lastly, we would like to extend a thank you to David Runesson from Volvo Cars for extending his knowledge on power electronics.

I, Carl, want to extend my deepest appreciation for my father who has always supported me throughout my life and encouraged me to be the best I can. Without this source of strength in my life I would not be where I am today.

I, Usman, would like to praise my family and special gratitude for my uncle for the continuous love and encouragement throughout my life, without your support it would have been difficult, your love means everything.

Carl Tisell & Usman Tariq, Gothenburg, June 2018

Contents

List of Figures **viii**

1 Introduction **1**
1.1 Background . . . 1
1.2 Integrated Modular Motor Drives concept . . . 1
1.3 Previous work . . . 2
1.4 Aim . . . 2
1.5 Scope . . . 3
1.6 Task formulation . . . 4
1.6.1 Type of inverter . . . 4
1.6.2 Wide-bandgap technology versus silicon switches . . . 4
1.6.3 Design Of Inverter . . . 5
1.6.4 Design Of Cooling Circuit . . . 5
1.6.5 Drive circuit . . . 5
1.6.6 Construction . . . 5
1.6.7 DC-link capacitor . . . 6
1.6.8 Evaluation . . . 6
1.6.9 Environmental assessment . . . 6

2 Theory **7**
2.1 Integrated modular motor drives . . . 7
2.1.1 Fractional-slot concentrated winding machine . . . 7
2.1.2 Inverter topologies . . . 8
2.1.2.1 Conventional two-level three phase converter . . . 8
2.1.2.2 Stacked polyphase bridges converter . . . 8
2.1.2.3 Parallel-connected polyphase bridges converter . . . 9
2.1.2.4 Modular high frequency converter . . . 10
2.2 Transistor losses calculation . . . 11
2.3 Theoretical calculation of steady-state temperature of switches . . . 16
2.4 Slew rate control of Transistors . . . 17
2.5 DC Capacitor Bank design . . . 19

3 Case setup **23**
3.1 Machine Parameters . . . 23
3.1.1 Choice of inverter topology . . . 23
3.2 Design aspects of prototypes . . . 24

3.3 Work approach . . . 24
3.4 Comparison of semiconducting switches . . . 26
3.5 OrCad and PSpice simulation . . . 26
3.6 GAMS Optimization of DC capacitor bank . . . 29
3.7 Construction of inverter . . . 29
3.7.1 Prototype 1 . . . 29
3.7.2 Prototype 2 . . . 30
3.8 Measurements . . . 33
3.8.1 Prototype 1 . . . 33
3.8.2 Prototype 2 . . . 33

4 Results **35**
4.1 Results from Prototype 1 . . . 35
4.1.1 Performance and losses . . . 35
4.2 Results from Prototype 2 . . . 44
4.2.1 Optimization of DC capacitor bank . . . 44
4.2.2 Performance and losses . . . 47
4.2.3 Efficiency of Prototype 2 . . . 58
4.2.4 Thermal development and evaluation of liquid cooling . . . 61

5 Conclusion **63**
5.1 Inverter . . . 63
5.2 Environmental aspect . . . 63
5.3 Future work and recommendations . . . 64
5.3.1 Wide-bandgap technology . . . 64
5.3.2 Interleaving switching . . . 65
5.3.3 DC capacitor bank . . . 65

A Appendix 1 **I**

List of Figures

1.1 Concept figure of an IMMD illustrating how power electronics will be mounted on an EM. 2
1.2 Explanatory figure of the scope of the whole thesis excluding battery and electric motor which are substituted by a dummy load and a power supply. 3
1.3 Overview of a mild hybrid drive system in P2 configuration. 4
1.4 Schematic of dc-link circuit. 6

2.1 Illustrative figure of an FSCW and its windings. 7
2.2 Schematic of conventional two-level three phase converter, where L and R are parisitic inductance and resistance respectively. 8
2.3 Schematic of stacked polyphase bridge converter, where L and R are parasitic inductance and resistance respectively. 9
2.4 Schematic of Parallel Polyphase Bridges-I converter, where L and R is the parisitic inductance and resistance respectively. 10
2.5 Schematic of Parallel Polyphase Bridges-II converter, where L and R are parisitic inductance and resistance respectively. 10
2.6 Schematic of moudular high frequency converter, where L and R are parisitic inductance and resistance respectively. 11
2.7 Descriptive figure of the switching waveforms for an inverter. 12
2.8 Current path during four quadrant operation when the load is inductive. 13
2.9 Schematic of the n-channel MOSFET. 15
2.10 A resistive thermal network of the MOSFET and cooling plate. . . . 16
2.11 Diagram of MOSFET gate turn-on in case of fast gate turn-on and slow gate turn-on. 18
2.12 Schematic of the slew rate RCD circuit connecting to the gate of the MOSFET. 19
2.13 Illustrative schematic of how to model the capacitor currents. 22

3.1 Preliminary sketch of how the inverter will be set up for measurements. 25
3.2 OrCad design of the first prototype for simulation in PSpice. 28
3.3 1^{st} prototype setup. 30
3.4 Second prototype setup. 31
3.5 Overview of the 2^{nd} prototype. 32

4.1 Comparison of the lower transistor's switching waveforms in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 100 kHz switching frequency. 36
4.2 Zoom in on signal from gate driver and V_{gs} voltage to the the lower transistor's in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 100 kHz switching frequency. Measurements are taken from prototype 1B with the load of 440 μH and 440 $m\Omega$. 36
4.3 Load current and voltage during fast and slow gate turn-on at 100 kHz switching frequency. 37
4.4 Load current and voltage during fast and slow gate turn-on at 55 kHz switching frequency. 38
4.5 Zoom in on the lower transistor's switching waveforms in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 55 kHz switching frequency. 39
4.6 Zoom in on the lower transistor's turn-on in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 55 kHz switching frequency. 39
4.7 Zoom in on the lower transistor's turn-off in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 55 kHz switching frequency. 40
4.8 Graph of V_{ds}, I_{ds}, the average power loss measured and the average power loss calculated for 55 kHz. 41
4.9 Graph of V_{ds}, I_{ds}, the average power loss measured and the average power loss calculated zoomed in. 42
4.10 Graph of filtered V_{ds}, I_{ds}, the average power loss measured and the average power loss calculated zoomed in. 42
4.11 Graph of filtered V_{ds}, I_{ds}, the average power loss measured and the average power loss calculated zoomed in at the peak of the current. . 43
4.12 Graph of the voltage over the upper and lower part of the DC capacitor and the current through the load and the lower DC capacitor for fast turn-on (upper) and slow turn-on (lower). 44
4.13 DC bank capacitor needed as a function of frequency (upper fig.) and DC bank capacitor needed as a function of power factor (lower fig.) at 100 kHz. 46
4.14 Load current and track of V_{ds} presented for each phase with a switching frequency of 100 kHz and a fundamental frequency of 100 Hz. . . 47
4.15 Load current and V_{ds} of phase A. 48
4.16 Zoom in of the load current and V_{ds} of phase A. 48
4.17 Input voltage and current from the power supply to inverter. 49
4.18 Switching characteristics of the lower transistor of phase A leg. V_{ds}, V_{gs} and gate driver signal present. 50
4.19 Zoom in on turn-on and turn-off of lower transistor with V_{ds}, V_{gs} and gate driver signal present. 51
4.20 Switching characteristics of the lower transistor of phase A leg with the slew rate circuit changed. V_{ds}, V_{gs} and gate driver signal present. 52

4.21 Zoom in on turn-on and turn-off of lower transistor with V_{ds}, V_{gs} and gate driver signal present when the slew rate has been adjusted. . . . 53
4.22 Switching characteristics of the lower transistor of phase A leg with the slew rate circuit changed and frequency lowered to 50 kHz. V_{ds}, V_{gs} and gate driver signal present. 54
4.23 Zoom in on turn-on and turn-off of lower transistor with V_{ds}, V_{gs} and gate driver signal present when the slew rate has been adjusted and switching frequency decreased. 55
4.24 All three phases load current and track of V_{ds} for 50 kHz switching frequency. 56
4.25 Input current and voltage at 50 kHz and adjusted slew rate. 57
4.26 Zoom in on turn-on of transistor with V_{ds}, V_{gs} and gate driver signal present when the turn-off resistor has been increased. 57
4.27 Instantaneous and average efficiency for the inverter. 58
4.28 Reactive power for each phase and the sum of the reactive output power. 59
4.29 Active power for each phase, the input power and the sum of the output power. 59
4.30 Apparent power for each phase and the sum of the apparent output power. 60
4.31 Two temperature readings with and without integrated water cooling. 62

1
Introduction

1.1 Background

In recent years the automotive industry has been moving with fast pace in a new direction of development: electricfication. The rapid increase of electrified passenger vehicles is a solution employed by car manufacturers to comply with more demanding CO_2 and emission requirements. One of the many approaches in this electrified revolution is the mild hybrid. A mild hybrid electric propulsion system is, in this scope, a mid way between conventional combustion engine and pure electrification strategy which is based on 48 V that has the potential to suit most car models and offer many important benefits from full hybrids. Typically, this type of hybrid system consists of an Electric Machine (EM) compactly integrated with a traditional Internal Combustion Engine (ICE), gearbox and motor controller with power electronics. With an efficient battery system, this mild hybrid setup has the possibility to increase the total efficiency by utilizing the EM in combination with the ICE for coasting, recuperation of energy and torque assist. Furthermore, using the 48 V system comes with many other benefits, first and foremost, the vehicle's electrical system will be able to handle a higher power rating and thereby more electric functions can be installed. Among these are electric air conditioning, pumps, 48 V generator and accumulator which may contribute to a cost reduction of the car [1]. Additionally, infotainment and autonoumous drive which is currently being developed for the near future will benefit from 48 V system.

In order to deliver a cost efficient, well performing mild hybrid, one thing that can prove to be crucial for achieving this is to implement power electronics and EM tightly integrated. With the major advancements made in semiconducting devices allowing for smaller and more efficient power electronic devices, this mild hybrid system has become viable and attractive from a manufacturer's point of view with regartds to costs and profit. The EMs that are subject for being integrated with the inverter are in the power size of $20 - 35$ kW peak power.

1.2 Integrated Modular Motor Drives concept

The Integrated Modular Motor Drive (IMMD) concept utilizes the design of certain machines where the phase windings can be seperated into several segments, e.g. a Fractional-Slot Concentrated Winding (FSCW) machine or tooth-wound machines [2]. This allows for the possiblility to mount smaller modules of the inverter directly

onto the machine's stator, close to the phase windings. The advantage of using a modular inverter over the conventional one is that manufacturers are able to eliminate long cables and big connectors between the EM and inverter and now have the possibility to integrate the cooling of the machine with the inverter.

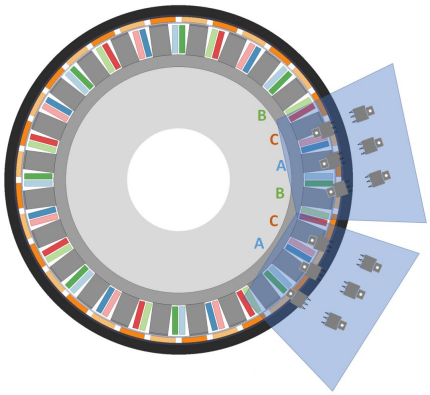


Figure 1.1: Concept figure of an IMMD illustrating how power electronics will be mounted on an EM.

1.3 Previous work

There are various publications available on the topic of IMMDs about the different topologies that can be used in automotive industry. In [2], [3], [4] a concept where conventional three-phase inverter can be replaced with several modularized drives where each drive unit is comprised of a DC-bank unit, control circuitry and power electronics along with integrated cooling.

Experiences from other similar projects within our research divisions show that a satisfactory cooling system is needed in order to control the temperature and achieve better operation of the MOSFETs. The design of a proper and optimized DC-link capacitor bank was crucial in most of the readings for a good end result. Because of unoptimzed DC-link bank, capcitors reached very high temperatures during normal operation in these projects [5], [6]. To conclude, these missteps were realized in the start of our project and necessary actions were made during the thesis to avoid the same design flaws.

1.4 Aim

The aim of this master thesis is to design and construct a distributed inverter prototype with integrated cooling as well as to provide a power switch design for a full 3-phase inverter for a FSCW machine. The work will first be based on calculations of expected performance of key elements and later on compared with measured results once the prototype is built. The result of the project will be evaluated from a technical point of view including lab measurements. There will also be a financial and enviromental analysis of the result.

1.5 Scope

The project will include theoretical modeling of a prototype 3-phase 48 V inverter, together with design and experimental validation of a full-power prototype with commercially available high-performance components. For comparison and learning, a half-bridge inverter will be developed and then further developments will be made based of this design until a module of an integrated three phase inverter is achieved. The final inverter will then be compared with the initial inverter. The design of the inverter will be made with respect to thermal capabilities, efficiency, size, cost and output power ratings.

Since, the inverter will be part of a hybrid car, the ambient temperature is higher due to compact space and other heat generating devices in such a close proximity, therefore the control of the inverter's temperture is critical for continuous operation hence there is a need for a well performing cooling system. Moreover, the close space will impose geometrical constraints which will limit the design. The project will not focus on closed loop current control. Moreover, a detailed analysis on the cooling system, such as cooling plate material, coolant type, flow path of the liquid, optimal dimensioning of cooling plate, liquid pressure etc. will not be performed due to the complexitity and not being a subject of electrical power engineering.

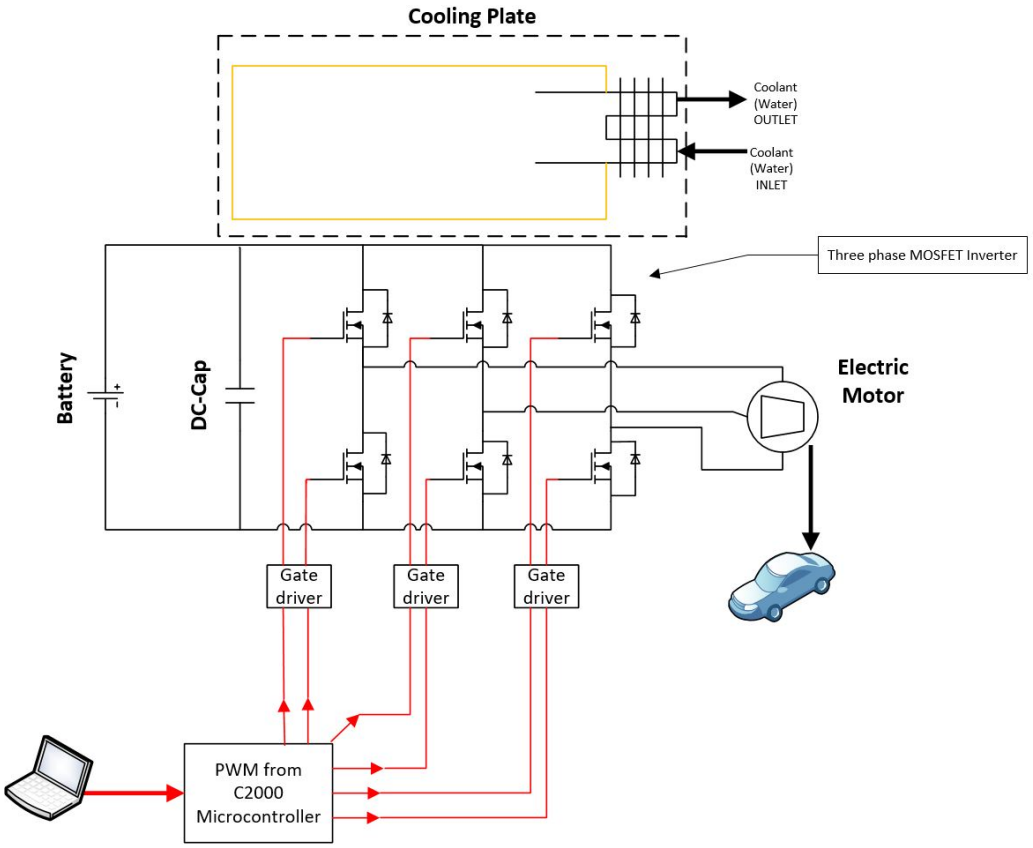


Figure 1.2: Explanatory figure of the scope of the whole thesis excluding battery and electric motor which are substituted by a dummy load and a power supply.

1.6 Task formulation

The goal of this thesis is to design, construct and evaluate a distributed 48 V inverter for a mild hybrid vehicle. Therefore, to execute this project optimally, it is necessary to define the details of the many challenges that lies between the start and finished product. Fig 1.3 gives an overview of the mild hybrid vehicle drivetrain in P2 configuration and main features are presented in blocks.

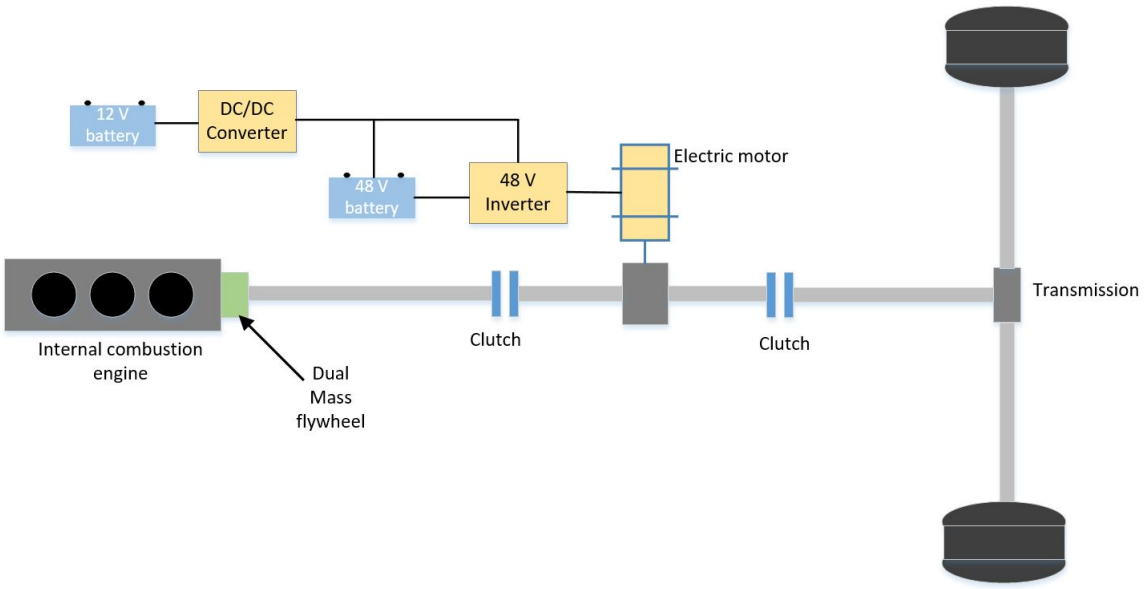


Figure 1.3: Overview of a mild hybrid drive system in P2 configuration.

1.6.1 Type of inverter

The first important decision to make is to decide which type of inverter that will be designed, which dictatates the placement of the inverter on the machine. This is crucial since it gives the project different limitations and restrictions later on when designing the inverter. Additionally, there is data supporting that this choice has a significant impact on performance, CO_2-limitations and cost of the vehicle [7].

1.6.2 Wide-bandgap technology versus silicon switches

First and foremost, given the two to ten second RMS peak output power of 30 kW that the inverter is required to provide for a small duration of time, a selection of semiconductor switches has to be made with respect to performance and cost. When making this choice an interesting technology that has recently become more economically viable for this type of application is wide-bandgap semiconductors. More specifically Silicon Carbide (SiC) and Gallium Nitride (GaN), which are of most interest based on research [8]. However, these technologies compete with high performance Silicon (Si) switches and a comparsion between different transistors of

both kinds has to be made in order to find the optimal candidate. The parameters that will be compared in regards to the switches will be cost, on-state losses, switching losses, maximum frequency operation and robustness.

1.6.3 Design Of Inverter

For the initial design of the inverter, simulations will make out the base to build the first prototype of. The things that needs to be simulated is the base inverter, i.e. number of switches, phase legs and DC-capacitor, and the necessary components needed to perform open-loop operation, which includes drive circuit, externally set PWM, snubbers and filters. The parameters that are of importance are currents and voltages as well as switching frequency, harmonics and efficiency. Additionally, in the designing of the inverter, implementing protection for overvoltages and overcurrents is important to maintain the safety of the inverter to prevent the vehicle from malfunctioning. Another significant part of the design phase includes reducing losses, transients, harmonics and such which is traditionally done with in-/output filters and snubbers. However, in the scope of this thesis a gate drive slew rate control approach will be evaluated instead.

1.6.4 Design Of Cooling Circuit

Cooling the inverter will also need to be resolved. This is bound to be done by using the same liquid coolant that is used to cool the rest of the vehicle's propulsion system. To be able to cool the inverter optimally, the heat development from the inverter is calculated. This includes four different kinds of losses that can be considered to be the key losses: MOSFET conduction losses, MOSFET switching losses, change in switching losses from increased slew rate and DC capacitor bank losses.

1.6.5 Drive circuit

For the switching of MOSFET based gate drive circuit for the inverter, a switching pattern for at least one of the phases is to be implemented and tested to ensure that it can operate as intended. Some important requirements should be kept in mind when designing the drive circuit which includes: ensuring no simultaneous conduction between high and low-side switches, low cost, small size and low amount of external passive components [9]. Another important design aspect to consider is if fast or slow turn-on of the gate is to be implemented, which will affect the number of components included in the gate driver, transients as well as the efficiency of the switching.

1.6.6 Construction

A first prototype is constructed and its performance evaluated. This part of the project requires a lot of time in the lab and also innovative and creative solutions in order to realize the inverter. After construction, important characteristics and traits that needs to be evaluated includes, but is not limited to; losses, switching

frequency, thermal capabilites, transients, effect of parasitic inductances and harmonics. During this project two prototypes will be constructed and different design aspects of these inverters will be considered which are further elaborated in section 3.2.

1.6.7 DC-link capacitor

The selection of an appropriate DC-link capacitor for the inverter is essential. The key features that should be considered when designing includes high ripple current capability, high temperature robustness, total volume, low series inductances and resistances as well as low power loss [10]. The size selection for the DC-link capacitor should suit the design of the inverter and be geometrically fitting.

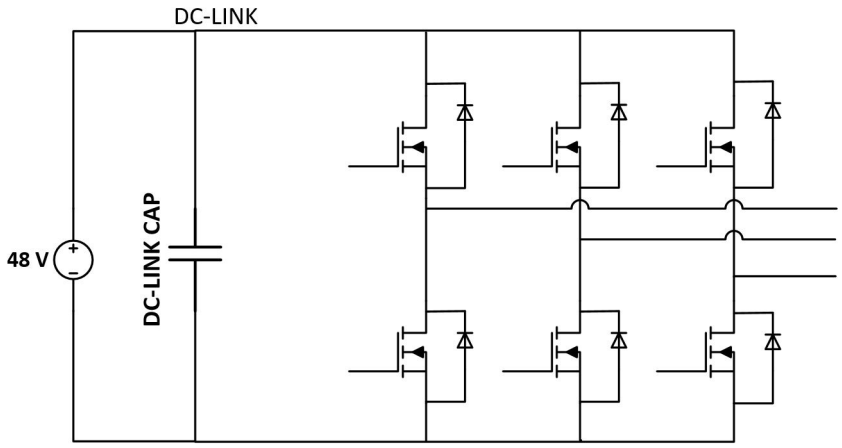


Figure 1.4: Schematic of dc-link circuit.

1.6.8 Evaluation

Once the inverter is finalized and all the necessary measurements have been taken, a concluding evaluation of the inverter as a whole will be made. This will include the losses and performance of the inverter with regards to the theoretical calculations that the design was based on. A cost analysis will be made to determine how favorable it would be for mass production.

1.6.9 Environmental assessment

One of the underlying reasons for the sudden shift towards electric vehicles is sprung from the need to reduce the environmental impact that traditional combustion engine vehicles have. Therefore, an assessment on how this distributed inverter will improve the already existing hybrid vehicles with regards to being environmentally friendly will be made.

2

Theory

2.1 Integrated modular motor drives

The IMMD provides the opportunity to integrate the drive power electronics as well as cooling onto the electrical machine in the form of several smaller modules. Each module is an inverter for either one or three phases, these are enclosed with the windings of the machine, which can be realized through different inverter topology. This approach allows for the benefit of reducing the cable size, electromagnetic interference (EMI) and cost.

2.1.1 Fractional-slot concentrated winding machine

The design of an FSCW machine has the stator windings divided into several sections that are relatively independent of each other, which makes it possible to connect the inverter modules and realize the IMMD concept [2]. In fig, 2.1 one can see how the different phases are structured B, C, A, B, C, A which allows for either single or three phases inverter modules to connect and be tightly integrated since the windings are not overlapping.

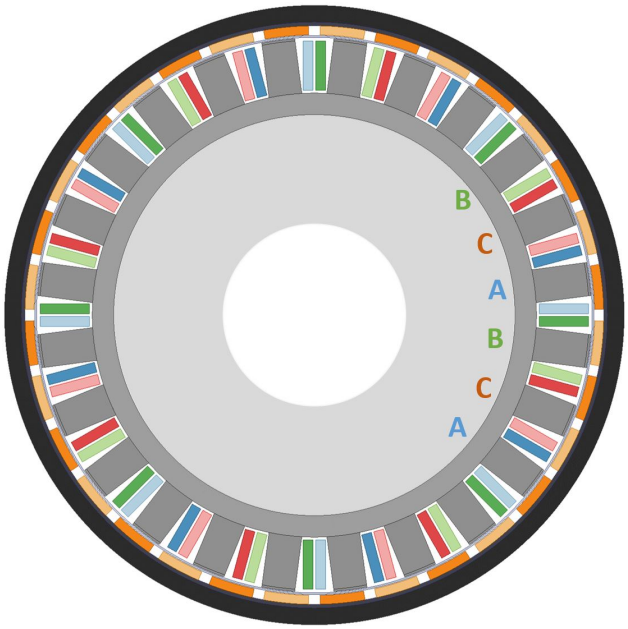


Figure 2.1: Illustrative figure of an FSCW and its windings.

2.1.2 Inverter topologies

2.1.2.1 Conventional two-level three phase converter

In fig. 2.2 the principal schematic of a two-level three phase converter is shown. This type of converter is usually used in the Electric Vehicles (EV) powertrain for transforming the current between DC and AC between the battery and EM. The converter consists generally of a power supply, which would be the battery in automotive applications, a DC-link capacitor and two transistors with antiparallel diodes for each phase leg. This device allows the battery to supply the EM with three phase voltages where frequency and amplitude can be varied using control of the transistors [2].

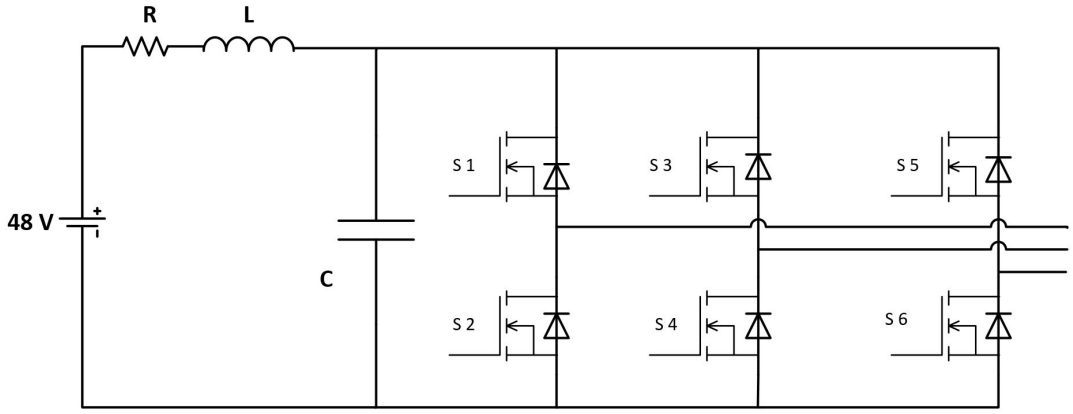


Figure 2.2: Schematic of conventional two-level three phase converter, where L and R are parisitic inductance and resistance respectively.

2.1.2.2 Stacked polyphase bridges converter

One type of converter topology is the Stacked Polyphase Bridges (SPB) converter which consists of several modules connected in series, which can be seen in fig. 2.3. One module consists of a two-level three phase converter of lower rating than that of a conventional two-level converter for this application. An advantage with this design is that due to the series connection, of the modules, the voltage rating for each module is lower than the one previous although DC voltage control is required [2].

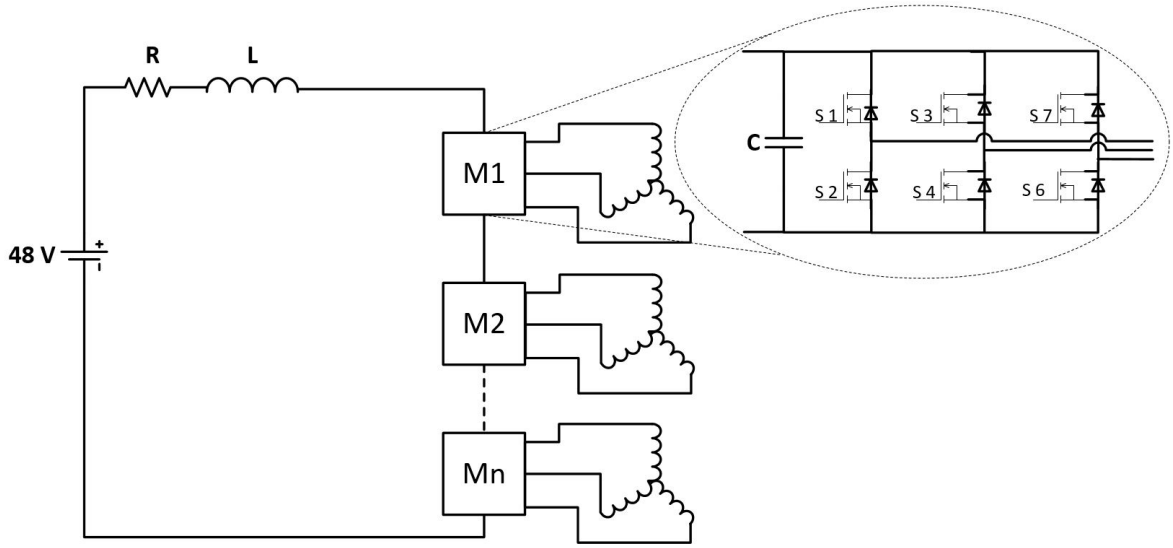


Figure 2.3: Schematic of stacked polyphase bridge converter, where L and R are parasitic inductance and resistance respectively.

2.1.2.3 Parallel-connected polyphase bridges converter

There are two different kinds of Parallel-Connected Polyphase Bridges (PPB) converter, PPB-I and PPB-II, which the schematics can be seen below in figures 2.4 and 2.5. The difference in design between the two topologies is that PPB-I is a traditional multiphase inverter. For PPB-I each phase leg can be constructed as a single module with its power electronics inside. This then connects in parallel to the common DC-link and the output goes to one of the coils of the EM. Compared with the conventional and SPB converter this design lowers the current rating of each switch significantly. The design also allows for reducing torque ripple by increasing the number of phases as well as it can introduce post-fault operation with proper control [2].

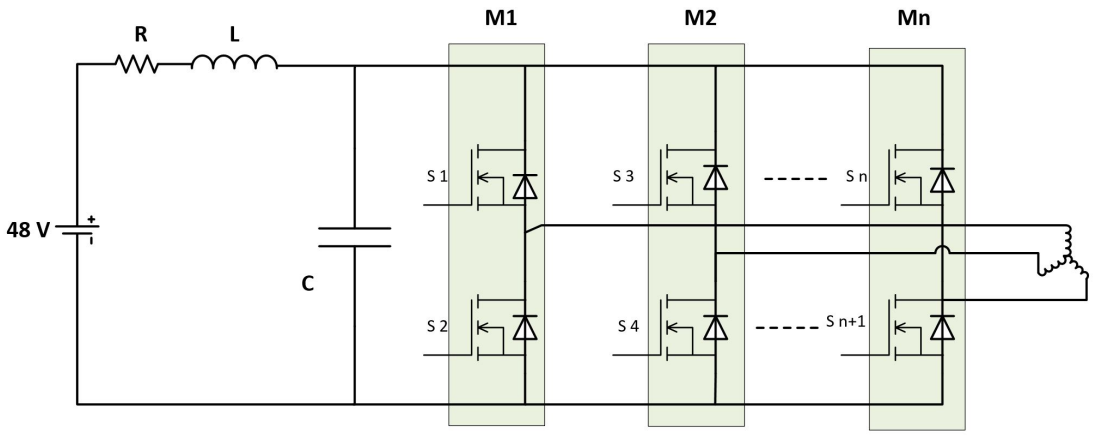


Figure 2.4: Schematic of Parallel Polyphase Bridges-I converter, where L and R is the parisitic inductance and resistance respectively.

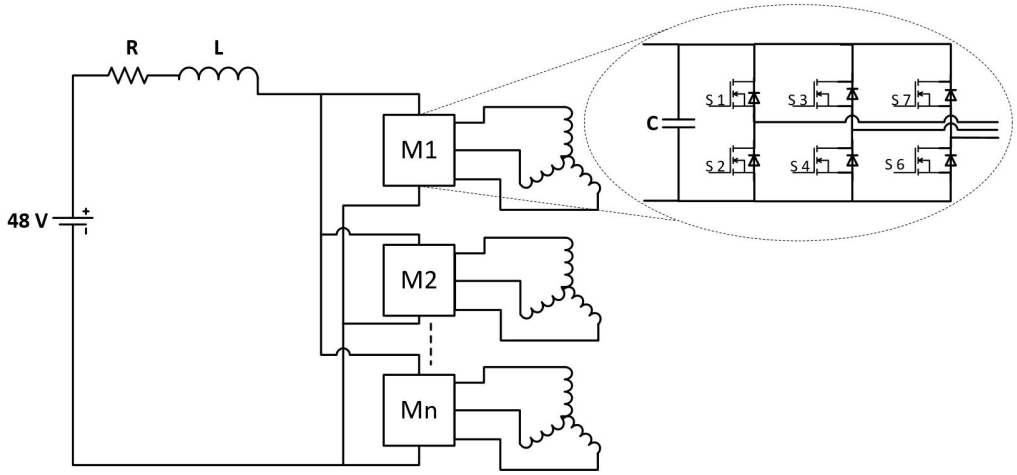


Figure 2.5: Schematic of Parallel Polyphase Bridges-II converter, where L and R are parisitic inductance and resistance respectively.

PPB-II's modules are consisting of two-level three phase converters connected in parallel. For instance, an EM with 24 windings would have 8 modules in total connected in parallel. Similar to PPB-I, this design also lowers the power rating of the switches [2].

2.1.2.4 Modular high frequency converter

Another type of converter topology of interest is the Modular High Frequency (MHF) converter. This converter's modules are constructed by a step-up converter in combination with an H-bridge. Both of these are connected to a DC capacitor. Like the previously mentioned topologies, the MHF converter also allows for the use of switches with lower rating than the conventional one. A schematic of the MHF converter is presented below in fig. 2.6.

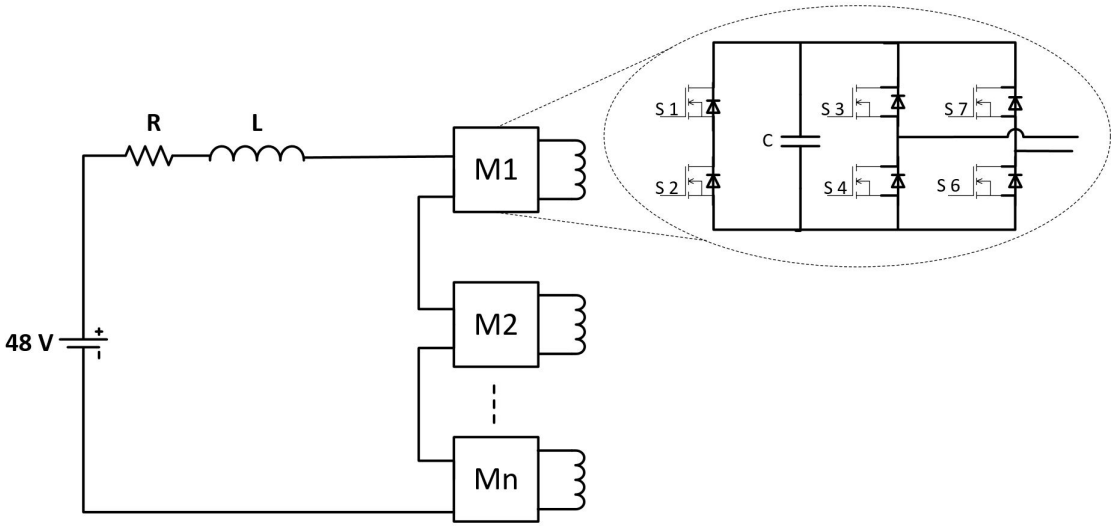


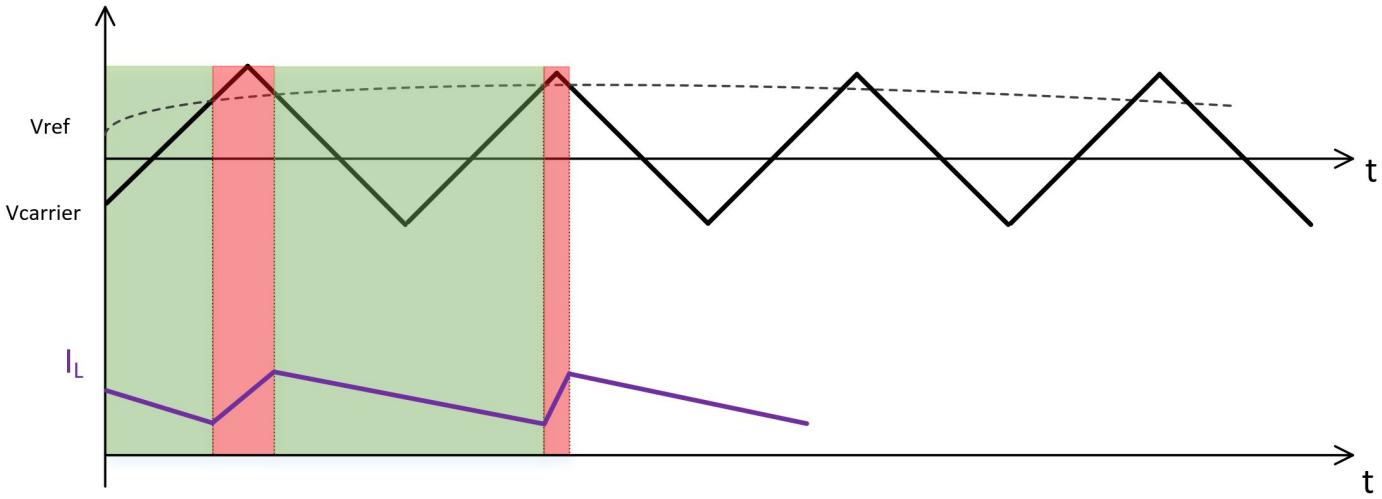
Figure 2.6: Schematic of moudular high frequency converter, where L and R are parisitic inductance and resistance respectively.

2.2 Transistor losses calculation

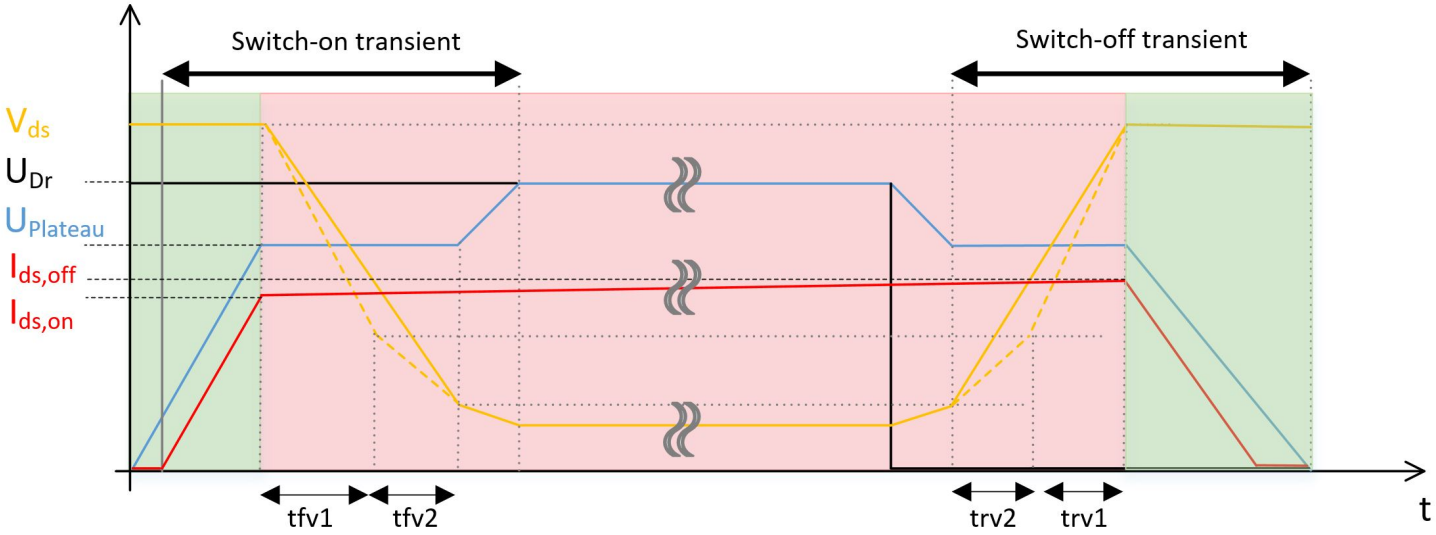
The inverter is operated in four different quadrant operations. The conduction losses through the anti-parallel diode can be elaborated through table 2.1 and figure 2.8

Table 2.1: Four quadrant operation for the inverter

4 quadrant operation				
No.	**Load V**	**Load I**	**Conduction**	**Sub-figure reference**
$\mathbf{1}^{st}$	> 0	> 0	TA	(a)
$\mathbf{2}^{nd}$	> 0	< 0	DA,TA	(b)(e)
$\mathbf{3}^{rd}$	< 0	> 0	DB,TB	(c)(f)
$\mathbf{4}^{th}$	< 0	< 0	TB	(d)

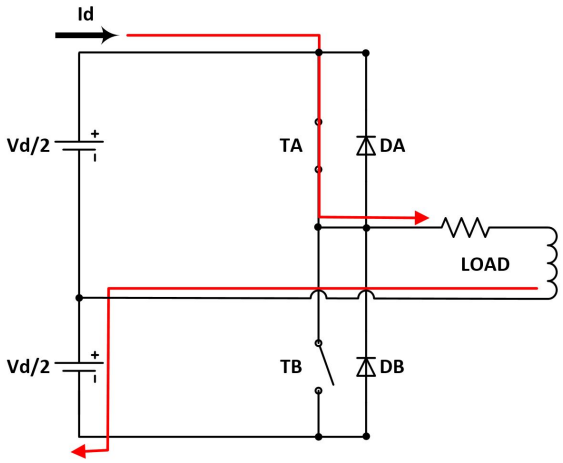


(a) Illustrative figure of how the switching patter is generated with the reference wave, carrier wave and load current.

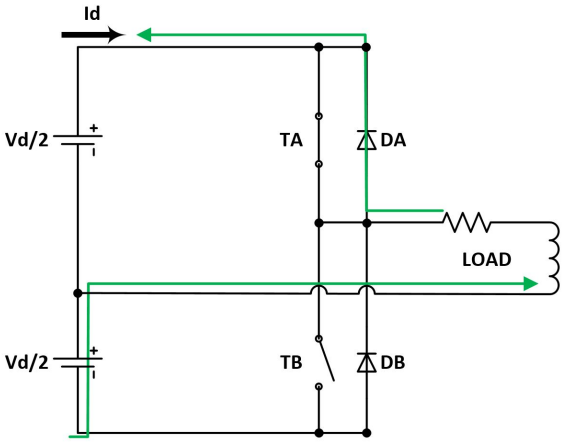


(b) Zoomed in view of the switching characteristics of the turn-on and turn-off, showing the drain-to-source voltage V_{ds}, gate-to-source voltage V_{gs}, gate drive signal U_{Dr} and the drain-to-source current I_{ds}.

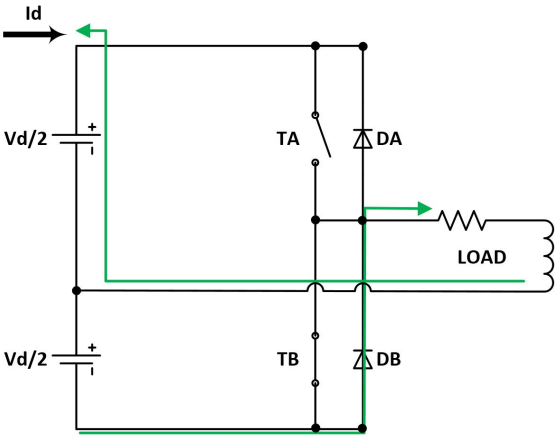
Figure 2.7: Descriptive figure of the switching waveforms for an inverter.



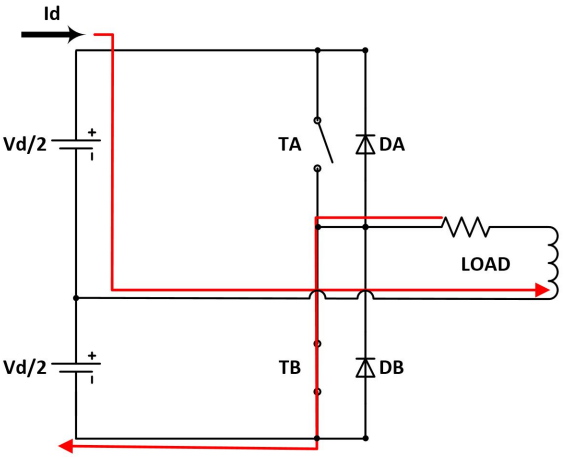
(a) Load voltage and current is positive



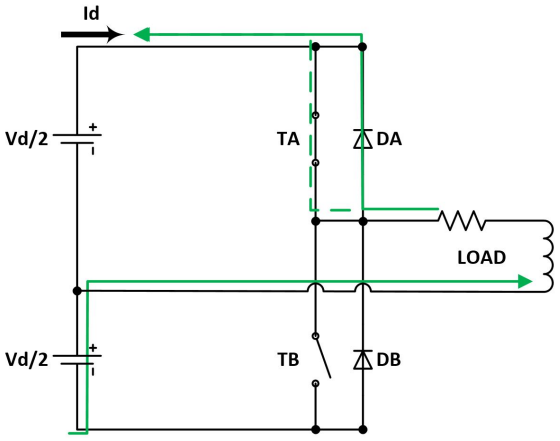
(b) Load voltage is positive and current is negative



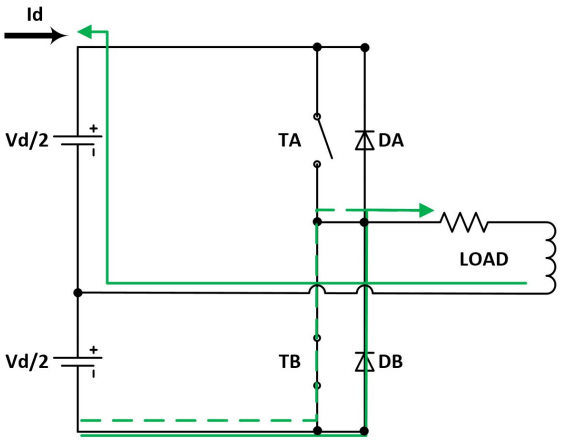
(c) Load voltage is negative and current is positive



(d) Load voltage and current is negative



(e) Current path when both diode and main channel conducting with negative current



(f) Current path when both diode and main channel conducting with positive current.

Figure 2.8: Current path during four quadrant operation when the load is inductive.

Where I_L is the load current. Fig. 2.7 illustrates the switching modes over one cycle of PWM. In addition, switching modes along with the direction of current is illustrated in fig 2.8, where $TB-$, $TB+$ are MOSFETS and $DA-$, $DA+$ are anti-parallel diodes. The anti-parallel diodes can only conduct when the inverter is operating in 2^{nd} and 3^{rd} quadrant and the MOSFETS are in the blocking state. MOSFETs and the diode can be in the conducting state at the same instant therefore, deadtime is implemented. The main channel of the MOSFET is conducting for longer durations of time. Most of the current is flowing through the MOSFET's main channel and not from the anti-parallel diode, which makes conduction losses very low, in many cases negligible.

The theoretical losses of a MOSFET can be split into conduction and switching losses, where conduction losses of the MOSFET can be describe with

$$P_{cond,M} = R_{ds,on} I_{ds,rms}^2 \tag{2.1}$$

where $R_{ds,on}$ is the on-state resistance of the transistor and $I_{ds,rms}$ is the RMS current through drain to source during conduction of one switching period [11].

The switching losses are more complicated and can be calculated with the following equations, one for the MOSFET's switching losses and one for the anti-parallel diode

$$P_{sw,M} = (E_{on,M} + E_{off,M}) f_{sw} \tag{2.2}$$

$$P_{sw,D} = (E_{on,D} + E_{off,D}) f_{sw} \approx E_{on,D} f_{sw} \tag{2.3}$$

where $E_{on,M}$ is the MOSFET turn-on energy, $E_{off,M}$ is the MOSFET turn-off energy and $E_{on,D}$ is the diode turn-on energy. The $E_{off,D}$ can be negelected from (2.3) due to that the majority of this loss is due to reverse recovery in the diode and it is shown later in this section that this is included in the turn-on energy of the complementary MOSFET. The turn-on and turn-off energy of the MOSFET can be written as

$$E_{on} = V_{ds} I_{ds,on} \frac{t_{ri} + t_{fv}}{2} + Q_{rr} V_{ds} \tag{2.4}$$

$$E_{off,M} = V_{ds} I_{ds,off} \frac{t_{fi} + t_{rv}}{2} \tag{2.5}$$

where V_{ds} is the blocking voltage of 48 V from the battery, $I_{ds,on}$ and $I_{ds,off}$ are approximated to be the current flowing through one switch when it is on. According to [11], these currents can differ a bit but they were assumed to be the same for our application, hence $I_{ds,off} = I_{ds,on}$. Q_{rr} is the charge resulting from the reverse recovery current from the diode. t_{ri}, t_{fi}, t_{rv} and t_{fv} is the rise and fall times for the current and voltage respectively. The current's switching times are given in the data sheet of each transistor while for the voltage rise and fall time, it is calculated according to [11] with the following equation

$$t_{fv} = \frac{t_{fv1} + t_{fv2}}{2} \tag{2.6}$$

where

$$t_{fv1} = (V_{ds} - R_{ds,on} I_{ds,on}) R_g \frac{C_{gd1}}{(U_{Dr} - U_{plateau})} \tag{2.7}$$

$$t_{fv2} = (V_{ds} - R_{ds,on} I_{ds,on}) R_g \frac{C_{gd2}}{(U_{Dr} - U_{plateau})} \tag{2.8}$$

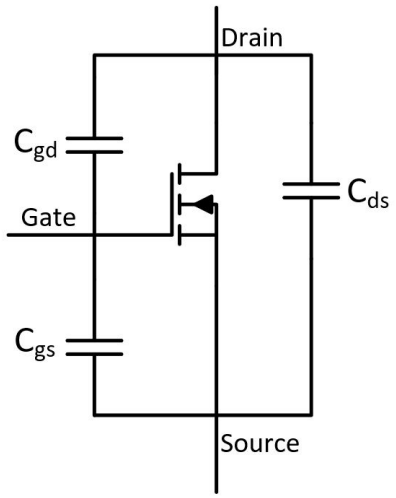


Figure 2.9: Schematic of the n-channel MOSFET.

where U_{Dr} is the voltage of the gate signal of 10 V, C_{gd1} and C_{gd2} is the gate-drain capacitance for the blocking voltage of 48 V and the on-state voltage drop of $R_{ds,on} I_{ds,on}$ respectively, how to acquire these values is elaborated more on in [11] and how C_{gd} is located in the MOSFET structure and is visible in fig. 2.9. R_g is the gate resistance and $U_{plateau}$ is the clamped voltage level when the Miller effect takes place. For some transistors, this parameter is given in its datasheet but for others it has to be calculated according to [12]. Equation (2.6), which gives t_{fv}, is a two-point approximation due to the complex dependency of the non-linear gate-drain capacitance during turn-on, as well as for turn-off shown later. This calculation combined with the fact that the drain-source voltage is assumed to have linear form, gives that this is a worst-case analysis for the switching losses calculation [11].

The $E_{on,D}$ is the diode turn-on energy and can be calculated as

$$E_{on,D} = \frac{1}{4} Q_{rr} U_{D,rr} \tag{2.9}$$

where $U_{D,rr}$ is the voltage across the anti-parallel diode during reverse recovery, it can be approximated to be equal to the supply voltage of V_{ds} for worst case scenario [11].

Voltage rise time is calculated from the following equation,

$$t_{rv} = \frac{t_{rv1} + t_{rv2}}{2} \tag{2.10}$$

$$t_{rv1} = (V_{ds} - R_{ds,on} I_{ds,on}) R_g \frac{C_{gd1}}{U_{plateau}} \tag{2.11}$$

$$t_{rv2} = (V_{ds} - R_{ds,on} I_{ds,on}) R_g \frac{C_{gd2}}{U_{plateau}} \tag{2.12}$$

where $U_{plateau}$, R_g, C_{gd1} and C_{gd2} are the same as in the equations (2.7) and (2.8). Summing up the losses in the MOSFET and its anti-parallel diode gives the total loss for one switching cycle

$$P_{total} = P_{sw,M} + P_{sw,D} \tag{2.13}$$

2.3 Theoretical calculation of steady-state temperature of switches

When the power electronic components are exposed to a current and voltage they will be heated up due to losses. In the case of a transistor, this thermal development will affect performance. At high operating temperatures, the performance can degrade. In the worst case scenario, the switch can overheat and break. Therefore, it is important to be able to estimate the junction temperature a switch will have when designing the circuit. In fig. 2.10, a simplified steady-state thermal model of the junction temperature to water temperature is presented with the thermal resistances between junction-to-case, R_{jc}, thermal-interface-material, R_{cp}, and plate-to-water, R_{hs} and the power generation from MOSFET operation.

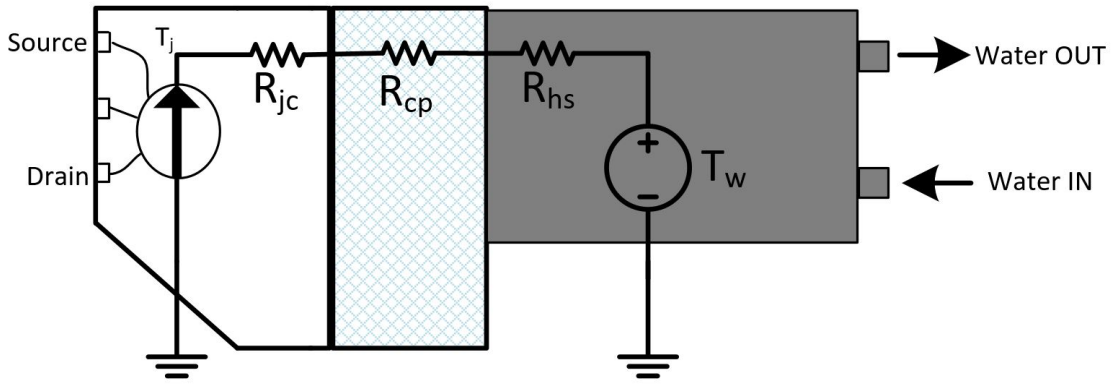


Figure 2.10: A resistive thermal network of the MOSFET and cooling plate.

The steady-state temperature of the MOSFET can be calculated according to

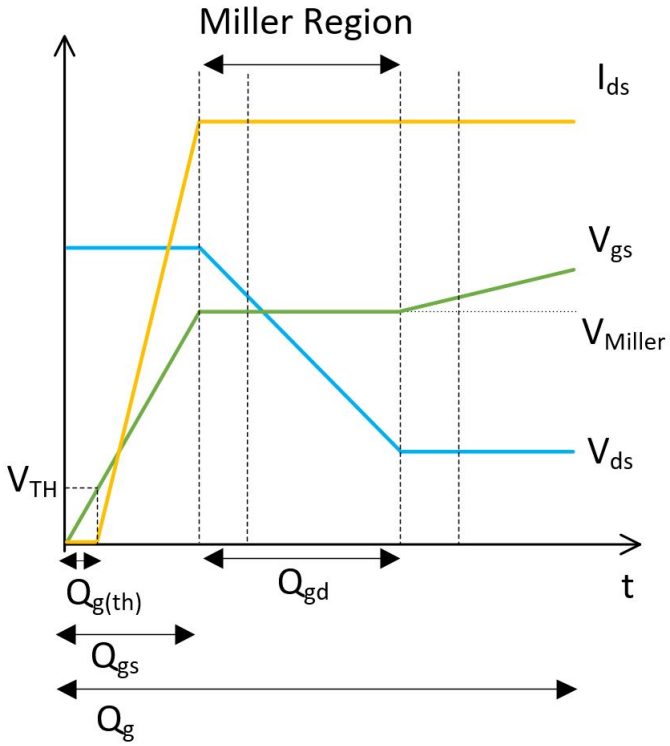
$$T_j = P_{tot}(R_{th,jc} + R_{th,cp} + R_{th,hs}) + T_w \tag{2.14}$$

where $R_{th,jc}$ is the thermal resistance for junction to case, $R_{th,cp}$ is the thermal resistance of the cooling paste and $R_{th,hs}$ is the thermal reistance of the heat sink to water. T_w is the water temperature and P_{tot} is the sum of the switching and conduction losses. The thermal resistance of the heat sink and the thermal interface material have been calculated according to [5].

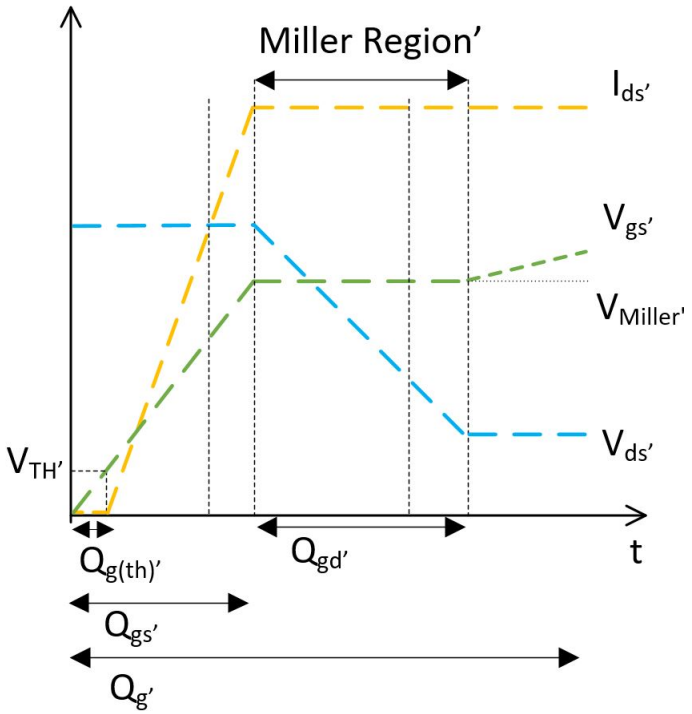
2.4 Slew rate control of Transistors

Slew rate control of the transistors can be implemented simply by inserting a resistor of 0.1 to a few hundreds of Ohms between the gate driver and MOSFET gate. The purpose of adjusting the slew rate is to have a smooth transistion of conduction between the MOSFETs within a half leg in order to minimize transients and avoid the need of having both input and output filters added to the circuit, which can be very large, lossy and expensive.

Figure 2.11 shows the turn-on behaviour of the MOSFET. The gate-to-source voltage starts to increase as charge flows into the gate, from the gate controller. The rise in V_{gs} at start is achieved by charging the capacitance C_{gd} and C_{gs}. When voltage between gate-to-source crosses the threshold voltage of the MOSFET (typically 2.5 V), current starts to flow between drain-to-source. Eventually, gate-to-source voltage reaches a constant value which is due to the Miller region. The slope of the Miller region is generally zero or near zero, but it is dependent on allocation of the drive current between C_{gd} and C_{gs}. If the slope is not zero that means that some of the drive current is flowing into C_{gs}. If the slope is zero then all the current is flowing into C_{gd}. The voltage between drain-to-source reduces in this region. Once V_{gs} crosses the Miller region, the voltage between gate-to-source continues to increase until gate saturation, decided by the gate drive circuit [13]. If the main current path contains parasitic inductance, the risk of ringing in the Miller region is substantial.



(a) Illustration of MOSFET's fast gate turn-on.



(b) Illustration of MOSFET's slow gate turn-on.

Figure 2.11: Diagram of MOSFET gate turn-on in case of fast gate turn-on and slow gate turn-on.

In this thesis, when adjusting the slew rate, the slope of V_{gs} is changed during turn-

on and turn-off with an RCD circuit, which an example of can be seen in fig. 2.12. The turn-on time is increased by forcing the turn-on pulse to go through the turn-on resistor, R_{on}, due to the diode blocking in that direction. The turn-off is kept short since the turn-off resistor, R_{off}, is of a lower value than R_{on}. This is done to avoid shoot-through of the current in the phase leg between the two MOSFETs by utilizing the diode in series with this low resistance. The rise time of V_{gs} is determined by the time constant, τ, that is equal to $R_{on}C_{gs}$ during turn-on and $R_{off}C_{gs}$ during turn-off. As mentioned previously in section 2.2, V_{ds} goes between blocking voltage to $R_{ds,on}I_{ds,on}$ during the Miller region, which is dependent on C_{gd}. By inserting the external capacitor between gate and source, C_{gd} is not affected directly. However, since the slope of V_{gs} is lower, the gate current increase, which in turns charges C_{gd} and thus overcoming the Miller region, will also be lower and thereby extending the time when V_{ds} is changing. This is illustrated in fig. 2.11 [13].

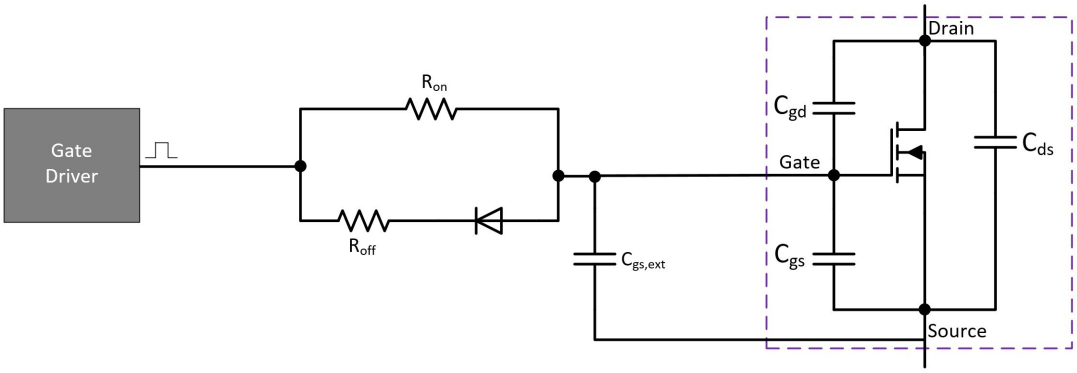


Figure 2.12: Schematic of the slew rate RCD circuit connecting to the gate of the MOSFET.

Increasing the slew rate leads to increased losses in the MOSFET but with the benefit of reducing the high dV/dt that would otherwise be present when V_{ds} goes from high to low, which in turn would introduce transients and ripple. The advantage of adjusting the slew rate is smoother switching waveforms. It is also possible to reduce losses (snubber circuit and/or filter losses), reduce EMI, and improve the efficiency of the converter. More importantly for the design this thesis deals with, the overall size of the inverter can be reduced due to eliminating the need for filters.

2.5 DC Capacitor Bank design

Due to the inverter being a non-ideal circuit which contain a lot of parasitic inductances there will be transients and harmonic present when operating it. To negate the effect of these and also make sure that a stable DC voltage is supplied a DC capacitor bank is needed to make the voltage stiff. The design of the DC capacitor bank is dependent on many things, such as frequency, current ripple and voltage ripple but also temperature when selecting the type of capacitor.

Since the inverter in question is fed power from a battery, harmonics and ripple from the input side will be negelected in the calculations. The average current that goes into the inverter can be expressed as

$$I_{avg} = \frac{3}{4} I_{ph,peak} m_a cos(\phi) \tag{2.15}$$

where m_a is the modulation index, $cos(\phi)$ is the power factor of the load and $I_{ph,peak}$ is the peak value of any phase current [14]. The capacitor current consists of sideband harmonics around the switching frequency and multiples of it. The RMS current in the capacitor bank can therefore be expressed as

$$I_{c,rms} = I_{ph,rms} \sqrt{2m_a(\frac{\sqrt{3}}{4\pi} + cos(\phi)^2(\frac{\sqrt{3}}{\pi} - \frac{9}{16}m_a))} \tag{2.16}$$

where $I_{ph,rms}$ is the phase RMS current. In [14], a formula is presented that models the peak-to-peak voltage ripple on the DC link as a function of switching frequency, capacitance and capacitor voltage and current, but it is neglecting the ESR of the capacitor bank

$$V_{dc,pk-pk,ripple} = \frac{0.7(I_{ph,peak} - I_{avg})m_a}{C_{dc} f_{sw}} \tag{2.17}$$

where f_{sw} is the switching frequency, C_{dc} is the capacitance in the capacitor bank. Rewriting (2.17) and allowing the DC ripple to be no more than for instance 5% of the battery voltage gives that the minimum capacitance needed can be expressed as

$$C_{dc} = \frac{0.7(I_{ph,peak} - I_{avg})m_a}{0.05 V_{dc} f_{sw}} \tag{2.18}$$

Besides using the equations above for design of the DC capacitor bank there are different ways this design can be optimized with regards to volume, cost and losses. The capacitors for the DC bank that are being considered are ceramic, film and electrolytic ones. These different objective functions can then be expressed as equations, where the objective function with respect to volume is

$$V_{total} = n_{film} V_{film} + n_{ceramic} V_{ceramic} + n_{elec} V_{elec} \tag{2.19}$$

where V_{film}, $V_{ceramic}$ and V_{elec} is the volume of one capacitor of each kind while n_{film}, $n_{ceramic}$ and n_{elec} is the number of each type of capacitor. V_{total} is the total volume where the objective function is to minimize this equation. The cost equation can similarly be expressed as

$$Total\ Cost = n_{film} Cost_{film} + n_{ceramic} Cost_{ceramic} + n_{elec} Cost_{elec} \tag{2.20}$$

where $Cost_{film}$, $Cost_{ceramic}$ and $Cost_{elec}$ is the cost for one film capacitor at a certain bulk price for each type of capacitor. And lastly, the loss equation can be expressed as

$$P_{tot} = I_{film}^2 ESR_{film} + I_{ceramic}^2 ESR_{ceramic} + I_{elec}^2 ESR_{elec} \tag{2.21}$$

where I_{film}, $I_{ceramic}$ and I_{elec} is the total current going through all each respective capacitors. ESR_{film}, $ESR_{ceramic}$ and ESR_{elec} is the equivalent series resistance of each respective capacitor. If one would like to take all these objective functions into consideration when optimizing it can easily be done by minimizing the following expression,

$$optimization = \frac{V - V_{opt}}{V_{opt}} + \frac{P - P_{opt}}{P_{opt}} + \frac{C - C_{opt}}{C_{opt}} \tag{2.22}$$

where V is the volume, P is the losses and C is the cost. Meanwhile, V_{opt} is the optimized case when minimizing volume, C_{opt} is the optimized case when minimizing cost and P_{opt} is the optimized case when minimizing losses.

Each of these objective functions have constraints presented to them. One that applies to all of them is a minimum capacitance that must be achieved which can be decided with (2.18), then the following must hold

$$C_{min} \leq n_{film}C_{film} + n_{ceramic}C_{ceramic} + n_{elec}C_{elec} \tag{2.23}$$

where C_{film}, $C_{ceramic}$ and C_{elec} is the capacitance per capacitor for each type. Furthermore, another constraint that holds true for all the objective functions is that the maximum ripple current per capacitor must be below the limit specified for each type of capacitor. Assuming the the capacitors are connected in parallel with each other as in fig. 2.13 where each capacitor represents n number of capacitors. Then the RMS current through each capacitor can be expressed as

$$\frac{I_{film}}{n_{film}} \leq I_{c,rms}\frac{\frac{1}{ESR_{film}}}{\frac{n_{film}}{ESR_{film}} + \frac{n_{ceramic}}{ESR_{ceramic}} + \frac{n_{elec}}{ESR_{elec}}} \tag{2.24}$$

$$\frac{I_{ceramic}}{n_{ceramic}} \leq I_{c,rms}\frac{\frac{1}{ESR_{ceramic}}}{\frac{n_{film}}{ESR_{film}} + \frac{n_{ceramic}}{ESR_{ceramic}} + \frac{n_{elec}}{ESR_{elec}}} \tag{2.25}$$

$$\frac{I_{elec}}{n_{elec}} \leq I_{c,rms}\frac{\frac{1}{ESR_{elec}}}{\frac{n_{film}}{ESR_{film}} + \frac{n_{ceramic}}{ESR_{ceramic}} + \frac{n_{elec}}{ESR_{elec}}} \tag{2.26}$$

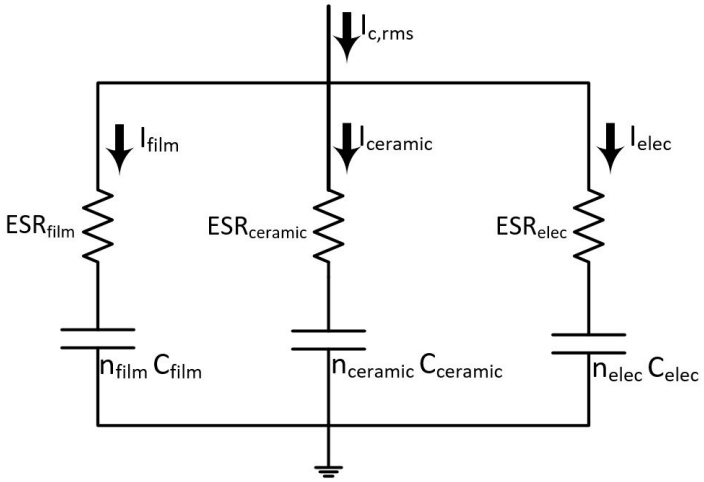


Figure 2.13: Illustrative schematic of how to model the capacitor currents.

3

Case setup

3.1 Machine Parameters

The machine that is provided for the inverter design is crankshaft integrated starter generator (CISG). The machine winding parameters are then scaled to 48 V. Table 3.1 illustrate machine parameters and parameters for each individual coil, i.e. there are eight individual coils per phase which are normally connected in parallel, but not in the case where IMMD concept is applied.

Table 3.1: Machine parameters and values for individual coil.

	Machine Parameters	1/8th of the machine	Units
Pole pairs	16	2	-
Maximum speed	7000	7000	RPM
i_{RMS}	658	82.3	A
Torque	63.7	8	Nm
Self inductance	2.88	23	μH
Coil resistance	3.79	3.79	$m\Omega$
Electrical time constant	6.071	6.07	ms

3.1.1 Choice of inverter topology

The topology that was chosen for the design of the inverter was PPB-II, which was presented in 2.1.2. This choice was made based of [2], where PPB-II displays superior properties to the MHF and SPB converters. While the PPB-I performed similar to PPB-II there was a quite a big difference in the energy storage requirement which made the choice of PPB-II final due to the desire to minimize the volume of the inverter. Moreover, utilizing a series connected topology requires DC voltage control over each submodule to ensure that the maximum voltage is not exceeded. This is complex to design and quite unnecessary when dealing with a low voltage level. One thing to keep in mind is that the article [2] is a study of different converter topologies applied in a fully electric vehicle while this report deals with a mild hybrid however, the reasoning applies the same is assumed.

3.2 Design aspects of prototypes

Table 3.2: Design aspects considered during construction of of two prototypes

	Prototype - 1	**Prototype - 2**
Type of inverter	Single phase half bridge	Distributed inverter
Inverter topology	Nil	PPB-II
Board	Breadboard+Veroboard	PCB
Power Rating	1/8th of full machine power	1/8th of full power
Choice of transistors	Based on if it can be hand soldered	Highest performance + cost aspect, Si/WBG
Snubbers	Yes, add on	None
Harmonic Filters	No	Yes, add on outside PCB if needed
Slew rate gate control	Yes, experimental	Yes
Cooling	Simple air cooling	Integrated water cooling
DC-Cap	Electrolytic	hybrid ceramic (two different capacitor in parallel)
Pspice design	Yes	No
Measurements		
Total efficiency	No	Yes
Losses		
Transistor losses	Yes	Yes
DC-Cap losses	No (try the method)	Yes
Snubber losses	Yes	Yes
Gate drive losses	No	Maybe
Temperature		
DC-Cap temp	No	Yes
Switch case temp	Yes	Yes
Gate driver temp	No	Yes
Abnormalities	Yes	Yes
Frequency	Yes	Yes

Table 3.2 illustrates different features that were included in the design and construction of two prototypes. The key factors which were improved among both prototyes were inverter topology, board classification, selection of transistors, dc-capacitor bank design. Moreover, other worth measuring parameters were losses (mainly transitor and dc-cap), temperature rise and efficiency.

3.3 Work approach

A litterature study on 48 V system, different inverter topologies and modular inverters for hybrid electric cars is carried out for full understanding of this topic. This involves reading scientific papers and journals, data sheets and student litterature on the subjects. The basis of the pre-study is to get familiar with the concept of 48 V system and how compact and intergrated inverters can improve the performance of electric drivetrains.

To assist in the designing phase of the project, simulations were intended to be carried out, but this proved to not be possible. For designing the circuit, PSpice is used as simulation and computational software during this project, but is not limited to this one exclusively. MATLAB will be used to handle data and create graphs for presenting results.

Moreover, to realize the two prototypes of the inverter, components are acquired either from the available labs at the department or ordered from retailers. These are then mounted either by hand soldering or, for the surface mounted type components, a reflow oven is used. For the second prototype, a PCB is ordered from a manufacturer and is created by the supervisor of this project since he possess the knowledge to design it. Various instruments are used in order to carry out relevant measurements of current, voltage, frequency and temperature.

Even though the inverter is to be implemented in a mild hybrid vehicle, using an electric machine as load and a battery as energy supply is tedious. Therefore, a dummy load is used instead of an electric machine and instead of a 48 V battery a power supply that can provide the required current and voltage is used. Below in fig. 3.1 a preliminary scheme of the setup and interesting measurement points are presented. Here all three phases would have voltage and current measured, but it is not drawn to avoid cluttering the figure.

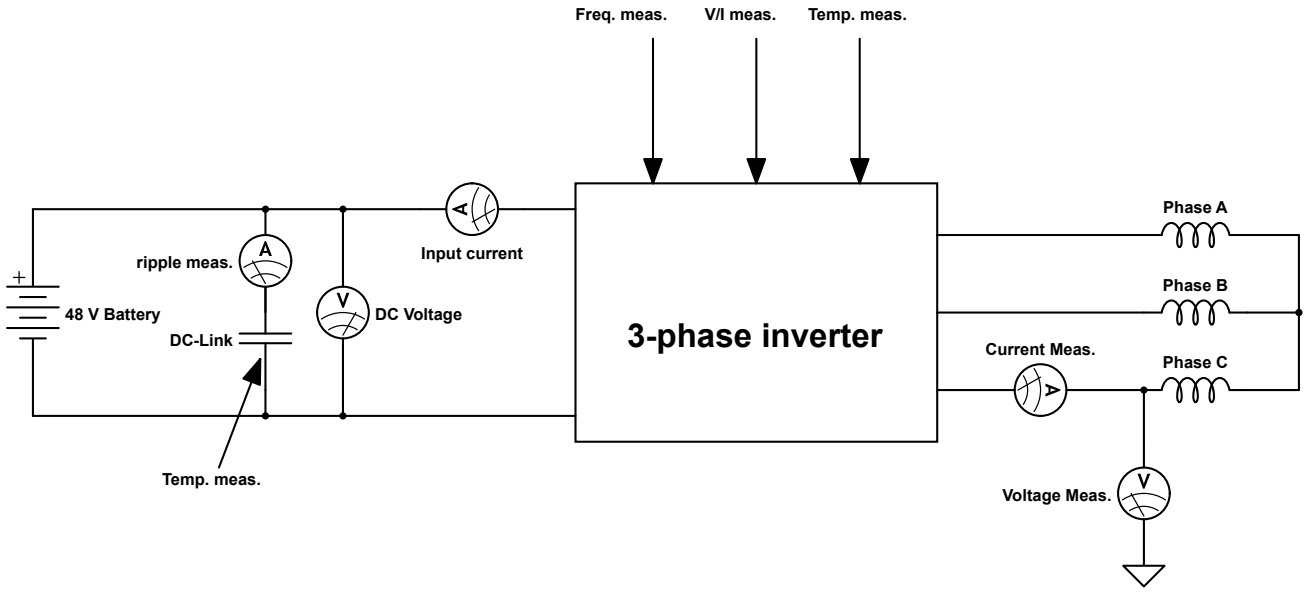


Figure 3.1: Preliminary sketch of how the inverter will be set up for measurements.

The measurements that are taken are at the DC-link capacitor, the switches in the inverter and output and input power. The quantites that are measured are current, voltage and frequency throughout the inverter to determine necessary parameters such as the transistors switching characteristics, current and voltage at load and DC capacitor currents and voltages.

3.4 Comparison of semiconducting switches

A theoretical comparison of 35 different high-performance transistors based of Si, SiC and GaN has been made. This comparison focused on losses, cost and thermal development with respect to certain parameters, see appendix A for the full list. This list is used as a basis for the selection of switches needed for each prototype. The reason for looking more carefully at these parameters are listed below.

1. Losses - high efficiency of the inverter is one of the top priorities for this project and the switches will affect this a lot.
2. Cost - The goal is to deliver a prototype that in the future will be implemented in a mild hybrid vehicle. Since the aim of selling a vehicle is to make a profit, the cost will affect the choice of switches.
3. Junction temperature - Seeing that a big benefit of a distributed inverter is the possiblity to integrate it tightly with the electric motor, it would be beneficial to have a compact cooling system as to decrease the total weight and size of the inverter. Having low thermal resistance in the cooling circuit as well as in the switches, assures that the junction temperature will be at a good operating range while minimizing the size of the cooling circuit.
4. Number of switches and size - How many switches that are being used will affect the size of the whole inverter, whereas a small one would be preferable with the reasons given above. Aditionally, depending on the price, the number of switches can greatly affect the cost of the inverter.

The conduction losses in a switch are calculated with (2.1) while the switching losses are computed with (2.2) and (2.3). These are summed up to get the total loss for one switch during one switching cycle. The cost of each switch has been made with the perspective of putting the inverter into series production. Therefore, by visiting different retailers' website and analyzing the price for different off-the-shelf components and the amount of switches needed for a certain number of inverters, a cost of the switches has been listed.

The junction temperature affects not only the whole performance of the switch but also indirectly the dimensioning of the cooling circuit. To theoretically determine the junction temperature the equations (2.14) and fig. 2.10 was used. Lastly, the number of switches and the size of these affect mainly the cooling circuit but also cost and was taken into consideration given the power ratings and what topology that was being built in each prototype.

3.5 OrCad and PSpice simulation

For a theoretical comparison with the different prototypes that are constructed, a model of the each prototype is intended to be created in OrCad and simulated in PSpice. Due to complications with long simulation times and trouble finding non-ideal components created by manufacturers this part of the project was abandoned

due to being too time consuming while not yielding related results. However, the early stages of simulation gave a lot of knowledge and understanding of the circuit in question and helped with grasping the behaviour of the MOSFETs. Therefore the circuit is presented below since the first prototype was built of this schematic before abandoning the simulations.

In fig. 3.2, a circuit of the first prototype is shown however, a different MOSFET is used in the schematic than in the prototypes due to not being available at all retailers. As explained previously, the first prototype is a single phase half bridge that was made with the intention to be operated at 1/8th of the power. The circuit consist of the non-ideal Si transistors as well as the gate driver, where the PSpice models have been provided by the manufacturer. The gate driver was later changed in the practical part of the project for the first prototype due to intermittent errors that kept occurring which would brake it. Due to this, the simulations did not yield any result that was considered relevant since the new gate driver that was used in prototype 1 did not have a working PSpice model. Some series inductances and resistances have been implemented to make the battery more realistic, $R23$ and $1.24\ \mu H$. Additionally, it can be seen that a dead-time circuit had to be implemented between the PWM generation and gate driver, consisting of an RCD circuit, since this gate driver did not have that function integrated. Between the gate of each transistor and the gate driver there is another RCD circuit, which is made to adjust the slew rate as explained in section 2.4. The turn-on resistors are $R28$ and $R29$ and the turn-off resistors are $R30$ and $R31$. The capacitor connected to each source is to improve the transistors' switching operation and prevent that it conducts through its internal capacitances. These resistor values have been changed to higher and lower values to investigate how the losses of the transistor change depending on if the switching of the transistors is either done hard or soft.

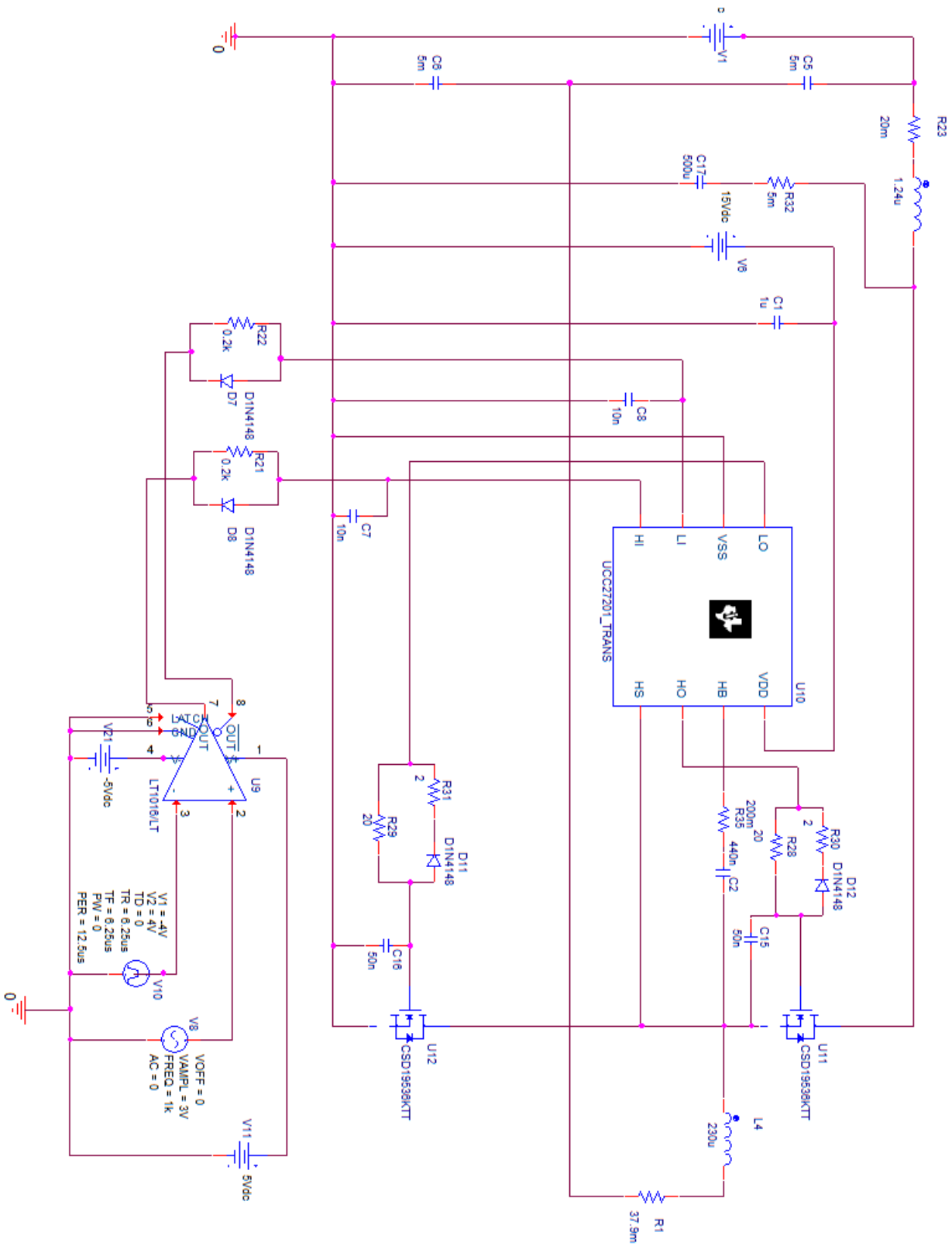


Figure 3.2: OrCad design of the first prototype for simulation in PSpice.

3.6 GAMS Optimization of DC capacitor bank

In designing an inverter usually the DC capacitor bank occupy a lot of space, sometimes it constitutes up to 30% of the total volume of the inverter and can also make up 20% of the cost and weight [14]. With the use of the objective functions and constraints presented in section 2.5 the optimization program GAMS (General Algebraic Modeling System) was used to find an optimal solution with respect to volume, cost and losses and would then decide how many capacitors of which kind would be needed. This program was implemented on short notice, therefore the script is quite simple and require the user to feed in the parameters of each capacitor.

The capacitors that were considered can be seen in table 3.3 where all of them are rated for 100 V and the ensuing parameters have been calculated for 100 kHz. The reason for chosing these capacitors are due to their high performance, commercial availability and that they are cost efficient. The last ceramic capacitor presented in table 3.3 has not been subject to optimization but is added to the design to damp ripple due to its higher impedance at higher frequencies.

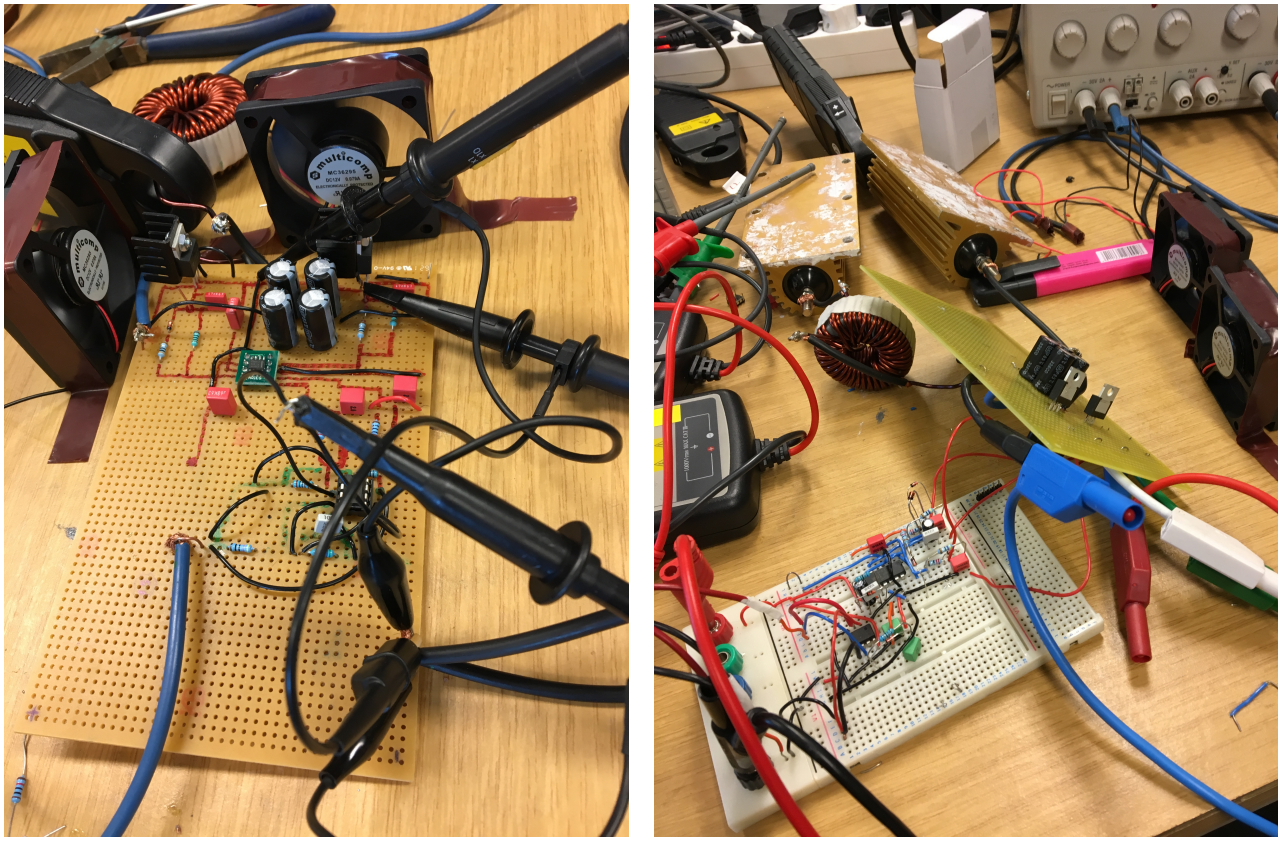
Table 3.3: Capacitor candidates for the DC capacitor bank.

	Nominal cap. $[\mu F]$	**Cap. @ 48 V DC Bias** $[\mu F]$	I_{max} $[A]$	**Volume per unit** $[cm^3]$	**ESR @ 100 kHz** $[m\Omega]$	**Cost per 1000 units** [€]
Electrolytic Capacitor Rubycon, 100 V 100ZLJ330M12.5X35	330	330	2.6	2.1476	0.386	864.6
Ceramic capacitor TDK, 100 V C5750X7S2A156M250KB	15	6.239	5	0.03312	3.165	1540
Film capacitor Kemet, 100 V MDC10106K100A58P7TUBE	10	10	13	3.2131	2.645	6240
Ceramic capacitor TDK, 100 V C4532X7R2E474K230KA	0.47	0.401	1.3	0.0331	32.86	329

3.7 Construction of inverter

3.7.1 Prototype 1

Prototype one is built after the schematic made in OrCad as can be seen in fig. 3.2. The MOSFET which was selected for this prototype is of Texas Instruments, model CSD19531KCS and was selected because of its availability. However, the passive components in the slew rate circuit has different values and were changed depending on the measurements that were carried out. See appendix A for list of values on the final version of the first prototype one. Worth mentioning here is that many lessons were learned during the construction of the first version of prototype 1, which can be seen in fig. 3.3a. This delayed the project quite a lot. These errors were due to unknown faults occuring with the gate driver, despite following the manufacturer's reference design, as well errors in design, such as traces that were not soldered properly.



(a) Version 1A of first prototype. **(b)** Version 1B of the first prototype.

Figure 3.3: 1^{st} prototype setup.

Finally, the decision was made to remake the first prototype and seperating the gate driver and PWM generating circuitry from the load and transistors. The gate driver and PWM generation was mounted on a bread board for easy maintencance and error searching while keeping the transistors and load on a separate vero board. This version of prototype one can be seen in fig. 3.3b. The original gate driver evenutally had to be replaced with one from International Rectifier, model IR2010, which resolved the problems that kept occuring on the second version of prototype 1.

3.7.2 Prototype 2

Prototype two is built on the base of prototype 1. However, prototype 2 is constructed on PCB and the design is made by our supervisor. The passive components in the slew rate circuit are mounted through female connectors for easy access to investigate different slew rate setups. Two different PCBs are designed and stacked on top of each other, one for the gate driver circuitry and other for the MOSFETs and DC capacitor bank. The MOSFET which is selected for this second prototype is from Infineon Technologies model, IPP045N10N3GXKSA1 and was chosen based on its availability. The DC capacitor bank that was installed utilized all space available for the ceramic type of capacitors. 60 units of the ceramic capacitor with 15 μF and as well as 24 units of the smaller ceramic capacitor of 0.47 μF presented in

table 3.3 was soldered onto the board resulting in a capacitance of 384 μF at a 48 V DC voltage bias. Fig. 3.4 gives an overview of the prototype 2 setup. The laptop generates the code for the microcontroller which then gives the switching signals to the gate drivers, seen in 3.5a. These controls the MOSFETs seen in fig. 3.5c and lastly the power goes to the load.

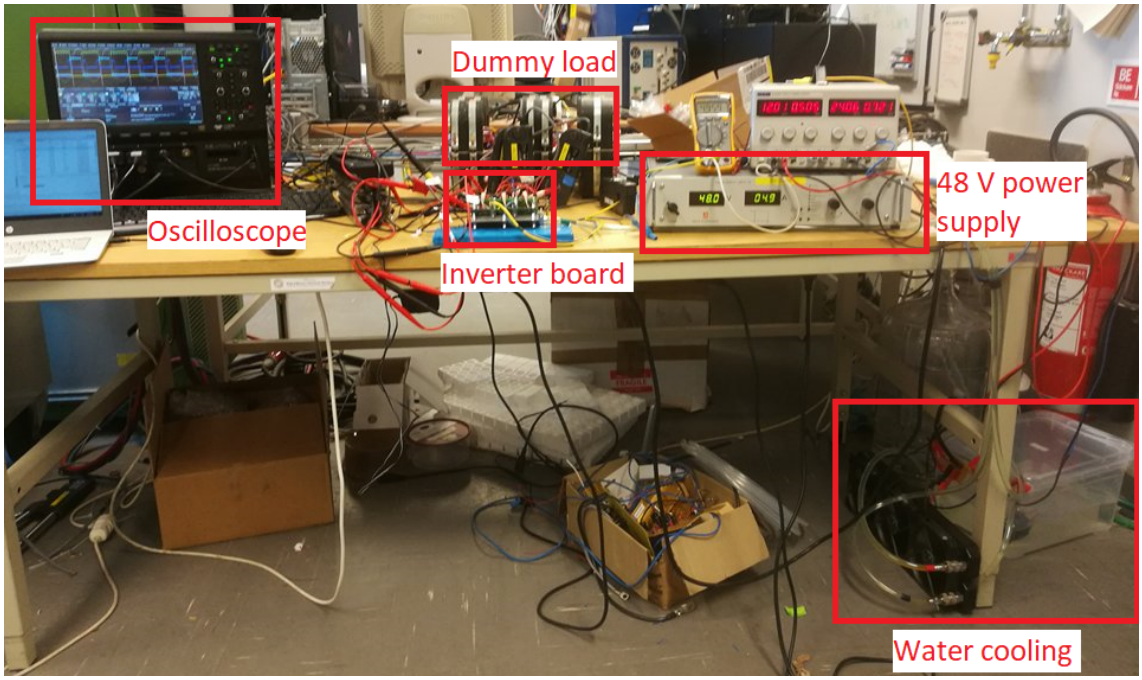
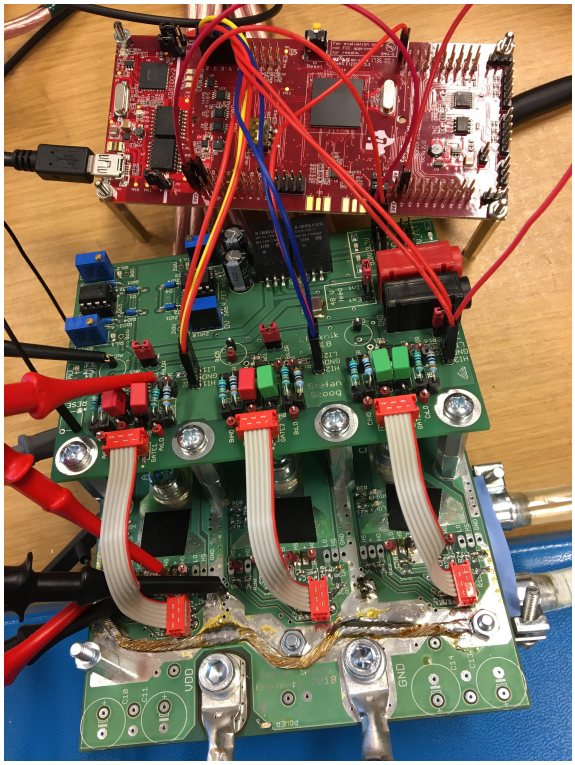
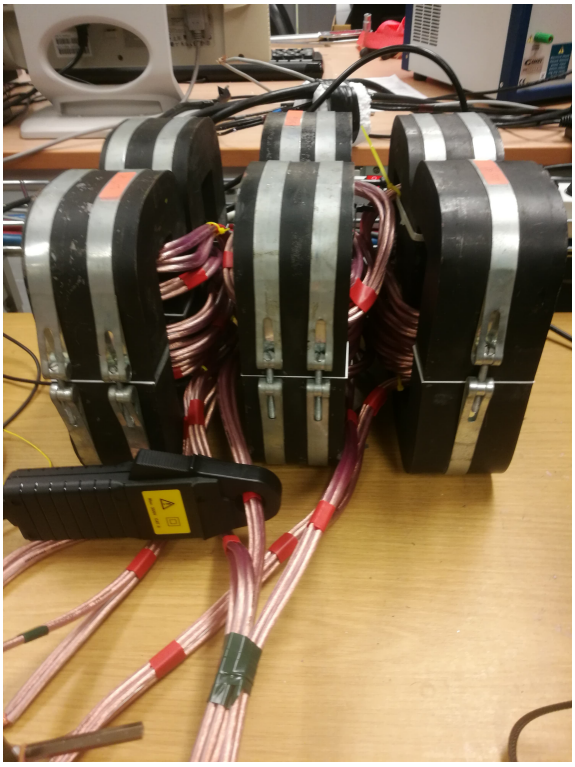


Figure 3.4: Second prototype setup.

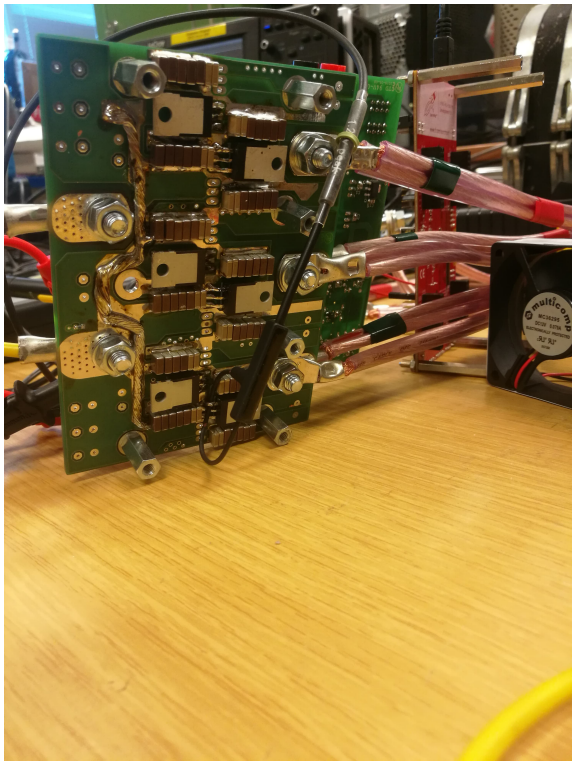
The water cooling can be seen in the bottom right of the picture. Moreover, to protect the PCB board from over- and undervoltages, a protection circuit is implemented. A microcontroller from Texas instruments, C2000 family, model TMS320F28379D LaunchPad is adopted to generate PWM of required switching frequency of 100 kHz. MTALAB simulink blocks are used to generate the PWM signal in the form of C language code. This is then executed in Code Composer Studio 6.2.0, a recommended software which is used to link the microcontroller with computer in order to achive required PWM signal, as can be seen in fig. 3.5c. In addition, the same gate driver of Texas instruments, model UCC27201 is used in protopye 2. Instead of an electric motor, a dummy load is used, consisting of three coils with inductances of 24.8 μH, 23.5 μH and 23.5 μH and all of them have approximately 3.6 $m\Omega$ in coil resistance. These are visible in fig. 3.5b. Fig. 3.4 gives an overview of the prototype 2 setup. The laptop generates the code for the microcontroller which then gives the switching signals to the gate drivers, seen in 3.5a. These controls the MOSFETs seen in fig. 3.5c and lastly the power goes to the load. The water cooling can be seen in fig. 3.5d.



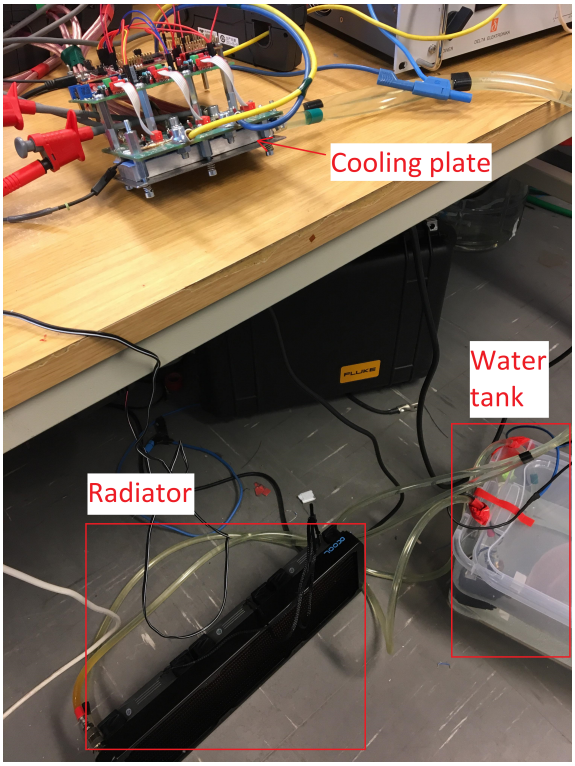
(a) Gate driver board with PWM signals from microcontroller.



(b) Three phase dummy load.



(c) PWM from microcontroller for gate driver and MOSFETs implementation along with DC capacitor bank.



(d) Integrated cooling plate setup.

Figure 3.5: Overview of the 2^{nd} prototype.

3.8 Measurements

3.8.1 Prototype 1

For prototype one, the following measurement points are taken into consideration for analyzing the transistor operation: gate-to-source voltage V_{gs}, drain-to-source voltage V_{ds}, drain-to-source current I_{ds} and gate driver input. The voltages are measured with two different differential probes, one is from Pico Technology, model TAO43 and Testec, model TT-SI 9101, the current is measured with a current transducer, also known as a Rogowski coil, of brand CWT Mini HF3R. These measurements are taken for both of the MOSFETs. Moreover, the load current and voltage are measured with the same differential probes mentioned above and for current, a current clamp from LeCroy, model AP011. To examine if the supplied voltage possess an acceptable ripple, the voltage over the upper and lower part of the DC capacitor link are measured with the differential probes and the current through the lower DC capacitor is measured with the Rogowski coil previously mentioned. Two seperate power supplies are used, one for the gate driver circuit, from manufacutrer Aim TTI, model EL302RT, and another for the transistors supply from Hewlett Packard, model 6274B. Due to the Hewlett Packard power supply having analogue gauges, for accurate measurement of the power supply, digital multimeter instruments fluke 117 and 175 are incorporated. The reference wave and triangular wave are generated with two function generators, DMI FG1201B and Aim tti tg315 respectively, and all the measurements are viewed on an oscilloscope from LeCroy, model Waverunner 620Zi.

In fig. 3.3b some of the measurement points mentioned above can be seen. To get the first prototype operational and get the measurements a dummy load is used that consists of an inductor of 440 μH with two series resistors of 220 $m\Omega$ instead of an actual rotating machine.

3.8.2 Prototype 2

For prototype two, the same type of measurements are taken in order to make a comparison between the two prototypes with the exception of measuring current through the DC capacitor bank due to a measurement point for this not being available. The value of the inductance for each phase in the dummy load is measured with Atlas LCR, model LCR40. However, for the current measurement a new current transducer, of brand CWT, model 015b ultra mini is used because of its smaller size which can easily be maneuvered around the MOSFET's legs. Due to the MOSFETs placement and how the cooling plate is installed, the current transducer is setup on only one transistor whereas the other transistor measurements, such as V_{gs}, V_{ds} and gate signal can be carried out for all three transistors. Moreover, thermal development and temperature rise of the components is measured from thermal imager of brand Fluke model Ti45. An overview of the measurement points can be seen in fig. 3.4. For measuring the second prototype, a new oscilloscope with eight channels is acquired of brand LeCroy, model MDA805.

4

Results

4.1 Results from Prototype 1

4.1.1 Performance and losses

The first prototype was operated and measured initally at 10 kHz to confirm that it was working as intended and then the switching frequency was increased all the way up to 100 kHz. The amplitude modulation index was kept constant at 42.3 % and all measurements are taken from prototype 1B with the load of 440 μH and 440 $m\Omega$. The measurements carried out at the different frequencies was done with the slew rate adjusted, in one case the gate's turn-on was fast and in another its turn-on was slower. For the fast case, the turn-on resistor had a value of 4.7 Ω and for the slow case it was 100 Ω. In the case of slower gate turn-on, a capacitance was placed between gate and source of the MOSFETs which had a value of 32 nF. For the case of faster gate turn-on, a gate to source capacitance was not intended initally but was installed it anyway due to that there was too much transients making the switching unstable, most likely due to the Miller Effect [15]. The capacitance used in this case was 4.7 nF. In both cases the turn-off resistor was kept at 2.2 Ω.

In fig. 4.1, the lower transistor is presented with the two different slew rates compared against each other. Further down, in fig. 4.3, the load current and load voltage have been measured during the same events. Worth commenting here is that due to being two separate measurements with different signals, the trigger requirement on the oscilloscope was not set to the same value in order to capture the signals. This is the reason why the load currents look like they are phase shifted. When comparing these figures with each other it is observable that for the hard turn-on of the gate there are a lot of transients presents. In the case of V_{ds} the transients are almost twice the size of what the blocking voltage should be when turning off. This makes soft turn-on of the gate preferable, not from an efficiency perspective but rather to avoid input and output filters in the end product and thereby reducing the size and complexity of the inverter design. However, as can be seen in fig. 4.3 the load current in the soft turn on case has become distorted from its sine wave reference.

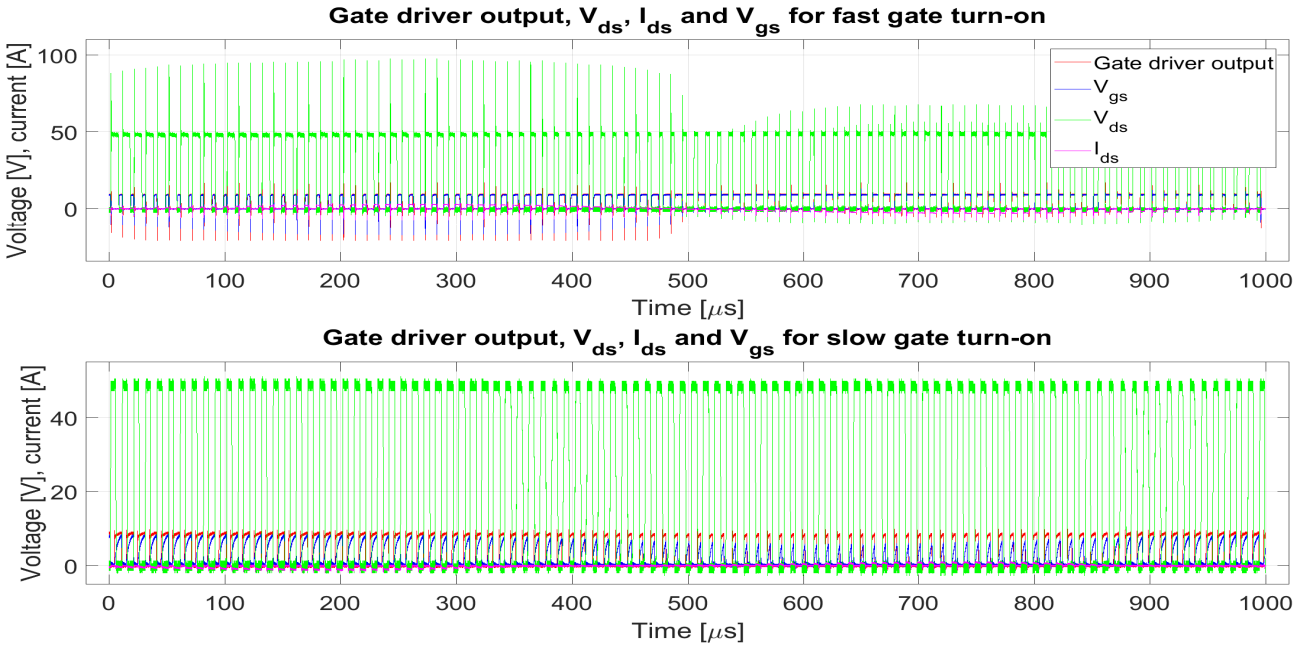


Figure 4.1: Comparison of the lower transistor's switching waveforms in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 100 kHz switching frequency.

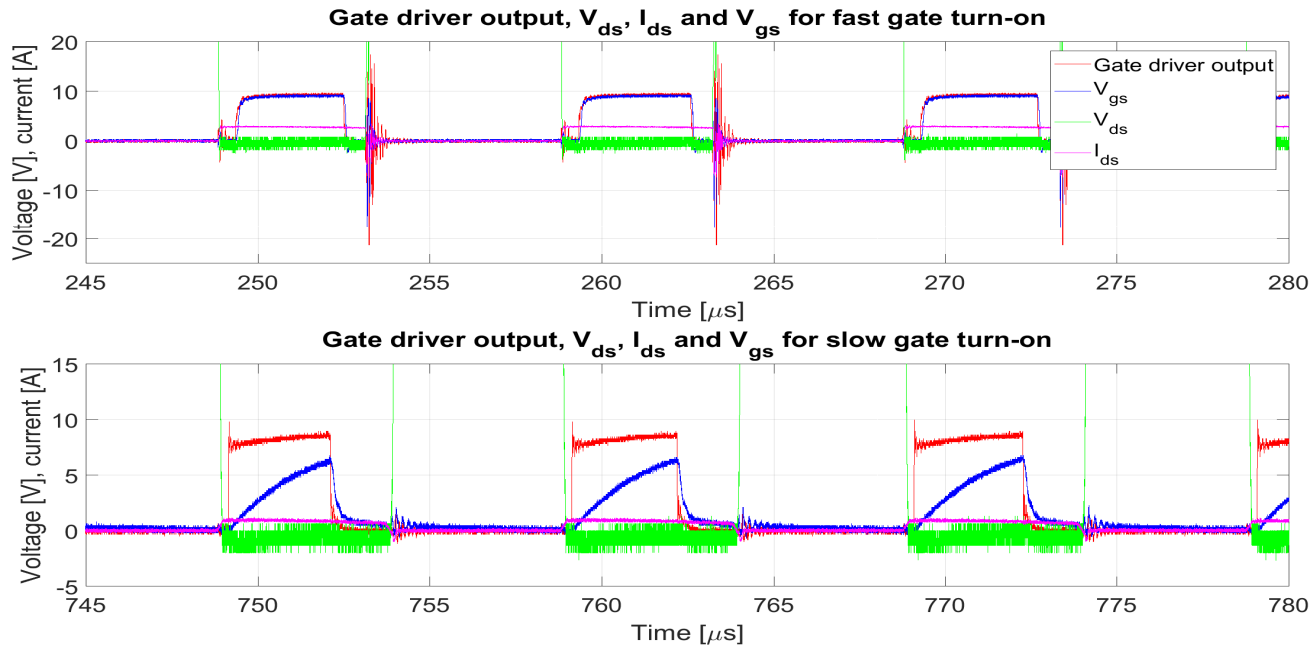


Figure 4.2: Zoom in on signal from gate driver and V_{gs} voltage to the the lower transistor's in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 100 kHz switching frequency. Measurements are taken from prototype 1B with the load of 440 μH and 440 $m\Omega$.

This can be explained from the fact that when switching as fast as 100 kHz the slow turn-on of the gate is too slow and the MOSFET never reaches its saturated mode. Taking a closer look at the transistor's switching waveforms in fig. 4.2 reveals that the signal V_{gs} does not reach 10 V properly as it does when turning on the gate fast. Moreover, in the zoomed figure 4.2 the transients that occur when turning off the MOSFET can be observed on all signals, including the gate driver output. The transients are there in both cases of fast and slow turn-on however, with the increased resistance and capacitance in the slew rate circuit they are damped significantly.

In order to utilize the slow turn-on of the gate while making sure the load current is not distorted, the frequency had to be lowered. It would have been possible to try and improve the dead-time circuit as well as the slew rate circuit until switching at 100 kHz could be achieved with minimum distortion however, this is very complicated to do as well as time consuming and an easier approach would be to lower the frequency.

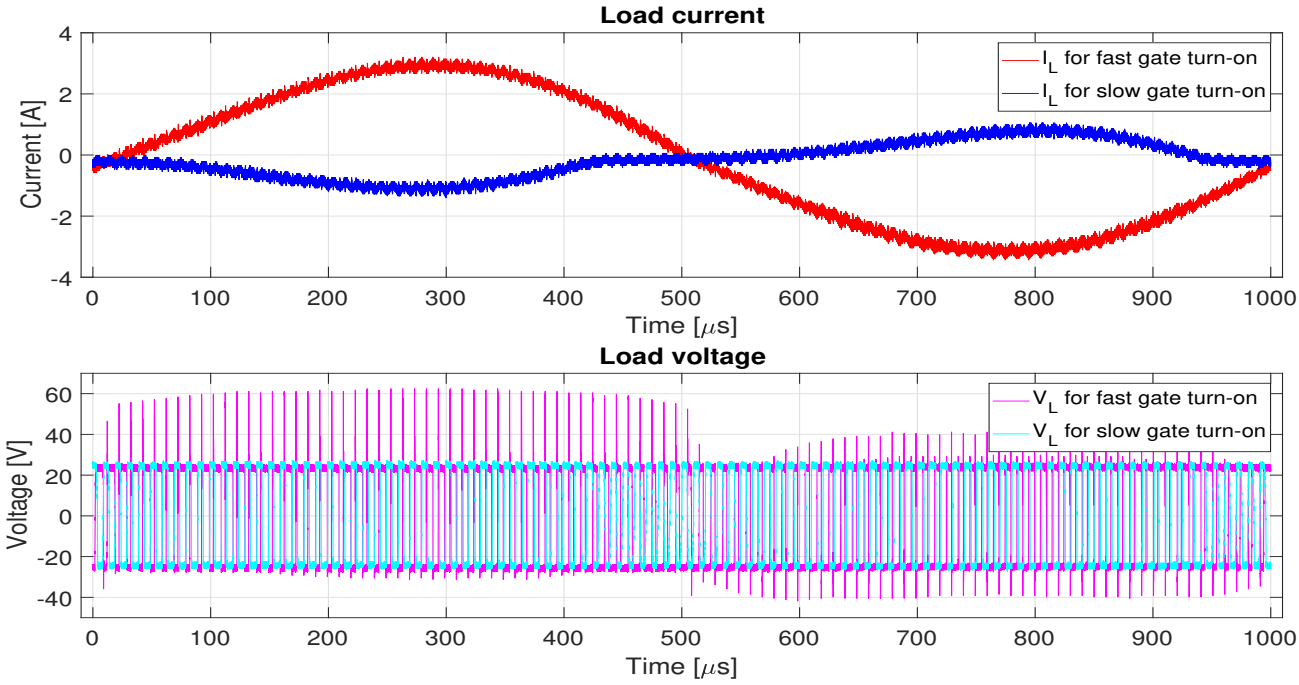


Figure 4.3: Load current and voltage during fast and slow gate turn-on at 100 kHz switching frequency.

The switching frequency was adjusted until the load current showed no visible sign of distortion. There is still some conduction time that is sacrificed, which leads to a lower peak amplitude of the current in the case of slow gate turn-on as opposed to the fast turn-on case however, this was accepted. At a frequency of around 55 kHz the current showed to not be distorted from its reference sine wave. Figure 4.4 shows the load current and load voltage in the different turn-on cases for 55 kHz. It can be observed that in both cases the current keeps its fundamental sine wave.

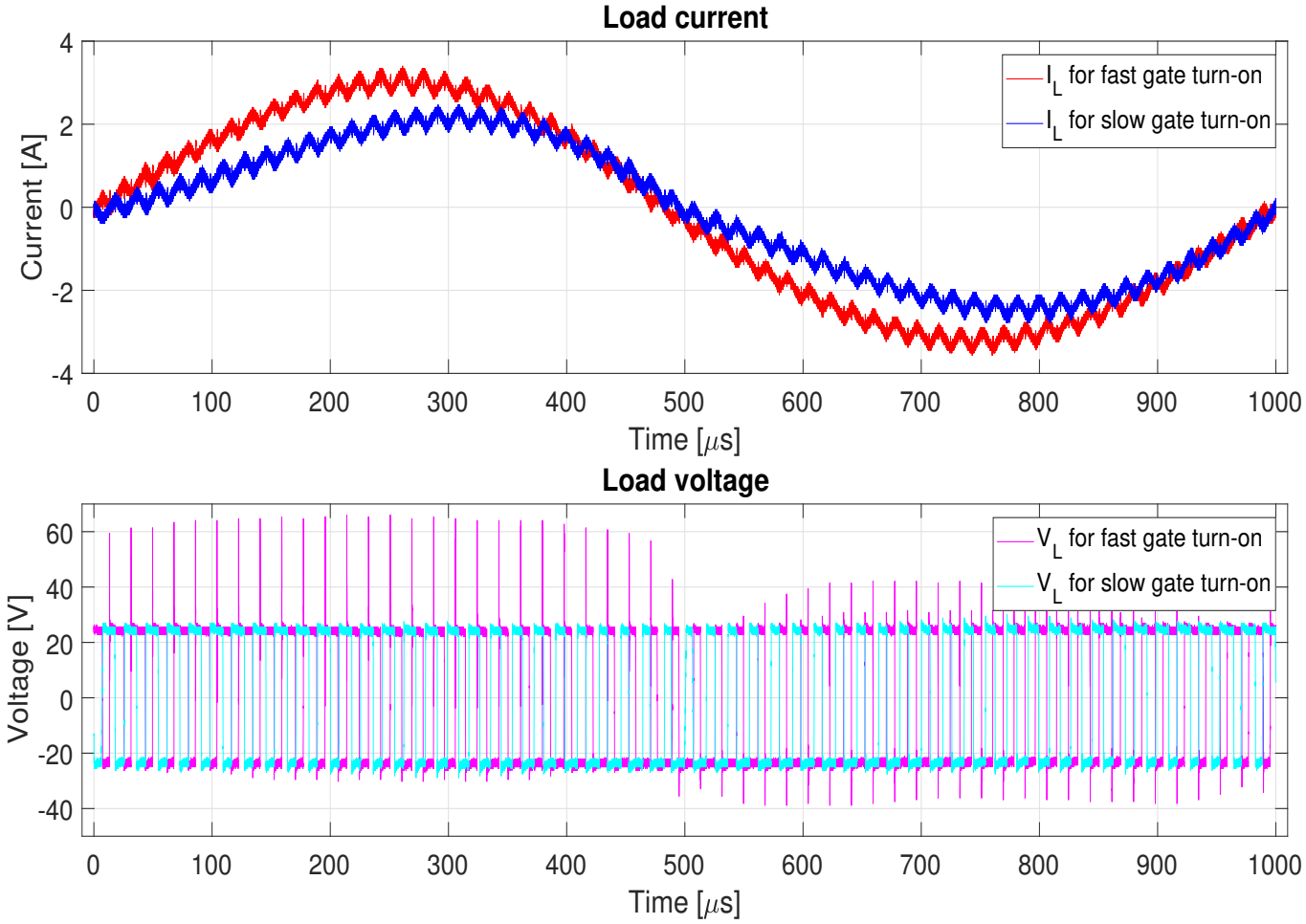


Figure 4.4: Load current and voltage during fast and slow gate turn-on at 55 kHz switching frequency.

Looking at the switching characteristics of the lower transistor at 55 kHz in fig. 4.5 shows us that V_{gs} manage to almost reach 10 V. Zooming in more in fig. 4.6 on the turn-on of these pulses and comparing them shows that the adjusted slew rate is working as intended and that V_{ds} has an increased time while decreasing. This still holds despite that the fast turn-on is delayed due to the ringing. Similar effect can be observed for turn-off in fig. 4.7.

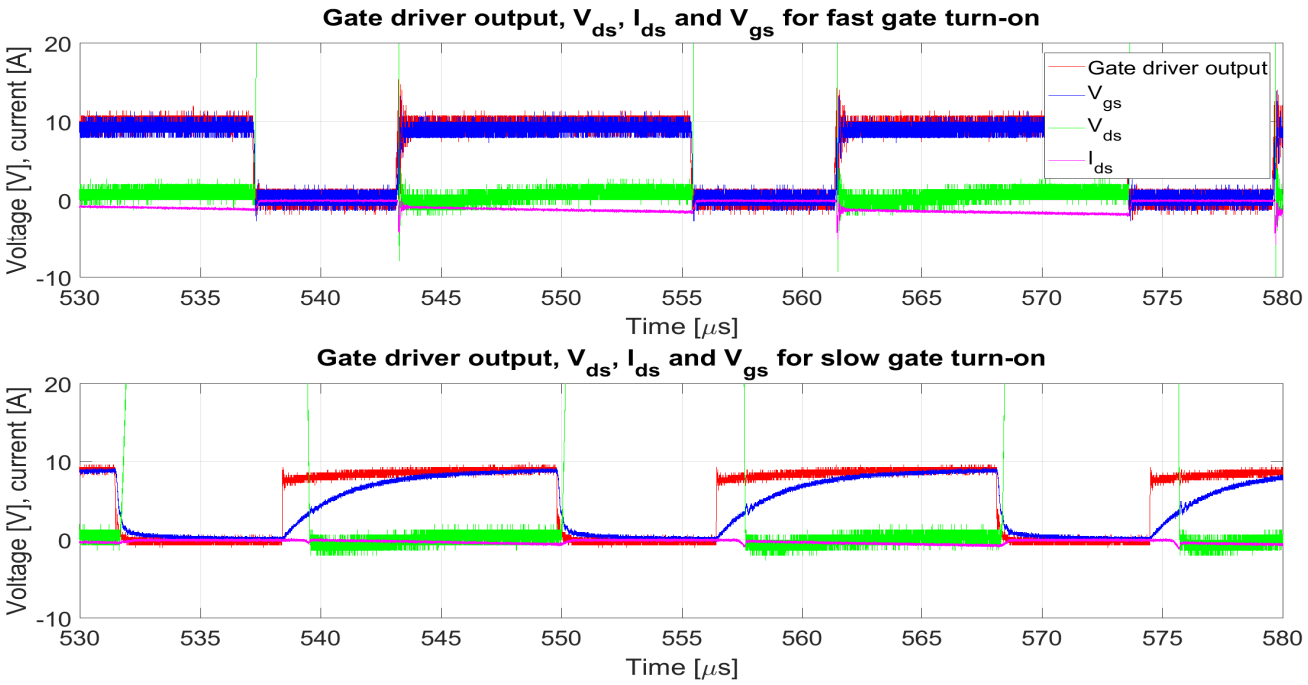


Figure 4.5: Zoom in on the lower transistor's switching waveforms in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 55 kHz switching frequency.

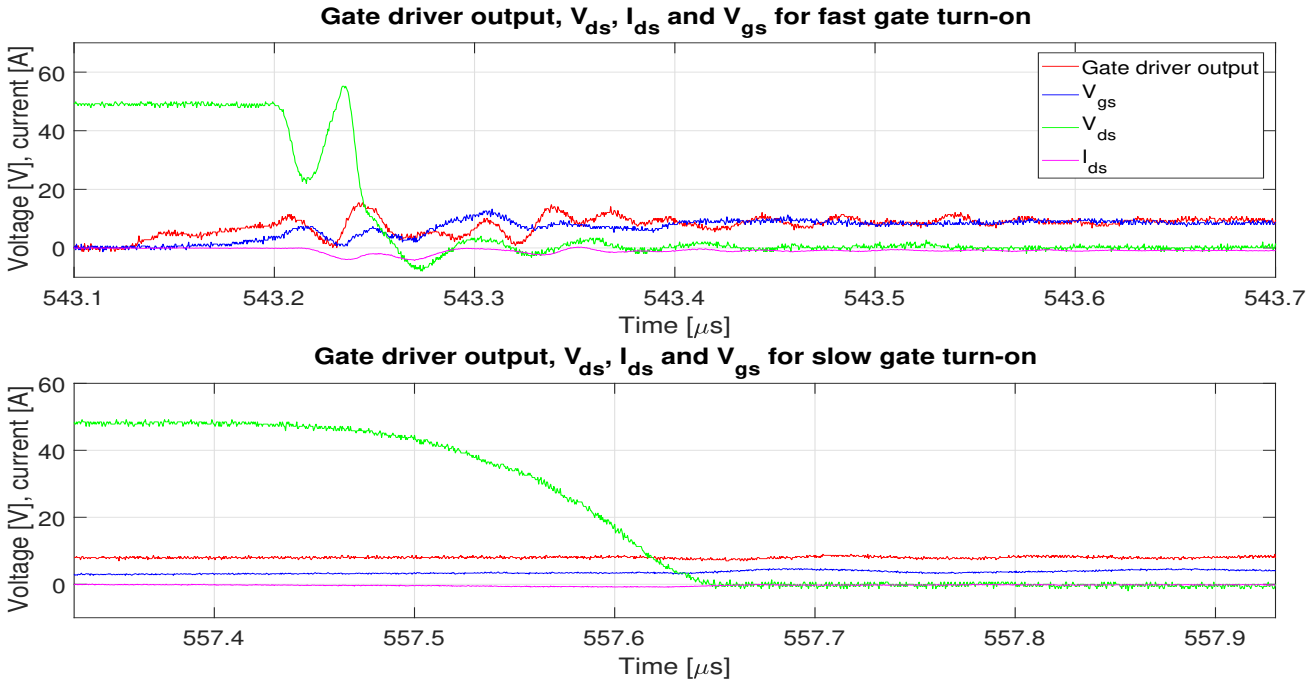


Figure 4.6: Zoom in on the lower transistor's turn-on in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 55 kHz switching frequency.

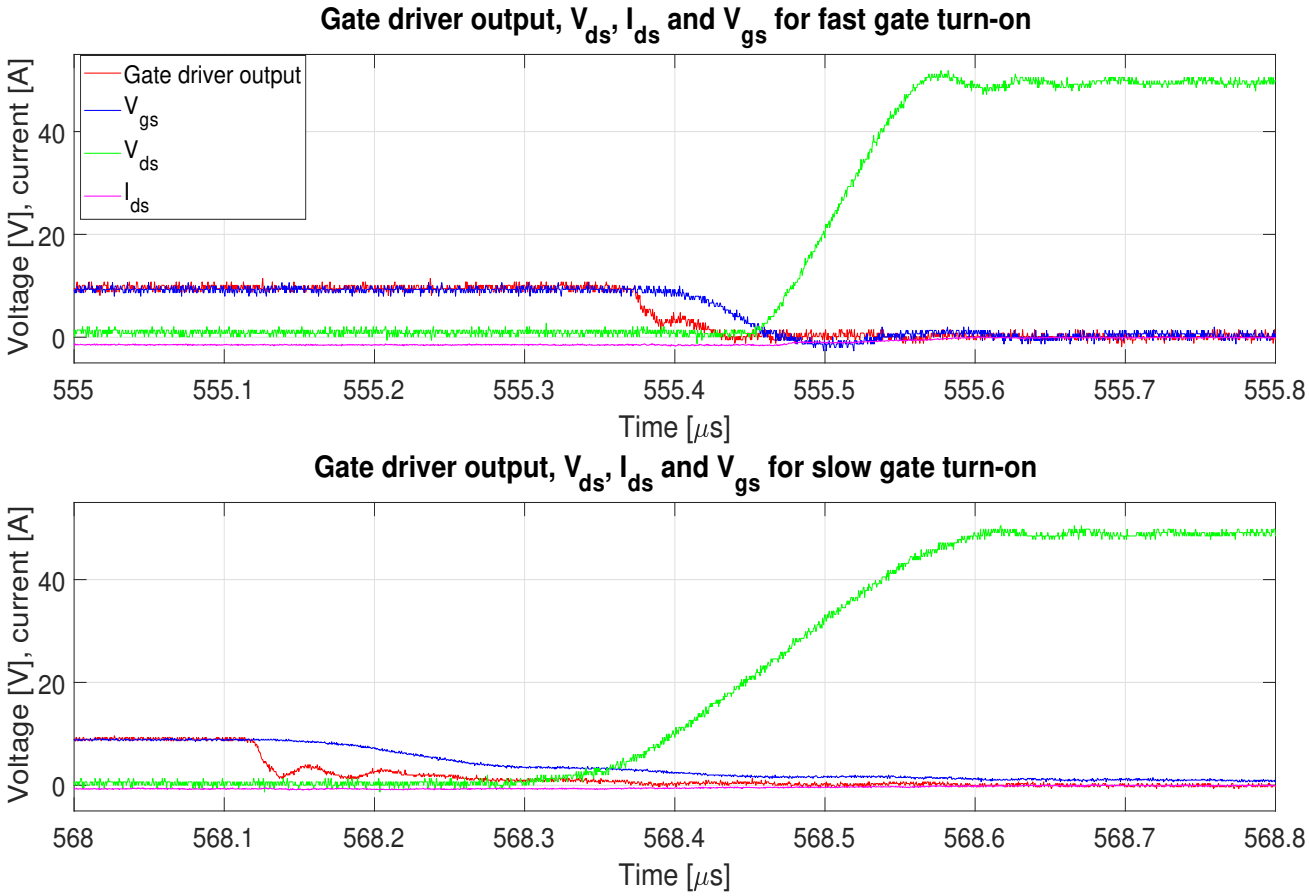


Figure 4.7: Zoom in on the lower transistor's turn-off in the case of fast gate turn-on (upper fig.) versus slow turn-on of the gate (lower fig.) at 55 kHz switching frequency.

Analyzing the case of operating the single phase half bridge at 55 kHz yielded the following results, in fig. 4.9 the losses for the transistor are presented with the theoretical calculations for each case calculated as in 2.2. The measured losses for fast gate turn-on are calculated to 5.21 W and for slow gate turn-on it is 2.53 W. For fast gate turn-on it was theoretically calculated to 1.18 W per transistor for one switching cycle. In the case of slow turn-on it was calculated to 1.39 W per transistor and switching cycle. Worth noting here is that the RMS current that was used to calculate these theoretical values are different since it is based on values from the respective measurements. As has been explained previously in this section, the slow gate turn-on resulted in a lower load current for the same modulation index. Therefore it should be remembered that these theoretical values compare poorly to each other but better to the measurements.

The measured power loss have been calculated using a cumulative sum in MATLAB and taking the absolute values of I_{ds} multiplied with the absolute of V_{ds}. There is quite a lot of discrepancy between the measured power loss and the theoretically calculated power loss which can be seen better in 4.9. A possible reason for this

is that the measurement of V_{ds} contains a lot of noise due to having to high V/div resolution on the oscilloscope. As can be seen in fig. 4.9, V_{ds} goes below zero quite a lot which would result in an increased power loss due to how the cumulative sum being calculated. The value it should have is $R_{ds,on}I_{ds,on}$ which should be in the order of 0.02 V, while measured it is around 10 times greater. This can be controlled by filtering the V_{ds} signal to see how much the cumulative sum differs if the voltage is changed to $R_{ds,on}I_{ds,on}$. Unfortunately, prototype 1 was broken during a short circuit when measuring and the error could not be fixed. However when this happened the PCB and new components for prototype 2 was being shipped hence, no significant effort was made to repair prototype 1 and redo these measurements.

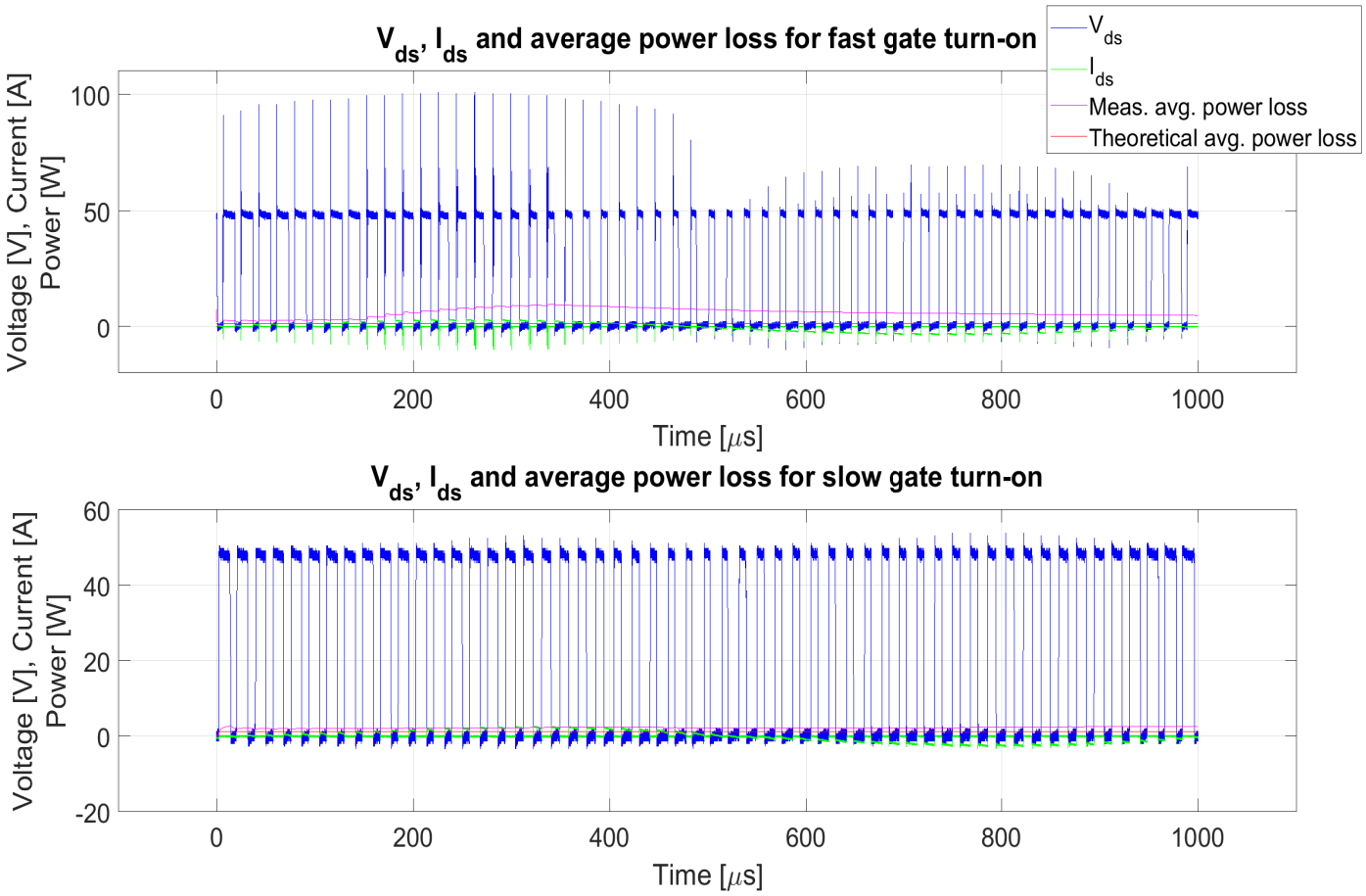


Figure 4.8: Graph of V_{ds}, I_{ds}, the average power loss measured and the average power loss calculated for 55 kHz.

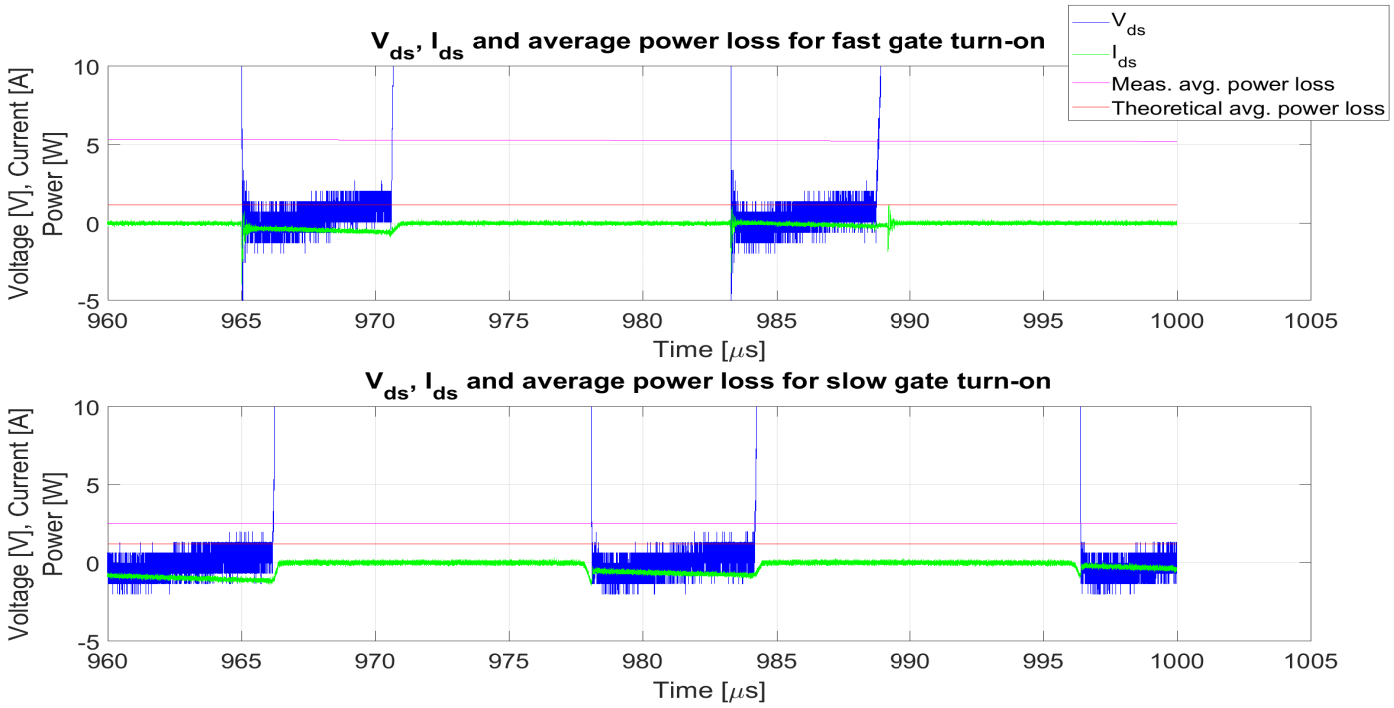


Figure 4.9: Graph of V_{ds}, I_{ds}, the average power loss measured and the average power loss calculated zoomed in.

Filtering the drain-to-source voltage, as explained above, with a simple if-statement in MATLAB yields the following figure seen below.

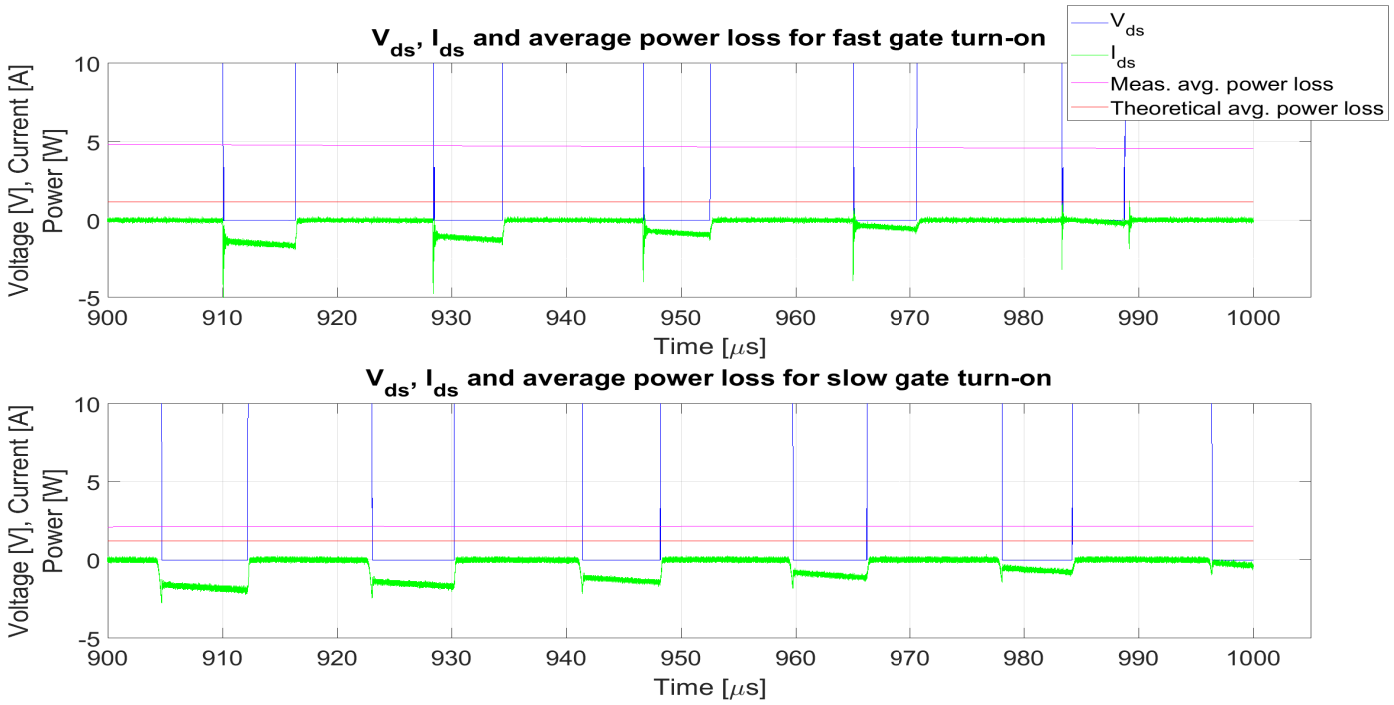


Figure 4.10: Graph of filtered V_{ds}, I_{ds}, the average power loss measured and the average power loss calculated zoomed in.

Figure 4.10 shows the same plots as in 4.9 but with V_{ds} being filtered. It is noticeable that for the slow turn-on of the gate the calculations are matching even better. In the case of fast turn-on, there is a slight change in favour of matching the calculations more however, there is still quite a lot of discrepancy. This is surprising that the fast turn-on contain more losses than the slow turn-on. This could be because of the big transients that are occuring in the fast turn-on case. A way to analyze if this holds true is to do a cumulative sum for a few switching periods when the current is at its peak, i.e. where the transients are the biggest.

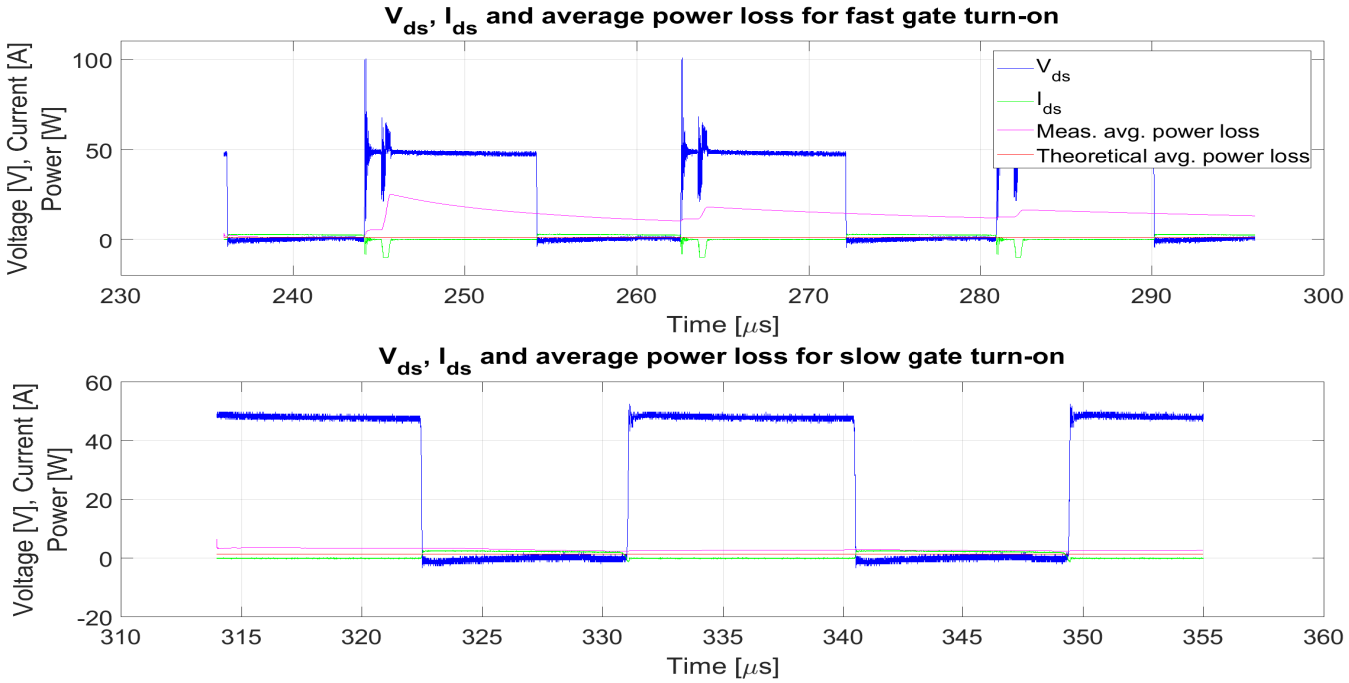


Figure 4.11: Graph of filtered V_{ds}, I_{ds}, the average power loss measured and the average power loss calculated zoomed in at the peak of the current.

In fig. 4.11 one can see that even when the V_{ds} voltage is filtered the measured power loss is significantly higher due to the transients when calculating for a few switching periods. The final value of the cumulative sum in fig. 4.11 for the fast turn-on is 12.78 W while for the slow turn-on it is 2.115 W. This shows that the transients have a much stronger impact than was first anticipated. This may very well be because of the poor construction of the single phase half bridge inverter and that it contains a lot of parasitic elements, such as inductive loops contributing to the ringing.

Something important to take into consideration when descreasing the frequency is the DC capacitor bank's capacitance size. In this first prototype, the DC bank consists of two parallel connected legs with two series connected capacitors of 470 μF each. The voltage over the the two upper and lower DC bank capacitors can be seen in fig. 4.12 with the load current and current through the lower DC capacitor also presented.

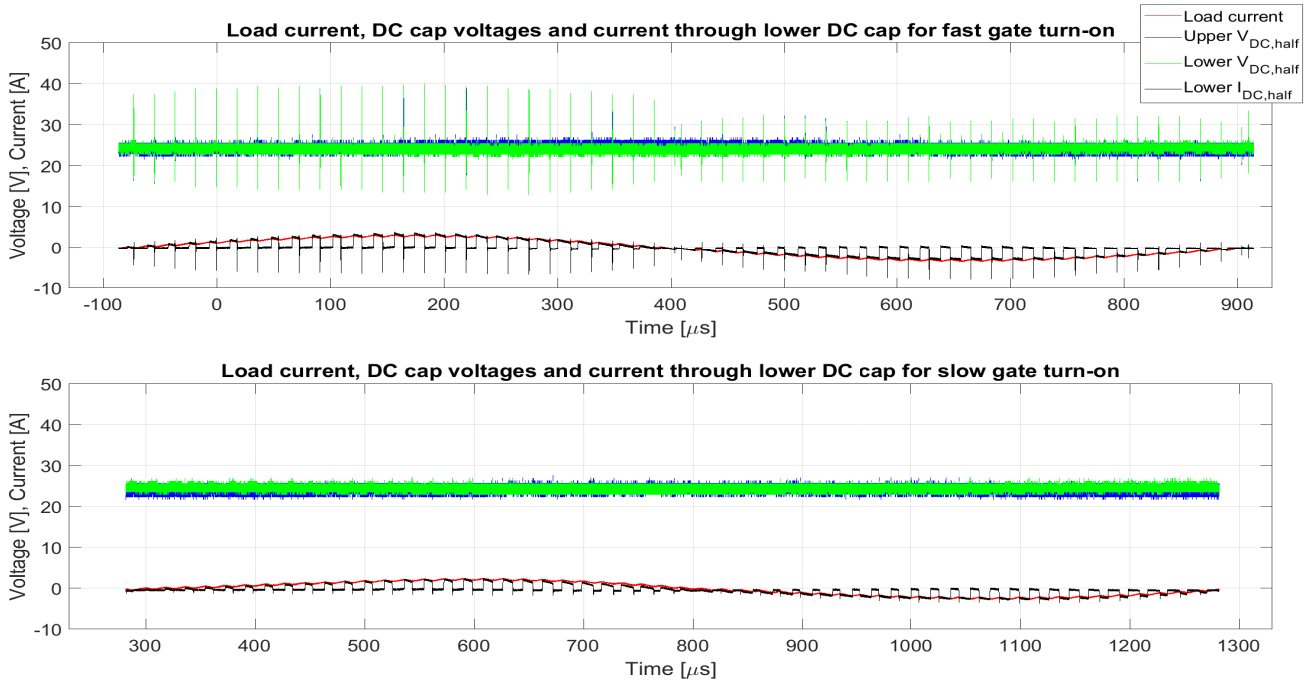


Figure 4.12: Graph of the voltage over the upper and lower part of the DC capacitor and the current through the load and the lower DC capacitor for fast turn-on (upper) and slow turn-on (lower).

This design was made to make sure the capacitance was sufficient and although no changes were ever made to change this, the fact that the capacitance is dependent on the frequency among other things is taken into consideration for the next prototype where volume will be minimized.

4.2 Results from Prototype 2

4.2.1 Optimization of DC capacitor bank

The next prototype board that is designed had space alloted for 11 electrolytic aluminium capacitors and 12 film or 36 ceramic capacitors, since these compete for the same space, from table 3.3. If the ceramic capcaitors are placed on their side, standing up, then there is a possibility to mount 72 of these capacitors onto the board. Since minimizing the total volume of the inverter is a crucial goal, it would be desirable to not use electrolytic capacitors due that even though they are energy dense, they have trouble handling high RMS currents which would lead to a great amount of volume being taken up by these. In table 4.1 the number of capacitors needed to meet the required capacitance at 100 kHz is presented together with different constraints, cost and volume using solely one type of capacitor from table 3.3. The RMS current that is required to be handled is also calculated at 100 kHz.

Table 4.1: Number of capacitors needed to satisfy capacitance and RMS current, with other important parameters presented as well, using only one type of capacitor.

	Film capacitor Kemet, 100 V **MDC10106K100A58P7TUBE**	**Ceramic capacitor TDK,** 100 V **C5750X7S2A156M250KB**	**Electrolytic capacitor Rubycon,** 100 V **100ZLJ330M12.5X35**
Nominal capacitance $[\mu F]$	*10*	*15*	*330*
Effective capacitance @ 48 V $[\mu F]$	*10*	*6.239*	*330*
No. of caps. needed to satisfy capacitance [-]	*14*	*21*	*1*
No. of caps. needed to not exceed current ripple [-]	*4*	*10*	*19*
I_{rms} **per capacitor*** $[A]$	*3.44*	*2.394*	*2.536*
Volume per unit $[cm^3]$	*3.213*	*0.0713*	*2.148*
Total Volume* $[cm^3]$	*44.98*	*1.496*	*40.8*
ESL per capacitor $[nH]$	*4*	*0.65*	*n/a*
Effective capacitance per volume* $[\mu F/cm^3]$	*3.113*	*87.57*	*153.7*
RMS current handling per volume* $[A/cm^3]$	*4.046*	*70.18*	*23*
Total losses $[mW]$	*31.3*	*16.66*	*895.7*
Cost per effective capacitance [€/μF]	*0.624*	*0.247*	*0.0026*

The reason for using 100 kHz instead of 55 kHz for the calculations in table 4.1 is because the second prototype can probably handle switching at 100 kHz much better due to having much less parasitic inductances.

Using the GAMS optimization software to generate a combination between these three types of capacitors based on the equations presented in 2.5 gives a solution to use 24 of the ceramic capacitor type. This is with regards to cost, volume and losses as can be seen in (2.22). Note that this program was implemented on short notice and was not very sophisticated hence, a lot of effort was required by the user when putting in parameters as well as interpreting the results. Due to this, it was noticed that film capacitors was not ideal due to size and cost and they were never included in an optimal solution. Because of this they were excluded from the optimization. Furthermore, with regards to how the resonant frequency change for ceramic capacitors, there is a risk of harmonics not being damped enough at frequencies of $0.5-2$ MHz since the high-capacitance ceramics acts as inductors at these frequencies. A way to prevent this error in design is to use ceramic capacitors of a lower capacitance which a much higher resonant frequency at these frequencies. Because of this reason a minimum limit of 12 smaller ceramic capacitors (2 for each

*This number is determined by the amount of capacitors that is needed to fulfill both the req. capacitance as well as RMS current handling.

transistor pair) were introduced to GAMS to optimize with. The smaller ceramic capacitor is presented in table 3.3 and replaced the film capacitor in the GAMS code.

The new suggestion from GAMS gives the combination of 12 small ceramic capacitors of 0.47 μF and 24 big ceramic capacitors of 15 μF. This would according to GAMS result in a total capacitance of 189.4 μF, a total volume of 2.1 cm^3, a cost of 40.9 € (if the capacitors a bought in bulk of 1000) and a total power loss of 300.4 mW.

The equations presented in section 2.5 are used to create the following plots assuming that the modulation index m_a is equal to 0.8 which yields the highest ripple current according to [14] and calculating a power factor of around 86.6% for the dummy load.

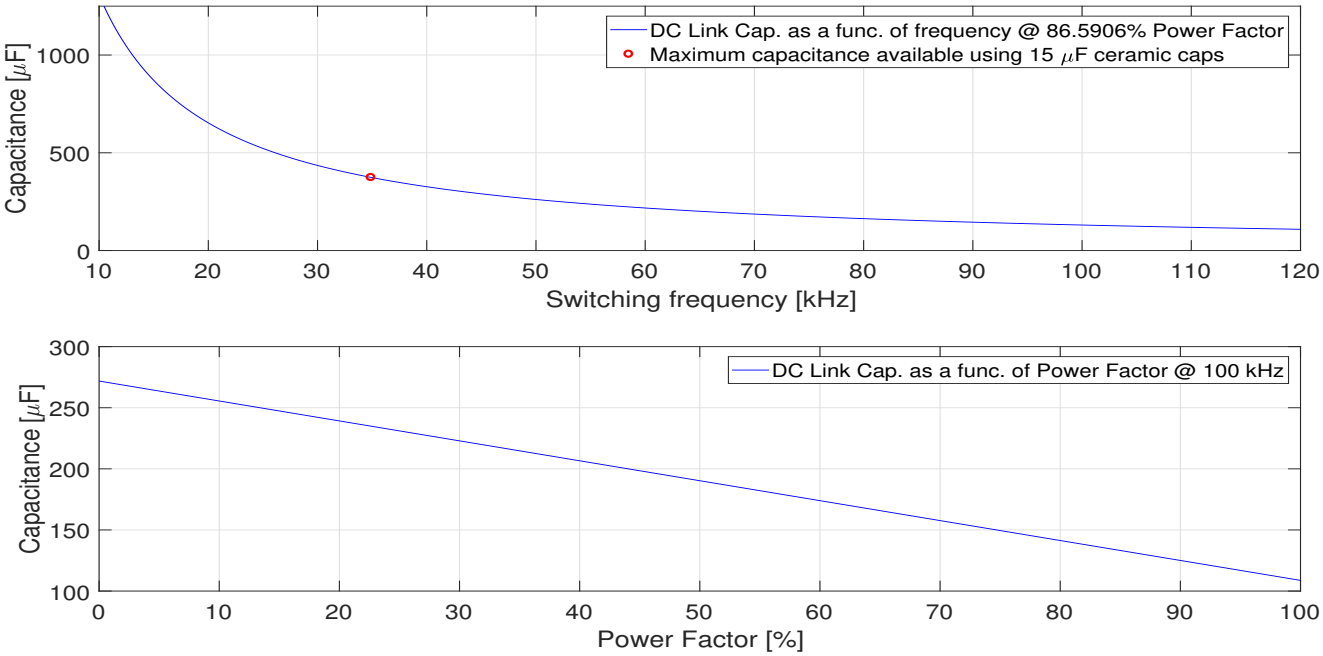


Figure 4.13: DC bank capacitor needed as a function of frequency (upper fig.) and DC bank capacitor needed as a function of power factor (lower fig.) at 100 kHz.

In fig. 4.13 the red circle in the upper figure marks the maximum available capacitance of 374.34 μF on the PCB board if 60 ceramic capacitors would be utilized with the larger ceramic capacitor presented in table 3.3. The capacitance from the smaller ceramic capacitors that is used can be neglected. The reason for why it is not 900 μF is due to that the DC voltage bias lowers the effective capacitance value from 15 μF to around 6.239 μF. This means that in order to have enough capacitance while not using any electrolytic capacitors a swithcing frequency above 35 kHz has to be achieved. Therefore, the slow turn-on of the gate can be utilized for prototype 2 at a frequency above 35 kHz while satisfying the capacitance needed for a voltage ripple no greater than 5% of the battery voltage.

4.2.2 Performance and losses

With the construction of prototype two complete and verified that it works, the following measurement was initially carried out and investigated. Switching frequency was set to 100 kHz and the fundamental frequency was 100 Hz, modulation index was increased until a peak current of around 64 A was reached for phase A load current. The slew rate circuit had a turn-on resistor of 20 Ω installed and turn-off resistor with a value of 1 Ω. The PCB with the MOSFETs on them had a capacitor of 3.3 nF and a resistor of 3.3 Ω mounted by soldering. In fig. 4.14 the three phases are presented with load current and a track of V_{ds} plotted. This track function is available on the oscilloscope that was used for observing the signals. It is a function that traces a signal and demodulates it.

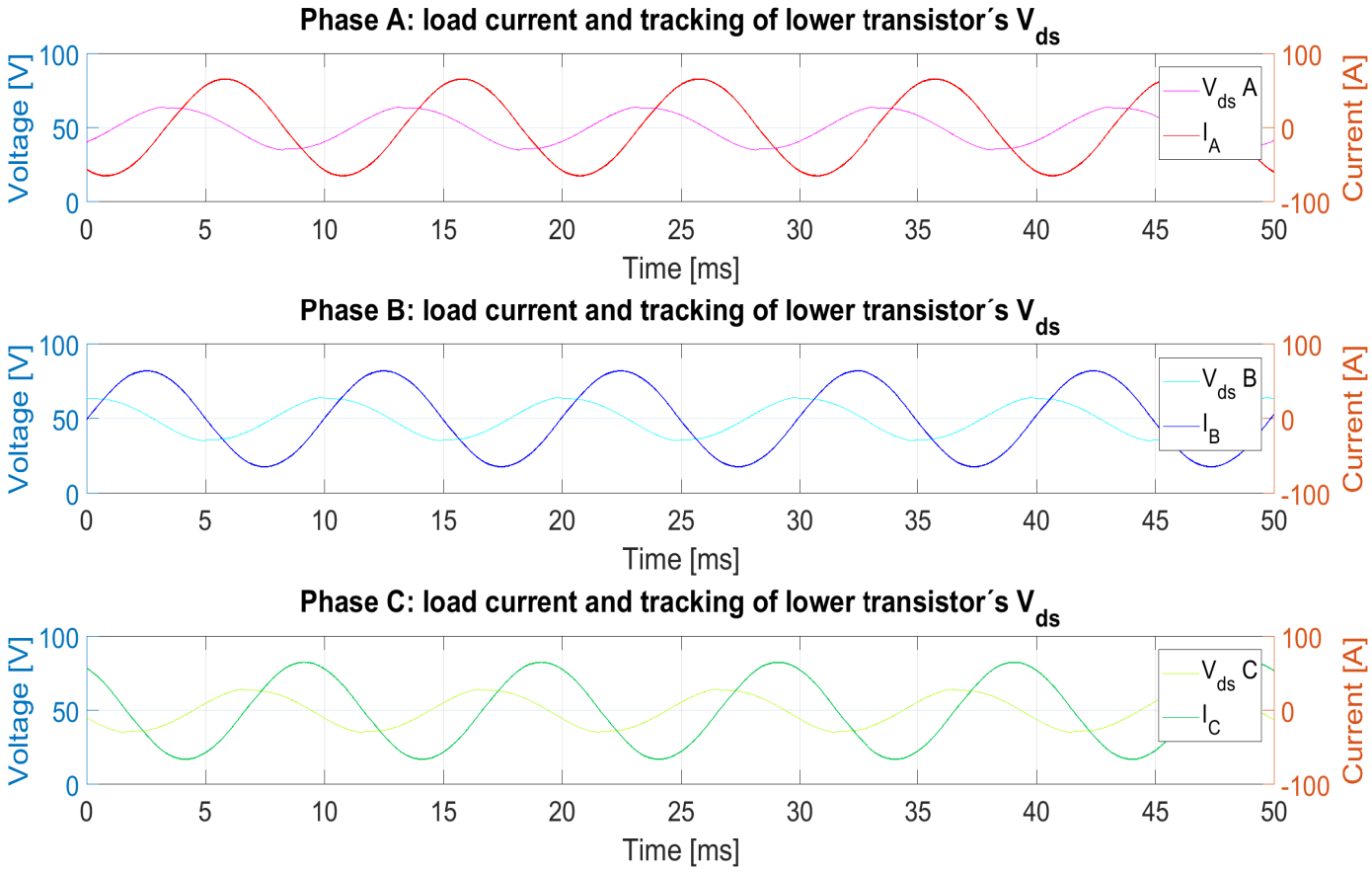


Figure 4.14: Load current and track of V_{ds} presented for each phase with a switching frequency of 100 kHz and a fundamental frequency of 100 Hz.

An example of how the original V_{ds} signal for each phase looked like can be seen in fig. 4.15 where V_{ds} is enlarged in fig. 4.16

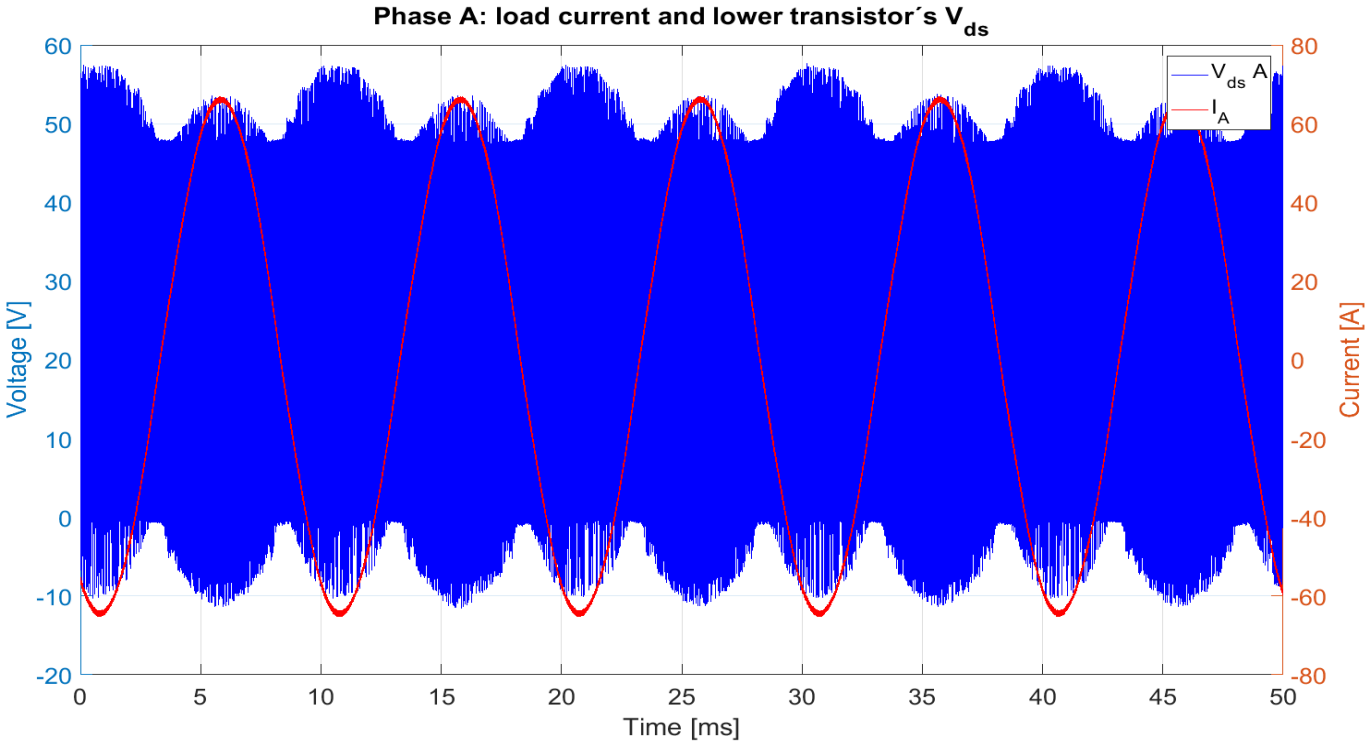


Figure 4.15: Load current and V_{ds} of phase A.

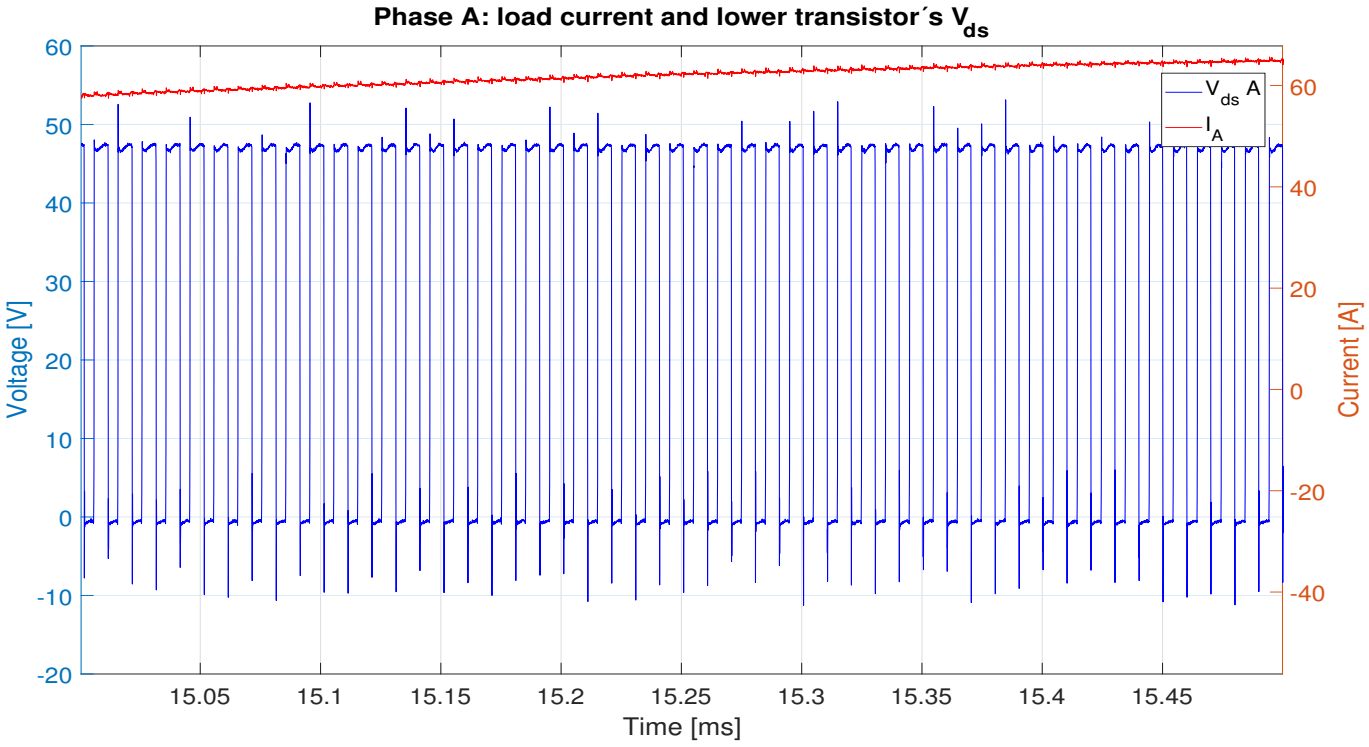


Figure 4.16: Zoom in of the load current and V_{ds} of phase A.

Figure 4.14 confirms that the inverter is working as intended as well as the control and generation of the PWM. Even though GAMS is used for an optimized DC capacitor bank that was presented in 4.2.1 this inverter had as many ceramic capacitor mounted on it as possible. Measurements of the input current and voltage is presented in 4.17 and shows that the voltage is varying within 3.13% of 48 V. The input current however posses quite a high relative ripple.

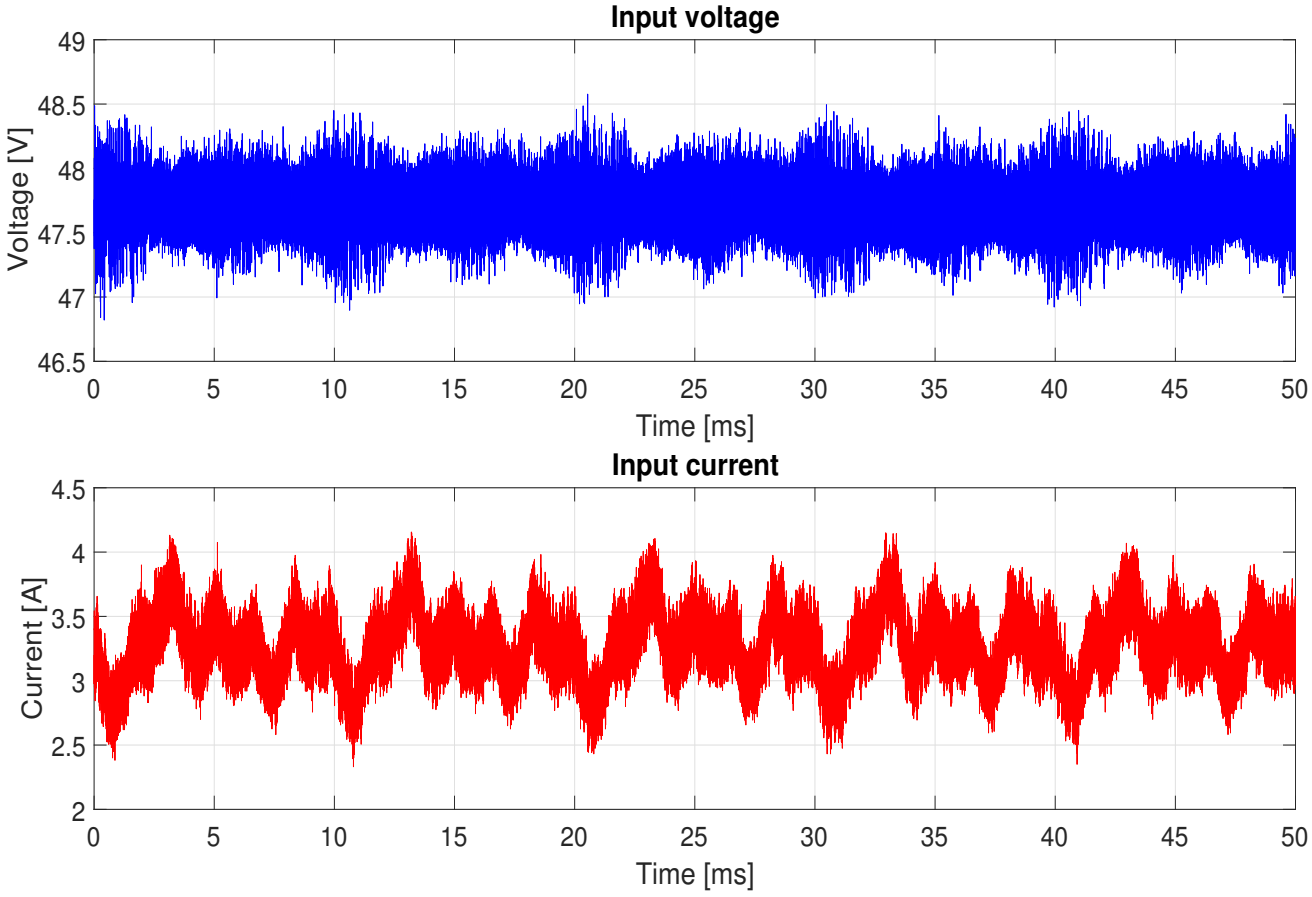


Figure 4.17: Input voltage and current from the power supply to inverter.

Observing the switching waveforms of the transistor in fig. 4.18 shows that there is quite a lot of ripple present, especially on V_{ds}. This zoom in is when the load current was at its peak value of around 64 A. For some reason, in this measurement the gate input signal seems to have become distorted and have a negative offset introduced to it. Why this happened is unknown and due to time limit, this measurement could not be repeated but it is quite possible that the negative end of the differential probe was not attached correctly.

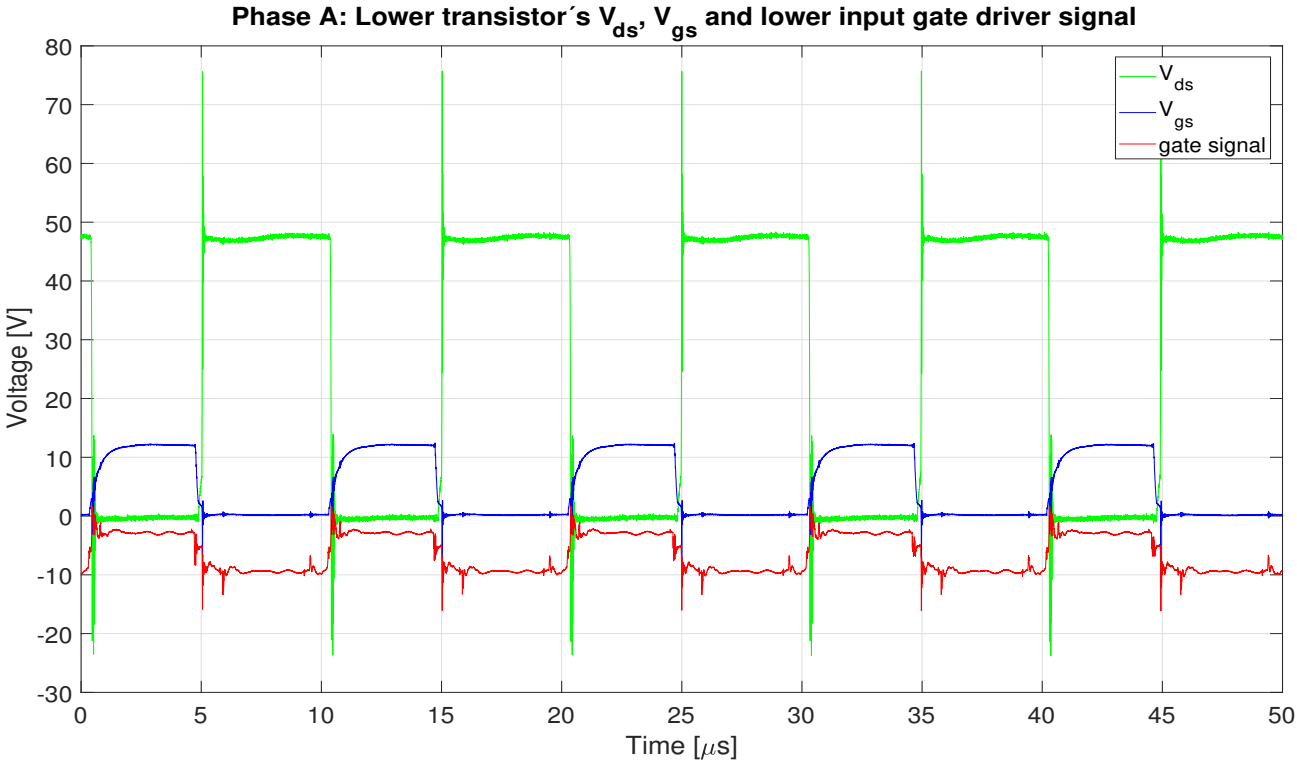
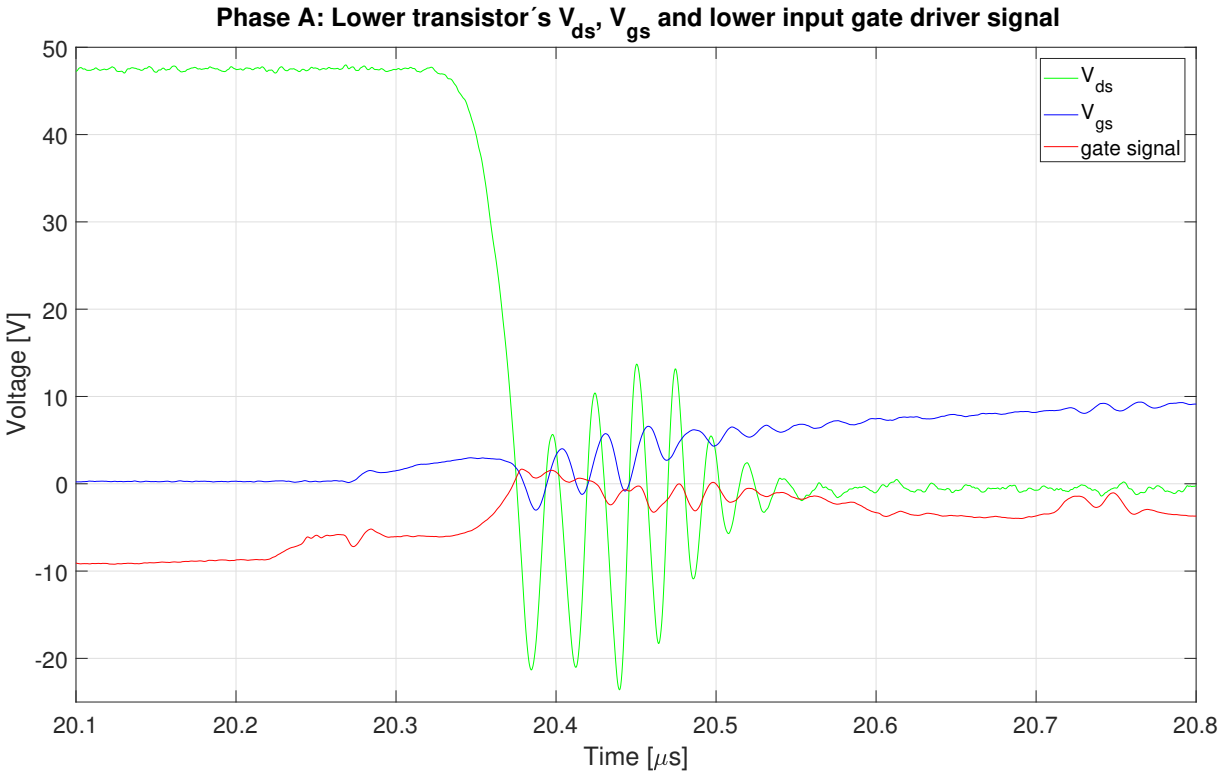
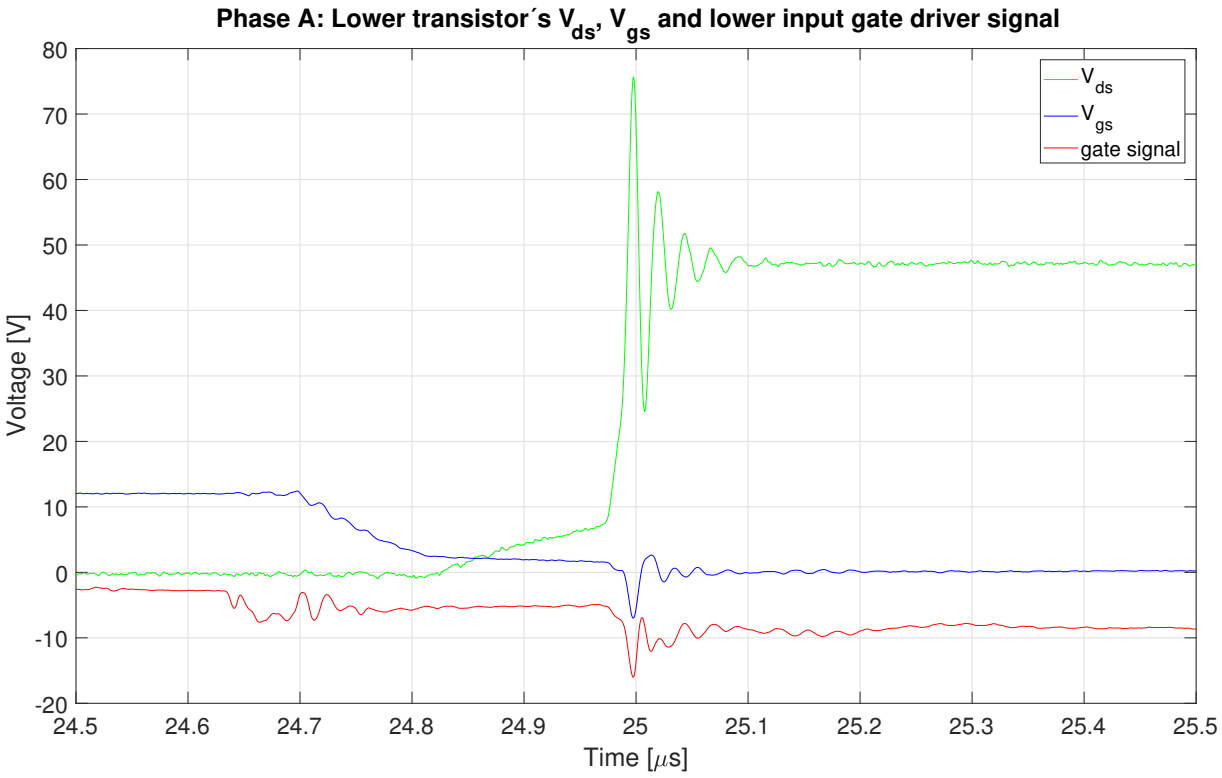


Figure 4.18: Switching characteristics of the lower transistor of phase A leg. V_{ds}, V_{gs} and gate driver signal present.

Enlarging fig. 4.18 to view the turn-on and turn-off periods more in detail shows that there is a high frequency ripple present on V_{ds}, V_{gs} and the gate driver signal when turning on and off. In the turn-off scenario it is however damped much faster. The frequency of the ringing during turn-on is calculated to 37.3 MHz while for turn-off it is calculated to 44.6 MHz.



(a) Zoom in on turn-on of transistor with V_{ds}, V_{gs} and gate driver signal present.



(b) Zoom in on turn-off of transistor with V_{ds}, V_{gs} and gate driver signal present.

Figure 4.19: Zoom in on turn-on and turn-off of lower transistor with V_{ds}, V_{gs} and gate driver signal present.

An attempt to damp these oscillations was made by adjusting the slew rate circuit. The turn-on resistor's value was increased to 56 Ω and a capacitance was added between gate and source with the value of 3.3 nF. Therefore, the following measurements have a slew rate circuit with the following parameters: Turn-on resistance of 59.3 Ω, Turn-off resistance of 4.3 Ω and external capacitance of 6.6 nF. Again, the zoom in of the following figures are when the modulation index is adjusted to reach a load current of around 64 A.

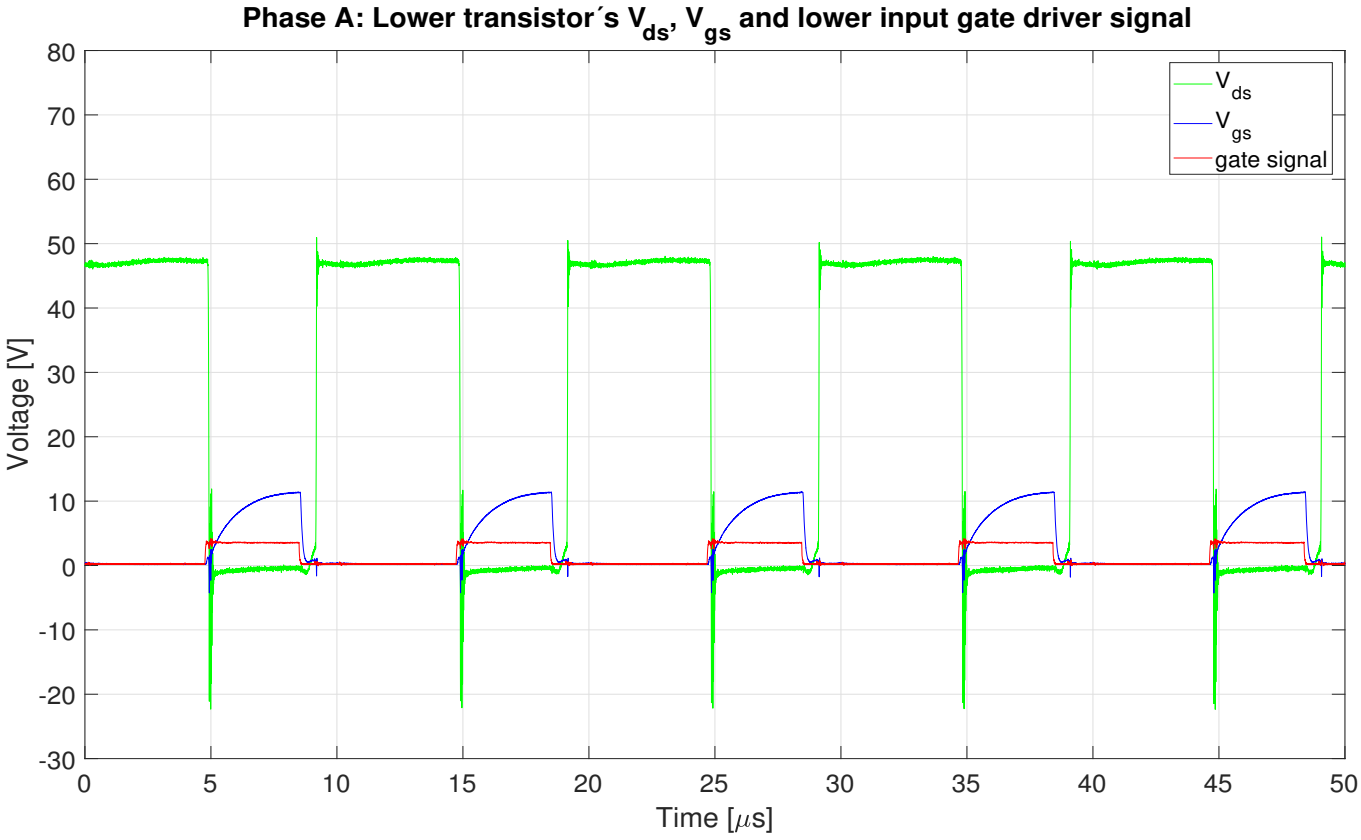
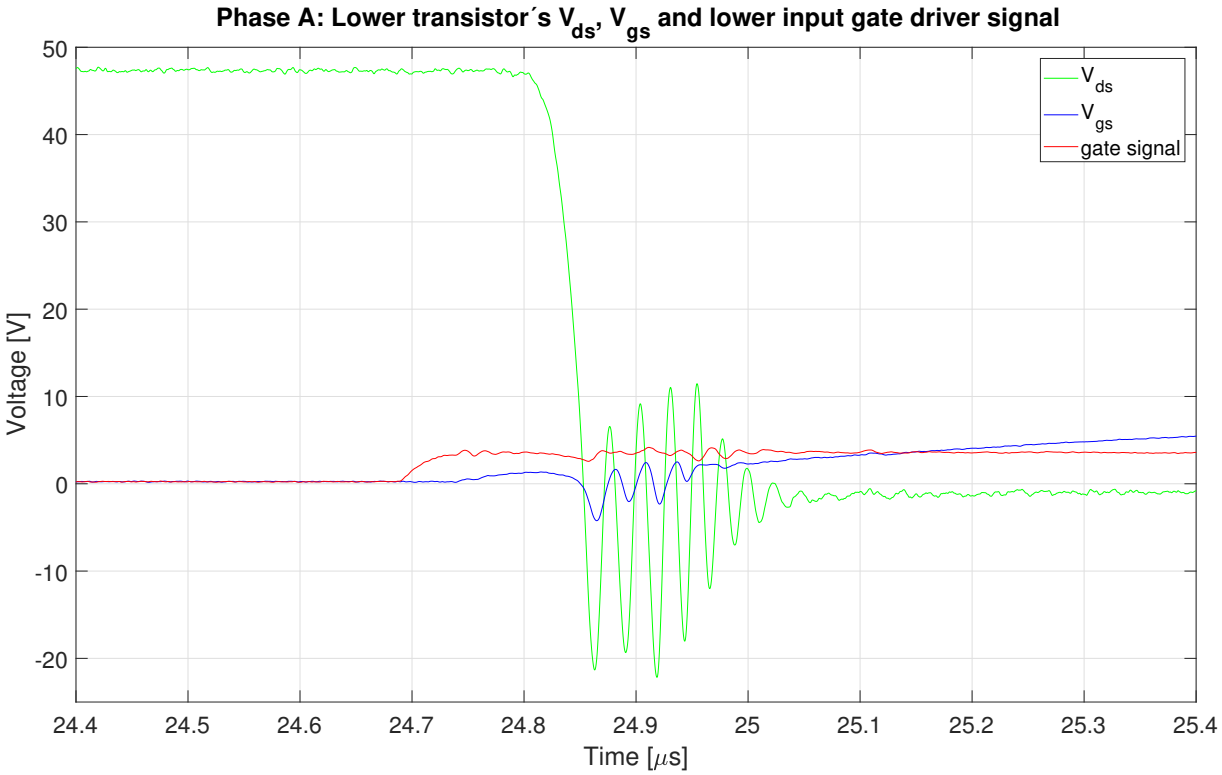
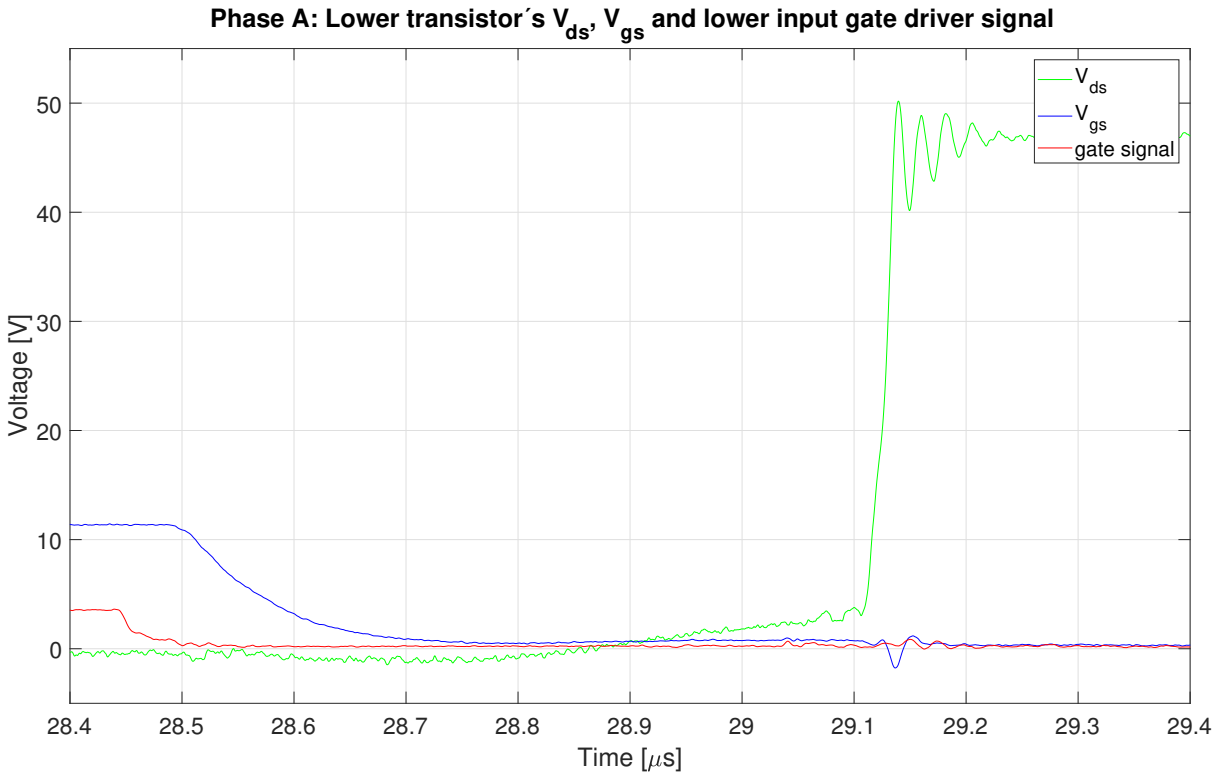


Figure 4.20: Switching characteristics of the lower transistor of phase A leg with the slew rate circuit changed. V_{ds}, V_{gs} and gate driver signal present.



(a) Zoom in on turn-on of transistor with V_{ds}, V_{gs} and gate driver signal present.



(b) Zoom in on turn-off of transistor with V_{ds}, V_{gs} and gate driver signal present.

Figure 4.21: Zoom in on turn-on and turn-off of lower transistor with V_{ds}, V_{gs} and gate driver signal present when the slew rate has been adjusted.

As can be seen in fig. 4.21b the oscillations during turn-off are damped significantly but for turn-on there is barely any difference as can be seen in fig. 4.21a. Why this is the case is not known but another attempt at increasing the slew rate was made. To be able to increase the slew rate more and still have the transistors turn on properly the switching frequency was lowered to 50 kHz and the slew rate circuit changed so that the turn-on resistor's value changed to 100 Ω and the external gate to source capacitor was changed to 6.8 nF. A total turn-on resistance of 103.3 Ω and gate to source capacitance of 10.1 nF was implemented for the following measurements. The following measurement are shown for when the peak load current in phase A is around 64 A.

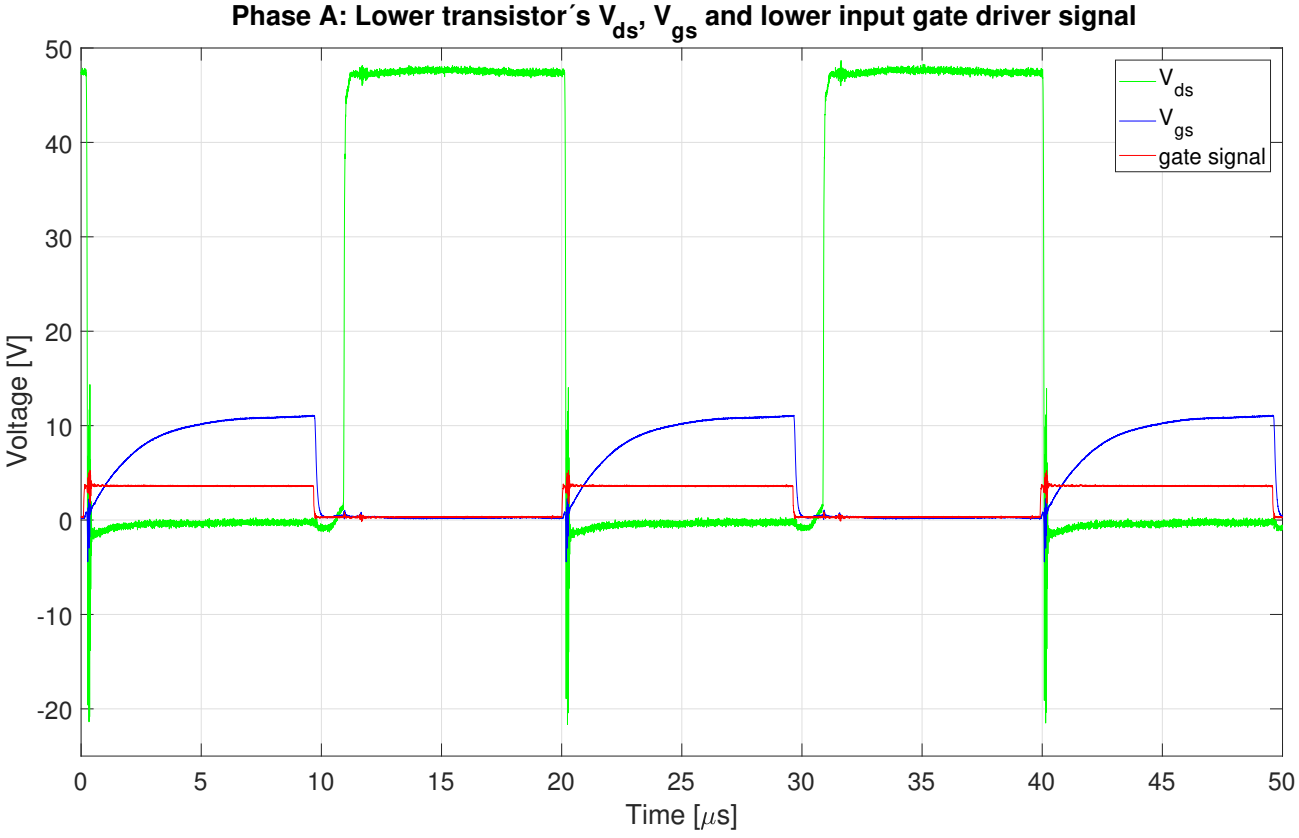
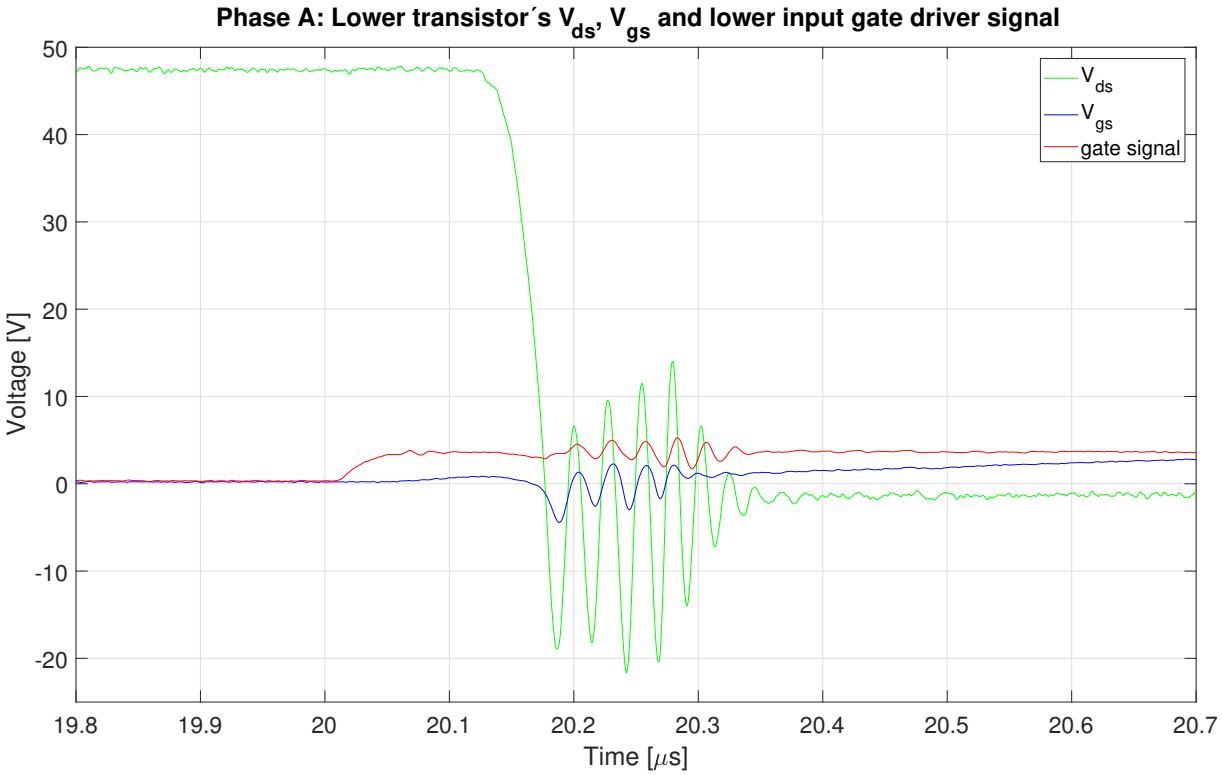
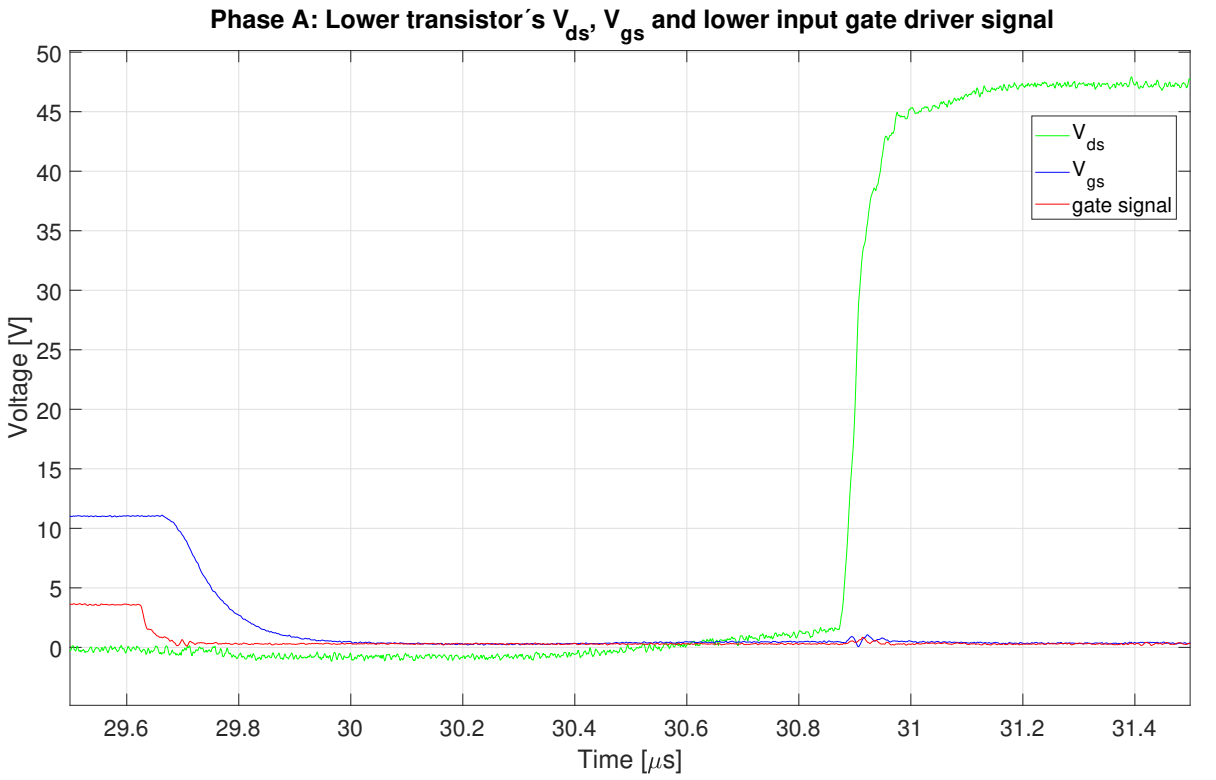


Figure 4.22: Switching characteristics of the lower transistor of phase A leg with the slew rate circuit changed and frequency lowered to 50 kHz. V_{ds}, V_{gs} and gate driver signal present.



(a) Zoom in on turn-on of transistor with V_{ds}, V_{gs} and gate driver signal present.



(b) Zoom in on turn-off of transistor with V_{ds}, V_{gs} and gate driver signal present.

Figure 4.23: Zoom in on turn-on and turn-off of lower transistor with V_{ds}, V_{gs} and gate driver signal present when the slew rate has been adjusted and switching frequency decreased.

It can be seen that lowering the frequency in order to increase the slew rate gives even more damping when turning the transistor off, as can be seen in fig. 4.23b. However, in fig. 4.23a one can see that the turn-on oscillations are still present and has not been damped in any significant way. To confirm that the inverter is still working properly at this frequency, the load currents and track of V_{ds} has been presented in fig. 4.24 as well as the input voltage and current in fig. 4.25.

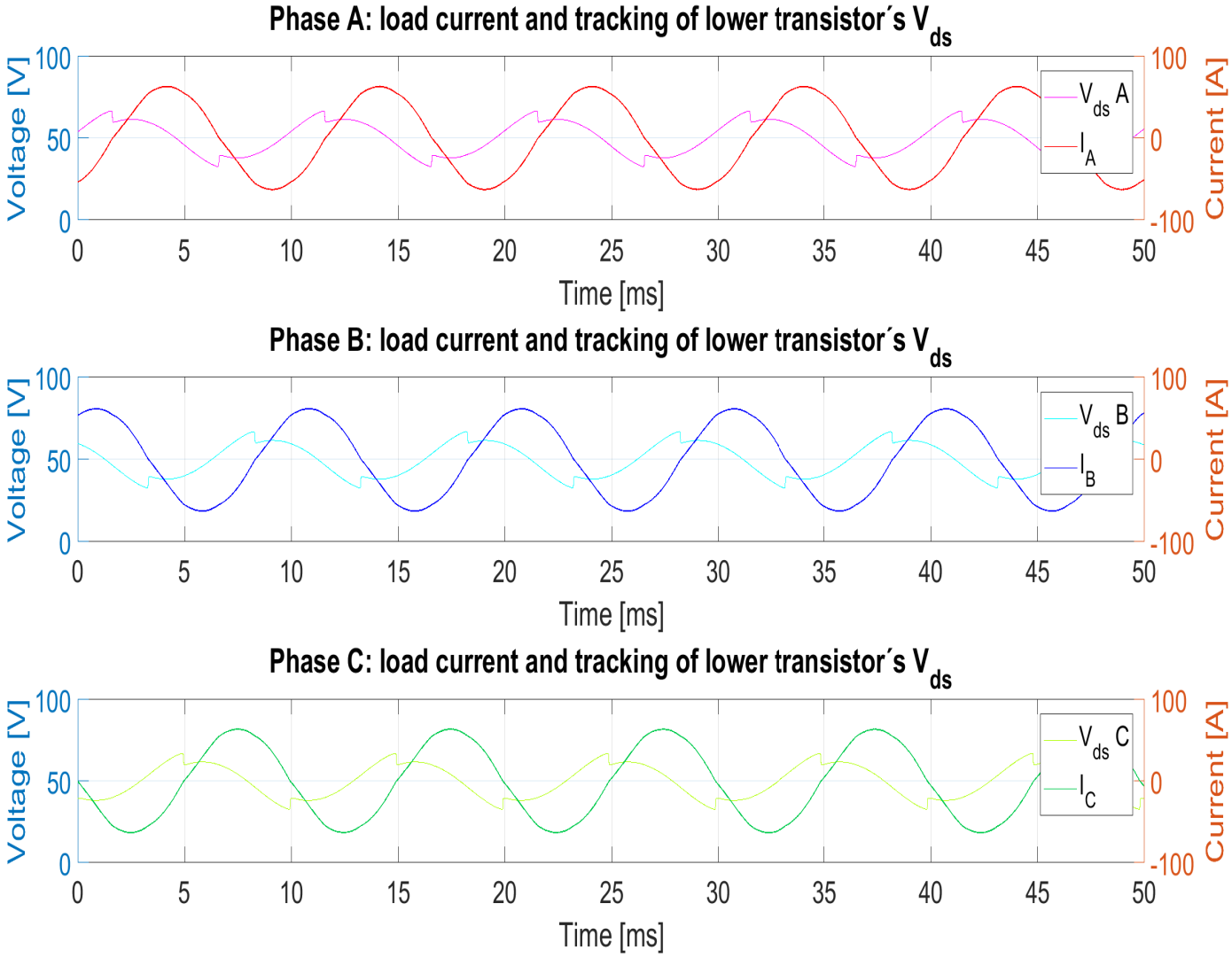


Figure 4.24: All three phases load current and track of V_{ds} for 50 kHz switching frequency.

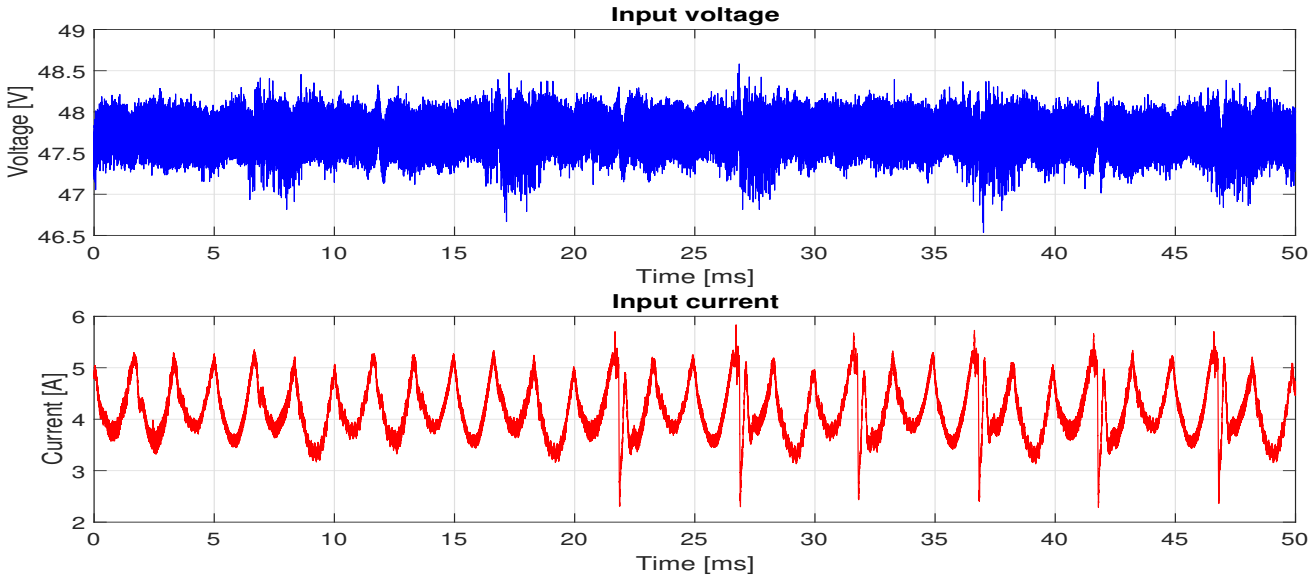


Figure 4.25: Input current and voltage at 50 kHz and adjusted slew rate.

One last attempt to damp the oscillations during turn-on were made by increasing the turn-off resistance with 3.5 Ω see if there would be any change. The following measurements presented below are carried out at a switching frequency of 50 kHz, turn-on resistance of 103.3 Ω, turn-off resistance of 6.8 Ω and a gate to source capacitance of 10.1 nF.

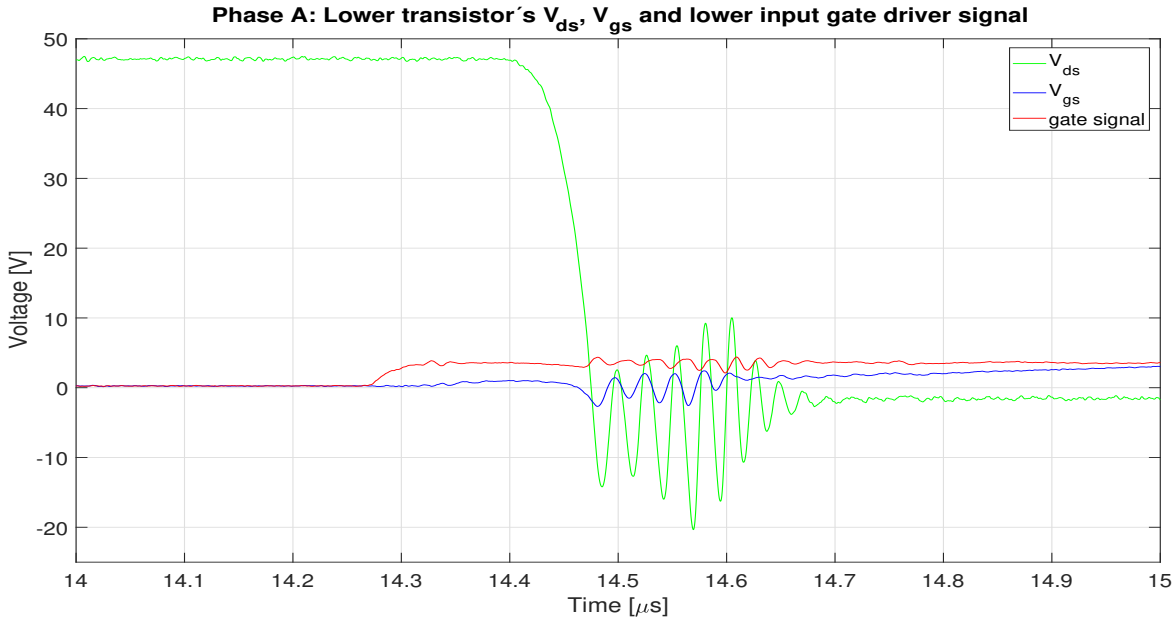


Figure 4.26: Zoom in on turn-on of transistor with V_{ds}, V_{gs} and gate driver signal present when the turn-off resistor has been increased.

Again there is no change in dampening the oscillations during turn-on as can be seen in fig. 4.26.

4.2.3 Efficiency of Prototype 2

By measuring the input power from the power supply and load current as well as voltage over the load for each phase the total efficiency of the inverter could be investigated. In fig. 4.27 the average and instantaneous efficiency can be seen for the inverter in the case of a switching frequency of 50 kHz and with the slowest slew rate installed as was presented in the previous section. This efficiency is very low but that is due to that there is no back EMF in the load which would generate high active power.

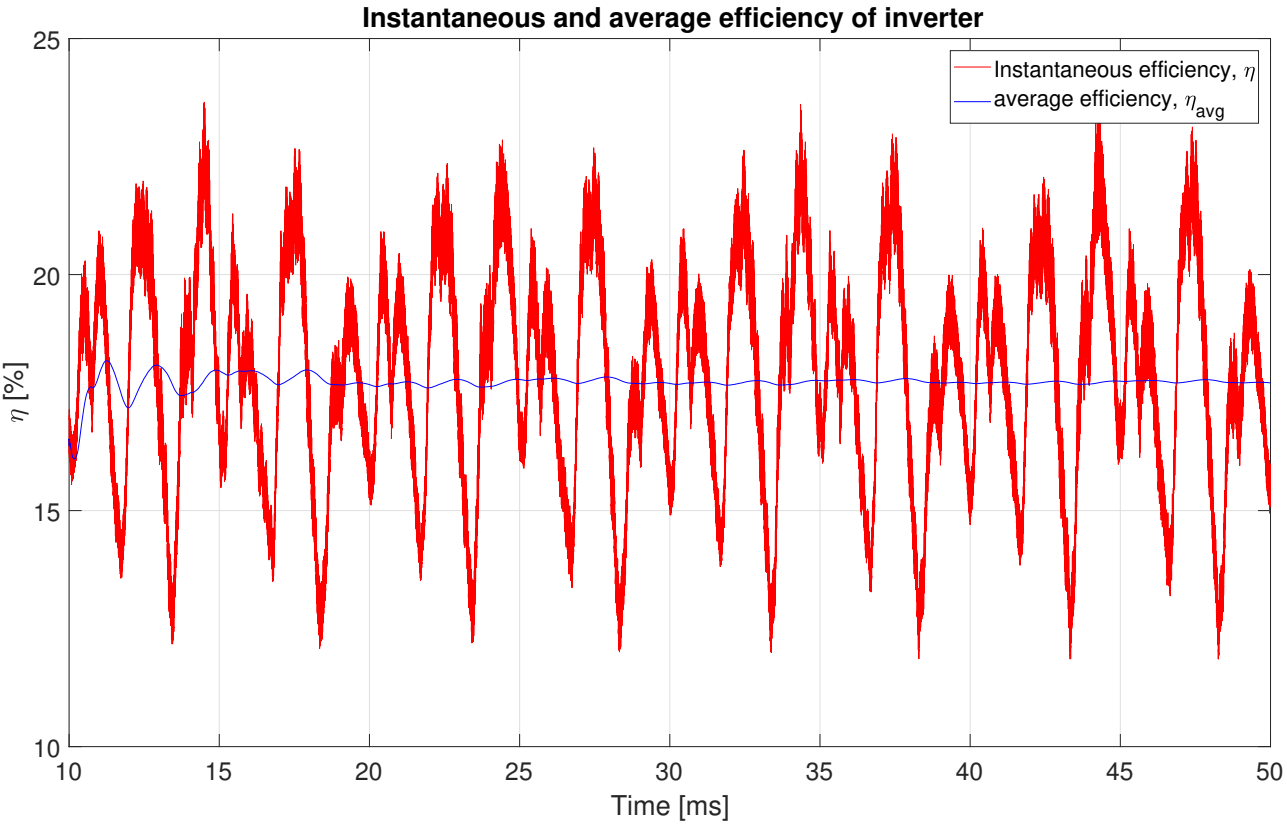


Figure 4.27: Instantaneous and average efficiency for the inverter.

Additionally, the reactive power is very high as can be seen in fig. 4.28 compared to the active power as can be seen in fig. 4.29 since the resistance is very low in the load. Furthermore, the apparent power is shown as well in fig. 4.30.

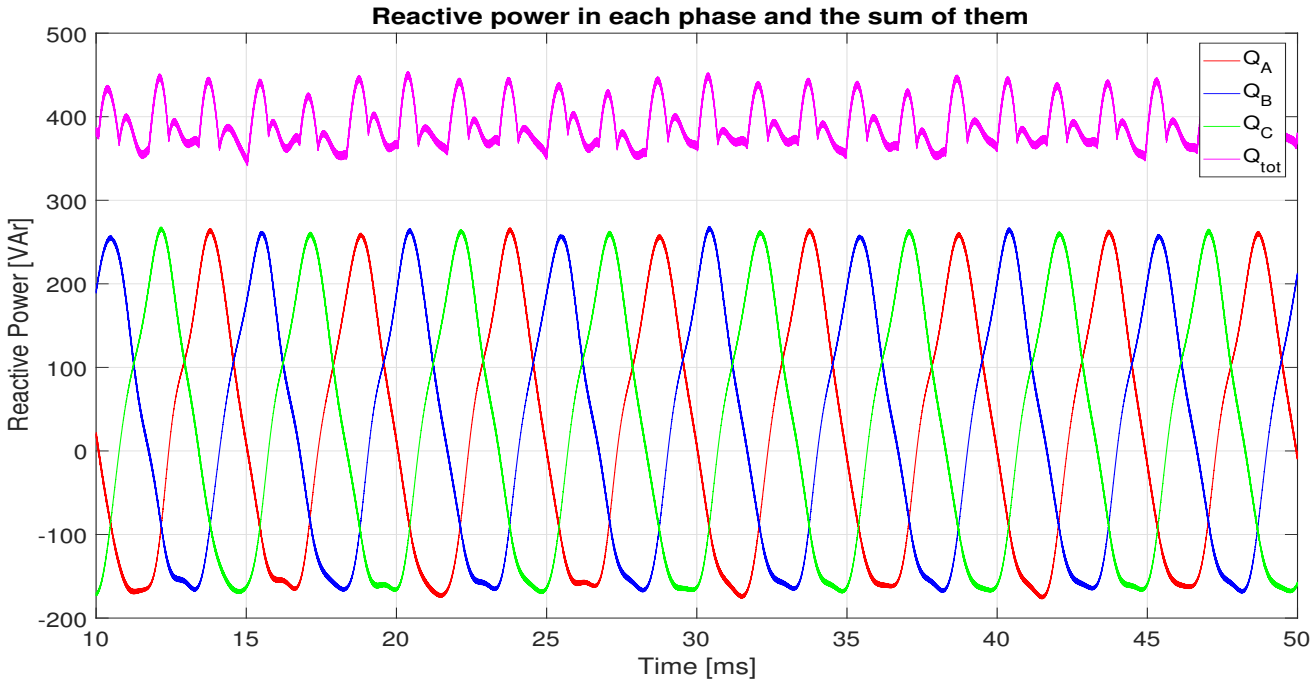


Figure 4.28: Reactive power for each phase and the sum of the reactive output power.

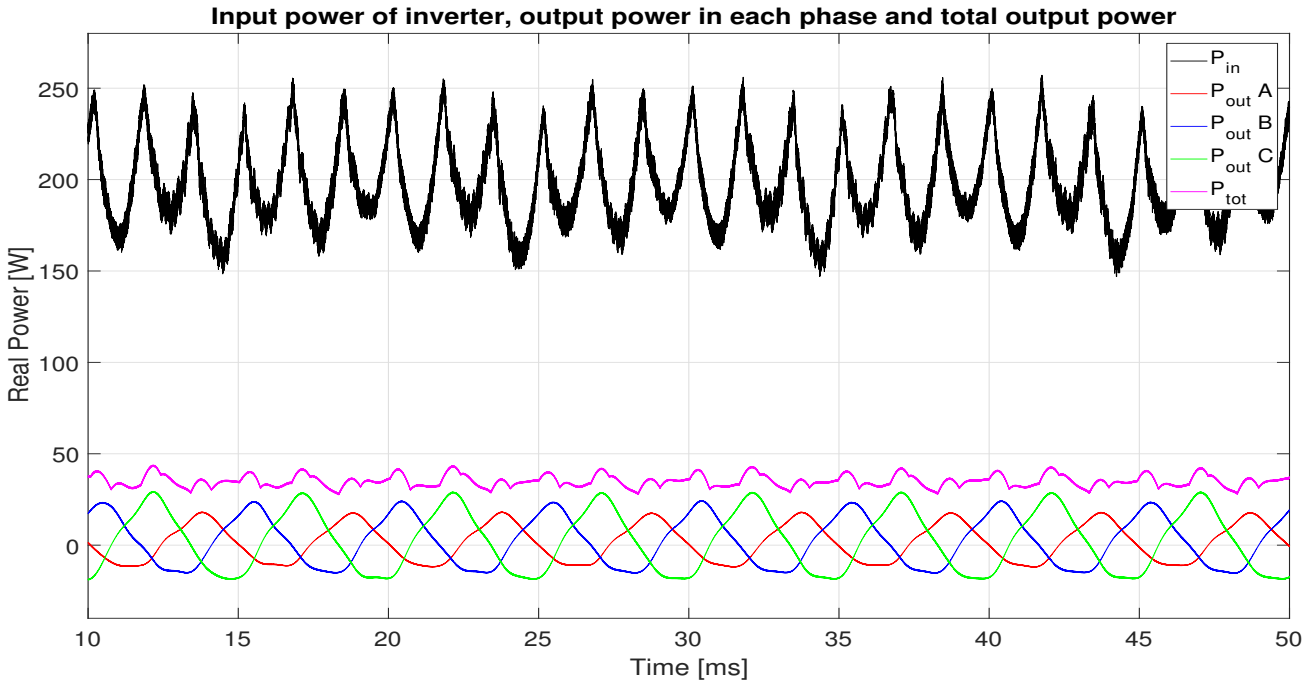


Figure 4.29: Active power for each phase, the input power and the sum of the output power.

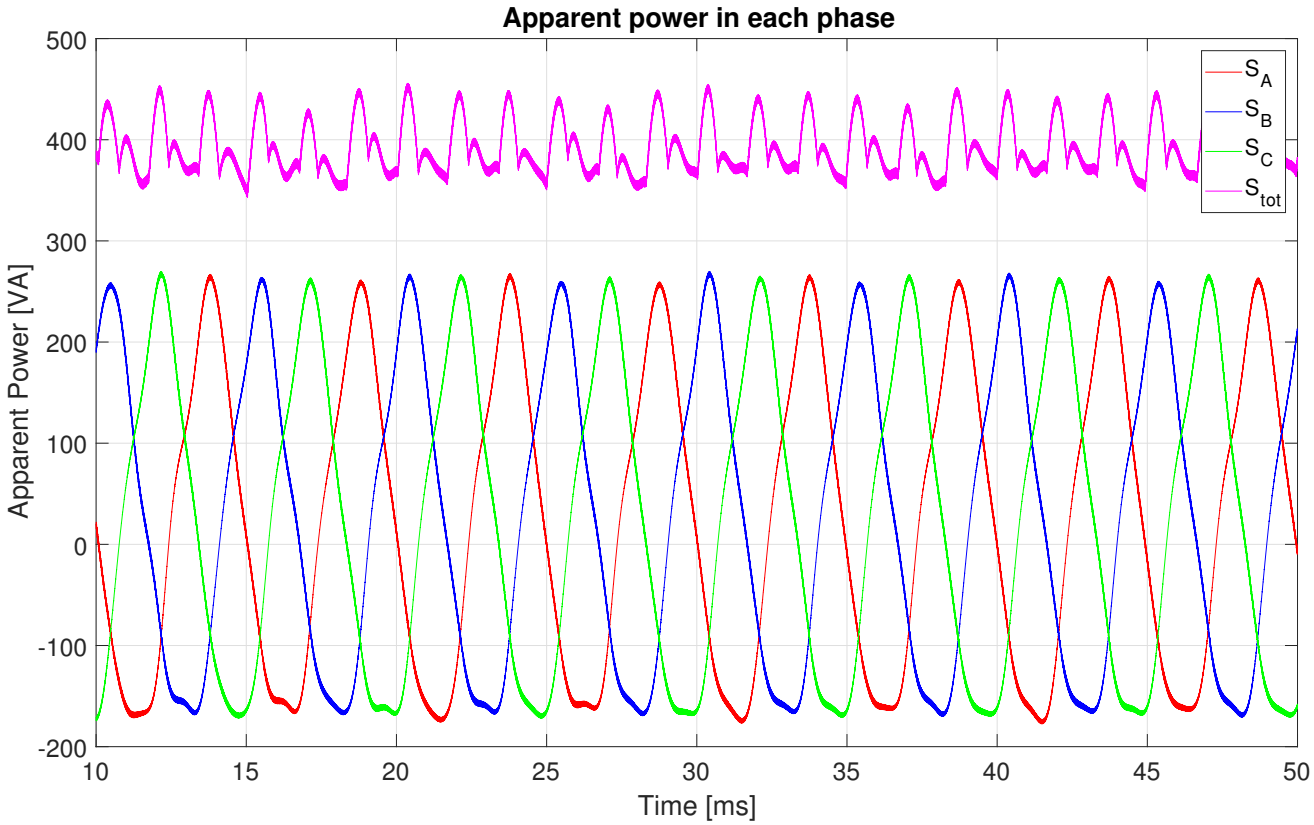


Figure 4.30: Apparent power for each phase and the sum of the apparent output power.

The efficiency is calculated by filtering the load current and load voltage for each phase so the fundamental curve can be acquired without introducing any phase shift to the signals. It should be noted it is the voltage over each load and not the output of the transistor that is referred to as load voltage. Both current and voltage are rescaled back to their original values by comparing the raw data of the current and filtered data, since the filter that is used is not perfect. The apparent power, S, is then calculated and by acquiring the phase angle for each case the real and reactive power is calculated. In the table 4.2 below, the average efficiency is presented for different switching frequencies and slew rates. These numbers are calculated by using a cumulative sum and then averaging it and using the last value.

Table 4.2: The inverter's efficiency at different switching frequencies and slew rates.

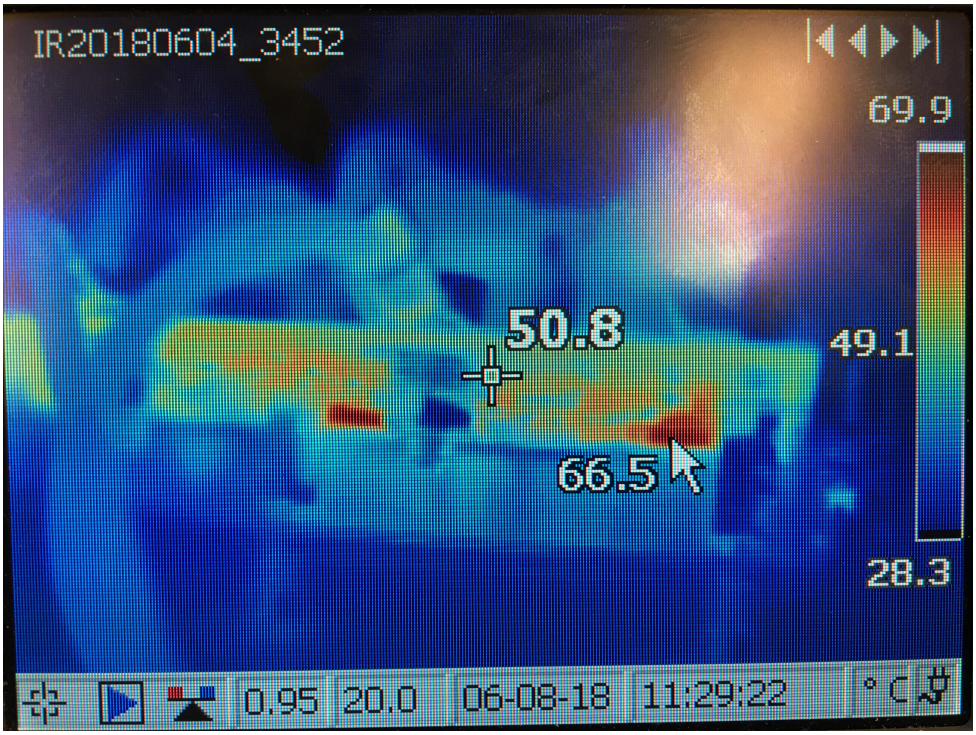
Switching Frequency $[kHz]$	**Slew rate** (Ω/nF)	η_{avg} [%]
50	23.3/3.3	21.7
50	59.3/6.6	16.5
50	103.3/10.1	17.7
100	23.3/3.3	16.5
100	59.3/6.6	15.1

4.2.4 Thermal development and evaluation of liquid cooling

Thermal development and temperature rise of the components is measured from thermal imager of brand Fluke model Ti45. Firstly, an image is taken at low current which can be seen in the fig. 4.31a. During this measurement water cooling was not implemented instead fans are used to cool down the MOSFETs and the temperature recoreded to be 66.6 $°C$. The rise in temperature at this low currents drive us to implement water cooling. Secondly, at $I_{phase} = 63.8\ A_{peak}$ on the inverter with maximum temperatue of 69.9 $°C$ on one of the MOSFET legs, can be seen in fig. 4.31b. Due to integrated cooling and placement of components the thermal temperature cannot be oberserved for the whole DC capacitor bank and all MOSFETs. But it was observed to be similar for all the MOSFETs as shown in the figure below. At this high current, water cooling seems to be working well and the temperature of DC capacitor bank along with the MOSFETs is kept at an acceptable level. The cause for achieving these acceptable temperatures is due to the fact that water is cooled through the radiator placed before the cooling plate, which can be seen in fig. 3.5d.



(a) Illustrative picture of temperature variation on MOSFETs without water cooling implemented.



(b) Illustrative picture of temperature variation on MOSFETs with water cooling.

Figure 4.31: Two temperature readings with and without integrated water cooling.

After the implementation of water cooling one can see the difference of temperature and increase in power.

5
Conclusion

5.1 Inverter

The final prototype of the inverter is realized within the time scope and is working as intended. The measurements were unfortunately not carried out for the full power however, the data sheets support that the transistors should be able to withstand that level of current if more of them are installed. Although, as can be seen in the thermal calculations in appendix A, most transistors reach a temperature that would destroy them, including the transistors used in this final prototype. However, these calculations may be prone to error. The calculations of the thermal resistance of the thermal interface cloth adds in some cases around $300°C$ of generated heat to the junction temperature. When running a peak load current of around 64 A in one phase the thermal camera showed a case temperature of around $70°C$ when only six transistors were installed. In the case that twelve transistors would be installed the peak current in one phase would be 115 A at full power. This means that the transistors that handled 64 A have handled current than what they would at full power and twelve transistors installed which indicates that the inverter would be fully functional at full power operation.

Moreover, as shown in 4.2.2 the inverter possess some sort of parasitic elements which introduce high frequency ringing during turn-on for V_{ds}. This could be because of the transistor where the ringing occurred possess some error. It is believed by the authors of this report that there might be some transient that is introduced from the gate driver PCB as well. There is one capacitor mounted on this PCB to damp any ringing however, the resonant frequency for this type of capacitor is well below the frequency of the oscillations that were discovered during turn-on.

The slew rate that damps the ringing the most is the one when switching frequency is set to 50 kHz, turn-on resistance of 103.3 Ω, turn-off resistance of 4.3 Ω and gate to source capacitance of 10.1 nF and is the setup that is recommended for the inverter to operate with.

5.2 Environmental aspect

From an environmental point of view, improving a part of the powertrain in a mild hybrid can be beneficial in many regards. First and foremost, what has been presented and discussed in this thesis regarding the technical improvements from using

an integrated inverter are obvious such as the elimination of cables which reduce copper losses and weight as well as the integrated cooling with the EM. Both of these advancements allow for a more fuel efficient vehicle which brings the automotive industry closer to their goals of adapting to more stringent environmental regulations. Moreover, making a mild hybrid vehicle a more efficient and better performing will strengthen its prescence on the market making more customers inclined to purchase it instead of a classic ICE vehicle which will lead to reducing environmental impact of the automotive industry and also speed up the transistion into fully electric vehicles.

The best measured efficiency of the final prototype was 21.7% which is very low compared to industry manufactured inverters however, we believe that investing more time and work into this design and this efficiency can be increased. Even if this efficiency is not achieved, an interesting evaluation would be to measure the vehicle's overall performance with the old inverter concept implemented versus the integrated one. This analysis has not been possible for us to conduct due to working with a prototype that will be implemented in future vehicles. However, if one were to conduct this comparison, looking at how the difference in weight affects energy consumption, performance of acceleration and deceleration of the EM and range would be of interest. This study could show that even though the inverter itself might not be performing more efficiently than the old concept, the benefits of the integrated inverter takes form in other ways.

5.3 Future work and recommendations

To further improve this design of an integrated distributed inverter there are a lot of things to consider. These ideas were given thought during the project but not pursued due to either the complexity or time that would be needed for successful results.

5.3.1 Wide-bandgap technology

When studying the performance of different switches it was found that the only GaN transistor that was available for these power ratings performed very well. However, when working with the first prototype we learnt how sensitive the transistors are to parasitic inductances and how careful one must be in optimizing the circuit when increasing the frequency. When analyzing the GaN transistor's internal capacitances and turn-on and turn-off times it was realized that working with this component and getting the inverter to work for high frequencies would be difficult. Given the delay that we already had, we decided against using GaN since there were a lot of Si transistors that had similar performance but did not require as much work. However, the authors of this report believe that more investigation with GaN (and SiC if one finds transistors for high current low voltage) should be made since this can result in even smaller and more efficient integrated inverters if a higher switching frequency is achieved. The price and compelexity of using GaN is what can be limiting but both are areas where improvements are made.

5.3.2 Interleaving switching

In order to optimize the inverter there is a switching technique called interleaving switching. This switching technique utilizes the fact that there are several inverters (or phase legs) in parallel and by allowing the carrier wave for each inverter to be phase shifted from other carrier waves the harmonic current ripple on the DC capacitor bank can be reduced [16]. This in turns leads to that the DC capacitor bank can be reduced in both capacitance and volume which will save space and cost in the vehicle. Although this was not part of our master thesis to perform, using this technique allows for a smaller DC capacitor bank which would additionally improve the inverter.

5.3.3 DC capacitor bank

To save costs and volume the DC bank could have been made even smaller, as was reported in section 4.2.1. If one would take more time into investigating different capacitors there is a chance of an even better optimization with regards to cost, losses and volume. The GAMS code can also be made more sophisticated to not demand so much input from the user as well as take regards to more parameters and have a more developed loss model.

Bibliography

[1] T. Dörsam, S. Kehl, A. Klinkig, A. Radon, and O. Sirch, "The new voltage level 48 v for vehicle power supply," *ATZelektronik worldwide*, vol. 7, no. 1, pp. 10–15, 2012.

[2] H. Zhang, L. Jin, O. Wallmark, and S. Norrga, "Evaluation of modular integrated electric drive concepts for automotive traction applications," 2017.

[3] J. Wang, Y. Li, and Y. Han, "Evaluation and design for an integrated modular motor drive (immd) with gan devices," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*. IEEE, 2013, pp. 4318–4325.

[4] T. M. Jahns and H. Dai, "The past, present, and future of power electronics integration technology in motor drives," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 197–216, 2017.

[5] F. FÜRST, "Design of a 48 v three-phase inverter for automotive applications," 2015.

[6] Y. RASTOGI, "Design and testing of a 3-phase voltage source inverter for mild hybrid vehicle application." 2018.

[7] B. Mckay, "Benefits of a 48v p2 mild hybrid," in *Advanced Clean Cars Symposium: The Road ahead*, 2016.

[8] S. Taranovich, "Si vs. gan vs. sic: Which process and supplier are best for my power design?" *EDN Network*, 2013.

[9] A. Patzak and D. Gerling, "Design of a multi-phase inverter for low voltage high power electric vehicles," in *Electric Vehicle Conference (IEVC), 2014 IEEE International*. IEEE, 2014, pp. 1–7.

[10] *Capacitors for fast-switching semiconductors*, TDK Group Company, 03 2017, rev. 5.0.

[11] A. K. Dr. Dušan Graovac, Marco Pürschel, "Mosfet power losses calculation using the datasheet parameters," *Infineon MOSFET Converter Losses*, July, 2006.

[12] T. I. Incorporated, "Estimating mosfet parameters from the data sheet," 2002.

[13] N. Oborny, "Understanding idrive and tdrive in ti smart gate drivers," *Texas Instrument website*, 2018.

[14] M. Uğur and O. Keysan, "Dc link capacitor optimization for integrated modular motor drives," in *Industrial Electronics (ISIE), 2017 IEEE 26th International Symposium on*. IEEE, 2017, pp. 263–270.

[15] J. Boehmer, J. Schumann, and H.-G. Eckel, "Effect of the miller-capacitance during switching transients of igbt and mosfet," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*. IEEE, 2012, pp. LS6d–3.

[16] B. Rubey, A. Patzak, F. Bachheibl, and D. Gerling, “Dc-link current harmonics minimization in iscad multi-phase inverters with interleaving,” in *2017 IEEE Vehicle Power and Propulsion Conference (VPPC)*, Dec 2017, pp. 1–7.

A

Appendix 1

This appendix includes a list of the semiconducting devices that were investigated for the project with regards to different aspects such as cost, package, losses, thermal capabilites etc. All calculations are made for 64 A peak current.

Table A.1: List of transistor properties with regards to performance and cost.

Material	Brand Model	BD. Voltage[V]	ID @ 25°C[A]	ID @ 100°C[A]	Rds(on) (Vgs=10 V) (typ.) [Ω]	Vgs(th) (typ.) [V]	No. of switches req. per inverter	Cost for 10000 units [€]	Transistor cost per inverter [€]
Si	TI CSD19535KTT	100	197	139	0.0028	2.7	6	12600	7.56
	TI CSD19532Q5B	100	140	100	0.004	2.6	12	8028	9.63
	TI CSD19536KCS	100	259	150	0.0023	2.5	6	16762	10.06
	TI CSD19536KTT	100	272	192	0.002	2.5	6	18700	11.22
	TI CSD19531KCS	100	110	78	0.0064	2.7	12	13000	15.6
	Inf IAUT260N10S5N019	100	260	197	0.0016	3	6	17000	10.2
	Inf IAUT300N10S5N015	100	300	247	0.0013	3	6	26700	16.02
	Inf IPB036N12N3 G	120	180	139	0.0029	3	6	28198.2	16.92
	Inf IPB180N10S4-03	100	180	134	0.0027	2.7	6	15872.4	9.523
	IR IRFB4110PbF	100	180	130	0.0037	4	6	11700	7.02
	IR IRLB4030PbF	100	180	130	0.0034	2.5	6	15000	9
	VISHAY SiR668DP	100	95	76	0.0048	3.4	12	9100	10.92
	VISHAY SiDR870ADP	100	95	77.8	0.0066	3	12	7310	8.772
	VISHAY SiR680DP	80	100	100	0.0029	3.4	12	8780	10.536
	VISHAY SQR70090ELR	100	86	50	0.0087	2	18	4970	8.946
	TOSHIBA TPW3R70APL	100	90	150	0.0031	2.5	6	N/A	N/A
	Inf IPT015N10N5	100	300	243	0.0015	3	6	28000	16.8
	FAIRCHILD FDBL0200N100	100	300	n/a	0.0015	3.1	6	24200	14.52
	Inf IPP045N10N3GXKSA1	100	100	100	0.0042	2.7	12	37190	44.63
	Inf IPD50N10S3L-16	100	50	38	0.0125	1.7	24	4210	10.10
	Inf IPD60N10S4L-12	100	60	43	0.012	1.6	18	40690	73.24
	Inf IPD70N10S3-12	100	70	48	0.0111	3	18	5210	9.38
	NEX PSMN016-100YS	100	51	37	0.0163	3	24	44080	105.79
GaN	EPC EPC2022	100	90	n/a	0.0032	1.4	12	42242.2	50.69

Table A.2: List of transistor losses with fast turn-on resistor.

Material	Brand Model	Rg [Ω]	no. of sw. for calc.	Switching frequency [Hz]	Conduction losses [W]	Turn-off losses Transistor [W]	Turn-on losses Transistor [W]	Turn-on losses Diode [W]	Switching losses [W]	Total theoretical losses for one switching cycle [W]
Si	TI CSD19535KTT	23.3	1	50000	11.47	8.92	12.03	0.261	21.21	32.68
	TI CSD19532Q5B	23.3	2	50000	4.1	1.94	2.59	0.149	4.68	8.78
	TI CSD19536KCS	23.3	1	50000	9.42	10.18	13.11	0.329	23.62	33.04
	TI CSD19536KTT	23.3	1	50000	8.19	17.53	18.57	0.329	36.43	44.62
	TI CSD19531KCS	23.3	2	50000	6.55	1.49	2.65	0.162	4.3	10.85
	Inf IAUT260N10S5N019	23.3	1	50000	6.55	21.33	18.27	0.108	39.71	46.26
	Inf IAUT300N10S5N015	23.3	1	50000	5.32	29.16	21.69	0.132	50.98	56.3
	Inf IPB036N12N3 G	23.3	1	50000	11.88	22.82	26.06	0.214	49.09	60.97
	Inf IPB180N10S4-03	23.3	1	50000	11.06	17.9	14.5	0.102	32.5	43.56
	IR IRFB4110PbF	23.3	1	50000	15.16	36	40.75	0.056	76.81	91.97
	IR IRLB4030PbF	23.3	1	50000	13.93	42.55	41.66	0.053	84.26	98.19
	VISHAY SiR668DP	23.3	2	50000	4.92	4.64	7.72	0.069	12.43	17.35
	VISHAY SiDR870ADP	23.3	2	50000	6.76	5.01	4.44	0.046	9.5	16.26
	VISHAY SiR680DP	23.3	2	50000	2.97	5.3	7.87	0.069	13.24	16.21
	VISHAY SQR70090ELR	23.3	3	50000	3.96	2.99	2.59	0.069	5.65	9.61
	TOSHIBA TPW3R70APL	23.3	1	50000	12.7	13.56	9.63	0.044	23.23	35.93
	Inf IPT015N10N5	23.3	1	50000	6.14	20.99	27.16	0.19	48.34	54.48
	FAIRCHILD FDBL0200N100	23.3	1	50000	6.14	5.79	10.79	0.103	16.68	22.82
	Inf IPP045N10N3GXKSA1	23.3	2	50000	4.3	5	9.31	0.081	14.39	18.69
	Inf IPD50N10S3L-16	23.3	4	50000	3.2	1.61	0.68	0.107	2.4	5.6
	Inf IPD60N10S4L-12	23.3	3	50000	5.46	2.63	0.66	0.09	3.38	8.84
	Inf IPD70N10S3-12	23.3	3	50000	5.05	1.86	1.12	0.159	3.14	8.19
	NEX PSMN016-100YS	23.3	4	50000	4.17	2.26	1	0.079	3.34	7.51
GaN	EPC EPC2022	23.3	2	50000	3.28	2.15	1.39	0	3.54	6.82

Table A.3: List of transistor losses with slow turn-on resistor.

Material	Brand Model	Rg [Ω]	no. of sw. for calc.	Switching frequency [Hz]	Conduction losses [W]	Turn-off losses Transistor [W]	Turn-on losses Transistor [W]	Turn-on losses Diode [W]	Switching losses [W]	Total theoretical losses for one switching cycle [W]
Si	TI CSD19535KTT	103.3	1	50000	11.47	35.57	45	0.261	80.83	92.3
	TI CSD19532Q5B	103.3	2	50000	4.1	7.8	8.65	0.149	16.6	20.7
	TI CSD19536KCS	103.3	1	50000	9.42	43.82	51.48	0.329	95.63	105.05
	TI CSD19536KTT	103.3	1	50000	8.19	76.15	75.73	0.329	152.21	160.4
	TI CSD19531KCS	103.3	2	50000	6.55	6.07	8.56	0.162	14.79	21.34
	Inf IAUT260N10S5N019	103.3	1	50000	6.55	84.54	76.62	0.108	161.27	167.82
	Inf IAUT300N10S5N015	103.3	1	50000	5.32	116.62	90.42	0.132	207.17	212.49
	Inf IPB036N12N3 G	103.3	1	50000	11.88	95.66	98.89	0.214	194.76	206.64
	Inf IPB180N10S4-03	103.3	1	50000	11.06	67.47	60.27	0.102	127.84	138.9
	IR IRFB4110PbF	103.3	1	50000	15.16	136.4	162.24	0.056	298.7	313.86
	IR IRLB4030PbF	103.3	1	50000	13.93	143.8	96.96	0.053	240.81	254.74
	VISHAY SiR668DP	103.3	2	50000	4.92	19.12	30.4	0.069	49.59	54.51
	VISHAY SiDR870ADP	103.3	2	50000	6.76	21.02	17.2	0.046	38.27	45.03
	VISHAY SiR680DP	103.3	2	50000	2.97	22.05	30.79	0.069	52.91	55.88
	VISHAY SQR70090ELR	103.3	3	50000	3.96	12.74	10.08	0.069	22.89	26.85
	TOSHIBA TPW3R70APL	103.3	1	50000	12.7	42.19	36.55	0.044	78.78	91.48
	Inf IPT015N10N5	103.3	1	50000	6.14	85.14	109.88	0.19	195.21	201.35
	FAIRCHILD FDBL0200N100	103.3	1	50000	6.14	23.31	39.83	0.103	63.24	69.38
	Inf IPP045N10N3GXKSA1	103.3	2	50000	4.3	20.33	32.37	0.081	52.78	57.08
	Inf IPD50N10S3L-16	103.3	4	50000	3.2	6.82	1.24	0.107	8.17	11.37
	Inf IPD60N10S4L-12	103.3	3	50000	5.46	9.81	1.44	0.09	11.34	16.8
	Inf IPD70N10S3-12	103.3	3	50000	5.05	7.55	2.09	0.159	9.8	14.85
	NEX PSMN016-100YS	103.3	4	50000	4.17	8.65	1.75	0.079	10.48	14.65
GaN	EPC EPC2022	103.3	2	50000	3.28	8.2	4.83	0	13.03	16.31

Table A.4: List of transistor temperature calculations with fast turn-on resistor and water temperature assumed to be 35°C.

Material	Brand Model	Rg [Ω]	Switching frequency [Hz]	T_j operating [°C]	T_{RJC} [°C/W]	T_{RCP} [°C/W]	Packaging type	cooling area[m^2]	T_j [°C]
Si	TI CSD19535KTT	23.3	50000	-55 to 175	0.5	2.558	D^2 PAK (TO-263)	0.00006515	177.58
	TI CSD19532Q5B	23.3	50000	-55 to 155	0.8	8.735	SON 5 x 6 mm Plastic Package	0.00001908	155.63
	TI CSD19536KCS	23.3	50000	-55 to 175	0.4	1.457	TO-220 NexFET	0.0001144	121.76
	TI CSD19536KTT	23.3	50000	-55 to 175	0.4	1.863	D^2 PAK (TO-263)	0.00008946	173.65
	TI CSD19531KCS	23.3	50000	-55 to 175	0.7	1.479	TO-220 NexFET	0.000112712	70.99
	Inf IAUT260N10S5N019	23.3	50000	-55 to 175	0.5	3.137	P/G-HSOF-8-1	0.000053125	262.7
	Inf IAUT300N10S5N015	23.3	50000	-55 to 175	0.4	3.137	P/G-HSOF-8-1	0.000053125	301.16
	Inf IPB036N12N3 G	23.3	50000	-55 to 175	0.5	3.332	PG-TO263-7	0.000050025	355.16
	Inf IPB180N10S4-03	23.3	50000	-55 to 175	0.6	3.332	PG-TO263-7-3	0.000050025	273.7
	IR IRFB4110PbF	23.3	50000	-55 to + 175	0.402	1.479	TO-220	0.000112712	273.93
	IR IRLB4030PbF	23.3	50000	-55 to + 175	0.4	1.479	TO-220AB	0.000112712	288.34
	VISHAY SiR668DP	23.3	50000	-55 to +150	0.9	11.193	PowerPAK SO-8 Single	0.00001489	326.7
	VISHAY SiDR870ADP	23.3	50000	-55 to +150	1.1	11.144	PowerPAK SO-8DC	0.0000149552	321.67
	VISHAY SiR680DP	23.3	50000	-55 to +150	0.9	5.262	PowerPAK SO-8 Single	0.0000316725	170.71
	VISHAY SQR70090ELR	23.3	50000	-55 to +175	1.1	8.591	TO-252 Reverse Lead DPAK	0.0000194	168.6
	TOSHIBA TPW3R70APL	23.3	50000	-55 to +175	0.93	7.891	DSOP Advance	0.00002112	485.87
	Inf IPT015N10N5	23.3	50000	- 55 to + 175	0.2	1.671	PG-HSOF-8	0.000099716	173.44
	FAIRCHILD FDBL0200N100	23.3	50000	- 55 to + 175	0.35	1.484	MO-299A	0.000112326	94.32
	Inf IPP045N10N3-GXKSA1	23.3	50000	-55 to 175	0.7	1.41	PG-TO220-3	0.000118243	90.1
	Inf IPD50N10S3L-16	23.3	50000	-55 to 175	1.5	4.49	PG-TO252-3-11	0.00003712	84.74
	Inf IPD60N10S4L-12	23.3	50000	-55 to 175	1.6	4.962	PG-TO252-3-313	0.000033588	122.66
	Inf IPD70N10S3-12	23.3	50000	-55 to 175	1.2	4.136	PG-TO252-3-11	0.0000403	100.57
	NEX PSMN016-100YS	23.3	50000	-55 to 175	0.54	8.13	LFPAK Power-SO8	0.0000205	131.65
GaN	EPC EPC2022	23.3	50000	-40 to 150	0.4	11.977	Passivated die form w/ solder bumps	0.000013915	158.87

Table A.5: List of transistor temperature calculations with slow turn-on resistor and a water temperature assumed to be 35°C.

Material	Brand Model	Rg [Ω]	Switching frequency [Hz]	T_j operating [°C]	T_{RJC} [°C/W]	T_{RCP} [°C/W]	Packaging type	cooling area[m^2]	T_j [°C]
Si	TI CSD19535KTT	103.3	50000	-55 to 175	0.5	2.558	D^2 PAK (TO-263)	0.00006515	415.77
	TI CSD19532Q5B	103.3	50000	-55 to 155	0.8	8.735	SON 5 x 6 mm Plastic Package	0.00001908	302.57
	TI CSD19536KCS	103.3	50000	-55 to 175	0.4	1.457	TO-220 NexFET	0.0001144	298.33
	TI CSD19536KTT	103.3	50000	-55 to 175	0.4	1.863	D^2 PAK (TO-263)	0.00008946	517.95
	TI CSD19531KCS	103.3	50000	-55 to 175	0.7	1.479	TO-220 NexFET	0.000112712	101.05
	Inf IAUT260N10S5N019	103.3	50000	-55 to 175	0.5	3.137	P/G-HSOF-8-1	0.000053125	839.01
	Inf IAUT300N10S5N015	103.3	50000	-55 to 175	0.4	3.137	P/G-HSOF-8-1	0.000053125	1021.66
	Inf IPB036N12N3 G	103.3	50000	-55 to 175	0.5	3.332	PG-TO263-7	0.000050025	1081.92
	Inf IPB180N10S4-03	103.3	50000	-55 to 175	0.6	3.332	PG-TO263-7-3	0.000050025	761.68
	IR IRFB4110PbF	103.3	50000	-55 to + 175	0.402	1.479	TO-220	0.000112712	824.5
	IR IRLB4030PbF	103.3	50000	-55 to + 175	0.4	1.479	TO-220AB	0.000112712	676.45
	VISHAY SiR668DP	103.3	50000	-55 to +150	0.9	11.193	PowerPAK SO-8 Single	0.00001489	906.66
	VISHAY SiDR870ADP	103.3	50000	-55 to +150	1.1	11.144	PowerPAK SO-8DC	0.0000149552	776.15
	VISHAY SiR680DP	103.3	50000	-55 to +150	0.9	5.262	PowerPAK SO-8 Single	0.0000316725	487.57
	VISHAY SQR70090ELR	103.3	50000	-55 to +175	1.1	8.591	TO-252 Reverse Lead DPAK	0.0000194	384.45
	TOSHIBA TPW3R70APL	103.3	50000	-55 to +175	0.93	7.891	DSOP Advance	0.00002112	1119.11
	Inf IPT015N10N5	103.3	50000	- 55 to + 175	0.2	1.671	PG-HSOF-8	0.000099716	536.33
	FAIRCHILD FDBL0200N100	103.3	50000	- 55 to + 175	0.35	1.484	MO-299A	0.000112326	207.13
	Inf IPP045N10N3-GXKSA1	103.3	50000	-55 to 175	0.7	1.41	PG-TO220-3	0.000118243	196.71
	Inf IPD50N10S3L-16	103.3	50000	-55 to 175	1.5	4.49	PG-TO252-3-11	0.00003712	129.47
	Inf IPD60N10S4L-12	103.3	50000	-55 to 175	1.6	4.962	PG-TO252-3-313	0.000033588	190.24
	Inf IPD70N10S3-12	103.3	50000	-55 to 175	1.2	4.136	PG-TO252-3-11	0.0000403	146.59
	NEX PSMN016-100YS	103.3	50000	-55 to 175	0.54	8.13	LFPAK Power-SO8	0.0000205	211.66
GaN	EPC EPC2022	103.3	50000	-40 to 150	0.4	11.977	Passivated die form w/ solder bumps	0.000013915	310.59

Table A.6: List of all transistors that were investigated.

Brand - Model
TI - CSD19535KTT
TI - CSD19532Q5B
TI - CSD19536KCS
TI - CSD19536KTT
Inf - IAUT260N10S5N019
Inf - IAUT300N10S5N015
Inf - IPB036N12N3 G 120
Inf - IPB180N10S4-03 100
EPC - EPC2022
VISHAY - SQJQ410EL
IR - IRF8010PbF
IR - IRFB4110PbF
IR - IRFP4110PbF
IR - IRFPS3810PbF
IR - IRLB4030PbF
IR - IRFP4568PbF
VISHAY - SiR668DP
VISHAY - SiDR870ADP
VISHAY - SiR680DP
VISHAY - SQM120N10-3m8-GE3
VISHAY - SQR70090ELR
VISHAY - SQJQ910EL
TOSHIBA - TPW3R70APL
Inf - IPT015N10N5
FAIRCHILD - FDBL0200N100
IR - AUIRFN7110
Inf - IPD50N10S3L-16
Inf - IPD60N10S4L-12
Inf - IPD70N10S3-12
NEX - PSMN016-100YS
Inf - BSC252N10NSF G
Vishay - SiR878ADP
TI - CSD19534Q5A
Inf - IRFH7110PbF
ON - NTMFS6B14N