

Investigation of Bridgeless Power Factor Correction Topologies for 3 kW Operation

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MASTER'S THESIS 2021

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CHALMERS UNIVERSITY OF TECHNOLOGY
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Abstract

Power Factor Correction (PFC) circuits are widely used today in switch mode power supplies. The purpose of these circuits is to improve the quality of power drawn from the grid by reducing the reactive power drawn by the application as well as reducing the harmonic content of the current. Conventional PFCs consist of a bridge rectifier that rectifies the AC voltage to DC which is then followed by a boost converter which shapes the input current of the converter to be in phase with the input voltage and thereby obtaining a power factor close to unity. The aim of this project was to investigate PFC topologies which eliminate the bridge rectifier to increase the efficiency and improve the thermal performance of the converter. First, a literature study was conducted to select the three most suitable topologies for 3 kW operation. The selected topologies are the Semi-Bridgeless Boost PFC, Bridgeless Interleaved Boost PFC and Totem-Pole Boost PFC utilizing Gallium Nitride transistors. Thereafter a performance analysis of each topology was carried out using Matlab and Simulink simulations. The parameters of interest are efficiency, power factor, input current ripple, inrush current and thermal performance as well as the component count and complexity of the converters.

The Bridgeless Interleaved PFC was found to be the topology with leading performance in all parameters of interest. The peak efficiency achieved was 97.86 percent with Totem pole closely thereafter at 97.55 percent. All the topologies achieved a power factor near unity. Due to the inherent ripple cancellation of the Bridgeless Interleaved PFC, this topology had the lowest input current ripple as well as the lowest total harmonic distortion for full load operation.

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1

Introduction

1.1 Background

Switching mode power supply (SMPS) units are widely used to convert between different voltage levels. At the input stage of power supply units which are used for AC/DC applications, a diode bridge rectifier is often used to rectify the AC voltage connected to the DC/DC converter. The utilization of the bridge and the DC/DC converter will lead to a non-optimal power factor as well as current harmonics being injected both into the grid and the circuit. To increase the power factor in the SMPS, a Power Factor Correction (PFC) circuit is commonly used between the rectifier stage and the DC/DC converter. There are different types of PFC circuits but a commonly used topology is a Boost-converter circuit which is connected in between the bridge rectifier and the DC/DC converter. By adjusting the duty cycle in the Boost circuit, the current wave form can be adjusted so that it is in phase with the voltage waveform. This will lead to high power factor which is desired. The bridge rectifier will be one of the main sources of losses in this setup. This is due to the conduction losses in the diodes of the bridge rectifier. Due to this it is of interest to investigate different types of bridgeless topologies for power factor correction which eliminate the bridge rectifier in order to further reduce the losses in the SMPS.

1.2 Aim

The aim of this project is to investigate different topologies of power factor correction circuits which eliminate the need for the diode bridge rectifier at the input to further increase the efficiency and thermal performance of the PFC. The PFC should be able to operate with 86-264 VAC as well as 260-400 VDC input voltage. The output voltage of the PFC should be 405 VDC and the output power should be 3 kW.

1.3 Problem Description

Operating requirements for the PFC are given in the table 1.1.

Table 1.1: Specifications for the Power Factor Correction circuit

Input voltage	86-264 VAC & 260-400 VDC
Input frequency	47-63 Hz
Nominal output voltage	405 V
Hold up time	20 ms
Output power	3 kW

A literature study of bridgeless PFC topologies is conducted and the most suitable topologies are selected and investigated in detail. The selection of suitable topologies is based on following parameters:

- Does the topology meet the operating requirements given in table 1.1?
- Power Factor
- Efficiency
- Total Harmonics Distortion (THD)
- Input current ripple
- In-rush current
- Electromagnetic Interference
- Complexity
- Component Count

Simulations of selected topologies are conducted and comparisons of different topologies is done based on the above mentioned parameters.

1.4 Scope

In this project the performance of different bridgeless PFC topologies is investigated with help of calculations and computer simulations. The goal of the project is not to build a physical bridgeless power factor correction circuit or any kind of converter, rather to investigate which bridgeless PFC topologies are most suitable for the above mentioned operating requirements.

1.5 Sustainable Aspects

One of the greatest challenges the human species have to face in the coming years is the challenge of global warming. In order to tackle the effects of global warming, 189 countries have joined the Paris agreement where the goal is to limit the global temperature rise at 2 °C during this century [1]. The world needs to make the transition from the use of fossil fuels to more renewable energy sources such as wind and solar in order to reduce the amount of CO_2 released into the atmosphere, but this

transition is a big one and will take long time to achieve. Another way to decrease the amount of the CO_2 released into the atmosphere is to decrease the consumption of electrical energy. This can be done by further improving the efficiency of the electrical devices and converters. The power factor correction circuits are used in AC/DC converters to improve the power factor and total harmonics distortion of the current drawn from the grid. With the use of PFC circuits, greater efficiency of the AC/DC converter can be achieved. By finding ways to get rid of the diode bridge rectifier which can be seen in the most common Active Boost PFC topology, the efficiency of the PFC stage can be further improved. Due to the wide use of PFC circuits and a necessity to convert AC voltage to DC in many cases before use, it is important that the PFC circuits have high efficiency. In this project different bridgeless PFC topologies which increase the efficiency of the PFC are investigated. By improving the efficiency of the PFC stage, less power needs to be consumed which means less CO_2 needs to be released into the atmosphere.

2

Theoretical Background

2.1 AC/DC Converters

The dominant way of transmitting electrical power is in the form of a high voltage alternating current (AC). The advantage of AC compared to direct current (DC) transmission is lower transmission costs and a simple way of converting between different voltage levels with the help of transformers. Even though most of the power is transmitted in the form of AC, a large part of the power consumption is done using DC power. Due to this fact there is a necessity to efficiently convert the transmitted AC power to DC before use. AC/DC converters are used to accomplish this task, a block diagram of a typical AC/DC converter is shown in the figure 2.1. From the block diagram, it can be seen that the AC voltage is first converted to varying DC voltage using a diode bridge rectifier, thereafter a power factor correction (PFC) stage is found where the current waveform is shaped to be in phase with the voltage waveform. After the PFC stage, a DC/DC converter will convert the voltage to a required voltage level for the load. This chapter will introduce some of the necessary terminology needed to understand the AC/DC converters with emphasis placed on the PFC stage.

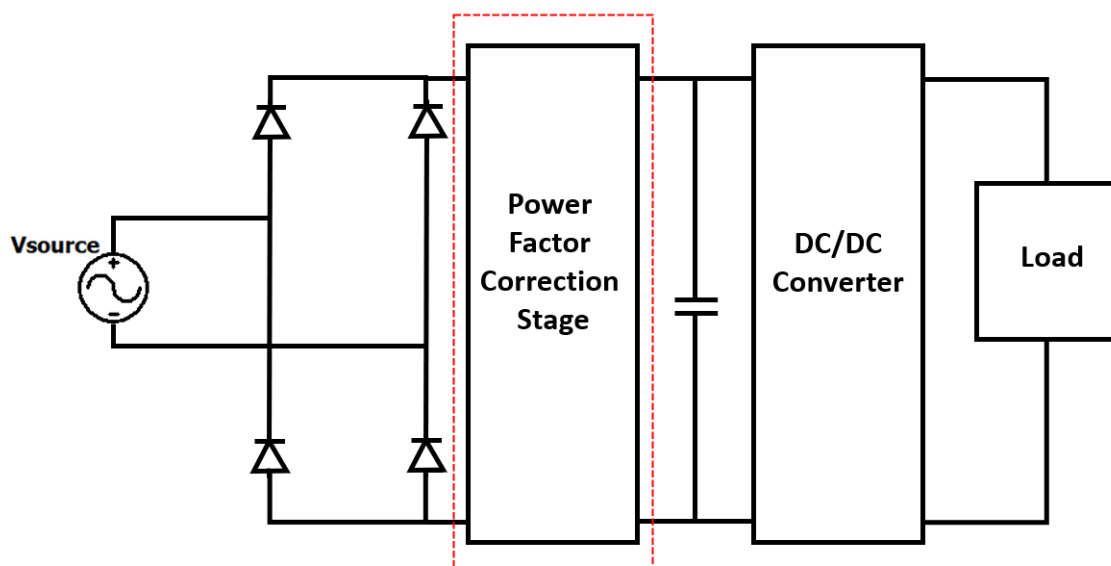


Figure 2.1: Block diagram of an AC/DC converter

2.1.1 Power Factor Correction

Most of the electrical equipment in use today is in some way connected to the grid, either constantly or for some duration of time. Such equipment ranges from phone chargers that consume a couple of Watts of power to charging stations for electrical vehicles which consume a couple of kW and beyond. When electrical equipment is connected to the grid it will be represented as a complex load. In many cases this load will draw a current that is not in phase with the input voltage. This will lead to consumption of both active and reactive power from the grid. The definition of power factor is the ratio between the usable active power (P) and the apparent power (S) which is the sum of active and reactive power (Q),

$$PF = \frac{P}{|S|} \quad (2.1)$$

A power factor which is equal to one indicates that the voltage and current waveforms are in phase with each other and that only active power is consumed. When the power factor is below one, it means that the voltage and current waveforms are displaced from one another and that both active and reactive power is consumed. The reactive power is not usable but the consumption of it will lead to circulating currents in the system which in turn lead to higher currents drawn from the grid. This means more losses and a need for example thicker cables that can handle higher currents. To minimize the reactive power and therefore minimize the total apparent power consumed from the grid, power factor correction circuits are utilized. These circuits shape the current drawn from the grid to be in phase with the voltage. They are also used to reduce the harmonic distortion of the input current which will lead to higher efficiency and lower distortions in the grid. In recent years more strict limits have been placed on the amount of harmonics all electrical equipment can inject to the grid. In the European Union, electrical systems are required by law to meet the requirements which are stated in EN 61000-3-2 which is a standard for the limitation of harmonic current emissions. Power factor correction circuits are critical when it comes to meeting these requirements.

2.1.2 Total Harmonic Distortion

Total harmonic distortion (THD) is the measure of the amount of distortions in a specific signal. It is defined as the ratio between the sum of all of the harmonic components and the fundamental component of the signal. The expression is

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \quad (2.2)$$

The current harmonic components will not contribute to the real power drawn from the sinusoidal source [2]. The THD and the power factor can then be related to each other with the following expression

$$PF = \frac{\cos\theta}{\sqrt{1 + THD^2}} \rightarrow \cos\theta = \text{Displacement Power Factor} \quad (2.3)$$

2.1.3 AC/DC Conversion

One of the simplest ways of converting AC voltage to DC is with the help of a bridge rectifier with a capacitive filter at the output. The bridge rectifier consists of four diodes which convert the AC input waveform from a varying signal with negative and positive pulses to two consecutive DC pulses. This new signal is then fed to the smoothing capacitor that is in parallel with the load. The capacitor is charged during the rise of a pulse and discharged during the fall but is discharged slower as to keep the voltage at a steady level. This is what generates the DC voltage on the output. The basic rectifier circuit can be seen in figure 2.2.

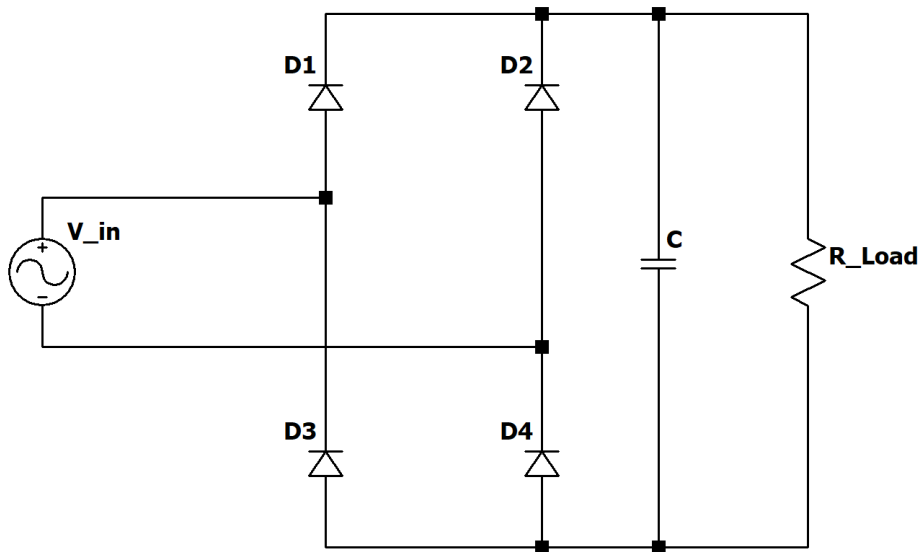


Figure 2.2: Diode bridge rectifier connected to a smoothing capacitor and the load

The advantage of this circuit is the low cost and complexity but it has some inherent issues when it comes to the quality of current drawn from the AC source. What will happen in this case is that the current will flow only when the input voltage is higher than the voltage across the filter capacitor. This will result in a non-sinusoidal current waveform with low power factor and a high harmonic distortion, see figure 2.3

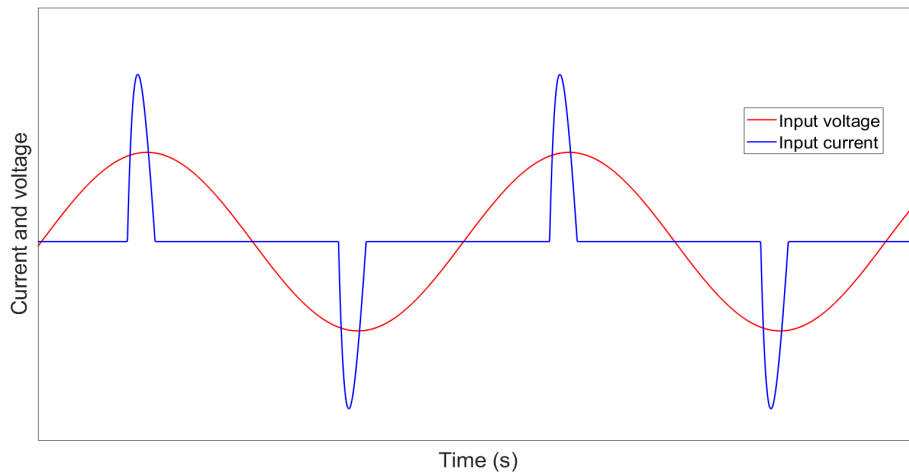


Figure 2.3: Input voltage and current waveforms of the circuit in figure 2.2

For this reason PFC circuits are used in order to improve the quality of the power drawn from the grid. There are many possible PFC topologies, these are divided into passive and active PFCs. Passive PFC topologies do not use any control loops but rather use passive components such as inductors in combination with the bridge rectifier and the filtering capacitor to improve the power factor and current harmonics. One simple and popular example of a passive PFC is to place an inductor in series with the AC source just before the bridge rectifier. This will lead to an improvement in the power factor and harmonic distortion in the input current. Passive PFC circuits are simple and easy to implement but they are not suitable for high power applications due to the size increase of the inductor. At high power levels the inductor on the AC input has to be very large, which will increase the size and losses of the converter. Also it is difficult to achieve high power factor for applications which need to work in a range of different input voltages [3]. Due to these reasons the emphasis in this project will be put on active PFC topologies.

2.1.4 Modes of Operation for Power Converters

For active PFC topologies the power is controlled by transistors that are in turn controlled by a control circuit. The operation of these switches determine the shape of the current waveforms and the most common modes of operation are presented below.

2.1.4.1 Continuous Conduction Mode (CCM)

When the converter is in CCM mode of operating the inductor current will be continuous. This means that the current coming from the grid and going through the inductors won't be zero with the exception of the zero crossings. The waveform can be seen in figure 2.4. This results in a low dI/dt over both the inductors and the switches since the current doesn't have to rise from zero to the reference. This mode of operation is therefore more suitable for higher power levels. A drawback

with this mode is that since the current doesn't reach zero, the switches are hard switched. Hard switching is when the drain-source voltage overlaps with the drain current. This results in higher switching losses.

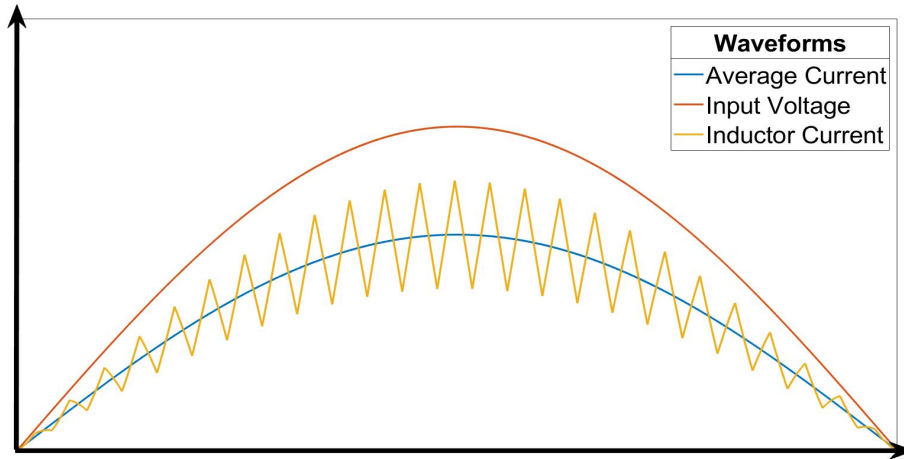


Figure 2.4: Wave forms of currents during CCM

2.1.4.2 Discontinuous Conduction Mode (DCM)

Discontinuous conduction mode is as the name implies when the current coming from the grid and going through the inductors is discontinuous, meaning that during a voltage period of the grid, the current is switched from zero to the level needed multiple times. The waveform can be seen in figure 2.5. As opposed to CCM this results in high dI/dt over the inductors and switches. This also means that the switches can be soft switched lowering the switching losses. DCM has higher electromagnetic interference than CCM which is very apparent when utilized for high power levels.

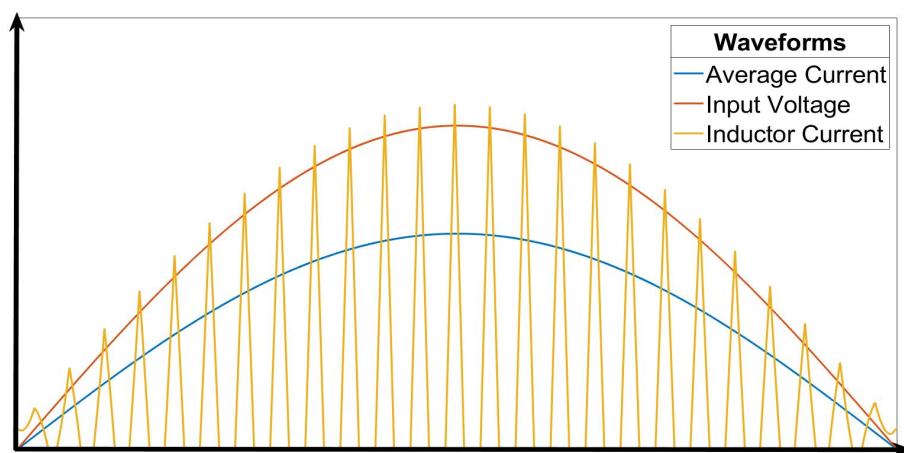


Figure 2.5: Wave forms of currents during DCM

2.1.4.3 Critical Conduction Mode (CrCM)

The critical conduction mode or boundary conduction mode as it is also called, is when the current average is achieved by the switching current reaching a sufficiently high level but then switched completely off for a very brief time. Contrary to DCM the current doesn't stay at zero level for a significant amount of time instead only stays down long enough to achieve soft switching and minimize switching losses. The waveform can be seen in figure 2.6. As for the DCM mode the CrCM will also have higher EMI and lower switching losses.

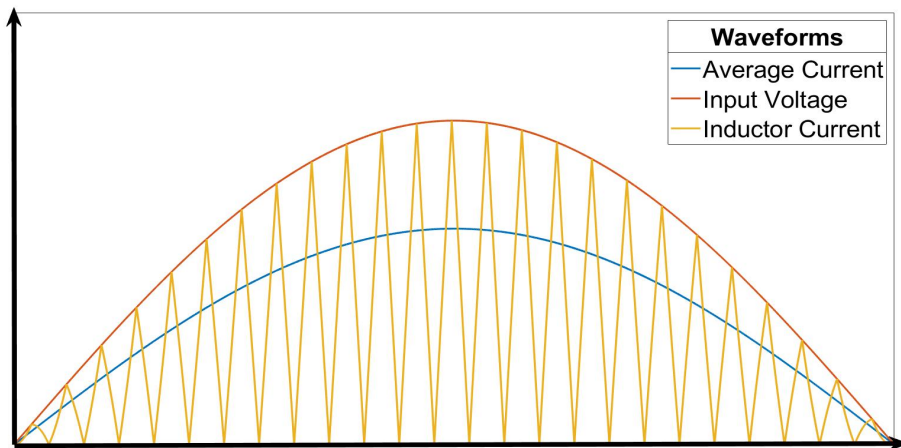


Figure 2.6: Wave forms of currents during CrCM

2.2 Active Power Factor Correction Topologies

Active PFC topologies improve the power factor by using active components such as transistors and diodes in combination with passive components such as inductors and capacitors. Some sort of control feedback loop is used to shape the input current to be in phase with the supply voltage. There are many possible active PFC topologies to choose from. These include PFC topologies that are based on Buck, SEPIC, Flyback, CUK and Buck-Boost converters but the most popular active PFC topologies for high power are based on some kind of Boost converter topology. Since the PFC circuit in this project requires a high power and a steady high voltage level, systems derived from the boost topology are chosen to be investigated. In the text below the operating principles for different active PFC topologies based on the Boost converter will be given.

2.2.1 Active Boost PFC

The Active Boost PFC consists of a diode bridge rectifier at the input followed by a boost stage containing an inductor, a diode, a switch and lastly an output filter capacitor. The schematic of the active boost PFC can be seen in figure 2.7. The diode bridge will rectify the sinusoidal input to a positive sinusoidal half wave voltage and by adjusting the duty cycle of the switch, the current waveform can be placed in phase with the voltage waveform, making it possible to obtain a power factor close to unity and to improve the total harmonics distortion of the input current. This circuit is popular due to its simplicity and low cost but one of its drawbacks is the diode bridge in the front end. The conduction losses of the bridge diodes will be responsible for a large part of the losses inside the boost PFC. This will lead to a lower efficiency of the circuit but will also cause some issues with the thermal management when it comes to high power application. Due to these issues, the active boost PFC should only be used for powers up to 1kW [4].

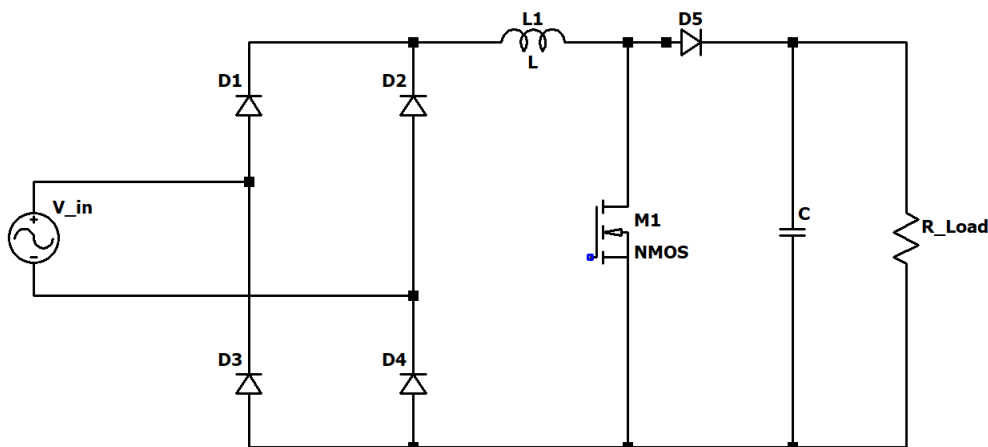


Figure 2.7: Schematic of the active boost PFC

2.2.2 Interleaved Boost PFC

The interleaved boost PFC consists of a diode bridge rectifier at the input stage, followed by two boost converters connected in parallel and a storage capacitor at the output. The circuit schematic of the interleaved boost PFC can be seen in figure 2.8. The diode bridge rectifies the input sinusoidal voltage to a varying DC voltage. With help of the boost stage and by adjusting the duty cycle of the transistors the current waveform can be placed in phase with the voltage waveform. Finally the output capacitor will filter out the AC component and provide the load with a DC voltage. The two boost converters in the interleaved PFC will operate 180 degrees out of phase [5] and the input current will be the sum of the two currents flowing through inductor L_1 and L_2 . Due to the interleaving and the fact that the inductor currents flowing through L_1 and L_2 are out of phase, the ripple current flowing through the inductors tend to cancel each other out, leading to a lower input current ripple [5]. Also the advantage of interleaving two boost converters is that it makes the converter more suitable for high power applications. When the interleaving is utilized the current flowing through the transistors will be lower than in the case of the conventional active boost PFC [6]. This will lead to better performance of the converter when it comes to efficiency and thermal management which is important at high power ratings. Another result of interleaving is the size reduction of both the boost inductors as well as the EMI filter [6]. The output capacitor high frequency ripple is also reduced as a result of interleaving. Although the Interleaved Boost PFC is more suitable for higher power application and has better performance than the conventional active boost PFC, it still has the drawback that come with the use of a diode bridge rectifier at the input. The bridge will cause additional losses and problems with thermal management in the converter. In the following section, PFC topologies which eliminate the input diode bridge rectifier will be discussed.

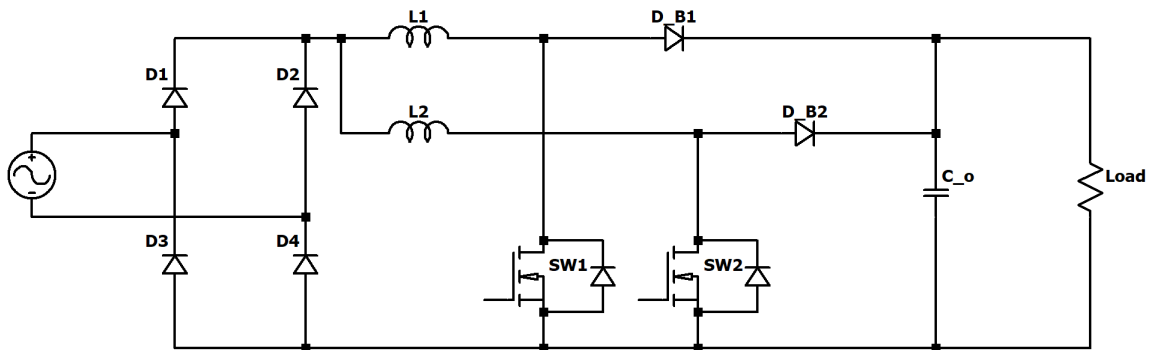


Figure 2.8: Schematic of Interleaved boost PFC

2.3 Bridgeless Power Factor Correction Topologies

To solve the problem of heat management and to further increase the efficiency of the PFC, bridgeless topologies can be used. Bridgeless PFC topologies eliminate the diode bridge rectifier at the AC input which reduces number of diode forward drops in the path of the current which flows from the AC source to the load. This will result in lower conduction losses in the circuit. As there are many different bridgeless PFC topologies to choose from, it was necessary to conduct a literature study to determine which topologies are most suitable for the application. The operating requirements for the PFC application as well as other important parameters that need to be considered when selecting suitable topologies can be seen in section 1.3.

From the literature study it was found that most suitable bridgeless PFC topologies are in some way based on the boost converter topology. This is the case for two reasons, the first reason is that for this project one of the requirements was that the output voltage of the PFC should be higher than the input voltage and this can be achieved with the help of a boost converter. The second reason was that the input current of the boost converter operated in CCM has low conducted electromagnetic interference when compared to other topologies such as buck-boost or buck converter for high power operation [6]. Three topologies were selected, which are thought to be the most suitable for the given application. These topologies are the Semi-Bridgeless Boost PFC, the Bridgeless Interleaved Boost PFC and the Totem-pole PFC utilizing Gallium Nitride transistors. These topologies were found suitable because they can operate at high output power levels > 3 kW, have a good efficiency $\eta > 92\%$, yield high power factor, have low input current ripple and have low electromagnetic interference. Other topologies which were investigated include bridgeless PFC topologies based on SEPIC, CUK, Buck, Buck-Boost and Flyback converters. Some other bridgeless boost topologies which were investigated include the Bridgeless boost PFC with a bidirectional switch, the Three level Bridgeless boost PFC and Bridgeless Pseudo-boost PFC. These topologies were found to be inferior compared to the three chosen topologies in terms of possibility to handle high output power, efficiency, EMI, component count and/or complexity. In the text below the operational principles of Semi-Bridgeless Boost PFC, Bridgeless Interleaved Boost PFC and Totem-pole PFC utilizing Gallium Nitride transistors will be presented.

2.3.1 Semi-Bridgeless PFC

To further improve the efficiency and thermal performance of the Active Boost PFC the diode bridge rectifier at the input needs to be removed. One topology which manages to remove the input diode bridge rectifier and increase the efficiency of PFC circuit is the Semi-Bridgeless Boost PFC. This topology consists of two Boost converters where one operates during the positive half cycle of the AC input and the other one for the negative half cycle. Two additional slow diodes D_2 and D_4 are introduced to connect the ground to the neutral terminal and provide a return path

for the current, see figure 2.9. The addition of the return diodes prevent the input voltage from floating and rather being referenced to ground [7]. As a result, the input voltage sensing is made easier because a voltage divider can be used instead of a low frequency transformer or optocoupler [8]. Another benefit of the return diodes is that the EMI performance of the PFC will be improved. As mentioned these diodes provide the return path for the current but all of the current will not always flow through them. A large portion of the current will return through the body diode of the non-switching MOSFET. The reason this occurs is due to the low impedance of the inductor at line frequency [8]. How large portion of the current that flows through the body diode and the return diodes is determined by the component characteristics. The double inductors reduce the dV/dt from the switches making the signal more stable and less prone to peaking. Two inductors help with thermal management since they split the input and are only active during one half cycle respectively. This circuit is relatively simple to control and drive because both transistors can be driven with the same gate signal. This topology is suited for high power application $>1kW$ but due to the higher component count it will have higher cost when compared to the conventional Active Boost PFC. The schematic of the Semi-Bridgeless PFC can be seen in figure 2.9 and detailed operation of the PFC for both the positive and negative half cycles will be presented in the text below.

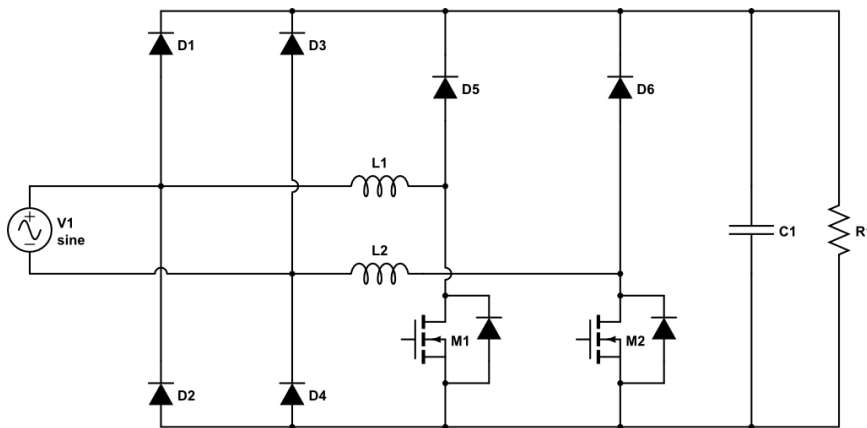


Figure 2.9: Schematic of the semi bridgeless boost PFC

2.3.1.1 Converter Operation for Positive Half Cycle

The Semi-Bridgeless PFC converter operation for the positive half cycle can be divided into two different states, when the transistor M_1 is conducting and when it is not. When it isn't conducting as can be seen in figure 2.10, the source and inductor L_1 supplies the load and capacitor with current. The current flows through D_5 and returns through D_4 to the source. In the other state M_1 is conducting and the inductor, L_1 is charging whilst the capacitor is discharged to keep the load voltage steady. The current flows through M_1 and D_4 to charge the inductor.

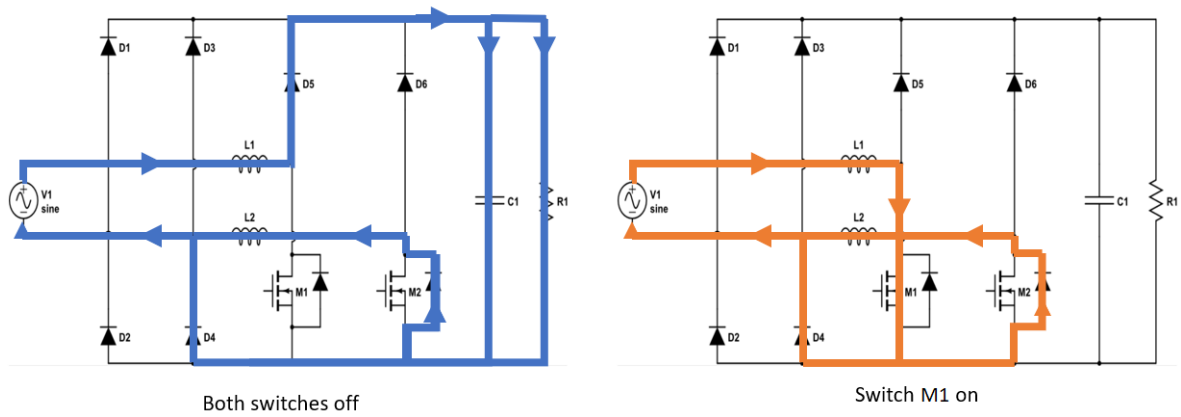


Figure 2.10: Converter operation for positive half cycle

2.3.1.2 Converter Operation for Negative Half Cycle

Just as for the positive half cycle there are two different states of operation for the negative half cycle. The first one being when the switch M_2 isn't conducting and the current is discharged from inductor L_2 and the supply to the output and capacitor. The current flows through and from the inductor, through the diode D_6 and then back again through the return diode D_2 . The other state is when the switch is conducting and the inductor, L_2 is charged with current flowing through the transistor M_2 and returning through D_2 whilst the capacitor is discharged to the load to keep the voltage at the desired level.

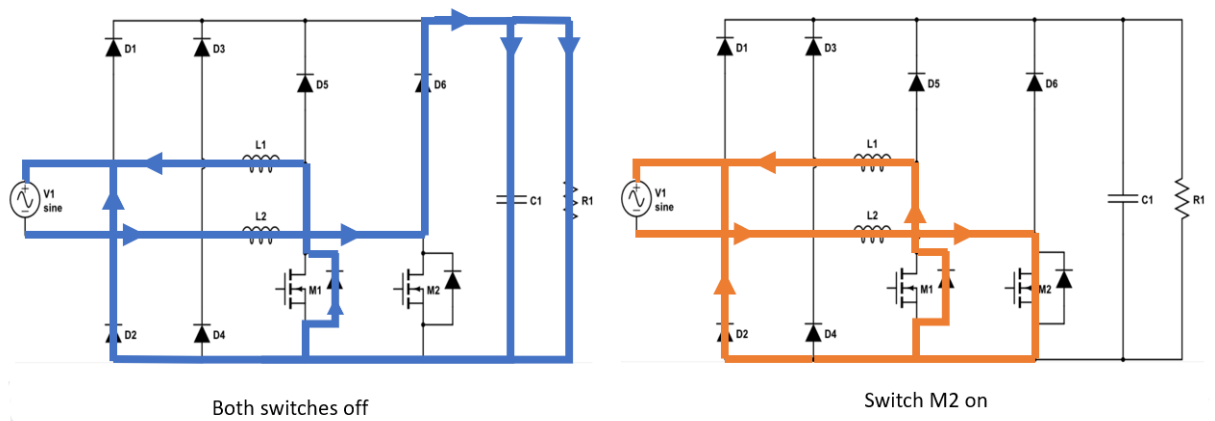


Figure 2.11: Converter operation for negative half cycle

Design challenges

The Semi-Bridgeless PFC is a promising topology with its advantages but there are some challenges that need to be overcome in the design stages. Some of these challenges are mentioned below.

Reverse recovery

One of the challenges with this topology is that the output diodes will cause severe reverse-recovery problems which occur due to the high output voltage and high diode forward current [6]. The reverse-recovery of the output diodes will be more significant during high switching frequencies and can lead to additional turn-on losses and higher EMI noise. For this reason the reverse recovery can be a bottleneck when it comes to high switching frequencies [9]. In order to improve the reverse recovery of the output diodes, Silicon Carbide (SiC) Schottky Diodes which have no reverse recovery charge can be used.

Current Sensing

Current sensing for this topology is relatively complex. Because all of the current will not return through the return diodes it is not possible to use a single shunt resistor to measure the current like in the case of the Active Boost PFC. One way of measuring the current which is mentioned in [10] is to use four current transformers to measure the current in both switches as well as the current flowing through the output capacitor and the load. These currents are then summed together and applied to a shunt resistor which is used to measure the total current. This method will lead to a more complex control circuit and will also need some sort of reset network which will demagnetize the current transformers [10]. This can be simplified with a dedicated controller IC such as UCC28070 which will eliminate the need for modification of the sensing circuit. Another way is to use a differential mode amplifier to sense the current in the front of the PFC inductor.

2.3.2 Bridgeless Interleaved Boost PFC

The Bridgeless Interleaved (BLIL) Boost PFC is similar to the Interleaved Boost PFC but the diode bridge rectifier at the input is removed. The number of semiconductors in this topology will be the same as in the Interleaved Boost PFC but two additional transistors and two fast switching diodes will replace the four slow diodes of the input bridge of the Interleaved PFC. The circuit schematic for the Bridgeless Interleaved Boost PFC can be seen in the figure 2.12. This topology will retain the advantages of the Interleaved PFC such as good thermal performance, low input current ripple, good EMI and high efficiency. Due to the elimination of the input bridge and interleaving of four boost converters instead of two, an improved efficiency and better thermal performance can be obtained which makes this topology suitable for high power applications above 3 kW [5]. The detailed operation of BLIL Boost PFC for both the positive and negative half cycles will be presented in the text below.

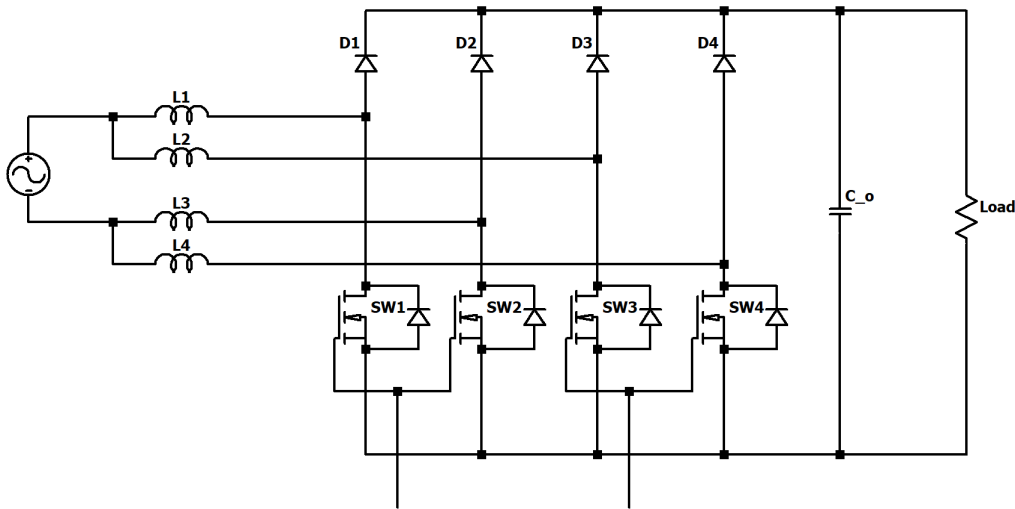


Figure 2.12: Schematic of Bridgeless Interleaved PFC

2.3.2.1 Converter Operation for Positive Half Cycle

During the positive cycle of the AC input voltage, the switches SW_1 and SW_2 will be conducting. The current will then flow from the input through the inductors L_1 , switches SW_1 and SW_2 and finally through the inductor L_2 before returning to line. At this time the current will magnetize the inductors resulting in energy being stored within them. When the switches SW_1 and SW_2 are turned off, the stored energy inside the inductors will be released in form of a current which will then flow through the diode D_1 , the load and finally through the body diode of the switch SW_2 before returning to the line. A similar operation will happen for switches SW_3 and SW_4 but it will be delayed with 180° . When switches SW_3 and SW_4 are turned on the current will flow from input through the inductor L_2 and switches SW_3 and SW_4 finally making its way through the inductor L_4 before returning to the line. The energy will be stored in these inductors during this time and when the SW_3 and SW_4 are turned off this energy will be released in form of a current that flows through diode D_3 , the load and the body diode of the SW_4 before returning to the line. The current paths for the positive cycle operation can be seen in figure 2.13.

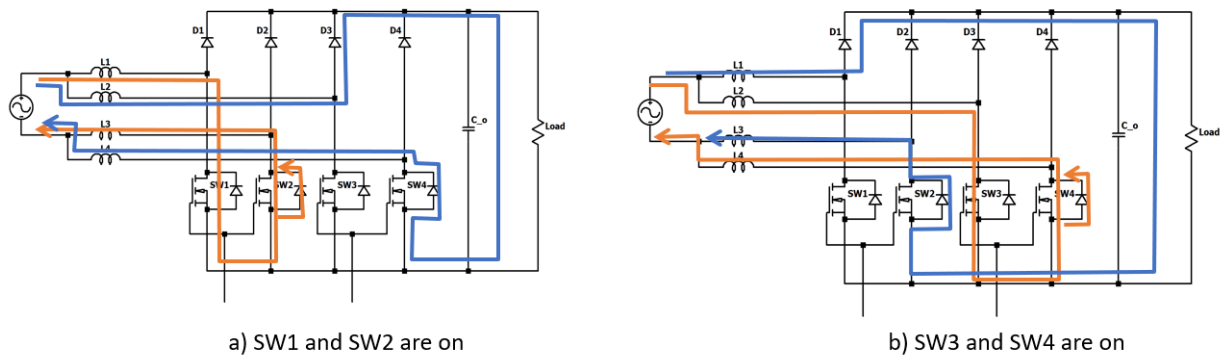


Figure 2.13: Positive cycle operation for Bridgeless Interleaved Boost PFC

2.3.2.2 Converter Operation for the Negative Half Cycle

During the negative half cycle the switches SW_1 and SW_2 are turned on and the current will flow through the inductor L_3 , switches SW_1 and SW_2 and finally through L_1 and back to the source. During this time the inductors L_1 and L_3 are charged. When the switches turn off, the energy stored inside the inductors will be released in form of a current which will go through diode D_2 , the load, the body diode of the switch SW_1 and L_1 back to the source. Similar operation happens for the switches SW_3 and SW_4 but with a 180° phase delay.

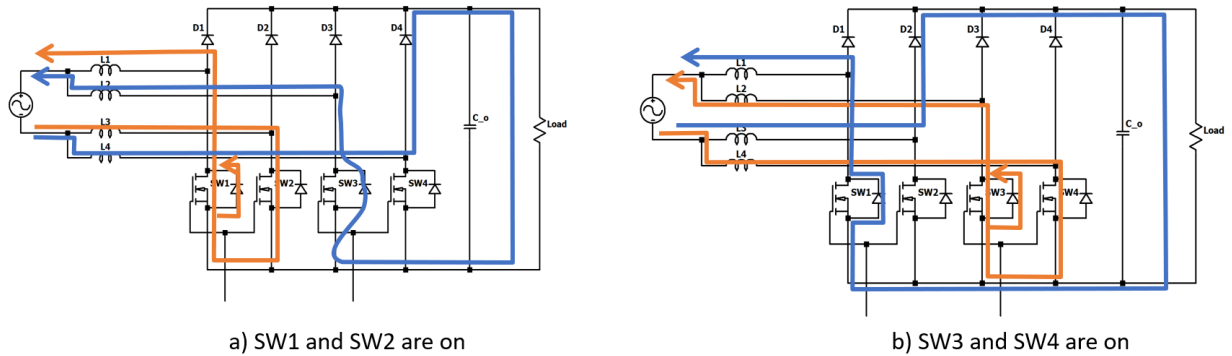


Figure 2.14: Negative cycle operation for Bridgeless Interleaved Boost PFC

The operation of the Bridgeless Interleaved Boost PFC will also depend on the duty cycle and the operation of the converter will be different for duty cycles which are greater than 0.5 compared to the duty cycles that are lower than 0.5. In the text below a detailed description will be given of the converters operations for duty cycles, $D > 0.5$ and $D < 0.5$ for the positive half cycle but the operation for the negative half cycle will be similar to the one presented below.

Converter Operation for Positive Half Cycle and Duty Cycle, $D > 0.5$

The steady state wave forms for duty cycles > 0.5 of the converter are shown in figure 2.15 a), these wave forms are obtained from [5]. The operation of the converter during these conditions can be divided into four different intervals, these will be explained in the text below.

Interval 1, t_1-t_2 : At time t_1 , the switches SW_1 and SW_2 will be on, while switches SW_3 and SW_4 will be off. In this interval the current going through L_1 and L_3 will increase linearly and charge the inductors. At the same time the current going through the inductors L_2 and L_4 will decrease linearly and energy stored inside the inductors will be transferred to the load.

Interval 2, t_2-t_3 : At time t_2 the switches SW_3 and SW_4 will be turned on while the switches SW_1 and SW_2 will remain on. The current flowing through all four inductors will increase linearly and all four inductors will be charged.

Interval 3, t_3-t_4 :

At time t_3 the switches SW_3 and SW_4 will remain on while switches SW_1 and SW_2 will be turned off. During this interval the current through inductors L_2 and L_4 will increase linearly, which will charge the inductors. The energy stored inside the inductors L_1 and L_3 will be released to the load through diode D_1 , output capacitance C_o and body diode of switch SW_2 . During this interval the current through L_1 and L_3 will decrease linearly.

Interval 4, t_4 - t_5 : During this interval all four switches will be on and the current through all four inductors will increase linearly which will charge the inductors. Operation inside the interval t_5 - t_6 will be the same as in interval 1.

Converter Operation for Positive Half Cycle and Duty Cycle, $D < 0.5$

The steady state wave forms for duty cycles < 0.5 of the converter are shown in figure 2.15 b). The operation of the converter during these conditions can be divided into four different intervals, these will be explained in the text below.

Interval 1, t_1 - t_2 :

During this interval all four switches will be off. The energy stored inside the inductors will be released to the load through D_1 , D_3 , output capacitance and body diodes of switches SW_2 and SW_4 . The current flowing thorough all four inductances will decrease linearly during this interval.

Interval 2, t_2 - t_3 :

At time t_2 the switches SW_1 and SW_2 will turn on, while SW_3 and SW_4 remain off. During this interval the current flowing through inductances L_1 and L_3 will increase linearly which will charge up the inductors. Inductors L_2 and L_4 will continue transferring the stored energy to the load which will result in a linear decrease of the current flowing through these inductors.

Interval 3, t_3 - t_4 :

During this interval all four switches will be off. All four inductors will release the stored energy to the load, which will result in a linear decrease in the current flowing through the inductors.

Interval 4, t_4 - t_5 :

At time t_4 switches SW_3 and SW_4 will be turned on while SW_1 and SW_2 remain off. The current through L_2 and L_4 will increase linearly and charge the inductors. Energy stored in L_1 and L_3 will be transferred to the load. Due to this the current flowing through these inductors will decrease linearly. The operation inside the interval t_5 - t_6 will be similar to the interval 1. The detailed converter operation during the negative half cycle will not be given here since it is similar to the positive half cycle operation.

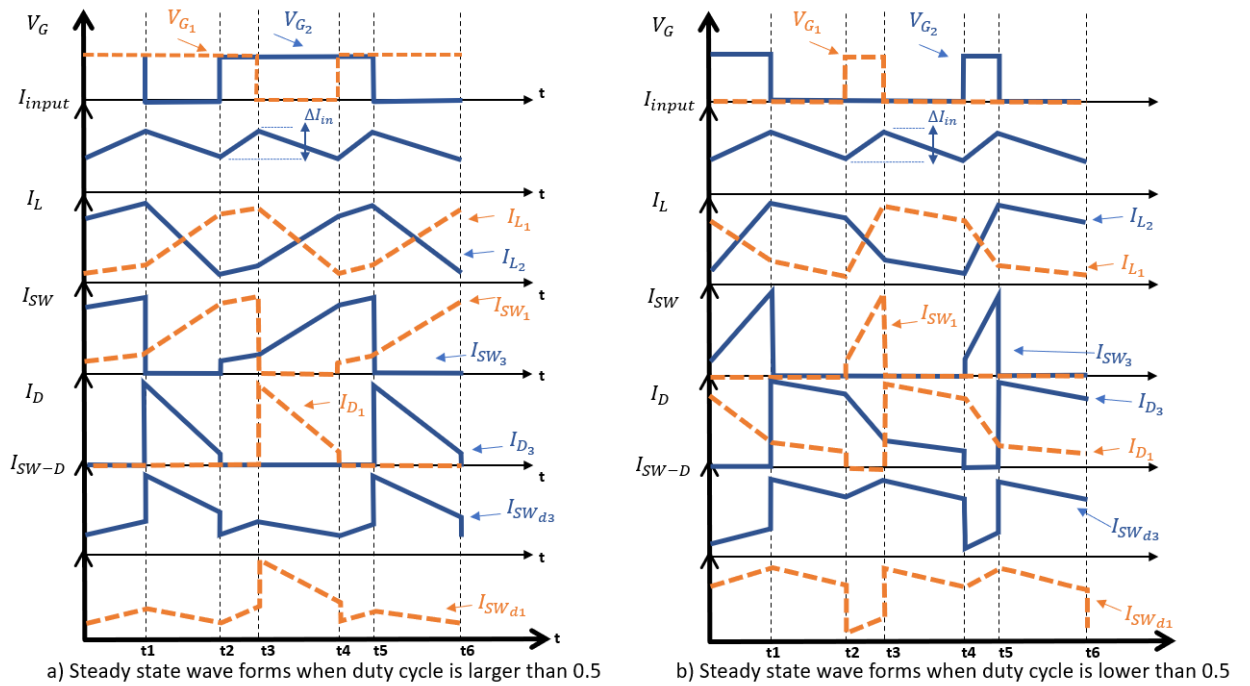


Figure 2.15: Steady state wave forms for the positive half cycle and both when duty cycle is greater than 0.5 in a) and smaller than 0.5 in b). Wave forms are obtained from [5]

Design Challenges

Reverse Recovery

The Bridgeless Interleaved Boost PFC encounters the same issues as the Semi-Bridgeless Boost PFC when it comes to the reverse recovery of the boost diodes. Due to the fact that the converter will operate in CCM, this will lead to significant reverse-recovery losses of the diodes. Same as in the case of the Semi-Bridgeless PFC, silicon carbide diodes with no reverse-recovery charge can be used to overcome this issue.

Increased Complexity

Another challenge with this topology is that due to the increased number of components the complexity of the drive and control circuits will increase. Due to the fact that the MOSFETs will operate in pairs with each pair being 180 degrees phase shifted from each other, sophisticated control algorithms might be required to make sure that the phase shift between gate signals of the MOSFET pairs is exactly 180 degrees.

2.3.3 Totem-Pole Bridgeless Boost PFC Utilizing GaN Transistors

Bridgeless Totem-Pole PFC aims to, in a similar manner as the other two bridgeless PFC topologies, improve the efficiency and power density of the PFC by reduc-

ing the number of semiconducting devices in the path of the current. The circuit schematic of this topology can be seen in figure 2.16. The topology is similar to the Semi-Bridgeless PFC topology but instead of having two switching legs with one transistor on each leg, both transistors are placed on the same switching leg.

This topology has been proposed in the past for other applications but its use has been limited. The reason for this is the reverse recovery issues of the Silicon (Si) MOSFETS body diodes in the totem-pole configuration. Due to the poor reverse recovery performance of the Si MOSFETS this topology was limited to the DCM or CrCM mode of operation which are not suitable for high power applications [11], [12]. In recent years with the rise of wide band gap semiconductor technologies such as Gallium Nitride (GaN) transistors, this topology has been more attractive for high power applications. The reason for this is that the GaN transistors unlike the Si MOSFETS does not have the intrinsic body diode. Due to this the reverse recovery issue caused by the body diode is eliminated. The diodes D_1 and D_2 can be slow recovery diodes, meaning a lower lower price. To further increase the efficiency of this topology, the diodes can be changed out with slow switching MOSFET transistors. Due to the fact that the output is never floating with respect to the input, the input voltage measurement is relatively easy to implement where a simple voltage divider can be used [11]. Also due to the non-floating output voltage, this topology has a good EMI performance. This circuit has the advantage of high efficiency, low device count and high device utilization. A more detailed converter operation is given in the text below.

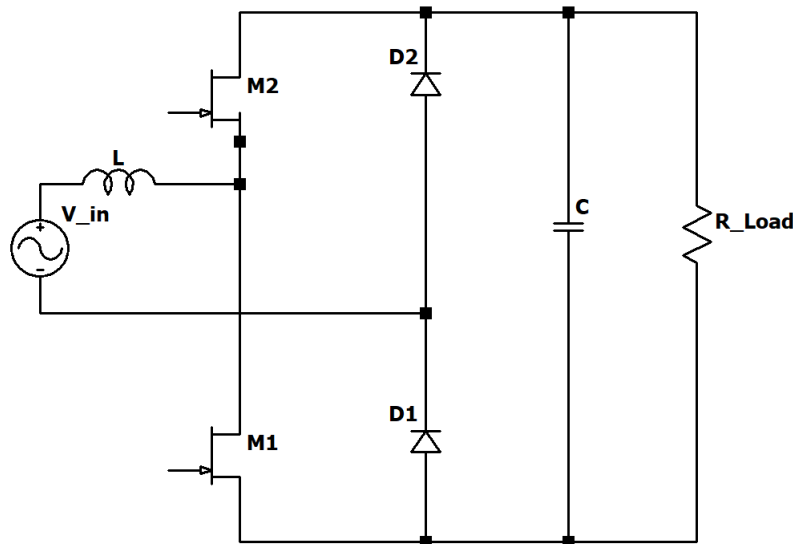


Figure 2.16: Schematic of the bridgeless totem pole boost PFC

2.3.3.1 Converter Operation for Positive Half Cycle

Totem-Pole PFC has two different states of operation. The first state is when M_2 is conducting and M_1 isn't meaning the input and the inductor is supplying the load and charging the capacitor. The current flows from the inductor and input through

the capacitor and load through the diode D_1 and back to the input. The other state is when M_2 isn't conducting but M_1 is, meaning the inductor is charged by the input and the capacitor is discharging through the load to keep the voltage level constant. The current flows through inductor, through M_2 and then flows back to the input by D_1 . This can be seen in figure 2.17.

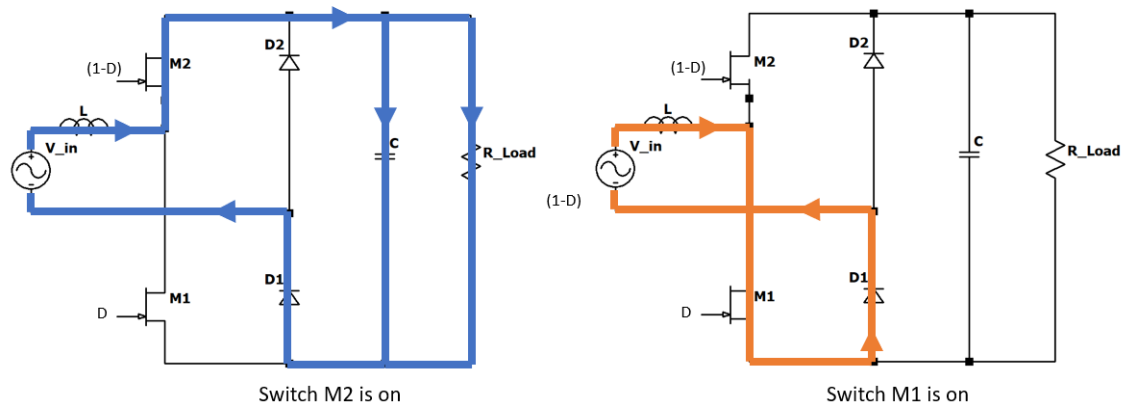


Figure 2.17: Positive cycle operation of the bridgeless totem pole boost PFC

2.3.3.2 Converter Operation for Negative Half Cycle

The negative half cycle also consists of two states of operation. The first one being when M_2 isn't conducting but M_1 is hence the inductor and input supplies the load and capacitor. The current flows through D_2 by the capacitor and load and back to the input through the switch M_1 . The other state being when M_2 conducts and M_1 isn't, the inductor is charged whilst the capacitor keeps the voltage at the output constant. The current flows through the diode D_2 first and then through M_1 to charge the inductor as can be seen in figure 2.18

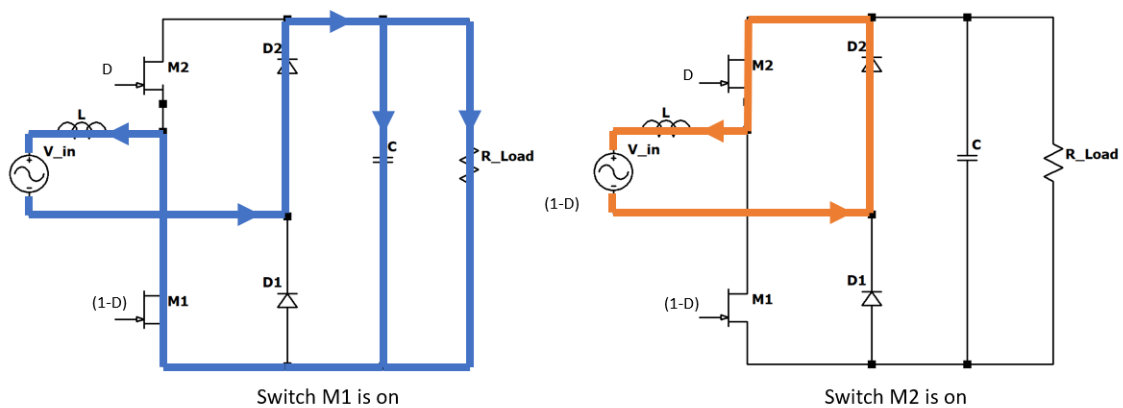


Figure 2.18: Negative cycle operation of the bridgeless totem pole boost PFC

Design challenges

Stringent Gate Driver Requirements

The challenge with the GaN transistors when compared to the Si MOSFETs is that the gate driver requirements are more stringent in terms of the gate-to-source (V_{GS}) voltage range. While the maximum allowed V_{GS} for Si MOSFETs might be as high as +30V, the GaN devices have much lower allowed V_{GS} which is generally closer to +6V [13]. To fully turn on the GaN transistors the V_{GS} of generally +5V needs to be applied. This gives a quite narrow V_{GS} range for the the GaN transistors and an accurate gate driver is needed to drive the transistors.

High Side Transistor Driving

Due to the Totem-pole configuration, a so called high-side driving of the transistor is required. The voltage at the source terminal of the high-side transistor will be varying and this will make the driving of the transistor more complicated. The transistor is turned on when a certain voltage difference occurs between the gate and source terminals of the transistors. The source terminal of the high-side transistor is connected to the input voltage which means that the voltage at source terminal can approximately reach the peak of the input voltage. This means that to turn the transistor on, a higher voltage is needed on the gate of the transistor which is non-practical. This problem can be solved with isolated gate driver or so called bootstrap configuration for the high-side switch but both of these methods will introduce more complexity and higher cost to the circuit.

Another issue which occurs due to the Totem-pole configuration is that a so called dead time needs to be introduced in the gate signals of the transistors. Dead time is a short time where none of the transistors are conducting and is introduced in order to prevent the high shoot-through current that can occur if both of the switches are on at the same time. The length of the dead time will have an impact on the performance of the converter and should be as low as possible.

2.4 Analytical Modeling

Analytical modeling is an important part of converter design. Values and equations derived in analytical modeling are used to determine proper component selection for the converter. These values are also very helpful when simulations of the converter are performed and can be used to determine if the simulation results are realistic. This chapter will present analytical modeling of the Semi-Bridgeless Boost PFC, Bridgeless Interleaved Boost PFC as well as the Bridgeless Totem-pole PFC. The equations derived in this chapter follow the method described in [14] and [15].

The following assumptions are made in order to derive the equations below:

1. The PFC is operating in CCM operation
2. Power Factor is assumed to be equal to unity
3. The output voltage of the PFC is DC without voltage ripple

2.4.1 Semi-Bridgeless PFC and Bridgeless Totem-pole PFC

MOSFET RMS Current

If the switching frequency is much higher than the input AC line frequency the RMS current through the transistor can be approximated as a double integral. The instantaneous transistor current is first squared and integrated to find the average value over a switching period and thereafter it is integrated once more to find the average value over the AC line period. Finally a square root of the whole expression is done to obtain the transistor RMS current.

$$I_{SW-RMS} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{1}{T_s} \int_t^{t+T_s} i_{SW}^2(\tau) d\tau dt} \quad (2.4)$$

The duty cycle of the boost converter is given as

$$D(t) = 1 - \frac{V_{in-peak} |\sin(\omega t)|}{V_o} \quad (2.5)$$

In the case of the boost converter the current flowing through the transistor $i_{SW}(t)$ is equal to the input current when the transistor is on and is zero when the transistor is off. Therefore the average of transistor current squared (i_{SW}^2) over a single switching period will be

$$\begin{aligned} [i_{SW}^2]_{T_s} &= \frac{1}{T_s} \int_t^{t+T_s} i_{SW}^2(t) dt = D(t) \cdot i_{in}^2(t) \\ &= (I_{in-peak} \cdot \sin(\omega t))^2 \cdot \left(1 - \frac{V_{in-peak} |\sin(\omega t)|}{V_o}\right) \end{aligned} \quad (2.6)$$

By instering (2.6) into (2.4) the following expression is obtained

$$I_{SW-RMS} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} I_{in-peak}^2 \left(1 - \frac{V_{in-peak} |\sin(\omega t)|}{V_o}\right) \cdot \sin^2(\omega t) dt} \quad (2.7)$$

The equation above can be simplified to

$$I_{SW-RMS} = \sqrt{\frac{2}{T_{ac}} I_{in-peak}^2 \int_0^{\frac{T_{ac}}{2}} \left(\sin^2(\omega t) - \frac{V_{in-peak} \cdot \sin^3(\omega t)}{V_o}\right) dt} \quad (2.8)$$

Finally by solving the integral term, the transistors RMS current can be obtained as in the expression below

$$\begin{aligned}
 I_{SW-RMS} &= \sqrt{\frac{1}{\pi} I_{in-peak}^2 \int_0^{\pi} \left(\sin^2(wt) - \frac{V_{in-peak} \cdot \sin^3(wt)}{V_o} \right) dt} \\
 &= I_{in-peak} \sqrt{\frac{1}{2} - \frac{4V_{in-peak}}{3\pi V_o}} = \frac{P_{in}}{V_{in-RMS}} \sqrt{1 - \frac{8V_{in-peak}}{3\pi V_o}} \quad (2.9) \\
 &\rightarrow P_{in} = \frac{P_o}{\eta}, \text{ where } \eta = \text{Efficiency of converter}
 \end{aligned}$$

Boost Diode Current

The RMS current for the boost diode can be obtained with similar methodology used for the transistor RMS current calculation. Assuming efficiency, $\eta = 100\%$, the duty cycle of the boost diode is expressed as

$$D_{diode}(t) = 1 - D(t) = \frac{V_{in-peak} \cdot |\sin(wt)|}{V_o} \quad (2.10)$$

In the same manner as the transistor current, the average of the squared diode current $i_D^2(t)$ can be expressed as

$$[i_D^2] = i_{in}^2(t) \cdot D_{diode}(t) = (I_{in-peak} \cdot \sin(wt))^2 \cdot \frac{V_{in-peak} |\sin(wt)|}{V_o} \quad (2.11)$$

The boost diode RMS current is

$$\begin{aligned}
 I_{D-RMS} &= \sqrt{\frac{1}{\pi} I_{in-peak}^2 \frac{V_{in-peak}}{V_o} \int_0^{\pi} \sin^3(wt) d(wt)} \\
 &= I_{in-peak} \sqrt{\frac{4V_{in-peak}}{3\pi V_o}} = \frac{P_{in}}{V_{in-RMS}} \sqrt{\frac{8V_{in-peak}}{3\pi V_o}} \quad (2.12)
 \end{aligned}$$

Inductor RMS current

The inductor RMS Current is defined as

$$I_{L-RMS} \approx I_{in-RMS} = \frac{P_{in}}{V_{in-RMS}} \quad (2.13)$$

Capacitor Current

The output current of the filter capacitor consists of two components, a low frequency component $I_{Cout-LF}$ which occurs at twice the line frequency and a high

frequency component $I_{Cout-HF}$ at the switching frequency. Expressions for the both components can be formulated as.

$$I_{Cout-LF} = \frac{P_{in}}{\sqrt{2}V_o} \quad (2.14)$$

$$I_{Cout-HF} = \sqrt{\left(\frac{P_{in}}{V_o} \sqrt{\frac{16V_o}{6\sqrt{2}V_{in-RMS}} - \frac{P_o^2}{P_{in}^2}}\right)^2 - \left(\frac{P_{in}}{\sqrt{2}V_o}\right)^2} \quad (2.15)$$

Boost Inductor Calculation

The design of the boost inductor is done for the worst case scenario and that is when the input voltage is at its lowest. In this case that is 86 V RMS. The inductor design starts with first calculation of the duty cycle needed to boost the lowest input voltage of 86 V to the necessary output voltage of 405 V. This was calculated as

$$D_{86V} = \frac{V_{out} - \sqrt{2} \cdot V_{in,min}}{V_{out}} = \frac{405 - \sqrt{2} \cdot 86}{405} = 0.6997 \quad (2.16)$$

Thereafter the RMS input current as well as the inductor ripple current are calculated, see

$$I_{In,RMS} = \frac{P_{out}}{V_{in,min,RMS} \cdot \eta} = \frac{3000}{86 \cdot 0.95} = 36.72A \quad (2.17)$$

$$\Delta I_L = \frac{P_{out} \cdot \sqrt{2} \cdot 0.25}{V_{in,RMS} \cdot \eta} = \frac{3000 \cdot \sqrt{2} \cdot 0.25}{86 \cdot 0.95} = 12.98A \quad (2.18)$$

In this case the maximum allowed inductor ripple was set to 25 % and efficiency η of the converter was assumed to be 95 %. Finally the inductance for both of the inductors can be calculated as

$$L_1 = L_2 = \frac{V_{in,min} \cdot \sqrt{2} \cdot D_{86V}}{\Delta I_L \cdot f_{sw}} = \frac{86 \cdot \sqrt{2} \cdot 0.6997}{12.98 \cdot 100000} = 65.6\mu H \quad (2.19)$$

The switching frequency of the converter is 100 kHz.

Output Capacitor Calculation

As written in [16], there are three main factors to dimensioning the output capacitors, the voltage ripple, the hold up time and the current going through the capacitor. These three factors are described in the following three equations where a resistive load is assumed.

$$V_{ripple(p-p)} = \frac{P_{out}}{2 \cdot \pi \cdot f_{line} \cdot C_{out} \cdot V_{out}} \quad (2.20)$$

$$I_{Cout(rms)} = \sqrt{\frac{32 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}}\right)^2} \quad (2.21)$$

$$t_{hold-up} = \frac{C_{out} \cdot (V_{out}^2 - V_{min}^2)}{2 \cdot P_{out}} \quad (2.22)$$

The hold up time and the allowed voltage ripple are often given depending on the load and specific use which means that (2.20) and (2.22) can be re-written to give the wanted capacitor value. The new equations become

$$C_{out} = \frac{P_{out}}{2 \cdot \pi \cdot f_{line} \cdot V_{ripple(p-p)} \cdot V_{out}} \quad (2.23)$$

$$C_{out} = \frac{t_{hold-up} \cdot 2 \cdot P_{out}}{(V_{out}^2 - V_{min}^2)} \quad (2.24)$$

By solving these two equations one obtains two different values for the capacitance where the highest value is chosen. The output voltage ripple is set to 10V, the hold-up time is 20 ms and the minimum voltage at the PFC output is set to 370 V. With these values the output capacitance of the PFC is calculated to be 4.4 mF.

2.4.2 Bridgeless Interleaved Boost PFC

The equations for the Bridgeless Interleaved Boost PFC are derived in the same manner as the Semi-Bridgeless PFC. One thing to note is that due to the interleaving the Bridgeless Interleaved PFC is dimensioned for half of the output power rating and not for full power as the Semi-Bridgeless PFC.

MOSFET RMS Current

The transistor RMS current is calculated as.

$$I_{SW-RMS} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{1}{T_s} \int_t^{t+T_s} i_{SW}^2(\tau) d\tau dt} = \frac{P_{in}}{2V_{in-RMS}} \sqrt{1 - \frac{8V_{in-peak}}{3\pi V_o}} \quad (2.25)$$

Boost Diode RMS Current

The RMS current flowing through the boost diode will be

$$I_{D-RMS} = \sqrt{\frac{1}{\pi} I_{in-peak}^2 \frac{V_{in-peak}}{V_o} \int_0^\pi \sin^3(wt) dt} = \frac{P_{in}}{2V_{in-RMS}} \sqrt{\frac{8V_{in-peak}}{3\pi V_o}} \quad (2.26)$$

InDuctor RMS Current

The inductor RMS current flowing through each inductor will be

$$I_{L-RMS} \approx \frac{I_{in-RMS}}{2} = \frac{P_{in}}{2V_{in-RMS}} \quad (2.27)$$

Capacitor Current

The low and high frequency components of the output capacitor current are given as.

$$I_{Cout-LF} = \frac{\sqrt{2}P_o}{2V_o} \quad (2.28)$$

$$I_{Cout-HF} = \frac{P_{in}}{V_o} \sqrt{\frac{16V_o}{6\pi V_{in-peak}} - \frac{P_o^2}{P_{in}^2}} \quad (2.29)$$

Boost Inductor Calculation

The inductor value is calculated as.

$$L = \frac{V_{out}}{4 \cdot f_{sw} \cdot \Delta I} \quad (2.30)$$

The peak-peak current ripple ΔI is $0.4I_{in,RMS}$. Due to the ripple cancellation phenomenon in the Bridgeless Interleaved PFC the current ripple is allowed to be higher when compared to the Semi Bridgeless and Totem-pole PFC. The output capacitance is calculated in the same manner as for the Semi-Bridgeless PFC.

2.5 Small Signal Models of Bridgeless PFC Topologies

Small signal models represent a linearized system. The large signal model is evaluated at a steady state operating point and consider the dynamics for a small signal perturbation

2.5.1 Semi Bridgeless and Bridgeless Totem-pole Boost PFC

The small signal model for the Semi-Bridgeless and the Totem-Pole topology will be exactly the same which means that the derivations will also be identical. In this section the Semi-Bridgeless small signal model will be derived. First and foremost the averaged large signal model needs to be derived to get necessary parameters to derive the small signal model. This is done by inserting the averaged current and voltage from the four states described in converter operation for positive and negative half cycle. As described in sections 2.5.1, 2.5.2 and 2.5.3, in the first two states the input voltage is positive and for the other two negative.

The first state being when M_1 is conducting and the inductor L_1 is charging.

$$\frac{di_{in}}{dt} = \frac{v_{in}}{L_1} \quad \frac{dv_{C1}}{dt} = -\frac{v_{C1}}{C_1 R_1} \quad (2.31)$$

Second state is when the M_1 isn't conducting and L_1 is supplying the capacitor and the load.

$$\frac{di_{in}}{dt} = \frac{v_{in} - v_{C1}}{L_1} \quad \frac{dv_{C1}}{dt} = \frac{i_{C1} + i_{R1}}{C_1} - \frac{v_{C1}}{C_1 R_1} \quad (2.32)$$

The third state is when M_2 is conducting and inductor L_2 is charging,

$$\frac{di_{in}}{dt} = \frac{v_{in}}{L_2} \quad \frac{dv_{C1}}{dt} = -\frac{v_{C1}}{C_1 R_1} \quad (2.33)$$

The fourth and final state is when M_2 isn't conducting and L_2 is supplying the capacitor and the load,

$$\frac{di_{in}}{dt} = \frac{v_{in} - v_{C1}}{L_2} \quad \frac{dv_{C1}}{dt} = \frac{i_{C1} + i_{R1}}{C_1} - \frac{v_{C1}}{C_1 R_1} \quad (2.34)$$

With the values of the voltage over the capacitor and the input current from (2.31) through (2.34) the large signal model can be built. Since the inductors L_1 and L_2 are assumed to have the same value the large signal model can be simplified to two matrix systems representing when the switches are on and when the switches are off. The both inductors are identical and thereby, $L_1 = L_2 = L$. So for the case when both switches are on i.e state one and three the matrix equation given below is obtained.

$$\begin{bmatrix} \frac{di_{in}}{dt} \\ \frac{dv_{C1}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C_1 R_1} \end{bmatrix} \cdot \begin{bmatrix} i_{in} \\ v_{C1} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{in} \quad (2.35)$$

The two matrices in 2.35 have representing parameters A_1 and B_1 respectively. The other matrix equation representing state two and four which represents when both switches are off is presented below in 2.36.

$$\begin{bmatrix} \frac{di_{in}}{dt} \\ \frac{dv_{C1}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_1} & -\frac{1}{C_1 R_1} \end{bmatrix} \cdot \begin{bmatrix} i_{in} \\ v_{C1} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{in} \quad (2.36)$$

The two matrices in eq 2.36 have representing parameters A_2 and B_2 respectively. The duty cycle needs to be accounted for and is done with duty cycle = D , $D' = 1 - D$. For state space averaging (2.35) is multiplied with D and (2.36) with D' . Both parts are combined to obtain matrix equations for all states which then can be simplified to a combined A and B matrices seen in (2.37) respectively.

$$\begin{aligned} \dot{x} &= (A_1 x + B_1 v_{in})D + (A_2 x + B_2 v_{in})D' \\ \rightarrow \dot{x} &= (A_1 D + A_2 D')x + (B_1 D + B_2 D')v_{in} \end{aligned} \quad (2.37)$$

To transform this new matrix system into the small signal model the duty cycle, V_{in} , V_{C0} and i_{in} need to be transformed. This is done by letting them be represented with a DC part plus a small signal ac part seen in equation 2.38.

$$D = D_{avg} + \hat{d} \quad v_{in} = V_{in-avg} + \hat{v}_{in} \quad x = X_{avg} + \hat{x} \quad (2.38)$$

The new values needs to be substituted in to equation 2.39, to get a non linear small signal model which can be seen in (2.39). To linearize this some assumptions need to be made, namely that products of two perturbation variables are neglectable compared to the rest and therefore considered equal to zero. This will give us the following eq 2.40.

$$\begin{aligned} \dot{x} = & (A_1(D_{avg} + \hat{d}) + A_2(1 - (D_{avg} + \hat{d}))) \cdot (X_{avg} + \hat{x}) \\ & + (B_1(D_{avg} + \hat{d}) + B_2(1 - (D_{avg} + \hat{d}))) \cdot (V_{in-avg} + \hat{v}_{in}) \end{aligned} \quad (2.39)$$

$$\dot{\hat{x}} = AX_{avg} + BV_{in-avg} + A\hat{x} + B\hat{v}_{in} + ((A_1 - A_2)X_{avg} + (B_1 - B_2)V_{in-avg})\hat{d} \quad (2.40)$$

To get the steady state model, this equation is evaluated with all the time derivatives in (2.40) being set to zero. The matrix A need to be inverted and this is done to solve for the matrix X_{avg} seen below.

$$\begin{aligned} \frac{dx_{avg}}{dt} = AX_{avg} + BV_{in-avg} = 0 \\ x_{avg} = -A^{-1}BV_{in-avg} \end{aligned} \quad (2.41)$$

$$\rightarrow X_{avg} = \begin{bmatrix} I_{in-avg} \\ V_{C1-avg} \end{bmatrix} = \begin{bmatrix} \frac{V_{in-avg}}{R_0(1-D)^2} \\ \frac{V_{in-avg}}{1-D} \end{bmatrix} \quad (2.42)$$

With this we can get the final and linearized model by incorporating 2.41 in 2.40. This gives us the small signal linearized state space model seen in equation 2.43.

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{v}_{in} + ((A_1 - A_2)X_{avg} + (B_1 - B_2)V_{in-avg})\hat{d} \quad (2.43)$$

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{C1} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{1-D}{C_1} & -\frac{1}{C_1R_1} \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{C1} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot \hat{v}_{in} + \begin{bmatrix} \frac{V_{in-avg}}{L(1-D)} \\ -\frac{V_{in-avg}}{C_1R_1(1-D)^2} \end{bmatrix} \cdot \hat{d} \quad (2.44)$$

The model can then be converted into s-domain to get the transfer fucitons, seen below.

$$\begin{aligned} ((A_1 - A_2)X_{avg} + (B_1 - B_2)V_{in-avg})\hat{d} = E\hat{d} \\ \text{With } \hat{v}_{in} = 0 \quad \rightarrow \quad \frac{\hat{x}(s)}{\hat{d}(s)} = (s1 - A)^{-1}E \\ \text{With } \hat{d} = 0 \quad \rightarrow \quad \frac{\hat{x}(s)}{\hat{v}_{in}(s)} = (s1 - A)^{-1}B \end{aligned} \quad (2.45)$$

$$\frac{\hat{x}(s)}{\hat{d}(s)} = \frac{\begin{bmatrix} \hat{i}_{in}(s) \\ v_{\hat{C}1}(s) \end{bmatrix}}{\hat{d}(s)} = \frac{1}{s^2 + \frac{s}{C_1 R_1} + \frac{(1-D)^2}{C_1 L}} \begin{bmatrix} (s + \frac{1}{C_1 R_1}) \left(\frac{V_{in-avg}}{L(1-D)} \right) + \frac{V_{in-avg}(1-D)}{C_1 R_1 L(1-D)^2} \\ \frac{V_{in-avg}}{C_1 L} - \frac{V_{in-avg}s}{C_1 R_1 (1-D)^2} \end{bmatrix} \quad (2.46)$$

$$\text{with } v_{\hat{C}1}(s) = 0 \rightarrow \frac{\hat{i}_{in}(s)}{\hat{d}(s)} = \frac{v_{in-avg}(2 + C_1 R_1 s)}{R_1(1-D)^3 \left(\frac{C_1 L s^2}{(1-D)^2} + \frac{Ls}{R_1(1-D)^2} + 1 \right)} \quad (2.47)$$

The transfer function for the output voltage depending on the input current can be seen below.

$$\frac{v_{\hat{C}1}(s)}{\hat{i}_{in}(s)} = \frac{v_{in-avg} \cdot R_1}{2 \cdot v_{C1}(R_1 C_1 s + 1)} \quad (2.48)$$

2.5.2 Bridgeless Interleaved Boost PFC

For the Bridgeless Interleaved Boost PFC, the methodology for finding the small signal model and transfer function is the same as for the Semi-Bridgeless PFC. The exception being how the system is analysed, the interleaved topology has four switches and two controllers. To fit the transfer function for use in one of these controllers the topology is effectively halved to be only two switches/legs where only one of the inductor currents is of interest. Firstly analyzing the different modes of operation and drawing the same conclusions as for semi bridgeless and totem pole PFC.

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{2 \cdot L} \quad \frac{dV_{C0}}{dt} = \frac{i_{L2}}{C_0} - \frac{V_{C0}}{R_{load} \cdot C_0} \quad (2.49)$$

$$\frac{di_{L1}}{dt} = \frac{V_{in} - V_{C0}}{2 \cdot L} \quad \frac{dV_{C0}}{dt} = \frac{i_{L1}}{C_0} - \frac{V_{C0}}{R_{load} \cdot C_0} \quad (2.50)$$

Since the system is symmetrical over positive and negative half cycles, only one of them needs to be considered. Here, the positive half cycle is chosen, as seen in the above equations. This gives the following matrix equations.

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{R_{load} \cdot C_0} \end{bmatrix}, X = \begin{bmatrix} i_{L1} \\ V_{C0} \end{bmatrix}, A_2 = \begin{bmatrix} 0 & \frac{-1}{2 \cdot L} \\ \frac{1}{C_0} & \frac{-1}{R_{load} \cdot C_0} \end{bmatrix}, B_1 = B_2 = \begin{bmatrix} \frac{1}{2 \cdot L} \\ 0 \end{bmatrix} \quad (2.51)$$

$$A = (A_1 \cdot D + A_2 \cdot (1-D)) = \begin{bmatrix} 0 & \frac{-(1-D)}{2 \cdot L} \\ \frac{1-D}{C_0} & \frac{-1}{R_{load} \cdot C_0} \end{bmatrix} \quad (2.52)$$

$$B = (B_1 \cdot D + B_2 \cdot (1-D)) = \begin{bmatrix} \frac{1}{2 \cdot L} \\ 0 \end{bmatrix} \quad (2.53)$$

introducing the same perturbations as in the earlier section using (2.38) through (2.40) and solving for X_{avg} we get the following equation.

$$X_{avg} = -A^{-1} B V_{in-avg} = - \begin{bmatrix} 0 & \frac{-(1-D)}{2 \cdot L} \\ \frac{(1-D)}{C_0} & \frac{-1}{R_{load} \cdot C_0} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{2 \cdot L} \\ 0 \end{bmatrix} V_{in-avg} = \begin{bmatrix} \frac{V_{in-avg}}{R_{load} \cdot (1-D)^2} \\ \frac{-V_{in-avg}}{D-1} \end{bmatrix} \quad (2.54)$$

Translating this to s-domain results in the transfer function for the current $\frac{i_{L1}(s)}{\hat{d}(s)}$ by doing the same operations as equations (2.43) through (2.47), as seen in the equations below.

$$\begin{bmatrix} \frac{di_{L1}(s)}{\hat{d}(s)} \\ \frac{dv_{C0}(s)}{\hat{d}(s)} \end{bmatrix} = \begin{bmatrix} s & \frac{1-D}{2 \cdot L} \\ \frac{D-1}{C_0} & s + \frac{1}{R_{load} \cdot C_0} \end{bmatrix}^{-1} \left(\begin{bmatrix} 0 & \frac{1}{2 \cdot L} \\ \frac{-1}{C_0} & 0 \end{bmatrix} \begin{bmatrix} \frac{V_{in-avg}}{R_{load} \cdot (1-D)^2} \\ \frac{-V_{in-avg}}{D-1} \end{bmatrix} \right) \quad (2.55)$$

$$\text{with } v_{in}(s) = 0 \quad \rightarrow \quad \frac{i_{L1}(s)}{\hat{d}(s)} = \frac{-2V_{in-avg} - C_0 R_{load} V_{in-avg} s}{R_{load}(D-1)^3 + 2C_0 L R_{load} s^2 (D-1) + L s (D-1)} \quad (2.56)$$

The transfer function for the output voltage depending on the input current can be seen below.

$$\frac{v_{\hat{C}0}(s)}{\hat{i}_{in}(s)} = \frac{v_{in-avg}}{2v_{C0}C_0s} \quad (2.57)$$

3

Simulations

3.1 Modeling of Topologies

The chosen topologies were first modeled in continuous time utilizing ideal components directly based on the theoretical values calculated in chapter 2. The circuits were then tested with a rudimentary control system which creates a constant duty cycle to the switches to ensure the functionality of the PFC topologies. In order to reduce the simulation time, the models were converted from continuous time domain to discrete time domain. The rudimentary control systems were then replaced with digital PI current controllers in an open loop configuration to test the power factor correction capability of the systems. Once it was ensured that the current controller were working as expected and were able to place the input current in phase with the input voltage, the systems were reconfigured to closed loop where another PI controller was introduced which controls the output voltage. The input and output signals were then observed to ensure the correct functionality of the whole system. The modeling of each topologies will be discussed in more detail in the sections below.

3.1.1 Semi-Bridgeless Boost PFC

The Simulink circuit model of the Semi-Bridgeless Boost PFC can be seen in figure 3.1. Modeling of this circuit is done using MOSFETs and diodes with ideal switching. This means that the switching behavior is assumed to be perfect and that the devices will behave as linear resistors with constant on resistance when they are conducting. This means that the switching losses are not included in the simulations, which is a simplification. In reality the switching losses can account for a significant portion of the total power losses [17]. Especially at high frequency and/or at light loads the switching losses can trump the conduction losses of the device [17]. The reason ideal switching devices are used is because the simulations were simplified at the beginning stage and due to the time constraints it was not possible to replace the components to more realistic ones at the later stage. Components and component values used for the simulations can be found in table 3.1. The values for the capacitance and inductance are calculated in chapter 2.4.1. It should be noted that the inductance value calculated is approximately five times lower than the actual value used in the simulations. The reason for this is that with the calculated value, the total harmonic distortion was deemed to be too high at the higher input voltages. The same inductance is also used for the Totem Pole PFC.

Table 3.1: Component values used for the simulation of Semi-Bridgeless Boost PFC

Switching Frequency	100 kHz
Sampling Frequency	3 MHz
Boost Inductors L1,L2	$L = 300 \mu\text{H}$, $R = 80.7\text{m}\Omega$
Output Capacitor	4.4 mF
Boost Diodes	<i>SCS320AJ</i>
Mosfets	<i>NTP082N65S3F</i>
Return Diodes	<i>DSEI120-06A</i>

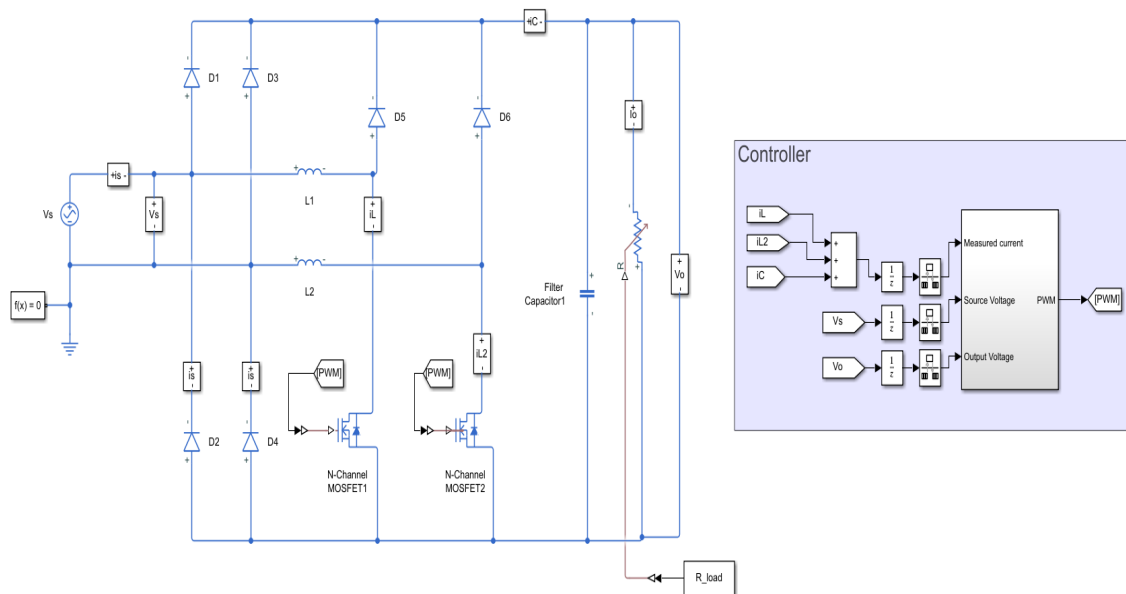


Figure 3.1: Model of the Semi-Bridgeless Boost PFC in Simulink

3.1.2 Bridgeless Interleaved Boost PFC

The modeling of the Bridgeless Interleaved Boost PFC was done in the same manner as the Semi-Bridgeless PFC, ideal switching MOSFETs and diodes were used. The component values used can be seen in table 3.2 and the Simulink model can be seen in figure 3.2.

Table 3.2: Component values used for the simulation of Bridgeless Interleaved PFC

Switching Frequency	100 kHz
Sampling Frequency	10 MHz
Boost Inductors L_1, L_2, L_3, L_4	$L = 130 \mu\text{H}$, $R = 52 \text{ m}\Omega$
Output Capacitor	4.4 mF
Boost Diodes	<i>SCS320AJ</i>
Mosfets	<i>NTP082N65S3F</i>
Return Diodes	<i>DSEI120-06A</i>

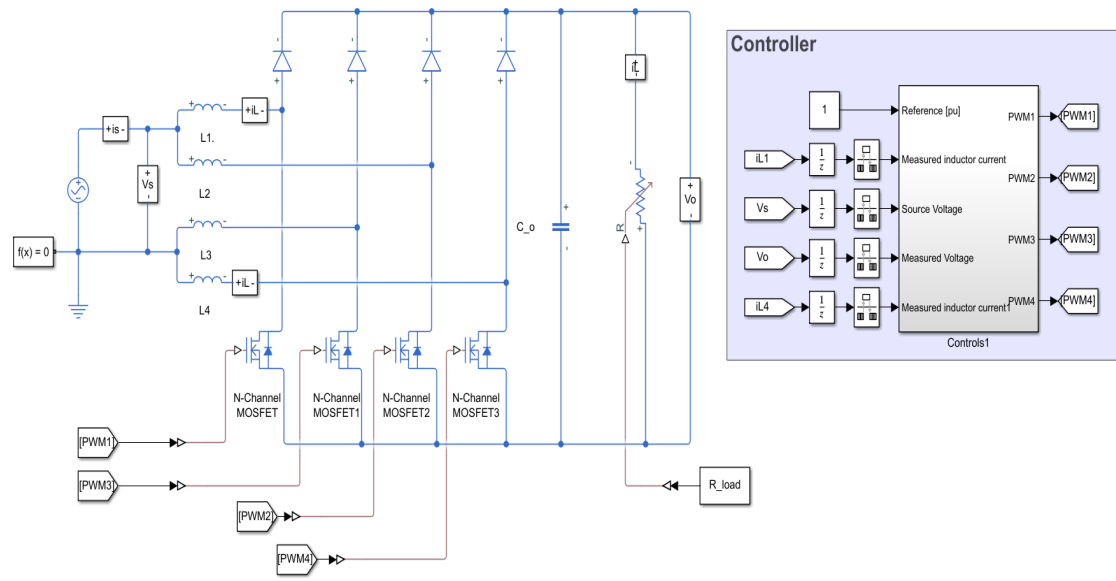


Figure 3.2: Model of the Bridgeless Interleaved Boost PFC in Simulink

3.1.3 Bridgeless Totem-Pole Boost PFC utilizing GaN Transistors

The Simulink circuit model of the Totem-pole PFC can be seen in figure 3.3. Due to the fact that there is no add-in model for GaN transistors in any of the available Simulink libraries a simplification is made where the MOSFETs with ideal switching are used instead in the same as in the other two topologies. The difference in this case is that the intrinsic body diode is removed from the device model. The component values used for modeling can be found in 3.3.

Table 3.3: Component values used for the simulation of Bridgeless Totem-Pole Boost PFC utilizing GaN transistors

Switching Frequency	100 kHz
Sampling Frequency	3 MHz
Boost Inductor L	$L = 300 \mu\text{H}$, $R = 80.7\text{m}\Omega$
Output Capacitor	4.4 mF
Transistors	GS66516T
Slow Diodes	DSEI120-06A

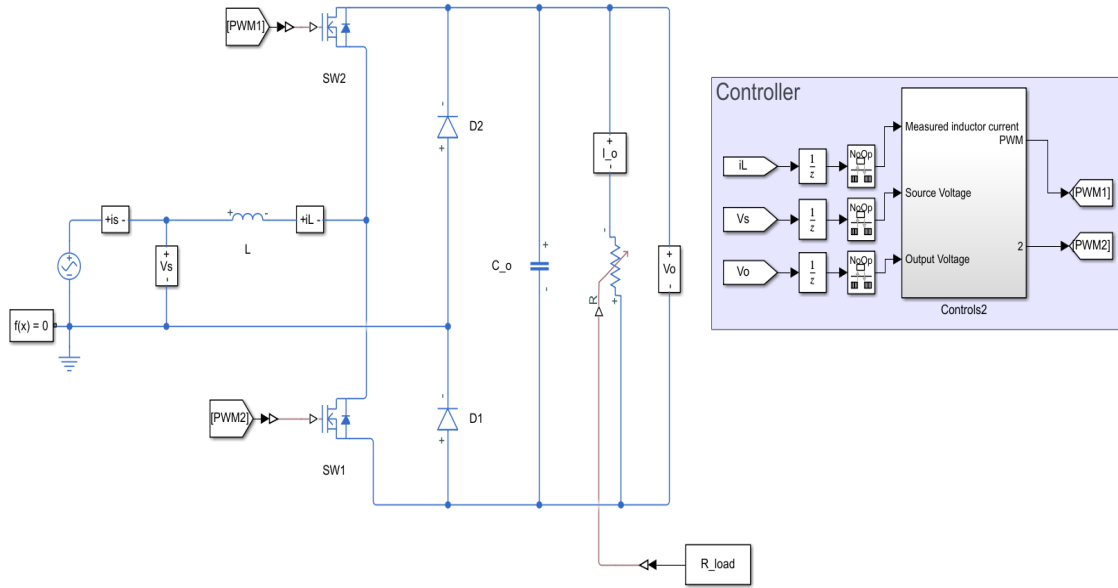


Figure 3.3: Model of the Totem-pole Boost PFC in Simulink

3.2 Implementation of the Control Systems

The control systems for the different topologies were built in the same manner, with a slower outer voltage controller and a fast inner current controller. The block diagram of the controller structure can be seen in figure 3.4. First, a voltage reference is given which is compared to the output voltage and the error is sent to the voltage PI controller. The output of the voltage controller is then multiplied with the the absolute value of the input voltage. The product of the input voltage and the output from the voltage controller will be the current reference which is sent to the inner current control loop. The current reference is compared with the inductor current and the error is sent to the current PI controller. The output of the current controller will be the duty cycle which will be sent to the modulator that will create the PWM which will drive the switches.

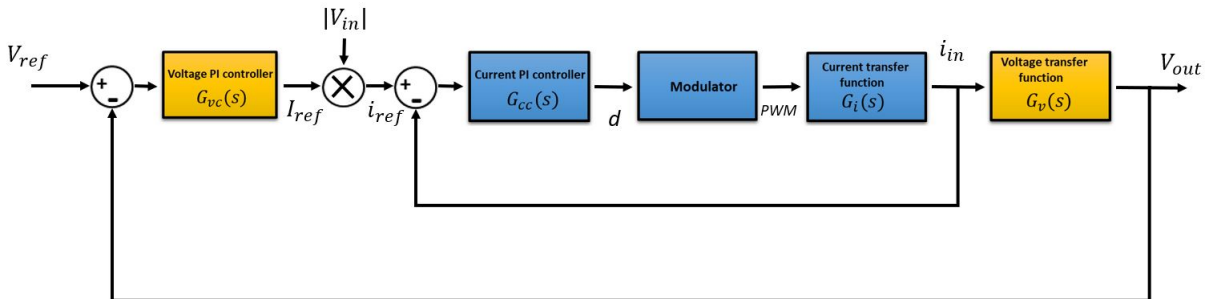


Figure 3.4: Block diagram of the controller structure

3.2.1 Tuning of the Controllers

To achieve the desired performance of the PFC it is important that the inner current controller is fast enough to track the input voltage and that outer voltage controller is able to bring up the output voltage to reference in reasonable amount of time without negatively affecting the current controller. To tune the controller it was first necessary to derive the current and voltage transfer functions for the chosen topologies, the derived transfer functions can be seen in sections 2.5.1 and 2.5.2. Thereafter the controller was tuned with help of the bode plots for the transfer functions using Sisotool in Matlab. The controller performance is defined by the cross-over frequency f_c and the phase margin θ_{pm} . The cross-over frequency is the frequency where the magnitude curve crosses the zero dB axis in the bode plot and the phase margin is defined as the difference between the phase of the response and the -180 degrees line of the bode plot at cross-over frequency. The cross-over frequency determines the speed and the phase margin will determine the stability of the response. The cross-over frequency will affect the total harmonic distortion of the PFC and should be as high as possible in order to give good THD performance [18]. There is a limitation to how high the cross-over frequency of the current open loop response can be, a rule of thumb is that it should be somewhere in between 10-20 % of the switching frequency [18]. In this work, the chosen cross-over frequency of the current open loop response for all three topologies is chosen to be close to 10 % of the switching frequency which is 10 kHz. The phase margin will affect the overshoot of the response. A rule of thumb is that the phase margin of the current controller should be between 45-60 degrees [18]. The current controllers for all three topologies are tuned so that the current open loop response has close to 60 degrees of phase margin. The current controller for all three topologies were tuned at the midpoint of the required AC input voltage range for the PFC topologies, which is 175 V RMS see table 1.1. This is so that the current controller can have a good behavior for the whole range of the required input voltages. Also the controllers were tuned at full load of 3kW in order to guarantee the best THD performance at full load operation.

The requirements for the voltage controller is to attenuate the output voltage ripple which occurs at twice the line frequency and to have close to 90 degrees of phase margin because the voltage overshoot at the output is not desired [18]. The cross-over frequency of the voltage controller should be low enough to attenuate the output voltage ripple and also low enough to not affect the reference tracking of the current controller. The cross-over frequency of the voltage controller should be set to 10-20 % of $2 \cdot f_{line}$ [18]. In this work the voltage controllers are tuned so that the voltage open loop response has a cross-over frequency of $f_c \leq 20$ Hz at 230V RMS input voltage and close to 90 degrees of phase margin. As for the current controller the voltage controller is tuned for full load operation, but unlike the current controller, the voltage controller is tuned for higher input voltage. In this way the voltage controller is not unacceptably slow at low input voltages. The bode plots used for current and voltage controller tuning for the Semi-Bridgeless Boost PFC can be seen in figures 3.5 and 3.6 respectively. The tuning is done in the same manner for the other two topologies. In the subsections below a more detailed description of the

Simulink controller implementation for the different topologies will be given.

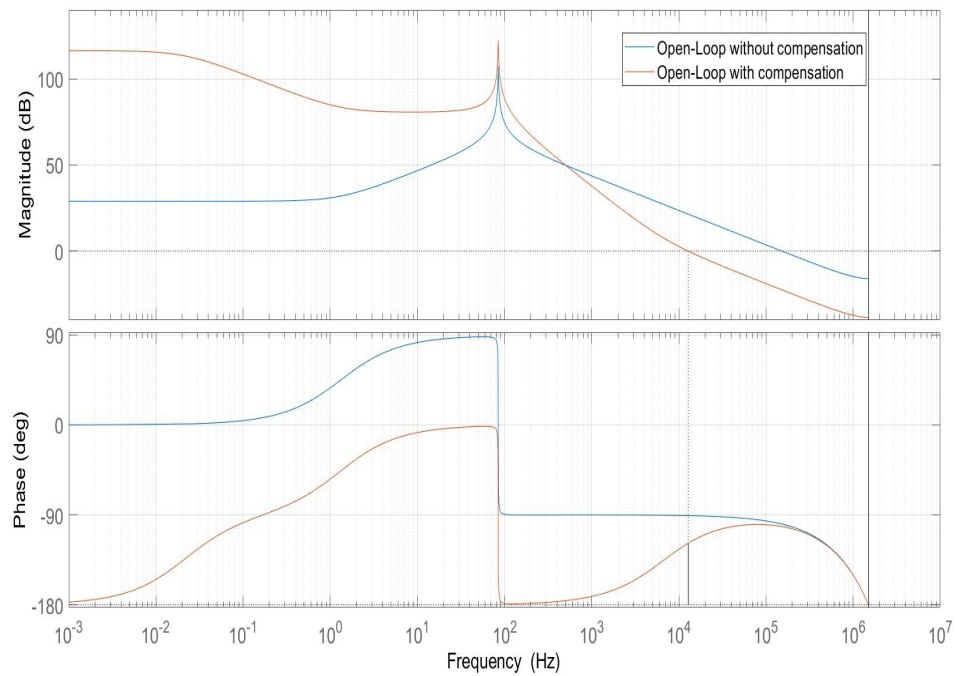


Figure 3.5: Bode plot for the current open loop response with and without the current controller for the Semi-Bridgeless PFC

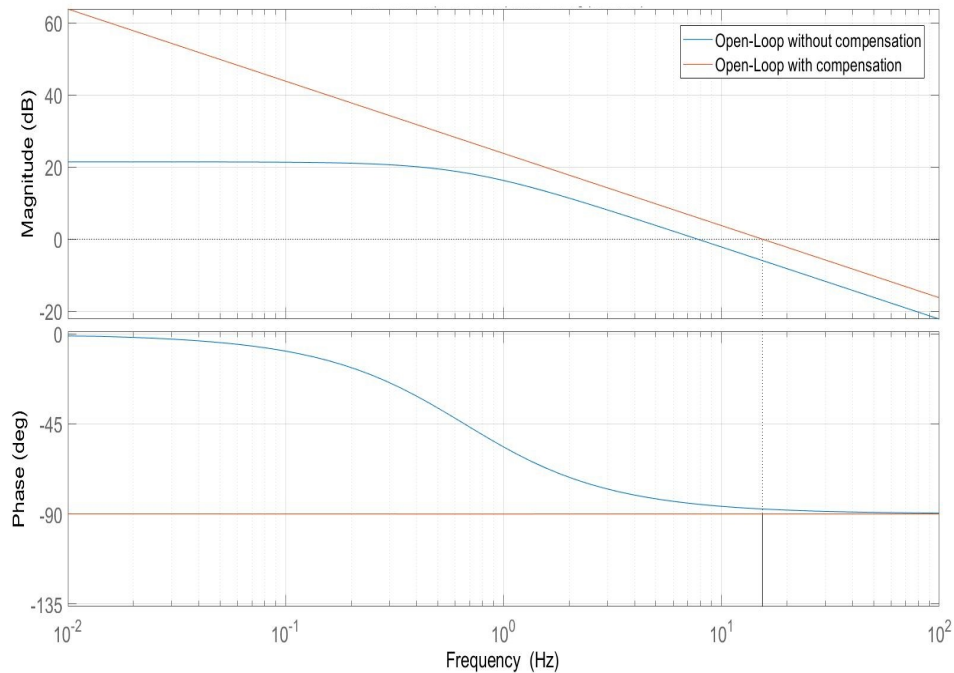


Figure 3.6: Bode plot for the voltage open loop response with and without the voltage controller the Semi-Bridgeless PFC

3.2.2 Simulink Implementation and System Testing

Controller Simulink models for each topology as well as the testing of closed loop systems are presented in this section.

3.2.2.1 Semi-Bridgeless Boost PFC

The closed loop controller implemented in Simulink follows the structure from figure 3.4. The closed loop controller implemented in Simulink can be seen in figure 3.7. The input voltage, output voltage and the sum of the current flowing through the switches and the current flowing to the load and the capacitor are first measured and normalized. The output voltage is compared to the reference and the error is then sent to the voltage controller. The input voltage is rectified and multiplied with the output of the voltage controller. The product is then compared to the measured current and error is sent to the current control loop which generates the PWM signal necessary for driving the switches.

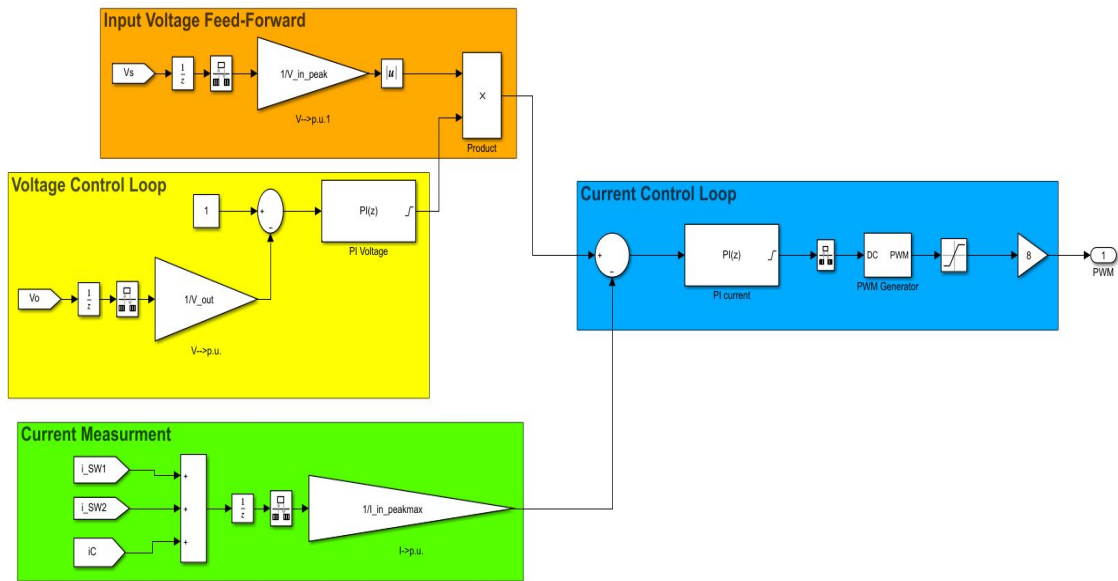


Figure 3.7: Simulink model of the closed loop controller for the Semi-Bridgeless Boost PFC

Once the controller was implemented, the testing of the whole system was done for different input voltages. The input current, input voltage and load voltage waveforms for input voltage of 230V RMS and load of 3kW can be seen in figures 3.8 and 3.9 respectively. In figure 3.8 the input voltage amplitude is scaled in order to easier compare the current and voltage waveforms. From this figure, it can be seen that the input current is tracking the input voltage, which indicates that the current controller is working as desired. During the simulations it was observed that the input current has a very high value during the first half cycle of operation, this is due to the inrush current. From figure 3.9 it can be seen that the load voltage follows reference which is 405V. It can be seen that the voltage rises quickly to just below 400 V and drops just before it once again rises and continues to reference. The fast initial rise in voltage is due to the large in-rush current. Once the current passes the inrush stage, the voltage will drop for a short moment. This is because the voltage controller is quite slow and it will take some time for it to regulate the voltage back to the setpoint. It can be seen that the steady state for the load voltage is reached just before approximately 1.5 seconds. In reality the voltage controller should be faster but for this work, this time was deemed to be acceptable. The voltage controller can be tuned for a faster response but there is a limit for how fast it can be before it starts to affect the voltage tracking capability of the current controller.

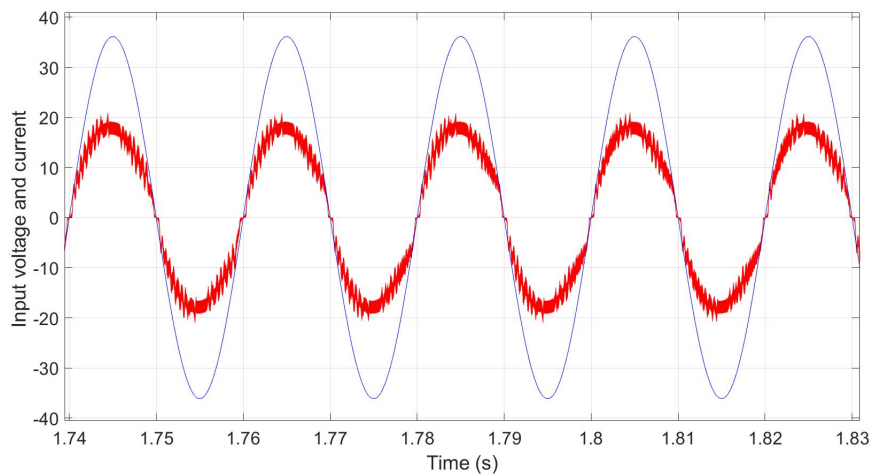


Figure 3.8: Steady state waveform of the input current in red and source voltage in blue for Semi-Bridgeless Boost PFC

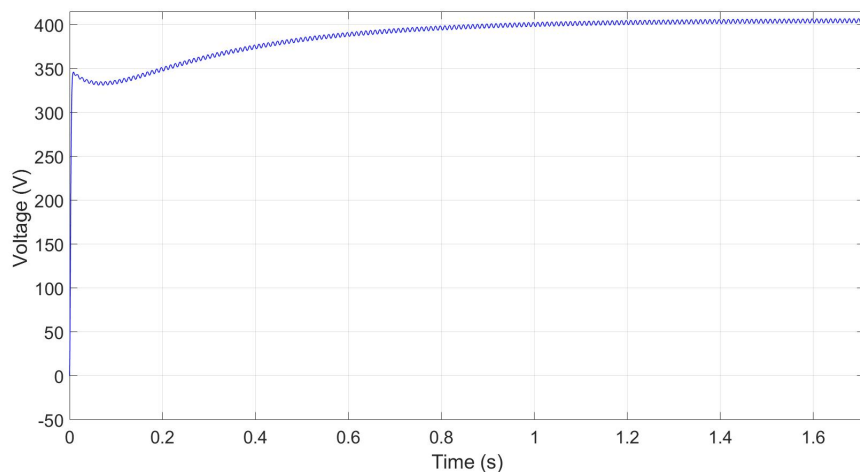


Figure 3.9: Load voltage waveform for Semi-Bridgeless Boost PFC

3.2.2.2 Bridgeless Interleaved Boost PFC

The control system for the Bridgeless Interleaved Boost PFC is structured in the same way as for the Semi-Bridgeless PFC. The difference in this case is that two current PI controller are used instead of one, with each of them getting half of the respective current references. For this topology the switches are driven in pairs and the PWM signals for these pairs are phase shifted with 180 degrees. The complete control circuit can be seen in the figure 3.10.

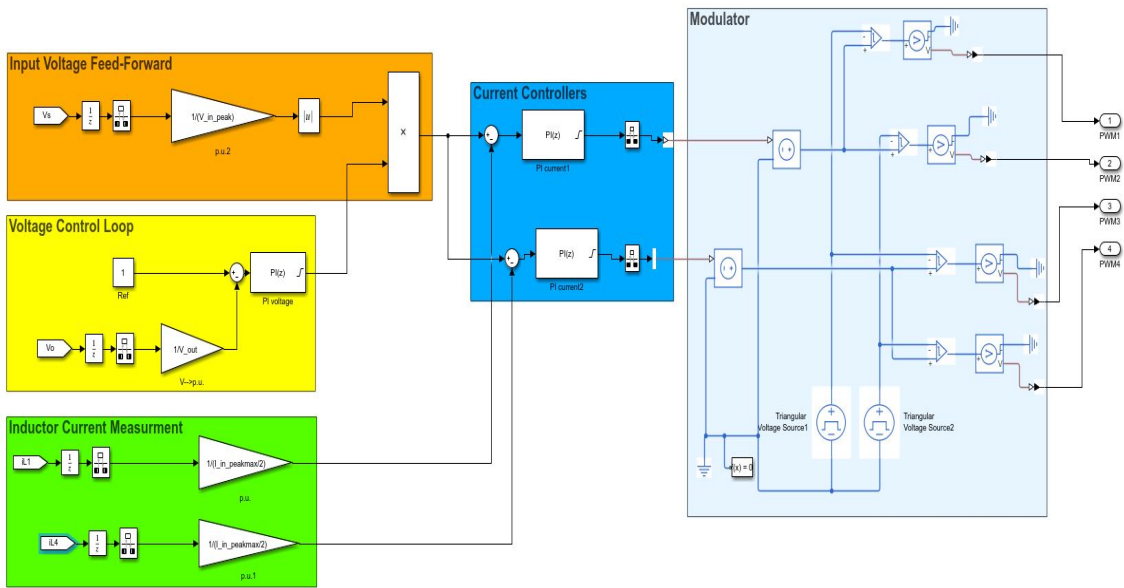


Figure 3.10: Simulink model of the closed loop controller for the Bridgeless Interleaved Boost PFC

The system response for the input voltage of 230V RMS and load of 3kW is presented in in figures 3.11 and 3.12. The load voltage reaches steady state after approximately 1 second.

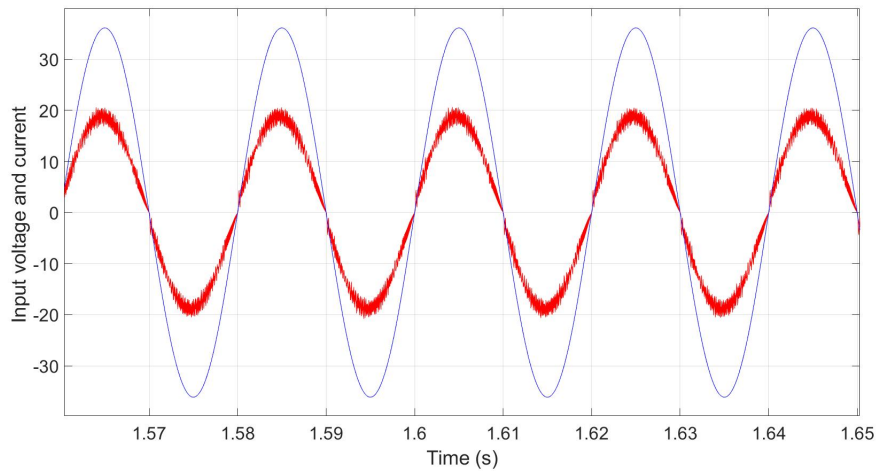


Figure 3.11: Steady state waveform of the input current in red and source voltage in blue for Bridgeless Interleaved Boost PFC

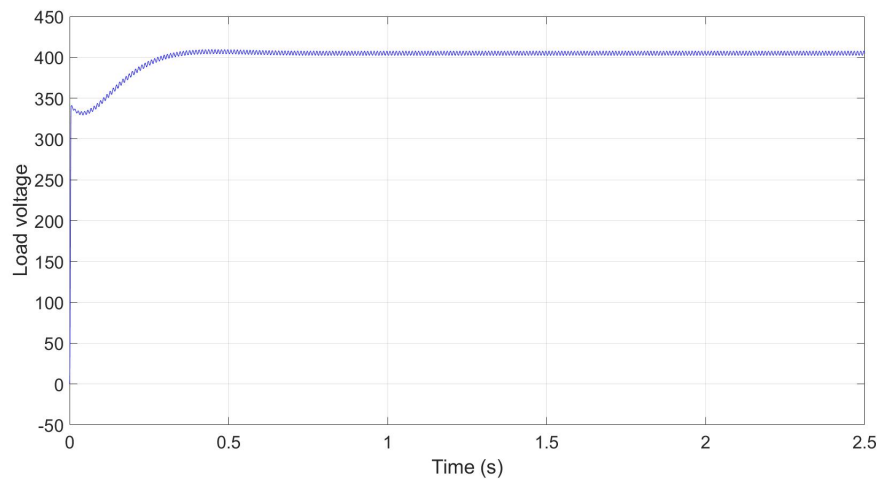


Figure 3.12: Load voltage waveform for Bridgeless Interleaved Boost PFC

3.2.2.3 Bridgeless Totem-Pole Boost PFC Utilizing GaN transistors

The control system for the Bridgeless Totem-Pole PFC is structured in the same way as for the other two topologies. The major differences of this controller compared to the other two topologies is that the PWM signals are inverted compared to each other and a polarity detection is introduced. The controller will sense the polarity of the input voltage and adjust which of the two PWM signals is sent to which switch depending on if the input voltage is in the positive or negative half cycle.

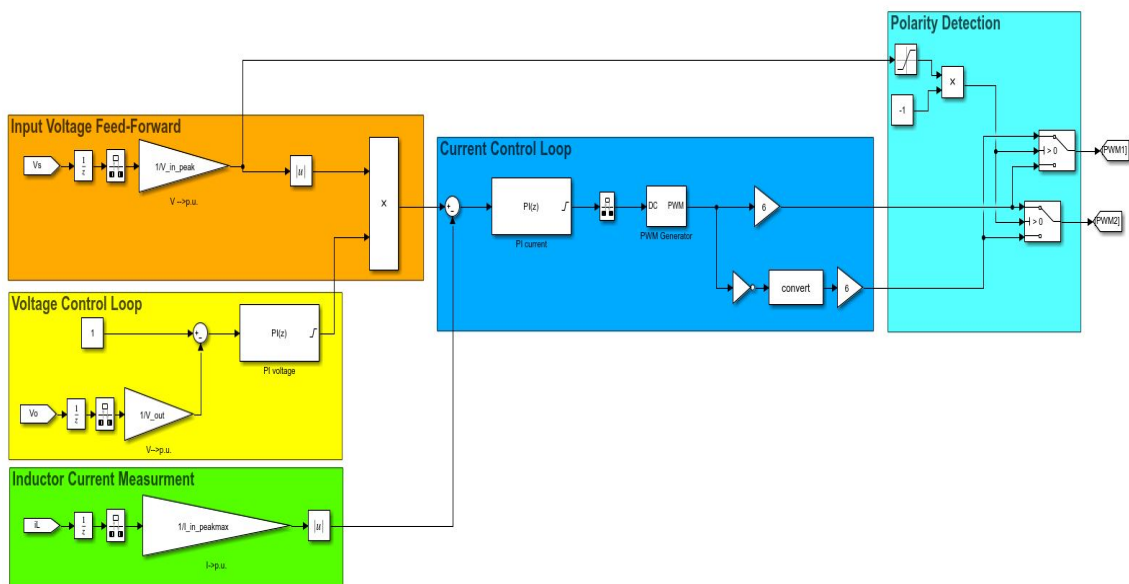


Figure 3.13: Simulink model of the closed loop controller for the Totem-pole Boost PFC utilizing GaN transistors

As for the other two topologies, the system response for the input voltage of 230V RMS and load of 3kW is presented in in figures 3.14 and 3.15. It can be seen that

the current tracks the input voltage as desired and that the steady state for the load voltage is reached just before approximately 1 second.

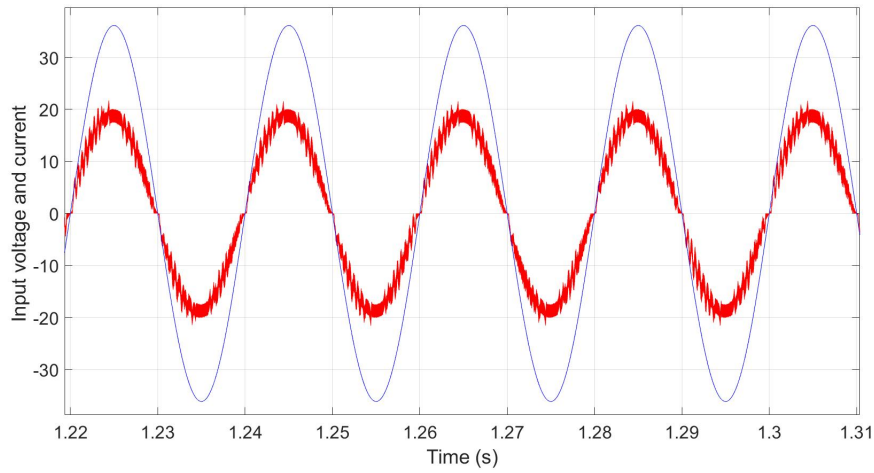


Figure 3.14: Steady state waveform of the input current in red and source voltage in blue for Totem-pole Boost PFC utilizing GaN transistors

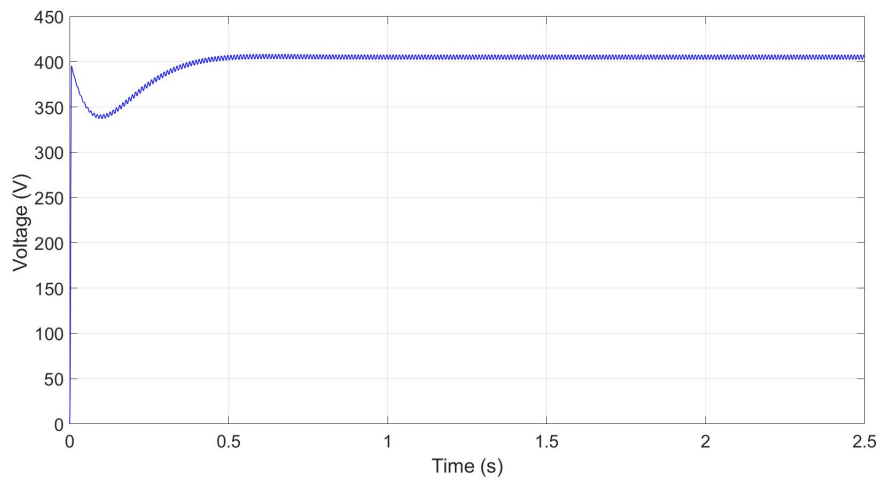


Figure 3.15: Load voltage waveform for Totem-pole Boost PFC utilizing GaN transistors

4

Results

In this section the simulation results as well as some of the results from the literature study will be presented.

4.1 Efficiency

4.1.1 AC Input Voltages

Efficiency plots for six different input voltages can be seen in figures 4.1-4.3. It can be seen that the Bridgeless Interleaved Boost PFC topology is the most efficient of the three topologies for the majority of input voltages and load powers. An exception to this is seen at the low load powers and high input voltages. The Totem-Pole PFC is just below the Bridgeless Interleaved PFC at most of the input and load ranges but has higher efficiency at low load operation at the input voltage of 240 and 264V RMS. It can be seen that the Semi Bridgeless PFC is the least efficient out of the three. This is most likely a result of the conduction losses being the biggest contributor to efficiency drop in the simulations. The Bridgeless Interleaved PFC is the most efficient since the current going through each of the active components is effectively halved compared to the input current. The Totem-Pole PFC is not quite as efficient as the Bridgeless Interleaved but performs better than the Semi-Bridgeless PFC. This is because the transistors in the circuit have lower resistance and there are also less components in the current path. The peak efficiency for Bridgeless Interleaved PFC, Semi-Bridgeless PFC and Totem-pole PFC was estimated to be 97.86%, 96.93% and 97.55% respectively, with a input voltage of 264V RMS and a output of 3000W. Similar, but just a bit lower efficiencies can be observed at a voltage of 230V RMS.

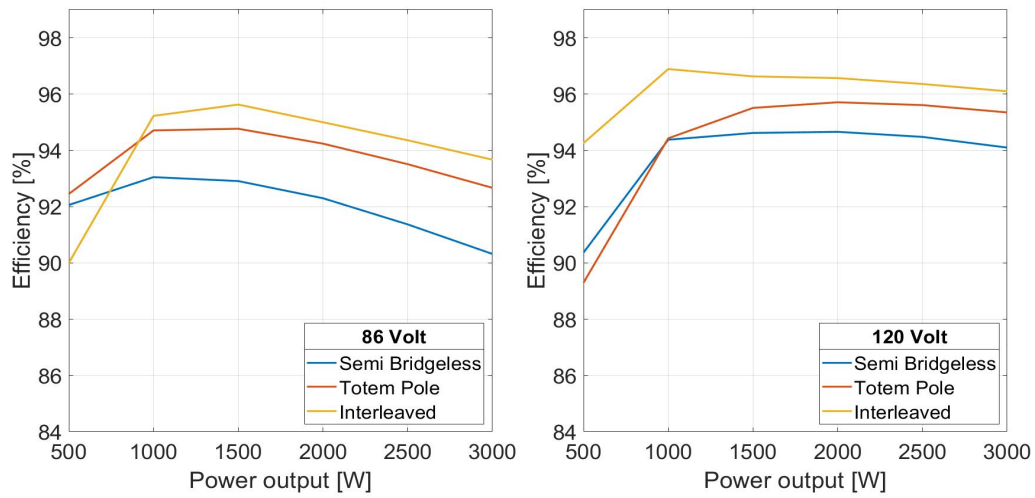


Figure 4.1: Efficiency plots for 86V, 50Hz input voltage and 120V, 60Hz input voltage for the chosen topologies

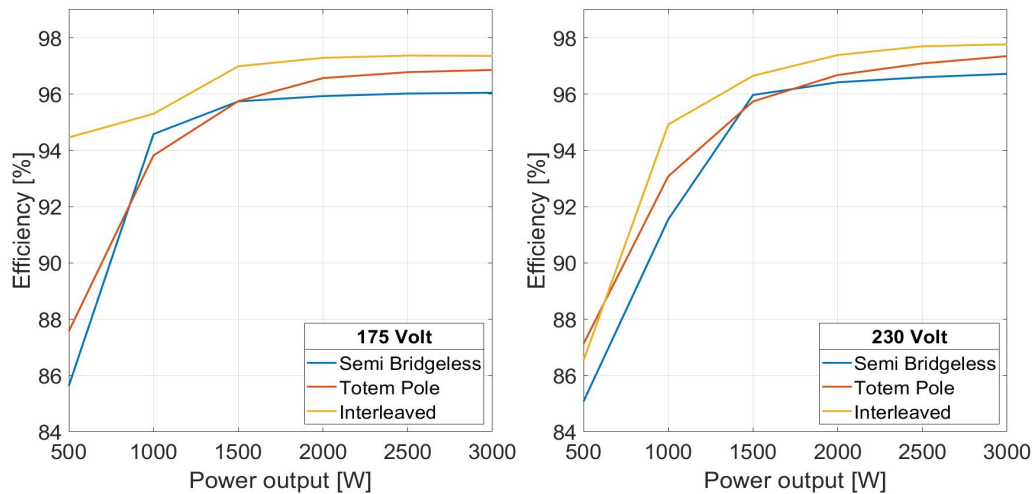


Figure 4.2: Efficiency plots for 175V and 230V, 50Hz input voltages for the chosen topologies

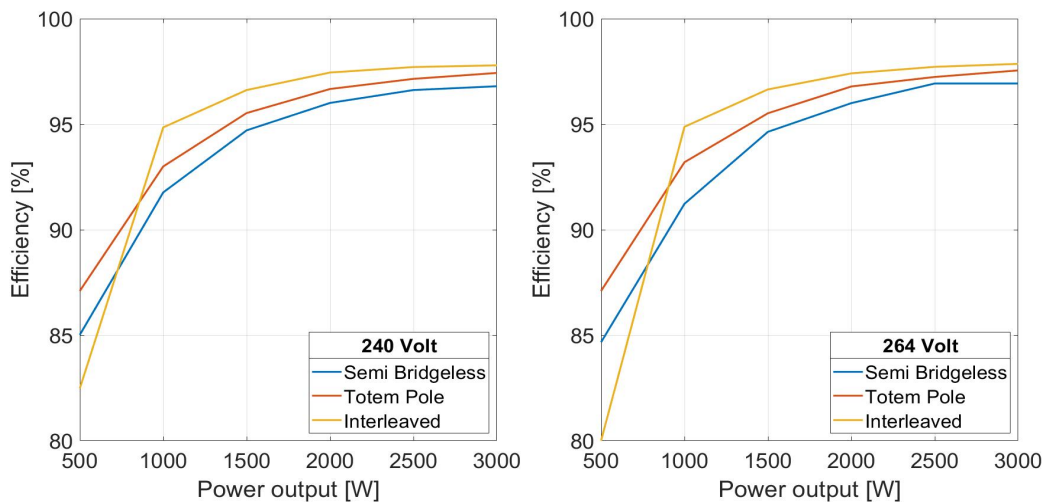


Figure 4.3: Efficiency plots for 240V and 264V, 50Hz input voltages for the chosen topologies

4.1.2 DC Input Voltages

Efficiency results for 350V and 400V DC input voltages are presented in the figure 4.4. From the figure it can be seen that the Totem-Pole PFC topology is the most efficient of the three, for a load power lower than 2.5 kW for 350V input and load power lower than 2 kW for 400V input. The Bridgeless Interleaved PFC is the most efficient at full load of 3 kW, while the Semi-Bridgeless PFC has the lowest efficiency out of the three. The peak efficiency of 99.27 % for Totem-Pole PFC is observed at the load power of 1.5 kW and a input voltage of 400V. The peak efficiency for Bridgeless Interleaved and Semi Bridgeless PFC were 99.25 % at load of 3 kW and 98.75 % at load of 1.5 kW, respectively.

It can be seen that unlike for the AC inputs, the efficiency curves of all three topologies are more linear even for lower power. In the AC case, the low efficiency for low loads can be attributed to the high amount of harmonic distortions in the current. The current controller is tuned for 3 kW operation and behaves poorly at low loads. This is not the case for the DC input voltages. The current distortions for DC voltages were not significant. This can also be the reason why the Totem-Pole PFC has a higher efficiency than Bridgeless Interleaved PFC for lower load power. For AC input voltages, the current controller might be slightly better tuned for the Bridgeless Interleaved when compared to the Totem-Pole and due to this the Bridgeless Interleaved PFC experienced lower THD which lead to a greater efficiency. Another possible reason is that due to the inherent current ripple cancellation of the Bridgeless Interleaved PFC, the THD was lower than the other topologies which again lead to a greater efficiency for this topology.

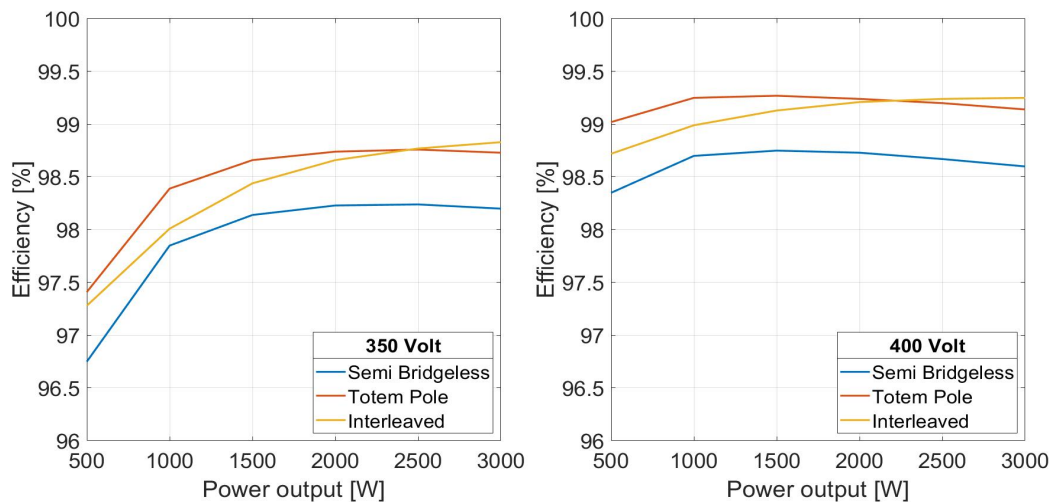


Figure 4.4: Efficiency plots for 350V and 400 V DC input voltages for the chosen topologies

4.2 Harmonic Distortion and Power Factor

The total harmonics distortion for six input voltages and different loads can be seen in figures 4.5 - 4.7. The same trend as in the efficiency plots can be observed, the Bridgeless Interleaved PFC has the best performance for most of the input voltages and loads. The reason for this is probably a result of its inherent input current ripple cancellation. It can also be seen that the Semi-Bridgeless PFC has the highest THD out of the three topologies. One reason for why a difference in THD values can be seen between the Semi-Bridgeless PFC and the Totem-Pole PFC might be due to the small signal modeling of the topologies which is used to tune the current controller. The small signal model for both topologies is derived in the same way, but in the case of the Semi-Bridgeless PFC a simplification is made where it is assumed that all of the return current will flow through the return diodes. In reality this is not the case, and a significant portion of the return current will flow through the body diode of the non-switching MOSFET.

The power factor for the three topologies was found to be better for higher power output regardless of input voltage. It was also found that as the input voltage increased, the power factor for the lowest power output got progressively worse across the board, resulting in a power factor as low as 0.90 for the three topologies. The power factor for all power levels above 500 W was above 0.98. The most likely reason for this being the case is because the controllers for all topologies were tuned for higher power levels. The low power factor at the lowest output power is as expected since the total harmonic distortion is at its highest during that power level.

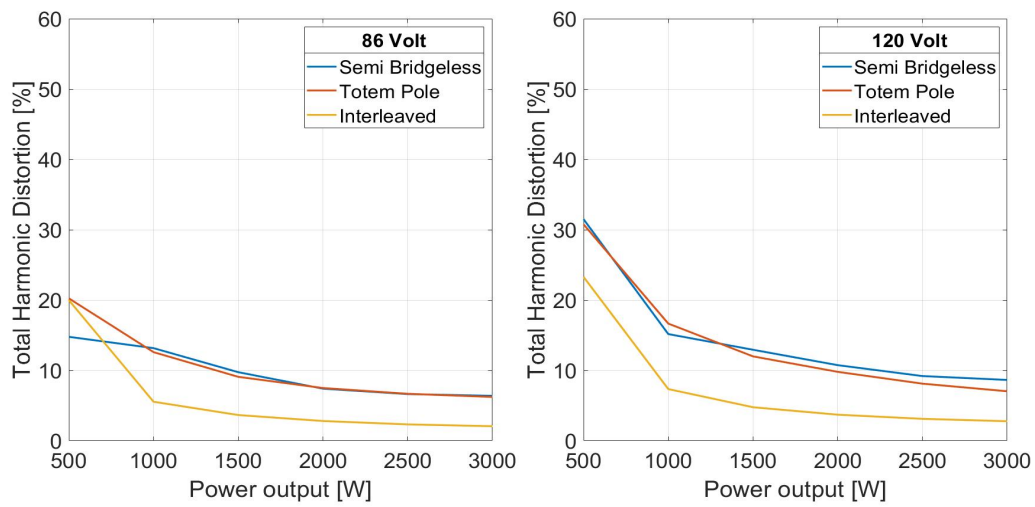


Figure 4.5: Total harmonic distortion plots for 86V, 50Hz input voltage and and 120V, 60Hz input voltage for the chosen topologies

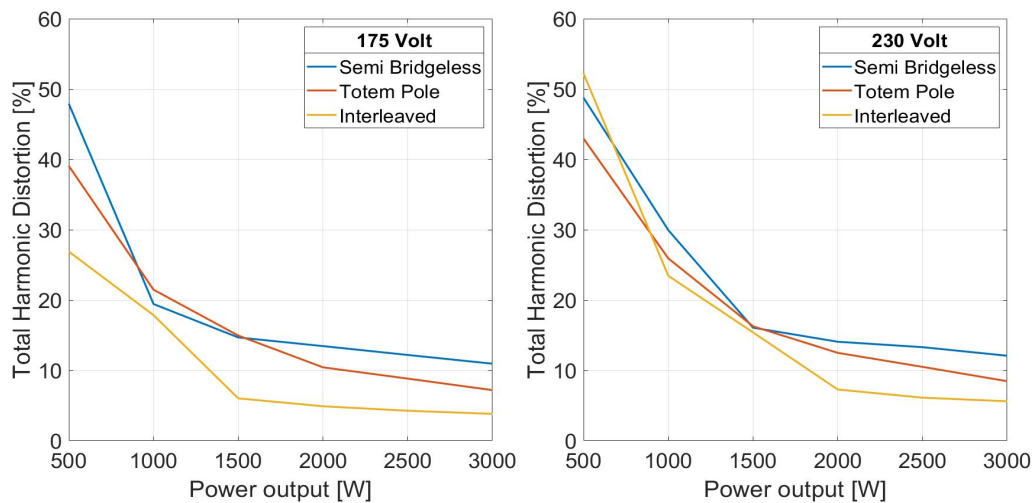


Figure 4.6: Total harmonic distortion plots for 175V and 230V, 50Hz input voltages for the chosen topologies

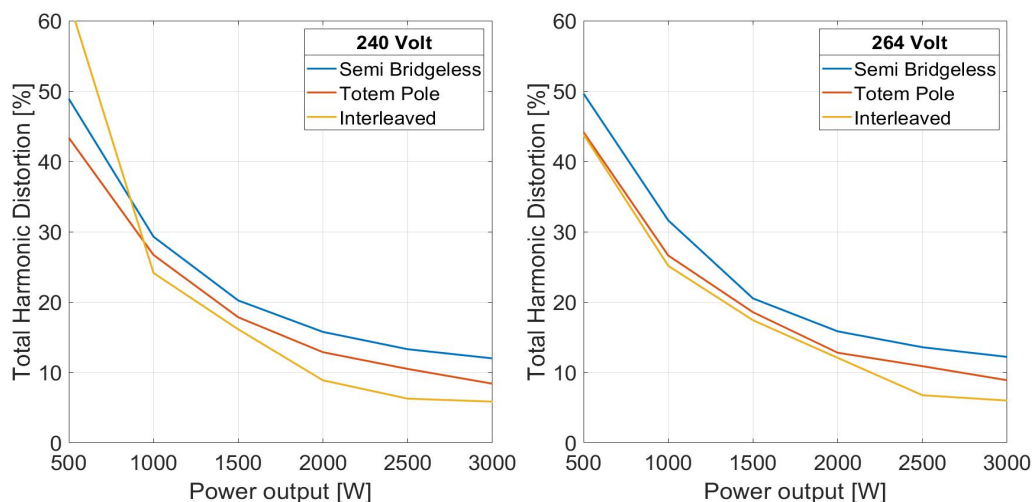


Figure 4.7: Total harmonic distortion plots for 240V and 264V, 50Hz input voltages for the chosen topologies

4.3 Input Current Ripple

The input current ripple for the three topologies was found to be constant for a specific voltage input regardless of power output. For all voltage levels and all topologies the current ripple was below 5A with the highest being 3.3A. The Totem-Pole PFC and the Semi-Bridgeless PFC had very similar input current ripples whereas the Bridgeless Interleaved PFC topology was halved in comparison. This is due to the inherent current ripple cancellation mentioned before.

4.4 Inrush Current

4.4.1 AC Input Voltages

From the simulations it was observed that all topologies experience significant inrush current during the first half cycle of the input voltage. The highest inrush current is experienced at the highest input voltage, since that is when the voltage difference between the input voltage and the output capacitor is the greatest. The Totem-Pole PFC having the lowest conductive resistance due to lowest amount of components and its switches, it experienced the highest inrush current of the three topologies. This occurs at 264V and the amplitude of the inrush was 592.7A for a very short period of time. The highest experienced inrush current by the Bridgeless Interleaved topology is 498.8A. In contrast to the Totem-Pole, this current is divided between two legs of the circuit lowering the current flowing through sensitive components. The Semi-Bridgeless PFC experiences the highest inrush at the same point as the other two topologies and the amplitude is roughly the same as for the Bridgeless Interleaved. One way to reduce the current flowing through sensitive semiconductors is with additional circuitry. Two so called peak charging diodes can be connected between line and neutral of the voltage source and the output capacitor. As seen

in the semi bridgeless PFC topology. With these diodes in place the inrush current can circumvent the sensitive semiconductors and flow straight to the capacitance. The inrush diodes, D_1 and D_3 can be seen in figure 2.9.

4.4.2 DC Input Voltages

The inrush current for the DC input voltages was higher than for the AC input. The peak inrush currents observed were 1532A, 1400A, 871A at 400V input for the Bridgeless Interleaved, the Semi-Bridgeless PFC and Totem-Pole PFC respectively. It can be seen that the inrush current is significantly larger for the DC input voltages. This is partly due to the fact the DC input voltages are higher than the peak voltage of the AC input and partially that in the case with DC simulations, a large voltage is directly available from the source. In the case of the simulations with AC input, the source voltage will be sinusoidal which means that it will start of at zero and ramp up to peak value. The peak value is reached after one quarter of the cycle which leads to a more of a soft start when compared to instantly applying the DC input voltage. Due to the high inrush current, additional circuitry is needed to lower the inrush current to more reasonable values.

4.5 Component Count

In the table below the component count as well as the component type used for each of the chosen topologies is presented. One should note that the peak charging diodes needed for the in-rush protection are excluded from this table. From the table can be seen that the topology with the lowest component count is the Totem-Pole (BTP) PFC, followed by the Semi-Bridgeless (SBL) PFC and finally by the Bridgeless Interleaved PFC (BLIL). Of course, the total amount of components is not the only thing of interest but also the type of components used. Due to the use of the GaN transistors and the higher cost of them when compared to Si Mosfets, the total cost of the Totem-Pole PFC is generally higher when compared to the Semi-Bridgeless PFC. On the other hand the amount of fast diodes and MOSFETs used in the Bridgeless Interleaved PFC topology will lead to a cost which is generally closer to the cost of the Totem-Pole PFC.

Table 4.1: Table of number of specific components for specific topology

	BLIL	SBL	BTP
Fast diodes	4	2	0
Slow diodes	0	2	2
Mosfets	4	2	0
Inductors	4	2	1
GaN Transistors	0	0	2

5

Conclusion

The aim of this thesis was to investigate and compare bridgeless PFC topologies that are suitable for power levels of 3kW. It was found that the three most suitable topologies for this power level are Semi-Bridgeless Boost PFC, Bridgeless Interleaved Boost PFC and Totem-Pole Boost PFC utilizing Gallium Nitride transistors. From the simulations that were carried out it was observed that the Bridgeless Interleaved PFC had the highest efficiency for most of the input voltages and output loads. Totem-Pole PFC was closely behind the Bridgeless Interleaved PFC and finally the Semi-Bridgeless PFC had the lowest efficiency out of the three. The same trend can be seen in the total harmonic distortion, power factor and input current ripple where the Bridgeless Interleaved PFC performed better than the other two topologies. All three topologies experience significant in-rush current at the start of the operation. In the case of the Bridgeless Interleaved PFC unlike the other two topologies, this current will be divided between two of the switching legs of the converter. This means that the components experience half of the in-rush current and as a result of this, additional circuitry for in-rush handling might not be necessary. This is not the case for the other two topologies. With this said, the Bridgeless Interleaved is the topology which contains the highest amount of components out of the three, which can be correlated to a higher price for the converter compared to the other two topologies.

6

Discussion and Future Work

As previously mentioned in chapter 3, the simulations of all three topologies were executed using ideal switching devices meaning that the switching losses of the transistors and reverse recovery losses of the diodes are not included in the simulations. In reality the switching losses and reverse recovery losses can be a significant portion of the total power losses. With that said, the efficiency results obtained from the simulations match quite closely to the experimental results seen in the literature study when it comes to full load operation and the loads near the full load operation [5], [8], [19], [20], [21], [12], [22]. The reason for this is probably that the converter design was more extensively optimized, which was not possible to do in this thesis due to the time constraints. One thing to note when it comes to the Totem-Pole PFC is, as mentioned in chapter 2.3.3 that the slow diodes of the the converter can be replaced with slow switching MOSFETs to further increase the efficiency of PFC. With this implementation it is expected that the Totem-Pole PFC could achieve highest efficiency out of the three topologies - up to 99 % [12], [22], [23].

This project has investigated the performance of three bridgeless PFC topologies with help of a literature study as well as computer simulations. The simulations done in this project were simplified, where the ideal switching devices instead of more realistic components were used. These kind of simulations in combination with the literature study can be used to determine general performance of the PFC topologies but does not give 100 % accurate results. To further improve the accuracy of the results the simulations should include more realistic switching components, which is something that can be implemented in future work. A detailed loss distribution could also be added to get a better picture of how losses as well as the heat is distributed throughout the converter. Simulations of the topologies give a good idea of their performance but of course to fully analyse the performance of the topologies, prototypes should be designed and manufactured to measure experimental performance.

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