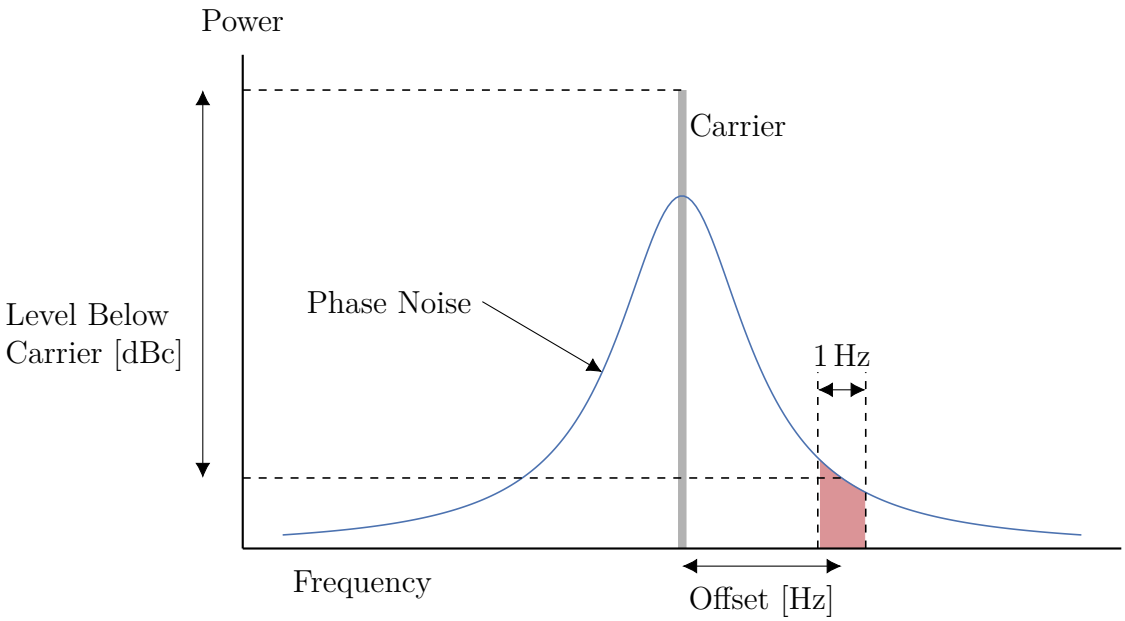
CHALMERS
UNIVERSITY OF TECHNOLOGY



Phase Noise Tracking

Circuit design and construction

Master's thesis in Electrical Engineering

Johan Olson

Hugo Thunberg

NEW CONCEPTS AND SYSTEM STUDIES
SAAB SURVEILLENCE
Gothenburg, Sweden 2022
www.saab.com

DEPARTMENT OF ELECTRICAL ENGINEERING
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2022
www.chalmers.se

Master's thesis 2022

Phase Noise Tracking

Circuit design and construction

Johan Olson

Hugo Thunberg

CHALMERS
UNIVERSITY OF TECHNOLOGY

Surveillance
New Concepts and System Studies
Saab
Gothenburg, Sweden 2022

Department of Electrical Engineering
Division of Communication Antennas and Optical Systems
Chalmers University of Technology
Gothenburg, Sweden 2022

Phase Noise Tracking
Circuit Design and Construction
JOHAN OLSON, HUGO THUNBERG

Supervisors: Martin Ankel, Saab & Chalmers, Tomas Bryllert, Saab & Chalmers, Rune Olsson, Saab
Examiner: Thomas Eriksson, Electrical Engineering

Master's Thesis 2022
Department of Electrical Engineering
Division of Communication Antennas and Optical Systems
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover: Illustration of phase noise on a carrier signal measured in a 1 Hz bandwidth

Typeset in LaTeX
Printed by Chalmers Reproservice
Gothenburg, Sweden 2022

Phase Noise Tracking
Circuit Design and Construction
JOHAN OLSON, HUGO THUNBERG
Department of Electrical Engineering
Chalmers University of Technology

Abstract

In order to detect small targets in an environment with interference using radar systems, an oscillator exhibiting low phase noise is required. An oscillator with poor phase noise can disguise the object of interest due to clutter. Therefore a method has been proposed to reduce phase noise, but in order for this method to be implemented, phase noise must first be measured. The goal of this thesis has been to design and construct a system capable of estimating the instantaneous phase noise of an oscillator. In addition, the system has been analyzed to determine its functionality, where its potential to measure low phase noise was vital. This thesis was limited to the delay line discriminator method, since all other methods rely on their own local oscillators. However, a variant using a RF-interferometer was investigated as well. Three different designs were constructed and all were analyzed using software before construction. The first served as a proof of concept while the second was intended as the final product. Although, a variant of it was proposed and constituted the third design, adding a RF-interferometer. All designs went through similar experiments were the phase noise from an oscillator had modelled phase noise superimposed on its own. The system output was measured using an analog-to-digital converter. The data collected shows that all the systems could measure instantaneous phase noise correctly. However, while functional, the conventional delay line discriminator suffer limitations in measuring low phase noise, in particular low frequency offset phase noise, at its lowest $-47\,\mathrm{dBc/Hz}$ at $100\,\mathrm{Hz}$. Two reason for this limitation was identified. First, the delay line discriminator itself filters low frequency offset phase noise, while the second limitation was caused by noise generated from a component in the system, namely the frequency mixer. This limitation was mitigated by using the RF-interferometer variant, which has better sensitivity, in particular at these low frequencies ($-71\,\mathrm{dBc/Hz}$ at $100\,\mathrm{Hz}$) and for short time delays. Still, it can be concluded that if the phase noise is sufficiently large, all designs investigated performs well. Ultimately, it is up to future studies to conclude whether the delay line discriminator is sensitive and robust enough to use in radar systems, and if the proposed method yields a worthwhile reduction of phase noise.

Keywords: Phase Noise, Delay Line Discriminator, Radar, Interferometer, Circuit Design

Acknowledgements

We would like to thank Saab for providing this interesting project, involving not just studies, but hands on experiments as well. Along the way our examiner Thomas Eriksson has hosted many interesting discussions and given insight on a topic that until recently was unknown to us. We would also like to thank our supervisors and other employees at Saab that has helped us with the experiments. Special thanks are in order to our supervisor Martin Ankel that encouraged us to do this project and has helped at every step of the way. This thesis would not be possible without you.

Johan Olson, Hugo Thunberg, Gothenburg, June 2022

List of Acronyms

ADC	Analog-to-Digital Converter.
AM	Amplitude Modulation.
BW	Bandwidth.
CL	Conversion Loss.
DAC	Digital-to-Analog Converter.
DLD	Delay Line Discriminator.
DR	Dynamic Range.
DSB	Double Sideband.
FM	Frequency Modulation.
FPGA	Field Programmable Gate-Array.
IF	Intermediate Frequency.
IL	Insertion Loss.
IMD	Intermodulation Distortion.
LNA	Low Noise Amplifier.
LO	Local Oscillator.
LSB	Least Significant Bit.
NF	Noise Figure.
PCB	Printed Circuit Board.
PLL	Phase Locked Loop.
PM	Phase Modulation.
PSD	Power Spectral Density.
RF	Radio Frequency.
SAW	Surface-Acoustic-Wave.
SNR	Signal-to-Noise Ratio.
SSB	Single Sideband.
UUT	Unit Under Test.
VC	Voltage Controlled.

Nomenclature

Below is the nomenclature of parameters, and variables that have been used throughout this thesis.

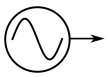
Constants

k_B	Boltzmann's Constant
c	Speed of Light

Parameters and Variables

f	Frequency
f_c	Carrier Frequency
t	Time
σ	Standard Deviation
τ_d	Time Delay
$\phi(t)$	Instantaneous Phase Fluctuations
$\mathcal{S}(t)$	A$(\phi(t) - \phi(t - \tau_d))$
$\mathcal{M}(t)$	Measured System Noise at Output
$\epsilon(t)$	Instantaneous Amplitude Fluctuations
φ	Phase Shift
$\mathcal{H}(f, \tau_d)$	Non-linear Filter Response
V	Voltage
T	Temperature
B	Bandwidth
P	Power Spectral Density
W_t	Brownian Motion Process
N	Mean Square Noise Voltage Density

Components



Oscillator/Signal Generator

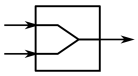
Analog to Digital Converter

Amplifier

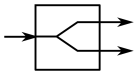
Delay Line

Low-Pass Filter

Frequency Mixer



Power Combiner



Power Splitter

Phase Shifter

Contents

List of Figures

List of Tables

1
Introduction

In a radar system one seeks to determine the position and velocity of targets in the surrounding environment[1]. The radar performance is adversely affected by phase noise which is an undesirable but unavoidable issue [1]. Phase noise reduces the ability to detect certain targets, especially in an environment where there is clutter present [2]. Clutter is unwanted radar echoes, e.g., rain, the sea, animals, etc. An oscillator is used in the radar transmitter and receiver for up- and down-conversion [3]. This oscillator requires good phase noise characteristics, otherwise the clutter performance will deteriorate, compromising detection of certain targets. Phase noise is instabilities in the phase of a signal, causing the power spectrum of the signal to appear in a band around the carrier frequency. If the oscillator in the radar has less phase noise, the detection will improve [1]. Higher quality oscillators is one way to improve detection, however there could be other ways. By measuring the instantaneous phase noise $\phi(t)$ from the oscillator one could potentially compensate for it in signal processing. Since $\phi(t)$ is not directly measurable in Radio Frequency (RF) applications, one resort to measuring a function $\mathcal{S}(t) = A\left(\phi(t) - \phi(t - \tau_d)\right)$, where τ_d is a time delay. Subsequently $\phi(t)$ can be estimated through a method developed by Thomas Eriksson and Anders Silander. However, $\mathcal{S}(t)$ must first be measured before this implementation. In this project the construction of a system that can measure $\mathcal{S}(t)$ is investigated.

1.1 Aim

The goal of this project is to design and construct a system capable of measuring the difference in phase noise at two different times, $\mathcal{S}(t)$. Analysis should be conducted to determine suitable setups. In addition, the sensitivity of the system should be investigated, to provide insight on its performance.

1.2 Scope

To measure $\mathcal{S}(t)$, an Analog-to-Digital Converter (ADC) is used to sample it. However, as one can not sample the phase noise $\phi(t)$ from an oscillator directly, some system is required first. The construction of this system is based on the Delay Line Discriminator (DLD) method. Where a frequency mixer acts as phase detector to

[1]The acronym RADAR refer to RAdio Detection And Ranging, although modern radar can do even more.

suppress the carrier. It accomplish this with a delay line with the delay τ_d and a phase shifter to achieve 90° quadrature between inputs [4]. A simple layout of the DLD is shown in the figure below.

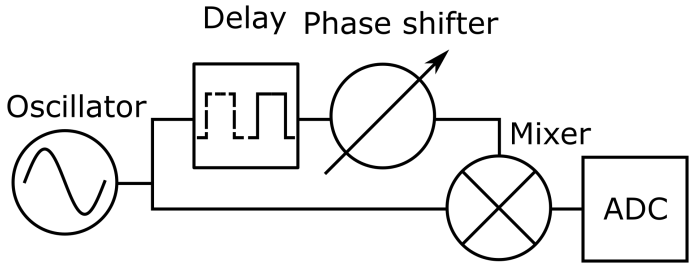


Figure 1.1: Simplified delay line discriminator system for phase noise measurement.

The simulation software AWR Microwave Office allows for simulation of the DLD systems to validate their functionality. Only one frequency is utilized in simulations and constructed systems, namely 1.3 GHz. A frequency in the L-band which is used in many radar systems [3]. Synthetic phase noise is created using the Wiener Process, and has properties suitable for comparing different system setups [5]. First, an initial DLD design is made as a proof of concept followed by an improved DLD design based on the initial results, which is used for measurement in a radar system. The improved DLD is also compared to a variant of the DLD, which utilizes a RF-interferometer for carrier suppression.

1.3 Structure of Thesis

In Theory phase noise is described more in detail. Different techniques for measuring phase noise is covered and the DLD technique is described comprehensively. Information about the operation of crucial components are covered in the end.

In Methods follows a description of how simulations and experiments are conducted in each design. All components in each setup are detailed. A measurement performance in a radar system using the improved DLD design system is done as well.

In Results findings from both simulations and experiments are presented. The obtained results are elaborated on in Discussion and Conclusions. Furthermore, important considerations for constructing the system are presented, with thoughts about the performance possible. Some conclusions are drawn from the project and a proposal is made for further studies.

2
Theory

In this section, a description of phase noise is provided first, followed by a method to simulate phase noise. Then follows a description of the phase noise measurement techniques. Moving on, a model for measurement of phase noise using the DLD is derived. Important considerations for the DLD are stated with focus on the Signal-to-Noise Ratio (SNR) throughout the system. A variant of the DLD called a RF-interferometer is also described briefly. Finally, components in a RF system are detailed with emphasis on specifications of interest in the DLD.

2.1 Phase Noise

A perfect frequency source generates only one output signal with no instability in frequency or amplitude [4]. The most fundamental signal is a sinusoidal AC signal, which can be described by its voltage V(t) as

$$V(t) = A\sin(2\pi f_c t)\,. \tag{2.1}$$

The signal has an amplitude, A, and carrier frequency, f_c. In reality, however, there are instabilities in both instantaneous frequency and amplitude [4]. There are two types of instabilities; long-term stability represent phenomena caused by the aging process of circuit elements, measured over time spans in the order of days to years. On the other hand, short-term stability relates to frequency changes occurring in less than a few seconds. Frequency and phase instability is related and hence it is enough to express just the phase instability [6]. The signal including phase and amplitude noise can be written in the following way

$$V(t) = (A + \epsilon(t))\sin(2\pi f_c t + \phi(t))\,, \tag{2.2}$$

where $\phi(t)$ and $\epsilon(t)$ are the instantaneous phase and amplitude fluctuations from a source (oscillator). The notion of Amplitude Modulation (AM) and Phase Modulation (PM) noise is used to describe amplitude and phase fluctuations respectively. Normally the AM noise is significantly smaller than the PM noise at offsets close to the carrier. Still, there are cases where AM noise is significant or where leakage occurs due to low isolation between mixer ports in the phase detector [6].

The perfect frequency source described by Equation 2.1 will in frequency domain concentrate all power at f_c and $-f_c$. The Fourier transform of real signals are Hermitian, hence only the upper side band is of interest. The noisy signal described by

Equation 2.2 will have a more distributed peak around f_c, as power distributes to frequencies close to the carrier. In addition, there will exist a certain noise power density at all frequencies, which is caused by thermal agitation. It is temperature dependent and has a uniform distribution [4].

Most often the frequency spectrum for phase noise in a signal is symmetric around the carrier and a plot is done on only one side, called SSB. To illustrate the phase noise of a signal, commonly a graph for SSB noise, showing the relative power of the phase noise to the carrier frequency is made (denoted in decibels as dBc). One measures the Power Spectral Density (PSD) at various offsets from the carrier frequency with a certain Bandwidth (BW). The power ratio is then normalised to be the equivalent signal power present in a measurement BW of 1 Hz. Note that phase noise is normally expressed in terms of the relative power (to the total carrier power) in a 1 Hz BW. But this does not mean that the signal is actually measured in a 1 Hz BW [4]. An illustration of phase noise on a carrier can be seen in Figure 2.1. Note that this graph shows the phase noise at both positive and negative offset, meaning it is DSB phase noise. The SSB is 3 dB higher than the DSB phase noise due to the folding of symmetric phase noise to one side.

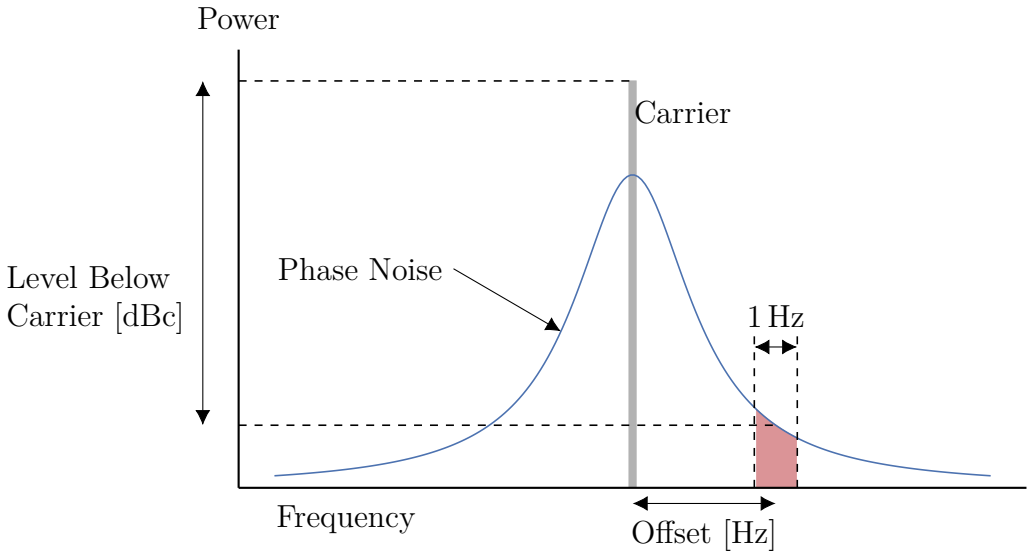


Figure 2.1: Illustration of phase noise in dB below carrier at different offsets.

The power of the thermal noise floor can be calculated as

$$P = k_B T B\,,$$

where k_B is Boltzmann's constant, T is the temperature and B is the BW. Using a 1 Hz BW and a room temperature of 290 K the thermal noise floor has a power of -174 dBm. Assuming real time measurement, this noise level represent the lowest power level a signal could possibly be measured. Note that the noise floor includes all unwanted noise, not just the thermal noise[1].

[1] This is the typical definition of noise floor and the one used in this project.

2.1.1 Simulating Phase Noise using the Wiener Process

There are several possible options to generate phase noise mathematically in order superimpose on a pure signal. One way to simulate phase noise is with a Wiener process [5]. This process, also known as Brownian motion process W_t is characterized by the following properties

- $W_0 = 0$,
- $W_{t+\Delta t} - W_t$, $\Delta t \geq 0$ is independent of $W_s, s < t$,
- $W_{t+\Delta t} - W_t \sim \mathcal{N}(0, \sigma^2 \Delta t)$,
- W_t is continuous in t ,

where σ is the standard deviation. From this, $W_t \sim \mathcal{N}(0, \sigma^2 t)$ is acquired and the covariance of the process at two points x and y where $x < y$, can be written as

$$\begin{aligned}\mathrm{Cov}(W_x, W_y) &= \mathbb{E}\left[W_x W_y\right] = \mathbb{E}\left[W_x\left(W_y + W_{x+\Delta t} - W_{x+\Delta t}\right)\right] \\ &= \mathbb{E}\left[W_x\left(W_y - W_{x+\Delta t}\right)\right] + \mathbb{E}\left[W_x W_{x+\Delta t}\right] .\end{aligned}$$

Since the process is continuous, Δt can be chosen such that $\Delta t \in (0, y-x]$. Using the second property of the Wiener process, one observes that $\mathbb{E}\left[W_x\left(W_y - W_{x+\Delta t}\right)\right] = 0$ since W_x and $W_y - W_{x+\Delta t}$ are independent variables, both with expectation value of zero. By letting Δt tend to zero it is found that

$$\mathrm{Cov}(W_x, W_y) = \mathbb{E}[W_x^2] = \mathrm{Var}(W_x) = \sigma^2 x\,.$$

Thus, a Wiener process can be recognized as a Gaussian process with the kernel $K(x, y) = \sigma^2 \min(x, y)$. This means that a discrete sampling of the process of length N can be described by the probability density function

$$f_W(x_1, ..., x_N) = \frac{\exp(-\frac{1}{2\sigma^2}\mathbf{W}^T \mathbf{\Sigma}^{-1} \mathbf{W})}{\sqrt{(2\pi)^N \det \mathbf{\Sigma}}}\,.$$

Inverting the matrix $\mathbf{\Sigma}_{ij} = \min(x_i, x_j)$ yields a symmetric triangular matrix. The main diagonal is given by

$$\Sigma^{-1}_{ii} = \Delta_i^{-1} + \Delta_{i+1}^{-1},\ i = 1, 2, ..., N-1 \text{ and } \Sigma^{-1}_{NN} = \Delta_N^{-1},$$

where $\Delta_i = x_i - x_{i-1}$ and $x_0 = 0$. Whereas the super- and sub-diagonals are given by

$$\Sigma^{-1}_{i-1,i} = -\Delta_i^{-1},\ i = 2, 3, ..., N \text{ and } \Sigma^{-1}_{i,i-1} = -\Delta_i^{-1},\ i = 2, 3, ..., N\,,$$

respectively. Assuming uniform time steps it can be shown that this process is equivalent to the sequence

$$W_n = W_{n-1} + \sigma f_s y_n, \quad n = 1, 2, ..., N\,,$$

where the random variables y_i are i.i.d. according to the standard normal distribution and f_s is the sampling frequency.

Using the above description, phase noise can be generated depending on magnitude of the σ, allowing the PSD for the simulated noise to also be calculated. First, the following relation holds for the Wiener Process W and the Gaussian noise w:

$$W = \int w dt \,,$$

$$w = \dot{W} \,.$$

This allows the following relation between the Fourier transforms of w and W:

$$\mathcal{F}(w) = j\omega \mathcal{F}(W) \,.$$

The PSD of the Gaussian noise is

$$|F(\omega)|^2 = S_0 = \sigma^2 \,.$$

From this the PSD can be calculated for the Wiener process as

$$\mathrm{PSD}_W = |F(W)|^2 = \left| \frac{F(w)}{\omega} \right|^2 = \frac{S_0}{\omega^2} = \left(\frac{\sigma}{2\pi f} \right)^2 \,.$$

Thus PSD can be calculated in decibels as[2]

$$P_W[\mathrm{dBc/Hz}] = 20 \log \left(\frac{\sigma}{2\pi f} \right) \,.$$

This noise extends to both positive and negative Fourier frequencies and hence this is DSB noise. The following phase noise levels can be calculated at certain offsets for a given σ in Table 2.1.

Table 2.1: DSB phase noise PSD corresponding to σ at a frequency offset of 100 kHz in dBc/Hz.

σ	**0.001**	**0.01**	**0.1**	**1**	**10**	**100**
dBc/Hz (100 kHz)	-176	-156	-136	-116	-96	-76

The simulated noise decays by -20 dB/decade from the carrier frequency, i.e., f^{-2} noise. In reality other types of phase noise is naturally present, but this is the noise studied in this project.

2.1.2 Phase Noise Measurement Techniques

There are several different techniques to measure phase noise of a signal source. In the case of phase noise, measuring usually means creating the SSB plot to illustrate the phase noise at an offset to the carrier. Four different techniques can be utilized in addition to the DLD method. A simple illustration of these can be seen in Figure 2.2.

[2]The phase noise power density is calculated in relation to the carrier power and hence dBc/Hz is the correct unit.

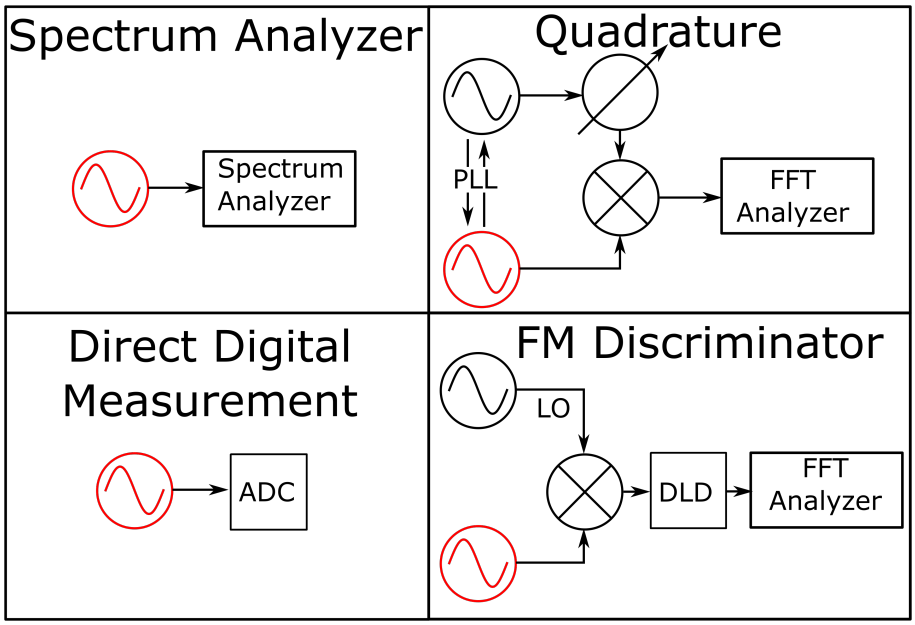


Figure 2.2: Simple illustration of four phase noise measurement techniques for a Unit Under Test (UUT) in red.

2.1.2.1 Spectrum Analyzer Method

This is the most simplistic way of measuring phase noise [7]. By using a readily available spectrum analyzer the phase noise can be extracted in the device and measured directly. Though simple, this method has limited phase noise measuring capability. Since it is a general purpose device, it contains many different components. In particular several Local Oscillator (LO)s that perform up- and down-conversion of the signal. If any LO has more noise than the input signal oscillator, the noise of the input oscillator cannot be measured. In addition, the mixers add noise as well, further reducing the sensitivity of the measurement. The requirement of high quality LOs and mixers leads to expensive spectrum analyzers, or if the input oscillators signal is very pure, no measurement of the UUT can be conducted [4].

2.1.2.2 Quadrature Technique

The quadrature method allows measurement of stable oscillators by use of a reference LO. This LO require at least the same spectral purity as the UUT, ideally much better such that its phase noise can be neglected. The reference LO will generate the same frequency signal as the UUT which is shifted into 90° quadrature. The UUT will have its output direct-converted in a mixer with the reference signal in quadrature, leaving the phase noise of the UUT as an output. Unwanted mixer products are eliminated with a low-pass filter.

This method suffers one major drawback similar to the spectrum analyzer because the reference LO must be of high quality and hence expensive. If the UUT is very pure, measurement is impossible. In addition, the frequency of the UUT and LO must be practically the same, necessitating phase-locking using a Phase Locked Loop

(PLL) [4].

2.1.2.3 FM Discriminator

In principle, the system behaves in a similar way to the DLD method with a discriminator. The difference is an initial down-conversion of the RF input to an Intermediate Frequency (IF) frequency. Since the following discriminator operates at an IF, an amplitude limiter can be used to ensure that the amplitude of the signal into the discriminator is always the same. The lower and predefined IF frequency makes this system easier to operate.

The performance of an Frequency Modulation (FM) discriminator system is limited by the Noise Figure (NF) of the amplifiers and limiters which recover the signal from the output of the mixer, and by the performance of the discriminator itself. In addition, performance also tends to be controlled by the slope of the discriminator. It can measure low phase noise but has limited bandwidth. The requirement of a mixer and LO for the down-conversion is a drawback [4].

2.1.2.4 Direct Digital Measurement

The performance of ADCs have improved over time and this measurement technique simply rely on using an ADC to digitize the signal. Then all the measurement would be conducted in the digital domain. Therefore it relies on use of a high quality ADC with good resolution. Low frequency sources can be directly digitized but higher frequency sources, such as in RF applications, must be down-converted to a lower IF frequency first using a low phase noise LO. Hence this system is similar to previous techniques in its reliance on a low noise LO. The main benefits of this system is that a digital signal is more easily handled [4].

2.1.2.5 Delay Line Discriminator

For both the FM Discriminator and quadrature technique, direct-conversion in a mixer is utilized. Using a delay line on the RF channel, a time difference can be created between the two inputs along with a phase shifter for quadrature. This will cancel the carrier signal in the mixer but allows the difference in phase noise to pass and be down-converted to a frequency offset to DC [4]. A mathematical derivation of this can be seen in Section 2.1.3.

The key advantage of this technique is that it does not require the use of a LO to down-convert the input signal. In fact, this is the only method that does not rely on any LO and this is the principal reason for using this method in this project. Using a more stable LO would defeat the purpose of improving the existing one.

If the frequency of the UUT varies with time, it does not significantly impact the operation of the system, since it simply generates a DC offset at the output. The DLD require calibration for each measurement by adjusting the phase shift to ensure the mixer inputs are in quadrature [4]. The following section provide a more

detailed description of the theory behind this method.

2.1.3 Delay Line Discriminator for Phase Noise Measurements

In the DLD, the mixer acts as a phase detector by multiplying the two input signals. When properly set up, it will have the following input signals, at the RF, and LO ports and corresponding output at IF port:

$$\text{RF} \propto \sin(2\pi f_{RF}t + \phi(t-\tau_d) - 2\pi f_{RF}\tau_d + \varphi)\,, \tag{2.4a}$$
$$\text{LO} \propto \sin(2\pi f_{LO}t + \phi(t))\,, \tag{2.4b}$$
$$\text{IF} \propto \cos(2\pi(f_{RF} - f_{LO})t + \phi(t-\tau_d) - \phi(t) - 2\pi f_{RF}\tau_d + \varphi)\,,$$

where τ_d is the time delay incurred by the delay line. Here double frequency and Intermodulation Distortion (IMD) components are ignored. The amplitude of the IF output will be decreased due to mixer operation, which is described by the Conversion Loss (CL). This CL is accounted for separately, and not included here. Using the phase shift φ, the following equality should be calibrated

$$\varphi - 2\pi f_{RF}\tau_d = \frac{\pi}{2} + n\pi, \quad n \in \mathbb{Z}\,.$$

Note that the phase shift φ should put the two input signals in quadrature. Small deviations from perfect quadrature does not degrade the measurement significantly. For example, a 10° deviation correspond to around a 0.35 dB error in phase noise measurement [8]. Using direct-conversion in the mixer followed by a low-pass filter to remove the product with double the frequency yields

$$\cos(2\pi(f_{RF} - f_{LO})t + \phi(t-\tau_d) - \phi(t) + \frac{\pi}{2})\,.$$

Since the RF and LO frequency are the same here, the following output is created:

$$-\sin(\phi(t-\tau_d) - \phi(t))\,.$$

Since the phase noise $\phi(t)$ is commonly minute, the small angle approximation can be used to simplify the expression as linear, yielding

$$-(\phi(t-\tau_d) - \phi(t))\,.$$

For real measurements some scaling factor will be present that relates the measured quantity with $\mathcal{S}(t)$. There will also be more noise present in the system, the sum of $\mathcal{S}(t)$ and other noise will be called $\mathcal{M}(t)$. To move into the frequency domain, the Fourier transform with $\omega = 2\pi f_{RF}$ is used on the signal, yielding

$$-\mathcal{F}(\phi(t))(e^{j\omega\tau_d} - 1)\,,$$

where $\mathcal{F}$ is the Fourier transform. By multiplying with the complex conjugate, the PSD of $\mathcal{S}(t)$ can be calculated as

$$2|\mathcal{F}(\phi(t))|^2(1-\cos(\omega\tau_d)) = 4|\mathcal{F}(\phi(t))|^2\sin^2(\frac{1}{2}\omega\tau_d)\,.$$

The nodes in the frequency response of the $\mathcal{S}(t)$ will be found at integer n spacing when

$$\frac{1}{2}\omega\tau_d = \pi f\tau_d = \pi n, \quad n \in \mathbb{N}\,.$$

Hence, the Fourier frequency at each node is

$$f = \frac{n}{\tau_d}\,.$$

The calculated period for a few different time delays can be seen in the Table 2.2. An extended time delay will yield a short period. Hence the nodes can appear inside of the desired BW, an eventuality that will have to be accounted for in the signal processing step.

Table 2.2: The period of the nodes in the non-linear filter for different delays.

Time Delay (τ_d)	10 ns	100 ns	200 ns	500 ns	1 µs	2 µs
f_{period}	100 MHz	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz

2.1.3.1 System as Non-Linear Filter

The aforementioned frequency response acts as a non-linear filter on the phase noise, denoted $\mathcal{H}(f, \tau_d)$. The frequency response in dB of this filter at a frequency offset f can be calculated as

$$\mathcal{H}(f, \tau_d) = 10\log(4\sin^2(f\pi\tau_d))\,.$$

For illustration, the filter response at a 100 kHz offset for different delays can be seen in Table 2.3.

Table 2.3: The non-linear filter response for different time delays at 100 kHz offset frequency.

Time Delay (τ_d)	**10 ns**	**100 ns**	**200 ns**	**500 ns**	**1000 ns**	**2000 ns**
$\mathcal{H}(100\,\text{kHz}, \tau_d)$ (dB)	-44.0	-24.0	-18.0	-10.1	-4.2	1.4

Hence a shorter delay will attenuate $\mathcal{S}(t)$ close to the carrier more severely. In this project, f^{-2} noise is typically analyzed which has the unique property that the PSD of phase noise decrease by 20 dB per decade. Simultaneously, the filter has the inverse property with 20 dB less attenuation per decade for low frequencies. This means that $\mathcal{S}(t)$ at a at close offsets will be virtually the same, assuming these frequencies are within half a period of f_{period}.

2.1.3.2 System Signal-to-Noise Ratio

The SNR is defined as the ratio of the input carrier signal power to the noise power density (consisting of all undesired signals). While the thermal noise floor is uncorrelated in frequency with the same PSD for all frequencies, noise generated by certain components can vary over frequencies. However, the noise added is assumed to be uniform over all frequencies. Note that the measuded phase noise $\mathcal{S}(t)$ is not considered to be part of the noise floor since it is not an undesired signal here.

The system is comprised of six distinct stages and at each stage the SNR is potentially affected. All these stages are illustrated in Figure 2.3. The thermal noise floor (TN) is the lowest level the noise floor can be reduced to.

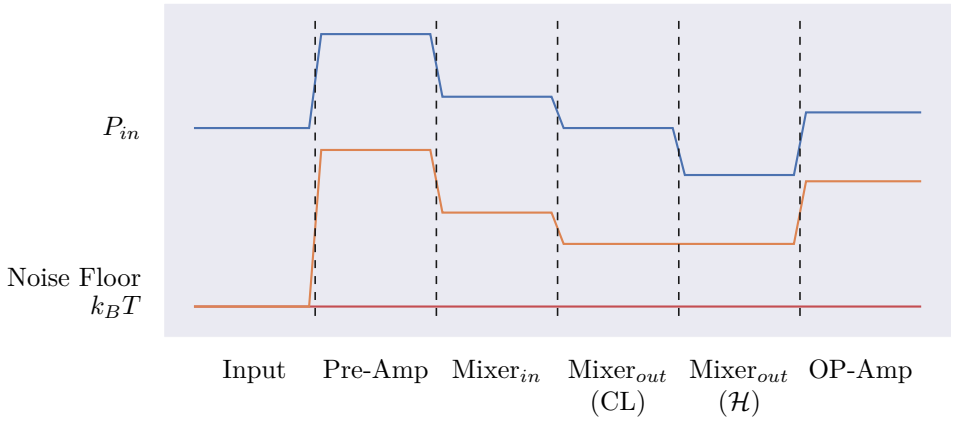


Figure 2.3: Illustration of the different power levels of the input carrier P_{in} and noise floor at various stages in the system, with the thermal noise floor TN included for reference.

The stages are summarized in Table 2.4. The first stage is the signal from an oscillator, with carrier power P_{in}, along with a thermal noise floor. The phase noise of this signal is not considered here directly but can at its lowest be related to signal SNR at output. At the input, signal SNR will be

$$\mathrm{SNR_{in}} = \mathrm{P_{in}} - \mathrm{TN}\,.$$

The pre-amplifier increases the power of carrier, phase noise and noise floor alike with the same constant gain G_{PA}. This is essential because without it any loss of power in subsequent components would reduce the power of both the carrier and the phase noise, but not the thermal noise floor, since it cannot be lowered (without cooling). Therefore, subsequent component could lower SNR, but this buffer mitigates this. Losses suffered will simply reduce all levels equally and hence no SNR will be lost. In addition, if sufficient gain is provided, noise contribution from subsequent components should be small or even negligible. The noise added by the pre-amplifier is defined by NF_{PA} and reduce SNR somewhat, but it is often a worthwhile investment, and the use of a Low Noise Amplifier (LNA) with low NF would limit the loss.

The RF input of the mixer has Insertion Loss (IL) suffered along the way and

is denoted IL_{tot}. Ideally with enough gain no SNR is lost at this stage.

Both mixer stages are in fact occurring simultaneously, but are split into two stages for clarity. First is simply the CL of the mixer. Any noise added by the mixer is disregarded, as it is assumed to be insignificant. This is however an important assumption to keep in mind, as it may not be valid in all cases.

The second mixer stage, on the other hand is the effect of the non-linear filter the mixer cause in a DLD system. Here the carrier is completely suppressed, but for the purpose understanding of the SNR in the system it can still be considered conceptually. In which case, the frequency response of the filter on phase noise at a specific frequency offset can be considered to attenuate the carrier equally, even though in reality the carrier is suppressed completely. This allows calculation of the signal SNR which corresponds to the lowest $\phi(t)$ measurable at this offset frequency.

The final stage is the OP-AMP which amplifies the output signal. The noise NF_{out} added by this amplifier is negligible if the noise floor out of the mixer is significantly higher than the thermal noise floor. However, it has the potential of reducing the SNR by NF_{out}

Table 2.4: Summary of the effect on the carrier and noise floor throughout the DLD system stages.

Stage	**Carrier**	**Noise Floor**
1. Input	P_{in}	Thermal Noise Floor, $-174\,\mathrm{dBm/Hz}$
2. Pre-Amplifier	Gain (G_{PA})	Gain (G_{PA}) and noise (NF_{PA})
3. Mixer Input	Insertion loss (IL_{tot})	Insertion loss (IL_{tot})
4. Mixer Output (CL)	Conversion loss (CL)	Conversion loss (CL)
5. Mixer Output ($\mathcal{H}$)	Non-linear filter on phase noise Carrier Suppressed	Unaffected
6. OP-AMP	Gain	Gain and noise (NF_{out})

The output SNR of the system at a frequency f is $SNR_{out}(f)$ and become the following:

$$\begin{aligned} SNR_{out}(f,\tau_d) =& SNR_{in} + \mathcal{H}(f,\tau_d) - NF_{Out} - \\ & - \begin{cases} NF_{PA}, & \text{if} \quad G_{PA} + NF_{PA} > IL_{tot} + CL \\ CL + IL_{tot} - G_{PA} - NF_{PA}, & \text{else}\,. \end{cases} \end{aligned} \tag{2.5}$$

The SNR at the output defined in this way determines the lowest measurable $\phi(t)$ by the system. For example, if the SNR at the output is 140 dB then the lowest measurable $\phi(t)$ for the given input signal is $-140\,\mathrm{dBc/Hz}$ at the frequency offset this calculation was conducted with. This is illustrated in Figure 2.4.

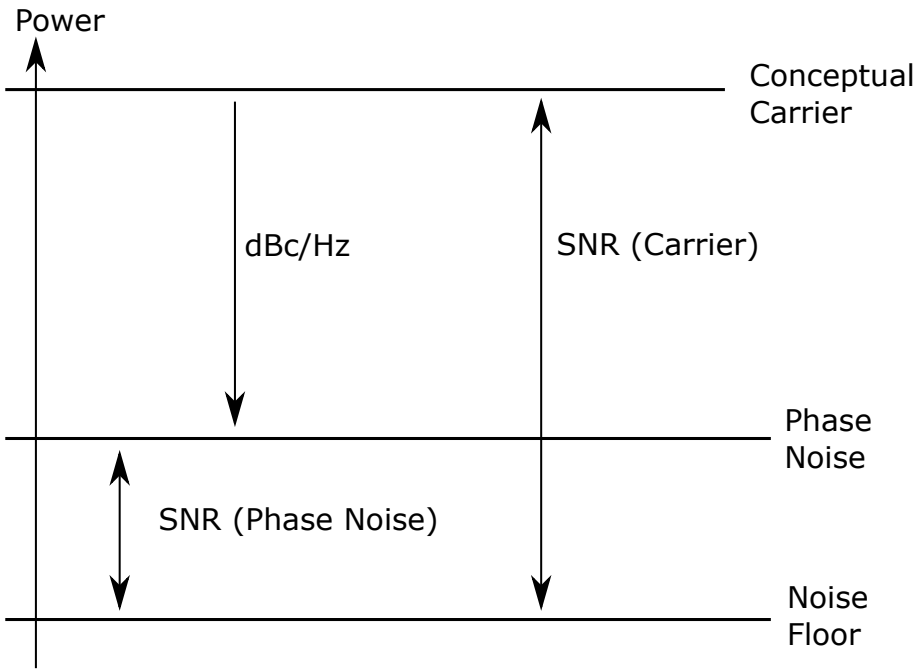


Figure 2.4: Illustration of the power levels for the conceptual carrier, phase noise and noise floor along with the SNR and phase noise at dBc/Hz below the carrier.

Looking at this figure, the following example can also be made: Assuming a conceptual carrier signal at the output at $-20\,\text{dBm}$ with a noise floor at $-150\,\text{dBm}$, and a phase noise power at $-100\,\text{dBm}$ (for some offset). Then the SNR for the signal is $130\,\text{dB}$, while the phase noise has a SNR of $50\,\text{dB}$. The phase noise is $-80\,\text{dBc/Hz}$ in this case and it is measureable in the system. In fact, phase noise as low as $-130\,\text{dBc/Hz}$ could be measured, albeit with zero SNR. At least a few dB of SNR is required, since the noise floor is gaussian distributed. A higher phase noise SNR will make the measurement more accurate. In the light of signal processing on the result, it also defines the magnitude of the phase noise suppression.

2.1.3.3 Definitions and Calculation of Noise

There are different ways to define the noise added from components in a system. One way is to use the input referred noise, while another is the NF. The level of the noise floor will then typically be specified in dBm/Hz. Hence a relation between these are required.

2.1.3.3.1 Input Referred Noise The input referred noise is the noise voltage that when applied as input to a noiseless circuit generates the same output noise as the actual circuit does. It is specified in $\text{nV}/\sqrt{\text{Hz}}$. The noise in an OP-AMP is typically specified this way. However, in RF systems the NF is more common.

2.1.3.3.2 Noise Figure The noise factor is the ratio of input and output SNR, while the NF is this quantity converted to dB. In RF systems the NF is normally specified at 290 K and 50 Ω impedance. However, it can be specified for another ref-

erence temperature and impedance instead, in which case the formula for calculating the NF is

$$\mathrm{NF} = 10\log(\frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}}) = 10\log(1 + \frac{\mathrm{N_{added}}}{\mathrm{N_{in}}})\,. \tag{2.6}$$

Where $\mathrm{N_{in}}$ is the power of the noise floor entering the system and $\mathrm{N_{added}}$ is the input referred noise added by the component, both in $\mathrm{nV^2\,Hz^{-1}}$ [9]. The $\mathrm{N_{in}}$ can be specified for the thermal noise floor but also for any other noise floor of interest. To relate PSD to $\mathrm{nV^2\,Hz^{-1}}$ the following relation is used (assuming $50\,\Omega$ impedance)

$$N = 50 \times 10^{(P+150)/10}\,. \tag{2.7}$$

Where P is the PSD of the noise floor and N is the mean square noise voltage density in $\mathrm{nV^2\,Hz^{-1}}$.

2.1.3.4 RF-Interferometer variant

The DLD can be modified to suppress the carrier power at the RF port of the mixer by introducing a RF-interferometer which can be calibrated to suppress the carrier power $\sim 30 - 40$ dB [6][10]. A schematic for the RF-interferometer can be seen in Figure 2.5. By adding the time delayed signal with the direct signal 180° out of phase the carrier is suppressed. This allows more amplification before the RF port without saturating the mixer. By placing the LO in quadrature with both the direct and delayed signals at the RF port, a similar result to the DLD is achieved. Using the RF-interferometer the white noise which is the noise floor would also be subject to the non-linear filter described above. A complete derivation pertaining to the RF-interferometer can be seen in Appendix E.

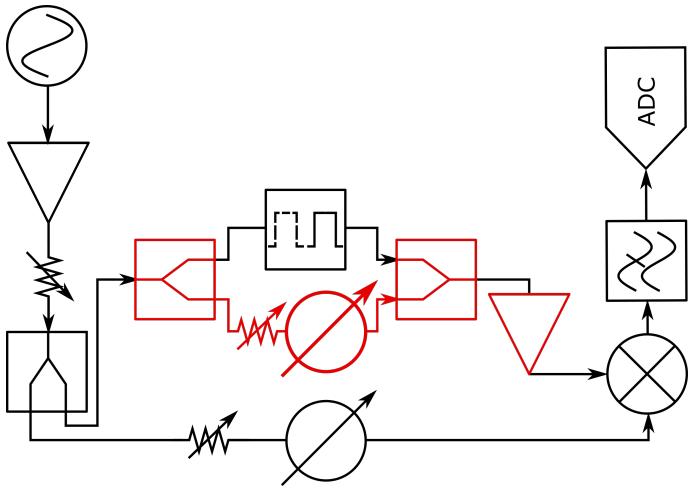


Figure 2.5: Illustration of RF-interferometer circuit, where the components marked in red constitute the modification to the DLD.

The suppression of the carrier w.r.t. power balance and phase error was also derived and is illustrated in Figure 2.6. Observe that for more than 30 dB of suppression, power and phase error are small, less than around 0.1 dB and 1 degree respectively.

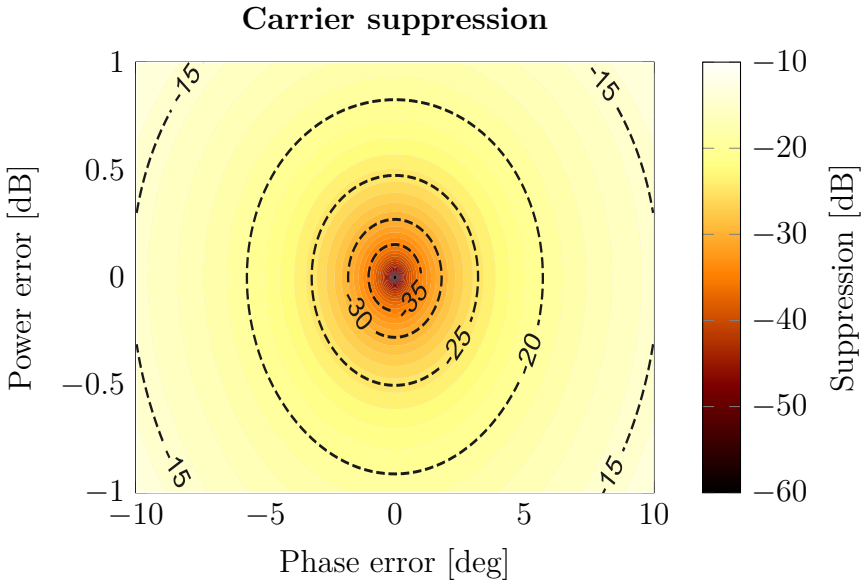


Figure 2.6: Suppression of the carrier using the RF Interferometer, depending on the deviation in both power and phase at the power combiner input ports. The y-axis show the power ratio between the direct signal against the time delayed signal while the x-axis show the phase error from 180° phase difference.

2.2 RF System

The components used in the system may have different functions in different systems. Here the emphasis is on their use in the DLD but some description of their general usage is also provided.

2.2.1 Oscillator

An oscillator is a signal generator. The theory of operation for a feedback oscillator is the following: power is turned on which produce noise in the circuit which is then amplified before being diverted into a feedback network. In the feedback network a filter function is applied to leave a desired signal, which is then returned to the input port to combine with the original signal in the same phase, and then passing the circuit again. When started the oscillator have a feedback factor greater than one providing positive feedback. Eventually the feedback factor reaches one, and the oscillator enters steady-state and a stable signal is generated [11]. The layout of a feedback oscillator can be seen in Figure 2.7.

2.2.2 Power Amplifier

The purpose of a power amplifier is to increases the power of an input signal, and both the amplitude of voltage and current in the signal may be increased, although it is commonly voltage. This key parameter is the gain of the amplifier, which is typically specified in the 3 dB bandwidth. Amplifiers designed for RF applications often have less gain than lower frequency amplifiers, but also have larger emphasis

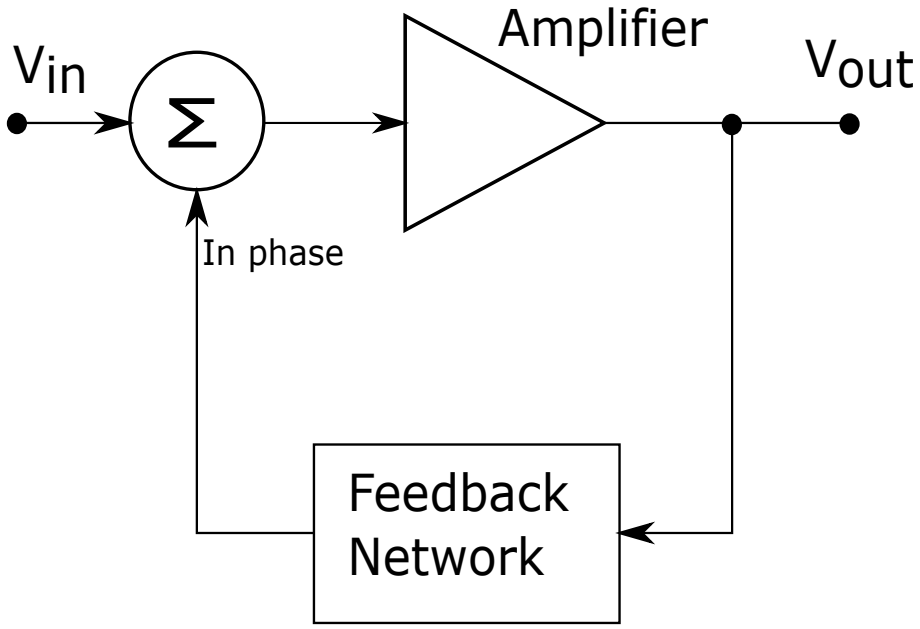


Figure 2.7: Illustration of the operation of a feedback oscillator where a portion of the amplifier output is diverted back through a feedback network.

on low noise performance [12].

The linearity specifies how much gain can be provided over input power levels. Once the input power is high, the gain in the amplifier will decrease and more input power yields less gain. Furthermore, the third order intercept can become important if high input powers are used, as it is an estimate of the size of IMD at the output [13].

The amplifier is an active device and as such, it also generates noise as it operates. The amplifier will raise the noise floor by its gain, but there is more noise added as well, defined by the NF. If multiple amplifiers are used in cascade. The amplifier with the lowest NF should be put first, according to Friis formula [14].

A specific type of amplifier of interest in this project is the Low Noise Amplifier (LNA). Commonly used to amplify weak signals, where added noise could could have dire impact on the SNR. Therefore its NF has to be as low as possible [13].

2.2.3 Power Divider

The purpose of a power divider is to split a signal at an input port into two or more output ports. Typically this involves two output ports and the power of the signal in either output may not be the same. It is a passive component and does not provide any gain. Hence there will be an IL.

For an equal split power divider, the outputs have the same power. The relative power exiting each output is therefore $-3\,\mathrm{dB}$ compared to input. The IL is added on this and less than half the input power exits the output ports. A power divider

can also be used as a power combiner by reversing operation [15].

2.2.4 Delay Line

The purpose of this component is to incur a delay in the transmission of a signal. It is simple to realize a digital delay, the signal is fed into one end of a shift register, and it appears at the other end after N clock periods, where N is the length of the register. An analog delay is more difficult to implement even though the operation of an analog delay line is, in essence, very simple. It takes time for signals to reach their destination, but signals typically travel very fast, close to the speed of light. The issue is the length required to achieve a delay more than a few nanoseconds without resorting to the use of an impractically long cable. For perspective the delay will be around 4 ns per meter of cable. The size of the delay line can be decreased by lowering the speed the signal travels.

In electromagnetic delays a delay is achieved with small physical size but limited delay (a few ns). A helical delay line wound around an insulating core is smaller than a coaxial cable but larger than the electromagnetic delay, and can give hundreds of ns delay for a modest size. One delay line that can yield a considerable delay in the range of µs is the acoustic delay line, such as a Surface-Acoustic-Wave (SAW) delay line. It uses a medium which slows the speed of the signal considerably, down to 10^4 m/s which gives $1\,\mu s\,cm^{-1}$, which allows a small delay line with a relatively long delay. The IL suffered from longer delays are however often considerable. To achieve even longer delay, up to seconds, one has to resort to recording and reproducing the signal [16].

2.2.5 Phase Shifter

The purpose of a phase shifter is to change the phase of a signal. It is a passive device that has several different types of implementations. Some provide a fixed phase shift and while others can be switched between different values. All phase shifters are analog but the way they are steered could vary between analog, digital and mechanical [17]. Relative to a delay line the time delays here tend to be very short and hence the size of the phase shifter must not be large [18]. The most straightforward way to design it is similar to the delay line, where a time delay is used. If the frequency is fixed, the length of the transmission line could be chosen to give the desired shift. If different shifts are desired, an implementation is to have a reference signal path for 0° phase shift and a switch that can be set to a number of transmission lines with different length, corresponding to different phase shift. This is called a switched delay line, whose main drawback is its frequency dependence [17].

The most common control elements in analog phase shifters are varactor diodes, whose capacitance can be varied with applied voltage. Varactor diode phase shifters are practical with few diodes, large phase shift and great phase resolution but suf-

fer several drawbacks compared to other types of phase shifters. Such as lowered accuracy, narrow bandwidth and low input power (less than 30 dBm) [18].

2.2.6 Frequency Mixer

The frequency mixer creates new output signals from two inputs. There are both active and passive mixers, the passive type will not provide any gain and a power drops at output compared to the RF input. The active type provide gain and require a power source, but also tend to generate more noise [19].

The inputs are called the RF and LO inputs. The RF signal is usually the frequency of interest and is up- or down-converted using the LO signal. The LO input signal drives the mixer and typically requires more power. The output is referred to as the IF signal. With two signals of frequency ω_{RF} and ω_{LO} the ideal output is a multiplication of the signals and trigonometry yields the following result:

$$\cos(\omega_{\mathrm{RF}}t)\cos(\omega_{\mathrm{LO}}t) = \frac{1}{2}\cos[(\omega_{\mathrm{RF}} + \omega_{\mathrm{LO}})t] + \frac{1}{2}\cos[\omega_{\mathrm{RF}} - \omega_{\mathrm{LO}})t]\,,$$

where the RF input is both up- and down-converted. There are also generation of harmonics of the input signals, which are also multiplied with sum and difference frequencies at the output. This is illustrated in Figure 2.8.

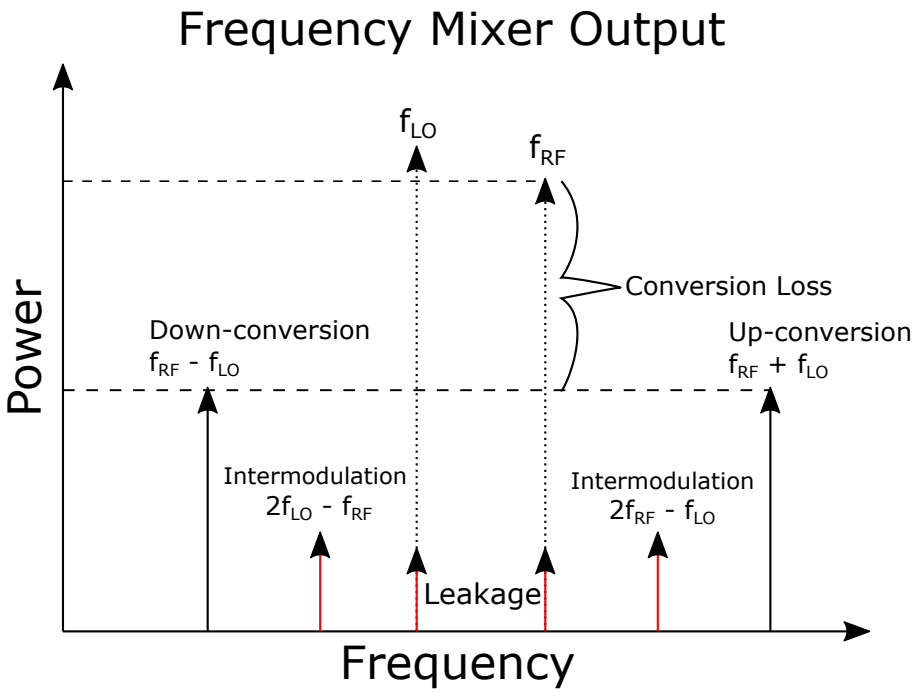


Figure 2.8: Illustration of the output from a frequency mixer. It performs both up- and down-conversion but also have leakage of the input signals along with harmonics or intermodulation.

There are two different mechanisms of operation for a mixer. There is the nonlinear transfer function but it is rarely used in practical applications. The other one work by switching and the faster the switching frequency the better the performance is,

e.g. less spurious signals [20].

The amount of RF and LO that leaks to output can be reduced by balancing the mixer which increase isolation. An unbalanced mixer leaks a lot of RF and LO but a (single) balanced mixer reduces this, and a double or triple balanced mixers even more so. Although more balancing leads to more complex mixers and hence increased cost. In addition, they require higher LO power to drive them [20].

Important parameters to consider for a passive mixer can be seen in Table 2.5.

Table 2.5: Description of mixer parameters.

Parameter	Impact
Conversion Loss (CL)	Reduces power at output
1-dB Compression Point	Input power level the CL increase by 1 dB
Third Order Intercept Point	Input power the IMD reach the same size as input signal
Isolation	Specifies leakage between ports
Noise Figure	Noise added by component to output signal

The CL in an ideal double-balanced switching mixer is 3.92 dB, but in practice it is higher. The 1-dB compression point defines when non-linear behavior starts to occur, e.g. increase in CL. Larger input powers also increase IMD products, which can be estimated via the third order intercept point[3]. It is often not possible to insert this much RF power, it rather acts as a reference to how large the IMD becomes. Isolation specifies the leakages of signal between the ports, LO-to-RF, LO-to-IF and RF-to-IF. Finally the NF of the mixer is the amount of noise added to the output signal, similar to an amplifier [21].

However, the NF of the mixer varies, depending on whether the signal is SSB or DSB. A SSB signal is a signal where the RF and LO signal is different, leading to noise folding. The folding is a result of the conversion of the image of the RF signal at the opposite side of the LO signal (frequency domain). Assuming equal noise floor at the image result in doubled noise power at the output. The NF for an ideal mixer and with a SSB signal is therefore 3 dB. However, when a mixer is used for direct-conversion, both RF and LO signal have identical frequency and no folding degrade the SNR. Hence DSB signals have a NF of 0 dB. Although noise will be added due to the non-ideal operation of the mixer [22].

[3]Specifically the third order intercept point specifies when the third order products of the intermodulation is the same size as the RF signal at output.

2.2.7 Analog-to-Digital Converter

The ADC measures the ratio of the analog input value to a reference value and then represents it as a digital value. A key parameter in an ADC is its resolution which is determined by the amount of bits and the amplitude of the reference. A 8 bit ADC with reference amplitude of 1 V could sample with a resolution of $\frac{1}{2^8}$ = 3.9 mV. This smallest resolution is often called the Least Significant Bit (LSB) since it is the smallest value a bit could quantify a signal. Values between the LSB will be converted to the closest representable value and the error compared to the real analog value incurred due to rounding, is quantization error. More bits or a smaller reference amplitude improves resolution. However, any signal that surpass the reference amplitude produce the maximum numeric value and hence cannot be accurately represented.

For best result using an ADC the signal peak should coincide with the peak amplitude since a weaker signal would use fewer bits and hence have worse resolution and therefore more quantization error.

The sampling rate of the ADC is also of paramount importance. It must adhere to the sampling theorem and hence the sampling rate must be at least twice the highest frequency sampled, in order to avoid aliasing. It is common to employ a low-pass or anti-alias filter which attenuates all out of band frequencies appropriately.

There are sources of error in the ADC such as offset error, gain error and non-linearity error. Without going into details on these, it is common for an ADC to specify an effective number of bits. These are fewer than those actually used in the ADC but account for the errors these errors. For example a 16 bit ADC could have 14 effective number of bits [23].

3
Methods

The project was divided into different parts, with the first as a proof of concept for the system. It was decided to measure $\mathcal{S}(t)$ using the conventional DLD. This method was first validated using components at hand in the initial DLD design, followed by an improved DLD design. The improved design was first tested before being employed in a radar measurement. The improved design was also analyzed in AWR with a comparison to the RF-interferometer. The RF-interferometer was also studied through rudimentary experiments.

3.1 Initial Delay Line Discriminator Design

Before creating the first design, the system had to be analyzed from a theoretical perspective first. In Theory important considerations for the DLD method are stated, in particular the SNR for the phase noise measurement in Section 2.1.3.2. This theory was used to design an appropriate setup of the circuit. In Figure 3.1 the layout of this system can be seen.

3.1.1 Components

The components used are summarized in Table 3.1. To generate signals containing phase noise, a dual-channel Digital-to-Analog Converter (DAC) was used. It was attached to the Field Programmable Gate-Array (FPGA) AD7S-v2. The DAC was configured through *ACE* and waveforms uploaded with *DPGdownloader*. The channel interpolation was set to 4, the datapath interpolation to 8 and the data rate was set to 3.9 GHz. The phase noise was generated on top of an 10 MHz signal while the NCO was set to 1.29 GHz resulting in $\phi(t)$ superimposed on an 1.3 GHz signal.

The pre-amplifier supply voltage was 15 V, and had a band-pass filter at its input. The delay line was a 50 m long coaxial cable. In order to use it, two approximately 1.4 m SMA-cables were used to connect it. These cables and the coaxial cable comprised the total delay line.

The mixer was designed for down-conversion all the way to DC. Meaning it could be used for direct-conversion. After the mixer a low-pass filter was used followed by the ADC in order to digitize the signal.

To connect all components, SMA-cables were used. Which were used according

to requirement and does not affect the system performance significantly. The use of attenuators were also employed to provide desirable power levels to components. Specifically at the LO channel in order to bring the LO power to the specified 7 dBm LO level. But also to limit the RF input power at the mixer to a manageable level.

Table 3.1: Inventory of the components used in the initial DLD design detailing the model and manufacturer along with some noteworthy specifications.

Component	Model	Manufacturer	Key Information
FPGA	ADS7-v2	Analog Devices	
DAC	AD9174	Analog Devices	Max output power: −3 dBm
Pre-Amplifier	ZVE-2W-272X+	Mini-Circuits	Bandpass filter 1.2-1.4 GHz Max Output: 32 dBm
Power Divider	PD1120	Instock Wireless	Max input power: 46 dBm
Delay Line	FSJ4-50B	CommScope	2 x 1.4 m SMA cables Total delay: 219 ns
Phase Shifter	PA0102	Clear Microwave	360° voltage controlled Max input power: 27 dBm
Mixer	ZEM-4300	Mini-Circuits	LO Level: 7 dBm Compression point: 1 dBm Max RF input: 17 dBm
Low-pass Filter	SLP-50+	Mini-Circuits	50 MHz cutoff
ADC	NI PXIe-5170R	National Instruments	14 bit resolution

3.1.1.1 Component Testing

Measurements were done component-wise to determine their IL, by measuring the output power of a component, as well as the power when said component was bypassed. Powers were measured using a spectrum analyzer. The gain from the pre-amplifier was measured in the same way as the IL in the other components. The measured losses and gain can be seen in Table 3.2. The total loss of the RF channel comprising the Power Divider, Phase Shifter and Delay along with Attenuator 1 was subsequently 27.4 dB.

Table 3.2: Gain and losses in initial DLD design.

Component:	Gain/Loss:
Pre-Amplifier	34.7 dB
Power Divider	−3.2 dB
Delay	−10.2 dB
Phase Shifter	−4.0 dB
Mixer (No Compression)	−4.2 dB
Attenuator 1	−10 dB
Attenuator 2	−9 dB

The CL through the mixer was measured by generating a RF- and LO-signal from the two channels in the DAC at two different frequencies, such that the IF frequency

did not overlap with the spectrum analyzers inherent DC signal. The LO signal was set to 1.3 GHz and the RF was set to 2.5 MHz higher than the LO. The CL was measured for RF input power from −10 dBm to 10 dBm to characterize it from the linear region as well as in compression. The CL of the mixer for different RF input powers can be seen in Appendix B.

3.1.2 AWR Simulation

The software *AWR Microwave Office* was used to model the initial design. The *Visual System Simulator (VSS)* was used to create a system diagram for the design. The entire description for the AWR setup can be seen in Appendix A. Simulation revealed that the design was theoretically feasible, facilitating the experimental setup.

3.1.3 Experimental Setup

For the experiment involving the initial design, phase noise was chosen for the simulations. This phase noise was generated using the Wiener Process, with the procedure outlined in Appendix C. A few σ were chosen and data files generated for their corresponding phase noise $\phi(t)$.

The initial circuit was constructed as shown in Figure 3.1 with the aforementioned components. Measurements were done with the DAC generating a signal with $\phi(t)$ from the data files superimposed. In addition, one experiment was conducted without any superimposed phase noise, allowing measurement of the DACs $\phi(t)$. A measurement with an open channel on the ADC was done as well to measure the noise of the ADC. The measurements were 500 ms long and performed with a sampling frequency of 125 MHz, achieved by setting the decimation factor to two for the ADC. The ADC was controlled via LabView.

The phase shifter was adjusted with a voltage source through an ocular inspection of the measured signal in LabView so that the signal had a 0 V offset which correspond to approximately a 90° phase shift between RF and LO.

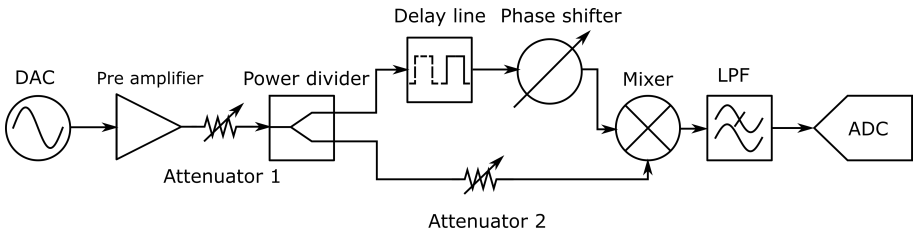


Figure 3.1: The circuit of the initial DLD design.

3.2 Improved Delay Line Discriminator Design

While the first design showed the feasibility of the DLD for measurement of phase noise, it suffered from unwanted noise at close in offsets. An OP-AMP was added at the input to the ADC to remedy potential noise in the ADC, and increase the number of bits used. In addition, the following was also added: a higher LO level mixer and a capacitor to remove DC from the output. The new design was not modelled directly in AWR, since it behaved similarly to the initial DLD design. However, a variant of the DLD was proposed using an RF-interferometer and this was compared to the conventional DLD in AWR.

3.2.1 Components

Another DAC was used and it was configured same way as in the initial design. The system setup was similar and is outlined in Figure 3.2. The same pre-amplifier, power divider, delay line and low pass filter were used. All components used for this design are summarized in Table 3.3.

Table 3.3: Inventory of the components used in the improved DLD design, detailing the model and manufacturer along with some noteworthy specifications.

Component	Model	Manufacturer	Key Information
FPGA	ADS7-v2	Analog Devices	
DAC	AD9162	Analog Devices	Max output power: 1 dBm
Pre-Amplifier	ZVE-2W-272X+	Mini-Circuits	Bandpass filter 1.2-1.4 GHz Max Output: 32 dBm
Power Divider	PD1120	Instock Wireless	Max input power: 46 dBm
Delay Line	FSJ4-50B	CommScope	With 2 × 1.4 m SMA cables Total delay: 219 ns
Phase Shifter	PA0102	Clear Microwave	360° voltage controlled Max input power: 27 dBm
Phase Shifter	Coaxial Model 3752	Narda	180° Mechanical
Mixer	ZX05-43H-S+	Mini-Circuits	LO Level: 17 dBm Compression point: 14 dBm Max RF input: 20 dBm
Lowpass Filter	SLP-50+	Mini-Circuits	50 MHz cutoff
OP-AMP	AD829JRZ	Analog Devices	Configured for 32 dB Gain 5 MHz Bandwidth (± 5 V)
ADC	NI PXIe-5170R	National Instruments	14 bit resolution

The OP-AMP was a surface mounted device that required a Printed Circuit Board (PCB) for operation. The evaluation board UG-755 accepts 0402 and 0602 surface mounted components. The feedback was created using a 50 Ω and 2 kΩ resistor to create a voltage gain of 40 or conversely, a 32 dB power gain. A 50 Ω resistor was used at the input for impedance matching in addition to a 4.7 µF capacitor. This

creates a high pass filter with cutoff around 700 Hz. SMA contacts were soldered to its input and output to allow connection with the rest of the system. For the UG-755 evaluation board to operate to correctly, the trace from pin 1 was removed, otherwise the feedback would yield a significant DC offset at the output. While different supply voltages can be used for the device, the OP-AMP was only driven at $\pm$ 5 V.

3.2.1.1 Components Testing

The new mixer and OP-AMP were investigated to verify their specifications. The CL through the mixer was measured with the exact same setup as before, described in Section 3.1.1.1. The CL for different RF input powers can be seen in appendix B.

The OP-AMP was investigated for its gain and to make sure the bandwidth was adequate. The output power of the DAC was compared to the output power from the OP-AMP between 1 MHz and 13 MHz in 0.5 MHz increments.

The measured gain and loss of the components used for the improved design can be seen in Table 3.4. The total loss of the RF channel with Attenuator 1 is subsequently 15.4 dB.

Table 3.4: Gain and losses in components of improved DLD design.

Component:	Gain/Loss:
Pre-Amplifier	34.7 dB
Power Divider	−3.2 dB
Delay	−10.2 dB
Phase Shifter (PA0102)	−4.0 dB
Phase Shifter (Narda)	−0.5 dB
Mixer (No Compression)	−5.6 dB
Output Amplifier	32 dB
Attenuator 1	−2 dB
Attenuator 2	−2 dB

3.2.2 AWR Simulation

The AWR simulation of the previous initial DLD system provided all necessary information about the system when used as a conventional DLD. Therefore the final design was instead compared to another variant of the DLD when a interferometer was used on the RF channel in order to suppress the carrier before it enters the mixer. The setup in AWR for these two DLD variants is explained in Appendix A.

3.2.3 Experimental Setup

Three different $\phi(t)$ were used at the experiment. Two of these were phase noise generated using the Wiener Process which were superimposed on the DACs, just as in the previous experiment. The maximum size of the system output noise $\mathcal{M}(t)$ was limited by the peak-to-peak voltage the ADC could handle. Hence the largest σ was set to 20. The setup for the experiment was done with the components described above and configured according to Figure 3.2.

Note that there were two different phase shifters specified. An initial experiment was first done using the PA0102 but this still yielded the same unwanted noise in $\mathcal{M}(t)$ at close in offset as the initial DLD design. Hence this phase shifter was replaced with the coaxial phase shifter. The noise was only present for the lowest $\phi(t)$ source, i.e. the DAC and hence the result from this measurement was kept for comparison. The new phase shifter had lower IL and this was compensated using 3 dB of extra attenuation. The experiment was then conducted using the new phase shifter. Through occular inspection, it was adjusted without the OP-AMP such that no DC offset was present in the ADC. Because calibration could not be conducted with the OP-AMP connected as the added capacitor removed DC offset at its input. Finally the measurements was done with the OP-AMP connected. The measurements were 500 ms long with a sampling frequency of 125 MHz and the voltage reference increased when required to avoid over-saturation.

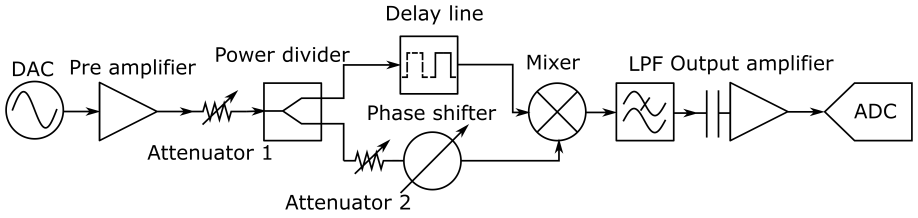


Figure 3.2: The circuit of the improved DLD design.

3.3 System Performance in Radar Measurements

The system was always intended to be used for application in a radar system. Therefore a measurement on such a system was conducted. The setup is illustrated in Figure 3.3. The system used in the experimental setup in Figure 3.2 was modified by removing the attenuators and splitting the DAC and pre-amplifier from the rest, which is labeled as the DLD. An identical power divider was used to split the output from the DAC in order to also drive the LO input on a mixer that performs down-conversion of the radar pulse. An attenuation of 19 dB was added before the mixer to bring the power to an adequate level. The mixer used was consequently the one from the initial design (ZEM-4300), which was sufficient for down-conversion of the radar pulse.

The radar pulses were output directly from a DAC into the mixer. The down-converting LO had added phase noise generated with a standard deviation $\sigma = 20$.

The radar pulses were 10 MHz linear chirps with a 10 kHz pulse repetition frequency and a 50 % duty cycle. Two channels were configured for the ADC to digitize both signals. The signal sources and the ADC were triggered with a pulse generator to align the measurement with the pulse data and $\mathcal{M}(t)$ data.

The data was exported to Anders Silander for testing of the proposed method. This method is not included in this project and as such no result is provided of it.

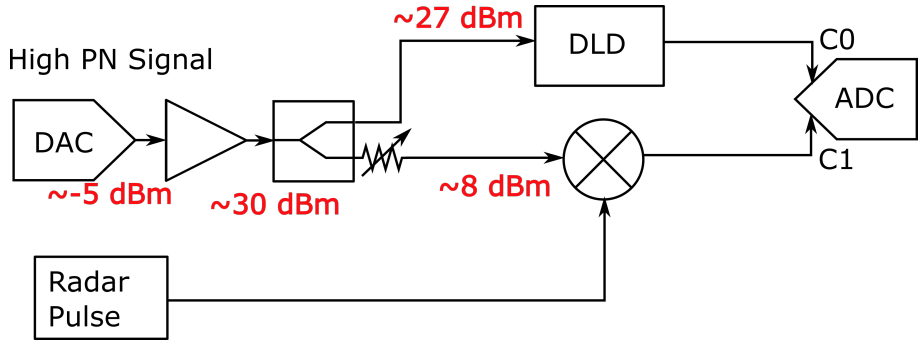


Figure 3.3: The circuit of the Radar measurement using the improved design labelled DLD.

3.4 RF-Interferometer Design

Due to the potential improvements the RF-interferometer yields, it was studied with an experiment as well. Some new components were introduced, like a new low-pass filter with a 5 MHz cutoff and two phase shifters of Narda Model 3752 and three power dividers of model PD1120 were used instead of one each. A new RF-power amplifier was added at the RF-channel before the mixer, and it was a Mini-Circuits ZX60-2522MA-S+, providing 24 dB of gain. The circuit schematic can be seen in Figure 3.4. Attenuators were added to match the inputs to the power combiner. First the output power of the delay line was measured using the spectrum analyzer to 16.5 dBm. Then 4 dB of attenuation was added to the other channel and its output measured. The output was close to the same but tweaking was done using SMA-cables to get the same output at the spectrum analyzer, 16.5 dBm. However, the measurement accuracy was no better than 0.2 dB in the spectrum analyzer. The output from the power combiner was then measured and the phase shifter adjusted to provide the lowest possible power, which were -20.7 dBm. Subtracting the loss from the power combiner, which were -3.2 dB, the carrier suppression was 34 dB.

The setup for generating signals were similar to the previous designs, using the DAC AD9162. The $\phi(t)$ of the DAC was measured along with superimposed $\phi(t)$ using $\sigma = 20$. In the ADC the recordings were 2.68 s long and performed with a sampling frequency of 12.5 MHz.

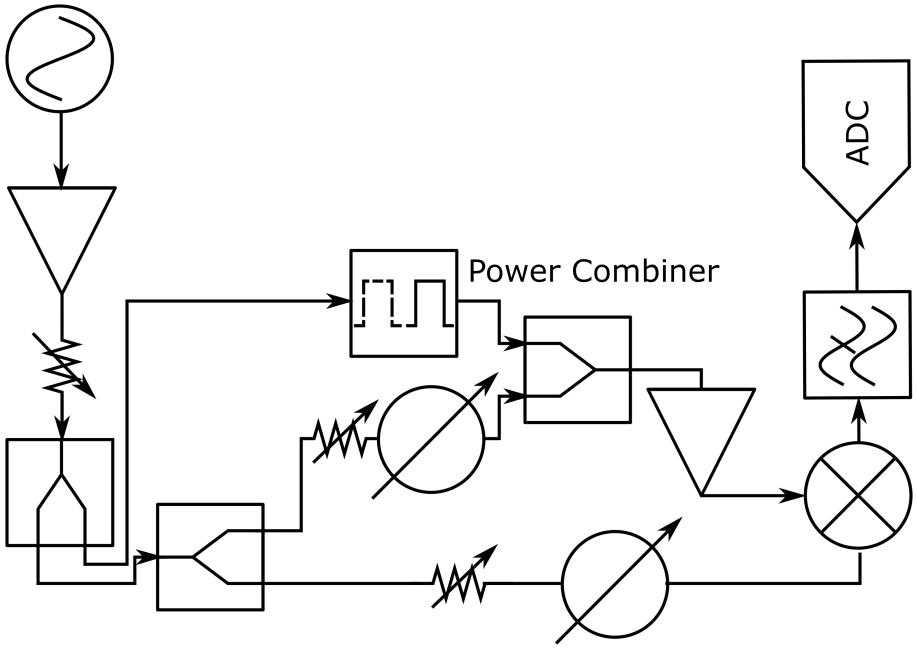


Figure 3.4: The circuit of the RF-interferometer design.

4
Results

All results are summarized into sections corresponding to the initial DLD design, improved DLD design and radar measurement. A final section regarding the RF-interferometer experiment is also included.

4.1 Initial Delay Line Discriminator Design

The PSD of $\mathcal{M}(t)$ at system output corresponding to $\sigma = 51$ simulated in AWR can be seen at the initial DLD system output in Figure 4.1. The resulting measurement $\mathcal{M}(t)$ has a flat curve up to around 1 MHz offset and at around 4 MHz offset a node is seen followed by another period before the 10 MHz offset, which is a clear effect of the non-linear filter acting on the phase noise.

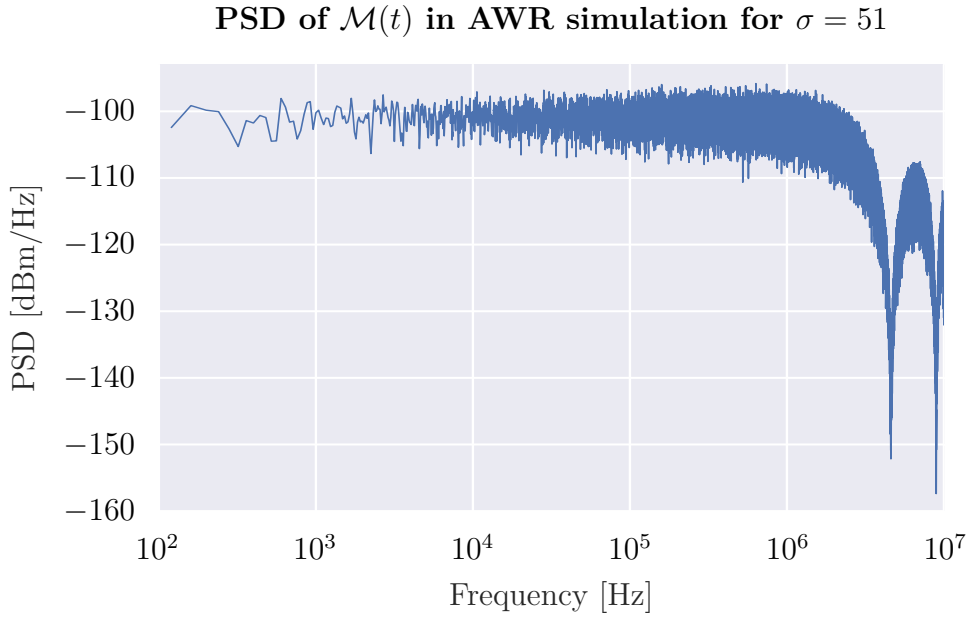


Figure 4.1: The PSD in AWR simulated initial system with $\phi(t)$ generated with the standard deviation $\sigma = 51$.

Next, a similar result for the experimental setup for the PSD of $\mathcal{M}(t)$ for four different types of input $\phi(t)$ can be seen in Figure 4.2. Phase noise $phi(t)$ generated corresponding to $\sigma = 51$ is at output $\mathcal{M}(t)$, which can be seen around -101 dBm/Hz, a level similar to the AWR simulation. In addition, the line provides the theoretically predicted $\mathcal{S}(t)$ for the system measurement at -100.2 dBm/Hz. A weaker $\phi(t)$

corresponding to $\sigma = 5.1$ can also be seen along with a line for its prediction. Additionally, the $\mathcal{M}(t)$ of the DAC is visible as well. Both of these exhibit a noise not predicted at a low offset, seen as a slope rising out of the otherwise flat line. Lastly, the noise in the ADC lies around $-160\,\mathrm{dBm/Hz}$ far from the carrier but exhibit an increased noise close to DC.

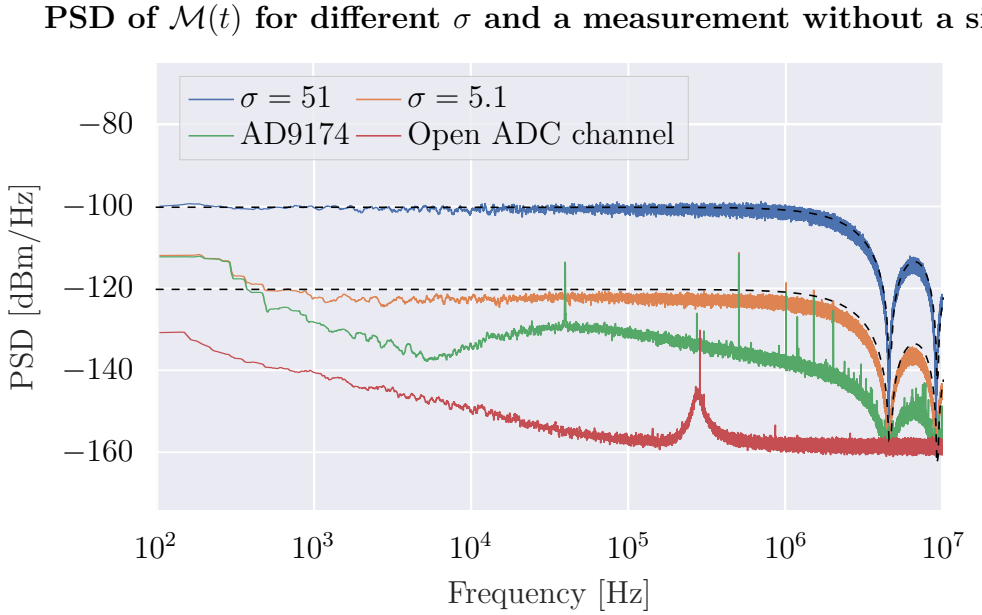


Figure 4.2: The measured PSD for the signals containing the generated phase noise as well as a measurement with an open ADC channel. The blue line corresponds to phase noise generated from standard deviation $\sigma = 51$, the orange line corresponds to phase noise with standard deviation $\sigma = 5.1$, while the green line correspond to the inherent phase noise of the DAC and the red line corresponds to the inherent noise of the ADC.

4.2 Improved Delay Line Discriminator Design

The improved DLD design was investigated in a number of different ways. First the experimental result for $\mathcal{M}(t)$ are shown. Then a comparison is provided showing how a simulation of the improved DLD system stacks up to a proposed variant with a RF-interferometer.

4.2.1 Experimental Results

The PSD for different $\mathcal{M}(t)$ in the improved DLD design can be seen in Figure 4.3. The measurements with $\sigma = 20$, $\sigma = 5$ and the single tone measurements were conducted using the coaxial phase shifter while the other single tone measurement was done with the PA0102. The measurements are attenuated compared to the expected results for frequencies below 1 kHz due to the DC blocking capacitor and above 5 MHz due to the bandwidth of the OP-AMP. Despite this, when the coaxial

phase shifter was used, $\mathcal{M}(t)$ of the single tones did not align at all with expectation. Some other noise was present at closer offsets than 2 kHz.

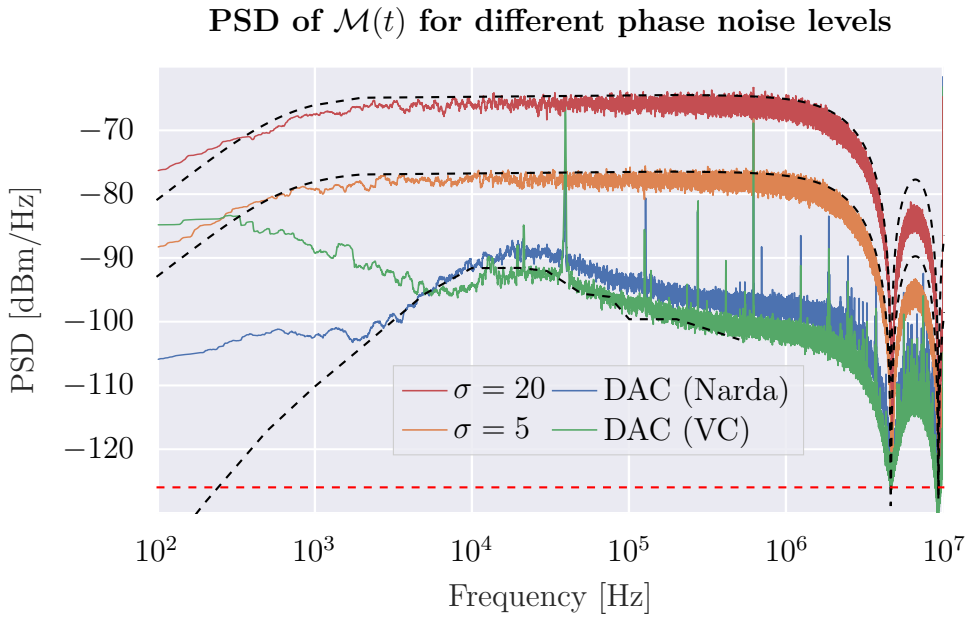


Figure 4.3: The red and the orange curves show the measured PSD when phase noise generated with $\sigma = 20$ and $\sigma = 5$ were used respectively. The blue and the green curves have no added phase noise. The green curve use the same Voltage Controlled (VC) phase shifter as the previous system while the blue curve use a coaxial phase shifter. The dashed black lines represent the expected PSD of the measurements and the dashed red line is the expected noise floor.

4.2.2 AWR Simulation

The simulation involving AWR for the two variants of the DLD are compared in Figure 4.4. The SNR of the two systems over frequency offset reveals that the interferometer yields improved SNR at close offsets but has a slightly lower SNR around 1-3 MHz. The PSD of $\mathcal{S}(t)$ is lower in the interferometer variant but so is the noise floor. From around 100 kHz offset the output noise floor is at the thermal noise floor.

4.3 RF-Interferometer Experiment

The experiment for the RF-interferometer along with a comparison to the DLD can be seen in Figure 4.5. These show similar results, although since the interferometer uses an amplifier, it should have larger measured PSD. The main difference is around 1 MHz where the interferometer shows an unexpectedly $\mathcal{M}(t)$. At low offsets the PSD of $\mathcal{M}(t)$ converge, an indication that another source of noise is present here, obscuring the DACs $\mathcal{S}(t)$. An experiment using the RF-interferometer and $\phi(t)$

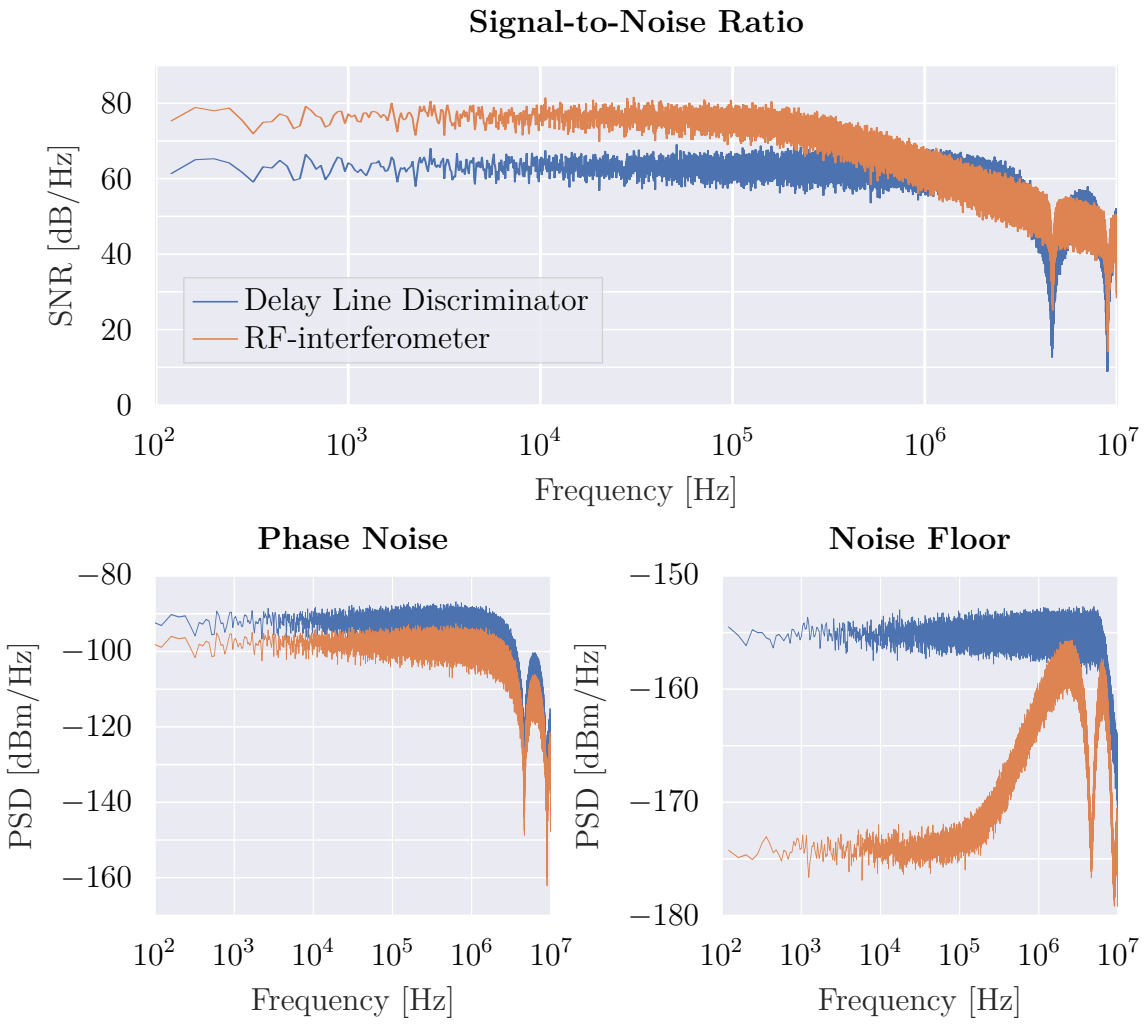


Figure 4.4: The SNR for $\mathcal{S}(t)$ with $\sigma = 20$ in the RF Interferometer and DLD between 100 Hz and 10 MHz offset, along with the measured PSD of phase noise and noise floor.

corresponding to $\sigma = 20$ was also done. These measurements $\mathcal{M}(t)$ follow a flat profile. However, it does not drop much at the node (around 4 MHz).

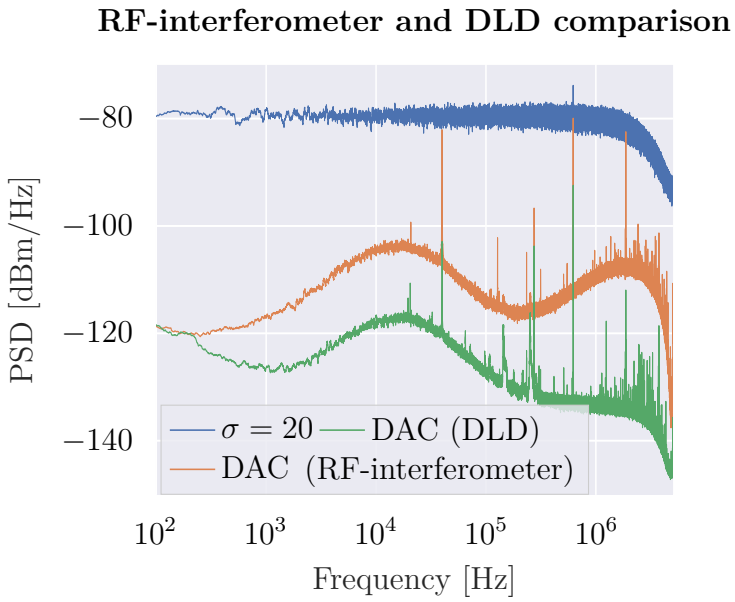


Figure 4.5: Measured PSD of $\mathcal{M}(t)$ in RF-interferometer design.

5
Discussion

A discussion of the result from the different designs are done separately. Then a section follows that provide considerations for the DLD system in general. Which is concluded with thoughts on future work related to his project.

5.1 Initial Design

The result from the AWR simulation shown in Figure 4.1 suggests the DLD method can perform phase noise measurements. Noise from a Wiener process should be flat and this is precisely what is observed. Because the Wiener phase noise decrease $-20\,\mathrm{dB/decade}$ and the non-linear filter has 20 dB less attenuation per decade. At least this will be true when looking at frequencies lower than half the period of the filter. The period of the filter should be around 4 MHz and this corresponds well with the node seen.

The experimental result in Figure 4.2 has a similar characteristic to the AWR result when f^{-2} noise is measured, proving the methods feasibility. It shows $\mathcal{S}(t)$ as predicted for $\sigma = 51$, aligning with theoretical predictions too, but for σ=5.1 $\mathcal{M}(t)$ has unwanted noise present around 100-500 Hz. The same unwanted noise appears in the DACs noise measurement as well. The DACs $\phi(t)$ is low close to the carrier and hence it should decrease for lower offset frequencies, shown in the data sheet in [24] for the DAC $\phi(t)$. Instead it increase from around 6-7 kHz, meaning noise is produced by some system component. The noise from the ADC was a potential source but it was measured separately and included in the same figure, clearly it is lower than the observed noise. Although, if this noise was not present, one should observe noise from the ADC in $\mathcal{M}(t)$.

This noise in the ADC at 100 Hz is around $-130\,\mathrm{dBm/Hz}$. Hence, one require amplification of the output signal to bring $\mathcal{S}(t)$ above this level. Additionally, it is desirable to use as many of the bits in the ADC as possible. By adding gain through an output amplifier, the resolution improves. The gain of the amplifier should be enough to ensure the ADC is not a limiting factor.

We can estimate the lowest noise floor at system output to be the thermal noise floor at $-174\,\mathrm{dBm/Hz}$, and in that case 44 dB of gain is enough at 100 Hz offset. At 1 kHz offset the noise is around $-140\,\mathrm{dBm/Hz}$, and then 34 dB gain is enough. The noise floor is likely a bit higher at the system output than the thermal noise, slightly

less gain is probably required. This estimate was used to determine reasonable gain for the OP-AMP, at 32 dB.

There is one issue though, the amplification will limit how large $\mathcal{S}(t)$ can be measured. The ADC can only handle a certain peak-to-peak voltage in its measurements and larger phase noise gives larger peaks. The largest peak-to-peak voltage the ADC can measure is 5 V [25]. Based on measurements shown in Appendix F one can estimate that a peak-to-peak voltage of 5 V correspond to a (for the Wiener process) PSD for $\mathcal{S}(t)$ of -55 dBm/Hz. This maximum was somewhat of an estimate and therefore -60 dBm/Hz is probably the max limit of PSD of $\mathcal{M}(t)$ to be measured in the output. Remember that $\mathcal{M}(t)$ is the actual output including all noise while $\mathcal{S}(t)$ is just the phase noise that has passed through the system from the oscillator.

5.2 Improved Design

The OP-AMP should remove any issue of noise in the ADC, eliminating one source of error. The system used limited the maximum σ to approximately 45, based on the estimate above. In Figure 4.3 the result is similar to previous measurement of $\mathcal{M}(t)$ for $\sigma = 20$ and $\sigma = 5$. Both show a flat curve but at a higher PSD than before, which is the $\mathcal{S}(t)$ output we expect in the dotted lines. The non-linear filter period is the same as before but the noise at close offset is lowered. This is due to a capacitor added to block DC at the input of the OP-AMP. The first order high-pass filter this produces should have a cutoff at 700 Hz and the dotted lines show the expected filter response on the noise which line up decently with $\mathcal{M}(t)$ for both cases. Although $\mathcal{M}(t)$ seem to be reduced a bit earlier at around 1 kHz. A possible explanation is that exact capacitance and resistance in use are not exactly the stated value, or the OP-AMP input interferes. Regardless, it is not a significant problem as phase noise below 1 kHz is only a fraction of the entire bandwidth of interest, which extends to 5 MHz.

The other experiments are compared to the expected $\mathcal{S}(t)$ from the DAC (AD9162) in [26], which is the $\mathcal{S}(t)$ that one could measure theoretically in the system, indicated by the other dotted curve. This was in fact an estimate and was not expected to line up perfectly, since the specifications for the signal are only similar, not identical. Its main purpose is to show what level $\mathcal{M}(t)$ should be around at very close offsets. First, one can conclude that $\mathcal{S}(t)$ of the DAC could be measured accurately down to an offset of a few kHz. Secondly, the presence of noise generated in the phase shifter PA0102 was identified. An unexpected result that swapping the phase shifter uncovered. Swapping to a new phase shifter (Narda Model 5732) the result improved. The noise from the phase shifter was not subject to the non-linear filter and thus not attenuated for low frequency phase noise. This implies extra consideration of noise performance of components in a single channel should be made. After swapping phase shifters the result still did not align with the expected line, indicating there was further noise caused by components in the system. We conclude it was probably not the noise originating from the OP-AMP which is constant from 100 Hz, and much lower, as can be seen in Appendix D.

It is likely that the cause of this noise is the mixer. It was assumed no noise was caused by the mixer previously, but mixers do generate noise at close in offsets [21]. The typically small NF is specified at large offsets and therefore the mixer is a likely source here. The noise of the ADC increase at close offsets, so it is reasonable to assume a mixer does as well. Therefore a conclusion would be that the mixer should be considered more carefully in the design.

The only other direct source of noise is the power amplifier. Power amplifiers do add additive phase noise to input signals [27], a consideration that was neglected when designing these experiments. Looking at the phase noise in the power amplifiers measured by Mini-Circuits in [27], the worst phase noise is $-128\,\mathrm{dBc/Hz}$ at 100 Hz, which is added onto the signal from the DAC. Looking at its specifications in [26], a 1.8 GHz output signal using a DAC sampling frequency of 4 GHz (close to our specifications) has a phase noise of $-110\,\mathrm{dBc/Hz}$, much worse. So it is unlikely that the power amplifier is the cause of the noise. Although it is a potential issue if one can measure very low phase noise oscillators.

If this system is considered theoretically, no noise should have been added by the phase shifter and mixer. Although it could not be measured directly, the noise these components add at 100 kHz offset should be minute and hence here the system should behave as the theory predicted. This means that the lowest measurable SSB $\phi(t)$ can be predicted using Equation 2.5 and would be $-143\,\mathrm{dBc/hz}$ at 100 kHz offset, providing an estimate of the systems sensitivity.

5.3 RF-Interferometer

Investigation of the RF-interferometer as an alternative to the conventional DLD reveals some interesting aspects. The AWR simulations in Figure 4.4 show the interferometer can increase the SNR at closer offsets and improve sensitivity. $\mathcal{S}(t)$ behaves similarly. However, the noise floor is reduced by the non-linear filter in this case (down to thermal) and this is where the improvement in SNR occurs. The 6 dB difference in the PSD of $\mathcal{S}(t)$ is caused by the two power dividers. The improvement in SNR close in should be the reduction in the noise floor, which is around 19 dB, with the 6 dB reduction in phase noise, hence 13 dB improvement in SNR is achieved.

In this simulation no amplifier was added at the mixer input, and hence one sees the thermal noise floor below 100 kHz offset. By adding an amplifier, phase noise and noise floor can be raised before the mixer. This provides a major advantage in this method. First of, the OP-AMP used previously should become redundant. Secondly, the higher noise floor before the mixer could prevent noise from the mixer from corrupting the measurement.

Looking back at Figure 4.3, the presumed mixer noise is measured at $-105\,\mathrm{dBm/Hz}$, but has been both amplified by the OP-AMP and reduced by the DC blocker, hence at mixer output it should be around -105-32+17 = $-120\,\mathrm{dBm/Hz}$. Consequently, in

order to avoid this noise from corrupting the measurement, one would require 54 dB of gain in addition to the CL in the mixer. This is perhaps an unreasonable gain, so the presumed mixer noise in this case is unavoidable. However, if consideration was taken when choosing the mixer, perhaps the mixer noise could be lower, which means less gain might be required.

The experiment result of the RF-interferometer can be seen in Figure 4.5. The intention was to show the feasibility of this method in practice but the result was less than ideal. A different $\mathcal{M}(t)$ from the DAC was observed, likely due change in the external clock used. It was however compared to a DLD setup identical to the previous improved design without OP-AMP, so conclusions could be drawn between them. A bump was shown at 1 MHz for the interferometer $\mathcal{M}(t)$, which is difficult to give a good explanation for. Secondly, the predicted level from $\mathcal{M}(t)$ using $\sigma = 20$ deviated from the expected value around -75 dBm/Hz a bit. Both the RF-interferometer measurements are lower than expected which indicate a faulty calibaration of the system. The RF-interferometer is likely harder to calibrate for accurate measurements. These are issues that can be investigated more in the future.

The measurement did however collaborate the aforementioned hypothesis that the mixer added noise. Since in both the RF-interferometer and DLD setup, $\mathcal{M}(t)$ was measured at -120 dBm/Hz at 100 Hz offset. Despite the two system having different PSDs at the output for the same frequency offsets otherwise. The RF-interferometer had amplification before the mixer which seems to allow measurement at close offsets before mixer noise starts to corrupt, proving the RF-interferometer indeed performs better at closer offsets, even when there is mixer noise.

5.4 Considerations for the System

There are several considerations for the system of importance. One is the impact of phase noise on a LO, several more regards the bottlenecks in the DLD. Finally, an estimation of sensitivity in the conventional DLD and the RF-interferometer is discussed.

5.4.1 Oscillator phase noise impact

Commonly, an oscillator drives the LO for a mixer in a receiver or transmitter. In receivers, the mixer down-converts an input signal to a lower frequency IF signal, where the LO ideally produce a signal with all of its power at one single frequency. This would yield a perfect down-conversion of the signal. However, the phase noise $\phi(t)$ of the LO will "smear" the input signal in the output IF signal. This could itself be an issue but an even more troublesome issue would be the presence of a large interfering signal close to the input signal [28]. This intereferer is in radar referred to as clutter [2]. This interferer would then also be down-converted close to the IF and in addition, be "smeared" out, which could result in the desired input signal being masked in the sideband of the interferer [28]. A similar issue can occur when a strong signal with large $\phi(t)$ and a weaker signal is transmitted separately.

When received, the large $\phi(t)$ of the first signal could then directly mask the second, weaker signal even though the signals have different frequencies. This does not even take into account the ramifications of mixing after receiving.

In this case, the presence of phase noise very close to the carrier might not be a big issue. Large phase noise further from the carrier would be the main culprit and this is a motivation as to why we limit our measurements at 100 Hz in this project. Sensitivity from 1 kHz to a few MHz might be the most important frequency offsets of interest. Although it will depend on the exact phase noise characteristics of the oscillator.

5.4.2 Bottlenecks in the Delay Line Discriminator

The sensitivity of the DLD are impacted by all the components. However, some are more crucial and constitute the bottlenecks that limit the lowest measurable phase noise, comprising the oscillator, delay line and frequency mixer.

5.4.2.1 Oscillator output power

The system is intended to work in tandem with a LO and therefore it can only use a portion of the power the LO require for its operation. The output power of an oscillator varies between types but an output of more than 10 dBm is common [9]. This scale is logarithmic and a few dB is a big difference in power. Therefore a handful dBm of power should be possible to divert into the DLD.

5.4.2.2 Delay Line

While a long delay line has been stated as desirable, the IL will increase with the delay along with the physical size of the delay line. The two main options for a delay line is either a SAW-filter or a coaxial cable as in this project. The SAW-filter is smaller but has high loss in addition to a limited maximum input power for the carrier. In [29] a SAW delay for 1.1 GHz was constructed with 2.8 dB IL and propagation loss 31.9 dB/µs and compression point at 30.4 dBm. Such a delay designed for 1.3 GHz would not impose any restrictions on the designs in this project. Meaning it can match the performance of the coaxial cable without large physical size. All in all, the performance of a SAW delay line cannot quite match a coaxial cable except at physical size. Although the other bottlenecks in the system means it performs similarly.

5.4.2.3 Frequency Mixer

In the mixer the limiting factor is the compression point. Even if the input power could be increased e.g. larger SNR at input. More input power will linearly increase the CL. A maximum output power will be reached and hence the 1-dB compression point is a key consideration when choosing mixer in addition to its specified CL as these set the Dynamic Range (DR) of the mixer.

The RF-interferometer suppresses the carrier which coupled with an amplifier improves the DR in the mixer (for phase noise measurement). However, there is a limit to the suppression and hence this method is also limited by the mixer, although it is mitigated.

5.4.3 Phase Noise Measurement Sensitivity

The lowest measurable phase noise for the two methods can be compared. The discussed bottlenecks gives some indication of the best sensitivity possible. Firstly, as mentioned around 10 dBm of input power is possible and not an unreasonable assumption for the system. Furthermore, a decent pre-amplifier can output around 30 dBm (1 W). More than that would however quickly become expensive in all respects. The compression point of the mixer is assumed at 15 dBm and ideally a mixer has about 4 dB of CL, factor the compression in at this point and the loss is 5 dB. The delay for the proposed system is assumed it can handle the conditions it is put through with desired delay. Furthermore, the NF of an OP-AMP is difficult to reduce and over 10 dB is normal. As such, any used is assumed to have at least 10 dB of NF. The assumptions made can be seen in Table 5.1.

Table 5.1: Assumptions for the comparison of the DLD and the RF-interferometer in ideal setup.

Component or Stage	**Assumption**
Input power	10 dBm
Pre-Amplifier Output	30 dBm
Mixer	P1dB = 15 dBm No Noise
Delay Line	Provides any delay desired 12 dB insertion loss
OP-AMP	NF = 10 dB
Power Dividers	No insertion loss
All Components	Noise generated distributed uniformally

The RF-interferometer was assumed to have enough suppression and subsequent gain to avoid mixer compression and ADC-noise. Using these assumptions, the sensitivity of the two systems could be estimated and can be seen in Figure 5.1. The difference in sensitivity is also compared and it is clear that the RF-interferometer has better sensitivity for all frequency offsets and delays.

The DLD require the use of an OP-AMP and will therefore lose 10 dB of SNR, in addition to SNR lost from the pre-amplifiers NF, which were disregarded here (because it is low). However, the measurements in the project shows that the noise from the mixer is a major issue close to the carrier. Perhaps at a large offset, the OP-AMP is limiting, however, from perhaps 10 kHz and closer, the mixer limits measurements instead. It will have a NF at around 50 dB at 100 Hz. So the SNR here is abysmal

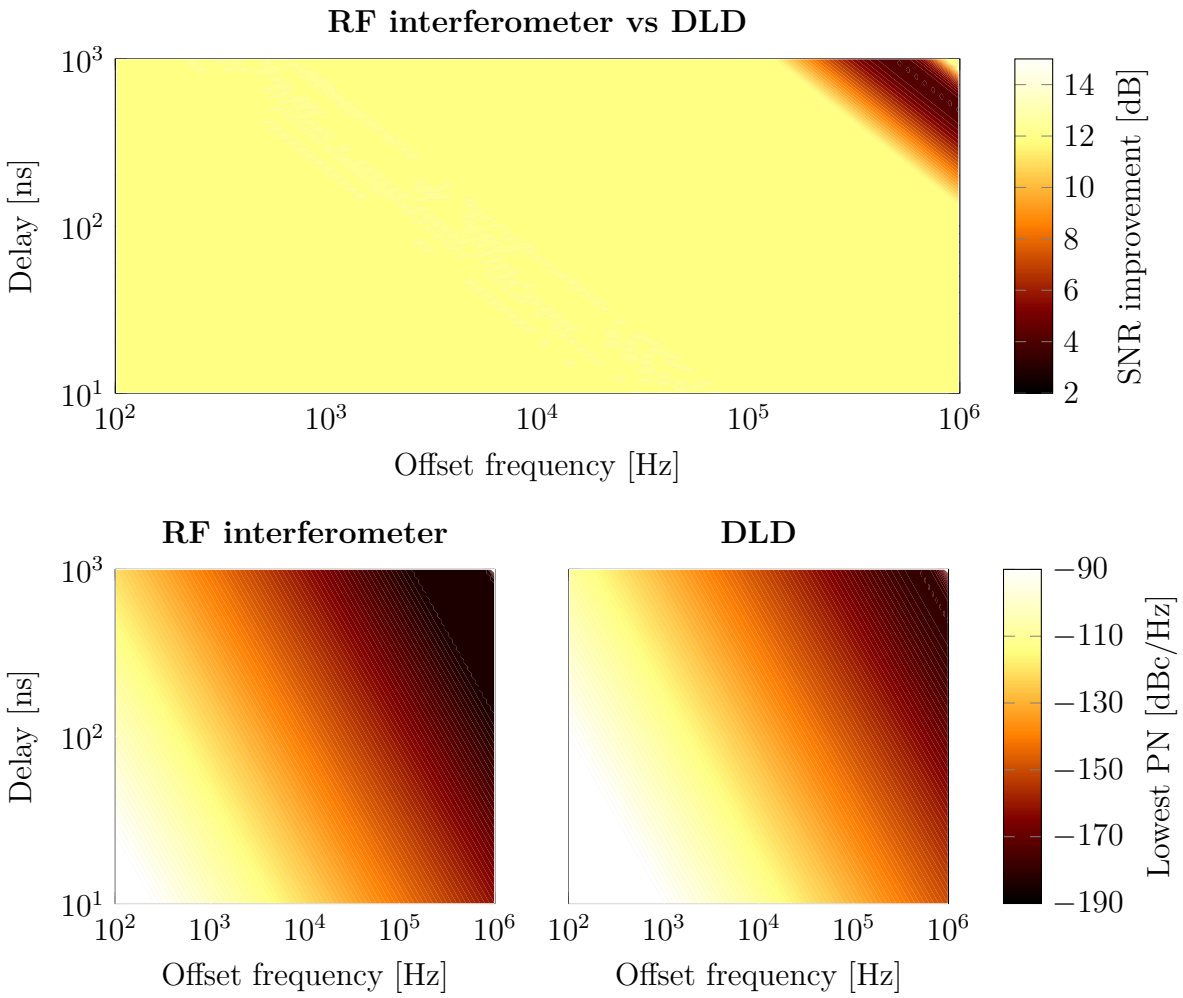


Figure 5.1: The improvement in SNR for the RF-interferometer compared to the DLD under the assumptions above, along with the lowest measurable phase noise at different delays and frequency offsets.

and only really poor phase noise could be measured using the DLD at close in offsets.

These issues are less pronounced in the RF-inteferometer, which in addition seems to outperform the DLD in terms of sensitivity at all frequencies for the ideal case assumed. Thanks to the amplification before the mixer, an OP-AMP can be disregard for the RF-inteferometer but can also be included without (meaningful) noise added. In addition to the mitigation of mixer noise already discussed above. The only other extra noise added in the RF-interferometer is the extra noise from the amplifier at the mixer input. Due to the suppression, the noise floor out of the power combiner is at the thermal noise floor and hence the SNR degrades by the amplifiers NF. So in the RF-interferometer, both pre-amplifier and mixer amplifier should be LNAs.

5.4.3.1 Sensitivity of constructed systems

The sensitivity of the improved DLD design and RF-interferometer can be estimated. At a close offset, namely 100 Hz, the mixer noise was a clear limit to the phase noise measurement and hence the sensitivity calculated in Table 5.2. The sensitivity at 100 kHz was also added but since the noise floor at this level could not be measured directly, it was estimated theoretically. At this large offset this should be a valid estimate although it is optimistic. So it is likely the sensitivity here is slightly worse.

The ideal sensitivity was also included from as a reference and one can see that the close in phase noise measurement is much worse than ideal. Although the RF-interferometer is better and can potentially be even more so. However, at a 100 kHz offset the constructed systems are closer to the ideal system. Here the mixer noise is probably at or below the theoretical noise floor and hence the sensitivity much closer to the ideal case.

Table 5.2: Lowest measurable SSB phase noise in different setups, including both the constructed designs and ideal setups.

	Lowest Measurable Phase Noise at Offset:	
Setup:	**100 Hz**	**100 kHz**
Improved DLD Design	-47 dBc/Hz	-143 dBc/Hz
Ideal DLD	-93 dBc/Hz	-153 dBc/Hz
RF-interferometer Design	-71 dBc/Hz	-159 dBc/Hz
Ideal RF-interferometer	-102 dBc/Hz	-162 dBc/Hz

5.4.4 Future Work

Work on this circuit can be continued by further investigation of the RF-interferometer. This thesis has presented some information about this variant and concluded it can improve the SNR. Although the experiment involving it presented flaws and this could be investigated in a continuation of this work. In addition to investigating what sensitivity can be reached experimentally, one could investigate whether increased sensitivity is in fact necessary, although this will depend on the method implemented to actually reduce the phase noise. This is the most direct investigation to conduct, to determine if it is viable at all and if so, to what degree.

Further study of the noise generated by components such as phase shifters and mixers could also be of interest in future study, in particular if improved sensitivity at closer in offsets are desirable.

In the end, should the method prove useful, investigation of the implementation to measure phase noise in an actual system could be investigated, both in radar and communication systems. In radar systems, the sensitivity might be an issue, as high quality oscillators are already used [3]. However, in communication systems

oscillators tend to have worse performance, whereas this system can provide improvement [30]. Therefore, future studies could be directed at PCB design in order to determine if it is commercially viable to implement.

6
Conclusions

The DLD was constructed successfully, providing a functional system. The sensitivity of this system was limited to $-143\,\mathrm{dBc/Hz}$ at $100\,\mathrm{kHz}$ offset, although the sensitivity were worse at close in offsets. The main cause for this reduced sensitivity was unexpectedly large noise generated by the components in the system, in particular the phase shifter but also the mixer, albeit not as severe. Disregarding unwanted noise, the delay line and frequency mixer were identified as the main bottlenecks in the system. The delay due to issues in realizing a device with long time delay and the mixer due to its limited input carrier power. An alternative to mitigate this issue in the mixer were proposed with the RF-interferometer which showed improvement in sensitivity of the system. Mostly investigated through simulation but also with some limited experimental testing. The improved sensitivity comes at some cost in increased complexity but also potentially removing the requirement of an output amplifier. It also mitigates the potential noise in mixer and output amplifier (if used). The immediate natural continuation of this project to investigate it further, particularly in experiments. Finally, should the novel method prove useful, future study could be directed at PCB design of the systems. To find out whether implementing the novel method can result in worthwhile improvements of radar and/or communication systems.

Bibliography

[1] A. W. Doerry, "Radar receiver oscillator phase noise," *Airborne ISR radar analysis and design*, 4 2018.

[2] M. Dudek, I. Nasr, D. Kissinger, R. Weigel, and G. Fischer, "The impact of phase noise parameters on target signal detection in fmcw-radar system simulations for automotive applications," in *Proceedings of 2011 IEEE CIE International Conference on Radar*, vol. 1, 2011, pp. 494–497.

[3] M. Skolnik, *Introduction to Radar Systems*, ser. Electrical engineering series. McGraw Hill, 2001.

[4] D. Owen, "Good practice guide to phase noise measurement." National Physical Laboratory, Measurement Good Practice Guide 68, May 2004.

[5] H. Schulze, "Stochastic models for phase noise," 05 2022.

[6] A. L. Lance, W. D. Seal, and F. Labaar, "Phase noise and AM noise measurements in the frequency domain," in *IN: Infrared and millimeter waves. Volume 11 (A85-47951 23-33). Orlando*, vol. 11, Jan. 1984, pp. 239–289.

[7] "Phase noise measurement solutions," Published in USA, Keysight Technologies, Tech. Rep., Jan 26. 2018, 5990-5729EN.

[8] P. O'Brien, "A comparison of two delay line discriminator implementations for low cost phase noise measurement." Analog Devices, 2010.

[9] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, "Microwave circuit design using linear and nonlinear techniques," 2005.

[10] E. Rubiola and V. Giordano, "Dual carrier suppression interferometer for measurement of phase noise," *Electronics Letters*, vol. 36, pp. 2073 – 2075, 01 2001.

[11] B. Razavi, *Fundamentals of microelectronics / Behzad Razavi.* Hoboken, NJ: Wiley, 2008.

[12] E. Coates, "Amplifiers," accessed April 2022. [Online]. Available: https://learnabout-electronics.org/Downloads/amplifiers-module-01.pdf

[13] B. Schweber, "Understanding the basics of low-noise and power amplifiers in wireless designs," *Electronic Products*, october 2013.

[14] I. Rosu, "Understanding noise figure," accessed April 2022. [Online]. Available: https://www.qsl.net/va3iul/Noise/Understanding%20Noise%20Figure.pdf

[15] "Microwave power dividers and couplers tutorial," Marki Microwave, 215 Vineyard Ct. Morgan Hill, CA 95037, accessed April 2022. [Online]. Available: https://www.markimicrowave.com/assets/appnotes/microwave_power_dividers_and_couplers_primer.pdf

[16] J. B. Calvert, "Analog delay devices," January 2002, accessed April 2022. [Online]. Available: http://mysite.du.edu/~etuttle/electron/elect39.htm

[17] L. Devlin, "The design of integrated switches and phase shifters," accessed May 2022. [Online]. Available: https://www.prfi.com/wp-content/uploads/2016/01/design_of_switch_phaseshifter_MMICs.pdf
[18] I. Rosu, "Phase shifters," accessed April 2022. [Online]. Available: https://www.qsl.net/va3iul/Phase_Shifters/Phase_Shifters.pdf
[19] "How to select a mixer," Mini-Circuits, 2015, accessed Mars 2022. [Online]. Available: https://www.minicircuits.com/app/AN00-010.pdf
[20] G. Breed, "Understanding mixers from a switching perspective," *High Frequency Electronics*, april 2006.
[21] I. Rosu, "Rf mixers," accessed Mars 2022. [Online]. Available: https://www.qsl.net/va3iul/RF%20Mixers/RF_Mixers.pdf
[22] C. Razzell, "System noise-figure analysis for modern radio receivers," *Microwave Journal*, june 2013.
[23] J. Fiore, *Op Amps and Linear Integrated Circuits: Theory and Application*, ser. Student Material TV Series. Delmar Thomson Learning, 2001, no. v. 1.
[24] *AD9174*, Analog Devices, Inc., 2018, rev. B.
[25] *PXIe-5170*, National Instruments, 2017, pXIe, 4- or 8-Channel, 100 MHz Bandwidth, 14-Bit, Reconfigurable Oscilloscope.
[26] *AD9161/AD9162*, Analog Devices, Inc., 2018, rev. D.
[27] Mini-Circuits, "Additive phase noise in amplifiers," 2021, accessed 19 may 2022.
[28] C. J. Grebenkemper, "Local oscillator phase noise and its effect on receiver performance," 2000.
[29] R. Lu, Y. Yang, A. E. Hassanien, and S. Gong, "Gigahertz low-loss and high power handling acoustic delay lines using thin-film lithium-niobate-on-sapphire," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 7, pp. 3246–3254, 2021.
[30] A. Piemontese, G. Colavolpe, and T. Eriksson, "Phase noise in communication systems: from measures to models," *CoRR*, vol. abs/2104.07264, 2021. [Online]. Available: https://arxiv.org/abs/2104.07264

A

AWR Simulation Setup

Here the setup for the AWR simulations are described. Each setup has an accompanying figure of the AWR environment.

A.1 Initial Design

The source TONE were used to generate the 1.3 GHz carrier signal with a power of -5 dBm as a complex envolope signal. In order to superimpose phase noise to this signal, a subcircuit was created and added after the source. Subcircuits are built using two ports, the first as an input and the second as a output. In this subcicuit the input was first divided into magnitude and phase part using component C2MP. Utilizing a real source SRC_R the text file containing the phase noise could be entered into this circuit and with an add component ADD the phase noise was added to the phase of the input signal. After having added the phase noise to the signals phase, magnitude and phase was recombined using component MP2C (Magnitude and Phase to Complex Envelope).

The behavioral amplifier AMP_B2 was used as amplifier and an attenuator RFATTEN was then added before the power divider SPLITTER. The LO channel to the mixer had an additional attenuator added while the RF channel had the delay and phase shifter. Using the delay RFDELAY resulted in unwanted operations due to it utilizing a digital delay. Instead a subcircuit was created using a circuit schematic. In this circuit two input ports were used similarly to previous case, an attenuator ATTEN was added to account for all attenuation in the delay line, which was known. The delay was instead controlled by adding coaxial cables COAXI2 and tuning their parameters to produce the wanted delay. The phase shifter component was APHSHIFT_VAR which can vary the phase shift between 0 and π using a specified voltage. Following this, the mixer MIXER_B2 was used with the option NFTYP set to Double Sideband Noise Figure and the NF set to 0. The last component added was a low pass filter LPFC set to an order 3 Chebyshev with cutoff 50 MHz. The end of the system was a port and result for simulations could be measured here.

Each component used in the program had its parameters set the same as the components procured for the initial design. The purpose of the system was to verify the functionality of the system and make sure considerations in the theory could be simulated.

A rectangular graph was created using PWR_SPEC as measurement type at the output port. A resolution BW was chosen of 500 000 FFT Bins and the Y-Axis output was PSD (Pwr/Hz). Frequencies desplayed were Non-Negative, truncated. This only accounts for the positive frequencies, and in order to get the single sided power, the PSD was increased 3 dB. The result was subsequently exported to Python for plotting.

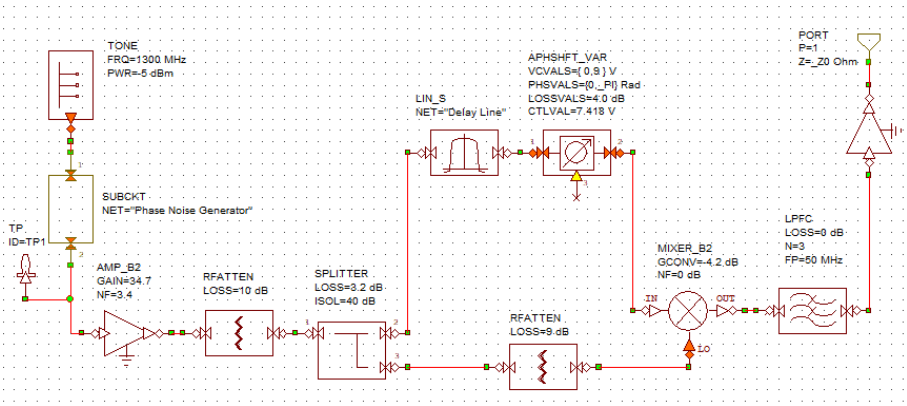


Figure A.1: Setup for the circuit in AWR for the initial design.

A.2 Comparison with Interferometer Variant

For a fair comparison the mixer was modelled without any compression in the conventional method since the new method would circumvent the issue of compression. Two different system schematics were created in AWR whereas the first one was almost the same as the previous system, with only minor changes. The mixer component MIXER_B2 was used but both CL and NF was changed to 6.5 dB, the approximate parameters of the mixer to be used in the final design, assuming no compression. Two attenuators were added and the phase shifter moved from RF channel to LO channel. In the second system the only difference between them was the RF channel. It was changed to the following in the interferometer variant.

First a power divider component SPLITTER was added after the first divider, only this one had no IL, it was a perfect split. Then the same delay subcircuit as laid out in the previous design was used on one channel, while the other channel had an attenuator RFATTEN and phase shifter APHSHIFT_VAR with phase shift φ_1. The attenuation of these two channels was calibrated to exactly the same by setting IL of the attenuator to 6.3 dB. Lastly, the two channels were combined before entering the mixer using a COMBINER component, with no IL. This design has two phase shifters, the second at the LO channel with shift φ_2 and these had to be calibrated for this setup. In order to do so the delay was measured accurately using the software first. While simple in the software this is more challenging in practical applications. in software this was done by creating a rectangular plot and using the RF Budget Analysis measurement C_{GD} with start test point at a Test Point added at just after the input TONE component while the end point was added at Port 1, at the end of the system. This provided the exact time delay of 218.969997 ns and

by using the following calculations, the system was calibrated for an almost perfect setup of both systems. Conversely the following phase is required to get quadrature in the mixer for the conventional method

$$\varphi = (2n+1)\frac{\pi}{2} - 2\pi f \tau_d = \pi(0.1780078)\,. \tag{A.1}$$

While for the interferometer, there where two phases to calibrate for as

$$\varphi_1 = \pi(2n+1) - 2\pi f \tau_d = 2\pi(0.839004)\,, \tag{A.2}$$

$$\varphi_2 = \varphi_1 - \frac{\pi}{2} = 2\pi(0.589004)\,. \tag{A.3}$$

The subsequent result of the simulations where created for both systems using two different noise measurements. The rectangular plot used was the same as in the initial design utilizing PWR_SPEC measurement and the same options. In the first case phase noise using $\sigma = 51$ was added to the input signal and measured through both systems. In the second no noise was added to the signal by disabling the SRC_R, hence the only noise beside the carrier would be the thermal noise floor. The noise floor at the output was then measured and all this data exported to Python.

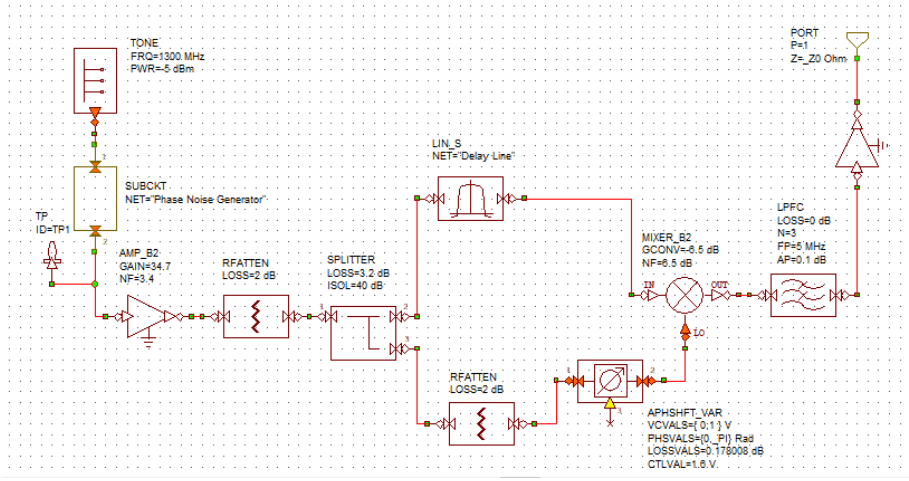


Figure A.2: Setup for the circuit in AWR for the improved design.

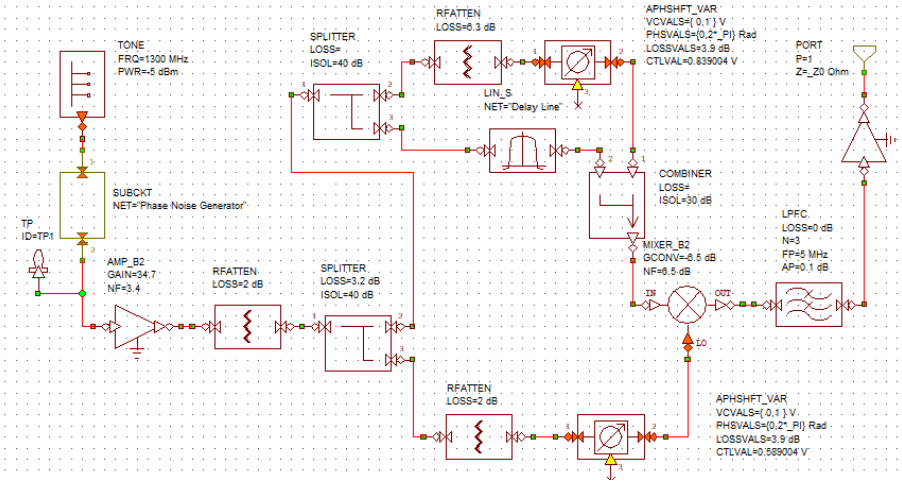


Figure A.3: Setup for the circuit in AWR for the RF Interferometer.

B

Mixer Measurement

The characterisation of the mixers input vs output power can be seen in the following figures. For the mixer used in the initial design; ZEM4300, the CL can be seen in figure B.1. Two measurements of the CL were made corresponding to two different relations between LO and RF frequency. In both cases the LO frequency was set to 1.3 GHz while the RF was set the corresponding amount higher. With a larger difference the CL was larger than the case when the two frequencies were close together. However, in both cases a similar compression characteristic was observed. At around -2 dBm the increase in output power did not correspond linearly to the input any more and the conversion loss subsequently increase.

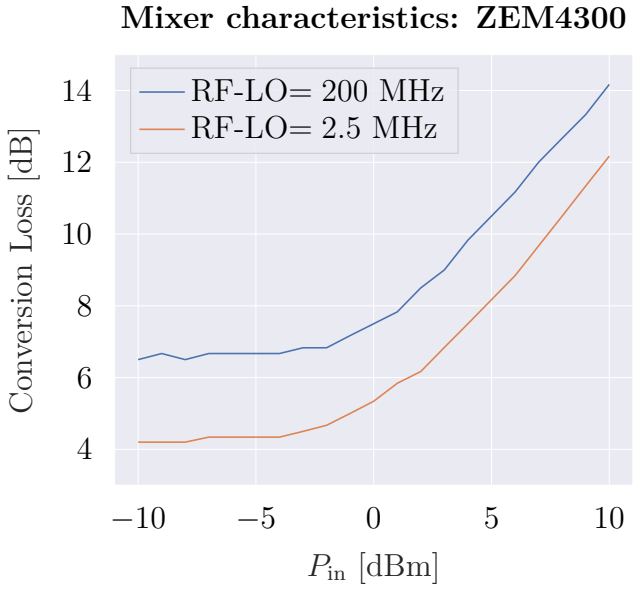


Figure B.1: Conversion loss in mixer depending on RF power for mixer ZEM-4300 at two different relations between the RF and LO.

The mixer used in the final design was ZX05-43H-S+, and its CL can be seen in figure B.2. The measurement were conducted similarly to the previous case but only for a relation where the RF and LO frequencies were close to the same. The conversion loss for this mixer is a little higher in the linear region but it takes until around 11 dBm of RF input power before the CL starts to increase due to compression.

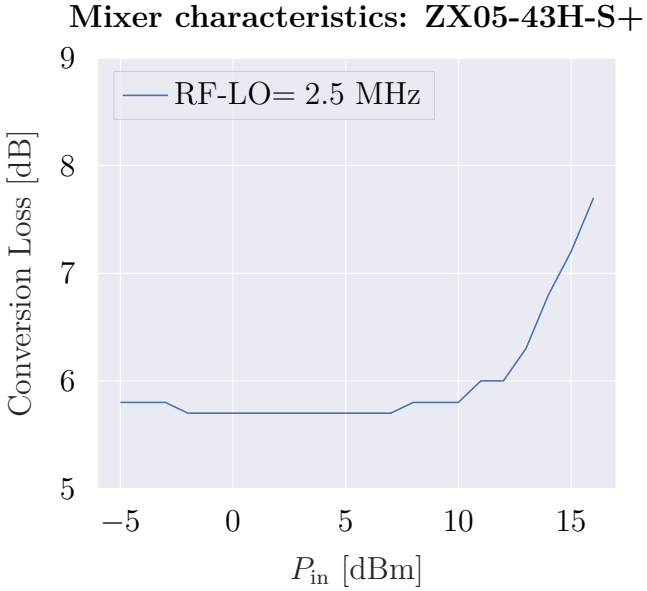


Figure B.2: Conversion loss in mixer depending on RF power for mixer ZX05-43H-S+ with RF at 1.3025 GHz and LO at 1.3 GHz.

C

Creating Noise for Initial Experiment

In the initial experiment the noise used was chosen using the following derivation. By first choosing a desired SNR for phase noise at the output for an experiment, a σ can be calculated (at specific offset 100 kHz) that will provide phase noise at a level such that the specified SNR should be attained. The power of the phase noise at the output for a given SNR will be

$$\mathrm{PN_{meas}} = \mathrm{N_{out}} + \mathrm{DR_o}\,.$$

Where $\mathrm{N_{out}}$ is the PSD of the noise floor. From this measured phase noise, the level of the phase noise required to be added to the system becomes the following by going backwards through the system:

$$\mathrm{P_{needed}} = \mathrm{P_{meas}} - \mathrm{G_o} + \mathcal{H}(\mathrm{f}, \tau_\mathrm{d}) + \mathrm{CL} + \mathrm{IL_{tot}} - \mathrm{G}\,.$$

With the specified power of the phase noise given, the σ required to generate this phase noise on the carrier signal with power P_{in} can be calculated as

$$\sigma = 2\pi f \; 10^{(\frac{P_{needed} - P_{in}}{20})}\,. \tag{C.1}$$

D

Component Noise Measurement

The noise generated by a few components was measured in the project and presented here.

D.1 ADC

The noise generated for the ADC at different reference peak voltages was measured directly.

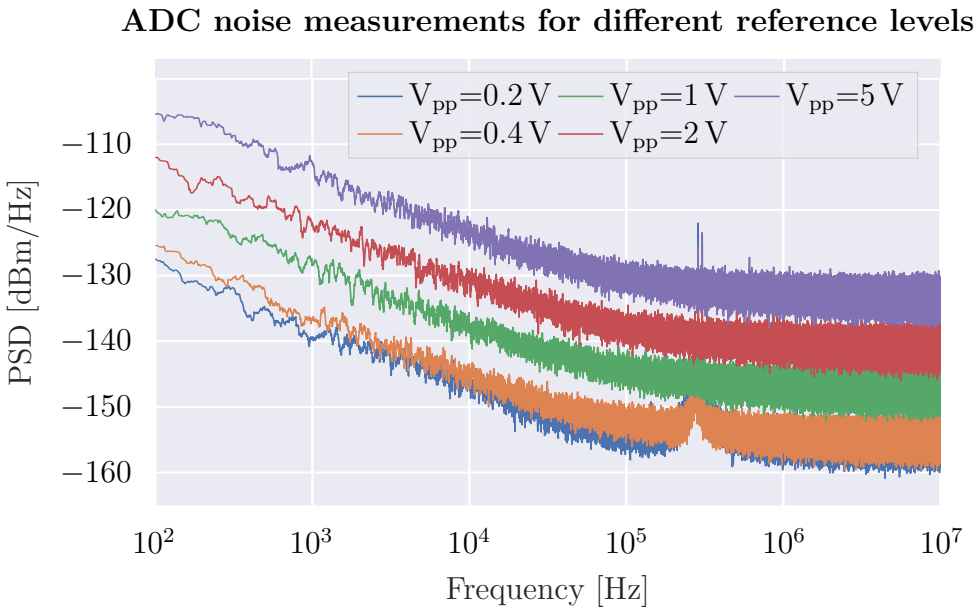


Figure D.1: The PSD for the ADC for different V_{pp} values without any input signal.

D.2 OP-AMP

The noise in the OP-AMP was measured using the ADC with the 200 mV reference with no input signal. The gain was 32 dB which was subtracted from the measured noise, yielding the extra noise added by it. Outside of the bandwidth of the OP-AMP this is incorrect since the gain is no longer 32 dB, hence frequencies beyond 5 MHz are disregarded.

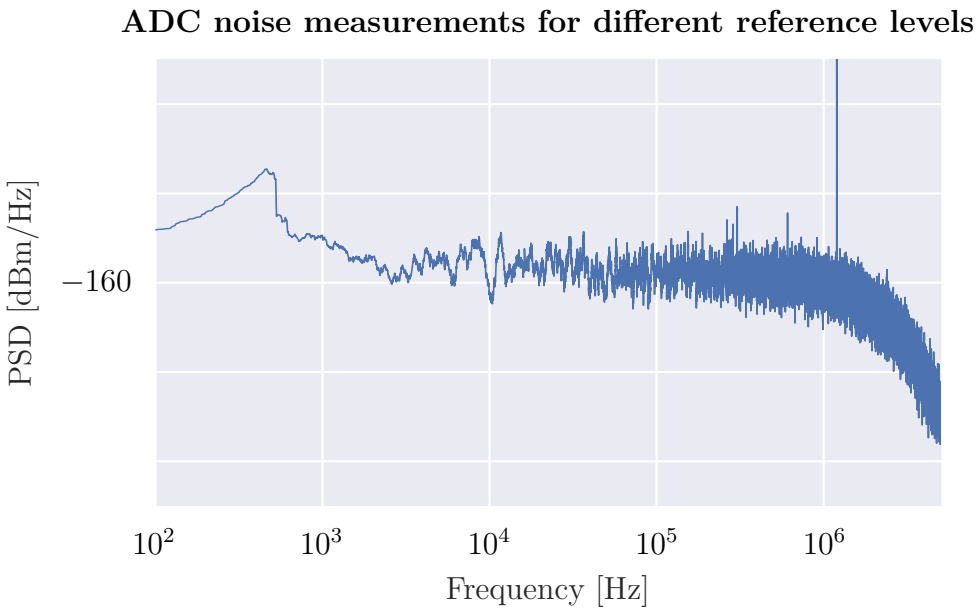


Figure D.2: The PSD for the OP-AMP noise with the gain removed.

E

RF-Interferometer

For derivation of system response, assume the signals at the input of the power combiner is Derivation of carrier suppression given the signals

$$\sin\left(\omega_0(t-\tau_d)+\phi(t-\tau_d)\right),$$
$$(1+\epsilon)\sin\left(\omega_0 t+\phi(t)+\varphi\right),$$

where ω_0 is the angular frequency, φ a phase shift and ϵ the amplitude error. Using that $\varphi = (2n+1)\pi - \omega_0\tau_d + \delta$ and ignoring the loss in the power combiner, the output signal takes the following form:

$$2\sin\left(\omega_0 t+\frac{\phi(t-\tau_d)+\phi(t)+\varphi-\omega_0\tau_d}{2}\right)\sin\left(\frac{\phi(t)-\phi(t-\tau_d)+\delta}{2}\right)+ \\ +\epsilon\sin\left(\omega_0 t+\phi(t)+\varphi\right).$$

Squaring the expression yields

$$\epsilon^2\sin^2\left(\omega_0 t+\phi(t)+\varphi\right)+2\epsilon\sin^2\left(\frac{\phi(t-\tau_d)-\phi(t)-\delta}{2}\right)+ \\ +4\sin\left(\omega_0 t+\frac{\phi(t-\tau_d)+\phi(t)+\varphi-\omega_0\tau_d}{2}\right)\sin^2\left(\frac{\phi(t-\tau_d)-\phi(t)-\delta}{2}\right)- \\ -2\epsilon\sin\left(\frac{\phi(t-\tau_d)-\phi(t)-\delta}{2}\right)\cos(2\omega_0 t+...).$$

Over longer time spans the last term will integrate to zero and thus, the output power can be written as

$$P\propto\epsilon^2+(4+2\sqrt{2}\epsilon)\sin^2\left(\frac{\phi(t-\tau_d)-\phi(t)-\delta}{2}\right).$$

F

Time Data Illustration

A histogram of the phase noise measured in the ADC are shown in Figures F.1 and F.2. The PSD of this noise was calculated and is illustrated in the result. Here an estimated relation between the peak-to-peak voltage and the PSD can be determined. Where a 5 V peak-to-peak voltage correspond to around a phase noise PSD of −55 dBm/Hz. From Figures 4.3 and F.2 it can be seen that phase noise at −65 dBm/Hz approximately correspond to a 1.5 V peak-to-peak which is equivalent to phase noise at −55 dBm/Hz correspond to a 4.7 V peak-to-peak.

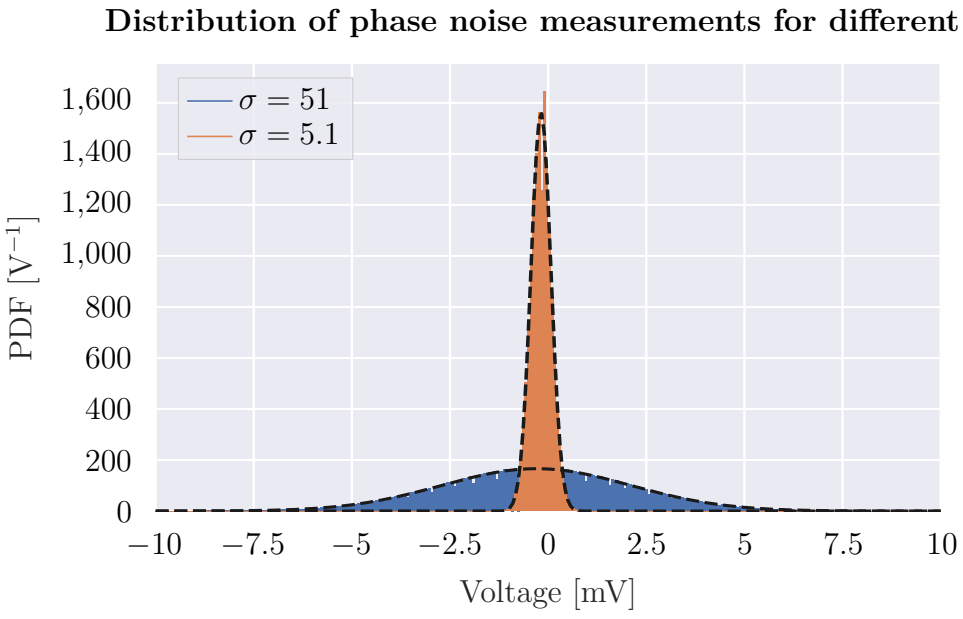


Figure F.1: The distribution of measured voltages for initial design system. The blue correspond to a Wiener process with $\sigma = 51$, the corresponding dashed black line is a Gaussian distribution with mean −0.3 mV and standard deviation 2.4 mV. The orange correspond to a Wiener process with $\sigma = 5.1$, the corresponding dashed black line is a Gaussian distribution with mean −0.2 mV and standard deviation 0.26 mV.

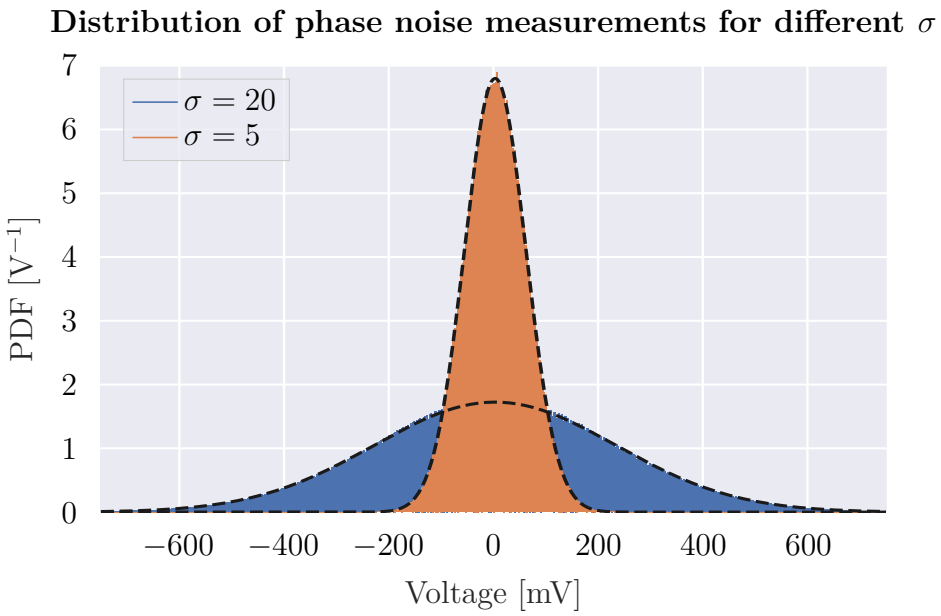


Figure F.2: The distribution of measured voltages for initial design system. The blue correspond to a Wiener process with $\sigma = 20$, the corresponding dashed black line is a Gaussian distribution with mean 3 mV and standard deviation 230 mV. The orange correspond to a Wiener process with $\sigma = 5$, the corresponding dashed black line is a Gaussian distribution with mean 3.4 mV and standard deviation 59 mV.

DEPARTMENT OF SOME SUBJECT OR TECHNOLOGY
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden
www.chalmers.se

CHALMERS
UNIVERSITY OF TECHNOLOGY