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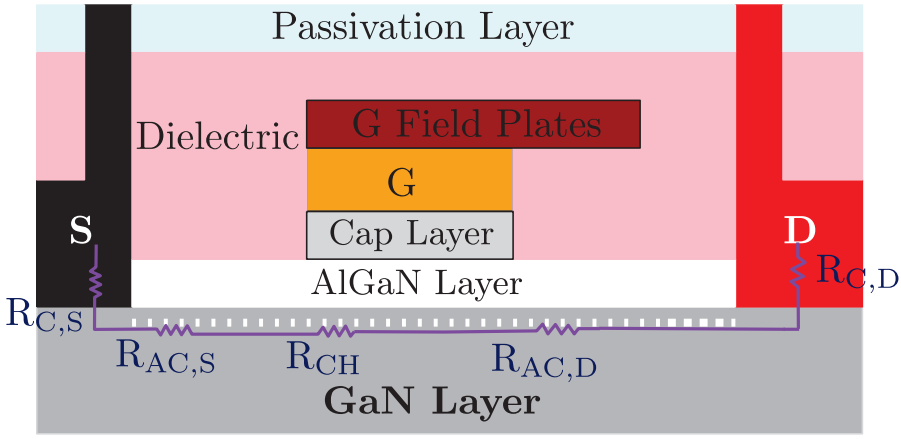

Determining Dynamic On-resistance of Lateral Gallium Nitride Devices in Motor Driver Applications

Master's thesis in Sustainable Electric Engineering and Electromobility (MPEPO)

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Gothenburg, Sweden 2025
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Cover: Illustration of Lateral Gallium Nitride Device's Structure and Inner Resistance.

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This thesis is a collaboration between two students from different universities: Mikael from Linköping University and Daihui from Chalmers University of Technology. The thesis is published at both universities but has different covers. Only the examiner and supervisor from Chalmers University of Technology are mentioned on this cover.

Abstract

This report investigates different challenges of determining the effects of dynamic on-resistance (D-$R_{ds(on)}$) in lateral Gallium Nitride High Electron Mobility Transistors (GaN-HEMT) operated in automotive traction inverter conditions. A literature review identifies the operational parameters of the devices that affect D-$R_{ds(on)}$ most adversely. The accuracy, complexity, and testable operational parameters of different measurement methods, i.e., double pulse test, multi-pulse test, and steady-state continuous switching, are investigated. The report also examines different on-state voltage measurement circuits (OVMCs) needed to measure D-$R_{ds(on)}$ accurately. The report concludes that operational parameters, such as drain-to-source voltage, drain current, switching frequency, duty cycle, and turn-on gate resistance, significantly influence D-$R_{ds(on)}$. Moreover, these parameters exhibit a synergistic relationship. In contrast, the impact of junction temperature on D-$R_{ds(on)}$ is ambiguous and varies between studies. Additionally, D-$R_{ds(on)}$ varies with production batches and device structures. Further, a double pulse test is a suitable first method to determine whether a device suffers from D-$R_{ds(on)}$. If accuracy is prioritized, the multi-pulse test serves as an alternative method. Finally, two different OVMCs are concluded to have sufficient performance for determining D-$R_{ds(on)}$.

Keywords: GaN-HEMT; Dynamic on-state resistance; Traction inverter

Acknowledgments

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Finally, we would like to thank the friends we made during this thesis journey, including Dongying, Ye, Salman, Kaixin, Vishal, and many others, for all the fun and laughter.

Mikael Josefsson and Daihui Zhu

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Linköping, December 2024
Mikael Josefsson

First and foremost, I would like to express my deepest gratitude to Mikael. He has been a reliable thesis partner and a great friend throughout this journey. His profound expertise, particularly in electronics design, has been a constant source of inspiration, and I am deeply grateful for his invaluable contributions.

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Göteborg, December 2024
Daihui Zhu

Contents

1 Introduction

This thesis project investigates challenges related to determining dynamic on-resistance of lateral GaN-on-Si HEMTs in motor driver applications. The thesis was conducted at Volvo Cars in Gothenburg, Sweden. This chapter presents the project's motivation, research aim, research questions, and delimitations.

1.1 Motivation

Electric vehicles (EVs) are undergoing rapid development to mitigate the transport industry's effect on climate change [1]. In battery EVs, a traction inverter takes a DC input from the battery and produces an AC output to drive the motor [2]. Minimizing the losses of the power conversion and physical size of the inverter is important to maximize the range of the vehicle.

The power semiconductor device is the key component in traction inverters because it dictates efficiency and reliability. So far, the most popular device for traction inverters in automotive applications has been the Silicon Insulated Gate Bipolar Transistor (Si-IGBT). However, Si-based devices have started to reach their theoretical limits in terms of switching and conduction losses, due to the intrinsic material properties of Si. Hence, new power semiconductor devices based on other materials are needed to keep on reducing losses in existing and popular inverter topologies [1].

Wide-bandgap (WBG) devices are emerging as a solution. In general, devices built with WBG materials can operate at higher temperatures, have lower conduction and switching losses, and have a higher breakdown voltage [3]. Commercial power devices include Silicon Carbide (SiC) and Gallium Nitride on Silicon High Electron Mobility Transistors (GaN-on-Si HEMTs).

SiC devices have become increasingly popular in automotive traction inverters due to their extremely high power capability, low losses, and overall robustness [4]. GaN devices are predicted to compete with SiC devices in the future in automotive inverter applications [5]. SiC devices have a higher power capability, while GaN devices, in theory, have lower conduction and switching losses [3], and are expected to become cheap, possibly cheaper than Si devices [6].

However, GaN-on-Si HEMTs are known to suffer from an effect known as dynamic on-resistance (D-$R_{ds(on)}$). Due to the unique device structure, electrons are trapped within the structure when exposed to a high off-state drain-to-source voltage and during the switching transients. The trapped electrons adversely affect conduction performance and increase conduction losses. For automotive traction inverter designers considering GaN devices, it is essential to understand and measure D-$R_{ds(on)}$ under varying conditions to account for the increased losses.

1.2 Research Aim

D-$R_{ds(on)}$ is dependent on operating parameters such as the drain-to-source voltage (V_{ds}), drain current (I_d), switching frequency (f_{sw}), etc. To properly determine D-$R_{ds(on)}$ it is important to characterize D-$R_{ds(on)}$ in conditions similar to the real application. This thesis aims to investigate which operational parameters are the most important to consider and which method is the most suitable for determining D-$R_{ds(on)}$ of GaN devices operating in EV traction conditions. Furthermore, to acquire a high-resolution measurement of D-$R_{ds(on)}$, an on-state voltage measurement circuit (OVMC) is required due to the large difference in V_{ds} between the devices on- and off-states. Different types of OVMCs will be investigated and the most suitable circuit will be selected for implementation.

1.3 Research Questions

With operating conditions typical of EV traction inverters in mind, i.e., high current and high voltage, the following research questions will be answered:

1. How do operational parameters (V_{ds}, I_d, f_{sw}, etc.) affect D-$R_{ds(on)}$?

   Through a literature review, the effect of operational parameters on D-$R_{ds(on)}$ is studied to identify which parameters are the most important to investigate in vehicle applications.

2. What measurement methodology should be used to determine D-$R_{ds(on)}$?

   On-resistance of a device is measured in a half-bridge setup. The measurement methodology, i.e., the number of times the device under test is

switched and the load used in the half-bridge, affects how adverse the effect of D-$R_{ds(on)}$ is. Through a literature review, various methodologies are compared to identify the one most capable of replicating the effects of D-$R_{ds(on)}$ observed in the electric motor drive applications. PLECS simulations are then used to assess the ease of implementation.

3. What on-state voltage measurement circuit should be used to determine D-$R_{ds(on)}$?

   GaN devices used in high-voltage applications have a large difference in on-state and off-state drain-to-source voltage. An on-state voltage measurement circuit is needed to acquire a high-resolution measurement of the on-state voltage, which is necessary for determining D-$R_{ds(on)}$. The performance of different OVMCs is compared through simulation in LTSpice. The most promising circuit is realized and tested.

1.4 Delimitations

This thesis was conducted at Volvo Cars, Inverter Electronics Design team. The work was conducted by two students for 20 weeks. The devices considered in this thesis were chosen by Volvo Cars and can be seen in Table 1.1. Due to the time restriction of the thesis work, the GS66516T was prioritized by Volvo Cars and was the sole device used for evaluating measurement methodologies. In the selection and design of the on-state voltage measurement circuits, all devices were considered. To determine D-$R_{ds(on)}$ of a GaN device, measurements of its drain-to-source voltage and drain current are required. Drain-to-source voltage measurements were concluded to be the most challenging and, therefore, were prioritized in this project. Some results on current measurements were reached and is given in Appendix C as extra material.

Table 1.1: *List of devices used in tests. Data not available in the datasheet are marked as N/A. $V_{ds(on)}$ is calculated by multiplying $I_{d,cont}$ with $R_{ds(on)}$.*

Device	BV_{DSS}	$R_{ds(on)}$	$I_{d,cont}$	$V_{ds(on),max}$	t_r	t_f
GS66516T [7]	650 V	25 mΩ	60 A	1.5 V	12.4 ns	22 ns
V08TC065S1X11 [8]	650 V	8 mΩ	180 A	1.44 V	N/A	N/A
IGT60R042D1 [9]	600 V	42 mΩ	23 A	0.97 V	8 ns	11 ns
GPI65060DFC [10]	650 V	30 mΩ	60 A	1.8 V	17 ns	17 ns
GPIXV30DFN [11]	1200 V	70 mΩ	30 A	2.1 V	20 ns	40 ns

2

Theory

This chapter is divided into three sections. Section 2.1 covers the fundamentals of the GaN-on-Si devices' structure, the electrical properties, the origins of D-$R_{ds(on)}$, and how to determine D-$R_{ds(on)}$. Section 2.2 covers the theory used in testing the semiconductor device, including the principle of the half-bridge circuit and the basics of the test setups and methodology. Section 2.3 covers the theory of on-state voltage measurement circuits (OVMC). Different OVMCs are presented and design considerations are explained.

2.1 The Lateral GaN-on-Si Device

The dynamic on-resistance (D-$R_{ds(on)}$) is intricately tied to the device's structure and operational principles. To understand the origin of the effect, the structure of the lateral GaN-on-Si device is first introduced in Section 2.1.1, followed by an examination of its electrical characteristics in Section 2.1.2. Then, the root causes of D-$R_{ds(on)}$ are investigated in Section 2.1.3. Lastly, the measurement principles are explained in Section 2.1.4.

2.1.1 Device Structure

This section begins by discussing the structure of a general lateral GaN-on-Si device, which is normally on. It then explains how the transformation to a normally-off device is achieved.

General Structure

Power semiconductor devices constructed of, e.g., silicon, are commonly vertical devices. This means that the current direction through the substrate of the de-

vice is vertical. However, as the title suggests, the GaN-on-Si device has a lateral current direction. The GaN-on-Si device is typically constructed as depicted in Figure 2.1 [12–15]. This figure illustrates the GaN-on-Si device's general structure and does not represent a specific GaN-on-Si device [16].

Vertical devices composed of only GaN have proven difficult to produce and are still in research. Growing GaN on other substrates and making a lateral device has been more successful. A channel is spontaneously created by a polarization effect when combining layers of AlGaN and GaN crystals, see Figure 2.1. The channel is situated at the junction of these two layers and is highly conductive. The channel is typically referred to as a 2-Dimensional Electron Gas (2DEG) channel due to the confinement of electrons to a planar region. The spontaneous formation of the channel indicates that the device is normally-on. Transistors utilizing this polarization effect to make a highly conductive channel are usually referred to as a High Electron Mobility Transistors (HEMT).

Lateral GaN devices can be grown on many different substrates, e.g., Si, SiC, sapphire [13] and diamond [17]. At the moment, the Si substrate is preferred for power GaN devices due to its affordability and scalability [13].

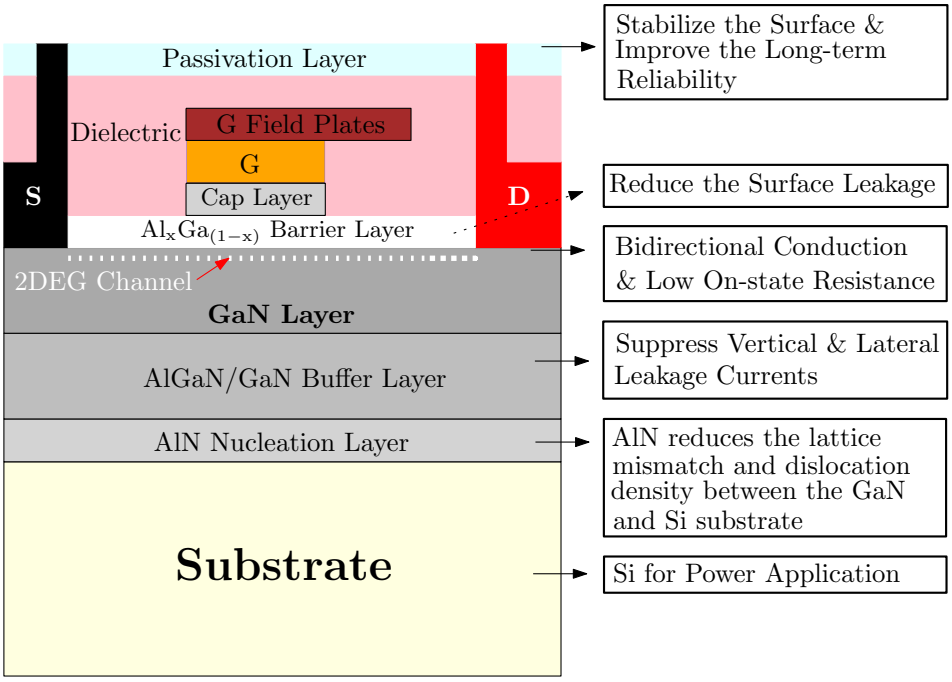

Figure 2.1: *The summarized general structure and functions of a typical lateral GaN-on-Si device. The structure is general and does not represent a specific type of GaN-on-Si device.*

After the substrate, an AlN nucleation layer is typically used as an initiating layer for GaN growth [13], due to a large lattice (crystal structure) mismatch and a strong difference in thermal expansion coefficient between GaN and Si. Then, the buffer layer, or stress relief layer, plays a pivotal role in suppressing vertical and lateral leakage currents, enhancing device reliability and performance [18].

The GaN layer is grown upon the buffer layer. The AlGaN top barrier layer [19] lies upon the GaN layer, forming the 2DEG channel in the junction. At the same time, the AlGaN barrier layer mitigates the leakage in the surface areas [15]. Then a cap layer, typically made of GaN or SiN [13], is built on the barrier layer to minimize oxidation of the underlying AlGaN film.

Finally, the passivation layer reduces the leakage at the surface area and at the interface with the barrier, as well as provides protection to the device [13]. This passivation layer increases the reliability of the device.

Table 2.1 summarizes the materials and the functions of each layer of the GaN-on-Si device. As has been discussed, the 2DEG channel is formed spontaneously and the device is therefore normally-on. A normally-on device is also known as a depletion mode (D-Mode) device, meaning a negative gate-to-source voltage is required to deplete the electrons in the 2DEG and turn off the device. This is illustrated in Figure 2.2. However, this characteristic poses safety and controllability concerns in power electronic applications. Therefore, the transformation into a normally-off configuration is essential [15].

Table 2.1: *Summary of different layers in GaN-on-Si devices for power applications, including their materials and main functions.*

Layers	**Materials**	**Main Functions**
Substrate	Si for power application	Structural support for the upper layers.
Nucleation Layer	AlN;	Reduce the thermal and lattice mismatch.
Buffer Layer	Superlattice: AlN and GaN Step-graded: $Al_{(1-x)}Ga_xN$ [13]	Mitigate the leakage current.
GaN & Top Barrier layer	GaN; $Al_xGaN_{(1-x)}$	Form the 2DEG and mitigate surface leakage.
Cap Layer	GaN or SiN	Minimize oxidation of the underlying AlGaN film.
Passivation Layer	SiN; SiO_2	Reduce leakage at the surface and protect the device.

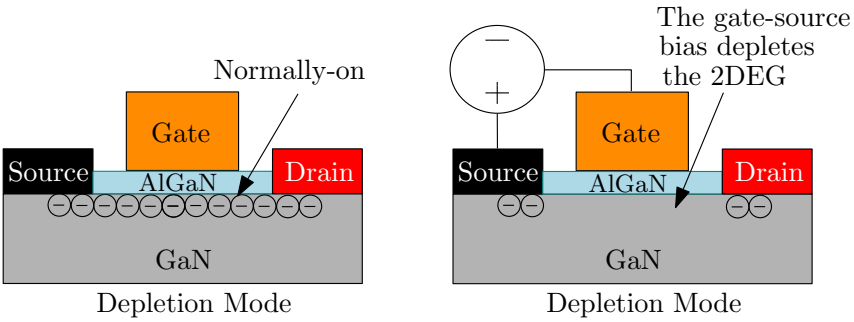

Figure 2.2: *Two operation states of the D-Mode GaN-on-Si devices. The left figure depictcs that the D-Mode devices without the gate-source bias are normally on. The right figure depicts that the D-mode device requires a negative gate-source bias to turn the device off.*

Transformation to a Normally-Off GaN Device

Various methodologies have been devised to achieve the normally-off configuration. The two most common methods are utilizing the cascode structure and transforming the D-Mode device into the enhancement mode (E-Mode) device [18].

The first way is to transform the D-Mode device into the cascode structure, which is depicted in Figure 2.3. For the cascode structure, the gate of the D-Mode GaN HEMT is connected to the source of the E-Mode Si MOSFET. When the MOSFET is activated by a positive gate voltage, the gate voltage of the D-Mode GaN transistor approaches zero volts, causing it to turn on. This allows current to flow through the series connected GaN HEMT and the Si MOSFET. When the gate voltage on the Si MOSFET is removed, a negative voltage is generated between the gate and source of the D-Mode GaN transistor, turning off the GaN device. The high drain voltage is handled by the GaN HEMT, not the Si MOSFET device, which brings better reliability [13]. However, it should be noted that the cascode structure has higher $R_{ds(on)}$ compared to a GaN-on-Si device. This is due to the presence of the Si device [13], which has higher $R_{ds(on)}$ and the reverse recovery phenomenon.

For transforming into the E-Mode device, several methods exist, including but not limited to a gate recessed metal–insulator–semiconductor (MIS-HEMT) with partial or complete AlGaN barrier removal [13], the use of a p-GaN-gated HEMT, and fluorine implantation under the gate [20].

The commercial E-Mode GaNs nowadays commonly adopt the structure of the p-GaN-gated HEMT [13]. Notable examples of such layout are the hybrid-drain gate injection transistor (HD-GIT) [Figure 2.4, left] and the Schottky p-GaN-gated HEMT (SP-HEMT) [Figure 2.4, right]. P-GaN is typically the Magnesium (Mg)

doped GaN during the epitaxy process [21]. The Mg doping provides holes to the GaN, which act as the primary charge carriers and make the GaN material exhibit p-type conductivity. In this way, the depletion region is formed, which blocks the electron flow in the 2DEG. This depletion area requires a positive V_{gs} higher than the threshold voltage ($V_{gs(th)}$) to reduce the depletion region and reform the 2DEG channel.

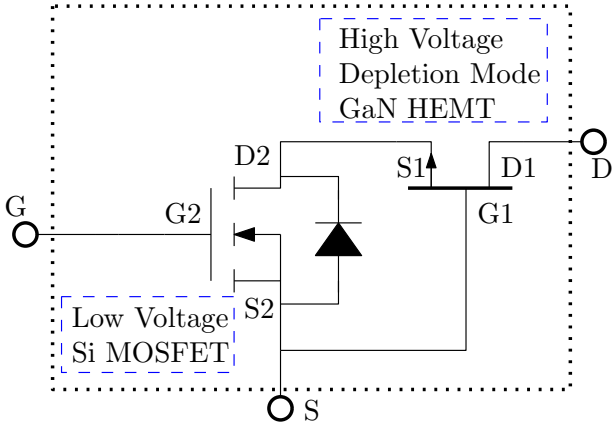

Figure 2.3: *A general cascode configuration to achieve the normally-off operation.*

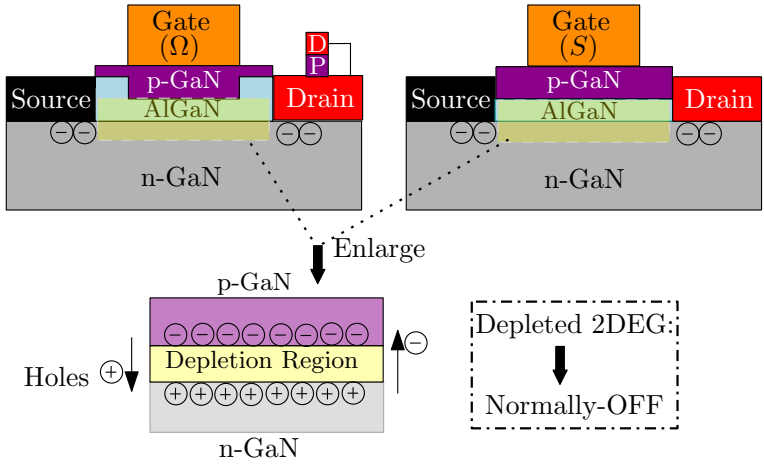

Figure 2.4: *The principle of the p-GaN-gated E-Mode GaN HEMT. The left device represents the general layout of the HD-GIT device while the right represents the general structure of the SP-HEMT device. Their 2DEGs under the p-GaN regions are depleted, making them normally-off. The structures are general and do not represent certain types of GaN-on-Si devices*

The distinctions between the HD-GIT and SP-HEMT are mainly located at the gate and drain regions. In HD-GIT, the gate metal forms an ohmic contact to p-GaN, while in SP-HEMT, they form a Schottky contact. And the AlGaN layer in the HD-GIT is usually recessed, which enables closer proximity of p-GaN to the 2DEG. Moreover, the HD-GIT incorporates a p-GaN region connected to the drain, facilitating the injection of holes into the channel and the buffer layer to mitigate electron trapping [16].

2.1.2 Electrical Modeling and Characteristics

In this section, the basic electrical characteristics of the lateral GaN-on-Si devices are introduced, including the electrical modeling, device ratings, reverse conduction capability and the on-state resistance.

Electrical Modeling

The electrical modeling of the GaN-on-Si device is shown in Figure 2.5 [15]. In this model, C_{ds}, C_{gs}, and C_{gd} represent the node capacitances between the drain-source, gate-source, and gate-drain areas, respectively. And the R_s, R_d, R_g, and $R_{ds(on)}$ represent the source, drain, gate and on-state resistance, respectively. The drain current I_d can be modeled as a voltage controlled current source, in which I_d is a function of both the V_{gs} and V_{ds} [15].

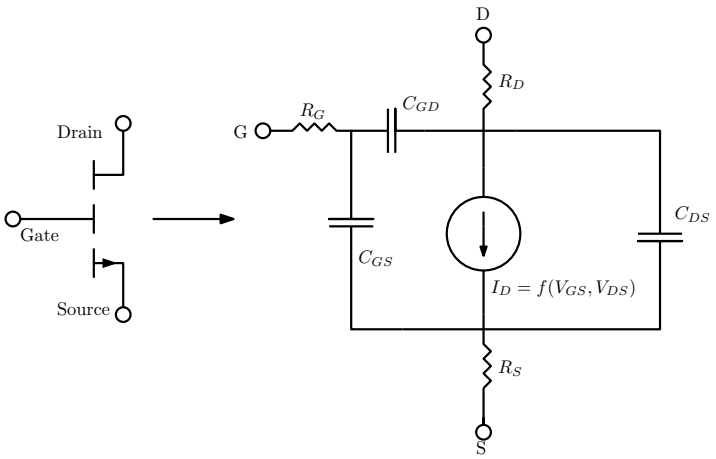

Figure 2.5: *The GaN-on-Si device's electrical model. This model does not includes D-$R_{ds(on)}$.*

The input capacitance C_{iss} and output capacitance C_{oss} are defined the same way as the MOSFET, shown in Equation (2.1).

$$C_{iss} = C_{gs} + C_{gd} \qquad C_{oss} = C_{ds} + C_{gd} \tag{2.1}$$

The capacitances of the GaN-on-Si device are intrinsic and decided by the internal layout and design. Figure 2.6 illustrates the capacitance of a GaN-on-Si device. C_{gs} and C_{gd} are both formed by two capacitors. The capacitors C_{gs1} and C_{gd1} represent the metal-to-metal capacitances, which are constant. The capacitors C_{gs2} and C_{gd2} are voltage-dependent capacitors associated with the 2DEG. The increased V_{gs} enhances the density of the 2DEG, leading to the increase in C_{gs2} and C_{gd2} [22].

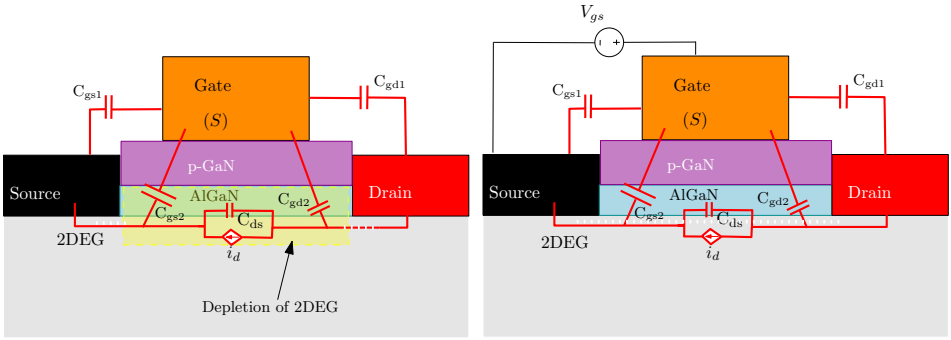

Figure 2.6: *Origins of the GaN's internal capacitors. The structures are general and do not represent certain types of GaN-on-Si devices*

The breakdown voltage and threshold voltage are two other important parameters of the GaN-on-Si devices. The threshold voltage ($V_{gs(th)}$) is the gate voltage, at which the device begins to conduct current between the drain and the source. As has been discussed in Section 2.1.1, the $V_{gs(th)}$ is the voltage to remove the depletion zone in the 2DEG, so that the 2DEG can be reformed and the current can begin to flow through this channel. The term breakdown voltage is often abbreviated as BV_{DSS} [23]. This abbreviation stands for breakdown voltage, drain-source, with the source terminal shorted to the gate. When the critical electric field of any material within a semiconductor transistor is exceeded, the transistor will break down and conduct a significant amount of current I_{DSS}, which may result in device destruction [15].

Turn-on Process

The V_{ds}, I_d and V_{gs} of a typical GaN device during the turn-on process are shown in Figure 2.7.

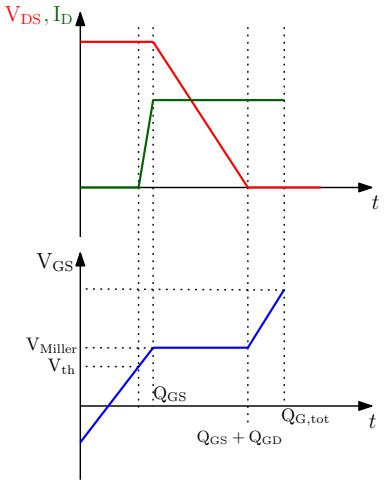

Figure 2.7: *Simplified voltage, current and gate charge characteristics for a typical transistor's turn-on process. The upper plot illustrates the drain source voltage and drain current during the turn-on process while the lower one depicts the gate source voltage during the turn on process. The V_{gs} is negative at the beginning of the turn-on process to ensure the devices' safety by preventing unintended turn-on due to the noise and parasitics.*

It can be noticed that there exists a V-I overlap during this process. This V-I overlap causes turn-on losses.

On-state Resistance

The on-state resistance of a GaN-on-Si device is the sum of all resistive components of the device, which is illustrated in Figure 2.8.

The total on-state resistance $R_{ds(on)}$ is the sum of several resistive components:

- The channel resistance in the gate region (R_{CH})
- The access region resistance (R_{AC}) between the gate and source/drain ($R_{AC,S}$ and $R_{AC,D}$)
- The source/drain contact resistance ($R_{C,S}$ and $R_{C,D}$)

All of the resistive components are affected by temperature. And R_{AC} and R_{CH} are also affected by the operation parameters, which will be covered in Section 2.1 [15].

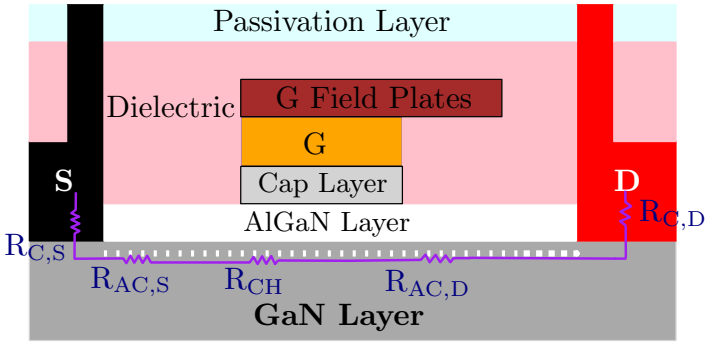

Figure 2.8: *Illustration of the on-state resistance in a GaN-on-Si device. The structure is general and does not represent a certain type of GaN-on-Si device.*

Reverse Conduction

A MOSFET's body diode enables reverse conduction through the p-n junction of the body and drift regions. However, the GaN HEMT lacks a body region and doping in the drift region, resulting in the absence of a body diode [24]. GaN-on-Si device channel inherently supports reverse conduction, and displays varying characteristics based on the applied gate voltage.

This inherent reverse conduction capability is also referred to as the self-commutated reverse conduction (SCRC) or diode-like behavior. This mechanism is primarily attributed to the symmetry of the device: the channel turns on when the gate-source voltage V_{GS} exceeds the threshold V_{th}, and it similarly turns on when the gate-drain voltage V_{GD} exceeds V_{th} [25], which is illustrated in Figure 2.9.

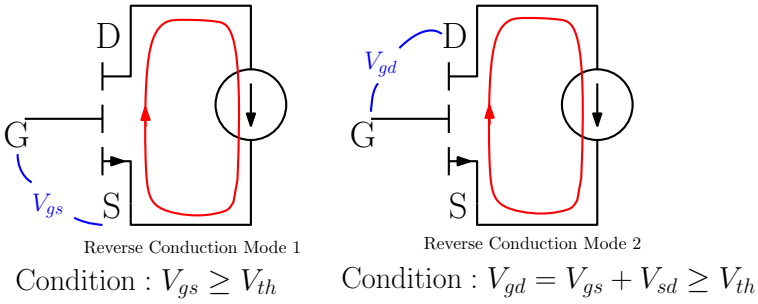

Figure 2.9: *Two conditions to turn on the GaN-on-Si device's channel in the reverse conduction. The device is on when either V_{gs} or V_{gd} is higher than V_{th}.*

The I/V curve of the D-Mode GaN-on-Si HEMT reverse conduction is depicted in Figure 2.10, which is from GaN System's application note [26]. Also, a com-

parison of GaN-on-Si and Si MOSFET's conduction modes is summarized in Table 2.2.

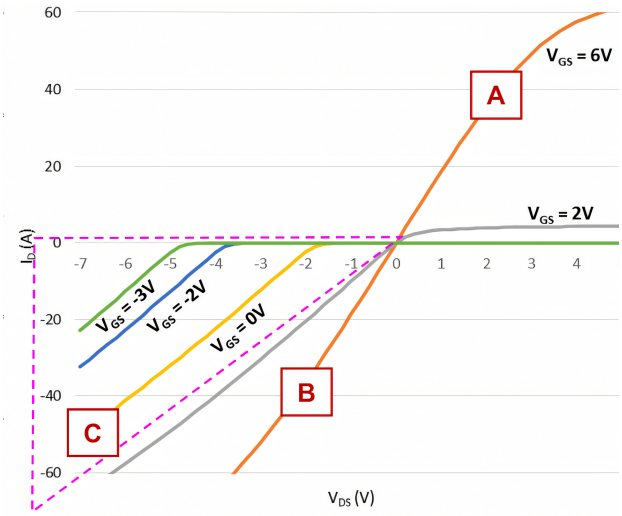

Figure 2.10: *Normally-off GaN HEMT's reverse conduction I/V curve from GaN System's application note [26]*

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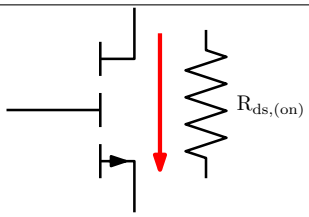
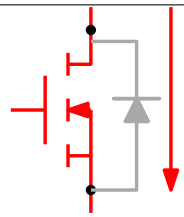
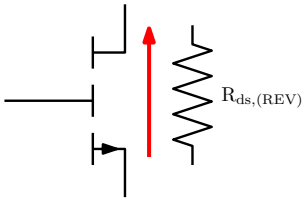
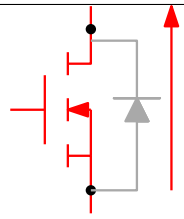
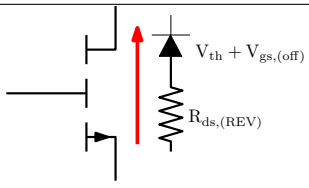
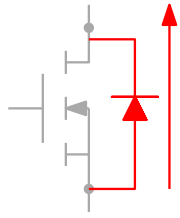
When the device is on ($V_{GS} \geq V_{th}$), the reverse conduction characteristics of a GaN-on-Si HEMT is similar to that of a Si MOSFET, with the I-V curve symmetrical about the origin. And it exhibits a channel resistance $R_{ds(REV)}$, nearly equivalent to forward conduction resistance $R_{ds(on)}$.

When the device is off ($V_{GS} < V_{th}$), the reverse characteristics of a GaN-on-Si device differ from that of a Si MOSFET device, as the GaN-on-Si device has no body diode. In the reverse direction, the device starts to conduct when V_{GD} exceeds the threshold voltage V_{th}. This is the so called diode-like behavior with slightly higher forward voltage drop V_F compared to a Si MOSFET.

Table 2.2: *A summary and comparison of the E-Mode GaN HEMT and Si MOSFET conduction paths under three different operation conditions.*

Type	Gate	GaN E-HEMT	Si MOSFET
A	**ON**	 Forward conduction, the current I_d flows through the 2DEG Channel.	 Forward conduction, the current I_d flows via the MOSFET Channel.
B	**ON**	 Reverse conduction, the current flows through the 2DEG channel.	 Reverse conduction, the current flows through the MOSFET channel.
C	**OFF**	 Reverse conduction, the current flows through the 2DEG channel. The forward voltage drop is calculated as: $V_F = V_{th} + V_{GS,(Off)} + I_d \cdot R_{ds(REV)}$	 Reverse conduction, the current flows through the inherent diode.

2.1.3 Origins of Dynamic On-resistance

D-$R_{ds(on)}$ is an effect specific for lateral GaN-on-Si devices, that adversely affects the devices' conduction performance and junction temperature. This effect is well known, but is often poorly specified by the vendors of the devices [27]. This chapter discusses the physical origins and trapping mechanisms of D-$R_{ds(on)}$.

The unique structure of GaN-on-Si devices is described in Section 2.1.1. There exist impurities and defects in various parts of the GaN-on-Si structure, for example, the buffer layer. These impurities and defects can act as traps for electrons. Trapped electrons reduce the number of free electrons in the 2DEG channel, thereby effectively decreasing its conductivity. This effect is known as D-$R_{ds(on)}$. The electron trapping occurs during two different states of the device: during the off-state [16] and during the turn-on transients, see Figure 2.11.

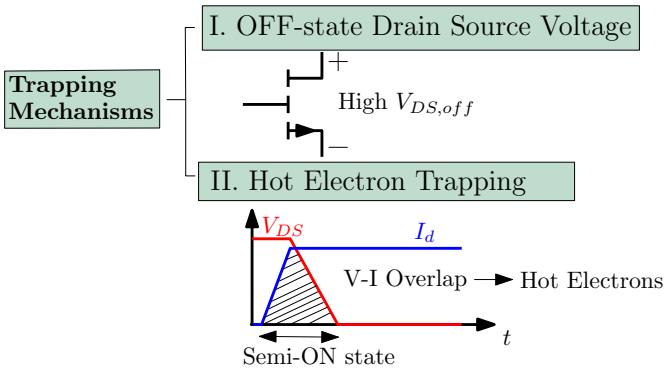
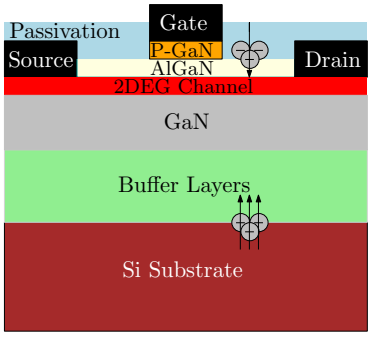


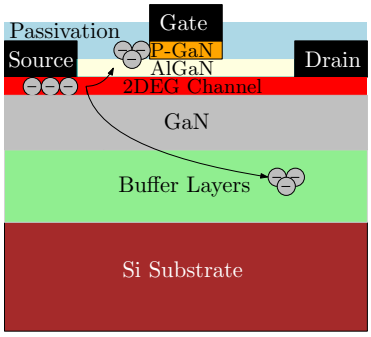
Figure 2.11: *A summary of the electron trapping mechanisms.*

During the off-state, the drain terminal has a high potential, and a large electric field exists between the drain–source and drain–gate areas. During this period, deep-level acceptors within both the buffer and GaN channel layers become ionized or occupied by electrons due to leakage currents passing through the Si substrate, see Figure 2.12a [28, 29]. The deep-level acceptors are specific impurities (e.g., C-doped GaN) or defect sites within semiconductor materials, such as gallium vacancies(V_{Ga}), nitrogen vacancies(V_N), and others [13]. These trapped negative charges act as a 'virtual gate' at the 2DEG channel [13], which reduces the carrier density in the 2DEG, weakening its conductivity. As a result, the observed effect is an increase in the conduction resistance.

The other trapping mechanism, hot-electron trapping, occurs during the turn-on transients, or the semi-on state. In the semi-on state, there is an overlap between the high drain-to-source voltage and a drain current. This overlap can create a large number of high-energy electrons, so-called hot electrons. Due to their high energy, these electrons can penetrate the buffer layers and gate-drain access



(a) Charge trapping due to OFF-state voltage bias



(b) Charge trapping due to hot electrons injection.

Figure 2.12: *Cross section of a simplified GaN-on-Si device illustrating trapped charges within the substrate. Arrows indicate from which direction the charges were attracted [28].*

region, and even the dielectric layer near the gate and drain, see Figure 2.12b [13, 29]. In the same way as for off-state-trapping, the trapped electrons will increase the on-state resistance. It should be noticed that the hot electron-related trapping only exists in hard-switching situations, not soft-switching [29]. In [16], it's shown that hot electron trapping has a larger impact than the high drain-to-source voltage off-state trapping.

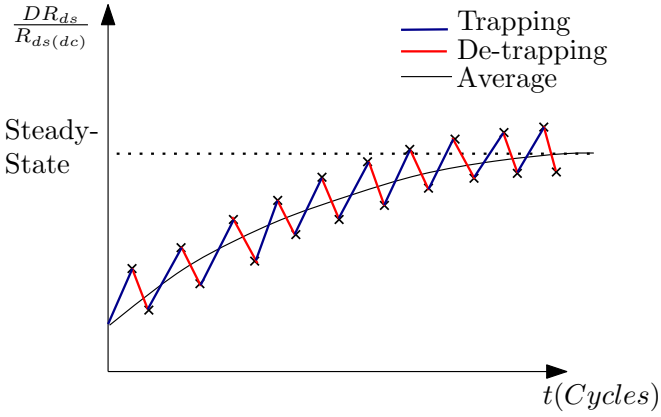


Figure 2.13: *Accumulated effect of trapping and de-trapping during continuous switching. Note that this is an illustrative example, and typically, many more cycles are required to reach steady-state.*

In the device's on-state, trapped electrons are released, and consequently, the on-resistance decreases. There are different time constants related to the detrapping

of electrons stemming from hot-electron trapping and off-state trapping. The hot electron detrapping time constant is in the range of 5 µs to 50 µs, while the off-state detrapping time constant can be much longer, on the order of 1 s to 10 s for GaN-on-Si [29]. Electrons are accumulated during the operation of the device until a balance between trapping and de-trapping, i.e., a steady-state is reached [12], see Figure 2.13. In [29], the time for D-$R_{ds(on)}$ to reach the steady state has been observed on orders from 100 µs to 1 ms to seconds.

2.1.4 Determining Dynamic On-resistance

To determine the impact of dynamic on-resistance (D-$R_{ds(on)}$), the on-state resistance of a device is measured and compared under two conditions: when the effect of D-$R_{ds(on)}$ is present and when it is absent. As described in Section 2.1.3, D-$R_{ds(on)}$ gives an increase of the on-state resistance due to electron trapping during the off-state and the switching transient. In the on-state, trapped charges are released and the on-state resistance decreases. With time the on-state resistance reaches a static value ($R_{ds(on),stat}$), i.e., the on-state resistance without the effect of D-$R_{ds(on)}$, see Figure 2.14. To quantify the impact of D-$R_{ds(on)}$, it is common to normalize the on-state resistance when the effects of D-$R_{ds(on)}$ are present ($R_{ds(on)}(t)$) versus not ($R_{ds(on),stat}$), in other words

$$\text{Impact of D-R}_{ds(on)} = \frac{R_{ds(on)}(t)}{R_{ds(on),stat}}. \tag{2.2}$$

A common setup for determining D-$R_{ds(on)}$ is shown in Figure 2.15. The on-state resistance of the device under test (DUT) is calculated using the on-state drain-to-source voltage ($V_{ds(on)}$) and drain current (I_d) as

$$R_{ds(on)} = \frac{V_{ds(on)}}{I_d}. \tag{2.3}$$

GaN devices with a high blocking voltage usually have a large discrepancy between $V_{ds(on)}$ and $V_{ds(off)}$. Measuring $V_{ds(on)}$ with passive probe results in poor vertical resolution in the oscilloscope. An on-state voltage measurement circuit (OVMC) is commonly is used for measuring $V_{ds(on)}$ to determine D-$R_{ds(on)}$, see Figure 2.15. The purpose and operation of OVMCs are presented in more detail in Section 2.3.

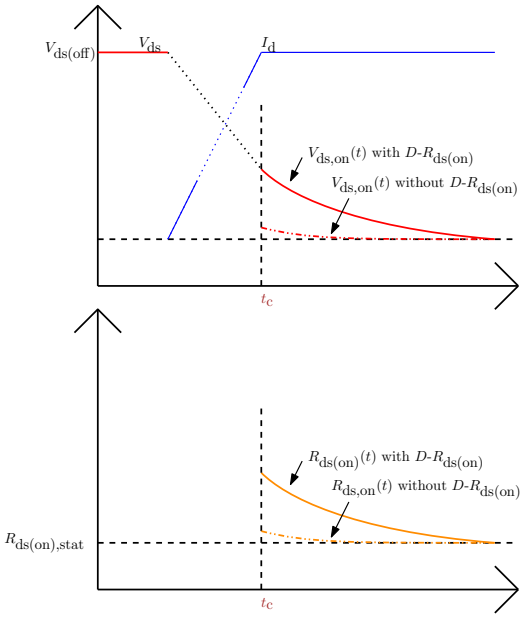


Figure 2.14: *Illustration of the on-state resistance when the effects of D-$R_{ds(on)}$ is present versus absent. The transistor is fully on at time t_c. The time needed for $R_{ds(on)}$ to recover to $R_{ds(on),stat}$ depends on the device structure and operational parameters.*

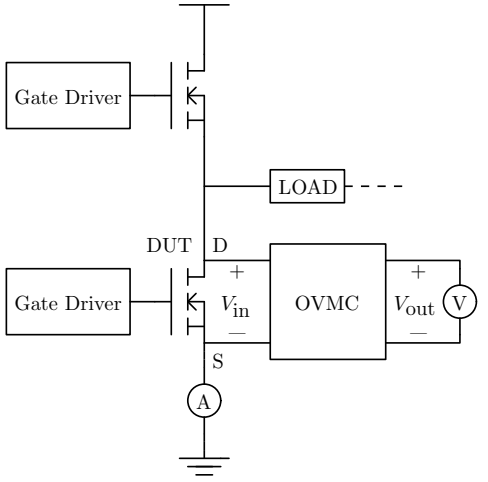


Figure 2.15: *General setup for determining D-$R_{ds(on)}$. V_{in} and V_{out} are the input and output voltages of the OVMC respectively. The voltage and current probes are connected to an oscilloscope.*

2.2 Converter Testing Basics

In this section, the fundamentals of the half-bridge circuit, its extension as a buck converter, and the double pulse test (DPT) are described.

2.2.1 Half-Bridge Circuit

In motor driver applications, the inverter configuration typically involves a two-level, three-phase inverter. This topology is based on the fundamental unit, a bridge leg or a half-bridge. Therefore, the half-bridge configuration is commonly used in motor-driver-related inverter tests. In this section, the half-bridge circuit, including its configuration and working principle, is introduced.

Configuration and Principles

A half-bridge circuit is shown in Figure 2.16. The circuit is composed of the DC power source, two capacitors and two switches. For IGBT devices, The anti-parallel diodes are needed, whereas for GaN-on-Si it is not needed.

The single phase half-bridge inverter converts a DC input into a single-phase AC output by switching two power electronic switches in an alternate manner. This operation creates an AC voltage waveform across the load. The output frequency is determined by the PWM modulation waves' frequency applied to the switches.

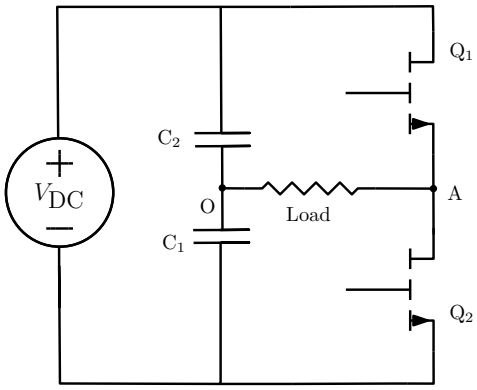


Figure 2.16: *Illustration of the half-bridge circuit topology*

The following accounts for different working schemes of the half-bridge circuit.

- **Scenario 1**: Top switch is ON and bottom switch is OFF
  Q1 is turned on for a duration of $T_0/2$. This results in a voltage of $V_{DC}/2$ appearing across the load, which is the resistance R. Hence, the output current is given as $V_{DC}/2R$. During this period, Q2 remains off.

- **Scenario 2**: Both switches are OFF (Dead time)
  No current flows in the resistive load since there is no voltage applied to the load.

- **Scenario 3**: Top switch is OFF and bottom switch is ON
  The bottom switch Q2 is turned on from $T_0/2$ to T_0 and Q1 is off. A voltage of $-V_{DC}/2$ appears across the load resistance R. The load current can be determined as $-V_{DC}/2R$.

The above schemes, without considering the dead time, is illustrated in the Figure 2.17.

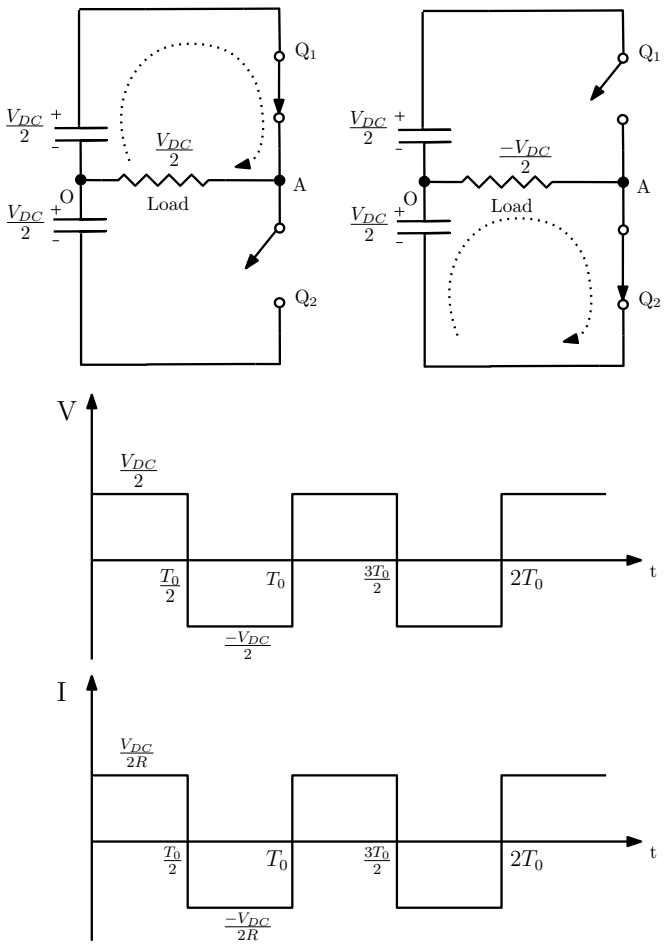


Figure 2.17: *The working principle of a half-bridge circuit with a resistive load*

Principle of Synchronous Buck Converter

The half-bridge switches, as shown in Figure 2.16, are commonly referred to as synchronous switches. To prevent a short circuit, which would occur if both switches were turned on simultaneously, these switches are always operated alternately and synchronously. The synchronous buck converter is designed based on this principle of synchronous switching. An idealized topology of a synchronous buck converter is illustrated in Figure 2.18.

The operation of the converter is controlled by two switches: Q1 (the high-side switch) and Q2 (the low-side switch). This circuit topology supports two modes of operation: continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

- In CCM, the inductor current remains above zero throughout the entire switching cycle, ensuring continuous energy transfer. The operation principle of CCM is discussed below and depicted in the Figure 2.19

- In DCM, the inductor current decreases to zero during part of the switching cycle, typically occurring at light load conditions. The operation of DCM is illustrated in Figure 2.20.

When Q1 is ON ($0 \leq t < t_{on}$), the voltage across the inductor is $V_{DC} - V_{OUT}$, causing the inductor current (I_L) to increase. When Q1 turns off and Q2 turns on ($t_{on} \leq t < t_{on} + t_{off}$), the inductor voltage becomes $-V_{OUT}$, leading to a decrease in the inductor current. To prevent shoot-through (a condition where both switches are ON simultaneously, causing a short circuit), a dead time is introduced between the transitions of the two switches. This dead time is typically much shorter than the switching period, and its effect is often negligible in most calculations.

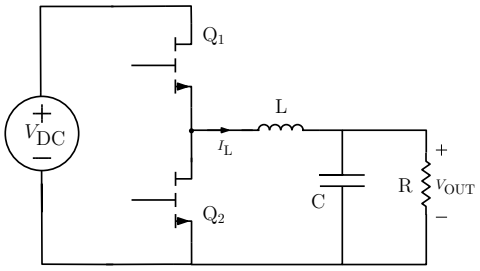


Figure 2.18: *The structure of the synchronous buck converter*

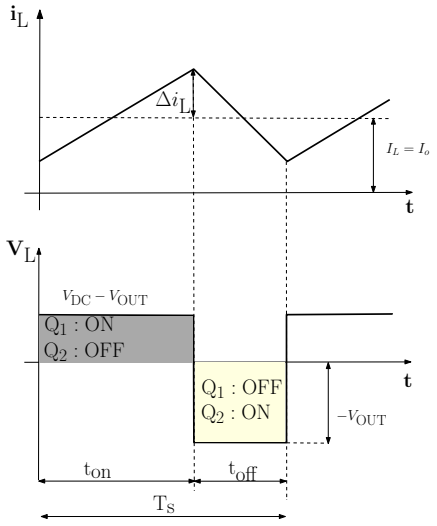


Figure 2.19: *The CCM operation of a synchronous buck converter*

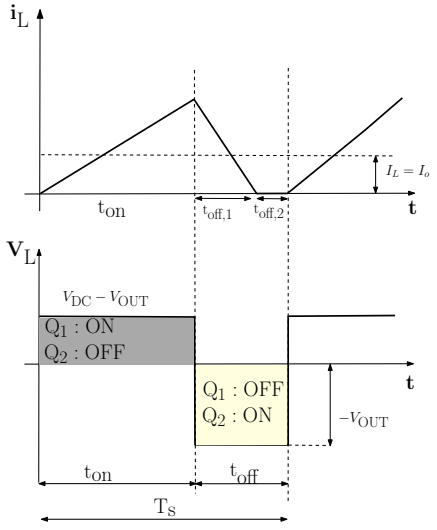


Figure 2.20: *The DCM operation of a synchronous buck converter*

For a buck converter operating in CCM, in the steady-state, the output voltage can be expressed using Equation (2.4). Here, ΔU represents the voltage ripple, and D represents the duty cycle, defined as the fraction of the switching period during which the high-side switch (Q1) is ON (t_{on}). When the inductance value L is high, the voltage ripple ΔU is low. For a given resistive load, the current ripple is therefore also low. Consequently, the capacitor becomes less critical when the inductance value is high.

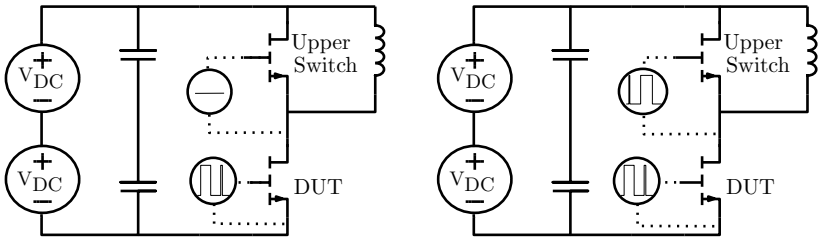
For DCM, the derivation follows a similar process and is thus omitted here for simplicity.

$$\Delta U = \frac{(V_{\mathrm{DC}} - V_{\mathrm{OUT}})DT_s}{L} = \frac{V_{\mathrm{OUT}}(1-D)T_s}{L} \qquad V_{\mathrm{OUT}} = D \cdot V_{\mathrm{DC}} \tag{2.4}$$

2.2.2 Double Pulse Test

DPT is a commonly used test method to evaluate the switching parameters and evaluate the dynamic behaviors of power transistors [30]. In this section, the DPT's operation principle, its configuration, and its setup are introduced.

The DPT adopts the half-bridge configuration discussed in Section 2.2.1, which is the fundamental unit of most inverter topologies. DPT has two basic configurations: the switch-switch configuration and the switch-diode configuration. The two configurations are shown in Figure 2.21 and Figure 2.22. Each configuration has a DC-link voltage input, an inductor as the load, a device under test (DUT) and a gate driver circuit to turn the transistors on and off. The DUT is commonly placed in the lower switch of the half bridge circuit due to the stable measurement ground [31]. The test is carried out on the DUT, by imposing two pulses of gate signals to control the devices' on and off, which avoids too much heat generated in the DUT.



(a) *The upper device is constantly off* ***(b)*** *The upper device is switched conplemetarily to the DUT*

Figure 2.21: *Illustration of switch-switch DPT configurations*

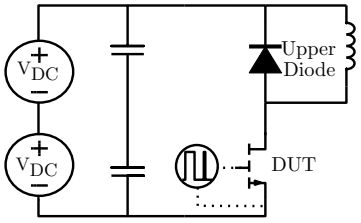


Figure 2.22: *Switch-diode DPT configuration*

The selection of the upper device can affect the results of the DPT, since different devices have different output capacitances and dynamic characteristics [31]. In this case, the switch-switch configuration is a better representation of the motor driver application. Therefore, in this project the switch-switch configuration is adopted. For switch-switch configuration, as shown in Figure 2.21, there are two switching patterns for the upper GaN transistor, which is further explained below:

- **The First Switching Pattern**: The first switching mode is to turn off the upper switch during the DPT, called 'constantly-off'. In this case, the upper GaN transistor exhibits the type B reverse conduction in Table 2.2.

- **The Second Switching Pattern**: The second switching mode is to switch the upper switch complementarily to the DUT. In this case, the upper switch exhibits the type C reverse conduction in Table 2.2.

The turn-on and turn-off of the GaN-on-Si transistors, like the Si-based transistors, are controlled by the gate driver circuit. A gate driver circuit interfaces low-power signals, for example, from an arbitrary function generator, with high-power semiconductor switches [32]. The gate driver circuit charges and discharges the transistor nodes to realize the turn-on and turn-off process of the transistors. Figure 2.23 interprets the typical gate turn-on and turn-off loops.

DPT works in the following way. At first, the DC-link capacitor is charged to the required voltage level. Then, during the first pulse, DUT is turned on at t_1 and the DC-link voltage is imposed on the load inductor. As a result, the load current ramps up linearly if the load inductor is considered to work without saturation. The charging of the inductor is shown with the red current path in Figure 2.24a. The slope of current ramp, di/dt and the charging duration t_2 of the inductor can be calculated by the Equation (2.5). When the current reaches the desired current I_L, the DUT turns off.

$$\frac{di}{dt} = \frac{V_{DC}}{L} \qquad t_2 = \frac{I_L}{\frac{di}{dt}} \tag{2.5}$$

In the second stage, the DUT remains off. The current in the inductor can not change abruptly, therefore, the current freewheels through the GaN's 2DEG channel, as shown in Figure 2.24b. The value of the current will decrease due to the reverse conduction losses in 2DEG channel and the parasitic loss in the inductor. The duration of this stage t_3 should be larger than the summation of the switching time of the DUT and the dead time (if the upper GaN adopts the second switching pattern). However, this time could not be too large to prevent the current from dropping too much.

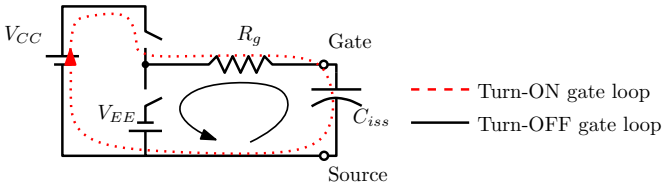
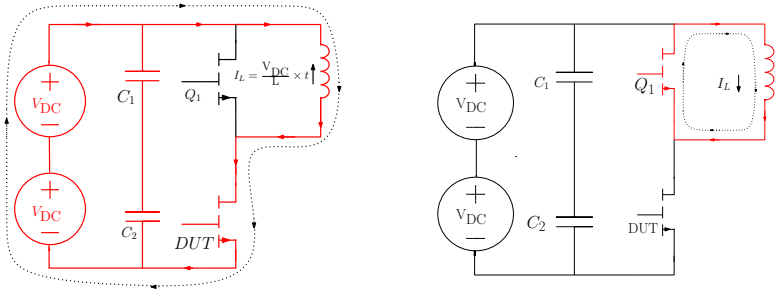


Figure 2.23: *Typical gate loop. VCC and VEE are two voltage sources.*

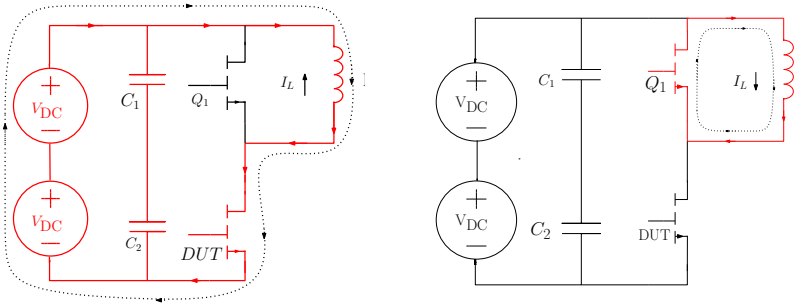


(a) *DUT first turn-on.* ***(b)*** *DUT first turn-off.*

Figure 2.24: *DPT's first turn-on and turn-off events.*

In the third stage of the DPT, the current commutes from the upper GaN to the lower GaN, as shown in Figure 2.25a. The current starts to increase from the inductor's charged current I_{L}, minus the current lost, δI, due to losses. The rate of increase is the same as the first stage. The duration of this stage t_4 should be designed so that the final current does not exceed the rated pulse current $I_{\mathrm{pulse,rated}}$ listed on the device data sheet, as shown in Equation (2.6).

$$I_{\mathrm{L}}^{'} = I_{\mathrm{L}} - \delta I \qquad I_{\mathrm{L}}^{'} + \frac{di}{dt} \cdot t_4 \leq I_{\mathrm{pulse,\ rated}} \tag{2.6}$$



(a) *DUT second turn ON period* ***(b)*** *DUT* 2^{nd} *Turn-off period*

Figure 2.25: *DPT's second turn-ON and turn-off events*

In the last stage, the DUT is turned off. The current flows reversely into the upper switch again and gradually decays to zero over time.
Figure 2.26 describes the waveform patterns for both switching patterns. It should be noted that there are parasitics in both the gate loop and the power loop. Therefore, the switching pattern here is ideal. In reality, there will be overshoot and oscillations.

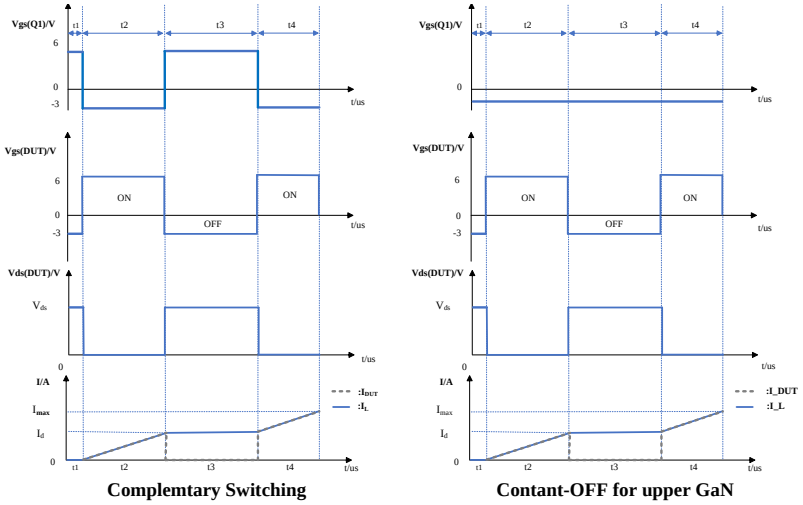


Figure 2.26: *V_{gs} and V_{ds}, and I_d waveforms during the DPT, without considering the transients*

2.3 On-State Voltage Measurement Circuits

This section analyses state-of-the-art on-state voltage measurement circuits (OVMCs) used for acquiring accurate measurements of the on-state voltage $V_{\mathrm{ds(on)}}$ of a device under test (DUT). An introduction to the operating principle and challenges of OVMCs are given in Section 2.3.1. Then, properties of diodes that are important for circuit performance are covered in Section 2.3.2. The mismatch in a full Wilson Current mirror is derived in Section 2.3.3. The mirror is used in the implemented circuit, and the derivation shows how the gain of the transistors affects the current mismatch. Then transistor, diode and matched diode OVMCs found in literature are discussed in Sections 2.3.4 to 2.3.6. These sections describe the operating principles and discuss the pros and cons of each type of OVMC. Finally, settling time considerations are discussed in Section 2.3.7.

2.3.1 Introduction

Determining D-$R_{\mathrm{ds(on)}}$ of GaN devices presents several practical challenges, with one of the most significant being the accurately measuring $V_{\mathrm{ds(on)}}$. In GaN

devices with high blocking voltage, there is often a large discrepancy between $V_{ds(on)}$ and $V_{ds(off)}$. This is also the case for the devices selected in this thesis, see Table 1.1. The off-state blocking voltage can reach several hundred volts, while $V_{ds(on)}$— determined by the load current I_d and $R_{ds(on)}$— is typically much lower, ranging from a few volts down to mere millivolts due to the inherently low $R_{ds(on)}$ of GaN devices.

Assume we measure $V_{ds(on)}$ using a passive probe with an oscilloscope that has an effective number of bits (ENOB) of 12. For example, the device GPIXV30DFN, see Table 1.1, could be operated at an off-state voltage of 800 V, the resulting vertical resolution is calculated as

$$\text{Vertical Resolution} = \frac{800}{2^{12}} \approx 195\,\text{mV}, \tag{2.7}$$

This resolution is insufficient for accurately measuring the desired voltage range, $[0, 2]$ V. To address this, on-state voltage measurement circuits (OVMC), also referred to as voltage clamping circuits, are commonly employed to improve vertical resolution for $V_{ds(on)}$ measurements, which are essential for determining D-$R_{ds(on)}$ [33].

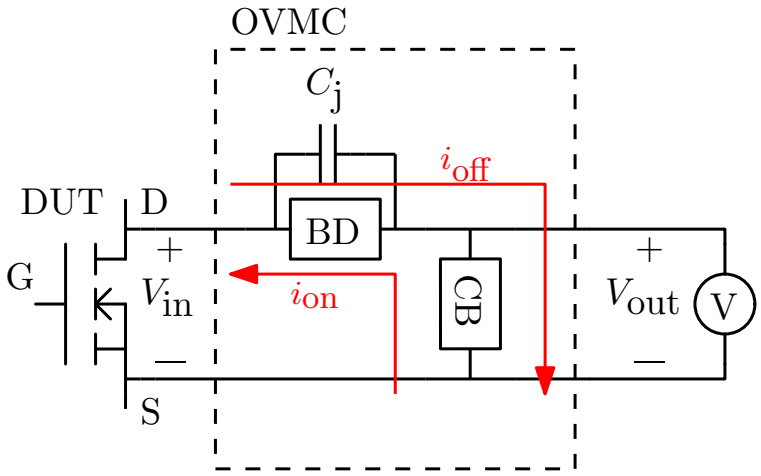


Figure 2.27: *Conceptual schematic of a OVMC showcasing its two fundamental parts: the Blocking Device (BD) and the Clamping Branch (CB). The junction capacitance C_j of the BD and the high slew rate of the device under test cause two currents, I_{on} and I_{off}, to flow through the OVMC circuit as illustrated, during the on-state and off-state transients respectively. The voltage probe is assumed to be connected to an oscilloscope.*

A general OVMC can be divided into two fundamental circuit blocks, a blocking device (BD) and a clamping branch (CB). An OVMC connected to a device under test (DUT) and an oscilloscope is presented in Figure 2.27. During the blocking

state, the blocking device prevents high voltage from reaching the input terminals of the oscilloscope, and the clamping branch keeps V_{out} below V_{clamp}. While during the measurement state [34], V_{out} is ideally measured as

$$V_{out} = V_{in} = V_{ds(on)}. \tag{2.8}$$

Assume the same measurement scenario as described above is repeated using an OVMC with a V_{clamp} of 4 V. The resulting vertical resolution that can achieved in the oscilloscope is

$$\text{Vertical Resolution} = \frac{4}{2^{12}} \approx 1\,\text{mV}, \tag{2.9}$$

which is much better compared to 195 mV.

All OVMCs are faced with a common problem, currents caused by the parasitic junction capacitance (C_j) of the blocking device and the high slew rate of the DUT, see Figure 2.27. During the DUT turn-on transient, the current I_{on} flows as shown in Figure 2.27. Similarly, the current I_{off} flows in the opposite direction during the turn-off transition. If there isn't a low impedance path in both current directions, voltage peaks that are many times larger than V_{clamp} can occur, which can either harm the OVMC or force an increase of the vertical scale, thus decreasing the vertical resolution of the oscilloscope [35]. Hence, there should exist a low impedance current path in both current directions, furthermore, a BD with small C_j should be selected to minimize the induced currents.

2.3.2 Diodes

Diodes are central components in OVMCs. As will be explained in Section 2.3.5, Schottky diodes are commonly used as blocking devices and Zener diodes are used to select the clamping voltage V_{clamp} of the circuit. This section highlights properties of the diode that are of importance for the OVMCs' operation.

A diode is commonly used as a rectifier. It has three operating regions: the forward-bias region, the blocking region, and the break-down region, see Figure 2.28. In its on-state, i.e. the forward-bias region, the IV relationship is given by

$$I = I_s[\exp(\frac{qV}{KT}) - 1], \tag{2.10}$$

where I_s is a device-specific constant, k is Boltzmann's constant, T is the absolute temperature in Kelvin, and q is the charge of one electron. The forward voltage $V_f(I, T)$ is dependent on both temperature and current. In reverse bias, the diode operates in the blocking region and only a small leakage current is conducted through the diode. For a large enough reverse voltage (V_{BR}) the diode enters the breakdown region and the diode conducts in reverse. Operating in the breakdown region is usually not destructive if the power dissipation is limited [36].

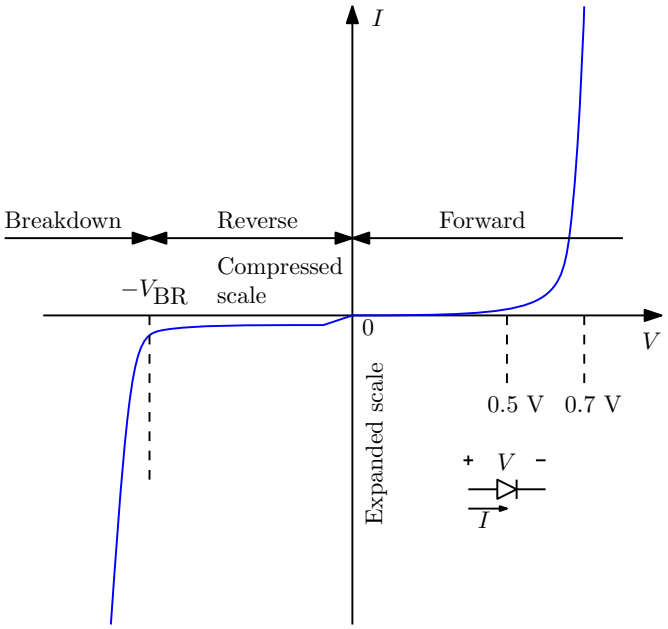


Figure 2.28: *I-V characteristic of a diode.*

Zener diodes are PN junction diodes designed to operate in reverse breakdown. The steep slope of the IV-curve makes them useful for voltage clamping [36]. However, to ensure proper voltage regulation the IV-curve must be studied in detail, see Figure 2.29.

In the blocking region, a leakage current, that is dependent on the reverse voltage, flows through the diode. At $-V_{ZK}$, the Zener breakdown region is entered and the current increases rapidly. I_{ZK} is often given in datasheets and is the minimum current required for reasonable regulation. The Zener voltage is not constant. For increasing currents, there is a slope in the IV-curve that can be modeled as a resistor. For proper operation, a Zener diode is often operated above or around a specified test current I_{ZT} [37].

Minimizing the parasitic capacitances of diodes is essential in fast-switching circuits. A PN junction diode has two main types of capacitance: junction capacitance C_j and diffusion capacitance C_d. In reverse bias, the diode's depletion region acts as an insulator, allowing the diode to function like a parallel plate capacitor - this is known as C_j. As the reverse voltage increases, the capacitance decreases due to the widening of the depletion region and the removal of additional charges. In forward bias, however, excess charge accumulates within the diode, leading to what is referred to as diffusion capacitance C_d. When the voltage of a diode in forward conduction switches polarity, the diode will briefly reverse conduct as it discharges the diffusion capacitance, and reaches the off-state [36]. The discharge of C_d is normally called reverse recovery [2].

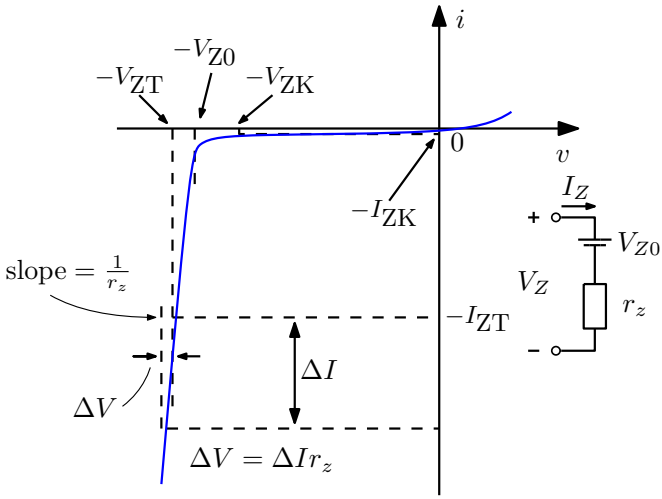


Figure 2.29: *I-V characteristic of a Zener diode.*

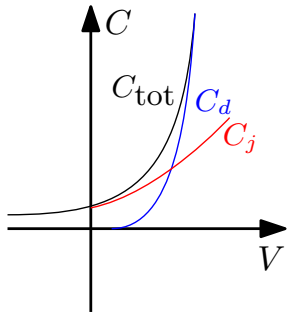


Figure 2.30: *Size of diffusion capacitance C_d and junction capacitance C_j of diode as a function of voltage, and C_{tot} is the sum of the two.*

In reverse biased condition the capacitance is dominated by C_j and in forward conduction usually by C_d [36], see Figure 2.30.

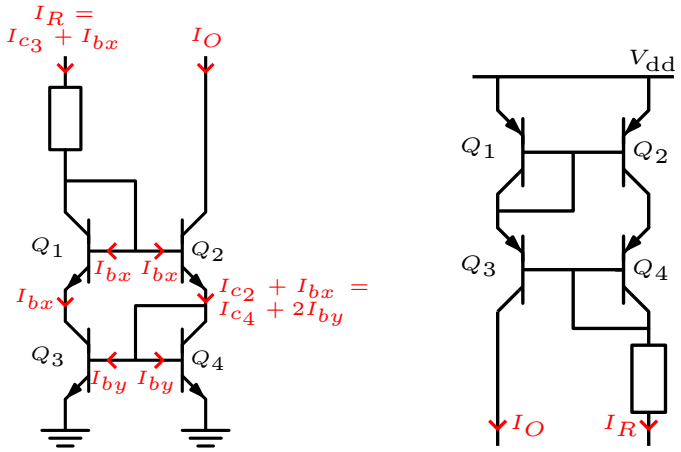
Schottky diodes don't have a PN junction. Instead, they are formed by a metal together with a semiconductor. Schottky diodes has almost no diffusion capacitance and are therefore faster than pn junction diodes and more suitable for fast-switching applications [2].

2.3.3 Full Wilson Current Mirror

A current mirror ideally generates an output current that is a perfect copy of a reference current. This property is crucial to attain high accuracy in matched diode circuits, this is further discussed in Section 2.3.6. In this section the error, i.e. the current mismatch between the copy and reference current of a Full

Wilson Current Mirror is derived.

Two Full Wilson Current Mirrors can be seen in Figure 2.31. The first mirror is implemented using NPN BJTs and acts like a current sink, while the other is implemented using PNP BJTs and acts like a current source, see Figures 2.31a and 2.31b.



(a) *NPN mirror (sinking current).* ***(b)*** *PNP mirror (sourcing current).*

Figure 2.31: *Full Wilson Current Mirrors.*

Figure 2.31a is used to analyze the error between I_R and I_O, where I_R is the reference current controlled by R, and I_O is the output current. The analysis also holds for Figure 2.31b [38]. Starting, we assume that Q_1 and Q_2 have the same gain β_x, similarly Q_3 and Q_4 have the same gain β_y. Since the base to emitter voltage of Q_{3-4} are the same, we assume that

$$I_{c_3} = I_{c_4}. \tag{2.11}$$

From the KCL in Figure 2.31a, we get

$$I_R = I_{c_3} + I_{bx} \tag{2.12}$$

and

$$I_{c_2} + I_{bx} = I_{c_4} + 2I_{by}. \tag{2.13}$$

Using the relation $I_c = \beta I_b$ for a BJT, we can rewrite Equations (2.12) and (2.13) as

$$I_{c_3} = I_R - \frac{I_{c_2}}{\beta_x} \tag{2.14}$$

and

$$I_{c_2}(1 + \frac{1}{\beta_x}) = I_{c_4}(1 + \frac{2}{\beta_y}). \tag{2.15}$$

Substituting Equations (2.14) and (2.15) into Equation (2.11) and solving for $\frac{I_O}{I_R}$ we get

$$\frac{I_O}{I_R} = \frac{1 + \frac{2}{\beta_y}}{1 + \frac{2}{\beta_x} + \frac{2}{\beta_x \beta_y}}. \tag{2.16}$$

Assuming $\beta_x, \beta_y >> 1$, we get approximately

$$\frac{I_0}{I_R} \approx 1. \tag{2.17}$$

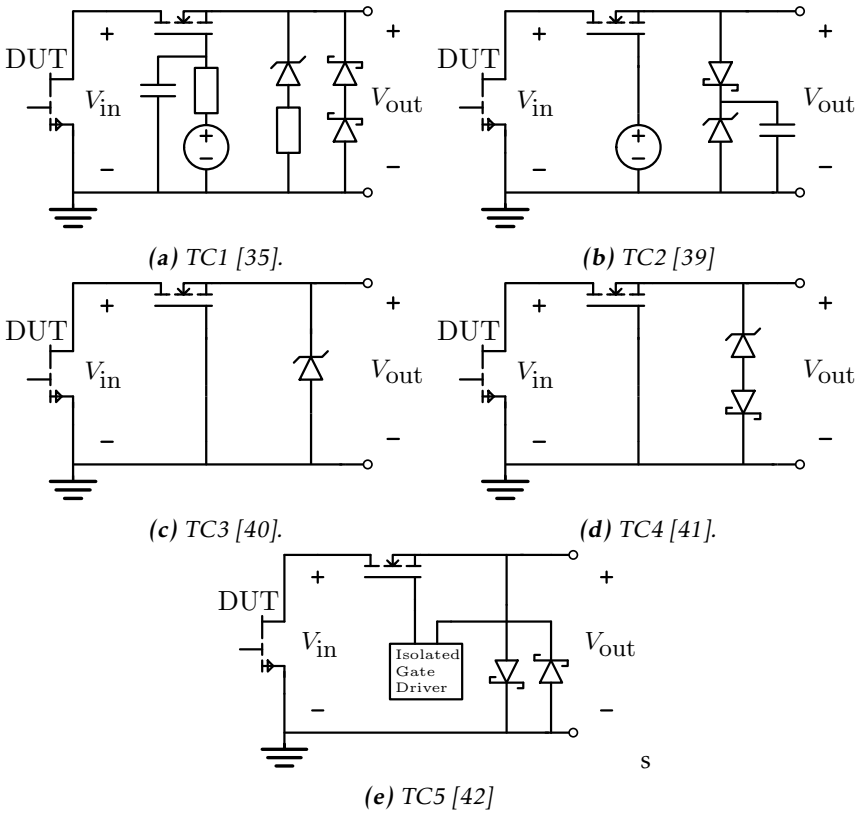
This analysis concludes that the gain of the transistors should be as large as possible to minimize the error between the reference current I_R and the output current I_O.

2.3.4 Transistor Circuits

This section reviews OVMCs using a transistor as a blocking device. All circuits use an N-channel transistor, which can be either an enhancement mode or depletion mode transistor. The transistor is either actively switched or constantly biased. A summary of the transistor configurations can be seen in Table 2.3, and the circuits are shown in Figure 2.32.

Table 2.3: *Summary of transistor configurations in Figure 2.32.*

Figure	Gate Control	Transistor Type
Figure 2.32a	Constantly biased	Enhancement mode
Figure 2.32b	Constantly biased	Enhancement mode
Figure 2.32c	Constantly biased	Depletion mode
Figure 2.32d	Constantly biased	Depletion mode
Figure 2.32e	Actively switched	Enhancement mode



(a) TC1 [35]. *(b) TC2 [39]*

(c) TC3 [40]. *(d) TC4 [41].*

(e) TC5 [42]

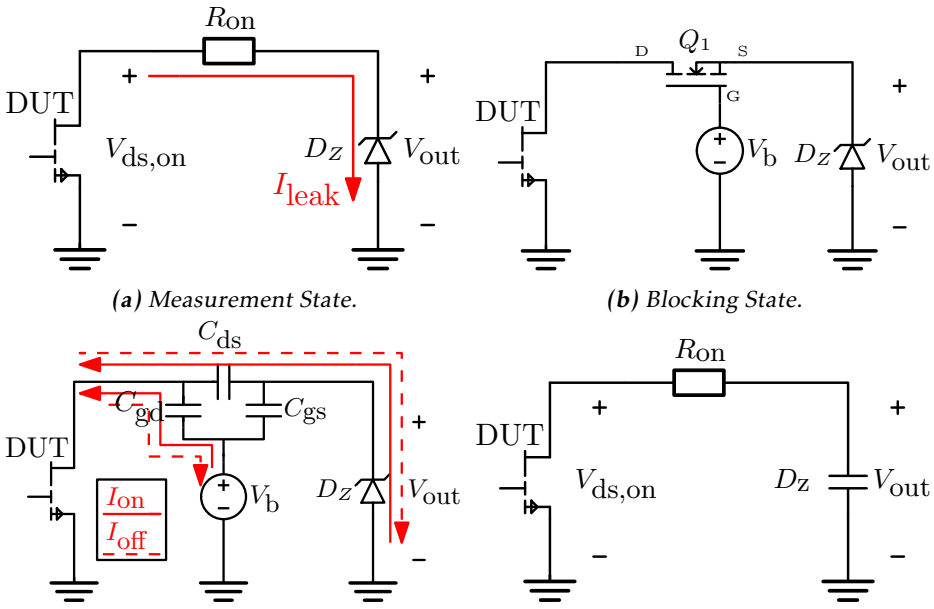
Figure 2.32: *Transistor OVMCs.*

The operation of TC1 and TC2 is described in Figure 2.33. The circuit uses a constantly biased enhancement mode transistor as a blocking device and a Zener diode as clamping branch. During the measurement state, the transistor operates in the linear region and the Zener diode operates in the blocking region. Thus, only a small leakage current flows through the Zener diode and V_{out} is given by

$$V_{out} = V_{ds(on)} - I_{leak} R_{on}, \tag{2.18}$$

where R_{on} is the resistance of the blocking transistor, see Figure 2.33a. The term $I_{leak} R_{on}$ is usually small enough to be negligible, so

$$V_{out} = V_{ds(on)}. \tag{2.19}$$



(a) Measurement State. *(b) Blocking State.*

(c) Transient State. *(d) Settling State.*

Figure 2.33: *Schematic describing the operating principles of transistor OVMCs in different states. In the measurement and blocking state, the DUT is on and off, respectively. For the transient state, currents during turn-on and turn-off transients are illustrated. The settling state shows the equivalent circuit immediately after the turn-on transient of the DUT.*

During the on-state and off-state transients, the currents I_{on} and I_{off} flow through D_z, forward and reverse biasing D_z, see Figure 2.33c. After the turn-on transient, the settling time of the circuit is dependent on the RC circuit formed by Q_1's on-state resistance and the junction capacitance of D_z, see Figure 2.33d. In the blocking state, V_{out} is charged to

$$V_{clamp} = V_{bias} - V_{th,min}, \tag{2.20}$$

and Q_1 is turned off. The Zener voltage must be selected sufficiently high so that it doesn't reverse conduct before Q_1 is turned off, i.e.,

$$V_z > V_{clamp} = V_{bias} - V_{th,min}. \tag{2.21}$$

The operational principles of a circuit using depletion-mode transistors are essentially analogous. The obvious benefit is that it doesn't require an external power supply to provide a gate bias voltage [41]. However, here the maximum measurable $V_{ds(on)}$ is limited by the transistor threshold voltage, i.e.

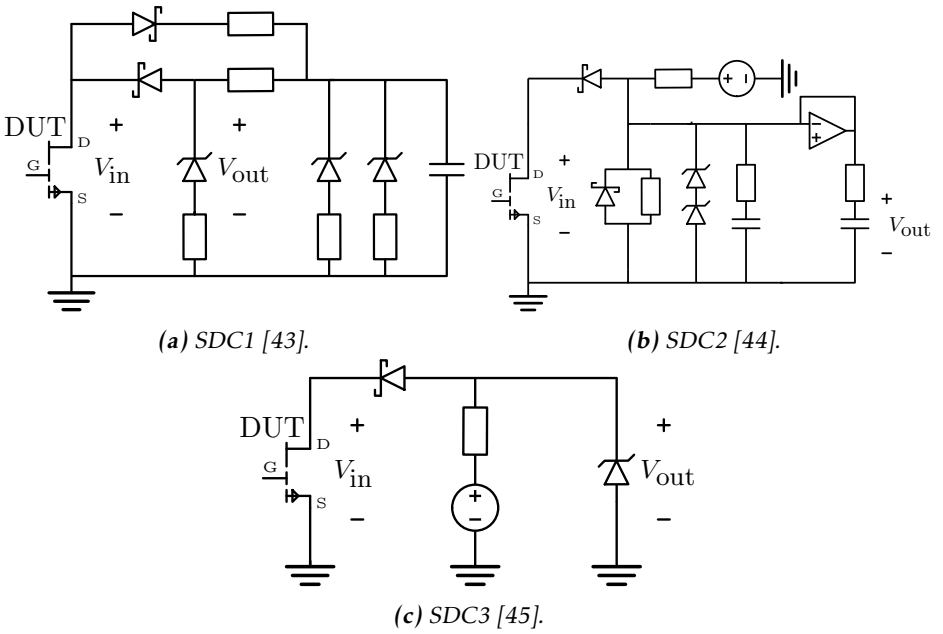
$$V_{out} \leq V_{th}. \tag{2.22}$$

In TC5, see Figure 2.32e, the transistor is actively switched by an isolated gate driver. A delay circuit is used to turn the transistor on after a specific amount of

time once the DUT is turned on and $V_{ds(on)}$ of the DUT is small. A benefit of using an actively switched transistor is that V_{clamp} can be selected independently from V_{bias}, thus V_{clamp} must only be larger than the largest $V_{ds(on)}$. In [42], Schottky diodes are used for clamping instead of Zener diodes and the measured $V_{ds(on)}$ is in the range of 100 mV.

2.3.5 Diode Circuits

This section reviews OVMCs using a diode as blocking device. Investigated circuits can be seen in Figure 2.34.



(a) SDC1 [43]. *(b) SDC2 [44].*

(c) SDC3 [45].

Figure 2.34: *Diode OVMCs.*

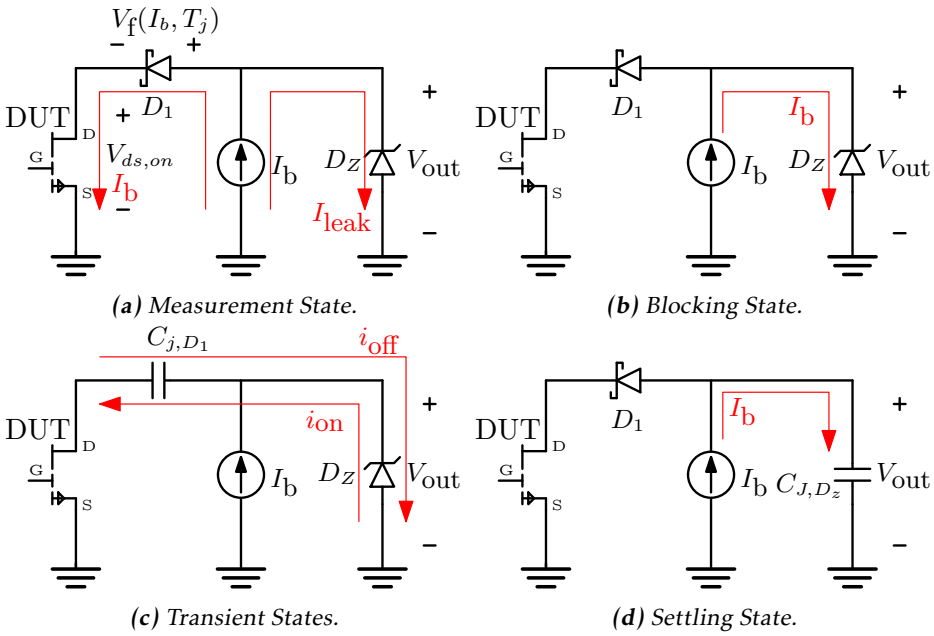
Figure 2.35 describes the different operating principles of diode circuits during their different states. Diode circuits use a voltage or current source to generate a biasing current I_b. During the measurement state, I_b flows through the blocking diode D_1 and is injected into the DUT, see Figure 2.35a. The output voltage V_{out} is given by

$$V_{out} = V_f(I_b - I_{leakage}, T_j) + V_{ds,on}, \tag{2.23}$$

where I_{leak} is the leakage current through the Zener diode and T_j is the junction temperature of D_1. With a proper selection of Zener diode, i.e.,

$$V_z > V_f(I_b, T_j) + V_{ds,on}, \tag{2.24}$$

and the Zener diode test current I_{ZT} should be smaller than I_b, so that the Zener diode operates well in the Zener breakdown region. Assuming $I_{leakage}$ is small



(a) Measurement State. *(b) Blocking State.*

(c) Transient States. *(d) Settling State.*

Figure 2.35: *Schematic describing the operating principles of diode OVMCs in different states. In the measurement and blocking state, the DUT is on and off, receptively. For the transient state, currents during turn-on and turn-off transients are illustrated. The settling state shows the equivalent circuit immediately after the turn-on transient of the DUT.*

enough to be neglected

$$V_{out} = V_f(I_b, T_j) + V_{ds,on}. \tag{2.25}$$

To extract $V_{ds(on)}$, the forward voltage $V_f(I_b, T)$ must be characterized for the given I_b and junction temperature T_j, and removed from measurements during post-processing. The accuracy of the measurement is thus dependent on a stable I_b and T_j, and also the quality of the IVT characterization of the diode. During the blocking state, V_{in} is much higher than V_z, hence I_b flows through D_z and V_{out} is clamped to V_z, see Figure 2.35b.

During the turn-on transient, V_{out} is negative and equal to the forward voltage of the Zener diode, see Figure 2.35c. Immediately after the turn-on transient, the Zener diode can be modeled as a capacitor and I_b charges the junction capacitance, see Figure 2.35d. The circuit enters the measurement state as soon as the output node is charged to

$$V_{out} = V_f(I_b, T_j) + V_{ds,on}. \tag{2.26}$$

Thus, settling time is determined by I_b, the reverse recovery, and the junction capacitance (C_j) of the Zener diode. An advantage of diode circuits is that I_b

is under the designer's control and the response time can be controlled freely. However, I_b adds to the drain current of the DUT introducing a measurement error. A trade-off between response time and the error introduced must be made. During the turn-off transient, D_z operates in the Zener breakdown region and V_{out} is equal to V_z, see Figure 2.35c.

2.3.6 Matched Diode Circuits

This section reviews matched diode OVMCs, investigated circuits can be found in Figure 2.37. Matched diode circuits use two diodes, one as a blocking device and another to compensate for the voltage offset caused by the blocking diode's forward voltage. Two biasing currents I_{b_1} and I_{b_2}, are generated either by a voltage source together with resistors, see Figures 2.37a to 2.37c, or a current mirror, see Figures 2.37d and 2.37e.

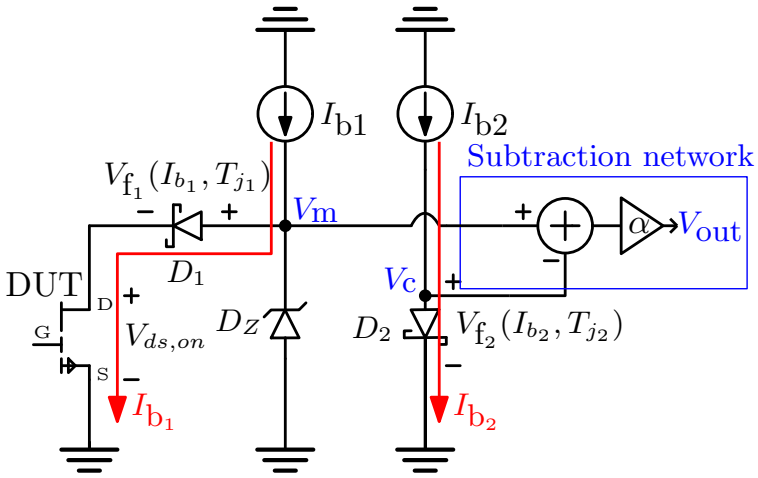


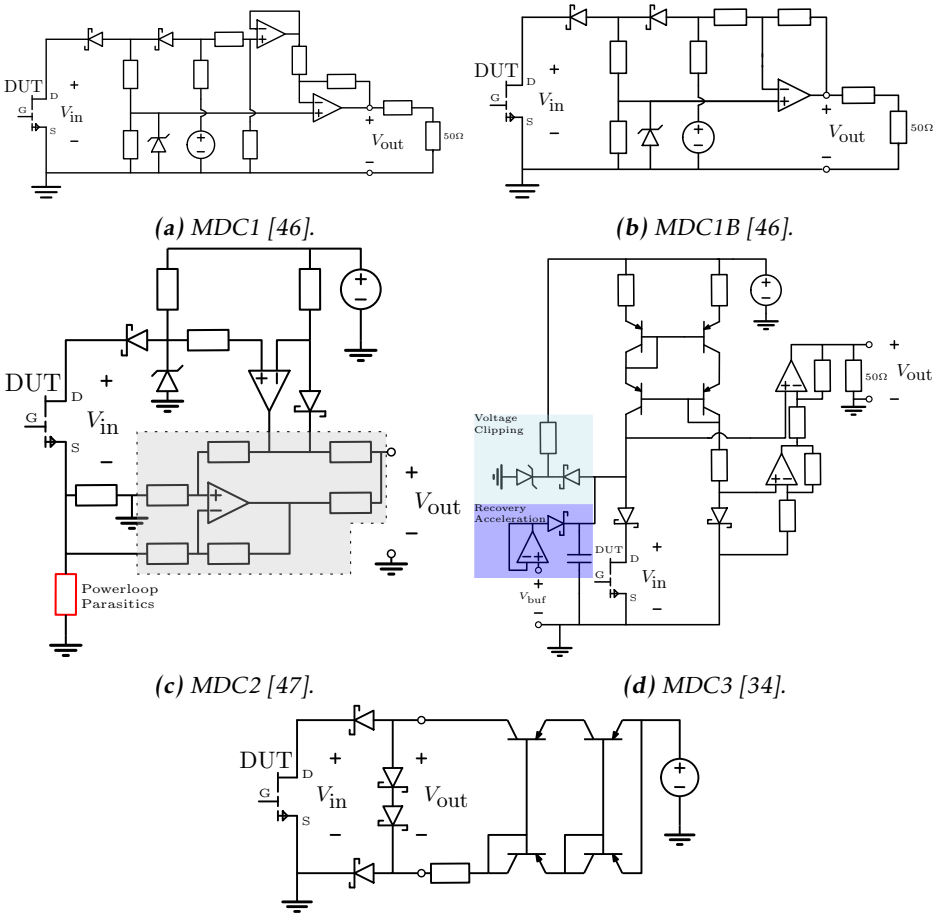
Figure 2.36: *Schematic describing the operating principle of a matched diode circuit with a subtraction network during the measurement state.*

Most commonly, these circuits employ a subtraction network, see Figures 2.37a to 2.37d. A schematic describing the concept of using a subtraction network can be seen in Figure 2.36. In the measurement state, I_{b_1} flow through D_1 and the DUT, and I_{b2} through the compensation diode D_2. Hence, the voltage in the measurement node V_m is $v_{ds,on} + V_{f1}(I_{b1}, T_1)$, and in the compensation node V_c, the voltage is $V_{f2}(I_{b2}, T_2)$. Subtracting V_c from V_m, the output is

$$V_{out} = V_{ds,on} + V_{f1}(I_{b1}, T_1) - V_{f2}(I_{b2}, T_2). \tag{2.27}$$

Using the same type of diode for D_1 and D_2, they ideally have the same forward voltage

$$V_{f1}(I_{b1}, T_1) = V_{f2}(I_{b2}, T_2) \tag{2.28}$$



(a) *MDC1 [46].*

(b) *MDC1B [46].*

(c) *MDC2 [47].*

(d) *MDC3 [34].*

(e) *MDC4 [48].*

Figure 2.37: *Matched diode OVMCs.*

and

$$V_{\text{out}} = V_{\text{ds,on}}. \tag{2.29}$$

Further, the subtraction network usually enables the output to be scaled with a factor α according to

$$V_{\text{out}} = \alpha V_{\text{ds,on}}. \tag{2.30}$$

The possible scaling factors of MDC1, MDC2 and MDC3 are as follows:

- MDC1: $\alpha \leq 1$.
- MDC2: $\alpha = 1$,
- MDC3: $\alpha > 1$.

If MDC1 with $\alpha = 1$ is used, MDC1 can be simplified to MDC1B.

Matched diode circuits can be employed without a subtraction network, see Figure 2.37e. In [49, 50], MDC4 is used together with an active differential probe to directly measure the on-state voltage. The operating principles of matched diode circuits in the blocking state, and during turn-on and turn-off of the DUT, as well as response time considerations, are the same as for single diode circuits discussed in Section 2.3.5.

Selection of the matching diode pair is discussed in [46]. For the best accuracy, a component including two diodes in the same package is optimal. Then the diodes will maintain the same temperature and be from the same production process. However, due to multiple special requirements on the diode such as high blocking voltage and low C_{j}, such a component might be difficult to find. Two single diodes of the same type can be used. For optimal accuracy, an IVT characterization should be performed to ensure they have the same forward voltage drop within the operation region. Furthermore, D_1 is excited to higher voltage swings and is placed closer to the DUT, hence in the PCB layout the diodes should be placed close to each other to enable thermal coupling and could also be covered with thermal paste.

2.3.7 Settling Time Considerations

This section discusses different methods to improve settling time suggested in [51]. One of the factors dominating the settling time of the OVMCs is the output node capacitance. One efficient way to decrease the node capacitance is putting Schottky diodes, with small C_{j}, in series with the Zener diode which usually have a large C_{j}. Putting N Schottky diodes with junction capacitance C_{s} in series with a Zener diode with junction capacitance C_{z} yields the total junction capacitance C_{tot} as

$$\frac{1}{C_{\text{tot}}} = \frac{N}{C_{\text{s}}} + \frac{1}{C_{\text{z}}}. \tag{2.31}$$

Assuming $C_z \gg C_s$, gives

$$C_{tot} \approx \frac{C_s}{N}. \tag{2.32}$$

An additional method called reverse recovery acceleration is discussed in [51]. The settling time is sped up by "pre-charging" the junction capacitance using a voltage source between the ground and the Schottky diode, see Figure 2.38.

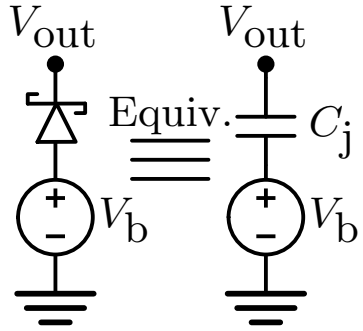


Figure 2.38: *Reverse recovery acceleration circuit.*

3
Method

This chapter outlines the methodology used to investigate the research questions presented in the first chapter. Section 3.1 details the literature review conducted to explore how different operational parameters, e.g., V_{ds}, I_d, and f_{sw}, affect dynamic on-resistance. Further, Section 3.2 examines various measurement methodologies that have been employed in previous research, providing insight into their strengths and limitations. Finally, Section 3.3 describes the selection, design, implementation, and evaluation of an on-state voltage measurement circuit.

3.1 Operational Parameters' Effect on D-$R_{ds(on)}$

This section outlines the process of conducting a literature review on parameters that influece D-$R_{ds(on)}$. Given the relatively novel nature of the research on D-$R_{ds(on)}$, most of the reviewed material was sourced from reputable journals, such as IEEE and doctoral theses. Initially, the impact of various parameters on D-$R_{ds(on)}$ was unclear, and this required an iterative approach in which new parameters were identified and added as the review progressed. The findings of the literature review are detailed in Section 4.1.

3.2 Measurement Methodologies

This section outlines the method for identifying the most suitable approach to measure D-$R_{ds(on)}$ in electric motor drive applications. Various measurement methodologies have been documented in the literature. The most commonly used testing methodologies include the Pulsed I-V Test [52], Double-Pulse Test (DPT), Multiple-Pulse Test (MPT) [45], and Steady-State Continuous Switching

Test (SSCS) [53].

Although SSCS is frequently cited as the most effective method for D-$R_{ds(on)}$ characterization [16, 53, 54], these studies often lack application-specific context, such as the power ratings and operational conditions. Therefore, it is necessary to determine which method is suitable for determining D-$R_{ds(on)}$ in electric motor drive applications.

3.2.1 Figures of Merit

This section presents the figures of merit (FOM) used to evaluate the measurement methodologies.

As presented in Section 2.1.3, it could take up to several seconds for D-$R_{ds(on)}$ to reach an equilibrium state in an actual motor drive application. Therefore, it was assumed that the longer the device was switched, the more precise the measurement of D-$R_{ds(on)}$ would be. Consequently, the number of switching cycles, or equivalently, the test duration, was chosen as one of the FOM.

Moreover, the measurement method should be practically feasible to conduct. Therefore, the complexity of the laboratory setups and the number of testable operational parameters that the methodology can assess were included as figures of merit.

Lastly, in the literature review of the effect of the operation parameters on D-$R_{ds(on)}$, see Section 4.1, it was found that the effect of T_j on D-$R_{ds(on)}$ is arbitrary and unknown. Therefore, it was assumed crucial to limit the heat dissipated during the test to isolate the impact of T_j. A maximum temperature change $\Delta T_j \leq 10°C$ was defined as acceptable under forced air cooling and a constant $R_{ds(on)}$. Under this limitation, the testable range of the operational parameter was chosen as one of the FOM. All figures of merit are summarized in Table 3.1.

Table 3.1: *FOM of Measurement Methodology*

Figures of Merit	**Details**
Number of switching cycles	More cycles, better accuracy
Complexity of test setups	Simpler is better
Number of testable operational parameters	More is better
Testable range of the operational parameters	Higher is better

3.2.2 Evaluation Method and PLECS Setup

This section describes the evaluation method used for selecting the most suitable measurement method for determining D-$R_{ds(on)}$ in electric motor drive applications based on the FOM defined in Table 3.1. It also details the thermal and electrical parameters used in PLECS simulations to determine the testable range of parameters. The individual PLECS schematics and calculated component values are presented in their respective subchapters.

For most of the measurement methods, the number of cycles were trivial, such as the DPT and SCSS. DPT is conducted using two switching cycles, while SCSS switches until the device reaches the thermal-steady state. MPT strikes a balance between DPT and SCSS, trading off between the number of cycles and heat dissipation. The number of switching cycles is reduced to limit heat dissipation. As a result, the number of cycles in MPT lies between those of DPT and SCSS, offering medium accuracy.

The number of testable parameters was also straightforward to determine. For DPT, it was concluded that evaluating the effects of switching frequency and duty cycle was difficult since it has only two pulses. For MPT and SCSS, all the parameters, including D, f_{sw}, could be evaluated.

The complexity of the test setup was determined by factors such as the number of components, their cost, and availability. Other factors, such as the complexity required to control the switching of the devices, were also taken into consideration. A qualitative assessment was then used to rank the various setups.

Conducting simulations in PLECS determined the testable range of the parameters, which was mainly limited by heat dissipation. Due to the project's time constraint, the GS66516T [7] was selected as the only device for evaluation. It has a blocking voltage of 650 V. The maximum V_{ds} was chosen to be 400 V for a safety margin. The device is rated for a maximum continuous current of 60 A, and the maximum current was selected to be 60 A.

The switching frequency (f_{sw}) for a traction inverter usually lies between 10 kHz and 25 kHz. In this study, the frequency was investigated in the range from 10 kHz to 100 kHz. The first reason is that GaN devices exhibit less switching loss due to the reduced gate charge and output capacitance. Second, GaN device does not have a body diode as exists in Si based devices. This means there is no reverse recovery charge that can cause voltage and/or current spikes during the operation [5]. Therefore, GaN devices offer the possibility of high f_{sw}. Literature [55] implemented 100 kHz in its experimental test, which further proves the GaN device's high-speed switching possibility.

The duty cycle D used in this evaluation varied between 0.1 and 0.9. All parameters are summarized in Table 3.2.

Table 3.2: *Table of Common Thermal and Electric Parameters Used in Evaluation*

Parameters	Value
R_{jc}	0.27°C/W
R_{ch}	1.23°C/W
R_{ha}	1.5°C/W
Room Temperature	25°C
V_{ds}	100 – 400 V
I_d	Maximum 60 A
D	0.1 - 0.9
f_{sw}	10 – 100 kHz
Parasitics	1 $\mu\Omega$ and 1 nH

3.2.3 Pulsed-IV Test

The Pulsed I-V Test is widely employed in trapping physics studies, which requires sophisticated lab setups. This method focuses on the device mechanism analysis and is suitable for static characterization on a single die or a packaged device [45]. Therefore, the Pulsed I-V test cannot accurately replicate the actual electric motor drive applications and was concluded unsuitable for characterizing D-$R_{ds(on)}$ in electric motor drive applications.

3.2.4 Double Pulse Test

DPT is a method commonly used in the field of power electronics for evaluating the performance and reliability of semiconductor devices. The basic principle of DPT was discussed in Section 2.2.2. To evaluate DPT for D-$R_{ds(on)}$ characterization, the test was first configured to test all parameters described in Section 3.2.2. Several design considerations had to be taken into account, the most important issues were:

- Load inductance value
- DC-Link capacitance value
- How to realize the soak time control
- Length of each time sequence in DPT
- DPT structure and switching pattern

The load inductance was selected as large as possible to minimize the variation of the inductor current ΔI_L during the switching transient. From Volvo's experience, DPT is capable of handling currents up to 100 A without significant overheat. Hence, the minimum test current was selected to be 10 A for DPT. The minimum load inductance was calculated using Equation (3.1) [31]. In Equation (3.1), $k_{\Delta i}$ denotes the current ripple coefficient, typically between 1% and 5% [31]. Here,

5% was selected. $t_{\mathrm{sw(max)}}$ represents the maximum switching time. And in the device data sheet [7], only the switching time under "V_{ds} = 400 V, I_d = 16 A, R_g = 5 Ω, and T_j = 25 °C" was given. Here, $t_{\mathrm{sw(max)}}$ = 50 ns was chosen for some extra margin.

The DUT's switching performance is usually evaluated at various operating points. And the worst-case scenario for selecting the load inductance occurs at the maximum operating voltage $V_{DC(\mathrm{max})}$ = 400 V and minimum current $I_{L(\mathrm{min})}$ = 10 A, according to Equation (3.1).

$$L \geq \frac{V_{DC(\mathrm{max})} \times t_{\mathrm{sw(max)}}}{k_{\Delta i} \times I_{L(\mathrm{min})}} = \frac{400 \times 50 \times 10^{-9}}{0.05 \times 10} = 40 \times 10^{-6} H = 40\,\mu\mathrm{H} \tag{3.1}$$

Equation (3.1) gives the minimum of the required inductance. And it is suggested to select the inductance value close or equal to the result in Equation (3.1) to reduce the current rise time and heat dissipation [31]. Therefore, the value of the inductance was determined as 40 μH.

The DC-Link capacitance was determined to limit the DC bus voltage variation ΔV_{DC} according to Equation (3.2) [31]. The voltage ripple coefficient k_Δ was selected to be in the typical range 1-5% [31], and 5 % was selected for this study. Based on the calculations in Equation (3.2), a capacitance greater than 144 μF was required. Consequently, a capacitance of 200 μF was selected.

$$C_{\mathrm{DC}} \geq \frac{LI_L^2}{(2V_{DC} - \Delta V_{DC})\Delta V_{DC}} = \frac{LI_L^2}{(2 - k_\Delta)k_\Delta V_{DC}^2} \approx \frac{LI_{L(\mathrm{max})}^2}{2k_\Delta V_{DC(\mathrm{min})}^2} = 144\,\mu\mathrm{F} \tag{3.2}$$

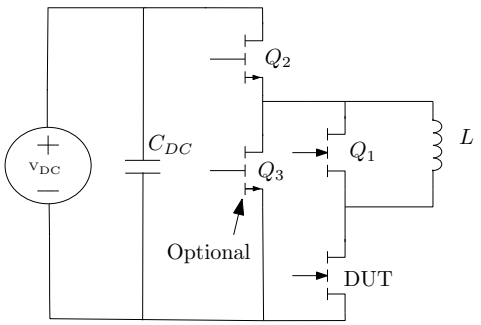


Figure 3.1: *Modified DPT circuit with soak time control*

Then the soak time was determined. Soak time (in Figure 2.26, t_1) is the time duration before starting sending pulses to the DUT, when, the DUT has already been subjected to high voltage. This has a non-negligible effect on the D-$R_{\mathrm{ds(on)}}$ measurement results. In [56], it is shown that the D-$R_{\mathrm{ds(on)}}$ results are constant when the soak time varies from 100 μs to 600 μs, but that there are large

deviations when soak times are from 2 s – 10 s. As a consequence, the soak time should be carefully controlled in D-$R_{ds(on)}$ characterization to achieve a fairer measurement result.

To realize the soak time control, a modification has to be made on the original DPT circuit, as shown in Figure 3.1. Here, Q2 (Q3, optional) serves as an additional control leg to control the soak time to be identical for each test. This realization of soak time control increases control complexity and the component cost in the test.

After the soak time control, the time sequence of DPT should be defined, including the soak time t_1, first pulse duration t_2, rest time t_3 and second pulse duration t_4.

Here, the soak time t_1 was selected to be 100 μs and was identical for all tests, considering that t_1 from 100 μs - 600 μs has similar results, and that a very short soak time is more difficult to implement. t_2 is dependent on I_L and was calculated using Equation (3.3). t_3 needed to be larger than the turn-on and turn-off switching times. However, it could not be excessively long, since the current I_L decays with time. Hence, 1 μs was selected. During t_4, I_L increases, to minimize excessive heat and to observe the detrapping effect, t_4 was set to 1.5 μs.

$$t_2 = \frac{I_L L}{V_{DC}} \tag{3.3}$$

In addition, the optimal turn-on voltage $V_{gs,on}$ and turn-off voltage $V_{gs,off}$ were defined. For the GS66516 device, the transistor is fully enhanced and reaches its optimal efficiency point at 6 V gate drive voltage[7]. The turn-off voltage $V_{gs,off}$ was selected as −3 V to ensure the safe operation against the voltage spike at the gate [7].

Lastly, the DPT structure and switching pattern were defined. Section 2.2.2 introduced the two different DPT structures and switching patterns and provided justification for selecting the switch-switch configuration. The selection of the switching pattern and the evaluation of the DPT were based on the results of PLECs simulations.

The DPT PLECs schematic is presented in Figure 3.2, and the pulse generation process is illustrated in Figure 3.3. The parameter values used in the DPT test are listed in Table 3.2 and Table 3.3. The two switching patterns were simulated using the durations defined above. The voltage and current was set to 400 V and 60 A, representing the worst-case condition. The evaluation was carried out according to the FOM described in Table 3.1, with the results detailed in Section 4.2.1.

Table 3.3: *DPT Parameters*

t1	t2	t3	t4	L
100 μs fixed	Varies with I_L and V_{DC}	1 μs fixed	1.5 μs fixed	40 μH

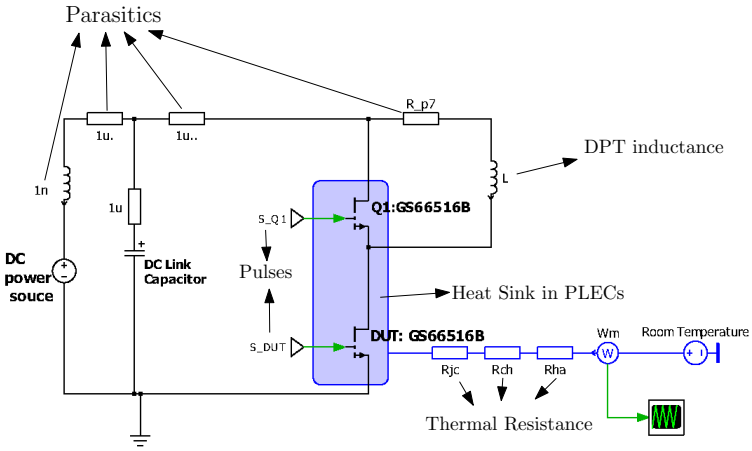


Figure 3.2: *DPT PLECs schematics. The GaN model has loss descriptions of GS66516T installed. The simulation does not consider the soak time control since the soak time's effect on D-$R_{ds(on)}$ is hard to model in PLECs*

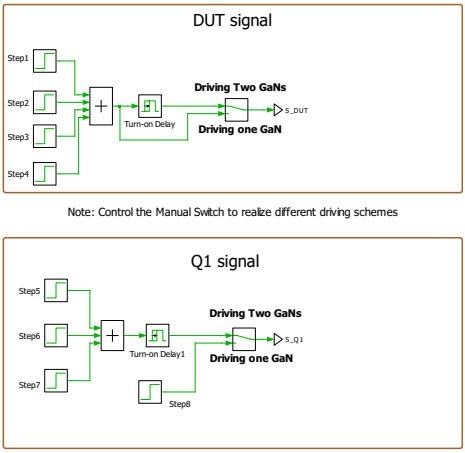


Figure 3.3: *DPT's switch signal generation block in PLECs*

3.2.5 Steady-State Continuous Switching

In SSCS, the DUT is continuously switched until it reaches the thermal steady state. However, for high current and voltage settings, the steady state is reached at extreme temperatures. Therefore, it was decided that it is important to investigate the voltage and current intervals at which SSCS remains a viable option. To address this, a PLECs simulation was done.

There are many possible setups for SSCS, the selected setup is shown in Figure 3.4. It was chosen because of its similarity in structure and setup with the DPT. Additionally, if this setup were to be realized, it would be relatively simple to implement in practice.

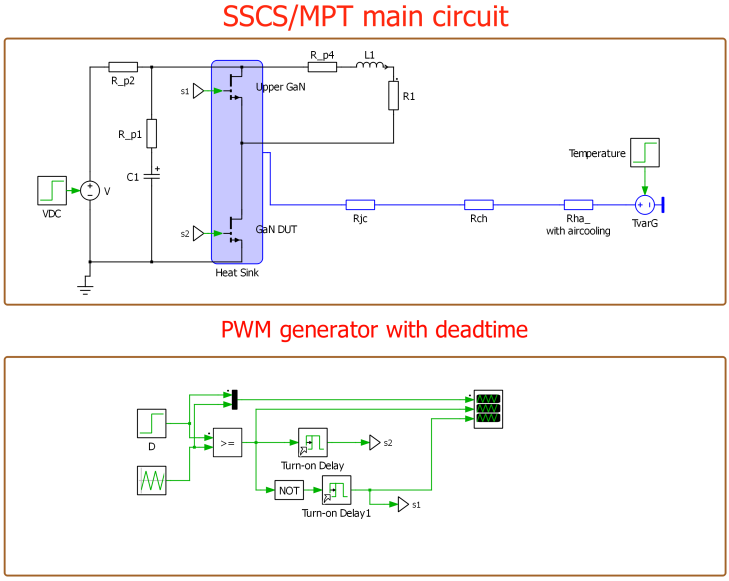


Figure 3.4: *PLECs Schematics of SSCS*

The principle of SSCS is similar to the synchronous buck converter without the capacitor. The two switches operate in a complementary way. Similarly to the synchronous buck converter in Section 2.2.1, the inductance and resistance values were determined using Equation (3.4). The calculated parameters are listed in Table 3.4. This resulted in a minimum load current of 10 A and 20% current ripple.

$$L \geq [\frac{D(1-D)V_{ds}}{\Delta i_L f_{sw}}]_{max} = 5\,\text{mH} \quad R = \frac{DV_{in}}{I_0} \in [0.67\,\Omega, 360\,\Omega] \tag{3.4}$$

To evaluate the testable current interval of SSCS without causing excessive heating, the worst-case drain-to-source voltage and duty cycle were selected and fixed.

Table 3.4: *SSCS Parameters*

Parameters	**Values**
Inductance L_1	5 mH
Resistance R_1	0.67 Ω – 360 Ω

To begin with, the duty cycle D does not affect the switching loss. However, the conduction loss for the DUT is affected by D. For the DUT (lower switch in Figure 3.4), the higher the D, the longer the conduction duration will be. Thus, the conduction loss for the DUT increases with D. For the worst-case thermal evaluation, in this simulation, the duty cycle D was fixed to 0.9. In addition, the switching frequency affects the switching loss but does not affect the conduction loss, thus the worst thermal case occurs at 100 kHz. The first simulation was conducted under 400 V and 100 kHz, to find the maximum current range for which SSCS could determine D-$R_{ds(on)}$. And the second evaluation focused on the commonly used switching frequency 10 kHz in the current electric motor drive system. The results are shown in Section 4.2.2.

3.2.6 Multi-Pulse Test

The difference between MPT and SCSS is that it only operates a few cycles, rather than reaching the thermal steady state. This is to achieve a trade-off between the temperature rise and measurement accuracy.

The same circuit layout and parameters as SSCS, shown in Figure 3.4, were selected. First, the number of possible switching cycles was determined. Neither too few nor too many cycles is acceptable. Too many cycles would cause overheating, while the inductor current I_{L} would not reach the desired test point if the cycles were too few. The time constant for I_{L} was calculated by the RL circuit time constant τ. And I_{L} was assumed to reach the steady state (within 99% of the final value) after 4.6τ, as in Equation (3.5).

$$R = \frac{DV_d}{I_{\mathrm{L}}} \quad \tau = \frac{L}{R} \quad T_s = 4.6\tau \tag{3.5}$$

MPT was also evaluated at the worst condition at 400 V. The frequency selection was analogous to SSCS, one at the worst case 100 kHz, another at the commonly used electric motor drive's switching frequency 10 kHz. For each current level, T_j was measured in PLECs when the current rose up to the steady state. The number of cycles was determined by making the T_j previously measured at the steady state increase up to 35 °C, according to the FOM. The selection of cycles and the thermal simulation results are shown in Section 4.2.3.

3.3 On-State Voltage Measurement Circuits

This chapter describes how the realized OVMC was selected, designed, implemented, and evaluated. A pre-study of OVMCs was performed and is presented in Section 2.3. The pre-study concluded that the most interesting circuit topologies were matched diode circuits and enhancement mode transistor circuits with a constantly biased supply. One circuit of each type was designed, and their performance was compared. The most promising circuit was selected for implementation. The selected figures of merit used for comparision are presented in Section 3.3.2 and the design requirements of the circuit in Section 3.3.3. The design methodology can be found in Section 3.3.4. The design of the transistor circuit is described in Section 3.3.5, and the matched diode circuit in Section 3.3.6. For the comparison of the circuits, see Section 3.3.7. The matched diode circuit was selected for implementation. The design of the PCB is described in Section 3.3.8. The assembled PCB can be seen in 3.3.9. Finally, the DC accuracy of the PCB was evaluated and is described in Section 3.3.10.

3.3.1 Pre-Study

A pre-study was performed to identify state-of-the-art OVMCs and is presented in Section 2.3. The majority of the material used in the pre-study was sourced from IEEE. From the pre-study, it was concluded that the most promising topologies were the matched diode circuits and constantly biased transistor circuits. The matched diode circuit was especially interesting since it does not require an IVT characterization of the blocking diode to compensate for its forward voltage drop during measurement. The constantly biased transistor circuit (TC) does not require any timing circuitry and is, therefore, much simpler, without any obvious trade-off in terms of performance compared to an actively switched TC.

3.3.2 Figures of Merit

Relevant figures of merit (FOMs) were identified through a literature review, including DC error, settling time, and bandwidth. The FOMs are summarized in Table 3.5. The definition of settling time, also commonly known as response time or dynamic response, varies between different OVMC studies. In this thesis, the definition from [34] was used, i.e., the time from that V_{ds} starts falling until the error of the measured value stays below 1 %.

Table 3.5: *FOMs found in the literature.*

Figure of Merit	Reference
DC error	[34, 46, 47]
Bandwidth	[34, 46, 47]
Settling time	[34, 35, 39, 42–47]

As presented in Sections 2.1.3 and 2.1.4, D-$R_{ds(on)}$ is a time-varying effect that we want to capture as accurately as possible. Therefore it was assumed that the

output of the OVMC should be a perfect copy of the input for all frequencies. Therefore, an ideal OVMC was assumed to be an ideal all-pass filter with linear phase in the measurement state. In other words, ideally, the OVMC should not attenuate or amplify the measured voltage — its magnitude response should be flat and infinite. Further, it should not mix frequency components, and as such, it should have a linear phase. Another aspect is the OVMCs output voltage range, which should be as small as possible to maximize the vertical resolution in the oscilloscope. The chosen FOMs are summarized in Table 3.6.

Table 3.6: *Selected FOMs.*

Figure of Merit	Purpose
Settling time	Measurement delay
DC error	DC accuracy
Bandwidth	AC accuracy
Flatness	
Phase linearity	
Vertical resolution	Oscilloscope measurement error

3.3.3 Design Requirements

The following requirements were assumed for the OVMC: The maximum $V_{ds(on)}$ of the devices listed in Table 1.1 is 2.1 V. Assuming a maximum 2x increase in D-$R_{ds(on)}$ and that the DUT will operate at 80 % of its maximum continuous current, the maximum input voltage of the OVMC during the measurement state was set to 4 V. Additionally, the circuit was designed to handle the maximum blocking voltage of the selected devices, which is 1200 V.

Table 3.7: *Summary of design requirements for OVMC.*

Requirement	Target
Blocking voltage	1200 V
Input voltage range	[0, 4] V

3.3.4 Design Methodology

This section describes the OVMC design methodology. One transistor circuit and one matched diode circuit were designed. Through simulation, different circuit topologies from the pre-study were investigated, and a clamping branch for each circuit type was designed. The results were compared using the figures of merit defined in Table 3.6. The most promising circuit was selected for implementation. Simulations were performed using LTSpice. To measure the circuits' performance, a transient, DC, and AC analysis was performed. The analysis settings are described below.

Transient Analysis

A transient analysis was conducted to measure the settling time and output voltage range. This output voltage range was then used to calculate the achievable vertical resolution of the oscilloscope. Additionally, surge currents and voltages in the circuits were observed to assess the stresses on components. A voltage source with a pulse was used to mimic the switching transients of a device, see Figure 3.5. The pulse parameters used are shown in Table 3.8. Worst-case values for the DUT off-state voltage, rise, and fall times were selected based on the values in Table 1.1. Duration of the transient analysis was selected to 300 ns. The worst-case settling time was assumed to be achieved for maximum input voltage, i.e., a $V_{\mathrm{ds(on)}}$ of 4 V.

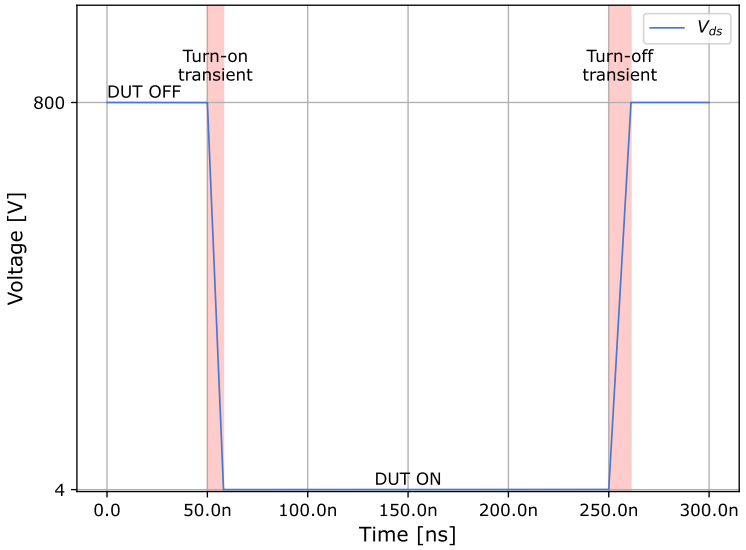


Figure 3.5: *Simulation of DUT switching. The DUT turn-on and turn-off transients are highlighted in red.*

Table 3.8: *LTSpice voltage source pulse parameter settings.*

Parameter	Value
Vinital	800 V
Von	4 V
Tdelay	250 ns
Trise	8 ns
Tfall	11 ns
Ton	300 ns
Tperiod	1 µs
Ncycles	1

DC Analysis

A DC analysis was used to measure the DC error of each circuit. The following settings were used:

Table 3.9: *LTSpice DC analysis settings.*

Parameter	Value
Type of sweep	Linear
Start value	0 V
Stop value	4 V
Increment	0.01

AC Analysis

An AC analysis was used to measure the bandwidth, flatness and phase linearity. The AC amplitude of the voltage source was set to 1 V and the AC analysis settings are presented in Table 3.10.

Table 3.10: *LTSpice AC analysis settings.*

Parameter	Value
Type of sweep	Decade
Number of points per decade	1000
Start frequency	10 kHz
Stop frequency	500 MHz

3.3.5 Design of the Transistor Circuit

This section describes the design process of the constantly biased transistor circuit (TC). From the pre-study, see Section 2.3.4, it was concluded that two key components of the TC required careful design: a low-pass filter to protect the gate supply from surge currents and voltage spikes, and a clamping branch (CB) to safeguard the oscilloscope from high voltage. Care was taken to ensure that the selected components operated within their specified limits. Various circuit designs were evaluated and iterated, with the most promising approach described in three iterations.

In the first iteration, a simple circuit, consisting solely of the blocking device and a Zener diode as clamping branch, was simulated to observe current stresses on the components. In the second iteration, a redesigned clamping branch was proposed to mitigate current stresses on the gate supply and Zener diode during switching transients. In the third iteration, the impact of minimizing the output node capacitance on circuit performance was investigated. It should be noted that only the most significant results are presented for each iteration.

Iteration 1

The simulated circuit can be seen in Figure 3.6. The SiC MOSFET C3M0350120D [57], manufactured by Wolfspeed, was chosen as a blocking transistor for its 1200 V rating, low $R_{ds(on)}$ and small C_j. Special attention was taken to ensure that the transistor's LTSpice model included parasitic inductances and capacitances so that parasitic oscillations and the frequency response were as accurate as possible. The bias voltage of Q_1 was set to 15 V, as recommended in the datasheet [57]. The minimum required Zener voltage to keep Q_1 off during the blocking state was calculated according to Equation (2.21), and off-the-shelf BZX84B15VLY was selected as Z_1, which has a Zener voltage of 15 V.

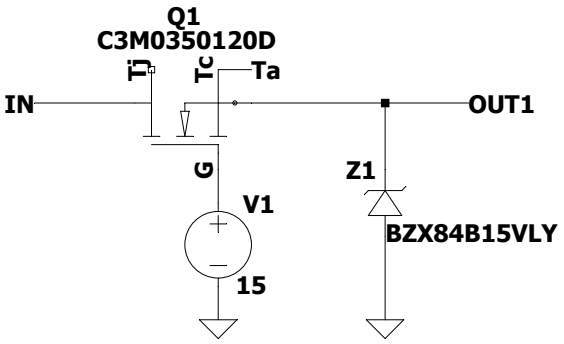
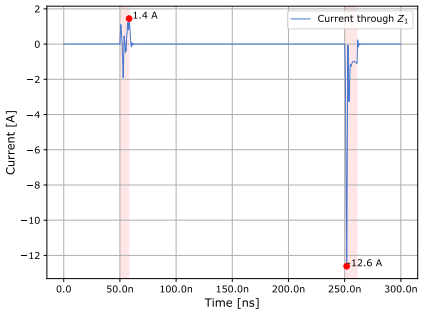
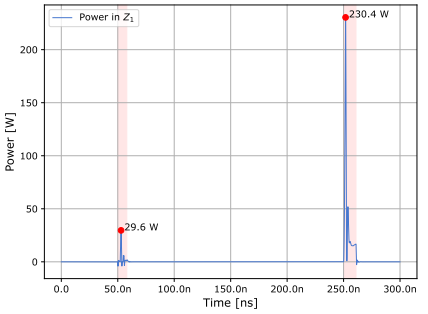


Figure 3.6: *Simulation setup for the 1st iteration of the transistor circuit design.*

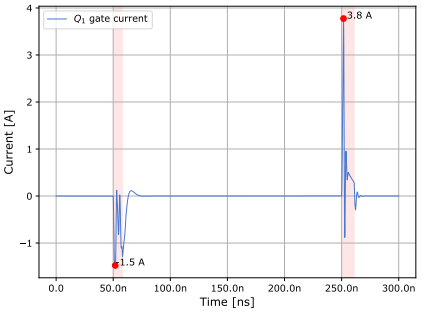
A transient analysis was performed to observe surge voltages and currents, and the most interesting results can be found in Figure 3.7. The peak current through Z_1 was measured to 1.4 A and 12.6 A during the turn-on and turn-off transients of the DUT, respectively, see Figure 3.7a. Similarly, the peak power in Z_1 was measured to 29.6 W and 230 W during the transitions, see Figure 3.7a. Maximum peak currents on the gate voltage supply were 1.5 A and 3.8 A, see Figure 3.7c. These peak values only persisted for nanoseconds, and thus the average power and current stresses were small. However, out of caution, a clamping branch that mitigates the stress on the gate supply and Z_1 was designed to ensure robustness.



(a) Z_1 *current stress.*



(b) Z_1 *power.*



(c) Q_1 *gate current stress.*

Figure 3.7: *Results from the transient analysis of the 1st iteration of the transistor circuit design. Current stresses on* Z_1 *and the gate supply were observed.*

Iteration 2

The resulting clamping branch can be seen in Figure 3.8. An RC filter was added to the gate to protect both the gate and supply from current and voltage spikes. To mitigate the current stresses on Z_1, the capacitors C_1 and C_2 were added in parallel to create a low impedance path for the transient currents. Schottky diodes were used to minimize the output node capacitance. PMEG2015EA [58] was selected for D_1, and PMEG2020EH [59] was selected for D_2 and D_3, which have repetitive current rating of 5.5 A and 7 A, respectively, and was thus rated for the current spikes presented in Figure 3.7a. A non-ideal capacitor was used for C_{1-3} to model current stresses as accurately as possible. To provide a low impedance path for as high frequencies as possible, the selection aimed to optimize for large capacitance in a small package to minimize ESL. Further, ceramic capacitors were considered for their low ESR. The capacitor GRT188C81C106ME13 [60] was selected, it provides a capacitance of 10 µF in a 0603 package. The value of R_1 was determined through simulation.

The results from the clamping circuit are presented in Figure 3.9. The current

through Z_1 had a peak amplitude lower than 60 mW and the peak power was below 800 mW, see Figures 3.9a and 3.9c, respectively. For the gate supply, the peak current was below 15 mA, see Figure 3.9b. It was concluded that the clamping circuit effectively mitigates the component current stresses. The remaining stresses were caused by very high-frequency components in the GHz range, and are thus difficult to filter out due to the ESL of C_{1-3}. When the capacitors were replaced with ideal ones, the stresses were essentially zero.

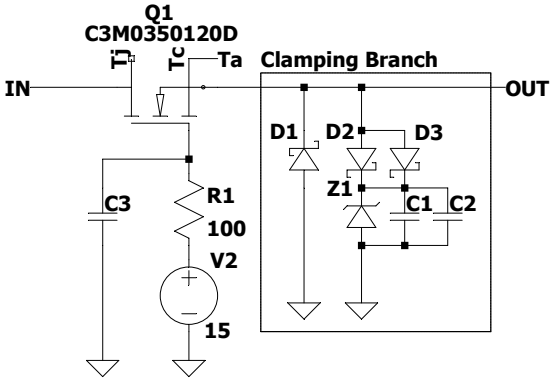
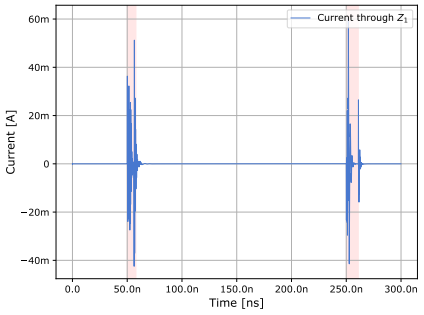
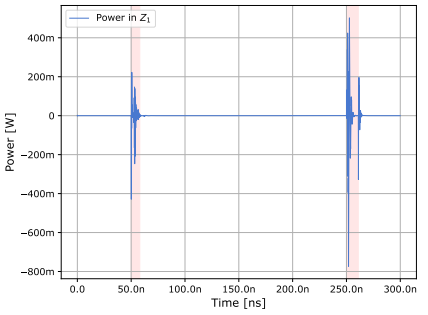


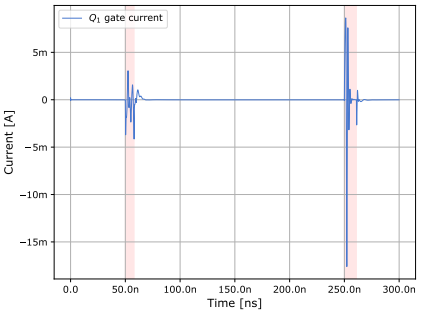
Figure 3.8: *Simulation setup for the 2nd iteration of the transistor circuit design.*



(a) *Z_1 current stress.*



(b) *Z_1 power.*



(c) *Q_1 gate current stress.*

Figure 3.9: *Results from the transient analysis of the 2nd iteration of the transistor circuit design. Current stresses on Z_1 and the gate supply were observed.*

Iteration 3

In the third iteration, more Schottky diodes were added in series with the existing ones to further minimize the output capacitance and see its effect on circuit performance. Four Schottky diodes were added in series and compared to the original clamping branch, see Figure 3.10. The results are presented in Figure 3.11. The additional Schottkys improved the response time with 2.5 ns. It was concluded that the extra complexity was not worth the performance improvement. The selected design of the TC was iteration 2, which is presented in Figure 3.8.

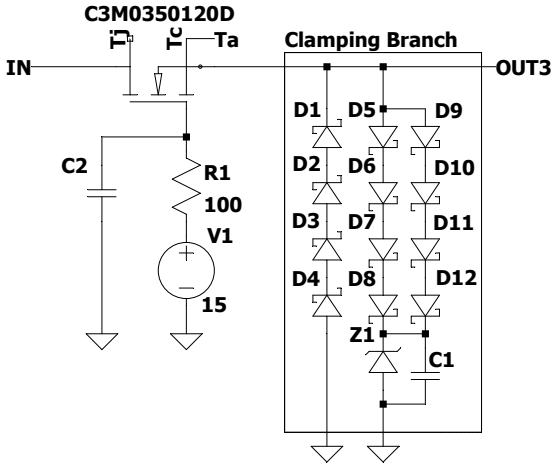
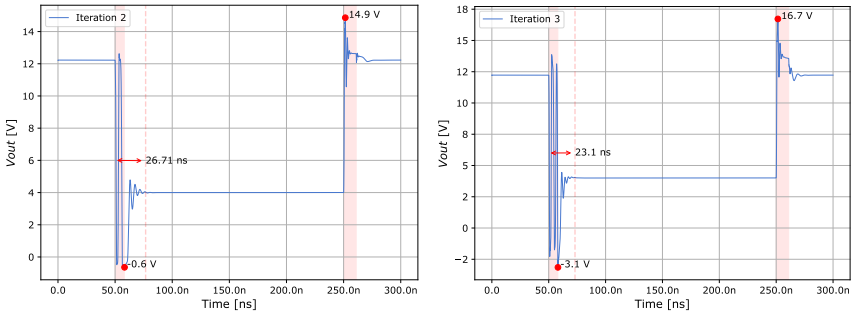


Figure 3.10: *Simulation setup for the 3rd iteration of the transistor circuit design.*



(a) *Settling time of iteration 2, 1x Schottky diode in series.*

(b) *Settling time of iteration 3, 4x Schottky diodes in series.*

Figure 3.11: *Settling time comparision when using 1x Schottky diode (iteration 2) in series versus using 4x Schottky diodes in series (iteration 3).*

3.3.6 Design of the Matched Diode Circuit

This section describes the design of a matched diode circuit across three iterations. In iteration 1, a clamping branch was designed using a single diode circuit, with a focus on optimizing the clamping branch. In iteration 2, matched diode topologies were compared, and the most promising topology was selected. In iteration 3, the final circuit was designed. As with the transistor circuit design, only the most significant results are presented for each iteration.

Iteration 1

A single diode circuit was used to observe current stresses in the output node and design a proper clamping branch. The schematic of the first iteration is presented in Figure 3.12. When selecting the blocking device, SiC Schottky diodes were considered because they do not suffer from reverse recovery. The SiC Schottky diode GB01SLT12-214 [61], manufactured by GeneSic, was selected as the blocking diode. It features a blocking voltage of 1200 V and a small junction capacitance (C_j). Special attention was taken to ensure that the diode's LTSpice model included parasitic inductances and capacitances so that parasitic oscillations and the frequency response were as accurate as possible.

A small biasing current I_b of 10 mA was selected because I_b will add to the drain current of the DUT and introduce an error in the on-state voltage measurement. A modified clamping branch from Figure 3.8 was used. PMEG2015EA [58] and PMEG2020EH [59] were selected for D_2 and D_3, respectively. Selecting the Zener diode, the test current I_{ZT} was considered so that the Zener diode operated well in the Zener region for the small I_b. The Zener voltage was chosen by Equation (2.24). AZ23C5V6 with a power rating of 300 mW, a Zener voltage of 5.6 V and a I_{ZT} of 10 mA was selected.

A transient analysis was performed, and the results are presented in Figure 3.13. The currents through the blocking diode D_1 were measured to 2.14 A and 3.88 A during the DUT turn-on and turn-off transient, respectively, see Figure 3.13a. The resulting current and power stresses on Z_1 can be seen in Figures 3.13b and 3.13c. The peak current was within 150 mA and peak power 800 mW. It was concluded that the clamping branch effectively reduces current stress on Z_1. Adding more capacitors in parallel with C_{1-2} could further reduce the current stresses. However, due to the short time of the current stresses, this design was concluded to be sufficient.

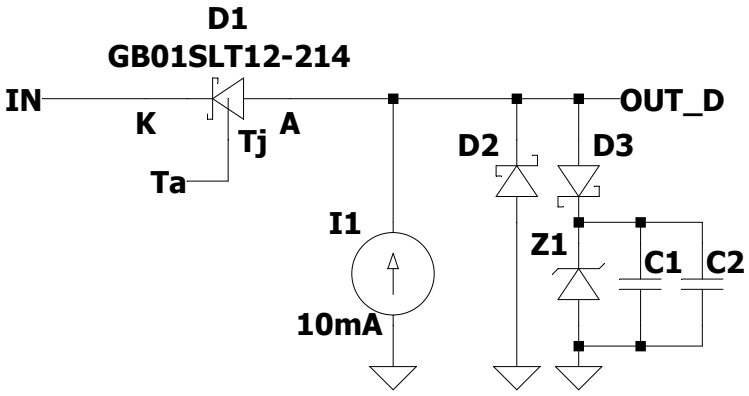
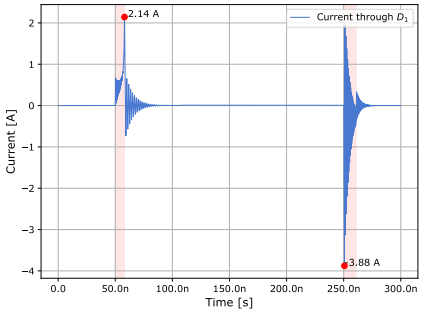
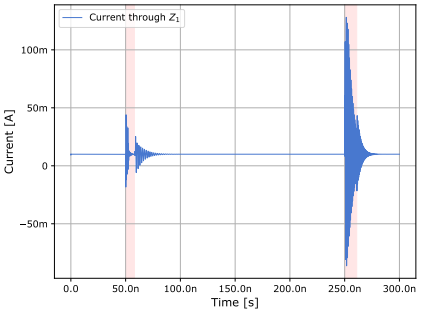


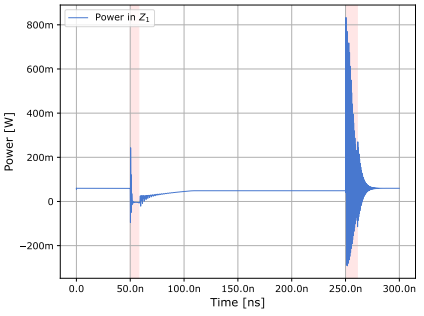
Figure 3.12: Simulation setup for the 1st iteration of the matched circuit design.



(a) D_1 *current stresses.*



(b) Z_1 *current stresses.*



(c) Z_1 *power stresses.*

Figure 3.13: Results from the transient analysis of the 1st iteration of the matched diode circuit design. Current stresses on Z_1 *and total induced current through* D_1 *was observed.*

Iteration 2

The matching diode circuits MDC1B, MDC2 and MDC3 were selected as candidate circuits for the design. The testbench of iteration 2 is presented in Figure 3.14. Extra features of the individual circuits, such as the reverse recovery acceleration branch in MDC3, were removed since they could be implemented in all circuits. The clamping branches of the original circuits were replaced by the designed clamping branch. MDC3 was assumed to be matched to an oscilloscope using 50 Ω output termination. AD8045 from Analog Devices was selected as an operational amplifier for all circuits. The gain of the circuits was selected as 1, 1, and 2 for MDC1B, MDC2, and MDC3, respectively. The size of the feedback resistors was chosen as recommended in the datasheet of AD8045. Ideal current sources were used to bias the circuits. A small I_b of 10 mA was selected. Biasing voltages of the operational amplifiers were selected through simulation to optimize the accuracy in the input range $[0, 4]$ V, selected voltages can be seen in Figure 3.14.

A transient analysis was performed to compare the settling time of the circuits. The results showed that MDC2 and MDC3 had almost identical settling times of 52.6 ns, while MDC1B had a longer settling time of 61.6 ns, see Figure 3.15a. A DC analysis was performed to observe the DC error of the circuits. The circuits showed similar absolute errors, see Figure 3.15b. The errors were of the same magnitude but had different zero crossings. The difference in error was attributed to the circuits having different feedback networks and supply voltages for the operational amplifier. MDC3 had the smallest relative error, see Figure 3.15c. An AC analysis was performed to observe bandwidth, flatness and phase linearity. The bandwidth of MDC1B, MDC2 and MDC3 was measured to 351.6 MHz, 184.1 MHz, and 392.6 MHz, respectively, see Figure 3.15d. MDC1B had the highest bandwidth, while MDC3 had a slightly smaller bandwidth but flatter magnitude response. Further, MDC3 has the most linear phase response, see Figure 3.15e. To summarize the results, the circuits showed very similar performance. However, based on the figures of merit, MDC3 showed the best overall performance and was selected as a candidate for the matched diode circuit.

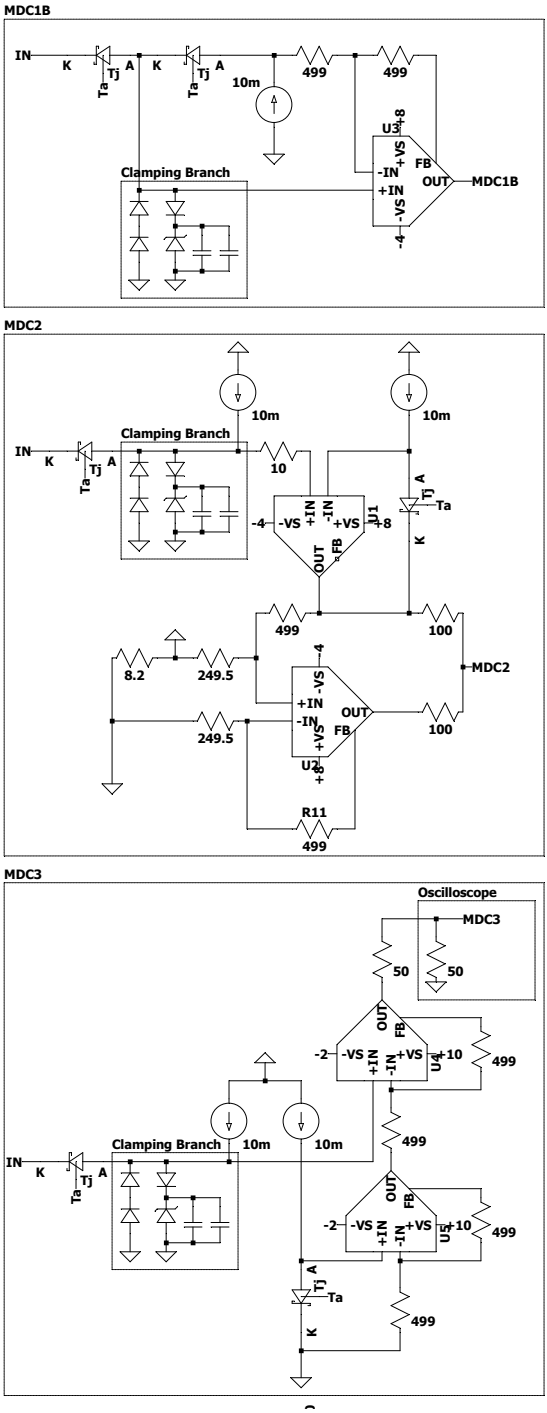
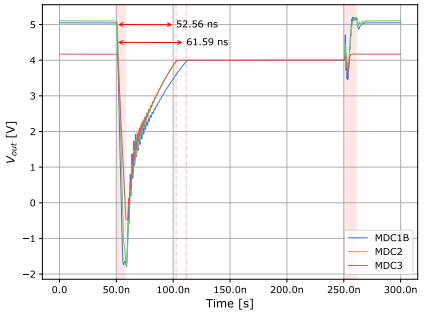
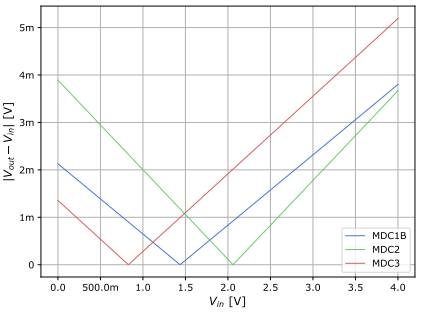


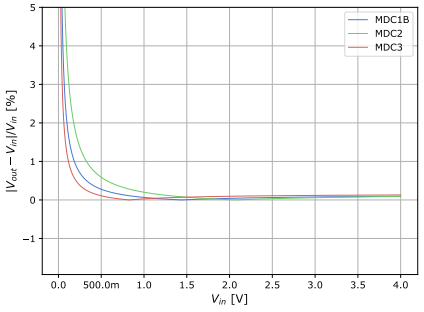
Figure 3.14: *Simulation setup for the 2nd iteration of the matched circuit design. The matched diode circuits MDC1B, MDC2, and MDC3 were compared.*



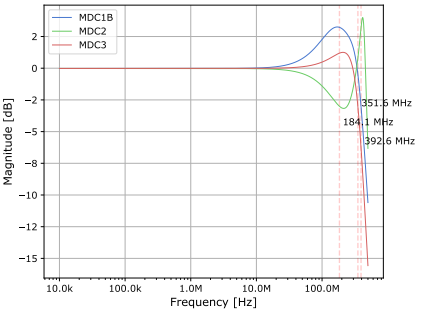
(a) Settling time.



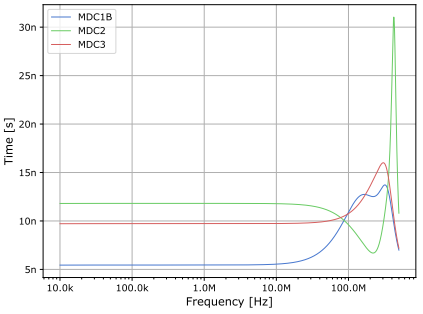
(b) Absolute error.



(c) Relative error.



(d) Magnitude response.



(e) Group delay.

Figure 3.15: *Results from the transient, DC, and AC analysis of the 2nd iteration of the matched diode circuit design.*

Iteration 3

The selected design of the matched diode circuit is presented in Figure 3.16. A full Wilson current mirror, also used in the original design of MDC3 [34], was implemented to replace the ideal current sources. To minimize the current mismatch in the mirror, the transistors should have a high and equal gain, see Section 2.3.3. BCV62C [62], a high gain ($\beta > 420$) matched BJT transistor pair, was selected. According to Equation (2.16), this gave a maximum error of

$$\left|1 - \frac{I_O}{I_R}\right| = \left|1 - \frac{1 + \frac{2}{420}}{1 + \frac{2}{420} + \frac{2}{420^2}}\right| \approx 0.24\,\% \tag{3.6}$$

To minimize the BOM, the current limiting resistor was set to the same value as the feedback resistors, 499 Ω, giving a I_b of 15.3 mA. The current mismatch between the legs of the current mirror was measured to 10 µA. Multiple Schottky diodes were added in series to reduce output node capacitance and to improve settling time. Blocking diode GB01SLT12-214 was unavailable for purchase at the vendor and replaced with GD02MPS12E [63], which is another 1200 V SiC Schottky diode with small C_j. The reverse recovery effect on settling time was investigated and the results can be seen in Figure 3.17. An acceleration voltage of 1.40 V was tested but it had little effect on the settling time, see Figure 3.17, hence it was decided that the settling time improvement was not worth the extra complexity.

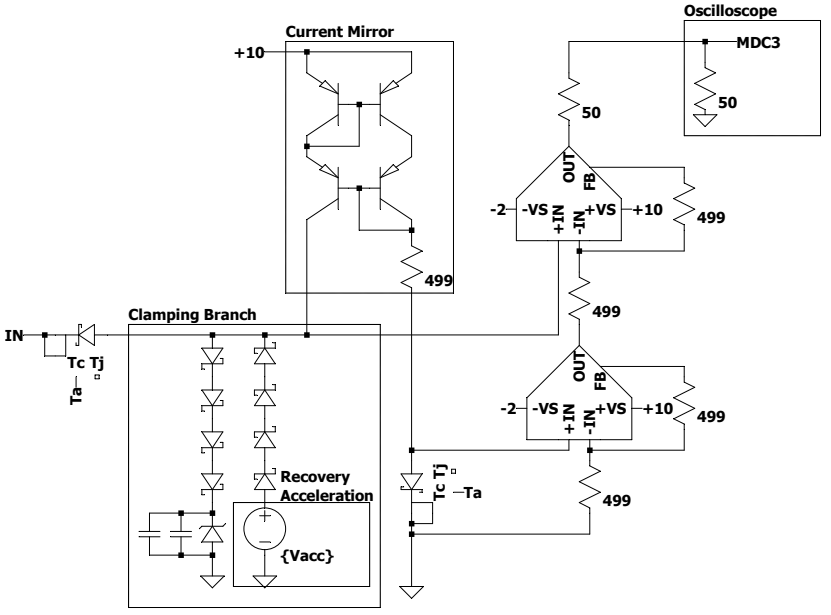


Figure 3.16: Simulation setup for the 3rd iteration of the matched circuit design.

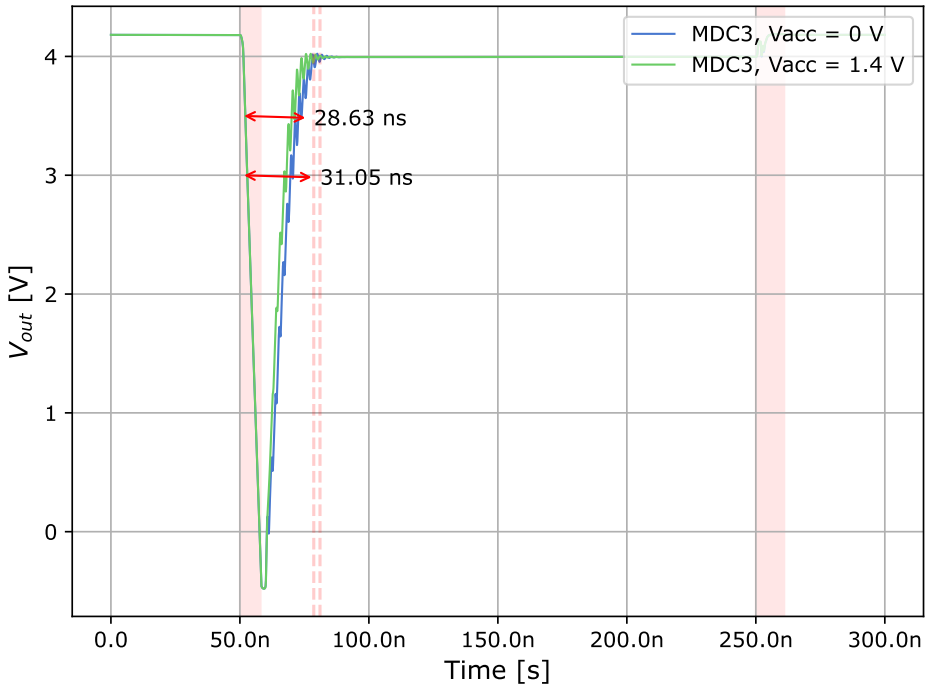


Figure 3.17: *Results from the transient analysis of the 3rd iteration of the matched diode circuit design. The effects of using a reverse recovery branch on the settling time were observed.*

3.3.7 Simulation of the Transistor Circuit and Matched Diode Circuit

In Sections 3.3.5 and 3.3.6, a transistor circuit (TC) and matched diode circuit (MDC) was designed. A simulation was performed to compare the two circuits' performance. The results are presented in Section 4.3.1 and summarized in Table 4.3.

The primary advantage of the TC was its exceptional DC accuracy, with a DC error of essentially zero across the entire input voltage range. In contrast, the absolute DC error of the MDC ranged between 0 and 5 mV over the same range. The MDC's relative DC error remained below 1 % for $V_{\text{in}} > 0.12\,\text{V}$. The TC's achievable vertical resolution was worse (3.8 mV) due to its larger output voltage range compared to the MDC (1.1 mV), assuming a 12-bit oscilloscope. Additionally, the TC demonstrated a faster settling time by 4.6 ns, though the MDC's settling time could be improved by increasing its biasing current. The MDC outperformed the TC in bandwidth, flatness, and phase linearity, as shown in Figures 4.8e and 4.8f.

To summarize, based on the results in Table 4.3, it was concluded that the MDC exhibited the best overall performance and was selected for implementation. It demonstrated sufficient accuracy, and its settling time could be further improved by increasing its biasing current.

3.3.8 PCB Design

This chapter describes how the final circuit and PCB were designed. The design was made using Altium Designer 24 [64]. The full schematic and BOM can be found in Appendix B.

Schematic

Most of the circuit had already been designed in Section 3.3.6. The remaining circuitry to design were the power supplies for the operational amplifiers and current mirrors, and to add connectors and decoupling capacitors.

The PCB was designed to be used with an external power board that contained the half-bridge circuitry. The high di/dt of GaN devices and parasitic inductances of the power loop were taken into consideration when designing the PCB. Isolated DC-to-DC converters were used to separate the ground of the measurement circuit from the noisy ground of the power loop, see Figure 3.18, where L_d and L_s are the wire inductance's of the device package, and $L_\mathrm{d,ext}$ and $L_\mathrm{s,ext}$ are the parasitic loop inductances. The plan was to connect the measurement PCB to the DUT on the power board by removing the solder mask at the DUT's drain and source terminals and soldering the PCB directly to the power board's traces. This would minimize the wire length between the PCB and the DUT, reducing parasitic loop inductances in the measurement circuit. The DC-to-DC converters TMR 4-2413 [65] and TMV2405S [66], rated for a minimum of 1600 VDC, where selected to generate +15 V and −5 V, respectively, see Figure 3.19. The variable low-dropout (LDO) regulators LM317 [67] and LM337 [68] were selected to filter the voltages generated by the DC-to-DC converters and generate clean +10 and −2 voltages, see Figure 3.20. The value of the program resistors of the LDOs were selected as given in the data sheets, 240 Ω for LM317 and 120 Ω for LM337. The formulas in the data sheets were used to select the other resistors so that the desired output voltages were achieved. Reverse current protection diodes were also added as recommended.

In the clamping branch, one extra Zener diode and two extra capacitors were added so that the decoupling could be tweaked and the power rating could be increased if needed, see Figure 3.21. Further, test points were added for all supply voltages, and in- and outputs. SMA connectors were added for the input and output for easy connection to an oscilloscope or vector network analyzer. Throughout the design, resistors with a tolerance of 0.1 % and power rating of 0.1 W were used. Decoupling capacitors for the DC/DC converters, LDOs and OP-AMP were added as described in the datasheets.

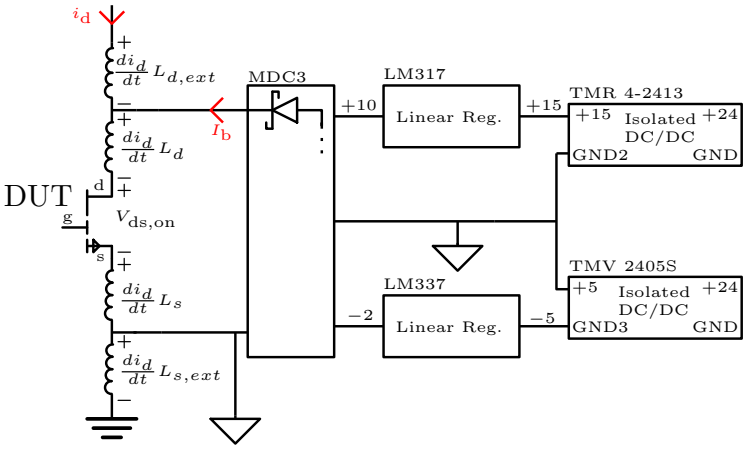


Figure 3.18: *Separation of the power loop ground and the measurement circuit ground.*

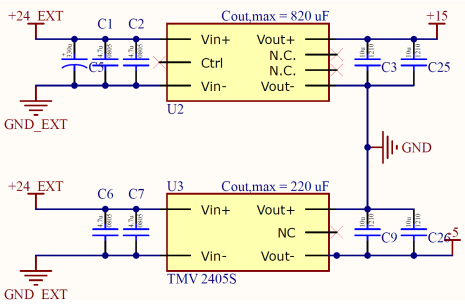


Figure 3.19: *DC-to-DC converters with decoupling capacitors.*

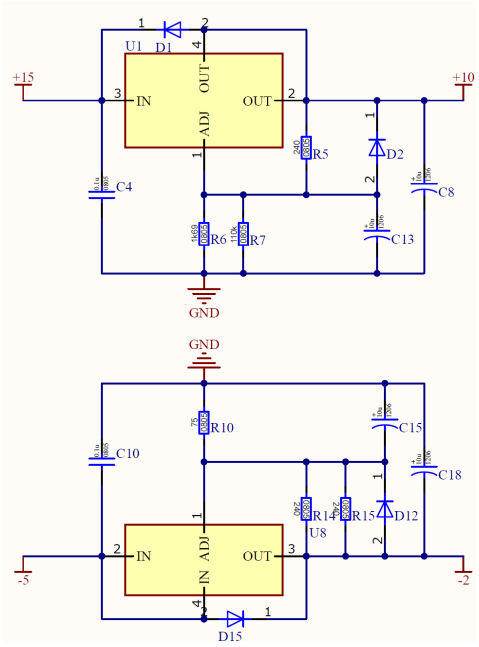


Figure 3.20: *Adjustable low-dropout regulators.*

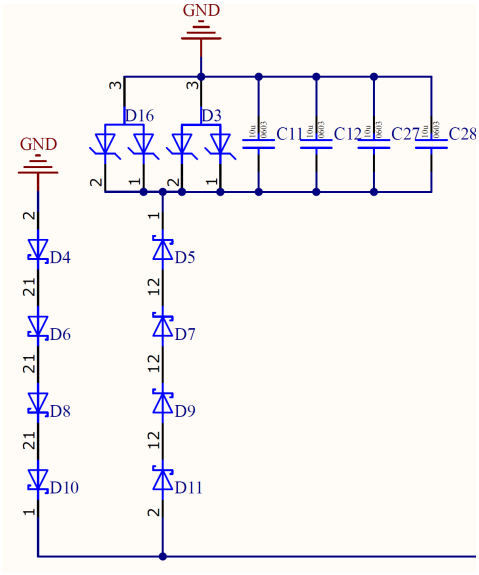


Figure 3.21: *Clamping branch.*

Layout

For the stack up, a simple two-layer PCB with an 18 µm copper thickness was used. The PCB was produced by Cogra Pro AB [69]. There was plenty of room on the PCB and wide traces of 1 µm could be used to minimize stray inductance and resistance. For narrow spaces, traces of 0.5 µm were used. The hole size of the vias was selected to 0.5 mm, the width of the pad was calculated to 1 mm, which fulfills IPC2221 class 3 [70]. In other words, the vias could be produced even if the worst drill tolerances were assumed.

All components were mounted in the top layer. Signal and power traces were routed on top layer, see Figure 3.22. The ground connections were put on the bottom layer, one pour was used for each ground, see Figure 3.23. The power flow is from top to bottom, while the signal flow is from the left to the right. An overview of component placement can be seen in Figure 3.24.

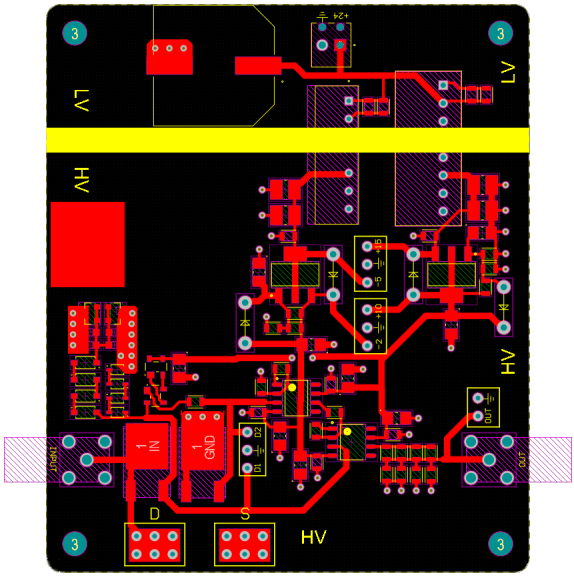


Figure 3.22: *Layout top layer.*

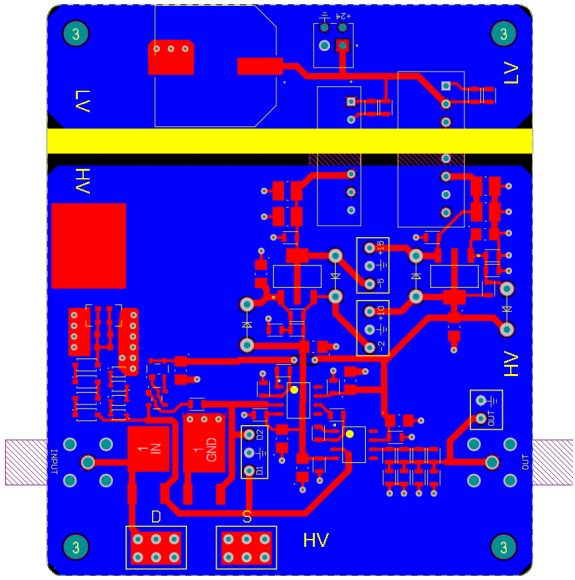


Figure 3.23: *Layout bottom layer.*

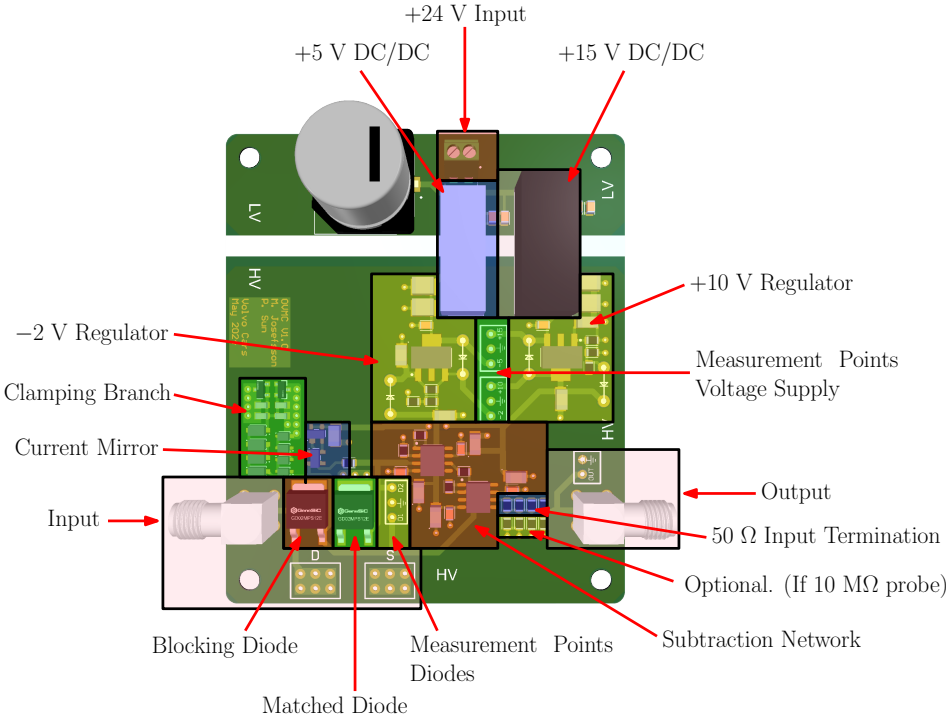


Figure 3.24: *Annotated overview of the PCB.*

3.3.9 PCB Assembly

When the PCB was received, the SMD components were soldered using solder paste and a reflow oven, and through-hole components were hand-soldered. The fully assembled PCB is presented in Figure 3.25.

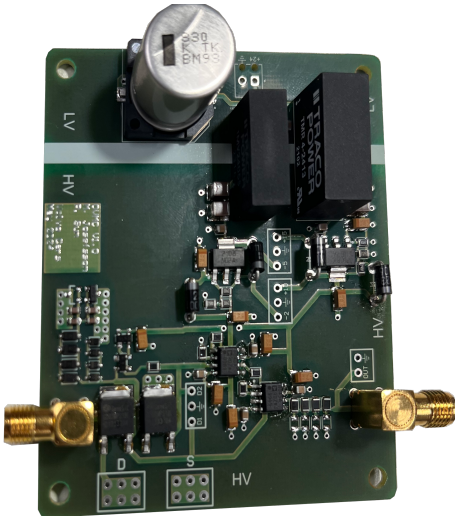


Figure 3.25: *Assembled PCB.*

3.3.10 PCB Evaluation

This section describes evaluation of the assembled PCB. The used lab equipment can be seen in table Table 3.11.

Description	Instrument
Oscilloscope	Lecroy Waverunner 620Zi
Multimeter	Fluke 117
Bench Supply	Manson EP-613
Bench Supply	Aim-TTi instruments EL302RT

Table 3.11: *Lab equipment used during evaluation of PCB.*

After the PCB was assembled, the operation of the power supply circuitry was verified by measuring the +10 V and −2 V test points on the PCB with a multimeter. The values were measured to 10.01 V and −2.039 V. The standby current consumption was measured to 70 mA, when the input voltage was 24 V, by observing the bench supply.

The DC error of the PCB was evaluated using the setup in Figure 3.26. A schematic of the setup is presented in Figure 3.27. The input and output of the

PCB was connected to the oscilloscope using the PCB's SMA connectors, SMA to BNC-adapters, and BNC cables. A 1 MΩ input impedance was used for measuring V_{in} and 50 Ω for measuring V_{out}, see Figure 3.27. The Aim-TTi bench supply was used to simulate the on-state voltage of the DUT. Connecting the bench supply directly to the PCB caused it to malfunction — the supply's voltage became fixed and could not be adjusted. The cause was believed to be that the bench supply could only source current, while the current mirror on the PCB also functioned as a current source. A workaround was implemented by adding a resistor, as shown in Figure 3.27. With the resistor in place, the bench supply sourced current and operated normally when

$$V_{\text{s}} > R_1 I_{\text{b}}. \tag{3.7}$$

To simulate small $V_{\text{ds(on)}}$ values, R_1 had to be small, as shown in Equation (3.7). This resulted in the power dissipated in the resistor exceeding its rated maximum power for higher V_{s}. To address this issue, the upper voltage bound for the resistor was calculated as

$$V_{\text{s}} < \sqrt{PR_1}, \tag{3.8}$$

where P is the power limit of the resistor. The input voltage was varied in steps of 100 mV and the resistance was varied to fulfill Equations (3.7) and (3.8). The voltage of the bench supply was adjusted until the oscilloscope's measured mean value of V_{in} came close to a multiple of 100 mV, then it was compared to the measured mean value of V_{out}. This process was repeated until the entire input range $[0, 4]$ V had been measured. Higher input voltages up to 10 V were tested to verify the functionality of the clamping branch. The vertical sensitivity of the oscilloscope was set to 200 mV to achieve a measurement with good resolution. The observed mean value could sometimes flicker with 1 to 2 mV. When that happened, the value that gave the worst accuracy was noted. The raw measurement data and used resistor values can be found in Table B.1.

Unfortunately, only the DC accuracy of the PCB could be evaluated. The plan was also to evaluate the frequency response of the PCB using a vector network analyzer and perform actual $V_{\text{ds(on)}}$ measurements in a half-bridge. However, the vector network analyzers at Volvo were not accessible during the evaluation period, and no power board could be attained.

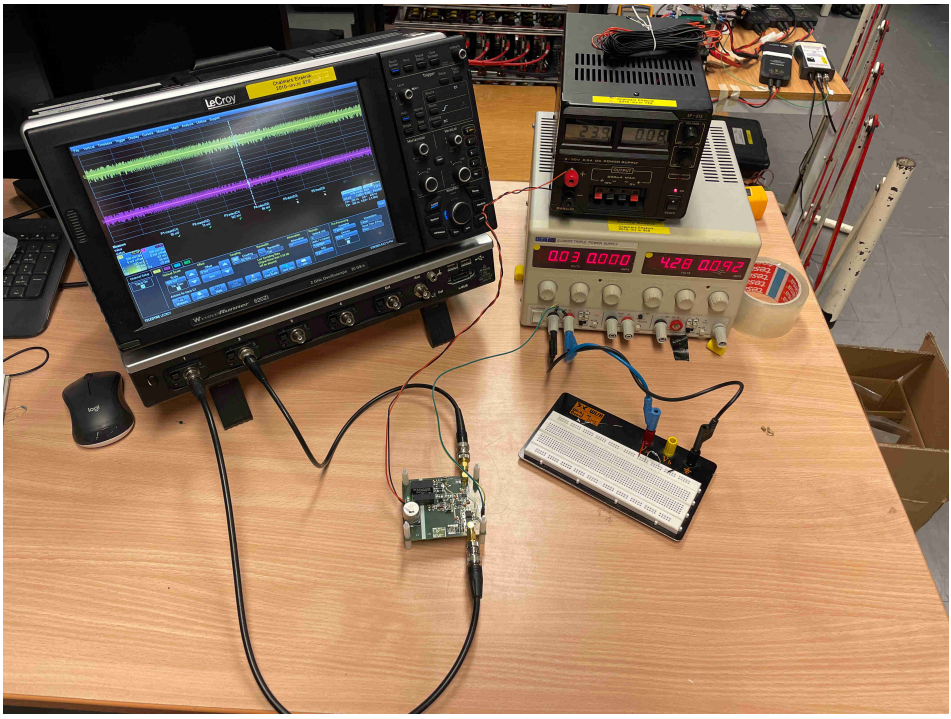


Figure 3.26: *Lab setup for evaluating accuracy.*

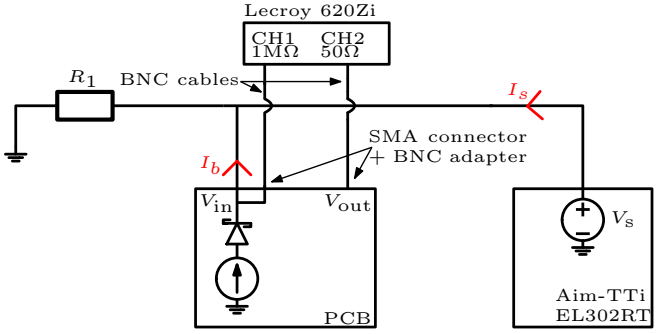


Figure 3.27: *Schematic of lab setup for evaluating accuracy.*

4

Results

This chapter presents the result of the investigations conducted in Chapter 3. First, the literature review's result on the parameters' effect on D-$R_{ds(on)}$ is presented in Section 4.1. Then, the results of the measurement methodologies are presented in Section 4.2. Finally, the simulation results of the designed on-state voltage measurement circuits and evaluation of the realized PCB are presented in Section 4.3.

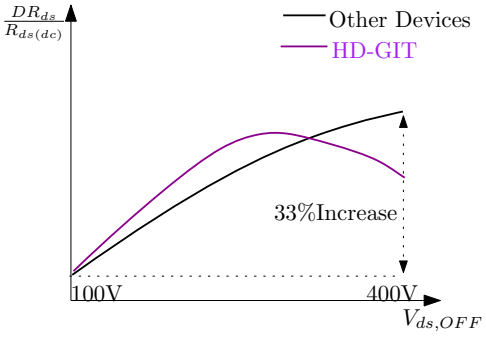
4.1 Operational Parameters' Effect on D-$R_{ds(on)}$

The operational parameters, such as V_{ds}, I_d, f_{sw}, D, T_j, and the effects of R_g, are summarized from the literature and compiled in this section. It should be noted that some sources do not specify the device structures or part numbers. In this review, the effects of device structures on D-$R_{ds(on)}$ are considered only for V_{ds} and f_{sw}.

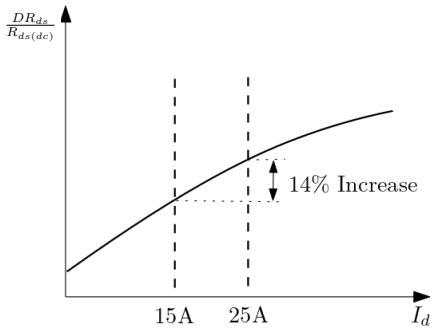
Table 4.1 summarizes the effects of the operational parameters, while Figure 4.1 shows a more detailed illustration of how each operational parameters affect D-$R_{ds(on)}$. A discussion of the results and the related analysis is presented in Section 5.1.2.

Table 4.1: *Different operating parameters' effects on D-$R_{ds(on)}$ during hard switching*

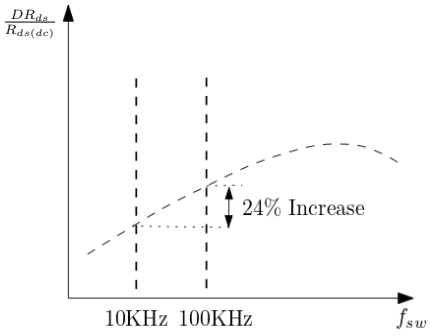
Items	Description	Ref
V_{ds}	D-$R_{ds(on)}$ has a nonmonotonic relation with the V_{ds} for the HD-GIT and monotonic increase for other GaN HEMT	[16][12][28]
I_d	D-$R_{ds(on)}$ increases in both hard and soft switching with the increase of drain current	[12][28]
f_{sw}	D-$R_{ds(on)}$ increases monotonically over a switching frequency up to of 2 MHz	[29][71]
D	Decreasing D-$R_{ds(on)}$ over increased D. The device has a longer on time, therefore a shortened off trapping time and prolonged detrapping time.	[28]
T_j	More complex, the dependence between D-$R_{ds(on)}$ on T_j maybe device-specific and impacted by switching schemes.	[16]
R_g	A higher value of D-$R_{ds(on)}$ is observed with a bigger turn-on gate resistance R_g, especially at the high DC-link voltage and high load current conditions	[72]



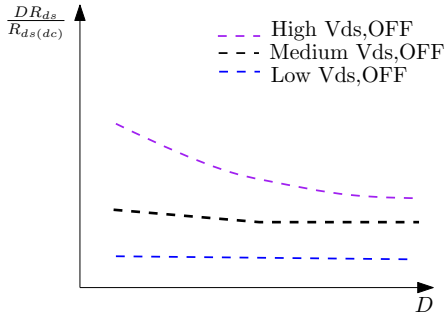
(a) V_{ds}*'s effect on D-*$R_{ds(on)}$ *[28]*



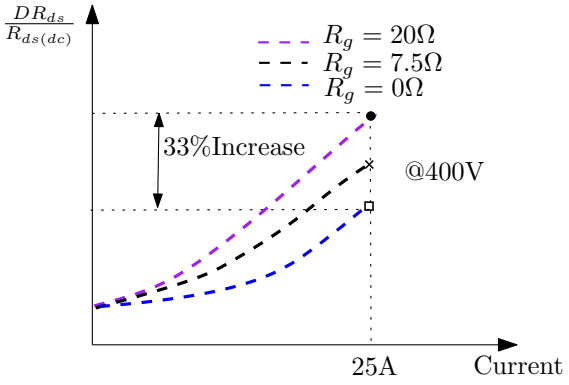
(b) I_d*'s effect on D-*$R_{ds(on)}$ *[73]*



(c) f_{sw}*'s effect on D-*$R_{ds(on)}$ *[28, 71]*



(d) D's effect on D-$R_{ds(on)}$ *[28]*



(e) R_g*'s Effect on D-*$R_{ds(on)}$ *[28]*

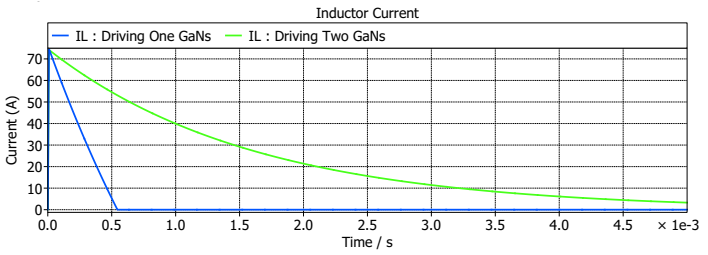
Figure 4.1: *Operational parameters' effects on D-*$R_{ds(on)}$

4.2 Measurement Methodologies

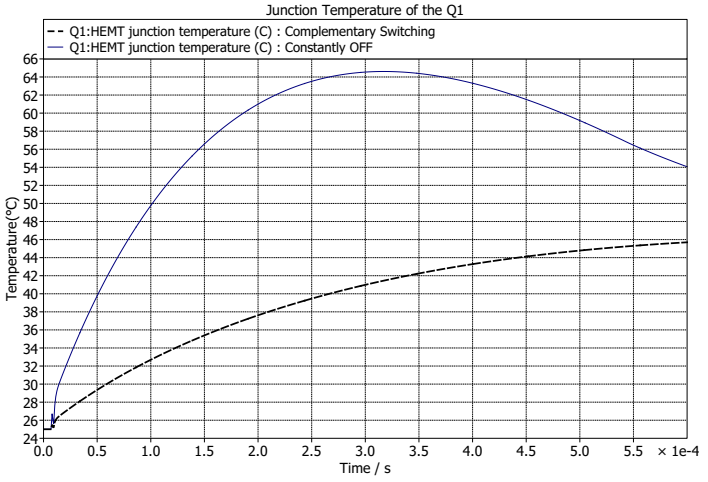
This section summarizes the methodology evaluation. The simulation results for DPT, SSCS, and MPT are presented in Section 4.2.1, Section 4.2.2, and Section 4.2.3 respectively. The related discussions on the results are presented in Section 5.2.

4.2.1 Evaluation of DPT

DPT evaluation was conducted at the worst thermal condition: 400 V and 60 A, for two DPT schemes: switch-switch and switch-to-diode. The evaluation results for DPT are shown in Figure 4.2. And the discussion on the results is presented in Section 5.2.2.



(a) *I_L of the Two Switching Patterns*



(b) *Junction Temperature of Q_1*

Figure 4.2: *Comparison of the two switching patterns in DPT. The comparison considers the inductor current I_L and the junction temperature rise*

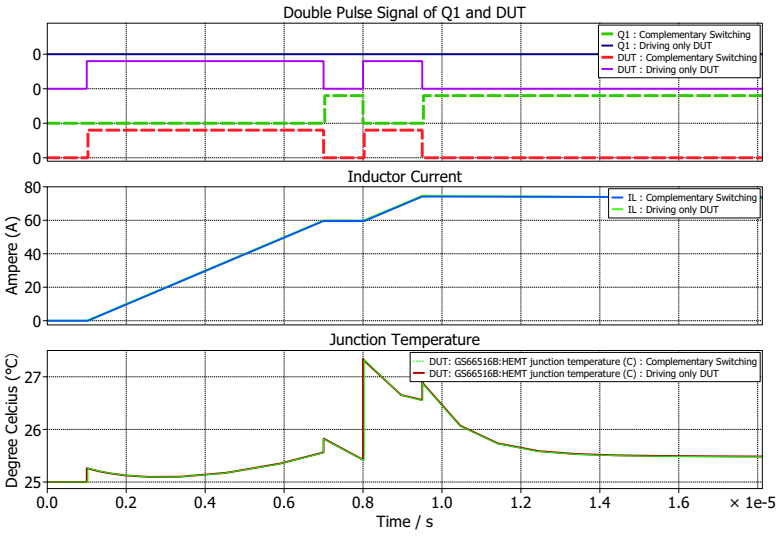


Figure 4.3: *Junction temperature variation of DUT during DPT*

4.2.2 Evaluation of SSCS

The result for the first SSCS evaluation (400 V, 100 kHz, $D = 0.9$) is shown in Figure 4.4. And the result for the second evaluation (400 V, 10 kHz, $D = 0.9$) is shown in Figure 4.5.

The designed minimum current is 10 A for SSCS, however, at this current level, the steady-state temperatures for both 10 kHz and 100 kHz go beyond 35 °C. Therefore, for SSCS, the minimum current for evaluation is reset to 1 A, with the inductance changed to 50 mH to ensure the same current ripple according to Equation (3.4).

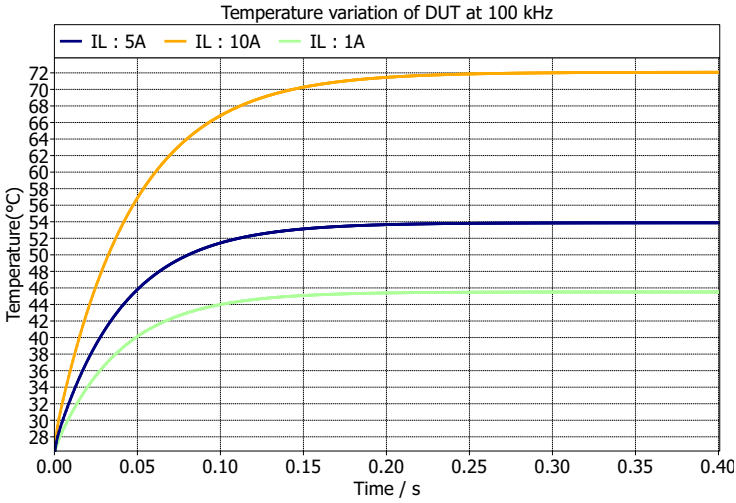


Figure 4.4: *SSCS Evaluation : DUT T_j's variation with time and the load current I_L (*1 A,5 A,10 A*). The evaluation was done under* 400 V, 100 kHz, D = 0.9.

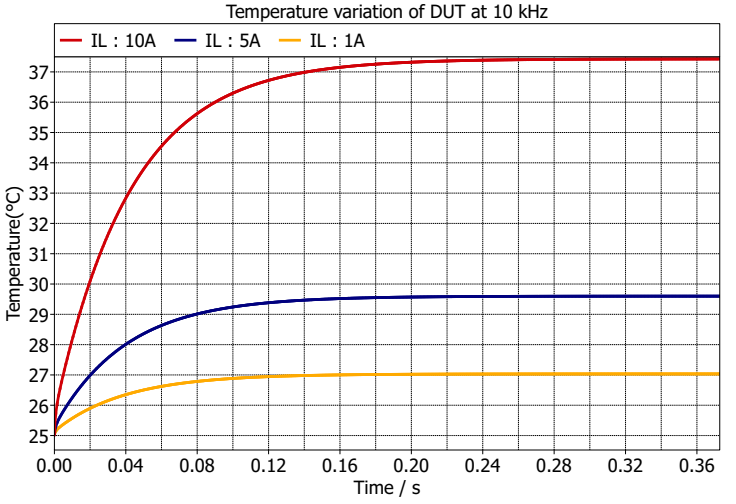


Figure 4.5: *SSCS Evaluation : DUT T_j's variation with time and the load current I_L (*1 A,5 A,10 A*). The evaluation was done under* 400 V, 10 kHz, D = 0.9.

4.2.3 Evaluation of MPT

Table 4.2 shows the simulation results for MPT, and Figure 4.6 illustrates this process in a time-scale plot.

Table 4.2: *Evaluation Results for MPT at* 400 V, $D = 0.9$

$I_L(A)$	$R(\Omega)$	4.6τ(ms)	T_j (10/100 kHz)
10	36	0.6389	25.5/27.1°C
20	18	1.2778	**27.5/30.6**°C
30	12	1.9167	**31.7**/36.9°C
40	9.0	2.5556	39.3/47.5°C
50	7.2	3.1944	51.9/65.3°C
60	6.0	3.8333	73.0/96.1°C

The number of MPT cycles is determined by satisfying the maximum T_j requirement for load currents of 20 A and 30 A, as illustrated in Figure 4.6. At 20 A and 10 kHz, T_j reaches 35 °C after 80 steady-state cycles. Similarly, T_j reaches 35 °C after 180 steady-state cycles at 20 A, 100 kHz, and after 15 steady-state cycles at 30 A, 100 kHz.

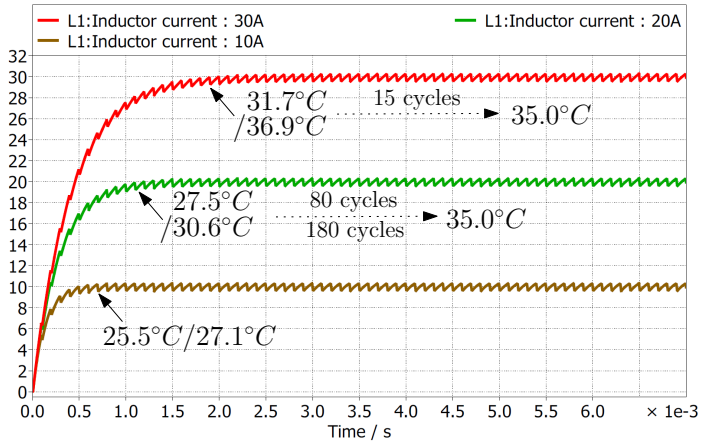


Figure 4.6: *Evaluation results for MPT. The load current curves are for* 100 kHz *switching frequency. The numbers under each curve represents T_j when load current reaches its maximum. The left number to the slash represents T_j for* 10 kHz *while the right represents the result for* 100 kHz.

4.3 On-State Voltage Measurement Circuits

This chapter contains the results for the on-state voltage measurement circuits (OVMCs). Simulation results comparing the designed transistor circuit and the matched diode circuit are presented Section 4.3.1. The results from the evaluation of the realized PCB are presented in Section 4.3.2.

4.3.1 Simulation of the Transistor Circuit and Matched Diode Circuit

This chapter presents the results of the designed transistor circuit (TC) and the matched diode circuit (MDC). The results are summarized in Table 4.3, and the simulation setup is shown in Figure 4.7. A transient, AC, and DC analysis were performed using LTSpice, with the configuration of these analyses outlined in Section 3.3.4. Graphs showing the results are displayed in Figure 4.8.

Table 4.3: *Summary of simulation results for the transistor circuit (TC) and matched diode circuit (MDC).* † *Presented in terms of the ranking between the TC and MDC.* ‡ *Assuming an oscilloscope with an ENOB of 12, it is calculated by dividing the output voltage range by* 2^{12}.

FOM	TC	MDC
Settling time	26.5 ns	31.1 ns
Absolute DC error	≈ 0	0 - 5 mV
Relative DC error	≈ 0	< 1 % for $V_{\text{in}} \geq 0.12$ V
Bandwidth	145.2 MHz	538.8 MHz
Flatness †	2	1
Phase linearity †	2	1
Vertical resolution‡	3.8 mV	1.1 mV

Upon reviewing the results, it is observed that the TC has a faster settling time compared to the MDC, 26.5 ns versus 31.1 ns, see Figure 4.8a. Additionally, the output voltage range is larger for the TC than the MDC, 15.8 V versus 4.7 V. The vertical resolution is calculated as 3.8 mV for the TC and 1.1 mV for the MDC, respectively.

Regarding accuracy, the TC exhibits an absolute error smaller than 3 µV (see Figure 4.8b), whereas the MDC's absolute error remains below 1.5 mV for input voltages in the range of 0 – 1.75 V, increasing to 5 mV for higher input voltages. Consequently, the relative error stays below 1 % for input voltages above 123 mV, as shown in Figure 4.8d.

The magnitude response in Figure 4.8e indicates that the TC and MDC have bandwidths of 145.2 MHz and 538.3 MHz, respectively. Additionally, the magnitude response of the MDC is flatter than that of the TC. As shown in Figure 3.15e,

the group delay of the MDC remains constant over a wider frequency range compared to the TC, indicating a more linear phase.

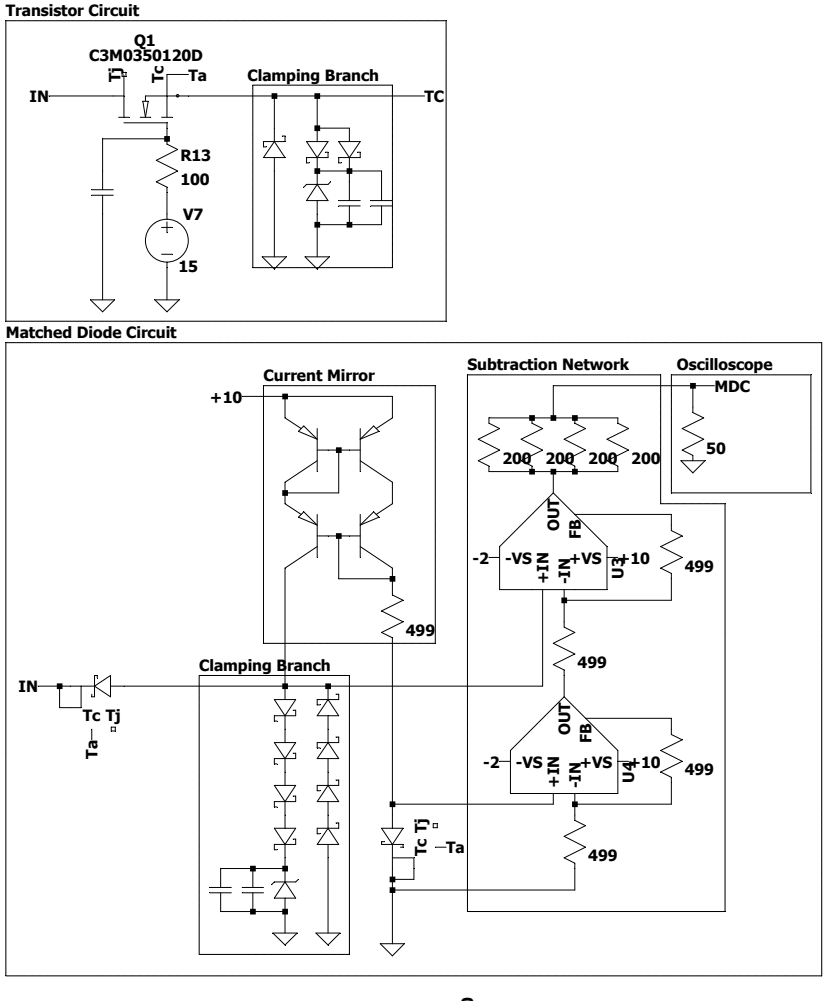
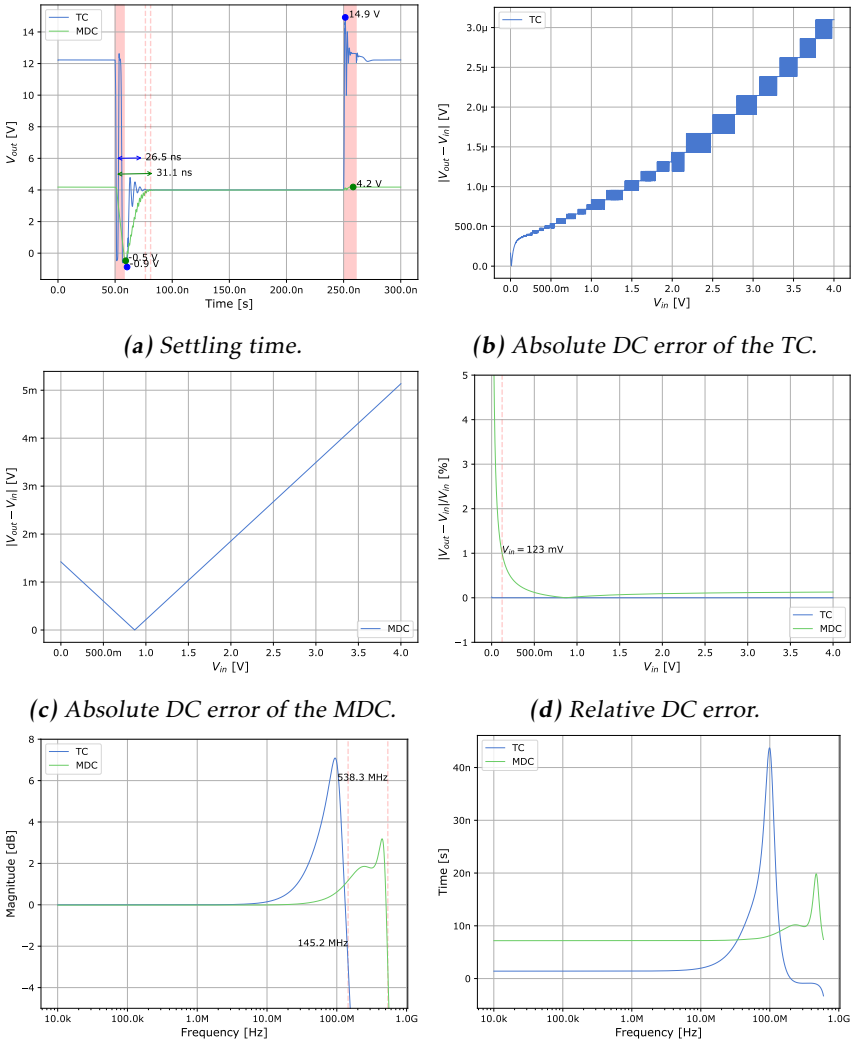


Figure 4.7: *Simulation setup for the comparison of the transistor circuit (TC) and the matched diode circuit (MDC).*



(a) *Settling time.*

(b) *Absolute DC error of the TC.*

(c) *Absolute DC error of the MDC.*

(d) *Relative DC error.*

(e) *Magnitude response.*

(f) *Group delay.*

Figure 4.8: *Results from the transient, DC, and AC analysis of the transistor circuit (TC) and the matched diode circuit (MDC).*

4.3.2 PCB Evaluation

This chapter presents the results of the DC error evaluation for the PCB, based on the setup outlined in Section 3.3.10. The maximum absolute DC error is 8 mV, as shown in Figure 4.9. No apparent relationship between the input voltage and the achieved accuracy is observed. The relative error remains below 1 % for input voltages above 0.32 V, as indicated in Figure 4.10. In Figure 4.11, the input voltage is swept from 0 to 10 V, and the output voltage is clamped at 4.2 V.

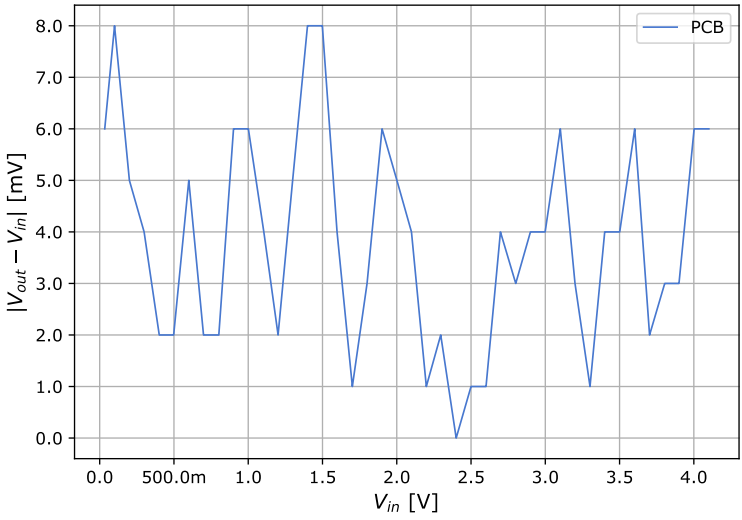


Figure 4.9: *Absolute DC error of PCB.*

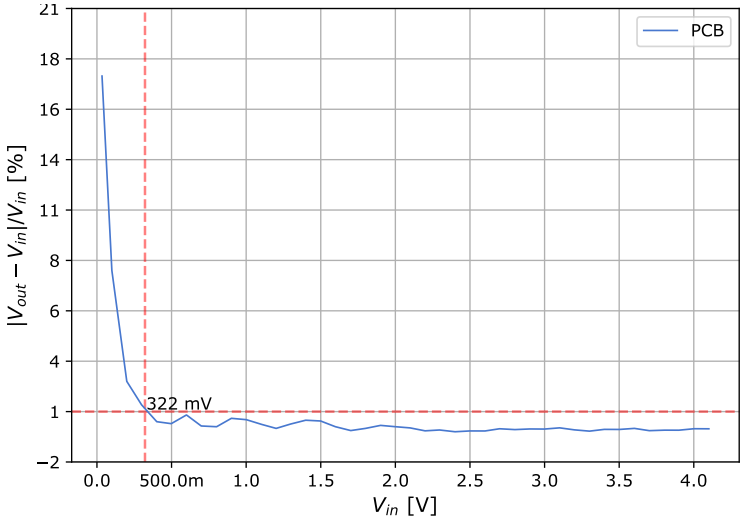


Figure 4.10: *Relative DC error of PCB.*

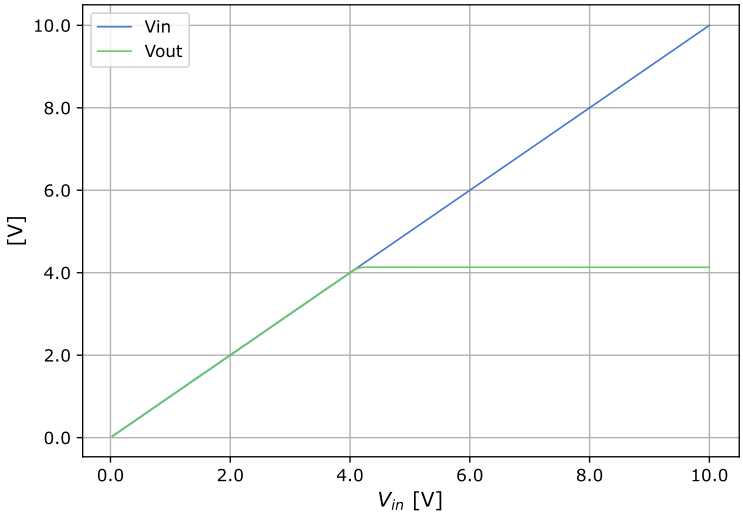


Figure 4.11: *Verification of clamping functionality of the PCB.*

5

Discussion

This chapter discusses the methods and results of each research question introduced in the first chapter and suggestions for future work related to these questions.

5.1 Operational Parameters' Effect on D-$R_{ds(on)}$

This section discusses the effects of operational parameters on D-$R_{ds(on)}$. Section 5.1.1 outlines the method, with an analysis of the results presented in Section 5.1.2. Finally, Section 5.1.3 discusses potential future work.

5.1.1 Method

Given the time constraint of the project, performing a literature review was the only feasible way to understand each parameter's effect on D-$R_{ds(on)}$. Knowing how the parameters may affect D-$R_{ds(on)}$ also helped evaluate the measurement methodologies. Most of the material was sourced from reputable journals such as IEEE and doctoral theses.

5.1.2 Result

There are many operational parameters that affect electron trapping and its efficacy. The most common parameters are the drain-source voltage (V_{ds}), the drain current (I_d), the switching frequency(f_{sw}), the duty cycle (D), the operation mode (hard switching or soft switching), the junction temperature (T_j), and the turn-on gate resistance R_g.

For V_{ds}, there is a 33% increase of D-$R_{ds(on)}$ when V_{ds} increases from 100 V to 400 V for the device tested in [28], since a higher V_{ds} increases the hot electron trapping and off-state trapping. However, for HD-GIT device, it shows a non-monotonic increase with increasing V_{ds}. This is because the HD-GIT device features hole injection at high V_{ds}. The effect of V_{ds} is illustrated in Figure 4.1a.

For I_d, there is an 14% increase when I_d increases from 15 A to 25 A [73], since it leads to a stronger V-I overlap, which increases the hot-electron trapping. The literature review found that only a few sources cover high current applications, i.e., up to 60 A. The effect of I_d is illustrated in Figure 4.1b.

For the switching frequency f_{sw}, D-$R_{ds(on)}$ increases monotonically over a switching frequency up to 2 MHz [71]. This effect is intrinsically linked to the trapping and detrapping time constant [71]. In the electric motor drive application, the switching frequency f_{sw} is far from 2 MHz, therefore the D-$R_{ds(on)}$ commonly has a monotonic increase with f_{sw} in this range. In [28], the on-resistance increases about 24% from 10 kHz to 100 kHz. The effect of f_{sw} is illustrated in Figure 4.1c.

For T_j, there exists controversy on the effects of T_j. The junction temperature can have an impact on the internal structural stress, thus affecting the trapping and detrapping time constant and the trapping efficacy [12]. The relationship between temperature and D-$R_{ds(on)}$ is complex and depends on various factors. Some studies report that D-$R_{ds(on)}$ increases with higher temperature near 50 °C. But at even higher temperatures (e.g., 90 °C), D-$R_{ds(on)}$ becomes nearly flat with voltage and even bent downwards, which indicates a non-monotonic relationship with temperature [74]. [16] suggests that the dependence between D-$R_{ds(on)}$ and T_j may be device-specific. In addition, literature [74] suggests the decrease in D-$R_{ds(on)}$ with temperature is due to the reduced hot-electron trapping, although the influence of temperature on D-$R_{ds(on)}$ is not universally consistent across different studies. Therefore, the junction temperature should be kept from large variations during the characterization tests.

For the duty cycle, as D increases, the duration of the off-state decreases. Therefore, the off-state trapping effect is mitigated and D-$R_{ds(on)}$ is decreasing. The effect is more prominent if V_{ds} is high. When V_{ds} is low, the D's effect is negligible [28]. The effect of D is illustrated in Figure 4.1d.

Figure 4.1e summarizes the R_g's effect on D-$R_{ds(on)}$. The turn-on gate resistance R_g affects the slew rate during the hard turn-on process, therefore affecting the V-I overlap. It has been reported in [72] that, at 400 V 25 A test condition, a 33% increase of D-$R_{ds(on)}$ is observed when the turn-on resistance R_g changes from 0 Ω to 20 Ω.

Table 4.1 summarizes these operational parameters, categorizing the reasons for D-$R_{ds(on)}$ for each parameter and their priority in the characterization. From the table, five parameters, including the effect of V_{ds}, I_d, f_{sw}, D, and R_g are

consistent in the literature, while the effect of T_j is ambiguous and inconsistent.

Therefore, to precisely measure D-$R_{ds(on)}$ under different parameters, the effect of T_j should not be neglected. In the electric motor drive application, high V_{ds} and I_d switching will bring a great amount of losses, which can increase T_j. To better grasp the effects of these parameters on D-$R_{ds(on)}$, maintaining the junction temperature rise is crucial. In this context, the literature review provides the foundation for determining the FOMs of the measurement methodologies.

From the results, it can also be noted that there exists a synergy in these parameters. For example, the effect of D is more prominent when V_{ds} is high. Similarly, the effect of R_g is also prominent when I_d is high. Therefore, I_d and V_{ds} are identified as the most critical operating parameters because they each directly influence $R_{ds(on)}$ and also consolidate the impact of other parameters on $R_{ds(on)}$.

5.1.3 Future Work

To begin with, from the results of the literature review, it can be noted that the effects of the GaN-on-Si devices' structures on D-$R_{ds(on)}$ are limited and yet to be evaluated, both theoretically and experimentally. Future work can be done to address this point.

Moreover, since the statistic results are from various literature, some literature do not specify the structures and the part numbers of their devices under test. In addition, the test methodology is not consistent in all the literature. As a result, a consistent review of D-$R_{ds(on)}$ of GaN-on-Si devices, considering the device structures and measurement methodology, could be conducted.

5.2 Measurement Methodologies

This chapter discusses the measurement methodologies. To begin with, Section 5.2.1 discusses how the measurement methodologies are evaluated. Then, Section 5.2.2 starts to discuss the evaluation results, followed by the possible future research plans in Section 5.2.3.

5.2.1 Method

To determine the most suitable measurement methodology for the application of electric motor drives, a literature review was conducted to examine the parameters influencing D-$R_{ds(on)}$, and a conceptual study was performed to understand the physical mechanisms behind D-$R_{ds(on)}$. These investigations form the foundation for determining the FOM of the measurement methodology.

The studies revealed that numerous parameters affect $R_{ds(on)}$. Additionally, T_j significantly influences $R_{ds(on)}$ characterization results, but its effect remains ambiguous in the literature. Consequently, T_j must be carefully controlled

during testing to isolate its impact on $R_{ds(on)}$ characterization.

Different measurement methodologies were studied, including DPT, SSCS, MPT and Pulse-IV tests. First, the Pulsed-IV test was not a good choice for motor drive application since the test is complicated and conducted on a single die, which can not represent the electric motor drive applications. The circuit schematics, principles, and parameter calculations of the other three methods were introduced. Evaluation of these methods was based on the figures of merit, including the method's accuracy (number of switching cycles), the number of the testable parameters, the range of testable parameters in the tests, and the complexity of the equipment used in the tests.

5.2.2 Result

The results for DPT, SSCS and MPT are discussed in this chapter.

DPT

As shown in Figure 4.2a, the current I_L decreases much more slowly when both GaN devices are driven (complementary switching). This occurs because, in complementary switching, Q_1 operates under Type B reverse conduction (Table 2.2), where the channel does not exhibit diode-like behavior, and the forward voltage drop is purely due to $R_{ds(on)}$.

In contrast, when only the DUT is driven (constantly off), Q_1 undergoes Type C reverse conduction, resulting in a significantly higher forward voltage drop and a faster decrease in I_L as depicted in Figure 4.2a. However, this rapid current drop has minimal impact on the DPT results because the rest time (t_3) is 1 μs, during which the current drop for both methods remains nearly identical, see Figure 4.3. Due to a higher voltage drop in Q_1's "virtual diode", the T_j of Q_1 is evaluated until current I_L drops to zero, as shown in Figure 4.2b. It can be seen that this virtual diode indeed causes higher T_j in Q_1, however, T_j is much lower than the max T_j requirement and will not affect normal operation and $R_{ds(on)}$ measurement of DUT. As can be seen in Figure 4.3, T_j of DUT has the same behavior during DPT test, the maximum T_j rise is 2.3 °C.

Therefore, it is appropriate to conclude that the constantly-off switching scheme is a better choice for DPT, given its simpler control strategy. Also, DPT is proven capable of testing $R_{ds(on)}$ at the worst thermal condition, 400 V and 60 A. But it is worth noting that DPT can not verify f_{sw}'s effect on $R_{ds(on)}$ and that the accuracy is limited due to two pulses' short duration. In addition, in terms of complexity, DPT itself is a mature testing method. However, the DPT requires the control of the soak time due to short test duration, which adds complexity to the test setup.

SSCS

For SSCS, while it theoretically achieves the highest number of switching cycles, its performance is constrained by heat dissipation. As shown in Figure 4.4, at 100 kHz, the junction temperature (T_j) rises to 54 °C at a load current of 5 A and 46 °C at 1 A. Similarly, Figure 4.5 demonstrates that at 10 kHz, T_j increases to 37.5 °C at 10 A. With a better cooling, this temperature can be below 35 °C. These results indicate that SSCS cannot effectively isolate the impact of T_j for higher current applications.

Moreover, SSCS requires large, high-power-rated load resistors and inductors, which are bulky and expensive. For example, a 50 mH inductor and a variable resistor (0.67 Ω to 360 Ω) are necessary, significantly increasing the system's size and cost. An electric machine can be used as an alternative to the bulky passive components, but it involves a two-level three-phase inverter and sophisticated control for each machine operation points. On the positive side, SSCS does not require a complex control strategy and is capable of evaluating all operational parameters.

In summary, while SSCS benefits from simplicity and comprehensive parameter evaluation, its limitations include reliance on bulky, costly components and a restricted current range. These constraints make SSCS unsuitable for $R_{ds(on)}$ characterization in electric motor drive applications.

MPT

For MPT, the first task for the simulation is to determine the switching cycles. As depicted in Section 4.2.3. MPT has different maximum testable load currents and the number of cycles, which are related to f_{sw}. For a 10 kHz f_{sw}, the maximum testable combinations are 20 A, 80 cycles and 30 A, 15 cycles. For a 100 kHz f_{sw}, the maximum testable combinations are 20 A, 180 cycles.

Results shows that for the same switching frequency, there exists a trade-off between accuary and testable current range. By sacrificing the number of cycles from 80 to 15, the testable current range increases from 20 A to 30 A.

For MPT, it requires sophisticated control strategies and lab equipments to precisely control the number of the pulses in a test. Also, if the number of pulses are limited due to high current, the soak time control is also needed, which further increases the complexity of the test.

Summary

In summary, results shows that DPT can test full current range, but has limited accuracy and can not evaluate f_{sw} and D. SSCS has the best accuracy, but has very limited testable current range. The scope of current range can be extended in the case of liquid cooling but limited. For MPT, the range of evaluation current

rises to 30 A at 10 kHz and 20 A at 100 kHz. This range can be extended in the case of a stronger cooling, but still hard to cover the whole 60 A range.

After the evaluations, it is found that only DPT can evaluate the full current range in electric motor drive applications. Though DPT has the minimum accuracy, it is able to reflect the variation trend of $R_{ds(on)}$ when operational parameters changes, if the soak time is well controlled. MPT, which although can not test the full current range, offers a more accurate measurement. SSCS, on the contrary, fails to evaluate high-current applications due to excessive heat generated during the tests. This excessive heat increases T_j and makes it hard to separate T_j's effect on D-$R_{ds(on)}$.

Therefore, DPT is finalized as the first methodology in D-$R_{ds(on)}$ characterization for the electrical motor drive application. When accuracy is prioritized, MPT can be a good alternative at the cost of testable current range.

A summary of the comparison of these three methods is provided in Table 5.1.

Table 5.1: *Test Methodology Summary*

Rank	Method	I_d	Complexity	Accuracy	Testable parameters
1	DPT	0-60 A	Lowest	Lowest	Not f_{sw} and D
2	MPT	<30 A	Highest	Higher	All
3	SSCS	<5 A	Higher	Highest	All

The probes selected for the test and the initial test plans for DUT are listed in Appendix C.

5.2.3 Future Work

A preliminary investigation into the measurement methodology of D-$R_{ds(on)}$ was conducted, and the results indicate that DPT is the best initial option for characterizing D-$R_{ds(on)}$. When accuracy is the primary concern, MPT serves as a secondary approach. Therefore, it would be both beneficial and insightful to implement and compare two practical D-$R_{ds(on)}$ measurement tests using DPT and MPT to verify these conclusions.

5.3 On-State Voltage Measurement Circuits

This chapter discusses the method and results of the on-state voltage measurement circuit (OVMC). Drawbacks of the method and made assumptions are discussed in Section 5.3.1. The results of the OVMC simulation and PCB evaluation are analyzed in detail and discussed in Section 5.3.2. Finally, suggestions on future work are given in Section 5.3.3.

5.3.1 Method

To design an on-state voltage measurement circuit (OVMC), a pre-study was conducted where different types of OVMCs were identified. The operating principles of the various types of circuits were analyzed in the pre-study, and inherent advantages and disadvantages were highlighted. Testbenches were created in LTSpice, and simulations were performed to select the most promising OVMC. The chosen circuit was realized as a PCB, and its DC accuracy was evaluated. Further tests with a vector network analyzer and on-state voltage measurements of a GaN device were planned. Unfortunately, given the project's time constraint, these tests could not be performed. This discussion will highlight different drawbacks of the selected method and decisions that would have been made differently given the possibility.

Defining the design requirements for the OVMC and prioritizing the figures of merit (FOM) presented a significant challenge. The primary design requirement was that the OVMC must handle input voltages up to 1200 V to accommodate the highest voltage among the selected devices, see Table 1.1. An assumption, based on the maximum $V_{ds(on)}$ and the effects of D-$R_{ds(on)}$, suggested that the input voltage of the OVMC should range from 0 to 4 V. Whether this assumed voltage range is adequate will depend on the extent of the D-$R_{ds(on)}$ effect and the magnitude of oscillations in the power loop. Additionally, the amplitude of these oscillations will be influenced by parasitics in a real half-bridge circuit. Therefore, actual on-state voltage measurements should be conducted to fine-tune the measurement circuit for the specific input voltage range.

During the simulations, efforts were focused on optimizing all FOMs. Additionally, the literature review of D-$R_{ds(on)}$ revealed that the detrapping of D-$R_{ds(on)}$ can be modeled as an RC circuit discharging with time constants of 5 µs and longer, as discussed in Section 2.1.3. For a single-pole low-pass filter, the relationship between rise-time and bandwidth is commonly approximated by

$$\mathrm{BW} = \frac{0.35}{t_r}. \tag{5.1}$$

For a RC circuit, which is a single-pole low-pass filter, the relation between the time constant and the rise time is given by

$$t_r = 2.2RC = 2.2\tau. \tag{5.2}$$

Combining the two equations and assuming that the fastest time constant of D-$R_{ds(on)}$ is 1 µs (worst-case), the largest bandwidth of D-$R_{ds(on)}$ is thus

$$\mathrm{BW} = \frac{0.35}{2.2\tau} = \frac{0.35}{2.2\,\mu\mathrm{s}} \approx 159\,\mathrm{kHz}. \tag{5.3}$$

A common rule of thumb for oscilloscopes is that the oscilloscope bandwidth should be at least five times the signal bandwidth. Applying this requirement to the OVMC gives a bandwidth requirement of only 795 kHz. This is a crude

estimate. However, it indicates that a bandwidth requirement of, for example, 10 MHz might have been more than sufficient. This would make the transistor circuit a more appealing choice, as it offers higher accuracy but with a narrower bandwidth compared to the matched diode circuit.

During iteration 3 of the transistor circuit, four Schottky diodes were put in series to minimize the output capacitance and see its effects on the settling time, see Figure 3.11b. However, the effects on the frequency response were overlooked. The results of the AC analysis can be seen in Figure 5.1. The bandwidth of the transistor circuit essentially doubled and achieved a bandwidth of 309 MHz compared to 145.2 MHz. However, the achieved bandwidth was still lower compared to the designed matched diode circuit, which had a bandwidth of 538.3 MHz, see Figure 4.8e. However, using iteration 3 instead of iteration 2 for the final comparison would have given a better result for the transistor circuit.

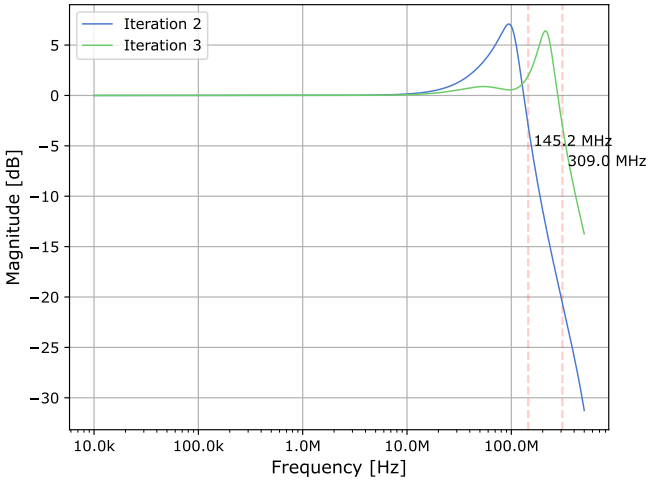


Figure 5.1: *Magnitude response of the transistor circuit with 1x Schottky diode (TC iteration 2) versus 4x Schottky diodes (TC iteration 3) in series in the clamping branch.*

Different matched diode circuits were compared in Section 3.3.6. Several operational amplifiers were tested, and AD8045 was selected for its high bandwidth of 1 GHz, adequate gain, and input voltage range. However, as discussed above, the bandwidth may not be as important as the accuracy. Instead, an amplifier with lower bandwidth and higher gain could have been selected to improve the accuracy of the MDC. Further, using matched transistor pairs to create a current mirror was not the most efficient approach; opting for a current mirror IC that meets the specifications would have been a better choice. This was a mistake made due to a stressful design period. Moreover, the operational amplifiers supply voltages could have been tweaked more for MDC1B and MDC2 to give

a smaller error for the specified input voltage range ($[0, 4]$ V). Although MDC3 was chosen for its overall best performance, all three circuits showed very similar results, see Figure 3.15. Any of these circuits could have been selected and optimized. The input voltage range of the circuits was limited by the linear operating region of the operational amplifier. Since MDC3 had a gain of 2, it lost half of its input range. If the decision were to be made again, MDC1B would have been selected for its simple topology and higher input voltage range.

To summarize, various OVMCs were investigated, highlighting the advantages and disadvantages of different TCs and MDCs. One circuit of each type was designed and compared through simulation. The MDC outperformed the TC in terms of bandwidth, flatness, phase linearity, and vertical resolution, whereas the TC excelled in DC accuracy and settling time. A notable oversight in the TC design was neglecting the frequency response of iteration 3, which, in hindsight, offered a better design than iteration 2. The discussion also suggests that the circuit's bandwidth requirements may be much lower than initally thought, meaning the bandwidth of TC iteration 2 might have been sufficient. Despite this, the MDC remains a strong candidate, with potential accuracy improvements achievable by selecting an operational amplifier with a higher gain. Finally, the investigated MDCs demonstrated very similar performance, with MDC1B providing a simpler topology at the cost of slightly reduced performance.

5.3.2 Results

In simulation, the transistor circuit (TC) and matched diode circuit (MDC) showed similar performance in terms of settling time, 26.5 ns versus 31.1 ns, see Figure 4.8a. The settling time of the MDC could be further improved by increasing the biasing current I_b. Hence, there is no important difference.

The group delay of the MDC remained constant over a higher frequency range than the TC; in other words, it has a more linear phase, as shown in Figure 4.8f. Both circuits' magnitude responses roughly resembled those of a first-order LC low-pass filter, with a peak in the amplitude before attenuation, as seen in Figure 4.8e. The peaking is more pronounced in the TC, which exhibits the worst flatness of the two circuits. A bandwidth of 145.2 MHz and 538.8 MHz was achieved for the TC and MDC, respectively. But, as discussed in Section 5.3.1, an oversight occurred in the TC design. Iteration 3 outperformed iteration 2 in terms of bandwidth and should have been selected for the comparison between the TC and MDC. Iteration 3 achieved a bandwidth of 309 MHz, as shown in Figure 5.1. When comparing the clamping branches of the MDC in Figure 4.7 and the TC (iteration 3) in Figure 3.10, it is clear that the TC has an additional branch of Schottky diodes, which contributes to the output capacitance and degrades the magnitude response. This suggests that by redesigning the TC's clamping branch, it could potentially perform as well as the MDC in terms of bandwidth. On the other hand, a practical advantage of the MDC is its 50 Ω output termination, which eliminates the need for a probe that could further degrade the frequency response.

The TC exhibited essentially no DC error, see Figure 4.8b. In simulation, the DC error of the MDC was less than 1 % for input voltages above 0.12 V and was considered small enough to be acceptable. Selecting another operational amplifier with a higher gain could further reduce this error. For the implemented MDC, the relative error is higher; the error stays below 1 % for input voltages above 0.32 V. No diodes were characterized to ensure that they have the same forward voltage for the biasing current I_b, which could be one reason that the implementation performs worse than in simulation. Another reason could be the evaluation itself. The DC error appears random for the different input voltages, see Figure 4.9, which could suggest that it is noise that causes the most error. However, the measurement indicates that a good accuracy can be achieved. Further tests need to be performed to draw a strong conclusion.

The achievable vertical resolution was 3.8 mV for the TC and 1 mV for the MDC. The worst absolute DC error in the MDC was 5 mV. As a result, the errors caused by the vertical resolution of the TC and the DC error of the MDC were of similar magnitude. The vertical resolution of the TC could not be improved with the current setup, as it requires a high clamping (Zener) voltage to turn the transistor off during the blocking state. Lowering the gate voltage would enable a lower clamping voltage; however, this would likely degrade performance by

increasing the transistor's resistance in the measurement state. An alternative solution is to actively switch the transistor, as discussed in Section 2.3.4. This would allow the clamping (Zener) voltage to be selected independently of the gate-to-source voltage, enabling better vertical resolution. In conclusion, the MDC provides better vertical resolution, and it may be worthwhile to explore the potential of actively switching the transistor to further enhance the vertical resolution of the TC.

To summarize the discussion, an MDC with promising simulation results was designed and implemented. The DC error evaluation of the PCB showed strong performance, but further testing is required to verify its functionality and performance thoroughly. In the simulation, both the TC and MDC showed promising results, with the MDC outperforming the TC in terms of bandwidth, flatness, phase linearity, and vertical resolution. In contrast, the TC excelled in DC accuracy and exhibited better settling time. Modifications to both designs that could address their weaknesses and improve performance have been discussed.

5.3.3 Future work

A thorough investigation of various on-state voltage measurement circuits has been conducted. One transistor circuit (TC) and one matched diode circuit (MDC) were designed and compared through simulation. The MDC was selected and implemented. Due to time constraints, only a DC error evaluation was performed on the implemented PCB. The most important future work involves conducting actual on-state voltage measurements to verify the circuit's functionality and performance further. Additionally, implementing a TC and comparing it with the MDC in real-world conditions could help identify potential drawbacks that may have been overlooked during the pre-study and design phase. Finally, exploring the implementation of an actively switched TC and comparing its performance to the constantly biased version could be worthwhile. As discussed in Section 2.3.4, the actively switched design has the potential to achieve a lower clamping voltage, which could significantly improve vertical resolution — a key limitation of the designed TC.

6

Conclusion

This chapter presents the conclusions to the research questions introduced in the first chapter.

6.1 Research Questions

1. How do operational parameters (V_{ds}, I_d, f_{sw}, etc.) affect D-$R_{ds(on)}$?

   Several parameters influence and can contribute to an increase of D-$R_{ds(on)}$, including V_{ds}, I_d, f_{sw}, D, R_g, and T_j. All mentioned parameters are consistently described in the literature, except for T_j. The effect of T_j remains ambiguous and contradictory across research papers. These effects are summarized in Table 4.1.

   Among these, V_{ds} and I_d are identified as the most significant parameters, as they not only directly influence D-$R_{ds(on)}$ but also increase the other parameters' effect on D-$R_{ds(on)}$.

2. What measurement methodology should be used to determine D-$R_{ds(on)}$?

   The investigation of measurement methodology is based on the accuracy of the D-$R_{ds(on)}$ measurement within the assumed thermal limitation, the complexity of the test setups, and the number of operational parameters and range of operational parameters the methods can evaluate. Results show that DPT is the only method to evaluate the entire current and voltage range without excessive overheating. Since voltage and current were concluded to be the operational parameters that affect D-$R_{ds(on)}$ the most, DPT is selected as the primary method to determine whether a

device suffers from D-$R_{ds(on)}$ or not. Suppose the accuracy of the D-$R_{ds(on)}$ measurement is prioritized. In that case, MPT is a suitable method because it has an extended number of switching cycles, giving a higher accuracy than DPT, while it can still evaluate a large portion of the current range.

3. What on-state voltage measurement circuit should be used to determine D-$R_{ds(on)}$?

   Two on-state voltage measurement circuits (OVMCs) were designed and compared through simulation: one transistor circuit (TC) and one matched diode circuit (MDC). The MDC was selected, implemented, and evaluated. A first test of the implemented MDC's DC error shows promising results; it has a relative DC error less than 1 % for input voltages larger than 0.32 V. However, further tests are necessary to thoroughly verify its functionality, such as observing its frequency response using a vector network analyzer and performing actual on-state voltage measurements of GaN devices. Simulations show that the MDC and TC perform similarly; see Table 4.3. The MDC outperforms the TC regarding bandwidth, flatness, phase linearity, and vertical resolution.

   In contrast, the TC excelled in DC accuracy and exhibited better settling time. However, the differences in performance are not significant enough to make either circuit a clear choice over the other. Further, the bandwidth requirement of the circuit might be lower than initially thought; see the discussion in Section 5.3.1; which strengthens the case for the TC. This report concludes that both the TC and the MDC would be viable options for determining D-$R_{ds(on)}$. To fully evaluate their capabilities, both circuits should be implemented and tested physically to highlight any additional benefits or drawbacks.

Appendix

A

Appendix 1

Table A.1 shows the authors' contribution.

Table A.1: *Chapter contributions.*

Chapter	Title	Author
1	Introduction	Both
2	Theory	
2.1	The Lateral GaN-on-Si Device	
2.1.1	Device Structure	Both
2.1.2	Electrical Modeling and Characterisitics	DZ
2.1.3	Origins of Dynamic On-Resistance	Both
2.1.4	Determining Dynamic On-Resistance	MJ
2.2	Converter Testing Basics	DZ
2.3	On-state Voltage Measurement Circuits	MJ
3	Method	
3.1	Operational Parameters' Effect on D-$R_{ds(on)}$	DZ
3.2	Measurement Methodologies	DZ
3.3	On-state Voltage Measurement Circuits	MJ
4	Results	
4.1	Operational Parameters' Effect on D-$R_{ds(on)}$	DZ
4.2	Measurement Methodologies	DZ
4.3	On-state Voltage Measurement Circuits	MJ
5	Discussion	
5.1	Operational Parameters' Effect on D-$R_{ds(on)}$	DZ
5.2	Measurement Methodologies	DZ
5.3	On-state Voltage Measurement Circuits	MJ
6	Conclusion	Both

B

Appendix 2

Table B.1: *Raw data from PCB accuracy evaluation.*

Vin,mean [mV]	Vout,mean [mV]	R_1 [Ω]
34	40	1.1
100	108	1.1
200	205	1.1
299	303	1.1
401	403	20
498	500	20
600	605	20
699	701	20
802	804	20
901	907	20
1001	1007	20
1105	1109	20
1201	1203	20
1299	1304	20
1399	1407	75
1499	1507	75
1598	1602	75
1701	1702	75
1800	1803	75
1901	1907	75
2001	2006	75
2099	2103	75

Vin,mean [mV]	Vout,mean [mV]	R_1 [Ω]
2199	2200	75
2296	2298	75
2400	2400	75
2500	2499	75
2601	2602	75
2698	2702	75
2801	2804	110
2900	2904	110
2999	3003	110
3101	3107	110
3200	3203	110
3301	3300	110
3400	3404	180
3501	3505	180
3602	3608	180
3702	3704	180
3804	3801	180
3900	3897	180
4002	3996	180
4101	4095	180
4201	4130	180
4302	4134	180
10000	4132	470

Table B.2: *Bill of materials for on-state voltage measurement circuit PCB.*

Designator	Manufacturer Part Number
C11, C12, C27, C28	GRT188C81C106ME13D
J4, J5	73100-0114
U5, U6	BCV62C,215
C3, C9, C25, C26	CGA6P3X7S1H106K250AB
R10	MCWF08R75R0BTL
U8	LM337IMP/NOPB
R5, R14, R15	MCWF08R2400BTL
U4, U7	AD8045ARDZ
D3, D16	AZ23C5V6-7-F
C4, C10, C16, C17, C23, C24	C0805Y104K5RACTU
C1, C2, C6, C7	GRM21BR61H475KE51L
C8, C13, C14, C15, C18, C19, C20, C21, C22	T491A106M020AT
D1, D2, D12, D15	1N4006G-T
D13, D14	GD02MPS12E
C5	EEETKK331UAM
U2	TMR 4-2413
D4, D6, D8, D10	PMEG2015EA,115
D5, D7, D9, D11	PMEG2020EH,115
R6	RN73C2A1K69BTDF
R7	ERJ-6ENF1103V
R1, R2, R3, R4, R13, R17, R18, R19	RS73F2ATTD2000B
R8, R9, R11, R12, R16	ERA-6AEB4990V
U1	LM317AEMP/NOPB
U3	TMV 2405S

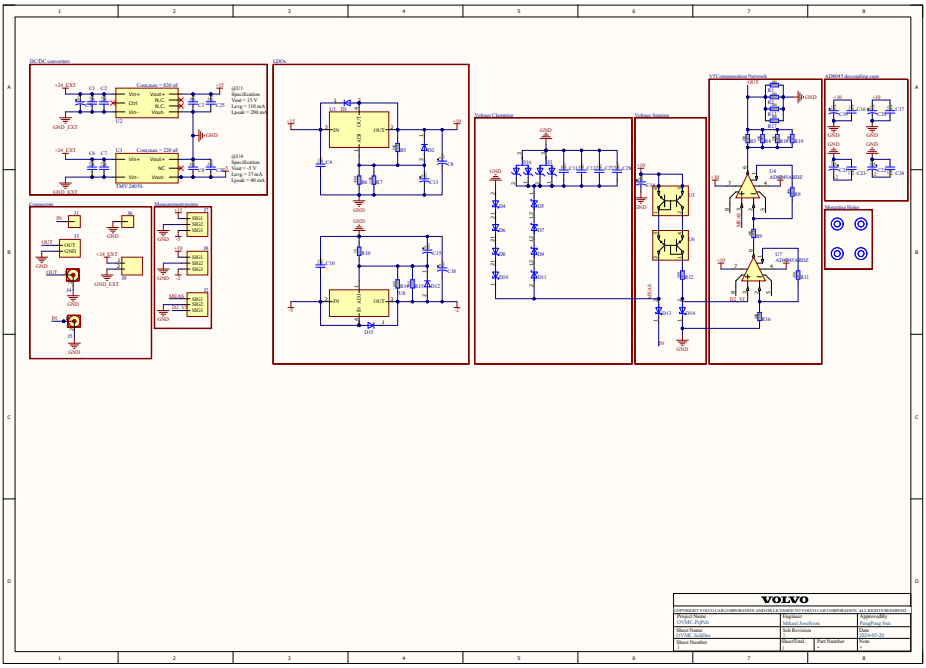


Figure B.1: *Schematic of the realized on-state voltage measurement circuit.*

C

Appendix 3

C.0.1 Measurement Equipment and Probe Selection

GaN device has fast voltage rise time and current rise time. According to [7], GS66516 has a voltage rise time of 12.4 ns. The current has even faster rise time, which is around 2.2 ns tested by LTSpice simulation from GaN Systems. The current curve during the DPT is extracted, as in Figure C.1, and the result shows an approximately 2.2 ns current rise time. This current curve is then emulated in PLECs, sent to low pass filters with different cut-off frequencies to evaluate the bandwidth of the probes' effect on the measurement signal delay, as shown in Figure C.2. And the simulation plot is shown in Figure C.3.

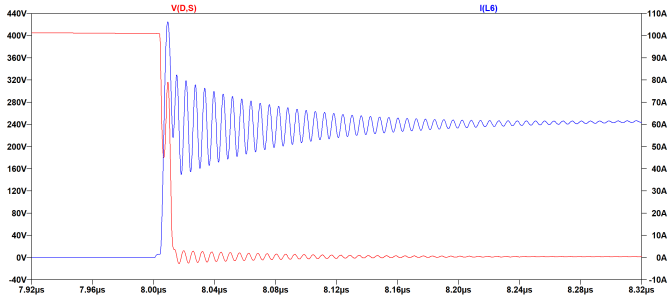


Figure C.1: *DPT in LTSpice simulation to extract current rise time of GS66516.*

Results show that the probe with a bandwidth of 30 MHz (commonly adopted Rogowski Coil's bandwidth on the market) will introduce a measurement delay of 10 μs, which is not acceptable since this time is in the range of trapping and detrapping time constant. This will lead to error in D-$R_{ds(on)}$ measurement. To

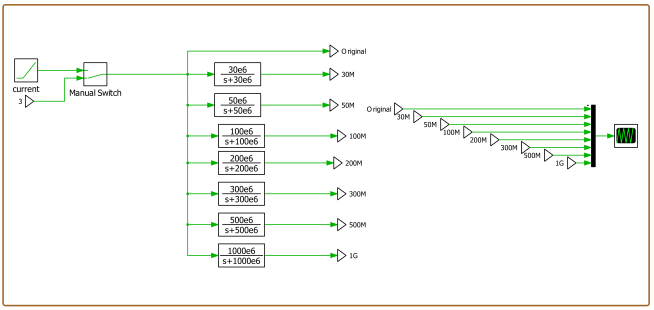


Figure C.2: *Evaluation of the bandwidth of probe's effect on measuring delay using the low-pass filter in PLECs*

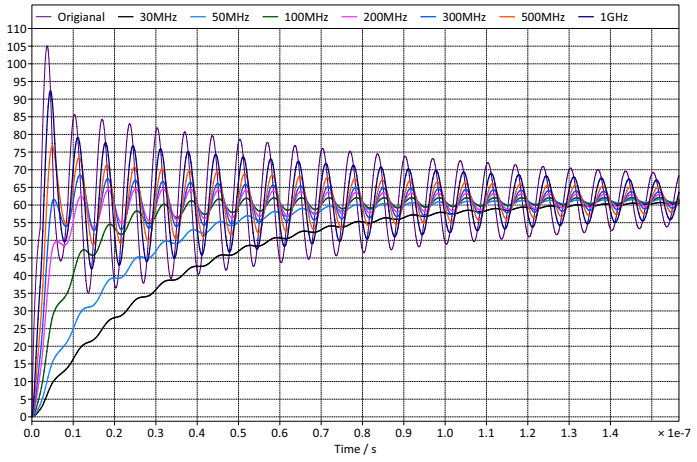


Figure C.3: *The simulation result for the probes' bandwidth evaluation. The bandwidth is simulated through a first-order low pass filter*

precisely obtain the current trace, a precise shunt resistor together with a high bandwidth probe is preferred for current measurement.

Table C.1: *Probes selected for the test*

Parameters	**Measurement**	**Comments**
I_d	Current shunt resistor and TPP1000 High bandwidth passive probe	To reduce the effect of measurement delay
I_L	Rogowski Coil PEM CWT Ultra Mini Rogowski Coil 30 MHz	It is helpful for configuring and debugging the DPT setup.
T_j	Thermal Camera	Use when having the thermal pad
V_{gs} (DUT)	TPP1000 High bandwidth passive probe and in 1x mode with short ground loop	Give additional details such as the delay times and gate voltage overshoot

Table C.2: *DPT Plan - I_d*

Investigation of the effect of I_d								
No.	$t_1/\mu s$	$t_2/\mu s$	$t_3/\mu s$	$t_4/\mu s$	$L/\mu H$	V_{ds}/V	I_d/A	T_j/°C
1	100	1	6	1.5	**40**	400	**60**	25
2	100	1	6	1.5	**60**	400	**40**	25
3	100	1	6	1.5	**120**	400	**20**	25
4	100	1	6	1.5	**240**	400	**10**	25

Table C.3: *DPT Plan - V_{ds}*

Investigation of the effect of V_{ds}								
No.	$t_1/\mu s$	$t_2/\mu s$	$t_3/\mu s$	$t_4/\mu s$	$L/\mu H$	V_{ds}/V	I_d/A	T_j/°C
1	100	1	6	1.5	**40**	**400**	60	25
2	100	1	6	1.5	**30**	**300**	60	25
3	100	1	6	1.5	**20**	**200**	60	25
4	100	1	6	1.5	**10**	**100**	60	25

Table C.4: *DPT Plan - T_j*

Investigation of the effect of V_{ds}								
No.	$t_1/\mu s$	$t_2/\mu s$	$t_3/\mu s$	$t_4/\mu s$	$L/\mu H$	V_{ds}/V	I_d/A	T_j/°C
1	100	1	6	1.5	**40**	**400**	60	25
2	100	1	6	1.5	**40**	**400**	60	50
3	100	1	6	1.5	**40**	**400**	60	0
4	100	1	6	1.5	**40**	**400**	60	-25

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