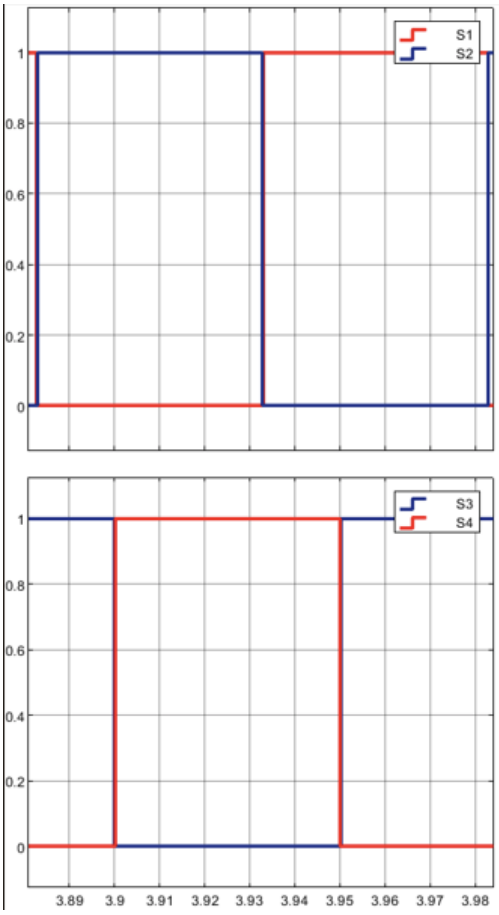

Investigation of HV-LV Isolated DC-DC Converter Topologies for Automotive Applications

Master's thesis in Sustainable Electric Power Engineering and Electromobility

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DEPARTMENT OF ELECTRICAL ENGINEERING
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2025
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Cover: Gate pulses for the primary switches created using pulse generator in Simulink.

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Abstract

In this work the design of isolated DC/DC converter such as phase shifted full bridge with three different secondary topologies full bridge (FB), center tapped (CT) and current doubler(CD) are discussed which are to be used in auxiliary power module (APM) to power the LV battery in an electric vehicle. The converters are designed for a full load power of 7500 W and an input voltage range of 370 V - 920 V to achieve regulated output of 15 V at an operating frequency of 100 kHz. The main work involves the design of transformer, inductor, component level loss analysis and estimation of efficiency of the converters at various loads and input voltages.

Phase shift is a modulation technique used to control the operation of the switches in the primary where all the switches in the primary operate for a fixed duty cycle of 50% but with a phase shift. The phase shift depends on the input voltage and turns ratio of the transformer. In this topology zero voltage switching (ZVS) is achieved through the leakage inductance of the transformer so turn on losses are zero but turn off losses are unavoidable. Silicon carbide (SiC) MOSFET's are used in the primary and Silicon (Si) MOSFET's are used in the secondary.

Several design considerations were taken into account such as paralleling of switches on the secondary, variation of on state resistance ,$R_{\mathrm{ds,on}}$, junction temperature rise of the switches. All the converters were simulated in MATLAB/Simulink to find the currents in the components to estimate the conduction , switching losses in MOSFET's, copper losses in transformer and inductor.The waveforms of the converters are verified theoretically and through simulations. Comparison of the converters based on the total losses and efficiency is done at the end of this work which made it evident that the PSFB-CT has a better performance at low load PSFB-CD has a better performance at high load. Further investigationss and comparison of topologies such as traditional half bridge and LLC can be considered. Different topology architectures involving interleaving/paralleling of the power stages or components can be considered to improve the performance.

Keywords: Phase shifted full bridge, Silicon Carbide(SiC), Silicon (Si), Zero voltage switching (ZVS), full bridge (FB), Center tap (CT), current doubler (CD)

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Meghana Viswanath Tuppada, Gothenburg, August 2025

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

APM	Auxiliary Power Module
CD	Current doubler
CT	Center tap
EV	Electric Vehicle
FB	Full bridge
HV	High Voltage
LV	Low Voltage
MOSFET	Metal Oxide Semiconductor Field effect transistor
PSFB	Phase Shifted Full Bridge
PWM	Pulse width modulation
$R_{\text{th,JC}}$	Thermal resistance junction to case
SR	Synchronous rectification
T_j	Junction temperature
ΔT	Rise in temperature
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching

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1
Introduction

1.1 Problem Background

Transportation industry is one of the main contributors to greenhouse gas (GHG) emissions, in addition to power plants. The world is shifting towards sustainable energy in the production of power through renewable energy sources, and so is the transportation industry towards developing electric vehicles. The emphasis on electric vehicles (EV) is increasing day by day with the aim of reducing the use of fossil fuels, to provide energy efficient and environment friendly transportation [1].This was emphasized further with the Paris Agreement to keep the global temperature rise to less than 2^0C [2]. According to a survey by a consulting firm Deloitte, in 2030, 32% of the vehicles sold in the world would be electric or hybrid [2] . To accommodate this automotive industry is continuously adapting itself for innovative solutions [3].

The EV's feature a High voltage (HV) battery/traction battery that can be charged from the on board charger (OBC) and as well as while regenerative braking through a AC-DC converter. This is a high voltage battery rated around 400 V or 800 V which is a nominal voltage and has to be stepped down in order to power the loads, hence we need a DC-DC converter, this unit is also called as Auxiliary power module(APM) or Auxiliary power unit(APU) or low voltage DC-DC converter. The APM should be reliable and efficient enough to provide power to the LV system (communication and control units) [4] for safe vehicle operation.

The DC-DC converter in an electric vehicle transfers power from the high-voltage traction battery to the low-voltage electrical systems and the 12 V battery [5], [6], [7]. In a typical electric vehicle,the traction battery operates at 400 V, with a range of 250-450 V, while the low-voltage side operates between 10-16 V [6]. Consequently, the APM must be designed to handle a wide voltage range on both the high-voltage (HV) and low-voltage (LV) sides. For electric vehicles with a 800 V battery, this voltage range is even broader on both HV and LV side [6]. Furthermore, the increased power demands from the LV side, due to both basic and

additional loads, require a design that supports high output current and power ratings. 800 V battery packs are becoming popular due to less current, better charging speeds , so it is necessary to have 800 V -15V DC-DC system to supply the LV system. This requirement highlights the need for the APM to deliver high efficiency, galvanic isolation, high power density and wide input/output range. The DC-DC converter topologies are classified as shown in the Figure 1.1.

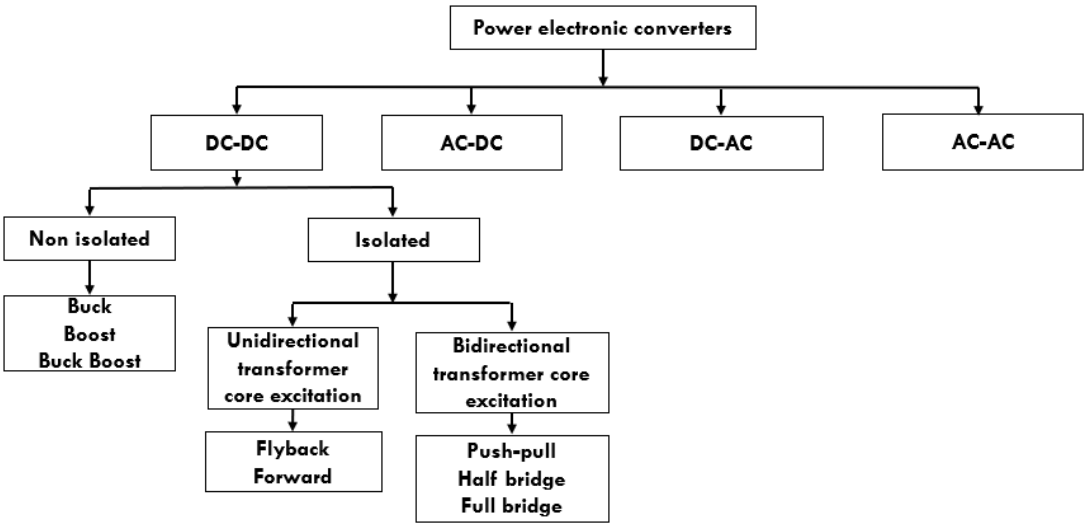


Figure 1.1: Classification of DC-DC converters

Only isolated DC-DC converters were considered for investigation. As shown in figure 1.1 the flyback and forward converter topologies fall under uni-directional transformer core excitation it means flux is not balanced in a cycle and also the currents in these converters are very high which will not be efficient for high power requirement. So bi-directional transformer core excitation converters were the main focus.
Based on theory:

1. Push pull converter is bulky as the transformer windings on primary and secondary are center tapped and the voltage stress on the MOSFET'S on primary will be $2V_{\text{in}}$ and $\frac{2V_{in}}{n}$ on secondary , this converter is usualy very uncommon in automotive application and was not found in literature so this topology was not considered for further investigation
2. Half bridge converter can be considered for the analysis but the switch currents and turns ratio are twice that of full bridge for the same input, output and power requirement. So, the switch conduction losses and transformer copper losses are higher in this topology.

Full bridge converter was considered for further analysis in this thesis with three different secondary topologies.

1.2 Aim

To investigate HV-LV isolated DC-DC converter topologies that can meet high power requirements, wide range of input/output voltages, high efficiency,high power density, galvanic isolation and is efficient. The selected topologies are to be designed for an HV input of 800 V nominal, 4000 W nominal output power and 7500 W peak power.

1.3 Scope

The scope of this thesis will involve investigating and evaluating isolated DC-DC converter topologies selected from the literature. An open loop control is implemented for all converters. A comparison will be made based on component losses, power density, and overall efficiency for each topology. The analysis and comparison will be based on simulation results.

1.3.1 Limitations

1. Implementation of closed loop control, thermal management, overall cost considerations, and hardware implementation are beyond the scope of this thesis.
2. This thesis is just a relative comparison of the converters , some practical considerations such as PCB losses , total thermal impedance of the MOSFET's , thermal and magnetic simulations of the magnetics have not been considered
3. Paralleling /interleaving of the power stages and investigation of other topologies should be considered

1.4 Specification of the issue being investigated

The DC-DC converter has a defined requisite of the input/ output voltage ranges and power as discussed in section 1.2.The converters selected are designed with a modulation technique to maximize efficiency and reduce losses. Comparison of the converters based on the losses ,power density, efficiency ,

ability to handle the wide range of input/output voltages is done.Based on this the converters are compared relatively.

1.5 Methodology

There are various DC-DC converter topologies available, but selecting the ones that meet our specific requirements is crucial. A thorough literature review is conducted to select appropriate topologies, followed by performing design calculations. The workflow is broken down into the following objectives:

1.5.1 Objectives

(a) To investigate and select isolated DC-DC converter topologies that meet the requirements of wide input/output voltage ranges and power
(b) To perform the circuit design calculations for the selected topologies
(c) To design a open-loop control for all the selected topologies
(d) To incorporate various design considerations such as variation of $R_{\mathrm{ds,on}}$, paralleling of MOSFET's on the secondary to keep the junction temperature below 150^0C
(e) To design the transformer
(f) To design inductor for LC filter
(g) To calculate the losses of all the components in the converter
(h) To compare the selected topologies based on the component losses, converter losses and efficiency
(i) Report writing and presentation

2

Theory

A careful review is conducted, taking into account of the requirements of the DC-DC converter. So, based on power requirements, safety concerns and zero voltage switching (ZVS) on the primary, isolated converters are chosen. Such as full bridge converter, and on the secondary it can be full bridge, center-tapped transformer, and current doubler. A thorough analysis will be conducted of these converters and will be checked for the regulated output and ZVS on the primary.

2.1 Phase shifted full bridge converter- full bridge on secondary

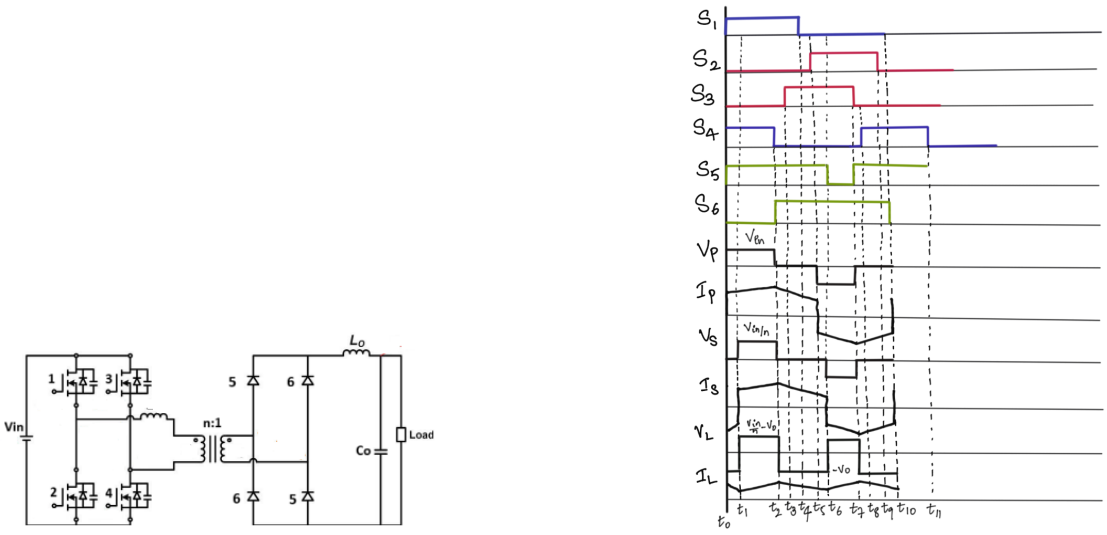


Figure 2.1: Circuit and Waveforms of Phase shifted full bridge converter-bridge rectifier

Mode 1: $t_0 - t_1$ Duty cycle loss mode
At $t = t_0$ switch 1 turns on with ZVS and 4 is on so the voltage across the primary of the transformer is V_{in} and the current in the transformer primary is increasing. But the voltage does not appear across the secondary as the current changes it's direction because switches 4 and 2 were on at t_{11}. Both switches marked 5 will conduct as the gate signal is given but as the voltage across the secondary is zero the inductor is discharging and the current freewheels.

Mode 2: $t_1 - t_2$ Power delivery mode
Both the switches 1 and 4 are on the voltage appears across the primary and secondary until t_2 till both the switches conduct. Switch 5 is on the inductor charges.

Mode 3: $t_2 - t_3$ Switch 3 ZVS mode
At t_2 switch 4 turns off and the primary current charges the output capacitance of 4 and discharges the output capacitance of 3. Once the output capacitance is completely discharged the diode conducts and 3 completely turns on with ZVS. The currents in the primary and secondary reduce as the voltage across primary and secondary are zero. During this period switch 5 still is on and 6 turns on the inductor discharges through these switches.

Mode 4: $t_3 - t_4$ Freewheeling mode
At t_3 switch 3 is turned on and 1 is on so the current freewheels through the upper switches. 5 and 6 are on and the inductor is discharging.

Mode 5: $t_4 t_5$ Switch 2 ZVS mode
At t_4 switch 1 turns off and the primary current charges the output capacitance of switch 1 and discharges 2. Once the capacitance is discharged diode conducts and 2 turns on with ZVS.

Mode 6 :$t_5 - t_6$ Duty cycle loss mode
At t_5 2 and 3 are on but the current uses the primary voltage across the transformer to change its direction, and hence the voltage across the secondary of the transformer is zero. During this period, 5 and 6 are on and the inductor is still discharging through these switches.

The modes of operation will repeat in the same manner for the next cycle.

2.2 Phase shifted full bridge converter-center tap on secondary

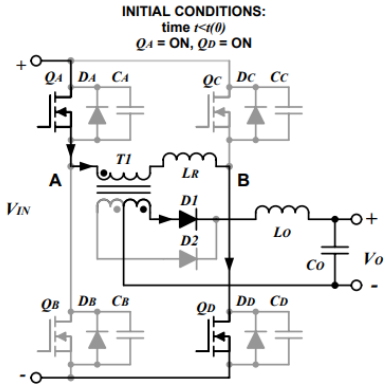


Figure 2.2: Circuit of Phase shifted full bridge converter-center tap on secondary [7]

The power is transferred to the load when two of the diagonal switches are conducting and when either two upper switches/lower switches are on, the voltage across the primary winding of the transformer is zero and the current is freewheeling.

Mode 1:t=t(0)
Q_A and Q_D are conducting. During this operation the voltage across the transformer primary is $+V_{\text{in}}$

Mode 2: t(0) < t < t(1): Right leg transition
Q_D is turned off but the primary current continues to flow through the output capacitance C_D charging it to $+V_{\text{in}}$, simultaneously output capacitance of the switch Q_C, C_C is discharged. This enables ZVS. During this transition the voltage across the transformer primary is decreased from $+V_{\text{in}}$ to zero. During this transition the primary voltage drops below reflected secondary voltage V_o*N and the output inductor voltage changes polarity. It supplements the primary until the primary contribution reaches to zero.

Mode 3: t(1) < t < t(2): Clamped freewheeling
The current freewheels through Q_A and the body diode of Q_C . Switch Q_C turns on in this period.

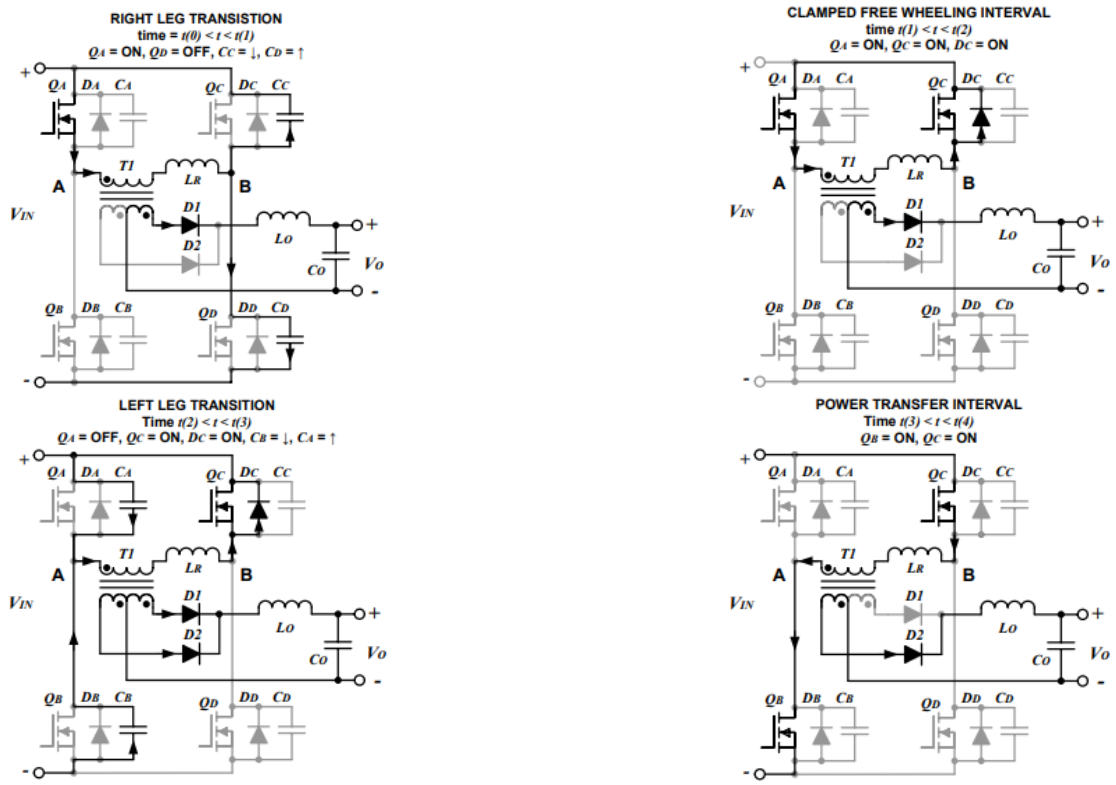


Figure 2.3: Right leg and left leg transition of phase shifted full bridge converter-center tap on secondary [7]

Mode 4: t(2) < t < t(3): Left leg transition
During this period switch Q_A is turned off. The current will flow through C_A charging it. The primary current continues to flow but clamped by the body diode D_B. Once Q_B is on the power is transferred to the load. The transition takes longer time as the energy stored in the resonant inductor and the magnetising inductor is not clamped to zero this is considered as a loss. This including the loss during the previous transition reduces the primary current. Thus taking longer time for transition.

Mode 5: t(3) < t < t(4) : Power transfer interval
The switches Q_B and Q_C are on, the voltage across the primary of the transformer is -V_{in}.

Mode 6: t=t(4) Turn off
The C_C is charged and the C_D is discharged enabling ZVS for Q_D.
The modes of operation will repeat in the same manner.

2.3 Phase shifted full bridge converter-current doubler on secondary

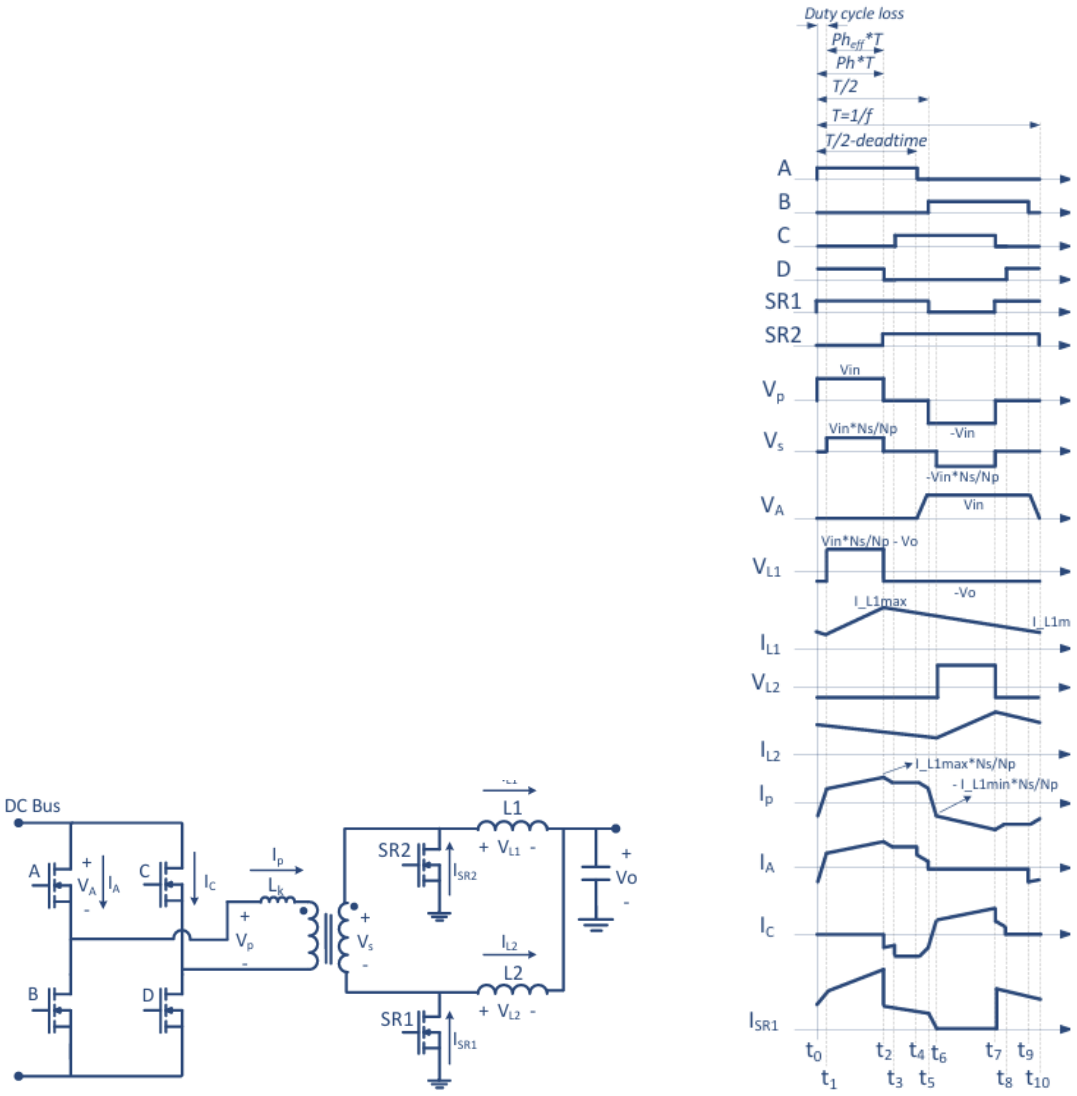


Figure 2.4: Circuit and waveforms of Phase shifted full bridge converter-current doubler on secondary[8]

The modes of operation of the phase shifted full bridge current doubler is explained in this section

Mode 1 :$t_0 - t_1$ Duty cycle loss mode At t=0 siwtch A is turned on with ZVS , V_s is zero , SR_1 and SR_2 will conduct , L_1 and L_2 are discharging , V_s will remain zero until the primary current's direction is reversed to reach the inductor current IL_1 at t=t1. No power is delivered to the output in this mode.

Mode 2: $t_1 - t_2$ Power delivery mode
At $t = t_1$ $V_s = \frac{V_{\text{in}}}{n}$, L_1 is charging , L_2 is discharging because of the positive half cycle . IL_1 completes its loop through transformer secondary winding and IL_2 discharges through SR_1.

Mode 3: $t_2 - t_3$ Switch C ZVS mode
At $t = t_2$ switch D is turned off , I_p charges the capacitance of D and discharges the capacitance of C. Once the capacitor is completely discharges the diode conducts so that the voltage across the switch is zero and then the switch C turns on. During this time both SR's will carry current.

Mode 4: $t_3 - t_4$ Freewheeling mode
At $t = t_3$ switch A and C are on and I_p freewheels, so the voltage across the primary and secondary of the transformer is zero. Both inductors discharge , L_1 through SR_2 and L_2 through SR_1.

Mode 5: $t_4 - t_5$ Switch B ZVS mode
At $t = 4$ switch A is turned off and I_p charges the output capacitance of A and discharges output capacitance of B. Once the capacitance is fully discharged the diode conducts and the switch B turns on with zero voltage across it. The voltage across the primary and secondary of the transformer is zero and hence both the inductors discharge.

Mode 6: $t_5 - t_6$ Duty cycle loss mode
At $t = t5$ switch B is turned on with ZVS now the current I_p changes direction and uses the voltage across transformer so there is duty cycle loss in the voltage appearing across V_s. SR_1 and SR_2 remain conducting and both inductor discharge . In this mode power is not delivered to the load.

2.4 Transformer design

From Faraday's law of electromagnetic induction we have :

$$V = N\frac{d\phi}{dt} \tag{2.1}$$

Where V is the voltage induced , N is the number of turns,$\frac{d\phi}{dt}$ is the rate of change of flux.
The total flux passing through the area of the core A_c is given by

$$\phi = BA_c \tag{2.2}$$

where B is the flux density So equation (2.1) can be written as

$$V = N_1 A_c \frac{dB}{dt} \tag{2.3}$$

The flux density is

$$B = \frac{1}{N_1 A_c}\int V dt \tag{2.4}$$

From this we can write

$$B = \frac{V_{\text{in}} D}{2 f_s N_1 A_c} \tag{2.5}$$

where B varies from $+B_{\max}$ to $-B_{\max}$
So N1 is given by

$$N_1 = \frac{V_{\text{in}} D}{2 B_m f_s A_c} \tag{2.6}$$

The window area where the primary and secondary coils will be placed is given by

$$A_w * k_w = N_1 * awp + N_2 * aws \tag{2.7}$$

Where k_w is the fill factor of the window area and a_w is the area of the wire in primary and seocndary and is given by

$$awp = \frac{I_{1,\text{rms}}}{J} \tag{2.8}$$

$$aws = \frac{I_{2,\text{rms}}}{J} \tag{2.9}$$

Substituting (2.8) and (2.9) in (2.7) we have

$$A_w k_w = \frac{V_{\text{in,min}} I_{1,\text{rms}} D_{\max}}{2 B_m f_s A_c J} + \frac{V_o I_{2,\text{rms}} D_{\max}}{2 B_m f_s A_c J} \tag{2.10}$$

$$A_p = A_w A_c = \frac{(V_{\text{in,min}} I_{1,\text{rms}} + V_o I_{2,\text{rms}}) * D_{\max}}{2 B_m f_s k_w J} \tag{2.11}$$

This equation gives an insight of the selection of the flux density of the core such that the area product is minimal. Which means the area occupied by the transformer is less [8],[11],[12].

2.4.0.1 Sizing of the conductor

From equations 2.8 and 2.9 we know the area of the primary and secondary winding to be used in the application. The diameter of the wire can be calculated by:

$$awp = \frac{\pi D^2}{4} \tag{2.12}$$

Considering the skin effect and proximity effect to calculate the resistance of the primary winding as follows:
For the primary winding we can find the resistance of the winding by considering the skin effect and proximity effect as follows: Skin depth is defined as

$$\delta_s = \sqrt{\frac{\rho}{\pi f_s \mu}} \tag{2.13}$$

where μ is permeability (H/m) , f_s is switching frequency (Hz), ρ conductivity Ωm. For a copper wire skin depth at $20^0 C$ is given by:

$$\delta_s = \frac{65.23}{\sqrt{f_s}} mm \tag{2.14}$$

Using litz wire to reduce the skin effect and proximity effect consisting of thin strands of wire twisted and wound together. The number of litz wire in a conductor is calculated by considering the skin depth. The area of each litz wire is given by:

$$A_{\text{cu}} = \pi \delta^2 \tag{2.15}$$

If diameter of the wire is greater than $2\delta_s$ litz wire has to be considered . The number of litz wire is calculated as follows :

$$N = \frac{awp}{A_{\text{cu}}} \tag{2.16}$$

2.4.0.2 Resistance of the primary and secondary winding

(a) The dc resistance of the winding is calculated as follows:

$$R = \frac{\rho l}{aw} \tag{2.17}$$

Where ρ is resistivity of the copper wire Ωm, l_p is the length of the conductor (m) and a_w cross section of the primary winding in mm^2 as mentioned in equation (2.8). The length of the conductor for primary winding calculated by:

$$l_p = N_p W \tag{2.18}$$

Where N is the number of turns in the primary , W is the perimeter of the transformer core.

(b) The resistance of the secondary winding is chosen and the area of the winding is calculated from 2.9. 2.17 is used to calculate the length of the winding.

2.5 Inductor design

The flux linking the inductor is given by:

$$L = \frac{\Psi}{I_{L,max}} \tag{2.19}$$

$$L = \frac{N * \phi}{I_{L,max}} \tag{2.20}$$

$$LI_{L,max} = N\phi \tag{2.21}$$

This equation can be written as

$$LI_{L,max} = NB_{max}A_c \tag{2.22}$$

Where A_c is the area of the core The winding area of the core that accommodates the windings is given by

$$W_a k_u = N a_w \tag{2.23}$$

We can calculate the number of turns as

$$N = \frac{W_a k_u}{a_w} \tag{2.24}$$

where a_w is the area of the wire and is given by

$$a_w = \frac{I_L, rms}{J} \tag{2.25}$$

where $k_u = 0.5$ and is known as fill factor The energy stored in an inductor is given by

$$E = \frac{1}{2} L(I_{\mathrm{L,max}})(I_{\mathrm{L,rms}}) \tag{2.26}$$

Substituting (52) and (53) in (50) we have

$$LI_{\mathrm{L,max}} = \frac{W_a k_u}{I_{\mathrm{L,rms}}} * B_{\max} * A_c J \tag{2.27}$$

$$LI_{\mathrm{L,max}} I_{\mathrm{L,rms}} = W_a k_u B_{\max} A_c J \tag{2.28}$$

This equation can be written as

$$2E = W_a k_u B_{\max} A_c J \tag{2.29}$$

The area product is given by

$$A_P = W_a A_c = \frac{2E}{k_u B_{\max} J} \tag{2.30}$$

Once the energy stored in the inductor is estimated from equation 2.19 we can choose the core with the area product slightly higher than the obtained value for the application [10],[11].

3

Design considerations

3.1 Phase shifted full bridge converter

In this chapter the design of the converter is explained in detail, relating to chapter 2 with the theory and equations obtained. The selection of switches according to the voltage stress, current stress, paralleling of switches to keep the junction temperature rise within 150^0C, design of magnetics is emphasized.

3.1.1 Design considerations

The voltage V_L when the diagonal switches are on the primary side is:

$$V_L = (\frac{1}{n}) * V_{\text{in}} - V_o \tag{3.1}$$

And during freewheeling the voltage across the inductor is

$$V_L = -V_o \tag{3.2}$$

3.1.1.1 Phase shift

The average voltage across the output inductor V_L is zero and hence by integrating it we get the phase shift as follows:

$$D = (\frac{V_o}{V_{\text{in}}}) * n \tag{3.3}$$

The converter is designed to handle peak power of 7500 W
The maximum effective phase shift occurs when the input voltage is minimum in our case 330 V, to accommodate worst case scenario 300 V is considered as the minimum input voltage.

(a) Considering 0.9 as the maximum phase shift in PSFB-FB and CT topologies.
(b) Considering 0.45 as the maximum phase shift in PSFB-CD topology.

Based on the number of turns of the transformer, the phase shift is calculated for the input range to obtain the regulated output of 15 V. The worst case scenarios of accommodating the output voltage range and input voltage range is tested.

3.1.1.2 Leakage inductance selection

The main aim is to drain the capacitance energy by the inductor energy and the minimum current required is

$$\frac{L_k I_{\text{pri}}^2}{2} = \frac{C_{\text{oss}} V_{\text{in,max}}^2}{2} \tag{3.4}$$

$$I_{\text{pri}} = \sqrt{\frac{C_{\text{oss}} V_{\text{in,max}}^2}{L_k}} \tag{3.5}$$

The output current is given by:

$$I_o = \frac{P_0}{V_0} \tag{3.6}$$

3.1.1.3 Output filter selection

To keep the rms current in the output capacitance to minimum L_{out} will be selected such that ripple current:

$$\Delta I_L out = I_{0,\text{max}} * 5\% \tag{3.7}$$

$$V_L = \frac{V_{\text{in,max}}}{n} - V_{\text{o}} \tag{3.8}$$

$$V_L = L\frac{di}{dt} \tag{3.9}$$

Based on this the output inductor value is calculated as follows:

$$L = \frac{V_L * DT_s}{\Delta I_L out} \tag{3.10}$$

The current through the inductor is given by

$$i_L = i_C + i_o \tag{3.11}$$

The average current through the capacitor is zero ie., $I_C = 0$ and the output voltage is a DC -voltage , the output current must be a pure DC-current

i_0=I_0 assuming pure resistive load. The average capacitor current can be calculated as

$$I_c = \frac{1}{T}\int_0^T (i_L(t)\,dt - I_0 = 0 \tag{3.12}$$

$$\frac{1}{T}\int_0^T i_L(t)\,dt = I_0 = I_L \tag{3.13}$$

This means that the average inductor current is equal to the output current so the ripple current in the inductor must go through the capacitor.

$$i_C = i_L(ripple) - I_L \tag{3.14}$$

Assuming the output voltage ripple to be 5% of the output voltage.

$$\Delta V_0 = 5\% * V_0 \tag{3.15}$$

Calculating the value of the output capacitor from this as follows:

$$i_c = C\frac{dv}{dt} \tag{3.16}$$

$$C = \frac{i_c * DT_s}{\Delta V_0} \tag{3.17}$$

3.1.1.4 Voltage stress on switches

The switches in the primary and secondary are chosen based on the voltage stress.

Table 3.1: Voltage stress on the switches

Topology	Primary Switches	Secondary Switches
FB	V_{in}	$\frac{V_{\text{in}}}{n}$
CT	V_{in}	$\frac{2V_{\text{in}}}{n}$
CD	V_{in}	$\frac{V_{\text{in}}}{n}$

The maximum phase shift in FB and CT topologies is 0.9 as the inductor is operating throughout. But the maximum phase shift in the CD topology is 0.45 as one inductor charges during one half cycle and the other discharges. So even though the voltage stress on the secondary MOSFET appears the same as in FB , it is the same as in CT configuration as the turns ratio is lower.

3.1.1.5 Synchronous rectification

The rectifier diodes in the secondary of the topologies are replaced with the MOSFET's to increase the efficiency. This is considered because when the diode conducts the forward voltage of the diode has to be considered but when it is replaced with a MOSFET, it is only the on state resistance ,$R_{\mathrm{ds,on}}$ and it is in terms of mΩ. Based on this paralleling of devices is also taken into consideration which in turn reduces the equivalent resistance.

3.1.1.6 Thermal consideration

The junction temperature rise in the switches is estimated as follows:

$$T_j = T_c + \Delta T \tag{3.18}$$

where T_c is the coolant temperature and ΔT is the rise in temperature of the switch. It is given as $\Delta T = P_{\mathrm{loss}} R_{\mathrm{th,jC}}$. Where P_{loss} includes conduction and switching loss of the switch , $R_{\mathrm{th,jC}}$ is junction to case thermal resistance as specified in the datasheet. The junction temperature of the switch is kept within 150^0C. The variation of $R_{\mathrm{ds,on}}$ of the switches with the increase in junction temperature rise is also taken into consideration for both primary and secondary switches. It is an iteration until the $R_{\mathrm{ds,on}}$ stabilizes. Paralleling of the devices in the secondary is considered based on the junction temperature rise. So, two MOSFET's in the secondary were paralleled in order to keep the junction temperature rise within 150^0C.

3.2 Converter specifications

3.2.1 Requirements of DC-DC Converters

The auxiliary power module in a car has it's requirement of its own and it is mentioned as below in table 3.2.

V_{in} (V)	V_o (V)	Continuous power (W)	Transient power (W)	Derating (V)	Withstand(V)
370-920	8-16	4000	7500 @1.5s	370-330,950-920	>920(950&1035)

Table 3.2: Requirements of DC-DC converter

3.2.1.1 Selection of leakage inductance

As mentioned in section 3.1.1.1 the leakage inductance is selected in such a way that Zero voltage switching (ZVS) for the primary is achieved at all the load ranges to reduce the switching losses as shown in table 3.3. The number of turns in the transformer as calculated from (3.3) is $n = 17$ for PSFB-FB and CT topologies and for PSFB-CD , $n = 8$.

Table 3.3: Selection of leakage inductance

Power (W)	R_{load} (Ω)	$L_{\text{k}}(\mu H)$	ΔD	D
7500	0.03	0.34	0.0003	0.9003
5000	0.045	0.7656	0.0005	0.90005
4000	0.056	1.196	0.0007	0.9007
3000	0.075	2.12	0.0009	0.9009
2500	0.1125	3.06	0.0014	0.901
1000	0.225	19.142	0.002	0.9028
500	0.45	76.56	0.005	0.9057

The leakage inductance is selected such that ZVS is achieved at continuous load and the maximum phase shift should be not more than 0.9.
The leakage inductance as tabulated in table 3.3 was chosen for continuous power as $L_k = 1.196\mu H$ .At lower loads the left legs switches loose ZVS as the output inductor current is at the valley and there is no room to charge and discharge the output capacitance of the switches , while ZVS is achieved in the right leg as there is much current to achieve ZVS.

3.2.1.2 Design table

The design parameters of the phase-shifted full bridge are as mentioned in Table 3.4 . The values mentioned in the table are used in the simulations. This is specified for the nominal voltage and peak power. The current changes with the change in input voltage and power.

3.2.1.3 Selection of primary and secondary switches

SiC MOSFET is chosen for the primary and Si MOSFET is chosen for the secondary. The $R_{\text{ds(on)}}$ should be less to minimize the conduction losses. The switching losses are mainly dependent on the switching frequency .
Two different switches were chosen because of the higher voltage stress in the CT and CD topology.

Table 3.4: Design table of PSFB

Parameters	FB	CT	CD
Output current (A)	500		500
Ripple current(A)	15		15
Ripple voltage(mV)	90		100
Secondary Peak current(A)	500		273
Secondary RMS current (A)	406	324	234
Primary Peak current (A)	31		34
Primary RMS current (A)	25		
Leakage inductance (μH)	1.19		
Magnetising inductance (μH)	600		825
Ouput inductor(μH)	3.527		
Minimum output capacitance(μF)	116		

Table 3.5: Primary MOSFET parameters

Parameter	Value
SiC MOSFET	SCT070HU120G3AG
V_{ds}	1200V
I_d	30A
$R_{\text{ds(on)}}$	63 m Ω
$V_{\text{gs(th)}}$	3V
C_{iss}	900pF
C_{oss}	40pF
C_{rss}	5pF
Q_g	37nC

Table 3.6: Secondary MOSFET parameters

	FB	CT and CD
Parameter	Value	Value
Si MOSFET	RS7N200BH	IPT025N15NM6
V_{ds} (V)	80	150
I_d (A)	230	263
$R_{\text{ds(on)}}$ (m Ω)	2	2.1
$V_{\text{gs(th)}}$(V)	4	3.5
C_{iss} (pF)	6550	7500
C_{oss} (pF)	1440	2300
C_{rss}(pF)	48	25
Q_g(nC)	92	105

4

Phase shifted full bridge converter

This chapter discusses about the implementation of phase shifted full bridge converter with all the three secondary topologies.

4.1 Implementation of the circuit in Simulink

The ideal switch model and ideal transformer are used to simulate the converter.

(a) The $R_{\mathrm{ds,on}}$ of the MOSFET could be manually entered in the switch model.

(b) The leakage inductance of the transformer as calculated in the section 3.2.1.1 could be entered in the transformer model. So a separate inductor is not considered in the model.

All the figures shown below are verified at peak load of 7500 W and nominal voltage 800 V

4.1.1 Phase shifted full bridge-full bridge on secondary

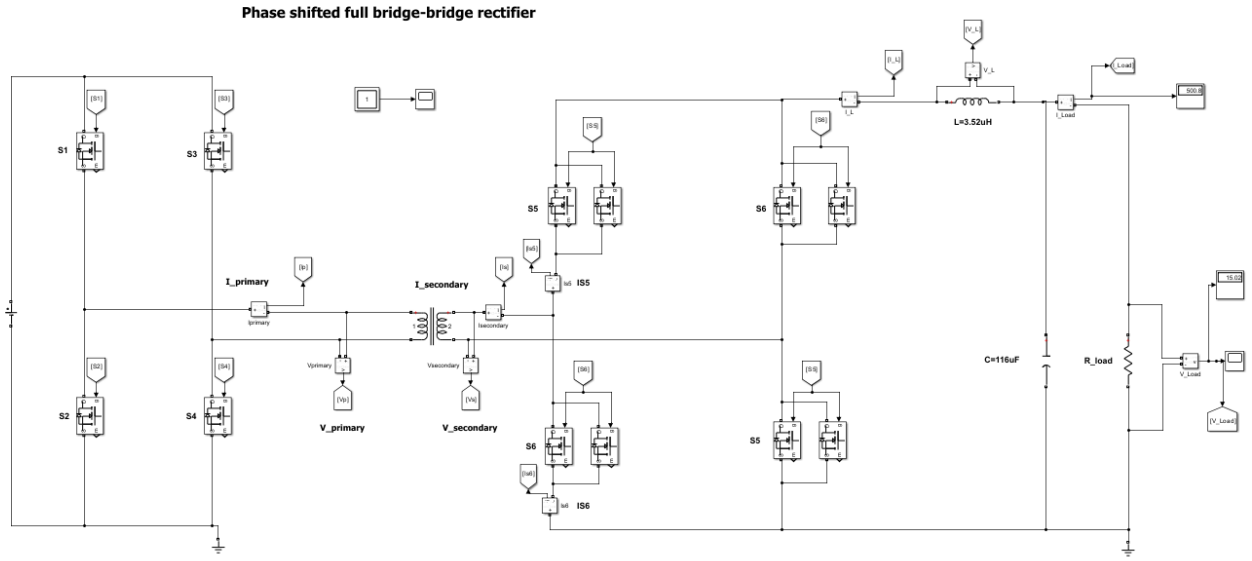


Figure 4.1: Circuit of PSFB-FB implemented in simulink

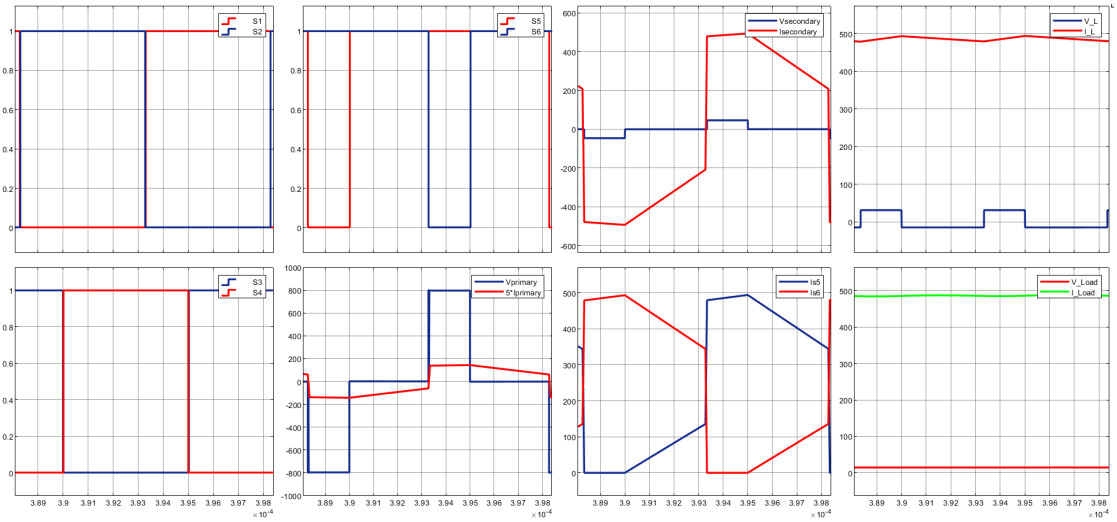


Figure 4.2: Waveforms of PSFB-FB obtained from circuit shown in figure 4.1

The Figure 4.1 shows the implementation of the phase shifted full bridge-full bridge on the secondary. Figure 4.2 shows the pulses that drive the switches indicated as $S1$,$S2$,$S3$,$S4$, $S5$, $S6$. V_{primary}, I_{primary} indicate the voltage and

current of the transformer primary and $V_{\text{secondary}}$, $I_{\text{secondary}}$ indicate the voltage and current of the transformer secondary. IS_5 and IS_6 indicate the switch currents through the switches 5 and 6. V_L is the voltage across the inductor and I_L is the current through the inductor. V_{load} and I_{load} are the output voltage and current delivered to the load. All these waveforms are verified in simulation and in theory as shown in Figure 2.1.

4.1.2 Phase shifted full bridge converter-center tap on secondary

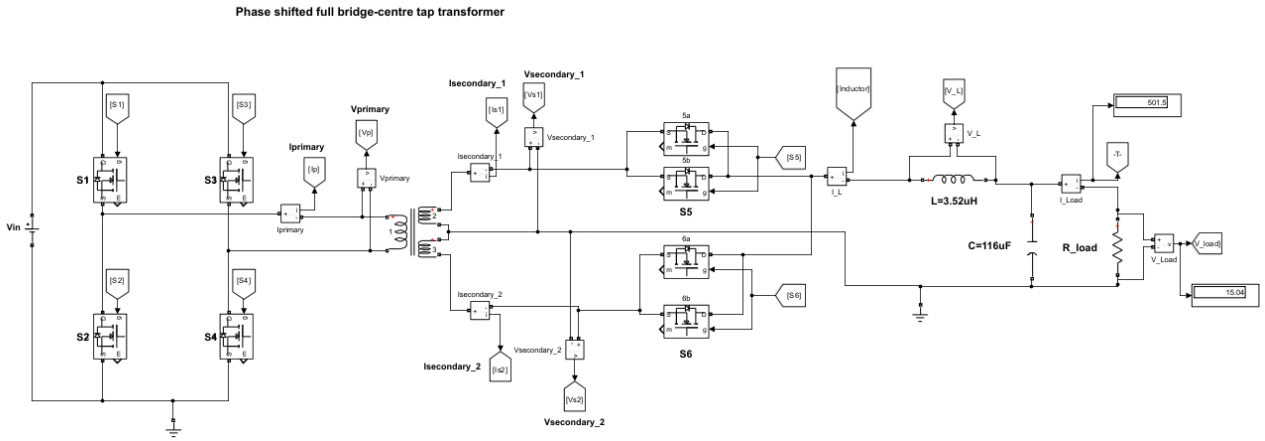


Figure 4.3: Circuit of PSFB-CT implemented in simulink

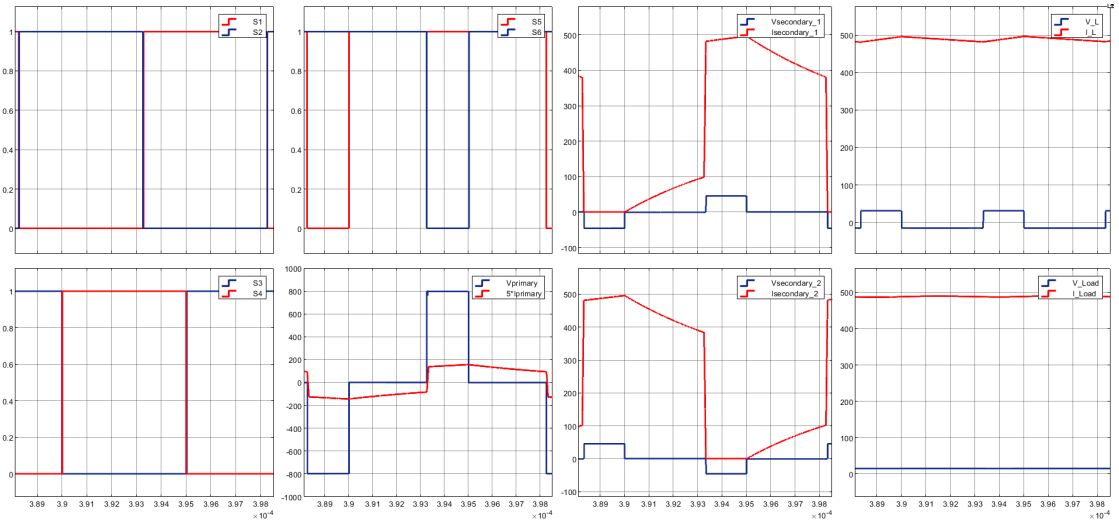


Figure 4.4: Waveforms of PSFB-CT obtained from circuit shown in figure 4.3

The Figure 4.3 shows the implementation of the phase shifted full bridge-center tap on the secondary. Figure 4.4 shows the pulses that drive the switches indicated as $S1$,$S2$,$S3$,$S4$, $S5$, $S6$. V_{primary} ,I_{primary} indicate the voltage and current of the transformer primary and $V_{\text{secondary}}$, $I_{\text{secondary}}$ indicate the voltage and current of the transformer secondary. The switch

currents through the switches 5 and 6 are the same as the transformer currents as they are series connected. V_L is the voltage across the inductor and I_L is the current through the inductor. All these waveforms are verified in simulation and in theory.

4.1.3 Phase shifted full bridge-current doubler on secondary

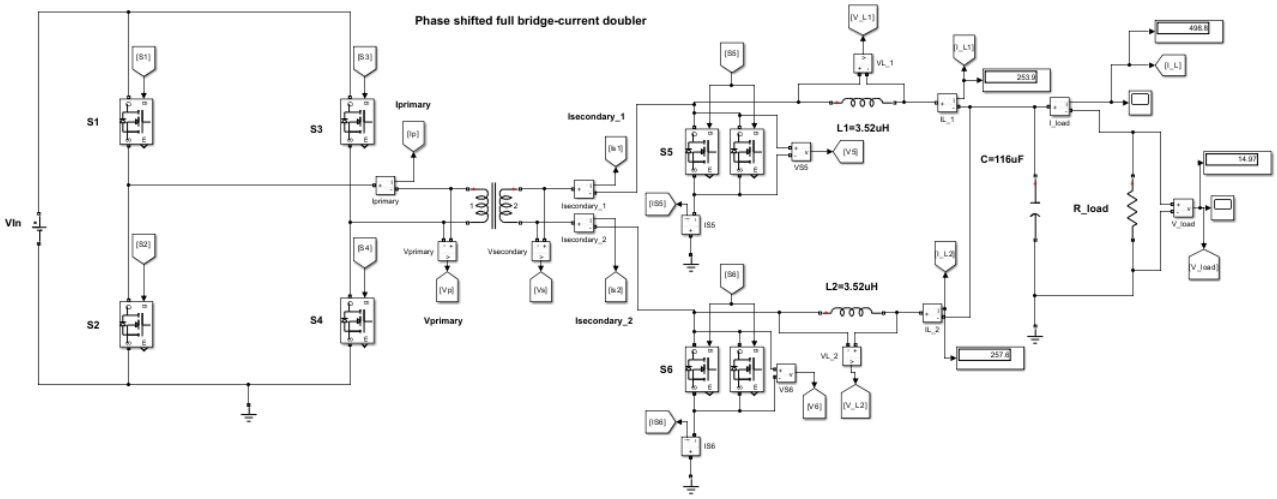


Figure 4.5: Circuit of PSFB-CD implemented in simulink

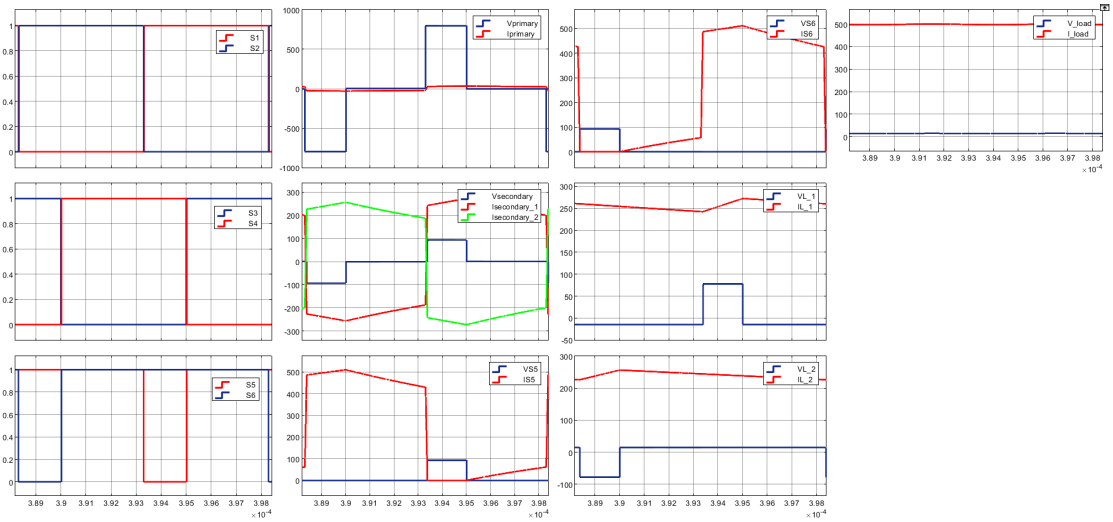


Figure 4.6: Waveforms of PSFB-CD obtained from circuit shown in figure 4.5

The Figure 4.5 shows the implementation of the phase shifted full bridge-current doubler on the secondary. Figure 4.6 shows the pulses that drive the switches indicated as $S1$,$S2$,$S3$,$S4$, $S5$, $S6$. V_{primary}, I_{primary} indicate the voltage and current of the transformer primary and $V_{\text{secondary}}$, $I_{\text{secondary}}$

indicate the voltage and current of the transformer secondary. The switch currents through the switches are indicated as IS_5 and IS_6. V_{L1}, V_{L2} are the voltages across the inductors 1 and 2 ,I_{L1}, I_{L2} are the currents through the inductors 1 and 2 respectively. V_{load} and I_{load} are the output voltage and current delivered to the load. V_{load} and I_{load} are the output voltage and current delivered to the load. All of these waveforms are verified in simulation and in theory as shown in figure 2.4.

4.2 Transformer details

4.2.1 Sizing of the conductor

Table 4.1: Conductor sizing

	AWG	Skin depth (mm)	Dpri(mm)	Acu(mm2)	awp(mm2)	N,litz	lp(m)	Rp	aws(mm2)	Rs	ls(m)
FB	19	0,412	0,912	0,6532	6,22	10	5	13,5	105	1	6,29
CT									77,55	1	9,23
CD							2	5,1	52	1	3

4.2.2 Resistance and length of the conductor

Topology	$R_p(\Omega)$	lp (m)	$R_s(\Omega)$	ls (m)
PSFB-FB	13,5	5	1	6,29
PSFB-CT				9,23
PSFB-CD	5,1	2		3

Table 4.2: Caption

4.2.3 Transformer core details

Table 4.3: Transformer core details

Transformer core details		
	FB & CT	CD
Magnetising inductance, L_m (μH)	600	825
Area of the core, A_c (mm^2)	388	417
Primary turns ,N_p	33	16
Secondary turns ,N_s	2	2
Volume of the core ,V_e (mm^3)	143600	102600
Peak magnetic flux density, B_m (mT)	100	
Resistance of the primary winding ,$R_p(m\Omega)$	14	5
Resistance of the secondary winding, R_s ($m\Omega$)	1	
Core type	E 80/38/20	00K5530E026
Materail	DMR95	

Two E-cores are used in order to complete the magnetic path for the transformer so the volume mentioned is for two E cores.

Topology	Aw,req (mm2)	Aw,avai (mm2)	Ap,req (mm4)	Ap,avai(mm4)
PSFB-FB	833	1079	272620	418652
PSFB-CT	1000		324500	
PSFB-CD	345	381	98421	158877

Table 4.1 gives the details of the design of the transformer and table 4.2 gives the area of the winding and area product. From these two tables following observations are made:
The area product required for PSFB-CD is approximately three times lesser compared to PSFB-FB and CT configurations. This means less area occupied on the PCB.

4.3 Inductor details

From table 4.1 and 4.2 it is clear that the area of the core is approximately 3 times bigger than the transformer because the area product is dependant on the energy stored in the inductor as derived in section2.5.
In all the three topologies the same inductor is used it means that in the CD topology there are two output inductors and the area occupied on the PCB is quite . But seperate inductor is supposed to be designed for CD topology

Table 4.4: Details of the inductor

Inductance (μH)	3.527
Area of the core, A_c (mm^2	1225
Volume of the core ,V_e (mm^3)	491200
Peak magnetic flux density, B_m (mT)	100
Resistance of the winding, R_l ($m\Omega$)	1
Number of turns , (N_l)	3
Air gap , (mm)	2.5
Core type	EE140/86/35
Material	DMR95

Table 4.5: Details of the window and area product of the inductor

Aw,req(mm2)	Aw,avai(mm2)	Ap,req(mm4)	Ap,avai(mm4)
658	4830	1539555	5916750

4.4 Loss analysis of the converters

In this section, the currents at various inputs and loads are tabulated for all the converters and the losses, efficiencies are estimated.The following are valid as the input voltage increases:

(a) The rms currents decrease and the conduction losses in the switches decrease.

(b) The copper losses in the transformer will decrease while the iron loss will remain the same at a particular voltage.

(c) The switching losses will increase

4.4.1 PSFB-FB

Table 4.6: Currents at various inputs at 7500W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)		IL,rms(A)
370/15/7500	20,47	25,6	28	476	168,8	168,8	497
	18,7	23,7			165	165	
	19,28	28,3			165	165	
	19,94	32			168,8	168,8	
600/15/7500	18,8	18	25	432	157,3	157,3	497
	17,36	16,6			162,9	162,9	
	18,06	29,74			162,9	162,9	
	18,14	32			157,3	157,3	
800/15/7500	17,42	14,6	24,17	406	155	155	497
	16,41	14,71			153,5	153,5	
	17,47	32			153,5	153,5	
	16,43	33,33			155	155	
920/15/7500	17	15	23,48	393	152	152	497
	16	12,4			150	150	
	16,8	29,2			150	150	
	16,18	30,6			152	152	

Table 4.7: Currents at various inputs at 4000W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)		IL,rms(A)
370/15/4000	10,78	15,5	14,5	239,8	86,57	86,57	264
	8,9	12,8			86,57	86,57	
	10,53	15,8			86,57	86,57	
	9,28	15,8			86,57	86,57	
600/15/4000	10,53	9,8	13,81	227	85,69	85,69	264
	9,16	8,22			87	87	
	9,9	16			87	87	
	9,7	17			85,69	85,69	
800/15/4000	9,9	8,7	13,35	217	84	84	264
	8,69	6,6			84,4	84,4	
	9,5	15,78			84,4	84,4	
	9	18,6			84	84	
920/15/4000	9,6	10,2	13	209	82,8	82,8	264
	8,81	6,2			84,6	84,6	
	9,7	16,2			84,6	84,6	
	8,73	16,7			82,8	82,8	

Table 4.8: Currents at various inputs at 2000W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)		IL,rms(A)
370/15/2000	5,25	7,36	7,48	129,3	46,09	46,09	132,7
	5,32	7,47			46,57	46,57	
	5,33	8,19			46,57	46,57	
	5,25	8,12			46,09	46,09	
600/15/2000	5,7	6,6	7,2	114	42,3	42,3	132,7
	4,66	4,6			43,8	43,8	
	5,33	8,5			43,8	43,8	
	4,9	9,9			42,3	42,3	
800/15/2000	5,6	5,3	7	107	41,9	41,9	132,7
	4,35	3,5			41,8	41,8	
	5,2	8			41,8	41,8	
	4,72	10			41,9	41,9	
920/15/2000	5,57	5,44	6,9	105	41,46	41,46	132,7
	4,2	3			42,18	42,18	
	5,24	8,6			42,18	42,18	
	4,67	10,7			41,46	41,46	

Table 4.9: Currents at various inputs at 1000W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)		IL,rms(A)
370/15/1000	3,4	3,5	4,4	54,8	20,6	20,6	66,19
	2,2	2,15			21,6	21,6	
	3,2	4,6			21,6	21,6	
	2,6	6,4			20,6	20,6	
600/15/1000	3,5	4,2	4,2	54	21,24	21,24	66,1
	2,3	2,4			22,17	22,17	
	3,12	4,29			22,17	22,17	
	2,8	6,7			21,24	21,24	
800/15/1000	3,5	4,2	4,09	53	20,8	20,8	66
	2,3	2,1			21,46	21,46	
	3,1	4,3			21,46	21,46	
	2,6	7			20,8	20,8	
920/15/1000	2,4	3,48	3,53	52	20,6	20,6	66
	2,59	3,61			21,6	21,6	
	2,43	4,5			21,6	21,6	
	2,56	4,5			20,6	20,6	

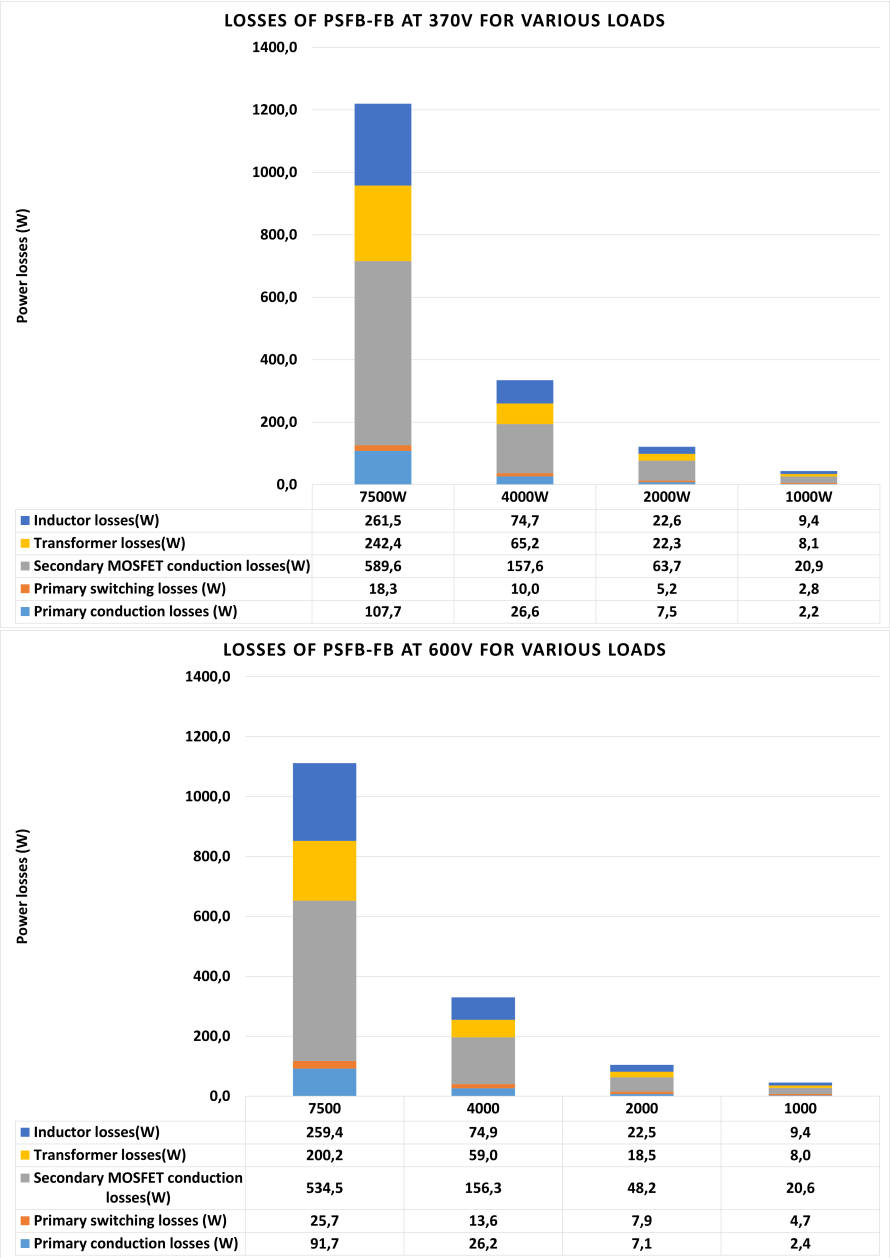


Figure 4.7: Losses of PSFB-FB at various loads for 370V and 600V input

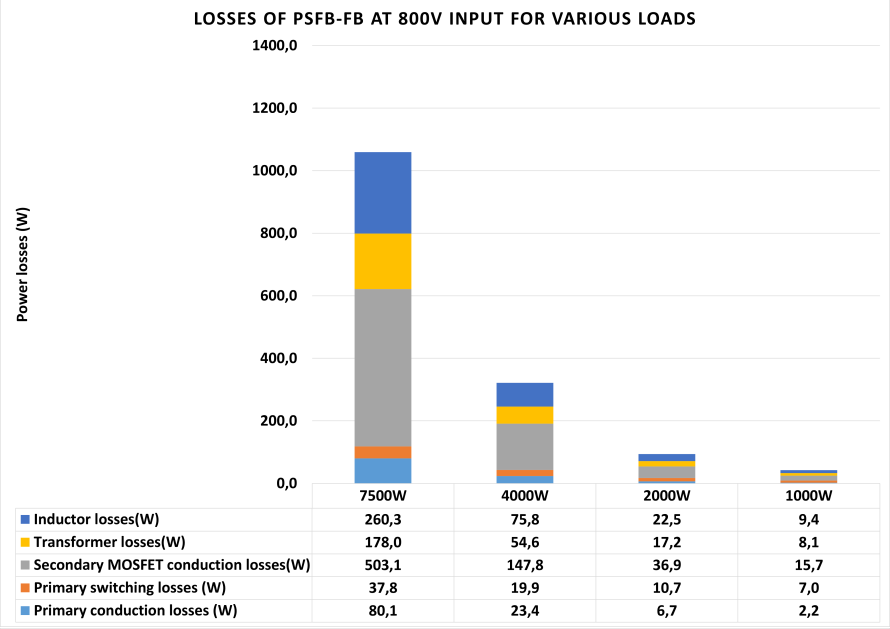


Figure 4.8: Losses of PSFB-FB at various loads for 800V and 920V input

Table 4.10: Transformer currents

Po(W)	Vin (V)	Ip,pk(A)	Ip,rms(A)	Is,pk(A)	Is,rms(A)
7500	370,0	31,0	28,0	500,0	476,0
	600,0	31,9	25,0	504,0	432,0
	800,0	31,7	24,2	502,0	406,0
	920,0	31,7	23,5	505,0	393,0
4000	370,0	15,7	14,5	270,2	239,8
	600,0	19,3	13,8	271,0	227,0
	800,0	18,3	13,4	273,9	217,0
	920,0	18,3	13,0	275,0	209,0
2000	370,0	7,9	7,5	136,6	129,3
	600,0	10,5	7,2	139,0	114,0
	800,0	10,5	7,0	140,9	107,0
	920,0	10,6	6,9	141,0	105,0
1000	370,0	6,7	4,4	74,6	54,8
	600,0	6,7	4,2	72,9	54,0
	800,0	6,7	4,1	73,9	53,0
	920,0	4,5	3,5	74,6	52,0

Table 4.11: Transformer losses

Po(W)	Core Loss(W)	Pcu,pri(W)	Pcu,sec(W)	Total Loss(W)
7500	4.8	11.0	226.6	242.4
	4.8	8.8	186.6	200.2
	5.0	8.2	164.8	178.0
	5.0	7.7	154.4	167.2
4000	4.8	2.9	57.5	65.2
	4.8	2.7	51.5	59.0
	5.0	2.5	47.1	54.6
	5.0	2.4	43.7	51.1
2000	4.8	0.8	16.7	22.3
	4.8	0.7	13.0	18.5
	5.0	0.7	11.4	17.2
	5.0	0.7	11.0	16.7
1000	4.8	0.3	3.0	8.1
	4.8	0.2	2.9	8.0
	5.0	0.2	2.8	8.1
	5.0	0.3	2.7	8.0

Table 4.12: Inductor currents and Losses

Po (W)	Vin(V)	IL,rms	Core loss(W)	Pcu(W)	Total loss(W)
7500	370	497,00	14,73	247,01	261,74
	600				
	800				
	920				
4000	370	264,00	5,00	69,70	74,70
	600				
	800				
	920				
2000	370	132,70	5,00	16,72	21,72
	600				
	800				
	920				
1000	370	66,19	5,00	3,00	8,00
	600				
	800				
	920				

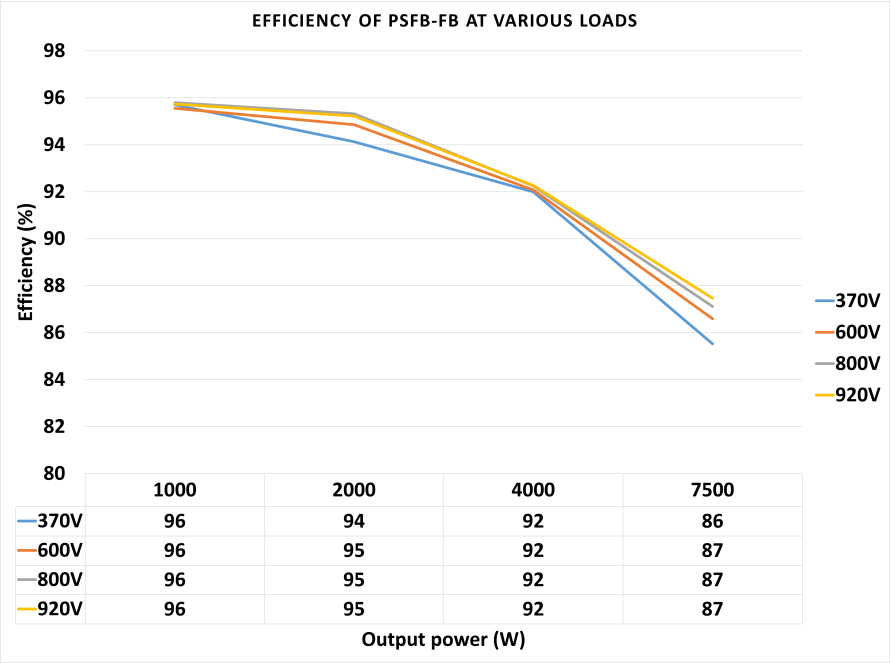


Figure 4.9: Efficiency of PSFB-FB

4.4.2 PSFB-CT

Table 4.13: Current at various input at 7500W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)	IL,rms(A)
370/15/7500	20,15	24,64	27,9	349	168,7	497
	18,03	22,6			168,7	
	18,75	28		349	171	
	19,47	29			171	
600/15/7500	19,09	22,7	26,25	333	164	497
	17,91	16,8			164	
	19,25	30,7		330	162	
	17,7	30,8			162	
800/15/7500	18,67	18,6	25,2	324,5	159	497
	17,13	17,6			159	
	18,18	29,3		324,5	161	
	17,6	33			161	
920/15/7500	18,48	18,11	25,2	322	159	497
	17,02	18,8			159	
	18,19	28,05		322	160	
	17,3	32,4			160	

Table 4.14: Current at various input at 4000W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)	IL,rms(A)
370/15/4000	11,73	15,34	15,28	185	91,71	264
	9,85	15,34			91,71	
	10,63	15,34		185	91,2	
	11,03	17,7			91,2	
600/15/4000	11	12,9	14,46	179	88,19	264
	9,3	11,4			88,19	
	10,5	14,9		179	89,15	
	10,1	18,96			89,15	
800/15/4000	10,13	10,6	14,1	175	87,1	264
	9,65	9,6			87,1	
	10,3	16,3		175	87,3	
	9,5	18,6			87,3	
920/15/4000	10,46	10,08	13,9	173,2	86,4	264
	9,12	8,5			86,4	
	10,21	16,8		173,2	86,9	
	9,39	18,23			86,9	

Table 4.15: Current at various input at 2000W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)	IL,rms(A)
370/15/2000	6,42	8,7	7,92	92,9	46,24	133
	4,7	7			46,24	
	5,3	9,45		92,9	46,24	
	5,9	10,4			46,24	
600/15/2000	6,07	7,8	7,7	90	44,21	133
	4,7	5,7			44,21	
	5,5	8,5		89,42	44,4	
	5,2	10			44,4	
800/15/2000	6,1	7	7,5	87,74	43,5	133
	4,5	4,9			43,5	
	5,6	8,2		87,74	44,2	
	5	10			44,2	
920/15/2000	6,12	6,8	7,5	86,77	43,4	133
	4,5	4,8			43,4	
	5,7	8,4		86,77	43,9	
	5	11,16			43,9	

Table 4.16: Current at various input at 1000W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)	IL,rms(A)
370/15/1000	3,7	5,2	4,28	46,89	23	65,6
	2,23	3,9			23	
	2,87	4,9		46,89	23,5	
	3,1	6,8			23,5	
600/15/1000	2,5	2,49	3,5	45,65	22,12	65,6
	2,48	2,55			22,12	
	2,53	4,23		45,65	22,12	
	2,49	4,4			22,12	
800/15/1000	3	4,45	4,38	44,3	22	65,6
	2,3	3			22	
	2,3	4,8		44,3	22,4	
	2	6,5			22,4	
920/15/1000	2,2	4	4,4	44,5	22	65,6
	2,3	2,9			22	
	2,2	5,2		44,5	22,4	
	2,2	6,18			22,4	

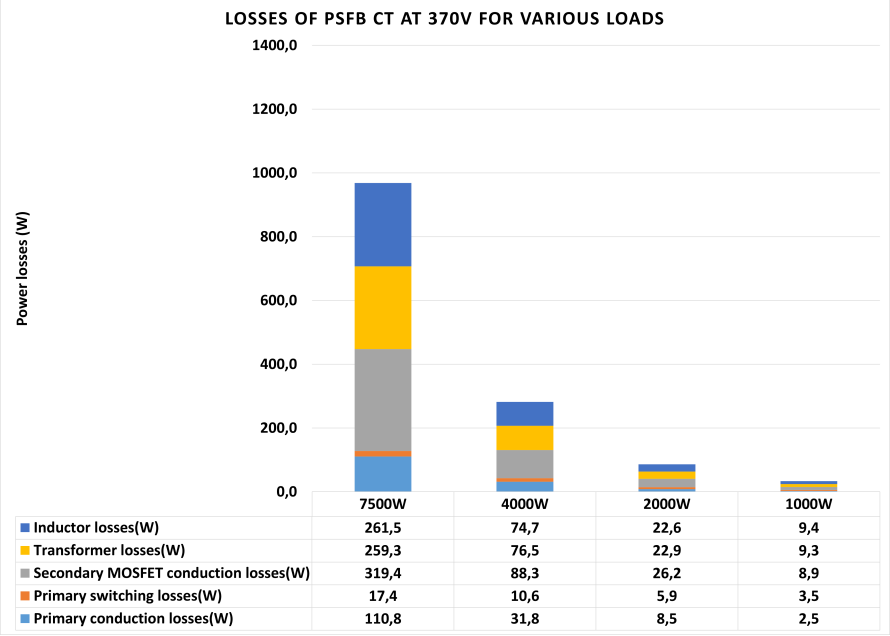


Figure 4.10: Losses of PSFB-CT at various loads for 370V and 600V input

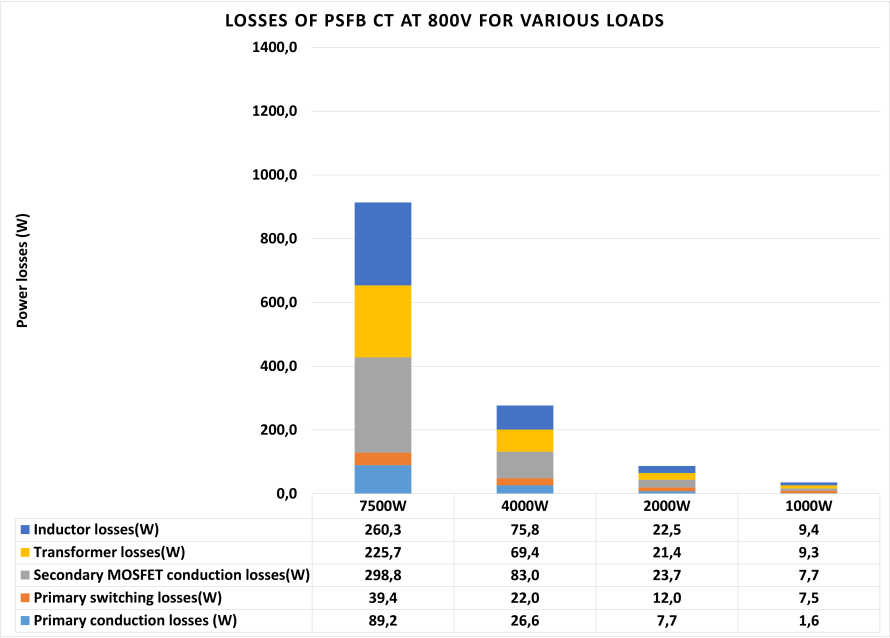


Figure 4.11: Losses of PSFB-CT at various loads for 370V and 600V input

Table 4.17: Transformer currents

Po(W)	Vin (V)	Ip,pk(A)	Ip,rms(A)	Is,pk(A)	Is1,rms(A)	Is2,rms
7500	370	31,7	27,9	500,0	349,0	343,0
	600	31,8	26,3	502,0	333,0	330,0
	800	31,6	25,2	501,0	324,5	326,4
	920	32,0	25,2	506,0	322,0	322,0
4000	370	18,3	15,3	269,0	185,0	185,0
	600	18,5	14,5	273,0	179,0	179,0
	800	18,1	14,1	274,3	176,0	176,0
	920	18,2	13,9	174,0	173,2	172,0
2000	370	10,6	7,9	136,0	92,9	92,5
	600	10,5	7,7	138,8	90,0	89,4
	800	10,7	7,5	140,5	87,7	88,6
	920	10,8	7,5	141,1	86,8	88,2
1000	370	6,3	4,3	69,0	46,9	45,7
	600	4,2	3,5	64,6	43,4	45,7
	800	6,5	4,4	74,0	44,3	44,9
	920	6,3	4,5	74,6	44,5	44,8

Table 4.18: Transformer losses

Po(W)	Core Loss(W)	Pcu,pri(W)	Pcu,sec(W)	Total Loss(W)
7500	4,8	10,8	243,6	259,3
	4,8	9,6	219,8	234,2
	5,0	8,9	211,8	225,7
	5,0	8,9	207,4	221,3
4000	4,8	3,2	68,5	76,5
	4,8	2,9	64,1	71,8
	5,0	2,8	61,6	69,4
	5,0	2,7	59,6	67,3
2000	4,8	0,9	17,2	22,9
	4,8	0,8	16,1	21,7
	5,0	0,8	15,5	21,4
	5,0	0,8	15,3	21,1
1000	4,8	0,3	4,3	9,3
	4,8	0,3	4,0	8,9
	5,0	0,3	4,0	9,3
	5,0	0,3	4,0	9,3

Table 4.19: Inductor currents and losses

Po (W)	Vin(V)	IL,rms	Core loss(W)	Pcu(W)	Total loss(W)
7500	370	497	14,73	247,009	261,739
	600				
	800				
	920				
4000	370	264	5	69,696	74,696
	600				
	800				
	920				
2000	370	133,33	5	17,777	22,777
	600				
	800				
	920				
1000	370	65,6	5	4,303	9,303
	600				
	800				
	920				

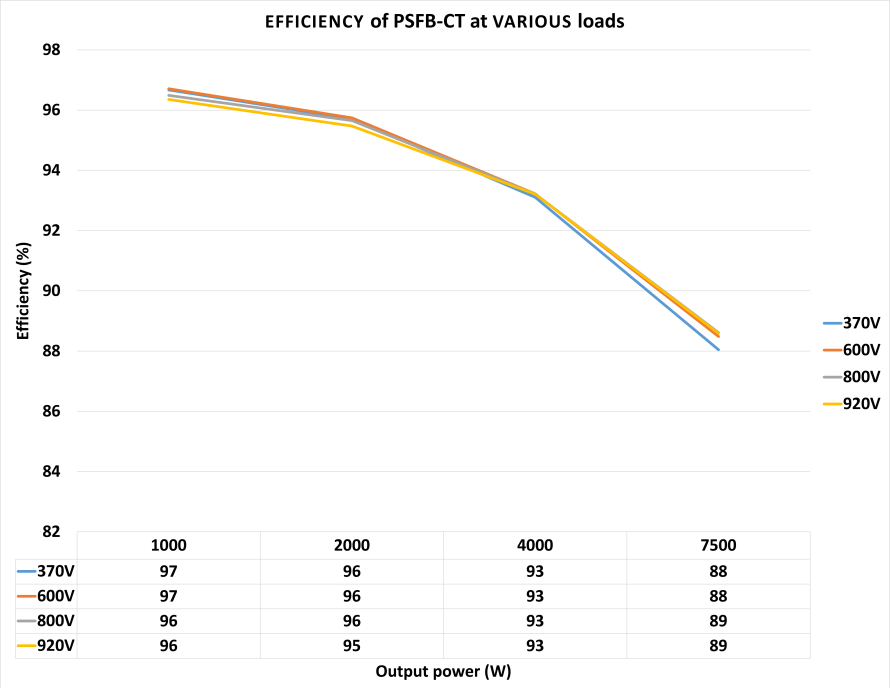


Figure 4.12: Efficiency of PSFB-CT

4.4.3 PSFB-CD

Table 4.20: Current at various input at 7500W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)	IL,rms(A)
370/15/7500	21,99	29,55	28,96	243	173	256
	19,1	26,46			173	
	20	29			167	242
	20,93	33			167	
600/15/7500	21,69	25,7	28,45	236	169	256
	18,69	22,6			169	
	20,36	28,4			169	242
	20,12	34,5			169	
800/15/7500	21,39	24,99	24	234,4	163	256
	18,46	24,11			163	
	20,53	29			163	242
	19,4	33			163	
920/15/7500	21,24	30,3	25,43	232	164	256
	18,48	29,88			164	
	20,54	29			164	242
	19,22	29			164	

Table 4.21: Current at various input at 4000W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)	IL,rms(A)
370/15/4000	12,7	18,4	17	131,9	92,8	141
	9,8	14,6			92,8	
	10,91	15,65			92,4	125
	11,8	20			92,4	
600/15/4000	11,1	16,6	16,21	129	91,6	141
	9,98	12,8			91,6	
	11,6	16,5			91,4	125
	11,23	20			91,4	
800/15/4000	11	15,7	16	128,7	90,8	141
	10	12			90,8	
	11	17,2			90	125
	10,9	20			90	
920/15/4000	10	16,4	15,77	127	87,85	141
	10,94	15			87,85	
	11	16			87,85	125
	10,7	16,6			87,85	

Table 4.22: Current at various input at 2000W

Vin(V)/Vo(V)/Po(W)	Im,rms(A)	I,off(A)	Ip,rms(A)	Is,rms(A)	ISR,rms(A)	IL,rms(A)
370/15/2000	7,3	10,25	8,6	68,27	46,55	71,3
	4,7	7,6			46,55	
	5,8	8,7			46,27	60,82
	6,4	12,6			46,27	
600/15/2000	7,29	9,5	9	68	46,18	71,3
	5,4	7,9			46,18	
	6,6	9,1			45,73	60,82
	6,1	12,16			45,73	
800/15/2000	7,3	10	9	68	46	71,3
	5	6,2			46	
	6	9,7			45,5	60,82
	5	12,6			45,5	
920/15/2000	5,8	8,6	7,9	67,35	45	71,3
	5,3	7,9			45	
	5,8	7,9			46	60,82
	5,4	8,4			46	

Table 4.23: Current at various input at 1000W

Vin(V)/Vo(V)/Po(W)	Imrms(A)	Ion(A)	Ioff(A)	Iprms(A)	Isrms(A)	ISRrms(A)	ILrms(A)
370/15/1000	4,3	2,5	7,2	5	36	23,49	39
	3,2	0	4,9			23,49	
	3,45	0	5,3			23,2	28,61
	4	2,6	7,8			23,2	
600/15/1000	4	2,13	6,3	5,55	37,99	23,3	38
	3	0	4,5			23,3	
	3	0	5,8			23,5	30,8
	3,7	2	8,4			23,5	
800/15/1000	3	1,7	6	5	38,7	23,6	36,5
	3	0	5			23,6	
	3	0	6,3			23,3	32,5
	3,7	1,9	7,6			23,3	
920/15/1000	2,7	4,5	3,3	3,57	29,8	23	33,8
	2,36	0	2,8			23	
	2,6	0	4,3			23	32,43
	2,44	3,8	4,47			23	

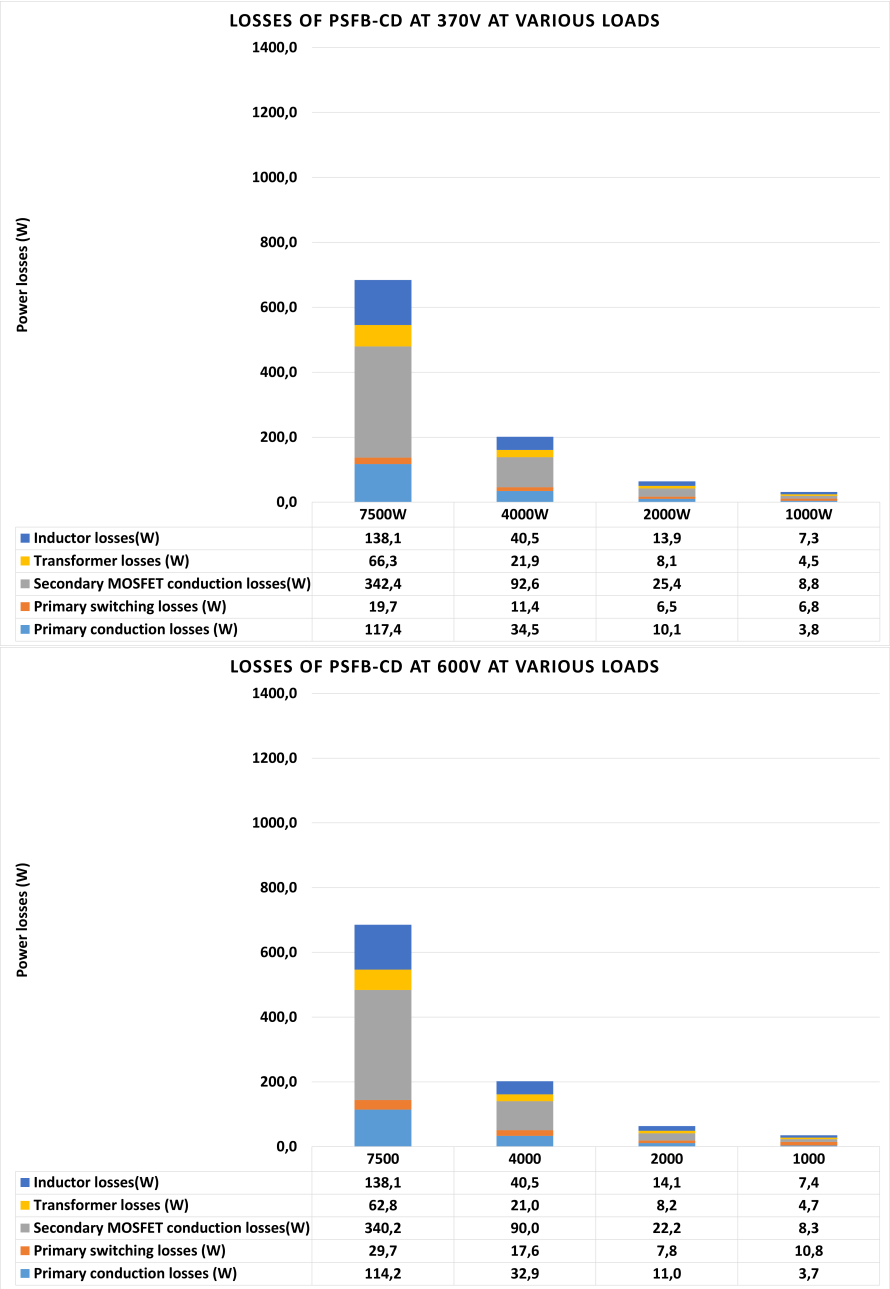


Figure 4.13: Losses of PSFB-CD at various loads for 370V and 600V input

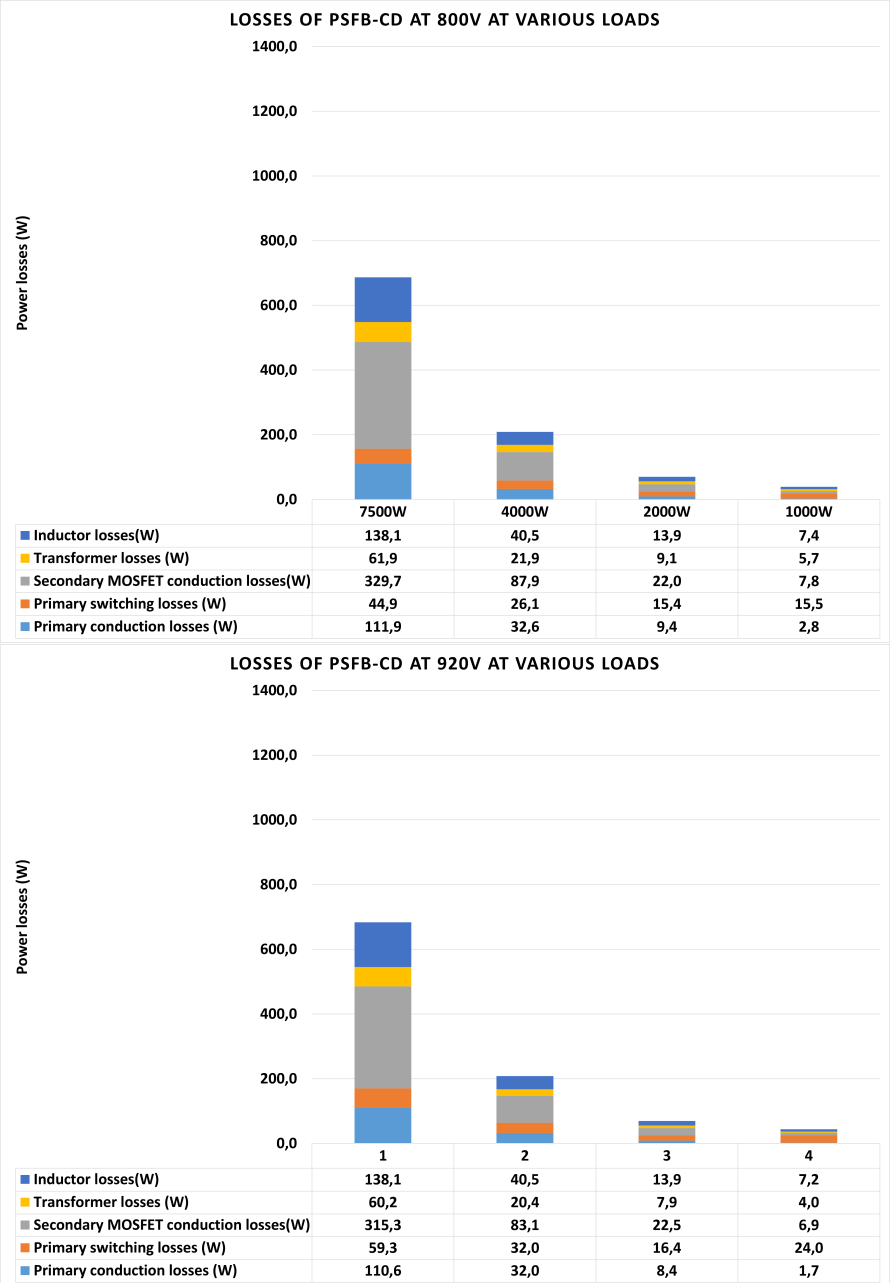


Figure 4.14: Losses of PSFB-CD at various loads for 800V and 920V input

Table 4.24: Transformer currents

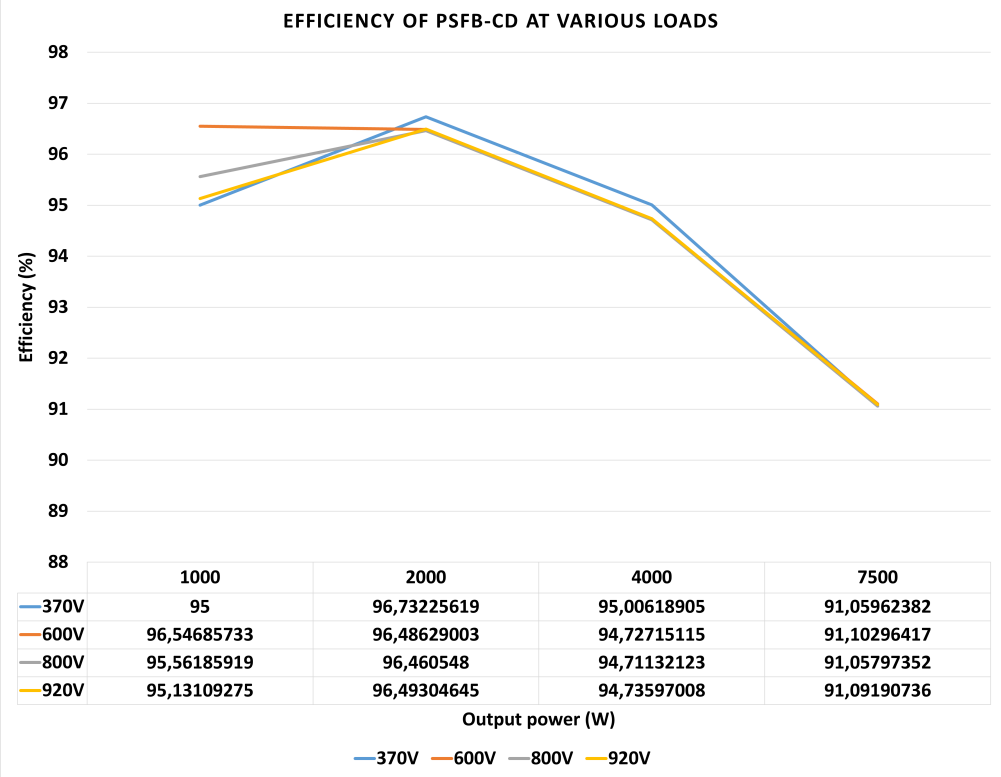
Po(W)	Vin (V)	Ip,pk(A)	Ip,rms(A)	Is,pk(A)	Is,rms(A)
7500	370	34,0	29,0	268,0	243,0
	600	31,5	25,4	267,0	232,0
	800	34,0	24,0	273,0	234,4
	920	34,5	28,5	271,0	236,0
4000	370	20,3	17,0	151,0	131,9
	600	16,9	15,8	142,9	127,0
	800	20,7	16,0	155,0	128,7
	920	20,8	16,2	154,0	129,0
2000	370	12,4	8,6	85,2	68,3
	600	8,5	7,9	71,5	67,4
	800	12,2	9,1	86,0	68,0
	920	12,9	9,0	87,0	68,8
1000	370	8,0	5,0	49,0	36,0
	600	4,4	3,6	36,0	29,8
	800	7,7	5,0	50,8	38,7
	920	8,0	5,6	49,8	38,0

Table 4.25: Transformer losses

Po (W)	Pi (W)	Pcu,pri (W)	Pcu,sec (W)	Ptotal (W)
7500	3,1	4,2	59,0	66,3
	3,1	3,3	53,8	60,2
	4,1	2,9	54,9	61,9
	3,1	4,0	55,7	62,8
4000	3,1	1,4	17,4	21,9
	3,1	1,2	16,1	20,4
	4,1	1,3	16,6	21,9
	3,1	1,3	16,6	21,0
2000	3,1	0,4	4,7	8,1
	3,1	0,3	4,5	7,9
	4,1	0,4	4,6	9,1
	3,1	0,4	4,7	8,2
1000	3,1	0,1	1,3	4,5
	3,1	0,1	0,9	4,0
	4,1	0,1	1,5	5,7
	3,1	0,2	1,4	4,7

Table 4.26: Inductor currents and losses

Po (W)	Vin(V)	IL,rms	Core loss(W)	Pcu(W)	Total loss(W)
7500	370	256	7	65,536	72,536
		242		58,564	65,564
	600	256	7	65,536	72,536
		242		58,564	65,564
	800	256	7	65,536	72,536
		242		58,564	65,564
	920	256	7	65,536	72,536
		242		58,564	65,564
4000	370	141,000	2,5	19,881	22,381
		125		15,625	18,125
	600	141,000	2,5	19,881	22,381
		125		15,625	18,125
	800	141,000	2,5	19,881	22,381
		125		15,625	18,125
	920	141,000	2,5	19,881	22,381
		125		15,625	18,125
2000	370	72,28	2,5	5,22	7,72
		60,82		3,70	6,20
	600	71,3	2,5	5,08	7,58
		60		3,60	6,10
	800	72	2,5	5,18	7,68
		60,82		3,70	6,20
	920	72	2,5	5,18	7,68
		60,82		3,70	6,20
1000	370	39	2,5	1,52	4,02
		28,61		0,82	3,32
	600	38	2,5	1,44	3,94
		30,8		0,95	3,45
	800	36,5	2,5	1,33	3,83
		32,2		1,04	3,54
	920	33,8	2,5	1,14	3,64
		32,43		1,05	3,55



	1000	2000	4000	7500
370V	95	96,73225619	95,00618905	91,05962382
600V	96,54685733	96,48629003	94,72715115	91,10296417
800V	95,56185919	96,460548	94,71132123	91,05797352
920V	95,13109275	96,49304645	94,73597008	91,09190736

Figure 4.15: Efficiency of PSFB-CD

(a) The tables $4.6 - 4.9$, 4.13-4.16 ,4.20-4.23 indicate the MOSFET rms currents denoted by Im, rms and ISR, rms on the primary and secondary side respectively constituting for conduction losses $I, rms^2 * R_{\text{ds,on}}$ note that there are 8 MOSFETS's on the secondary side of PSFB-FB. I, off indicates the turn off currents on the primary side MOSFET's. Ip, rms and Is, rms are the primary and secondary transformer currents. IL, rms is the rms current through the inductor which is helpful in calculating the copper losses in the inductor. The currents were taken for various inputs and for load conditions, as explained previously.

(b) Figures 4.7 - 4.8, 4.10-4.11 ,4.13-4.14 indicate complete losses in the PSFB-FB, PSFB-CT and PSFB-CD respectively including primary MOSFET conduction and switching losses. Secondary MOSFET conduction losses. Transformer and inductor copper and core losses. The switching losses in the primary MOSFEt's are calculated by taking the energy losses from the data sheet of the MOSFET.

(c) Table 4.10,4.17,4.24 indicate the transformer currents where Ip, pk , Ip, rms indicate primary transformer peak and rms currents respectively. Is, pk , Is, rms indicate the secondary transformer peak and rms currents respectively. Table 4.11,4.18,4.25 indicate the losses in the transformer with core and copper losses (Primary and secondary)

(d) Table 4.12,4.19,4.26 indicates the inductor rms current,IL, rms and the losses in the inductor such as core and copper losses . Figure 4.10, 4.12,4.15 shows the efficiency of the PSFB-FB,PSFB-CT and PSF-CD respectively at various loads and input voltages . We can observe that the efficiency drops as the load increases this is because the conduction losses increase with increase in load as the RMS currents increase.

5

Topology comparison

This chapter discusses about the comparison of all the secondary topologies implemented based on theory , currents, losses and efficiency at various loads and input voltages

5.1 Comparison of converters

Table 5.1: Theoretical comparison of converters

	FB	CT	CD
Maximum phase shift	0,9		0,45
Number of switches in primary	4		
Number of switches in secondary	8	4	
Number of secondary winding	1	2	1
Transformer utilization	High	Low	High
Secondary transformer currents	Full load		Half load
Size of the transformer	Larger		Smaller
Voltage stress on secondary MOSFET's	$\frac{V_{\text{in}}}{n}$	$\frac{2V_{\text{in}}}{n}$	$\frac{V_{\text{in}}}{n}$ (same as that of CT)
Tunrs ratio	n	n	n/2 (Half of FB and CT)
Inductors	1(Carries full load current)		2 (Carries half of the load current)
Inductor operating frequecny	Twice the primary switching frequency , $2f_s$		Same as the primary switching frequency, f_s
Size of inductor	Larger		Smaller

The table below shows the comparison of the currents of all the topologies at a nominal input voltage of 800 V and full load 7500 W.

Table 5.2: Comparison of the currents in the converters

	Vin(V)/Vo(V)/Po(W)	Ipri,mos,rms(A)	Ip,rms(A)	Ip,pk(A)	Is,pk(A)	Is,rms(A)	Isr,rms(A)		Il,rms(A)
FB	800/15/7500	17,42	24,17	31,66	502	406	155	155	497
		16,41					153,5	153,5	
		17,47					153,5	153,5	
		16,43					155	155	
CT	800/15/7500	18,67	25,2	31,6	501	326,5	159		496,7
		17,13					159		
		18,18				326,5	161		
		17,6					161		
CD	800/15/7500	21,39	28	34	273	234,4	168		256
		18,46					168		
		20,53					168		242
		19,4					168		

The following observations are made from the tables 5.1 and 5.2

(a) The phase shift in CD topology is $0,45$ as one inductor operates for only one half cycle , due to this the turns ratio are halved and the voltage stress on the secondary MOSFET's is the same as in CT topology

(b) The rms currents in the switches in CD topology is higher compared to FB and CT this is because of the higher ripple in the inductors ,so the switch conduction losses will be higher in this topology.

(c) The FB topology has the highest transformer secondary current compared to the CT and CD topology. However, the copper losses in the CT topology will be higher because the secondary of the transformer is center tapped and the number of secondary windings are doubled.

(d) The transformer secondary rms current in CD topology is least compared to FB and CT topologies. This is because only half of the output current flows through the secondary of the transformer. The inductor that is charging completes its path through the secondary of the transformer and the other inductor discharges through the switch so this current doesn't flow through the secondary winding of the transformer. This indicates smaller transformer.

(e) The transformer secondary currents in FB topology is 1.24 times the transformer secondary currents in CT topology.

(f) The transformer secondary currents in CT topology is almost $\sqrt{2}$ times the transformer secondary currents in the CD topology. This is observed at all loads and also at all the input voltages. Table 5.2 is just for comparison but tables of the currents discussed in Chapter 4 gives the clear idea.

(g) Since the inductors conduct only for the half cycle in CD topology and carry only half of the load current the size of the inductor is smaller.

(h) The inductors in CD topology charge only for half the cycle and discharge throughout so the inductor operating frequency is same as the primary switches. Whereas in FB and CT topology the inductor charges twice in one cycle so the operating frequency is twice that of the primary switching frequency.

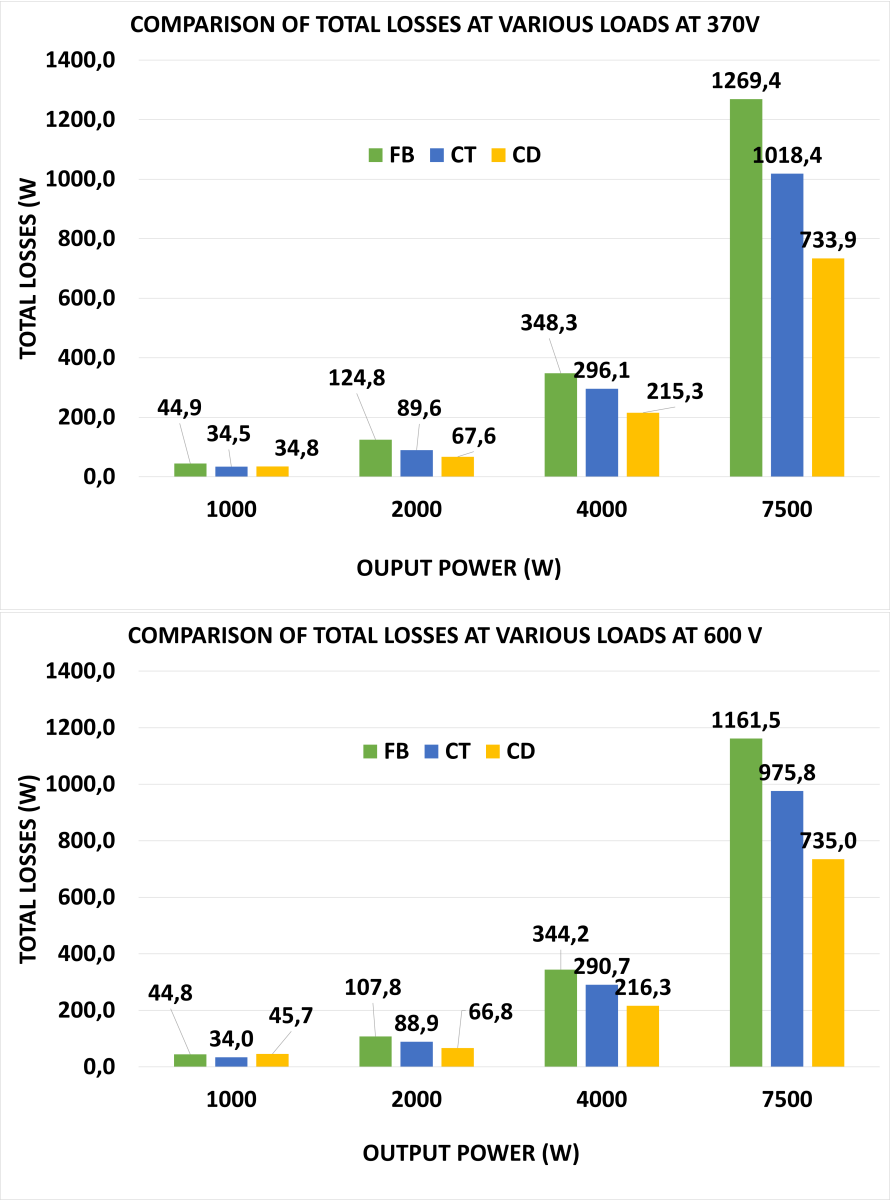


Figure 5.1: Comparison of all the three topologies at 370 V and 600 V input

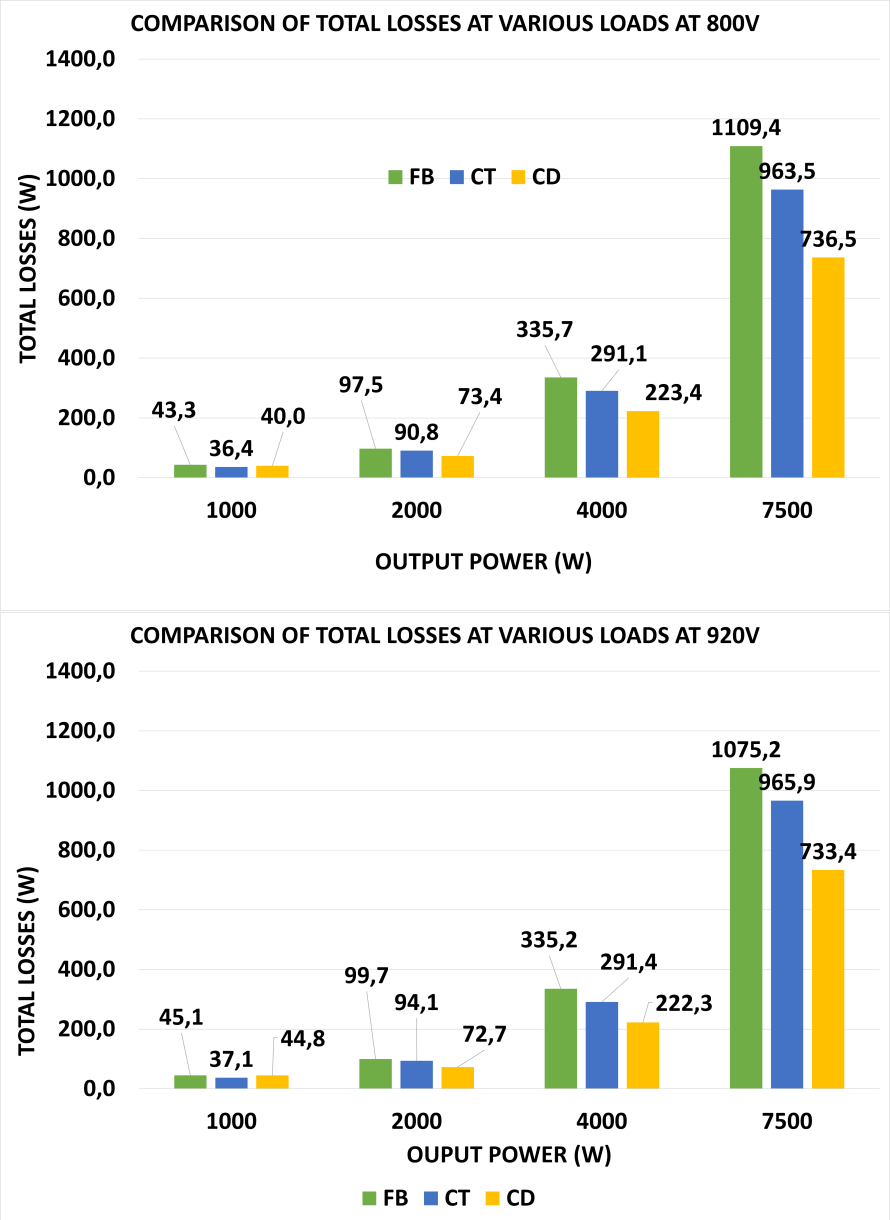


Figure 5.2: Comparison of all the three topologies at 800 V and 920 V input

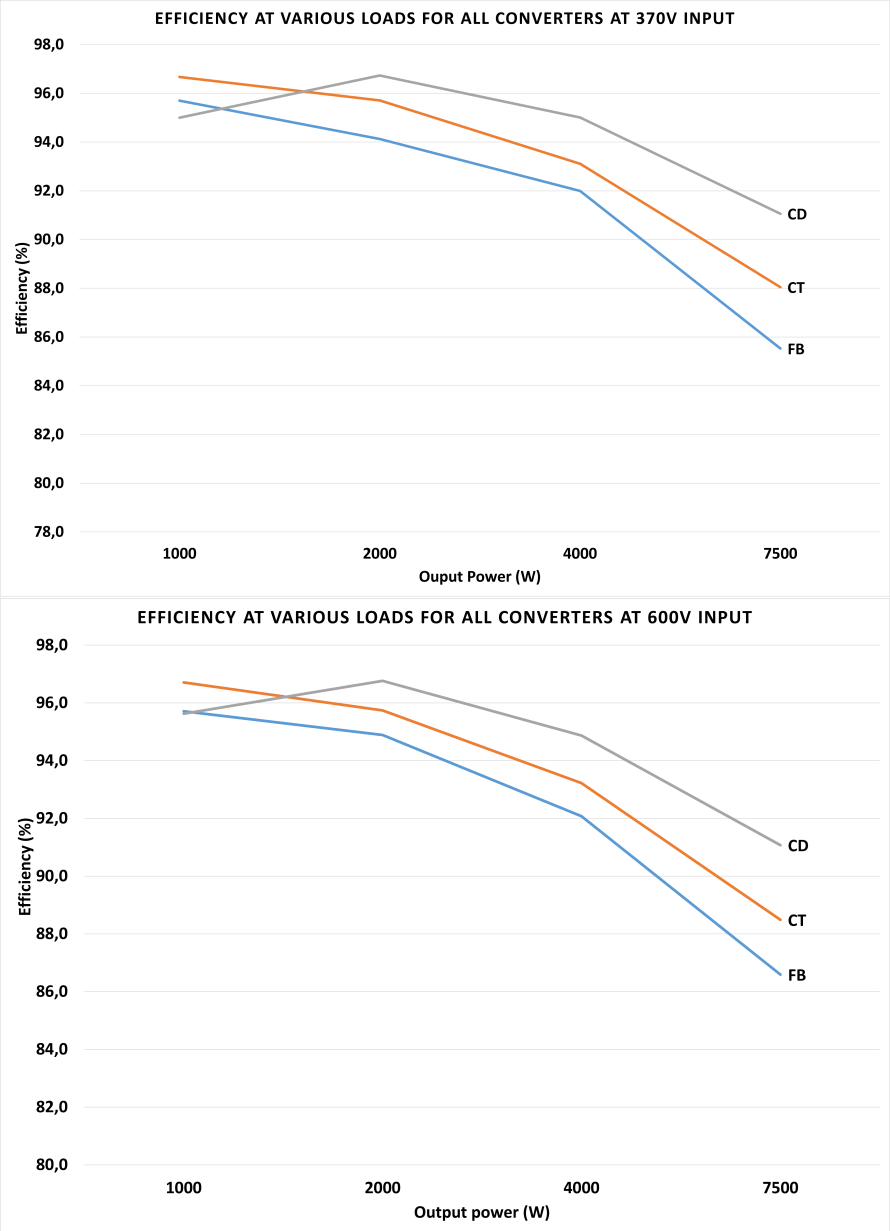


Figure 5.3: Comparison of efficiency of all the three topologies at 370 V and 600 V input

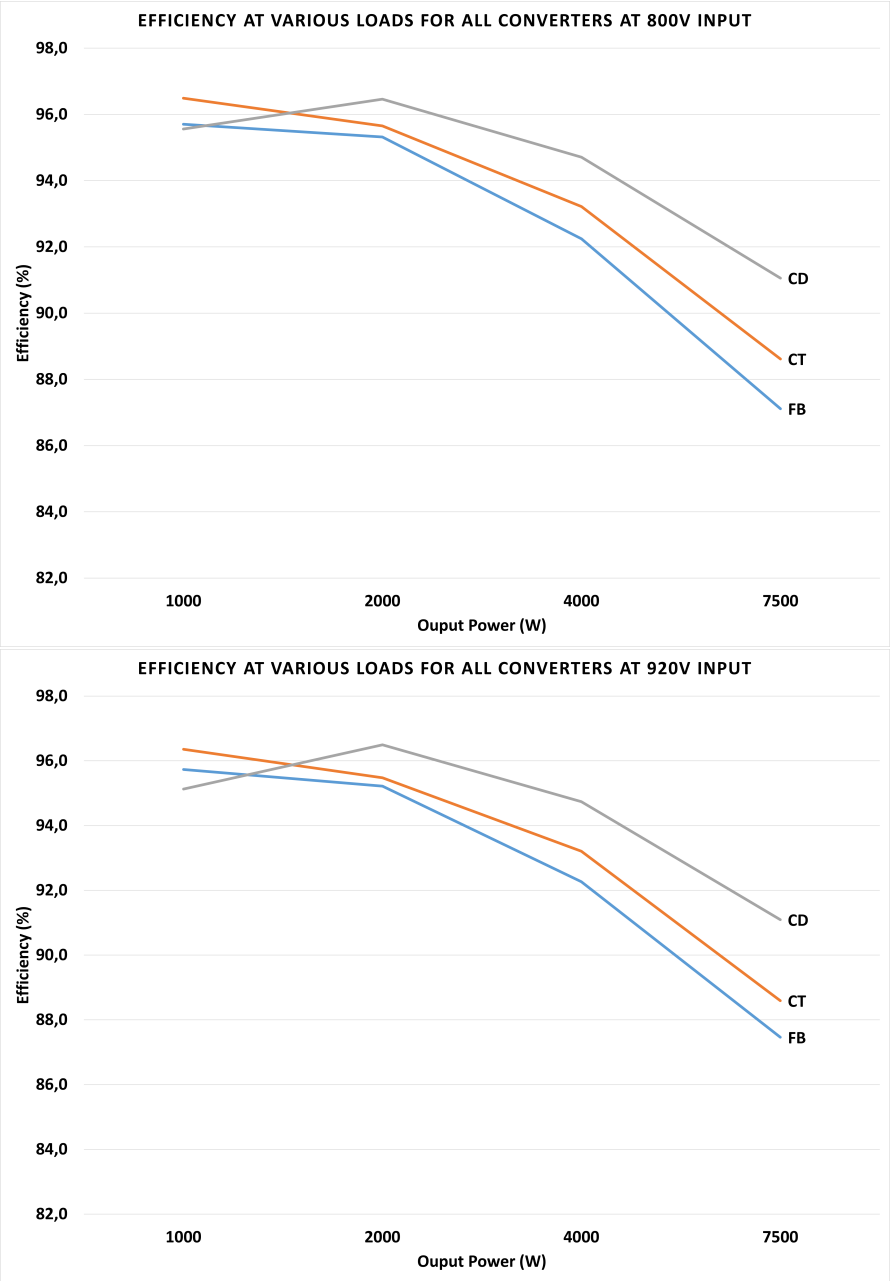


Figure 5.4: Comparison of efficiency of all the three topologies at 800 V and 920 V input

The following observations are made from the figures 5.1 and 5.2:

(a) The total losses in the PSFB-CD topology are comparably less than the FB and CT topology
(b) The losses in CD topology at 1000 W is slightly higher compared to CT topology that is because switch 1 and 4 lose ZVS at this load and there will be turn on and turn off losses this is also indicated in the table 4.15
(c) The losses in PSFB-FB are the highest and close to $1kW$ because of the following reasons:
    i. The higher rms current in the secondary of the transformer.
    ii. The number of secondary switches are 8 in the secondary which will increase the conduction losses and this is the dominant loss.

The following observations are made from the efficiency graphs 5.3 and 5.4:

(a) The efficiency of the PSFB-CD is comparably higher than the FB and CT topologies at all loads and at all input voltages
(b) At low load PSFB-CT is efficient and this topology is usually preferred in automotive as the cost is lesser
(c) At high load PSFB-CD is efficient

6

Conclusion and future work

6.1 Conclusion

In this work isolated DC/DC converter , phase shifted full bridge with three secondary topologies full bridge, center tap and current doubler were analyzed based on component losses and efficiency at various loads and various input voltages . It is very evident that the secondary switch conduction losses are the dominant losses in all the topologies with highest being in PSFB-FB topology as the number of switches in the secondary are doubled.

All the converters were simulated in MATLAB/Simulink and the waveforms were verified with the theory. It is found that the voltage stress on the secondary MOSFET's in CD topology though looks the same as in FB, it is equivalent to CT topology as the turns ratio is halved. The FB and CT topology transformer secondary winding have to be designed for full load current which will make the transformer lossy, but CD topology can be designed for half load current as one of the inductor charges in one half cycle and completes it's path through the transformer secondary but the other inductor is discharging through the switch. So it means that the size of the transformer is comparably smaller in CD topology. The transformer utilization is lesser in PSFB-CT topology as only one half winding is excited in half cycle but both the windings have to be designed to handle the full load current. Though the inductance is same in all the topologies the size of the inductor in CD topology could be smaller as it carries only half of the load current.

It is found that PSFB-CT is efficient at low loads and PSFB-CD is efficient at high loads. The conduction losses in the secondary switches are dominant in all the three topologies as the current stress is high.The MOSFET conduction losses are higher in CD topology as the current ripple in the inductor is higher in this topology.

The peak and rms currents are higher in the secondary of the transformer in all the topologies that might cause significant copper losses in the printed circuit boards (PCB). Hence, a need for interleaving/paralleling of power stages to improve the efficiency is to be considered. This work is a relative comparison, further investigation of topologies such as half bridge , LLC can be carried out.

6.2 Future work

(a) Analysis of more isolated topologies such as LLC and half bridge can be considered
(b) Interleaving/paralleling of the power stages to improve the efficiency can be considered
(c) The variation of junction temperature was considered from the datasheet which is $R_{\text{th,jc}}$ but total thermal impedance of the MOSFET's should be considered which needs thermal simulations
(d) For the magnetics, magnetic and thermal simulations should be carried out with the magnetic supplier
(e) LV voltage drops and voltage regulation needs to be accounted
(f) In this thesis, the design of the transformer with the estimation of the resistance of the primary winding for the converters is done. Layering of windings with the insulation and arrangement of the windings with probable solutions with the estimation of temperature rise of the transformer can be an interesting topic to research on.
(g) Prototyping the design to validate the results is a must , design optimization based on the results msut be carried out accordingly.

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