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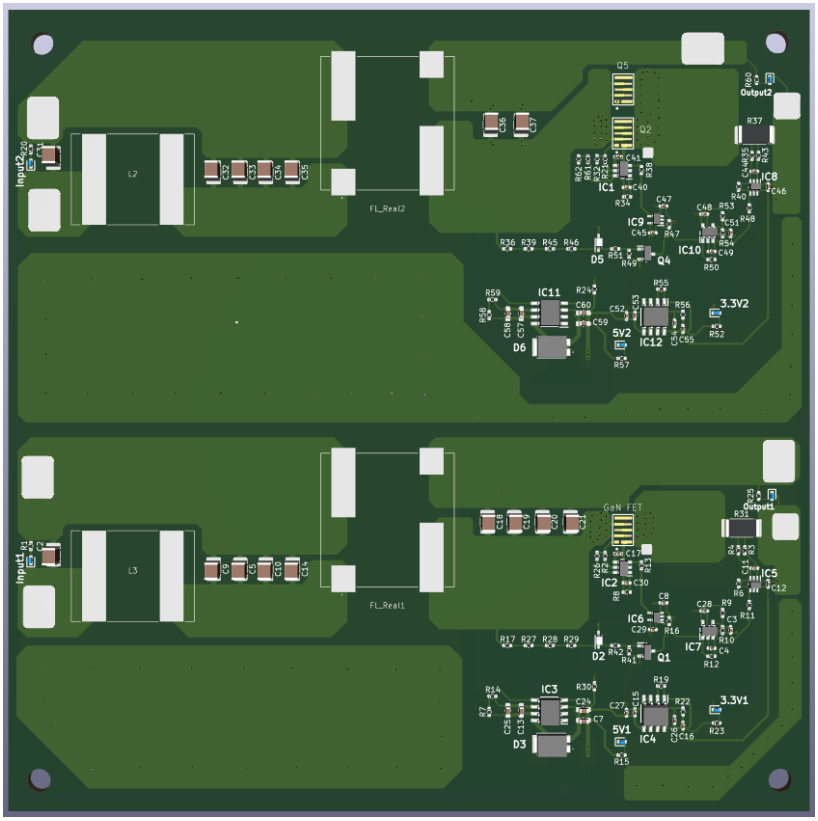

GaN FETs in Polarity Protection

Designing and testing reverse current protection solutions for -48V DC system using GaN FETs

Master's thesis in Sustainable Electric Power Engineering and Electromobility

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Cover: KiCad 3D model of the designed reverse polarity protection board, featuring two separate circuits for single and parallel-connected GaN FET configurations.

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Abstract

In -48 V DC telecommunication systems, wiring errors, hot-plug events, and load-side backfeed can create reverse current paths that may damage sensitive electronics. Conventional silicon MOSFET-based protection circuits are widely used to prevent such failures. However, they often require several parallel devices to reduce conduction loss and support higher load current, increasing the required PCB area. To reduce PCB area, Gallium Nitride (GaN) FETs offer a promising alternative due to their low on-state resistance, compact package size, and strong electrical performance. Therefore, this thesis investigates whether GaN FETs can provide reverse current protection in a -48 V DC system with comparable efficiency to silicon-based solutions, while enabling a more compact PCB implementation.

The thesis presents the design, simulation, PCB implementation, and experimental validation of single and parallel GaN-based protection circuits. The single-device circuit was validated up to 500 W as a proof of concept, which can be scaled to higher power levels using parallel transistors. The results show that the GaN-based protection circuit conducts during forward operation and blocks reverse current during fault conditions. Compared with the silicon-based reference, the GaN solution provides comparable efficiency and manageable thermal performance, while reducing component count and PCB area. Furthermore, the parallel configuration improves current capability and reduces thermal stress. However, due to GaN sensitivity to parasitic effects, careful gate-drive tuning and PCB layout are required. Overall, the results show that the GaN FET-based approach is a suitable solution for compact polarity protection in -48 V applications, particularly when PCB area reduction is a key design requirement.

Keywords: GaN FET, Polarity protection, -48 V DC system, Silicon MOSFET, Parallel devices, Power loss, Thermal performance, False triggering.

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Nattamon Suraamornkul & Natthawat Luangbanthao, Gothenburg, June 2026

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

DC	Direct Current
EMI	Electromagnetic Interference
EUT	Equipment Under Test
E-load	Electronic Load
FET	Field-Effect Transistor
GaN	Gallium Nitride
LDO	Low Dropout
MCU	Microcontroller Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOV	Metal Oxide Varistor
Op-amp	Operational Amplifier
PCB	Printed Circuit Board
PIG	Power Interrupt Generator
PSU	Power Supply Unit
RPP	Reverse Polarity Protection
SI	Silicon
SiC	Silicon Carbide
SOA	Safe Operating Area
SPICE	Simulation Program with Integrated Circuit Emphasis
WBG	Wide Bandgap

Nomenclature

Below is the nomenclature of parameters and variables that have been used throughout this thesis.

Parameters

V_{nom}	Nominal input voltage
V_{min}	Minimum operating voltage
V_{max}	Maximum operating voltage
P_{rated}	Rated output power
I_{rated}	Rated current
$R_{DS(on)}$	Drain-to-source on-resistance
R_{sense}	Current sensing resistor
R_G	Gate resistance
R_θ	Thermal resistance
R_{thJA}	Junction-to-ambient thermal resistance
R_{thJC}	Junction-to-case thermal resistance
T_{max}	Maximum allowable device temperature

Variables

V_{in}	Input voltage
V_{out}	Output voltage
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
I_{in}	Input current
I_{out}	Output current
P_{in}	Input power

P_{out}	Output power
P_{cond}	Conduction loss
η	Efficiency
T_{amb}	Ambient temperature

Contents

1
Introduction

Modern telecommunication systems are a central part of today's digital infrastructure and must continuously develop as the demand for data transmission and network usage increases. As users expect faster and more reliable communication services, the power electronics used in telecom equipment must also become more efficient, compact and reliable. This is especially important in the power input stage, where conduction losses and heat generation can directly affect system performance, power efficiency and long-term reliability.

A key part of the power input stage is the protection against incorrect current flow and fault conditions. In high-power telecommunication equipment, even small voltage drops can increase losses and create additional thermal stress. Improving the performance and size of protection circuits is therefore relevant not only for protecting the hardware, but also for reducing power losses and enabling more compact circuit board designs with higher power density.

1.1 Background

In –48V DC power systems, faults such as miswiring, hot-plug transients and load backfeed can cause reverse current and damage hardware. Conventional Silicon MOSFET protection circuits reduce this risk, but losses and thermal constraints can limit efficiency and power density. With advances in device technology, GaN FETs have been introduced and applied in many applications to enable improved performance. In this project, GaN FETs are implemented and investigated as a potential improvement over existing solutions with the intention of achieving higher efficiency and performance while enabling a more compact design.

1.2 Aim

The main purpose of this project is to design and experimentally validate a reverse current protection solution for -48V DC power systems using GaN FETs. This thesis aims to demonstrate that a GaN FET-based solution can reliably handle input power levels of up to 500 W while at the same time achieving higher efficiency and better overall performance compared with the state-of-the-art Silicon-based protection designs. In addition, the importance of size and cost reduction of the system will be addressed and taken into account in comparative studies.

1.2.1 Objectives

- To make a hardware prototype that can handle up to 500 W of input power.
- To investigate the challenges and requirements of using GaN FETs in polarity protection applications.
- Benchmark the GaN-based design against the state-of-the-art silicon-based protection solutions.
- Optimizing and adapting the design in terms of performance and size.
- To apply the knowledge in power electronics in a real challenge innovation.

1.3 Limitations

Due to the limited availability of GaN FETs suitable for polarity protection applications currently available on the market, the achieved performance may not represent the optimal potential of GaN technology. Therefore, the objective of this project is primarily focused on demonstrating the proof of concept of using a GaN FET as a replacement for six parallel silicon MOSFETs, while optimizing performance is considered a trivial concern at the pre-phase.

2
Theory

The following chapter introduces the fundamental theoretical principles governing GaN power semiconductors and their integration into reverse polarity protection solutions for high-power DC systems. Furthermore, it investigates the conduction and switching loss mechanisms, alongside a brief comparative analysis between GaN FET technology and traditional Si based semiconductors. This section also includes the gate drive requirements and control methods essential for this system.

2.1 Reverse Polarity Protection

Reverse polarity protection (RPP) is a critical protection mechanism intended to prevent damage to internal electronics under abnormal polarity and fault conditions in the power path. This is particularly important in -48V telecommunication power systems, where wiring faults, transient disturbances and load side fault events may impose reverse-voltage stress or unintended current paths across sensitive components. If not properly mitigated, such conditions can result in excessive power dissipation, thermal overstress and permanent failure of downstream circuitry. Several conventional models exist to mitigate the effects of reverse polarity, ranging from simple passive components to advanced active switching circuits. These topologies are evaluated based on their operational complexity and their effectiveness of minimizing parasitic conduction losses.

2.1.1 Passive Diode Blocking

The basic design of an RPP circuit includes a series connected diode which utilizes the unidirectional conduction property of the PN junction allowing current flow under normal operation. During fault events of reverse polarity, the diode becomes reverse biased, blocking current flow and protects the circuit from damage [1]. Although this method provides robust protection against reverse polarity by fully blocking reverse current paths, its primary drawback is the considerable forward voltage drop during standard operation. This drop results in a continuous power dissipation which can be expressed as,

$$P = V_F \cdot I \tag{2.1}$$

where V_F is the forward voltage drop and I is the current through the diode [2]. This degrades system efficiency and introduces thermal manage complications since higher current leads to increased power loss and consequently more heat generation.

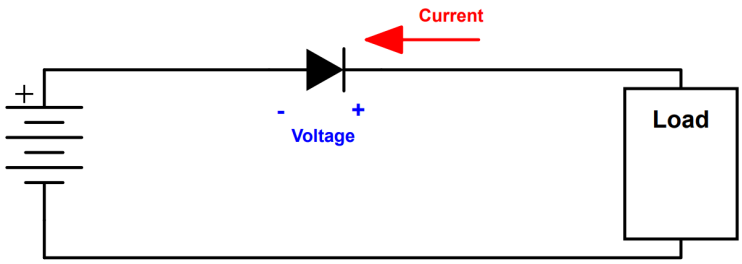

Figure 2.1: Series diode reverse polarity protection topology.

To reduce this limitation, Schottky diodes are a more convenient alternative and commonly used since they offer a lower voltage drop than the conventional PN diode. However, V_F is still present that causes power dissipation and must be considered in component sizing, while the Schottky diode is generally also more expensive [1].

2.1.2 Active Transistor Based Blocking

Active transistor-based blocking typically adopts MOSFETs in modern high-power designs to mitigate the main efficiency drawbacks of passive diodes. Unlike a diode-based RPP stage, where relatively fixed V_F is introduced, the MOSFET has a voltage drop set by the on state resistance $R_{DS(on)}$, which can be selected to be significantly smaller and therefore reduces conduction losses and heat generation [1], [3]. In these configurations, the device is arranged so that the intrinsic body diode is positioned in the direction of expected forward current [1]. This implies that, the body diode may conduct shortly during start-up until the gate-source voltage V_{GS} becomes large enough to turn on the MOSFET. Subsequently, the body diode shorts out and the main current paths shifts to the MOSFET channel, reducing the voltage drop that is determined by the on-state resistance $R_{DS(on)}$ [1],[3]. During a reverse polarity event, the MOSFET remains turned off due to the bias conditions so the reverse input voltage is blocked from reaching the protected downstream path [1].

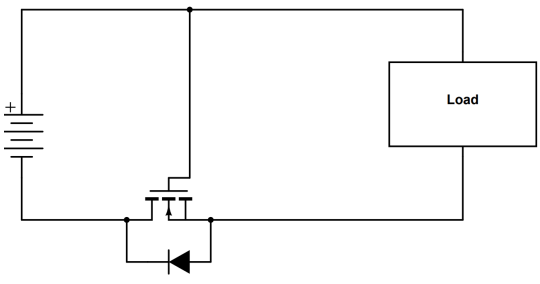

Figure 2.2: NMOS FET based RPP model.

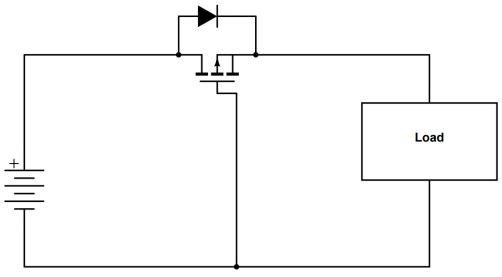

Figure 2.3: PMOS FET based RPP model.

2.2 Power Semiconductors Technologies

Power semiconductor devices define the technological foundation of modern power electronics and are used for switching and control of electrical energy [4]. Both their electrical and physical characteristics determine the achievable balance between conduction performance, blocking capability, switching dynamics and reliability [5], [6]. While Silicon (Si) remaining as the more dominant and mature baseline, advancement has directed towards wide-bandgap (WBG) semiconductors such as gallium nitride (GaN) and silicon carbide (SiC) [5]. This improvement is driven by material level advantages, providing potential for higher power density and efficiency [4], [5]. The comparative material properties of Si, SiC and GaN is shown in Figure 2.4.

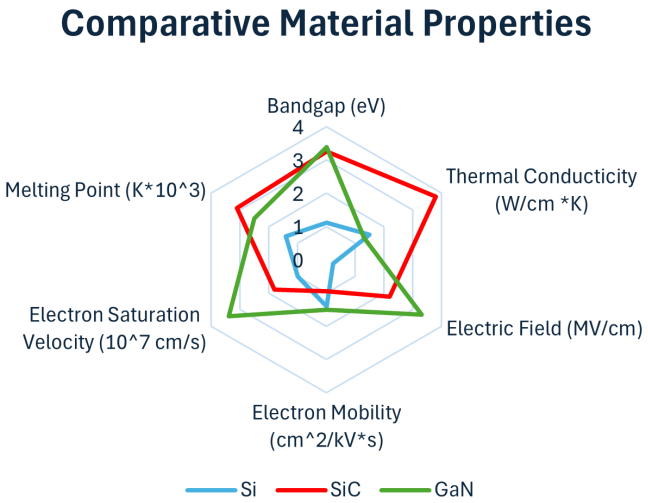

Figure 2.4: Comparative Material Properties of Si, SiC and GaN.

The dominant distinction between Si and WBG semiconductors are the wide bandgap and greater critical electric field that GaN and SiC comprises [5], [6]. The bandgap energy can be approximated as $E_g = 1.12$ eV for Si, 3.26 eV for SiC and 3.39 eV for GaN, while the critical electric field is estimated to be $E_{crit} = 0.23$ MV/cm for Si, 2.2 MV/cm for SiC and 3.3 MV/cm for GaN [6]. The higher critical electric field of WBG devices allows the same blocking voltage with a thinner drift region compared with conventional Si devices [5], [6]. This drift region scaling is directly linked to $R_{DS(on)}$, making WBG devices to achieve lower specific $R_{DS(on)}$ than silicon [6]. This results in lower I^2R loss, reduced heat generation, and improved efficiency [5], [6].

Important differences also emerge from thermal properties and carrier transport behavior [5], [6]. The electron mobility has been reported to be around 1400 $cm^2/V{\cdot}s$ for Si, 950 $cm^2/V{\cdot}s$ for SiC and 1500 $cm^2/V{\cdot}s$ for GaN ,while thermal conductivity values are roughly 1.5 W/cm·K for Si, 3.8 W/cm·K for SiC and 1.3 W/cm·K for GaN [6]. SiC and GaN are differentiated by their strengths. SiC has the strongest thermal conduction capability with high critical field, which is advantageous with respect to heat dissipation and voltage robustness. While, GaN combines a high critical electric field with high electron mobility, making it suitable for compact and

fast switching applications [5], [6]. However, practical GaN implementation remains challenging due to layout sensitivity, reliability constraints, ringings, and parasitic-related oscillations in the power stage [5], [6].

Improved power density is achievable from the combined effects of lower $R_{DS(on)}$, lower conduction loss, higher switching speed, higher voltage tolerance and improved thermal behavior [4], [5]. Lower semiconductor losses can reduce cooling demand, while a higher switching frequency enables smaller passive components. Overall, Si remains as the widely deployed and mature cost optimized benchmark, while GaN and SiC allows higher efficiency and power density by enabling faster switching, lower conduction losses and stronger voltage blocking capability [4], [5].

2.2.1 Parallel Devices and Current Sharing

In high-current applications, a single GaN FET may not always be sufficient to carry the required load current. One solution is to connect two or more GaN FETs in parallel. This increases the current capability of the protection stage and reduces the current stress in each individual device, and lowers the effective $R_{DS(on)}$. This reduces the voltage drop and conduction losses during normal operation. This is especially useful in low-voltage and high-current systems, where even a small resistance can create noticeable power loss and heating [7, 8].

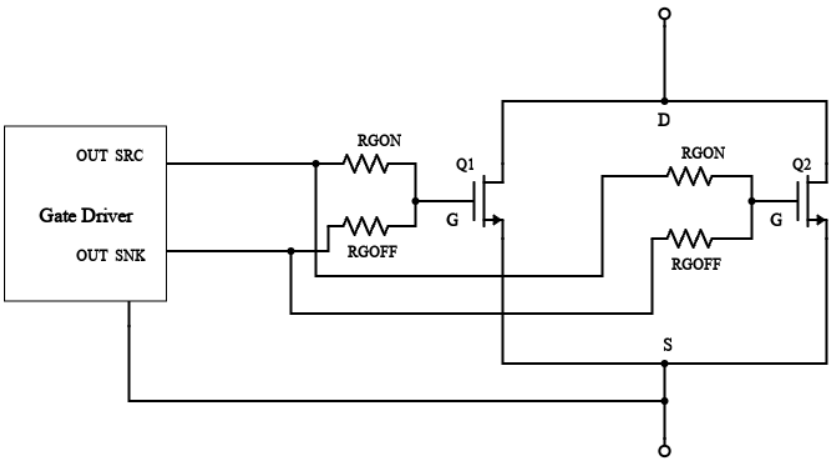

Figure 2.5: Parallel GaN FET gate-drive circuit with separate $R_{G,on}$ and $R_{G,off}$ paths.

Parallel connection can also improve the thermal distribution of the circuit. Instead of dissipating the total loss in one device, the loss can be distributed between several devices. If the current sharing is well balanced, this can reduce the thermal stress on each GaN FET and improve the reliability of the protection stage. In addition, paralleling devices can give more flexibility in the design. This can be useful when optimizing cost, availability, PCB layout and thermal performance [7, 9].

However, parallel operation also introduces the challenge of current sharing. Ideally, the total current should be divided equally between the devices. In practice, this

is difficult to achieve because the devices and PCB branches are not exactly identical. Differences in device parameters, gate-drive conditions and layout parasitics can cause one device to carry more current than the other. This can lead to higher losses, increased temperature and reduced reliability for the most stressed device [7, 9].

Current sharing can mainly be divided into static and dynamic current sharing. Static current sharing refers to the current distribution when the devices are fully turned on and operate in steady-state conduction. In this condition, the current distribution is mainly determined by $R_{DS(on)}$. A device with the lower $R_{DS(on)}$ will carry a larger share of the total load current. This means that even small differences in $R_{DS(on)}$ can create unequal current distribution during conduction.

However, $R_{\mathrm{DS(on)}}$ normally increases with temperature. This is known as a positive temperature coefficient. If one device initially carries more current, its temperature increases, which also increases its $R_{DS(on)}$. This limits further current increase through that device and supports a more stable current distribution in steady-state operation [7].

Dynamic current sharing is more difficult to control than static current sharing. During turn-on and turn-off, the current distribution is affected by parameters such as threshold voltage $V_{\mathrm{GS(th)}}$, transconductance, gate resistance and PCB parasitic inductances. If one device has a lower $V_{\mathrm{GS(th)}}$, it can start conducting before the other device and temporarily carry a larger part of the current, even if the static current sharing is acceptable [7, 8].

The PCB layout has a strong influence on the dynamic behaviour. Source inductance is especially important because it is included in both the power loop and the gate-drive loop. A mismatch in source inductance changes the effective gate-source voltage during switching, which can make one device turn on faster than the other. Drain inductance mainly affects voltage and current oscillations while gate inductance affects the gate-drive waveform and switching delay [7, 9].

Parasitic capacitances can also contribute to transient current imbalance during fast switching. When the drain-source voltage changes rapidly, the output capacitance of the devices and the equivalent PCB capacitance can generate additional transient current. This effect becomes more relevant when several GaN FETs are connected in parallel since the total capacitance in the circuit increases [10].

For reliable parallel operation, the GaN FETs should have similar electrical parameters, especially $R_{\mathrm{DS(on)}}$ and $V_{\mathrm{GS(th)}}$. The gate-drive paths should also be kept as equal as possible. In addition, the PCB layout should be symmetrical with short and equal current paths to improve current sharing and reduce the risk of one device becoming more thermally stressed than the other [7, 9, 10].

2.3 Loss Mechanisms and Efficiency

The total power loss in a FET device is composed of several factors given by

$$P_{tot} = P_{cond} + P_{sw} \tag{2.2}$$

where P_{cond} is the conduction losses in the FET and P_{sw} is the switching losses. The following subsection presents an analysis of the primary losses which constitutes to the total power loss in the device [11].

2.3.1 Conduction Losses

Conduction losses emerge when the semiconductor operates in the on-state and carries current. In this instance, the channel formed inside the device introduces $R_{DS(on)}$ between drain and source [11]. The conduction losses can be expressed as

$$P_{cond} = I^2_{DS,RMS} R_{DS(on)} \tag{2.3}$$

where I_{DS} is the drain to source current during conduction and $R_{DS(on)}$ is the internal resistance of the device. These losses persist throughout the entire on-state, introducing heat generation and reduces the efficiency [11].

2.3.2 Switching Losses

The primary switching-related energy dissipation arises during switching transitions between on and off state when V_{DS} and I_{DS} are present at the same time in an overlapping condition. Time period t_{on} is interpreted as the difference in time between t_1 and t_3 which is the rising current t_{ri} and falling voltage t_{fv}. In contrast, t_{off} defines the time period during turn-off switching transients between t_4 and t_6 from rising voltage t_{rv} duration to the time it takes for the current t_{fi} to fall [11]. This event constitutes to switching losses and the energy can be obtained by,

$$p(t) = v(t)i(t) = \frac{V_{DS} I_{DS}}{(t_x)} t, \;\; t_x = t_{on} \; or \; t_{off} \tag{2.4}$$

$$E_{on} = \int_{t_1}^{t_3} p(t)dt = \frac{1}{2} V_{DS} I_{DS} t_{on} \tag{2.5}$$

where E_{on} is the energy dissipation at turn-on and p(t) is the instantaneous power as the product of the maximum voltage and current between drain and source.

$$E_{off} = \int_{t_4}^{t_6} p(t)dt = \frac{1}{2} V_{DS} I_{DS} t_{off} \tag{2.6}$$

where E_{off} is the energy dissipation at turn-off and $p(t)$ is the instantaneous power as the product of the maximum voltage and drain-source current. The switching losses can be found to be

$$P_{sw(on)} = E_{on} f_{sw} \tag{2.7}$$

$$P_{sw(off)} = E_{off} f_{sw} \tag{2.8}$$

The total switching power loss in the device can be calculated from the sum of turn-on and turn-off power loss which is illustrated in Figure 2.6 and is presented by the following equation,

$$P_{sw} = P_{sw(on)} + P_{sw(off)} \tag{2.9}$$

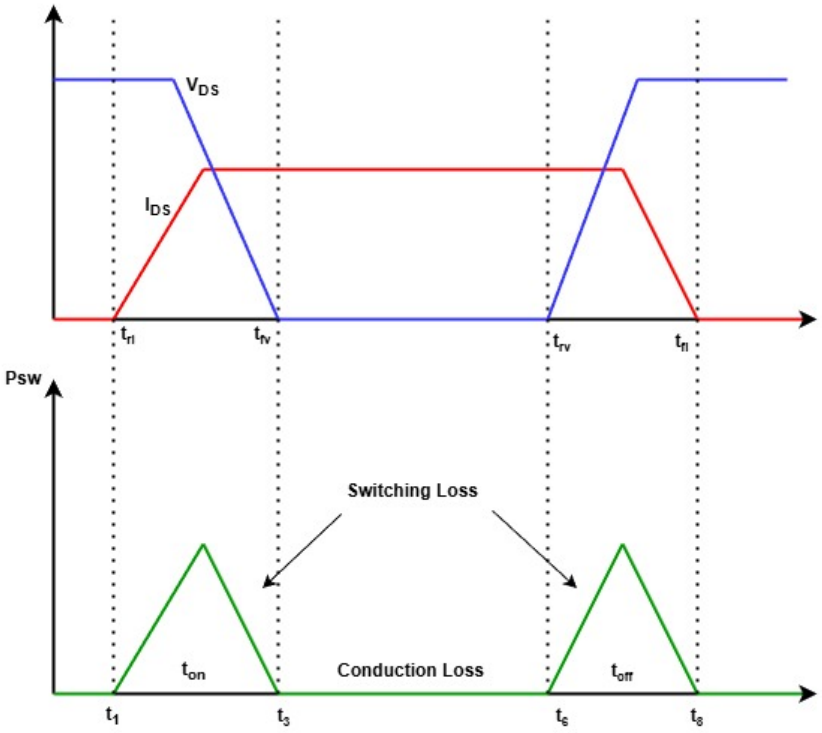

Figure 2.6: Turn-on and turn-off switching losses of FET

2.3.3 Protection Stage Efficiency

The efficiency of the protection stage is determined by the power loss introduced in the series current path between the input source and the load. In normal forward operation, the reverse polarity protection circuit should ideally behave as a closed switch with negligible voltage drop. This follows the general principle of switch-mode power electronics, where high efficiency is achieved by minimizing the dissipated power in the conducting device [12].

The protection stage efficiency can be expressed as

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} 100\% \tag{2.10}$$

where P_{out} is the power delivered to the load and P_{loss} is the total power dissipated in the protection path. P_{loss} is related to the previously introduced loss terms, where

the GaN FET is mainly divided into conduction loss P_{cond} and switching loss P_{sw}. The conduction loss is associated with the device on-state resistance $R_{DS(on)}$ while switching loss occurs during the transition intervals when voltage and current overlap [12].

In a reverse polarity stage, the power transistor typically operates as a static series switch during normal forward conduction rather than as a continuously switching device. When the device is fully enhanced, the load current flows through the low resistance drain-source path and the resulting loss is mainly determined by the on-state resistance and the load current. Therefore, the average efficiency of such a protection stage is primarily determined by steady-state conduction losses. Switching losses are mainly associated with short transient intervals such as turn-on, turn-off and fault interruption and therefore have a smaller influence on the steady-state efficiency.

2.4 Gate Driving and Dynamic Behavior of GaN FETs

This section presents the main design considerations for the gate-drive operation of GaN FETs, with focus on gate resistance selection, switching behavior, Miller-related disturbances and safe gate-voltage limits.

2.4.1 Gate Resistance and Switching Speed

The external gate resistance R_g is a critical tuning parameter in the gate-drive path, as it controls the transistor switching speed and overall transient behavior. A lower R_g increases the gate charging and discharging current, leading to faster switching. However, this reduces damping and thereby increases the risk of transient instability, such as voltage overshoot, undershoot and ringing caused by parasitic inductance and capacitance interaction. In contrast, a higher R_g improves damping and suppresses oscillations, but also increases the rise and fall times, possibly resulting in higher switching losses [13], [14]. Therefore, R_g selection involves a trade-off between transient stability and switching speed. In addition, using separate turn-on and turn-off R_g values enables independent control of each switching transition [14].

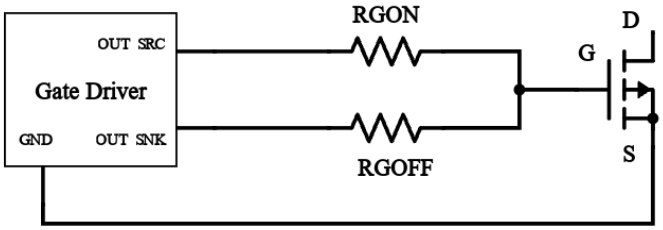

Figure 2.7: Gate-drive configuration with separate R_{Gon} and R_{Goff} gate resistors.

2.4.2 Miller Coupling and False Turn-On

During fast switching or transient operation, the gate voltage of a GaN FET can be affected even when the device is intended to remain turned off. This is mainly caused by the capacitance between the drain and gate, commonly referred to as the Miller capacitance C_{gd}. When the V_{ds} changes rapidly, part of this voltage transition is coupled to the gate through C_{gd}. This can create a temporary disturbance in the V_{GS}.

This effect is important for GaN devices because they operate with high switching speed and can therefore experience high dv/dt. In addition, GaN devices commonly have a relative low threshold voltage and a limited allowable gate-voltage range. If the induced V_{GS} becomes higher than the threshold voltage, the device may turn on unintentionally. This is known as false turn-on or crosstalk induced turn-on [15], [16].

The false turn-on mechanism is connected to both the device capacitances and the gate-drive path. The gate-drain capacitance C_{gd} couples the V_{ds} transition to the gate while the gate-source capacitance C_{gs} is charged by the coupled current. The impedance in the gate turn-of path determines how easily this current can be discharged. If the gate path has high impedance or large parasitic inductance, the gate voltage can rise more easily during a transient [15], [16]. Figure 2.8 shows how a fast change in the drain-source voltage generates a Miller current through C_{gd}, which can disturb the gate node and temporarily increase V_{gs}.

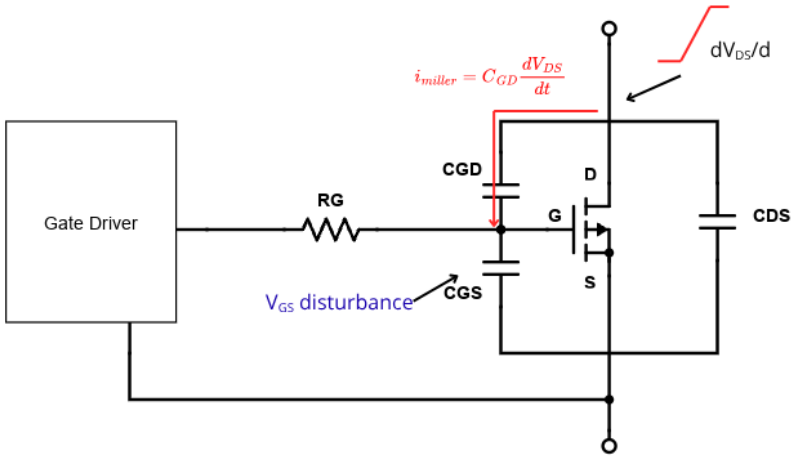

Figure 2.8: Simplified Miller coupling mechanism in a GaN FET during a fast drain-source voltage transient.

A simplified way to describe the origin of this disturbance is the capacitive discharging effect caused by $C\frac{dv}{dt}$. This means that a rapid voltage change across a capacitance produces a current. In the case of Miller coupling, the relevant capacitance is C_{gd} and the voltage change is the V_{ds} transition. This can be described as displacement current through C_{gd} which charges C_{gs} and creates a gate crosstalk voltage [15]. Therefore, the faster the V_{ds} changes, the more important the gate-

drive design becomes.

False turn-on can lead to unwanted current flow, additional losses, voltage oscillations and reduced reliability. In a reverse polarity protection, this is problematic because the protection device must remain in a defined off-state during abnormal input conditions. If a fast drain-source transient couples into the gate and raises V_{GS}, the GaN FET may partially conduct even though the protection logic requires it to remain off. This can reduce the blocking capability of the protection stage and allow unwanted current to flow during input disturbances or fault interruption.

The risk of false turn-on can be reduced by keeping the gate turn-off path low impedance and by minimizing the parasitic inductance in the gate loop. The gate resistance has a direct influence on the transient behavior of the GaN FET. By controlling the gate current, the resistor affects how fast the device turns on and off. A larger gate resistance gives a slower transition and can help reduce gate-voltage oscillations while a smaller gate resistance gives faster switching but can make the circuit more sensitive to ringing and parasitic effects [16]. Therefore, the gate resistance must be selected as a compromise between switching speed and gate stability.

Common methods to reduce Miller related turn-on include Miller clamping, separate turn-on and turn-off paths, negative turn-off voltage and careful PCB layout. The main purpose is to provide a low-impedance path for the coupled current and keep the gate voltage controlled during fast transients [16], [17]. Therefore, the gate driver should be placed close to the GaN FET and the gate loop should be kept short to reduce inductance and unwanted ringing.

2.4.3 Gate Voltage Limits and Safe Drive Requirements

The gate-source voltage, V_{GS}, is an important design parameter for GaN FET operation since it determines the transition between the off-state, partial enhancement and low-resistance on-state. Compared with conventional silicon MOSFETs, GaN devices typically have lower threshold voltage, lower gate charge and a narrower allowable gate-voltage range. These characteristics allow fast switching but they also make the gate-drive design more sensitive to voltage deviations and transient disturbances [6], [18].

The threshold voltage should not be considered as the required gate-drive voltage for normal operation. It only defines the voltage level where the device begins to conduct under specified datasheet conditions. For the GaN FET used in this project, the threshold voltage is approximately 2.2 V, while the typical recommended gate-source voltage is 5 V. Operating close to the threshold voltage would not fully enhance the channel and can increase the effective $R_{DS(on)}$, voltage drop, conduction loss and device temperature. If the gate-drive requirement is met, the device reaches a low $R_{DS(on)}$ which improves efficiency and reduces thermal stress in the protection path [6], [19].
The selected gate-drive level must also provide margin to the maximum allowed

gate-source voltage. For the GaN FET used in this project, the recommended maximum V_{GS} is 5.5 V, which gives a limited margin above the normal 5 V drive level. This is a key difference compared with many silicon MOSFETs which commonly tolerate considerably higher gate-source voltages. As a result, even if the nominal driver voltage is correctly selected, short gate-voltage overshoots caused by an underdamped gate-drive path may overstress or damage the device [18].

The lower gate-voltage limit must also be considered. During turn-off and transient operation, the V_{GS} can experience short negative voltage spikes due to parasitic effects in the gate loop. For the GaN FET used in this project, the recommended lower V_{GS} limit is -4 V. Safe gate driving therefore requires control of both positive overshoot and negative undershoot, not only the steady-state gate-drive level.

Undervoltage lockout is another relevant safe-drive function. If the driver supply voltage is too low, the GaN FET may not be fully enhanced, which can increase $R_{DS(on)}$, conduction loss and device heating. A gate driver with undervoltage lockout prevents switching until the supply voltage is above the required threshold, reducing the risk of weak turn-on and excessive dissipation during low-supply conditions [20].

2.5 Current Sensing and Protection Logic

A GaN-based reverse polarity protection stage requires a control structure that can determine whether the power device should be enabled or disabled. During normal operation, the GaN FET should be fully enhanced in order to reduce voltage drop and conduction losses. During reverse-current or fault conditions, the gate-drive signal must instead be forced active low, so that the device enters an off-state.

Protection circuits for power semiconductor devices often use a similar structure, where current information is first detected, compared with a defined limit and then processed by logic before the driver is disabled [21, 22]. In GaN-based systems, the speed of this chain is crucial because GaN devices can be exposed to high current slew rates and have limited tolerance to abnormal current conditions [21].

In the protection concept used, the current is first represented as a voltage across a sensing resistor. This voltage is then amplified and conditioned by an op-amp stage before the signal is evaluated by a comparator. The comparator output is processed by a logic stage, including an AND gate, to determine whether the gate driver should remain enabled or disabled. The control chain is shown in Figure 2.9.

Figure 2.9: Control chain of the GaN-based protection circuit from current sensing to gate-driver control.

2.5.1 Shunt-Based Current Measurement

A shunt resistor provides a direct method for converting current into a measurable voltage. The resistor is placed in series with the power path, which means that the current flowing through the circuit also flows through the sensing element. The resulting voltage follows Ohm's law

$$V_{\text{sense}} = IR_{\text{sense}} \tag{2.11}$$

where V_{sense} is the voltage across the shunt resistor, I is the current through the power path and R_{sense} is the resistance of the sensing element. This type of direct sensing is simple and suitable for protection circuits, but it also affects the current path because the resistor is physically inserted into it [23]. Current-sense and operational amplifier stages are then used to extract this small voltage signal and convert it into a useful signal for the following control circuit [24].

The sign of the sense voltage depends on the current direction. This is important in reverse polarity protection because the same sensing element can be used to distinguish between allowed forward current and unwanted reverse current. For a selected current threshold, the corresponding sense-voltage threshold is

$$V_{\text{sense,th}} = I_{\text{th}}R_{\text{sense}} \tag{2.12}$$

This means that the protection level is defined by the combination of the shunt resistance, amplifier gain and comparator reference voltage. The main limitation of shunt-based sensing is the additional loss introduced in the power path. Since the load current passes through the resistor, the dissipated power is

$$P_{\text{sense}} = I^2R_{\text{sense}} \tag{2.13}$$

The shunt value must therefore be selected as a compromise between signal quality and power loss. A higher resistance produces a larger voltage signal, which improves measurement margin and reduces the relative influence of amplifier offset. At the same time, it increases voltage drop, power dissipation and local heating. A lower resistance improves efficiency and thermal performance, but the measured voltage becomes smaller and more sensitive to offset, noise and PCB parasitic effects [24]. For high-current protection paths, this trade-off is important because even a small resistance can contribute to measurable power loss.

2.5.2 Op-Amp Signal Conditioning

The voltage across R_{sense} is normally small, especially when the shunt resistance is selected to minimize conduction loss. This signal is therefore not always suitable to feed directly into a comparator. The op-amp stage is used to scale the differential shunt voltage to a level that can be evaluated reliably by the threshold-detection circuit. In simplified form, the conditioned output voltage can be expressed as

$$V_{\text{amp}} = GV_{\text{sense}} \tag{2.14}$$

where G is the amplifier gain and V_{sense} is the voltage across the shunt resistor. The equation describes the ideal relationship between the differential shunt voltage and the amplifier output. Since the polarity of V_{sense} depends on the current direction, the resulting output signal can be used by the comparator to identify whether the current flow is normal or reversed.

Several amplifier parameters affect the accuracy and robustness of the protection threshold. The common-mode input range must be compatible with the voltage level at the sensing point. The input offset voltage is also important because the shunt voltage can be only a few millivolts. If the offset is too large compared with the measured signal, the effective current threshold may shift and cause incorrect turn-off or delayed protection. Gain accuracy and temperature drift also influence the threshold because they change the relationship between current and comparator input voltage [24].

The signal-conditioning stage may also include filtering to reduce high-frequency noise, ringing and short disturbances caused by switching events or parasitic elements. However, filtering adds delay to the protection path. This creates a trade-off between noise immunity and response speed. Protection circuits often include delay or blanking functions so that short transient spikes do not produce false triggering [22]. In reverse-current protection, the same principle applies. The circuit should react to a real reverse-current condition, not to a short measurement disturbance.

2.5.3 Comparator Threshold and Hysteresis

After amplification, the conditioned current signal is compared with a reference level. The comparator converts the analog current information into a digital signal that can be used by the protection logic. In principle, an activation signal is generated when

$$V_{\text{amp}} > V_{\text{th}}$$

where V_{amp} is the amplified current-sensing signal and V_{th} is the comparator threshold. In a reverse-current protection circuit, this threshold is selected so that the GaN FET remains enabled during normal forward conduction, while it is disabled when the sensed current corresponds to reverse current below the threshold level.

A comparator can become unstable if the input signal is noisy near the threshold. The output may toggle several times when the input signal crosses the reference level. These repeated transitions can create unnecessary gate-drive switching and uncertain fault detection. Hysteresis is therefore used to give the comparator different switching levels for entering and leaving the fault state [25].

By separating the detection and recovery thresholds, small disturbances around the comparator threshold are less likely to cause repeated output transitions. This improves the robustness of the protection decision, especially when the sensed current signal contains ringing, ground disturbance, load step transients or cable-induced oscillations. However, excessive hysteresis can make the circuit less sensitive to real

reverse-current events. Therefore, the comparator threshold and hysteresis must be selected together with the shunt resistance and amplifier gain.

2.5.4 Logic and Gate Driver Enable

The comparator output is used as a protection signal, but it is not connected directly to the GaN FET gate. Instead, the signal is first sent through a logic stage before it reaches the gate driver. This allows the circuit to combine the current-sensing result with other enable conditions. Similar protection circuits use current detection, threshold comparison, and control logic before the driver is disabled during a fault condition [22].

In this circuit, the logic stage includes an AND gate, which gives a high logic output only when both input signals are high. Therefore, the gate driver can only be enabled when the comparator output indicates a valid current condition and the second enable signal is also active. This second enable path includes a glitch-filtering function, which suppresses short-duration pulses caused by comparator noise, startup transients or current ringing. As a result, the AND gate does not enable the gate driver unless the signal remains stable for a sufficient time. If reverse current or another fault condition is detected, the comparator output changes state and the AND gate output then becomes low. This pulls the gate driver output low and forces the GaN FET into the off-state [22].

The response time of the protection path depends on the delay of each stage, mainly affected by the op-amp, comparator, glitch-filtering network, AND gate and gate driver. A short response time is important because the GaN FET should be turned off quickly when reverse current is detected. At the same time, the circuit should not react to very short noise spikes or temporary disturbances [21].

The gate driver is the final stage between the logic circuit and the GaN FET. Its task is to provide the required gate-source voltage during normal operation and to remove the gate charge when the protection logic disables the device. Since GaN FETs have a limited allowed gate-voltage range and can be sensitive to unwanted gate disturbances, the gate driver is important for controlled turn-on and turn-off behavior [21, 22].

2.6 Transient Behavior and Parasitic Effects

In an ideal DC circuit, the voltage and current would change without oscillations or temporary peaks. However, in practical power electronic circuits the physical layout affects the transient behavior. This is especially important in GaN-based circuits, since the fast switching capability makes the circuit more sensitive to parasitic inductance and capacitance. These parasitic elements can lead to voltage overshoot, ringing and increased electrical stress during fast current transitions [26], [27].

2.6.1 Cable and PCB Parasitic Inductance

In a practical power circuit, the current path always contains parasitic inductance. This is also commonly referred to stray inductance. During steady-state DC operation, the influence of this inductance is limited since the current is almost constant. However, when the current changes rapidly during switching, load transients or fault interruption, the inductance can generate a voltage spike.

The voltage across an inductive path is described by

$$V_L = L\frac{di}{dt} \tag{2.15}$$

where L is the inductance and di/dt is the rate of current change. This relation shows that even a small inductance can create a high transient voltage if the current changes quickly [27], [12]. Therefore, a DC circuit can still experience short voltage peaks during dynamic operation even if the nominal supply voltage is constant.

The energy stored in an inductance is expressed as

$$E_L = \frac{1}{2}LI^2 \tag{2.16}$$

where I is the current through the inductance. When the current path is interrupted, this stored energy has to be transferred or dissipated somewhere in the circuit. As a result, higher current levels and larger loop inductance increase the transient stress on the switching or protected device.

In GaN circuits, both the power loop and the gate loop are important parts of the layout. Parasitic inductance in the power loop can contribute to drain-source ringing while parasitic inductance in the gate loop can disturb the gate-source voltage during switching and cause overvoltage and false turn-on [26]. Since GaN devices operate with higher current slew rates, the layout must be designed to reduce loop inductance as much as possible [27].

2.6.2 Voltage Overshoot and Ringing

Voltage overshoot occurs when the current through an inductive path changes rapidly. During turn-off or current interruption, the inductance opposes the change in current and generates an additional voltage across the device. The magnitude of the overshoot is therefore related to the stray inductance and the current slew rate [26], [27].

This voltage contribution from the stray inductance can be expressed as

$$V_L = L_{stray}\frac{di}{dt} \tag{2.17}$$

where L_{stray} is the inductance in the switching path and $\frac{di}{dt}$ is the current slew rate. This shows that the voltage overshoot increases when either the parasitic inductance or the current transition speed increases. Therefore, minimizing the loop

inductance is important to reduce voltage stress during fast switching and fault interruption events.

After the initial overshoot, ringing can occur. This happens when inductance interacts with capacitance in the circuit. In GaN circuits, the transistor output capacitance C_{oss} is one of the main capacitances involved in the ringing. The power-loop inductance and C_{oss} can form an oscillating circuit during the switching transient [26], [27].

The natural frequency of this oscillation can be approximated as

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.18}$$

where L is the effective loop inductance and C is the effective capacitance. A lower loop inductance therefore changes the ringing behavior and reduces the voltage stress caused by the oscillation.

The oscillation decreases depending on the damping in the circuit. A higher resistance can reduce the ringing faster but resistance in the main current path also increases conduction losses. Therefore, the preferred solution is normally to reduce the parasitic inductance through the layout rather than unnecessary resistance [27]. This is why compact current loops, short connections and properly placed decoupling capacitors are important in GaN power stage design.

2.6.3 Capacitor Charging and Discharging During Transients

Capacitance also has a strong influence on transient behavior. In GaN circuits, the transistor output capacitance C_{oss} is especially important since it can interact with the loop inductance and contribute to drain-source voltage ringing during switching transients [26], [27]. Other capacitances such as decoupling and input/output capacitors can also influence the measured waveform by charging or discharging during fast voltage changes.

The current through a capacitor is given by

$$i_C = C\frac{dV}{dt} \tag{2.19}$$

where C is the capacitance and dV/dt is the rate of voltage change. This relation shows that a rapid voltage change can create a temporary current through the capacitance [12], [27].

The energy stored in a capacitor is

$$E_C = \frac{1}{2}CV^2 \tag{2.20}$$

Where V is the voltage across the capacitor. During a transient event, this energy can be exchanged with the energy stored in the circuit inductance. This energy

exchange is one reason why ringing can appear in the voltage waveform.

For this reason, a short voltage movement or current pulse in a measured waveform does not always mean that there is continuous conduction through the main switching device. It can also be caused by charging and discharging of circuit capacitances. Therefore, both inductive and capacitive effects need to be considered when analyzing transient voltage and current waveforms in GaN-based circuits.

2.7 Thermal Behavior

Thermal behavior is important in power semiconductor applications because electrical losses are converted into heat during operation. Excessive semiconductor temperature can affect electrical characteristics, accelerate ageing mechanisms and reduce reliability [28]. The thermal performance of a power device is therefore determined by both the generated power loss and the ability of the package and PCB to transfer heat away from the semiconductor junction [28].

2.7.1 Thermal resistance and junction temperature

The temperature rise of a power semiconductor can be approximated using thermal resistance. In simplified form, the temperature increase is expressed as

$$\Delta T = P_{loss} R_\theta \tag{2.21}$$

where P_{loss} is the dissipated power and R_θ is the thermal resistance of the heat transfer path. The junction temperature can be estimated as

$$T_j = T_a + P_{loss} R_{\theta JA} \tag{2.22}$$

where T_j is the junction temperature, T_a is the ambient temperature and $R_{\theta JA}$ is the junction to ambient thermal resistance [28].

For surface-mounted power devices, the PCB is a major part of the thermal path. Heat is transferred through the package, solder joints, copper areas, vias, PCB layers and surrounding air. Therefore, $R_{\theta JA}$ should not be treated as a fixed device only value since it depends on the PCB and the thermal test conditions [28].

As described in Section 2.3, the main steady state losses in the protection path are the conduction loss of the FET and the loss in the current sense resistor. Since both losses are proportional to I^2, higher load current produces significantly higher thermal stress. In addition, $R_{DS(on)}$ is temperature dependent. For fully enhanced, $R_{DS(on)}$ generally increases as junction temperature rises which can further increase conduction loss [29].

Infrared thermography and thermocouples are methods for temperature measurement. Infrared thermography is useful for identifying hot spots and comparing surface temperatures but the result depends on the surface radiation properties of

the measured material and selected measurement point. The measured temperature is not identical to the internal junction temperature but it can still provide useful information about thermal behavior and heat distribution [28].

2.7.2 Localized Heating in Single and Parallel Device Implementations

The thermal behavior of a power stage depends not only on total power loss but also on how current and heat are distributed between devices. In a single-device implementation, the full current flows through one semiconductor package. This can reduce component count and occupied area but it also concentrates heat generation into one local region.

In parallel implementations, the current can be shared between several devices. For n identical devices in parallel, the equivalent on-state resistance can be approximated as

$$R_{eq} = \frac{R_{DS(on)}}{n} \tag{2.23}$$

If the current is shared equally, the current through each device becomes

$$I_{device} = \frac{I_{total}}{n} \tag{2.24}$$

and the loss in each device is

$$P_{device} = \left(\frac{I_{total}}{n}\right)^2 R_{DS(on)} \tag{2.25}$$

This explains why paralleling devices can reduce thermal stress on each individual component. Using multiple FETs in parallel lowers the effective resistance of the conduction path and distributes the generated heat across more than one package. With balanced current sharing, this reduces the thermal load on each individual device and improves the margin to the allowable junction temperature [30].

3
Case Setup

3.1 Simulation Setup

To validate the theoretical operation of the GaN-based reverse polarity protection model, a virtual testbench was developed using LTspice. The LTspice schematic is designed using manufacturer provided SPICE models as illustrated in Figure 3.1, to apply the real characteristics, data and behavior of the components.

In this model, the control circuitry includes an Op-amp, a comparator and an AND logic-gate. Since a SPICE model for the specific GaN transistor intended for the hardware prototype was not available, a complementary GaN device with similar specifications was integrated as a functional equivalent. The transistor is paired with a compatible gate driver model that provides the necessary voltage levels and sourcing capabilites required for GaN technology.

This comprehensive modeling approach allows for the precise fine-tuning of passive component values including the RC filters for signal decoupling and the resistor networks defining the circuit hysteresis. Optimizing these parameters ensures stable gate drive operation, preventing unintended oscillations and false triggering of the GaN FET during operation.

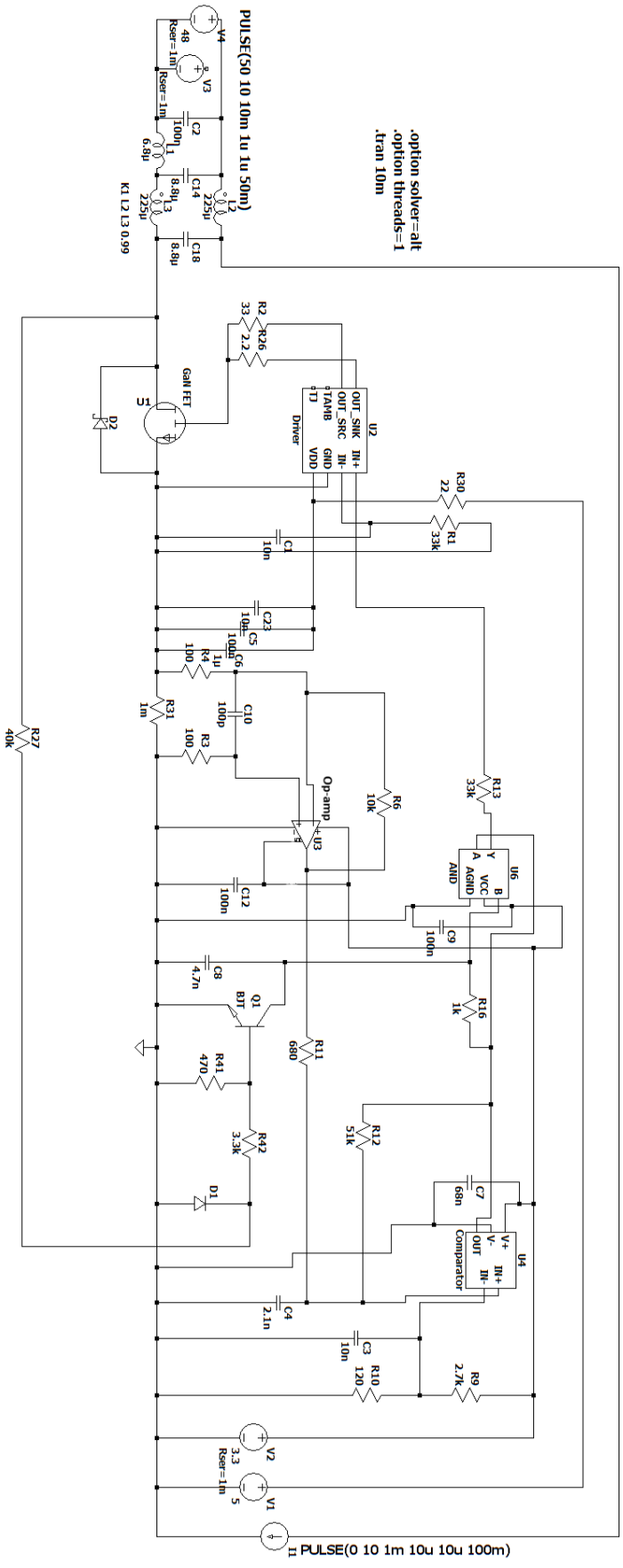

Figure 3.1: LTspice circuit schematic for the GaN FET based polarity protection.

3.2 Hardware Design and Implementation

A hardware prototype of the polarity protection circuit using a GaN FET and two parallel GaN FETs will be implemented on a PCB to evaluate the proof of concept of using GaN FETs instead of six parallel MOSFETs in a -48 V DC polarity protection application. The main objective of the hardware implementation is to demonstrate that GaN FETs can reliably operate as the primary protection device in a primarily static polarity protection application and provide comparable or improved performance relative to a conventional silicon MOSFET-based solution.

3.2.1 Electrical Requirements

In telecommunication systems, -48 V DC systems are commonly used. Therefore, a polarity protection circuit is designed to operate in a typical -48 V DC system. For experimental proof of concept, a 500 W output is targeted for the single device configuration. Accordingly, the key electrical specifications of the prototype are defined as follows:

- Nominal input voltage: -48 V
- Rated output power: 500 W
- Nominal output current:

$$I_{nom} = \frac{P_{rated}}{V_{nom}} = \frac{500}{48} = 10.42A \tag{3.1}$$

The polarity protection circuit must be capable of conducting the rated current continuously without excessive voltage drop or thermal overstress. In addition, it must block reverse current under fault conditions to protect upstream equipment. The selected GaN FET must also withstand the maximum operating voltage with sufficient safety margin to ensure reliable operation. The main specifications of the selected GaN FET are summarized in Table 3.1.

Table 3.1: Main specifications of the selected GaN FET

Parameter	Symbol	Value
Maximum drain-source voltage	V_{DS}	200 V
Pulsed drain-source voltage	$V_{DS,pulse}$	240 V
Continuous drain current	I_D	75 A
Drain-source on-state resistance	$R_{DS(on)}$	3.9 mΩ typ., 5.0 mΩ max.
Recommended gate-source voltage	V_{GS}	5.0 V typ., 5.5 V max.
Gate threshold voltage	$V_{GS(th)}$	2.2 V typ.
Gate charge	Q_G	17 nC typ.
Output charge	Q_{oss}	115 nC typ.
Reverse continuous current	I_S	21 A
Source-drain reverse voltage	V_{SD}	1.9 V typ. at 17 A
Reverse recovery charge	Q_{rr}	0 nC
Thermal resistance, junction-to-case top	R_{thJC}	0.5 °C/W typ., 0.6 °C/W max.
Operating temperature	T_j	-40 °C to 150 °C

Since the application is primarily static, the GaN FET operates in the enhanced state during normal operation for the most of the time. As a result, conduction loss becomes the dominant component of power dissipation, while switching losses are negligible. Therefore, minimizing $R_{DS(on)}$ is critical to improving overall efficiency and thermal performance.

3.2.2 Environmental Requirements

A 2-layer PCB is used for the prototype due to its cost efficiency and ease of measurement during experimental validation. The size of the PCB is 150 × 150 mm, with two circuits on the same board. The upper circuit on the PCB consists of a polarity protection circuit with two parallel GaN FETs, while the lower circuit uses a single GaN FET. Components are placed on both top and bottom sides of the PCB to minimize loop inductance.

In addition, it is important to ensure that heat is well distributed and that the PCB maintains a safe operating temperature during continuous operation. As the GaN implementation replaces multiple parallel silicon MOSFETs with a single or two devices, effective heat spreading through copper planes and proper component placement are crucial to prevent thermal concentration. However, using only two layers introduces limitations in heat dissipation and cooling. Therefore, this prototype may have poor thermal dissipation and may not be suitable for prolonged operation.

3.2.3 Block Diagram

An overall system block diagram is shown in Figure 3.2.

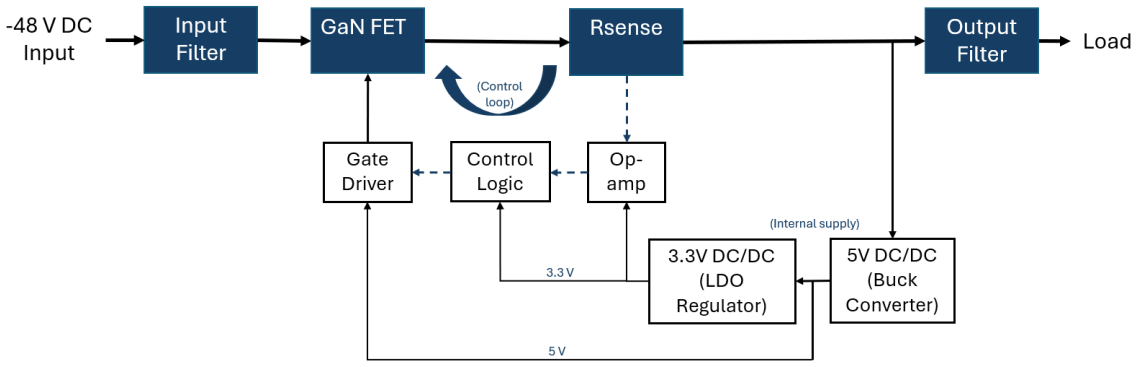

Figure 3.2: Overall Block Diagram.

The circuit receives a -48 V DC input and includes input filtering to reduce conducted disturbances. The input filter consists of capacitors, an inductor, and a common-mode choke to stabilize the input voltage and suppress noise. In addition, surge protection devices, metal oxide varistors (MOVs), are used at the input stage to protect the circuit from transient voltage surges. In the main power path, the voltage drop across a current sensing resistor, R_{sense}, is amplified by an operational

amplifier and forwarded to the control logic.

An auxiliary power supply is derived from the -48 V input using a step-down DC–DC converter to generate 5 V. This 5 V rail supplies the gate driver and an LDO regulator, which generates 3.3 V to power the control circuit. The control logic, including a comparator and an AND gate, evaluates the detected signal from the operational amplifier and polarity conditions, and generates the control signal for the gate driver.

The gate driver is supplied by 5 V from the step-down DC–DC converter and is controlled by the logic circuitry to drive the GaN FETs. During normal forward conduction, the GaN FETs are fully enhanced. During reverse polarity events, the control logic disables the gate driver, turning the GaN FETs off and thereby blocking reverse current flow to protect the upstream system.

3.2.4 Schematic Design

The schematic of the input filtering stage is shown in Figure 3.3. This stage consists of copper pads for connection to the input wires, input capacitors, a series inductor, and a common-mode choke to suppress conducted noise from the input supply. In addition, MOVs are incorporated to protect the circuit against transient voltage surges.

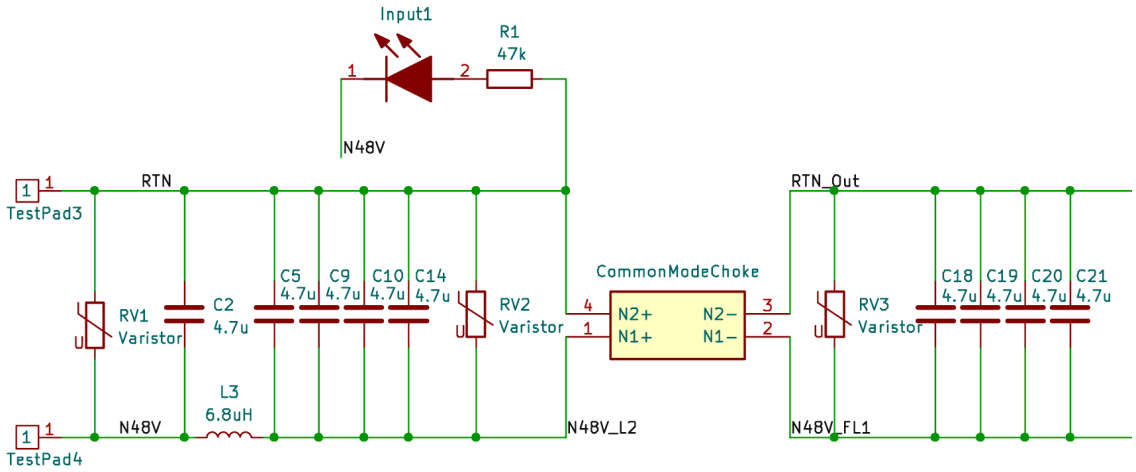

Figure 3.3: Schematic of the input filtering stage.

After the input filtering stage, the voltage is supplied to the auxiliary power supply stage. This stage includes a buck converter circuit that steps down the input voltage from 48 V to 5 V. The 5 V output is used to power the gate driver according to the required operating voltage specified in the GaN datasheet as shown in Table 3.1. Subsequently, a LDO regulator generates a 3.3 V supply for the control circuit. The schematic of the auxiliary power supply stage is shown in Figure 3.4.

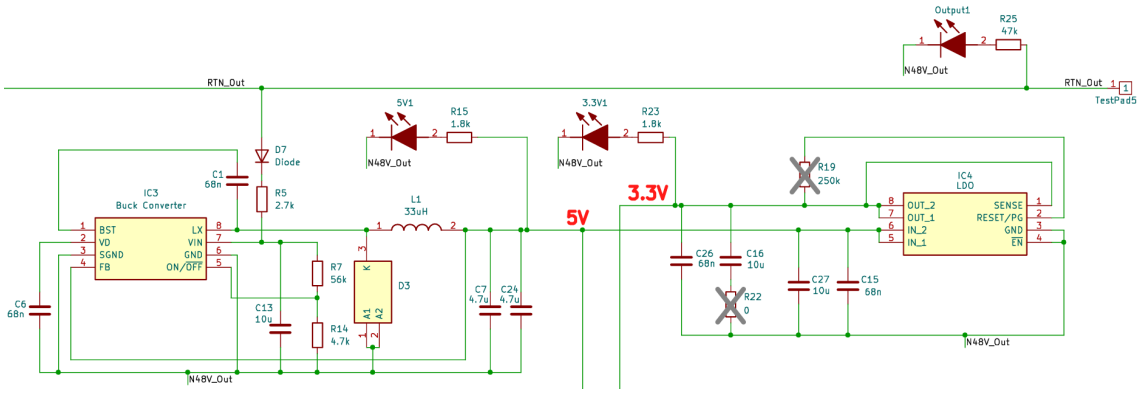

Figure 3.4: Schematic of the auxiliary power supply stage.

The voltage drop across R_{sense} is sensed and amplified by the operational amplifier before being forwarded to the control logic circuit. The control logic, consisting of a comparator and an AND gate, evaluates the sensed current condition and generates the control signal for the gate driver. In addition, the BJT is incorporated as an overvoltage protection. The schematic of the control stage is shown in Figure 3.5.

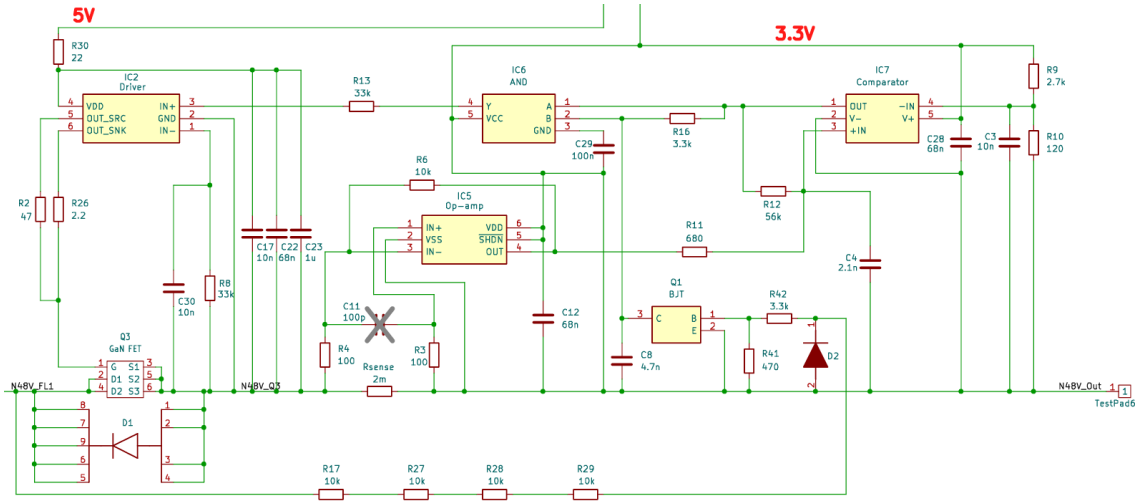

Figure 3.5: Schematic of the control stage.

3.2.5 PCB Layout

The PCB layout is designed with a focus on minimizing parasitic inductance, reducing EMI, and improving thermal performance. The components are carefully placed on the PCB according to the following layout considerations:

- Short and wide traces in the main current path to reduce conduction losses
- Minimized loop area in the gate drive path to prevent oscillation
- Placement of the gate driver close to the GaN FET to reduce parasitic inductance
- Sufficient copper area around the GaN device to enhance heat spreading

As GaN FETs exhibit high switching speed and sensitivity to parasitic inductance, careful PCB layout is crucial to prevent voltage overshoot, ringing, and potential

instability. In particular, the high dV/dt capability of GaN FETs makes the design sensitive to layout-induced parasitic elements. Although the polarity protection application is relatively static and does not involve continuous high-frequency switching, unlike power converters, transient events during turn-on and reverse blocking still require a well-optimized layout to ensure stable operation. The final PCB layout of the prototype is shown in Figure 3.6.

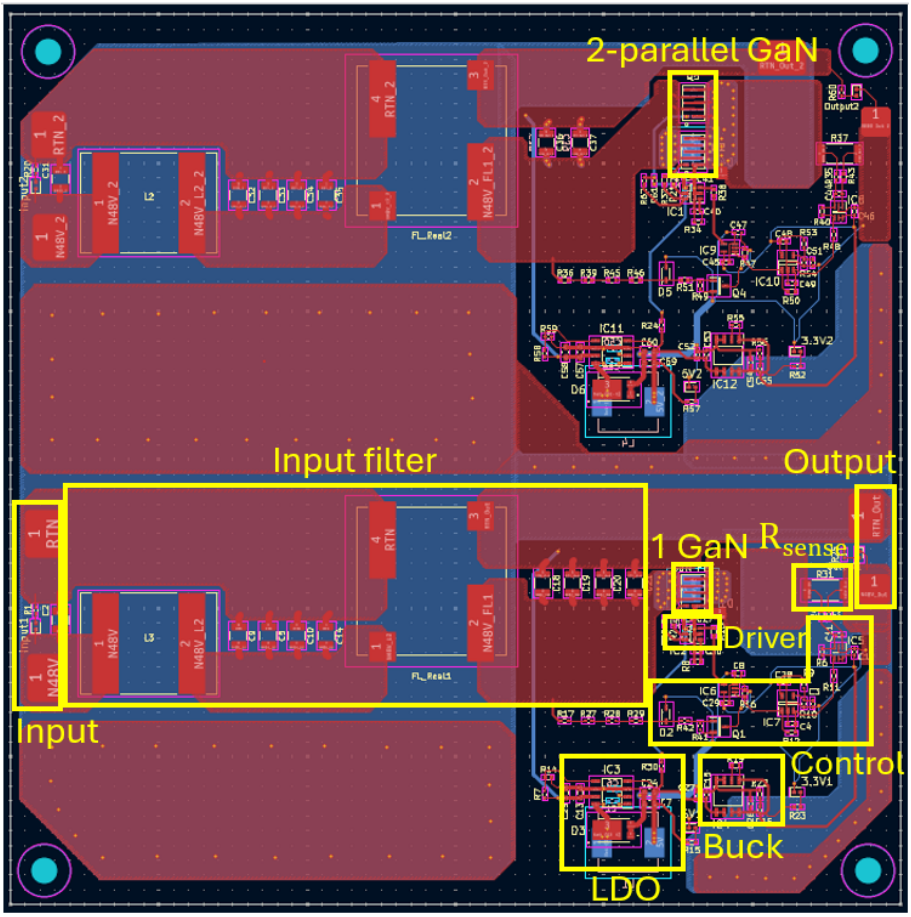

Figure 3.6: PCB Layout.

The top and bottom layer of the PCB are shown in Figure 3.7 and 3.8, respectively. Most components are placed on the top layer for easy measurement and surface thermal inspection. The main power path is also routed on this layer. The bottom layer is mostly used for additional routing traces and placing components that cannot be accommodated on the top layer. As a two-layer PCB is used, some components are placed on the bottom layer to minimize loop area and keep current paths as short as possible.

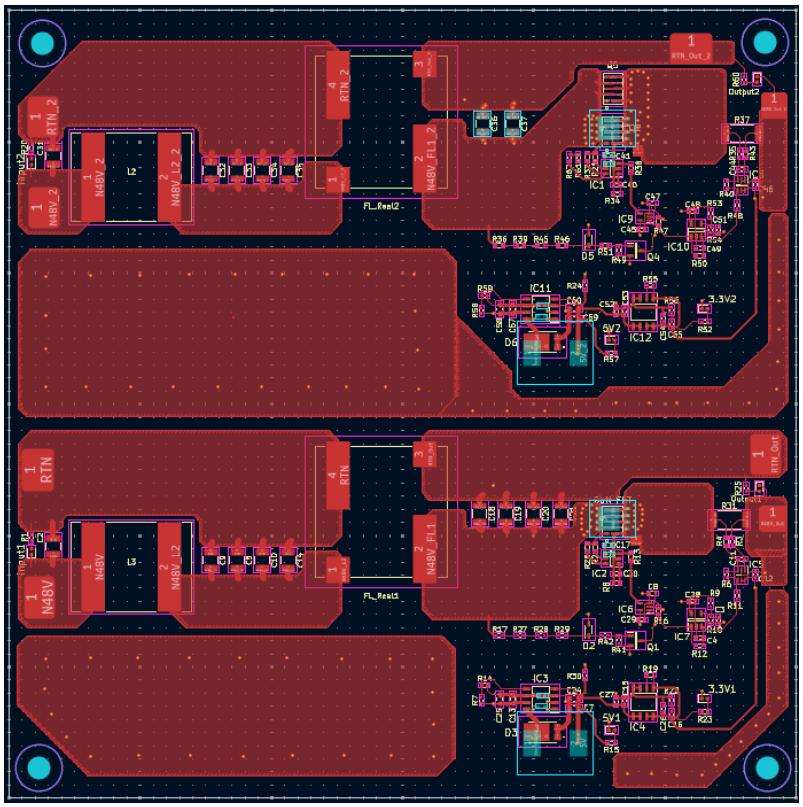

Figure 3.7: Top Layer of PCB Layout.

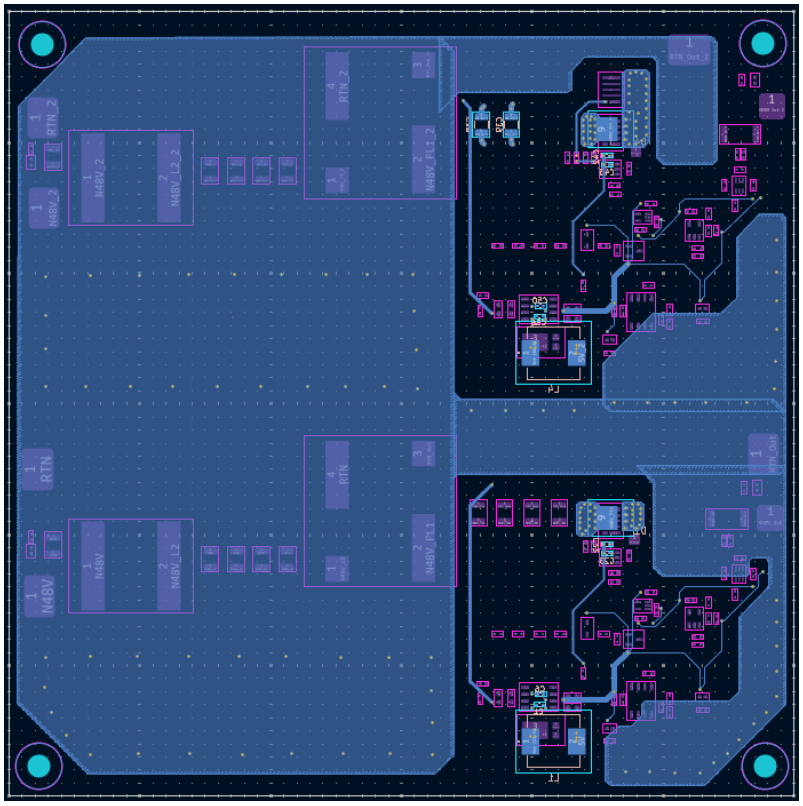

Figure 3.8: Bottom Layer of PCB Layout.

The placement of the single and two parallel GaN FETs with their driver circuits is shown in Figure 3.9 and Figure 3.10, respectively. The components are placed according to the driver datasheet recommendations and as close as possible to each other to minimize loop inductance and reduce EMI. Several vias are implemented between the top-layer GaN FET copper plane and the bottom-layer Schottky diode copper plane to enhance thermal dissipation and improve heat spreading.

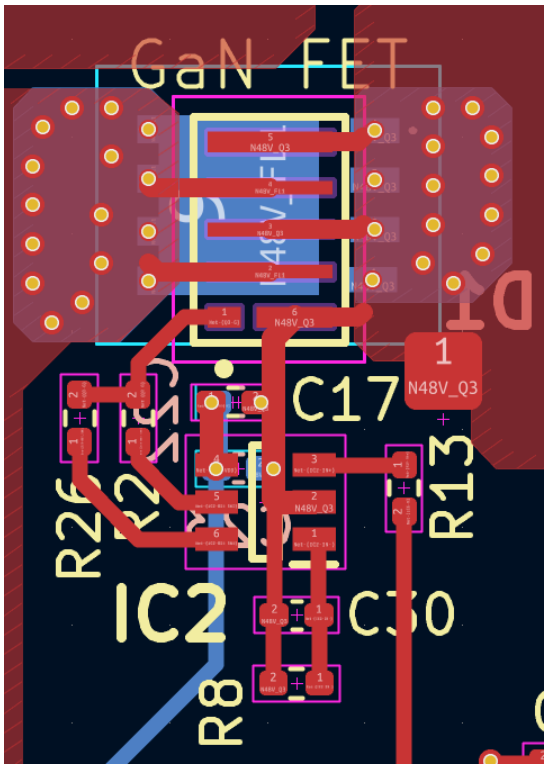

Figure 3.9: GaN Placement.

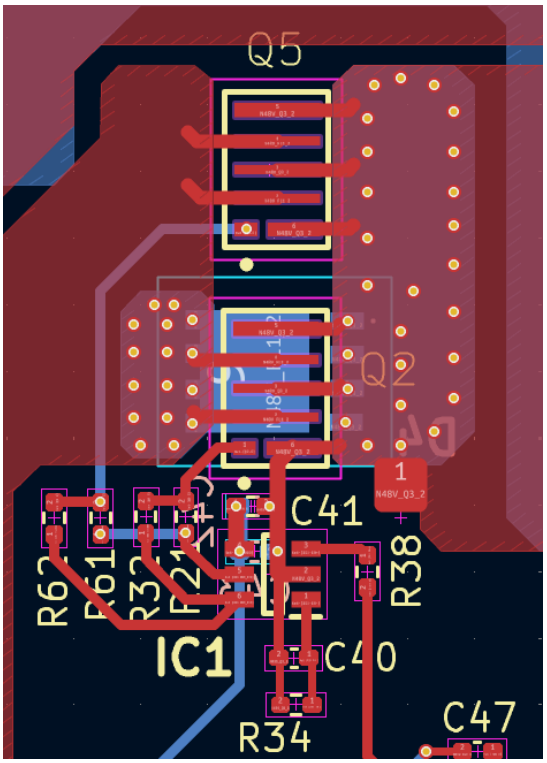

Figure 3.10: Parallel GaN Placement.

The assembled PCB prototypes after hand soldering and modification for the single GaN FET and two-parallel GaN FET configurations are shown in Figures 3.11 and 3.12, respectively. These prototype PCBs are used for hardware testing to verify the proof of concept of using GaN FETs in the polarity protection circuit.

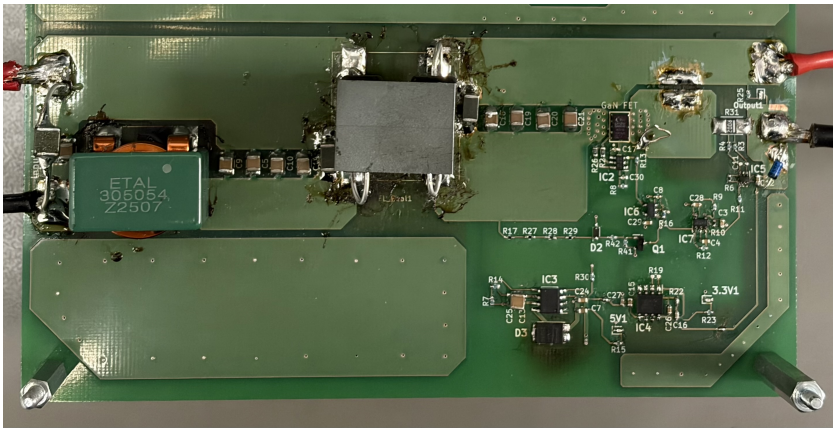

Figure 3.11: Assembled PCB prototype configured with a single GaN FET.

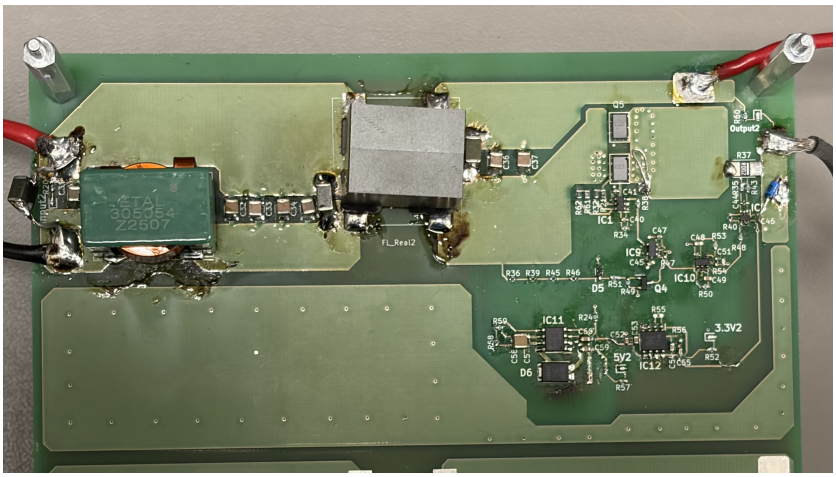

Figure 3.12: Assembled PCB prototype configured with two parallel GaN FETs.

3.3 Experimental Setup and Test Procedure

The main purpose of the experimental work is to provide proof of concept and functional validation of GaN FETs used in a reverse polarity protection circuit for a -48 V DC power system. The testing is designed to verify correct operation under normal and fault conditions and to evaluate the electrical and thermal performance. All hardware testing will be conducted in a laboratory.

3.3.1 Equipment

The experimental setup consists of the following laboratory instruments:

- DC power supply
- Electronic load: 0-750 V, 0-20 A, 0-1200 W
- Oscilloscope: 350 MHz
- Multimeter
- DC current probe: 50 MHz, Max peak 50 A, Max Perm. DC 30 A
- Differential voltage probe: 500 MHz, 10 pF
- High voltage differential probe: 120 MHz
- Thermal imaging camera
- Power interrupt generator
- Y-cable
- Long cable (100 μH equivalent inductance) used to emulate line inductance
- Additional filter circuit (π-filter + hold up capacitor) used to emulate the real application connected to the output of the polarity protection circuit.

3.3.1.1 Differential Voltage Probe

To investigate the influence of the probe on the measured waveforms, a comparison between a normal differential voltage probe and a high-impedance active probe was performed. The measured V_{DS} waveforms using the normal differential probe and the high-impedance active probe are shown in Figure 3.13 and 3.14, respectively.

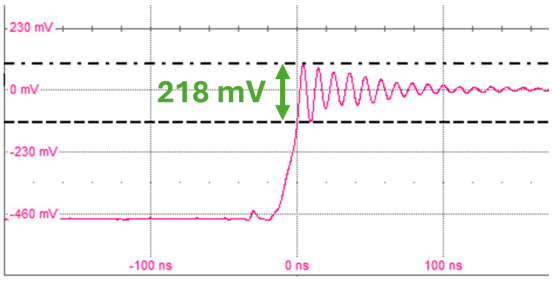

Figure 3.13: V_{DS} measured using a normal differential voltage probe

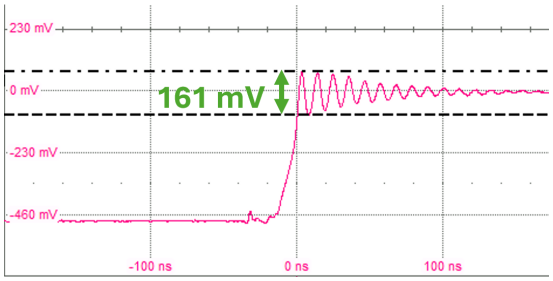

Figure 3.14: V_{DS} measured using a high-impedance active probe.

It can be seen that the normal probe produces a ringing amplitude of around 218 mV as shown in Figure 3.13, while the high-impedance active probe reduces the measured ringing amplitude to approximately 161 mV as shown in Figure 3.14, around 26% reduction. This difference is caused by the lower input capacitance and higher input impedance of the active probe, which minimize loading effects on the measured circuit. As a consequence, the high-impedance active probe can capture fast switching transients with higher accuracy and less waveform distortion.

However, in this report, the normal differential voltage probe was primarily used due to equipment availability. In addition, the normal probe was considered sufficient for proof-of-concept validation, where extremely high measurement accuracy was not required. Consequently, some of the ringing observed in the measured waveforms during the analysis may originate not only from the circuit or the GaN FET itself, but also from the influence of the measurement probe.

3.3.1.2 Long Cable at Input

A long cable with an equivalent inductance of approximately 100 μH is used to emulate line inductance. In practical installations, the distance between the PSU and the load can be large, leading to high parasitic inductance. Therefore, the long cable is introduced at the input in some tests to evaluate whether the polarity protection circuit operates correctly in the presence of input inductance. The experimental setup with the long cable at the input is shown in Figure 3.15.

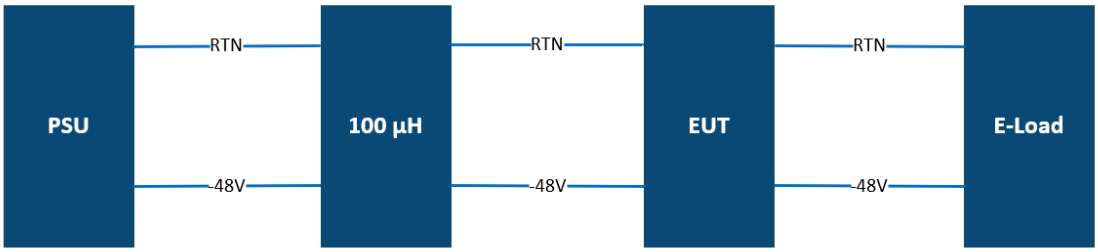

Figure 3.15: Experimental setup with the long cable at input.

3.3.1.3 Additional Filter Circuit at Output

An additional filter circuit, implemented as a π-filter and hold up capacitors, as shown in Figure 3.16, is connected at the output in some tests to emulate the downstream circuitry present in real applications.

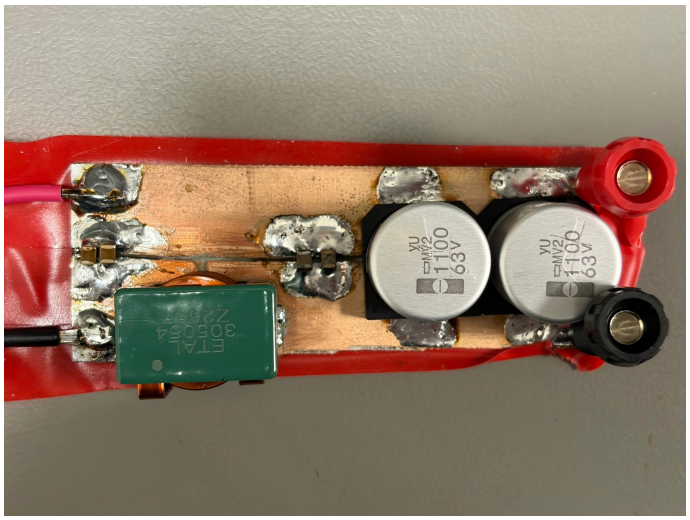

Figure 3.16: Additional filter circuit (π-filter + hold up capacitors).

In practical systems, the polarity protection stage is typically followed by other power conditioning or filtering stages. Therefore, incorporating this this filter at the output allows evaluation of whether the protection circuit maintains stable operation in the presence of output-side impedance and capacitance. The experimental setup with an additional filter circuit at the output is shown in Figure 3.17.

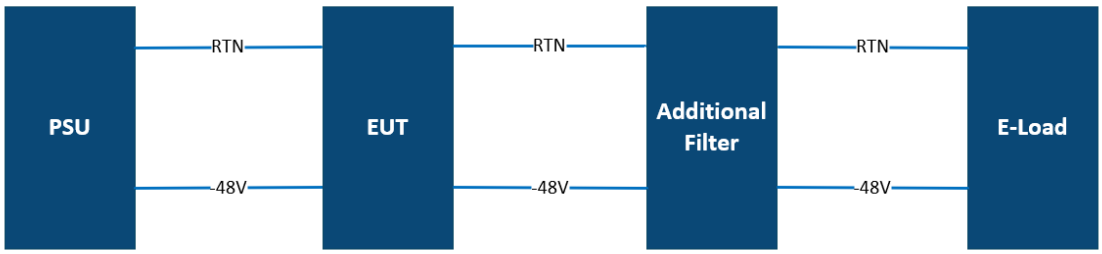

Figure 3.17: Experimental setup for an additional filter circuit at the output.

3.3.2 Functional Verification Test

This test is conducted to validate the protection functionality of the proposed GaN-based circuit.

3.3.2.1 Functional Verification Under Forward Operation

This test is carried out to verify the basic functionality of the GaN-based polarity protection prototype under normal forward operating conditions. The objective is to

confirm that the implemented gate-drive circuitry turns on the GaN device correctly and establishes the intended low-resistance conduction path.

3.3.2.2 Thermal Distribution

Thermal performance is evaluated during both continuous and step load operation. Measurements are taken after 5 minutes of operation at 10 A of both circuits. A thermal imaging camera is used to capture the surface temperature distribution of the PCB and the GaN FETs. The maximum device temperature and hotspot locations are identified to evaluate heat dissipation and the PCB heat-spreading capability. Since conduction losses are converted directly into heat, thermal measurements provide an indirect validation of the calculated electrical losses.

3.3.2.3 Power Losses

As a primary static application, the dominant loss mechanism is the conduction loss associated with the drain-to-source on-resistance of the GaN FET. The power loss corresponds to the electrical power dissipated across the protection stage during steady-state operation. Switching losses occur only during the turn-off transient of the GaN FET. However, they are included in the overall loss calculation for completeness.

3.3.2.4 Efficiency

The efficiency of GaN FET is evaluated at 10 A and 19 A load. The efficiency is determined as

$$\eta_{GaN} = \frac{P_{load}}{P_{load} + P_{loss}} \cdot 100\% \tag{3.2}$$

Since the PCB prototype is used only for experimental validation and includes additional parasitic losses from traces, connectors, and sensing elements, the efficiency analysis is limited to the GaN FET itself. Therefore, the GaN FET efficiency is calculated based on the measured drain-source voltage and load current, excluding losses from the remaining PCB components.

3.3.3 Step Load Test

The step load test is conducted to evaluate the dynamic stability of the protection circuit under transient load conditions. Although the polarity protection function is primarily static, rapid variations in load current commonly occur in telecommunication applications and may introduce transient disturbances. The objective of this test is to verify that the circuit maintains stable forward conduction during load transitions without falsely triggering the reverse protection mechanism. Controlled current steps are applied using the electronic load in constant current mode while maintaining the input voltage at -48 V. The load current is stepped between 0 A and 10 A to generate abrupt transitions.

The transient response is evaluated in terms of voltage overshoot and undershoot, oscillations, current slew rate, and settling time. Overshoot and undershoot are defined as the maximum deviations from the steady-state voltage immediately after a load transition, while oscillations are analyzed to evaluate the effects of PCB parasitics. The current slew rate is determined from the slope of the measured current waveform, and the settling time is defined as the time required for the output voltage to return to and remain within a specified tolerance band around its steady-state value. The experimental setup for the step load test is shown in Figure 3.18.

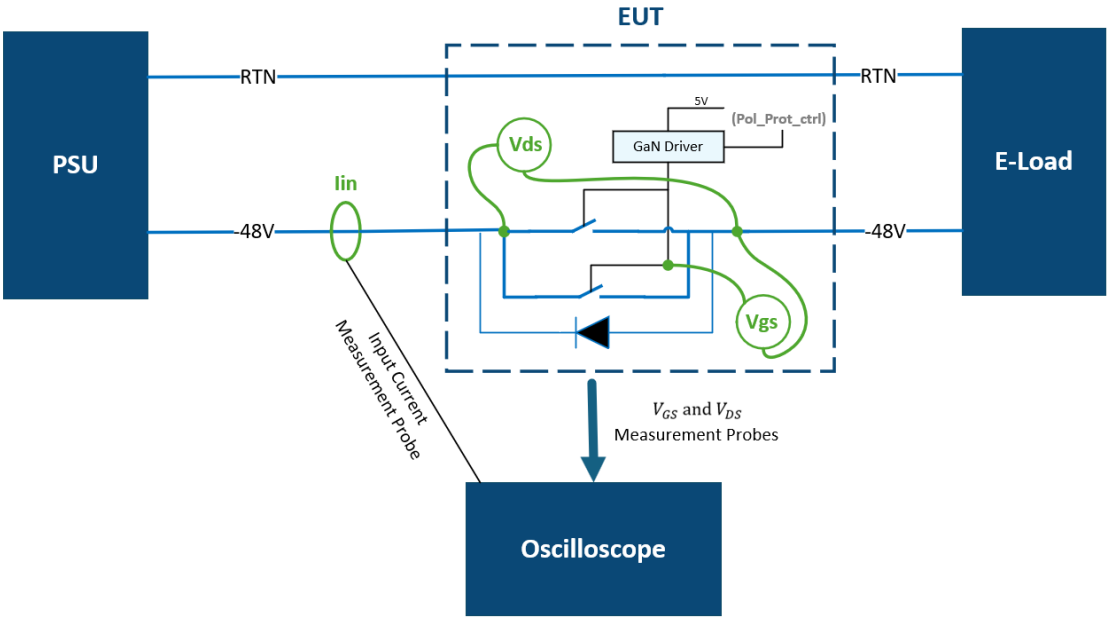

Figure 3.18: Experimental setup for step load test.

3.3.4 Real Application Emulation Test

The objective of this test is to emulate realistic operating conditions encountered in telecommunication applications and to evaluate the robustness of the protection circuit under practical installation scenarios.

3.3.4.1 Input Supply Reversal Test

To emulate a realistic installation fault, the input supply wires are intentionally reversed to apply a reverse voltage across the protection circuit. The response of the protection circuit is observed as the gate driver disables the GaN FETs and the gate voltage transitions to the off-state level. This verifies that the circuit successfully blocks reverse current flow under a polarity fault condition. The experimental setup for the input supply reversal test is shown in Figure 3.19.

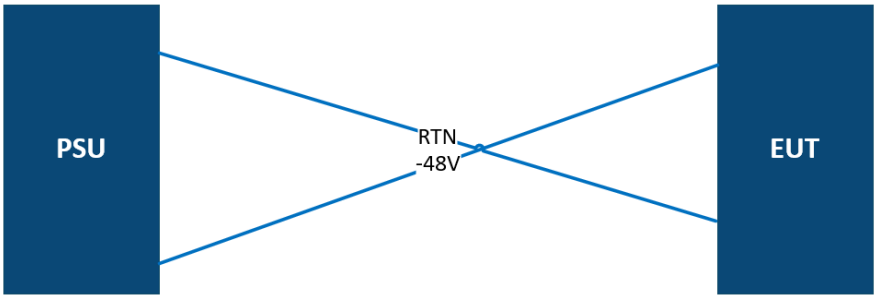

Figure 3.19: Experimental for input supply reversal test.

3.3.4.2 Y-cable simulation

In telecommunication radio applications, a single power supply unit may be connected to multiple radio units. In this test, two loads, representing independent radio units, are connected to the supply through a Y-cable configuration. When the load current condition of one branch changes, it can lead to current redistribution between the parallel branches. This is because the path to other radio units may be shorter than the path back to the PSU, meaning that the impedance between radios may be lower than the impedance back to the PSU. Therefore, current can unintentionally flow from one radio branch into another instead of being fully supplied directly by the PSU. This may lead to reverse current flow, instability, or unwanted interaction between connected units. The purpose of this test is to evaluate whether the protection circuit within the EUT can effectively block reverse current between parallel branches and maintain stable operation during asymmetric loading conditions.

The experimental setup for the Y-cable simulation is shown in Figure 3.20. One load is connected to the output of the EUT to represent a radio unit, while a second dynamic load is applied at the input side to emulate load variations from another radio sharing the same supply. The dynamic load is configured to produce a 10 A transient, while the E-load at the EUT output is set to a continuous 1 A load. This condition is used to investigate how the EUT responds when when another radio unit attempts to draw current from the parallel branch rather than directly from the PSU, due to the lower impedance path between the radios. In addition, the current threshold required to turn on the GaN FET is approximately 0.7 A. Therefore, the continuous 1 A load is used to keep the GaN FET initially conducting and to observe whether the protection circuit can properly respond and turn off the GaN FET during a reverse-current condition. This test also includes an input inductance of 100 μH to emulate line effects, and an additional filter circuit connected at the output of the EUT to represent downstream filtering and hold-up capacitance.

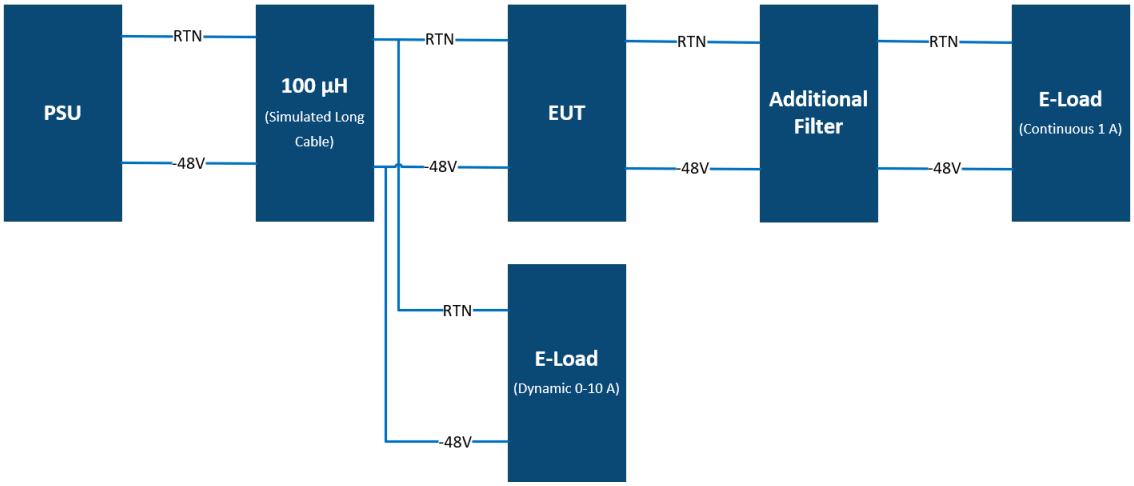

Figure 3.20: Experimental setup for Y-cable simulation.

3.3.4.3 Input Short Circuit Test

In this test, a power interrupt generator is used to intentionally create a controlled short circuit at the input of the EUT. The power interrupt generator operates using two switches. During normal operation, the switch connecting the positive and negative terminals is open, while the switch on the negative path is closed. Under this condition, the PSU delivers power to the load through the EUT, and the system operates normally. To initiate the short circuit condition, the switching states are reversed. The switch connecting the positive and negative terminals is closed, while the switch on the negative path is opened. This configuration creates a short circuit across the input of the EUT, forcing a fault condition.

This test is performed to evaluate the ability of the protection circuit to withstand high fault currents, respond rapidly to abnormal conditions, and prevent damage to the GaN FETs and surrounding components. The experimental setup for the short circuit test using the power interrupt generator is illustrated in Figure 3.21.

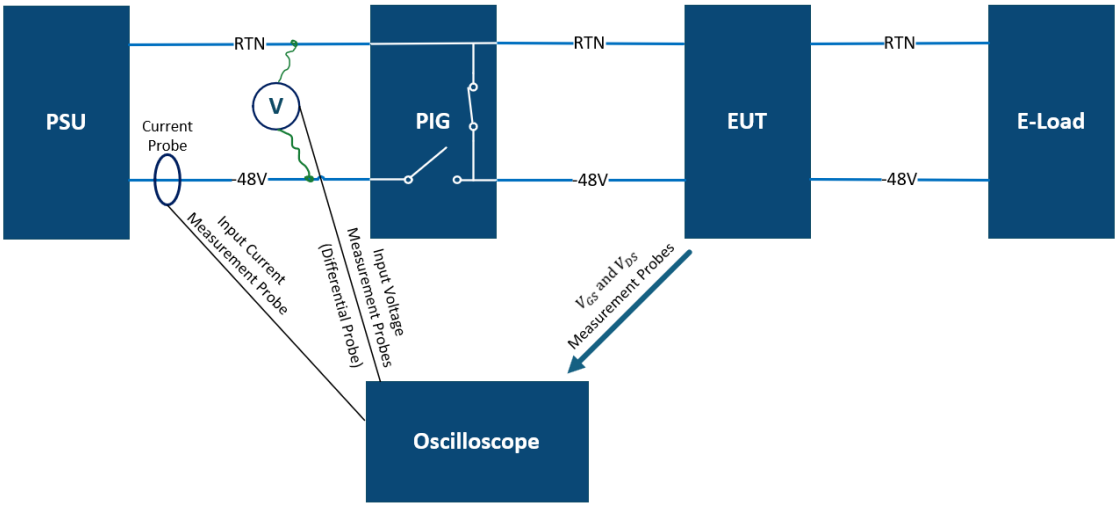

Figure 3.21: Experimental setup for short circuit test using power interrupt generator.

3.3.5 Robustness Test

The objective of the robustness test is to evaluate the operational limits of the GaN FETs and the overall prototype when subjected to conditions that exceed their rated values.

3.3.5.1 High Current Load Test

The high current load test evaluates the robustness of the prototype under overload conditions. The electronic load is set to constant current mode, while maintaining a constant input voltage of -48 V. The load current is gradually increased beyond 10 A to inspect the maximum current at which the circuit operates without thermal or electrical instability as the operational limit of the prototype.

3.3.5.2 High Slew Rate Test

The high slew-rate test evaluates the circuit performance under fast transient conditions. Fast load transitions are applied using the electronic load to generate high dI/dt stress by reducing the transition time. The maximum dI/dt at which the circuit operates normally without false turn-on or overvoltage stress is recorded as the operational limit under transient conditions.

4
Analysis

In this section, a series of LTspice simulations and hardware experiments were conducted to evaluate the dynamic performance of the proposed GaN-based reverse polarity protection.

4.1 Simulation Results

These simulation results represent an ideal case. In practice, parasitic inductances from the PCB layout and external connections may cause ringing and overshoots during step-load transients. Furthermore, rapid switching can generate electromagnetic interference (EMI), while thermal variations may cause device parameters to drift under load.

4.1.1 Simulation of Reverse Polarity Protection Circuitry

In this case study, a 10 A step load is applied to the protection circuitry to simulate a rapid power-up event. The simulation is configured to monitor gate-source voltage (V_{GS}), drain-source voltage (V_{DS}) and load current (I_{LOAD}). This represents a critical operating scenario where the protecting stage must handle full load current while the gate driving logic is still in its initial state. The resulting waveform of the step load test is shown in Figure 4.1.

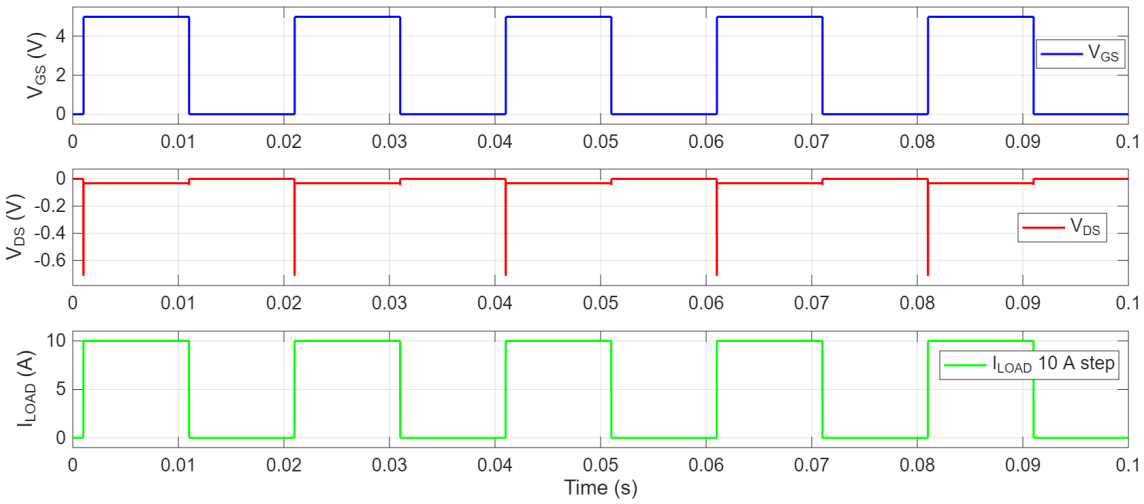

Figure 4.1: LTspice verification of the GaN FET behavior during power-up using 48 V input and 10 A load step.

Figure 4.2 presents a magnified view of the transition region from Figure 4.1, showing the change from passive protection to high-efficiency conduction. Upon the application of the 10 A load at t = 1.0 ms, V_{GS} remains at 0 V forcing the device to third quadrant conduction. During this interval, V_{DS} is observed to clamp at approximately -0.7. This confirms that the external Schottky diode is successfully commutating the current. Without this parallel diode, the GaN FET would exhibit a significant higher voltage drop leading to high instantaneous power dissipation. At about t = 1.02 ms, V_{GS} transitions to 5 V and fully enhances the GaN channel. Consequently V_{DS} collapses towards a near-zero ohmic level as the current shifts from the external diode to the active transistor channel.

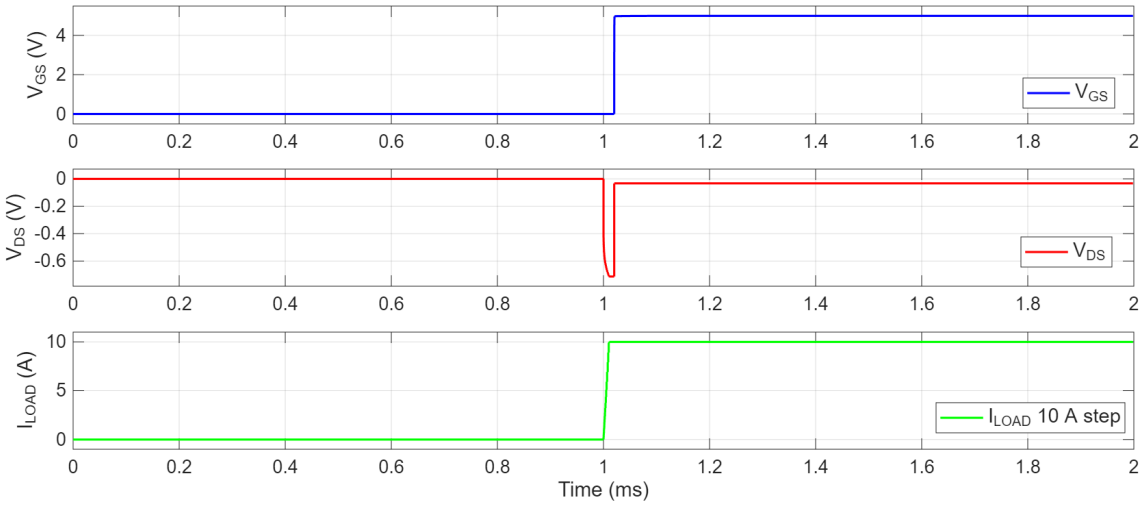

Figure 4.2: Close-up analysis of the V_{DS} voltage drop during the transition from third quadrant conduction to active channel conduction at 10 A.

4.1.2 Comparative Results

Using a simple polarity protection circuit in LTspice, the conduction losses of the diode, silicon MOSFET, and GaN FET implementations are compared in Table 4.1 at a load current of 10 A. The calculated loss was obtained from datasheet parameters, while the simulated loss was calculated from the voltage drop measured across each device in LTspice.

Table 4.1: Power loss comparison at 10 A load

Device	Datasheet parameter	Calculated P_{loss} [W]	Simulated V_{DS}/V_F [mV]	Simulated P_{loss}[W]	Simulated $V_{DS,off}$ [V]
Diode	V_F = 0.88 V	8.80	711.45	7.11	N/A
MOSFET	$R_{DS(on)}$ = 2.8 mΩ typ., 4.5 mΩ max.	0.28–0.45	34.96	0.35	0.7372
GaN	$R_{DS(on)}$ = 3.2 mΩ typ., 3.9 mΩ max.	0.32–0.39	32.98	0.33	1.6431

From Table 4.1, the diode exhibits the highest voltage drop and therefore the highest conduction loss among the three devices. This is mainly due to its forward voltage, which is significantly higher than the voltage drop across the transistors, especially at higher load current. Although the diode is simple and does not require a gate-drive circuit, its main limitations are reduced efficiency and heat generation.

In contrast, the MOSFET and GaN FET show much lower losses because their conduction losses are mainly determined by their $R_{DS(on)}$. Among the three implementations, the GaN FET gives the lowest simulated loss due to its low $R_{DS(on)}$, making it the most efficient option from a conduction loss perspective.

However, the last column of Table 4.1 shows that the GaN FET has a higher $V_{DS,off}$ when the device is turned off. This is because the MOSFET contains an intrinsic body diode, which can provide a reverse current path and clamp the voltage across the device to a diode-like voltage drop. In contrast, the GaN FET used in the LTspice simulation does not have a body diode. This highlights an important trade-off in the GaN FET implementation. While the GaN FET performs the lowest forward conduction loss, an external diode may be required across the GaN FET in applications where reverse current is expected.

4.1.3 Proof of Parallel Concept

One possible way to reduce the current stress in a power device is to connect devices in parallel. However, paralleling diodes is unusual because small differences in V_F can cause unequal current sharing between the devices. The diode with the lowest V_F will conduct more current, causing it to heat up more than the others. As temperature increases, V_F decreases further and diode attracts more current. This can lead to current imbalance, thermal runaway, and device failure.

In contrast, paralleling transistors is more practical because current sharing is mainly influenced by $R_{DS(on)}$. However, equal current sharing cannot be assumed automatically, since PCB layout, trace symmetry, R_g matching, and thermal coupling can affect current balance between the parallel GaN FETs. Since the GaN FET showed the lowest simulated conduction loss in Table 4.1, the parallel configuration was further investigated. Table 4.2 evaluates whether two GaN FETs in parallel can reduce the effective $R_{DS(on)}$, voltage drop, and conduction loss of the polarity protection circuit.

Table 4.2: Power loss comparison when using parallel GaN FETs

Configuration	Equivalent $R_{DS(on)}$	Calculated P_{loss} [W]	Simulated V_{DS}/V_F [mV]	Simulated P_{loss}[W]	Simulated $V_{DS,off}$ [V]
1 GaN	3.2 mΩ typ., 3.9 mΩ max.	0.32–0.39	32.98	0.33	1.6431
2 GaN	1.6 mΩ typ., 1.95 mΩ max.	0.16–0.20	16.49	0.16	1.5182

As shown in Table 4.2, the simulated V_{DS} and power loss decrease by half when two GaN FETs are connected in parallel. This confirms that paralleling GaN FETs can effectively reduce the conduction loss and thermal stress of the polarity protection circuit.

The $V_{DS,off}$ is also slightly reduced in the parallel configuration, from 1.6431 V to 1.5182 V. However, this reduction is much smaller than the reduction in the on-state voltage drop and power loss. This indicates that the main benefit of paralleling GaN FETs is the reduction of forward conduction loss.

4.2 Hardware Validation of GaN-Based Prototype

This section presents the analysis of the experimental results obtained from hardware testing of the prototype. It should be noted that the prototype employs discrete control logic components for validation purposes, whereas the final real-world implementation will utilize only the GaN FET and gate driver, with the control logic integrated into a microcontroller (MCU). Therefore, any instability, oscillation, noise sensitivity, or switching irregularities observed in the prototype are expected to be reduced in the final design due to improved control integration and signal management.

4.2.1 Evaluation of Components

Key component choices are evaluated before the prototype is tested under full operating conditions. The analysis first focuses on the gate resistance values, which affect switching speed and transient stability. It then examines the external diode requirement, which affects the reverse-conduction behavior before the GaN FET is fully enhanced.

4.2.1.1 Evaluation of Gate Resistance

The gate resistance was varied to evaluate how the turn-on and turn-off behavior of the GaN FET changed with different resistor values. The purpose of this test was to identify suitable values for the final gate-drive configuration, where OUT_SRC controls the turn-on path and OUT_SNK controls the turn-off path. Both the gate-source voltage V_{GS} and the drain-source voltage V_{DS} were analyzed, since V_{GS} shows the gate-drive behavior while V_{DS} shows how the switching transition affects the power path.

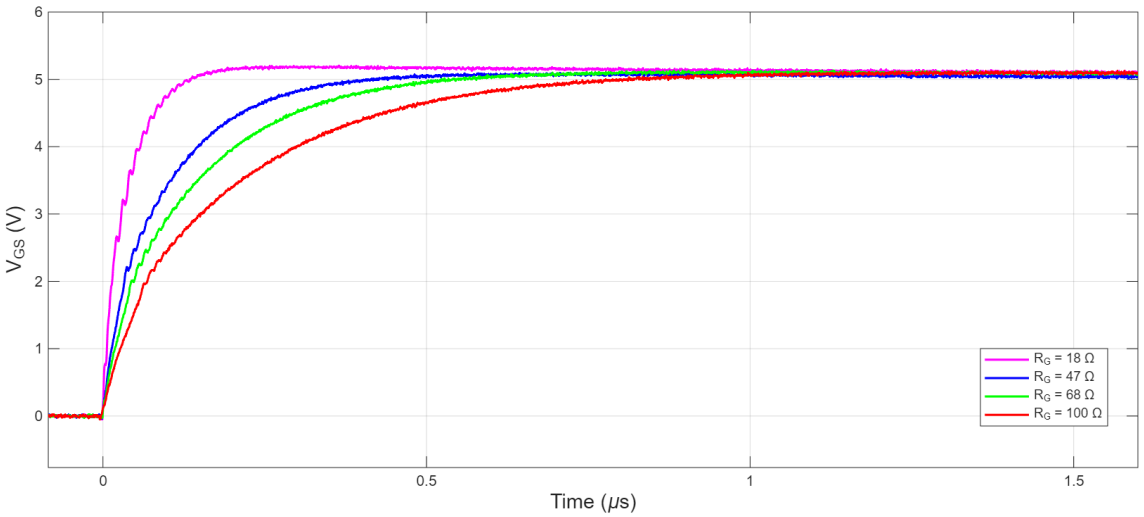

Figure 4.3: Effect of gate resistance on V_{GS} during turn-on.

From the turn-on measurements in Figure 4.3, the expected behavior can be seen, i.e that lower gate resistance values give a faster increase in V_{GS}. This confirms that the gate is charged faster when the resistance in the source path is reduced. However, the fastest turn-on response also gives a sharper transition and a less damped response after the voltage rise. As anticipated, higher resistance values give a smoother waveform, but the turn-on transition becomes slower than necessary.

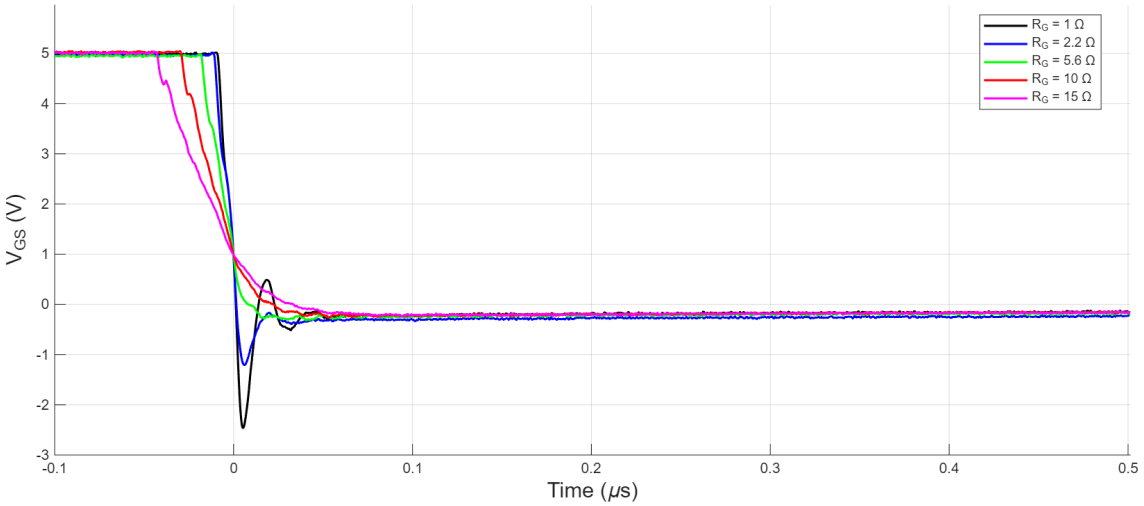

Figure 4.4: Effect of gate resistance on V_{GS} during turn-off.

The turn-off measurements in Figure 4.4 show that a lower resistance gives a faster decrease in V_{GS}. This is beneficial because the gate charge is removed more quickly and the GaN FET is forced into the off-state faster. In a reverse polarity protection circuit, fast turn-off is important because the device must stop conducting quickly during abnormal or fault-related conditions.

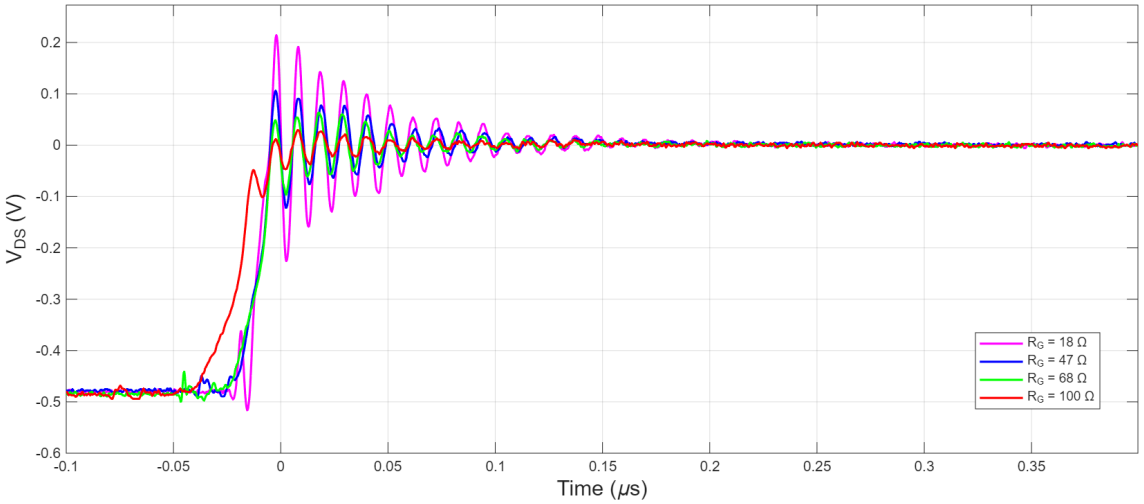

Figure 4.5: V_{DS} turn-on response for different gate resistance values.

The corresponding V_{DS} turn-on response in Figure 4.5 shows that the faster turn-on cases produce a sharper voltage transition and more visible ringing. This indicates that the lowest resistance values provide less damping in the gate-drive and power-loop transient. Since GaN devices are sensitive to gate-voltage disturbances and fast voltage changes, excessive ringing can increase the risk of unstable switching behavior and possible false turn-on.

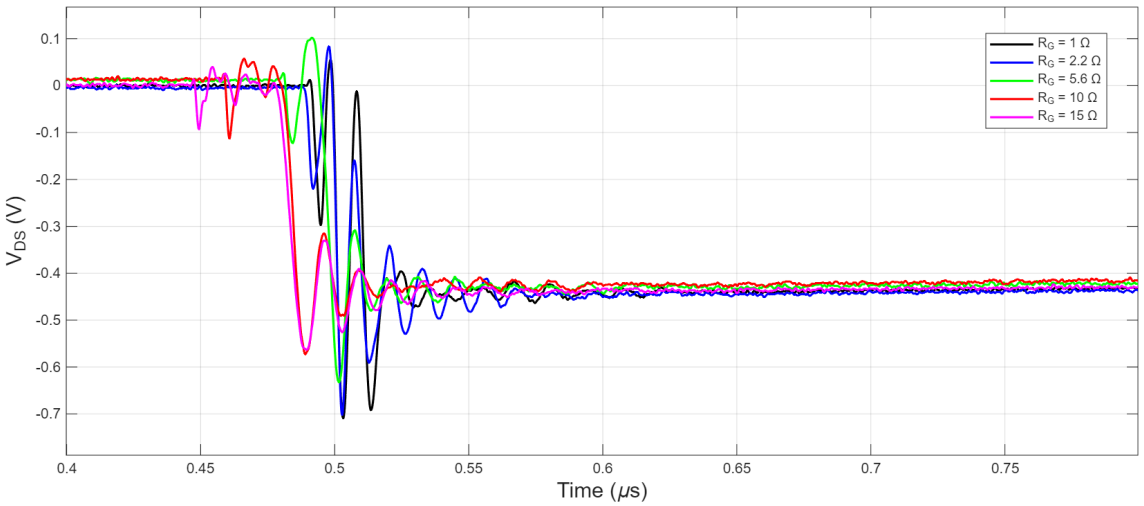

Figure 4.6: V_{DS} turn-off response for different gate resistance values.

The V_{DS} turn-off response in Figure 4.6 shows that the voltage transition includes some undershoot and ringing, which is expected during fast switching because of parasitic inductance and capacitance in the circuit. However, the waveform settles quickly and does not show excessive oscillation for the selected value. This supports the use of a low turn-off resistance, since it gives a fast gate discharge while still maintaining acceptable transient behavior.

Table 4.3: Measured effect of turn-on gate resistance on waveform characteristics

$R_{G,on}$ [Ω]	V_{GS} rise time [ns]	$V_{GS,peak}$ [V]	V_{GS} ringing amplitude [V]	$V_{DS,peak}$ [V]	V_{DS} ringing amplitude [V]	Waveform observation
18	82.20	5.20	0.096	0.21	0.44	Fastest turn-on, sharpest transition
47	213.20	5.13	0.059	0.11	0.23	Fast turn-on with visible ringing
68	307.20	5.13	0.042	0.06	0.12	Moderate transition and improved damping
100	447.60	5.13	0.032	0.03	0.07	Smoothest response, slower turn-on

Table 4.4: Measured effect of turn-off gate resistance on waveform characteristics

$R_{G,off}$ [Ω]	V_{GS} fall time [ns]	$V_{GS,min}$ [V]	V_{GS} ringing amplitude [V]	$V_{DS,min}$ [V]	V_{DS} ringing amplitude [V]	Waveform observation
1	8.60	-2.46	2.951	-0.71	0.76	Fastest discharge, most aggressive transient
2.2	10.40	-1.20	1.035	-0.70	0.79	Fast turn-off with acceptable damping
5.6	18.40	-0.32	0.108	-0.63	0.74	Balanced turn-off response
10	34.80	-0.27	0.080	-0.57	0.63	Slower discharge, smoother waveform
15	51.00	-0.24	0.056	-0.56	0.60	Slowest turn-off, highest damping

Based on these results, $R_{g,on} = 47\ \Omega$ was selected for OUT_SRC. This value provides a balanced turn-on response, where the V_{GS} rise time is still acceptable while the ringing in both V_{GS} and V_{DS} is reduced compared with the lowest resistance values. The selected value therefore avoids an unnecessarily aggressive turn-on transition and gives better damping against switching-related disturbances. For the turn-off path, $R_{g,off} = 10\ \Omega$ was selected for OUT_SNK. This value gives a strong gate-discharge path and supports a fast and reliable turn-off response. A low turn-off resistance also helps keep the gate voltage low, improving immunity against false turn-on caused by transient coupling through parasitic capacitances.

The final choice of 47 Ω for turn-on and 10 Ω for turn-off is therefore based on the measured trade-off between damping, switching speed, V_{DS} transient behavior and false turn-on immunity. A higher resistance is used during turn-on to reduce ringing and improve waveform stability while a lower resistance is used during turn-off to quickly discharge the gate and keep the device securely in the off-state.

4.2.1.2 Evaluation of External Diode Requirement

During OFF-state operation, reverse current flows through the reverse conduction path of the transistor. In conventional silicon MOSFETs, this current is carried by the intrinsic body diode. In contrast, the selected GaN FET employs an integrated Schottky diode, addressing the lack of a body diode in GaN transistors. Although the datasheet specifies a source-drain reverse voltage of $V_{SD} = 0.9$–1.9 V depending on pulsed source current, the practical loss was experimentally evaluated.

The test was performed using only the GaN FET, without an external parallel diode. At a load current of 0.2 A, the measured voltage drop was 0.832 V, corresponding to a power dissipation of 0.1664 W. Consequently, an equivalent reverse conduction resistance can be estimated as R = 0.832/0.2 = 4.16 Ω. Using this measured value, the estimated conduction loss just before the GaN FET turns ON at the threshold current of 0.7 A becomes approximately 2.04 W. This is relatively high at a low current level. Therefore, the external diode connected in parallel with the GaN FET is required to provide a lower-loss reverse current path during the OFF period before the GaN FET turns ON.

4.2.2 Functional Verification

Before moving into the dynamic response tests, the prototype is first evaluated under steady and basic operating conditions. This section examines the forward conduction behavior, thermal distribution, voltage drop, power loss and efficiency of the GaN-based protection circuit, while also comparing the single-GaN, two-parallel GaN and MOSFET-based configurations under relevant load conditions

4.2.2.1 Functional Verification Under Forward Operation

The prototype was tested under forward bias with a load current of 10 A. The measured waveforms include the current I, the drain to source voltage V_{DS} and the gate to source voltage V_{GS} are shown in Figure 4.7.

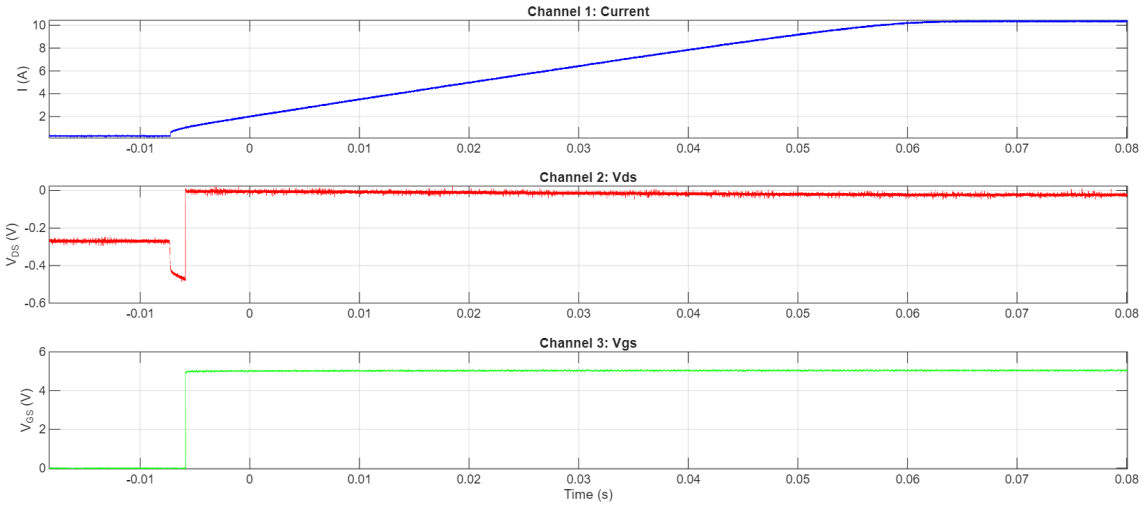

Figure 4.7: Measured forward conduction test of the GaN device at 10A during turn-on.

Figure 4.7 shows the measured forward conduction response of the GaN-based polarity protection at a load current of 10 A. Before turn-on, the gate to source V_{GS} is at 0 V while the drain to source voltage V_{DS} remains at a negative value, indicating that the device is not fully enhanced. When the gate-drive signal is applied, V_{GS} rises to approximately 5 V causing the GaN device to transition into the on-state. This is followed by a rapid reduction from initial negative level in V_{DS} toward 0 V, showing that the voltage drop across the transistor becomes very small in the on-state. At the same time, the load current increases to the defined operating level of 10 A and remains stable after turn-on. The measured waveform therefore confirms correct switching operation of the implemented prototype under forward conduction.

The low V_{DS} is consistent with the low on-state $R_{DS(on)}$ characteristic of the GaN device which is a key factor for achieving low conduction losses in the proposed polarity protection circuit. In addition, no significant oscillatory behavior or false triggering is observed in the measured V_{GS} waveform, indicating stable turn-on behavior for this operating condition.

4.2.2.2 Thermal Performance During Operation

The overall thermal distribution of the PCB during operation is shown in Figure 4.8.

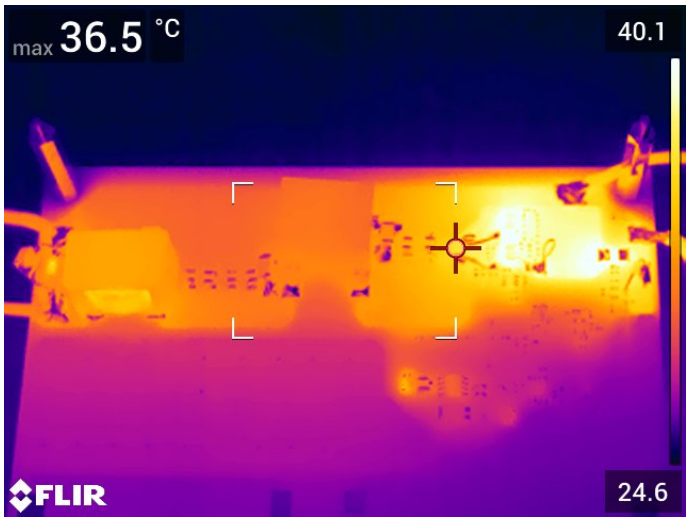

Figure 4.8: Thermal image of the PCB under operating condition.

It can be observed that the heat is mainly concentrated around the GaN FETs and R_{sense}, with no unexpected hotspots occurring. This indicates that both components are the main contributors to power dissipation during operation. Therefore, the following thermal analysis focuses on the GaN FET and R_{sense} under three load conditions, including 10 A continuous load, 0-10 A step load, and 0-19 A step load. For both step load tests, the ON and OFF times are 100 ms. The measured surface temperatures after 5 minutes of operation are summarized in Table 4.5.

Table 4.5: Measured surface temperature under different load conditions after 5 minutes of operation

Configuration	Device	Continuous Load (10 A) [°C]	Step Load (0–10 A) [°C]	Step Load (0–19 A) [°C]
1 GaN	GaN	54.1	38.8	–
	R_{sense}	44.4	37.2	–
2 GaN	GaN	41.9	33.7	54.3
	R_{sense}	45.1	34.9	62.1

The results in Table 4.5 show that thermal performance is strongly affected by both device configuration and load condition. This behavior can be explained by conduction loss, which is the dominant loss mechanism in this primarily static application, using (2.3). As load current increases, power loss increases with the square of current, resulting in higher temperature rise.

According to the GaN FET datasheet, the typical $R_{DS(on)}$ is 3.9 mΩ at $V_{GS} = 5$ V and 25 °C, with a maximum value of 5.0 mΩ. Since $R_{DS(on)}$ increases with temperature, device heating leads to higher conduction loss. The datasheet also mentions R_{thJA} is 38 °C/W for a 4-layer PCB with thermal vias, while the R_{thJC} (top) is only 0.5 °C/W. These values indicate that heat can be transferred efficiently from the junction to the package surface. However, the dissipation to ambient depends

strongly on the PCB layout and cooling conditions.

For the single-GaN configuration, when the load current was increased to 19 A, both continuous-load and step-load tests showed a rapid and continuous temperature rise without approaching thermal equilibrium and exceeded the acceptable touch-safe operating temperature before 5 minutes. This indicates that a single device has a potential risk of thermal runaway, as the cooling capability of the prototype was insufficient for high-current operation.

In contrast, the parallel GaN configuration reduced the GaN FET measured temperature as it shares current between devices. However, R_{sense} became the hottest component, as shown in Figure 4.9. This is because it continuously carried the full load current, while the parallel GaN FETs shared the conduction current.

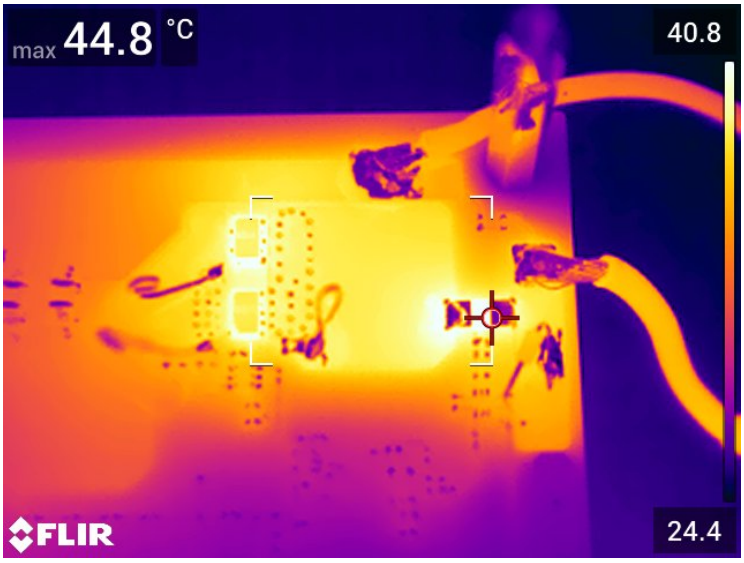

Figure 4.9: Thermal image of the parallel GaN FETs and R_{sense}.

Therefore, for higher load conditions, a higher power rated R_{sense} or parallel R_{sense} configuration should be considered. In addition, localized heating near R_{sense} indicates that the copper area in that region may be insufficient for effective heat spreading. Narrow copper traces or limited copper plane area, as shown in Figure 3.7 and 3.8, can increase current density and reduce thermal dissipation capability.

Overall, the thermal performance of the circuit does not only depend on the GaN device itself, but also by the PCB thermal design. Hence, proper PCB layout, thermal management, and component selection are crucial to fully utilize the low-loss characteristic of the GaN FET and ensure reliable long-term operation.

4.2.2.3 Power Losses

In this primarily static application, the GaN FET is used as a polarity protection switch. During normal operation, the device remains in the ON state and continuously conducts the load current. Under polarity fault or transient conditions,

the device is turned OFF to block reverse current. Since the circuit does not operate under continuous high-frequency switching, conduction loss is the dominant loss mechanism, The conduction loss can be calculated using (2.3). The measured voltage drop and corresponding power loss are summarized in Table 4.6.

Table 4.6: Measured voltage drop and power loss under different load conditions for single and two-parallel GaN configurations

Configuration	I_{load} [A]	Measured V_{DS} [mV]	Measured P_{loss} [W]	Calculated P_{loss} [W]
1 GaN	1	3.85	0.0039	0.0039
	5	19.85	0.0993	0.0975
	10	44.55	0.4455	0.3900
2 GaN	1	2.03	0.0020	0.0020
	5	10.20	0.0510	0.0488
	10	21.04	0.2104	0.1950
	15	33.25	0.4988	0.4388
	19	46.50	0.8835	0.7040

According to Table 4.6, measured V_{DS} and power loss increase with load current. The two-parallel GaN configuration exhibits lower voltage drop and power dissipation than the single GaN configuration. This is because the parallel configuration reduces the effective $R_{DS(on)}$, enabling the circuit to handle higher load currents.

Based on the equivalent $R_{DS(on)}$ derived from the typical $R_{DS(on)}$ values from datasheet, the theoretical conduction losses were calculated using (2.3). However, the theoretical values calculated using room-temperature resistance represent the minimum expected loss during operation. In practical operation, $R_{DS(on)}$ increases with junction temperature, which causes additional conduction loss under elevated thermal conditions. To verify the theoretical analysis, hardware testing was performed by measuring the drain-source voltage drop as shown in Table 4.7.

Table 4.7: Comparison of calculated and measured losses, V_{DS}, and dV/dt for different device configurations after 10 seconds of continuous load operation at 10 A and 19 A.

Configuration	Equivalent $R_{DS(on)}$ [mΩ]	Calculated P_{loss} at 10 A [W]	Measured V_{DS} at 10 A [mV]	Measured P_{loss} at 10 A [W]	dV/dt at 10 A [mV/s]	Calculated P_{loss} at 19 A [W]	Measured V_{DS} at 19 A [mV]	Measured P_{loss} at 19 A [W]	dV/dt at 19 A [mV/s]
6-parallel MOSFET	2.533	0.253	18.6	0.186	0.01	0.914	35.4	0.673	0.05
1 GaN FET	3.9	0.39	41.9	0.419	0.32	1.408	106.4	2.020	2.88
2-parallel GaN FET	1.95	0.195	20.6	0.206	0.03	0.704	41.6	0.790	0.32

According to Table 4.7, overall, the parallel-device configurations exhibit a lower calculated loss than single GaN configuration due to its lower $R_{DS(on)}$. The six-parallel

MOSFET configuration provides a calculated loss higher than the dual-parallel GaN configuration. This shows that the lower intrinsic resistance of the GaN device allows fewer devices to achieve comparable or better conduction performance.

Furthermore, the measured power loss of the single GaN configuration was 0.419 W at 10 A and increased significantly to 2.020 W at 19 A, which is higher than the theoretical calculations. This is mainly due to self-heating during operation, as the single-GaN configuration was not capable of efficiently handling the high current load, which increases the junction temperature and consequently raises the effective $R_{DS(on)}$ value.

However, at 19 A load current, the measured power loss of the six-parallel MOSFET configuration is lower than that of the two-parallel GaN FET configuration, which contrasts with the calculated values. This is because the thermal spreading in the MOSFET configuration is better. In this test, the MOSFETs use a larger 5×6 package on a 14-layer PCB, while the GaN FETs use a smaller 3×5 package on a 2-layer PCB. In addition, the MOSFET configuration consists of two strings of three parallel devices, allowing heat to be distributed across multiple devices and a larger PCB area. Therefore, in practical operation, the two-parallel GaN FET configuration exhibits higher measured loss and larger dV/dt due to more limited thermal dissipation capability and poorer cooling conditions.

In addition, the measured dV/dt values indicate that the single-device configuration experienced a faster rise in voltage drop over time, particularly at 19 A. The dual-parallel GaN arrangement showed a much smaller dV/dt, indicating improved thermal stability. This is because when two GaN FETs are connected in parallel, the effective output capacitance (C_{oss}) and total gate charge increase approximately in proportion to the number of devices.

4.2.2.4 Efficiency

The calculated and measured power losses from Table 4.7 were further used to determine the conduction efficiency of GaN FET using (3.2), where only the loss at GaN FET is considered. The results are presented in Table 4.8.

Table 4.8: Theoretical and measured efficiency of GaN FET at 19 A

Configuration	Theoretical η_{GaN} at 19 A [%]	Measured η_{GaN} at 19 A [%]
6-parallel MOSFET	99.8999	99.9263
1 GaN FET	99.8459	99.7790
2-parallel GaN FET	99.9229	99.9135

According to Table 4.8, efficiencies of all configurations are higher than 99%, This means the conduction loss of the protection device is very small compared with the load power. The 2-parallel GaN FET configuration provided the highest theoretical

efficiency at 99.9229%, due to its lowest calculated ON-state loss.

In practical measurement, the 6-parallel MOSFET configuration achieved the highest efficiency of 99.9263%, mainly due to lower measured loss under actual thermal conditions. The single-GaN configuration showed the lowest measured efficiency of 99.7790%, caused by the higher voltage drop and power dissipation at 19 A. These results confirm that reducing conduction loss through parallel-device operation improves the efficiency of the protection stage, especially under high-current operation.

4.2.3 Dynamic Response Under Step Load Test

The dynamic response test evaluates how the GaN-based protection circuit behaves during rapid load current changes. This section first analyzes the transient behavior of the GaN prototype during step load operation and then compares its response with the existing MOSFET-based protection solution.

4.2.3.1 Dynamic Response of GaN FET Under Step Load Test

The dynamic response of the GaN-based protection stage was evaluated using a 10 A step load test. The measured signals were the load current I_{load}, the drain-source voltage V_{DS} and the gate-source voltage V_{GS}. These signals were selected because they show the interaction between the control circuit and the main power path. The load current represents the response of the protected output path, V_{DS} shows the voltage drop and transient stress across the GaN device and V_{GS} shows whether the gate driver keeps the GaN device correctly controlled during the transient. The turn-on and turn-off responses are illustrated in Figure 4.10 and Figure 4.11.

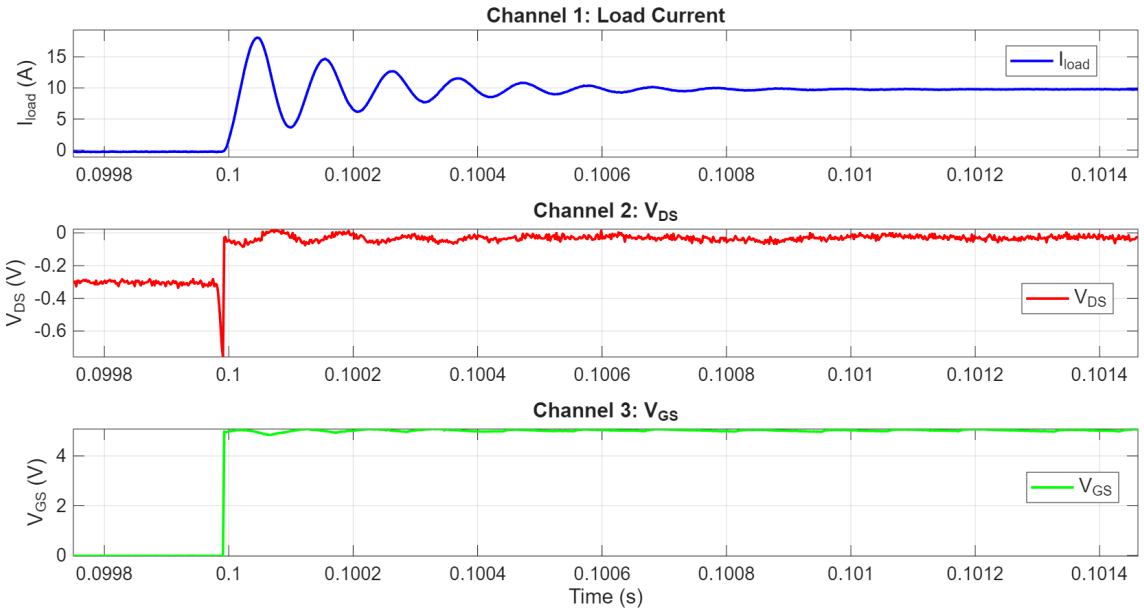

Figure 4.10: Measured turn-on transient for the two-parallel connected GaN FETs.

Figure 4.10 shows the turn-on response when the GaN device is enabled and the 10 A load is applied. Before the transition, V_{GS} is close to 0 V which means that the

GaN channel is not actively enhanced. At approximately $t = 0.1\ s$, V_{GS} rises rapidly to about 5 V. This indicates that the control chain has enabled the gate driver and that the GaN device is driven into conduction. Since the GaN FET is used as the main series element in the protection path, the rise in V_{GS} allows current to flow from the input to the load.

The load current rises quickly and reaches an initial peak of approximately 18 A before it oscillates and settles close to 10 A. This overshoot is caused by the fast establishment of the current path together with the parasitic inductance and capacitance in the circuit. When the GaN device turns on, the current changes with a high di/dt. The stored energy in the inductive parts of the current path and the charging or discharging of circuit capacitances create a temporary oscillation. Since the oscillation is damped and the current stabilizes at the intended 10 A level, the result shows that the circuit reaches a stable operating point after the initial transient.

The V_{DS} waveform supports this interpretation. Before turn-on, a small voltage is present across the GaN device. At the switching instant, V_{DS} shows a short disturbance and then settles close to 0 V. This behavior is expected because the device changes from an off-state condition to a low-resistance conducting state. Once the gate voltage has reached the drive level, the GaN channel is fully enhanced and the voltage drop across the device becomes low. The small remaining V_{DS} during steady state operation is mainly related to the on-state resistance of the device and the load current.

The V_{GS} waveform remains close to 5 V after turn-on with only a small ripple. This is an important observation because the current overshoot does not cause a significant gate disturbance. The gate driver therefore maintains the GaN device in the in-state during the transient. This indicates that the gate-drive path and the local gate control are sufficiently stable for the tested 10 A step load condition.

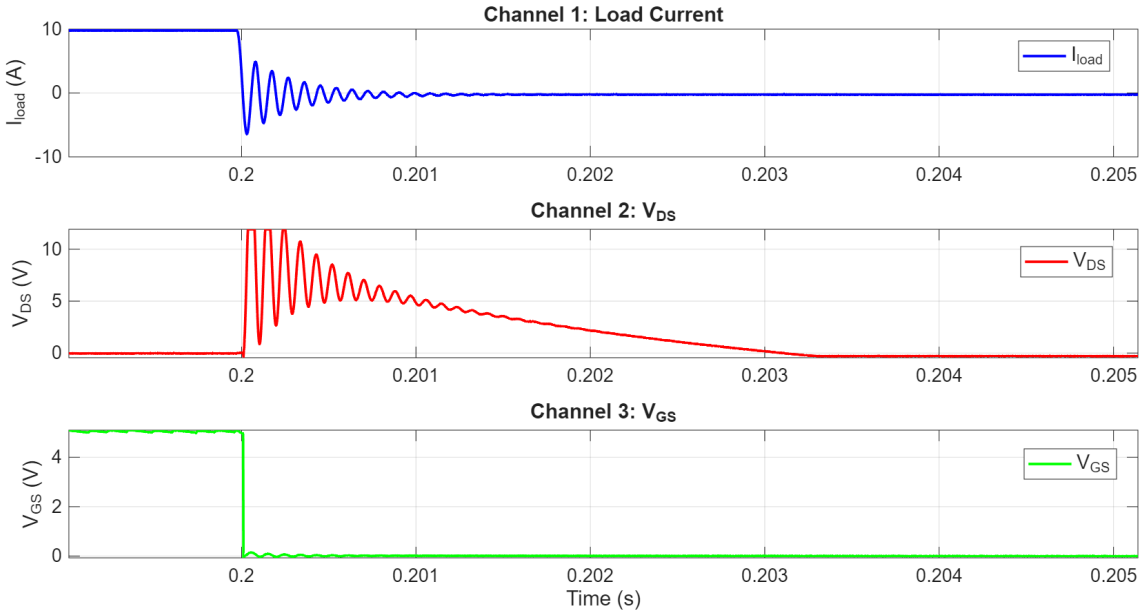

Figure 4.11: Turn-off transients response of the two-parallel connected GaN FETs

Figure 4.11 shows the turn-off response when the GaN device is disabled from the 10 A load condition. Before the transition, V_{GS} is approximately 5 V and the load current is close to 10 A. At approximately $t = 0.2\ s$, V_{GS} drops rapidly to 0 V. This removes the gate drive from the GaN device and turns off the main current path.

After turn-off, the load current falls rapidly and shows a negative undershoot followed by damped oscillations. This behavior occurs because the current in an inductive path cannot change instantaneously. When the GaN device interrupts the current, the energy stored in the parasitic inductance and the external current path must be redistributed in the circuit. This produces and oscillating current response until the energy is dissipated. The current settles close to 0 A which confirms that the load current has been interrupted and that no continuous conduction remains after turn-off.

The V_{DS} waveform increases during turn-off and reaches a temporary overshoot of approximately 12 V before decaying. This is caused by the fast current decrease through the parasitic inductance of the current path. According to the inductive voltage relation in (2.15), a high current slew rate produces an additional voltage across the inductive path of the circuit. This voltage appears across the GaN device and results in the observed V_{DS} overshoot. The following ringing is caused by the interaction between loop inductance and capacitance in the circuit. The oscillation decays as the stored energy is dissipated through the resistive part of the circuit.

The gate-source voltage remains close to 0 V after the turn-off command with only a small disturbance during the transient. This shows that the gate driver keeps the GaN device in the off-state even while I_{load} and V_{DS} are oscillating. This is important because a large disturbance on V_{GS} could unintentionally turn the GaN device on again. In this measurement, the gate voltage remains below the threshold which

indicates that the gate-drive circuit maintains proper control during the turn-off transient.

4.2.3.2 Comparison of Dynamic Response of GaN FET and MOSFET-Based Solution

The dynamic response of the GaN FET-based protection board was compared with the existing six-MOSFET-based solution by analysing the measured input current, drain-source voltage and gate-source voltage waveforms. Since the two boards use different control circuits and different semiconductor devices, the comparison is made at system level. This means that the measured response represents the complete protection solution, including the power devices, gate-drive circuit, current path, PCB layout and parasitic effects.

The comparison focuses mainly on the switching behaviour and transient response during normal load transients. The most relevant parameters are the V_{GS} rise and fall times, the steady-state V_{DS} during conduction, the peak V_{DS} during turn-off, the voltage overshoot, ringing amplitude, settling time and current fall time. The input current level is included only to confirm that both boards were tested under the same load condition.

Figure 4.12 shows the measured turn-on response of the two protection solutions. Both boards establish the same load current, but the gate-source voltage behaviour is clearly different. The GaN FET-based solution reaches its gate-drive level almost immediately after the transient, while the MOSFET-based solution shows a considerably slower V_{GS} rise. This indicates that the GaN board has a faster gate-drive response during activation.

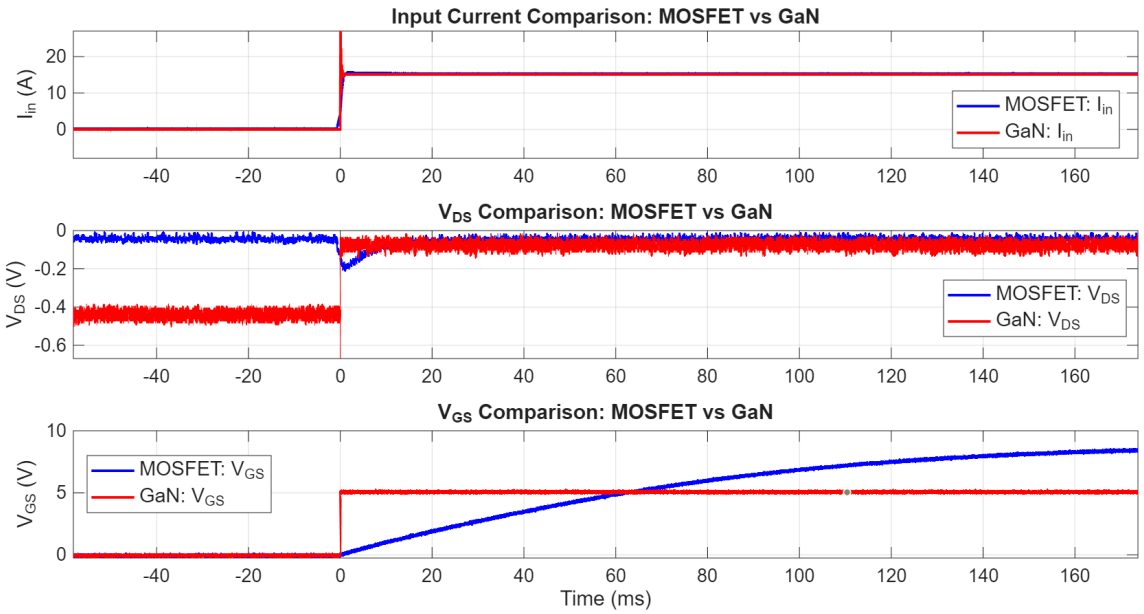

Figure 4.12: Measured turn-on waveforms of I_{in}, V_{DS}, and V_{GS} for the six-MOSFET and GaN FET boards.

Figure 4.13 shows the measured turn-off response. The GaN FET-based solution interrupts the current faster than the MOSFET-based solution. However, the faster turn-off also produces a higher V_{DS} transient and more pronounced ringing. In comparison, the MOSFET-based solution turns off more gradually and shows a smoother voltage response. This behavior illustrates the trade-off between fast switching and transient voltage stress.

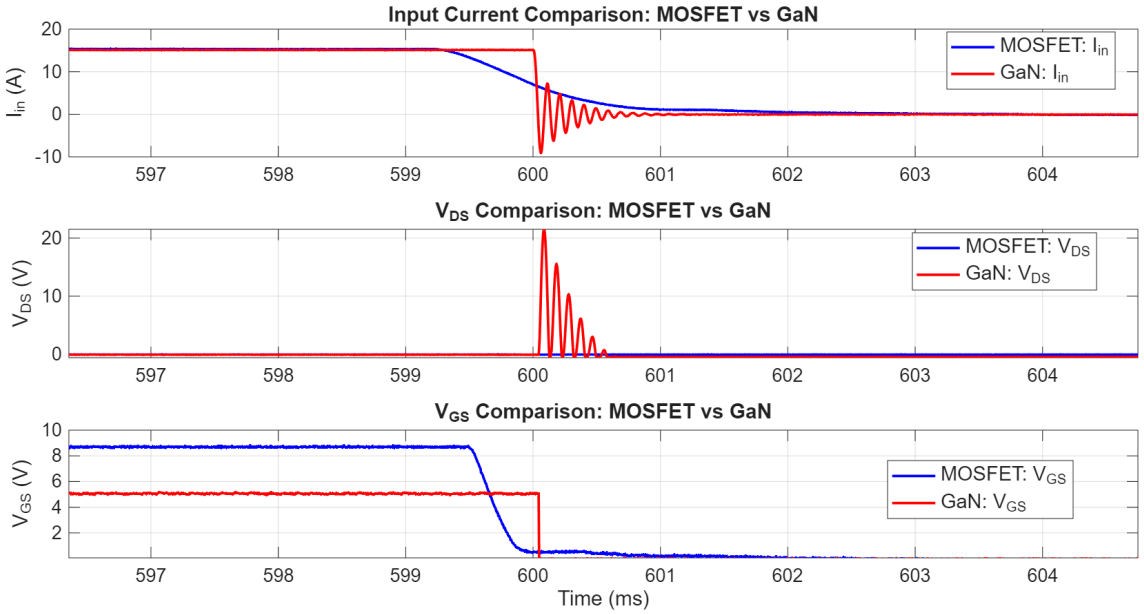

Figure 4.13: Measured turn-off waveforms of I_{in}, V_{DS}, and V_{GS} for the six-MOSFET and GaN FET boards.

The quantitative values extracted from the measured waveforms are presented in Table 4.9. The V_{GS} rise and fall times were evaluated using the 10–90% transition method, while $\mathrm{d}V_{DS}/\mathrm{d}t$ was evaluated between 40% and 60% of the turn-off voltage transition. The steady-state V_{DS} was calculated from the settled conduction interval, while the peak V_{DS}, overshoot and ringing amplitude were extracted from the turn-off transient region. Since the GaN V_{GS} transition occurs within only a few samples, the values are limited by the measurement time resolution and should be interpreted as an indication of very fast gate response rather than exact switching times.

Table 4.9: Quantitative comparison of the measured dynamic response between the six-MOSFET-based solution and the GaN FET-based solution

Parameter	**Unit**	**6-parallel MOSFET solution**	**GaN FET solution**
Load current before turn-off	A	15	15
Final V_{GS} during conduction	V	8.69	5.06
V_{GS} rise time during turn-on	ms	108.32	< 0.004
V_{GS} fall time during turn-off	ms	0.343	< 0.004
Steady-state V_{DS} during conduction	V	0.0427	0.0787
Peak V_{DS} during turn-off	V	< 0.1	21.51
V_{DS} overshoot during turn-off	V	0.0385	21.95
$\mathrm{d}V_{DS}/\mathrm{d}t$ during turn-off	V/μs	0.0028	0.798
V_{DS} ringing amplitude during turn-off	V_{pp}	0.0826	22.10
V_{DS} settling time after turn-off	ms	0.068	0.400
Input-current fall time	ms	1.28	0.022

The quantitative comparison shows that both solutions were tested at approximately the same current level of 15 A. Therefore, the observed differences are mainly related to the dynamic behavior of the two protection solutions rather than differences in load current.

A clear difference can be observed in the gate-source voltage response. The GaN FET-based solution reaches its gate-drive level much faster than the MOSFET-based solution. The extracted V_{GS} rise and fall times for the GaN solution are below 0.004 ms, while the MOSFET-based solution has a measured V_{GS} rise time of 108.32 ms and a fall time of 0.343 ms. This indicates that the GaN-based board has a significantly faster gate-drive response. However, since the GaN transition is close to the measurement time resolution, the values should be interpreted as a resolution-limited result rather than exact rise and fall times.

The steady-state V_{DS} during conduction is lower for the MOSFET-based solution in this test. The measured value is approximately 0.0427 V for the MOSFET solution and 0.0787 V for the GaN solution. However, this value should be interpreted as the voltage drop of the complete measured current path, not only the voltage drop of the semiconductor device. The result is therefore affected by the PCB layout, current path, measurement points, sense resistor and other series resistances in the prototype.

During turn-off, the GaN-based solution shows a much faster current interruption. The measured input-current fall time is approximately 0.022 ms for the GaN solution, compared with 1.28 ms for the MOSFET-based solution. This confirms that the GaN board reacts faster during the transient. This is also supported by the

measured $\mathrm{d}V_{DS}/\mathrm{d}t$, which is approximately 0.798 V/μs for the GaN solution compared with 0.0028 V/μs for the MOSFET-based solution. The higher voltage slew rate indicates a much faster voltage transition during turn-off. However, this also means that the GaN solution is more sensitive to parasitic inductance in the current path.

The faster current interruption and higher $\mathrm{d}V_{DS}/\mathrm{d}t$ result in a much higher V_{DS} transient. The GaN solution reaches a peak V_{DS} of approximately 21.51 V during turn-off, while the MOSFET-based solution only shows a small voltage disturbance. The GaN waveform also shows a larger ringing amplitude, approximately 22.10 V_{pp}, compared with 0.0826 V_{pp} for the MOSFET solution.

This behaviour shows the trade-off between fast switching and transient stress. The GaN FET-based solution provides a significantly faster dynamic response, especially in the gate-voltage transition, voltage slew rate and current interruption. However, the rapid transition excites parasitic inductance in the current path, which results in higher V_{DS} overshoot and more pronounced ringing. The MOSFET-based solution has a slower response and much lower $\mathrm{d}V_{DS}/\mathrm{d}t$, but its turn-off transient is smoother and more damped.

4.2.4 Real Application Emulation

The real application emulation tests were performed to evaluate the GaN-based reverse polarity protection circuit under conditions closer to practical operation. In addition to normal forward conduction, the protection stage must also handle incorrect input connection and possible interaction with other connected load paths.

4.2.4.1 Input Supply Reversal

The reverse polarity test was performed to verify the blocking capability of the proposed GaN-based RPP circuit when the input is connected with incorrect polarity. The purpose of this test is to confirm that the protection stage does not establish a low-impedance conduction path under reverse polarity conditions and the downstream load is electrically isolated from reversed input source.

In contrast to the forward conduction test, the GaN device is not expected to be actively enhanced during reverse polarity. Therefore the measured waveform does not represent normal turn-on behavior. Instead, the response is mainly dominated by the trasient interaction between the input side capacitance, the device parasitic capacitance, the supply path inductance and the measurement loop inductance. The measured reverse polarity response is shown in Figure 4.14 which includes the input current I_{in}, the drain to source voltage V_{DS}, the gate to source voltage V_{GS} and the input voltage V_{in}.

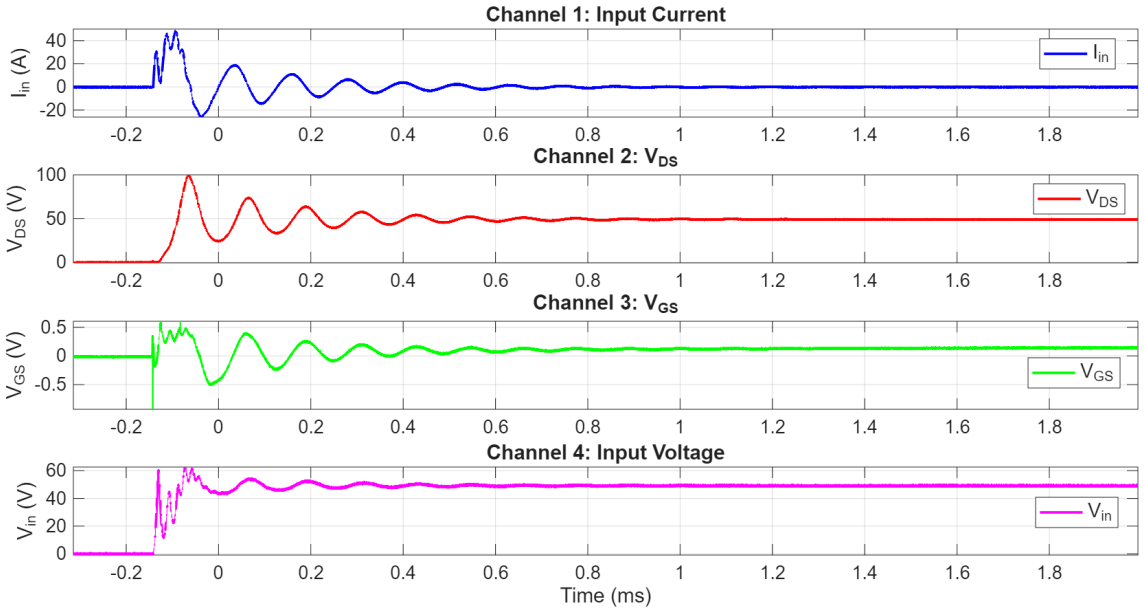

Figure 4.14: Measured transient response of the GaN-based RPP during input supply reversal test

As shown in Figure 4.14, the application of reverse polarity produces a short transient response at the input of the circuit. The input current I_{in} reaches a peak of approximately 48 A, followed by a negative drop to approximately -26 A. After this initial event , the current oscillates with decreasing amplitude and finally settles at 0 A. This indicates that the observed current is not a continuous reverse conduction current through the GaN device. Instead, it is mainly caused by the charging and discharging of the capacitative elements at the input and around the device.

The transient current can be described by the capacitor current relation

$$i_c = C\frac{dv}{dt} \tag{4.1}$$

where C represents the effective input side and device related capacitances. This includes contributions from the input capacitance , PCB parasitic capacitance and the output capacitance of the GaN device. Since the reverse input is applied rapidly, dv/dt becomes high which produces a short displacement current even though the transistor remains in the blocking state. This explains why a large current spike is observed only during the transient interval, while the steady-state current approaches zero after the circuit has settled.

The measured V_{DS} rises sharply during the same interval and reaches a peak close to 100 V before settling to approximately 48-50 V. This indicates that the GaN device supports the applied reverse voltage across its drain-source terminals. In other words, the device behaves as the main blocking element of the protection stage rather than as a conducting switch. The initial overshoot in V_{DS} is caused by the interaction between the fast current transient and the parasitic inductance in the input path. This can be described by

$$v_L = L\frac{di}{dt} \tag{4.2}$$

where L is the effective loop inductance and di/dt is the rate of change of the transient current. A high current slope during the connection event therefore generates an additional inductive voltage component, which appears as the measured overshoot across the device.

The input voltage V_{in} shows a similar transient behavior. It rises rapidly, overshoots to approximately 60 V and then settles around the nominal reverse input level of 48 V. The fact that both V_{in} and V_{DS} settle to almost the same voltage level shows that the reverse voltage is mainly blocked across the protection stage. This is the expected behavior for a RPP circuit since the protected output side should not be forced into reverse supply operation.

The ringing observed in I_{in}, V_{DS} and V_{in} can be interpreted as an underdamped parasitic LC response. The effective resonance is determined by the total parasitic inductance L_p and capacitance C_p according to

$$f_r = \frac{1}{2\pi\sqrt{L_p C_p}} \tag{4.3}$$

where L_p includes contributions from the supply cable, PCB traces, connectors and probe loop while C_p includes the GaN output capacitance C_{oss}, drain-gate capacitance C_{GD}, input capacitance and additional capacitance in the input node. Since the oscillation is damped and disappears after the first transient interval, the waveform indicates that the reverse polarity event excites the parasitic network only temporarily and does not lead to sustained instability.

The V_{GS} waveform remains small during the entire reverse polarity event. The disturbance is within the range of -1 V to 0.6 V, which is far below the gate-drive voltage used during forward operation where V_{GS} is approximately 5 V. Therefore, the GaN device is not intentionally enhanced during the reverse polarity transient.

The small oscillation observed in V_{GS} is attributed to the gate node being floating or weakly referenced during the blocking condition. When the drain voltage changes rapidly, charge can be coupled into the gate through the drain-gate capacitance C_{GD}, also referred to as Miller capacitance. The induced gate disturbance can be expressed as

$$i_{G,coupled} = C_{GD}\frac{dV_{DS}}{dt} \tag{4.4}$$

This means that a rapid change in V_{DS} can inject a small displacement current into the gate loop, causing the measured V_{GS} disturbance. However, since the amplitude remains below threshold level of the GaN device, the disturbance does not cause false turn on. This is important because unintended enhancement during reverse polarity could create a reverse current path through the transistor channel.

Although the measured V_{GS} disturbance does not reach the threshold voltage in this text, it is important to reduce it because a floating gate gives a less defined off-state and reduces the design margin during reverse polarity.

To improve this condition, a 4.7 kΩ was inserted between gate and source. This resistor acts as a high-ohmic pull-down path that references the gate to the source when the driver is not actively controlling the device. The resistance value is high enough to avoid significantly loading the gate driver during normal operation but low enough to discharge coupled gate charge and pull V_{GS} back toward 0 V during blocking condition.

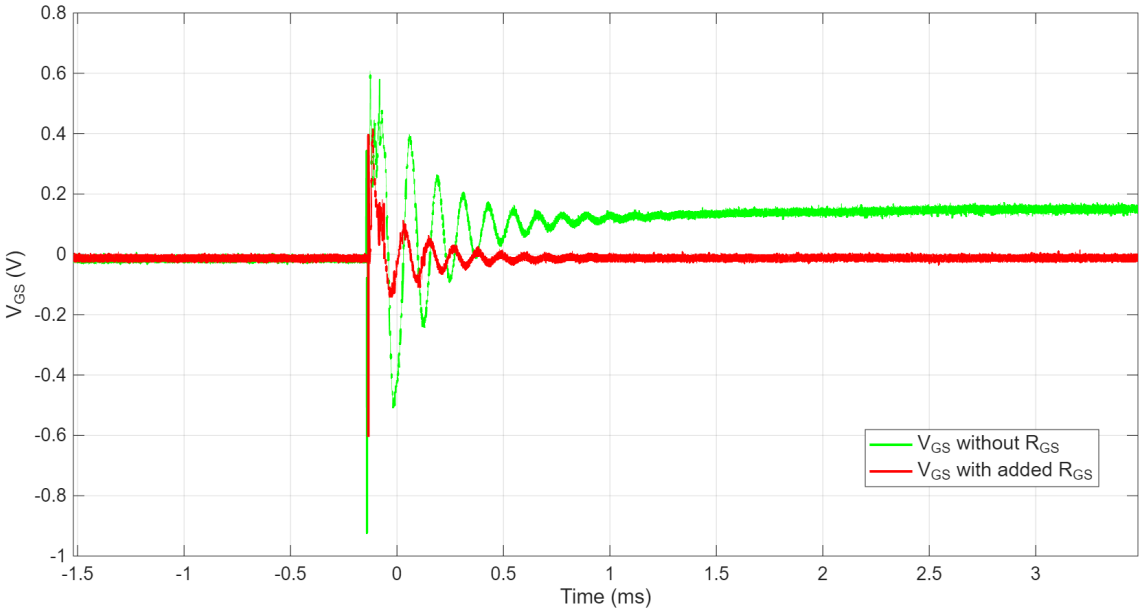

Figure 4.15: Comparison of V_{GS} with and without added R_{GS}.

As shown in 4.15, the waveform without R_{GS} shows a larger negative undershoot, a higher positive peak and more visible ringing after the transient. This indicates that the gate node is more sensitive to the coupled disturbance when it is left floating. With the added 4.7 kΩ, the oscillation is reduced and V_{GS} remains closer to 0 V. Although both waveforms remains below threshold voltage, the added resistor gives a more defined gate state and improves the safety margin against false turn-on during reverse polarity.

From a device level perspective, the result can be summarized by comparing the forward and reverse cases. In forward operation, V_{GS} rises to approximately 5 V, V_{DS} collapses close to 0 V and the device conducts the load current through its low $R_{DS(on)}$ channel. In the reverse polarity test, V_{GS} remains close to 0 V, V_{DS} remains high at 48-50 V and I_{in} decays to nearly 0 A. This is the opposite of forward conduction and confirms that the device remains in its blocking state.

4.2.4.2 Y-cable Simulation

In this Y-cable simulation test, the dynamic load is configured to produce a 10 A transient with a switching period of 30 ms, while the E-load connected at the EUT output is set to a continuous 1 A load. The measured waveforms obtained during the test include V_{in}, V_{GS}, I_{in}, and I_{load} shown in Figure 4.16.

Figure 4.16: Waveforms of V_{in} (Pink), V_{GS} (Yellow), I_{in} (Green), and I_{load} (Blue) of Y-cable simulation with 10 A dynamic load and 1 A EUT load current

Based on the experimental setup shown in 3.20, V_{in} represents the input voltage from the PSU, while PolGate or V_{GS} represents the gate-source voltage of the GaN FET within the EUT. I_{in} represents the current flowing from the EUT-side branch to the dynamic load branch, and I_{load} represents the total current flowing into the dynamic load, including contributions from both the PSU and the EUT-side load branch.

When the dynamic load is switched ON, I_{load} increases rapidly, causing a temporary voltage drop at V_{in}. Due to the presence of the 100 μH input inductance and parasitic impedance within the Y-cable configuration, the sudden increase in current demand generates transient voltage disturbances and ringing. At the same time, energy stored in the output-side filter capacitors and the EUT branch attempts to support the load transient. Consequently, current momentarily flows backward from the EUT-side branch toward the dynamic load branch, which is observed as an increase in I_{in}.

The reverse current detection circuit continuously monitors the sensed current through the sensing resistor. Once the detected reverse current exceeds the threshold level of approximately 0.7 A, the op-amp and comparator circuit rapidly pull down the gate voltage of the GaN FET. As a result, the GaN FET turns OFF and blocks the reverse-current path. The measured V_{GS} waveform shows that the GaN FET responds immediately to the reverse-current condition without noticeable false triggering, indicating stable operation of the control and protection circuit during transient load changes.

In addition, ringing and transient disturbances can be observed on V_{in} during the switching transitions. These oscillations are mainly caused by the interaction between the input inductance, parasitic impedance, and the capacitance of the additional filter circuit, which together form an LC resonant network. Although overshoot and undershoot are present, the voltage recovers shortly after each switching event and does not cause unwanted triggering of the protection circuit.

Overall, the Y-cable simulation confirms that the EUT can detect and block reverse current caused by current redistribution between parallel branches, while maintaining stable operation during transient load changes.

4.2.4.3 Short Circuit Interruption Response

To evaluate the behavior of the proposed GaN-based reverse polarity protection during an abrupt fault event, a short circuit interruption test was carried out using the power interrupt generator described in Section 3.3.5. As shown in Figure 4.17, the circuit operates in steady state before the fault is introduced, where the measured current is approximately 10 A, which is close to the rated current of the prototype. At t = 0, when the power interrupt generator applies the short-circuit condition, the current waveform exhibits a fast transient response. A short negative deviation is first observed, followed by a sharp current peak reaching approximately 70 A. This corresponds to about 7*$Irated$ indicating that the short-circuit event introduces a very high transient di/dt in the input path. After the peak, the current does not remain at the fault level but instead shows a damped oscillatory decay before gradually returning toward a lower steady-state level. This behavior indicates that the transient is strongly influenced by parasitic inductances and capacitances present in the switching loop, the cable path and the input of the EUT.

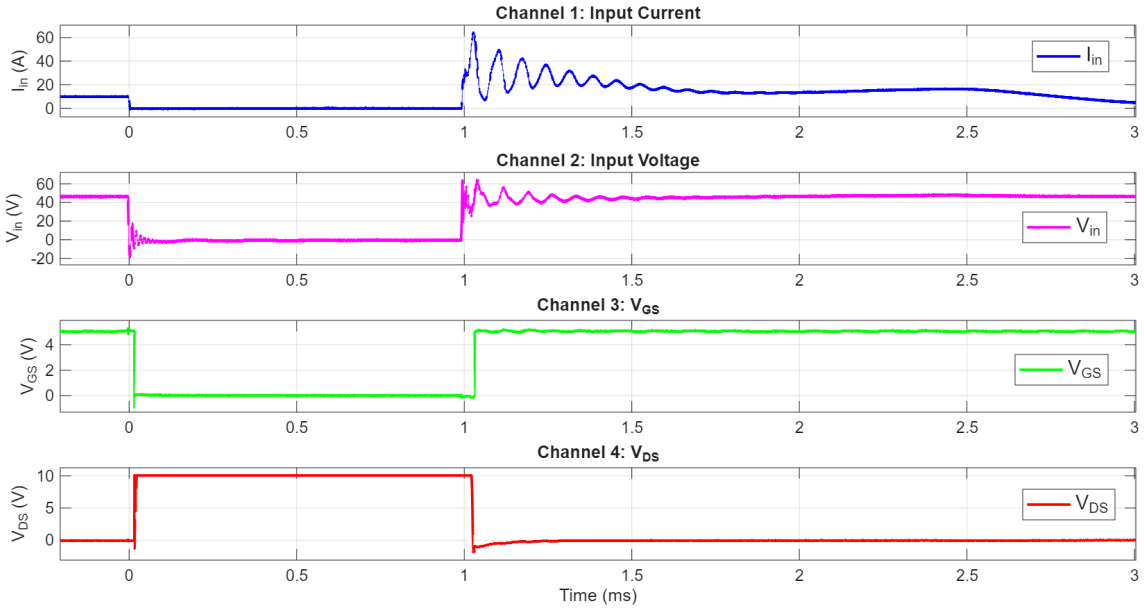

Figure 4.17: Measured polarity protection behavior during short circuit test.

The voltage waveform in Figure 4.17 also shows a clear disturbance at the moment of fault initiation. A temporary voltage dip is observed, followed by a limited overshoot and a short settling interval with small oscillations. This means that the short-circuit event causes a brief disturbance at the EUT input but that the voltage recovers relatively quickly. The fast recovery suggests that the reverse polarity protection inside the EUT responds rapidly and prevents the fault condition from causing a prolonged collapse of the input voltage.

The measured response also gives information about the dynamic behavior of the GaN switch in the protection stage. During normal forward operation, the GaN FET is in the enhanced state and behaves as a low-resistance conduction path. When the short-circuit condition is introduced, the protection circuit is exposed to a rapid change in both current and voltage. Due to the high switching speed of the GaN device, the protection stage can react quickly to the abnormal event and limit the duration of the electrical stress. At the same time, the fast switching transition of the GaN device produces high di/dt and dv/dt, which excites the parasitic elements in the hardware and results in the oscillatory behavior visible in the waveforms.

Overall, Figure 4.17 shows that the proposed GaN-based reverse polarity protection is capable of responding quickly during a short-circuit interruption event. At the EUT input, MOVs are incorporated to protect the circuit components from excessive voltage stress during the short-circuit transient. These MOVs act as voltage-clamping devices, limiting overvoltage and absorbing the surge energy generated during the fault condition, thereby mitigating the risk of damage to the circuit. Even though a high transient current peak is observed, the event is limited in duration and the voltage at the EUT input recovers rapidly.

4.2.5 Robustness

The robustness evaluation investigates the behavior of the GaN-based protection circuit under more demanding operating conditions than the nominal load case. High current and high slew rate tests were performed to assess the thermal margin, transient stability and practical operating limits of the prototype.

4.2.5.1 High Current Load Test

The high current load test was conducted to evaluate the thermal and transient load robustness of the prototype under overload conditions up to 19 A at 2 A/μs slew rate, which is the limitation of the E-load. The results at 19 A with a current slew rate of 2 A/μs are summarized in Table 4.10.

Table 4.10: Temperature observations at 19 A with a current slew rate of 2 A/μs

Test Condition	On/Off Time [s]	Duration [min]	Temp at R_{sense} [°C]	Temp at GaN FET [°C]	Observation
Continuous 19 A	–	1.5	80	57	No thermal equilibrium reached
Step load 0–19 A	0.1 / 0.1	10	63	54	Low heating, steady-state reached
Step load 0–19 A	3 / 3	10	72	57	Moderate heating, steady-state reached

The results in Table 4.10 show that both the temperature of R_{sense} and GaN FET increases noticeably. R_{sense} generates higher temperature than the GaN FET due to its higher power dissipation in the two-parallel GaN FET configuration.

During continuous operation at 19 A, R_{sense} reached a temperature of approximately 80°C after 1.5 minutes, while the GaN FET reached around 57 °C. The temperature continues to rise and does not reach thermal equilibrium within the observed time.

For step load conditions (0–19 A) with a rise and fall time of 0.01 ms and on- and off-times of 100 ms, the temperature remained lower than safe operating range over time. After approximately 10 minutes, R_{sense} stabilized around 63 °C, while the GaN device remained near 54 °C, same as after 5 minutes in Table 4.5. This is because of the rapid switching nature of the load, where the short duration at high current does not allow sufficient time for heat accumulation. Additionally, the fast transient may exceed the response capability of the power supply, so that it limits the delivered current and reducing thermal stress.

When the on and off time were increased to 3 seconds under the same step load amplitude, higher temperatures were observed. At 10 minutes, R_{sense} reached approximately 72 °C, while the GaN device stabilized near 57 °C. Unlike the continuous load case, both components appear to reach a steady-state condition without further significant temperature increase. This indicates that the longer on-time allows thermal accumulation, while the off-time still provides partial cooling, preventing temperatures from reaching the maximum observed under continuous operation.

4.2.5.2 High Slew Rate Test

Due to the limitation of the E-load, the minimum rise time and fall time can be set for step load test are 0.01 ms. The on-time and off-time were both set to 100 ms. Therefore, for a current step of 20 A, the maximum current slew rate (dI/dt) in this test is approximately 2 A/μs. The measured waveforms of I_{in}, V_{DS}, and V_{GS} of a two-parallel GaN FET configuration during turn-on and turn-off are shown in Figure 4.18 and 4.19, respectively.

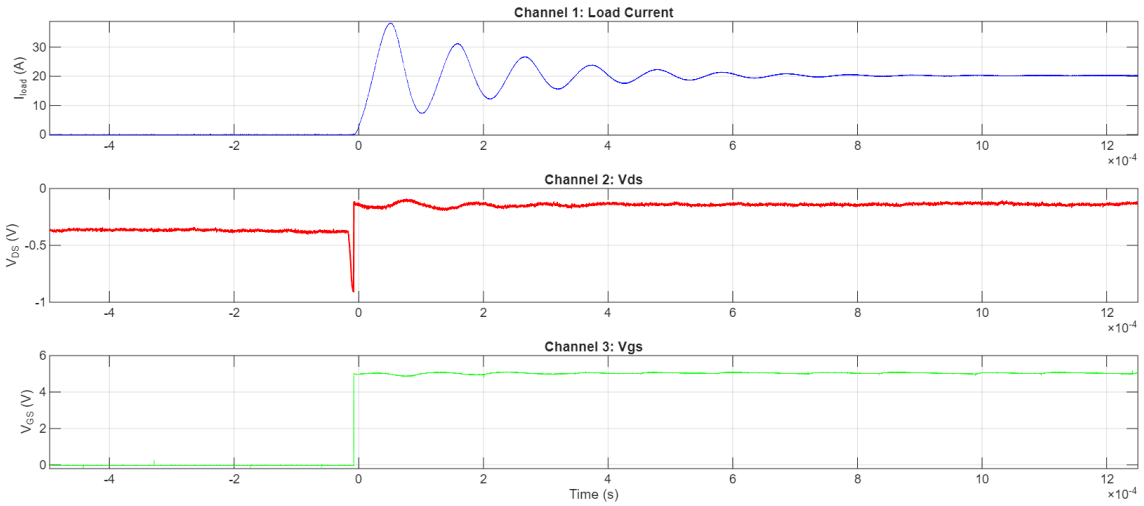

Figure 4.18: Measured waveforms of I_{in}, V_{DS}, and V_{GS} during turn-on of a two-parallel GaN FET configuration under a 20 A step-load condition with a current slew rate of approximately 2 A/μs.

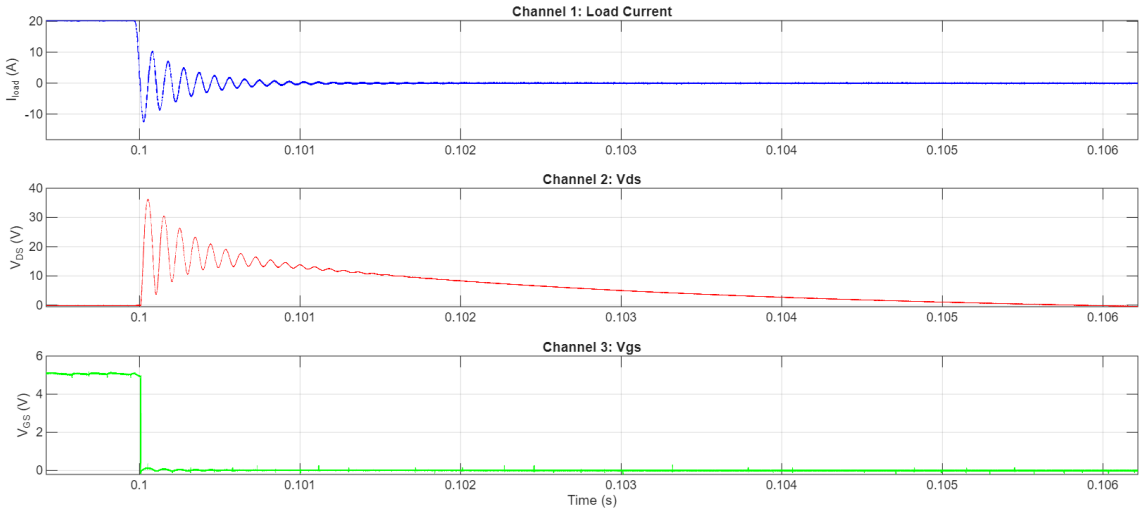

Figure 4.19: Measured waveforms of I_{in}, V_{DS}, and V_{GS} during turn-off of a two-parallel GaN FET configuration under a 20 A step-load condition with a current slew rate of approximately 2 A/μs.

As shown in Figure 4.18 and 4.19, the GaN FET operates normally during both turn-on and turn-off transitions, without false triggering or voltage overshoot exceeding the maximum values specified in the datasheet as shown in Table 3.1.

However, the slew rate available from the electronic load is insufficient to effectively evaluate the high-speed switching performance and associated ringing behavior of the GaN device. The rise and fall times configurable on the electronic load are significantly slower than typical GaN switching transitions, which often occur in the nanosecond range. Therefore, this test cannot be considered adequate for assessing high-slew-rate performance. A more suitable test setup or higher speed switching equipment is required for better evaluation.

4.2.6 Device Package Size

One of the objectives of this thesis is to reduce the size of the polarity protection circuit compared with conventional silicon-based protection solutions. The package dimension comparison between the currently used MOSFET and the selected GaN FET is presented in Table 4.11.

Table 4.11: Comparison of package dimensions of MOSFET and GaN FET

Device	Package	Dimensions $[mm \times mm]$	Footprint area $[mm^2]$
MOSFET	Power 56	5 × 6	30
GaN FET	PG-TSON-6	3 × 5	15

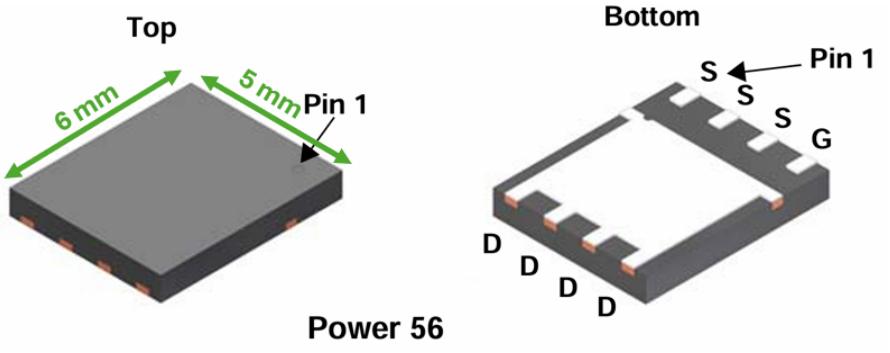

Figure 4.20: Package dimensions of the MOSFET in Power 56 package.

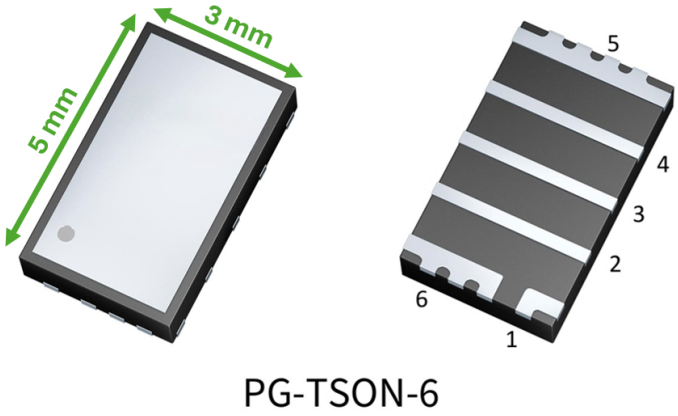

Figure 4.21: Package dimensions of the selected GaN FET in PG-TSON-6 package.

As shown in Table 4.11, the selected GaN FET in Figure 4.21 has a smaller package than the conventional MOSFET in Figure 4.20. The footprint area of the GaN FET is 15 mm^2, while the footprint area of the MOSFET is 30 mm^2, which is a 50% reduction in device footprint area. This reduction contributes to a more compact PCB layout, increases the available PCB space, and improves overall power density of the protection circuit.

In practical telecommunication applications, a smaller PCB can enable a more compact and lighter mechanical enclosure, resulting in easier transportation, installation, and maintenance. In addition, a smaller product can reduce overall system cost and shorten installation and maintenance time, since the equipment becomes easier to handle manually without requiring lifting equipment such as a crane. Therefore, replacing conventional MOSFET devices with GaN FET technology can significantly reduce the overall hardware size and enhance product competitiveness in the market.

5
Conclusion

5.1 Results from Present Work

This master thesis investigated the feasibility of using GaN FETs as the main protection device in a -48 V DC polarity protection circuit. The work included LTspice simulation, PCB implementation, and hardware validation of both single GaN FET and two-parallel GaN FET configurations. The results show that GaN FETs can provide correct forward conduction and reverse-current blocking in a -48 V DC system, while offering a more compact alternative to the conventional six-parallel silicon MOSFET solution.

The simulation results confirmed that the diode-based solution has the highest conduction loss. At 10 A, the simulated diode loss was 7.11 W, while the MOSFET and GaN FET losses were only 0.35 W and 0.33 W, respectively. This shows that an active transistor-based solution is much more suitable for high-current polarity protection than a passive diode. The simulation also showed that using two GaN FETs in parallel reduced the simulated loss by half, confirming the benefit of reducing the effective on-resistance through parallel operation. The hardware measurements verified the same trend. This confirms that paralleling GaN FETs improves conduction performance and current capability compared with a single-device implementation.

The gate resistance investigation showed that the GaN FET switching behavior is sensitive to the gate-drive design. $R_{g,on} = 47\ \Omega$ and $R_{g,off} = 10\ \Omega$ were selected as a suitable compromise between switching speed, damping, and false turn-on immunity. The results also showed that an external diode is required in the implemented circuit, since the GaN FET without the external diode produced a voltage drop of 0.832 V at only 0.2 A during reverse conduction. This would create unnecessary loss before the GaN FET fully turns on. The addition of $R_{GS} = 4.7\ k\Omega$ also improved the off-state behavior during reverse polarity by reducing the VGS oscillation and helped keep the gate voltage closer to 0 V

Thermal testing showed that the two-parallel GaN FET configuration provided better thermal behavior than the single GaN FET. Under 0-19 A step-load operation, the two-parallel GaN FET reached 54.3 °C, while the current sensing resistor reached 62.1 °C. This indicates that the GaN FETs were not the only thermal limitation of the prototype, the sensing resistor and PCB heat spreading also became important design constraints.

Compared with the six-parallel MOSFET reference, the two-parallel GaN FET showed an obvious advantage in size. The selected GaN FET package has a footprint area of 15 mm², while the MOSFET package has a footprint area of 30 mm². This corresponds to a 50% reduction in device footprint. However, at 19 A, the measured loss of the six-parallel MOSFET solution was 0.673 W, while the two-parallel GaN FET solution showed 0.790 W. This difference is mainly related to thermal dissipation, since the MOSFET used more devices, larger heat-spreading area, and more PCB layers, while the GaN prototype was implemented on a two-layer PCB. For the dynamic comparison, GaN FET provided much faster gate response, but this also resulted in higher V_{DS} overshoot and more pronounced ringing. In contrast, the MOSFET had a slower response, but showed a smoother and more damped transient behavior.

The real-application emulation tests confirmed that the protection circuit can respond to fault and transient conditions. During input supply reversal, the GaN FET remained in the blocking state and the current settled close to 0 A after the initial transient. In the Y-cable simulation, the circuit detected reverse current above approximately 0.7 A and turned off the GaN FET to block the unintended current path. During the short-circuit interruption test, the circuit experienced a transient current peak of approximately 70 A, but the peak was limited to a short transient interval and and the input voltage recovered rapidly. This means the disturbance was temporary and did not lead to sustained instability.

Overall, the present work demonstrates that GaN FETs are a feasible solution for -48 V DC polarity protection. The two-parallel GaN FET configuration is more suitable than the single GaN FET for high-current operation because it reduces conduction loss and improves thermal behavior. The main advantage of the GaN solution is its potential to reduce the required PCB area and component count in the protection stage. However, the results also show that the final performance depends strongly on PCB layout, thermal design, gate-drive tuning, and the external reverse-current path. Therefore, the GaN-based polarity protection circuit can be considered a successful proof of concept, but further optimization is required before it can fully replace the conventional silicon MOSFET solution in a real product.

5.2 Future Work

The present work has demonstrated that GaN FETs can be implemented as the main protection element in a -48 V DC polarity protection circuit. Through simulation and hardware testing, the prototype has verified the basic operating principle including forward conduction, reverse blocking behavior, transient response and thermal performance under selected load conditions. The results show that the GaN based solution can reduce component count and support compact implementation compared with conventional silicon based protection solutions. However, the results also indicate that there is potential for further improvement of the hardware design, especially regarding thermal performance, PCB implementation, component selection and validation under extended operating conditions.

Future work should therefore focus on developing the prototype from a functional proof of concept into a more product-oriented protection module. One important continuation is to evaluate GaN devices with lower $R_{DS(on)}$ and improved package level thermal performance. Since the circuit operates mainly in the enhanced state during normal forward operation, the dominant loss mechanism is conduction loss rather than repetitive switching loss. A lower $R_{DS(on)}$ would directly reduce the power dissipated in the device and would therefore reduce the temperature rise during continuous load operation. A GaN package with improved thermal connection to the PCB could also reduce local heat concentration, especially in the single device implementation where the current and heat are concentrated in one semiconductor.

Another important continuation is the redesign of the PCB. The present prototype was implemented on a two-layer board which is suitable for laboratory verification but limited for both a thermal and parasitic perspective. A future design should investigate a mulitlayer PCB with improved current return paths and better copper heat spreading around the GaN devices. Thermal management should also be developed further. The results indicate that the GaN solution can reduce component count and PCB area, but the heat is concentrated in fewer devices compared with a solution based on several parallel silicon MOSFETs. Future work should therefore investigate improved heat extraction from the GaN device to the PCB and surrounding mechanical structure. The aim should be to reduce maximum device temperature rather than only the average board temperature since localized hot spots can become a limiting factor for reliability even when the total power loss is relatively low.

A further improvement would be to include an MCU-based supervisory function. In the present design, the protection behavior is mainly determined by the analog sensing and comparator based circuitry. This provides a fast hardware response and a reliable logic control logic, but it limits the possibility to adapt the protection behavior to different operating conditions. An MCU could be used for monitoring, configurable thresholds, fault history and diagnostic logging. The main protection action should be hardware-based for fast response while the MCU would improve system-level control and make the circuit easier to integrate in a practical telecommunication power system. With these improvement, the GaN-based topology could become a realistic replacement for conventional silicon-based polarity protection in -48 V telecommunication applications.

5.3 Ethical and Sustainability Aspects

From ethical aspects, the design and testing results must be reported accurately, including both the advantages and limitations of using GaN FETs in polarity protection. The final design should be carefully validated to ensure reliability in the power system and safety for users.

The sustainability aspects can be viewed from ecological, economic and social per-

spectives. Ecologically, the GaN-based protection concept supports improved energy efficiency in telecom power systems by reducing conduction losses over the product lifetime. Its compact implementation improves material efficiency by reducing component count and PCB footprint, which can lower environmental impact.

Economically, the compact solution can contribute to lower lifecycle cost by reducing material usage and board area and production complexity. Improved thermal performance can support longer service life and lower maintenance demand. In telecom infrastructure, this creates long-term value by improving efficiency and reliability while reducing replacement needs.

Socially, reliable telecom power systems are important for maintaining digital connectivity, emergency communication and critical services. A robust reverse-current protection circuit reduces the risk of hardware damage during fault conditions, which supports system availability and helps prevent premature electronic waste.

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