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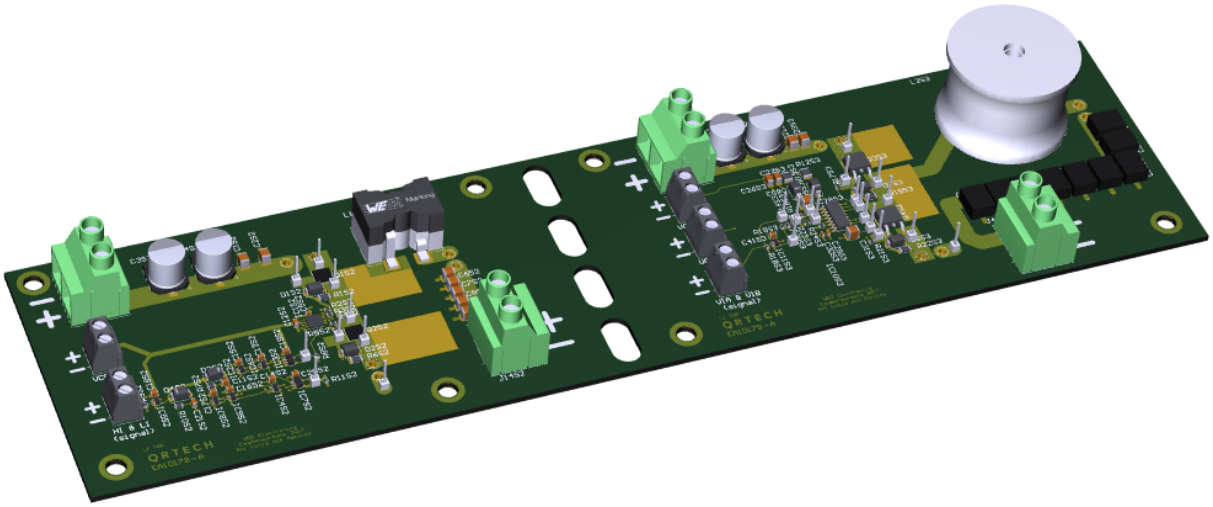

WBG Electronics for Energy-Efficient Power Electronic Applications

Master Thesis in Electric Power Engineering

LUCIA EL-ACHKAR
MATILDA HILDESSON

Department of Energy and Environment
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2017

Master Thesis 2017-06

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LUCIA EL -ACHKAR
MATILDA HILDESSON

Supervisor: Carl Petersson, Qrtech AB
Examiner: Torbjörn Thiringer, Energy and Environment

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Department Energy and Environment
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone: +46 31 772 1000

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MATILDA HILDESSON
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Abstract

An investigation between Wide Band Gap (WBG) transistors and silicon (Si) transistors were performed to investigate characteristics, materials, and best practice usage of different WBG transistors. The investigated WBG transistors were silicon carbide (SiC) and GaN transistors, but only GaN transistors were used as WBG transistors since the SiC transistors today are more applicable for high voltage applications. Two small compact dc/dc converters, with Si and gallium nitride (GaN) transistors respectively, were designed and constructed. The main purpose of the thesis was to investigate if WBG transistors had potential for future use in power electronic applications. The benefit of WBG transistors is that they can operate at higher switching frequencies and with lower switching losses compared to Si transistors. From the investigation of the WBG transistor it could be concluded that GaN transistors have a big potential. This is due to that GaN transistors can operate at higher switching frequencies and have smaller designs for almost the same efficiency as Si transistors.

Keywords: WBG transistors, dc/dc converter, integrated converter, gate driver, converter layout

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Lucia El-Achkar and Matilda Hildesson
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Introduction

1.1 Background

The increase of CO_2 emissions have led to climate changes such as melting glaciers, air pollution etc. These climate changes are a cause of growing concern, and therefore some changes need to be made in order to decrease the CO_2 emissions. There are many ways to decrease CO_2 emissions, one of these is to use electrified vehicles rather than Internal Combustion Engine (ICE) vehicles [1]. Electric vehicles can be divided into two categories: Electric Vehicles (EV) and Hybrid Electric Vehicles (HEV). The latter category can be further divided into four categories: full hybrid, mild hybrid, micro hybrid, and plug-in hybrid. An electric vehicle only contains an Electric Machine (EM), while a hybrid contains an ICE and an EM [2, 3]. The main components in a power train for electrified vehicles are ICE, battery, power electronics such as dc/dc converters, EM and inverter [4].

The demand for more compact and smaller electric devices increases in all technical areas. In the vehicle industry, the need for smaller, more efficient electric devices increases as the need for more electrified vehicles increases. If the components in the vehicle could be more compact and efficient, it would lead to less weight of the car, which in turn would lead to less energy for propulsion. If the vehicle need less energy for propulsion, the cost to operate an electric or hybrid vehicle will decrease. With more compact components in electric vehicles the use of materials for the manufacturing could reduce, and this could lead to a lower manufacturing cost. The lower cost of both manufacturing and driving an electric or hybrid vehicle could interest more people to switch from ICE vehicles to more sustainable options. If dc/dc converters could become more efficient and more compact, it would benefit many technical areas, for example the electric and hybrid vehicle industry. That is why it is important to investigate other types of semiconductors for converters.

Development of Si-based components have slowed, and today most improvements are only minor. Significant improvements on the already well-established, and well-researched, Si technology is unlikely to be made. In order to achieve significant improvements, other materials besides silicon can be used which have the same characteristics or better. One attractive alternative is the semiconductors with wider band gap. However, these semiconductors still need to be tested and evaluated. The

benefits of WBG components compared to Si are higher efficiency and breakdown voltages, lower switching losses, higher switching frequency, and higher temperatures [5, 6, 7]. Companies today strive to have more compact devices with higher efficiency, which reduces cost of materials and contributes to less losses in the application etc. One way to achieve this is by using semiconductors with a WBG. Using WBG semiconductors allow devices to operate at higher switching frequencies. With higher switching frequencies, lower inductance and capacitance values can be achieved, which result in smaller components and more compact devices. The most common WBG materials today are silicon carbide (SiC) and gallium nitride (GaN) [8].

1.2 Aim

The aim of this thesis is to investigate characteristics, materials, and best practice usage of different WBG transistors. Two small compact dc/dc converters will also be designed and constructed.

1.3 Task

The main task of this thesis was to design dc/dc converters with WBG transistors in order to decrease the size of the converters. The main challenges of the project were: constructing the converter in such a way that it utilized the potential of the new semiconductors, measurements of fast current/voltage changes, simulation of semiconductors and parasitic elements, and to compare the different types of semiconductors and evaluate the pros and cons. In order to achieve the aim of the thesis, three tasks were completed.

1. Effect and Selection of Semiconductor Materials

   The semiconductor materials that were studied in this master thesis were Si, SiC and GaN. The effect of these materials used in a dc/dc converter were simulated and evaluated in order to choose the most suitable semiconductor material for the switch in the dc/dc converter. The losses, efficiency, and ripple in the dc/dc converter was studied in LTSpice and MATLAB to determine the effects of the semiconductor material.

2. Effect of Parasitic Elements

   All the electric components contain one or several parasitic elements. Depending on the component, its specific parasitic element contributes to interference in the circuit. Not all the parasitic elements in the circuit affect the overall performance of the circuit; some of them can be neglected since they are small compared to the component's overall effect on the circuit. The parasitic ele-

ments in a circuit are parasitic resistance, parasitic capacitance and parasitic inductance [9]. A study of the effect of the parasitic elements in the circuit were performed and analyzed to investigate the performance of the converters.

3. Design, Test and Evaluation of dc/dc Converter

   The impact of the WBG transistors in the converters were studied and simulated. A comparison between the different transistor materials in regards to the requirements of the dc/dc converters were performed. The values of the inductor and capacitor used in the converters were calculated, and the converters were constructed and tested. Finally, with the results of the testing, the performance of the different transistor materials were compared in regards to efficiency, size, issues with interference etc.

1.4 Scope

The project describes WBG electronics for energy-efficient power electronic applications. The main focus for the project was to design a compact dc/dc converter, to investigate the characteristics of WBG transistors, and to find the best suitable material for the selected WBG transistor. Due to the time frame the focus was to design one dc/dc converter, however there were time to design two dc/dc converters. The requirements for the dc/dc converter are that the input voltage should be around 40 V, the input power should be between 100 W and 500 W and the output current should be between 9.6 A and 45 A in the converter. The semiconductor materials that were investigated and tested for the WBG transistor were Si, SiC and GaN. Study of the EMC performance of the converter to investigate whether the dc/dc converter is exposed to interference was not carried out. Only a literature study regarding EMC performance was done.

The project took into consideration sustainability and ethics of constructing the dc/dc converters. The sustainability aspect of constructing the dc/dc converters consist of investigating how the materials and the different components will affect the environment. The investigation took into account both the construction of the individual components, and the assembly of the converters. The ethical aspect of the dc/dc converters and the different semiconductor materials were handled by investigating and comparing the prototype constructions, and the operation to the IEEE code of ethics.

Limitations:
In the thesis, a regulator that automatically changes the duty cycle in order to get a voltage output between 9.6 V and 24 V was not considered, as it was too complex to cover sufficiently well in the scope of this master thesis. The duty cycle is changed manually in order to get an output voltage of 9.6 V. A gate driver for the gate of the transistors was not designed. Instead, a suitable gate driver was selected and purchased. Since there are several different molecule structures that are all referred

to as SiC, which have differently sized band gaps, only the three most common structures of SiC (3C-SiC, 4H-SiC, and 6H-SiC) were investigated.

1.4.1 Ethics

The ethic aspect of the dc/dc converter and the three different semiconductor materials are a comparison of the prototype constructions. Three relevant points to this project from the IEEE code of ethics are used and modified to fit our project.

1. *To be honest and realistic in stating claims or estimations based on the available data from the simulations and the prototypes*

   Before any claims about the designed converter could be made, it was essential to do some research in order to have facts that can back up the claims. To be honest about the results of the converters, to be clear on how it worked and which type of problems that was encountered were important. Because if the problems of the converters were not highlighted and only their benefits, it could lead to technical problems when they are being used. For instance if the converters have unmentioned problems and then sold for example to the car industry and then start to malfunction, it could in worst case scenario lead to a car crash with people getting injured. Therefore the importance of being honest and clear about the results of the project. It is also good to compare the simulation and the practical results as a way to validate the practical results. In order to claim that the prototypes have a good design, the simulation values were verified with analytical expressions. The components in the designs were selected in order to reduce the ripples, losses, and costs.

2. *Safety measures in the converter designs*

   Before the final prototypes were finished it was necessary to test and evaluate if the dc/dc converters were safe to use. The dc/dc converters were not considered every safety procedures such as to protect the human from example electric shock. The focus of the designs was to have a working converter with high efficiency and as compact as possible. It was not taken into account for example thermal protection and short-circuit protection. Those protection will be a subject for research in a future project.

3. *To improve the understanding of technology for the dc/dc converters and the different semiconductor materials*

   Before designing dc/dc converters, some research regarding the technology and the semiconductor materials needed to be done. After the basic research, the converters were being designed and tested. This was to test and observe how the different semiconductor materials behaved for different switching frequencies, change in input voltages, adding interference in the circuit etc. In this way a more understanding of the converters was achieved. Then it was easier

to know what to change in the converters in order to improve them. If an understanding of the technology on how dc/dc converters and how the different semiconductor material works are lacking, then a proper design can not be designed which can lead to several technical problems when operating the converters.

1.4.2 Sustainable Development

In today's society, the need of making changes for the climate change and resource depletion is high. One of the solution is electrified vehicles since the emission of carbon dioxide can be decreased which in turn will reduce the cost of fuel. The question is, are the electrification of the electric vehicles a sustainable option? In order for the electric vehicles to be a sustainable option is if the electrification comes from renewable sources. If the electricity does not comes from renewable sources, but from fossile fuels then the problem is still an issue even though the emission of carbon dioxide is reduced. In order to generate electromobility as a sustainable option, then the electric vehicles need to be charged from renewable sources. For this to be possible, the renewable sources need to be incorporated which leads to some modifications to the existing power grids need to be done [10, 11].

To get better and more efficient electrified vehicles all the parts in the power train need to be more efficient and if possible more compact to get lighter vehicles and/or more spaces for the passengers. The designed dc/dc converters in this thesis could be a suitable part of a power train in an electrified vehicle. However, in order to create more environmentally friendly transportation it is important to know that the vehicle itself is produced as sustainable as possible and not just that their propulsion is sustainable. Therefore, the sustainability aspect of the dc/dc converters needs to be investigated such as how the semiconductor materials and the different components affects the environment.

The availability of the raw materials of the three semiconductor materials is high and those are scattered all over the world. Si is the eight most common element in the universe and it could be found in the crust of the earth and in the hydrosphere [12]. SiC are composed of silicon and carbon atoms that form crystal structures. SiC are created in electric furnaces at a temperature around 2000-2 500°C through a reduction of quartz sand with excess coke [13]. GaN are composed of gallium and nitrogen atoms. Gallium is found in the crust of the earth and is spread out there[14]. Nitrogen is the sixth most common element in the universe and it can be found in atmosphere, hydrosphere, and in the crust of the earth [15].

The environmental impact of the raw materials of the transistors themself are not hazardous, but when combining with other elements to create new materials such as SiC and GaN it could cause some environmental impacts and also the process of extracting the raw materials could impact the environment. The production and usage of chemicals stand for up to approximately ten percent of the emission of the

green house gases. The main emission is carbon dioxide from the production of the chemicals. The need of new energy technologies are created due to today's climate problems and the increase of this new theologies can increase the usage and spread of toxic chemicals. However, by trying to fix one problem another problem can occur. Gallium is a component part of GaN that is used for the new transistor technology. Gallium itself is seen as a toxic element and is extracted in a harmful way for the environment [16]. Silicon affects the environment mostly when it is extracted from mining. Mining affects the environment with dust, large noises and emission both to the air and closed waters. The people working with silicon as a raw material both to extract it from the earth crust and to cutting the stones, are at risk of getting the lung disease Silicosis due to that they are exposed to silica dust [17, 18].

In order to make as sustainable converters as possible it is important that all the components are chosen carefully and not only their performance is checked, but also what type of material they are manufactured from. In February 2003 the European Commission legalized the RoHS Directive. The RoHS Directive stands for Restriction of Hazardous Substances in electronic and electrical equipments, which means that all products in EU need to pass the RoHS compliance. The Directive also requires that heavy metals such as lead or mercury for instance should be changed to an environmentally friendlier alternative instead [19].

When the dc/dc converters are used, their operation could be considered to be sustainable. However, the production of the electricity for the converters need to be considered in order to see if the operation is sustainable. If the electricity that is used to drive the voltage supplier of the converter is produced in a coal mine, then it will not be a sustainable operation.

2

Theory

In this chapter the theory about dc/dc converter, MOSFET, Semiconductors, WBG materials, parasitic elements, thermal analysis and EMC is presented.

2.1 dc/dc Converter

A dc/dc converter is as the name implies, a device that converts from one dc voltage level to another. It is mainly used within the power electronic area, such as dc motor drive applications. The common dc/dc converters are: buck (step-down) converter, boost (step-up) converter, buck-boost (step-down/step-up) converter, flyback converter, forward converter, and full-bridge converter. The focus in this thesis is the buck converter [20, 21].

The main purpose of a buck converter is to convert from a higher input dc voltage to a lower average output voltage. The purpose of the diode is to prevent the switch from absorbing the inductive energy created by the inductance and the stray inductance in the converter. Otherwise, the switch might break. After the switch and the diode, the converter is followed by a low-pass filter that contains an inductor and a capacitor in order to dampen the output voltage fluctuations. The value of the inductor and the capacitor has to be sufficiently large in order to have sufficiently constant inductor current and output voltage respectively. The buck converter is using pulse width modulation (PWM) for its operation. The main concept of PWM encompasses that a pulse voltage creates an average voltage. The average voltage depends of the duty cycle, in other words the ratio between the high and low time of the pulsed voltage. The output voltage of the buck converter can be controlled by varying the duty cycle of the converter [20, 21].

The size of the low-pass filter of the buck converter depends on the switching frequency. The filter size can be lowered when using a higher switching frequency. Besides the filter size, the switching frequency also depends on what type of semiconductor device is used as switch. The switching frequency affects the converter size, weight, efficiency and cost. The usual range of the switching frequency is usually above 100 kHz [20, 21]. The ideal circuit of the buck converter with MOSFET

as a switch and a gate driver for the MOSFET is shown in Figure 2.1.

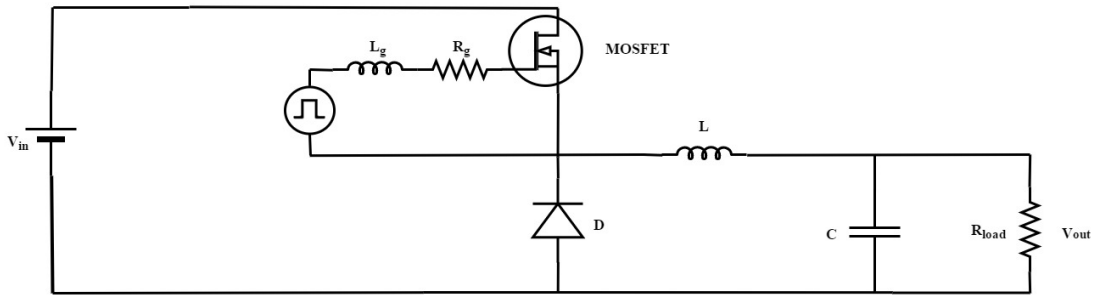

Figure 2.1: An ideal circuit of a buck converter with MOSFET as a switch

2.1.1 Parameter Calculations

The duty cycle for a buck converter can be expressed according to

$$D = \frac{U_o}{U_{in}}, \tag{2.1}$$

where U_{in} is the input voltage and U_o is the output voltage [20]. Using Ohm's law, the load can be calculated according to

$$R_{load} = \frac{U_o}{I_o}, \tag{2.2}$$

where I_o is the output current. The voltage across the inductor can be defined according to

$$u_L = L\frac{di_L}{dt}, \tag{2.3}$$

where L is the inductance and $\frac{di_L}{dt}$ is the rate of change of the current flowing through the inductor [20]. The value of the inductance can be calculated with the help of the on time during one switching period. This inductance value, combined with (2.3) can be used to transform the equation for the inductance to

$$L = \frac{u_L t_{on}}{\Delta i_L}, \tag{2.4}$$

where t_{on} is the on time [20]. The voltage ripple across the capacitor can be calculated according to

$$\Delta u_C = \frac{Q}{C}, \tag{2.5}$$

where Q is the charge of the capacitor seen in Figure 2.2 and gives the expression according to

$$Q = 0.5\,\frac{\Delta i_L}{2}\frac{T_{sw}}{2}, \tag{2.6}$$

where T_{sw} is the switching period [20]. Inserting (2.6) in (2.5) gives the value of the capacitance according to

$$C = \frac{\Delta i_L T_{sw}}{8\Delta u_C}, \tag{2.7}$$

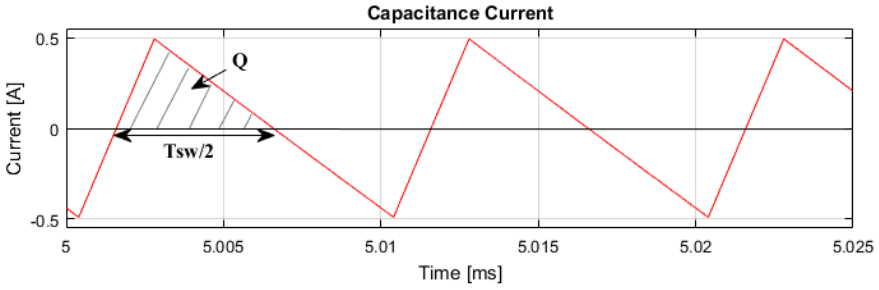

Figure 2.2: The current through the capacitor

2.2 MOSFET

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been available since early 1980s and is one of the most common transistors for switching electric signals. MOSFETs are appropriate for applications with high switching speed and are also used for both analog and digital circuits. MOSFET can be divided into two categories: N-type and P-type. This is because the polarity of the channels are different between the two types. The MOSFET has many advantages compared with the BJT and the thyristor and the advantages are high input resistance, low

drive power, and high switching speeds. Because of the higher switching speeds it performs well in high-frequency applications [20].

MOSFETs have three terminals: gate (G), source (S) and drain (D). The gate terminal is the input to the MOSFET, in which the current flows between the output terminals, source and drain. A MOSFET can be modeled from its equivalent circuits and are shown in Figure 2.3 and 2.4. The equivalent circuits give an understanding of the switching characteristics, the turn-off and turn-on characteristics, which are important to understand in order to design an appropriate gate drive for the MOSFET. In the equivalent circuits, the capacitance C_{ds} is not included since it does not psychically affect the waveforms or the switching characteristics. However, if a snubber was to be designed for the MOSFET it needs to be considered [20].

Figure 2.3 represents the MOSFET in the ohmic region and it enters the ohmic region when $V_{GS} \gg V_{GS_{(th)}}$. In the ohmic region the on-state resistance, $R_{DS_{(on)}}$ represents the ohmic losses that occur from the drain drift region. Figure 2.4 represents when the MOSFET is in the cutoff and active regions, where it contains a current source between drain and source. The current source is present because the drain current I_D is constant in the MOSFET's active region, and does not depend on V_{DS}. The current source is equal to $gm(V_{GS}$ - $V_{GS_{(th)}})$ in the active region and equal to zero when $V_{GS} < V_{GS_{(th)}}$.

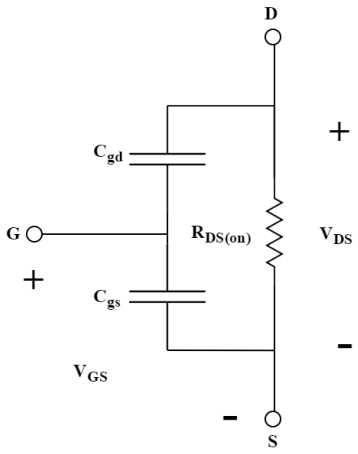

Figure 2.3: The equivalent circuit for the MOSFET in the ohmic region

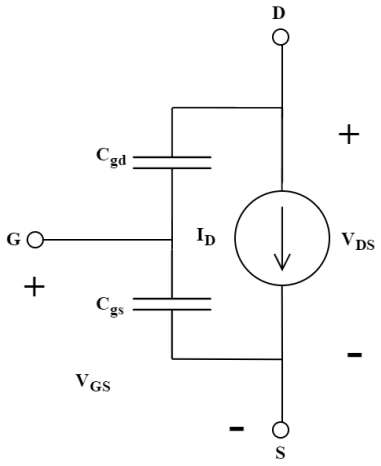

Figure 2.4: The equivalent circuit for the MOSFET in the cutoff and active regions

The internal capacitance value of the MOSFET model can be calculated from the values in the datasheet of the MOSFET, by using (2.8), (2.9) and (2.10)

$$C_{gd} = C_{rr}, \tag{2.8}$$

where C_{gd} is the gate-to-drain capacitance and C_{rss} is the reverse transfer capacitance [22]. The expression of C_{gs} can be determined as

$$C_{gs} = C_{iss} - C_{rss}, \tag{2.9}$$

where C_{gs} is the gate-to-source capacitance and C_{iss} is the input capacitance [22]. The expression of C_{ds} can be determined as

$$C_{ds} = C_{oss} - C_{rss}, \tag{2.10}$$

where C_{ds} is the drain-to-source capacitance and C_{oss} is the output capacitance [22].

2.3 Semiconductors

Semiconductors are materials that have a conductivity that lies in the interval between metals and insulators. Semiconductors can be divided into two types: single-element semiconductors and compound semiconductors. Single-element semiconductors are in group IV in the periodic table and examples of these are Si and SiC. The compound semiconductors are suitable for applications that involve light or for special electronic circuit applications. Compound semiconductors consist of combined elements from groups III and V or groups II and VI in the periodic table [23, 24].

The free-carrier density in a semiconductor can be changed due to an applied electric field. Where the electrical current in the material is a result of free charge carriers (often electrons) and an applied electric field. In order for the current to flow through the material, the free carriers need to be able to move in response to the electric field. The amount of free carriers varies depending on the material and if it is a metal, insulator or semiconductor. Semiconductors are seen as unique and useful materials for electrical applications because of their capacity to manipulate the free-carrier density [20].

Traditional semiconductor materials such as Si are limited in their operating temperature due to a low-energy barrier. The leakage current in Si devices increases when the temperature increases. Research in semiconductor materials has lead to progress in device design, fabrication and in semiconductor materials technology. These advancements are providing new solutions to the limitations of the traditional semiconductors. This has resulted in a development for semiconductor devices suitable for high power, high frequency and high temperature. Notable examples of these semiconductor materials are SiC and GaN, where the expectation of the devices are high reliability, smaller size and low cost [25].

2.3.1 Si

Si is the second-most abundant element on earth and in the hydrosphere, it is also the eighth most common element in the universe [12]. The first commercially available silicon transistor was produced in 1954 by Texas Instruments and it came quickly to dominate the new market. The silicon transistor would replace the vacuum tube in the power electronic area and due to the silicon transistor the technology developed and became more efficient with smaller sizes. Silicon was hard to work with because of its high melting temperature and reactivity compared to germanium. However, as a transistor material it provides major possibilities such as better performance in switching applications [26].

Gordon E. Moore, the research director at Fairchild Semiconductor Corporation made a prediction after observations and estimations in 1965 that transistors performance would double with a lowering cost every 18 months. This came to be called Moore's law. The reason for this exponential growth has turned out to be steadily shrinking size of transistors compared to its predecessor the vacuum tube [26]. New applications were made possible by using silicon, due to its many advantages relative its predecessor. Silicon was more reliable, easier to use and cost less [27]. Silicon transistors are the most common transistor today but the development of Si transistors has started to stagnate [26].

2.3.2 SiC

SiC is a semiconductor material that is composed of Si and carbon (C). There are three more common polytypes of SiC, which are 3C-SiC, 4H-SiC, and 6H-SiC. Because of the structure of the polytypes it gives the material different electrical characteristics. The characteristics can be observed in Table 2.1 [28, 25].

Table 2.1: Properties of SiC polytypes

Properties	**3C-SiC**	**4H-SiC**	**6H-SiC**
Energy gap : E_g [eV]	2.40	3.26	3.02
Electron mobility μ_e $[cm^2/Vs]$	800	1000	400
Hole mobility μ_h $[cm^2/Vs]$	40	115	101
Breakdown field : E_B $[MV/cm]$	2.12	2.2	2.5
Thermal Conductivity $[W/^\circ K - cm]$	4	4	4

Since the development of Si has stagnated, research in SiC material as substrate for transistors has been pursued for many years and now epitaxial SiC materials are available. SiC could be a possible successor of Si in order to develop high-power and high-frequency electronic applications. SiC has a breakdown field strength that is approximately ten times higher. This increase in breakdown field strength enables the applied voltage of SiC components to be ten times higher than comparable Si components. The advantages of SiC are low $R_{DS(on)}$, high voltage, fast switching

speed, suitable for high-radiation environments and that it can operate at higher temperatures [28, 25, 29].

2.3.3 GaN

GaN is a semiconductor material that could be a possible successor of Si. The first High Electron Mobility Transistor (HEMT) made of GaN appeared in 2004 with a radio frequency (RF) depletion-mode. GaN is suitable for use in semiconductor power devices, RF components and Light-Emitting Diodes (LEDs) [30, 27].

The capability to conduct electrons in GaN is more than 1000 times higher than for Si. A significant characteristic of semiconductor materials is the breakdown strength, which is ten times higher for GaN than for Si. This means that the applied voltage for GaN is ten times larger than for Si. The advantages of GaN as a semiconductor device are low $R_{DS(on)}$ (which result in low conduction losses), low cost, high switching speed (which result in lower switching losses), high current density, high operating strength, smaller size of the devices and lower internal capacitance (which results in lower losses in the device when charging and discharging) [30, 31, 32].

The usage of GaN in semiconductor devices, such as transistors, is still in the research stage and is not widely used in commercial products. This is due to little information about how GaN transistor works in practise and its disadvantages. However, the popularity of GaN transistors is growing. There are currently several manufacturers that produce GaN transistors, which will most likely lead to more commercially available products employing them in the near future.

2.4 WBG Materials

Semiconductors with wider band gaps have many benefits compared with the commonly used materials, silicon or other non-wide band gap materials. The development regarding WBG materials is new. Therefore, only a few companies develop these materials. The energy gap range for WBG materials is between 2 eV to 4 eV, while the regular materials (for example Si) have a band gap between 1 eV to 1.5 eV. The difference in band gap range for the WBG materials allows the components with these materials to have higher breakdown electric field. The common WBG materials are GaN and SiC. A comparison between SiC and Si shows that SiC has ten times higher breakdown electric field. Devices with WBG materials are more suitable for high-power and even high-temperature applications. Especially SiC since it allows higher current densities compared with the rest of the WBG materials. WBG materials can also operate at higher temperatures and switching frequency resulting in smaller components, lower costs and lower losses [7, 33]. A comparison of the properties of Si, SiC and GaN is presented in Table 2.2.

Table 2.2: Comparison of the semiconductors

Properties	**Silicon**	**3C-SiC**	**4H-SiC**	**6H-SiC**	**GaN**
Energy gap: E_g [eV]	1.12	2.4	3.26	3.02	3.4
Electron mobility μ_e $[cm^2/Vs]$	1400	800	1000	400	1400
Hole mobility μ_h $[cm^2/Vs]$	471	40	115	101	<20
Breakdown field: E_B $[MV/cm]$	0.25	2.12	2.2	2.5	3.5
Thermal Conductivity $[W/^\circ K - cm, atK = 300]$	1.5	4	4	4	2.3

WBG power electronics have many benefits within many applications, such as higher efficiency, higher breakdown voltages, higher switching frequency, higher temperatures and lower switching losses. Even though the WBG materials have many benefits, there are some disadvantages, and one of them is the high cost, since it is a new technology. Because of these disadvantages, there are only a few manufacturers that produce components in these materials. A byproduct of this is that there are only a few components out on the market made by these materials, compared with silicon [7, 33].

2.5 Parasitic Elements

Parasitic elements contributes to interference in an electric circuit. Depending on which component it is, the parasitic element has a certain interference in the overall performance of the circuit. The effect of some of the parasitic elements can be neglected since they are small compared to the components' effect in the overall performance [9]. The focus in this thesis are parasitic resistance, parasitic capacitance, and parasitic inductance.

Parasitic resistance exist either in series or in parallel with inductances, capacitances and the tracks on the printed circuit board (PCB). The overall effect on the performance in a circuit with the parasitic resistance is negligible, since compared with the effect of the impedance, it is higher. The parasitic inductance can be divided into two parts, self inductance and mutual inductance. The parasitic inductance occurs when current flows through a conductor, which creates a magnetic field around it. The two parts of the parasitic inductance are proportional, because when one of them is reduced then the other one is also reduced. The effect of the parasitic inductance can cause unwanted energy exchange between the two circuits, which in turn affect the overall performance of the circuit. The effect of parasitic capacitances increases when the frequency in the circuit increases, since the capacitor is inverse proportional to the frequency. This can be obtained in (2.7) and the overall performance of the circuit is affected because it couples interference in the circuit. Then the efficiency of the circuit is reduced because of the interference and the losses that occurs [9].

2.5.1 Parasitic Elements Calculations

In Figure 4.13 the buck converter with parasitic elements and with two MOSFETs is presented.

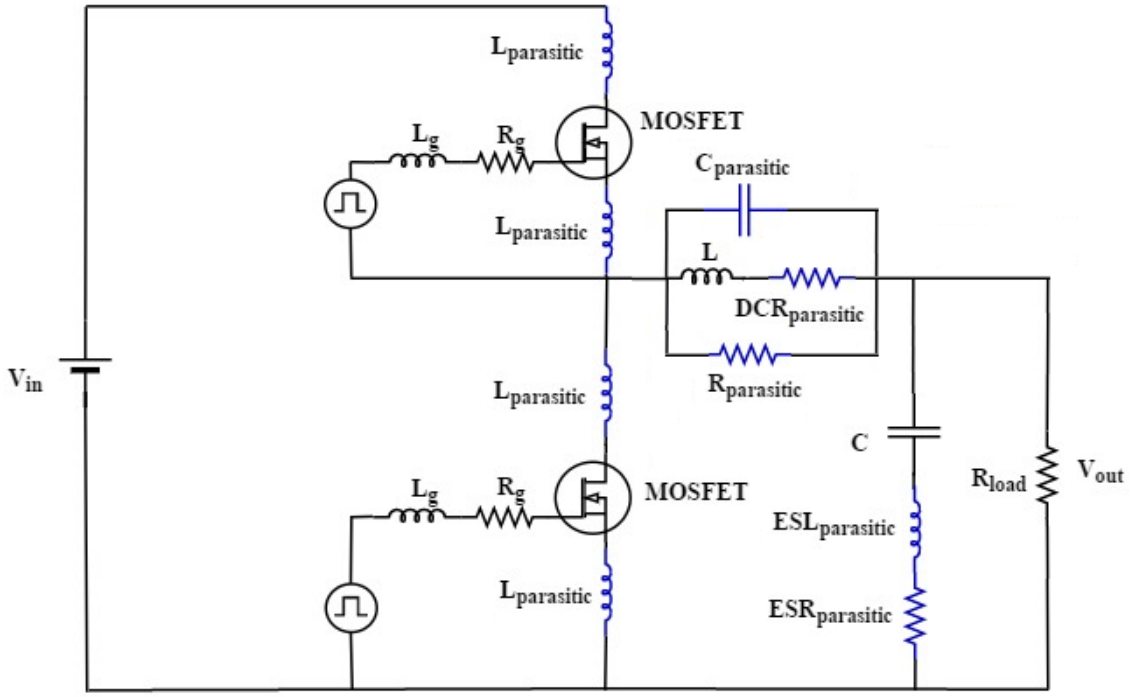

Figure 2.5: Buck converter with parasitic elements and MOSFET as switch

The parasitic elements in the MOSFET are given in its the data sheet. The self-resonant frequency can be expressed according to

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{LC}}, \tag{2.11}$$

where ω_o is the self-resonant frequency in rad/s, L is the inductance value at a certain switching frequency and C is the parasitic capacitance of the inductor [20]. Transforming (2.11), the parasitic capacitance can be calculated according to

$$C = \frac{1}{(2\pi f_o)^2 L}, \tag{2.12}$$

The iron resistance of the inductor can be calculated according to

$$R_{fe} = \frac{U_{fe}^2}{P_{fe}} = \frac{U_{L,rms}^2}{P_{fe}}, \tag{2.13}$$

where P_{fe} is the iron losses in the core and U_{fe} is the voltage across the parasitic resistance and it is the same as the rms value of the voltage across the inductor [34]. The iron losses in the core in W of the parasitic resistance can be calculated according to

$$P_{fe} = P_V V, \tag{2.14}$$

where P_V is the iron losses in the core in $\mathrm{W/m^3}$ and V is the volume of the inductor. In order to get the value of P_V from a figure in data sheet, the magnetic flux needs to be calculated and it is achieved according to

$$B = \frac{Li}{NA_e}, \tag{2.15}$$

where N is the number of turns in the inductor, i is the current ripple in the inductor and A_e is the effective magnetic cross section [20]. The number of turns in the inductor needed in order to achieve the inductance value can be calculated according to

$$L = N^2 A_L, \tag{2.16}$$

where A_L is the inductance factor [20]. The expression of the parasitic resistance in the capacitor with the help of Figure 2.6 is expressed according to

$$ESR = tan(\delta)\ \frac{1}{\omega C}, \tag{2.17}$$

where $tan(\delta)$ is the dissipation factor, C is the capacitance at a certain switching frequency and ω is the angular frequency [35].

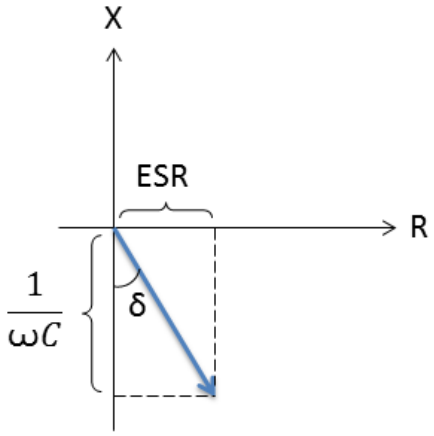

Figure 2.6: The vector of the capacitive load

2.6 Thermal Analysis

The thermal analysis in this project consist of loss calculation of the converter and the thermal model of the MOSFET. The losses in the converter are calculated and estimated through analytical methods. The thermal model of the MOSFET is studied to understand how the junction temperature affects the losses in the converter.

2.6.1 Loss Calculations

The voltage drop over the inductor's resistive part can be expressed according to

$$u_{L,drop} = R_L i_L, \tag{2.18}$$

where R_L is the internal series resistance of the inductor and i_L is the current of the inductor [20]. The conduction losses of the inductor can be calculated according to

$$P_{L,cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_L u_{L,drop}\, dt = \frac{R_L}{T_{sw}} \int_0^{T_{sw}} i_L^2\, dt = R_L I_{L,rms}^2, \tag{2.19}$$

where $I_{L,rms}$ is the average rms current of the inductor and can be calculated according to

$$I_{L,rms} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i_L^2 \, dt}$$

$$= \sqrt{\frac{1}{T_{sw}} (\frac{DT_{sw}}{DT_{sw}} \int_0^{DT_{sw}} i_L^2 \, dt + \frac{T_{sw} - DT_{sw}}{T_{sw} - DT_{sw}} \int_{DT_{sw}}^{T_{sw}} i_L^2 \, dt)} \tag{2.20}$$

$$= \sqrt{\frac{D}{6}((I_L - \frac{\Delta i_L}{2})^2 + 4I_L^2 + (I_L + \frac{\Delta i_L}{2})^2) + \frac{1-D}{6}((I_L + \frac{\Delta i_L}{2})^2 + 4I_L^2 + (I_L - \frac{\Delta i_L}{2})^2)},$$

where I_L is the average inductor current [20]. With the help of (2.13), the magnetization losses of the inductor can be rewritten according to

$$P_M = \frac{U_{L,rms}^2}{R_{fe}}, \tag{2.21}$$

The total losses for the inductor can be calculated according to

$$P_{L,tot} = P_M + P_{L,cond} \tag{2.22}$$

In order to calculate the total losses of the MOSFET, the losses can be divided in two parts: conduction losses and switching losses [20]. The total losses of the MOSFET can be expressed according to

$$P_{MOSFET} = P_{sw} + P_c, \tag{2.23}$$

where P_{sw} is the switching losses and P_c is the conduction losses [20]. The switching losses can be calculated according to

$$P_{sw} = (W_{sw(on)} + W_{sw(off)}) f_{sw}, \tag{2.24}$$

where $W_{sw(on)}$ and $W_{sw(off)}$ are the energy dissipated during on and off time of the switching event [20]. This can be calculated according to

$$W_{sw(on)} = \frac{u_{MOSFET} i_{MOSFET}}{2} \, t_{rise}, \tag{2.25}$$

$$W_{sw(off)} = \frac{u_{MOSFET} i_{MOSFET}}{2} t_{fall}, \tag{2.26}$$

where u_{MOSFET} is the peak value of the square wave voltage pulse, i_{MOSFET} the peak value of the square wave current pulse with the ripple, t_{rise} and t_{fall} is the rise time and the fall time respectively [20]. The conduction losses can be calculated according to

$$P_c = R_{DS(on)} I^2_{MOSFET,rms}, \tag{2.27}$$

where $R_{DS(on)}$ is the static drain-to-source on-resistance and $I_{MOSFET,rms}$ is the rms current of the MOSFET [20]. This can be calculated according to

$$I_{MOSFET,rms} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i^2_{MOSFET}\, dt} = \sqrt{\frac{D}{6}((I_L - \frac{\Delta i_L}{2})^2 + 4I_L^2 + (I_L + \frac{\Delta i_L}{2})^2)}, \tag{2.28}$$

where i_{MOSFET} is the current through the MOSFET [20]. The total losses over the MOSFET can also be calculated according to

$$P_{MOSFET,tot} = U_{MOSFET,avg} I_{MOSFET,avg} \tag{2.29}$$

The total losses over the diode when one switch and one diode are used in a buck converter can be calculated according to

$$P_{Diode,tot} = U_{diode,avg} I_{diode,avg} \tag{2.30}$$

where $U_{diode,avg}$ is the average voltage over the diode and $I_{diode,avg}$ is the average current through the diode. The losses of the capacitor can be expressed according to

$$P_{C,loss} = ESR I^2_{C,rms}, \tag{2.31}$$

where $I_{C,rms}$ is the rms current in the capacitor [20]. The rms current can be calculated according to

$$I_{C,rms} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i_C^2 \, dt}$$

$$= \sqrt{\frac{1}{T_{sw}} (\frac{DT_{sw}}{DT_{sw}} \int_0^{DT_{sw}} i_C^2 \, dt + \frac{T_{sw} - DT_{sw}}{T_{sw} - DT_{sw}} \int_{DT_{sw}}^{T_{sw}} i_C^2 \, dt)} \tag{2.32}$$

$$= \sqrt{\frac{D}{6}((-\frac{\Delta i_C}{2})^2 + (\frac{\Delta i_C}{2})^2) + \frac{1-D}{6}((\frac{\Delta i_C}{2})^2 + (-\frac{\Delta i_C}{2})^2)} \quad = \sqrt{\frac{D}{6}(\frac{\Delta i_C^2}{2}) + \frac{1-D}{6}(\frac{\Delta i_C^2}{2})},$$

In order to study if the converter has a good performance with small losses, the efficiency of the converter needs to be calculated and can be according to

$$\eta = \frac{E_{out}}{E_{in}}, \tag{2.33}$$

where E_{out} and E_{in} is the energy out from and in to the converter respectively and can be calculated according to

$$E = \int_0^t v \, i \, dt, \tag{2.34}$$

where v and i is the voltage and current in to and out from the converter respectively depending if the calculation of the energy is in or out and t is the simulation time [20]. When a component is applied with a dc voltage and dc current both its internal resistance and its total losses can be calculated according to

$$P_{tot} = U_{dc} \, I_{dc} \tag{2.35}$$

$$R_{internal} = \frac{U_{dc}}{I_{dc}} \tag{2.36}$$

2.6.2 Thermal Model

The transient thermal response of power devices could lead to a instantaneous dissipation that may exceed the average power rating of the device. The transient

thermal response is originated during transient overloads or at power-up or power-down of a systems with power devices. If the junction temperature exceeds the maximum permitted value or not, depends on the power surges magnitude and duration but also of the thermal properties of the device. Figure 2.7 shows a thermal model of a power device where C_s is the heat capacity, R_t is the thermal resistance, $T_j(t)$ junction temperature, T_a is the ambient temperature, and $P(t)$ is the input power. Both the junction temperature and the input power depends on the time [20].

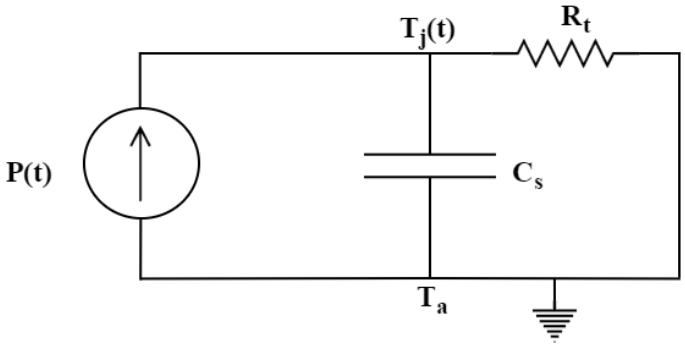

Figure 2.7: A general thermal model

The thermal resistance, R_t is defined according to

$$R_t = \frac{\Delta T}{P_{cond}}, \tag{2.37}$$

where ΔT is the temperature difference from the inside of the device to its surface [20]. The heat usually needs to flow through several different materials with different thermal conductivity. The total thermal resistance from junction to ambient can be calculated according to

$$R_{\theta ja} = R_{\theta jc} + R_{\theta cs} + R_{\theta sa}, \tag{2.38}$$

where $R_{\theta jc}$ is the juction to case resistance, $R_{\theta cs}$ is the case to sink resistance and $R_{\theta sa}$ is the sink to ambient resistance [20]. The junction temperature of the thermal model can be calculated according to

$$T_j = P_d(R_{\theta jc} + R_{\theta cs} + R_{\theta sa}) + T_a, \tag{2.39}$$

where P_d is the power dissipation [20]. The heat capacity of the sample from the thermal model is calculated according to

$$C_s = C_v A d, \tag{2.40}$$

where A is the cross section area of a rectangular block of material, d is the thickness and C_v is the heat capacity per unit volume [20]. The heat capacity can be calculated according to

$$C_v = \frac{dQ}{dT}, \tag{2.41}$$

where dQ is the change of the heat energy density Q and dT is the material temperature [20].

2.7 EMC

An interference between electric devices occur when they are connected to each other or closed. Electromagnetic Interference (EMI) is a result of unwanted higher harmonics in currents, voltages, or both. There are combinations of three factors that are the reasons that EMI occurs and these are: source, transmission path, and response. Where at least one of these factors is unplanned. Too much EMI can affect the functionality of devices in the environment negatively, which is undesired [36].

EMC is when the device behaves acceptably in the EMI environment, and at the same time does not generate too much EMI for other devices to function properly in near proximity to it. According to the European Commissions EMC directive, all electric devices need to be designed such that they are not generating, nor affected by the electromagnetic disturbances [36, 37].

Digital components that are located on a PCB assembly generates EMI. This EMI can take the shape of conducted voltages/currents, or as electromagnetic fields. Analog components are especially sensitive to exposure to radiated or conducted EMI. When designing a PCB there is a risk to not achieve the demand of the EMC compliance, and that the system causes harmful interference to both the outside environment, circuits and components in close proximity through the process of crosstalk. (Put simply, crosstalk can be regarded as interference at a localized level.) To counteract these risks, three areas are important to pay close attention to [38]:

- Routing transmission lines based on design requirements.
- Distributing power optimally to all components. This minimizes voltage fluctuations in both the power and ground planes.

- Referencing signals to power and ground planes properly.

3

Procedure

In this chapter the methods used in this project and the case set-up of the experiment are presented.

3.1 Method

1. A literature review was performed on WBG electronics where different transistor types were compared. From the literature study and the restriction of the dc/dc converters, a suitable transistor type was chosen. Three semiconductor materials - Si, SiC, and GaN - were studied and evaluated for the chosen WBG transistor.

2. The losses, efficiency, parasitic elements, and the size of the components of the converters were estimated and calculated through simulations of the dc/dc converter. The ripple and frequency range of the converters were studied by simulations. The simulations are done by using LTSpice and MATLAB. The complete converter layouts were modelled in Altium Designer.

3. Selection of materials and components, and constructing a suitable design of the converters. Testing and evaluating the converters and the different WBG transistor materials were done.

4. Analysis, design, and results of the dc/dc converters and the different WBG transistors were documented in a report.

3.2 Case set-up

The project specified some restrictions for the buck converters. These specifications can be seen in Table 3.1.

Table 3.1: Specifications for the buck converter

Specifications	
P_{in} [W]	100
V_{in} [V]	40
V_{out} [V]	9.6
I_{out} [A]	9.6
$f_{sw_{500}}$ [kHz]	500
$f_{sw_{200}}$ [kHz]	200

In order to test and evaluate the different WBG transistors, measurement equipments were used. The measuring devices that were used in this project are presented in Table 3.2.

Table 3.2: Measurement equipment used in this project

Instrument	**Name**
Multimeter	FLUKE 115
Function generator	AFG-2105
Power supply	EA-PS-2042-06B
Oscilloscope	DSO-X2014A
Current probe DC	N25783B
Current probe AC	CWT 015B ultramini
Isolation transformer	PFM 600
Heat camera	FLIR I50
Thermometer	TM-947SD
Differential probe	MX9030

The transistors that were tested, compared to each other, and used to evaluated the WBG transistors performance in this project are presented in Table 3.3.

Table 3.3: The used transistors in this project

Semiconductor	**Name**	**Manufacturer**	**Voltage rating [V]**	**Current rating [A]**
Si	STD47N10F7AG	STMicroelectronics	100	45
GaN	GS61004B	GaN systems	100	45

4

Simulations

In this chapter the simulation models of the two buck converters and their components are presented. Both a simplified simulation model and a model with parasitic elements were designed to evaluate how the different WBG materials would effect the converters efficiency. The simulation models were furthermore used as a tool to distinguish how the different waveforms would look like. They were also used as a benchmark for the practical design. The simulated WBG materials were Si and GaN only. SiC was not simulated or investigated more than a literature study which was presented in Subsection 2.3.2. The reason for that is because it is manufactured for high voltage applications and this project is targeting low voltage applications [39]. The chosen switching frequencies for each switch were 200 kHz for Si and 500 kHz for GaN. This is due to the limited time for the project and also, it is more interesting to simulate at higher switching frequencies. The reason GaN switchs were simulated at the higher switching frequency is because it is a WBG material and can operate at higher switching frequencies. This is mentioned in Subsection 2.3.3.

4.1 Circuit Simulations

At first, an initial simplified simulation model of the two buck converters was created. This simplified model uses a buck converter with a switch and a diode, it can be seen in Figure 2.1. Another simplified simulation model that uses a buck converter with two switches instead was constructed and is illustrated in Figure 4.1. In Table 4.1 the values for the diode and the switches are presented.

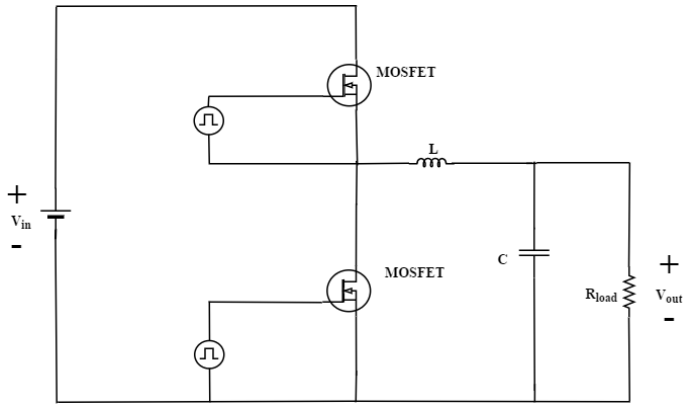

Figure 4.1: Model of the simplified buck converter with two switches

Table 4.1: Values for the diode and the switch in the simplified model

Parameters	**Values**
Diode resistance: R_{on} [Ω]	0.001
Forward voltage of the diode V_f [V]	0.8
MOSFET resistance R_{on} [Ω]	0.02
Body diode resistance in MOSFET R_d [A]	0.01

The value for the switches in the simplified models was chosen to be similar to the value of the actual switch in the practical design according to Appendix C and Appendix D. The diode value was chosen so that it would have a realistic forward voltage but with no slope due to the low R_{on} value. This is since the simplified models should be similar to an ideal model. The efficiency for the simplified models were calculated according to (2.33). The total diode losses were calculated using (2.30 and the total MOSFET losses were calculated according to (2.29). A comparison of the different efficiency for the two simulation models is shown in Table 4.2. It is clear that the two switches in a buck converter is a better option since it will decrease the losses and increase the efficiency in the converter. This is due to that a diode has a larger voltage drop. In the practical design, a buck converter with two switches was therefore used.

Table 4.2: Comparison of the simulation models

Parameters	**Switch & diode**	**Two switches**
Efficiency for 200kHz: η_{200} [%]	94.024	99.9
Efficiency for 500kHz: η_{500} [%]	94.026	99.9
$P_{diode_{500}}$ [W]	7.76	-
$P_{diode_{200}}$ [W]	7.76	-
$P_{Switch_{500}}$ [W]	0.33	0.77
$P_{Switch_{200}}$ [W]	0.33	0.77

The component sizes for the converters could be calculated by taking into account

the specifications of the project, which is presented in Table 3.1. Since the aim of the project was to design a compact dc/dc converter it resulted in that the size of the components, especially the inductor, should be as small as possible. In order to achieve a small value of the inductor, the chosen ripple of the i_L was 10 % since the inductance decreases with higher ripple according to (2.4). However, higher current ripple results in larger losses according to (2.20) and it is therefore necessary to take that into consideration and not just focus on the size of the inductance. The voltage ripple of the conductor, ΔVc, should be small in order to get as close to a pure dc voltage as possible. However, with higher voltage ripple the capacitance increases according to (2.7). The chosen value for ΔVc was 0.05 %. The value of the capacitor and the inductor was calculated using (2.7) and (2.4), the values for the different frequencies is presented in Table 4.3. The load was calculated to 1 Ω using Ohm's law in (2.2) with a V_{out} equal to 9.6 V and I_{out} equal to 9.6 A.

Table 4.3: Values for the capacitance and inductance

Parameters	**Values**
C_{200} [μF]	116.60
C_{500} [μF]	46.64
L_{200} [μH]	40.74
L_{500} [μH]	16.29

The type of switch chosen in this project was a MOSFET. When deciding which type of switch to use it is important to consider its operating range for voltage, current and frequency. In Figure 4.2 a comparison of the most common switches today and their ranges are presented. The frequency interval for this project was 100 kHz to 500 kHz and, as can be seen in the figure, only the MOSFET can operate at such high frequencies.

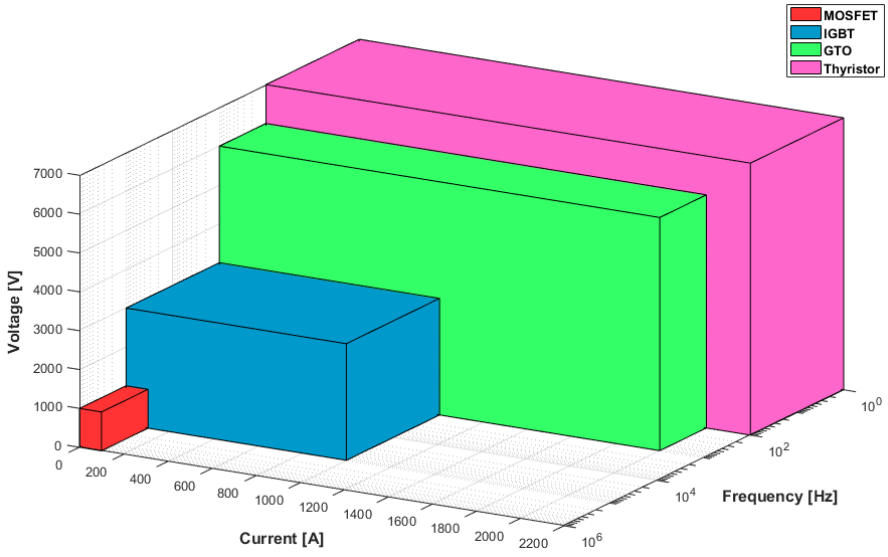

Figure 4.2: Comparison of different type of switches

4.1.1 Simulation of the Simplified Model with two Switches

The simplified simulation model, with two switches, is simulated for the frequencies at 200 kHz and 500 kHz. This is since these frequencies is where both the extended simulations model and the actually design is operated at. The model is simulated with a load of 1.072 Ω which is the value of the actual load that was used in the practical design. The input voltage and current for the model is presented in Figure 4.3 and 4.4.

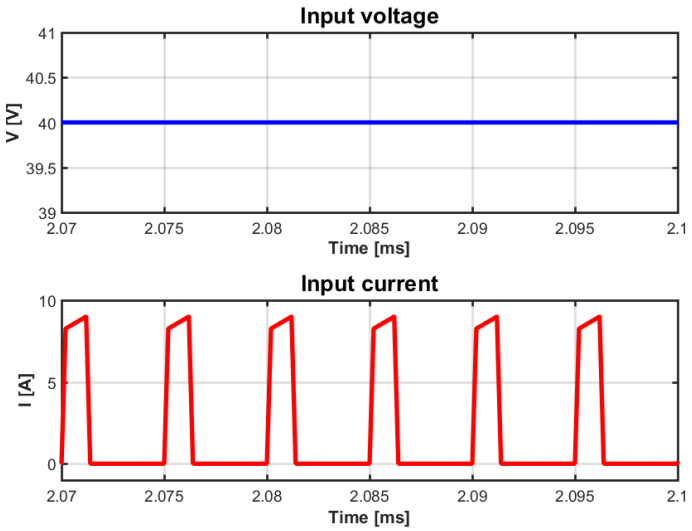

Figure 4.3: Input voltage and current for f_{sw}=200 kHz

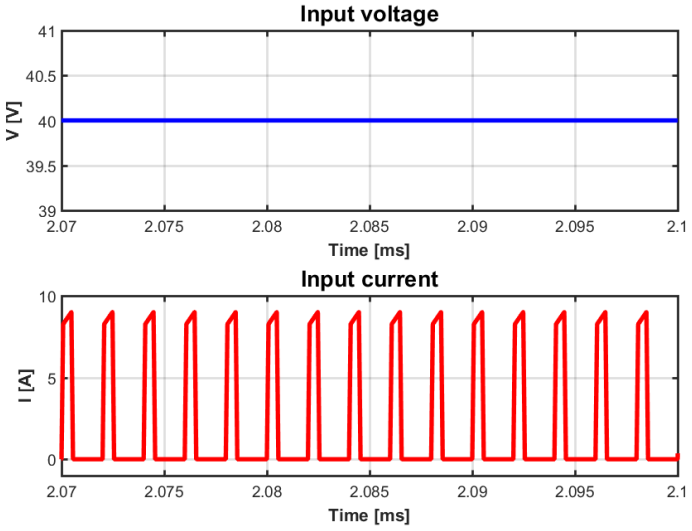

Figure 4.4: Input voltage and current for f_{sw}=500 kHz

As can be seen from these figures, the value of the input voltage is 40 V which is the same as the specification for the project. The input current is not a dc current, which it is in the practical design. The reason for the behaviour of the input current

waveform is because it is affected by the upper MOSFET in the circuit. When the upper MOSFET is turned off the current only flows through the LCR circuit, which makes the input current zero at the same time. The difference between Figure 4.3 and 4.4 is the difference in switch frequency. With f_{sw} at 500kHz, it has a smaller period time than for f_{sw} at 200kHz. The voltage over drain to source of both MOSFETs and the current through drain to source of both MOSFETs is shown in Figure 4.5 and 4.6.

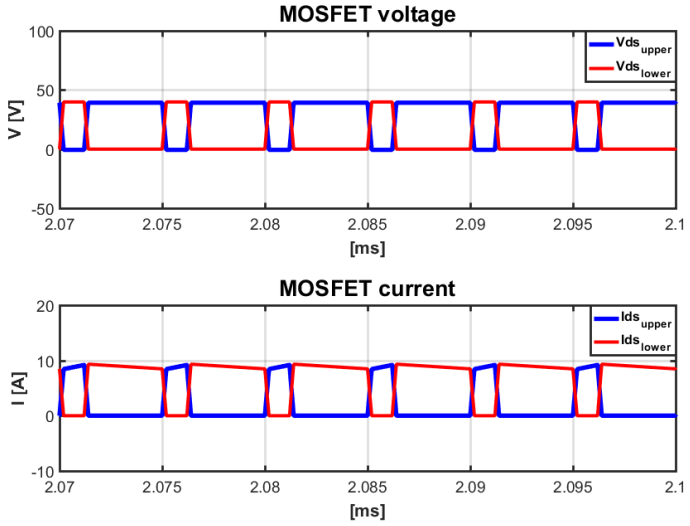

Figure 4.5: MOSFET voltage and current for f_{sw}=200 kHz

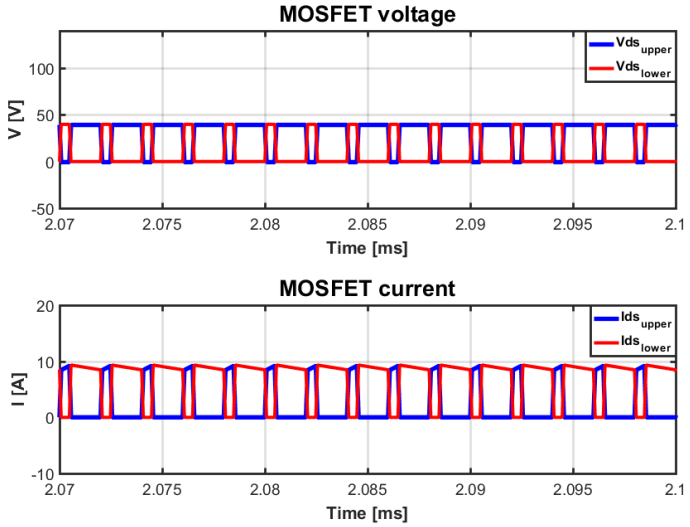

Figure 4.6: MOSFET voltage and current for f_{sw}=500 kHz

The total drain to source current from both the MOSFETs has a triangular behaviour in the waveform, which can been seen at the peak of the waveforms in Figure 4.5 and 4.6. The reason for this is because of the inductor in the circuit. The inductor current (i_L) consist of a triangular ripple and because of Kirchhoff's

current law (KCL), Ids_{above} is equal to i_L when the lower MOSFET is turned off. When the upper MOSFET is turned off, the Ids_{under} is equal to i_L. The voltage over the inductor and the inductor current is shown in Figure 4.7 and 4.8.

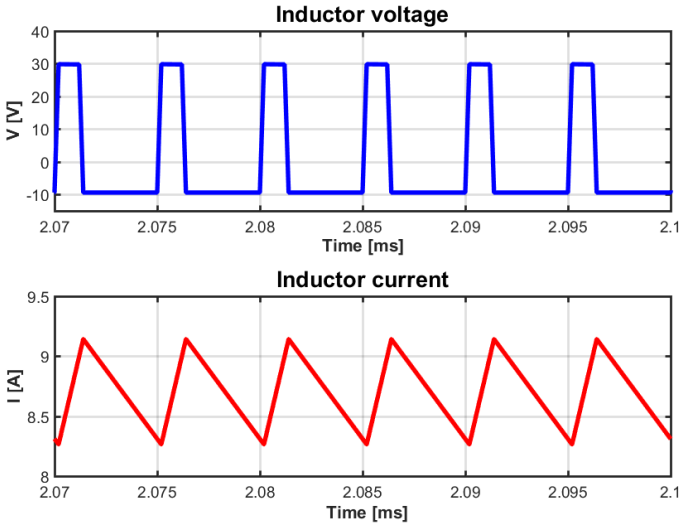

Figure 4.7: Inductor voltage and current for f_{sw}=200 kHz

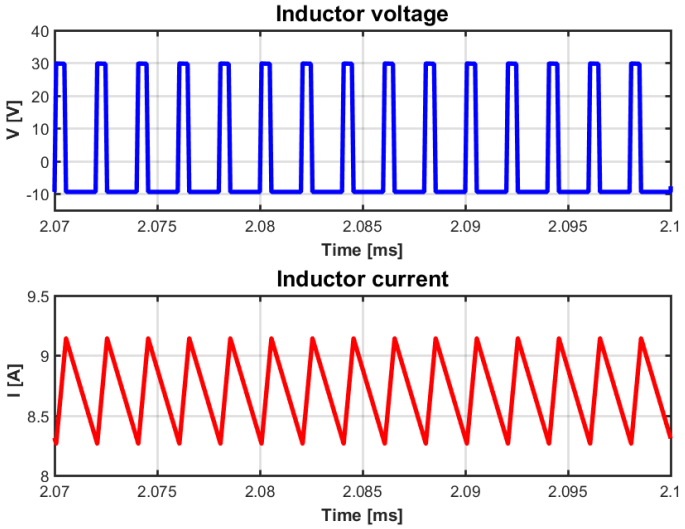

Figure 4.8: Inductor voltage and current for f_{sw}=500 kHz

In a buck converter the inductor's function is to store magnetic energy [20]. When the upper MOSFET is turned on, a positive voltage is applied over the inductor resulting in magnetic energy being stored in the inductor which can be concluded from Figure 4.5 and 4.7. When the upper switch is turned off, the stored magnetic energy in the inductor is dissipated to the load. This leads to that i_L will decrease linearly. The figures also show that i_L has a dc offset, which is a result from the load since the dc components of i_L flow through the load. When the lower MOSFET is

turned on and off it will not affect the inductor voltage or current, as can be seen in Figure 4.5 and 4.7.

The capacitors function in the buck converter is to both filter the output voltage so that it will be similar to a pure dc voltage and to store energy. The voltage over the capacitor is the result of the stored amount of charges and the capacitance in the capacitor [20]. The voltage over the capacitor and its current is presented in Figure 4.9 and 4.10.

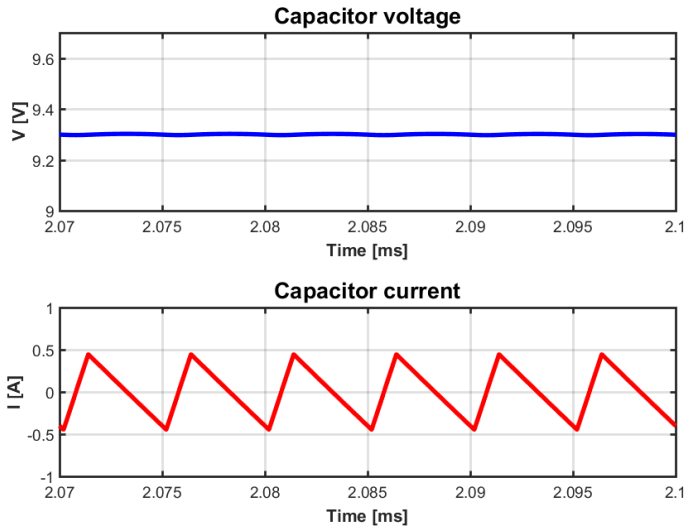

Figure 4.9: Capacitor voltage and current for f_{sw}=200 kHz

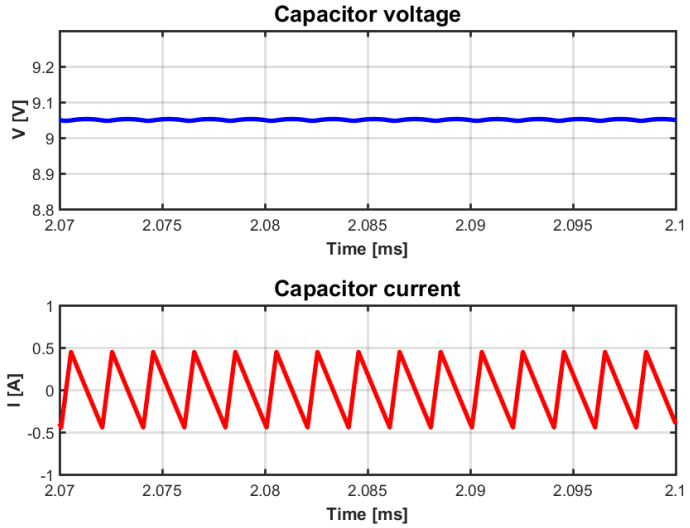

Figure 4.10: Capacitor voltage and current for f_{sw}=500 kHz

The output current i_{out} should be a dc current and according to KCL $i_{out} = i_L$ - i_C which means that the ripple component from the inductor current needs to flow through the capacitor. From Figure 4.5 and 4.9 it can be seen that the

capacitor current consist of the inductor ripple without the dc offset. The output voltage and current from the model is presented in Figure 4.11 and 4.12.

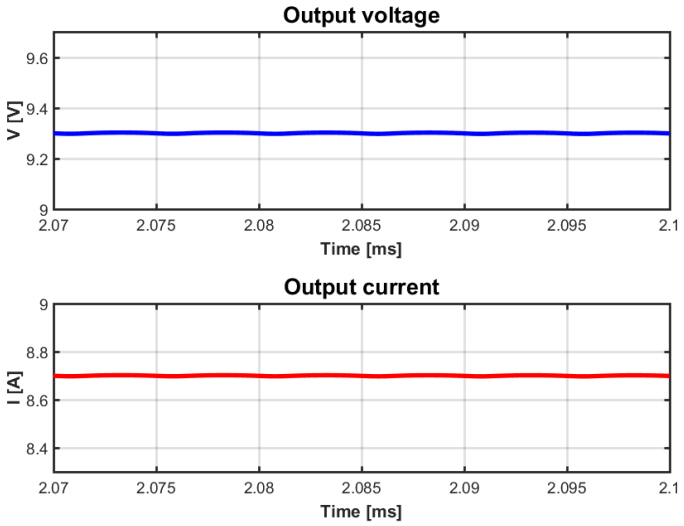

Figure 4.11: Inductor voltage and current for f_{sw}=200 kHz

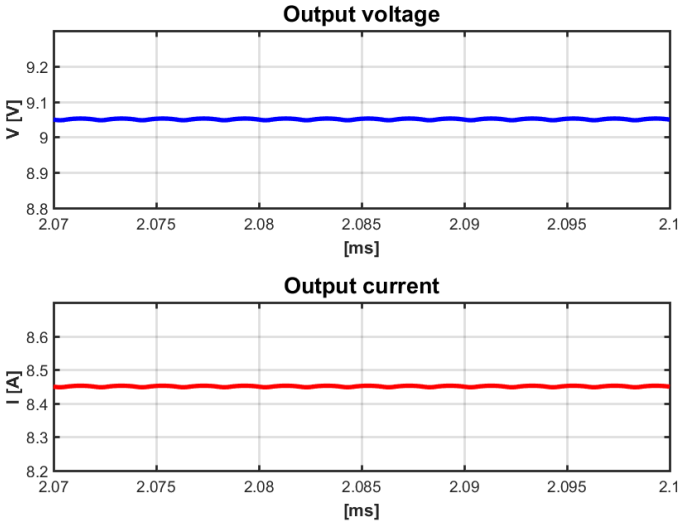

Figure 4.12: Inductor voltage and current for f_{sw}=500 kHz

The figures show that the output voltage is a dc voltage with a small ripple according to the specifications of the project. The figures also show how the output current is a dc current with a small ripple. However, the current is slightly below the specified value of 9.6 A and the reason being that the load that was used is 1.072 Ω and not 1 Ω.

4.2 Effect of Parasitic Elements

In Section 4.1 a simplified model of a dc/dc converter was simulated, but in practice there are losses due to for example the parasitic elements that each component contains. A simplified model of the buck converter with parasitic elements with two MOSFETs can be obtained from Figure 4.13.

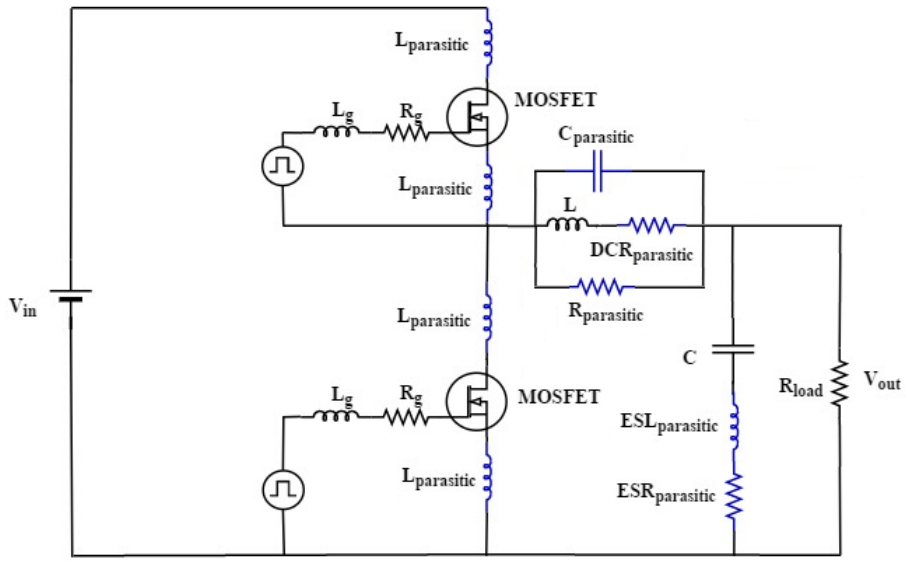

Figure 4.13: Buck converter with parasitic elements and MOSFET as switch

In Figure 4.13, the blue components indicate the parasitic elements for most of the components. Not all the parasitic components were considered because the model would be to complex. Therefore, only the parasitic elements from the components that have the largest effect on the circuit were considered. The values for the different parasitic elements and the gate components were first estimated, in order to get an approximated practical model. The exact values for the parasitic elements and the gate components are presented in Section 5.2. The values for the inductor, capacitor, the voltages etc. is the same as in the simplified model in Section 4.1.

5

Design

In this chapter the final designs of the dc/dc converters and selection of their components are presented. One of the dc/dc converter designs is with Si transistors and the other one is with GaN transistors. The two converters differ, since GaN transistors requires a different design in order to work. The design of the two converters was built in the 3D software called Altium Designer, in order to design them in 3D before ordering them. As mentioned in Chapter 4, SiC was not investigated further than a literature study.

5.1 Selection of Components

All the components in the converters were RoHS compliance since they are more sustainable. The components were ordered outside EU, which means that it was not a requirement to order the component to pass the RoHS compliance. If they were ordered inside EU then all products in EU needs to pass the RoHS compliance. The choice of using RoHS compliance components was easy to make since it is good to have the converters as sustainable as possible. Most of the components are surface mounted in order to reduce the stray inductance in the converter. The definition of surface mounted is that the components are directly attached to the PCB. When having little space between the component and the PCB then a loop of magnetic field and stray inductance emerges, which leads to more disturbance in the converter.

The component values were first calculated for each converter at their operating frequency. Then the selection of components was made, after the values was calculated in order to get as close to the calculated value as possible. Before the inductor, output capacitor and MOSFET could be selected their expected losses were calculated in both the simplified and parasitic simulation models in order to get as high efficiency as possible for the converter. The expected losses for the inductor, capacitor and MOSFET were calculated by inserting values from the components datasheets in the simulations models.

5.1.1 Selection of the Si converter components

The Si converter was designed for 100 kHz and the component values for the inductor and output capacitor were calculated for this frequency. In Table 5.1 a comparison of the calculated values and the selected values is presented.

Table 5.1: Comparison of calculated values and selected values for the inductor and output capacitor

Parameters	Calculated value	Selected value
L_{100} [μH]	91.2	100
C_{100} [μF]	208.33	198

The chosen inductor is of the type 'fixed inductor', which means that its wound turns of wire in the coil are fixed. It is important to consider both the current rating and the current saturation of the inductor when choosing an inductor. This is to ensure that the inductor can withstand the applied current but also so that it will not be saturated. The chosen inductor is a 100 μH inductor from the manufacture Bourns with the name 1140-101K-RC. In Table 5.2 the current rating and current saturation from Appendix E is compared to the average inductor current ($i_{L_{avg}}$) from the Si converter. It can be seen that $i_{L_{avg}}$ is lower than both the current rating and the current saturation which indicate that is was a suitable choice.

Table 5.2: Current specification of the 100 μH inductor

Parameters	value
Current rating [A]	10.5
Current saturation [A]	20.6
$i_{L_{avg}}$ [A]	8.7

For the output capacitor nine 22 μF capacitors were chosen. By connecting the nine capacitors in parallel, the output capacitor got a value of 198 μF. The output capacitor was of the type 'ceramic capacitor'. When choosing an appropriate capacitor it is important to consider the voltage rating. The reason that the nine capacitors in parallel were chosen over one bigger capacitor was because of the voltage rating. There were no available capacitors with the amount of capacitance needed and with the desired voltage rating. The selected capacitor was from the manufacturer United Chemi-Con with the name $KTS500B226M76N0T00$ and their voltage rating was 50 V, which can been seen in Appendix F. According to the project specification, the output voltage should be 40 V. The selected capacitor was therefore a suitable choice.

The selected Si MOSFET was of the type 'surface mounted' in order to decrease the stray inductance from the component. When selecting a MOSFET it is important to consider the current rating of I_{ds}, the rating of the drain to source voltage (V_{dss})

and the value of $R_{ds_{on}}$. It is suitable to have a margin for the applied I_{ds} and V_{ds} to the rating of I_{ds} and V_{dss} to make sure that the MOSFET can operate safely. A low value of $R_{ds_{on}}$ is preferable since it will give low conduction losses according to (2.27). The rating of I_{ds}, V_{dss} and $R_{ds_{on}}$ for the Si MOSFET was chosen to be similar to the GaN MOSFET, in order to make a fair comparison of the different materials. The selected Si MOSFET was from the manufacturer STMicroelectronics with the name $STD47N10F7AG$. In Table 5.3 the ratings for the Si MOSFET is presented.

Table 5.3: Specification of Si MOSFET

Parameters	**Value**
V_{dss} [V]	100
I_{ds} [A]	45
$R_{ds_{on}}$ [mΩ]	18

When selecting an appropriate gate driver, it is good to check the specifications of the MOSFET's gate threshold voltage ($V_{gs_{th}}$) and how V_{gs} is varying with I_d and V_{ds} as well as comparing them to the gate driver's power supply voltage. According to Appendix C the $V_{gs_{th}}$ is 4 V and therefore require the gate driver's power supply voltage to be higher than 4 V. In Appendix C on page 6 it is presented how V_{gs} is varying with I_d and V_{ds} and that a preferable V_{gs} is 10 V. This indicates that the gate driver's power supply voltage should be around 10 V. The selected gate driver $Si8233$ has a range of power supply voltages starting from 6.5 V up to 24 V, according to Appendix A. The gate driver's power supply voltage was chosen as 12 V to give a margin to the 10 V from the V_{gs} value of the MOSFET. The selected gate driver had been used in a similar project at the company before, which affected the choice of gate driver since it was known that it would work suitable and within the specifications of the MOSFET. The capacitors and resistors for the gate driver circuit was selected by the recommendations of the IC in Appendix A.

5.1.2 Selection of the GaN converter components

The GaN converter was designed for 400 kHz and the component values for the inductor and output capacitor were calculated for this frequency. In Table 5.4 a comparison of the calculated values and the selected values is presented.

Table 5.4: Comparison of calculated values and selected values for the inductor and output capacitor

Parameters	**Calculated value**	**Selected value**
L_{400} [μH]	22.8	22
C_{400} [μF]	52.083	50

The selected inductor for GaN is also of the type 'fixed inductor'. The inductor

is from the manufacturer Wurth Electronics Inc. with the name 7443632200. In Table 5.5 the current rating and current saturation from Appendix G is compared to the average inductor current ($i_{L_{avg}}$) from the GaN converter. It can be seen that $i_{L_{avg}}$ is lower than both the current rating and the current saturation which indicate that is was a suitable choice.

Table 5.5: Current specification of the 100 μH inductor

Parameters	**Value**
Current rating [A]	12
Current saturation [A]	15
$i_{L_{avg}}$ [A]	8.47

For the output capacitor, five 10 μF capacitor were chosen. By connecting the five capacitors in parallel, the output capacitor got a value of 50 μF. The output capacitor was of the type 'ceramic capacitor'. The selected capacitor was from the manufacturer TDK Corporation with the name $CGA6P3X7S1H106K250AB$ and the voltage rating is 50 V according to Appendix H. According to the project specification the output voltage should be 40 V, which made the selected capacitor a suitable choice.

The selected GaN MOSFET was also of the type 'surface mounted'. Since GaN MOSFETs are new on the market, the supply is quite limited. The limited selection of GaN MOSFETs was the reason that the rating of I_{ds} was 45 A and V_{dss} was equal to 100 V in order to get a low voltage application with a safety margin.

The selected GaN MOSFET was from the manufacture GaN Systems with the name $GS61004B$. In Table 5.6 the ratings for the GaN MOSFET is presented.

Table 5.6: Specification of Si MOSFET

Parameters	**Value**
V_{dss} [V]	100
I_{ds} [A]	45
$R_{ds_{on}}$ [mΩ]	15

The similarities between Table 5.3 and 5.6 implies that a comparison of the two materials will be fair, based on their parameter values.

The selected gate driver for the GaN converter was from the manufacturer TEXAS INSTRUMENTS with the name $LM5113$. According to Appendix D, for the GaN MOSFET the $V_{gs_{th}}$ is 1.3 V and therefore needs the gate driver's power supply voltage to be higher than 1.3 V. In Appendix D at page 4 it is presented how V_{gs} is varying with I_d and V_{ds} and that a preferable V_{gs} is 5 V to 6 V. This indicates that the gate drivers power supply voltage should be around 5 V. The selected gate driver $LM5113$ has a range for power supply voltages from 4.5 V to 5.5 V according

to Appendix B. The gate driver's power supply voltage was chosen as 5 V. The selected gate driver had been used in a similar project from the GaN MOSFET manufacture GaN System where they recommended the selected gate driver for the selected MOSFET. The capacitor and resistors for the gate driver circuit was selected by the recommendations of the IC in Appendix A.

5.2 dc/dc Converter

The final design of the two buck converters, one with Si transistors and one with GaN transistors, can be seen in Figure 5.1. It can be seen that the converter with the GaN transistors is smaller since it has smaller components, most significant is the inductor (white cylindrical for Si and black butterfly shaped for GaN) and the capacitors (nine next to the inductor for Si and 5 next to the inductor for GaN).

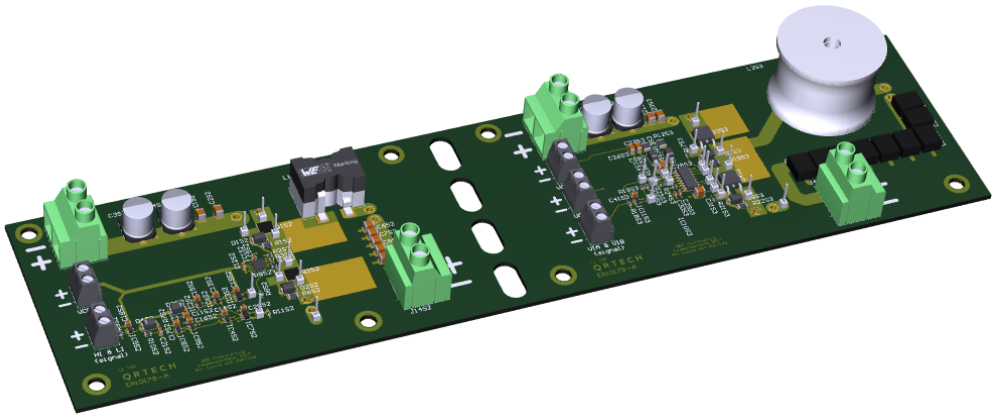

Figure 5.1: The final design of the buck converters with both Si (on the right) and GaN transistors (on the left) respectively

Both the converters were weighted and measured in order to compare if the theory behind the WBG semiconductor is accurate (smaller size at higher switching frequency). The weight and the measurements of the two converters are presented in Table 5.7.

Table 5.7: The weight and measurements of the two converters of the final circuit

Semiconductor	Components	Weight	Area	Piece price [SEK]
Si	Converter	204	170 x 84	12.19
	Inductor	102	19.05^2 x π	
	MOSFET	<1	9.725 x 6.50	
GaN	Converter	108	150 x 84	55.91
	Inductor	15	21.5 x 21.8	
	MOSFET	<1	4.6 x 4.4	

As the table clearly shows, the size of the components for the GaN converter is smaller and thereby has less weight than those of the Si one. The weight of the converter with Si transistors is almost two times more. The results match the theory, namely that at higher frequencies the size of components decrease. The buck converter with GaN transistors was designed for 400 kHz and for the Si converter it was designed for 100 kHz. The reason the design was for 100 kHz and 400 kHz is because that then the converters could also operate at 200 kHz and 500 kHz respectively. This is since it was decided that the converter with Si transistors should operate at 100 kHz and 200 kHz, and 400 kHz as well as 500 kHz for the converter with GaN transistors. The reason neither of the converters was operated at 300 kHz was due to the time limitation of the project.

5.2.1 Schematic of the two dc/dc Converters

The schematic of the two converters is presented in Figure 5.2 and 5.3. From the figures it can be seen that the design regarding the two converters are different because of the different transistor materials. One obvious difference between the two converters is the difference in gate drivers for the transistors. The set-up of the gate driver contains an IC, gate resistances, and a bootstrap capacitance. The amount of gate resistances and bootstrap capacitors depends on the chosen IC. This is since different ICs have different amount of input and output signals. The schematic of the chosen ICs are designed the same as a datasheet for the two different ICs. The chosen IC for the Si transistors was Si8233 och for GaN it was LM5113. The datasheet of the design and the pin configuration of the IC for Si can be seen in the pages 31 and 33 in Appendix A. The same thing for GaN can be seen in pages 1, 3 and 4 in Appendix B.

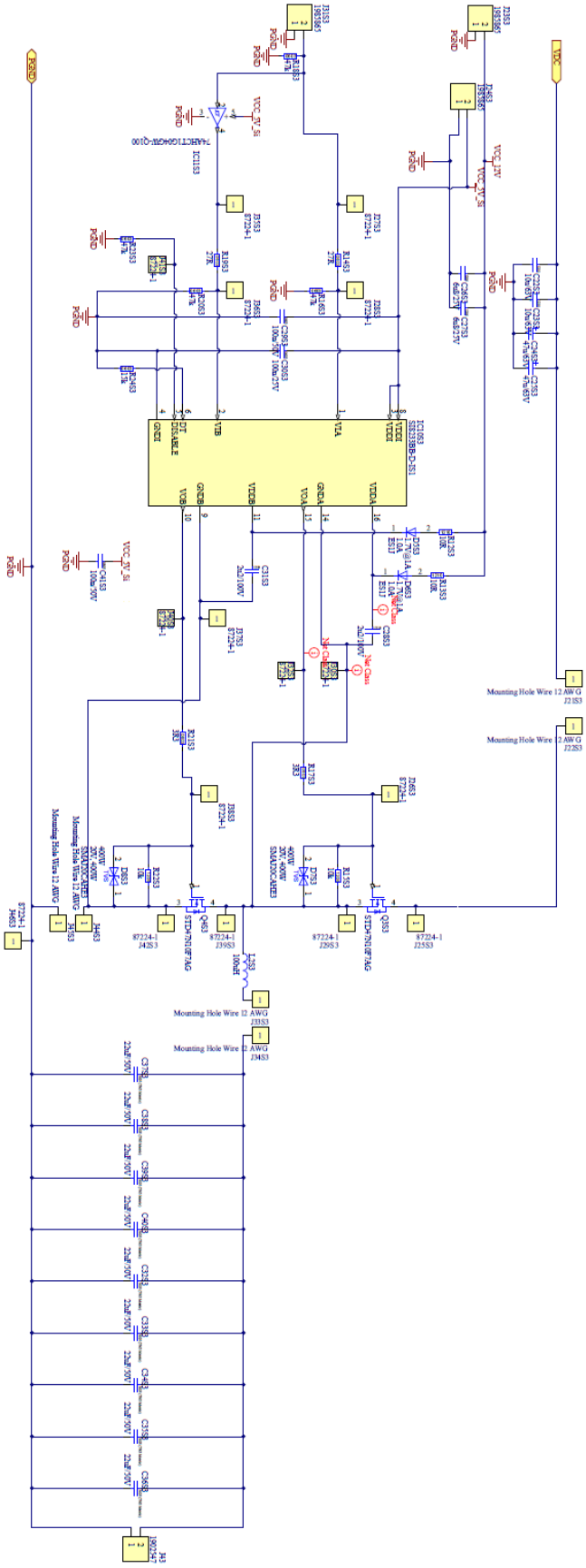

Figure 5.2: The schematic of the final design for the buck converters with Si transistors

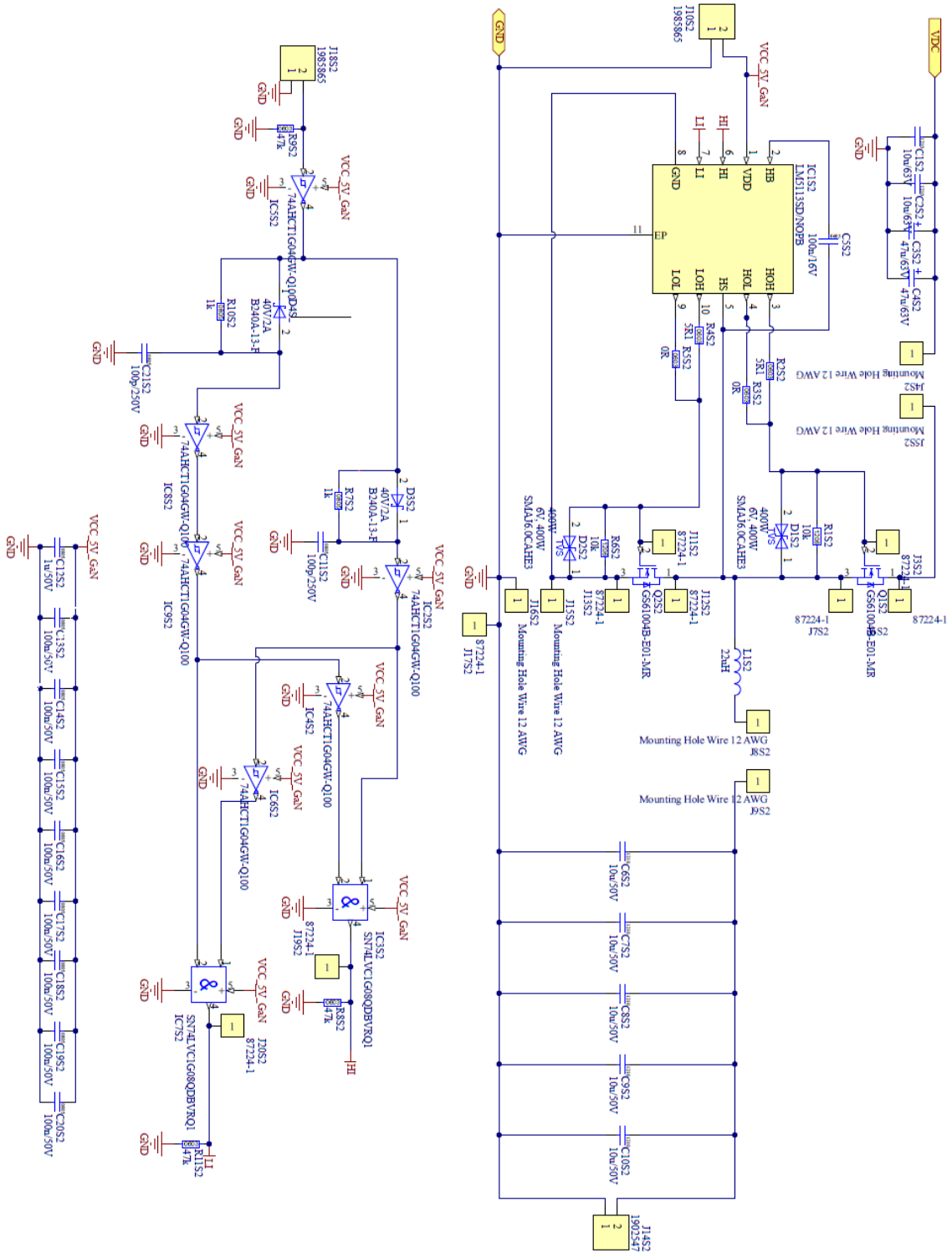

Figure 5.3: The schematic of the final design for the buck converters with GaN transistors

The four capacitors before the MOSFET above (C_{22S3}, C_{23S3}, C_{24S3}, C_{25S3} for Si and C_{1S2}, C_{2S2}, C_{3S2}, C_{4S2} for GaN) are present to make the input current as dc as possible, instead of a square wave current from the square wave pulse and also to

reduce the ripples and the disturbances. The four capacitors for each converter are highlighted with a red circle and can be obtained from Figure 5.4 and 5.5.

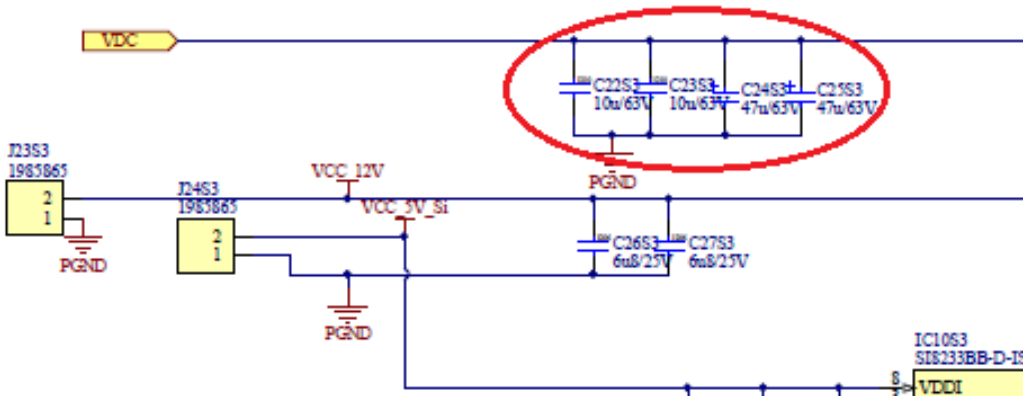

Figure 5.4: The capacitors to filter the input current in the converter with Si transistors

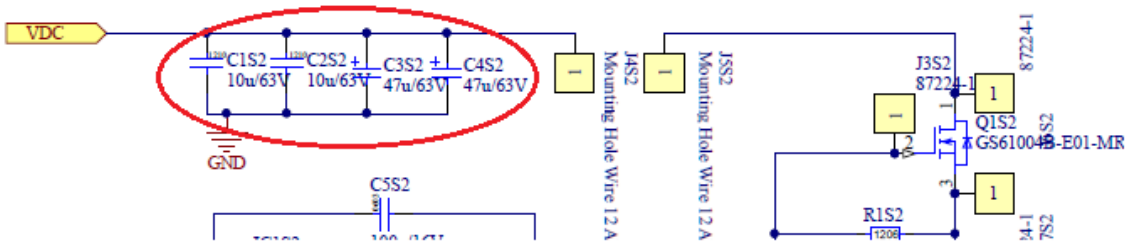

Figure 5.5: The capacitors to filter the input current in the converter with GaN transistors

In the buck converter with the GaN transistors, a logic circuit had to be designed since it was not present in the initial chosen IC for the gate driver. The logic circuit is needed to regulate the deadband for the logic signal into the IC. For the converter with the Si transistors a logic circuit was already present. The set-up of the logic circuit for the GaN transistors can be obtained in Figure 5.3, below the design of the buck converter. In Figure 5.6 the eight capacitors (C_{13S2}, C_{14S2}, C_{15S2}, C_{16S2}, C_{17S2}, C_{18S2}, C_{19S2}, C_{20S2}) represent logic gates, namely NOT and AND gates. They were implemented in order to filter out disturbances and keep the logic voltage smooth and continuous. This is to ensure that the logic circuit do not vary when they switch from high to low signals. A good design should include these capacitors since they reduce the ripple on the input voltage for the logic gates. The last capacitor (C_{12S2}) is for the IC and functions in the same as the mentioned eight capacitors, but for the IC instead. It should be close to the IC to maximize the performance of the gate driver.

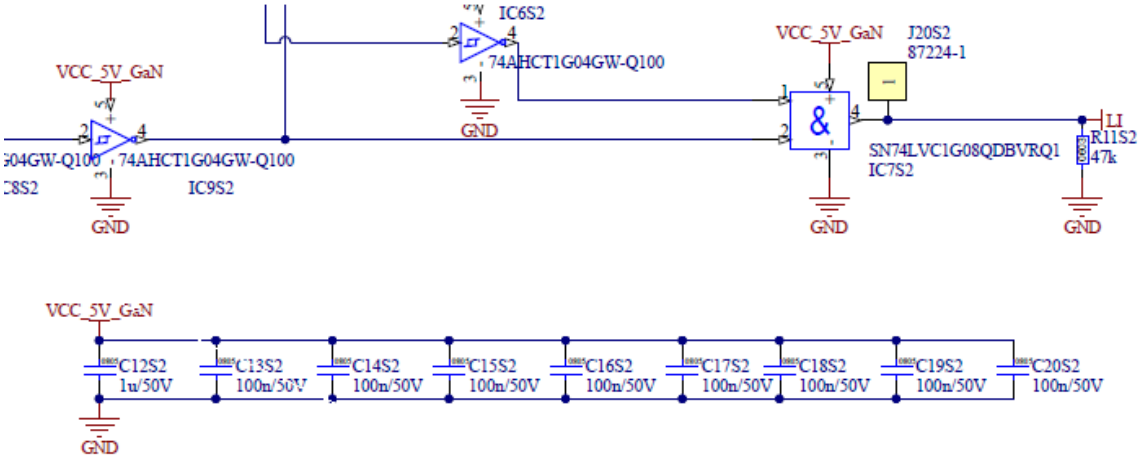

Figure 5.6: The capacitors for the logic circuit in the converter with GaN transistors

The reason for the deadband in the logic signals is to prevent the two MOSFETs to be turned on or off at the same time. The deadband was designed to be in ns, this is because when having a to large deadband it causes more losses in the converter. This occurs due to that the body diode in the MOSFETs conduct at that time (the time of the deadband) and the diode has more losses than the MOSFET. The deadband of the logic signals from this designed logic circuit for the GaN converter can be seen in Figure 5.7.

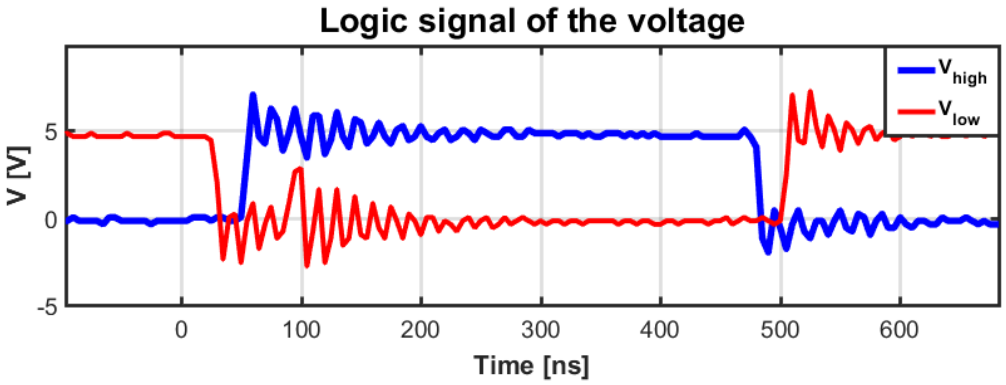

Figure 5.7: The deadband of the logic signals for the GaN converter

In both the converters there are interruption in the circuit in three places: one before the MOSFET above, one after the MOSFET below, and one after the inductor. These are marked with a red circle for both the Si and GaN converter and can be seen in Figure 5.8 and 5.9. This is to test the converters for disturbances and see how they operate when applying a disturbance source. The disturbance was applied by adding a larger metal wire, since larger metal wires lead to more magnetic field and stray inductance. With more magnetic field and stray inductance it results in more oscillation in the voltage and the current.

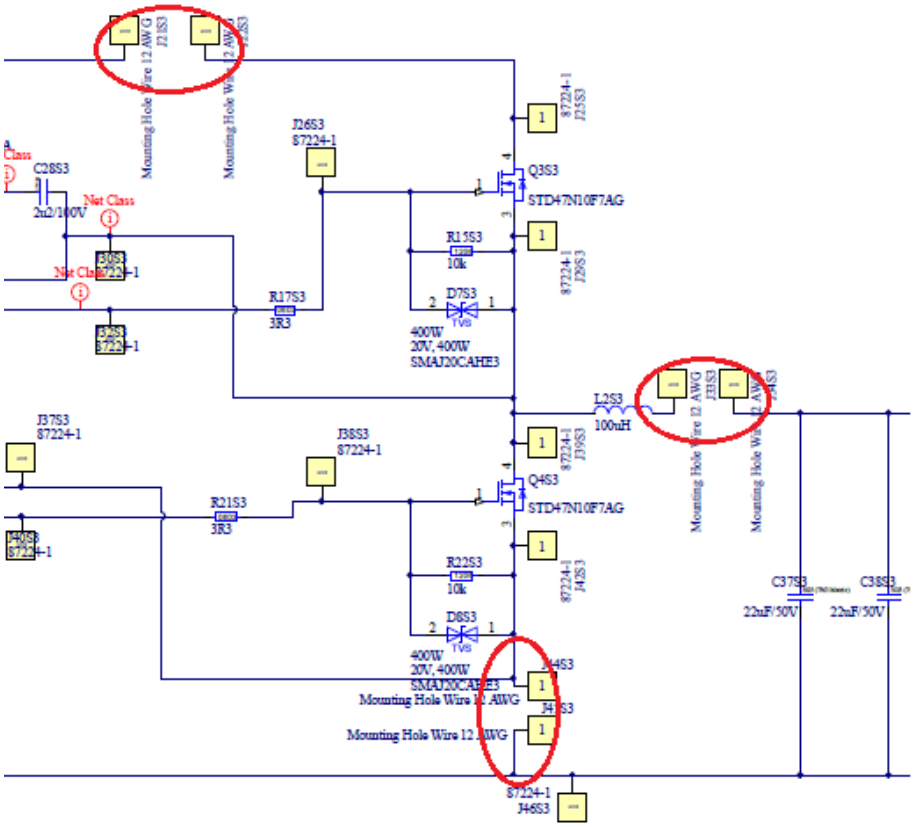

Figure 5.8: The interruptions in the converter with Si transistors

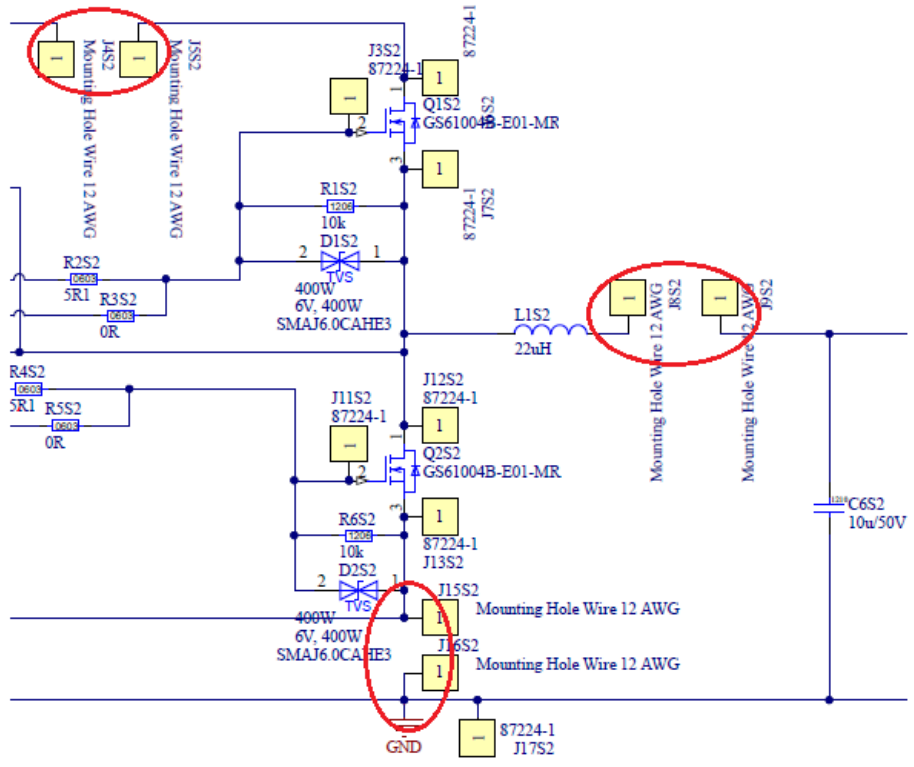

Figure 5.9: The interruptions in the converter with GaN transistors

6

Analysis

In this chapter the dc/dc converters performance and the WBG materials effect on the performance will be evaluated. The results of the simulated parasitic models, the measurement of the practical designs and a comparison between them are presented.

6.1 Component and Parasitic Element Classification

To have an idea on how much losses each component contributes, the parasitic elements of the components need to be measured. This was done with the measuring device, bode100. The parasitic elements of the capacitor are Equivalent Series Inductance (ESL) and Equivalent Series Resistance (ESR). By measuring the magnitude, with respect of the switching frequency, at certain phases the two parasitic elements can be extracted. The value of ESL was measured when the phase, φ, was at 90° because at that phase the capacitor becomes inductive. The value of ESR was measured when the phase was at 0° because at that phase the capacitor becomes resistive. The value of the capacitor was measured when φ was at -90°, to verify that it was correct. The same procedure was applied for the measurement on the inductor, but the parasitic elements of the inductor are Direct Current Resistance (DCR), iron resistance (R_{Fe}) and the parasitic capacitance (C_p). The measurement of R_{Fe} was performed when φ was at 0° and for C_p when φ was at -90°. The value of the inductor was measured when φ was at 90°. The value of DCR could not be measured with the bode100, it was instead measured by using a Kelvin connection which can handle small loads. The connection can be seen in Figure 6.1.

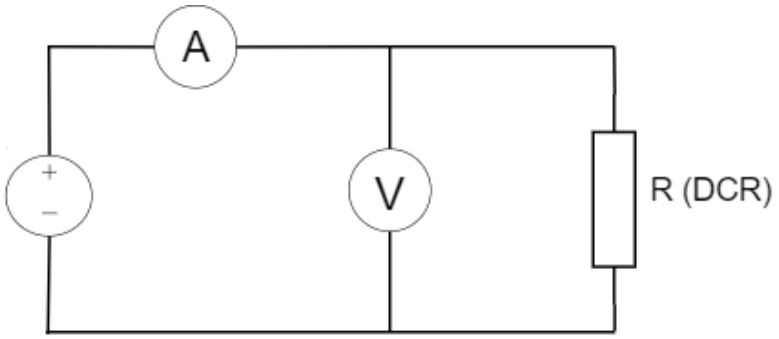

Figure 6.1: Kelvin connection used to measure DCR

The input voltage to the Kelvin connection was tested for three different voltage values, to ensure a correct value of DCR in the inductor. The three input voltages were 1 V, 2 V, and 3 V which allowed the current (A) and the voltage (V) to be measured using the FLUKEs. With the voltage and current value obtained, by using Ohm's law the DCR value was calculated.

The parasitic elements for the MOSFET are the parasitic inductance on the drain, gate, and source (L_D, L_G and L_S), internal resistance ($R_{DS(on)}$) and internal capacitances (C_{iss}, C_{oss} and C_{rss}). The parasitic inductances of the MOSFET were also measured by the bode100. By measuring the inductance on the drain, gate, and source of the PCB, the values of the inductances were obtained for $\varphi = 90°$. $R_{DS(on)}$ of the MOSFET was measured by heating up the MOSFET to a temperature corresponding to when the input voltage was at 40 V. More details regarding how the measurement was performed can be seen in Thermal Analysis in Section 6.3. C_{iss}, C_{oss} and C_{rss} were not measured since they are temperature dependent, which makes it difficult to get correct measurements. The values for those were instead taken from the datasheet in page 4 in Appendix C for the Si transistor and in page 3 in Appendix D for the GaN transistor. The values from all the measurements for both converters are presented in Table 6.1 and 6.2.

Table 6.1: The values of the parasitic elements of the components for the two converters

Components	Parasitic elements	Values	Values from measurement	Values from datasheet
L_{Si}	C_p DCR R_{Fe}	25.448 pF 18.9 mΩ 37.547 kΩ	88.391 μH	100 μH
C_{Si}	ESL ESR	984.827 pH 9.555 mΩ	20.938 μF x 9	22 μF x 9
L_{GaN}	C_p DCR R_{Fe}	4.065 pF 10.8 mΩ 7.774 kΩ	19.951 μH	22 μH
C_{GaN}	ESL ESR	359.631 pH 5.162 mΩ	9.321 μF x 5	10 μF x 5

Table 6.2: The values of the parasitic inductances of the PCB for the two converters

Parameters	Components	Values [nH]
L_{Si}	before $MOSFET_{upper}$	16.860
	between the MOSFETs	8.383
	after $MOSFET_{lower}$	15.842
	gate driver $MOSFET_{upper}$	21.732
	gate driver $MOSFET_{lower}$	30.705
L_{GaN}	before $MOSFET_{upper}$	12.204
	between the MOSFETs	9.701
	after $MOSFET_{lower}$	12.141
	gate driver $MOSFET_{upper}$	10.434
	gate driver $MOSFET_{lower}$	19.904

6.2 Parasitic Element Model

In Section 6.1 measurements of each component's parasitic elements were performed. In order to adapt the simulation models of the two converters to be as close to real converters, the parasitic elements were added to the models. This is to improve the simulation model and get as accurate measurements as possible, regarding the losses, efficiency, waveforms etc.

6.2.1 Simulated Parasitic Element Model

In Figure 6.2 and 6.3, the input voltage and current for both converters from the simulations are presented. The Si converter has a switching frequency of 200 kHz

and GaN has a switching frequency of 500 kHz.

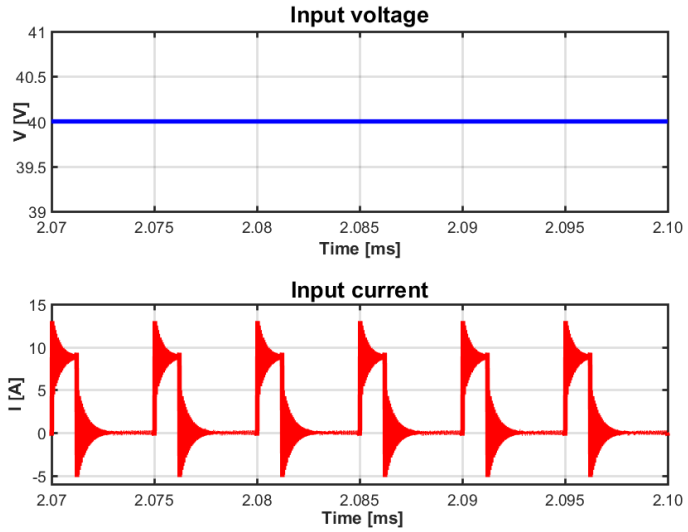

Figure 6.2: Input voltage and input current for the Si simulation with f_{sw}=200 kHz

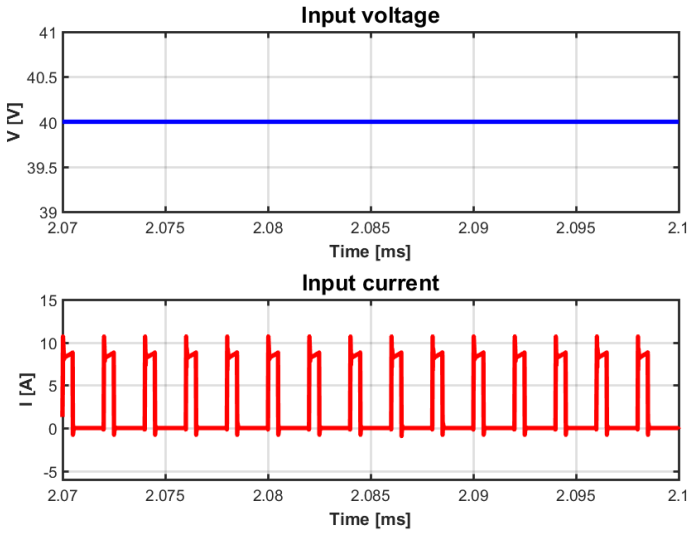

Figure 6.3: Input voltage and input current for the GaN simulation with f_{sw}=500 kHz

From the two figures it can be observed that the input voltage for both of the converters is as expected, a smooth dc signal at 40 V. On the other hand, the input current has more oscillations on both converters but more in the Si converter. The reason for the oscillations on the input current is because of the stray inductance between the input signal and the upper MOSFET. The reason that the Si converter has more oscillations is because the design of the real converter was not as tight as for the GaN converter, which resulted in more stray inductance in the Si converter. Another reason is that all the parasitic elements in the Si converter are larger than

for the GaN, as can be seen in Table 6.1 and 6.2. This results in more disturbances in the Si converter. The internal capacitances such as C_{iss}, C_{oss} and C_{rss} are also larger in the Si transistor than for the GaN transistor when comparing Appendix C at page 4 with Appendix D. The higher internal capacitance could also be an explanation as to why the Si converter has more oscillations in the input current. The reason that the GaN converter has more periods in the plot is because it has a higher switching frequency, which results in more switching in the same amount of time. In practice, the input current should also be a dc signal and not only the input voltage. The reason for the square wave pulse behaviour is due to that there are no capacitors before the upper MOSFET, which filter the current to be a dc signal. This is mentioned in Section 5.2. In Figure 6.4, 6.5, 6.6 and 6.7, both the current and voltage of the MOSFETs for both converters (200 kHz for Si and 500 kHz for GaN) can be seen.

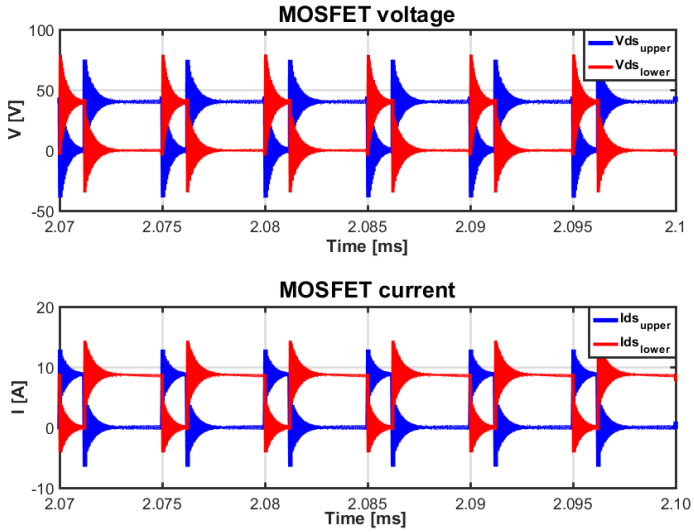

Figure 6.4: V_{ds} and I_{ds} for the Si simulation with f_{sw}=200 kHz

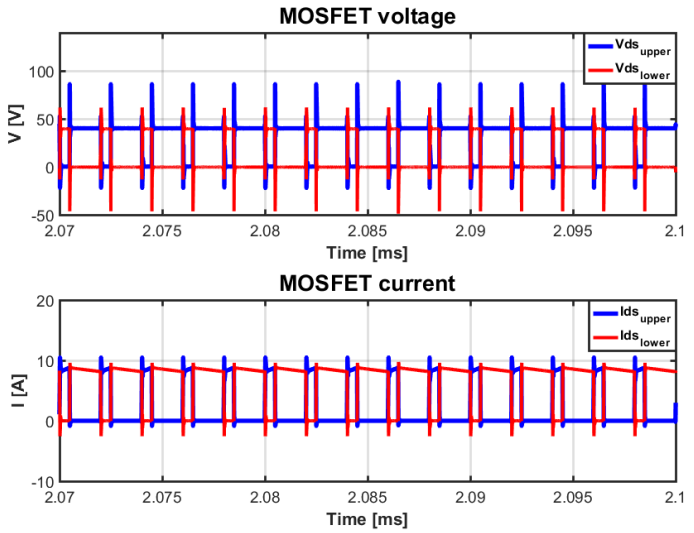

Figure 6.5: V_{ds} and I_{ds} for the GaN simulation with f_{sw}=500 kHz

From Figure 6.4 and 6.5 it can be observed that both the drain-to-source current (I_{ds}) and the drain-to-source voltage (V_{ds}) have oscillations. The Si converter has more oscillations compared to the GaN converter. It is reasonable for the oscillations to occur due to the addition of the parasitic elements to the model. The parasitic elements for the Si converter were larger than for the GaN converter, which resulted in more oscillations in I_{ds} and V_{ds} for the Si converter.

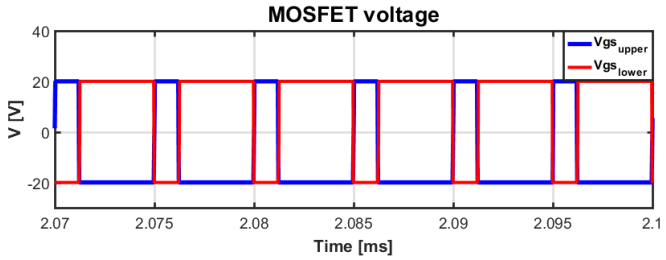

Figure 6.6: V_{gs} for the Si simulation with f_{sw}=200 kHz

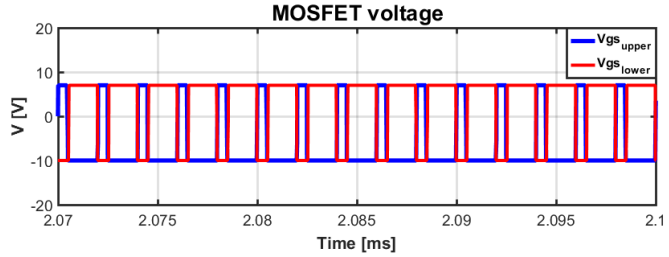

Figure 6.7: V_{gs} for the GaN simulation with f_{sw}=500 kHz

In Figure 6.6 and 6.7 the gate-to-source voltage (V_{gs}) of the two converters behave as the expected square wave pulses, but with no oscillations at all. This is because they are simulation models and do not take into account the outer losses in the surrounding. According to theory, V_{gs} of both converters should have oscillations due to the parasitic elements added to the models. In Figure 6.8 and 6.9, the inductor voltage and current for both the converters is presented.

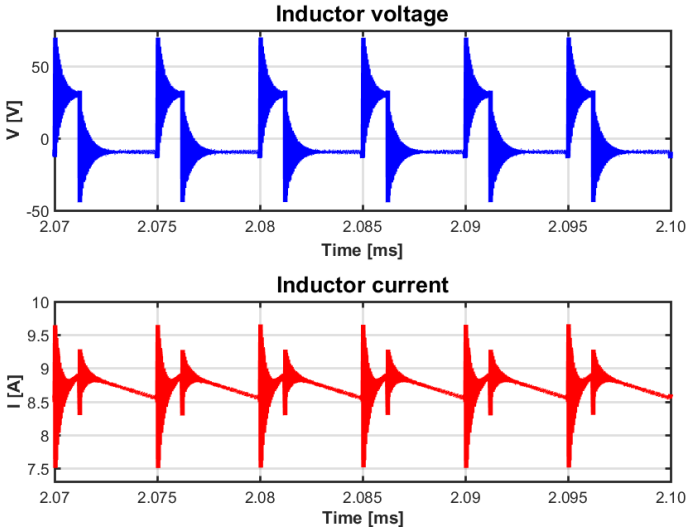

Figure 6.8: V_L and I_L for the Si simulation with f_{sw}=200 kHz

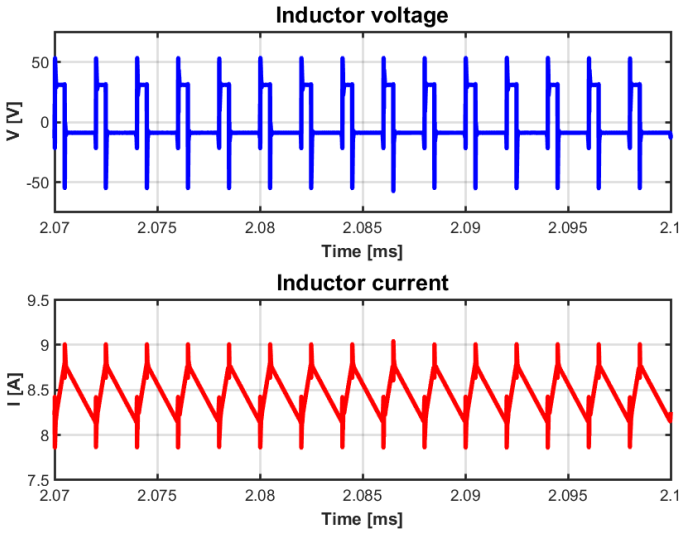

Figure 6.9: V_L and I_L for the GaN simulation with f_{sw}=500 kHz

The inductor voltage and current of both the converters contain oscillations, which can be seen in Figure 6.8 and 6.9. The reason for this kind of behaviour is again due to the addition of parasitic elements to the models. By adding parasitic elements, it results in more losses in the converter because of the oscillations that occurs in the components. Also here the Si converter have more oscillations due to the larger value of the parasitic elements. In Figure 6.10 and 6.11, the capacitor voltage and current for both the converter can be seen.

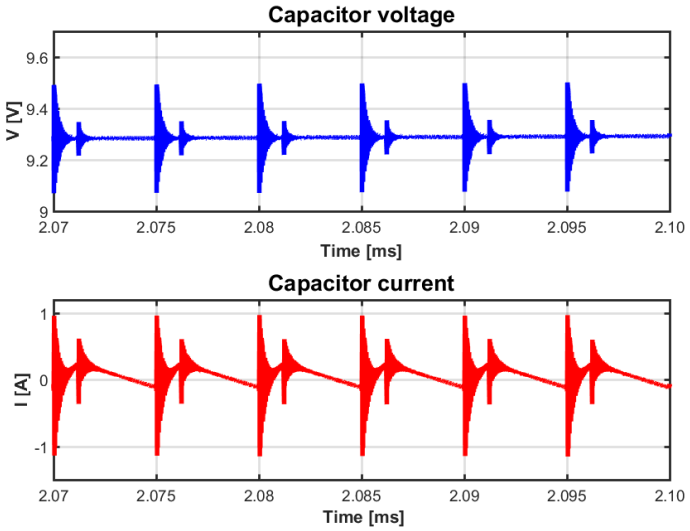

Figure 6.10: V_C and I_C for the Si simulation with f_{sw}=200 kHz

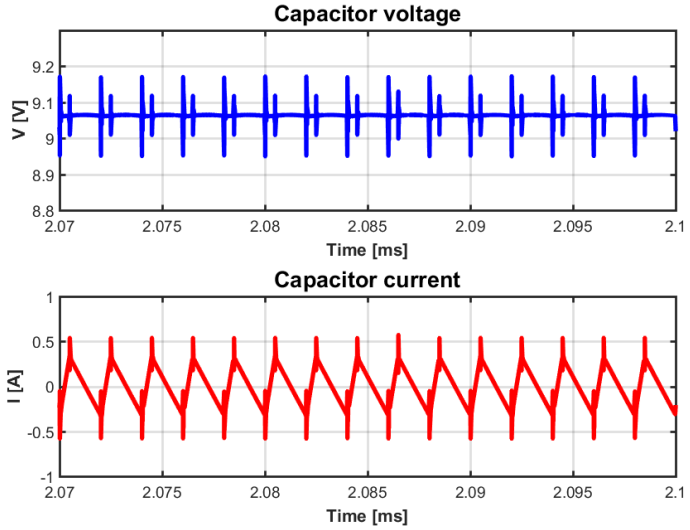

Figure 6.11: V_C and I_C for the GaN simulation with f_{sw}=500 kHz

Even in Figure 6.10 and 6.11 oscillations on both the voltage and current occurs. The Si converter have more oscillations, and this result is as expected since the parasitic elements creates more disturbance in the converters and with larger values on the parasitic elements it result in more oscillations. In Figure 6.12 and 6.13 the output voltage and current of the two converters can be obtained.

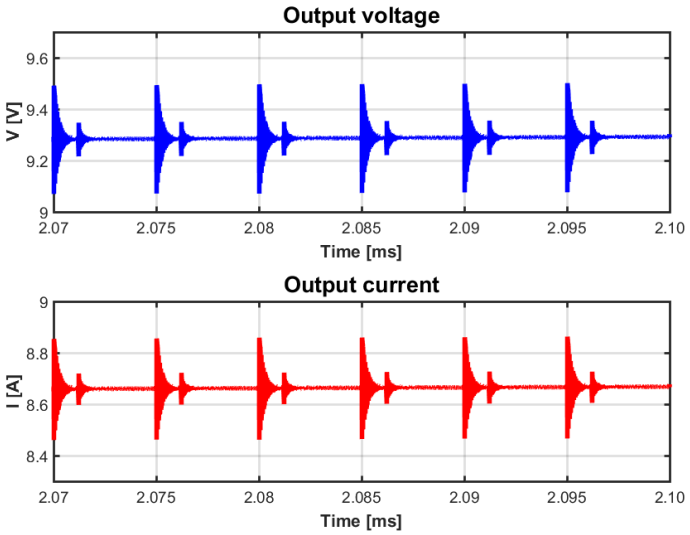

Figure 6.12: V_{out} and I_{out} for the Si simulation with f_{sw}=200 kHz

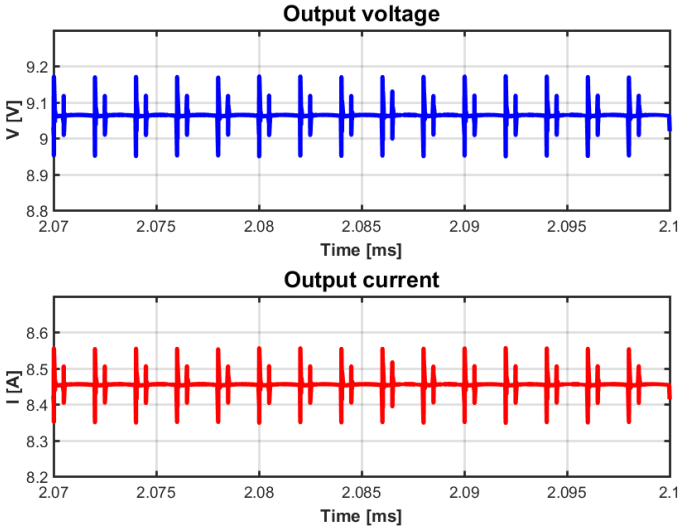

Figure 6.13: V_{out} and I_{out} for the GaN simulation with f_{sw}=500 kHz

In Figure 6.10 and 6.11, the Si converter has more oscillations with higher peaks compared to the GaN converter. Another reason that the Si converter have more oscillations in the components is due to that the design of GaN was tighter. This was possible due to the Si converter having larger component sizes, which takes more place in the converter and results in the design not being as tight as the GaN converter. The size of the components also resulted in a larger value for the parasitic elements, which leads to more and larger oscillations. The output current is almost a dc current which is reasonable since the LC circuit, before the load, filter the disturbance and the ripples.

6.2.2 Performance of the PCB

The equipments used for the measuring of the dc/dc converters are presented in Table 3.2 in Section 3.2. In Figure 6.14 and 6.15, the input voltage and current for both converters measured in the lab are presented.

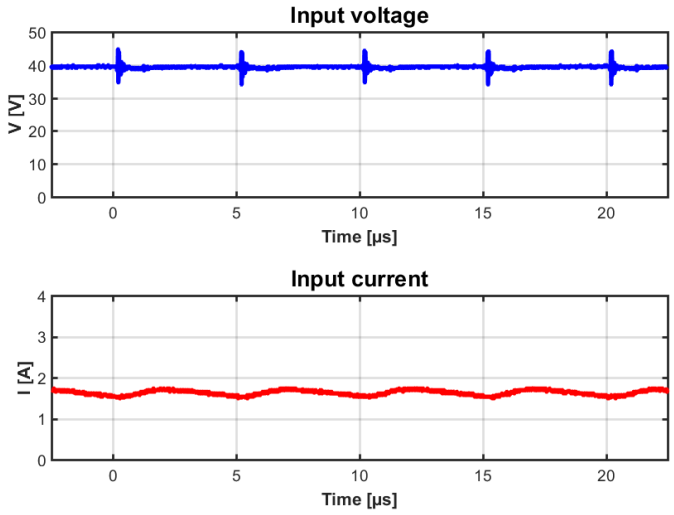

Figure 6.14: V_{in} and I_{in} for the Si measurement with f_{sw}=200 kHz

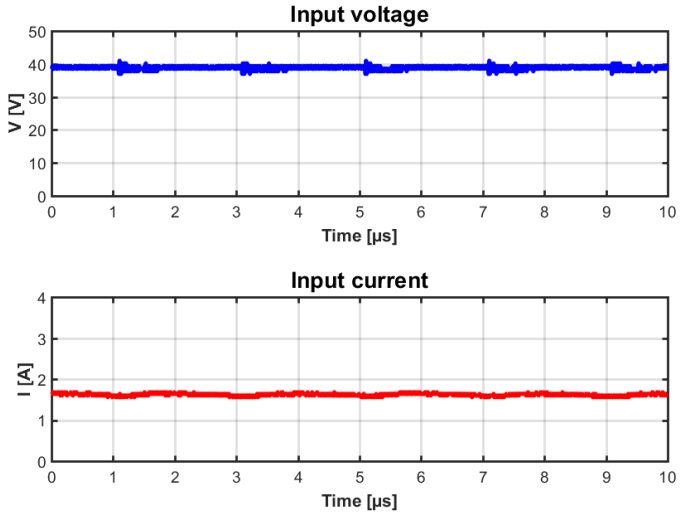

Figure 6.15: V_{in} and I_{in} for the GaN measurement with f_{sw}=500 kHz

The result of the waveforms measured in the lab were as expected. Both the current and the voltage are dc signals because in the real design there are capacitors before the upper MOSFET (mentioned in Section 5.2), which filter the current and make it a dc signal. The oscillations on the other hand are due to the parasitic elements in the components and the stray inductances from the PCB. The input voltage is not as smooth as in Figure 6.2 and 6.3 since the simulations do not account for

the temperature, air etc. in the surrounding and the cables. These aspects could cause further disturbances in the converter. The reason that the input current is not entirely a dc signal is because the value of the capacitors before the upper MOSFET are not large enough to reduce all the ripple. With a larger capacitance value on the capacitors, it reduces the ripple even more. In Figure 6.16, 6.17, 6.18 and 6.19, the voltage and the current for the MOSFETs can be observed.

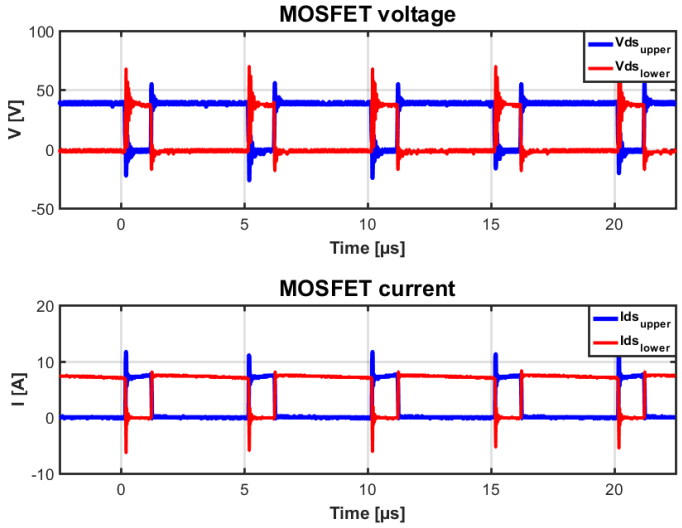

Figure 6.16: V_{ds} and I_{ds} for the Si measurement with f_{sw}=200 kHz

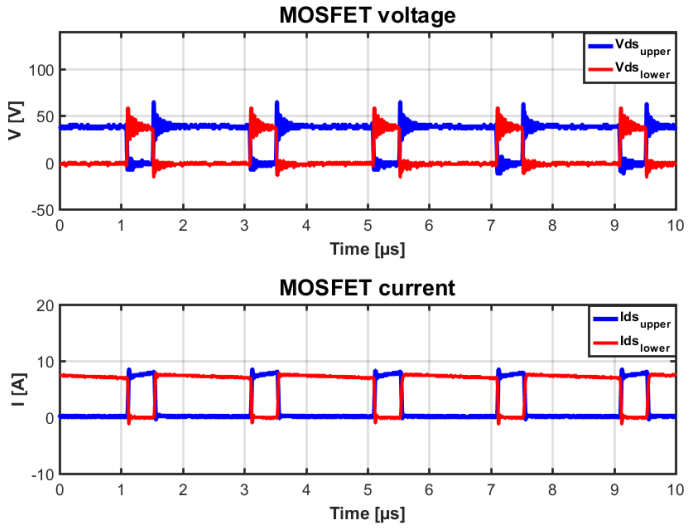

Figure 6.17: V_{ds} and I_{ds} for the GaN measurement with f_{sw}=500 kHz

From Figure 6.16 and 6.17, V_{ds} and I_{ds} for both converters have oscillations. There are more oscillations and they are larger in V_{ds} than for I_{ds}. There are more oscillations in V_{ds} for the GaN converter compared to the Si converter and this leads to more losses in the GaN converter, which in turn results in lower efficiency. The

comparison of the efficiency between the simulations and the measurements is presented in Table 6.10 in Section 6.5. The result from the simulations indicated that there should be more oscillations in the Si converter and not the GaN. One theory is that the gate driver of the GaN converter was not as good as the gate driver for the Si converter. The gate driver of the Si converter was tested and improved in other projects before it was used in this project. The gate driver for the GaN converter was not tested before since work with GaN transistors is still new. On the other hand, the current peak in the Si converter was higher than for the GaN converter. The reason for that is probably because of the inductor in the Si converter, since it has a larger value on the parasitic elements than the inductor in the GaN converter.

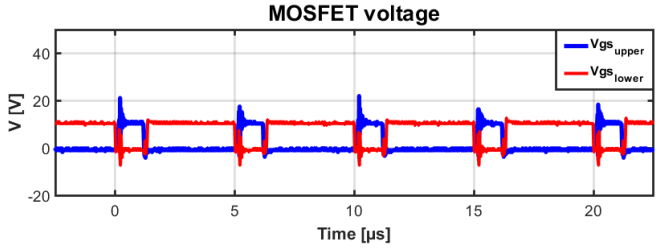

Figure 6.18: V_{gs} for the Si measurement with f_{sw}=200 kHz

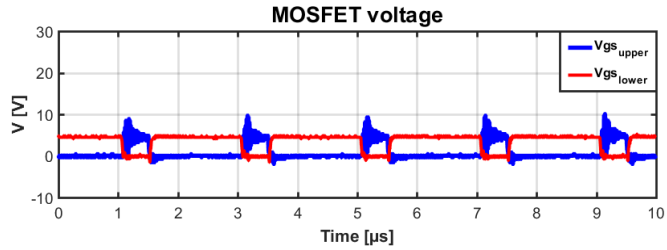

Figure 6.19: V_{gs} for the GaN measurement with f_{sw}=500 kHz

In Figure 6.18 and 6.19, V_{gs} has the same behaviour as for V_{ds} where the oscillations are more in the GaN converter. The theory behind it has already been explained in the section below Figure 6.16 and 6.17. In Figure 6.20 and 6.21, the inductor voltage and current of the real converters can be seen.

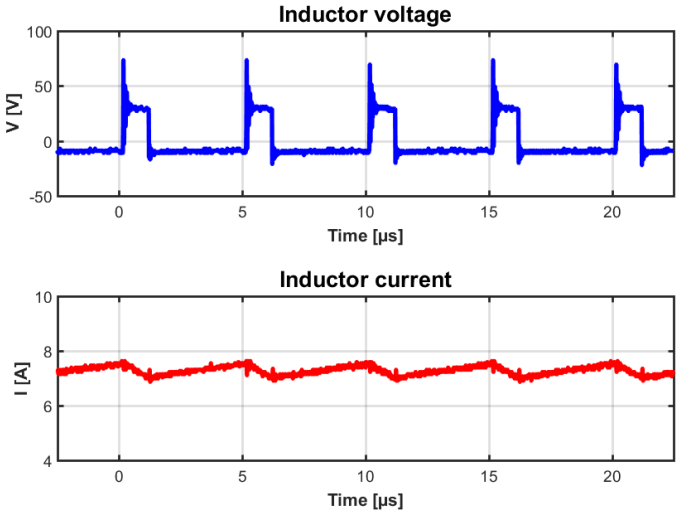

Figure 6.20: V_L and I_L for the Si measurement with f_{sw}=200 kHz

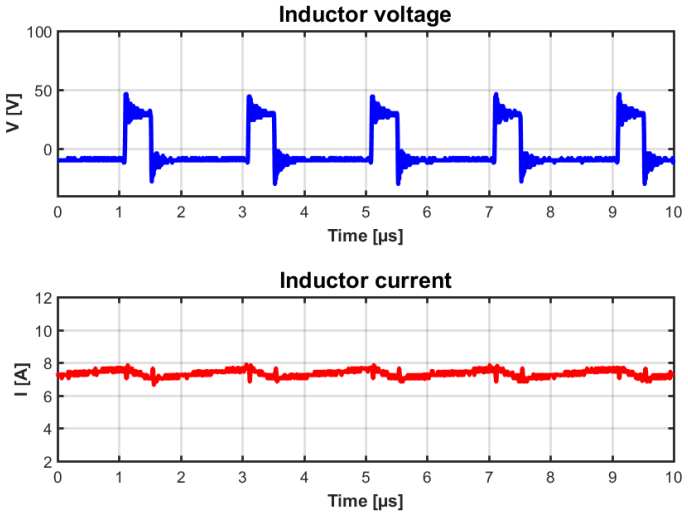

Figure 6.21: V_L and I_L for the GaN measurement with f_{sw}=500 kHz

The waveforms from the measurements are as expected when comparing them to the simulation waveforms in Figure 6.8 and 6.9. On the other hand, the inductor current for both converters is better in the measurements than in the simulations. The appearance of the currents are more similar to the waveforms of the ideal models. The current for the GaN converter has slightly higher peaks than for the Si converter. There are more oscillations in the GaN converter compared to the Si converter, but the oscillations have lower peaks. The current ripple of both converters is not large, this means that the goal of having a current ripple within 10 % in the inductor seems to be achieved. The capacitor voltage and current of the converters are presented in Figure 6.22 and 6.23.

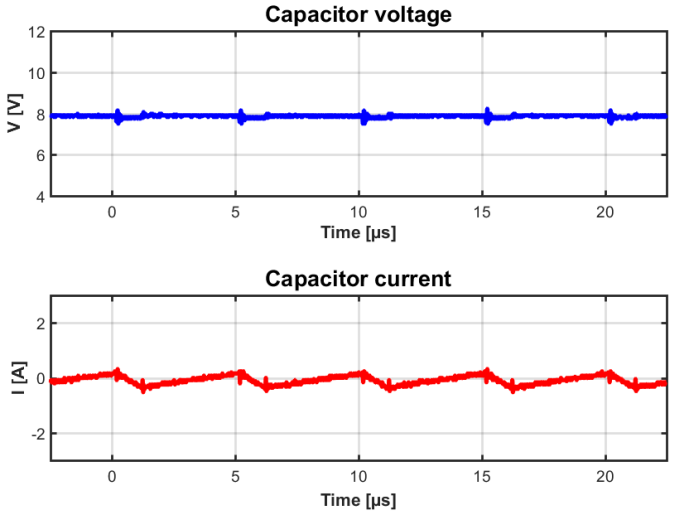

Figure 6.22: V_C and I_C for the Si measurement with f_{sw}=200 kHz

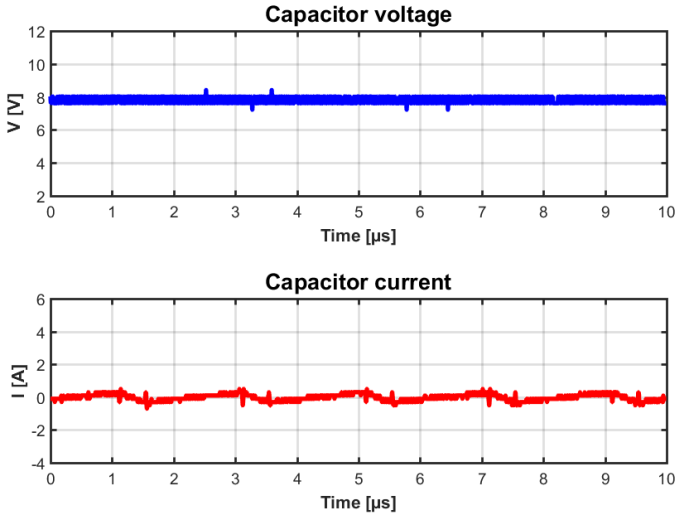

Figure 6.23: V_C and I_C for the GaN measurement with f_{sw}=500 kHz

The behaviour of the capacitor voltage and current is as expected since the voltage ripple for both converters is very small, as can be seen in Figure 6.22 and 6.23. This leads to almost a dc signal which was the purpose of the design of the two converters, to have a voltage ripple of 0.05 %. This small ripple in the capacitor voltage is achieved in the practical design. The current ripple of the capacitor is the same as the current ripple of the inductor, but the inductor has an offset of the output voltage. The small peaks in the capacitor voltage for the two converters is because of the disturbance created from the equipment used in order to measure the voltage and current. In Figure 6.24 and 6.24, the output voltage and current of the converters can be seen.

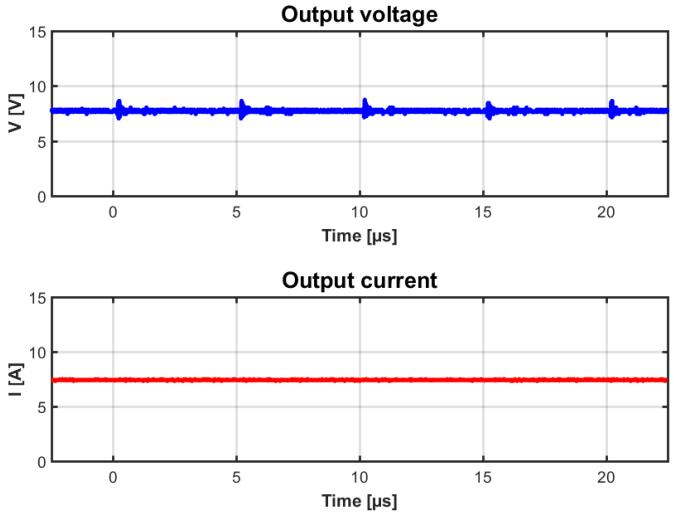

Figure 6.24: V_{out} and I_{out} for the Si measurement with f_{sw}=200 kHz

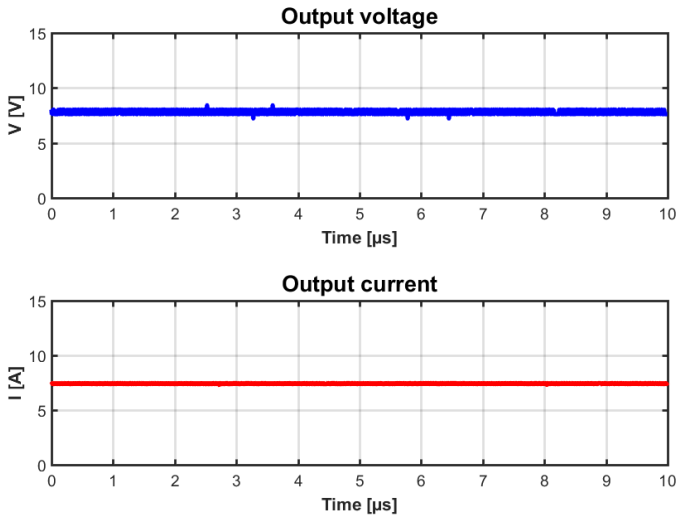

Figure 6.25: V_{out} and I_{out} for the GaN measurement with f_{sw}=500 kHz

The output voltage and current are as expected since the output current should be a dc signal and the the output voltage is designed to have a very small ripple. The output voltage is the same voltage as for the capacitor, this is since the load and the capacitor are in parallel. The reason that the output current is a dc current is due to the LC circuit, before the load, that filter the disturbance and the ripples from the switches.

6.3 Thermal Analysis

In this section the temperature of the circuits, components and the losses of the circuits are evaluated and presented. How the different WBG materials affect the circuits in a thermal aspect are also studied and discussed. The project did not have any temperature restrictions, however if the converter would be used in for example an electrical vehicle it would have such restrictions. The MOSFET components have temperature restrictions, which are described in Appendix C and D. If the MOSFET would exceed its temperature restriction the component would break.

6.3.1 Temperature measurement on the PCB

The temperature of both converters was monitored to evaluate the converters' temperature during operation. The temperature measurements were also monitored to see if the different types of transistor material would have any impact. The equipments used for the temperature measurements were a thermometer and a heat camera. The thermometer wires with heat sensors were placed on the component using electro-lube and heat resistance tape. Heat sinks to decrease the temperature of the MOSFETs even more were used in the converter.

The temperature measurements were performed both with a duty cycle of 24 % and with an adjustable duty cycle. From an ideal perspective, the duty cycle that is set in the function generator should give the calculated voltage. However, in the reality there are losses which means that if the duty cycle always stands at 24 % in the function generator it will not achieve the expected output voltage. In order to achieve the expected output voltage, the duty cycle was therefore adjusted. The duty cycle is calculated according to 2.1, where the theoretical V_{out} is equal to 9.6 V for a duty cycle of 24 %. The measured temperatures for the two converters with f_{sw}=200 kHz and f_{sw}=500 kHz respectively are presented in Table 6.3 and 6.4.

Table 6.3: The measured temperature for the Si converter

V_{out} [V]	**D** [%]	η [%]	**Temp.** $MOSFET_{upper}$ **Heat camera/ Thermometer** [°C]	**Temp.** $MOSFET_{lower}$ **Heat camera/ Thermometer** [°C]	**Temp. L** [°C]
7.94	24	92.96	56.4/55.8	81.5/79	45/44
9.59	28.4	92.85	69.4/67.3	101/98.5	50.5/48.6

Table 6.4: The measured temperature for the GaN converter

V_{out} [V]	**D** [%]	η [%]	**Temp.** $MOSFET_{upper}$ **Heat camera/ Thermometer** [°C]	**Temp.** $MOSFET_{lower}$ **Heat camera/ Thermometer** [°C]	**Temp. L** [°C]
7.99	24	91.92	99.5/102.8	79.1/85.2	64.9/54.9
9.61	28.6	91.52	126/137.1	106/111.2	74.5/64.3

From Appendix C on page 7, it can be seen that the maximum allowed temperature for the Si MOSFET is 175°C. According to Table 6.3 it can been seen that the maximum temperature during operation was 101°C for the lower MOSFET which is a good margin. The reason why the lower MOSFET is warmer then the upper MOSFET is because $I_{avg(ds_{lower})}$ is larger then $I_{avg(ds_{upper})}$ since the lower MOSFET is turned on more in one switching period (24 % for the MOSFET above and 76 % for the MOSFET below).

According to Appendix D on page 2, the maximum allowed temperature for the GaN MOSFET is 150°C. According to Table 6.4 the maximum temperature during operation was 137°C for the upper MOSFET, which is a decent margin. The reason the upper MOSFET had a higher temperature than the lower MOSFET is because of the gate driver circuit did not function properly for the upper MOSFET. In Figure 6.19 it is shown that V_{gs} has both a voltage overshoot and a lot of oscillations for the upper MOSFET compared to the lower MOSFET. This indicates that the gate driver circuit did not function correctly. The reason why the gate driver did not work properly is unkown.

6.3.2 Losses on the PCB

From the temperature measurements it was clear the components that generated most heat were the MOSFETs and the inductor in the converters. This indicates that the highest losses in the circuit were from the MOSFETs and the inductor. In order to calculate the losses for the MOSFETs and the inductor, the components were connected using a Kelvin connection seen in Figure 6.1, while the temperature was measured. The component was applied with a dc current and dc voltage in order to increase its temperature. When the temperature got the same value (see Table 6.3 and 6.4 with D=24 %) as from the measurement when V_{in} was 40 V, the voltage over the component and the current through it was noted. The noted voltage and current are presented in Table 6.5.

Table 6.5: The measured dc voltages and dc current for the temperature measurement

	I_{dc} [**A**]	V_{dc} [**mV**]
L_{Si}	9.03	186.1
L_{GaN}	11.23	137.5
$MOSFET_{upper_{Si}}$	7.7	134.3
$MOSFET_{upper_{GaN}}$	10.64	272.5
$MOSFET_{lower_{Si}}$	9.66	203.3
$MOSFET_{lower_{GaN}}$	9.57	210.1

From the measured voltage and current in Table 6.5, the internal resistance and the total losses for the components under operation were calculated. The total losses for the components were calculated using (2.35) and the internal resistance was calculated using (2.36).

The RMS currents of the MOSFETs and the inductors for both the converters were calculated from the collected data from the measurements of the PCB when the waveforms was studied in Subsection 6.2.2. The RMS currents were calculated using (2.20) and (2.28). With the internal resistances and the measured RMS currents of the components, the conduction losses were calculated according to (2.27) and (2.31). The measured RMS currents, the internal resistances, the losses for the MOSFETs and the losses for the inductors for both the converters are presented in Table 6.6. The switching losses for the MOSFETs can not be measured in practice and can therefore only be estimated according to (2.23) and it is referred to as P_{other} in Table 6.6.

Table 6.6: The losses and the internal resistance for the MOSFET and Inductor

	$P_{loss_{tot}}$ [**W**]	P_{cond} [**W**]	P_{other} [**W**]	DCR / $R_{ds_{on}}$ [**mΩ**]	I_{rms} [**A**]
L_{Si}	1.68	1.09	0.59	20.6	7.28
L_{GaN}	1.54	0.66	0.88	12.2	7.34
$MOSFET_{upper_{Si}}$	1.03	0.16	0.87	17.4	3.02
$MOSFET_{upper_{GaN}}$	2.13	0.20	1.937	22	3.07
$MOSFET_{lower_{Si}}$	1.96	0.20	1.76	21	3.09
$MOSFET_{lower_{GaN}}$	2.07	0.20	1.87	21.2	3.04

P_{other} in Table 6.6 is the difference between $P_{loss_{tot}}$ and P_{cond}. For the inductors, P_{other} represents the magnetization losses and the skin effect losses. From Table 6.6 it is clear the largest part of the losses for the MOSFETs is the switching losses. These switching losses increase with an increasing switching frequency, which is also shown in (2.24). According to Table 6.6 the MOSFET losses are larger than the inductor losses.

6.3.3 Losses from the Simulations

In the parasitic simulation models, the losses for the inductor and the MOSFETs were calculated in order to make a comparison between the simulation model and the practical design. In Table 6.7, the losses of the parasitic simulation models of both converters are presented.

Table 6.7: The losses of the parasitic simulation models

	$P_{loss_{tot}}$ [W]	P_{cond} [W]	P_{other} [W]
L_{Si} [μH]	1.43	1.56	-
L_{GaN} [μH]	0.73	2.44	-
$MOSFET_{upper_{Si}}$ [μF]	0.62	0.34	0.28
$MOSFET_{upper_{GaN}}$ [μF]	2.03	0.43	1.6
$MOSFET_{lower_{Si}}$ [μF]	1.26	1.05	0.21
$MOSFET_{lower_{GaN}}$ [μF]	2.53	1.36	1.17

When comparing the parasitic simulation models with the practical models, it becomes clear that the simulation models do not work correctly when calculating the inductor losses. According to Table 6.7, the conduction losses for both inductors is greater than the total losses of the inductors. This indicate that the I_{rmsL} is higher for the simulation models than for the practical models. Why the simulation models give higher RMS current is unknown, but it could be that there were some problems when measuring the I_L in the models. Figure 6.26 present the schematic from the I_L measurement used in the simulation models. From the figure it can be seen that the ampere meter is measuring the total inductor current through the coil and its parasitic elements. This results in the calculated I_{rmsL} corresponding to the total inductor, including the current through the parasitic capacitor and resistance, instead of the I_{rmsL} through only the coil and the DCR. This I_{rmsL} should be the current used when calculating the conduction losses for the inductor. To move the amperemeter inside the inductor, to measure the current through the DCR, would not be a realistic measurement or good to compare the practical designs with since to measure inside the inductor is impossible in practice.

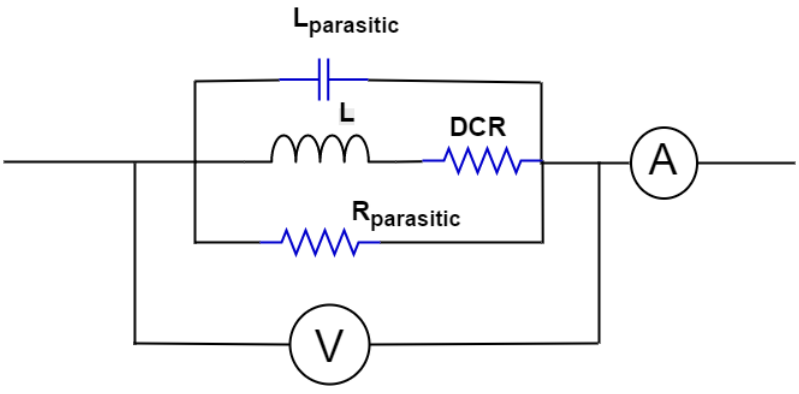

Figure 6.26: I_L measurement from the simulation

When comparing the loss calculations of the MOSFETs from the simulation models in Table 6.6 to the losses from the practical designs in Table 6.7, the losses are similar. However, the simulated conduction losses are larger than the real conduction losses. The reason that the simulation models does not work perfectly for the MOSFET losses could be that the parasitic capacitance in the MOSFET varies with the voltage according to Appendix C on page 7 and Appendix D on page 5. In the simulation models the parasitic capacitance has a fixed value which results in the simulations models not being perfect.

6.4 Interference of the PCB

The converters were tested in order to see how they would work if they were disturbed with a larger metal wire that will increase the magnetic field and stray inductances before and after the MOSFET. In Figure 6.27 and 6.28, the area where the stray inductance is increased before and after the MOSFETs are presented with a red circle. In Table 6.8 the inductance values from the different disturbances before and after the interference are presented.

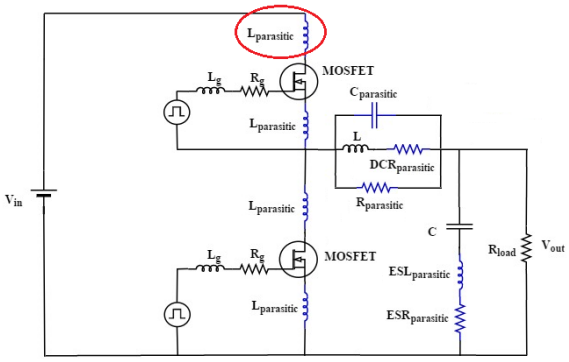

Figure 6.27: Buck converter with larger stray inductance value before the upper MOSFET

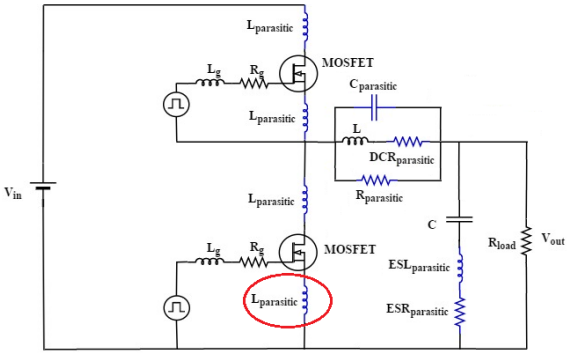

Figure 6.28: Buck converter with larger stray inductance value after the lower MOSFET

Table 6.8: The inductance values from the disturbances

Place of disturbance	**Inductance value [μH]**
Before $MOSFET_{upper_{Si}}$	0.2
After $MOSFET_{lower_{Si}}$	0.192
Before $MOSFET_{upper_{GaN}}$	0.209
After $MOSFET_{lower_{GaN}}$	0.167

6.4.1 Interference before the upper MOSFET

Figure 6.29 and 6.30 show the input voltage and current for both converters when they have been disturbed before the upper MOSFET. The Si converter has a switching frequency of 200 kHz and GaN has a switching frequency of 500 kHz.

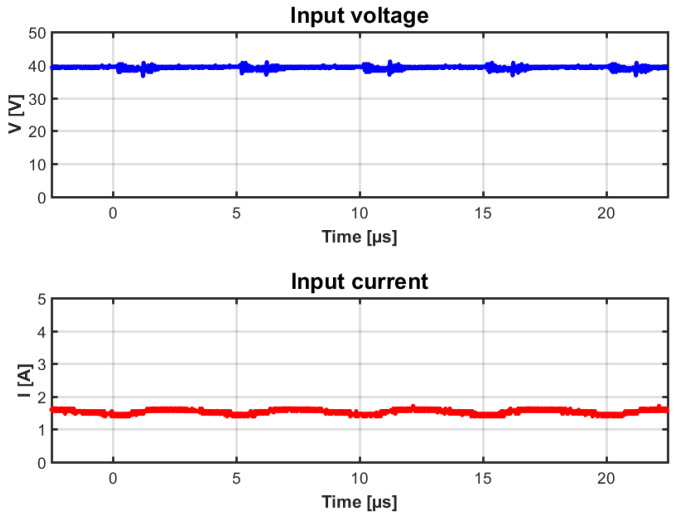

Figure 6.29: V_{in} and I_{in} for the Si measurement with disturbance before the upper MOSFET for f_{sw}=200 kHz

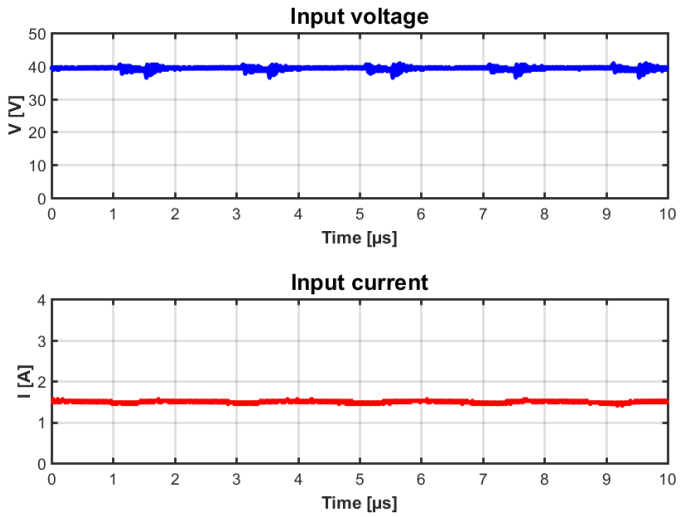

Figure 6.30: V_{in} and I_{in} for the GaN measurement with disturbance before the the upper MOSFET for f_{sw}=500 kHz

In Figure 6.29 and 6.30 there are no signs that the extra inductance from the disturbance affect V_{in} or I_{in}. When comparing the V_{in} or I_{in} with the disturbance, in Figure 6.29 and 6.30, to the V_{in} and I_{in} without the disturbance, in Figure 6.14 and 6.15, they seem to be almost identical. The reason why the circuit was not

affected by the disturbances was that the extra inductance was inserted after the measurement for V_{in} and I_{in}.

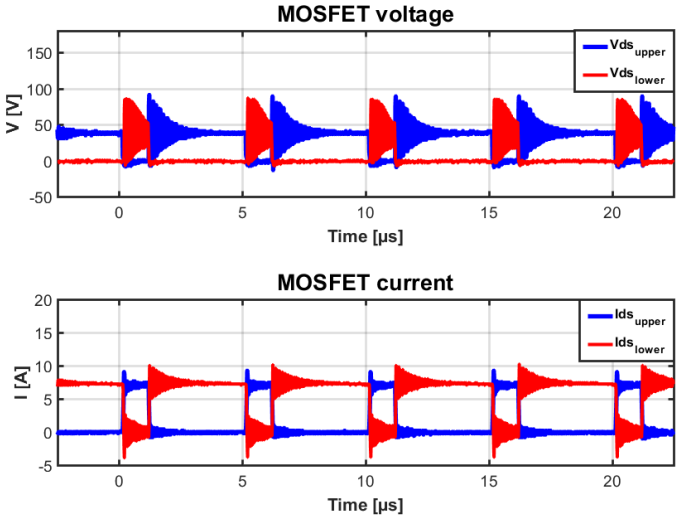

Figure 6.31: V_{ds} and I_{ds} for the Si measurement with disturbance before the upper MOSFET forf_{sw}=200 kHz

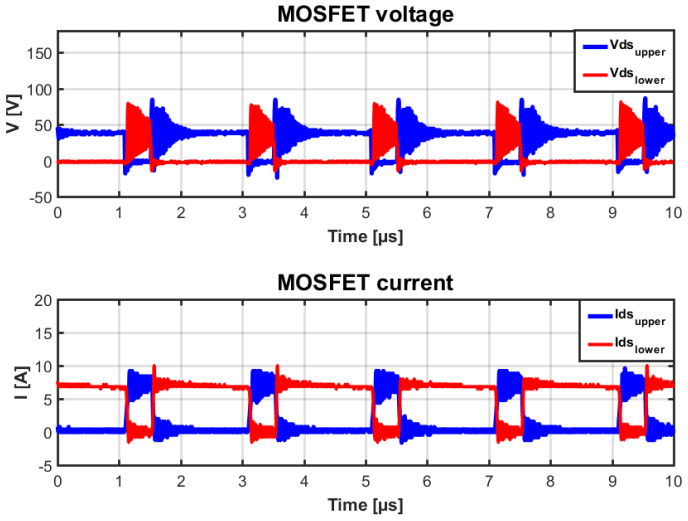

Figure 6.32: V_{ds} and I_{ds} for the GaN measurement with disturbance before the upper MOSFET for f_{sw}=500 kHz

According to Figure 6.31 and 6.32, both MOSFETs in the two circuits are affected by the extra inserted inductance from the disturbance. V_{ds} for both the upper and the lower MOSFET is affected in both converters with more oscillations, which can be seen in Figure 6.31 and 6.32. $V_{ds_{lower}}$ for both Si and GaN consist mostly of oscillations during its on-time. When comparing the Si MOSFET to the GaN MOSFET there is no significant difference in how the Vds is affected for the two materials. The I_{ds} current for both MOSFETs in both converters is affected as well,

with more oscillation during turn-on and turn-off which can be seen in Figure 6.31 and 6.32. For Si the $i_{ds_{lower}}$ has more oscillations than $i_{ds_{upper}}$. But for GaN $i_{ds_{upper}}$ has more oscillations than $i_{ds_{lower}}$. The reason why the i_{ds} appearance differ for the different converters could be that the gate driver do not work properly. The GaN transistor has a low $V_{gs(th)}$ of 1.3 V compared to Si $V_{gs(th)}$ of 4.5 V according to Appendix B on page 3 and Appendix A on page 4. With a low $V_{gs(th)}$ it means that the transistor could be turned on if there where fluctuations in the gate driver that exceeded the $V_{gs(th)}$. This could be a reason as to why there was more oscillation at the $i_{ds_{upper}}$ for GaN compared to Si.

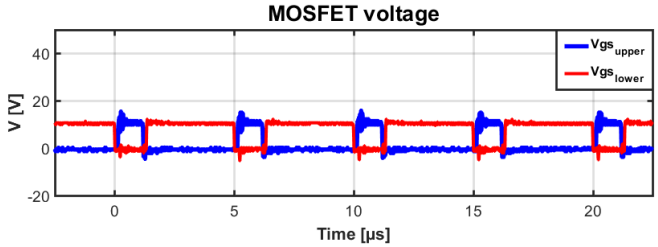

Figure 6.33: V_{gs} for the Si measurement with disturbance before the upper MOSFET for f_{sw}=200 kHz

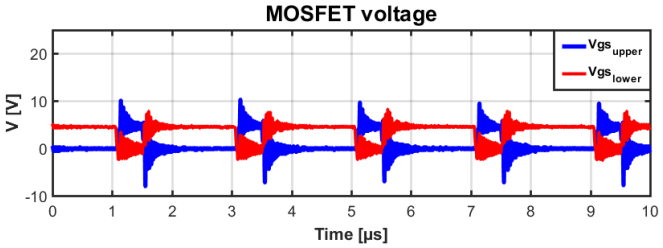

Figure 6.34: V_{gs} for the GaN measurement with disturbance before the upper MOSFET for f_{sw}=500 kHz

Figure 6.33 and 6.34 show how the different gate driver for the two converters is affected by the disturbance. The Si gate driver is not affected that much from the extra inserted inductance except for small oscillations for $V_{gd_{upper}}$, as can be seen in Figure 6.33. This indicates that the gate driver is working properly. The gate driver for GaN however, does not work properly since the disturbance is making $V_{gs_{upper}}$ and $V_{gs_{lower}}$ to oscillate at turn-on and turn-off. These oscillations for V_{gs} is shown in Figure 6.34.

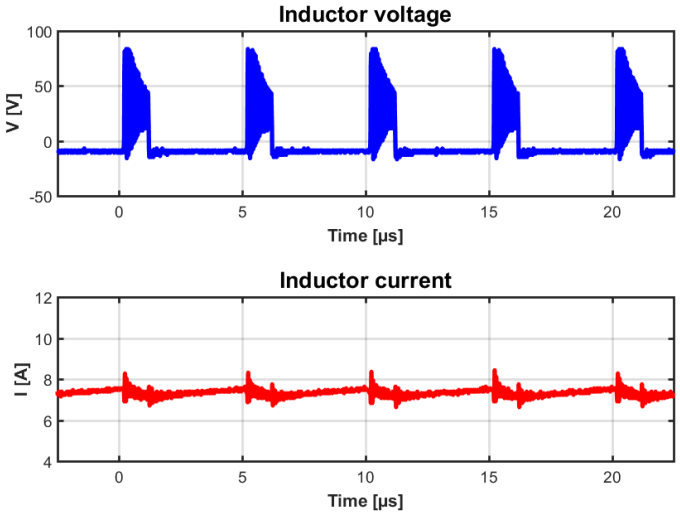

Figure 6.35: V_L and I_L for the Si measurement with disturbance before the upper MOSFET for f_{sw}=200 kHz

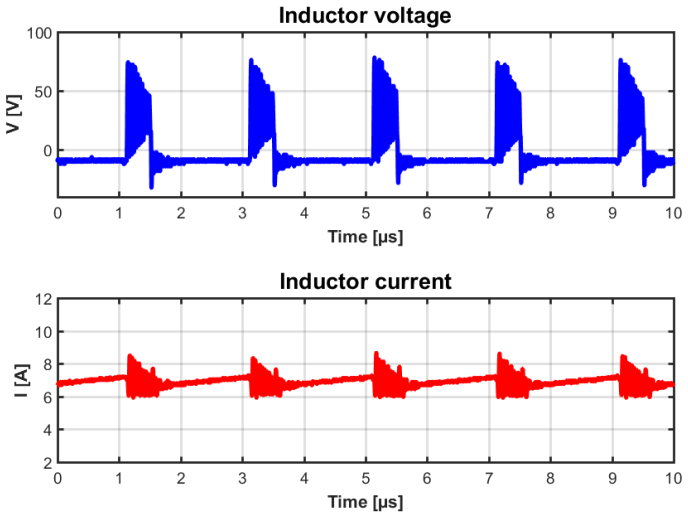

Figure 6.36: V_L and I_L for the GaN measurement with disturbance before the upper MOSFET for f_{sw}=500 kHz

The inductor is affected by the inserted inductance before the upper MOSFET, which can been seen in Figure 6.35 and 6.36. V_L for both Si and GaN consist mostly of oscillations. I_L for GaN is more affected by the disturbance resulting in oscillation at turn-off. I_L for Si is also affected with oscillations during turn-off but in a smaller amount compared to the GaN converter. The reason why V_L consist mostly of oscillations is most likely that the inductor is affected of the MOSFETs. The MOSFET do not work as a filter, so if there are oscillations on this component it would probably transfer to the other components near by, such as the inductor.

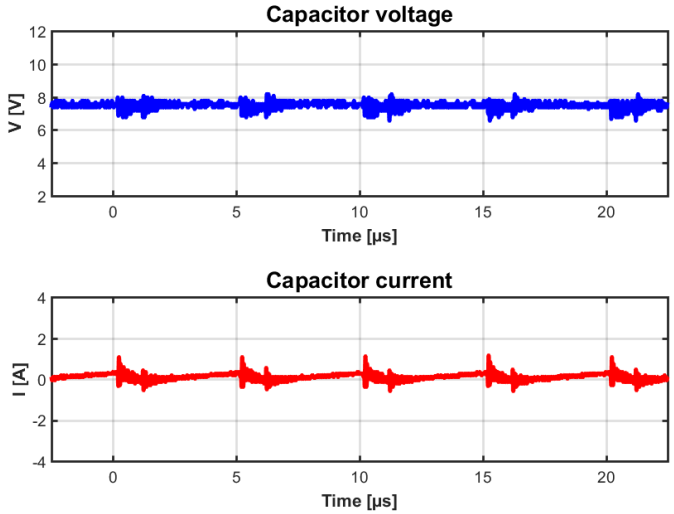

Figure 6.37: V_C and I_C for the Si measurement with disturbance before the upper MOSFET for f_{sw}=200 kHz

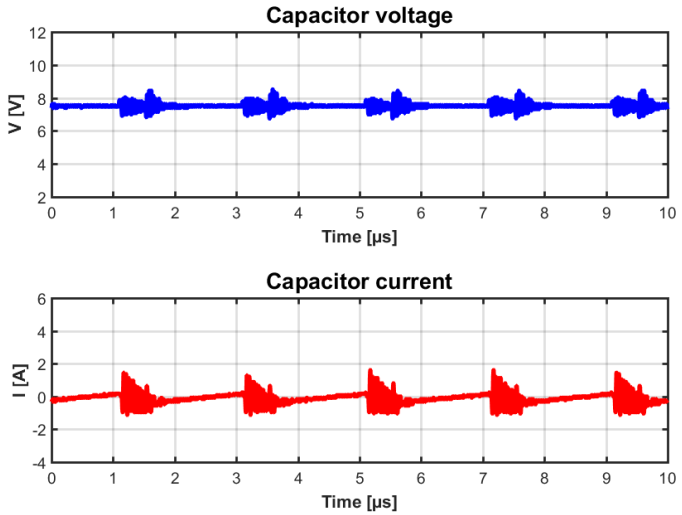

Figure 6.38: V_C and I_C for the GaN measurement with disturbance before the upper MOSFET for f_{sw}=500 kHz

Since I_c is the ripple of I_L, the capacitor is in one sense also affected by the disturbances. The appearance of I_C for both converters, with its oscillations, is shown in Figure 6.37 and 6.38. After the disturbance over the upper MOSFET, the voltage over the output capacitors of the Si converter oscillates more. The V_C for GaN oscillates more than for Si, especially during turn-off. The waveform for $V_{C_{GaN}}$ and $V_{C_{Si}}$ can be obtained from Figure 6.37 and 6.38.

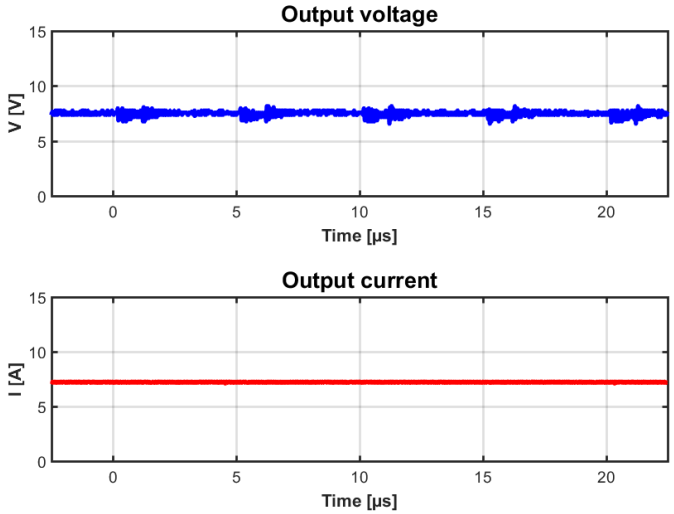

Figure 6.39: V_{out} and I_{out} for the Si measurement with disturbance before the upper MOSFET for f_{sw}=200 kHz

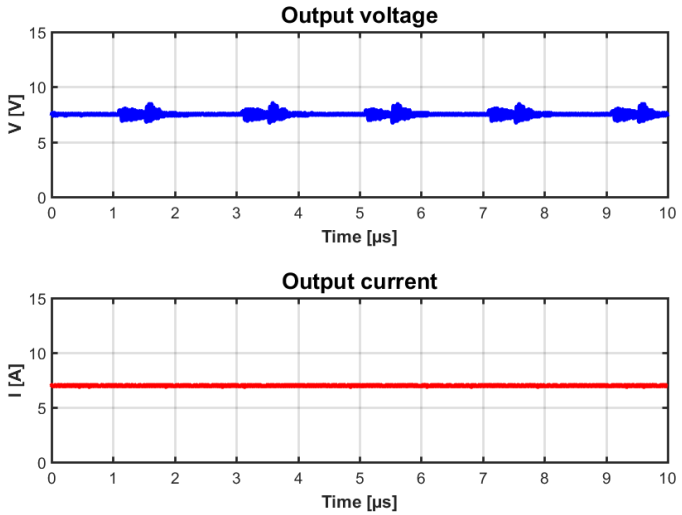

Figure 6.40: V_{out} and I_{out} for the GaN measurement with disturbance before the upper MOSFET for f_{sw}=500 kHz

From Figure 6.39 and 6.40 it is shown that the output current of the converters is not affected by the interference. The output voltage of the converters contain some oscillations, but nothing alarming. The LC circuit, before the load, filter the disturbance and the ripples from the switches which is the reason why there are small or no oscillations on the V_{out} and I_{out}. By studying the waveform from this section and the Table 6.9, both converters are decreasing their efficiency and performance when the circuit is interfered before the upper MOSFET. The GaN converter decrease more in efficiency, with 2.23 % compared to Si with 1.14 % according to Table 6.9. From the appearance of the waveforms in this section, it seems that the GaN converter has slightly lower performance than the Si converter.

The reason for this could be that the GaN converter's gate driver do not work as good as the Si gate driver, which will affect the transistor and the converter as a whole.

6.4.2 Interference after the lower MOSFET

The input voltage and current for the two converters when a longer iron wire was added under the lower MOSFET can be seen in Figure 6.41 and 6.42.

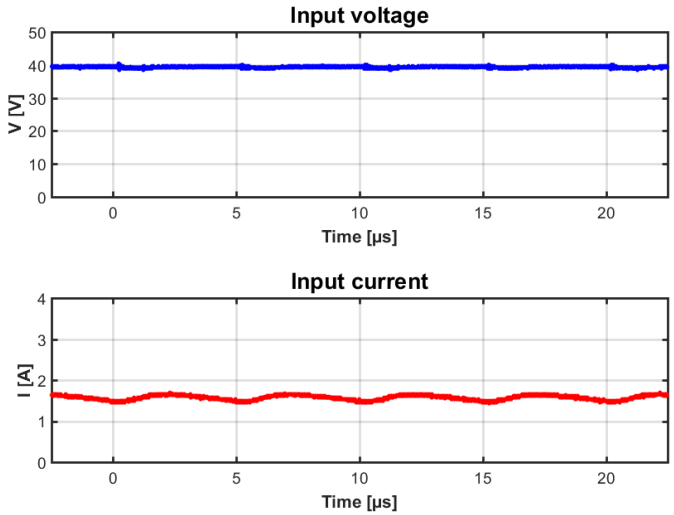

Figure 6.41: V_{in} and I_{in} for the Si measurement with disturbance after the lower MOSFET for f_{sw}=200 kHz

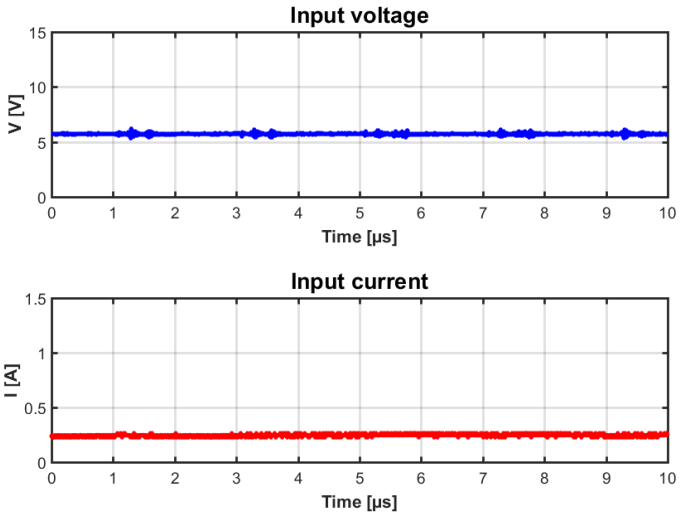

Figure 6.42: V_{in} and I_{in} for the GaN measurement with disturbance after the lower MOSFET for f_{sw}=500 kHz

The input voltage and current for the Si converter was as expected since the converter could handle the input voltage of 40 V, even though the interference in the converter was in place. For the GaN converter it could not reach 40 V, it could only come up to 6 V before it became unstable. This indicates that the gate driver of the GaN converter was not good enough to handle the interference. The Figure 6.43, 6.44, 6.45 and 6.46, show the voltage and current of the MOSFETs.

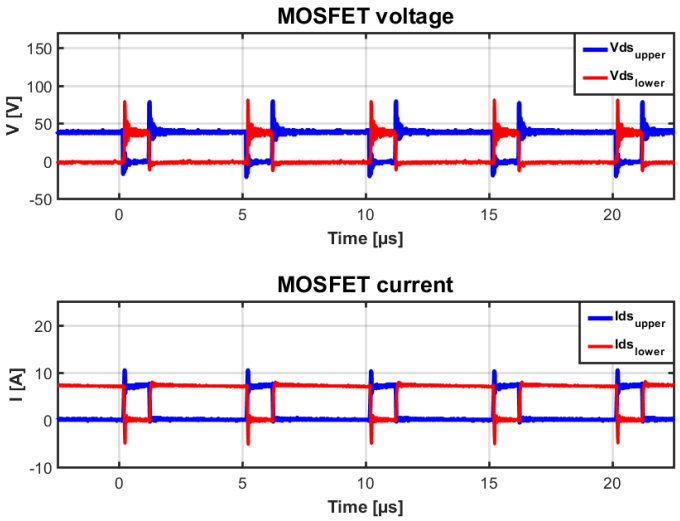

Figure 6.43: V_{ds} and I_{ds} for the Si measurement with disturbance after the lower MOSFET for f_{sw}=200 kHz

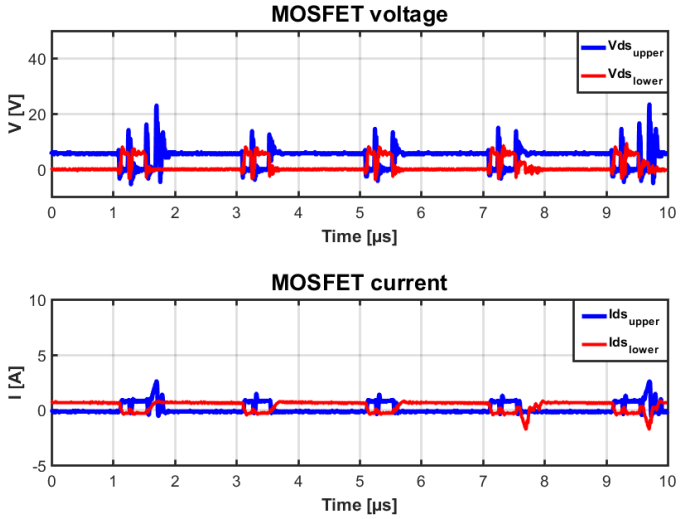

Figure 6.44: V_{ds} and I_{ds} for the GaN measurement with disturbance after the lower MOSFET for f_{sw}=500 kHz

The behaviour of V_{ds} and I_{ds} for the Si converter are as expected, they look the same as they did before the disturbance but with some more oscillations. This is a logic behaviour due to that the stray inductance is larger in the converter which

leads to more oscillations in the circuit. On the other hand, V_{ds} and I_{ds} for the GaN converter do not have this behaviour as can be seen in Figure 6.44. They are both unstable due to the disturbance. Below 6 V the waveforms were good, but at 6 V they get unstable. The efficiency is significantly affected by this behaviour. The efficiency was only 65.12 % as seen in Table 6.9 in the end of this section.

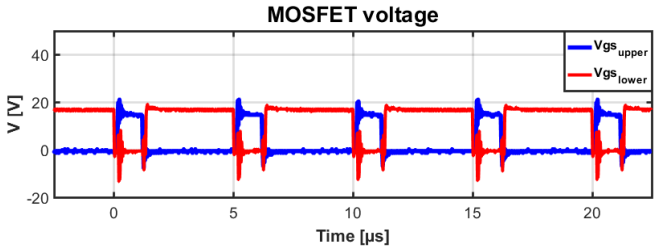

Figure 6.45: V_{gs} for the Si measurement with disturbance after the lower MOSFET for f_{sw}=200 kHz

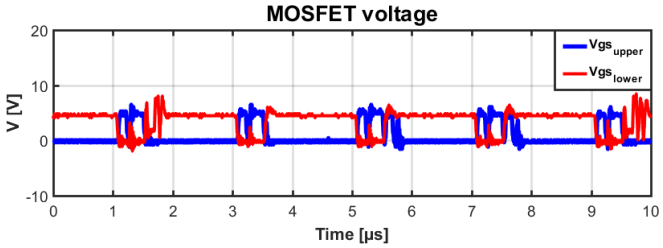

Figure 6.46: V_{gs} for the GaN measurement with disturbance after the lower MOSFET for f_{sw}=500 kHz

In Figure 6.45 and 6.46, V_{gs} for the Si converter is stable, but that is not the case for the GaN converter. The reason for this, as stated earlier, is because the gate driver of GaN could not handle the disturbance below the lower MOSFET. One theory is that a voltage arises between the signals EP and LOL on the IC for the GaN converter, since the EP signal is connected to the ground. This lead to the gate driver not operating as it should. The EP signal is marked with a red circle in Figure 6.47. In the IC for the Si converter, the IC does not have a connection to the ground and therefore no voltage between the signals for the lower MOSFET arises. This means that when the disturbance is added after the lower MOSFET, the gate driver is not affected of it since it is after the gate driver. This results in the disturbance being in series with the inductor instead. The IC of the Si converter is presented in Figure 6.48.

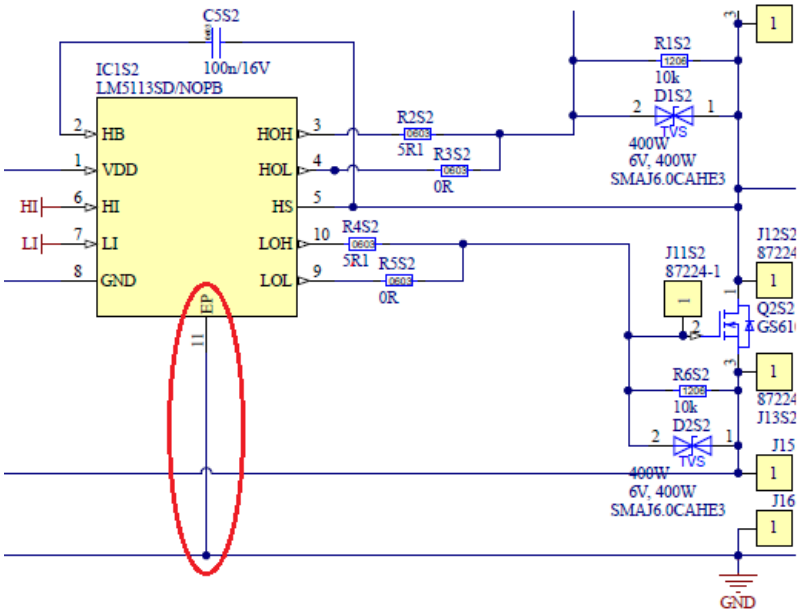

Figure 6.47: The IC for the GaN converter

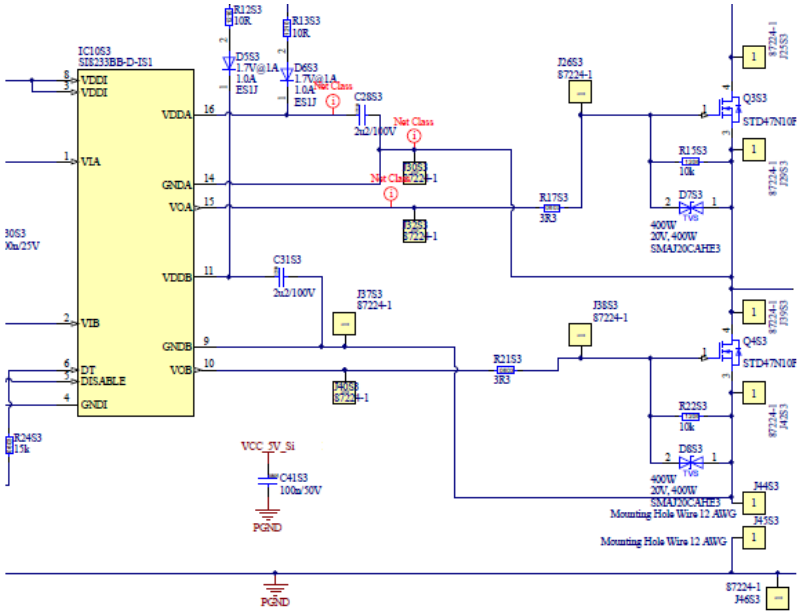

Figure 6.48: The IC for the Si converter

In Figure 6.49 and 6.50, the inductor voltage and current of the two converters can be obtained. The inductor voltage and current of the GaN converter only correspond to an input voltage of 6 V while the Si converter correspond to an input voltage of 40 V (the usual voltage).

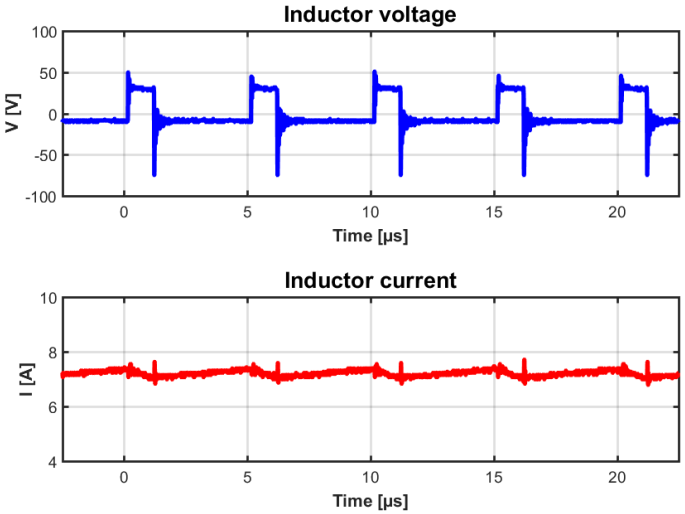

Figure 6.49: V_L and I_L for the Si measurement with disturbance after the lower MOSFET for f_{sw}=200 kHz

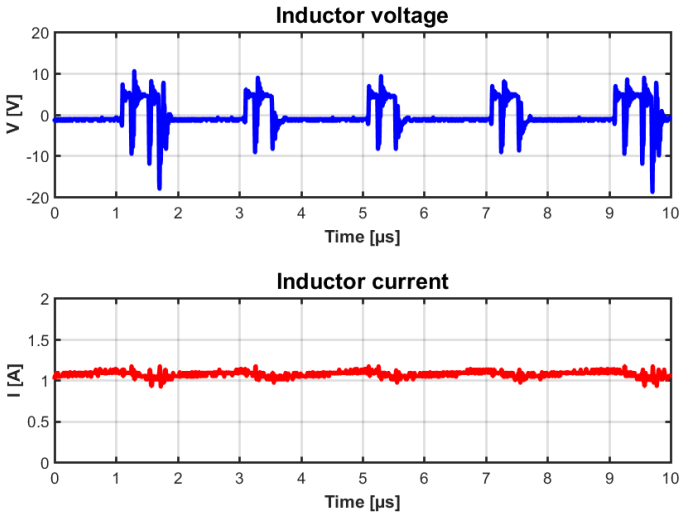

Figure 6.50: V_L and I_L for the GaN measurement with disturbance after the lower MOSFET for f_{sw}=500 kHz

The behaviour of the inductor voltage and current of the Si converter were as expected, with some larger peaks and more oscillations due to the disturbance being connected in series with the inductor. The waveforms of the voltage and current of the inductor for the Si converter are presented in Figure 6.49. On the other hand, the inductor voltage and current of the GaN converter were not expected since the converter could not even operate at 40 , only at input voltages below 6 V. The waveforms of the inductor voltage and current for the GaN converter were unstable at 6 V, which results in unstable signals of the voltage and the current. This can be seen in Figure 6.50, where the waveforms of the voltage and current are not what they should be. If the gate driver was designed to handle these kinds of disturbances,

then the converter could have operated at higher input voltages. The gate driver has the largest effect on the performance of the converter. Therefore, the design of the gate driver should be in focus when designing converters. In Figure 6.51 and 6.52, the voltage and current of the capacitor for both the converters are presented.

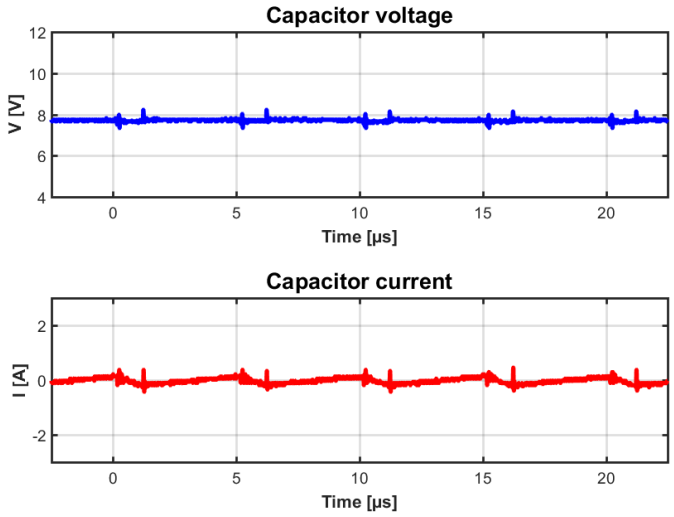

Figure 6.51: V_C and I_C for the Si measurement with disturbance after the lower MOSFET for f_{sw}=200 kHz

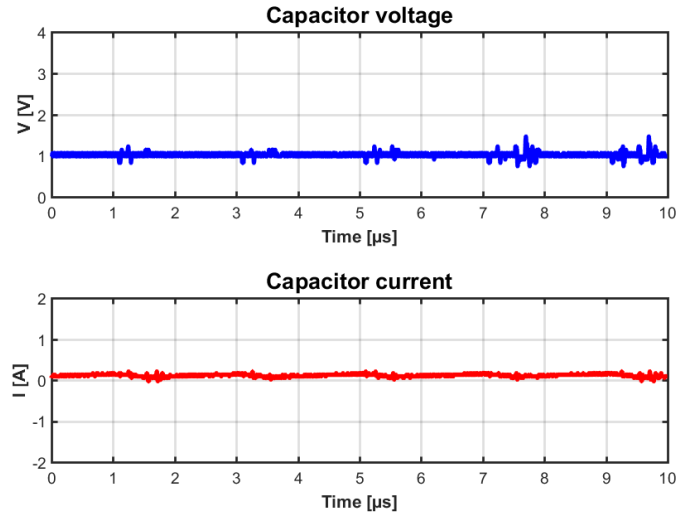

Figure 6.52: V_C and I_C for the GaN measurement with disturbance after the lower MOSFET for f_{sw}=500 kHz

The waveforms of the voltage and current of the Si converter are reasonable since they are the same as the capacitor voltage before the disturbances as seen in Figure 6.22. The only difference is that they have larger peaks and more oscillations, which is reasonable since there is more stray inductance in the PCB. The waveforms of the GaN converter on the other hand are not reasonable, since they are unstable

due to the interference in the PCB and the gate driver not being able to handle the disturbance. In Figure 6.53 and 6.54, the output voltage and current of the converters are presented.

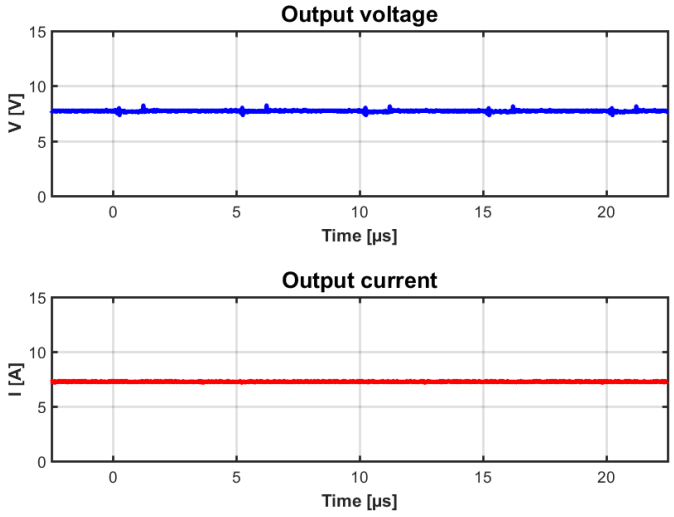

Figure 6.53: V_{out} and I_{out} for the Si measurement with disturbance after the lower MOSFET for f_{sw}=200 kHz

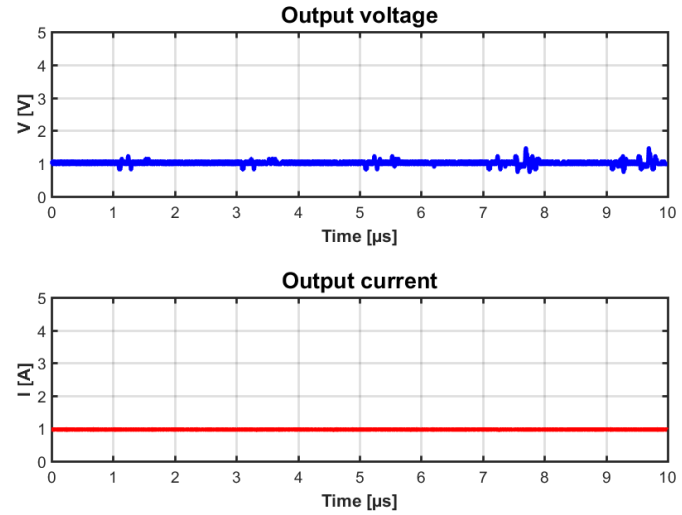

Figure 6.54: V_{out} and I_{out} for the GaN measurement with disturbance after the lower MOSFET for f_{sw}=500 kHz

Figure 6.53 shows that the behaviour of the output voltage and current for the Si converter were as expected. This is since the output voltage was the same as the capacitor voltage and the output current was a dc current. The output current for the GaN converter was also reasonable (dc current), but with a lower value due to the low input voltage (6 V). The reason that the output current was a dc current is because of the LC circuit before the load, which filter the disturbance

and the ripples from the switches. However, the output voltage fluctuates since the converter was unstable at 6 V and above. In Table 6.9 the efficiency before and after the interference are presented.

Table 6.9: The efficiency before and after the addition of disturbances for the two converters, with an input voltage of 40 V

Semiconductor	**Efficiency before disturbance** [%]	**Efficiency before MOSFET upper** [%]	**Efficiency after MOSFET below** [%]
Si	92.96	91.82	92.18
GaN	91.92	89.69	65.12

Table 6.9 show how the efficiency, after the addition of disturbances, of the Si converter decreased around 1 % both when it was added before the upper MOSFET and after the lower MOSFET. For the GaN converter the efficiency decreased around 1 % when the disturbance was added before the upper MOSFET and around 25 % when it was added after the lower MOSFET. The reason for the large drop is that the converter only had an input voltage of 6 V since the GaN converter got unstable after 6 V. With low input voltage the efficiency is lower, but the most significant effect on the efficiency was that the gate driver could not handle the disturbance and could not operate as it should.

6.5 Comparison between the Simulation Models and the PCB

The measurements of the practical design show that the gate driver for the GaN converter does not perform as good as the gate driver for the Si converter. A gate driver is sensitive to inductance and it is therefore important to have a compact design between the gate driver and the transistor it should drive. However, in Table 6.2 it is clear that the inductance around the gate driver and the MOSFETs is higher for the Si converter than for the GaN converter. Although the inductance is higher for the Si converter, its gate driver performs better. One reason that the gate driver for the GaN converter does not perform as well as the Si converter could be that it is not as robust. Another reason could be that the GaN transistor has a lower $Vgs(th)$ than the Si transistor which results in that the GaN transistor could be turned on more easily when there are fluctuations from the gate driver signal to the gate terminal.

The study of the waveforms and the efficiency from both the measurements and the simulations implies that the Si converter has better performance. However, the GaN converter operates at higher f_{sw} than the Si converter and with only a small difference in efficiency. Even though the gate driver of the GaN converter is not

as robust as the Si converter, the aspect of the GaN converter operating at higher switching frequencies and without interference makes the performance decent. This is mainly since it has a smaller sized converter.

When comparing the simulation model to the practical design they seem similar. However, the simulation model does not work perfectly due to its error in its losses calculations. The efficiency of the converters in the simulation models and the practical design differ. One reason for this could be the error in the loss calculation part of the simulation models. Other reasons could be more disturbances in the surrounding for the practical designs and the soldering of the components are not perfectly attached to the PCB. The results of the efficiency for both the simulated converters with the parasitic elements and the real converters for 40 V are presented in Table 6.10.

Table 6.10: Efficiency for both the simulated and the practical converters at input voltage of 40 V

MOSFET	**Efficiency,** η **simplified model** [%]	**Efficiency,** η **simulated** [%]	**Efficiency,** η **measured** [%]
Si (200 kHz)	99.9	96.24	92.96
GaN (500 kHz)	99.9	93.37	91.92

The reason the efficiency of the simplified models are not 100 %, which it should be is because of the switch block in MATLAB. The switch block was not ideal, since $R_{ds(on)}$ could not be set to zero, but it had a really small value or otherwise MATLAB gave an error.

7

Conclusion

An investigation between Wide Band Gap (WBG) transistors and silicon (Si) transistors was performed to investigate characteristics, materials, and best practice usage of different WBG transistors. Two small, compact dc/dc converters with Si and gallium nitride (GaN) transistors respectively were designed and constructed. The investigation showed that having GaN transistors instead of Si transistors looks promising, in the absence of disturbances. The difference in results between having GaN and Si transistors is almost the same, it only differs 1 % in efficiency. The major difference between them is that GaN can operate at higher switching frequency which leads to smaller components, less weight, more compact converter etc.

When comparing the simulations and the practical design, it is more important for the gate driver in the GaN converter to be as tight and as close to the transistors as possible. It is more important for the GaN converter than for the Si converter since the GaN converter is more sensitive regarding that area. One of the reasons that the GaN converter is more sensitive is because of its low V_{th} value in the transistor (1.3 V), while the V_{th} value for Si is 4.5 V. The lower the V_{th} value is, it results in the transistors switching on more easily. This in turn leads to more fluctuation in the gate terminal to the transistor. All these factors makes the GaN converter more sensitive to disturbances since its operation is not optimal. For the Si converter the V_{th} value was higher, which resulted in a more robust gate driver, transistors and design.

Regarding using SiC, the investigation concluded that the SiC today is not applicable for low voltage applications. Converters with GaN transistors have a great potential for future use in power electronic applications. Si is more robust then GaN, but if GaN is made more robust with an improved gate driver, then GaN is more desirable for power electronic applications. This is because it can operate at much higher switching frequencies.

7.1 Future Work

Future work on this thesis would be to improve the gate driver for the GaN converter and make it more robust to interference in the PCB. Also to have a tighter

construction in the PCB both for the Si and the GaN converter, especially between the gate driver and the transistors. It is more necessary for the GaN converter since it was not as robust as the Si converter when interference was added to the PCB. This would improve the performance of both converters. To also have no inductance at all, or at least very small, before the upper MOSFET is desirable. In order to achieve that, a tighter construction between the four capacitors (10 μF and 47 μF that filter the input current and makes it a dc current) and the first MOSFET could be implemented. With tighter constructions it leads to less stray inductance and the converter having less losses.

In order to reduce the overvoltage that occurred when the switch turned off, overvoltage snubbers for both transistors need to be designed. Another solution for the overvoltage is to increase the gate resistance (R_g) in the gate driver. When increasing R_g the rise time increases, which leads to the current derivative increasing and it takes longer time for the switch to turn off. This results in the voltage not increasing that drastically.

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A

Appendix: Datasheet of the IC for the Gate Driver of the Si Transistors

5. Applications

The following examples illustrate typical circuit configurations using the Si823x.

5.1 High-Side/Low-Side Driver

The Figure A in the drawing below shows the Si8230/3 controlled using the VIA and VIB input signals, and Figure B shows the Si8231/4 controlled by a single PWM signal.

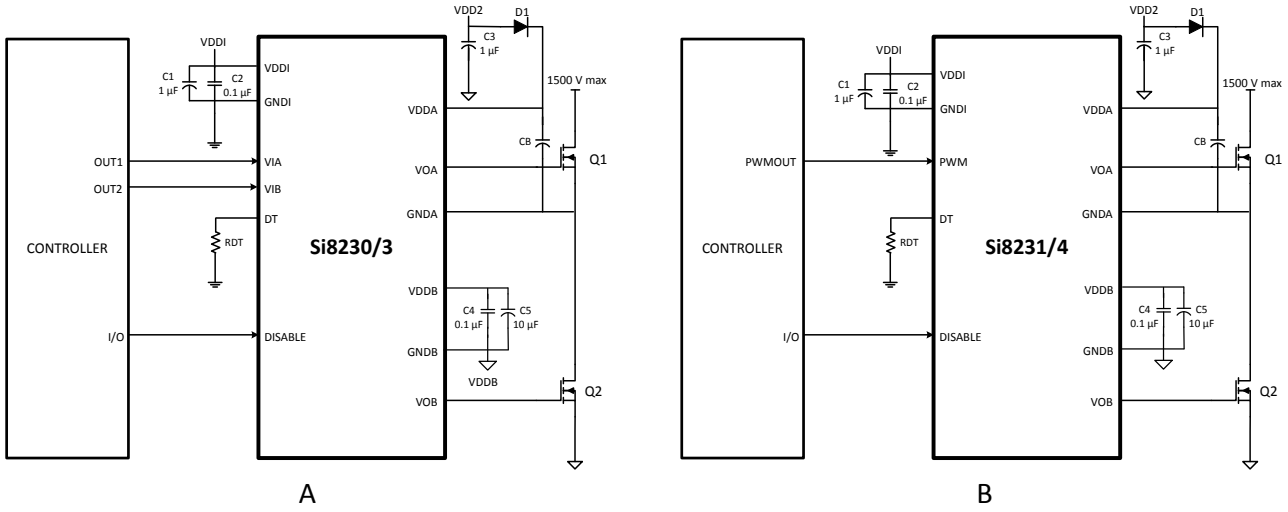


Figure 5.1. Si823x in Half-Bridge Application

For both cases, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. The boot-strap start up time will depend on the CB cap chosen. See application note, “AN486: High-Side Bootstrap Design Using Si823x ISODrivers in Power Delivery Systems”. VOB is connected as a conventional low-side driver, and, in most cases, VDD2 is the same as VDDB. Note that the input side of the Si823x requires VDD in the range of 4.5 to 5.5 V (2.7 to 5.5 V for Si8237/8), while the VDDA and VDDB output side supplies must be between 6.5 and 24 V with respect to their respective grounds. It is recommended that bypass capacitors of 0.1 and 1 µF value be used on the Si823x input side and that they be located as close to the chip as possible. Moreover, it is recommended that 0.1 and 10 µF bypass capacitors, located as close to the chip as possible, be used on the Si823x output side to reduce high-frequency noise and maximize performance.

5.2 Dual Driver

The figure below shows the Si823x configured as a dual driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 1500 V dc between them.

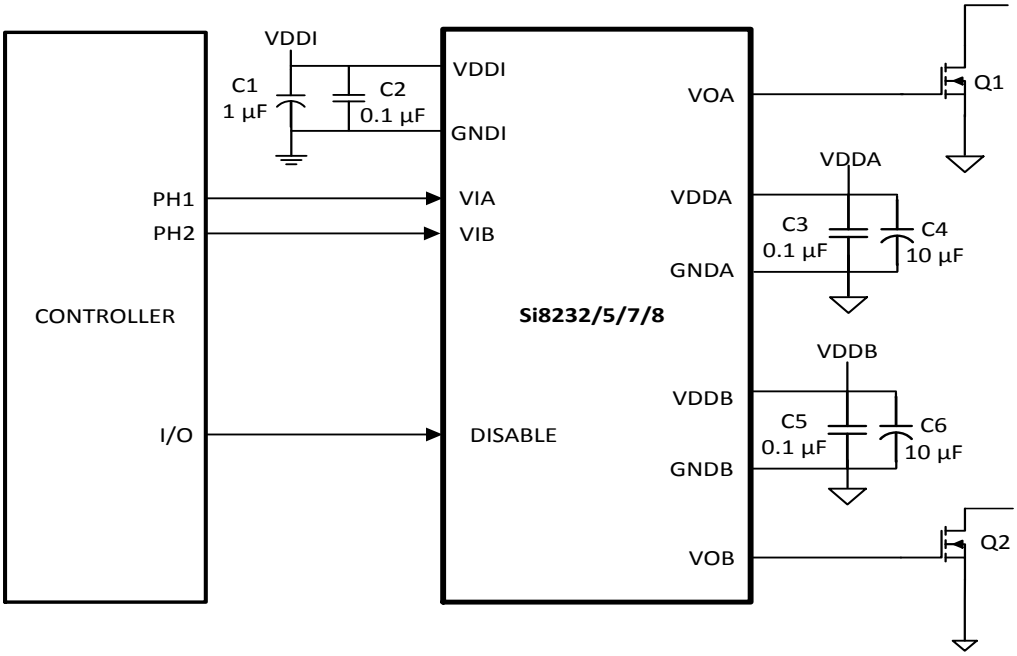


Figure 5.2. Si8232/5/7/8 in a Dual Driver Application

Because each output driver resides on its own die, the relative voltage polarities of VOA and VOB can reverse without damaging the driver. That is, the voltage at VOA can be higher or lower than that of VOB by VDD without damaging the driver. Therefore, a dual driver in a low-side high side/low side drive application can use either VOA or VOB as the high side driver. Similarly, a dual driver can operate as a dual low-side or dual high-side driver and is unaffected by static or dynamic voltage polarity changes.

5.3 Dual Driver with Thermally Enhanced Package (Si8236)

The thermal pad of the Si8236 must be connected to a heat spreader to lower thermal resistance. Generally, the larger the thermal shield's area, the lower the thermal resistance. It is recommended that thermal vias also be used to add mass to the shield. Vias generally have much more mass than the shield alone and consume less space, thus reducing thermal resistance more effectively. While the heat spreader is not generally a circuit ground, it is a good reference plane for the Si8236 and is also useful as a shield layer for EMI reduction.

With a 10mm^2 thermal plane on the outer layers (including 20 thermal vias), the thermal impedance of the Si8236 was measured at 50 °C/W. This is a significant improvement over the Si8235 which does not include a thermal pad. The Si8235's thermal resistance was measured at 105 °C /W. In addition, note that the GNDA and GNDB pins for the Si8236 are connected together through the thermal pad.

6. Pin Descriptions

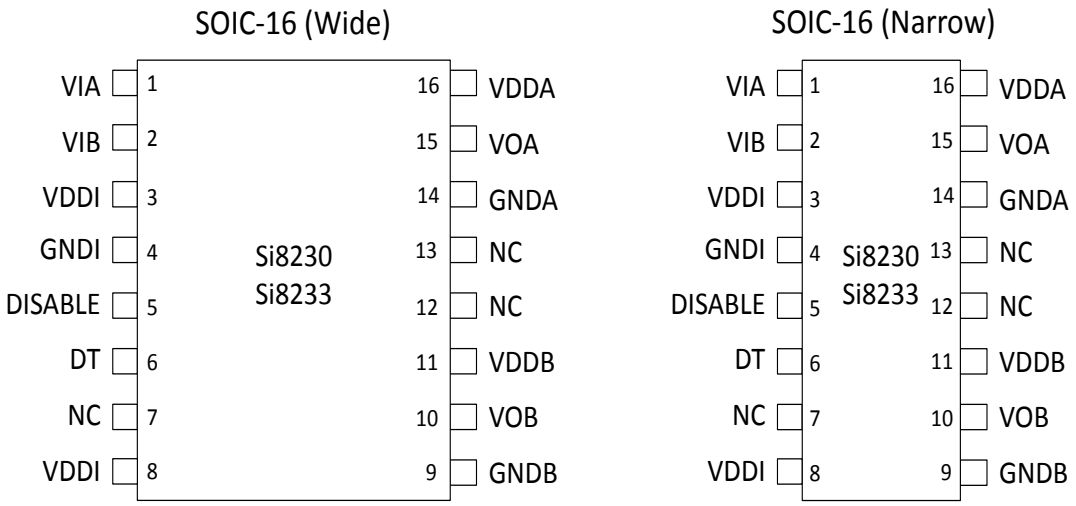


Table 6.1. Si8230/3 Two-Input HS/LS Isolated Driver (SOIC-16)

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 3.10 Programmable Dead Time and Overlap Protection).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

B

Appendix: Datasheet of the IC for the Gate Driver of the GaN Transistors

LM5113 100 V 1.2-A / 5-A, Half-Bridge Gate Driver for Enhancement Mode GaN FETs

1 Features

- Independent High-Side and Low-Side TTL Logic Inputs
- 1.2 A / 5 A Peak Source / Sink Current
- High-Side Floating Bias Voltage Rail Operates up to 100 VDC
- Internal Bootstrap Supply Voltage Clamping
- Split Outputs for Adjustable Turn-on/Turn-off Strength
- 0.6 Ω / 2.1 Ω Pull-down/Pull-up Resistance
- Fast Propagation Times (28 ns Typical)
- Excellent Propagation Delay Matching (1.5 ns Typical)
- Supply Rail Under-Voltage Lockout
- Low Power Consumption

2 Applications

- Current Fed Push-Pull Converters
- Half and Full-Bridge Converters
- Synchronous Buck Converters
- Two-Switch Forward Converters
- Forward with Active Clamp Converters

3 Description

The LM5113 is designed to drive both the high-side and the low-side enhancement mode Gallium Nitride (GaN) FETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of driving a high-side enhancement mode GaN FET operating up to 100 V. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.2 V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The inputs of the LM5113 are TTL logic compatible, and can withstand input voltages up to 14 V regardless of the VDD voltage. The LM5113 has split gate outputs, providing flexibility to adjust the turn-on and turn-off strength independently.

In addition, the strong sink capability of the LM5113 maintains the gate in the low state, preventing unintended turn-on during switching. The LM5113 can operate up to several MHz. The LM5113 is available in a standard WSON-10 pin package and a 12-bump DSBGA package. The WSON-10 pin package contains an exposed pad to aid power dissipation. The DSBGA package offers a compact footprint and minimized package inductance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5113	WSON (10)	4.00 mm × 4.00 mm
	DSBGA (12)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Diagram

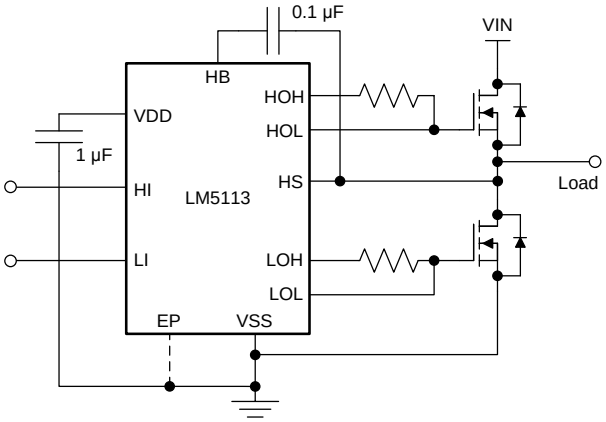


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2013) to Revision G — **Page**

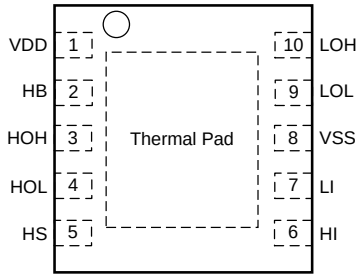
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision E (April 2013) to Revision F — **Page**

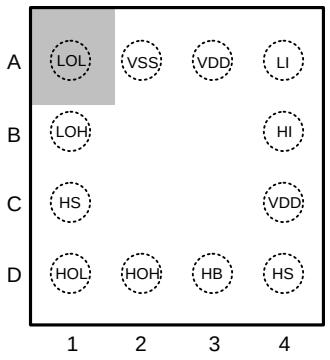
- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

DPR Package
10-Pin WSON With Exposed Thermal Pad
Top View



YFX Package
12-Pin DSBGA
Top View



Pin Functions

PIN			TYPE (1)	DESCRIPTION
NAME	WSON	DSBGA		
VDD	1	A3, C4 (2)	P	5 V Positive gate drive supply: locally decouple to VSS using low ESR/ESL capacitor located as close to the IC as possible.
HB	2	D3	P	High-side gate driver bootstrap rail: connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to the IC as possible.
HOH	3	D2	O	High-side gate driver turn-on output: connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turn-on speed.
HOL	4	D1	O	High-side gate driver turn-off output: connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turn-off speed.
HS	5	C1, D4 (2)	P	High-side GaN FET source connection: connect to the bootstrap capacitor negative terminal and the source of the high-side GaN FET.
HI	6	B4	I	High-side driver control input. The LM5113 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
LI	7	A4	I	Low-side driver control input. The LM5113 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
VSS	8	A2	G	Ground return: all signals are referenced to this ground.
LOL	9	A1	O	Low-side gate driver sink-current output: connect to the gate of the low-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turn-off speed.
LOH	10	B1	O	Low-side gate driver source-current output: connect to the gate of high-side GaN FET with a short, low inductance path. A gate resistor can be used to adjust the turn-on speed.
	EP			Exposed pad: TI recommends that the exposed pad on the bottom of the package be soldered to ground plane on the PC board to aid thermal dissipation.

(1) I = Input, O = Output, G = Ground, P = Power
(2) A3 and C4, C1 and D4 are internally connected

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VDD to VSS	–0.3	7	V
HB to HS	–0.3	7	V
LI or HI input	–0.3	15	V
LOH, LOL output	–0.3	VDD +0.3	V
HOH, HOL output	V_{HS} – 0.3	V_{HB} +0.3	V
HS to VSS	–5	100	V
HB to VSS	0	107	V
HB to VDD	0	100	V
Operating junction temperature		150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VDD	4.5		5.5	V
LI or HI input	0		14	V
HS	–5		100	V
HB	V_{HS} + 4		V_{HS} + 5.5	V
HS slew rate			50	V/ns
Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM5113		UNIT
		DPR (WSON)	YFX (DSBGA)	
		10 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.5	76.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	12.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.9	12.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Specifications are T_J = 25°C. Unless otherwise specified: V_{DD} = V_{HB} = 5 V, V_{SS} = V_{HS} = 0 V.
No load on LOL and HOL or HOH and HOL(1).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I_{DD}	VDD quiescent current	LI = HI = 0 V	T_J = 25°C		0.07		mA
			T_J = –40°C to 125°C			0.1	
I_{DDO}	VDD operating current	f = 500 kHz	T_J = 25°C		2.0		mA
			T_J = –40°C to 125°C			3.0	
I_{HB}	Total HB quiescent current	LI = HI = 0 V	T_J = 25°C		0.08		mA
			T_J = –40°C to 125°C			0.1	
I_{HBO}	Total HB operating current	f = 500 kHz	T_J = 25°C		1.5		mA
			T_J = –40°C to 125°C			2.5	
I_{HBS}	HB to VSS quiescent current	HS = HB = 100 V	T_J = 25°C		0.1		µA
			T_J = –40°C to 125°C			8	
I_{HBSO}	HB to VSS operating current	f = 500 kHz	T_J = 25°C		0.4		mA
			T_J = –40°C to 125°C			1.0	
INPUT PINS							
V_{IR}	Input voltage threshold	Rising edge	T_J = 25°C		2.06		V
			T_J = –40°C to 125°C	1.89		2.18	
V_{IF}	Input voltage threshold	Falling edge	T_J = 25°C		1.66		V
			T_J = –40°C to 125°C	1.48		1.76	
V_{IHYS}	Input voltage hysteresis				400		mV
R_I	Input pulldown resistance	T_J = 25°C			200		kΩ
		T_J = –40°C to 125°C		100		300	
UNDER VOLTAGE PROTECTION							
V_{DDR}	VDD rising threshold	T_J = 25°C			3.8		V
		T_J = –40°C to 125°C		3.2		4.5	
V_{DDH}	VDD threshold hysteresis				0.2		V
V_{HBR}	HB rising threshold	T_J = 25°C			3.2		V
		T_J = –40°C to 125°C		2.5		3.9	
V_{HBH}	HB threshold hysteresis				0.2		V
BOOTSTRAP DIODE							
V_{DL}	Low-current forward voltage	I_{VDD-HB} = 100 µA	T_J = 25°C		0.45		V
			T_J = –40°C to 125°C			0.65	
V_{DH}	High-current forward voltage	I_{VDD-HB} = 100 mA	T_J = 25°C		0.90		V
			T_J = –40°C to 125°C			1.00	
R_D	Dynamic resistance	I_{VDD-HB} = 100 mA	T_J = 25°C		1.85		Ω
			T_J = –40°C to 125°C			3.60	
	HB-HS clamp	Regulation voltage	T_J = 25°C		5.2		V
			T_J = –40°C to 125°C	4.7		5.45	

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Specifications are T_J = 25°C. Unless otherwise specified: V_{DD} = V_{HB} = 5 V, V_{SS} = V_{HS} = 0 V.
No load on LOL and HOL or HOH and HOL(1).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LOW & HIGH SIDE GATE DRIVER							
V_{OL}	Low-level output voltage	I_{HOL} = I_{LOL} = 100 mA	T_J = 25°C		0.06		V
			T_J = –40°C to 125°C			0.10	
V_{OH}	High-level output voltage V_{OH} = VDD – LOH or V_{OH} = HB – HOH	I_{HOH} = I_{LOH} = 100 mA	T_J = 25°C		0.21		V
			T_J = –40°C to 125°C			0.31	
I_{OHL}	Peak source current	HOH, LOH = 0 V			1.2		A
I_{OLL}	Peak sink current	HOL, LOL = 5 V			5		A
I_{OHLK}	High-level output leakage current	HOH, LOH = 0 V	T_J = –40°C to 125°C			1.5	µA
I_{OLLK}	Low-level output leakage current	HOL, LOL = 5 V	T_J = –40°C to 125°C			1.5	µA

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{LPHL}	LO turn-off propagation delay	LI falling to LOL falling	T_J = 25°C		26.5		ns
			T_J = –40°C to 125°C			45.0	
t_{LPLH}	LO turn-on propagation delay	LI rising to LOH rising	T_J = 25°C		28.0		ns
			T_J = –40°C to 125°C			45.0	
t_{HPHL}	HO turn-off propagation delay	HI falling to HOL falling	T_J = 25°C		26.5		ns
			T_J = –40°C to 125°C			45.0	
t_{HPLH}	HO Turn-on propagation delay	HI rising to HOH rising	T_J = 25°C		28.0		ns
			T_J = –40°C to 125°C			45.0	
t_{MON}	Delay matching LO on & HO off	T_J = 25°C			1.5		ns
		T_J = –40°C to 125°C				8.0	
t_{MOFF}	Delay matching LO off & HO on	T_J = 25°C			1.5		ns
		T_J = –40°C to 125°C				8.0	
t_{HRC}	HO rise time (0.5 V – 4.5 V)	C_L = 1000 pF			7.0		ns
t_{LRC}	LO rise time (0.5 V – 4.5 V)	C_L = 1000 pF			7.0		ns
t_{HFC}	HO fall time (0.5 V – 4.5 V)	C_L = 1000 pF			1.5		ns
t_{LFC}	LO fall time (0.5 V – 4.5 V)	C_L = 1000 pF			1.5		ns
t_{PW}	Minimum input pulse width that changes the output				10		ns
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, I_R = 100 mA			40		ns

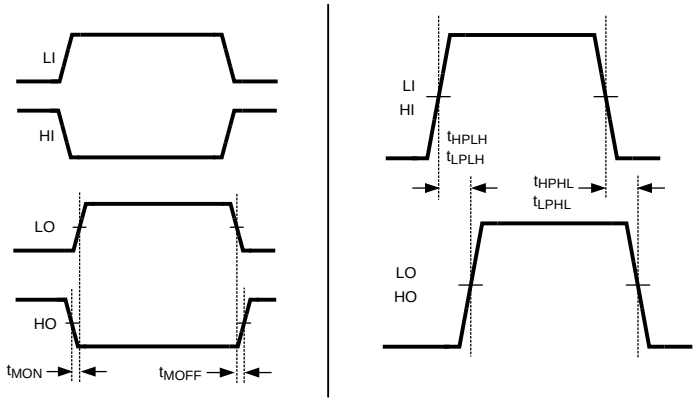


Figure 1. Timing Diagram

6.7 Typical Characteristics

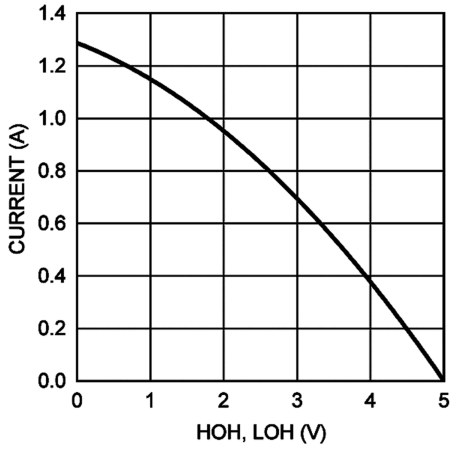


Figure 2. Peak Source Current vs Output Voltage

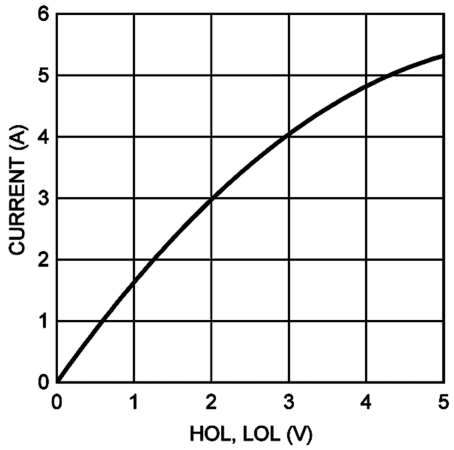


Figure 3. Peak Sink Current vs Output Voltage

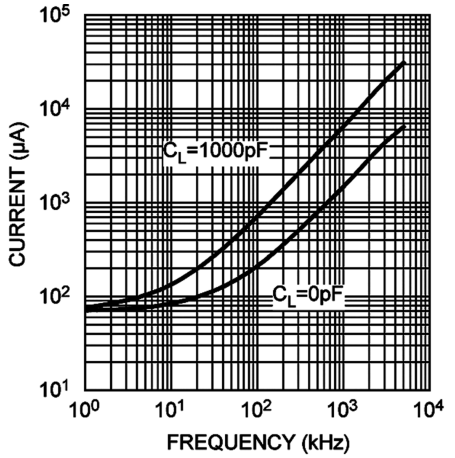


Figure 4. I_{DDO} vs Frequency

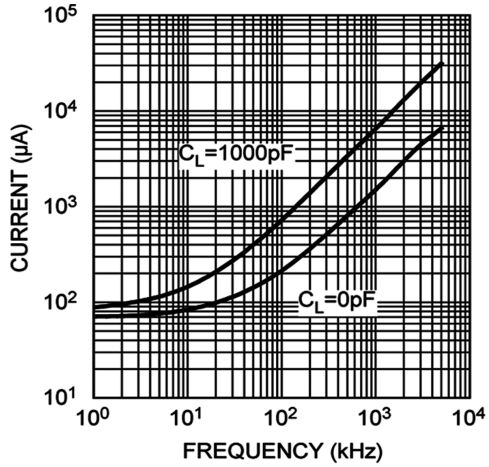


Figure 5. I_{HBO} vs Frequency

Typical Characteristics (continued)

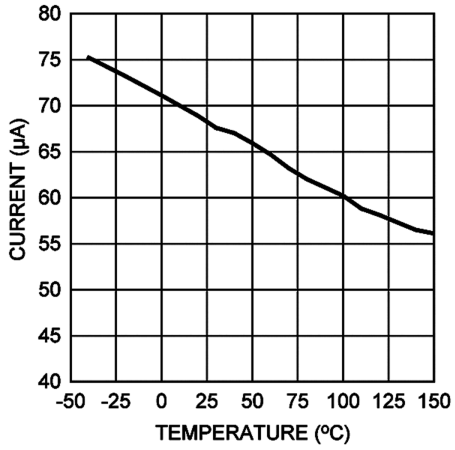


Figure 6. I_{DD} vs Temperature

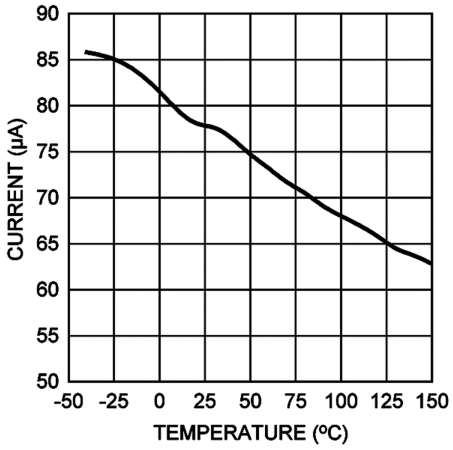


Figure 7. I_{HB} vs Temperature

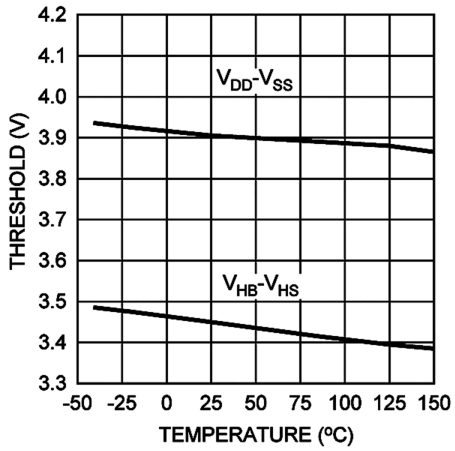


Figure 8. UVLO Rising Thresholds vs Temperature

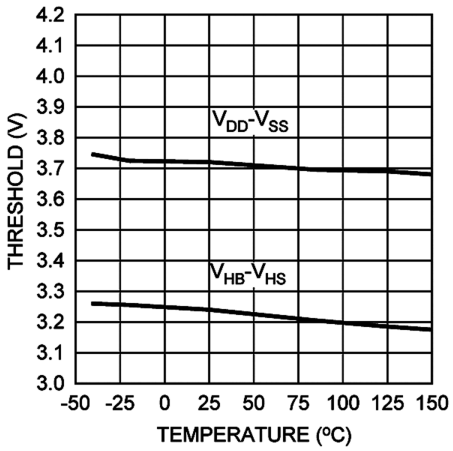


Figure 9. UVLO Falling Thresholds vs Temperature

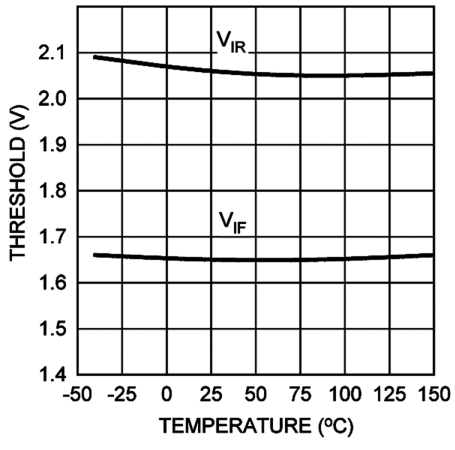


Figure 10. Input Thresholds vs Temperature

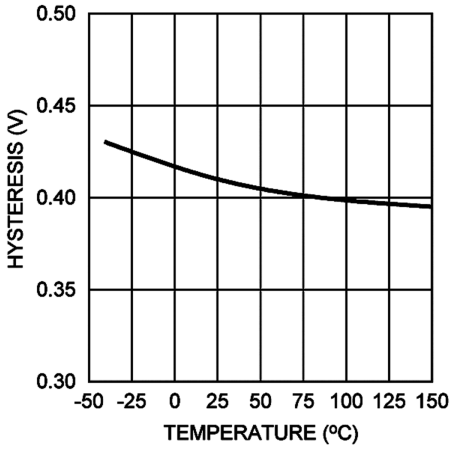


Figure 11. Input Threshold Hysteresis vs Temperature

Typical Characteristics (continued)

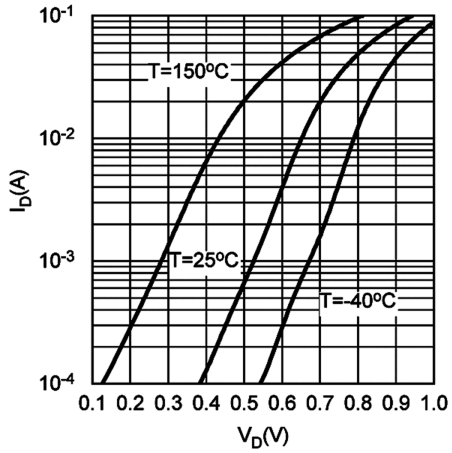


Figure 12. Bootstrap Diode Forward Voltage

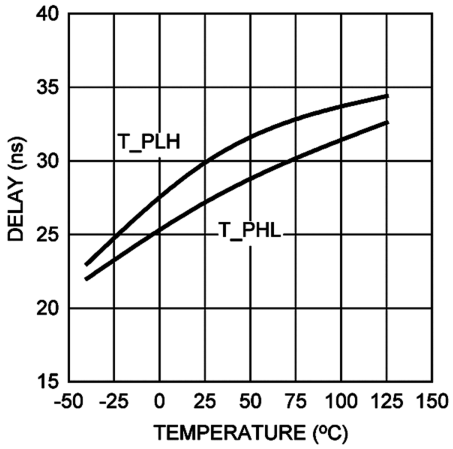
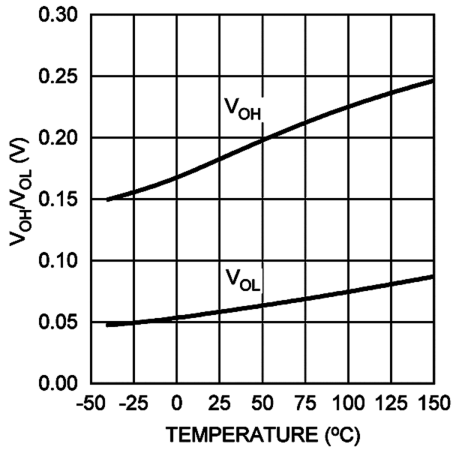
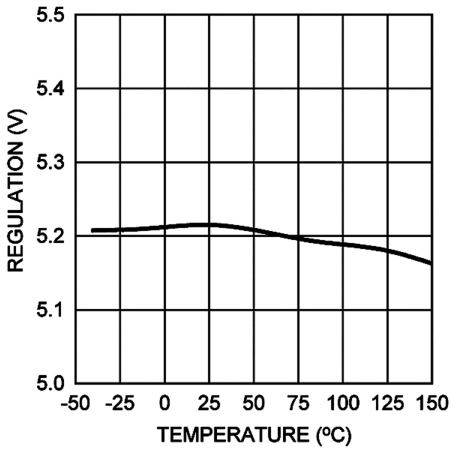


Figure 13. Propagation Delay vs Temperature



Note: Unless otherwise specified,
VDD = VHB = 5 V, VSS = VHS = 0 V.

Figure 14. LO & HO Gate Drive – High/Low Level Output Voltage vs Temperature



Note: Unless otherwise specified,
VDD = VHB = 5 V, VSS = VHS = 0 V.

Figure 15. HB Regulation Voltage vs Temperature

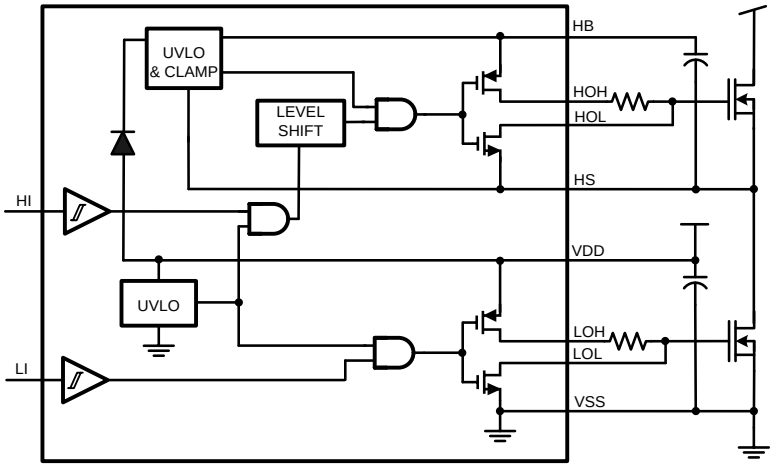
7 Detailed Description

7.1 Overview

The LM5113 is a high frequency high- and low- side gate driver for enhancement mode Gallium Nitride (GaN) FETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of driving a high-side enhancement mode GaN FET operating up to 100 V. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.2 V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The LM5113 has split gate outputs with strong sink capability, providing flexibility to adjust the turn-on and turn-off strength independently.

The LM5113 can operate up to several MHz, and available in a standard WSON-10 pin package and a 12-bump DSBGA package. The WSON-10 pin package contains an exposed pad to aid power dissipation. The DSBGA package offers a compact footprint and minimized package inductance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input and Output

The inputs are independently controlled with TTL input thresholds, and can withstand voltages up to 14 V regardless of the VDD voltage, which means it could be directly connected to the outputs of PWM controllers with up to 14V power supply, saving a buffer stage between output of higher-voltage powered controller, for example LM5025 with 10V, and input of the LM5113.

The output pull-down and pull-up resistance of LM5113 is optimized for enhancement mode GaN FETs to achieve high frequency and efficient operation. The 0.6 Ω pull-down resistance provides a robust low impedance turn-off path necessary to eliminate undesired turn-on induced by high dv/dt or high di/dt. The 2.1 Ω pull-up resistance helps reduce the ringing and over-shoot of the switch node voltage. The split outputs of the LM5113 offer flexibility to adjust the turn-on and turn-off speed by independently adding additional impedance in either the turn-on path and/or the turn-off path.

It is very important that, input signal of the two channels, HI and LI, which has logic compatible threshold and hysteresis, if not used, must be tied to either VDD or VSS. This inputs must not be left floating.

7.3.2 Start-up and UVLO

The LM5113 has an Under-voltage Lockout (UVLO) on both the VDD and bootstrap supplies. When the VDD voltage is below the threshold voltage of 3.8 V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. Also if there is insufficient VDD voltage, the UVLO will actively pull the LOL and HOL low. When the HB to HS bootstrap voltage is below the UVLO threshold of 3.2 V, only HOL is pulled low. Both UVLO threshold voltages have 200 mV of hysteresis to avoid chattering.

Feature Description (continued)

Table 1. VDD UVLO Feature Logic Operation

CONDITION (V_{HB-HS} > V_{HBR} for all cases below)	HI	LI	HO	LO
V_{DD} - V_{SS} < V_{DDR} during device start-up	H	L	L	L
V_{DD} - V_{SS} < V_{DDR} during device start-up	L	H	L	L
V_{DD} - V_{SS} < V_{DDR} during device start-up	H	H	L	L
V_{DD} - V_{SS} < V_{DDR} during device start-up	L	L	L	L
V_{DD} - V_{SS} < V_{DDR} - V_{DDH} after device start-up	H	L	L	L
V_{DD} - V_{SS} < V_{DDR} - V_{DDH} after device start-up	L	H	L	L
V_{DD} - V_{SS} < V_{DDR} - V_{DDH} after device start-up	H	H	L	L
V_{DD} - V_{SS} < V_{DDR} - V_{DDH} after device start-up	L	L	L	L

Table 2. V_{HB-HS} UVLO Feature Logic Operation

CONDITION (V_{DD} > V_{DDR} for all cases below)	HI	LI	HO	LO
V_{HB-HS} < V_{HBR} during device start-up	H	L	L	L
V_{HB-HS} < V_{HBR} during device start-up	L	H	L	H
V_{HB-HS} < V_{HBR} during device start-up	H	H	L	H
V_{HB-HS} < V_{HBR} during device start-up	L	L	L	L
V_{HB-HS} < V_{HBR} - V_{HBH} after device start-up	H	L	L	L
V_{HB-HS} < V_{HBR} - V_{HBH} after device start-up	L	H	L	H
V_{HB-HS} < V_{HBR} - V_{HBH} after device start-up	H	H	L	H
V_{HB-HS} < V_{HBR} - V_{HBH} after device start-up	L	L	L	L

7.3.3 HS Negative Voltage and Bootstrap Supply Voltage Clamping

Due to the intrinsic feature of enhancement mode GaN FETs, the source-to-drain voltage of the bottom switch, is usually higher than a diode forward voltage drop when the gate is pulled low. This will cause negative voltage on HS pin. Moreover, this negative voltage transient will be even worse, considering layout and device drain/source parasitic inductances. With high side driver using the floating bootstrap configuration, Negative HS voltage can lead to an excessive bootstrap voltage which can damage the high-side GaN FET. The LM5113 solves this problem with an internal clamping circuit that prevents the bootstrap voltage from exceeding 5.2V typical.

7.3.4 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output which is referenced to the HS pin and provides excellent delay matching with the low-side driver. Typical delay matching between LO and HO is around 1.5 ns.

7.4 Device Functional Modes

Table 3 shows the device truth table.

Table 3. Truth Table

HI	LI	HOH	HOL	LOH	LOL
L	L	Open	L	Open	L
L	H	Open	L	H	Open
H	L	H	Open	Open	L
H	H	H	Open	H	Open

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

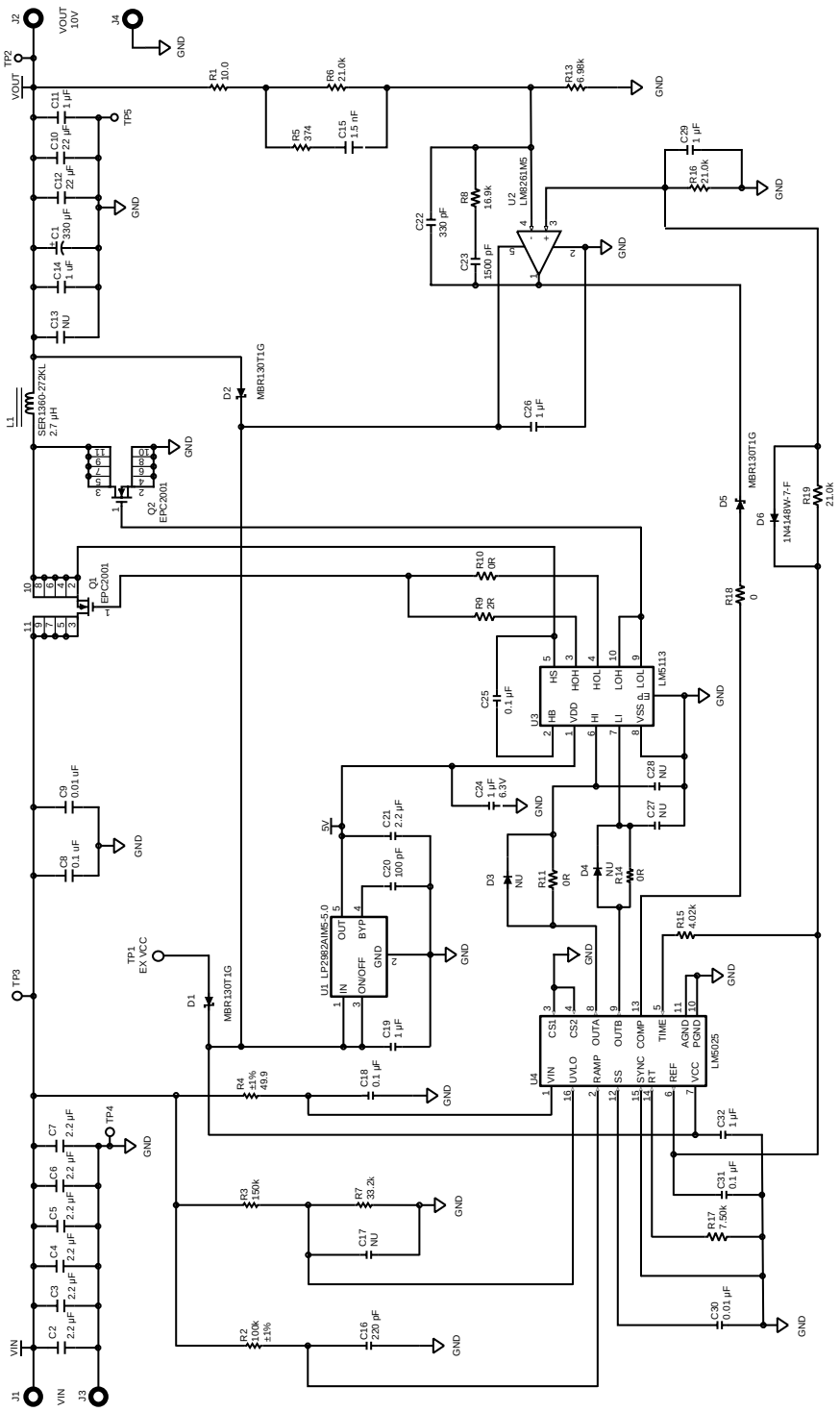
To operate GaN transistors at very high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the GaN transistor. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3 V logic signal which cannot effectively turn on a power switch. Level shift circuit is needed to boost the 3.3 V signal to the gate-drive voltage (such as 12 V) in order to fully turn-on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LM5113 is a MHz high- and low- side gate driver for enhancement mode Gallium Nitride (GaN) FETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of driving a high-side enhancement mode GaN FET operating up to 100V. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.2V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The LM5113 has split gate outputs with strong sink capability, providing flexibility to adjust the turn-on and turn-off strength independently.

8.2 Typical Application

The circuit in Figure 16 shows a synchronous buck converter to evaluate LM5113. Detailed synchronous buck converter specifications are listed in *Design Requirements*. The active clamping voltage mode controller LM5025 is used for close-loop control and generates the PWM signals of the buck switch and the synchronous switch. For more information, please refer to *Related Documentation*.

Typical Application (continued)



Input 15 V to 60 V, output 10 V, 800 kHz

Figure 16. Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

Table 4 lists the design requirements for the typical application.

Table 4. Design Parameters

PARAMETER	SPECIFICATION
Input operating range	15 – 60 V
Output voltage	10 V
Output current, 48 V input	10 A
Output current, 60 V input	7 A
Efficiency at 48 V, 10 A	>90%
Frequency	800 kHz

8.2.2 Detailed Design Procedure

This procedure outlines the design considerations of LM5113 in a synchronous buck converter with enhancement mode Gallium Nitride (GaN) FET. Refer to Figure 19 for component names and network locations. For additional design help, please see *Related Documentation*.

8.2.2.1 VDD Bypass Capacitor

The VDD bypass capacitor provides the gate charge for the low-side and high-side transistors and to absorb the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated with Equation 1.

$$C_{VDD} > \frac{Q_{gH} + Q_{gL} + Q_{rr}}{\Delta V} \quad (1)$$

Q_{gH} and Q_{gL} are gate charge of the high-side and low-side transistors respectively. Q_{rr} is the reverse recovery charge of the bootstrap diode, which is typically around 4nC. ΔV is the maximum allowable voltage drop across the bypass capacitor. A 0.1uF or larger value, good quality, ceramic capacitor is recommended. The bypass capacitor should be placed as close to the pins of the IC as possible to minimize the parasitic inductance.

8.2.2.2 Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side switch, DC bias power for HB under-voltage lockout circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated with Equation 2.

$$C_{BST} > \frac{Q_{gH} + I_{HB} \times t_{ON} + Q_{rr}}{\Delta V} \quad (2)$$

I_{HB} is the quiescent current of the high-side driver. t_{on} is the maximum on-time period of the high-side transistor. A good quality, ceramic capacitor should be used for the bootstrap capacitor. It is recommended to place the bootstrap capacitor as close to the HB and HS pins as possible.

8.2.2.3 Power Dissipation

The power consumption of the driver is an important measure that determines the maximum achievable operating frequency of the driver. It should be kept below the maximum power dissipation limit of the package at the operating temperature. The total power dissipation of the LM5113 is the sum of the gate driver losses and the bootstrap diode power loss.

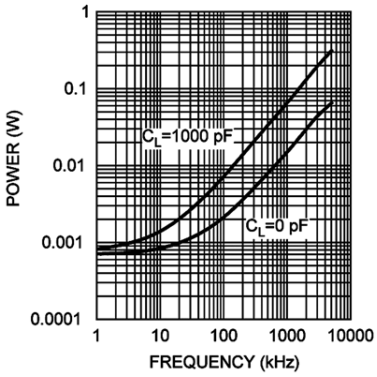
The gate driver losses are incurred by charge and discharge of the capacitive load. It can be approximated as

$$P = \left(C_{LoadH} + C_{LoadL}\right) \times V_{DD}^2 \times f_{SW} \quad (3)$$

C_{LoadH} and C_{LoadL} are the high-side and the low-side capacitive loads respectively. It can also be calculated with the total input gate charge of the high-side and the low-side transistors as

$$P = \left(Q_{gH} + Q_{gL} \right) \times V_{DD} \times f_{sw} \quad (4)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equations. This plot can be used to approximate the power losses due to the gate drivers.

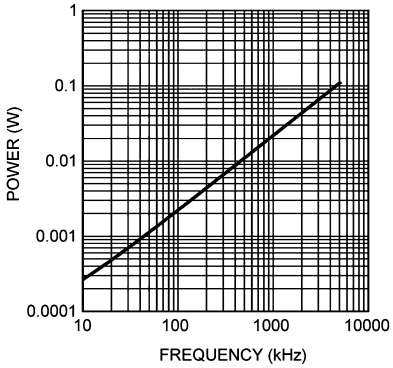


Gate Driver Power Dissipation (LO+HO), VDD = +5 V

Figure 17. Neglecting Bootstrap Diode Losses

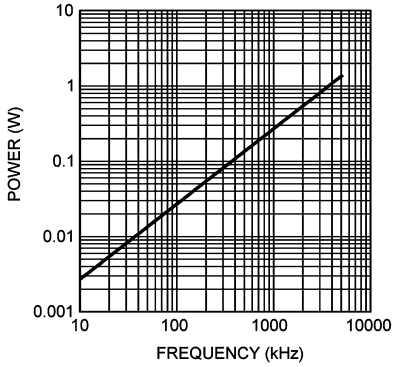
The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to the operating frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge also result in higher reverse recovery losses.

The following two plots illustrate the forward bias power loss and the reverse bias power loss of the bootstrap diode respectively. The plots are generated based on calculations and lab measurements of the diode reverse time and current under several operating conditions. The plots can be used to predict the bootstrap diode power loss under different operating conditions.



The Load of High-Side Driver is a GaN FET with Total Gate Charge of 10 nC.

Figure 18. Forward Bias Power Loss of Bootstrap Diode V_{IN}=50V



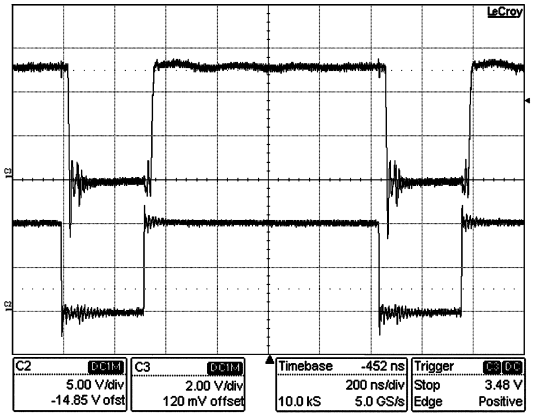
The Load of High-Side Driver is a GaN FET with Total Gate Charge of 10 nC.

Figure 19. Reverse Recovery Power Loss of Bootstrap Diode V_{IN}=50V

The sum of the driver loss and the bootstrap diode loss is the total power loss of the IC. For a given ambient temperature, the maximum allowable power loss of the IC can be defined as Equation 5.

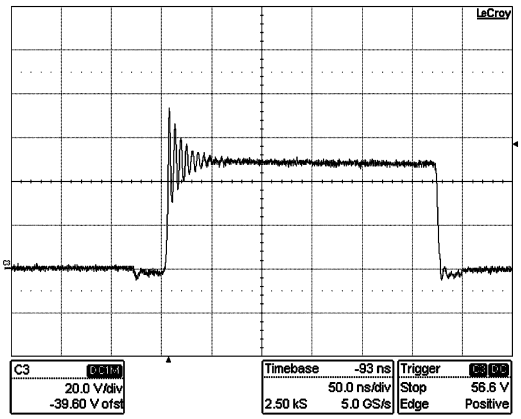
$$P = \frac{(T_J - T_A)}{\theta_{JA}} \quad (5)$$

8.2.3 Application Curves



Conditions:
Input Voltage = 48 V DC, Load Current = 5 A
Traces:
Top Trace: Gate of Low-Side eGaN FET, Volt/div = 2 V
Bottom Trace: LI of LM5113, Volt/div = 5 V
Bandwidth Limit = 600 MHz
Horizontal Resolution = 0.2 µs/div

Figure 20. Low-Side Driver Input and Output



Conditions:
Input Voltage = 48 V DC,
Load Current = 10 A
Traces:
Trace: Switch-Node Voltage, Volts/div = 20 V
Bandwidth Limit = 600 MHz
Horizontal Resolution = 50 ns/div

Figure 21. Switch-Node Voltage

9 Power Supply Recommendations

The recommended bias supply voltage range for LM5113 is from 4.5 V to 5.5 V. The lower end of this range is governed by the internal undervoltage lockout (UVLO) protection feature of the VDD supply circuit. The upper end of this range is driven by the 7 V absolute maximum voltage rating of the VDD or the GaN transistor gate breakdown voltage limit, whichever is lower. It is recommended to keep proper margin to allow for transient voltage spikes.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the VDD voltage drops, the device continues to operate in normal mode as far as the voltage drop do not exceeds the hysteresis specification, VDDH. If the voltage drop is more than hysteresis specification, the device will shut down. Therefore, while operating at or near the 4.5 V range, the voltage ripple on the auxiliary power supply output should be smaller than the hysteresis specification of LM5113 to avoid triggering device-shutdown.

A local bypass capacitor should be placed between the VDD and VSS pins. And this capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to 10 µF, for IC bias requirements.

10 Layout

10.1 Layout Guidelines

Small gate capacitance and miller capacitance enable enhancement mode GaN FETs to operate with fast switching speed. The induced high dv/dt and di/dt, coupled with a low gate threshold voltage and limited headroom of enhancement mode GaN FETs gate voltage, make the circuit layout crucial to the optimum performance. Following are some hints.

1. The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the GaN FETs gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the GaN FETs. The GaN FETs should be placed close to the driver.
2. The second high current path includes the bootstrap capacitor, the local ground referenced VDD bypass capacitor and low-side GaN FET. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
3. The parasitic inductance in series with the source of the high-side FET and the low-side FET can impose excessive negative voltage transients on the driver. It is recommended to connect HS pin and VSS pin to the respective source of the high-side and low-side transistors with a short and low-inductance path.
4. The parasitic source inductance, along with the gate capacitor and the driver pull-down path, can form a LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.
5. Low ESR/ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak current being drawn from VDD during turn-on of the FETs. Keeping bullet #1 (minimized GaN FETs gate driver loop) as the first priority, it is also desirable to place the VDD decoupling capacitor and the HB to HS bootstrap capacitor on the same side of the PC board as the driver. The inductance of vias can impose excessive ringing on the IC pins.
6. To prevent excessive ringing on the input power bus, good decoupling practices are required by placing low ESR ceramic capacitors adjacent to the GaN FETs.

The following figures show recommended layout patterns for WSON-10 package and DSBGA package respectively. Two cases are considered: (1) Without any gate resistors; (2) With an optional turn-on gate resistor. It should be noted that 0402 DSBGA package is assumed for the passive components in the drawings. For information on DSBGA package assembly, refer to *Related Documentation*.

10.2 Layout Example

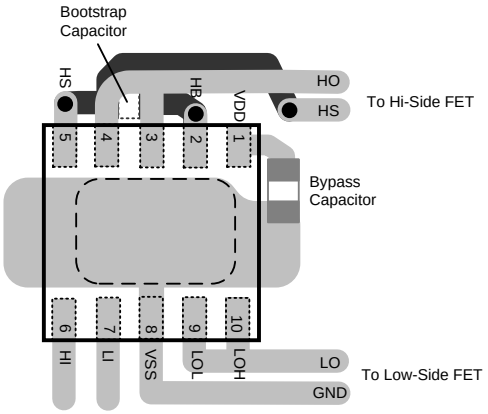


Figure 22. WSON-10 Without Gate Resistors

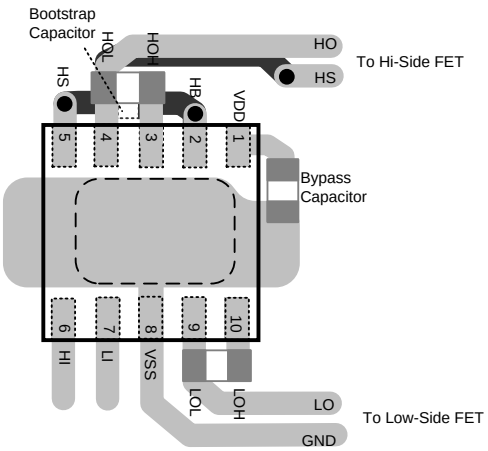


Figure 23. WSON-10 With HOH and LOH Gate Resistors

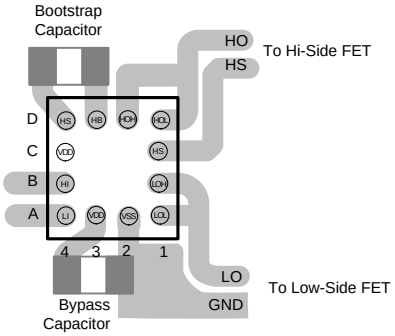


Figure 24. DSBGA Without Gate Resistors

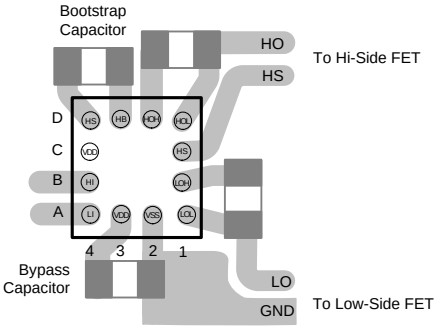


Figure 25. DSBGA With HOH and LOH Gate Resistors

C

Appendix: Datasheet of the Si Transistor

STD47N10F7AG

Automotive-grade N-channel 100 V, 12.5 mΩ typ., 45 A, STripFET™ F7 Power MOSFET in a DPAK package

Datasheet - production data

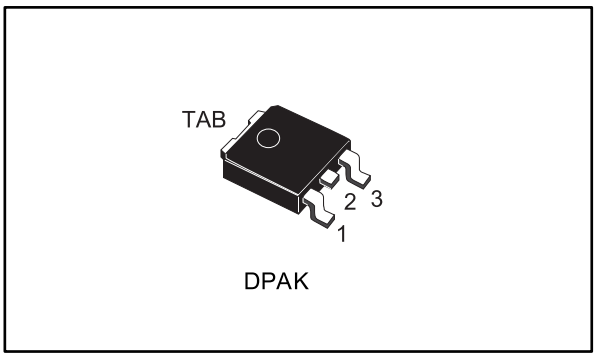
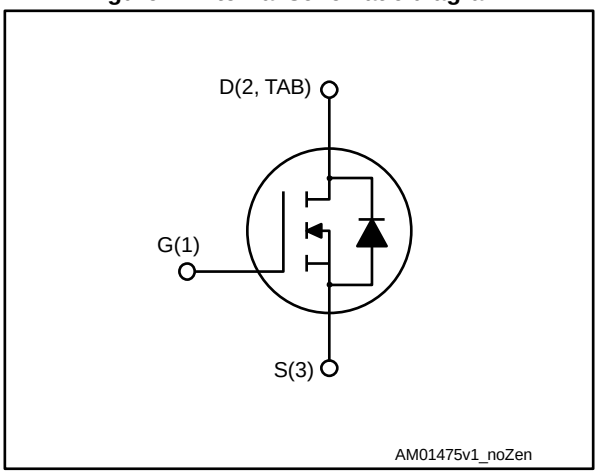


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD47N10F7AG	100 V	18 mΩ	45 A	60 W

- AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STD47N10F7AG	47N10F7	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	45	A
	Drain current (continuous) at T_C = 100 °C	32	
I_{DM}(1)	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at T_C = 25 °C	60	W
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		°C

Notes:

(1)Pulse width is limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.5	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50	

Notes:

(1)When mounted on a 1-inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 100 V			10	µA
		V_{GS} = 0 V, V_{DS} = 100 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 22.5 A		12.5	18	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	1640	-	pF
C_{oss}	Output capacitance		-	360	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 45 A, V_{GS} = 0 to 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	25	-	nC
Q_{gs}	Gate-source charge		-	5.1	-	nC
Q_{gd}	Gate-drain charge		-	12.2	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 22.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	15	-	ns
t_r	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	8	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		45	A
I_{SDM}(1)	Source-drain current (pulsed)		-		180	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 45 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 45 A, di/dt = 100 A/µs, V_{DD} = 80 V, T_J = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	53		ns
Q_{rr}	Reverse recovery charge		-	67		nC
I_{RRM}	Reverse recovery current		-	2.5		A

Notes:

(1)Pulse width is limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

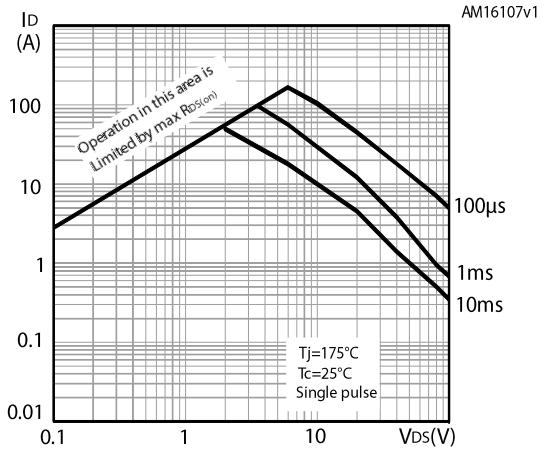


Figure 3: Thermal impedance

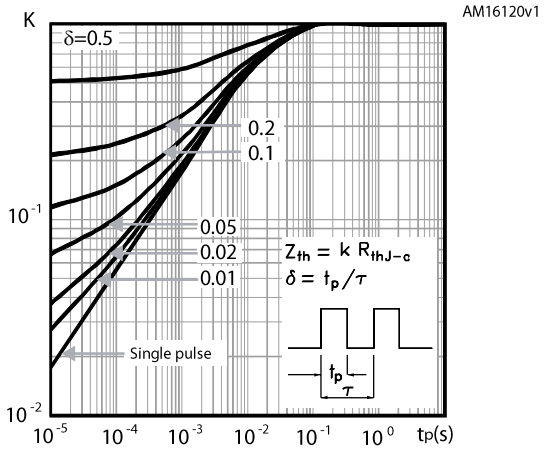


Figure 4: Output characteristics

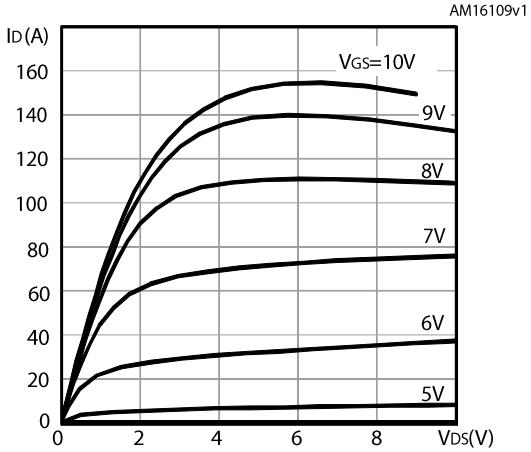


Figure 5: Transfer characteristics

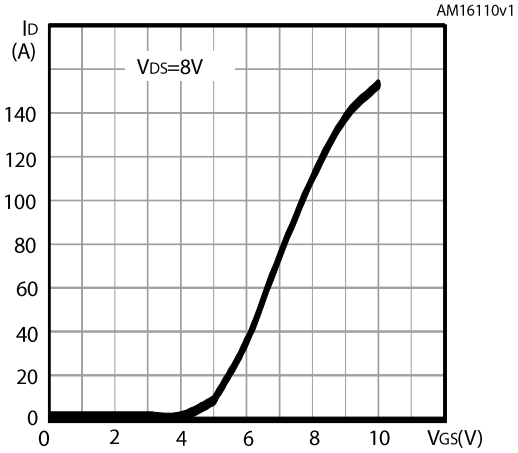


Figure 6: Gate charge vs gate-source voltage

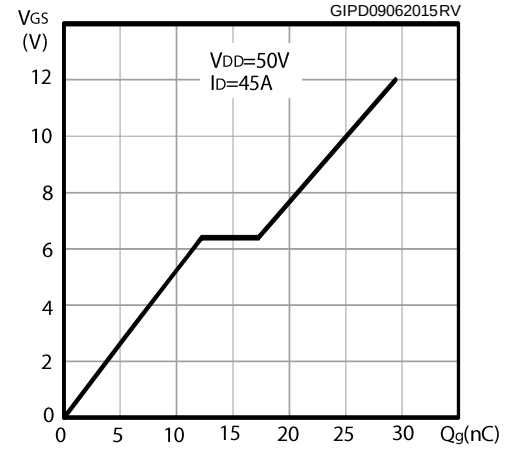


Figure 7: Static drain-source on-resistance

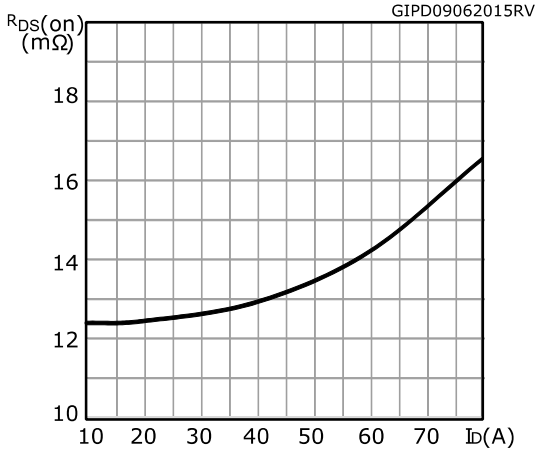


Figure 8: Capacitance variations

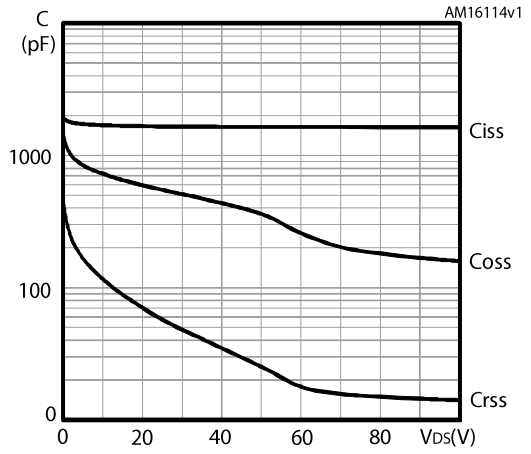


Figure 9: Normalized gate threshold voltage vs temperature

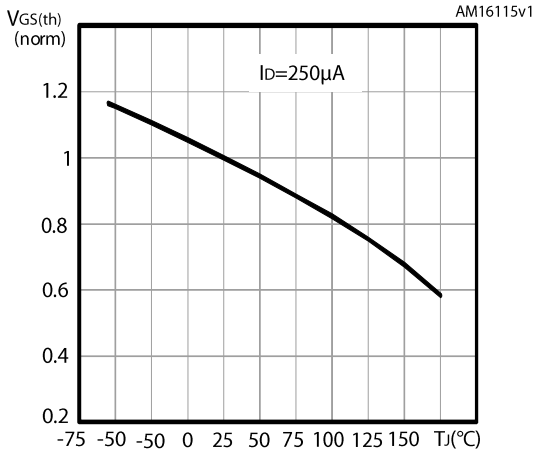


Figure 10: Normalized on-resistance vs temperature

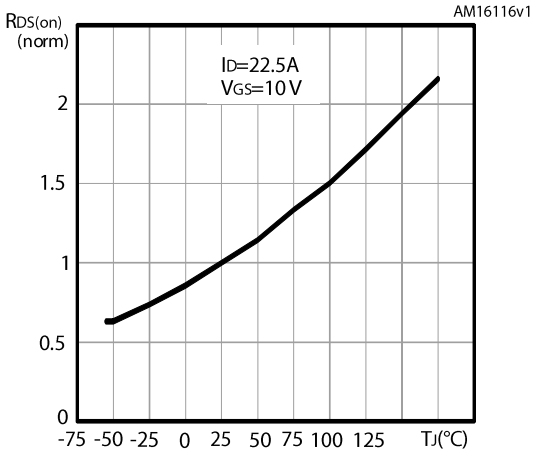


Figure 11: Source-drain diode forward characteristics

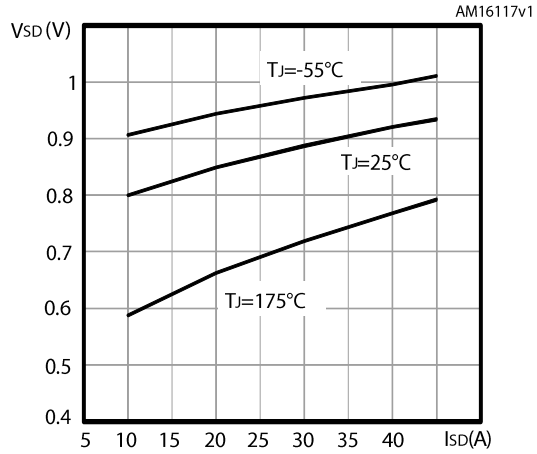
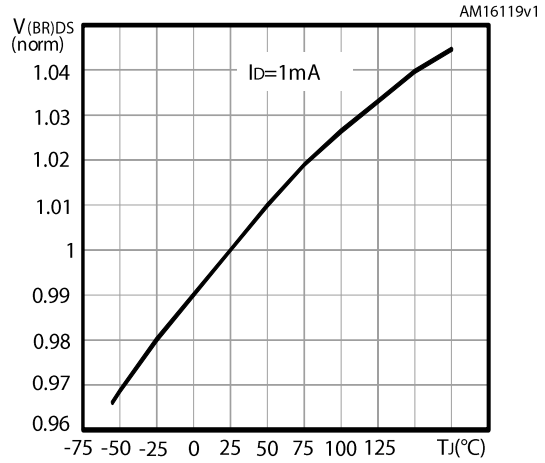


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13: Test circuit for resistive load switching times

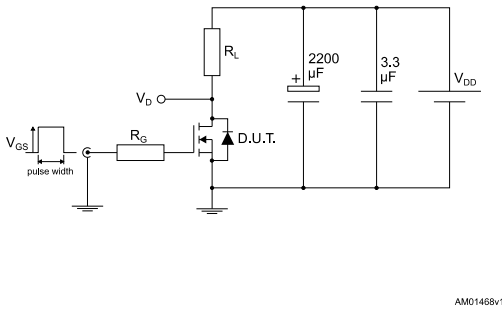


Figure 14: Test circuit for gate charge behavior

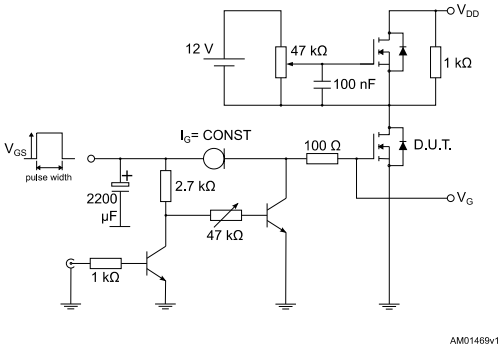


Figure 15: Test circuit for inductive load switching and diode recovery times

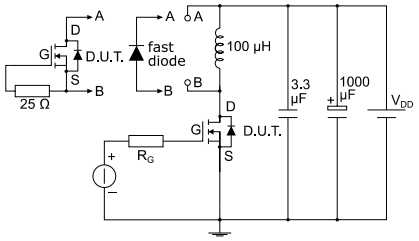


Figure 16: Unclamped inductive load test circuit

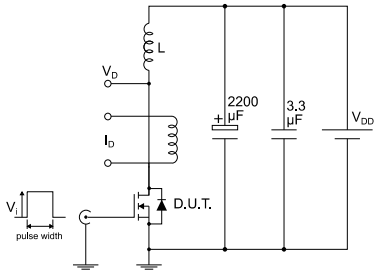


Figure 17: Unclamped inductive waveform

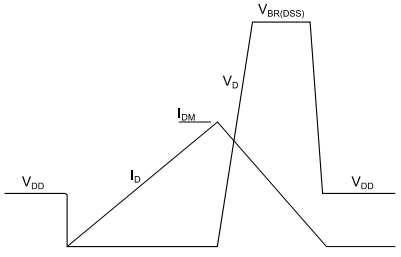
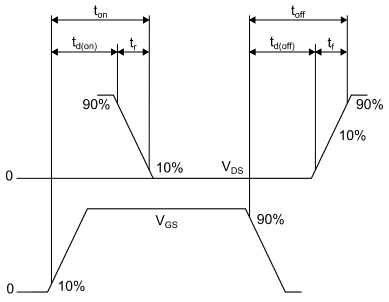


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 19: DPAK (TO-252) type A2 package outline

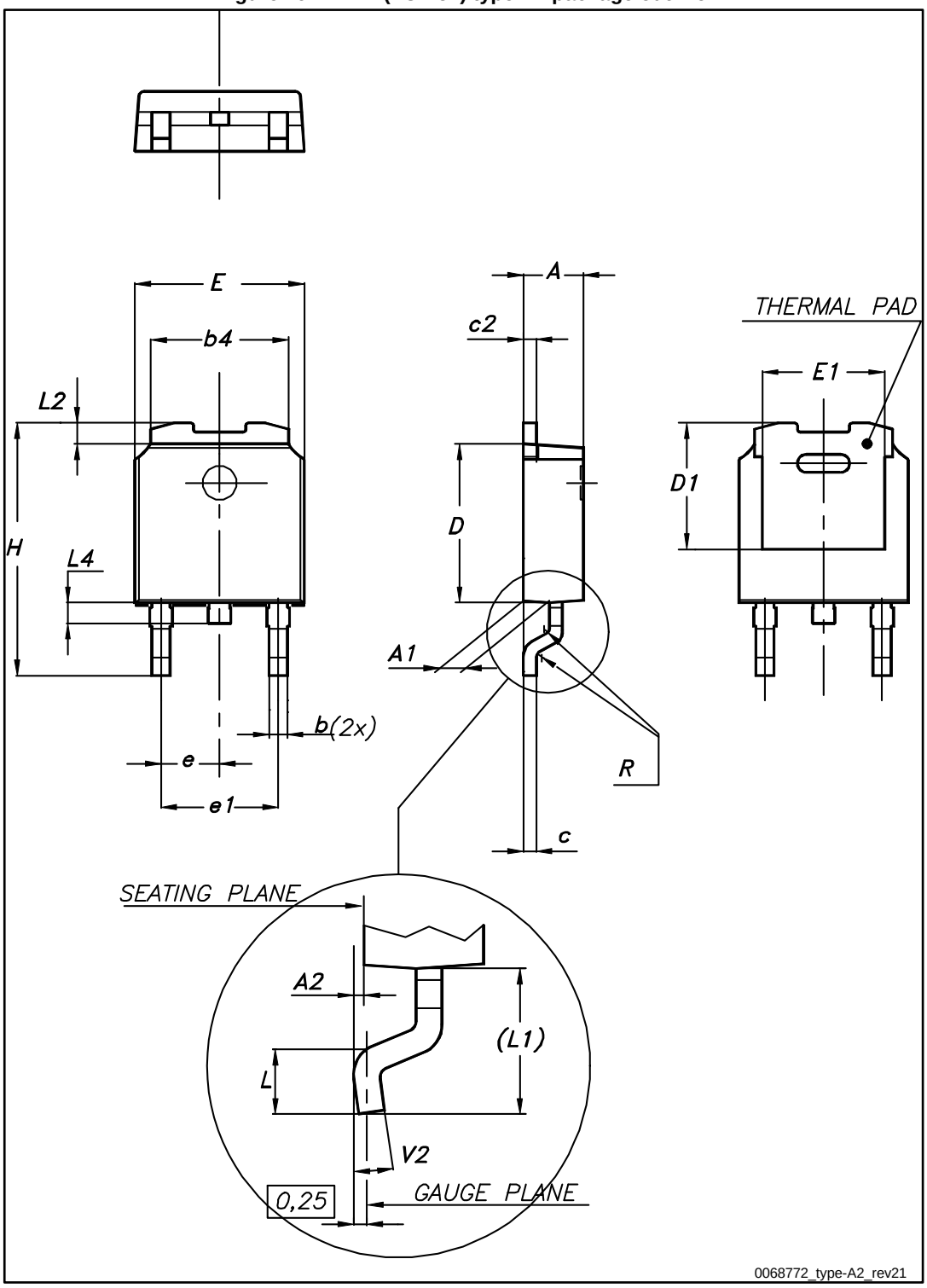
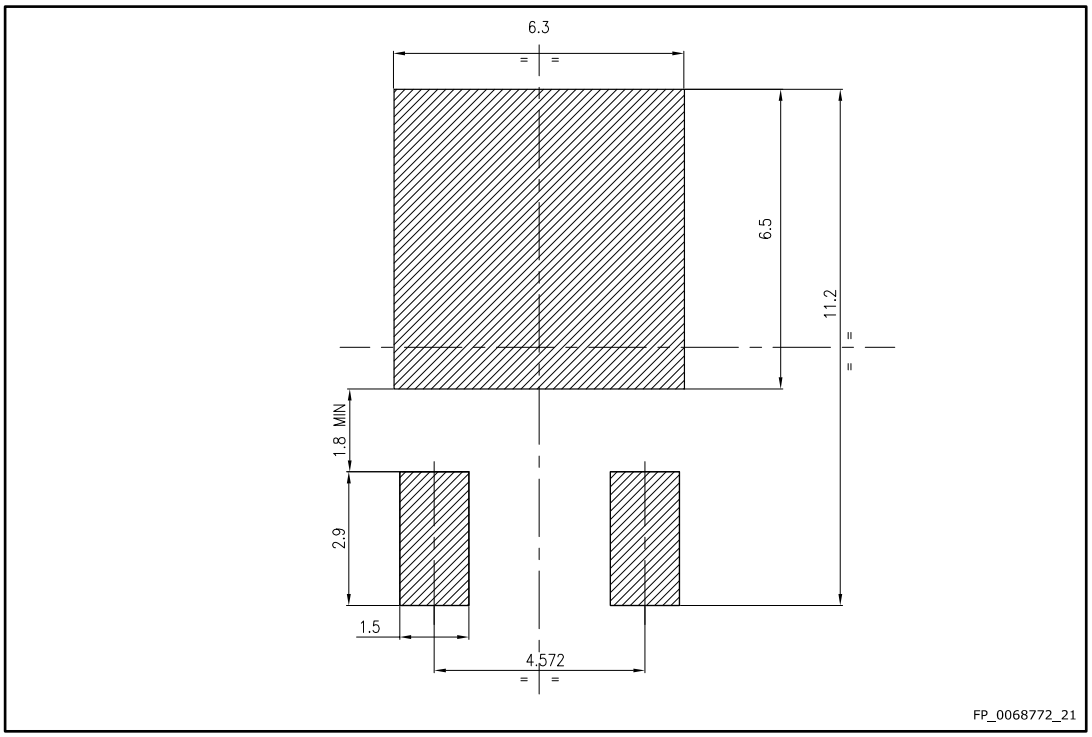


Table 8: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 21: DPAK (TO-252) tape outline

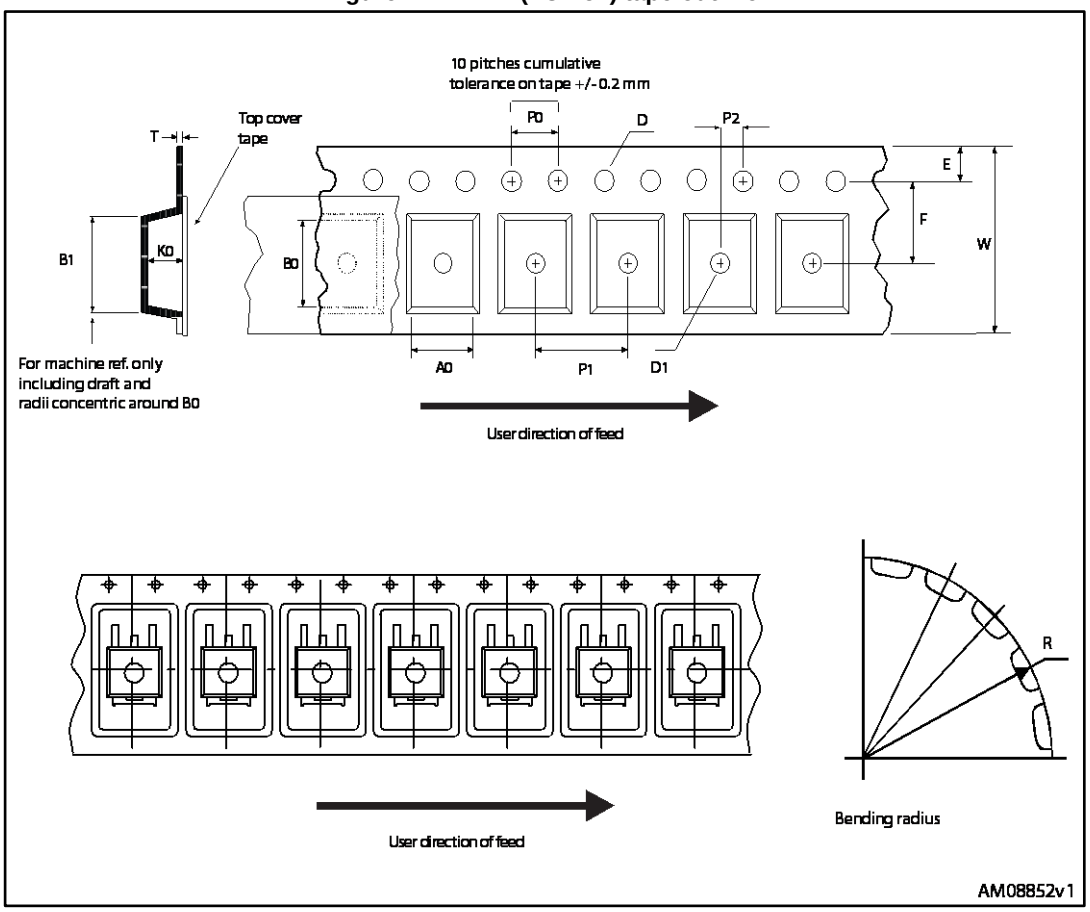


Figure 22: DPAK (TO-252) reel outline

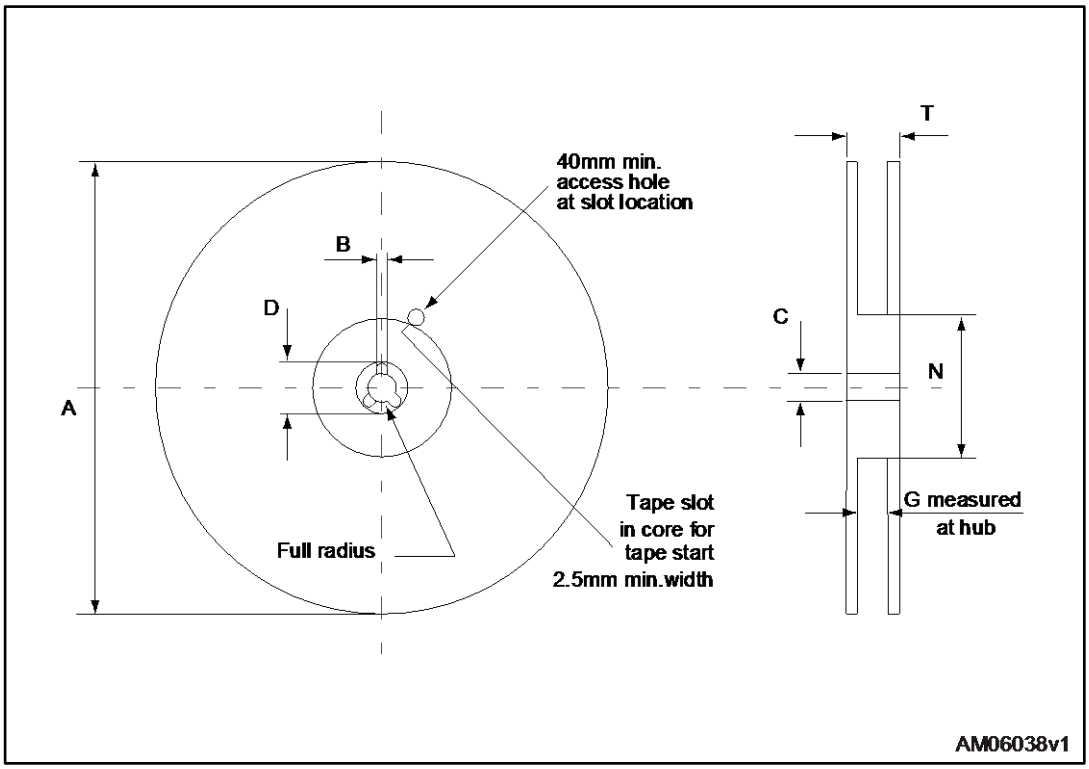


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
23-Feb-2015	1	First release
17-Jun-2015	2	Updated *Section 4: Package mechanical data*. Minor text changes
01-Feb-2017	3	Updated title and features on cover page. Updated *Section 1: "Electrical ratings"* and *Section 2: "Electrical characteristics"*. Minor text changes

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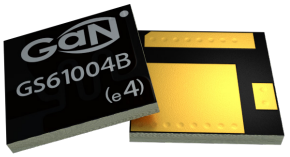
D

Appendix: Datasheet of the GaN Transistor

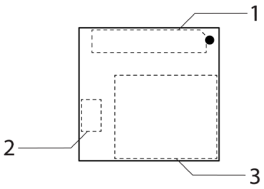
GS61004B
100V enhancement mode GaN transistor
Preliminary Datasheet

Features

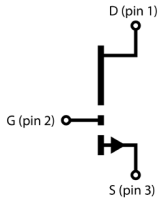
- 100V enhancement mode power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 15 mΩ
- $I_{DS(max)}$ = 45 A
- Ultra-low FOM Island Technology™ die
- Low inductance GaN*PX*™ package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (f > 100 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 4.6 x 4.4 mm^2 PCB footprint
- RoHS 6 compliant



Package Outline



Circuit Symbol



The Source (S- pin 3) and substrate are internally connected and serves as the thermal pad for the device

Applications

- High efficiency power conversion
- High density power conversion
- Enterprise and Networking Power
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Industrial Motor Drives
- Solar Power
- Fast Battery Charging
- Class D Audio amplifiers
- Smart Home

Description

The GS61004B is an enhancement mode GaN-on-Silicon power transistor. The properties of GaN allow for high current, high voltage breakdown, high switching frequency and high temperature operation. GaN Systems implements patented **Island Technology®** cell layout for high-current die performance & yield. **GaN*PX*™** packaging enables low inductance & low thermal resistance in a small package. The GS61004B is a bottom-cooled transistor that offer very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	100	V
Transient Drain to Source Voltage (note 1)	$V_{DS(transient)}$	130	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case}=25 °C) (note 2)	I_{DS}	45	A
Continuous Drain Current (T_{case}=100 °C) (note 2)	I_{DS}	35	A

(1) For 1 µs, duty cycle D<0.1

(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Units
Thermal Resistance (junction-to-case)	$R_{\Theta JC}$		1.1		°C /W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$		22		°C /W
Thermal Resistance (junction-to-ambient) (note 3)	$R_{\Theta JA}$		28		°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}			260	°C

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Ordering Information

Part Number	Package Type	Ordering Code	Packing Method	Quantity
GS61004B	GaN*PX*™ bottom cooled	GS61004B-TR	Tape-and-reel	1000 pcs
GS61004B	GaN*PX*™ bottom cooled	GS61004B-MR	Mini-reel	250 pcs

Electrical Characteristics (Typical values at T_J = 25 °C , V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}		100		V	V_{GS} = 0V, I_{DSS} = 50 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		15	20	mΩ	V_{GS} = 6V, T_J = 25 °C, I_{DS} = 13.5 A
Drain-to-Source On Resistance	$R_{DS(on)}$		39		mΩ	V_{GS} = 6 V, T_J = 150 °C, I_{DS} = 13.5 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.3		V	V_{DS} = V_{GS}, I_D = 7 mA
Gate-to-Source Current	I_{GS}		100		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 80 V, I_D = 45 A
Drain-to-Source Leakage Current	I_{DSS}		0.3		µA	V_{DS} =100 V, V_{GS} = 0 V, T_J = 25°C
Drain-to-Source Leakage Current	I_{DSS}		50		µA	V_{DS} = 100 V, V_{GS} = 0 V, T_J = 150 °C
Internal Gate Resistance	R_G		1.5		Ω	f = 1 MHz, open drain
Input Capacitance	C_{ISS}		328		pF	V_{DS} = 80 V, V_{GS} = 0 V, f = 1 MHz
Output Capacitance	C_{OSS}		133		pF	
Reverse Transfer Capacitance	C_{RSS}		4		pF	
Effective Output Capacitance, Energy Related (Note 4)	$C_{O(ER)}$		148		pF	V_{GS} = 0 V, V_{DS} = 0 to 100 V
Effective Output Capacitance, Time Related (Note 5)	$C_{O(TR)}$		183		pF	
Total Gate Charge	Q_G		6.2		nC	V_{GS} = 0 to 6 V, V_{DS} = 50 V I_{DS}= 45 A
Gate-to-Source Charge	Q_{GS}		2.4		nC	
Gate-to-Drain Charge	Q_{GD}		0.9		nC	
Output Charge	Q_{OSS}		11.5		nC	V_{GS} = 0 V, V_{DS} = 50 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(4) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(5) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

Electrical Performance Graphs

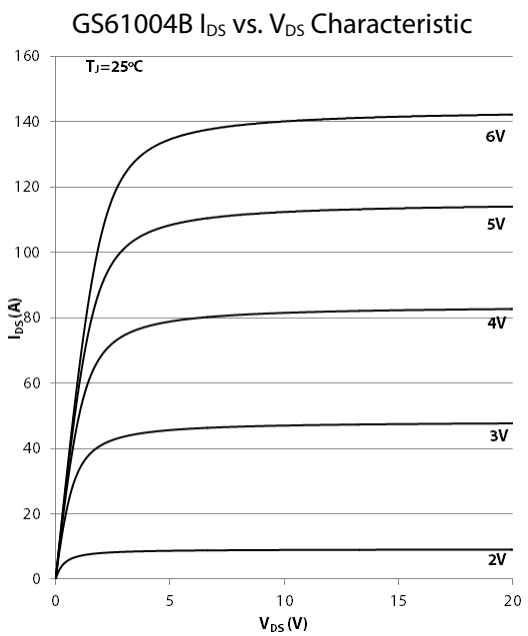


Figure 1 : Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

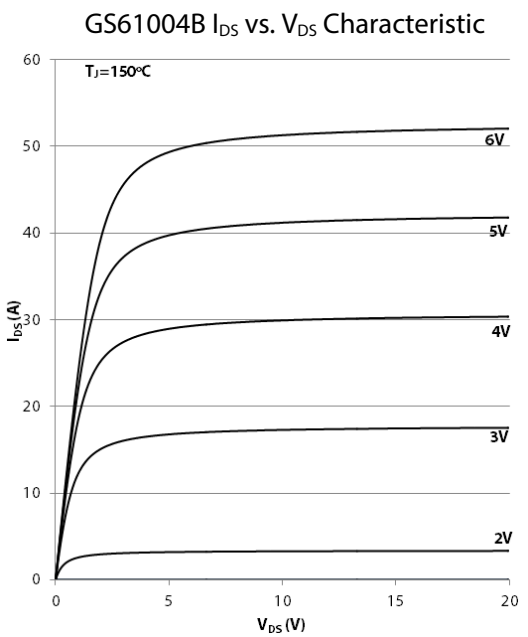


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

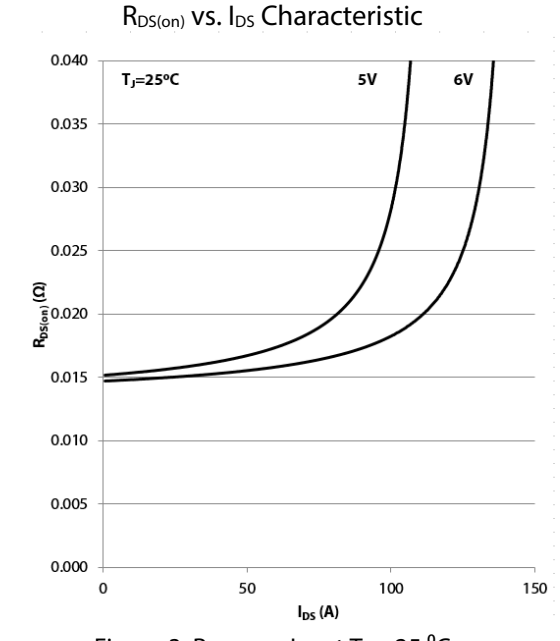


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

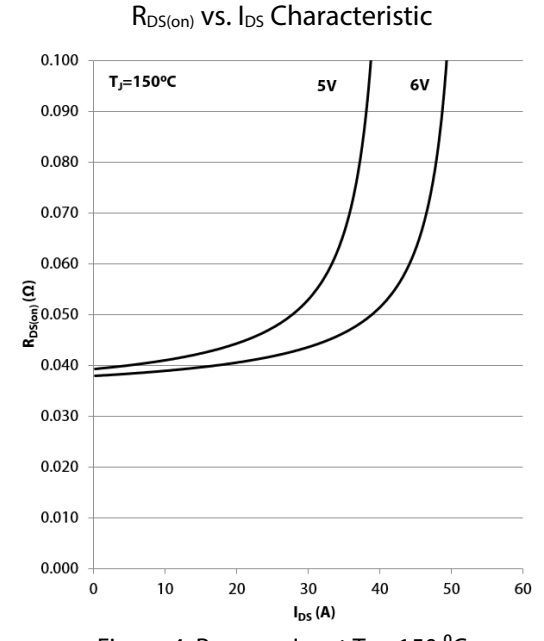


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 °C

Electrical Performance Graphs

GS61004B I_{DS} vs. V_{DS} , T_J dependence

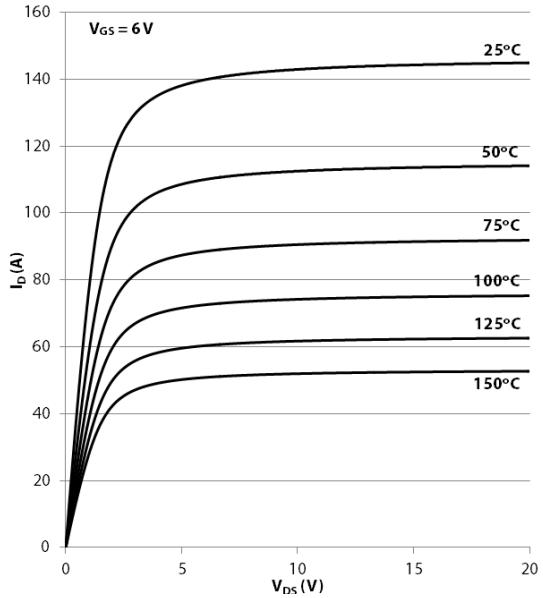


Figure 5 : Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

GS61004B Gate Charge, Q_G Characteristic

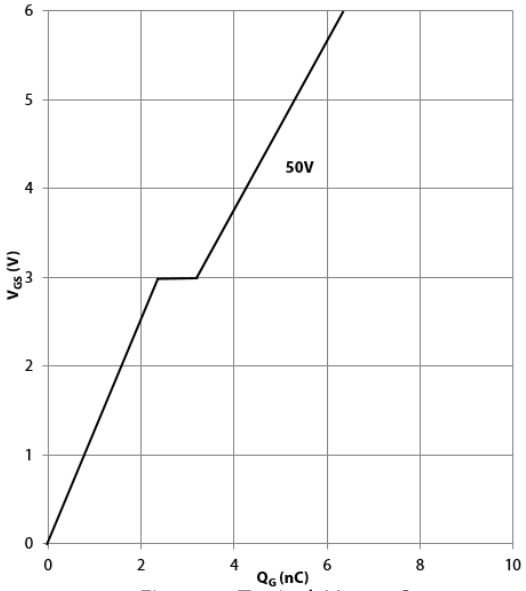


Figure 6: Typical V_{GS} vs. Q_G

GS61004B Capacitance Characteristics

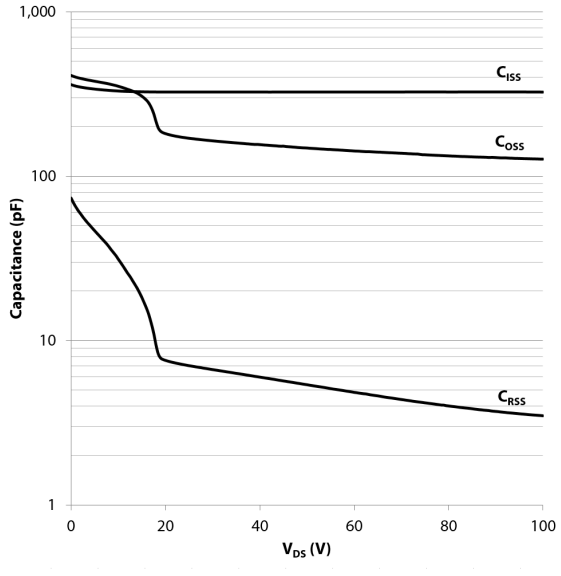


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

GS61004B Stored Energy Characteristic

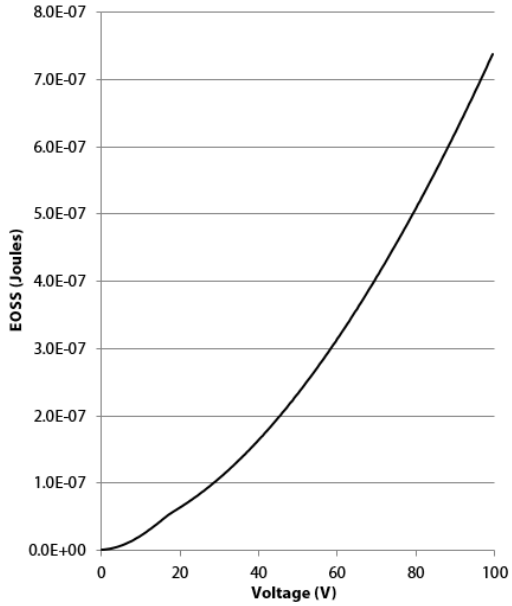


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

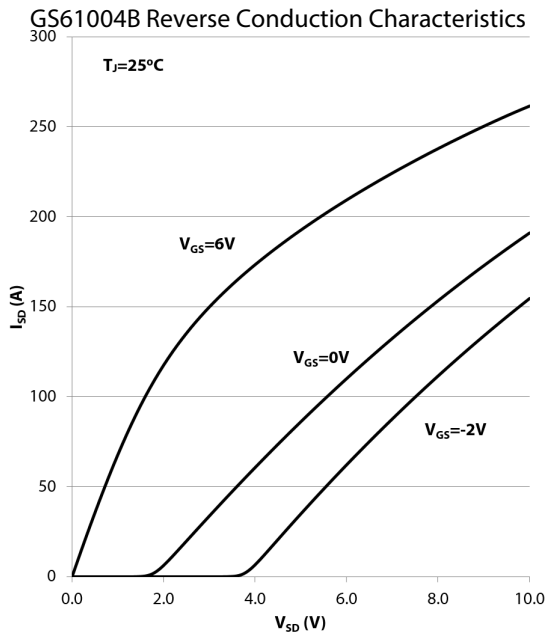


Figure 9 : Typical I_{SD} vs. V_{SD}

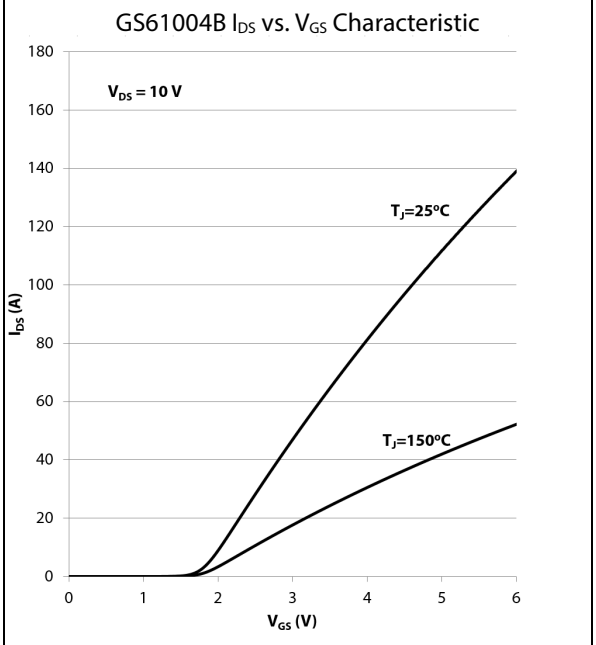


Figure 10 : Typical I_{DS} vs. V_{GS}

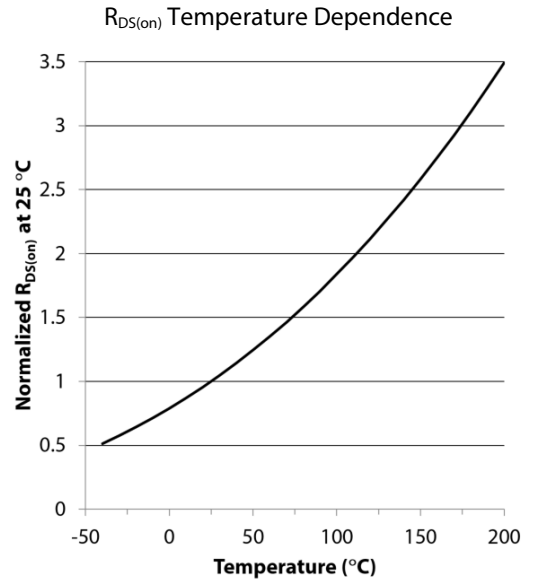


Figure 11: Normalized $R_{DS(on)}$ as a function of T_J

Thermal Performance Graphs

GS61004B I_{DS}-V_{DS} SOA

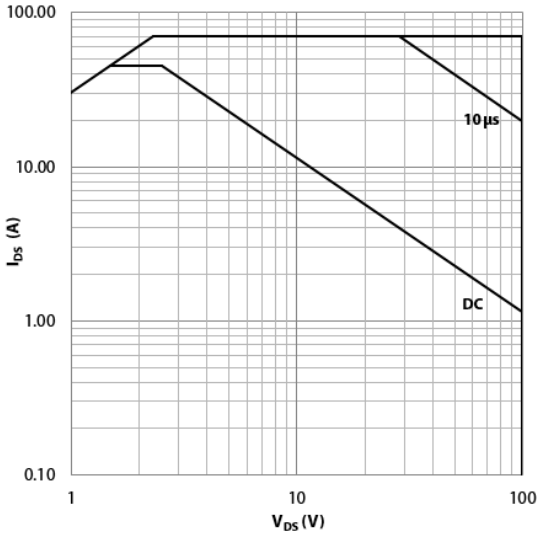


Figure 14: Safe Operating Area @ T_{case} = 25 °C

GS61004B Power Dissipation – Temperature Derating

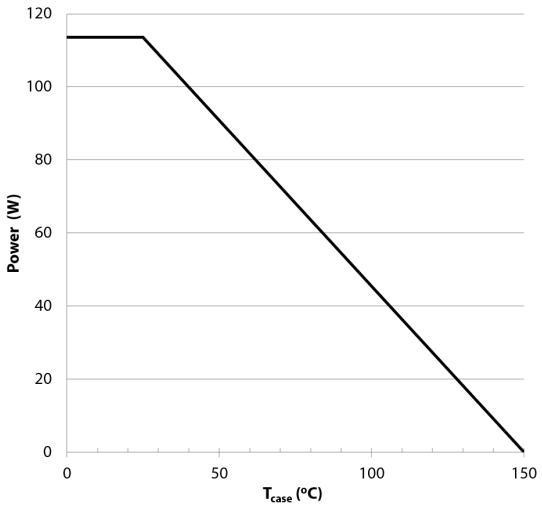


Figure 15: Derating vs. Case Temperature

GS61004B Transient $R_{\theta JC}$

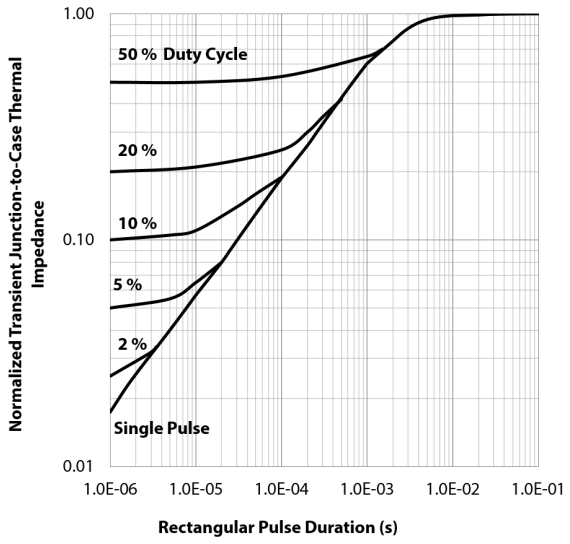


Figure 16: Transient Thermal Impedance

Application Information

Gate Drive

The recommended gate drive voltage for optimal $R_{DS(on)}$ performance and long life is +5 to 6 V. The absolute maximum gate-to-source voltage rating is +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs and duty cycle, D, < 0.1. These specifications allow designers to easily use 5 to 6 V, or even 6.5V gate drive voltage.

A standard MOSFET driver can be used if its UVLO supports 5–6 V operation for gate drive output. Gate drivers with low output impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

The dead time period in half bridge applications, should be minimized for optimum efficiency. Choose a 100V half bridge driver that can support 5-6V gate drive and small dead time. The Texas Instruments LM5113 is an example of a half-bridge driver for GaN E-HEMTs. It is recommended to add a voltage clamp circuit (5.1 or 6.2V zener diode for example) in parallel with bootstrap capacitor to limit the bootstrap voltage for high-side switch if driver does not provide this functionality

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

Although the GS61004B does not have a dedicated source sense pin, the GaN*PX*™ packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated “source sense” connection with a PCB trace from the gate driver output ground to the Source pad in a kelvin configuration with respect to the gate drive signal, the function can easily be implemented. It is recommended to implement a “source sense” connection to improve drive performance.

Thermal

The substrate is internally connected to the thermal pad and to the source pad on the bottom side of the GS61004B. The transistor is designed to be cooled using the printed circuit board.

Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.

Off-state condition (V_{GS} ≤ 0 V): The reverse characteristics in the off-sate are different from silicon MOSFET as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, (V_{GD}) exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}$+$V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $BV_{DS,}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30% higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating.
The absolute maximum drain-to-source rating is 100 V and doesn't change with negative gate voltage.

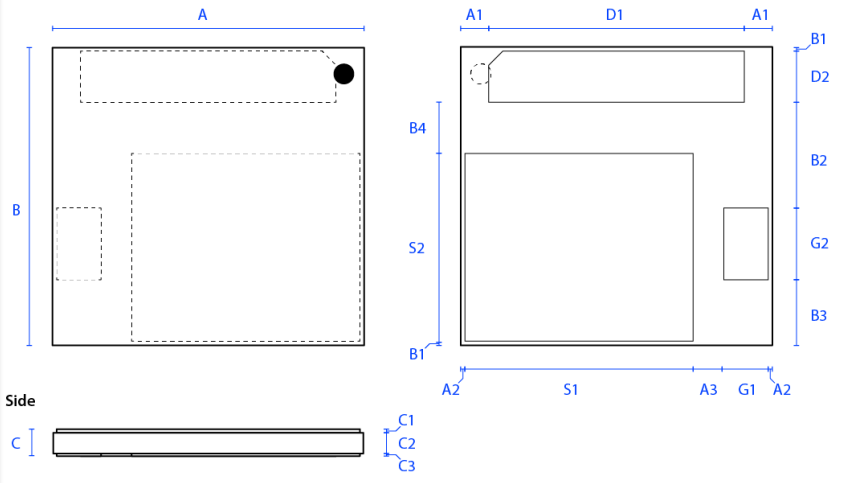
Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the GS61004B to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)
The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60-120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3°C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Package Dimensions

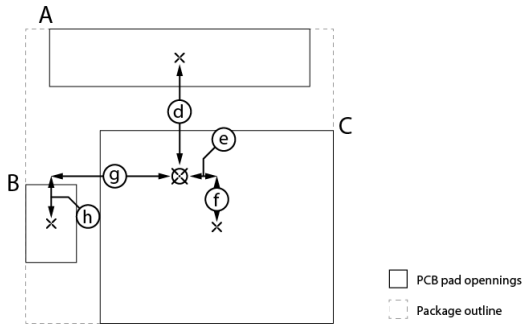


	mm	Inches	
A	4.57	0.180	± 0.10 mm (0.004")
A1	0.41	0.016	± 0.05 mm (0.002")
A2	0.06	0.002	± 0.05 mm (0.002")
A3	0.45	0.018	
B	4.37	0.172	± 0.10 mm (0.004")
B1	0.06	0.002	± 0.05 mm (0.002")
B2	1.55	0.061	
B3	0.96	0.038	± 0.05 mm (0.002")
B4	0.75	0.030	
C	0.48	0.0189	± 0.05 mm (0.002")
C1	0.04	0.0016	
C2	0.43	0.0169	
C3	0.01	0.0004	
D1	3.75	0.148	
D2	0.75	0.030	
G1	0.65	0.026	
G2	1.05	0.041	
S1	3.35	0.132	
S2	2.75	0.108	

Surface finish: ENIG
Ni: 4.5 µm +/- 1.5 µm
Au: 0.09 µm +/- 0.03 µm

Note: Inch measurements are approximate values

Recommended Minimum Footprint



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	3.85	0.85	0.152	0.033
B	0.75	1.15	0.030	0.045
C	3.45	2.85	0.136	0.112

Dimensions

	mm	Inches
d	1.75	0.069
e	0.55	0.022
f	0.75	0.030
g	1.90	0.075
h	0.70	0.028

Note: Inch measurements are approximate values

Mouser Electronics

Authorized Distributor

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GaN Systems:

GS61004B-E01-TY GS61004B-E01-MR

E

Appendix: Datasheet of the Inductor for Si

† RoHS COMPLIANT

High Current Chokes

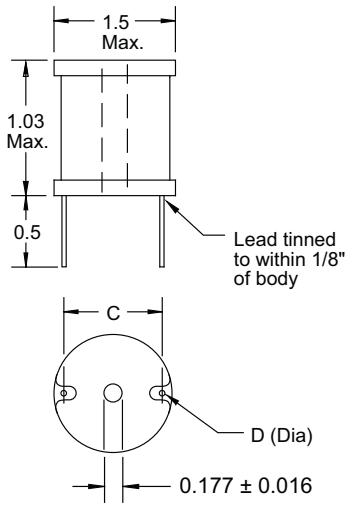
Special Features

- Very high current capacity
- Low DCR
- Epoxy coated ferrite bobbin core
- VW-1 rated shrink tubing to cover winding
- Self-leaded
- Fixed lead spacing
- Center hole for mechanical mounting
- Dielectric withstanding voltage:
  2500 Vrms terminal to shrink tube cover;
  1000 Vrms terminal to core
- Operating temperature -55 to +105 °C

Notes

* Rated current to cause 50 °C max. temperature rise and 5 % max. inductance drop

†RoHS Directive 2002/95/EC Jan. 27, 2003 including annex and RoHS Recast 2011/65/EU June 8, 2011.



Note: Major diameter of #6 screw = 0.138 ”

Dimensions: Inches

1140 Series						
Part Number	L (µH) ±20 % @ 1 KHz	DCR Ω Max.	Irms (A)	Isat (A)	Dim. C Approx.	Dim. D Nom.
1140-1R8M-RC	1.8	0.002	34.5	80.0	1.11	0.081
1140-2R2M-RC	2.2	0.002	34.5	80.0	1.11	0.081
1140-2R7M-RC	2.7	0.003	28.1	80.0	1.11	0.081
1140-3R3M-RC	3.3	0.003	28.1	80.0	1.11	0.081
1140-3R9M-RC	3.9	0.003	28.1	80.0	1.11	0.081
1140-4R7M-RC	4.7	0.003	28.1	80.0	1.11	0.081
1140-5R6M-RC	5.6	0.004	24.4	80.0	1.11	0.081
1140-6R8M-RC	6.8	0.004	24.4	73.5	1.15	0.081
1140-8R2M-RC	8.2	0.004	24.4	70.3	1.15	0.081
	± 10 %					
1140-100K-RC	10	0.005	21.8	65.3	1.15	0.081
1140-120K-RC	12	0.005	21.8	59.6	1.15	0.081
1140-150K-RC	15	0.006	19.9	53.9	1.15	0.081
1140-180K-RC	18	0.008	17.2	49.2	1.15	0.081
1140-220K-RC	22	0.009	16.2	43.7	1.15	0.081
1140-270K-RC	27	0.010	16.0	39.0	1.15	0.081
1140-330K-RC	33	0.011	15.8	36.5	1.15	0.072
1140-390K-RC	39	0.012	15.1	32.3	1.15	0.072
1140-470K-RC	47	0.018	12.3	30.6	1.15	0.072
1140-560K-RC	56	0.019	12.0	27.6	1.15	0.064
1140-680K-RC	68	0.021	11.4	25.2	1.15	0.064
1140-820K-RC	82	0.023	10.9	23.1	1.15	0.064
1140-101K-RC	100	0.025	10.5	20.6	1.15	0.064
1140-121K-RC	120	0.028	9.9	18.6	1.15	0.057
1140-151K-RC	150	0.040	8.3	16.9	1.15	0.057
1140-181K-RC	180	0.045	7.8	15.5	1.15	0.057
1140-221K-RC	220	0.050	7.4	14.0	1.15	0.051
1140-271K-RC	270	0.056	7.0	12.4	1.15	0.051
1140-331K-RC	330	0.074	6.1	11.2	1.15	0.051
1140-391K-RC	390	0.082	5.8	10.4	1.15	0.045
1140-471K-RC	470	0.114	4.9	9.5	1.15	0.045
1140-561K-RC	560	0.125	4.7	8.6	1.15	0.040
1140-681K-RC	680	0.139	4.4	7.9	1.15	0.040
1140-821K-RC	820	0.154	4.2	7.2	1.15	0.040
1140-102K-RC	1000	0.216	3.6	6.5	1.15	0.040
1140-122K-RC	1200	0.232	3.4	5.9	1.14	0.036
1140-152K-RC	1500	0.324	2.9	5.3	1.14	0.036
1140-182K-RC	1800	0.360	2.8	4.9	1.14	0.036
1140-222K-RC	2200	0.494	2.4	4.4	1.10	0.032
1140-272K-RC	2700	0.555	2.2	3.9	1.12	0.032
1140-332K-RC	3300	0.773	1.9	3.6	1.10	0.029
1140-392K-RC	3900	0.845	1.8	3.3	1.10	0.029
1140-472K-RC	4700	1.14	1.6	3.0	1.12	0.029
1140-562K-RC	5600	1.60	1.3	2.8	1.09	0.025
1140-682K-RC	6800	1.76	1.2	2.5	1.12	0.025
1140-822K-RC	8200	1.95	1.2	2.3	1.09	0.023
1140-103K-RC	10,000	2.76	1.0	2.1	1.11	0.023
1140-123K-RC	12,000	3.04	0.9	1.9	1.08	0.020
1140-153K-RC	15,000	3.39	0.9	1.7	1.10	0.020

“-RC” suffix indicates RoHS compliance.

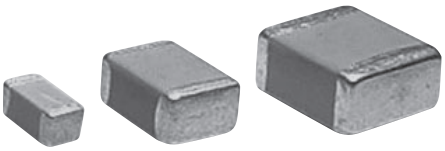
F

Appendix: Datasheet of the Capacitor for Si

NTS Series / NTF Series

RoHS Compliant

Temperature cycle : 1000 cycles



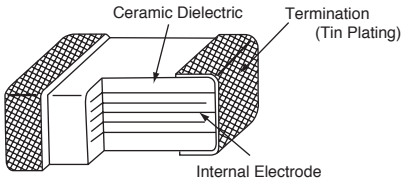
◆FEATURES

1. Large capacitance by small size.
2. Excellent noise absorption.
3. High permissible ripple current capability.
4. NTF: Temperature cycle : 1000 cycles.

◆APPLICATIONS

1. Smoothing circuit of DC-DC converters.
2. On-board power supplies.
3. Voltage regulators for computers.
3. Noise suppressor for various kinds of equipments.
4. High reliability equipments.

◆CONSTRUCTION



◆RATINGS

1. Category Temperature Range	-55 to +125℃
2. Rated Voltage Range	25, 50, 100, 250Vdc
3. Rated Capacitance Range	0.010 to 47μF
4. Rated Capacitance Tolerance	M (±20%) : Standard, K (±10%)
5. Temperature Characteristics	X7R
6. Rated Ripple Current	See No.5 on the following table

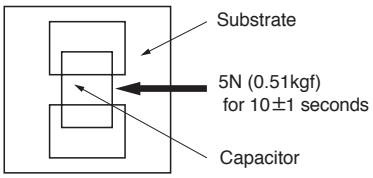
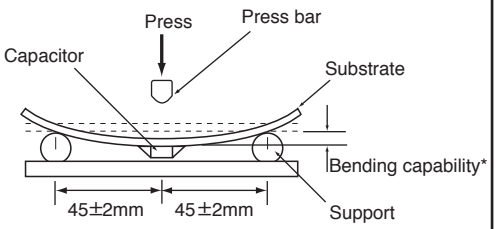
◆SPECIFICATIONS

<table>
<tr><th>No.</th><th>Items</th><th>Specification</th><th>Test Condition</th></tr>
<tr><td>1</td><td>Withstand Voltage</td><td>No abnormality.</td><td>250% of rated voltage shall be applied for 5 seconds.
(Only 250Vdc product : 475V)</td></tr>
<tr><td>2</td><td>Insulation Resistance</td><td>100/CR(MΩ) or 4000(MΩ)
whichever is less.</td><td>Rated voltage shall be applied for 60±5 seconds at temperature 25±2℃.</td></tr>
<tr><td>3</td><td>Rated Capacitance</td><td>Within specified tolerance.</td><td rowspan="2"><table>
<tr><td></td><td>CR≦10μF</td><td>CR>10μF</td></tr>
<tr><td>Temperature</td><td colspan="2">25±2℃</td></tr>
<tr><td>Frequency</td><td>1±0.1kHz</td><td>120±12Hz</td></tr>
<tr><td>Voltage</td><td>1±0.2Vrms</td><td>0.5±0.2Vrms</td></tr>
</table></td></tr>
<tr><td>4</td><td>Dissipation Factor</td><td>5.0% maximum.</td></tr>
<tr><td>5</td><td>Rated Ripple Current</td><td><table>
<tr><td>Size code</td><td>31</td><td>32</td><td>43</td><td>55</td><td>76</td></tr>
<tr><td>Arms</td><td>0.3</td><td>0.5</td><td>1.0</td><td>2.0</td><td>3.0</td></tr>
</table></td><td>10kHz～1MHz (sine curve)
Ripple voltage Vp shall be less than the rated voltage.</td></tr>
</table>

As customer requirement, Chemi-Con has submits the test results according to AEC-Q200 for Multilayer ceramic capacitors. Please contact us for more information.

NTS Series / NTF Series

◆SPECIFICATIONS

No.	Items	Specification	Test Condition
6	Adhesion	No visible damage.	
7	Bend strength of the face plating	Appearance : No visible damage. ΔC/C : ±15%	The substrate shall be bend at a rate of 1mm/s for 5 seconds.  *Bending capability NTS : 1mm NTF : 1mm or 2mm
8	Solderability	Min. 75% of surface of the termination shall be covered with new solder	Solder: Pb Free Solder Temperature: 245±5℃ Dipping Time: 2±0.5sec.
9	Resistance to Soldering Heat	Appearance : No visible damage. ΔC/C : ±15% D.F. : To meet the initial specification. I.R. : To meet the initial specification.	Preheating Condition : Step 1: 100±10℃, 2min. Step 2: 200±10℃, 2min. Solder Temperature : 260±5℃ Dipping Time : 2±0.5 seconds
10	Temperature Cycle	Appearance : No visible damage. ΔC/C : ±15% D.F. : To meet the initial specification. I.R. : To meet the initial specification.	Step 1: Min. Category temperature ±3, 30±3 Step 2: Room temperature, 3 max. Step 3: Max. Category temperature ±3, 30±3 Step 4: Room temperature, 3 max. For above temperature cycle. NTS : For 5 cycles NTF : For 1000 cycles
11	Humidity Load Life	Appearance : No abnormality. ΔC/C : ±15% D.F. : 10% maximum I.R. : 25/C_R(MΩ) or 1000(MΩ) whichever is less.	Temperature : 40±2℃ Humidity : 90 to 95%RH Voltage : Rated voltage Time : 500^{+24}_{0}hours
12	Endurance	Appearance : No abnormality. ΔC/C : ±15% D.F. : 10% maximum I.R. : 50/C_R(MΩ) or 1000(MΩ) whichever is less.	Temperature : 125±3℃ Voltage : Rated voltage Time : 1000^{+48}_{0}hours

*C_R : Rated Capacitance(μF)

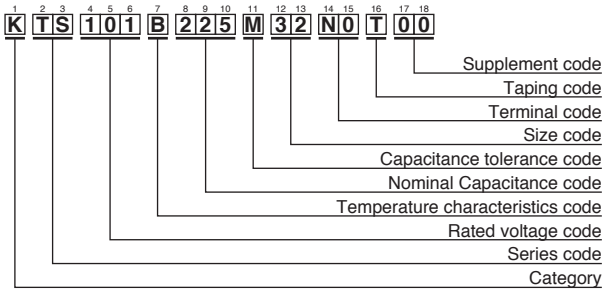
NTS Series

◆STANDARD RATINGS

Rated voltage (Vdc)	Rated Capacitance (μF)	Dimensions(mm) L	W	Tmax.	a	Maximum ripple current (Arms)	Part Number	Taping Quantity per reel (pcs. / reel)
25	1.0	3.2±0.2	1.6±0.2	1.8	0.5±0.3	0.3	KTS250B105M31N0T00	3,000
	1.5						KTS250B155M31N0T00	3,000
	2.2						KTS250B225M31N0T00	3,000
	3.3	3.2±0.4	2.5±0.3	2.6	0.6±0.3	0.5	KTS250B335M32N0T00	1,600
	4.7						KTS250B475M32N0T00	1,600
	6.8						KTS250B685M32N0T00	1,600
	10	4.5±0.4	3.2±0.4	2.8	0.6±0.3	1.0	KTS250B106M43N0T00	800
	15						KTS250B156M43N0T00	800
	22	5.7±0.4	5.0±0.4	2.8	0.8±0.5	2.0	KTS250B226M55N0T00	800
	33			3.0			KTS250B336M55N0T00	800
	47	7.5±0.5	6.3±0.5	4.0	1.0±0.5	3.0	KTS250B476M76N0T00	300
50	0.33	3.2±0.2	1.6±0.2	1.8	0.5±0.3	0.3	KTS500B334M31N0T00	3,000
	0.47						KTS500B474M31N0T00	3,000
	0.68						KTS500B684M31N0T00	3,000
	1.0						KTS500B105M31N0T00	3,000
	1.5	3.2±0.4	2.5±0.3	2.6	0.6±0.3	0.5	KTS500B155M32N0T00	1,600
	2.2						KTS500B225M32N0T00	1,600
	3.3						KTS500B335M32N0T00	1,600
	4.7	4.5±0.4	3.2±0.4	2.8	0.6±0.3	1.0	KTS500B475M43N0T00	800
	6.8						KTS500B685M43N0T00	800
	10	5.7±0.4	5.0±0.4	2.8	0.8±0.5	2.0	KTS500B106M55N0T00	800
	15						KTS500B156M55N0T00	800
	22	7.5±0.5	6.3±0.5	4.0	1.0±0.5	3.0	KTS500B226M76N0T00	300
100	0.1	3.2±0.2	1.6±0.2	1.8	0.5±0.3	0.3	KTS101B104M31N0T00	3,000
	0.15						KTS101B154M31N0T00	3,000
	0.22						KTS101B224M31N0T00	3,000
	0.33						KTS101B334M31N0T00	3,000
	0.47						KTS101B474M31N0T00	3,000
	0.68						KTS101B684M31N0T00	3,000
	1.0	3.2±0.4	2.5±0.3	2.6	0.6±0.3	0.5	KTS101B105M32N0T00	1,600
	1.5						KTS101B155M32N0T00	1,600
	2.2						KTS101B225M32N0T00	1,600
	1.5	4.5±0.4	3.2±0.4	2.8	0.6±0.3	1.0	KTS101B155M43N0T00	800
	2.2						KTS101B225M43N0T00	800
	3.3		3.2±0.5				KTS101B335M43J0T00	800
	4.7			3.2			KTS101B475M43E0T00	800
	3.3	5.7±0.4	5.0±0.4	2.8	0.8±0.5	2.0	KTS101B335M55N0T00	800
	4.7						KTS101B475M55N0T00	800
	6.8			3.2			KTS101B685M55F0T00	800
	6.8	7.5±0.5	6.3±0.5	3.5	1.0±0.5	3.0	KTS101B685M76N0T00	300
250	0.01	3.2±0.2	1.6±0.2	1.8	0.5±0.3	0.3	KTS251B103M31N0T00	3,000
	0.022						KTS251B223M31N0T00	3,000
	0.033						KTS251B333M31N0T00	3,000
	0.047						KTS251B473M31N0T00	3,000
	0.068						KTS251B683M31N0T00	3,000
	0.1						KTS251B104M31N0T00	3,000
	0.15	3.2±0.4	2.5±0.3	2.6	0.6±0.3	0.5	KTS251B154M32N0T00	1,600
	0.22						KTS251B224M32N0T00	1,600
	0.33						KTS251B334M32N0T00	1,600
	0.47	4.5±0.4	3.2±0.4	2.8	0.6±0.3	1.0	KTS251B474M43N0T00	800
	0.68						KTS251B684M43N0T00	800
	1.0	5.7±0.4	5.0±0.4	2.8	0.8±0.5	2.0	KTS251B105M55N0T00	800
	1.5						KTS251B155M55N0T00	800
	1.5	7.5±0.5	6.3±0.5	3.5	1.0±0.5	3.0	KTS251B155M76N0T00	300
	2.2			5.0			KTS251B225M76N0T00	300

※Please consult with us when you consider the rating other than a standard table.

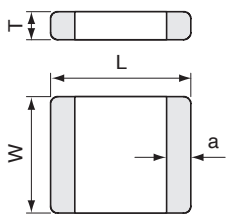
◆PART NUMBERING SYSTEM



Size Code

Size Code	Code JIS	Code EIA
31	3216	1206
32	3225	1210
43	4532	1812
55	5750	2220
76	7563	3025

◆DIMENSIONS



Please refer to"Part Numbering System" of the beginning of a catalog for the details.

NTF Series

◆STANDARD RATINGS

Rated voltage (Vdc)	Rated Capacitance (μF)	Dimensions(mm) L	W	Tmax.	a	Maximum ripple current (Arms)	Part Number	Taping Quantity per reel (pcs. / reel)
25	1.0	3.2±0.3	1.6±0.2	1.8	0.7±0.2	0.3	KTF250B105M31NLT00	3,000
	1.5						KTF250B155M31NLT00	3,000
	2.2						KTF250B225M31NLT00	3,000
	3.3	3.2±0.4	2.5±0.3	2.6	0.7±0.2	0.5	KTF250B335M32NHT00	1,600
	4.7						KTF250B475M32NHT00	1,600
	6.8						KTF250B685M32NHT00	1,600
	10	4.5±0.4	3.2±0.4	2.8	0.7±0.2	1.0	KTF250B106M43NHT00	800
	15						KTF250B156M43NHT00	800
	22	5.7±0.4	5.0±0.4	2.8	1.0±0.4	2.0	KTF250B226M55NHT00	800
	33			3.0			KTF250B336M55NHT00	800
50	0.33	3.2±0.3	1.6±0.2	1.8	0.7±0.2	0.3	KTF500B334M31NLT00	3,000
	0.47						KTF500B474M31NLT00	3,000
	0.68						KTF500B684M31NLT00	3,000
	1.0						KTF500B105M31NLT00	3,000
	1.5	3.2±0.4	2.5±0.3	2.6	0.7±0.2	0.5	KTF500B155M32NHT00	1,600
	2.2						KTF500B225M32NHT00	1,600
	3.3						KTF500B335M32NHT00	1,600
	4.7	4.5±0.4	3.2±0.4	2.8	0.7±0.2	1.0	KTF500B475M43NHT00	800
	6.8						KTF500B685M43NHT00	800
	10	5.7±0.4	5.0±0.4	2.8	1.0±0.4	2.0	KTF500B106M55NHT00	800
	15						KTF500B156M55NHT00	800
100	0.1	3.2±0.3	1.6±0.2	1.8	0.7±0.2	0.3	KTF101B104M31NLT00	3,000
	0.15						KTF101B154M31NLT00	3,000
	0.22						KTF101B224M31NLT00	3,000
	0.33						KTF101B334M31NLT00	3,000
	0.47						KTF101B474M31NLT00	3,000
	0.68						KTF101B684M31NLT00	3,000
	1.0	3.2±0.4	2.5±0.3	2.6	0.7±0.2	0.5	KTF101B105M32NHT00	1,600
	1.5						KTF101B155M32NHT00	1,600
	2.2						KTF101B225M32NHT00	1,600
	1.5	4.5±0.4	3.2±0.4	2.8	0.7±0.2	1.0	KTF101B155M43NHT00	800
	2.2						KTF101B225M43NHT00	800
	3.3		3.2±0.5				KTF101B335M43JHT00	800
	4.7			3.2			KTF101B475M43EHT00	800
	4.7	5.7±0.4	5.0±0.4	2.8	1.0±0.4	2.0	KTF101B475M55NHT00	800
	6.8			3.2			KTF101B685M55FHT00	800
250	0.033	3.2±0.3	1.6±0.2	1.8	0.7±0.2	0.3	KTF251B333M31NLT00	3,000
	0.047						KTF251B473M31NLT00	3,000
	0.068						KTF251B683M31NLT00	3,000
	0.1						KTF251B104M31NLT00	3,000
	0.15	3.2±0.4	2.5±0.3	2.6	0.7±0.2	0.5	KTF251B154M32NLT00	1,600
	0.22						KTF251B224M32NLT00	1,600
	0.33						KTF251B334M32NLT00	1,600
	0.47	4.5±0.4	3.2±0.4	2.8	0.7±0.2	1.0	KTF251B474M43NLT00	800
	0.68						KTF251B684M43NLT00	800
	1.0	5.7±0.4	5.0±0.4	2.8	1.0±0.4	2.0	KTF251B105M55NLT00	800
	1.5						KTF251B155M55NLT00	800

※Please consult with us when you consider the rating other than a standard table.

◆PART NUMBERING SYSTEM

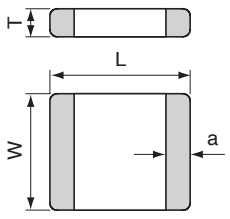
1	2 3	4 5 6	7	8 9 10	11	12 13	14 15	16	17 18
K	TF	101	B	225	M	32	NH	T	00

- 1 Category
- 2 3 Series code
- 4 5 6 Rated voltage code
- 7 Temperature characteristics code
- 8 9 10 Nominal Capacitance code
- 11 Capacitance tolerance code
- 12 13 Size code
- 14 15 Terminal code (Bending NL:1mm, NH:2mm)
- 16 Taping code
- 17 18 Supplement code

Size Code

Size Code	Code JIS	Code EIA
31	3216	1206
32	3225	1210
43	4532	1812
55	5750	2220
76	7563	3025

◆DIMENSIONS

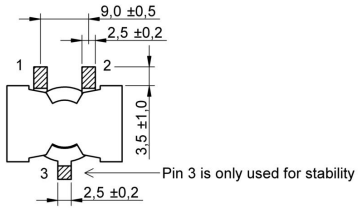


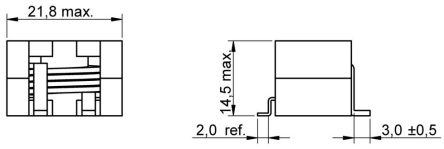
Please refer to"Part Numbering System" of the beginning of a catalog for the details.

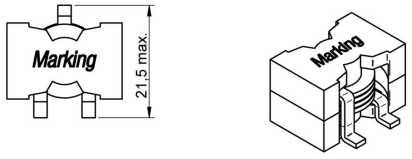
G

Appendix: Datasheet of the Inductor for GaN

A Dimensions: [mm]



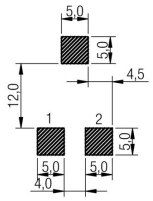




Scale - 1:1

Reference on drawing	Description
Marking	7443632200 (Article Number)
Date code	YYWW

B Recommended land pattern: [mm]



Scale - 1:1

C Schematic:

D Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance	100 kHz/ 10 mA	L	22	µH	± 15%
Rated current	ΔT = 50 K	I_R	12.5	A	max.
Saturation current	|ΔL/L| < 30%	I_{sat}	15.0	A	typ.
DC Resistance	@ 20°C	R_{DC}	10.65	mΩ	±10%
Self resonant frequency		f_{res}	12.5	MHz	typ.

E General information:

It is recommended that the temperature of the part does not exceed 125°C under worst case operating conditions.

- Ambient temperature: -40°C to +75°C (refering to I_R)
- Operating temperature: -40°C to +125°C
- Storage temperature (on tape & reel): -20°C to +40°C; 75% RH max.
- Test conditions of Electrical Properties: 20°C, 33% RH if not specified differently

REV	DATE	BY	CHECKED
2.3	2014-09-16	SSt	BD
2.2	2014-02-06	SSt	BD
2.1	2013-12-17	SSt	SSt
2.0	2013-06-17	SSt	BD
1.0	2010-06-12	BD	

Projection

Würth Elektronik eiSos GmbH & Co. KG
EMC & Inductive Solutions
Max-Eyth-Str. 1
74638 Waldenburg
Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
eiSos@we-online.com

DESCRIPTION

WE-HCF SMD High Current Inductor

Order.- No.

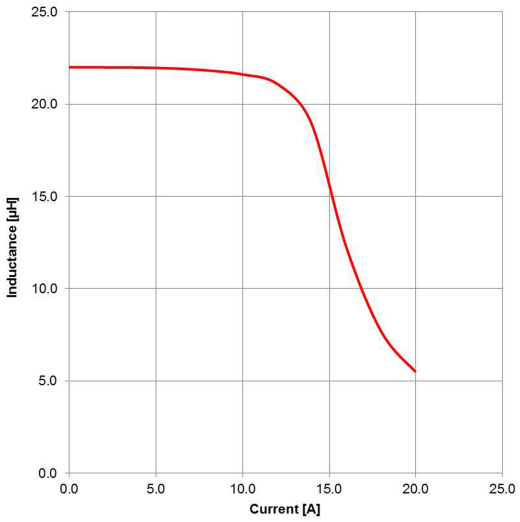
7443632200

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

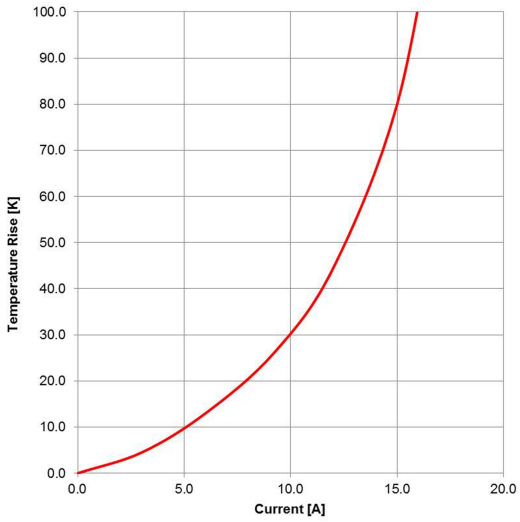
SIZE A4

Size: 2013

F1 Typical Inductance vs. Current Characteristics:



F2 Typical Temperature Rise vs. Current Characteristics:



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2.2	2014-02-06	SSt	BD
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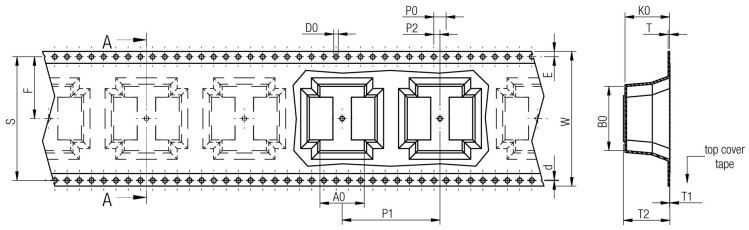
COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE

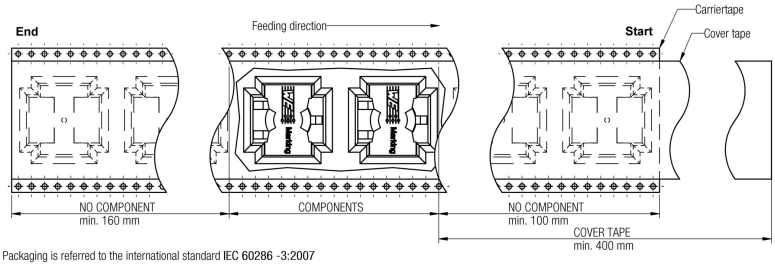
A4

Size: 2013

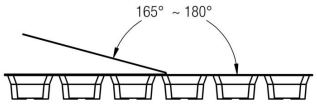
G Packaging Specification - Tape and Reel [mm]:



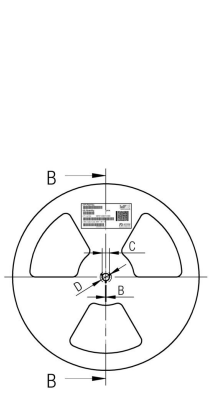
		A0	B0	W	T	T1	T2	K0	d	D0	E	S	F	P0	P1	P2	Tape	VPE / packaging unit
tolerance		typ.	typ.	± 0,3	± 0,05	typ.	max.	typ.	± 0,05	+0,1 -0,0	± 0,1	± 0,1	± 0,1	± 0,1	± 0,1	± 0,1		
size	2013	14,50	21,00	44,00	0,50	0,10	15,20	14,60	0,20	1,50	1,75	40,40	20,20	4,00	32,00	2,00	Polystyrene	100



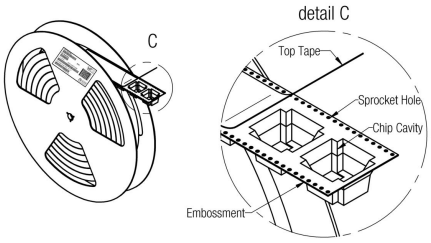
Packaging is referred to the international standard IEC 60286 -3:2007



Pull-of force		
Tape width	44 mm	0,1 N - 1,3 N



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	min.	+ 1,5	max.	min.	max.
Tape width	44 mm	330,00	1,50	13,00	20,20	100,00	44,40	50,40	43,90	47,40



2.3	2014-09-16	SSt	BD
2.2	2014-02-06	SSt	BD
2.1	2013-12-17	SSt	SSt
2.0	2013-06-17	SSt	BD
1.0	2010-06-12	BD	
REV	DATE	BY	CHECKED

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DESCRIPTION

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Order.- No.

7443632200

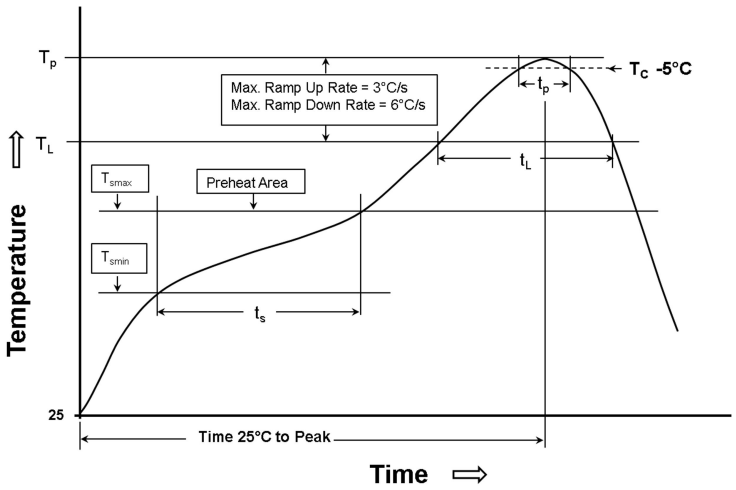
COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 2013

H Soldering Specifications:

H1: Classification Reflow Profile for SMT components:



H2: Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (t_s) from (T_{smin} to T_{smax})	 150°C 200°C 60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/ second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217°C 60-150 seconds
Peak package body temperature (T_p)	See Table H3
Time within 5°C of actual peak temperature (t_p)	20-30 seconds
Ramp-down rate (T_P to T_L)	6°C/ second max.
Time 25°C to peak temperature	8 minutes max.

refer to IPC/JEDEC J-STD-020D

H3: Package Classification Reflow Temperature

	Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
PB-Free Assembly	< 1.6 mm	260°C	260°C	260°C
PB-Free Assembly	1.6 - 2.5 mm	260°C	250°C	245°C
PB-Free Assembly	≥ 2.5 mm	250°C	245°C	245°C

refer to IPC/JEDEC J-STD-020D

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2.1	2013-12-17	SSt	SSt
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Order.- No.

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COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE A4

Size: 2013

I Cautions and Warnings:

The following conditions apply to all goods within the product series of WE-HCF of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the data sheet have to be complied with.

The usage and operation of the product within ambient conditions, which probably alloy or harm the wire isolation, has to be avoided.

If the product is potted in customer applications, the potting material might shrink during and after hardening. The product is exposed to the pressure of the potting material with the effect that the core, wire and termination is possibly damaged by this pressure and so the electrical as well as the mechanical characteristics are endangered to be affected. After the potting material is cured, the core, wire and termination of the product have to be checked if any reduced electrical or mechanical functions or destructions have occurred.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply to customer specific products.

Cleaning agents that are used to clean the customer application might damage or change the characteristics of the component, body, pins or termination.

Direct mechanical impact to the product shall be prevented as the core material could flake or in the worst case it could break.

Product specific:
Follow all instructions mentioned in the data sheet, especially:

- The soldering profile has to be complied with according to the technical reflow soldering specification, otherwise this will void the warranty.
- All products shall be used before the end of the period of 12 months based on the product date code, if not a 100% solderability can´t be ensured.
- Violation of the technical product specifications such as exceeding the nominal rated current will void the warranty.
- Due to heavy weight of the components of size 2013, strong forces and high accelerations might have the effect to damage the electrical connection or to harm the circuit board and will void the warranty.

The general and product specific cautions comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable; however, no responsibility is assumed for inaccuracies or incompleteness.

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2.3	2014-09-16	SSt	BD
2.2	2014-02-06	SSt	BD
2.1	2013-12-17	SSt	SSt
2.0	2013-06-17	SSt	BD
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7443632200

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE

A4

Size: 2013

J Important Notes:

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications.

In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

Therefore, customer is cautioned to verify that data sheets are current before placing orders. The current data sheets can be downloaded at www.we-online.com.

3. Best Care and Attention
Any product-specific notes, cautions and warnings must be strictly observed. Any disregard will result in the loss of warranty.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered.
The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG.

Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.

REV	DATE	BY	CHECKED
2.3	2014-09-16	SSt	BD
2.2	2014-02-06	SSt	BD
2.1	2013-12-17	SSt	SSt
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COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE

A4

Size: 2013

H

Appendix: Datasheet of the Capacitor for GaN

TDK

MULTILAYER CERAMIC CHIP CAPACITORS

CGA Series
Automotive Grade
General (Up to 50V)

Type:

CGA1 [EIA CC0201]
CGA2 [EIA CC0402]
CGA3 [EIA CC0603]
CGA4 [EIA CC0805]
CGA5 [EIA CC1206]
CGA6 [EIA CC1210]
CGA8 [EIA CC1812]
CGA9 [EIA CC2220]

Issue date:
Sep 2013

REMINDERS

Please read before using this product

SAFETY REMINDERS

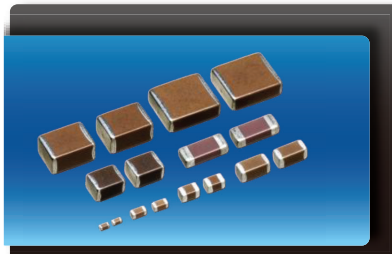
REMINDERS

1. If you intend to use a product listed in this catalog for a purpose that may cause loss of life or other damage, you must contact our company's sales window.
2. We may modify products or discontinue production of a product listed in this catalog without prior notification.
3. We provide "Delivery Specification" that explain precautions for the specifications and safety of each product listed in this catalog. We strongly recommend that you exchange these delivery specifications with customers that use one of these products.
4. If you plan to export a product listed in this catalog, keep in mind that it may be a restricted item according to the "Foreign Exchange and Foreign Trade Control Law". In such cases, it is necessary to acquire export permission in harmony with this law.
5. Any reproduction or transferring of the contents of this catalog is prohibited without prior permission from our company.
6. We are not responsible for problems that occur related to the intellectual property rights or other rights of our company or a third party when you use a product listed in this catalog. We do not grant license of these rights.
7. This catalog only applies to products purchased through our company or one of our company's official agencies. This catalog does not apply to products that are purchased through other third parties.

Notice : Effective January 2013, TDK will use a new catalog part number which adds product thickness and packaging specification detail. This new part number should be referenced on all catalog orders going forward, and is not applicable for OEM part number orders. Please be aware the last five digits of the TDK catalog part number will differ from the TDK item description (internal control number) on the product label. Contact your local TDK Sales representative for more information.

(Example)

Catalog Issued date	TDK Part Number (In Catalog)	TDK Item Description (On Delivery Label)
Prior to January 2013	C1608C0G1E103J	C1608C0G1E103JT000N
January 2013 and Later	C1608C0G1E103J080AA	C1608C0G1E103JT000N



CGA Series

General (Up to 50V)

Type: CGA1 [EIA CC0201], CGA2 [EIA CC0402], CGA3 [EIA CC0603], CGA4 [EIA CC0805], CGA5 [EIA CC1206], CGA6 [EIA CC1210], CGA8 [EIA CC1812], CGA9 [EIA CC2220]

Lead Free | RoHS COMPLIANT | Ecological

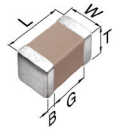
Features

- High capacitance has been achieved through precision technologies that enable the use of multiple thinner ceramic dielectric layers.
- A monolithic structure ensures superior mechanical strength and reliability.
- Low ESL and excellent frequency characteristics allow for a circuit design that closely conforms to theoretical values.
- Low self-heating and high ripple resistance due to low ESR.
- AEC-Q200 compliant.

Applications

- Automotive engine control units
- Automotive sensor modules
- Automotive battery line smoothing
- Applications requiring higher reliability
- Switching power supply smoothing

Shape & Dimensions



L	Body Length
W	Body Width
T	Body Height
B	Terminal Width
G	Terminal Spacing

Part Number Construction

CGA • 6 • P • 1 • X7S • 0J • 476 • M • 250 • A • C

Series Name

Dimensions L x W (mm)

Code	Length	Width	Terminal
1	0.60 ± 0.03	0.30 ± 0.03	0.10 min.
2	1.00 ± 0.05	0.50 ± 0.05	0.10 min.
3	1.60 ± 0.10	0.80 ± 0.10	0.20 min.
4	2.00 ± 0.20	1.25 ± 0.20	0.20 min.
5	3.20 ± 0.20	1.60 ± 0.20	0.20 min.
6	3.20 ± 0.40	2.50 ± 0.30	0.20 min.
8	4.50 ± 0.40	3.20 ± 0.40	0.20 min.
9	5.70 ± 0.40	5.00 ± 0.40	0.20 min.

*Dimension tolerance are typical values

Thickness T Code (mm)

Code	Thickness
A	0.30 mm
B	0.50 mm
C	0.60 mm
E	0.80 mm
F	0.85 mm
H	1.15 mm
J	1.25 mm
L	1.60 mm
M	2.00 mm
N	2.30 mm
P	2.50 mm
Q	2.80 mm
R	3.20 mm

Voltage Condition for Life Test

Symbol	Condition
1	1 × R.V.
2	2 × R.V.
3	1.5 × R.V.

Temperature Characteristics

Temperature Characteristics	Capacitance Change	Temperature Range
C0G	0±30 ppm/°C	-55 to +125°C
X5R	±15%	-55 to + 85°C
X7R	±15%	-55 to +125°C
X7S	±22%	-55 to +125°C

Rated Voltage (DC)

Code	Voltage (DC)
0J	6.3V
1A	10V
1C	16V
1E	25V
1V	35V
1H	50V

Nominal Capacitance (pF)

The capacitance is expressed in three digit codes and in units of pico Farads (pF). The first and second digits identify the first and second significant figures of the capacitance. The third digit identifies the multiplier. R designates a decimal point.

Ex. 0R2 = 0.2pF; 103 = 10,000pF; 105 = 1,000,000pF = 1,000nF = 1µF

Capacitance Tolerance

Code	Tolerance
C	± 0.25pF
D	± 0.50pF
J	± 5%
K	± 10%
M	± 20%

Nominal Thickness

Code	Thickness
030	0.30 mm
050	0.50 mm
060	0.60 mm
125	1.25 mm

*See Thickness T Code for complete list

Packaging Style

Code	Style
A	178" Reel, 4mm Pitch
B	178" Reel, 2mm Pitch
K	178" Reel, 8mm Pitch

Special Reserved Code

Code	Description
A, B	TDK Internal Code

004-01 / 20130905 / mlcc_automotive_general_en

Capacitance Range Chart

CGA1(0603) [EIA CC0201]

Capacitance Range Chart

Temperature Characteristics: X7R (±15%)

Rated Voltage: 50V (1H), 25V (1E), 16V (1C), 10V (1A), 6.3V (0J)

Capacitance (pF)	Code	Tolerance	X7R				
			1H (50V)	1E (25V)	1C (16V)	1A (10V)	0J (6.3V)
100	101	K : ± 10% M : ± 20%					
150	151						
220	221						
330	331						
470	471						
680	681						
1000	102						
1500	152						
2200	222						
3300	332						
4700	472						
6800	682						
10000	103						

Standard Thickness

0.30 mm

Capacitance Range Chart

CGA2(1005) [EIA CC0402]

Capacitance Range Chart

Temperature Characteristics: C0G (0 ± 30ppm/ºC), X5R (±15%), X7R (±15%)
Rated Voltage: 50V (1H), 35V (1V), 25V (1E), 16V (1C), 10V (1A), 6.3 (0J)

Capacitance (pF)	Code	Tolerance	C0G	X5R					X7R					
			1H (50V)	1H (50V)	1V (35V)	1E (25V)	1C (16V)	1A (10V)	1H (50V)	1V (35V)	1E (25V)	1C (16V)	1A (10V)	0J (6.3V)
1	010	C : ± 0.25pF												
1.5	1R5	D : ± 0.50pF												
2	020	J : ± 5%												
2.2	2R2	K : ± 10%												
3	030	M : ± 20%												
3.3	3R3													
4	040													
4.7	4R7													
5	050													
6	060													
6.8	6R8													
7	070													
8	080													
9	090													
10	100													
12	120													
15	150													
18	180													
22	220													
27	270													
33	330													
39	390													
47	470													
56	560													
68	680													
82	820													
100	101													
120	121													
150	151													
180	181													
220	221													
270	271													
330	331													
390	391													
470	471													
560	561													
680	681													
820	821													
1,000	102													
1,500	152													
2,200	222													
3,300	332													
4,700	472													
6,800	682													
10,000	103													
15,000	153													
22,000	223													
33,000	333													
47,000	473													
68,000	683													
100,000	104													
150,000	154													
220,000	224													

Standard Thickness

0.50 mm

Capacitance Range Chart

CGA3(1608) [EIA CC0603]

Capacitance Range Chart

Temperature Characteristics: C0G (0 ± 30ppm/ºC)
Rated Voltage: 50V (1H)

Capacitance (pF)	Code	Tolerance	C0G 1H (50V)
1	010	C: ± 0.25pF D: ± 0.50pF J: ± 5% K: ± 10% M: ± 20%	
1.5	1R5		
2	020		
2.2	2R2		
3	030		
3.3	3R3		
4	040		
4.7	4R7		
5	050		
6	060		
6.8	6R8		
7	070		
8	080		
9	090		
10	100		
12	120		
15	150		
18	180		
22	220		
27	270		
33	330		
39	390		
47	470		
56	560		
68	680		
82	820		
100	101		
120	121		
150	151		
180	181		
220	221		
270	271		
330	331		
390	391		
470	471		
560	561		
680	681		
820	821		

Standard Thickness
0.80 mm

Capacitance Range Chart

CGA3(1608) [EIA CC0603]

Capacitance Range Chart

Temperature Characteristics: C0G (0 ± 30ppm/ºC), X5R (±15%), X7R (±15%)
Rated Voltage: 50V (1H), 35V (1V), 25V (1E), 16V (1C), 10V (1A), 6.3V (0J)

Capacitance (pF)	Code	Tolerance	C0G	X5R						X7R				
			1H (50V)	1H (50V)	1V (35V)	1E (25V)	1C (16V)	1A (10V)	0J (6.3V)	1H (50V)	1V (35V)	1E (25V)	1C (16V)	0J (6.3V)
1,000	102	J: ± 5%												
1,200	122	K: ± 10%												
1,500	152	M: ± 20%												
1,800	182													
2,200	222													
2,700	272													
3,300	332													
3,900	392													
4,700	472													
5,600	562													
6,800	682													
8,200	822													
10,000	103													
15,000	153													
22,000	223													
33,000	333													
47,000	473													
68,000	683													
100,000	104													
150,000	154													
220,000	224													
330,000	334													
470,000	474													
680,000	684													
1,000,000	105													
1,500,000	155													
2,200,000	225													
3,300,000	335													
4,700,000	475													

Standard Thickness

0.80 mm

Capacitance Range Chart

CGA4(2012) [EIA CC0805]

Capacitance Range Chart

Temperature Characteristics: C0G (0 ± 30ppm/ºC), X5R (±15%), X7R (±15%)
Rated Voltage: 50V (1H), 35V (1V), 25V (1E), 16V (1C), 10V (1A), 6.3V (0J)

Capacitance (pF)	Code	Tolerance	C0G	X5R					X7R					
			1H (50V)	1H (50V)	1V (35V)	1E (25V)	1C (16V)	1A (10V)	1H (50V)	1V (35V)	1E (25V)	1C (16V)	1A (10V)	0J (6.3V)
1,000	102	J: ± 5% K: ± 10% M: ± 20%												
1,200	122													
1,500	152													
1,800	182													
2,200	222													
2,700	272													
3,300	332													
3,900	392													
4,700	472													
5,600	562													
6,800	682													
8,200	822													
10,000	103													
15,000	153													
22,000	223													
33,000	333													
100,000	104													
150,000	154													
220,000	224													
330,000	334													
470,000	474													
680,000	684													
1,000,000	105													
1,500,000	155													
2,200,000	225													
3,300,000	335													
4,700,000	475													
6,800,000	685													
10,000,000	106													

Standard Thickness

0.60 mm 0.85 mm 1.25 mm

Capacitance Range Chart

CGA5(3216) [EIA CC1206]

Capacitance Range Chart

Temperature Characteristics: C0G (0 ± 30ppm/ºC), X5R (±15%), X7R (±15%)
Rated Voltage: 50V (1H), 35V (1V), 25V (1E), 16V (1C), 6.3V (0J)

Capacitance (pF)	Code	Tolerance	C0G	X5R				X7R				
			1H (50V)	1H (50V)	1V (35V)	1E (25V)	1C (16V)	1H (50V)	1V (35V)	1E (25V)	1C (16V)	0J (6.3V)
4,700	472	J: ± 5%										
5,600	562	K: ± 10%										
6,800	682	M: ± 20%										
8,200	822											
10,000	103											
15,000	153											
22,000	223											
33,000	333											
47,000	473											
68,000	683											
100,000	104											
470,000	474											
680,000	684											
1,000,000	105											
1,500,000	155											
2,200,000	225											
3,300,000	335											
4,700,000	475											
6,800,000	685											
10,000,000	106											
15,000,000	156											
22,000,000	226											

Standard Thickness
- 0.60 mm
- 0.85 mm
- 1.15 mm
- 1.60 mm

Capacitance Range Chart

CGA6(3225) [EIA CC1210]

Capacitance Range Chart

Temperature Characteristics: C0G (0 ± 30ppm/ºC), X7R (±15%), X7S (±22%)
Rated Voltage: 50V (1H), 25V (1E), 16V (1C), 6.3V (0J)

Capacitance (pF)	Code	Tolerance	C0G	X7R			X7S	
			1H (50V)	1H (50V)	1E (25V)	1C (16V)	1H (50V)	0J (6.3V)
22,000	223	J: ± 5%						
33,000	333	K: ± 10%						
47,000	473	M: ± 20%						
68,000	683							
100,000	104							
1,000,000	105							
1,500,000	155							
2,200,000	225							
3,300,000	335							
4,700,000	475							
6,800,000	685							
10,000,000	106							
15,000,000	156							
22,000,000	226							
33,000,000	336							
47,000,000	476							

Standard Thickness
- 1.25 mm
- 1.60 mm
- 2.00 mm
- 2.30 mm
- 2.50 mm

Capacitance Range Chart

CGA8(4532) [EIA CC1812]

Capacitance Range Chart

Temperature Characteristics: C0G (0 ± 30ppm/ºC), X7R (±15%)
Rated Voltage: 50V (1H), 25V (1E), 16V (1C)

Capacitance (pF)	Code	Tolerance	C0G	X7R		
			1H (50V)	1H (50V)	1E (25V)	1C (16V)
47,000	473	J: ± 5%				
68,000	683	K: ± 10%				
100,000	104	M: ± 20%				
150,000	154					
220,000	224					
1,500,000	155					
2,200,000	225					
3,300,000	335					
4,700,000	475					
6,800,000	685					
10,000,000	106					
15,000,000	156					
22,000,000	226					
33,000,000	336					

Standard Thickness
- 1.60 mm
- 2.00 mm
- 2.30 mm
- 2.50 mm
- 2.80 mm
- 3.20 mm

Capacitance Range Chart

CGA9(5750) [EIA CC2220]

Capacitance Range Chart

Temperature Characteristics: X7R (±15%)
Rated Voltage: 50V (1H), 25V (1E), 16V (1C)

Capacitance (pF)	Code	Tolerance	X7R		
			1H (50V)	1E (25V)	1C (16V)
4,700,000	475	K: ± 10%			
6,800,000	685	M: ± 20%			
10,000,000	106				
15,000,000	156				
22,000,000	226				
47,000,000	476				

Standard Thickness
- 2.00 mm
- 2.30 mm
- 2.50 mm

Capacitance Range Table

Class 1 (Temperature Compensating)

Temperature Characteristics: C0G (-55 to +125ºC, 0 ± 30 ppm/ºC)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number
				Rated Voltage Edc: 50V
1 pF	1005	0.50 ± 0.05	± 0.25pF	CGA2B2C0G1H010C050BA
	1608	0.80 ± 0.10	± 0.25pF	CGA3E2C0G1H010C080AA
1.5 pF	1005	0.50 ± 0.05	± 0.25pF	CGA2B2C0G1H1R5C050BA
	1608	0.80 ± 0.10	± 0.25pF	CGA3E2C0G1H1R5C080AA
2 pF	1005	0.50 ± 0.05	± 0.25pF	CGA2B2C0G1H020C050BA
	1608	0.80 ± 0.10	± 0.25pF	CGA3E2C0G1H020C080AA
2.2 pF	1005	0.50 ± 0.05	± 0.25pF	CGA2B2C0G1H2R2C050BA
	1608	0.80 ± 0.10	± 0.25pF	CGA3E2C0G1H2R2C080AA
3 pF	1005	0.50 ± 0.05	± 0.25pF	CGA2B2C0G1H030C050BA
	1608	0.80 ± 0.10	± 0.25pF	CGA3E2C0G1H030C080AA
3.3 pF	1005	0.50 ± 0.05	± 0.25pF	CGA2B2C0G1H3R3C050BA
	1608	0.80 ± 0.10	± 0.25pF	CGA3E2C0G1H3R3C080AA
4 pF	1005	0.50 ± 0.05	± 0.25pF	CGA2B2C0G1H040C050BA
	1608	0.80 ± 0.10	± 0.25pF	CGA3E2C0G1H040C080AA
4.7 pF	1005	0.50 ± 0.05	± 0.25pF	CGA2B2C0G1H4R7C050BA
	1608	0.80 ± 0.10	± 0.25pF	CGA3E2C0G1H4R7C080AA
5 pF	1005	0.50 ± 0.05	± 0.25pF	CGA2B2C0G1H050C050BA
	1608	0.80 ± 0.10	± 0.25pF	CGA3E2C0G1H050C080AA
6 pF	1005	0.50 ± 0.05	± 0.50pF	CGA2B2C0G1H060D050BA
	1608	0.80 ± 0.10	± 0.50pF	CGA3E2C0G1H060D080AA
6.8 pF	1005	0.50 ± 0.05	± 0.50pF	CGA2B2C0G1H6R8D050BA
	1608	0.80 ± 0.10	± 0.50pF	CGA3E2C0G1H6R8D080AA
7 pF	1005	0.50 ± 0.05	± 0.50pF	CGA2B2C0G1H070D050BA
	1608	0.80 ± 0.10	± 0.50pF	CGA3E2C0G1H070D080AA
8 pF	1005	0.50 ± 0.05	± 0.50pF	CGA2B2C0G1H080D050BA
	1608	0.80 ± 0.10	± 0.50pF	CGA3E2C0G1H080D080AA
9 pF	1005	0.50 ± 0.05	± 0.50pF	CGA2B2C0G1H090D050BA
	1608	0.80 ± 0.10	± 0.50pF	CGA3E2C0G1H090D080AA
10 pF	1005	0.50 ± 0.05	± 0.50pF	CGA2B2C0G1H100D050BA
	1608	0.80 ± 0.10	± 0.50pF	CGA3E2C0G1H100D080AA
12 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H120J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H120J080AA
15 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H150J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H150J080AA
18 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H180J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H180J080AA
22 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H220J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H220J080AA
27 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H270J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H270J080AA
33 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H330J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H330J080AA
39 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H390J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H390J080AA
47 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H470J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H470J080AA
56 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H560J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H560J080AA
68 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H680J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H680J080AA
82 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H820J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H820J080AA
100 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H101J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H101J080AA
120 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H121J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H121J080AA
150 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H151J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H151J080AA
180 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H181J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H181J080AA

Capacitance Range Table

Class 1 (Temperature Compensating)

Temperature Characteristics: C0G (-55 to +125ºC, 0 ± 30 ppm/ºC)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number
				Rated Voltage Edc: 50V
220 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H221J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H221J080AA
270 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H271J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H271J080AA
330 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H331J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H331J080AA
390 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H391J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H391J080AA
470 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H471J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H471J080AA
560 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H561J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H561J080AA
680 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H681J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H681J080AA
820 pF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H821J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H821J080AA
1 nF	1005	0.50 ± 0.05	± 5%	CGA2B2C0G1H102J050BA
	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H102J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H102J060AA
1.2 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H122J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H122J060AA
1.5 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H152J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H152J060AA
1.8 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H182J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H182J060AA
2.2 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H222J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H222J060AA
2.7 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H272J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H272J060AA
3.3 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H332J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H332J060AA
3.9 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H392J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H392J060AA
4.7 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H472J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H472J060AA
	3216	0.60 ± 0.15	± 5%	CGA5C2C0G1H472J060AA
5.6 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H562J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H562J060AA
	3216	0.60 ± 0.15	± 5%	CGA5C2C0G1H562J060AA
6.8 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H682J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H682J060AA
	3216	0.60 ± 0.15	± 5%	CGA5C2C0G1H682J060AA
8.2 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H822J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H822J060AA
	3216	0.60 ± 0.15	± 5%	CGA5C2C0G1H822J060AA
10 nF	1608	0.80 ± 0.10	± 5%	CGA3E2C0G1H103J080AA
	2012	0.60 ± 0.15	± 5%	CGA4C2C0G1H103J060AA
	3216	0.60 ± 0.15	± 5%	CGA5C2C0G1H103J060AA
15 nF	2012	0.85 ± 0.15	± 5%	CGA4F2C0G1H153J085AA
	3216	0.60 ± 0.15	± 5%	CGA5C2C0G1H153J060AA
22 nF	2012	1.25 ± 0.20	± 5%	CGA4J2C0G1H223J125AA
	3216	0.60 ± 0.15	± 5%	CGA5C2C0G1H223J060AA
	3225	1.25 ± 0.20	± 5%	CGA6J2C0G1H223J125AA
33 nF	2012	1.25 ± 0.20	± 5%	CGA4J2C0G1H333J125AA
	3216	0.85 ± 0.15	± 5%	CGA5F2C0G1H333J085AA
	3225	1.60 ± 0.20	± 5%	CGA6L2C0G1H333J160AA
47 nF	3216	1.15 ± 0.15	± 5%	CGA5H2C0G1H473J115AA
	3225	2.00 ± 0.20	± 5%	CGA6M2C0G1H473J200AA
	4532	1.60 ± 0.20	± 5%	CGA8L2C0G1H473J160KA

Capacitance Range Table

Class 1 (Temperature Compensating)

Temperature Characteristics: C0G (-55 to +125ºC, 0 ± 30 ppm/ºC)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number
				Rated Voltage Edc: 50V
68 nF	3216	1.60 ± 0.20	± 5%	CGA5L2C0G1H683J160AA
	3225	2.00 ± 0.20	± 5%	CGA6M2C0G1H683J200AA
	4532	1.60 ± 0.20	± 5%	CGA8L2C0G1H683J160KA
100 nF	3216	1.60 ± 0.20	± 5%	CGA5L2C0G1H104J160AA
	3225	2.50 ± 0.30	± 5%	CGA6P2C0G1H104J250AA
	4532	2.00 ± 0.20	± 5%	CGA8M2C0G1H104J200KA
150 nF	4532	2.50 ± 0.30	± 5%	CGA8P2C0G1H154J250KA
220 nF	4532	3.20 ± 0.30	± 5%	CGA8R2C0G1H224J320KA

Class 2 (Temperature Stable)

Temperature Characteristics: X5R (-55 to +85ºC, ±15%)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number			
				Rated Voltage Edc: 50V	Rated Voltage Edc: 35V	Rated Voltage Edc: 25V	Rated Voltage Edc: 16V
220 pF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H221K050BA			
			± 20%	CGA2B2X5R1H221M050BA			
330 pF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H331K050BA			
			± 20%	CGA2B2X5R1H331M050BA			
470 pF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H471K050BA			
			± 20%	CGA2B2X5R1H471M050BA			
680 pF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H681K050BA			
			± 20%	CGA2B2X5R1H681M050BA			
1 nF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H102K050BA			
			± 20%	CGA2B2X5R1H102M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H102K080AA			
			± 20%	CGA3E2X5R1H102M080AA			
1.5 nF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H152K050BA			
			± 20%	CGA2B2X5R1H152M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H152K080AA			
			± 20%	CGA3E2X5R1H152M080AA			
2.2 nF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H222K050BA			
			± 20%	CGA2B2X5R1H222M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H222K080AA			
			± 20%	CGA3E2X5R1H222M080AA			
3.3 nF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H332K050BA			
			± 20%	CGA2B2X5R1H332M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H332K080AA			
			± 20%	CGA3E2X5R1H332M080AA			
4.7 nF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H472K050BA			
			± 20%	CGA2B2X5R1H472M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H472K080AA			
			± 20%	CGA3E2X5R1H472M080AA			
6.8 nF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1H682K050BA			
			± 20%	CGA2B2X5R1H682M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H682K080AA			
			± 20%	CGA3E2X5R1H682M080AA			
10 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X5R1H103K050BB	CGA2B3X5R1V103K050BB	CGA2B2X5R1E103K050BA	
			± 20%	CGA2B3X5R1H103M050BB	CGA2B3X5R1V103M050BB	CGA2B2X5R1E103M050BA	
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H103K080AA			
			± 20%	CGA3E2X5R1H103M080AA			
15 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X5R1H153K050BB	CGA2B3X5R1V153K050BB	CGA2B2X5R1E153K050BA	
			± 20%	CGA2B3X5R1H153M050BB	CGA2B3X5R1V153M050BB	CGA2B2X5R1E153M050BA	
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H153K080AA			
			± 20%	CGA3E2X5R1H153M080AA			
22 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X5R1H223K050BB	CGA2B3X5R1V223K050BB	CGA2B2X5R1E223K050BA	
			± 20%	CGA2B3X5R1H223M050BB	CGA2B3X5R1V223M050BB	CGA2B2X5R1E223M050BA	
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H223K080AA			
			± 20%	CGA3E2X5R1H223M080AA			

Capacitance Range Table

Class 2 (Temperature Stable)

Temperature Characteristics: X5R (-55 to +85ºC, ±15%)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number			
				Rated Voltage Edc: 50V	Rated Voltage Edc: 35V	Rated Voltage Edc: 25V	Rated Voltage Edc: 16V
33 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X5R1H333K050BB	CGA2B3X5R1V333K050BB	CGA2B2X5R1E333K050BA	CGA2B2X5R1C333K050BA
			± 20%	CGA2B3X5R1H333M050BB	CGA2B3X5R1V333M050BB	CGA2B2X5R1E333M050BA	CGA2B2X5R1C333M050BA
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H333K080AA			
			± 20%	CGA3E2X5R1H333M080AA			
47 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X5R1H473K050BB	CGA2B3X5R1V473K050BB	CGA2B2X5R1E473K050BA	CGA2B2X5R1C473K050BA
			± 20%	CGA2B3X5R1H473M050BB	CGA2B3X5R1V473M050BB	CGA2B2X5R1E473M050BA	CGA2B2X5R1C473M050BA
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H473K080AA			
			± 20%	CGA3E2X5R1H473M080AA			
68 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X5R1H683K050BB	CGA2B3X5R1V683K050BB	CGA2B3X5R1E683K050BB	CGA2B2X5R1C683K050BA
			± 20%	CGA2B3X5R1H683M050BB	CGA2B3X5R1V683M050BB	CGA2B3X5R1E683M050BB	CGA2B2X5R1C683M050BA
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H683K080AA			
			± 20%	CGA3E2X5R1H683M080AA			
100 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X5R1H104K050BB	CGA2B3X5R1V104K050BB	CGA2B3X5R1E104K050BB	CGA2B2X5R1C104K050BA
			± 20%	CGA2B3X5R1H104M050BB	CGA2B3X5R1V104M050BB	CGA2B3X5R1E104M050BB	CGA2B2X5R1C104M050BA
	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1H104K080AA		CGA3E2X5R1E104K080AA	
			± 20%	CGA3E2X5R1H104M080AA		CGA3E2X5R1E104M080AA	
150 nF	1005	0.50 ± 0.05	± 10%				CGA2B1X5R1C154K050BC
			± 20%				CGA2B1X5R1C154M050BC
	1608	0.80 ± 0.10	± 10%	CGA3E3X5R1H154K080AB	CGA3E3X5R1V154K080AB	CGA3E2X5R1E154K080AA	
			± 20%	CGA3E3X5R1H154M080AB	CGA3E3X5R1V154M080AB	CGA3E2X5R1E154M080AA	
	2012	1.25 ± 0.20	± 10%	CGA4J2X5R1H154K125AA			
			± 20%	CGA4J2X5R1H154M125AA			
220 nF	1005	0.50 ± 0.05	± 10%				CGA2B1X5R1C224K050BC
			± 20%				CGA2B1X5R1C224M050BC
	1608	0.80 ± 0.10	± 10%	CGA3E3X5R1H224K080AB	CGA3E3X5R1V224K080AB	CGA3E2X5R1E224K080AA	CGA3E2X5R1C224K080AA
			± 20%	CGA3E3X5R1H224M080AB	CGA3E3X5R1V224M080AB	CGA3E2X5R1E224M080AA	CGA3E2X5R1C224M080AA
	2012	1.25 ± 0.20	± 10%	CGA4J2X5R1H224K125AA			
			± 20%	CGA4J2X5R1H224M125AA			
330 nF	1608	0.80 ± 0.10	± 10%	CGA3E3X5R1H334K080AB	CGA3E3X5R1V334K080AB	CGA3E3X5R1E334K080AB	CGA3E2X5R1C334K080AA
			± 20%	CGA3E3X5R1H334M080AB	CGA3E3X5R1V334M080AB	CGA3E3X5R1E334M080AB	CGA3E2X5R1C334M080AA
	2012	1.25 ± 0.20	± 10%	CGA4J2X5R1H334K125AA			
			± 20%	CGA4J2X5R1H334M125AA			
470 nF	1608	0.80 ± 0.10	± 10%	CGA3E3X5R1H474K080AB	CGA3E3X5R1V474K080AB	CGA3E3X5R1E474K080AB	CGA3E2X5R1C474K080AA
			± 20%	CGA3E3X5R1H474M080AB	CGA3E3X5R1V474M080AB	CGA3E3X5R1E474M080AB	CGA3E2X5R1C474M080AA
	2012	1.25 ± 0.20	± 10%	CGA4J3X5R1H474K125AB	CGA4J3X5R1V474K125AB	CGA4J2X5R1E474K125AA	
			± 20%	CGA4J3X5R1H474M125AB	CGA4J3X5R1V474M125AB	CGA4J2X5R1E474M125AA	
	3216	1.60 +0.30/-0.10	± 10%	CGA5L2X5R1H474K160AA			
			± 20%	CGA5L2X5R1H474M160AA			
680 nF	1608	0.80 ± 0.10	± 10%	CGA3E3X5R1V684K080AB	CGA3E3X5R1H684K080AB	CGA3E3X5R1E684K080AB	CGA3E2X5R1C684K080AA
			± 20%	CGA3E3X5R1H684M080AB	CGA3E3X5R1V684M080AB	CGA3E3X5R1E684M080AB	CGA3E2X5R1C684M080AA
	2012	1.25 ± 0.20	± 10%	CGA4J3X5R1H684K125AB	CGA4J3X5R1V684K125AB	CGA4J2X5R1E684K125AA	CGA4J2X5R1C684K125AA
			± 20%	CGA4J3X5R1H684M125AB	CGA4J3X5R1V684M125AB	CGA4J2X5R1E684M125AA	CGA4J2X5R1C684M125AA
	3216	1.60 +0.30/-0.10	± 10%	CGA5L2X5R1H684K160AA			
			± 20%	CGA5L2X5R1H684M160AA			
1 µF	1608	0.80 ± 0.10	± 10%	CGA3E3X5R1H105K080AB	CGA3E3X5R1V105K080AB	CGA3E3X5R1E105K080AB	CGA3E1X5R1C105K080AC
			± 20%	CGA3E3X5R1H105M080AB	CGA3E3X5R1V105M080AB	CGA3E3X5R1E105M080AB	CGA3E1X5R1C105M080AC
	2012	1.25 ± 0.20	± 10%	CGA4J3X5R1H105K125AB	CGA4J3X5R1V105K125AB	CGA4J2X5R1E105K125AA	CGA4J2X5R1C105K125AA
			± 20%	CGA4J3X5R1H105M125AB	CGA4J3X5R1V105M125AB	CGA4J2X5R1E105M125AA	CGA4J2X5R1C105M125AA
	3216	1.60 +0.30/-0.10	± 10%	CGA5L2X5R1H105K160AA			
			± 20%	CGA5L2X5R1H105M160AA			
1.5 µF	1608	0.80 ± 0.10	± 10%				CGA3E1X5R1C155K080AC
			± 20%				CGA3E1X5R1C155M080AC
	2012	1.25 ± 0.20	± 10%	CGA4J3X5R1H155K125AB	CGA4J3X5R1V155K125AB	CGA4J3X5R1E155K125AB	CGA4J2X5R1C155K125AA
			± 20%	CGA4J3X5R1H155M125AB	CGA4J3X5R1V155M125AB	CGA4J3X5R1E155M125AB	CGA4J2X5R1C155M125AA
	3216	1.60 +0.30/-0.10	± 10%	CGA5L3X5R1H155K160AB	CGA5L3X5R1V155K160AB	CGA5L2X5R1E155K160AA	
			± 20%	CGA5L3X5R1H155M160AB	CGA5L3X5R1V155M160AB	CGA5L2X5R1E155M160AA	
2.2 µF	1608	0.80 ± 0.10	± 10%				CGA3E1X5R1C225K080AC
			± 20%				CGA3E1X5R1C225M080AC
	2012	1.25 ± 0.20	± 10%	CGA4J3X5R1H225K125AB	CGA4J3X5R1V225K125AB	CGA4J3X5R1E225K125AB	CGA4J2X5R1C225K125AA
			± 20%	CGA4J3X5R1H225M125AB	CGA4J3X5R1V225M125AB	CGA4J3X5R1E225M125AB	CGA4J2X5R1C225M125AA

Capacitance Range Table

Class 2 (Temperature Stable)

Temperature Characteristics: X5R (-55 to +85ºC, ±15%)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number			
				Rated Voltage Edc: 50V	Rated Voltage Edc: 35V	Rated Voltage Edc: 25V	Rated Voltage Edc: 16V
2.2 µF	3216	1.60 +0.30/-0.10	± 10%	CGA5L3X5R1H225K160AB	CGA5L3X5R1V225K160AB	CGA5L2X5R1E225K160AA	
			± 20%	CGA5L3X5R1H225M160AB	CGA5L3X5R1V225M160AB	CGA5L2X5R1E225M160AA	
3.3 µF	2012	1.25 ± 0.20	± 10%	CGA4J3X5R1H335K125AB	CGA4J3X5R1V335K125AB	CGA4J3X5R1E335K125AB	CGA4J3X5R1C335K125AB
			± 20%	CGA4J3X5R1H335M125AB	CGA4J3X5R1V335M125AB	CGA4J3X5R1E335M125AB	CGA4J3X5R1C335M125AB
	3216	1.60 +0.30/-0.10	± 10%	CGA5L3X5R1H335K160AB	CGA5L3X5R1V335K160AB	CGA5L2X5R1E335K160AA	
			± 20%	CGA5L3X5R1H335M160AB	CGA5L3X5R1V335M160AB	CGA5L2X5R1E335M160AA	
4.7 µF	2012	1.25 ± 0.20	± 10%	CGA4J3X5R1H475K125AB	CGA4J3X5R1V475K125AB	CGA4J3X5R1E475K125AB	CGA4J3X5R1C475K125AB
			± 20%	CGA4J3X5R1H475M125AB	CGA4J3X5R1V475M125AB	CGA4J3X5R1E475M125AB	CGA4J3X5R1C475M125AB
	3216	1.60 +0.30/-0.10	± 10%	CGA5L3X5R1H475K160AB	CGA5L3X5R1V475K160AB	CGA5L2X5R1E475K160AA	CGA5L2X5R1C475K160AA
			± 20%	CGA5L3X5R1H475M160AB	CGA5L3X5R1V475M160AB	CGA5L2X5R1E475M160AA	CGA5L2X5R1C475M160AA
6.8 µF	2012	1.25 ± 0.20	± 10%				CGA4J1X5R1C685K125AC
			± 20%				CGA4J1X5R1C685M125AC
	3216	1.60 +0.30/-0.10	± 10%	CGA5L3X5R1H685K160AB	CGA5L3X5R1V685K160AB	CGA5L3X5R1E685K160AB	CGA5L2X5R1C685K160AA
			± 20%	CGA5L3X5R1H685M160AB	CGA5L3X5R1V685M160AB	CGA5L3X5R1E685M160AB	CGA5L2X5R1C685M160AA
10 µF	2012	1.25 ± 0.20	± 10%				CGA4J1X5R1C106K125AC
			± 20%				CGA4J1X5R1C106M125AC
	3216	1.60 +0.30/-0.10	± 10%	CGA5L3X5R1H106K160AB	CGA5L3X5R1V106K160AB	CGA5L3X5R1E106K160AB	CGA5L1X5R1C106K160AC
			± 20%	CGA5L3X5R1H106M160AB	CGA5L3X5R1V106M160AB	CGA5L3X5R1E106M160AB	CGA5L1X5R1C106M160AC
15 µF	3216	1.60 +0.30/-0.10	± 20%				CGA5L1X5R1C156M160AC
22 µF	3216	1.60 +0.30/-0.10	± 20%				CGA5L1X5R1C226M160AC

Class 2 (Temperature Stable)

Temperature Characteristics: X5R (-55 to +85ºC, ±15%)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number	
				Rated Voltage Edc: 10V	Rated Voltage Edc: 6.3V
100 nF	1005	0.50 ± 0.05	± 10%	CGA2B2X5R1A104K050BA	
			± 20%	CGA2B2X5R1A104M050BA	
150 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X5R1A154K050BB	
			± 20%	CGA2B3X5R1A154M050BB	
220 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X5R1A224K050BB	
			± 20%	CGA2B3X5R1A224M050BB	
330 nF	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1A334K080AA	
			± 20%	CGA3E2X5R1A334M080AA	
470 nF	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1A474K080AA	
			± 20%	CGA3E2X5R1A474M080AA	
680 nF	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1A684K080AA	
			± 20%	CGA3E2X5R1A684M080AA	
1 µF	1608	0.80 ± 0.10	± 10%	CGA3E2X5R1A105K080AA	
			± 20%	CGA3E2X5R1A105M080AA	
1.5 µF	1608	0.80 ± 0.10	± 10%	CGA3E3X5R1A155K080AB	
			± 20%	CGA3E3X5R1A155M080AB	
	2012	1.25 ± 0.20	± 10%	CGA4J2X5R1A155K125AA	
			± 20%	CGA4J2X5R1A155M125AA	
2.2 µF	1608	0.80 ± 0.10	± 10%	CGA3E3X5R1A225K080AB	
			± 20%	CGA3E3X5R1A225M080AB	
	2012	1.25 ± 0.20	± 10%	CGA4J2X5R1A225K125AA	
			± 20%	CGA4J2X5R1A225M125AA	
3.3 µF	1608	0.80 ± 0.10	± 10%	CGA3E1X5R1A335K080AC	CGA3E3X5R0J335K080AB
			± 20%	CGA3E1X5R1A335M080AC	CGA3E3X5R0J335M080AB
	2012	1.25 ± 0.20	± 10%	CGA4J2X5R1A335K125AA	
			± 20%	CGA4J2X5R1A335M125AA	
4.7 µF	1608	0.80 ± 0.10	± 10%		CGA3E1X5R0J475K080AC
			± 20%		CGA3E1X5R0J475M080AC
	2012	1.25 ± 0.20	± 10%	CGA4J2X5R1A475K125AA	
			± 20%	CGA4J2X5R1A475M125AA	
6.8 µF	2012	1.25 ± 0.20	± 10%	CGA4J3X5R1A685K125AB	
			± 20%	CGA4J3X5R1A685M125AB	
10 µF	2012	1.25 ± 0.20	± 10%	CGA4J3X5R1A106K125AB	
			± 20%	CGA4J3X5R1A106M125AB	

Capacitance Range Table

Class 2 (Temperature Stable)

Temperature Characteristics: X7R (-55 to +125ºC, ±15%)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number			
				Rated Voltage Edc: 50V	Rated Voltage Edc: 35V	Rated Voltage Edc: 25V	Rated Voltage Edc: 16V
100 pF	0603	0.30 ± 0.03	± 10%	CGA1A2X7R1H101K030BA		CGA1A2X7R1E101K030BA	CGA1A2X7R1C101K030BA
			± 20%	CGA1A2X7R1H101M030BA		CGA1A2X7R1E101M030BA	CGA1A2X7R1C101M030BA
150 pF	0603	0.30 ± 0.03	± 10%	CGA1A2X7R1H151K030BA		CGA1A2X7R1E151K030BA	CGA1A2X7R1C151K030BA
			± 20%	CGA1A2X7R1H151M030BA		CGA1A2X7R1E151M030BA	CGA1A2X7R1C151M030BA
220 pF	0603	0.30 ± 0.03	± 10%	CGA1A2X7R1H221K030BA		CGA1A2X7R1E221K030BA	CGA1A2X7R1C221K030BA
			± 20%	CGA1A2X7R1H221M030BA		CGA1A2X7R1E221M030BA	CGA1A2X7R1C221M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H221K050BA			
			± 20%	CGA2B2X7R1H221M050BA			
330 pF	0603	0.30 ± 0.03	± 10%	CGA1A2X7R1H331K030BA		CGA1A2X7R1E331K030BA	CGA1A2X7R1C331K030BA
			± 20%	CGA1A2X7R1H331M030BA		CGA1A2X7R1E331M030BA	CGA1A2X7R1C331M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H331K050BA			
			± 20%	CGA2B2X7R1H331M050BA			
470 pF	0603	0.30 ± 0.03	± 10%	CGA1A2X7R1H471K030BA		CGA1A2X7R1E471K030BA	CGA1A2X7R1C471K030BA
			± 20%	CGA1A2X7R1H471M030BA		CGA1A2X7R1E471M030BA	CGA1A2X7R1C471M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H471K050BA			
			± 20%	CGA2B2X7R1H471M050BA			
680 pF	0603	0.30 ± 0.03	± 10%			CGA1A2X7R1E681K030BA	CGA1A2X7R1C681K030BA
			± 20%			CGA1A2X7R1E681M030BA	CGA1A2X7R1C681M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H681K050BA			
			± 20%	CGA2B2X7R1H681M050BA			
1 nF	0603	0.30 ± 0.03	± 10%			CGA1A2X7R1E102K030BA	CGA1A2X7R1C102K030BA
			± 20%			CGA1A2X7R1E102M030BA	CGA1A2X7R1C102M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H102K050BA			
			± 20%	CGA2B2X7R1H102M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H102K080AA			
			± 20%	CGA3E2X7R1H102M080AA			
1.5 nF	0603	0.30 ± 0.03	± 10%			CGA1A2X7R1E152K030BA	CGA1A2X7R1C152K030BA
			± 20%			CGA1A2X7R1E152M030BA	CGA1A2X7R1C152M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H152K050BA			
			± 20%	CGA2B2X7R1H152M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H152K080AA			
			± 20%	CGA3E2X7R1H152M080AA			
2.2 nF	0603	0.30 ± 0.03	± 10%			CGA1A2X7R1E222K030BA	CGA1A2X7R1C222K030BA
			± 20%			CGA1A2X7R1E222M030BA	CGA1A2X7R1C222M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H222K050BA			
			± 20%	CGA2B2X7R1H222M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H222K080AA			
			± 20%	CGA3E2X7R1H222M080AA			
3.3 nF	0603	0.30 ± 0.03	± 10%			CGA1A2X7R1E332K030BA	CGA1A2X7R1C332K030BA
			± 20%			CGA1A2X7R1E332M030BA	CGA1A2X7R1C332M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H332K050BA			
			± 20%	CGA2B2X7R1H332M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H332K080AA			
			± 20%	CGA3E2X7R1H332M080AA			
4.7 nF	0603	0.30 ± 0.03	± 10%				CGA1A2X7R1C472K030BA
			± 20%				CGA1A2X7R1C472M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H472K050BA			
			± 20%	CGA2B2X7R1H472M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H472K080AA			
			± 20%	CGA3E2X7R1H472M080AA			
6.8 nF	0603	0.30 ± 0.03	± 10%				CGA1A2X7R1C682K030BA
			± 20%				CGA1A2X7R1C682M030BA
	1005	0.50 ± 0.05	± 10%	CGA2B2X7R1H682K050BA			
			± 20%	CGA2B2X7R1H682M050BA			
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H682K080AA			
			± 20%	CGA3E2X7R1H682M080AA			
10 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X7R1H103K050BB	CGA2B3X7R1V103K050BB	CGA2B2X7R1E103K050BA	
			± 20%	CGA2B3X7R1H103M050BB	CGA2B3X7R1V103M050BB	CGA2B2X7R1E103M050BA	
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H103K080AA			
			± 20%	CGA3E2X7R1H103M080AA			

Capacitance Range Table

Class 2 (Temperature Stable)

Temperature Characteristics: X7R (-55 to +125ºC, ±15%)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number			
				Rated Voltage Edc: 50V	Rated Voltage Edc: 35V	Rated Voltage Edc: 25V	Rated Voltage Edc: 16V
15 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X7R1H153K050BB	CGA2B3X7R1V153K050BB	CGA2B2X7R1E153K050BA	
			± 20%	CGA2B3X7R1H153M050BB	CGA2B3X7R1V153M050BB	CGA2B2X7R1E153M050BA	
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H153K080AA			
			± 20%	CGA3E2X7R1H153M080AA			
22 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X7R1H223K050BB	CGA2B3X7R1V223K050BB	CGA2B2X7R1E223K050BA	
			± 20%	CGA2B3X7R1H223M050BB	CGA2B3X7R1V223M050BB	CGA2B2X7R1E223M050BA	
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H223K080AA			
			± 20%	CGA3E2X7R1H223M080AA			
33 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X7R1H333K050BB	CGA2B3X7R1V333K050BB	CGA2B1X7R1E333K050BC	CGA2B2X7R1C333K050BA
			± 20%	CGA2B3X7R1H333M050BB	CGA2B3X7R1V333M050BB	CGA2B1X7R1E333M050BC	CGA2B2X7R1C333M050BA
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H333K080AA			
			± 20%	CGA3E2X7R1H333M080AA			
47 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X7R1H473K050BB	CGA2B3X7R1V473K050BB	CGA2B1X7R1E473K050BC	CGA2B2X7R1C473K050BA
			± 20%	CGA2B3X7R1H473M050BB	CGA2B3X7R1V473M050BB	CGA2B1X7R1E473M050BC	CGA2B2X7R1C473M050BA
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H473K080AA			
			± 20%	CGA3E2X7R1H473M080AA			
68 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X7R1H683K050BB	CGA2B3X7R1V683K050BB	CGA2B3X7R1E683K050BB	CGA2B1X7R1C683K050BC
			± 20%	CGA2B3X7R1H683M050BB	CGA2B3X7R1V683M050BB	CGA2B3X7R1E683M050BB	CGA2B1X7R1C683M050BC
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H683K080AA			
			± 20%	CGA3E2X7R1H683M080AA			
100 nF	1005	0.50 ± 0.05	± 10%	CGA2B3X7R1H104K050BB	CGA2B3X7R1V104K050BB	CGA2B3X7R1E104K050BB	CGA2B1X7R1C104K050BC
			± 20%	CGA2B3X7R1H104M050BB	CGA2B3X7R1V104M050BB	CGA2B3X7R1E104M050BB	CGA2B1X7R1C104M050BC
	1608	0.80 ± 0.10	± 10%	CGA3E2X7R1H104K080AA		CGA3E2X7R1E104K080AA	
			± 20%	CGA3E2X7R1H104M080AA		CGA3E2X7R1E104M080AA	
	2012	1.25 ± 0.20	± 10%	CGA4J2X7R1H104K125AA			
150 nF	1608	0.80 ± 0.10	± 10%	CGA3E3X7R1H154K080AB	CGA3E3X7R1V154K080AB	CGA3E2X7R1E154K080AA	
			± 20%	CGA3E3X7R1H154M080AB	CGA3E3X7R1V154M080AB	CGA3E2X7R1E154M080AA	
	2012	1.25 ± 0.20	± 10%	CGA4J2X7R1H154K125AA			
			± 20%	CGA4J2X7R1H154M125AA			
220 nF	1608	0.80 ± 0.10	± 10%	CGA3E3X7R1H224K080AB	CGA3E3X7R1V224K080AB	CGA3E1X7R1E224K080AC	CGA3E2X7R1C224K080AA
			± 20%	CGA3E3X7R1H224M080AB	CGA3E3X7R1V224M080AB	CGA3E1X7R1E224M080AC	CGA3E2X7R1C224M080AA
	2012	1.25 ± 0.20	± 10%	CGA4J2X7R1H224K125AA		CGA4J2X7R1E224K125AA	
			± 20%	CGA4J2X7R1H224M125AA			
330 nF	1608	0.80 ± 0.10	± 10%		CGA3E1X7R1V334K080AC	CGA3E3X7R1E334K080AB	CGA3E1X7R1C334K080AC
			± 20%		CGA3E1X7R1V334M080AC	CGA3E3X7R1E334M080AB	CGA3E1X7R1C334M080AC
	2012	1.25 ± 0.20	± 10%	CGA4J2X7R1H334K125AA			
			± 20%	CGA4J2X7R1H334M125AA			
470 nF	1608	0.80 ± 0.10	± 10%		CGA3E1X7R1V474K080AC	CGA3E3X7R1E474K080AB	CGA3E1X7R1C474K080AC
			± 20%		CGA3E1X7R1V474M080AC	CGA3E3X7R1E474M080AB	CGA3E1X7R1C474M080AC
	2012	1.25 ± 0.20	± 10%	CGA4J3X7R1H474K125AB	CGA4J3X7R1V474K125AB	CGA4J2X7R1E474K125AA	CGA4J2X7R1C474K125AA
			± 20%	CGA4J3X7R1H474M125AB	CGA4J3X7R1V474M125AB	CGA4J2X7R1E474M125AA	
	3216	1.60 +0.30/-0.10	± 10%	CGA5L2X7R1H474K160AA			
			± 20%	CGA5L2X7R1H474M160AA			
680 nF	1608	0.80 ± 0.10	± 10%			CGA3E1X7R1E684K080AC	CGA3E1X7R1C684K080AC
			± 20%			CGA3E1X7R1E684M080AC	CGA3E1X7R1C684M080AC
	2012	1.25 ± 0.20	± 10%	CGA4J3X7R1H684K125AB	CGA4J3X7R1V684K125AB	CGA4J3X7R1E684K125AB	CGA4J2X7R1C684K125AA
			± 20%	CGA4J3X7R1H684M125AB	CGA4J3X7R1V684M125AB	CGA4J3X7R1E684M125AB	CGA4J2X7R1C684M125AA
	3216	1.60 +0.30/-0.10	± 10%	CGA5L2X7R1H684K160AA			
			± 20%	CGA5L2X7R1H684M160AA			
1 µF	1608	0.80 ± 0.10	± 10%			CGA3E1X7R1E105K080AC	CGA3E1X7R1C105K080AC
			± 20%			CGA3E1X7R1E105M080AC	CGA3E1X7R1C105M080AC
	2012	1.25 ± 0.20	± 10%	CGA4J3X7R1H105K125AB	CGA4J3X7R1V105K125AB	CGA4J3X7R1E105K125AB	CGA4J2X7R1C105K125AA
			± 20%	CGA4J3X7R1H105M125AB	CGA4J3X7R1V105M125AB	CGA4J3X7R1E105M125AB	CGA4J2X7R1C105M125AA
	3216	1.60 +0.30/-0.10	± 10%	CGA5L3X7R1H105K160AB		CGA5L2X7R1E105K160AA	
			± 20%	CGA5L3X7R1H105M160AB		CGA5L2X7R1E105M160AA	
	3225	1.60 ± 0.20	± 10%	CGA6L2X7R1H105K160AA			
			± 20%	CGA6L2X7R1H105M160AA			

Capacitance Range Table

Class 2 (Temperature Stable)

Temperature Characteristics: X7R (-55 to +125ºC, ±15%)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number			
				Rated Voltage Edc: 50V	Rated Voltage Edc: 35V	Rated Voltage Edc: 25V	Rated Voltage Edc: 16V
1.5 µF	2012	1.25 ± 0.20	± 10%		CGA4J1X7R1V155K125AC	CGA4J3X7R1E155K125AB	CGA4J3X7R1C155K125AB
			± 20%		CGA4J1X7R1V155M125AC	CGA4J3X7R1E155M125AB	CGA4J3X7R1C155M125AB
	3216	1.60 +0.30/-0.10	± 10%	CGA5L3X7R1H155K160AB	CGA5L3X7R1V155K160AB	CGA5L2X7R1E155K160AA	
			± 20%	CGA5L3X7R1H155M160AB	CGA5L3X7R1V155M160AB	CGA5L2X7R1E155M160AA	
	3225	2.00 ± 0.20	± 10%	CGA6M2X7R1H155K200AA			
				CGA6M3X7R1H155K200AB			
			± 20%	CGA6M2X7R1H155M200AA			
				CGA6M3X7R1H155M200AB			
	4532	1.60 ± 0.20	± 10%	CGA8L2X7R1H155K160KA			
2.2 µF	2012	1.25 ± 0.20	± 10%		CGA4J1X7R1V225K125AC	CGA4J3X7R1E225K125AB	CGA4J3X7R1C225K125AB
			± 20%		CGA4J1X7R1V225M125AC	CGA4J3X7R1E225M125AB	CGA4J3X7R1C225M125AB
	3216	1.60 +0.30/-0.10	± 10%	CGA5L3X7R1H225K160AB	CGA5L3X7R1V225K160AB	CGA5L2X7R1E225K160AA	
			± 20%	CGA5L3X7R1H225M160AB	CGA5L3X7R1V225M160AB	CGA5L2X7R1E225M160AA	
	3225	2.00 ± 0.20	± 10%	CGA6M3X7R1H225K200AB			
			± 20%	CGA6M3X7R1H225M200AB			
	4532	1.60 ± 0.20	± 10%	CGA8L2X7R1H225K160KA			
3.3 µF	2012	1.25 ± 0.20	± 10%			CGA4J1X7R1E335K125AC	
							CGA4J3X7R1C335K125AB
			± 20%			CGA4J1X7R1E335M125AC	CGA4J3X7R1C335M125AB
	3216	1.60 +0.30/-0.10	± 10%		CGA5L1X7R1V335K160AC	CGA5L1X7R1E335K160AC	
			± 20%		CGA5L1X7R1V335M160AC	CGA5L1X7R1E335M160AC	
	3225	2.50 ± 0.30	± 10%	CGA6P3X7R1H335K250AB			
			± 20%	CGA6P3X7R1H335M250AB			
	4532	2.00 ± 0.20	± 10%	CGA8M2X7R1H335K200KA			
4.7 µF	2012	1.25 ± 0.20	± 10%			CGA4J1X7R1E475K125AC	
							CGA4J3X7R1C475K125AB
			± 20%			CGA4J1X7R1E475M125AC	CGA4J3X7R1C475M125AB
	3216	1.60 +0.30/-0.10	± 10%		CGA5L1X7R1V475K160AC	CGA5L1X7R1E475K160AC	CGA5L3X7R1C475K160AB
			± 20%		CGA5L1X7R1V475M160AC	CGA5L1X7R1E475M160AC	CGA5L3X7R1C475M160AB
	3225	2.50 ± 0.30	± 10%	CGA6P3X7R1H475K250AB			
			± 20%	CGA6P3X7R1H475M250AB			
	4532	1.60 ± 0.20	± 10%			CGA8L2X7R1E475K160KA	
			± 20%			CGA8L2X7R1E475M160KA	
		2.00 ± 0.20	± 10%	CGA8M3X7R1H475K200KB			
	5750	2.00 ± 0.20	± 10%	CGA9M2X7R1H475K200KA			
6.8 µF	3216	1.60 +0.30/-0.10	± 10%			CGA5L1X7R1E685K160AC	CGA5L1X7R1C685K160AC
			± 20%			CGA5L1X7R1E685M160AC	CGA5L1X7R1C685M160AC
	3225	2.50 ± 0.30	± 10%			CGA6P3X7R1E685K250AB	
			± 20%			CGA6P3X7R1E685M250AB	
	4532	2.50 ± 0.20	± 10%	CGA8P3X7R1H685K250KB			
	5750	2.50 ± 0.30	± 10%	CGA9P2X7R1H685K250KA			
10 µF	3216	1.60 +0.30/-0.10	± 10%			CGA5L1X7R1E106K160AC	CGA5L1X7R1C106K160AC
			± 20%			CGA5L1X7R1E106M160AC	CGA5L1X7R1C106M160AC
	3225	2.00 ± 0.20	± 10%				CGA6M3X7R1C106K200AB
			± 20%				CGA6M3X7R1C106M200AB
		2.50 ± 0.30	± 10%			CGA6P1X7R1E106K250AC	
			± 20%			CGA6P1X7R1E106M250AC	
	4532	2.50 ± 0.20	± 10%			CGA8P2X7R1E106K250KA	
	5750	2.00 ± 0.20	± 20%			CGA9M2X7R1E106M200KA	
		2.30 ± 0.20	± 10%	CGA9N3X7R1H106K230KB			
15 µF	3225	2.50 ± 0.30	± 20%				CGA6P3X7R1C156M250AB
	4532	2.80 ± 0.30	± 20%			CGA8Q3X7R1E156M280KB	
	5750	2.30 ± 0.20	± 20%			CGA9N2X7R1E156M230KA	
22 µF	3225	2.50 ± 0.30	± 20%				CGA6P1X7R1C226M250AC
	4532	2.30 ± 0.20	± 20%				CGA8N3X7R1C226M230KB
		2.50 ± 0.20	± 20%			CGA8P1X7R1E226M250KC	
	5750	2.50 ± 0.30	± 20%			CGA9P2X7R1E226M250KA	
33 µF	4532	2.50 ± 0.20	± 20%				CGA8P1X7R1C336M250KC
47 µF	5750	2.30 ± 0.20	± 20%				CGA9N3X7R1C476M230KB

Capacitance Range Table

Class 2 (Temperature Stable)

Temperature Characteristics: X7R (-55 to +125ºC, ±15%)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number	
				Rated Voltage Edc: 10V	Rated Voltage Edc: 6.3V
10 nF	0603	0.30 ± 0.03	± 10%	CGA1A2X7R1A103K030BA	CGA1A2X7R0J103K030BA
			± 20%	CGA1A2X7R1A103M030BA	CGA1A2X7R0J103M030BA
150 nF	1005	0.50 ± 0.05	± 10%	CGA2B1X7R1A154K050BC	CGA2B3X7R0J154K050BB
			± 20%	CGA2B1X7R1A154M050BC	CGA2B3X7R0J154M050BB
220 nF	1005	0.50 ± 0.05	± 10%	CGA2B1X7R1A224K050BC	CGA2B3X7R0J224K050BB
			± 20%	CGA2B1X7R1A224M050BC	CGA2B3X7R0J224M050BB
1.5 µF	1608	0.80 ± 0.10	± 10%		CGA3E1X7R0J155K080AC
			± 20%		CGA3E1X7R0J155M080AC
2.2 µF	1608	0.80 ± 0.10	± 10%		CGA3E1X7R0J225K080AC
			± 20%		CGA3E1X7R0J225M080AC
3.3 µF	2012	1.25 ± 0.20	± 10%	CGA4J3X7R1A335K125AB	
4.7 µF	2012	1.25 ± 0.20	± 10%	CGA4J3X7R1A475K125AB	
6.8 µF	2012	1.25 ± 0.20	± 10%		CGA4J1X7R0J685K125AC
			± 20%		CGA4J1X7R0J685M125AC
10 µF	2012	1.25 ± 0.20	± 10%		CGA4J1X7R0J106K125AC
			± 20%		CGA4J1X7R0J106M125AC
22 µF	3216	1.60 +0.30/-0.10	± 20%		CGA5L1X7R0J226M160AC

Class 2 (Temperature Stable)

Temperature Characteristics: X7S (-55 to +125ºC, ±22%)

Capacitance	Size	Thickness (mm)	Capacitance Tolerance	TDK Part Number	
				Rated Voltage Edc: 50V	Rated Voltage Edc: 6.3V
4.7 µF	3225	2.30 ± 0.20	± 10%	CGA6N3X7S1H475K230AB	
6.8 µF	3225	2.50 ± 0.30	± 10%	CGA6P3X7S1H685K250AB	
			± 20%	CGA6P3X7S1H685M250AB	
10 µF	3225	2.50 ± 0.30	± 10%	CGA6P3X7S1H106K250AB	
			± 20%	CGA6P3X7S1H106M250AB	
33 µF	3225	2.50 ± 0.30	± 20%		CGA6P1X7S0J336M250AC
47 µF	3225	2.50 ± 0.30	± 20%		CGA6P1X7S0J476M250AC