

Energy storage systems to provide ancillary services to the power system

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Energy Storage systems integrated with grid-forming converters to provide inertia support to the power system

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Abstract

The power system has experienced a significant transformation in the last years, notably due to the large increase of power electronic-based technologies. These new technologies are mostly based on converter-interfaced generation (CIG), which have different dynamic response characteristics than classical synchronous generators. Power systems with high penetration of CIG are characterized by low grid inertia due to the lack of frequency containment provided by synchronous generators. This thesis discusses integrating energy storage systems into the power system to overcome the challenges caused by the increasing penetration of CIGs. Different types of energy storage technologies are studied, and recommendations on the size of energy storage systems are proposed based on the functionalities to be implemented. Moreover, modelling and control methods for Battery and Supercapacitor Energy Storage Systems integrated with grid-connected converters are presented. These grid-connected converters use grid-forming control strategies to provide functionalities of the synchronous generators, such as inertial response. Different grid-forming control strategies are presented and compared. Finally, a dc-link voltage based synchronization control is proposed. The dc-link voltage control utilized the dc-link dynamics to synchronize the grid-forming converter with the grid. Time domain simulations in Simulink and PSCAD are performed to analyze the different controllers and the system's dynamic behaviour.

Keywords: Energy Storage Systems, Battery Energy Storage Systems, Supercapacitor Energy Storage Systems, grid-forming power converters, inertia support, frequency support

Contents

Li	st of	Figure	es	ix
Li	st of	Table	5	xi
1	Intr	oducti	ion	1
2	Ene	ergy St	orage Systems	3
	2.1	Energ	y Storage Systems for power system applications	3
	2.2	Role c	of energy storage systems	7
	2.3	Model	ling and control of BESS	8
		2.3.1	BESS sizing	8
		2.3.2	Equivalent electrical model: Model 1	9
		2.3.3	Equivalent electrical model: Thévenin equivalent	10
	2.4	Model	ling and control of Supercapacitor Energy Storage System	11
		2.4.1	SCESS sizing to provide inertia support	11
		2.4.2	SCESS sizing to provide frequency support	15
		2.4.3	Supercapacitor banks	15
		2.4.4	Equivalent electrical model of a SCESS	16
3	Grie	d-form	ing power converters	19
	3.1	Grid-f	orming converter control strategies	19
		3.1.1	Power Synchronization Control	19
		3.1.2	Virtual Synchronous Machine	22
		3.1.3	PI based active power controller	24
Δ	DC.	-link c	ontrol strategies	29
•	4.1	Metho	d 1. Cascaded dc-link voltage controller	30
	42	Metho	a 2: dc-voltage based synchronization control	32
	1.2	421	Proportional-based DVSC	33
		422	PI-based DVSC	34
		423	PID-based DVSC	35
	43	Tests		35
	1.0	431	System of study	36
		432	Test cases and evaluation criteria	36
		433	Method 1	38
		4.3.4	Method 2	44
		1.0.1		**

5	Conclusions	49
Bil	oliography	51

List of Figures

2.1	Comparison of specific power and specific energy	5
2.3	Typical OCV versus SOC curve for a Li-ion battery	10
2.2	Model 1: OCV function of SOC and ESR	10
2.4	Model 2: Thévenin equivalent	11
2.5	Dynamic equivalent circuit of the dc-link	14
2.6	SCESS equivalent circuit model	17
3.1	Simplified vsc converter - ac system connection	20
3.2	Block diagram of the PSC	20
3.3	Implemented control structure of PSC	21
3.4	Active power response of PSC under unit step reference change (red	00
95	SCR = 10, green $SCR = 5$, blue $SCR = 2$)	22
3.5	Block diagram of the VSM	23
3.6	Active power response of VSM under unit step reference change (red $SCR = 10$ green $SCR = 5$ blue $SCR = 2$)	24
3.7	Block diagram of the PI-based active power controller	24
3.8	Block diagram of the PI-based active power controller with active	- 1
0.0	damping	25
3.9	Active power response of PI-based active power controller under unit	_0
	step reference change (red SCR = 10, green SCR = 5, blue SCR = 2).	26
3.10	Active power response of PI-based active power controller under unit	
	step reference change (red SCR = 10, green SCR = 5, blue SCR = 2).	27
4.1	dc-link voltage controller	30
4.2	Energy controller	31
4.3	Inertia emulation loop	31
4.4	Block diagram of general DVSC	33
4.5	Block diagram of proportional-based DVSC	33
4.6	Block diagram of PI-based DVSC	34
4.7	Block diagram of PID-based DVSC	35
4.8	Diagram of the simplified WPP system with GFM-SCESS	36
4.9	GFM-SCESS control structure	39
4.10	Response of the GFM-SCESS during the frequency event. Grid	
	frequency (dashed black), converter internal frequency (green), con-	
	verter power (blue) and converter output current (red)	41

4.11	Response of the GFM-SCESS during the frequency event. Dc-link	
	reference voltage (dashed black), dc-link voltage (green) and dc	
	$\operatorname{current} (\operatorname{blue}) \ldots \ldots$	42
4.12	Response of the GFM-SCESS during the frequency event. Com-	
	parison of the inertial power response with different dc-link voltage	
	controller bandwidth. $\alpha_{dc} = \alpha_{pc}$ (blue), $\alpha_{dc} = \alpha_{pc}/2$ (green),	
	$\alpha_{dc} = \alpha_{pc} / 5 $ (red)	43
4.13	Response of the GFM-SCESS during the frequency event. Com-	
	parison of the dc voltage response with dc-link voltage controller	
	bandwidth. $\alpha_{dc} = \alpha_{pc}$ (blue), $\alpha_{dc} = \alpha_{pc}/2$ (green), $\alpha_{dc} = \alpha_{pc}/5$	
	(red), dc voltage reference (dashed black).	43
4.14	Response of the GFM-SCESS after a 0.01 pu dc voltage step.	
	Comparison of the dc voltage step response with different dc-link	
	voltage controller bandwidth. $\alpha_{dc} = \alpha_{pc}$ (blue), $\alpha_{dc} = \alpha_{pc}/2$ (green),	
	$\alpha_{dc} = \alpha_{pc}/5$ (red), dc voltage reference (dashed black)	44
4.15	Response of the GFM-SCESS after a 0.01 pu dc voltage step.	
	Comparison of the active power response with different dc-link voltage	
	controller bandwidth. $\alpha_{dc} = \alpha_{pc}$ (blue), $\alpha_{dc} = \alpha_{pc}/2$ (green),	
	$\alpha_{dc} = \alpha_{pc}/5 $ (red)	44
4.16	GFM-SCESS control structure	45
4.17	Response of the GFM-SCESS after a 0.01 pu dc voltage step.	
	Comparison of the dc voltage step response with different dc-link	
	voltage controller bandwidth. Proportional controller (blue), PI	
	controller (red), PID controller (green), dc-link voltage reference	
	(dashed black).	46
4.18	Response of the GFM-SCESS during the frequency event. Propor-	
	tional controller (blue), PI controller (red), PID controller (green),	
	dc-link voltage reference (dashed black).	47
4.19	Response of the GFM-SCESS during the frequency event. Propor-	
	tional controller (blue), PI controller (red), PID controller (green),	
	dc-link voltage reference (dashed black).	48

List of Tables

2.1	Storage characteristics	3
3.1	Test system data	2
4.1	Parameters of the GFM-SCESS	7
4.2	Parameters of the emulated WPP	7
4.3	Grid parameters	7
4.4	Parameters of the GFM-SCESS controller	3

1

Introduction

The dynamic behaviour of power systems was determined by the dynamic performance of large synchronous generators and their controls. However, the power system has experienced a significant transformation in the last years, notably due to the large increase of power electronic-based technologies. These new technologies include wind and photovoltaic generation, high voltage direct current (HVDC) links, flexible ac transmission systems (FACTS) or storage systems. These converter-interfaced generation technologies (CIGs) have different dynamic response characteristics than classical synchronous generators. Thus, the dynamic response of the power system has become more dependent on fast-response power electronic devices, altering the power system dynamic behaviour [1].

Power systems with high penetration of CIG are characterized by low grid inertia due to the lack of frequency containment provided by synchronous generators. [2]. The rotating mass of the synchronous generators provides inherent inertia to the system, unlike CIG technologies [3]. The consequence is a reduction in the total system inertia that significantly affects the capability to provide instantly matching balancing power, increasing the rate of change of frequency of the system [4]. Thus, the secure and reliable operation of the power system can be compromised. In this context, Energy Storage Systems (ESS) are considered a useful technology to enhance the controllability and flexibility of the future power system. ESS are a potential solution to reduce fluctuations and improve the power quality of the entire grid. Among other existing technologies, Battery Energy Storage Systems (BESS) and Supercapacitor Energy Storage Systems (SCESS) arise as some of the most suitable types of ESS to provide ancillary services to the future power system.

1. Introduction

Energy Storage Systems

2.1 Energy Storage Systems for power system applications

Energy Storage Systems are used in modern grids to enhance the reliability and resilience of the power system. The suitability of an energy storage resource is determined by its specific power and specific energy [5]. Specific power refers to the energy storage technology's output power per unit of mass (power density in per unit of volume). Specific energy refers to the amount of energy stored in a given system per unit of mass (power density in per unit of volume). The specific energy determines how long the energy storage device can be utilised, and the specific power signifies how rapidly a device can deliver energy. Fig. 2.1 shows a Ragone plot describing the relation between specific energy and power for the main energy storage technologies used in power systems [6]. In Table 2.1, different technologies and ESS are compared based on parameters such as cycle efficiency, cycle lifetime, self-discharge ratio, specific energy, specific power, response time and discharge time (based on data from [6–8]). The values presented are estimated and can differ from case to case. Cycle efficiency is the system's electricity output ratio to the energy input. Self-discharge accounts for energy leakage, which is essential in deciding the suitable storage duration. Cycle lifetime refers to how many complete charges and discharges the ESS can withstand. The response time can be defined as the time the ESS takes to achieve the desired output power. Discharge time denotes the duration the ESS can provide the output power rating until depletion. Several methods exist for categorising EES technologies [9]. One of the most widely used methods is based on the form of energy stored and can be classified into:

Electrochemical storage The chemical energy contained in the active material of the storage device is transformed directly into electrical energy [10]. Batteries such as Li-ion, VRB (Vanadium redox battery) or NaS (Sodium-sulfur) are suitable for power quality and providing frequency control to the system due to their fast response time and relatively high specific energy and specific power. Li-ion batteries have a low self-discharge (around 0.1 - 0.3 % per day), a high cycle efficiency (90 - 97 %) and a fast response time. However, NaS and VRB technologies have lower specific power and cycle efficiencies. For grid integration of BESS, the li-ion seems to represent the leading technology due to both high specific energy and specific power [10].

Mechanical storage Pumped hydro storage (PHS) and Compressed Air Energy Storage (CAES) are used for electric grid support for load-levelling applications. A PHS consists of two reservoirs located at different elevations. Water is pumped to the higher reservoir during off-peak hours and discharged to the lower reservoir during peak hours. The energy is stored in the form of potential energy. CAES is based on the same principle but storing instead compressed air at high pressure [6]. Both technologies have low energy density but high-rated energy capacity. In such systems, energy is stored during periods of low demand and then converted back to electricity when the electricity demand is high. PHS and CAES have lower power and energy densities. Thus they require large reservoirs for grid-scale applications. However, PHS have a relatively high cycle efficiency (75 - 85%) and almost negligible self-discharge. The large capacity of both technologies allows them to provide power for a few hours or even days. Another type of mechanical energy storage technology flywheels (FES). A FES consists of a rotating mass connected to an electrical machine and a bearing system for stabilization [11]. Flywheels have moderate specific power and energy and are suitable for applications demanding high peak power for short durations. However, flywheels can provide the rated power only for a few seconds or minutes. Flywheels will discharge 100% of the stored energy if the storage period is longer than about one day [9].

Electrical storage Capacitors, supercapacitors (based on Electrochemical Double Layer Capacitors) and Superconducting Magnetic Storage (SMES). These technologies are suitable for systems demanding high peak power for short durations and are also used for power quality applications. Capacitors and supercapacitors store charge electrostatically (non-Faradaic) [12]. Ordinary capacitors have a very small amount of charge storage. In a common capacitor, the two conducting plates are separated by a dielectric, while in a supercapacitor are separated by an electrolytic solution. Capacitors and supercapacitors can be charged substantially faster than batteries and cycled thousands of times. The main issue with conventional capacitors is their low specific energy. Thus, even if they have very high specific power, they can only provide it for a short time. If a large capacity is required, the area of the dielectric must be very large. Therefore, supercapacitors can lead to much higher capacitance and energy density than typical capacitors. On the other hand, SMES consists of a superconducting coil capable of storing electrical energy in the magnetic field generated by the dc current flowing through it [13,14]. Capacitors, supercapacitors and SMES have very high daily self-discharge ratios, from 10 to 100%. Therefore, they can only be used for short-term storage durations. These technologies have high specific power but limited specific energy. Supercapacitors have an extremely high cycling time (more than 100000) and high efficiency (around 90 - 97 %). However, their self-discharge is considerable (between 5 - 40 % per day). Thus, supercapacitors are suitable for short-term applications. SMES include relatively high power density, a fast response time (miliseconds) and high cycle efficiency. However, their self-discharge is high, and they have a very high initial capital cost.

Chemical storage Hydrogen fuel cell systems combined with hydrogen production and storage can provide stationary or distributed power. A hydrogen fuel cell is an electrochemical device that uses hydrogen and oxygen to produce electricity and water [15]. Fuel cells have a high specific energy and a moderate specific power. Moreover, their discharge time at rated power can vary from a few seconds to days. They have a short response time (seconds), and their daily self-discharge is almost negligible. However, hydrogen fuel cells have a low cycle efficiency (between 20 and 66 %). A hydrogen fuel cell is a promising technology for grid-scale energy storage systems but is still in the development stage.

Thermal storage TES encompasses a variety of technologies that store materials at high/cold temperatures in insulated containments and are suitable for large-scale energy management [16]. These materials are then heat/cold recovered and are used to generate electricity using heat engine cycles. TES are classified into high-temperature energy storage (sensible heat systems such as steam or hot water accumulators) and low-temperature storage (such as cryogenic energy storage). TES have high specific energy with low specific power. However, the overall efficiency of TES is low (around 30 - 60 %).



Figure 2.1: Comparison of specific power and specific energy

Storage Type	Cycle efficiency (%)	Cycle lifetime (%/day)	Self-discharge (%/day)	Specific energy (Wh/kg)	Specific power (W/kg)	Response time	Discharge time
ctrochemical Lithium-ion VRB NaS	90-97 75-85 75-90	$1000-20000 \\ 12000+ \\ 2500-4000$	0.1-0.3 very low negligible	75-200 10-30 150-240	$150-2000 \\ 166 \\ 150-240$	seconds seconds seconds	seconds-hours seconds-hours seconds-hours
Mechanical Flywheels PHS CAES	90-95 75-85 60-70	20000+ 10000-30000 8000-12000	100 negligible negligible	5-100 0.5-1.5 30-60	400-1500 N/A N/A	miliseconds minutes minutes	seconds-minutes 1 h-days 1 h-days
Electrical Capacitors upercapacitors SMES	65-75 85-97 95-98	50000+ 100000+ 20000-100000+	50 5-40 10-15	0.05-5 2.5-15 0.5-75	100000+500-10000500-2000	miliseconds miliseconds miliseconds	miliseconds-minutes miliseconds-1 h miliseconds - minutes
Chemical rogen fuel cells	20-66	1000-20000+	negligible	800-10000	500-800	seconds	seconds-24 h +
Thermal TES	30-60	I	0.05-1	80-250	10-30	minutes	seconds-24 h $+$

 Table 2.1:
 Storage characteristics

2.2 Role of energy storage systems

Due to the intermittent nature of wind, wind power integration brings issues with system stability, reliability and power quality. Wind power plants have limited controllability due to their dependency on instantaneous wind conditions. In this context, ESS is considered an effective tool to enhance the flexibility and controllability of wind farms [17]. ESS can provide a reliable solution to control the WPP power output and to provide ancillary services to the grid [18]. ESS can facilitate the integration of wind power into the power system by participating in frequency regulation, synthetic inertia provision, voltage and reactive power support, and black start [19]. This facilitates the wind power plants to fulfil the future connection requirements. Battery Energy Storage Systems (BESS) and Supercapacitor Energy Storage Systems (SCESS) are considered the most interesting alternatives among the existing ESS technologies.

Unlike synchronous generators, wind turbine generators have limited or no contribution to inertia or frequency stability. High penetration of CIG into the grid affects the system's inertia response and the ability of the system to recover frequency stability after a disturbance. In the power system context, inertia response is defined as the energy exchanged by the grid and the rotor of a synchronous machine in case of a frequency deviation due to the rotor moment of inertia [20]. Therefore, the inertial response is inherent in the system due to the rotating mass of the large synchronous generators. When a frequency event occurs, the kinetic energy stored in the rotors of synchronous machines is released or stored, reducing the frequency deviation in the system [21]. However, in power converters, no rotating mass can provide inertia. Therefore, ESS can contribute to a virtual or synthetic inertial response by the wind turbine. Virtual or synthetic inertia is the ability of a grid-connected power converter to exchange energy with the grid when a frequency event occurs [2]. The ESS virtual inertial response can thus contribute efficiently to maintaining the system inertia [22-24]. SCESS are suitable for inertia support as they are characterized by a high power density, providing high peak power almost instantaneously. However, the fast frequency response is limited to short periods because the supercapacitors have limited energy storage capacity. Moreover, the power system's frequency regulation capacity is one of the main issues to consider when integrating WPPs into the system. Frequency regulation requires a rapid response, high power capability and high rate performance. In this context, BESS can provide frequency support, enabling their participation in system frequency regulation [19].

The basic structure of a BESS or a SCESS depends on the voltage level and the power ratings. A typical structure consists of a battery or a supercapacitor bank linked to a dc/ac power converter. In WPPs, static synchronous compensators (STATCOMs) are used for fast reactive power compensation and grid code fulfilment. However, STATCOMS cannot provide inertia, frequency regulation or power-related services [25]. Under such conditions, a STATCOM with integrated ESS can provide fast and bidirectional control of both active and reactive power [26, 27]. Therefore, in recent years, ESS have been integrated with STATCOMs to provide frequency and inertia regulation capabilities [28, 29]. In this context, STATCOMs based on Modular Multilevel Converters (MMCs) present significant advantages in the medium voltage and high power ranges compared to other topologies [30]. The most suitable topology for ES-STATCOM realization is a Double Star Bridge Cell - Centralized Energy Storage (DSBC-CES) [31]. In DSBC-CES topology, the ESS can be installed in the converter dc-link. Moreover, it has the advantage that the design does not depend on the minimum dc link voltage, as the full bridge cells can generate both positive and negative voltage [32]. Thus, the converter can operate for low dc-link voltages, allowing the battery or supercapacitor bank to have lower dc voltage ratings.

2.3 Modelling and control of BESS

A battery is a device that converts the chemical energy contained in its active materials into electric energy through an electrochemical reaction [33]. The basic electrochemical unit of a battery is the cell. A battery consists of one or multiple cells connected in series and parallel to obtain the desired voltage level and capacity. Batteries have a significant potential for application to grid-level ESS because of their fast response, modularization, and flexible installation [34].

Among the existing battery technologies, lithium-ion batteries are applied to grid storage due to their high-output voltages, high-energy densities, long cycle life, and low self-discharge [35, 36]. Given the high energy density of lithium-ion batteries, they are an ideal alternative for integrating renewable energy sources in grid-level energy storage systems. However, some major disadvantages of li-ion batteries are their high cost and the detrimental effect that deep discharging has on their lifetime.

Battery modelling plays an essential role in performance approximation and battery design. Batteries have a nonlinear behaviour, thus developing reliable models adapted to each particular study is essential [37]. An equivalent circuit model is the most common and practical way of representing the dynamic behaviour of a battery [38]. For power systems applications, circuit-based models are suitable as the complex electrochemical processes of a cell can be transformed into electrical circuit elements (R, L, C). Two equivalent electrical battery models are presented: i) OCV function of SOC and ESR, ii) Thévenin equivalent.

The principal performance characteristics of batteries intended for power system applications are power and energy capacity, battery efficiency level, battery temperature, State of Charge (SOC), Depth of Discharge (DOD), battery self-discharge, battery sizing and operation requirements [10, 39].

2.3.1 BESS sizing

A practical sizing for the BESS based on DSBC-CES STATCOM topology is proposed. First, the nominal and operational dc-link voltage of the converter should

be set. According to [31], the required dc-link nominal voltage, $v_{dc,n}$, is defined as

$$v_{dc,n} = \frac{2\hat{V}_s}{k_{om}} = \frac{2 \cdot 1.05 \hat{V}_g (1 + \Delta V_{ac} + I_{pu} x_{pu})}{k_{om}}$$
(2.1)

where $v_{dc,n}$ is the required dc-link voltage, \hat{V}_s is the sum of grid voltage and the voltage drop in the equivalent output inductance, \hat{V}_g is the peak of the line-to-neutral voltage, ΔV is the maximum ac grid voltage variation in pu, x_{pu} is the per unit equivalent output reactance of the converter, k_{om} is the over-modulation factor, and I_{pu} is the output current ($I_{pu} = 1$ inductive output current is considered).

To achieve the desired nominal dc voltage, a number of battery racks must be stacked in series. The total number of battery racks connected in series, $N_{b,s}$ can be computed as:

$$N_{b,s} = ceil\left(\frac{v_{dc,n}}{v_{b,max}}\right) \tag{2.2}$$

where $v_{dc,n}$ is the nominal dc-link voltage and $v_{b,max}$ is the maximum voltage of a battery rack.

Finally, the total number of battery racks connected in parallel must fulfil two requirements: i) the active power requirement P_n and ii) the energy requirement E_n . The number of parallel-connected battery racks, $N_{b,p}$, is given by as

$$N_{b,p} = ceil \left[max \left(\frac{P_n}{N_{b,s} v_{b,min} C_r C_b}, \frac{E_n}{N_{b,s} E_b \left(SOC_{max} - SOC_{min} \right)} \right) \right]$$
(2.3)

where E_n is the nominal energy storage of the BESS, E_b is the nominal energy storage capacity of each battery module, C_b is the battery capacity, C_r is the maximum recommended C-rate by the manufacturer, $v_{b,min}$ is the battery minimum allowed voltage, SOC_{max} is the maximum allowed State of Charge and SOC_m is the maximum allowed State of Charge.

2.3.2 Equivalent electrical model: Model 1

The dynamic battery model is shown in Fig.2.2. The open circuit voltage (OCV) of the battery is dependent on the state of charge of the battery, and its characteristics are included through a look-up table [40]. The OCV - SOC curve for lithium-ion batteries is quite flat, around 5% OCV variation between 10% and 90% battery SOC [41]. The resistance placed in series with the voltage source, R_s , accounts for the cell's terminal voltage drop or rise when the battery is discharged or charged. It also represents the battery power capability and power losses. This added resistance is the so-called equivalent series resistance (ESR) of the cell. The values for ESR are typically obtained by empirical tests. This model computes the battery output current and voltage. Moreover, its complexity does not depend on the number of cells in series, $N_{b,s}$, and parallel, $N_{b,p}$. The model also provides an estimation of the equivalent SOC of the battery. Fig.2.3 shows a typical open-circuit voltage (OCV) versus SOC curve of a Li-ion battery. The SOC approximation is given by:



Figure 2.3: Typical OCV versus SOC curve for a Li-ion battery

$$SOC(t) = SOC(0) - \int_0^t \frac{i_{bat}(t)}{N_{p,b}C_b} dt$$
 (2.4)

where C_b is the capacity of a single battery rack, $N_{p,b}$ is the number of battery racks connected in parallel and $i_{bat}(t)$ is the instantaneous current flowing through the battery.



Figure 2.2: Model 1: OCV function of SOC and ESR

2.3.3 Equivalent electrical model: Thévenin equivalent

The proposed Thévenin-equivalent electrical model of a battery is presented in [42] and shown in Fig. 2.4. This topology generally proposes a trade-off between battery cell computational requirements and voltage precision [43, 44]. The model consists of: i) a voltage source that accounts for the OCV, ii) the resistance R_s is responsible for the immediate voltage drop or rise when discharging or charging the battery, ii) two RC branches $(R_1, C_1 \text{ and } R_2, C_2)$. The circuit elements OCV, R_s , R_1 , C_1 , R_2 and C_2 are dependent on SOC, current and temperature. R_1 and C_1 account for the fast dynamics in the double layer capacitance. R_2 and C_2 are responsible for the slower dynamics of the cell. Unlike the *Model 1*, the transient responses of the battery cells are considered in the Thévenin-equivalent model. Moreover, the effect of current and temperature on the dynamic behaviour of the battery is added.

Another aspect to consider is the self-discharge of the battery. A large resistor can be placed in parallel with the voltage source to represent the self-discharge. However, its impact can be neglected in short-term dynamic studies [45].

In the scope of this thesis, the use of the Thévenin-equivalent model equivalent model does not provide relevant dynamic behaviour to the power converter response. Therefore, the choice of *Model 1* for BESS modelling is recommended for frequency stability studies.



Figure 2.4: Model 2: Thévenin equivalent

2.4 Modelling and control of Supercapacitor Energy Storage System

A supercapacitor is based on the same principle as a conventional capacitor. Both store charge electrostatically (non-Faradaic) [12]. Ordinary capacitors have a very small amount of charge storage, i.e., a low energy density for electrical energy storage. In a common capacitor, the two conducting plates are separated by a dielectric, while in a supercapacitor are separated by an electrolytic solution. Electrochemical Double Layer Capacitors (EDLCs) are the most used supercapacitors in systems demanding high peak power for short durations [46]. The construction of an EDLC comprises two carbon electrodes separated by the electrolyte interface, which results in high capacitance ratings (kilofarads versus milli- and microfarads for conventional capacitors) [35]. The operating principle of supercapacitors provides high energy efficiency, high power density and a long operational lifetime.

Supercapacitor banks integrated with STATCOMs can provide inertia support and thus decrease the system's RoCoF. In a case of a power imbalance in the grid, the supercapacitors' high power density allows for a very fast power response. However, the fast frequency response is limited to short periods of time because supercapacitors have limited energy storage capacity [12].

2.4.1 SCESS sizing to provide inertia support

As for the BESS, a practical sizing for the SCESS based on DSBC-CES STATCOM topology is proposed.

Power rating of the SCESS

First, the power rating of the STATCOM, S_n , and the desired virtual inertia, H_v , are set according to the requirements of each particular system. Secondly, the maximum RoCoF allowed in the grid should be determined, $\frac{d\omega}{dt}\Big|_{max}$. Then, the maximum grid frequency deviation allowed, $\Delta \omega_{g_{max}}$, needs to be defined. Both the maximum RoCoF allowed and the maximum grid frequency deviation can be set to the grid code requirements (for example, according to the Nordic Synchronous Area requirements [47]) or any desired value for design. Finally, the maximum inertial power required in case of a frequency event is determined. The equation of motion in per unit form is described as [21]:

$$\Delta P_1 = \frac{2H}{\omega_0} \frac{d\omega}{dt} = P_m - P_e \tag{2.5}$$

where H is the inertia constant of the synchronous generator, P_m is the mechanical power supplied by the prime mover, P_e is the electromagnetic power, ω_0 is the rated angular frequency, ω is the actual angular frequency and ΔP_1 is the power mismatch. Following the equation of motion, the maximum power imbalance ΔP_1 will occur with the maximum angular frequency deviation $\frac{d\omega}{dt}$. Therefore, the required active power provided by the SCESS needs to satisfy the following equation (2.6). By analogy, the maximum active power required in per unit form, $\Delta P_{SCESS,max}$, is defined by:

$$\frac{2H_v}{\omega_0} \frac{d\omega}{dt}\Big|_{max} = \Delta P_{SCESS,max} \tag{2.6}$$

The power rating of the supercapacitor bank, P_{SCESS} , is computed as:

$$P_{SCESS} = \Delta P_{SCESS,max} S_n \tag{2.7}$$

dc-link voltage levels

First, the nominal and operational dc-link voltage of the converter should be set. According to [31], the required dc-link nominal voltage, $v_{dc,n}$, is defined as

$$v_{dc,n} = \frac{2\hat{V}_s}{k_{om}} = \frac{2 \cdot 1.05\hat{V}_g(1 + \Delta V_{ac} + I_{pu}x_{pu})}{k_{om}}$$
(2.8)

where $v_{dc,n}$ is the required dc-link voltage, \hat{V}_s is the sum of grid voltage and the voltage drop in the equivalent output inductance, \hat{V}_g is the peak of the line-to-neutral voltage, ΔV is the maximum ac grid voltage variation in pu, x_{pu} is the per unit equivalent output reactance of the converter, k_{om} is the over-modulation factor, and I_{pu} is the output current ($I_{pu} = 1$ inductive output current is considered). Then, the dc-link voltage range needs to be defined. Two main aspects must be considered to calculate the dc-link minimum voltage, $v_{dc,min}$: i) the dc current flowing through the dc-link; ii) the current flowing through the semiconductor devices of the converter. In the discharging phase of the supercapacitor, the dc voltage decreases while the dc current increases. For this reason, setting a proper dc-link minimum voltage level is essential not to damage the converter's semiconductor devices. Moreover, both

the dc and ac current components flowing through the semiconductor devices of the converter must be considered, as the arm currents include an ac and a dc component in the CES topologies. The current that the semiconductor device should handle, I_n , is the peak value of the arm current at the rated operation as defined by [32]:

$$I_n = \frac{\hat{I}_g}{2} + \frac{I_{dc,n}}{3} = \frac{\hat{I}_g}{2} + \frac{P_n}{3v_{dc,n}}$$
(2.9)

where \hat{I}_g is the peak of the converter output current, P_n is the nominal active power of the SCESS and $v_{dc,n}$ is given by 2.8. However, the dc-link voltage variation needs to be considered. In the discharging phase of the supercapacitor bank v_{dc} decreases considerably while P_n remains constant. Therefore, the dc current component increases substantially. Then, equation 2.9 can be written as

$$I_{max} = \frac{\hat{I}_g}{2} + \frac{I_{dc,max}}{3} = \frac{\hat{I}_g}{2} + \frac{P_n}{3v_{dc,min}}$$
(2.10)

where I_{max} is the maximum allowed current flowing through each arm of the converter, $I_{dc,max}$ is the maximum dc current and $v_{dc,min}$ is the minimum dc voltage. Then, the dc-link minimum voltage can be defined by:

$$v_{dc,min} = \frac{2}{3} \frac{P_n}{2I_{max} - \hat{I}_g}$$
(2.11)

Finally, the maximum dc-link voltage must be set not to exceed the supercapacitor voltage ratings. In this case, the SCESS is sized to provide support both for same positive and negative RoCoFs. Therefore, the available energy for the discharging phase is set equal to the available energy for the charging phase.

$$E_{charging} = E_{discharging} \tag{2.12}$$

Therefore, the maximum allowed dc-link voltage is given as

$$v_{dc,max} = \sqrt{2v_{dc,n}^2 - v_{dc,min}^2}$$
(2.13)

SCESS equivalent capacitance

First, the equivalent dc-link voltage dynamics are presented. Then, the equivalent supercapacitor bank capacitance is deducted. The dc-link is modelled as a pure capacitor [48]. The stored energy in the supercapacitor bank is $Cv_{dc}^2/2$. The dynamic equivalent circuit of the dc-link is shown in Fig. 2.5, and the dc voltage dynamics can be written as

$$i_C = C_{eq} \frac{d(v_{dc})}{dt} = \frac{P_{ac}}{v_{dc}}$$

$$\tag{2.14}$$

Then, the power flowing through the capacitor, P_c , is equal to ac power exchanged with the grid, P_{ac} .

$$P_{C} = \frac{1}{2} C_{eq} \frac{d(v_{dc}^{2})}{dt} = C_{eq} v_{dc} \frac{dv_{dc}}{dt} = P_{ac}$$
(2.15)

13

where i_C is the current flowing through the capacitor, C_{eq} is the equivalent capacitance of the supercapacitor bank, $v_d c$ is the voltage of the capacitor, S_n is the rated apparent power of the converter used as an interface between the capacitor bank and the grid, P_C is the power flowing through the capacitor and P_{ac} is the power exchanged with the ac grid.

In per unit form, the active power exchanged between the dc- and ac-sides can be described as

 $\Delta P_2 = \frac{C_{eq} v_{dc}}{S_n} \frac{dv_{dc}}{dt}$

(2.16)

$$C_{eq} \xrightarrow{i_C} v_{dc} \xrightarrow{+} v_{dc} \xrightarrow{P_{ac}} \frac{P_{ac}}{v_{dc}}$$

Figure 2.5: Dynamic equivalent circuit of the dc-link

After introducing the dc-link voltage dynamics, a method to obtain the SCESS equivalent capacitance is described. The inertial response is the energy exchanged by the grid and the rotor of a synchronous machine in case of a frequency deviation (due to the moment of inertia of the rotor) [20]. Therefore, the inertial response is inherent in the system due to the rotating mass of the large synchronous generators. When a frequency event occurs, the kinetic energy stored in the rotors of synchronous machines is released or stored, reducing the frequency deviation in the system [21]. However, in power converters, no rotating mass can contribute to inertia. Therefore, SCESS can provide a *virtual* or *synthetic* inertial response. Thus, virtual or synthetic inertia is the ability of a grid-connected power converter to exchange energy with the grid when a frequency event occurs.

An analogy between the potential energy stored in the electrical capacitance and the mechanical rotational inertial energy stored in the rotor of a synchronous generator can be determined [49]. The energy stored by a capacitor is compared to the kinetic energy stored in the moment of inertia of the mechanical rotational system as

$$\frac{1}{2}Cv^2 = \frac{1}{2}J\omega^2$$
 (2.17)

where C is the electrical capacitance, v is the voltage, J is the moment of inertia and ω is the angular velocity of J. Following the presented analogy, the desired SCESS synthetic inertia time constant, H_v , can be set equating ΔP_1 in (2.5) and ΔP_2 in (2.16).

$$\Delta P_1 = \Delta P_2 \tag{2.18}$$

$$\Delta P = \frac{2H_v}{\omega_0} \frac{d\omega}{dt} = \frac{Cv_{dc}}{S_n} \frac{dv}{dt}$$
(2.19)

$$\Delta E = \int \frac{2H_v}{\omega_0} \frac{d\omega}{dt} = \int \frac{Cv_{dc}}{S_n} \frac{dv}{dt}$$
(2.20)

$$\frac{2H_v}{\omega_0}\omega - 2H_v = \frac{Cv_{dc}^2}{2S_n} - \frac{Cv_{dc,n}^2}{2S_n}$$
(2.21)

The equivalent capacitance of the supercapacitor bank, C_{eq} , is obtained.

$$C_{eq} = \frac{4 H_v S_n \frac{\Delta \omega_{g_{max}}}{\omega_0}}{v_{dc,max}^2 - v_{dc,n}^2} = \frac{4 H_v S_n \frac{\Delta \omega_{g_{max}}}{\omega_0}}{v_{dc,n}^2 - v_{dc,min}^2}$$
(2.22)

2.4.2 SCESS sizing to provide frequency support

The dc-link voltage levels are calculated as in the previous section. If the focus is on frequency support, the equivalent capacitance of the SCESS can be calculated in the following manner. First, the desired rated power for the energy storage, P_{SCESS} , is chosen based on each particular application. Then the frequency support duration must be defined, T_s , and is the time the rated power P_{SCESS} is desired to be provided. According to the Nordic Synchronous Area requirements, the minimum support duration for the *short support duration* FFR is 5s. The minimum support duration for the *long support duration* FFR is 30s [50]. Finally, the supercapacitor bank equivalent capacitance can be calculated as

$$C_{eq} = \frac{2 P_{SCESS} T_s}{v_{dc,max}^2 - v_{dc,n}^2} = \frac{2 P_{SCESS} T_s}{v_{dc,n}^2 - v_{dc,min}^2}$$
(2.23)

Where P_{SCESS} is the active power rating of the bank, T_s is the support duration, $v_{dc,n}$ is the dc-link nominal voltage, $v_{dc,max}$ is the maximum allowed dc voltage and $v_{dc,min}$ is the minimum allowed dc voltage.

2.4.3 Supercapacitor banks

Supercapacitors are usually rated between 2.3 - 3 V. Therefore, as in batteries, supercapacitor cells need to be stacked in series and parallel to obtain the desired voltage level and capacity. The total number of cells connected in series, $N_{c,s}$ can be computed as:

$$N_{c,s} = ceil(\frac{v_{dc,max}}{v_c}) \tag{2.24}$$

where $v_{dc,max}$ is the maximum dc-link voltage and v_c is the rated supercapacitor cell voltage. As in batteries, the number of cells in series is only a function of the required dc-link voltage level. The total number of cells in the bank must fulfil two requirements: i) the equivalent capacitance C_{eq} (energy rating requirement) and ii) the supercapacitor bank output dc current i_{dc} (power rating requirement). The number of parallel-connected capacitor cells $N_{c,p}$ is given by:

$$N_{c,p} = ceil\left[max\left(\frac{N_{c,s}C_{eq}}{C_{cell}}, \frac{I_{dc,max}}{i_{dc,c_{max}}}\right)\right]$$
(2.25)

where C_{eq} is the equivalent capacitance of the bank, C_{cell} is the capacitance of a single capacitor cell, $I_{dc,max}$ is the maximum dc-link current, and $i_{dc,max}$ is the maximum output dc current handled by a single capacitor cell. Another important factor to consider in the implementation of EDLCs is their Equivalent Series Resistance (ESR). The ESR defines the total electronic and ionic contributions to inhibiting current flow from the cell and balancing circuits [12]. The equivalent series resistance of the supercapacitor bank can be defined as

$$R_{s,eq} = \frac{R_{s,c} N_{c,s}}{N_{c,p}}$$
(2.26)

In addition, as the supercapacitor is an electrochemical device, it is essential to consider its self-discharge due to leakage [51]. The leakage current flows into the capacitor to maintain the capacitor at its nominal voltage. In a supercapacitor bank, the leakage current is the sum of cell and balancing circuit leakage currents [52]. The leakage current is measured in experimental tests. The time constant, τ_{leak} , defines the time in which the supercapacitor bank will be discharged if no current is flowing in. Therefore, a constant current, i_{leak} , must constantly flow into the capacitor to maintain the dc-link voltage at its nominal value.

$$\tau_{leak} = \frac{v_{dc}C_{eq}}{i_{leak}} \tag{2.27}$$

where v_{dc} is the voltage of the bank, C_{eq} is the equivalent capacitance and i_{leak} is the total leakage current.

2.4.4 Equivalent electrical model of a SCESS

A model based on electrical characteristics is convenient for power system stability studies. A practical supercapacitor model consists of three main elements [53,54]: i) C_{eq} is the total capacitance of the device; ii) $R_{s,eq}$ is the equivalent series resistance that represents the electrical resistances of the electrodes and the ionic resistance of the electrolyte; iii) $R_{leak,eq}$ represents the total leakage of the supercapacitor through the different leakage mechanisms. In modern supercapacitor cells used for grid and heavy industrial applications, the cell capacitance stands in the range of 1–5000 F while the ESR is in the order of mOhm [52, 54].

The equivalent electrical model of the SCESS is represented in Fig. 2.6.



Figure 2.6: SCESS equivalent circuit model

2. Energy Storage Systems

3

Grid-forming power converters

Power converters can be mainly classified into grid-following and grid-forming depending on their operation mode [55]. Grid-following power converters are designed to deliver power to an energized grid and are represented as a current source connected to the grid in parallel with high impedance. These converters inject active and reactive power into the grid according to the desired set points. They must be synchronized with the ac grid voltage at the connection point to provide the desired power. Nowadays, grid-following converters are used most to interface renewable generation, such as wind power, with the grid. However, grid-following converters need a synchronous generator to form the grid voltage to operate. For this reason, grid-forming converters interfacing renewable energy sources to the power system have emerged in recent years to account for reducing the conventional synchronous generators. The grid-forming converters can be represented as an ideal ac voltage source with a low-output impedance, imposing the voltage amplitude and frequency of the local grid [56]. Therefore, grid-forming converters can be seen as a controllable ac source behind a coupling impedance. similar to a synchronous generator. Grid-forming converters are designed to provide functionalities of the synchronous generators such as inertial response, frequency support, black-start, and synchronization capabilities [57]. Several converter control strategies to provide the mentioned functionalities have been developed in recent years [58–63]. In this chapter, three grid-forming control strategies are presented and compared. The analytical findings are verified using detailed time-domain simulations in Matlab-Simulink.

3.1 Grid-forming converter control strategies

3.1.1 Power Synchronization Control

The Power Synchronization Control (PSC) uses the internal synchronization mechanism in ac networks similar to the operation of a synchronous generator [62,63]. In this approach, the active power is controlled as in a synchronous machine by adjusting the converter-voltage angle. This principle is based on the power transfer between two sources (two synchronous generators in power systems) and can be described as [21].

$$P = \frac{E_1 E_2}{X} sin(\theta) \tag{3.1}$$

where E_1 is the voltage amplitude of the SG 1, E_2 is the voltage amplitude of SG 2,

X is the total reactance between both sources and θ is the phase angle between the two sources. Active power versus load angle is one of the basic dynamic relations in power systems. This dynamic relation can be considered quasi-static due to the power system's slow dynamics (traditionally). Then, $sin(\theta)$ can be approximated to θ . Therefore, the active power transfer between the two power sources is given by

$$P = \frac{E_1 E_2}{X} \theta \tag{3.2}$$

Then, the theoretical maximum active power transfer can be described as

$$P_{max} = \frac{E_1 E_2}{X} \tag{3.3}$$

In grid-connected converters, this same principle can be applied as illustrated in Fig. 3.1. Then, by analogy, E_1 becomes the converter voltage E_c , E_2 becomes the voltage at the converter connection point with the ac grid E_g , and X is considered as the reactance between the converter and the grid X_f .



Figure 3.1: Simplified vsc converter - ac system connection

Then, neglecting the losses in the converter filter, the plant of the system is given by

$$P_{max} = \frac{E_g E_c}{X_f} \tag{3.4}$$

The fundamental block diagram for a grid-connected converter based on the PSC is illustrated in Fig. 3.2. The controller is responsible for maintaining synchronism between the ac grid and the converter, and providing the required active power response. The active power controller of the converter defines the load angle θ (3.5) The resulting output signal of the power controller is added to the rated angular frequency, and the converter's internal frequency is obtained. The internal frequency of the converter is then integrated to calculate the phase angle, θ , of the emulated virtual synchronous generator. The power transmitted is increased by shifting the output voltage phasor of the converter, as to that of interconnected SGs.



Figure 3.2: Block diagram of the PSC

The implemented structure is defined by 3.5 where ω_c is the converter internal frequency, ω_N is the rated grid frequency, P* is the active power reference, P_g is the active power exchanged with the ac grid and k_p is the controller proportional gain.

$$\omega_c = \omega_N + k_p \left(P^* - P_g \right) \tag{3.5}$$

The obtained closed loop transfer function of the system shown in Fig. 3.2 is given as

$$G_{cl}(s) = \frac{k_p P_{max}}{s + k_p P_{max}} \equiv \frac{\alpha}{s + \alpha}$$
(3.6)

The resulting transfer function is compared to a general first order transfer function and the controller gain, k_p , is obtained. The controller bandwidth is α .

$$k_p = \frac{\alpha}{P_{max}} \tag{3.7}$$

The block diagram of PSC is shown in Fig. 3.3 as proposed in [63]. The same control structure is used for the analysis of the different grid-forming converter control strategies presented in this chapter. In this case, the controller is set as a proportional controller, k_p , with value $\omega_N/10$. The test system data is described in Table 3.1.





Figure 3.3: Implemented control structure of PSC

Parameter	Value	Unit
Rated power	12.7	kVA
Output Voltage (line-to-line)	400	kV
Nominal grid frequency ω_N	50	Hz
Filter bandwidth ω_f	31.4	rad/s
Active resistance R_a	0.1	pu
Output converter reactance X_f	0.1	pu
Output converter resistance R_f	0.01	pu

Table 3.1: Test system data

Fig. 3.4 shows the active power injected by the converter to the grid under a unit step change in the active power reference for strong (SCR = 10), medium (SCR = 5) and weak grid (SCR = 2). The measured active power follows the reference with the expected first order behaviour for medium and weak grids. In strong grid there is a slight overshoot in the response. However, there exists a decrease in the speed of response when the grid strength decreases. This is due to the grid reactance in the plant model. In weak grids the term X_g becomes higher therefore is not negligible (3.8). The main drawbacks of the PSC are: i) uncontrolled steady-state error in the active power response if the grid frequency is not equal to the rated; ii) Impossibility to emulate inertia.

$$P_{max} = \frac{E_g E_c}{X_f + X_g} \tag{3.8}$$



Figure 3.4: Active power response of PSC under unit step reference change (red SCR = 10, green SCR = 5, blue SCR = 2).

3.1.2 Virtual Synchronous Machine

Virtual Synchronous Machine (VSM) control is another grid-forming converter control strategy. The VSM control can mimic a synchronous machine behaviour by providing the power system with a virtual (or "synthetic") inertia. This control strategy was first proposed in [64]. The VSM approach is based on a direct emulation of the swing equation in the active power controller of the grid-forming converter. However, an uncontrolled steady-state error will exist if the grid frequency is not equal to the rated as in the PSC. The block diagram for a grid-connected converter based on the VSM is illustrated in Fig. 3.5.



Figure 3.5: Block diagram of the VSM

The implemented structure is defined by 3.9 where ω_c is the converter internal frequency, ω_N is the rated grid frequency, P^* is the active power reference, P_g is the active power exchanged with the ac grid, $M = \frac{2H}{\omega_0}$ is the ω_0 scaled virtual inertia and can be expressed in terms of the inertia constant H(s) [21], K_D is the virtual mechanical damping constant. However, the damping coefficient of the swing equation, K_D , introduces a steady-state droop effect of the value $1/K_D$ given a frequency deviation. This results in an uncontrolled steady-state error in the active power injected by the converter during frequency deviations [65].

$$\omega_c = \omega_N + \frac{1}{Ms + K_D} (P^* - P_g) \tag{3.9}$$

Then, the closed loop transfer function of the system is given as

$$G_{cl}(s) = \frac{\frac{P_{max}}{M}}{s^2 + \frac{K_D}{M}s + \frac{P_{max}}{M}} \equiv \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$
(3.10)

Comparing the closed loop transfer function with the general second order transfer function parameters M and K_D are obtained as

$$K_D = 2M\xi\omega_n = 2\xi\sqrt{MP_{max}} \tag{3.11}$$

where

$$M = \frac{2H}{\omega_0} \tag{3.12}$$

Fig. 3.6 shows the active power injected by the converter to the grid under a unit step change in the active power reference for strong (SCR = 10), medium (SCR = 5) and weak grid (SCR = 2). The virtual inertia is set to H = 5s and the damping ratio $\xi = 0.707$. The red curve shows a well-damped second order response as the controller is designed for strong grids. As in the PSC method, there exists a decrease in the speed of response when the grid strength decreases.



Figure 3.6: Active power response of VSM under unit step reference change (red SCR = 10, green SCR = 5, blue SCR = 2).

3.1.3 PI based active power controller

The presented PI-based active power controller was proposed in [66] and aims to improve the dynamic performance of grid-forming converters without compromising the inertia support or other good functionalities. The PI-based active power controller can fix the uncontrolled steady-state error in the active power response from the VSM and PSC implementations. Moreover, inertia emulation is possible, and the damping can be controlled. However, the integrator includes a zero in the closed loop, resulting in an overshoot in the active power response. The block diagram for a grid-connected converter based on the PI active power controller is illustrated in Fig. 3.7.



Figure 3.7: Block diagram of the PI-based active power controller

The converter internal frequency is defined by equation 3.13 where k_p is the proportional gain and k_i is the integral gain.

$$\omega_c = \omega_N + \left(\frac{1}{k_p + \frac{k_i}{s}}\right)(P^* - P_g)$$
(3.13)

The closed loop transfer function of the system is given by 3.14.

$$G_{cl}(s) = \frac{P_{max}k_p s + P_{max}k_i}{s^2 + P_{max}k_p s + P_{max}k_i} \equiv \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$
(3.14)

Moreover, an equivalence between the proposed PI active power controller and the swing equation can be also derived. This allows relating the bandwidth of the active power controller and the virtual inertia. The PI parameters of the VSM equivalent should be selected as

$$k_p = \xi \sqrt{\frac{1}{MP_{max}}} = \xi \sqrt{\frac{2X\omega_0}{H}} \; ; \; k_i = \frac{1}{M} = \frac{\omega_0}{2H}$$
 (3.15)

where $M = \frac{2H}{\omega_0}$ is the ω_0 scaled virtual inertia and can be expressed in terms of the inertia constant H(s) [21], and K_D is the virtual mechanical damping constant. However, the PI controller introduces an overshoot in the active power response. This is due to the presence of the zero in $G_{cl}(s)$. Therefore, an overshoot is observed in Fig. 3.9. One way to reduce the overshoot to include an active damping term, R_a , in the controller as shown in Fig. 3.8. This method is based on the design of two-degree-of-freedom current controller proposed in [67].



Figure 3.8: Block diagram of the PI-based active power controller with active damping

By introducing the active damping term, R_a , the closed loop transfer function of the system becomes

$$G_{cl}(s) = \frac{P_{max}k_p s + P_{max}k_i}{s^2 + P_{max}(k_p + R_a)s + P_{max}k_i}$$
(3.16)

Then, by setting $R_a = k_p$, one pole of $G_{cl}(s)$ is placed above the zero and the resulting transfer function is defined as

$$G'_{cl}(s) = \frac{P_{max}k_p}{s + P_{max}k_p} \equiv \frac{\alpha}{s + \alpha}$$
(3.17)

The PI controller parameters can be then described as

$$k_p = \frac{\alpha}{P_{max}} \quad ; \quad k_i = \frac{\alpha^2}{P_{max}} \quad ; \quad R_a = k_p \tag{3.18}$$

The relation between the controller bandwidth, α , and the virtual inertia provision is

$$\alpha = \sqrt{\frac{P_{max}}{M}} \tag{3.19}$$

Fig. 3.9 shows the active power injected by the converter to the grid under a unit step change in the active power reference for strong (SCR = 10), medium (SCR = 5) and weak grid (SCR = 2). A virtual inertia of H = 5s is seleted and a damping

ratio of $\xi = 0.707$. By using the active damping term R_a , the active power response becomes more damped, maintaining the same speed. A first-order unit step response is obtained for strong grids. However, for medium and weak grids, a slight overshoot appears. As the SCR ratio of the grid decreases, the active power response becomes slower and slightly damped.



Figure 3.9: Active power response of PI-based active power controller under unit step reference change (red SCR = 10, green SCR = 5, blue SCR = 2).

Fig. 3.10 shows the active power injected by the converter to the grid under a grid frequency variation from 50 Hz to 48 Hz with a RoCoF of 2 Hz/s for the different SCR. The inertial power response reaches a steady-state value of 0.4 pu as expected from (2.6) when 5s of virtual inertia is set. As in the active power step response, decreasing the SCR ratio implies a slower and more oscillating response. By implementing the active damping R_a , the overshoot in the inertial power response is removed for strong and medium grids. However, for weak grids, a slight overshoot can be observed.



Figure 3.10: Active power response of PI-based active power controller under unit step reference change (red SCR = 10, green SCR = 5, blue SCR = 2).

3. Grid-forming power converters

4

DC-link control strategies

Several studies have assessed the ac dynamics of grid-forming power converters, as mentioned in Chapter 3. However, a few research has focused on the dc-link voltage control (DCV) of GFM converters [62,63,68]. Conventional GFM control strategies use the active power loop to synchronize the converter with the ac grid. The DCV is added as an outer loop in cascade with the active power controller (APC). However, this method can limit the capability of the converter to provide an inertial response. In the cascaded control structure, the DCV calculates the reference active power for the active power loop. Then, the dc-link voltage controller needs to be set slower than the APC (often set as 10 times slower in cascaded structures). For example, in case of a negative frequency deviation in the grid, the dc-link needs to be discharged fast to deliver to the ac grid the required inertial power. The dc-link controller will try to maintain the dc voltage constant, while the active power controller will try to inject active power to the grid. Then, if both controllers have similar speeds, they will start *fighting* against each other, and the converter will not be able to provide the required inertial response [69]. For this reason, the classical approach of cascading the dc-link voltage controller with the APC is not suitable for providing an inertial response.

Some inertia emulation control strategies designed for grid-connected power converters have been proposed [70–72]. These control strategies generally use the dynamics of the dc-link to emulate the behaviour of the SGs rotor to provide a synthetic inertial response. However, these methods generally still need a PLL to realize grid synchronization. In [73], an inertia emulation strategy based on the swing equation is proposed, which utilizes the dynamics of the dc-link capacitor to realize self-synchronization. However, important grid frequency deviations can cause instabilities in the converter and make the dc voltage exceeds its operational limits.

In this chapter, a dc-voltage based synchronization control is proposed. The dc-link voltage control directly generates the internal frequency of the converter used to synchronize the GFM converter with the grid. This method can provide an inertial response to the grid and operate normally in weak grids without causing converter instabilities. This control strategy is presented to illustrate how it can give an inertial response and how this inertial response influences the dynamics of the dc voltage and the frequency of the ac grid. The presented schemes for virtual inertia provision are assessed and compared between them. Moreover, they are compared against the conventional control strategies for cascaded dc-link controllers in cascade with the

APC. The proposed method used the dynamics of the converter dc-link to realize grid synchronization. The dc-link voltage controller proposed approach controls the magnitude of the SCESS dc terminal voltage while realizing grid synchronization by the dynamics of the dc-link capacitance.

4.1 Method 1: Cascaded dc-link voltage controller

The dc-link voltage controller is used to regulate the SCESS dc voltage level and to calculate the reference active power, P^* , for the active power controller [63]. The energy, $W_{dc} \equiv v_{dc}^2$, is used to represent the dc voltage dynamics instead of the dc voltage itself. If operating with the error $(v_{dc}^* - v_{dc})$, the closed-loop dynamics would be dependent on the operating point [48]. As power is derivative of energy, having the dc-link voltage as a proportional gain with the dimension angular frequency, k_{dc} can be considered the DCV bandwidth [63]. The DCV structure is shown in Fig. 4.1 and the proportional gain k_{dc} can be calculated as:

$$k_{dc} = \frac{\alpha_{dc}C}{2} \tag{4.1}$$

where C is the dc-link equivalent capacitance in per unit and $\alpha_d c$ is the controller bandwidth. The unit of k_{dc} becomes then rad/s. For this reason, energy ($W = v^2$) multiplied by a derivative action results in power. The dc-link voltage controller structure is shown in Fig. 4.1.



Figure 4.1: dc-link voltage controller

If the converter aims to provide an inertial response, then the dc-link voltage should be set very slowly compared to the APC. Otherwise, the dc-link controller will try to maintain the dc voltage constant, while the active power controller will try to inject active power to the grid. Then, if both controllers have similar bandwidths, they will start *fighting* against each other, and the converter will not be able to provide the required inertial power. However, a slow dc-link voltage controller is unsuitable as an inertial response can not be provided. Moreover, the active power can not be easily limited if the inertial power response, higher inertia will result in a lower controller bandwidth, thus, a slower controller. These disadvantages can be overcome by using an energy controller in cascade with the dc-link voltage controller. The energy controller provides the dc-link voltage reference to the dc-link voltage controller as shown in Fig. 4.2. This cascaded control structure allows the converter to have a fast dc-link and active power controllers while maintaining the capability to provide synthetic inertia. This approach allows maintaining both the APC and the dc voltage controller fast by imposing the required dc-link voltage variation in case of a frequency deviation in the grid. ΔW_{dc} is defined as the required energy variation in the supercapacitor to provide the necessary synthetic inertia during a grid frequency disturbance. Then, the energy reference W_{dc}^* can be written as

$$W_{dc}^{*} = W_{dc,n} + \Delta W_{dc} = W_{dc,n} + \frac{P_{H}}{s}$$
(4.2)

As the energy stored in a capacitor is $Cv_{dc}^2/2$, the voltage reference v_{dc}^{2*} can be written as

$$v_{dc}^{2*} = \frac{2}{C} W_{dc}^* = \frac{2}{C} (W_{dc,n} + \Delta W_{dc})$$
(4.3)



Figure 4.2: Energy controller

Then, the energy controller needs an input corresponding to the inertial power required to be injected into the grid in case of a frequency deviation. The inertial emulation loop (IEL) concept is first presented in [74] and can be used for this purpose. The inertia emulation loop based on the structure of a PLL provides an active power reference corresponding to the desired amount of inertia. The IEL is tuned to behave equivalently in terms of inertial power contribution to a synchronous machine. This method provides the inertial power reference, P_H , to the energy controller. It allows it to generate an inertial response while maintaining a fast active power controller without exceeding the converter current limits. The output of the IEL provides the inertial power contribution, P_H , to the energy controller, where P_H is integrated to obtain ΔW_{dc} . The IEL structure is shown in Fig. 4.3.



Figure 4.3: Inertia emulation loop

The APC and DVC can then theoretically have the same bandwidth using this method. Then, the proportional gain of the DCV can also be written as

$$k_{dc} = \frac{\alpha_{dc}C}{2} = \frac{\alpha_{pc}C}{2} \tag{4.4}$$

where α_{pc} is the bandwidth of the active power controller in rad/s.

4.2 Method 2: dc-voltage based synchronization control

A dc-link voltage based synchronization control (DVSC) to synchronize the converter with the ac grid using the dc-link dynamics is proposed. The block diagram of the proposed controller is shown in Fig. 4.4, where P_{max} is the theoretical maximum active power transfer (as explained in Chapter 3), C is the SCESS equivalent capacitance, and R_a and R_b are two active damping terms. The active damping R_a acts on the active power, and the active damping R_b acts on the energy (as v_{dc}^2 is equivalent to energy). The output of the dc-link voltage controller is added to the rated angular frequency and the converter's internal frequency is obtained. The internal frequency of the converter is then integrated to calculate the phase angle. Then the phase angle, θ , is multiplied by P_{max} and the active power injected to the grid is obtained. The active power provided, P, is then multiplied by 2/Cs to calculate the energy released from the supercapacitor bank.

Depending on the controller, one or two active damping terms, R_a and R_b , are included to 'mimic' the response to general second-order or first-order transfer functions. Three different types of controllers are presented and tested to assess the most suitable dc-link voltage controller: i) Proportional, ii) PI, iii) PID. These controllers are selected as they are the most commonly used in industry. In general terms, the proportional controller can reduce the raising time but will produce a steady-state error. On the other hand, a PI controller can be used to remove the steady-state error caused by the proportional controller but will cause an overshoot in the response. Finally, a PID controller removes steady-state error and decreases the overshoot. However, its derivative component is quite susceptible to noise disturbance. The tuning of the three controllers is based on the same principle.



Figure 4.4: Block diagram of general DVSC

4.2.1 Proportional-based DVSC

The block diagram for a grid-connected converter based on the DVSC with a proportional controller is illustrated in Fig. 4.5.



Figure 4.5: Block diagram of proportional-based DVSC

The implemented structure is defined by eq. 4.5 where ω_c is the converter internal frequency, ω_N is the rated grid frequency, v_{dc}^* is the dc-link voltage reference given by the energy controller, v_{dc} is the dc-link voltage measurement, P is the active power exchanged with the ac grid, and R_a is the active damping term.

$$\omega_c = \omega_N + k_p (v_{dc}^2 * - v_{dc}^2) - R_a P$$
(4.5)

Then, the closed loop transfer function of the system is given in equiation 4.6. Then by comparing 4.6 and the general second order transfer function the proportional gain k_p and active damping term R_a can be calculated. This can be done by including the active damping, R_a , in the controller. Using this method, a well-damped second-order system response can be obtained. The dynamics of the dc link voltage controller are governed by the location of the two poles of 4.6.

$$G_{CL,P}(s) = \frac{\frac{2P_{max}}{C}k_p}{s^2 + R_a P_{max}s + \frac{2P_{max}}{C}k_p}$$
(4.6)

$$G_{CL,P}(s) \equiv \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{4.7}$$

$$k_p = \frac{\omega_n^2 C}{2P_{max}} \qquad R_a = \frac{2\xi\omega_n}{P_{max}} \tag{4.8}$$

4.2.2 PI-based DVSC

The block diagram for a grid-connected converter based on the DVSC with a PI controller is illustrated in Fig. 4.6.



Figure 4.6: Block diagram of PI-based DVSC

The implemented structure is defined by 4.9 where ω_c is the converter internal frequency, ω_N is the rated grid frequency, v_{dc}^* is the dc-link voltage reference given by the energy controller, v_{dc} is the dc-link voltage measurement, P is the active power exchanged with the ac grid, R_a is the first active damping term, R_b is the second active damping term and C is the equivalent capacitance.

$$\omega_c = \omega_N + (k_p + \frac{ki}{s})(v_{dc}^2 * - v_{dc}^2) - R_a P - R_b \frac{2}{Cs} P$$
(4.9)

The resulting closed loop transfer function of the system is given in 4.10. Then by comparing 4.10 and 4.11 the proportional gain k_p , the integral gain k_i , active damping R_a and active damping R_b can be obtained. Using this approach, one pole of 4.10 is placed above the zero, thereby cancelling its impact. This is achieved by including the two active dampings, R_a and R_b . Therefore, a well-damped second-order system response can be obtained.

$$G_{CL,PI}(s) = \frac{\frac{2P_{max}}{C}k_ps + \frac{2P_{max}}{C}k_i}{s^3 + R_a P_{max}s^2 + \frac{2P_{max}}{C}(k_p + R_b)s + \frac{2P_{max}}{C}k_i}$$
(4.10)

$$G_{CL,PI}(s) \equiv \frac{\omega_n^2(s+\omega_n)}{(s^2+2\xi\omega_n s+\omega_n^2)(s+\omega_n)}$$
(4.11)

$$G_{CL,PI}(s) \equiv \frac{\omega_n^2 s + \omega_n^3}{s^3 + (\omega_n + 2\xi\omega_n)s^2 + (2\xi\omega_n^2 + \omega_n^2)s + \omega_n^3}$$
(4.12)

$$k_p = \frac{\omega_n^2 C}{2P_{max}} \qquad k_i = \frac{\omega_n^3 C}{2P_{max}} \qquad R_a = \frac{\omega_n (1+2\xi)}{P_{max}} \qquad R_b = \frac{\xi \omega_n^2 C}{P_{max}} \tag{4.13}$$

4.2.3 PID-based DVSC

The block diagram for a grid-connected converter based on the DVSC with a PID controller is illustrated in Fig. 4.7.



Figure 4.7: Block diagram of PID-based DVSC

The implemented structure is defined by 4.14 where ω_c is the converter internal frequency, ω_N is the rated grid frequency, v_{dc}^* is the dc-link voltage reference power reference given by the energy controller, v_{dc} is the dc-link voltage measurement, P is the active power exchanged with the ac grid, R_a is the first active damping term, R_b is the second active damping term and C is the equivalent capacitance.

$$\omega_c = \omega_N + (k_p + \frac{ki}{s} + k_d s)(v_{dc}^2 * - v_{dc}^2) - R_a P - R_b \frac{2}{Cs} P$$
(4.14)

The system resulting closed-loop transfer function is given in 4.15. Then by comparing 4.15 and 4.16, the proportional gain k_p , the derivative gain k_d , the integral gain k_i , the active damping R_a and the active damping R_b are obtained. Two poles of 4.15 are then placed above the two zeros, thereby cancelling its impact. Therefore, a first-order transfer function is obtained, and the speed of response is governed by the bandwidth α .

$$G_{CL,PID}(s) = \frac{\frac{2P_{max}}{C}k_ds^2 + \frac{2P_{max}}{C}k_ps + \frac{2P_{max}}{C}k_i}{s^3 + (\frac{2}{C}k_d + R_a)P_{max}s^2 + \frac{2P_{max}}{C}(k_p + R_b)s + \frac{2P_{max}}{C}k_i}$$
(4.15)

$$G_{CL,PID}(s) \equiv \frac{\alpha(s+\alpha)^2}{(s+\alpha)^3}$$
(4.16)

$$k_{d} = \frac{\alpha C}{2P_{max}} \qquad k_{p} = \frac{\alpha^{2} C}{P_{max}} \qquad k_{i} = \frac{\alpha^{3} C}{2P_{max}}$$

$$R_{a} = \frac{2\alpha}{P_{max}} = \frac{k_{d}}{2} \qquad R_{b} = \frac{\alpha^{2} C}{2P_{max}} = \frac{k_{p}}{2}$$

$$(4.17)$$

4.3 Tests

The converter's dynamic performance is analysed under various test cases to evaluate the effectiveness of the proposed dc-link voltage controllers and their tuning approach. First, the control structure based on method 1 (APC cascaded with dc-link voltage controller) is tested. Then the three different DVSC structures are compared. Time domain simulations in PSCAD are performed to analyse the system's dynamic behaviour.

4.3.1 System of study

As a reference point, a simplification of the system presented in the IBESS project is used [27, 31, 75]. The system of study is presented in Fig. 4.8. A 400 MW WPP is modelled as a grid-following converter. A 112 MVA grid-forming SCESS (GFM-SCESS) with a 45 MW supercapacitor bank provides voltage and inertia support at the PCC. Both converters are connected in parallel at the PCC and to the 33 kV grid. No cables, shunt filters and reactors or transformers are considered in this study, as the main purpose is to study the inertial response of the GFM-SCESS under grid frequency disturbances. The nominal ratings for the GFM-SCESS and equivalent WPP are given in Table 4.1 and Table 4.2. The GFM-SCESS controller parameters are described in Table 4.4. The grid parameters are given in Table 4.3.



Figure 4.8: Diagram of the simplified WPP system with GFM-SCESS

4.3.2 Test cases and evaluation criteria

The system described in Fig. 4.8 is modelled in PSCAD and the simulation results are presented. The performed test cases are a grid frequency deviation and a dc-link voltage reference step change. The design verification criteria are: i) The converter stays in synchronism with the grid, and the system maintains its stability; ii) The GFM-SCESS provides the required synthetic inertial response; iii) The converter output current must not exceed the converter ratings; iv) The dc-link voltage varies according to the design; v) The dc-link current must not exceed the supercapacitor bank and converter ratings; vi) The dc-link voltage controller can be set as fast as the active power controller.

Parameter	Symbol	Value	Unit
Rated Apparent Power	S_{ns}	112	MVA
Rated Reactive Power	Q_{ns}	102	Mvar
Rated Active Power	P_{ns}	45	MW
Nominal dc-link voltage	$v_{dc,n}$	35 0.81	kV pu
Maximum dc-link voltage	$v_{dc,max}$	43.1 1	kV pu
Minimum dc-link voltage	$v_{dc,min}$	24.4 0.57	kV pu
Maximum inertial power	ΔP_{max}	0.4	pu
Maximum arm current	I_{max}	2000	А
Overmodulation factor	k_{om}	1.86	pu
SC bank equivalent capacitance	C_{eq}	0.212	F
Virtual inertia SC	H_v	5	\mathbf{S}
Output Voltage (line-to-line)	V_{g}	33	kV
Output converter reactance	x_{spu}	0.1	pu
Output converter resistance	r_{spu}	0.01	pu

Table 4.1: Parameters of the GFM-SCESS

 Table 4.2: Parameters of the emulated WPP

Parameter	Symbol	Value	Unit
Rated capacity	S_{nw}	444	MVA
Rated Active Power	P_{nw}	400	MW
Output Voltage (line-to-line)	V_{g}	33	kV
Output converter reactance	x_{wpu}	0.1	pu
Output converter resistance	r_{wpu}	0.01	pu

The grid model consists of an ideal voltage source with a line-to-line voltage of 33 kV behind the grid impedance. For this study, a weak grid is considered, and the Short Circuit Ratio (SCR) is set to 3. The maximum RoCoF in the grid is set to 2 Hz/s, and the maximum grid frequency is 3 Hz. These frequency variations will not occur in the current power system but are set to test the converter control in a sort of *worst-case scenario*.

 Table 4.3:
 Grid parameters

Parameter	Symbol	Value	Unit
Output Voltage (line-to-line)	V_g	33	kV
Frequency	f_n	50	Hz
Maximum RoCoF	$\frac{d\omega}{dt}\Big _{max}$	2	$\mathrm{Hz/s}$
Maximum grid frequency deviation	$\Delta \omega_{g_{max}}$	3	Hz
Short Circuit Ratio	SCR	3	pu

4.3.3 Method 1

The grid-forming converter control strategy used is proposed in [76]. The control structure of the GFM-SCESS is described in Fig. 4.9 when a dc-link voltage controller cascaded with the APC is used. The APC implemented is the PI-based regulator described in section 3.1.3. The PCC voltage controller regulates the PCC voltage magnitude and calculates the reference magnitude of the virtual back-emf, e_{emf}^{dq*} of the emulated virtual machine [66]. It is implemented as a simple current-droop model. The current controller is used to regulate the converter current and it calculates the reference voltages, e_c^{dq*} , for the modulation stage of the converter [77]. The current controller is based on a PI controller with PCC-voltage feed-forward and cross-coupling cancellation, which allows controlling components d and q independently. The reference for the current controller, i_f^* , is calculated using virtual admittance. The virtual admittance is used to calculate the current reference input to the current controller [76]. The equivalent 400 MW WPP is modelled as a PLL-synchronized grid-following converter, as shown in Fig. 4.8. It provides the active power setpoint to emulate the WPP.

Parameter	Symbol	Value	Unit			
Inertia emulation loop						
Virtual inertia	H_v	5	\mathbf{S}			
Bank equivalent capacitance [pu]	C_{eq}	2.32	pu			
Damping ratio	ξ	0.707	pu			
dc-link voltage controller						
dc-link voltage controller bandwidth [Hz]	α_{dc}	5	Hz			
Active power controller						
Active power controller bandwidth [Hz]	$lpha_{pc}$	5	Hz			
PCC voltage controller						
PCC-voltage controller bandwidth [Hz]	α_{vc}	5	Hz			
PCC-voltage controller integral gain	$K_{i,vc}$	188.5	\mathbf{pu}			
PCC-voltage controller droop constant	$K_{d,vc}$	0.05	pu			
Virtual admittance						
Virtual reactance	X_v	0.5	pu			
Virtual resistance	R_v	0.5/2	\mathbf{pu}			
Current controlle	er					
Current controller bandwidth	α_{cc}	500	Hz			

 Table 4.4:
 Parameters of the GFM-SCESS controller

Inertia emulation loop





dc-link voltage controller





PCC voltage controller

Virtual admittance

Current controller



Figure 4.9: GFM-SCESS control structure

39

Grid frequency deviation

In this test case, a RoCoF of 2 Hz/s is applied, and the grid frequency is reduced from 50 Hz to 47 Hz. A weak grid is considered (SCR = 3). The inertia constant is selected as $H_v = 5$ s, meaning that the frequency disturbance should result in an inertial response of 0.4 pu (see eq. 2.6). The dynamic responses of the converter during the frequency event are shown in Fig. 4.10 and Fig. 4.11. The converter and grid frequency, active power and output current responses are presented in Fig. 4.10. Fig. 4.11 shows the dc-link voltage and current. The dynamic responses demonstrate that the design criteria are fulfilled.

Synchronism The converter needs to stay in synchronism with the grid. Fig. 4.10 shows that the internal converter frequency follows the grid frequency.

Inertial response The GFM-SCESS provides the required synthetic inertial response. According to (2.6), given a 2 Hz/s RoCoF, the inertial power should be 0.4 pu. Fig. 4.10 demonstrates that the converter active power reaches steady-state at 0.4 pu. For the IEL, a damping ratio of $\xi = 0.707$ is suggested as a compromise between speed and damping of the inertial response [74]. As the active power controller does not provide the inertia, the dc-link voltage can be set as fast as the active power controller. By implementing this approach, the converter controller and a fast dc-link voltage controller.

Converter ratings Fig. 4.10 shows the converter output current is around 0.5 pu, which leaves a margin for reactive current. Moreover, the dc-link current must not exceed 1pu. The maximum dc current value is reached when the dc voltage is the minimum. In steady state $P_{dc} = v_{dc}i_{dc} = 0.4$ pu. As the dc power is constant, the dc current needs to increase to compensate for the decrease in the dc voltage.

dc-link voltage The dc-link voltage variation verifies the supercapacitor bank design. According to the design, the minimum dc-link voltage allowed is 0.57 pu in case of a 2Hz/s RoCoF and a 3 Hz grid frequency variation. Fig. 4.11 shows that the dc voltage reaches the minimum allowed dc-link voltage once the grid frequency deviation is cleared. The total usable energy stored in the dc-link is released to provide an inertial response to counteract the RoCoF in the grid. As a proportional controller is implemented, a steady-state error between the reference and actual dc voltage will exist if the grid frequency is not equal to the rated. The secondary and tertiary control reserves are activated once the frequency event is cleared. Then, the supercapacitor bank is slowly charged to not create any frequency disturbance in the grid.



Figure 4.10: Response of the GFM-SCESS during the frequency event. Grid frequency (dashed black), converter internal frequency (green), converter power (blue) and converter output current (red).



Figure 4.11: Response of the GFM-SCESS during the frequency event. Dc-link reference voltage (dashed black), dc-link voltage (green) and dc current (blue).

Impact of the dc-link voltage controller bandwidth, α_{dc} , on the inertial and dc voltage responses The dc-link controller can be set as fast as the active power controller. However, setting it slightly slower in real operation may be suitable. For this reason, the system is tested with different dc-link controller bandwidths, and its response is studied. Fig. 4.12 and Fig. 4.13 describe the active power and dc-link voltage responses for $\alpha_{dc} = \alpha_{pc}$, $\alpha_{dc} = \alpha_{pc}/2$, $\alpha_{dc} = \alpha_{pc}/5$. The inertial power response reaches the same steady state power, 0.4 pu. However, while decreasing the dc-link controller bandwidth, the power response becomes slower and more damped. On the other hand, the dc-link voltage response is hardly affected by the controller's speed.



Figure 4.12: Response of the GFM-SCESS during the frequency event. Comparison of the inertial power response with different dc-link voltage controller bandwidth. $\alpha_{dc} = \alpha_{pc}$ (blue), $\alpha_{dc} = \alpha_{pc}/2$ (green), $\alpha_{dc} = \alpha_{pc}/5$ (red).



Figure 4.13: Response of the GFM-SCESS during the frequency event. Comparison of the dc voltage response with dc-link voltage controller bandwidth. $\alpha_{dc} = \alpha_{pc}$ (blue), $\alpha_{dc} = \alpha_{pc}/2$ (green), $\alpha_{dc} = \alpha_{pc}/5$ (red), dc voltage reference (dashed black).

dc-link voltage step response

A 0.01 pu dc-link voltage reference step change is applied to validate the controller design. Low dc voltage variation results in a considerably high active power release, so the dc-voltage step change can not be set high. Fig. 4.12 and Fig. 4.13 describe dc-link voltage and active power responses for $\alpha_{dc} = \alpha_{pc}$, $\alpha_{dc} = \alpha_{pc}/2$, $\alpha_{dc} = \alpha_{pc}/5$. Once the frequency event is cleared, the supercapacitor bank must be charged again. However, if it is charged abruptly, the active power absorbed from the grid will be very high and negatively impact the system's frequency. Therefore, a slow charge of the supercapacitor bank is recommended. The dc voltage reference can be set as a ramp with a low slope. By changing the reference slowly, the dc voltage controller can remain fast, and the system's frequency will not deteriorate.



Figure 4.14: Response of the GFM-SCESS after a 0.01 pu dc voltage step. Comparison of the dc voltage step response with different dc-link voltage controller bandwidth. $\alpha_{dc} = \alpha_{pc}$ (blue), $\alpha_{dc} = \alpha_{pc}/2$ (green), $\alpha_{dc} = \alpha_{pc}/5$ (red), dc voltage reference (dashed black).



Figure 4.15: Response of the GFM-SCESS after a 0.01 pu dc voltage step. Comparison of the active power response with different dc-link voltage controller bandwidth. $\alpha_{dc} = \alpha_{pc}$ (blue), $\alpha_{dc} = \alpha_{pc}/2$ (green), $\alpha_{dc} = \alpha_{pc}/5$ (red).

4.3.4 Method 2

The GFM converter control used is the same as in the previous section. The dc-link voltage controller bandwidth for all DVSC types is set to 5 Hz and the damping ratio at 0.707. The overall GFM-SCESS control system is shown in Fig. 4.16.





Modulation



PCC voltage controller

Virtual admittance

Current controller



Figure 4.16: GFM-SCESS control structure

dc-link voltage step response

A 0.01 pu dc-link voltage reference step change is applied to validate the controller's designs. Fig. 4.17 shows the converter responses of the three controllers with a bandwidth, α_{dc} , of 5 rad/s: Proportional controller (blue), PI controller (red), PID controller (green), dc voltage reference (dashed black). The measured dc voltage follows the reference and behaves according to the controllers' design. However, the PID initial response differs from the P and PI ones, probably due to the derivative term. The PID also provides a response with less overshoot. The P and PI provide very similar responses even though the PI response oscillates slightly less. The three controllers provide a well-damped dc-link voltage response.



Figure 4.17: Response of the GFM-SCESS after a 0.01 pu dc voltage step. Comparison of the dc voltage step response with different dc-link voltage controller bandwidth. Proportional controller (blue), PI controller (red), PID controller (green), dc-link voltage reference (dashed black).

Grid frequency deviation

The test performed and parameters are the same as in Implementation 1. The dynamic responses of the converter during the frequency event are shown in Fig. 4.19 and Fig. 4.18. The converter and grid frequency, active power and output current responses are presented in Fig. 4.19. Fig. 4.18 shows the dc-link voltage and current.

Synchronism Fig. 4.19 shows that the internal converter frequency follows the grid frequency as in method 1. The DVSC controller can be used to synchronize the converter with the grid. However, the response obtained barely depends on the type of controller used, which means that the converter response is mainly governed by the energy controller.

Inertial response The GFM-SCESS provides the required synthetic inertial response as in method 1. Moreover, the converter inertial response barely depends on the type of controller used.

Converter ratings Fig. 4.19 shows the maximum converter output current is around 0.5 pu and reaches a steady state at 0.4 pu, which leaves a margin for reactive current. Moreover, the dc-link current must not exceed 1 pu. The maximum dc current value is reached when the dc voltage is around the minimum.

dc-link voltage The dc-link voltage variation verifies the supercapacitor bank design as in method 1. According to the design, the minimum dc-link voltage allowed is 0.57 pu in case of a 2Hz/s RoCoF and a 3 Hz grid frequency variation. Fig. 4.18 shows that the dc voltage reaches the minimum allowed dc-link voltage once the grid frequency deviation is cleared. In the case of using the proportional controller, a steady-state error between the reference and actual dc voltage will exist if the grid frequency is not equal to the rated. This steady-state error can be avoided by using the PI or the PID controllers.



Figure 4.18: Response of the GFM-SCESS during the frequency event. Proportional controller (blue), PI controller (red), PID controller (green), dc-link voltage reference (dashed black).



Figure 4.19: Response of the GFM-SCESS during the frequency event. Proportional controller (blue), PI controller (red), PID controller (green), dc-link voltage reference (dashed black).

Conclusions

This thesis has discussed the role of energy storage systems in the power system and wind power applications. Different types of energy storage technologies have been introduced. Battery Energy Storage Systems and Supercapacitor Energy Storage Systems are considered the most interesting alternatives among the existing ESS technologies. SCESS are suitable for inertia support, while BESS can provide frequency regulation of the power system. Therefore, recommendations on the size of BESS and SCESS based on the functionalities to be implemented have been proposed. Besides, equivalent circuit models for both technologies have been described. ESS can be integrated with VSC-based STATCOMs to provide inertial support and frequency regulation. These converters use GFM control strategies to provide the desired power-related services. Then, the GFM-SCESS dynamic performance was analyzed under various test cases. The results show that the converter stays in synchronism with the grid during high RoCoFs in a weak grid, provides the desired synthetic inertial response, and the dc-link voltage varies according to the SCESS design. Finally, the dc-link voltage based synchronization control proposed has shown good results. The results show the ability of the DVSC to provide an inertial response under weak grids without the need for an active power loop.

5. Conclusions

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