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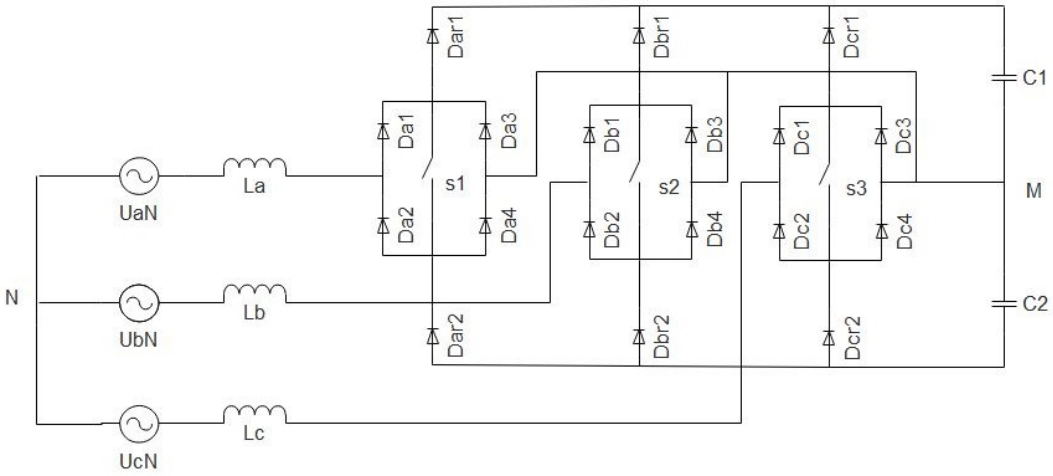

Vienna topology based active rectifier: Modulation and loss calculation

Master of Science Thesis

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Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2018

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Abstract

Due to the increase in the usage of renewable energy sector, the demand for energy has increased manifolds. With the increasing use of power electronic converter for processing power, it has become vital to select the topology for any given application. Rectifier market is huge because of its application as an active front end. So, one important aspect in designing is to determine the losses at various levels because of the efficiency constraint put forwarded by the end users.

In this thesis work an active rectifier using Vienna topology has been simulated in MATLAB. For modulating the switching pattern for sinusoidal waveform, sine triangle with third harmonic injection PWM technique is used. It gives a better voltage utilization as compared to the regular sine triangle PWM. Based on the rating, the components are selected, and loss calculation is performed and is compared with a two-level topology. 25 kW input power and 700 V DC link voltage are used in both cases. Considering only the semiconductor losses, the efficiency at the rated power is 97.9% for the two level converter and 99.2% for the Vienna rectifer.

Keywords: Vienna rectifier, PWM modulation, Active front end, Third Harmonic Injection.

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Vishal Mathur, Göteborg, 2018

Contents

1

Introduction

1.1 Problem Background

Power electronic converters depending upon their usage may exhibit characteristics, which in turn affects the power quality of mains supply in terms of low power factor and harmonic distortion. Such behaviour imposes a penalty on the users of these converters by the grid supplier. Using active front end rectifier is a common practice to overcome this problem. The most common topology in use is a two level active rectifier, which is relatively simple and robust and therefore its use is widespread. But, the distorting effect it has on the grid supply is quite significant and somehow does not provides a solution. It further needs a filter that can limit the current distortion by capturing the lower harmonics locally. This increases the size of the components as well as the cost of installation.

To overcome this problem, the use of multilevel converter as active front end (AFE) is becoming increasingly popular. This reduces the harmonic content of current at input side, thereby giving it a more sinusoidal shape. Moreover switching at higher frequency becomes feasible which in turn reduces the size and cost of the components required, thereby making the converter more compact.

1.2 Previous Work

The usage of active front end rectifiers is not a new notion, but nevertheless an ongoing and rapidly developing field. Extensive work has already been done involving novel circuits and devices with very interesting results. Many practical aspects are considered depending upon the constraints that may be relevant for a particular application from the user's end. Vienna topology has been used in power scale ranging from few kW's to MW for power system for different scenarios. As it constitutes the very first step towards the multilevel behaviour as compared to the conventional two level topology with less switching devices, it becomes an interesting proposition to carry out its study.

1.3 Purpose

The goal of the work undertaken in this thesis is to implement a model of an active rectifier based on MATLAB simulation using a three level Vienna topology for determining the semiconductor losses. Thereafter, a comparison is done based on the loss calculation between the two and three level converters.
The conventional two level rectifier utilizes six switches. The Vienna rectifier uses three switches and outputs a three level characteristics of phase voltage. It has a sinusoidal mains current at the input along with low common mode signal and displays ohmic mains behaviour. By comparison it can be shown that the Vienna rectifier has got greater advantage in terms of losses over the two level topology.

2

Theory

Three phase rectifiers are commonly used in several applications including drives, uninterrupted power supplies and various utility interfaces. Since a few decades the surge in renewable energy sector has increased the interest for research in development of power electronic systems. Various topologies exists today depending upon requirements and applications. As the main concern of this work is with a unidirectional power flow i.e: conversion from AC to DC side, the unidirectional Vienna topology is chosen.

As described in [1][3][4], a unidirectional three phase/switch/level PWM rectifiers has the following advantages as compared to a two level conventional rectifier:

*Lower harmonic level of the mains current.
*Lower blocking voltage stress on semiconductor devices.
*Less number of active switches (topology a)
*Higher power density.

However, the controlling complexity is higher compared to a two level topology, as the capacitive centre point balancing of the output voltage requires a symmetrization of output voltages, which would be analysed at a later stage.

The chapter herein presents the description of a unidirectional three phase/level/wire PWM rectifier circuit structure along with its operation. The two different topologies of the Vienna structures are given along with the rectifier voltage equations. Secondly, the space vector modulation is explained and the limitation associated with its operation is considered. The DC link neutral point potential is also discussed as it has got a direct relevance with the modulation method employed.

2.1 Operation of a two Level converter

Two level converters are widely used in power conversions within a wide range of power levels. The market domination of such converters have remained strong specially in the low voltage range of 690 V_{rms} line to line voltage for IEC and 575 V_{rms} line to line for ANSI standard[12]

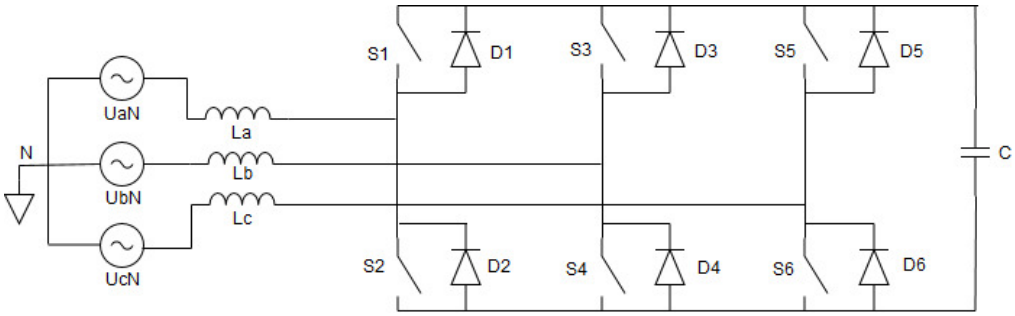

Figure 2.1: Two level converter

As shown in the Figure 2.1, the conventional two level VSC topology consists of six switches and corresponding six anti parallel diodes attached to each of them. It functions in all the four quadrants. For explanation consider the first leg connected to phase A. When the voltage and current are positive the switch S1 conducts and the current flows to the DC link at the output. When the current is positive but the voltage is negative i.e because of the PWM action where the reference is compared with carrier wave, lower diode D2 conducts, as the current cannot change direction immediately on account of the inductor present at the input. Similarly, when the current is negative and the voltage is positive, the upper diode D1 conducts, maintaining the flow of the current. When both voltage and current are negative, the lower switch S2 conducts. It should be noted that both the upper and lower switches have complementary switching states.

It can be seen that the voltage stress on the semiconductor switch and diode in blocking state is equal to the DC link voltage. The voltage that appears across the switches is from Vdc/2 to -Vdc/2, thereby giving a two level waveform of phase voltage at the converter side.

The simplicity and ruggedness of this topology has played important role as to its widespread usage for different applications. It has some drawbacks such as over-voltages when connected to cables, inferior harmonics spectrum and problem with higher common mode voltages as comapred to a multilevel topology [12]

2.2 Operation of the VIENNA rectifier

There are different ways of constructing a three level PWM rectifier according to the literature review[1][2][4][6][7]. The difference can be seen in the switch configuration which basically has a bidirectional nature, but facilitating the same operation required for rectification. Hence, the analysis presented for the conventional three switch rectifier holds true irrespective of topology used. Figure 2.2 (a) shows the structure of the Vienna rectifier having three switches (b) Structure that makes use of six switch.

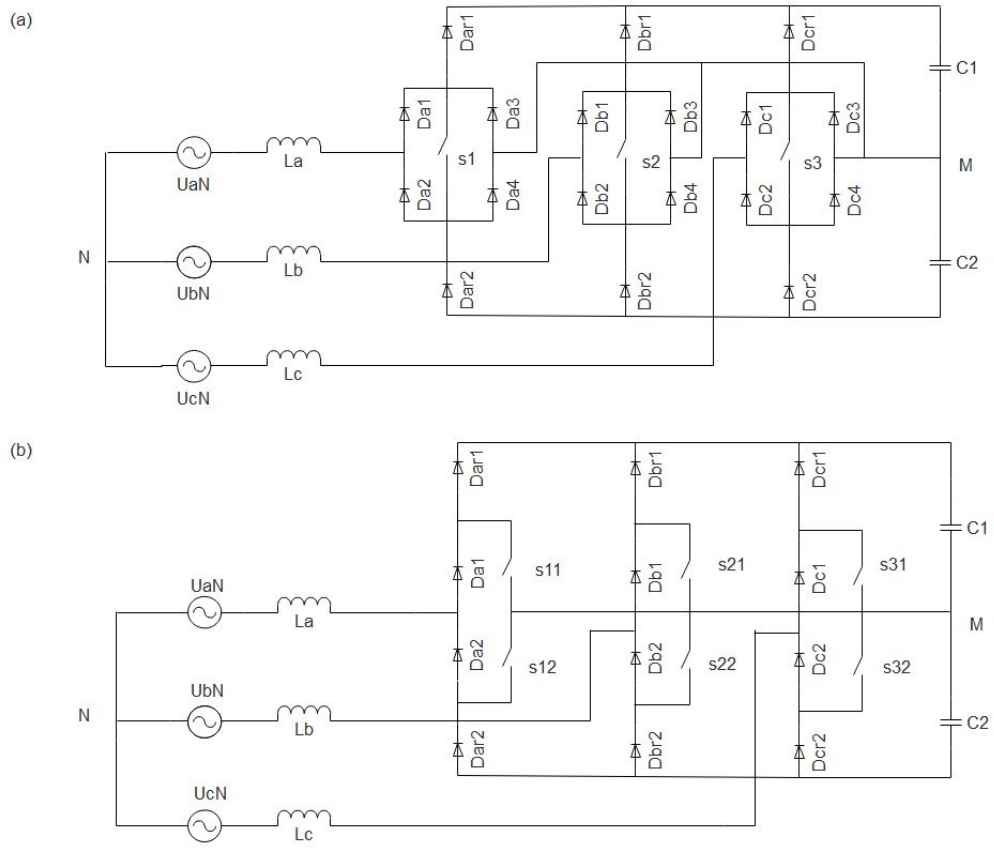

Figure 2.2: Vienna topology (a) Conventional three Switch (b) Six Switch

The diodes $D_{a_r}(1,2)$ should be fast recovery diodes operating at switching frequency. the maximum voltage stress across them is $U_{d_c}/2$. The diodes $D_a(1,2)$ operates at mains frequency and the voltage across them and the Switch S1, S11 as well as S12 is $U_{d_c}/2$. Despite the high frequency operation of the switching diodes $D_{a_r}(1,2)$ the active switch is always blocking the voltage. When Switch S1 is in on state, diodes D_a1 and D_a4 conducts for the positive half cycle, likewise D_a3 and D_a2 conducts during the negative half cycle. This leads to a higher conduction losses as compared to the second topology shown in figure 2.1(b) wherein the absence of the diodes on the right hand side of the switch results in lower conduction and switching losses, thereby increasing the efficiency. On this account the second topology is preferred.

Vienna rectifier obtains three level phase input characteristics with one active switch defined by the switching function $SW_{(a,b,c)} = (1,0)$ where 1 and 0 indicates switch in ON and OFF state respectively. This combination would be used to denote the switching instances on phase specific basis. e.g. $SW = SW_a$, SW_b, SW_c wherein $SW_a = 0$, $SW_b = 0$, $SW_c = 1$, gives SW = (0 0 1). For analysis purpose, it is assumed that the three phase system is balanced with no neutral point connected.

When phase currents $ir_{(a,b,c)}$ are positive and the switches are in OFF state, the diodes $D_{(a,b,c)1}$ and $D_{(ar,br,cr)1}$ connect the input to the positive bus of the DC link. Similarly, when the input current is negative the diodes $D_{(a,b,c)2}$ and $D_{(ar,br,cr)2}$ connects them to the negative bus of the DC link. When switches $S_{(1,2,3)}$ are on, diodes $D_a(1,4)$ $D_b(1,4)$ and $D_c(1,4)$ conduct thereby connecting the phase input to the DC link neutral point M. Likewise, when the current is negative and switches are in ON state, $D_a(2,3)$ $D_b(2,3)$ and $D_c(2,3)$ conduct. This shows that the operation is dependent on the state of switch as well as the direction of the phase input current.

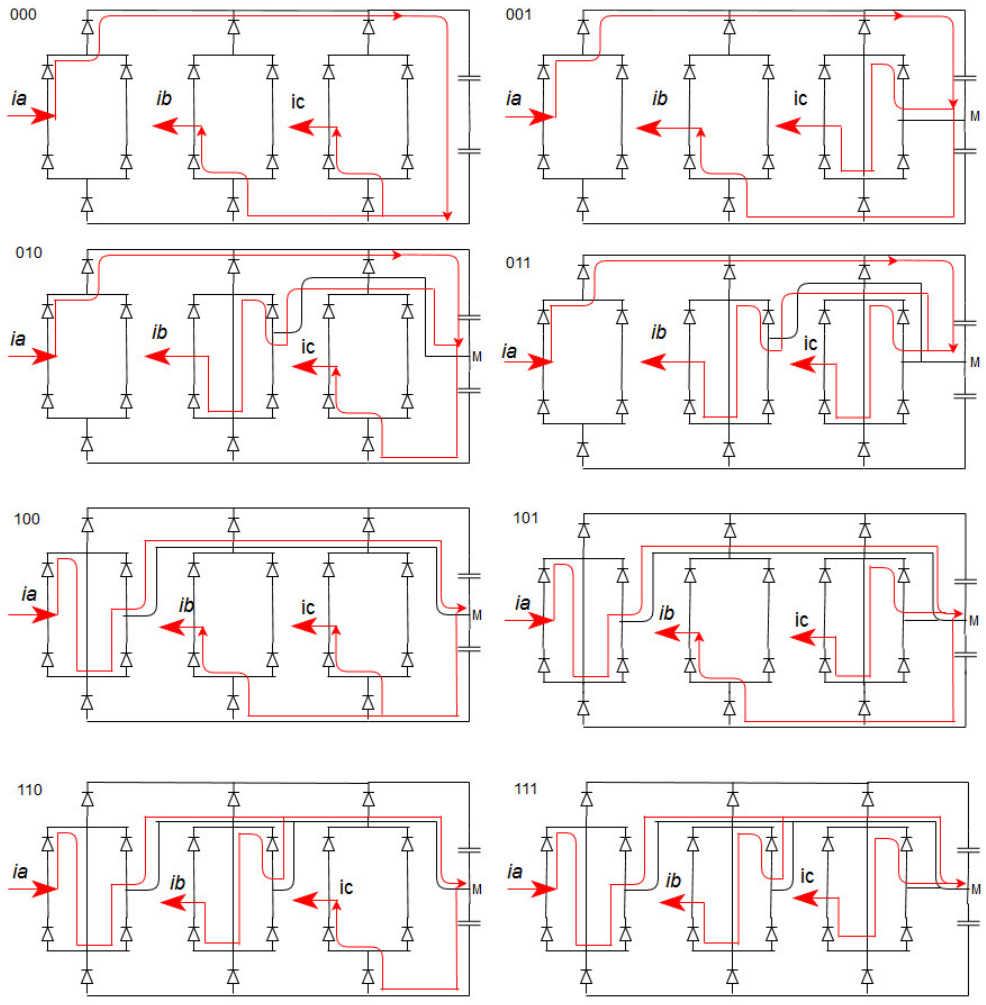

Figure 2.3: Rectifier input current $i_a > 0$, $i_b < 0$, $i_c < 0$. the arrow mark shows the direction of input phase and neutral point current

An example of current paths for a particular case of current directions $i_{ra} > 0, i_{rb} < 0, i_{rc} < 0$ is shown in fig(2.2).This case gives a total of $2^3 = 8$ switching combinations[1].

(1 1 1) and (0 0 0) are two combinations that do not induce a neutral current at point M. There exists only one zero state given by (1 1 1) as compared to the two level SVM, where the zero states are given by both (0 0 0) and (1 1 1) as given in [1]. The neutral point current is given as

$$i_M = sw_a.i_{ra} + sw_b.i_{rb} + sw_c.i_{rc} \tag{2.1}$$

$$i_{C1} = I_+ - i_{load} \tag{2.2}$$

$$i_{C2} = i_{C1} + i_M \tag{2.3}$$

It can be observed that the magnitude of i_M is always equal to one of the phase currents [1].

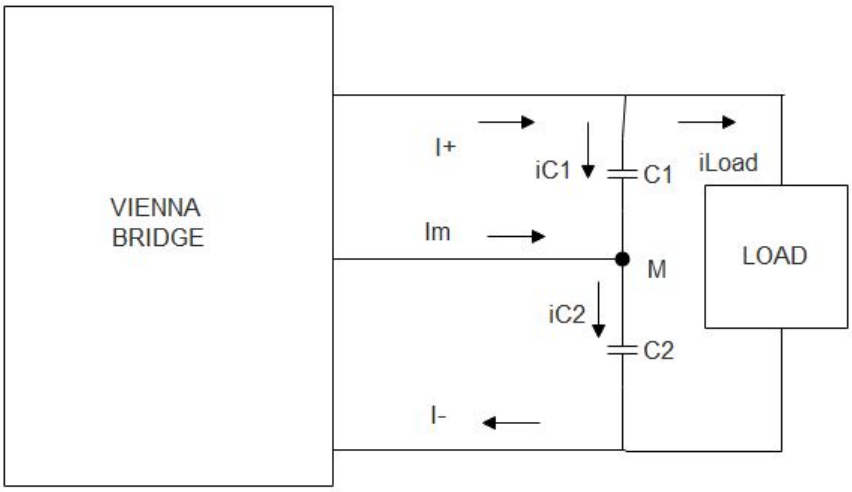

Figure 2.4: Midpoint neutral current along with the direction of positive and negative current

2.3 Modulation techniques for PWM converters

There exists various modulation schemes for obtaining a sinusoidal switching pattern as described in [1][2][6]. A brief explanation about the commonly used modulation techniques is given in this sub-chapter. However the loss calculation in the upcoming chapter is analyzed based on third harmonic injection technique (THI).

2.3.1 Sinusoidal PWM

Sinusoidal PWM (SPWM) is a basic method of modulation in which the gate pulses are generated by comparing the reference signal having fundamental frequency $\omega_0 = 2\pi f_0$ with a fixed triangle wave having $\omega_C = 2\pi f_C$ as carrier frequency [6]. The three phase reference voltages and currents as shown in Figure 2.4 are given

as

$$v_A^* = V_0 sin(\omega t) \tag{2.4}$$

$$v_B^* = V_0 sin(\omega t - \frac{2\pi}{3}) \tag{2.5}$$

$$v_C^* = V_0 sin(\omega t - \frac{4\pi}{3}) \tag{2.6}$$

$$i_A^* = I_0 sin(\omega t) \tag{2.7}$$

$$i_B^* = I_0 sin(\omega t - \frac{2\pi}{3}) \tag{2.8}$$

$$i_C^* = I_0 sin(\omega t - \frac{4\pi}{3}) \tag{2.9}$$

For a two level three phase voltage source converter (VSC) there are two switches present in each phase arm. When $V_{A,B,C}^* > V_{Carrier}$ the switch is set in ON state, which logically is 1, and when $V_{A,B,C}^* < V_{Carrier}$ the switch is set in OFF state defined as 0. The gate state of the upper and lower switches in each arm is complementary. i.e if the upper switch is 1, the lower would be 0. The modulation index is a ratio of peak phase voltage to peak carrier triangle wave. It can also be expressed in terms of the DC output voltage and phase voltage as $M = \frac{2V_{peak}}{V_{DC}}$, where V_{peak} is the peak value of the phase voltage.

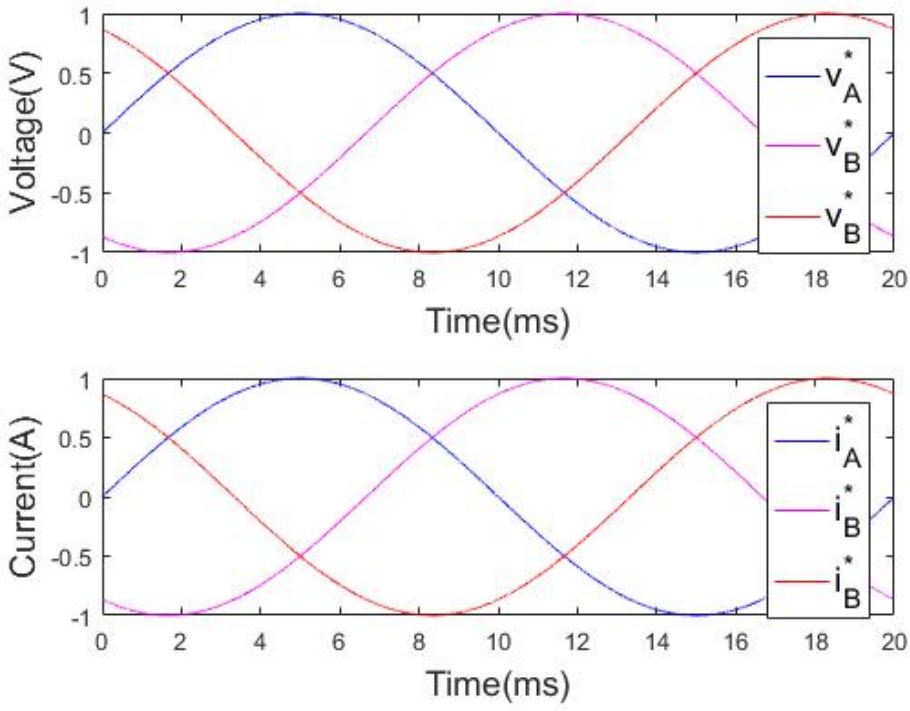

Figure 2.5: Three phase reference voltages and currents

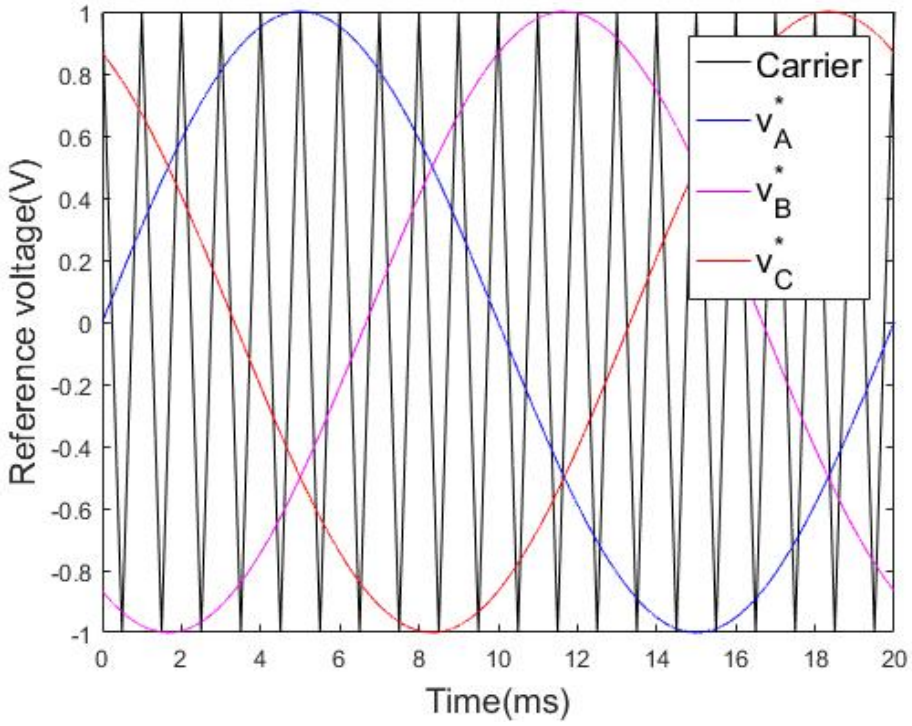

Figure 2.6: Reference voltages with triangle wave for SPWM for M=1

The wave-forms in Fig(2.5) shows the reference voltages along with a carrier wave, having modulation index M as one. The range of M for SPWM is from zero to one, where values lesser than one is known as under-modulation and values exceeding one is called over-modulation. It must be emphasized that the value of modulation index is important as in under-modulation the output voltage would be reduced below the required level needed. On the other hand over modulation may cease the switching and the corresponding switches remain in ON state within this carrier time period, resulting in the saturation of the reference voltages. This saturation leads to reduction in the voltage gain, as the average reference voltage per carrier cycle cannot be matched with the converter[7].

2.3.2 PWM with third harmonic injection (THI)

The main disadvantage of SPWM is that the DC bus utilization is not optimal as compared to other modulation techniques available such as space vector modulation (SVPWM). The modulation index could be further increased to 1.15 from 1 by injecting a third harmonic sequence[2][7]. There are different available techniques such as Min/Max, where the mean of maximum and minimum values of the voltages is subtracted from the corresponding waveform, thereby improving the voltage utilization of the DC side. The other way is by adding third harmonic signal ($3\omega_0$) having one-sixth of the fundamental magnitude, thereby increasing the modulation index to 1.15.

$$v^*_{A,B,C} = V_0 sin(\omega t \pm \phi) + \frac{V_0}{6} sin(3\omega t) \tag{2.10}$$

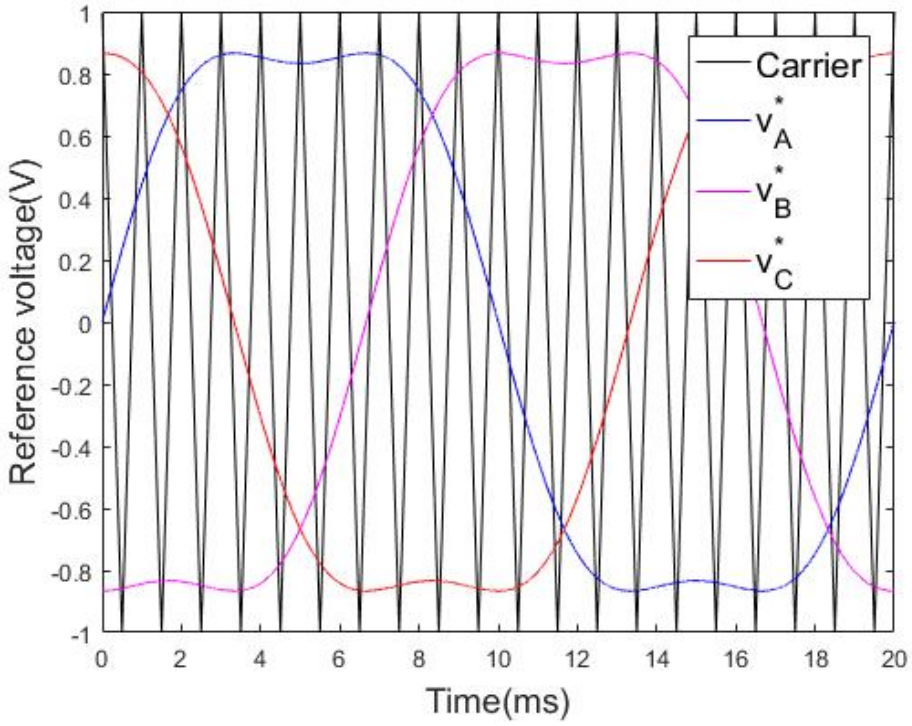

Figure 2.7: Reference voltages with third harmonic injection for M=1

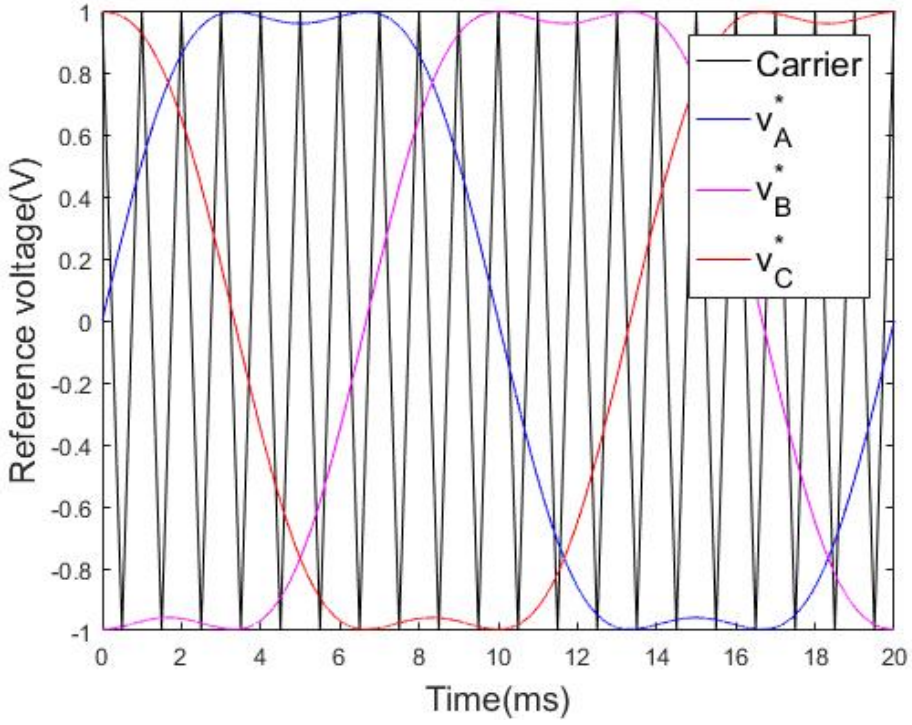

Figure 2.8: Reference voltages with third harmonic injection for M=1.15

As shown in Fig(2.6) after addition of the third harmonic sequence, the reference voltages do not reach the peak of the carrier wave for modulation value of 1. By increasing M to 1.15 it can be seen from Fig(2.7) that the reference voltages reaches the peak of the carrier, thereby maximizing the DC link utilization.

2.4 Loss calculation and component selection

Power loss calculation of switching devices in converters is important as it predicts the system efficiency and provides a reference for thermal management[8]. Two main type of losses are the conduction and switching losses, which would be analyzed for IGBT and diodes. Leakage losses are not considered here for the sake of brevity.

2.4.1 IGBT power losses

The IGBT conduction and switching losses are determined from the data sheet of the device manufacturer the method described in the following section is used for the respective loss analysis.

2.4.1.1 Conduction power losses

Equivalent circuit of an IGBT during on state comprises of two elements connected in series, a temperature dependent resistor and a DC voltage source as depicted in the Fig(2.8)

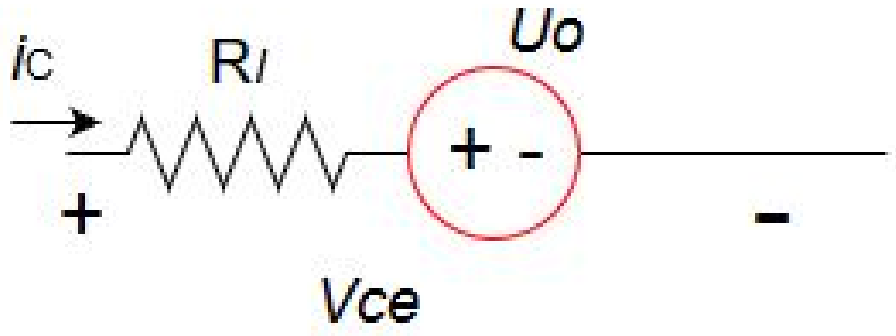

Figure 2.9: Equivalent circuit of an IGBT in on state

(U_0) and (R_I) are the zero current voltage depicted as (V_{CEO}) and the on state resistance respectively at a given temperature that can be obtained from the voltage characteristics of the IGBT [8]. The instantaneous conduction losses can thus be given as

$$P_C(t) = U_O i_C(t) + R_I i_C^2(t) \tag{2.11}$$

Integrating the above equation over one switching time period Tsw gives the average conduction loss.

$$P_C, avg = \frac{1}{Tsw} \int_0^{Tsw} (U_0 i_c(t) + R_I i_c^2(t)) dt. \tag{2.12}$$

$$P_C, avg = I_{rms}^2 . R_I + U_0 . I_{avg} \tag{2.13}$$

The conduction losses in a PWM converter depends on power factor (ϕ) as well as modulation index M. The conduction loss for a single IGBT using PWM (THI) is explained in[10][11] and can be expressed as

$$P_{C,THI} = U_0 . I_{peak} (\frac{1}{2\pi} + \frac{\pi}{8} . M . cos\phi) + R_I . I_{peak}^2 (\frac{1}{8} + \frac{M}{3\pi} . cos\phi - \frac{M_3}{15} . cos3\phi) \tag{2.14}$$

where M_3 is the amplitude of third harmonic and is selected as 1/6 for improving DC link utilization[10][11].

2.4.1.2 Switching power losses

The switching energy losses E_{on} and E_{off} can be determined from the plots given in the data sheets by the manufacturer. These parameters are proportional to the current i_C and off state voltage U_{dc} across the IGBT [8][9]. The instantaneous value of the Energy losses are given as

$$E_{on} = \frac{U_{dc}}{U_{ref}} . \frac{i_c}{I_{ref}} . E_{on,ref} \tag{2.15}$$

$$E_{off} = \frac{U_{dc}}{U_{ref}} . \frac{i_c}{I_{ref}} . E_{off,ref} \tag{2.16}$$

The average value can be determined by integrating (2.15) and (2.16) over one time period as

$$E_{on,avg} = \frac{1}{2\pi} \int_0^{\pi} \frac{U_{dc}}{U_{ref}} . \frac{i_c}{I_{ref}} . E_{on,ref} . d\omega t \tag{2.17}$$

$$E_{on} = \frac{\sqrt{2}}{\pi} . \frac{U_{dc}}{U_{ref}} . \frac{I_{rms}}{I_{ref}} . E_{on,ref} \tag{2.18}$$

$$E_{off,avg} = \frac{1}{2\pi} \int_0^{\pi} \frac{U_{dc}}{U_{ref}} . \frac{i_c}{I_{ref}} . E_{off,ref} . d\omega t \tag{2.19}$$

$$E_{off} = \frac{\sqrt{2}}{\pi} . \frac{U_{dc}}{U_{ref}} . \frac{I_{rms}}{I_{ref}} . E_{off,ref} \tag{2.20}$$

The total switching losses can be given as

$$P_{sw} = (E_{on} + E_{off}) . f_{sw} \tag{2.21}$$

2.4.2 Diode power losses

2.4.2.1 Conduction power losses

The conduction loss calculation of a diode is similar to that of an IGBT, as shown in Fig(2.9) and is given as

$$P_C, avg = I_{rms}^2.R_D + U_0.I_{avg} \tag{2.22}$$

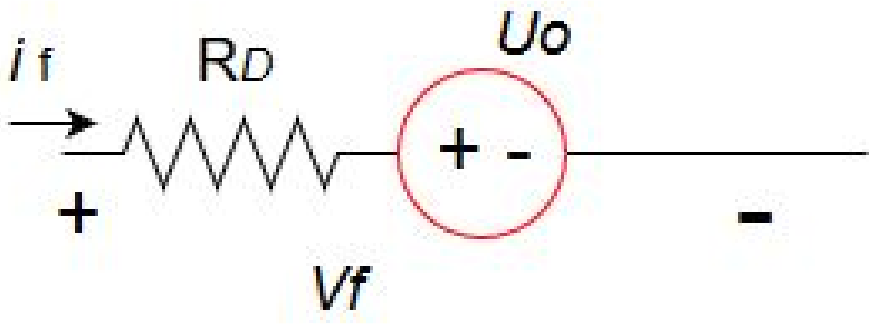

Figure 2.10: Equivalent circuit of a diode in on state

Similar to the IGBT conduction losses with third harmonic injection, the loss is given as [10][11]

$$P_{C,THI} = V_f.I_{peak}(\frac{1}{2\pi} - \frac{\pi}{8}.M.cos\phi) + R_D.I_{peak}^2(\frac{1}{8} - \frac{M}{3\pi}.cos\phi + \frac{M_3}{15}.cos3\phi) \tag{2.23}$$

2.4.2.2 Switching power losses

The switching losses in a diode is mainly caused by the reverse recovery charge during the turning off, as the turn on loss is negligible [9]. E_{rr} is determined from the datasheet and the procedure is same as that of E_{off} and E_{on}.

$$E_{rr} = \frac{U_{dc}}{U_{ref}}.\frac{i_f}{I_{ref}}.E_{rr,ref} \tag{2.24}$$

$$E_{rr,avg} = \frac{1}{2\pi}\int_0^\pi \frac{U_{dc}}{U_{ref}}.\frac{i_f}{I_{ref}}.E_{rr,ref}.d\omega t \tag{2.25}$$

$$E_{rr} = \frac{\sqrt{2}}{\pi}.\frac{U_{dc}}{U_{ref}}.\frac{I_{rms}}{I_{ref}}.E_{rr,ref} \tag{2.26}$$

Many of the data sheets contains the reverse recovery charge and the current, an empirical equation according to [9] is used to calculate the switching energy.

$$E_{rr} = \frac{1}{4}.Q_{rr}.U_{dc} \tag{2.27}$$

3

Case-Setup

The parameters for simulation and analytical calculation are given for a particular case as mentioned.

$Power_{input} = 25kW$
$Voltage_{input,LL} = 400V$
$Voltage_{DC} = 700V$
$Frequency_{supply} = 50Hz$
$Frequency_{sw} = 20kHz$

For the sake of analysis it is assumed that the phase angle ϕ between supply voltage and current is zero i.e no inductor is connected at the converter side and also, no capacitor was taken into account at the output side either. The modulation technique employed here is PWM with third harmonic injection (THI).

3.1 Loss calculation for a two level converter

Considering the input voltage of 400 V, and the power rating of 25kW, the current is calculated for component selection from (3.1)(3.2)(3.3)

$$P_{ac} = 3.U_{rms,ph}.I_{rms}.cos\phi \tag{3.1}$$

$$M = \frac{2.U_{ph,peak}}{U_{dc}} \tag{3.2}$$

$$I_{rms} = 29.3A \tag{3.3}$$

For component selection the peak value has to be considered which gives I_{peak} equals to 41.5 A. Calculation is done for M= 1.15. The IGBT and diodes would be subjected to a peak stress of 700V DC with 41.5 A current.

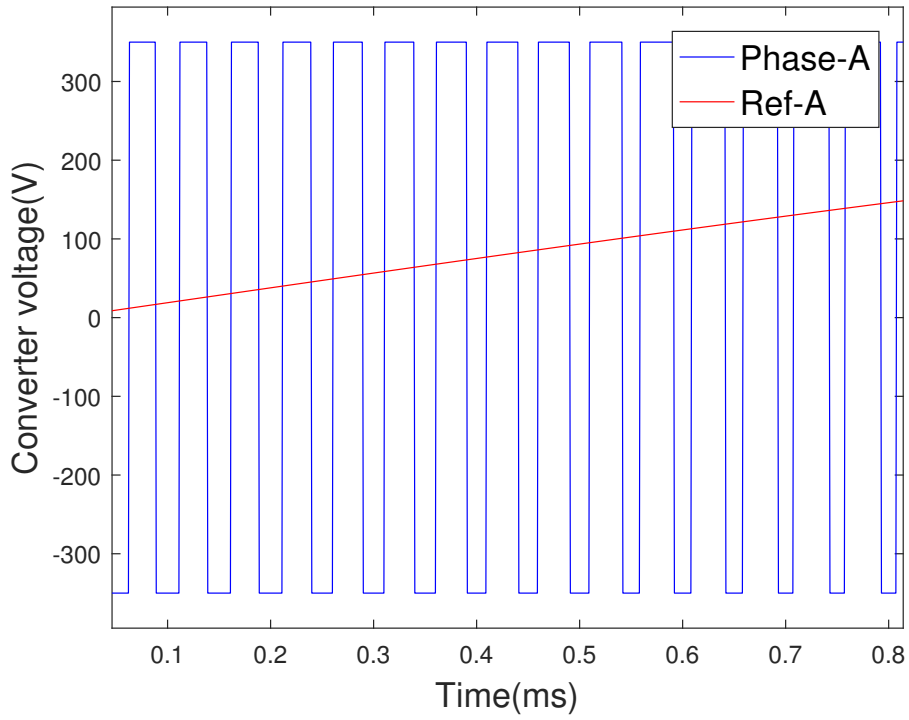

Figure 3.1: Two level phase voltage waveform

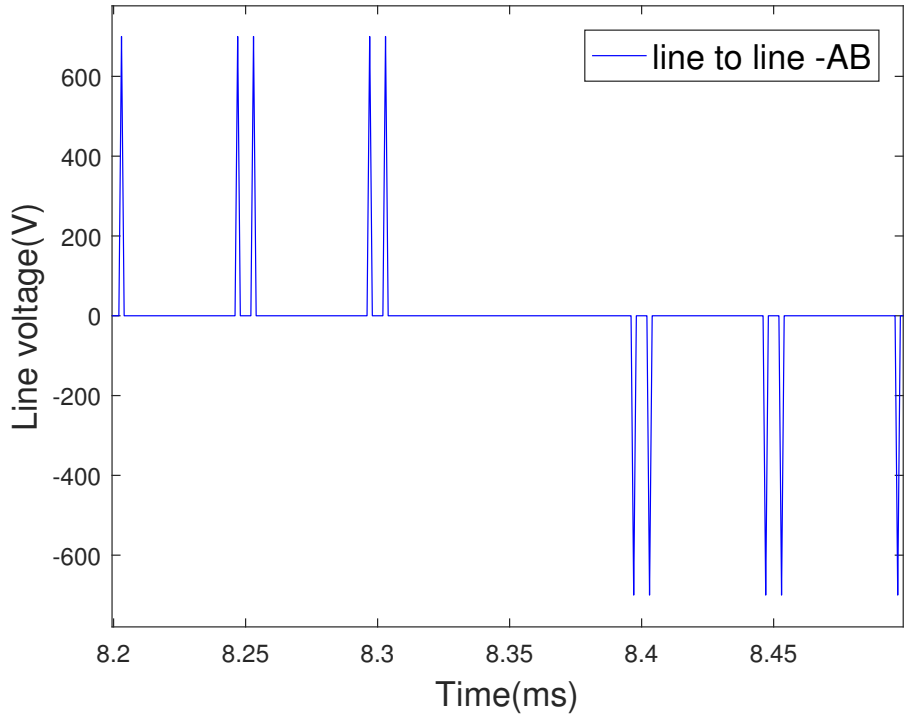

Figure 3.2: Three level line to line voltage waveform

3.1.1 Current waveform

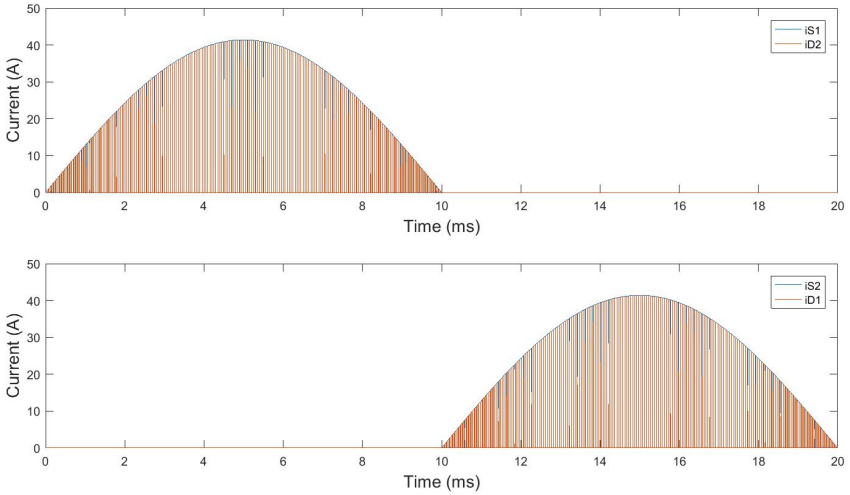

Figure 3.3: Two level diode and switch current waveform

As shown in Fig.(3.3) the chopped current waveform of the 2L-converter. The case setup is run for one fundamental cycle of 50Hz. The average and RMS values of the IGBT current are 12.46A and 20.33A respectively. Whereas for diode average and RMS values are 0.71A and 3.86A respectively.

3.1.2 On state loss calculation

Based on the requirement a 1200 V, 50 A infineon make IKY50N120CH3 IGBT with anti-parallel diode is selected.

For IGBT,the on state voltage drop V_{CEO} and the on-state resistance r_C are taken for reference value's of 50 A at 175°C. This gives V_{CEO}=0.8V and r_C=0.03 Ω from the slope of the datasheet.

For diode, the forward voltage drop and the onstate resistance are found to be 1.2V and 15mΩ respectively, as can be calculated from the datasheet.

3.1.3 Switching loss calculation

The parameters needed for calculating the switching losses for an IGBT are the on and off energies calculated for the base case as taken in the conduction loss calculation. From the data sheet the values for E_{on} and E_{on} are found out to be 4.3 mJ and 4 mJ respectively. The diode reverse recovery charge Q_{rr} is calculated for the DC voltage of 700 V, and is 8.8 µC. From this, the reverse recovery energy could be calculated using equation (2.27) and is found to be 1.54 mJ.

3.2 Loss calculation for three level Vienna converter

As explained in the theory chapter, the peak voltage stress experienced by the IGBT and diodes in half leg of the phase is half of the DC link voltage. So, for this case the voltage stress experienced by the devices would be 350 VDC which is half of the DC link voltage for the test setup. The peak current remains same at 41.5 A current. Based on the requirement 600 V infineon make IGBT IKW50N60H3 with anti parallel diode is selected. For the sake of brevity, the same kind of diode is used at the grid side as well as for the high switching connected to the DC link. A 600 V 50 A, Infineon make IDW50E60 diode is selected [15]
Fig(3.3) and (3.4) shows the phase voltage and line voltage at the converter side respectively. The three level characteristics could be seen for phase voltage where for this particular setup, the levels obtained are +350,0,-350. The line to line voltage shows a five level characteristic

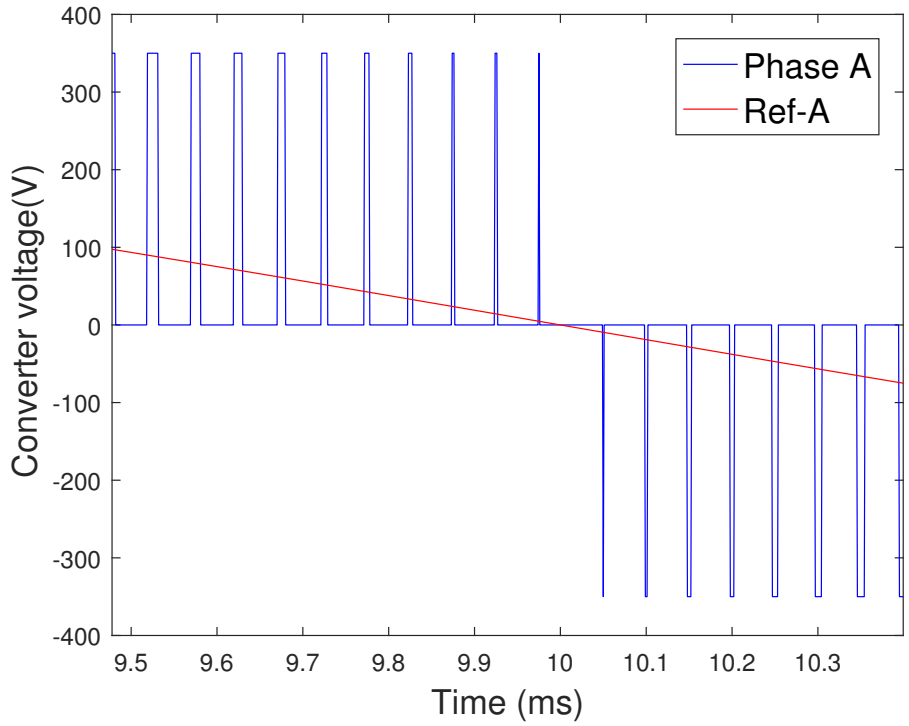

Figure 3.4: Three level phase voltage waveform

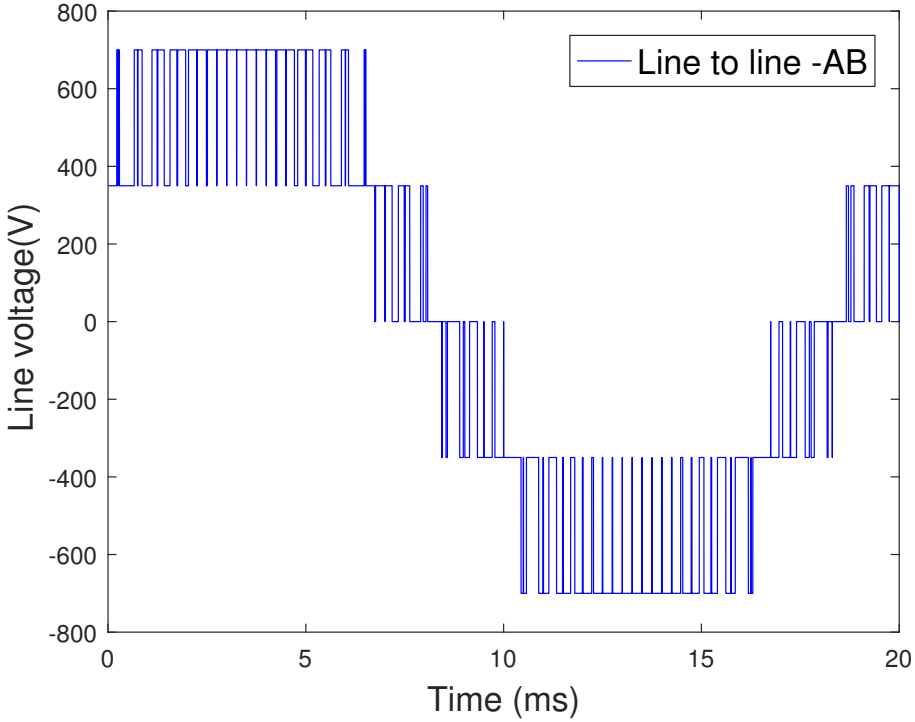

Figure 3.5: Three level line to line voltage waveform

3.2.1 Current waveform

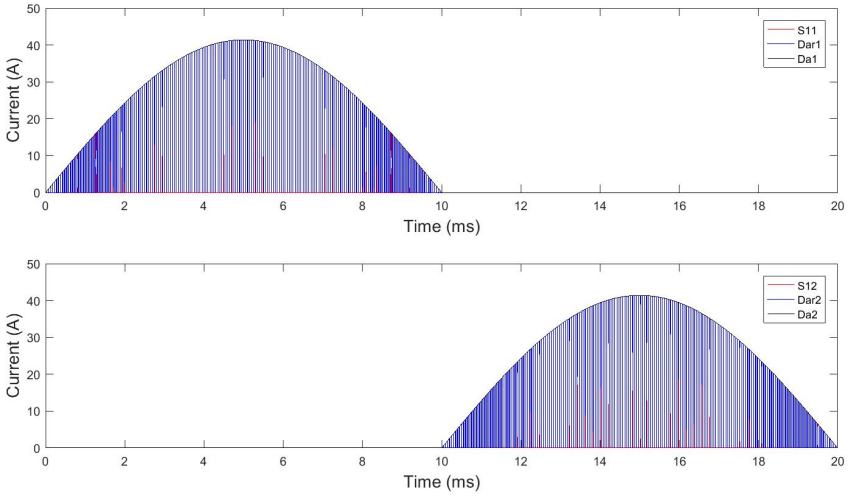

Figure 3.6: Diode and switch current waveform for Vienna rectifier

Fig.(3.6) shows the current waveform of the 3L-Vienna rectifier for one fundamental cycle of 50Hz. The average and RMS values of the IGBT current are 1.29A and 4.99A respectively. Whereas for diode D_{ar1}average and RMS values are 11.88A and

20.09A, whereas for D_{a1}, the average and RMS are 13.18A and 20.7A respectively. The values are based on simulation. The analytical values obtained from [3][4] are found to have a good match except the RMS value for the IGBT, which is 3.19A as compared to 4.99A by simulation [A.0.1]

3.2.2 On state loss calculation

As explained in the case of a two level converter, the two parameters needed for on state loss calculation are taken from the data-sheet given in the appendix. Zero current on state voltage drop and the on-state resistance are chosen for reference value's of 50 A at 175°C which are 0.9V and 20mΩ respectively for IGBT. For diode, the forward voltage drop and the on-state resistance are found to be 0.45V and 10mΩ respectively, as can be calculated from the data-sheet given in reference[13]

3.2.3 Switching loss calculation

The values of E_{ON}, E_{OFF} and Q_{rr} found for the reference values of 400 V and 50 A, are 1.42mJ , 1.13mJ and 8.8 µC respectively. This gives E_{rr} to be 0.358 mJ. The datasheet is as given in reference[14]

4

Result and Future work

4.1 Plots

In this chapter the loss calculation for both the converters are presented and analyzed for the base case. The results and figures plotted are based on one leg/per phase due to the symmetrical nature of operation of the other legs.

4.1.1 Loss Analysis of a two level converter

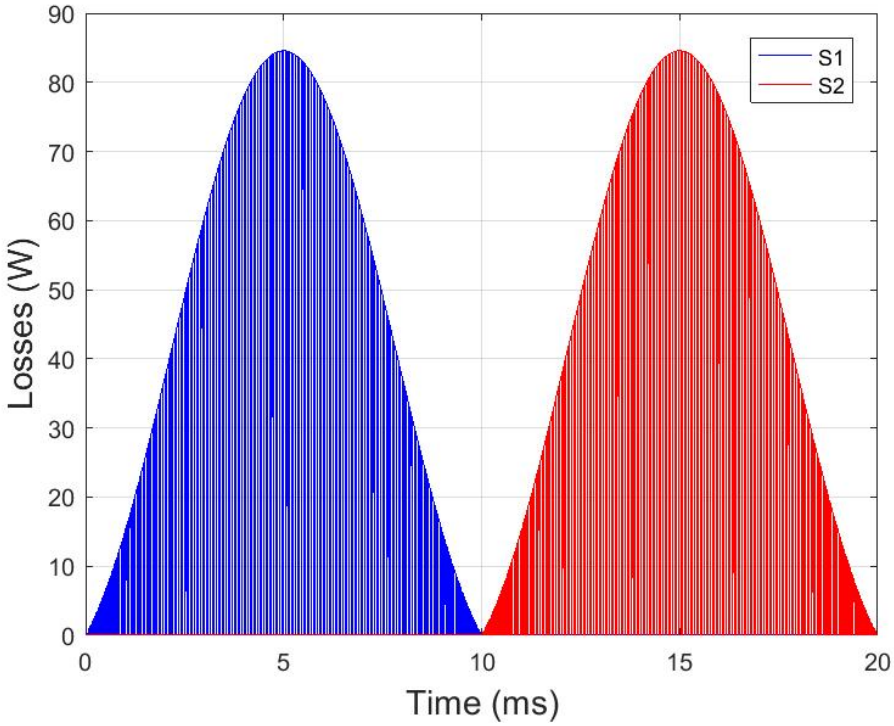

Figure 4.1: Instantaneous conduction losses of IGBT

Simulation was done keeping the value of modulation index M_a at 1.15, so as to optimally utilize the DC link voltage. The instantaneous values of the conduction losses per phase for the upper and lower IGBT's, has been depicted in Fig 5.1, the nomenclature followed for the components is as shown in Fig.2.1. It can be seen that the peak value for the IGBT loss is 84.5W.

Table 4.1: On state loss calculation using matlab model at 20kHz

On state losses in Watts				Net loss (Watts)
S1	S2	D1	D2	First leg
22.3	22.3	1.08	1.08	46.76
S3	S4	D3	D4	Second leg
22.3	22.3	1.08	1.08	46.76
S5	S6	D5	D6	Third leg
22.3	22.3	1.08	1.08	46.76
Net conduction losses				140.28 W

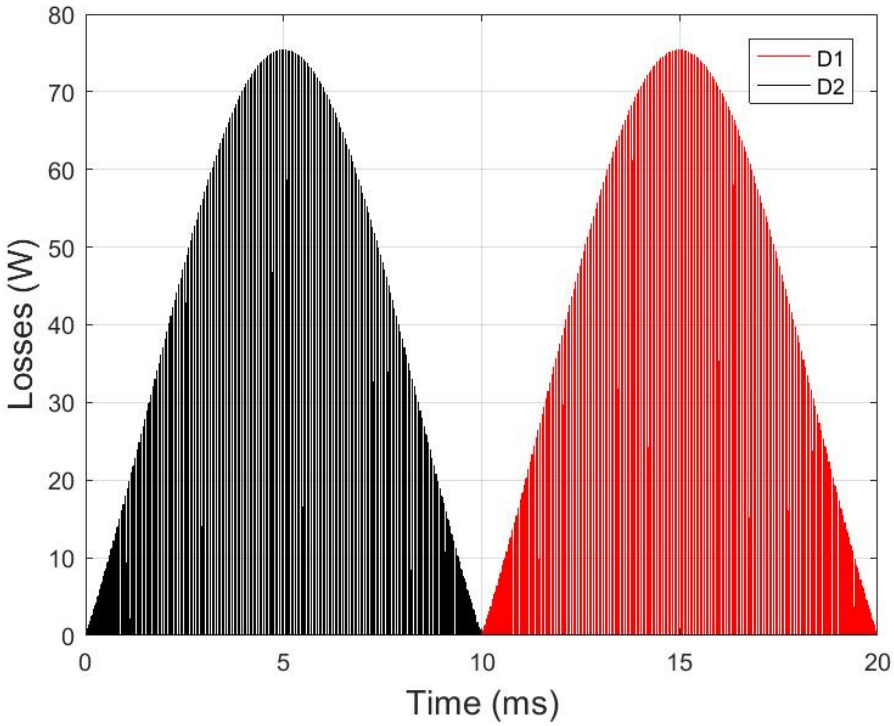

Figure 4.2: Instantaneous conduction losses of diodes

The component wise values of the conduction loss taken over once fundamental cycle i.e average, is given in Table 5.1. Using (2.14) the conduction loss calculated analytically is given by
$P_{C,T} = V_{CEO}.I_{peak}(\frac{1}{2\pi} + \frac{\pi}{8}.M.cos\phi) + R_I.I^2_{peak}(\frac{1}{8} + \frac{M}{3\pi}.cos\phi - \frac{1}{90}cos3\phi) = 22.2W$
The on state loss obtained using Matlab model in table 5.1 gives $P_{C,THI} = 22.3$ W.

The analytical onstate loss for a diode is calculated using (2.23) to be
$P_{C,D} = V_F.I_{peak}(\frac{1}{2\pi} - \frac{\pi}{8}.M.cos\phi) + R_I.I^2_{peak}(\frac{1}{8} - \frac{M}{3\pi}.cos\phi + \frac{1}{90}cos3\phi) = 1.1$W
The on state loss obtained using Matlab model gives $P_{C,D} = 1.08$W.
This shows a very good match between the analytical as well as simulated loss behaviour.

Table 4.2: Switching loss calculation using matlab model at 20kHz

Component wise switching losses breakdown				Losses (Watts)
S1	S2	D1	D2	First leg
53.8	53.8	8.9	8.9	125.4
S3	S4	D3	D4	Second leg
53.8	53.8	8.9	8.9	125.4
S5	S6	D5	D6	Third leg
53.8	53.8	8.9	8.9	125.4
Net switching losses				376.2 W

The average value of the switching losses over one fundamental cycle using the matlab model of the converter is given in the Table 5.2. For analytical calculation equations (2.18) and (2.20) are modified, wherein the coefficient's Ki=1 and Kv=1.35 are used in the equation for IGBT
$P_{sw,S} = f_{sw}(E_{on} + E_{off}).\frac{\sqrt{2}}{\pi}.(\frac{I_{rms}}{I_{ref}})^{ki}.(\frac{U_{dc}}{U_{ref}})^{kv} = 53.88\text{W}$
Similarly, for determining the switching losses of a diode the following equation is used, having Kid=1 and Kvd=0.6
$P_{sw,D} = f_{sw}(E_{RR}).\frac{\sqrt{2}}{\pi}.(\frac{I_{rms}}{I_{ref}})^{kid}.(\frac{U_{dc}}{U_{ref}})^{kvd} = 8.9\text{W}$

4.1.2 Loss Analysis of the Vienna rectifier

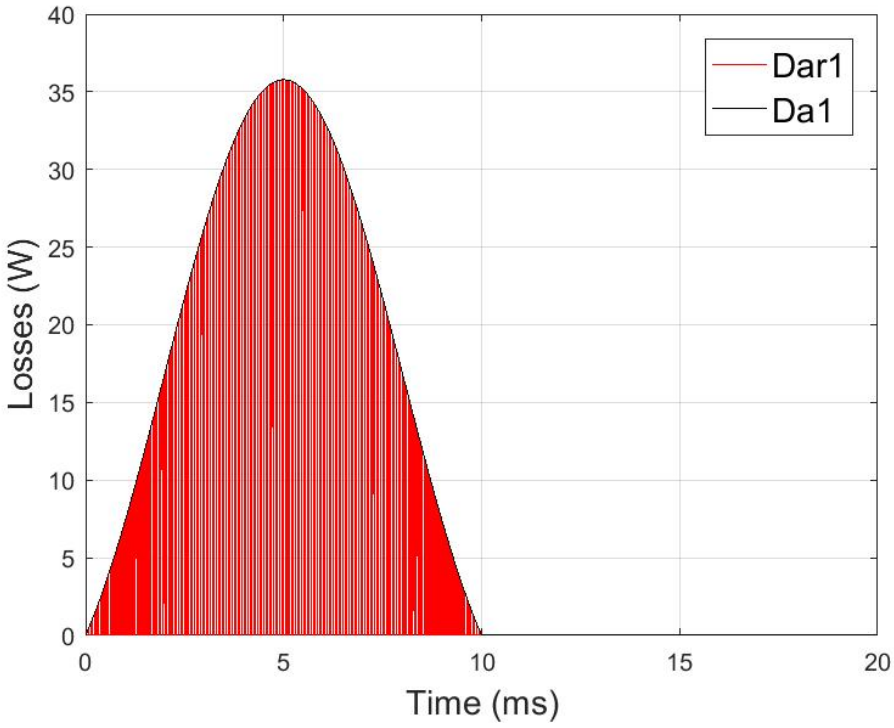

Figure 4.3: Instantaneous conduction losses of diodes

The instantaneous diode conduction losses depicted in Fig.4.3 comprises of the high frequency switching diode D_{ar1}, having a discretized waveform as well as the continuous conduction of D_{a1} at half of the fundamental cycle.The peak value of the diode conduction loss is 35.8W. However, loss pattern of D_{ar1} is chopped and the average value of the losses are given in the tabulated form. Fig. 4.4 shows the instantaneous conduction loss of IGBT S_{11} and S_{12}. It should be noted that the relative on time period of the switches is quite small in-spite of the peak onstate loss value being at 75W. This brings down the average value of the losses across the switches over a fundamental period.

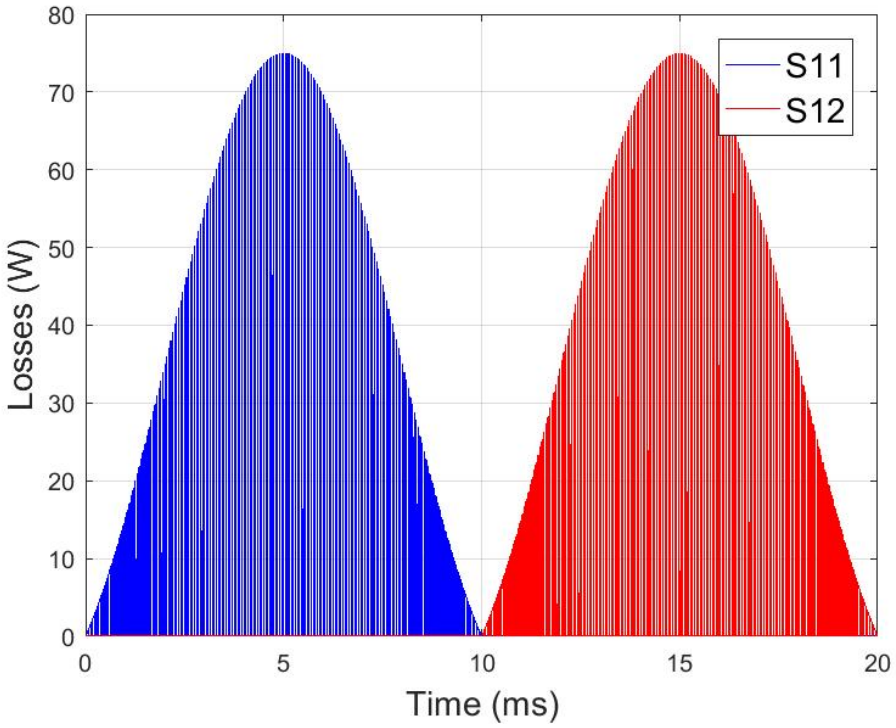

Figure 4.4: Instantaneous conduction losses of IGBT

For the matlab model the instantaneous losses are averaged over the fundamental cycle, the tabulation of which is given in Table 4.3. Analytically the conduction losses are determined using the average and root mean square values of the currents flowing through the components as calculated in the case-setup. The average value of the conduction losses for components found using (2.13) and (2.22) are

$P_S = 1.54\text{W}$
$P_{Dar} = 9.56\text{W}$
$P_{Da} = 10.23\text{W}$

On comparing the IGBT conduction loss calculated analytcially with the matlab model, it can be seen that there is a difference in the values. This is because of the difference in the RMS current of the IGBT, which is 4.19A found via the equation, whereas from the simulation the value turns out to be 4.99A.

Table 4.3: On-state loss calculation for Vienna rectifier

Component wise on state loss breakdown						Losses (Watts)
S11	S12	Dar1	Dar2	Da1	Da2	First leg
1.71	1.72	9.38	9.38	10.21	10.21	42.62
S21	S22	Dbr1	Dbr2	Db1	Db2	Second leg
1.72	1.72	9.37	9.37	10.21	10.21	42.62
S31	S32	Dcr1	Dcr2	Dc1	Dc2	Third leg
1.72	1.72	9.37	9.37	10.21	10.21	42.62
Net on state losses in Watts						127.86

Table 4.4: Switching loss calculation for Vienna rectifier

Component wise switching loss breakdown						Losses (Watts)
S11	S12	Dar1	Dar2	Da1	Da2	First leg
11.22	11.22	1.74	1.74	0	0	25.93
S21	S22	Dbr1	Dbr2	Db1	Db2	Second leg
11.22	11.22	1.74	1.74	0	0	25.93
S31	S32	Dcr1	Dcr2	Dc1	Dc2	Third leg
11.22	11.22	1.74	1.74	0	0	25.93
Net switching losses in Watts						77.80 W

Considering the difference in between the RMS value of the simulated current in the set-up and the analytical one, it is appropriate to use the later value of 4.99A. Using (2.18)(2.20) and (2.27) the switching losses are found. On account of the non-linear characteristics in the datasheet, Ki=1 and Kv=1.35 are included in the equation, as also considered in the case of two level rectifier. The results obtained thus are given as

$P_{sw|IGBT}$ = 11.22W
$P_{sw|Dar}$ = 1.74W
$P_{sw|Da}$ = 0W

It can be observed as explained in theory chapter, that the diode $D_{a(1,2)}$ does not have any switching losses as they operate at fundamental half cycle at instants where the voltage and current are zero. As shown in Table 4.4 the switching losses simulated via matlab model has good consistency with the results obtained analytically. In this case as the equations involved needed the peak value of the supply current i.e I_{peak}=41.4A, no difference in the two results was observed.

4.1.3 Conclusion

For determining the semiconductor efficiency, both type of losses are tabulated for the sake of ease and comparison as given in Table (4.5) and (4.6).

For the two level converter it is seen that the switching loss of the IGBT is dominant, whereas the diode conduction losses is negligible. Considering only the semiconduc-

Table 4.5: Total loss for two level converter

Two level Rectifier	Losses
IGBT Conduction loss	133.8
Diode Conduction loss	6.48
IGBT Switching loss	322.8
Diode Switching loss	53.4
Net loss (Watts)	516.48

Table 4.6: Total loss for Vienna rectifier

Vienna rectifier	Losses
IGBT Conduction loss	10.32
Diode Conduction loss	117.54
IGBT Switching loss	67.32
Diode Switching loss	10.44
Net loss (Watts)	205.6

tor losses, the efficiency at the rated power of 25kW is 97.93 %. On the contrary, in Vienna rectifier although the diode conduction loss is high, at component level, the switching loss of the IGBT is predominant. The semiconductor loss efficeiency for vienna rectifier at 25kW is 99.176%. The switching losses increases with increase in frequency, but the change in the conduction losses would be less comparatively. This is an important observation and should be considered for proper selection of the switching frequency.

4.2 Future Work

There are some aspects that needs attention such as design of heat sink. Depending upon application and purpose, it would be imperative to calculate the harmonics distortion of currents (THD) at different frequencies. Implementing a control strategy for midpoint voltage is also very important from the operational aspect, that needs to be addressed.

Bibliography

[1] Viitanen T. (2005) "Space vector modulation of Boost-Type Three phase, three switch, three level Unidirectional PWM Rectifier-Analysis and implementation" Thesis for Doctor of Technology, Tampere University of Technology, Finland.

[2] Lipo T.A, Holmes D.G (2003) "Pulse width Modulation for Power Converters: Principles and Practice" Wiley-IEEE press.

[3] Kolar J.W, Drofenik U, Zach F.C (1996) "Current Handling Capability of the Neutral Point of Three-Phase /Switch/Level Boost-Type PWM (VIENNA) Rectifier" IEEE Power Electronics Specialists Conference, 23-27 June 1996, Baveno, Italy.

[4] Kolar J.W, Drofenik U, Zach F.C (1995) "Space Vector Based Analysis of the Variation and Control of the Neutral Point Potential of Hysteresis Current Controlled Three-Phase /Switch/Level Rectifier Systems" IEEE Proceedings, International Conference on Power Electronics and Drive Systems, 21-24 Feb.1995, Singapore.

[5] Kolar J.W, Ertl H, Zach F.C (1996) "Design and experimental investigation of a three-phase high power density high efficiency unity power factor PWM (VIENNA) rectifier employing a novel integrated power semiconductor module" IEEE- Applied Power Electronics Conference and Exposition, Conference Proceedings, 3-7 March 1996, San Jose, CA, USA.

[6] Haghbin, S. and Thiringer .T (2014) DC bus current harmonics of a three-phase PWM inverter with the zero sequence injection. In Proceedings. Transportation Electrification-Conference and Expo (ITEC), pages 1-6, Dearborn, MI.

[7] Ahmet M. Hava, Russel J. Kerkman, Thomas A. Lipo (1998)"Carrier-Based PWM-VSI Overmodulation Strategies: Analysis, Comparison, and Design" IEEE Transactions on Power Electronics, VOL. 13, NO. 4, JULY 1998

[8] Guo.Jing (2017) "Modelling and design of inverters using novel power loss calculations and DC-link current/voltage ripple estimation methods and bus bar analysis" Thesis for Doctor of Philosophy, McMaster University, Hamilton, Ontario, Canada, Feb. 2017.

[9] Bierhoff, M. H. and Fuchs, F. W. (2004). "Semiconductor losses in voltage source and current source IGBT converters based on analytical derivation". In Proceedings, Power Electronics Specialists Conference (PESC), pages 2836-2842, Aachen, Germany.

[10] L. Mestha and P. Evans. (1989). “Analysis of on-state losses in pwm inverters,” Electric Power Applications, IEE Proceedings B, vol. 136, no. 4, pp. 189– 195.

[11] Ali Rabiei. (2015) " Efficiency Analysis of Drive-train for an Electrified Vehicle" PhD thesis, Chalmers University of Technology, Sweden.

[12] R. Teichmann, S. Bernet. (2005). "A comparision of three- level converters versus two level converters for low voltage drives, traction and utility applications" IEEE Transactions on industrial applications, vol 41, May/June.
[13] Infineon IKW50N60H3, high speed IGBT in trench and field stop technology.
[14] Infineon IDW50E60, emitter controlled diode series.
[15] Infineon IKY50N120CH3, high speed switching third generation IGBT

A

Appendix

A.0.1 Analytical equations for currents used in Vienna rectifier for loss analysis

$I_{T,avg} = (1/pi - ma/4) * Ipeak;$
$I_{Dar,avg} = ma/4 * Ipeak;$
$I_{Da,avg} = 1/pi * Ipeak;$

$I_{T,rms} = sqrt((1/4) - (2 * ma)/(3 * pi)) * Ipeak;$
$I_{Dar,rms} = sqrt((2 * ma)/(3 * pi)) * Ipeak;$
$I_{Da,rms} = 1/2 * Ipeak;$

A.0.2 Matlab file for Vienna rectifier

A.0.2 Matlab file for Vienna rectifier

```
Tsw=1/20e3;
fsw=20e3;
tstop = 1/50;
tstep = 1e-6;
time = (tstep : tstep : tstop);
Vdc = 700;
A = sqrt(2);
ma=1.15;
Urms_phase=(Vdc/2)*ma/sqrt(2);
%ma=(Uph_peak*2)/Vdc;
Pac = 25e3;
phi=0;
Irms = Pac/(3*Urms_phase)*cos(phi); % phi is zero
Ipeak= sqrt(2)*Irms;
% for conduction losses
VT_IGBT=0.9;
VT_D=0.45;
VT_DF=0.45; % ~ VT_D

Rf_IGBT=0.022;
Rf_D=0.01;
Rf_DF=0.01; % ~ Rf_D

% for switching losses at Iref:

Vref = 400;
Iref = 50;
Esw_IGBT_on = 1.42e-3;
Esw_IGBT_off = 1.13e-3;
Esw_diode = 0.358e-3;

KiD=1;
KvD=0.6;
KiIGBT=1;
KvIGBT=1.35;


% Creation of phase voltages and phase currents :
u1 = A*Urms_phase*sin(100*pi*time);
u2 = A*Urms_phase*sin(100*pi*time - 2*pi/3);
u3 = A*Urms_phase*sin(100*pi*time - 4*pi/3);

i1 = A*Irms*sin(100*pi*time); % considering phase angle as zero/ upf
i2 = A*Irms*sin(100*pi*time - 2*pi/3); % considering phase angle as
zero/ upf
i3 = A*Irms*sin(100*pi*time - 4*pi/3); % considering phase angle as
zero/ upf

% THI having freq 3*fundamental and amlitude 1/6th of fundamental:
```

```
u3h = (A*Urms_phase/6)*sin(300*pi*time);

%Creating reference voltages by adding 3rd harmonic injection:
uref1 = u1 + u3h;
uref2 = u2 + u3h;
uref3 = u3 + u3h;

%Generation of a triangle wave:
t_onehalfswitchingperiod = Tsw/tstep/2;
OnePiece = Vdc/2-Vdc*time(1:floor(t_onehalfswitchingperiod))/(Tsw/2);
OneTriangleperiod = [OnePiece,-OnePiece];
NumberOfTrianglePeriods = ceil(tstop/Tsw);

TriangleWave_unadapted=[];
TriangleWave=[];
for j=1:NumberOfTrianglePeriods
    TriangleWave_unadapted=[TriangleWave_unadapted,OneTriangleperiod];
end
TriangleWave=TriangleWave_unadapted(1:length(time));

% Generation of double triangle waveform:

UTR1 = 0.5*(TriangleWave)+Vdc/4; % DC positive shift from 0
UTR2 = 0.5*(TriangleWave)-Vdc/4; % DC negative shift from 0
figure(2)
plot(time/10,UTR1,'r',time/10,UTR2,'b',time/10,uref1,'k')

% % Creating instantaneous pole voltages:

u1_inst = zeros(1,length(time));
u1_inst(uref1 > UTR1 & uref1 > UTR2) = 0.5*Vdc; % upper switch is OFF
u1_inst(uref1 < UTR1 & uref1 < UTR2) = -0.5*Vdc;% lower switch is OFF

u2_inst = zeros(1,length(time));
u2_inst(uref2 > UTR1 & uref2 > UTR2) = 0.5*Vdc;
u2_inst(uref2 < UTR1 & uref2 < UTR2) = -0.5*Vdc;

u3_inst = zeros(1,length(time));
u3_inst(uref3 > UTR1 & uref3 > UTR2) = 0.5*Vdc;
u3_inst(uref3 < UTR1 & uref3 < UTR2) = -0.5*Vdc;


figure(3)
plot(time*1000,u1_inst,'b', time*1000,uref1,'r')
xlabel('Time (ms)','FontSize',14)
ylabel(' Converter voltage(V)','FontSize',14)
l = legend('Phase A','Ref-A');
l.FontSize = 14;


%% Creating line voltages:
```

```
u12=u1_inst-u2_inst;
u23=u2_inst-u3_inst;
u31=u3_inst-u1_inst;

figure(4)
plot(time*1000,u12,'b')
xlabel('Time (ms)','FontSize',14)
ylabel(' Line voltage(V)','FontSize',14)
l = legend('Line to line -AB');
l.FontSize = 14;

%Initialising of current variables :
i_T1U=0*time;
i_T1L=0*time;
i_D1U=0*time;
i_D1L=0*time;
i_D1P=0*time;
i_D1N=0*time;

i_T2U=0*time;
i_T2L=0*time;
i_D2U=0*time;
i_D2L=0*time;
i_D2P=0*time;
i_D2N=0*time;

i_T3U=0*time;
i_T3L=0*time;
i_D3U=0*time;
i_D3L=0*time;
i_D3P=0*time;
i_D3N=0*time;


% leg 1
for count = 1:length(time)
    i_inv = i1(count);
    u_inv = uref1(count);
    x = sign(u1_inst);
    y = x(count); % sign:1= +ve*dc/2, sign:0= 0 state, sign:-1 = -
ve*dc/2

    if u_inv > 0   % for positive currents
         i_D1P(count) = i_inv;
        if y==0 % When upper switch is ON, corresponds to sign: 0 state
            i_T1U(count)= i_inv;     % Current also flows from D1P
        else    % When upper switch is OFF, coresponds to sign: 1 state
            i_D1U(count) = i_inv;    % Current also flows from D1P
        end

    else           % for negative currents
          i_D1N(count) = i_inv;
```

```
        if y==0 % When lower switch is ON, corresponds to sign: 0 state
            i_T1L(count) = i_inv;    % Current also flows from D1N
        else    % When lower switch is OFF, coresponds to sign: -1
state
            i_D1L(count) = i_inv;    % Current also flows from D1N
        end
    end

    % Leg 2
    u_inv = uref2(count);
    i_inv = i2(count);
    x = sign(u2_inst);
    y = x(count);
    if u_inv > 0
         i_D2P(count) = i_inv;
        if y==0
            i_T2U(count)= i_inv;
        else
            i_D2U(count) = i_inv;
        end
    else
        i_D2N(count) = i_inv;
        if y==0
            i_T2L(count) = i_inv;
        else
            i_D2L(count) = i_inv;
        end
    end

    % Leg 3
    u_inv = uref3(count);
    i_inv = i3(count);
    x = sign(u3_inst);
    y = x(count);

    if u_inv > 0
        i_D3P(count) = i_inv;
        if y==0
            i_T3U(count)= i_inv;
        else
            i_D3U(count) = i_inv;
        end
    else
        i_D3N(count) = i_inv;
        if y==0
            i_T3L(count) = i_inv;
        else
            i_D3L(count) = i_inv;
        end
    end
end
```

```
%correcting into positive currents
i_T1L= -i_T1L;
i_D1L= -i_D1L;
i_T2L= -i_T2L;
i_D2L= -i_D2L;
i_T3L= -i_T3L;
i_D3L= -i_D3L;
i_D1N= -i_D1N;
i_D2N= -i_D2N;
i_D3N= -i_D3N;

figure(11)
subplot(2,1,1)
plot(time*1000,i_T1U,'r',time*1000,i_D1U,'b',time*1000,i_D1P,'k')
xlabel('Time (ms)','FontSize',14)
ylabel('Current (A)','FontSize',14)
legend('S11','Dar1','Da1')
subplot(2,1,2)
plot(time*1000,i_T1L,'r',time*1000,i_D1L,'b',time*1000,i_D1N,'k')
xlabel('Time (ms)','FontSize',14)
ylabel('Current (A)','FontSize',14)
legend('S12','Dar2','Da2')

% By Simulation:
AverageT1=mean(i_T1U);
AverageD1U=mean(i_D1U);
AverageD1P=mean(i_D1P);

rmsT=sqrt(sum(i_T1U.*i_T1U)/count);
rmsD1U=sqrt(sum(i_D1U.*i_D1U)/count);
rmsD1P=sqrt(sum(i_D1P.*i_D1P)/count);

% By analytical equation from kolar:
I_T_avg=(1/pi-ma/4)*Ipeak;
I_DU_avg= ma/4*Ipeak;
I_DP_avg= 1/pi*Ipeak;

I_T_rms=sqrt((1/4)-(2*ma)/(3*pi))*Ipeak;
I_DU_rms= sqrt((2*ma)/(3*pi))*Ipeak;
I_DP_rms= 1/2*Ipeak;

X = [AverageT1,I_T_avg,AverageD1U,I_DU_avg,AverageD1P,I_DP_avg];
Y= [rmsT,I_T_rms,rmsD1U,I_DU_rms,rmsD1P,I_DP_rms];
% Calculation of ON state losses

p_Onstate_T1U=0*time;
p_Onstate_D1U=0*time;
p_Onstate_T1L=0*time;
p_Onstate_D1L=0*time;
p_On__TD1P=0*time;
p_On__DD1P=0*time;
p_On__TD1N=0*time;
```

```
p_On__DD1N=0*time;

p_Onstate_T2U=0*time;
p_Onstate_D2U=0*time;
p_Onstate_T2L=0*time;
p_Onstate_D2L=0*time;
p_On__TD2P=0*time;
p_On__DD2P=0*time;
p_On__TD2N=0*time;
p_On__DD2N=0*time;

p_Onstate_T3U=0*time;
p_Onstate_D3U=0*time;
p_Onstate_T3L=0*time;
p_Onstate_D3L=0*time;
p_On__TD3P=0*time;
p_On__DD3P=0*time;
p_On__TD3N=0*time;
p_On__DD3N=0*time;

for count=1:length(time)

    %  %leg 1
    if i_T1U(count)>0
        p_Onstate_T1U(count)=(VT_IGBT +
Rf_IGBT*i_T1U(count))*i_T1U(count);
        p_On__TD1P(count)=(VT_D + Rf_D*i_T1U(count))*i_T1U(count);
    end
    if i_D1U(count)>0
        p_Onstate_D1U(count)=(VT_DF + Rf_DF
*i_D1U(count))*i_D1U(count);
        p_On__DD1P(count)=(VT_D + Rf_D*i_D1U(count))*i_D1U(count);
    end
    if i_T1L(count)>0
        p_Onstate_T1L(count)=(VT_IGBT +
Rf_IGBT*i_T1L(count))*i_T1L(count);
        p_On__TD1N(count)=(VT_D + Rf_D*i_T1L(count))*i_T1L(count);
    end
    if i_D1L(count)>0
        p_Onstate_D1L(count)=(VT_DF + Rf_DF*i_D1L(count))*i_D1L(count);
        p_On__DD1N(count)=(VT_D + Rf_D*i_D1L(count))*i_D1L(count);
    end


    % %leg 2
   if i_T2U(count)>0
        p_Onstate_T2U(count)=(VT_IGBT +
Rf_IGBT*i_T2U(count))*i_T2U(count);
        p_On__TD2P(count)=(VT_D + Rf_D*i_T2U(count))*i_T2U(count);
    end
    if i_D2U(count)>0
```

```
        p_Onstate_D2U(count)=(VT_DF + Rf_DF
*i_D2U(count))*i_D2U(count);
        p_On__DD2P(count)=(VT_D + Rf_D*i_D2U(count))*i_D2U(count);
    end
    if i_T2L(count)>0
        p_Onstate_T2L(count)=(VT_IGBT +
Rf_IGBT*i_T2L(count))*i_T2L(count);
        p_On__TD2N(count)=(VT_D + Rf_D*i_T2L(count))*i_T2L(count);
    end
    if i_D2L(count)>0
        p_Onstate_D2L(count)=(VT_DF + Rf_DF*i_D2L(count))*i_D2L(count);
        p_On__DD2N(count)=(VT_D + Rf_D*i_D2L(count))*i_D2L(count);
    end


    % %leg 3
    if i_T3U(count)>0
        p_Onstate_T3U(count)=(VT_IGBT +
Rf_IGBT*i_T3U(count))*i_T3U(count);
        p_On__TD3P(count)=(VT_D + Rf_D*i_T3U(count))*i_T3U(count);
    end
    if i_D3U(count)>0
        p_Onstate_D3U(count)=(VT_DF + Rf_DF
*i_D3U(count))*i_D3U(count);
        p_On__DD3P(count)=(VT_D + Rf_D*i_D3U(count))*i_D3U(count);
    end
    if i_T3L(count)>0
        p_Onstate_T3L(count)=(VT_IGBT +
Rf_IGBT*i_T3L(count))*i_T3L(count);
        p_On__TD3N(count)=(VT_D + Rf_D*i_T3L(count))*i_T3L(count);
    end
    if i_D3L(count)>0
        p_Onstate_D3L(count)=(VT_DF + Rf_DF*i_D3L(count))*i_D3L(count);
        p_On__DD3N(count)=(VT_D + Rf_D*i_D3L(count))*i_D3L(count);
    end

end

p_Onstate_D1P=(p_On__TD1P + p_On__DD1P);
p_Onstate_D1N=(p_On__TD1N + p_On__DD1N);

p_Onstate_D2P=(p_On__TD2P + p_On__DD2P);
p_Onstate_D2N=(p_On__TD2N + p_On__DD2N);

p_Onstate_D3P=(p_On__TD3P + p_On__DD3P);
p_Onstate_D3N=(p_On__TD3N + p_On__DD3N);

a=mean(p_On__TD1P + p_On__DD1P);
b=mean(p_On__TD1N + p_On__DD1N);

c=mean(p_On__TD2P + p_On__DD2P);
d=mean(p_On__TD2N + p_On__DD2N);
```

```
e=mean(p_On__TD3P + p_On__DD3P);
f=mean(p_On__TD3N + p_On__DD3N);

g=[a b c d e f];

figure(5)
plot(time*1000,p_Onstate_D1U,'r',time*1000,p_Onstate_D1P,'k')
xlabel('Time (ms)','FontSize',14)
ylabel('Losses (W)','FontSize',14)
legend('D1U','D1P')
l = legend('Dar1','Da1');
l.FontSize = 14;
grid on
figure(6)
plot(time*1000,p_Onstate_T1U,'b',time*1000,p_Onstate_T1L,'r')
xlabel('Time (ms)','FontSize',14)
ylabel('Losses (W)','FontSize',14)
legend('S11','S12')
l = legend('S11','S12');
l.FontSize = 14;
grid on
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%% Average losses of components over once cycle%%%%%
P_Onstate_T1U=mean(p_Onstate_T1U);
P_Onstate_T1L=mean(p_Onstate_T1L);
P_Onstate_D1U=mean(p_Onstate_D1U);
P_Onstate_D1L=mean(p_Onstate_D1L);
p_Onstate_D1P=a;
p_Onstate_D1N=b;


P_Onstate_T2U=mean(p_Onstate_T2U);
P_Onstate_T2L=mean(p_Onstate_T2L);
P_Onstate_D2U=mean(p_Onstate_D2U);
P_Onstate_D2L=mean(p_Onstate_D2L);
p_Onstate_D2P=c;
p_Onstate_D2N=d;


P_Onstate_T3U=mean(p_Onstate_T3U);
P_Onstate_T3L=mean(p_Onstate_T3L);
P_Onstate_D3U=mean(p_Onstate_D3U);
P_Onstate_D3L=mean(p_Onstate_D3L);
p_Onstate_D3P=e;
p_Onstate_D3N=f;


J=[P_Onstate_T1U,P_Onstate_T1L,P_Onstate_D1U,P_Onstate_D1L,a,b];
K=[P_Onstate_T2U,P_Onstate_T2L,P_Onstate_D2U,P_Onstate_D2L,c,d];
L=[P_Onstate_T3U,P_Onstate_T3L,P_Onstate_D3U,P_Onstate_D3L,e,f];
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%
%%%% Calculation of Switching losses:
%%% Finding out the switching instances

% Leg 1 ------------------------------------------------------------------
---
diffT1U=i_T1U(2:length(i_T1U))-i_T1U(1:length(i_T1U)-1);
diffT1L=i_T1L(2:length(i_T1L))-i_T1L(1:length(i_T1L)-1);
[~,TransistorTurnOn1U]=find(diffT1U>1);
[~,TransistorTurnOff1U]=find(diffT1U<-1);
[~,TransistorTurnOn1L]=find(diffT1L>1);
[~,TransistorTurnOff1L]=find(diffT1L<-1);
% Leg 1 positive current
EswOn_T1U_inst=Esw_IGBT_on*i1(TransistorTurnOn1U)/Iref*(Vdc/2/Vref)^KvI
GBT;
EswOn_T1U=sum(EswOn_T1U_inst);

EswOff_T1U_inst=Esw_IGBT_off*i1(TransistorTurnOff1U)/Iref*(Vdc/2/Vref)^
KvIGBT;
EswOff_T1U=sum(EswOff_T1U_inst);

Err_D1U_inst=Esw_diode*(i1(TransistorTurnOn1U))/Iref*(Vdc/2/Vref)^KvD;
Err_D1U=sum(Err_D1U_inst);
% Leg 1 negative current
EswOn_T1L_inst=Esw_IGBT_on*(-
i1(TransistorTurnOn1L))/Iref*(Vdc/2/Vref)^KvIGBT;
EswOn_T1L=sum(EswOn_T1L_inst);

EswOff_T1L_inst=Esw_IGBT_off*(-
i1(TransistorTurnOff1L))/Iref*(Vdc/2/Vref)^KvIGBT;
EswOff_T1L=sum(EswOff_T1L_inst);

Err_D1L_inst=Esw_diode*(-i1(TransistorTurnOn1L))/Iref*(Vdc/2/Vref)^KvD;
Err_D1L=sum(Err_D1L_inst);

% Leg 2 ------------------------------------------------------------
diffT2U=i_T2U(2:length(i_T2U))-i_T2U(1:length(i_T2U)-1);
diffT2L=i_T2L(2:length(i_T2L))-i_T2L(1:length(i_T2L)-1);
[~,TransistorTurnOn2U]=find(diffT2U>1);
[~,TransistorTurnOff2U]=find(diffT2U<-1);
[~,TransistorTurnOn2L]=find(diffT2L>1);
[~,TransistorTurnOff2L]=find(diffT2L<-1);
% Leg 2 positive current
EswOn_T2U_inst=Esw_IGBT_on*i2(TransistorTurnOn2U)/Iref*(Vdc/2/Vref)^KvI
GBT;
EswOn_T2U=sum(EswOn_T2U_inst);

EswOff_T2U_inst=Esw_IGBT_off*i2(TransistorTurnOff2U)/Iref*(Vdc/2/Vref)^
KvIGBT;
EswOff_T2U=sum(EswOff_T2U_inst);
```

```
Err_D2U_inst=Esw_diode*(i2(TransistorTurnOn2U))/Iref*(Vdc/2/Vref)^KvD;
Err_D2U=sum(Err_D2U_inst);
% Leg 2 negative current
EswOn_T2L_inst=Esw_IGBT_on*(-
i2(TransistorTurnOn2L))/Iref*(Vdc/2/Vref)^KvIGBT;
EswOn_T2L=sum(EswOn_T2L_inst);

EswOff_T2L_inst=Esw_IGBT_off*(-
i2(TransistorTurnOff2L))/Iref*(Vdc/2/Vref)^KvIGBT;
EswOff_T2L=sum(EswOff_T2L_inst);

Err_D2L_inst=Esw_diode*(-i2(TransistorTurnOn2L))/Iref*(Vdc/2/Vref)^KvD;
Err_D2L=sum(Err_D2L_inst);

% Leg 3 ----------------------------------------------------------------
-
diffT3U=i_T3U(2:length(i_T3U))-i_T3U(1:length(i_T3U)-1);
diffT3L=i_T3L(2:length(i_T3L))-i_T3L(1:length(i_T3L)-1);
[~,TransistorTurnOn3U]=find(diffT3U>1);
[~,TransistorTurnOff3U]=find(diffT3U<-1);
[~,TransistorTurnOn3L]=find(diffT3L>1);
[~,TransistorTurnOff3L]=find(diffT3L<-1);
% Leg 3 positive current
EswOn_T3U_inst=Esw_IGBT_on*i3(TransistorTurnOn3U)/Iref*(Vdc/2/Vref)^KvI
GBT;
EswOn_T3U=sum(EswOn_T3U_inst);

EswOff_T3U_inst=Esw_IGBT_off*i3(TransistorTurnOff3U)/Iref*(Vdc/2/Vref)^
KvIGBT;
EswOff_T3U=sum(EswOff_T3U_inst);

Err_D3U_inst=Esw_diode*(i3(TransistorTurnOn3U))/Iref*(Vdc/2/Vref)^KvD;
Err_D3U=sum(Err_D3U_inst);
% Leg 3 negative current
EswOn_T3L_inst=Esw_IGBT_on*(-
i3(TransistorTurnOn3L))/Iref*(Vdc/2/Vref)^KvIGBT;
EswOn_T3L=sum(EswOn_T3L_inst);

EswOff_T3L_inst=Esw_IGBT_off*(-
i3(TransistorTurnOff3L))/Iref*(Vdc/2/Vref)^KvIGBT;
EswOff_T3L=sum(EswOff_T3L_inst);

Err_D3L_inst=Esw_diode*(-i3(TransistorTurnOn3L))/Iref*(Vdc/2/Vref)^KvD;
Err_D3L=sum(Err_D3L_inst);

%% Switching loss coefficient summation

PswOn_T1U=EswOn_T1U/time(length(time));
PswOff_T1U=EswOff_T1U/time(length(time));
PswErr_D1U=Err_D1U/time(length(time));

PswOn_T1L=EswOn_T1L/time(length(time));
```

```
PswOff_T1L=EswOff_T1L/time(length(time));
PswErr_D1L=Err_D1L/time(length(time));

PswOn_T2U=EswOn_T2U/time(length(time));
PswOff_T2U=EswOff_T2U/time(length(time));
PswErr_D2U=Err_D2U/time(length(time));

PswOn_T2L=EswOn_T2L/time(length(time));
PswOff_T2L=EswOff_T2L/time(length(time));
PswErr_D2L=Err_D2L/time(length(time));


PswOn_T3U=EswOn_T3U/time(length(time));
PswOff_T3U=EswOff_T3U/time(length(time));
PswErr_D3U=Err_D3U/time(length(time));

PswOn_T3L=EswOn_T3L/time(length(time));
PswOff_T3L=EswOff_T3L/time(length(time));
PswErr_D3L=Err_D3L/time(length(time));

Psw_T1U=PswOn_T1U+PswOff_T1U;
Psw_T1L=PswOn_T1L+PswOff_T1L;
Psw_D1U=PswErr_D1U;
Psw_D1L=PswErr_D1L;
Psw_T2U=PswOn_T2U+PswOff_T2U;
Psw_T2L=PswOn_T2L+PswOff_T2L;
Psw_D2U=PswErr_D2U;
Psw_D2L=PswErr_D2L;
Psw_T3U=PswOn_T3U+PswOff_T3U;
Psw_T3L=PswOn_T3L+PswOff_T3L;
Psw_D3U=PswErr_D3U;
Psw_D3L=PswErr_D3L;
```