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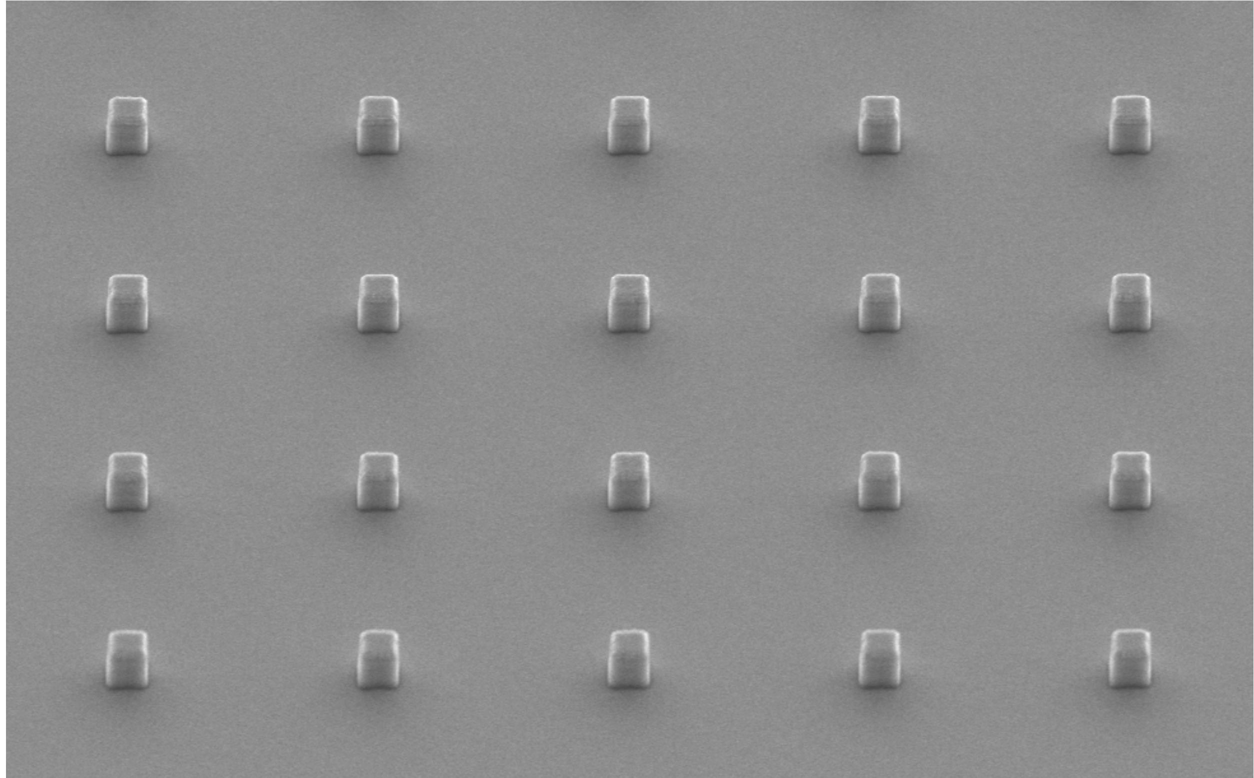

Development of a HBr-Based ICP-RIE Process for Smooth and Anisotropic Etching of III–V Semiconductors

Master’s thesis in Nanotechnology

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Cover: Collection of 0.25 µm^2 FMBD-D anodes etched with a HBr-based ICP-RIE dry etch process.

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Abstract

This thesis presents the development of a dry etching recipe using hydrogen bromide (HBr) for the fabrication of InP/InGaAs-based heterostructures. The recipe aims to replace a methane-based process to avoid chamber contamination while maintaining a highly directional etch profiles and smooth surfaces. HBr in particular was selected as an alternative etching chemistry due to its potential to achieve desired result, while also offering reduced plasma-induced damage compared to conventional processes. Though systematic research and optimization of process parameters such as, pressure, temperature, ICP-power, RF-power, and flowrate, a recipe was developed that produces sidewall-angles up to 88.9 degrees and smooth surfaces. A hard mask material combination of Ni and Cr was found to be optimal which yields a selectivity up to 22:1, and a Si carrier should be used to ad a passivation mechanism to the etching recipe. The developed recipe has successfully been applied to Fermi-level managed barrier diodes (FMBD), resonant-tunnelling diodes (RTD), and heterostructure barrier varactors (HBV), demonstrating consistent etch-performance across different InP/InGaAs-layer stacks. Electrical measurements confirmed functionality of devices fabricated using the new process, validating the suitability as a replacement for the methane-based dry etch process recipe.

Keywords: Dry etching, Hydrogen bromide (HBr), Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE), InP/InGaAs heterostructures, Anisotropic etching, Sidewall damage, hard mask, Fermi-level Managed Barrier Diode (FMBD)

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Emil Nyström, Gothenburg, February 2026

List of Acronyms

Acronyms used in this thesis are listed in alphabetical order below:

EDX	Energy Dispersive X-ray Spectroscopy
FMBD	Fermi-level Managed Barrier Diode
FMBD-S	Fermi-level Managed Barrier Diode (Single)
FMBD-D	Fermi-level Managed Barrier Diode (Double)
HBV	Heterostructure Barrier Varactor
ICP	Inductively Coupled Plasma
RIE	Reactive Ion Etching
RF	Radio frequency
RTD	Resonant-Tunnelling Diode
SEM	Scanning Electron Microscopy

Nomenclature

Symbols and Units

S	Selectivity
V_{dc}	DC bias voltage
$sccm$	Standard cubic centimeters per minute
eV	Electron volt

Materials and Compounds

HBr	Hydrogen bromide (etching gas)
CH_4	Methane (traditional etching gas)
CH_4/H_2	Methane-hydrogen gas mixture
InP	Indium phosphide
InGaAs	Indium gallium arsenide
InAlAs	Indium aluminum arsenide
AlAs	Aluminum arsenide
Ni	Nickel (hard mask material)
Cr	Chromium (hard mask material)
Ti	Titanium (hard mask material)
$NiBr_x$	Nickel bromide (etch byproduct)
$InBr_x$	Indium bromide (etch byproduct)

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1 Introduction

Dry etching is a important fabrication process in III-V semiconductor manufacturing, utilizing plasma-driven chemical reactions or accelerated ions to precisely remove material. Traditionally, methane (CH_4) or methane–hydrogen (CH_4/H_2) gas mixtures have been used for the dry etching of III–V semiconductor materials to form vertical profiles and smoothly etched surfaces [4]. This is partly due to the formation of a polymer-assisted sidewall passivation layer as a result of a CH-based plasma, which enables highly anisotropic etching while simultaneously reducing plasma-induced damage to the etched sidewalls. These advantages are particularly important for high-frequency and optoelectronic devices, where surface roughness and plasma-induced damage can have a significant impact on device performance. However, the same polymer-film also accumulates on the interior surfaces of the reaction chamber, leading to contamination and maintenance issues [5]. This becomes particularly problematic in a shared cleanroom environment where the same etching system is used for multiple different and sensitive processes. Therefore, based on prior work by Bouchoule et al. [6], this study investigates (HBr) as an alternative etching chemistry for III-V semiconductor materials. HBr is of interest due to its potential to achieve anisotropic etching without causing chamber contamination, while also offering the prospect of lower plasma-induced damage compared to conventional chlorine-based processes [7]. By exploring the usage of HBr, this thesis aims to develop a suitable ICP-RIE process recipe to etch III–V semiconductor heterostructures without contaminating the chamber. In doing so, this research will contribute to a cleaner and more maintainable semiconductor manufacturing processes, more suitable for a shared cleanroom environment. During the research and development of such a recipe a secondary aim was expand the understanding and documentation of dry etching effects. By providing a deeper understanding of parameter effects, future projects are able to more efficiently develop new recipes when required as well as further optimizing the process as research progresses.

1.0.1 Problem definition

The objective in this project can be summarized by the following questions:

- How do process parameters such as temperature, pressure, ICP and RF power, and HBr flow rate affect etching characteristics?
- Which parameter(s) are crucial for achieving vertical sidewalls and smooth surfaces?
- How can etching defects be avoided or limited by adjusting process parameters?
- Can the same recipe be used to etch different InP/InGaAs heterostructures?
- Which mask-material is suitable for the etching process?

1.0.2 Limitations

The project has a quite short time frame of 4 mounts, and to effectively work towards both objectives of the project, some limitations have been necessary. Due to the time constraint, the systematic study for parameter effects had to be limited to prioritise time and material towards the primary objective. Additionally, more advanced techniques to measure etching characteristics was not prioritised, as these generally are more time consuming and would require additional time to learn. This project was therefore limited primarily to SEM imaging for examination of etching results. Furthermore, the project limited research to a single gas and carrier wafer combination, due to experimentation with these effecting the chemistry and thus greatly raising the complexity of the project.

2

Theory

2.1 Dry etching

The high demand of verticality and surface quality requires a thorough understanding of the underlying mechanisms and principles of the dry etching process. In general, dry etching can be defined as a process utilizing plasma driven chemical reactions or accelerated ions to remove material. In contrast to wet etching, which is purely chemical and therefore isotropic, dry etching methods often include a directional component by accelerating ions towards the substrate. This gives the technique the potential for highly anisotropic etching for materials where this is not possible by wet etching. However, dry etching is in general more complicated, requires expensive equipment and need more resources to design and develop a good etching recipe [8]. In this project the Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE) technique is used. This process utilizes two electromagnetic fields in order to separate control of the plasma and the flow of ions. Therefore. the different etching mechanisms can almost be controlled independently in the process, which allows for etching to be anisotropic while damage is minimized [5]. To explain the ICP-RIE technique in detail the system can be divided into three parts; Plasma Generation, Ion Transport, and Etching. A schematic of a typical ICP-RIE reactor is displayed below in figure 2.1.

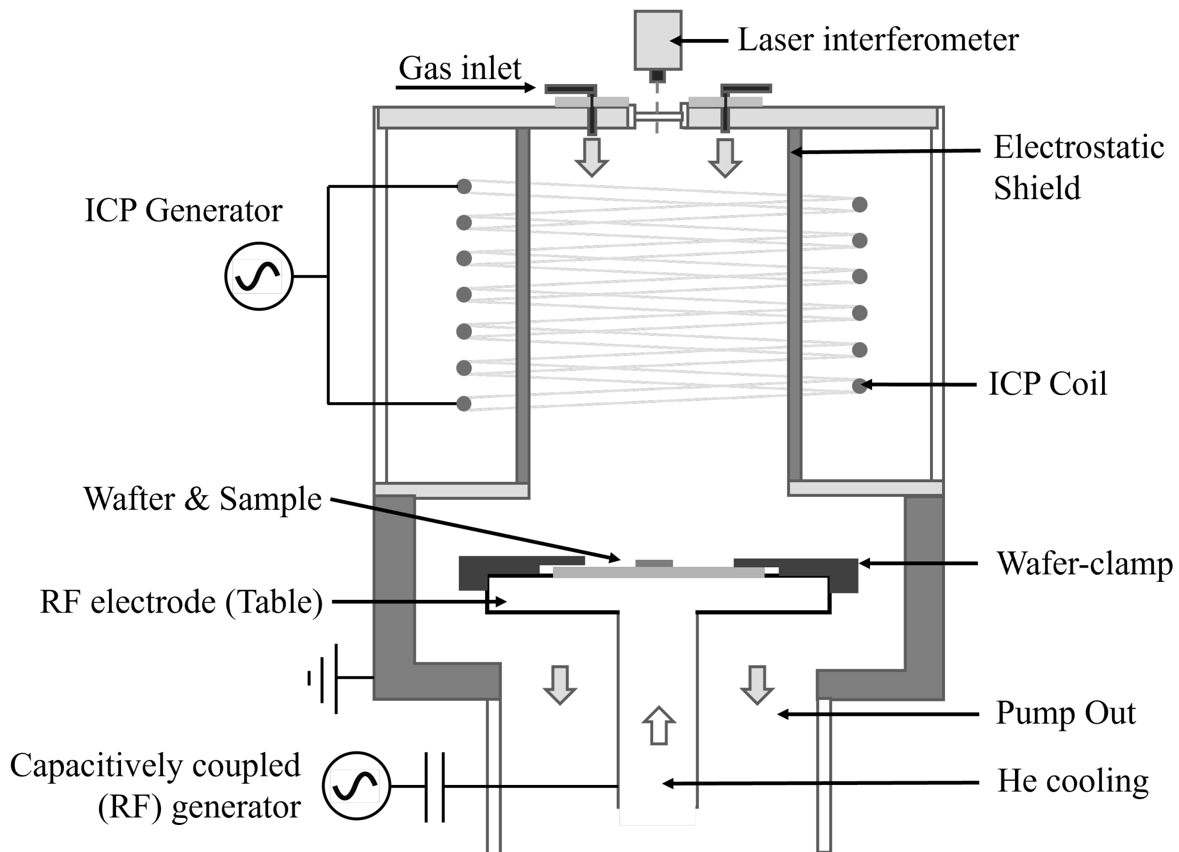


Figure 2.1: Schematic representation of the actual Plasmalab System 100 ICP-RIE process chamber configuration used in this study

Plasma generation

An ICP-RIE reactor creates a plasma by applying a electric field parallel to the substrate with a coil located at the top of the reactor as seen in figure 2.1. The field in turn accelerates electrons which collide with molecules in the gas, where one of four things can happen:

- Excitation: The collision provides energy for a electron within the molecule exist in a excited state. But since excited states are in general unstable, the electron will soon go back to it's previous state, releasing a photon in the process. This is why the plasma is seen to glow.

- Ionization: Here the colliding electron have enough energy to expel a electron from the gas-molecule, causing it to become a positive ion.

- Dissociation: If the the energy transferred by the electron collision is higher than the bonding energy of the molecule, it will cause it to separate into highly reactive neutral radicals.

- Electron attachment: The electron is attached to the molecule forming a negative ion.

Because the outcome of a collision largely depends on electron energy, the plasma composition can thus be adjusted by the ICP-power parameter [8].For the ICP-RIE process, ionization and dissociation are key, as these produces the highly reactive radicals and the positive ions utilized for etching. The ICP-power that corresponds to the optimal ratio of these reactions depends in turn on the gas type and composition, the pressure, and the flowrate of the process gas. The optimal ICP power is therefore highly process-specific, but values generally range from 300 to 1500 W. Furthermore, the amount of ions (degree of ionization) in turn defines the plasma potential, which is an important factor in relation to ion transport [9].

Ion transport

Some distance below the ICP, is the RF electrode (often referred to as the table), on which a carrier wafer is placed, as seen in figure 2.1. This electrode is connected to a radio-frequency (RF) power supply through a blocking capacitor, while a counter-electrode located at the top of the chamber is electrically grounded. Together, these electrodes establish an electric field normal to the substrate surface and perpendicular to the inductively coupled plasma (ICP) field. The frequency of this RF field is set so electrons oscillate with the electric field but not the much heavier ions, typically at a frequency of 13.56 MHz. Furthermore, because the lower electrode is connected to a blocking capacitor, the electrode is gradually biased to a negative potential. This results in the formation of a direct current (DC) bias between the electrode potential and the plasma potential which we refer to as self bias, V_{dc}. As a result of this negative self bias, very few electrons accumulate at the lower electrode. This creates a 'ion sheath' below the plasma, where very few excitations occur as the probability for collision with a electron is low, and almost no light is emitted. Since the bias is negative, the interface between the ion-sheath and plasma attracts nearby positive ions which are then accelerated towards the lower electrode [9]. For anisotropic etching, high directionality of ions when colliding with the substrate is key [8]. This is dependent on the average distance a ion on travel through the sheath without colliding with other species, otherwise known as the mean-free path. A longer mean free path thus results in higher overall directionality due to a less overall scattering effect. To reduce the probability of collision, one can either increase the velocity of the ion, or decrease the number of particles. In the ICP-RIE system ion velocity is directly controlled by the RF-power parameter as this determines the force with which these ions are accelerated, and the number of particles is controlled by the process pressure. Therefore, to increase the mean free path, one can either reduce the pressure or increase RF-power. However, as less kinetic energy is lost due to collisions,

ions will have more energy when colliding with the substrate, which can increase physical damage to the surface [9].

Etching mechanisms

Most of the etching in an ICP-RIE reactor, for a well optimized recipe, is performed by kinetically assisted chemical etching. But material may be removed by purely chemical and physical interactions as well [9]. Figure 2.2 show a illustration how material is removed in a ICP-RIE, and how a passivation layer may affect etch profile.

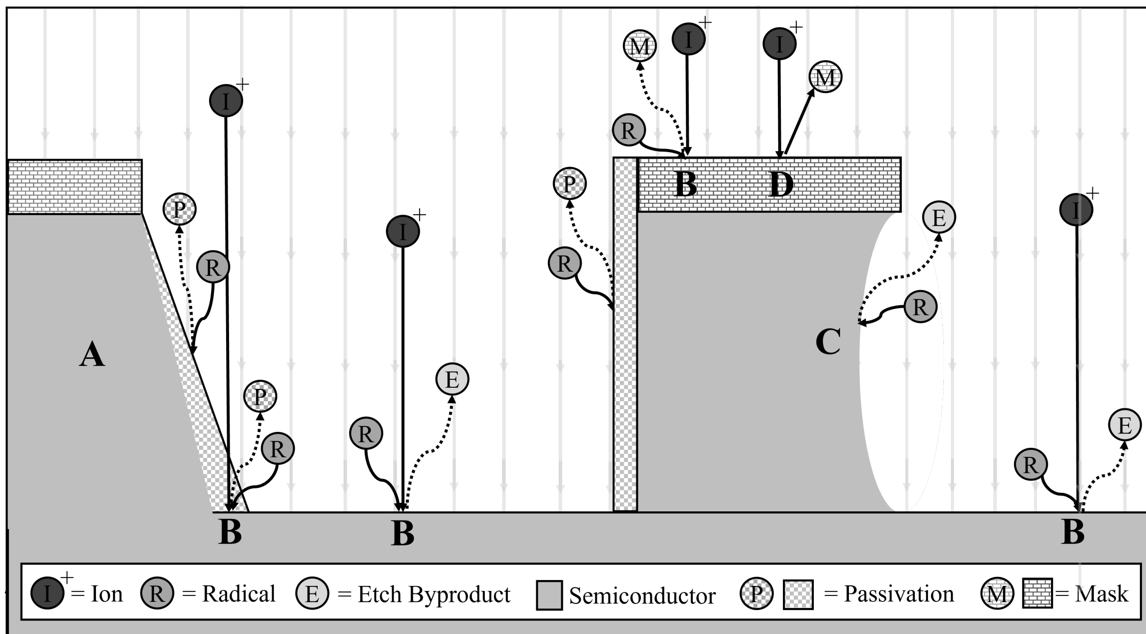


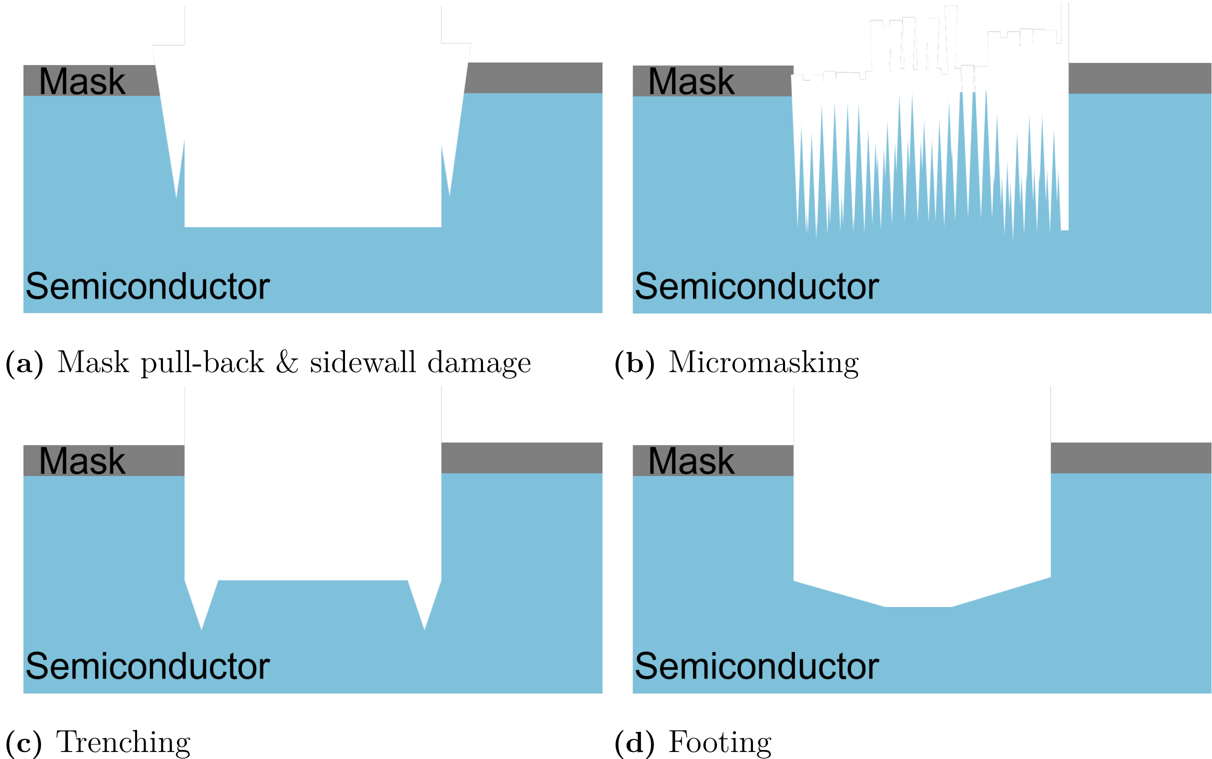
Figure 2.2: Illustration of the the combined etching mechanisms in a ICP-RIE system, and how a passivation layer effect resulting etch profile.

Chemical etching in a ICP-RIE system occurs when a radical comes in contact with the material where it reacts and forms new species, refereed to as etch by-products. These then desorb from the surface and thus remove material (Fig. 2.2 C). The volatility of these by-products is important to consider to make sure that they are efficiently removed. If by-product volatility is low they may not effectively desorb, or redeposit onto the surface, which can cause problems. To account for this, by-product volatility can be increased by increasing temperature [8]. Furthermore, the neutral radicals are not affected by the RF-fields and therefore etch in all directions, but this etching is relatively slow. Because of this, the process utilize the directed ions to kinetically assist the slow chemical etching, increasing the etch rate in the vertical direction (Fig. 2.2 B). This is how the ICP-RIE process achieves anisotropic etching, without relying on harsher physical sputter etching by ions [5]. However, as chemical etching still occurs in the horizontal direction, this can cause an undercut profile if not limited further (Fig. 2.2 C). Therefore, to achieve

a vertical etch-profile without a undercut, a passivating layer has to be introduced [9]. For etching mechanisms in the vertical direction the passivation layer have a relatively small effect on etch rate. But for the slow non-assisted chemical reactions this acts as a sacrificial layer on the sidewalls. Therefore, to achieve vertical sidewalls, the etch process is tuned so that the deposition rate of passivating film is in balance with horizontal etch rate. If not, the sidewall will be either over-passivated causing a sloped profile (Fig. 2.2A), or under-passivated resulting in a undercut (Fig. 2.2C). For some process gases, such as methane, the formation of a passivating film is included. But for most processes this is achieved by introducing a additional gas such as N_2 or Si_4, or by using a carrier wafer material such as Silicon, whose etch by-product form the passivation layer [9].

2.1.1 Etching defects

Although the ICP-RIE can be relatively gentle on the substrate, etch induced defects are likely to be encountered while developing a recipe. These usually are a result of a unoptimized process or with the fabrication of the mask which directly translates to etching defects. However, these defects also provide valuable information of etching characteristics which can be used to improve the process. Therefore, this section provides a overview of the most common defects one might encounter is presented. A schematic illustrating these viewed from the side is displayed in figure 2.3.



(a) Mask pull-back & sidewall damage **(b)** Micromasking

(c) Trenching **(d)** Footing

Figure 2.3: Illustration of common etching defects.

Sidewall damage

Sidewall damage is observed if ions start excessively striking the sidewall surface of the structure during etching. This can occur if edges of the mask are to thin and therefore has been etched away during the process, as if the mask had been 'pulled back' from the sidewalls. Highly directed ions can then start to attack the top of the material, effectively etching down into the sidewall as seen in figure 2.3a [10].

Micromasking

If the surface appears to have a rougher or 'grass-like' texture (Fig. 2.3b), micro-masking is most likely the cause. This occurs when small etch resistant particles are present on the surface during etching, which prevents even etching over the surface. For a anisotropic etch process this is further amplified, as there is little lateral etching to even out the defects [11].

Trenching

Trenching is characterised by a sidewall which ends in a narrow trench at the bottom (Fig. 2.3c). This occur when the sidewall builds up charge that redirects ions 'focusing' these towards a smaller area. Thus increasing etch rate at that location and forming a micro-trench. The effect is likely to be amplified if sidewalls are sloped or the directionally is lower. This defect can be a issue if the trench is deep enough to span multiple layers, which can have significant impact on device performance [10].

Footing

Footing is identifiable by a slight slope in the surface near structures (Fig. 2.3d). This occur when etch-rate is slower near structures, which is typically a result of lower amount of etchants in those areas or redirection of ions. As long as this footing is in one layer and the width does not impact further device fabrication, this defect has minimal impact on device performance [12].

Curtaining

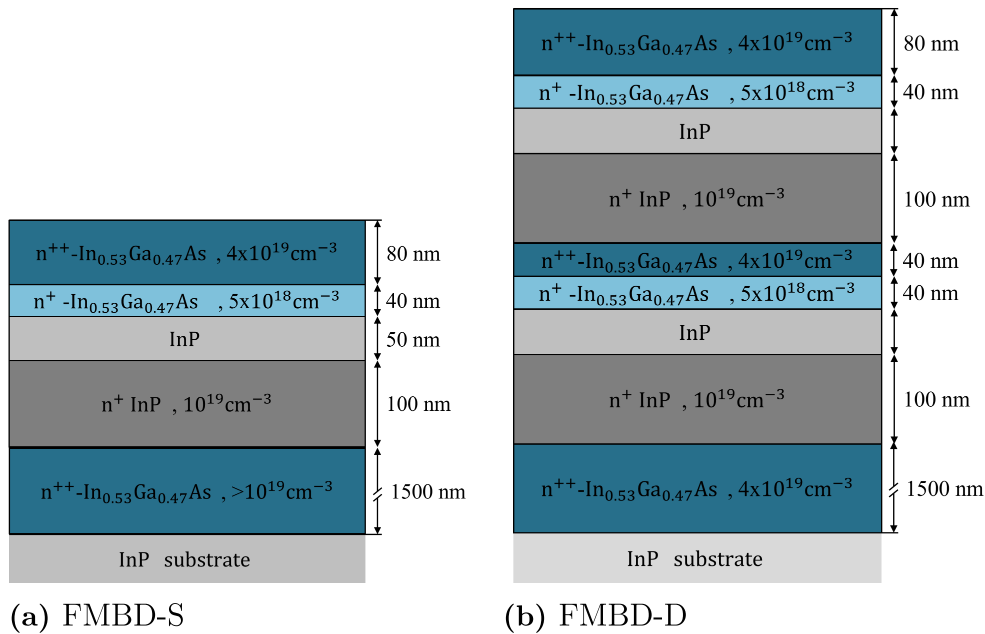
If the sides of the mask are to uneven this can transfer to the sidewall during etching, resulting in wavy texture which looks much like draped curtains. These can be caused by the granularity of the deposited mask or by the finite resolution of the beam step size in the lithography. [10].

2.2 Materials

During this project etching has been evaluated for three different III-V semiconductor heterostructures, each primary composed of InP and/or InGaAs layers. These are currently researched within the department to study various types of high frequency semiconductor devices. This section serves to outline the properties of the different heterostructures and device operation, in the context of ICP-RIE etching.

2.2.1 Fermi-level managed barrier diode

The primary heterostructure studied in this project is used to fabricate Fermi-Level Managed Barrier Diode (FMBD). Unlike a conventional Schottky barrier, this type of device creates a barrier by means of a interface between differently doped layers of InP and InGaAs [13]. In this work two FMBD configurations has been studied, one is refereed to as the single stack (FMBD-S) containing one barrier, and the other is refereed to as a double stack (FMBD-D), which repeats the top four layers of the single stack to include two barriers [14]. A schematic of these is displayed in figure 2.4, with the corresponding layer- , composition, doping level, and thickness.



(a) FMBD-S **(b)** FMBD-D

Figure 2.4: Schematic of the FMBD epitaxial layer stacks grown on a InP substrate. Top and bottom InGaAs layers are the contact layers.

The heterostructure is fabricated by epitaxial growth where doping can be very controlled, allowing for the formation of very low and controlled barrier heights. These properties results in a diode with very low turn on voltage and thus high a sensitivity. This is a key feature which makes FMBD-diodes suitable for applications such as zero bias detector

diodes, in this case intended for terahertz detection. However, due to the high capacitance between the highly doped InGaAs layer and the undoped InP layer, the high frequency behaviour is limited to around 300 GHz . One way to reduce capacitance is to decrease the junction area of the anode to sub-micrometer dimensions. This requires highly vertical etching, as well as smooth surfaces with without any surface defects, which significantly increases fabrication complexity and, to date, has only been feasible using dry etching techniques [1]. Another way to address the high capacity problem is to put layer stacks in series which reduce the effective junction capacitance while maintaining a relatively low series resistance [14]. This done in the 'Double-stack FMBD' (Fig. 2.4b) with two stacks. A characteristic I–V curve is shown in Fig. 2.5, alongside a schematic band diagram of the FMBD structure.

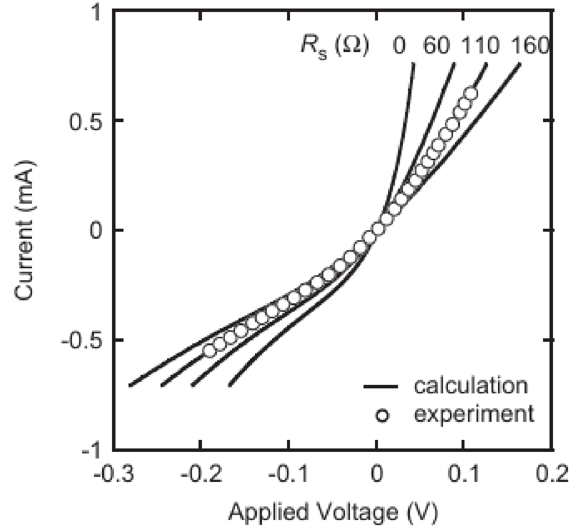


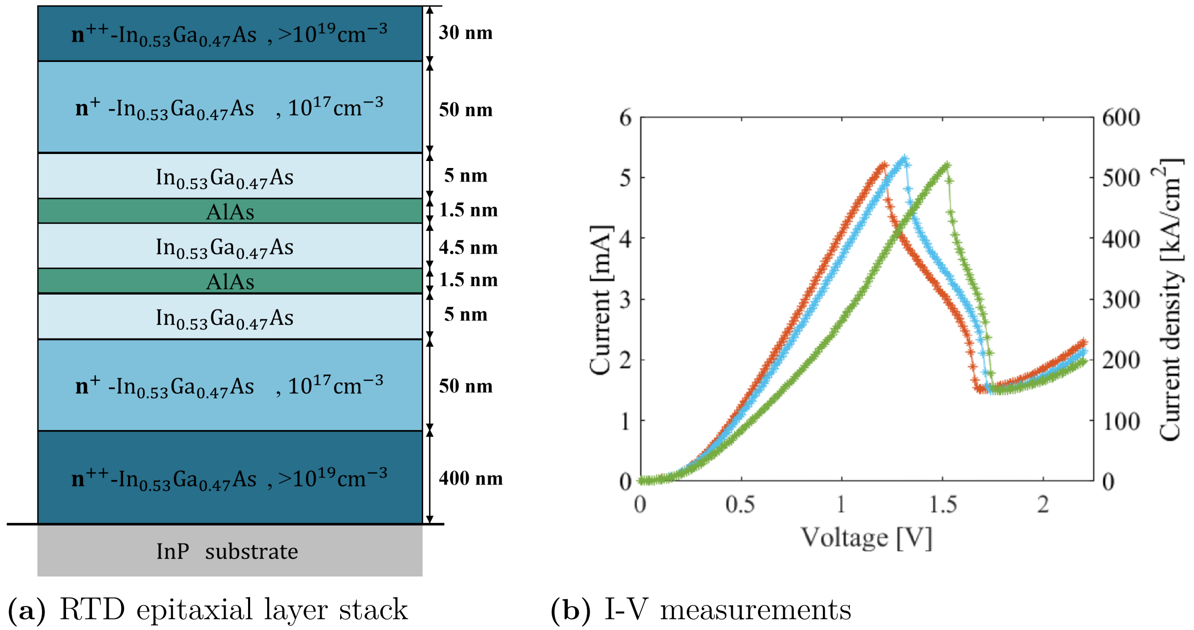
Figure 2.5: I-V characteristics for a single layer FMBD. Solid curves are fitting calculations for several series resistances [1].

As shown in Figure 2.5, the current starts to increase at very low applied voltages and rises sharply as the voltage is further increased, reflecting the low turn-on voltage and high sensitivity described previously.

2.2.2 Resonant-tunnelling diode

The second heterostructures studied in this thesis is the resonant tunnelling diode (RTD). These devices utilize a double-barrier structure to create a well with quantized states. Electrons may then tunnel trough this barrier with a high probability as their energy level align with the resonant states of the well formed between the barriers [15]. This property creates a negative differential conductance (NDC). Due to the fast dynamics of the NDC this enables high frequency oscillations as long as parasitic resistances are low.

The frequency of these is determined by the resonance of the internal capacitance and the external inductance [16]. Larger anodes are useful for higher power applications, but smaller sizes are required for high frequency operation [17]. The RTDs studied in this project are mainly comprised of InGaAs at different doping levels, with a thin undoped InGaAs layer (4.5 nm) sandwiched between two very thin (1.5 nm) undoped AlAs layers, which create the double-barrier [2]. A schematic of the cross-sectional layout for such a RTD device is displayed in 2.6a, along with measurements showing the characteristic I-V behaviour.



(a) RTD epitaxial layer stack **(b)** I-V measurements

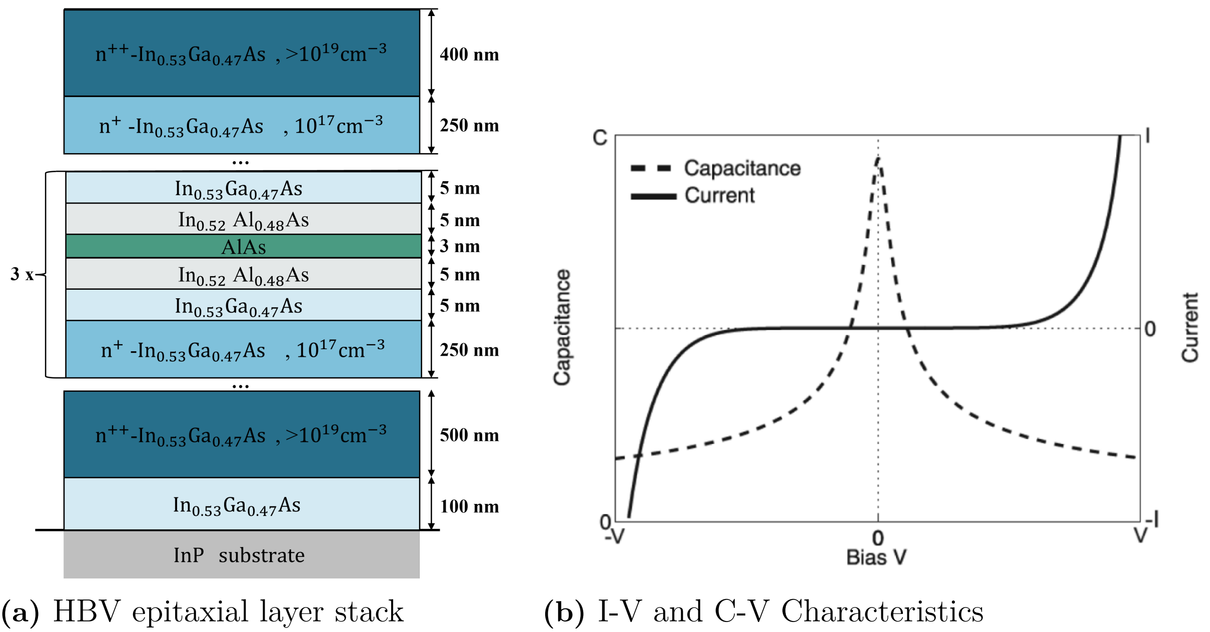
Figure 2.6: (a) Schematic of the RTD epitaxial layer stack (b) I-V measurements of three 1x1 um RTDs, fabricated with a methane based ICP-RIE process [2].

For device fabrication the RTD is etched down about ˜160 nm, stopping in the bottom n+ InGaAs layer. Afterwards the bottom contact is deposited on the same player completing the device. The diodes used for the I-V measurements seen in figure 2.6b, have a Ti/Pd/Au/Ti metal stack as top contact, and were etched with the previously used methane-based dry etch process. Furthermore, the characteristic measurements display a non-linear increase in current until it reaches the peak and current drops significantly. This region where current drops is the negative differential conductance region [2]

2.2.3 Heterostructure barrier varactor

The third layer stack studied in this project is a socalled heterostructure barrier varactor (HBV). As the name suggests, an HBV is a voltage-controlled semiconductor device in which the capacitance is tuned by the applied voltage. The HBV is designed for frequency multiplication through it's non-linear capacitance-voltage (C-V) characteristics,

which generate harmonics of an input signal due to the periodic modulation of capacitance with the applied voltage [18]. In this case this is achieved in a structure of mostly layers of InGaAs, where layers of undoped high-bandgap semiconductors (InAlAs) are used to create a barriers when sandwiched between the moderately doped InGaAs modulation-layers. This is refereed as the active region, and is responsible for the electrical characteristics, while highly doped InGaAs layers serve to provide low access resistance and good ohmic contacts [19]. Additionally, AlAs layers are included in-between InAlAs layers to improve the effective barrier height, and further suppressing leakage current [3]. A schematic of the HBV layer-stack is displayed in figure 2.7, along with a the typical I-V and C-V characteristics.



(a) HBV epitaxial layer stack

(b) I-V and C-V Characteristics

Figure 2.7: (a) A schematic of the HBV epitaxial layer stack, where the n^{++} InGaAs layers are the contact layers. (b) Typical I-V and C-V Characteristics of the HBV diode [3].

As seen in figure 2.7a, the HBV is a unipolar and symmetric device, which translates to the symmetric C-V and antisymmetric I-V characteristics seen in figure 2.7b. Where symmetric C-V characteristic is a result of the device's symmetric layer structure, while the antisymmetric I-V characteristic arises from the unipolar nature of the charge transport. As this kind of device is not limited by the capacitance, a small mesa size is not as crucial, and instead a optimal size relative the number of barriers is the vital for device performance, while minimizing self heating and leakage current [20].

3

Methods

3.1 Sample fabrication

All fabrication done within this project has been carried out in the MC2 Nanofabrication Laboratory at Chalmers University of Technology. The facilities is operated by Myfab - the Swedish research infrastructure for micro- and nanofabrication, where tools are shared among users from both Chalmers university and external companies. The clean-room is classified to ISO 5, with a maximum particle density of 3520 particles per cubic meter. It also features an exceptional vibration isolation rating of BBN-E, with additional isolation provided for particularly sensitive equipment. This section describes the anode fabrication process step by step, with detailed process parameters listed in Appendix A. A schematic illustrating fabrication steps can be seen in figure 3.1.

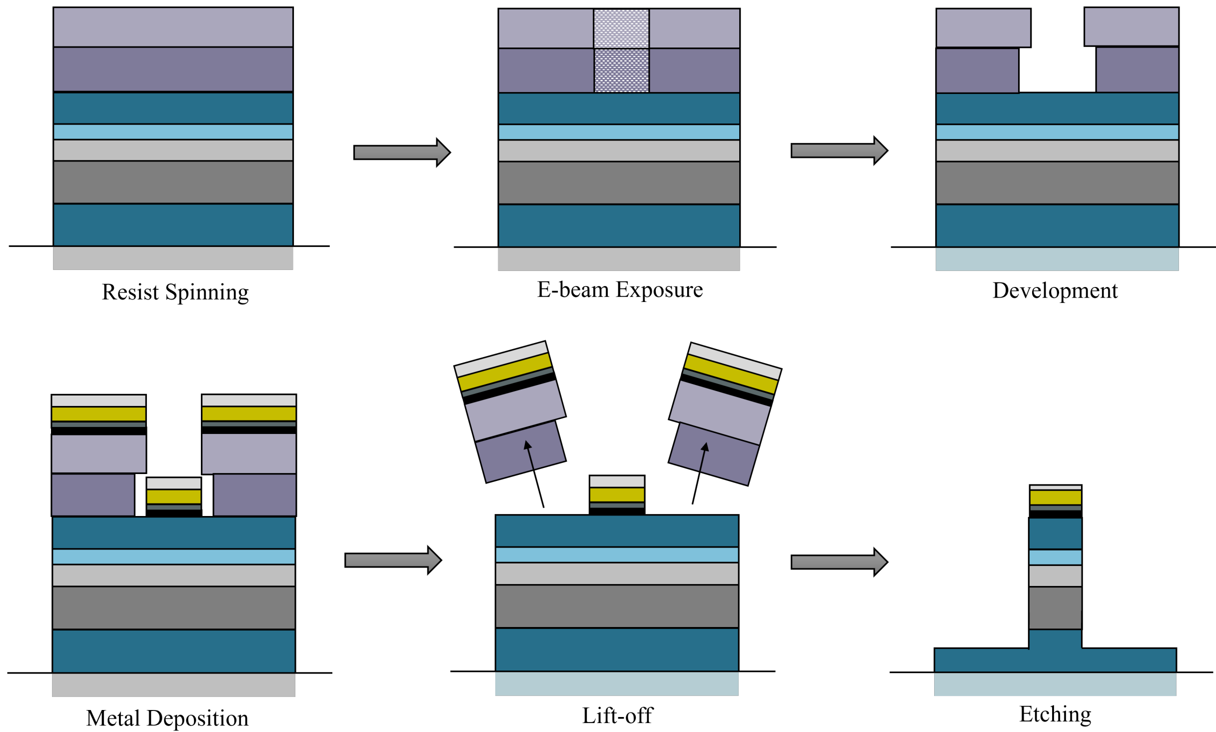


Figure 3.1: Illustration of consecutive fabrication steps for anode formation in the FMBD-S epitaxial layer stack.

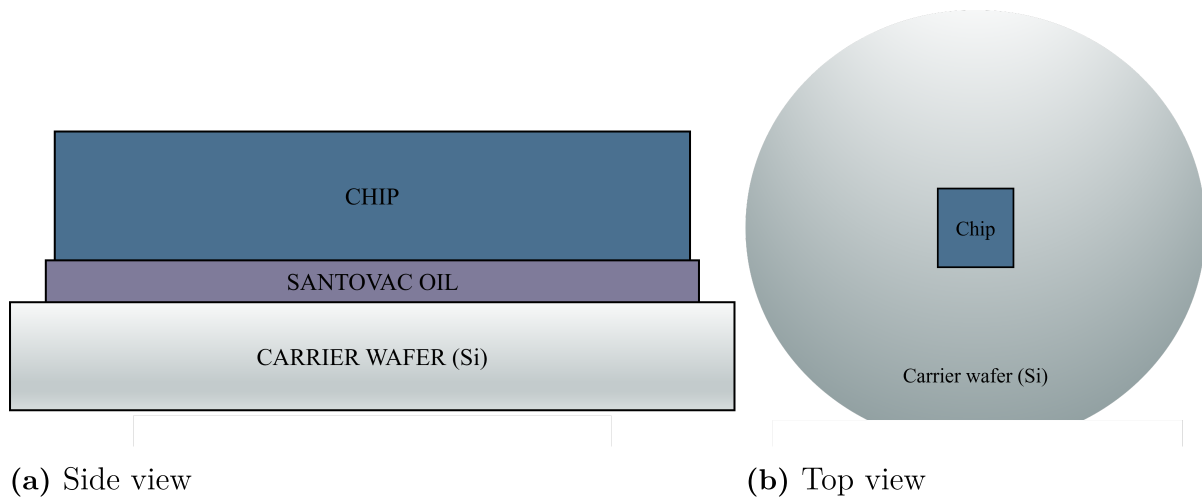
Fabrication of etch samples

The different epitaxial layer stacks were grown by molecular-beam epitaxy (MBE) on 3-inch InP wafers with a thickness of 635 µm. In order to create smaller samples for the process development and not to use up the whole wafer all at once, the wafers were first diced into smaller samples of 10x10 mm size. After dicing, organic contaminants and other residues were removed by oxygen plasma ashing and by sequential immersion in acetone and isopropanol (IPA) baths. A lift-off procedure was then carried out to define the top contact metal as well as a hard mask on the chips. For this purpose, a Raith EBPG 5200 electron-beam lithography system was used to write the desired pattern into a bi-layer resist of MMA and PMMA that was spin-coated on the chips. Development was carried out in an IPA:DI water solution and any residual resist after development was removed by a short oxygen plasma ashing step. By exploiting the higher sensitivity of MMA relative to PMMA, a resist profile with an undercut was obtained, enabling lift-off of subsequently deposited metals. For the deposition of the metal layer stacks, depending on availability, one of two different electron-beam metal evaporation tools were used, either a Kurt J. Lesker Spectros or a more modern Kurt J. Lesker PVD 225. The first three layers Ti/Pd/Au are deposited with thicknesses of 20/20/75 nm, which is then followed by a hard mask of either Ni or Cr. After the metal has visually separated from the chip during lift-off, it's moved to a fresh acetone batch, followed by a IPA bath to remove any

acetone residuals, and finally blown dryed with nitrogen. A metal stack now remains on the chip in the pattern defined during the E-beam exposure. If there if no intention to perform further fabrication with a chip after etching, these are scribed into smaller 5x5 mm pieces to conserve material.

Etching process

For this project a Oxford PlasmaPro 100 tool is used for etching. The samples are mounted in the centre of a 3-inch Si wafer with a small drop of santovac oil as seen in figure 3.2.



(a) Side view

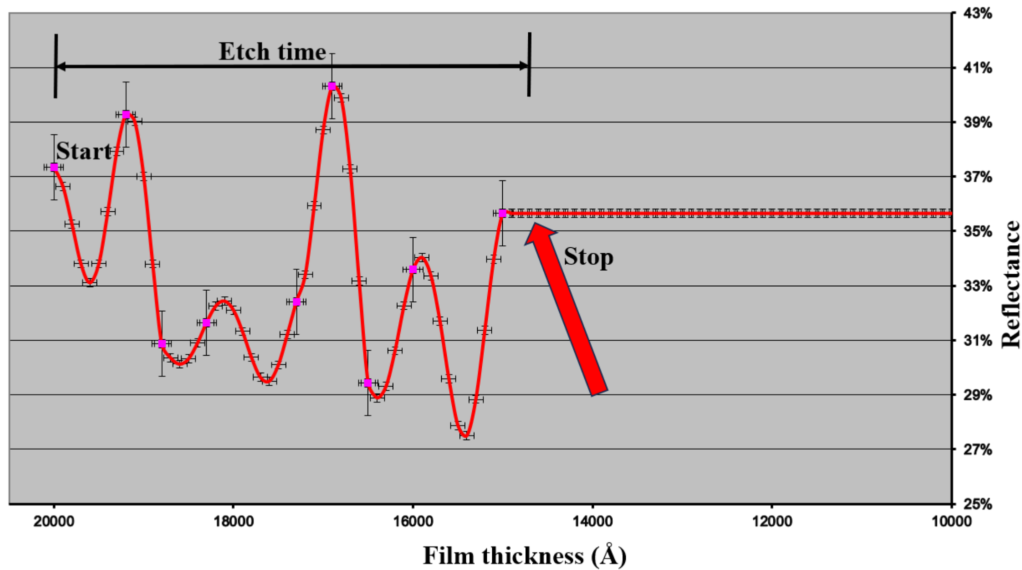
(b) Top view

Figure 3.2: Schematic illustrating chip mounting on carrier wafer (a) from the side (b) from the top.

The santovac oil provides adhesion to the wafer but also improves thermal conductivity so that heat built up during etching can efficiently escape through the carrier. In order to remove organic contaminations and other particles that may create micromasking during the etching process, an additional sequence of oxygen plasma ashing and acetone and IPA bathes is carried out, where ashing is conveniently done with the sample mounted on the carrier. Additionally, before each session a 2-3 minute etch of a sample with the same material is performed to pre-condition the chamber. The Oxford PlasmaPro 100 tool features a load-lock in which the carrier-wafer is placed and automatically transferred to the chamber where it is clamped in place. The wafer is then left to thermalize on the plate for three minutes before the plasma is ignited and etching starts. During this step the tool applies parameter values specified in the recipe. For etching at lower pressures where it's not possible to ignite the plasma due to the low density of particles, a 'strike phase' is incorporated in the recipe. In this case the first seconds of etching is done at a higher pressure, and after the plasma has stabilized the pressure is pumped down. Furthermore, In order to know when to stop the process a so called end point detections is performed. This technique measures reflectance with a laser interferometer which is compared to a

calculated model for the corresponding layer stack, where the user has identified which point in the model correspond to the desired etch depth. The process is then manually stopped when measured signal reaches this point. An example of such measurement and calculated model for a double stack FMBD is displayed in Figure 3.3.

(a) Measured reflectance



(b) Calculated reflectance model

Figure 3.3: The measured reflectance of a FMBD-D layer stack during etching and corresponding calculated reflectance model

For FMBD chips the point where signal derivative is equal to zero was chosen, which corresponds to a stop 30 nm into the bottom contact. Models of reflectance curves for FMBD, RTD and HBV heterostructures and their corresponding stop points can be found in appendix A. When etching is done, the wafer is unloaded and the sample is removed from the carrier by carefully applying force from the side with a tweezer. It is then immediately rinsed in DI, and thereafter IPA, to remove any $NiBr_X$ residue which might be left on the surface [5].

3.2 Measurements

3.2.1 Scanning electron microscopy

To evaluate the effects of etch parameters after every iteration this project have used scanning electron microscopy (SEM). Three SEMs; Zeiss Gemini 560, Zeiss Sigma 360 and Zeiss Supra 60 has been utilized throughout this project, with the Zeiss Sigma 360 accounting for most images featured in this thesis. A 5 keV electron energy is used in general, with samples mostly examined at an angle relative the gun of 45, 60, 80, or 90 degrees. This allows for evaluation of etch profile and surface characteristics, as well as size measurements, which are used to calculate the etch rate & selectivity.
To measure the distance with a SEM scan one can use photogrammetry, where the number of pixels between two points is measured and recalculated into distance based on the zoom level, aperture, etc. This calculation is integrated to the SEM software, so to get the real distance between two points one only needs to recalculate for the perspective. Although this approach is less precise compared to what is possible with other tools, mainly because where one layer starts and ends can be hard to precisely define, as well as being limited by scan resolution. The error is approximated to be about 15% for mask measurements, which limits the accuracy of later etch rate and selectivity calculations, but should have a relatively small effect on overall trends when comparing results. Taking into account the overall reduction in measurement complexity and time, this method was deemed a reasonable compromise given the time-frame of the project.

3.2.2 Etch rate and selectivity calculations

Metal-stack thickness and structure height is derived from SEM images taken at an angle of 80 degrees with a fixed zoom level of 70KX. Since the and metal thickness before etching is known, the thickness of remaining mask can be derived from measuring the metal stack height after etching. Ideally the mask thickness would be measured instead, but as the interface between Ti-layer and semiconductor is clearly identifiable by a dark line, this was deemed more reliable. Combined with the time it took to etch the measured chip, etch rate can be calculated with the following equation:

$$ER_{SC,M} = \frac{H_{SC,M}(t=0) - H_{SC,M}(t)}{t} \tag{3.1}$$

Where ER is the etch rate, where SC refer to the semiconductor material, and M the hard mask. H is measured height, and t is the etch-time. Furthermore from calculating ER for both the semiconductor and mask, selectivity S, can be calculated by

$$S = \frac{ER_{SC}}{ER_M} \tag{3.2}$$

3.2.2.1 Energy dispersive X-ray spectroscopy

The Zeis Supra 60 tool also features a IXRF energy dispersive X-ray spectroscopy (EDX) unit, which is used to gather data about material composition. During this measurement the electrons are accelerated by 20 keV, and the aperture is set to the largest value available. The EDX then detects emitted x-rays in the area the SEM is focused on, where X-rays may be emitted from up to a depth of 1-1.5um, with a detection resolution of 133eV. The number of x-rays emission and corresponding energy is counted over 60 seconds to generate the EDX spectrum, and by defining which elements are present in the material, the software normalises the data and computes the atomic composition.

3.2.3 Electrical measurements

In order to evaluate if a set of certain process parameter values is also suitable for use in real device fabrication, electrical properties of a diode fabricated with the final recipe has to be measured and compared to what is expected from the material. The most common method for this, and the approach taken in this project, is to measure the I-V (and C-V) characteristics. For this a probing setup was used, with one probe placed on the top contact of the diode (anode) and the other placed on a gold cathode deposited onto the sample after etching. A sweep over a range of voltages is performed and current or capacitance is measured plot the corresponding I-V or C-V plots.

3.3 Workflow

By adopting an iterative workflow, illustrated in Fig. 3.4, in which steps towards process prioritized over the isolation of individual process parameters, the project was able to balance the two objectives without exceeding the available time frame. This approach also enabled the timely delivery of a functional etching recipe to continue with real device fabrication. However, this approach also limited the amount of data that could be collected relating to each parameter.

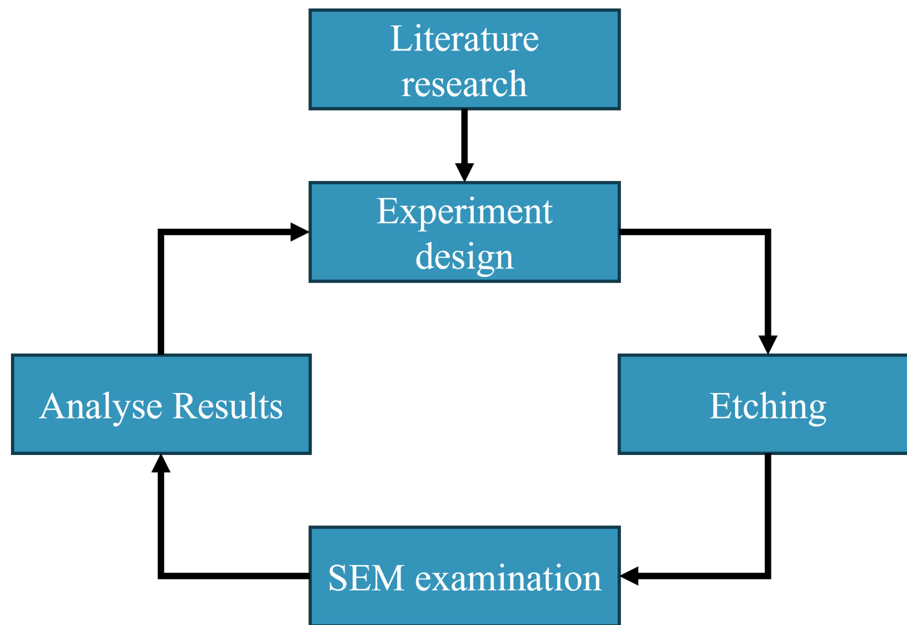


Figure 3.4: Project workflow illustration.

The first step in each iteration was to determine which process parameters would be varied in the subsequent etching session. These variations were selected based on previous SEM observations as well as relevant literature. While some experiments focused on evaluating the influence of individual parameters through single-variable variation, others involved simultaneous modification of multiple parameters to further optimize the etching recipe. Multiple chips processed with different recipes were then etched within a single session, as described previously. In the following step, the etched samples were examined using SEM, and the results were documented alongside other measurements in an Excel spreadsheet. The iteration cycle was repeated until a recipe that etched vertical sidewalls with minimal damage was found.

4

Results and discussion

4.1 Optimized process recipe

This section presents the etching recipe that will be used for future device fabrication. This recipe is the outcome of the development and optimization workflow described in the previous sections and is presented in Table 4.1, along with measured V_{dc} bias, etch rate and selectivity towards a nickel hard mask.

Parameter:	Value:
Pressure	0.3 mTorr
Temperature	150 °C
ICP power	800 W
RF power	100 W
HBr flow rate	9 sccm
V_{dc} bias	163-165 V
Etch rate	241-257 nm/min
Selectivity SC : Ni	12 : 1

Table 4.1: Optimized recipe parameters and the resulting V_{dc} bias, etch rate, and selectivity for etching a 25 mm^2 test sample.

Where a gas flow rate of 13 sccm is applied when etching larger 100 mm^2 chips. This is done to account for the loading effect which consumes reactants at a higher rate. The etch rate is slow enough to maintain control over etch depth with the endpoint detection. Selectivity towards Ni is high enough to function as a hard mask, and the measured V_{dc} bias is of similar magnitude as for that of other papers [21]. During development, pressure and temperature was found to be the most important parameters for achieving the desired profile, with HBr flow rate, as well as ICP and RF powers having a larger process window.

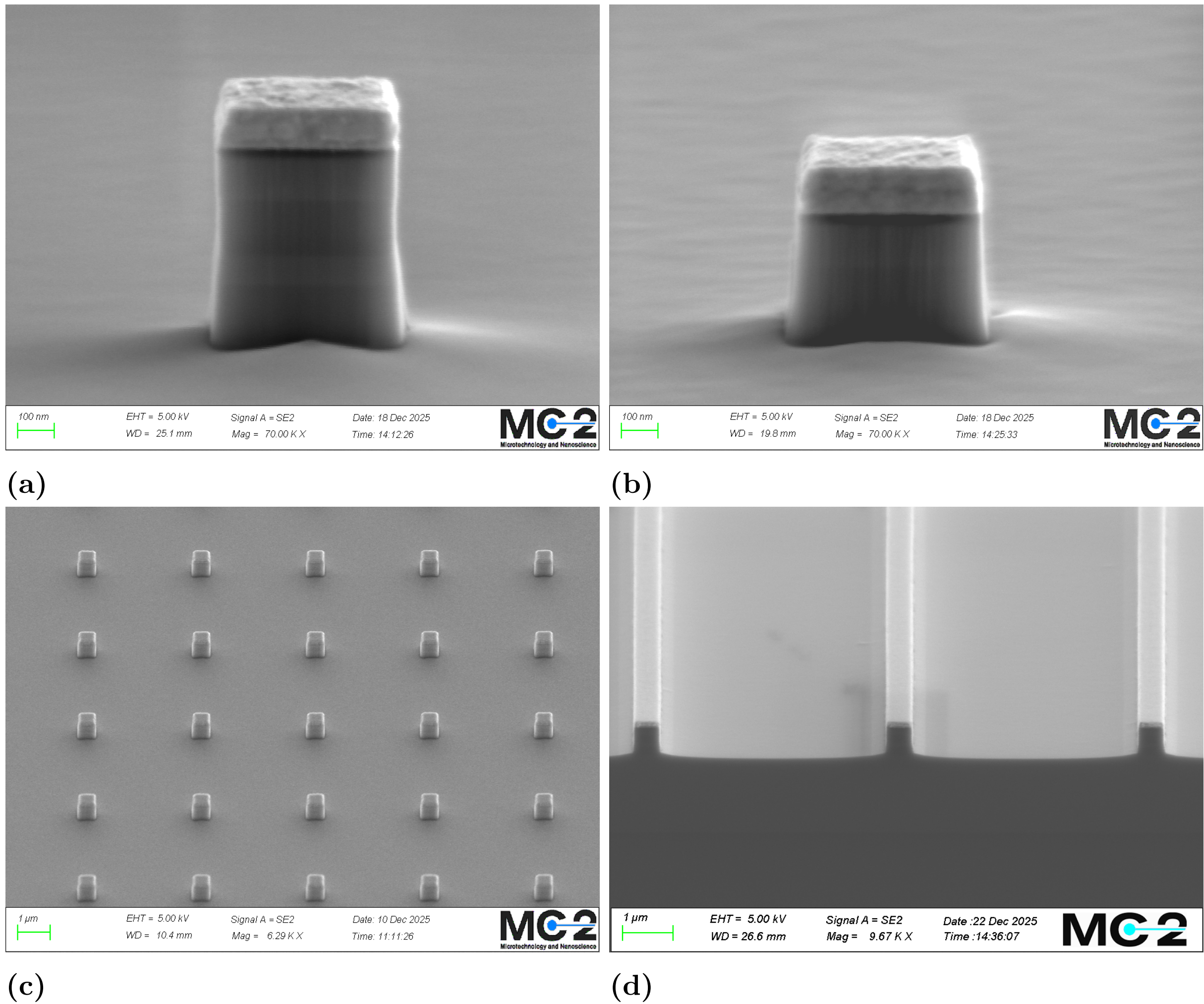


Figure 4.1: SEM images of structures etched with the optimized process recipe. Where (a & c) show 0.25 µm^2 FMBD-D anodes, (b) 0.25 µm^2 FMBD-S anode, (d) 0.5 µm wide FMBD-D gratings.

As seen in figure 4.1, the optimized recipe consistently produces small anodes with vertical sidewalls for both single and double FMBD layer-stacks. The sidewalls and overall surfaces are smooth with little to no etch induced damage. Figure 4.1c show the consistency of mesa profile, size and surface. For anodes of both layer stacks (fig 4.1a&4.1b), a very slight trenching is present along with slight footing at the middle of each side, and in figure 4.1d footing is seen to be no more than the width of the mesa. Both of these defects are common even for well optimized dry etch processes and should have minimal effect on device performance.

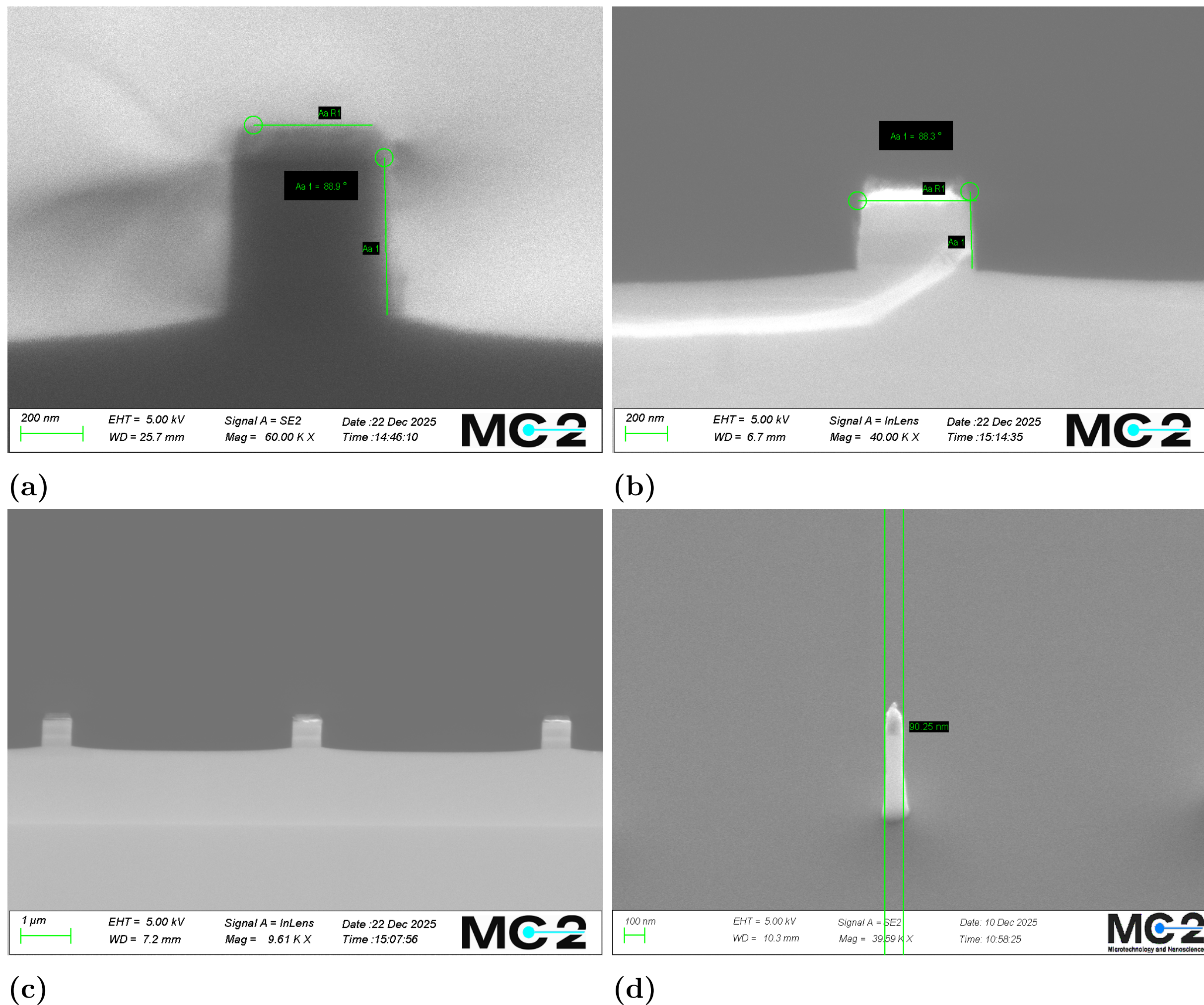


Figure 4.2: SEM images of scribed FMBD gratings etched using the optimized process recipe and viewed from the side. Where (a & c) show a sidewalls estimated to 88.9 degrees (FMBD-D) (b) 88.3 degrees (FMBD-S). (d) A 0.0081 μm^2 FMBD-D anode

Furthermore, figure 4.2 show scribed gratings where the sidewall angle is estimated to 88.9 degrees for a double layer (fig 4.2a & 4.2c), and 88.3 degrees for a single layer (fig 4.2b), which is both considered very high. Additionally, figure 4.2d show the smallest lateral dimensions 0.0081 μm^2, that a anode that could be reliably etched in the FMBD-D layer stack.

4.1.1 Hard mask materials

During the project three different metals, nickel (Ni), chromium (Cr) and titanium (Ti) were evaluated as a hard mask materials. Among these, titanium showed early in the process to etch away relatively fast by HBr, and were excluded from further testing at an early stage in the project. For Nickel and Chromium, etching was slow enough with a HBr-based process to be considered a good hard mask material, with corresponding etch results presented bellow in figure 4.3

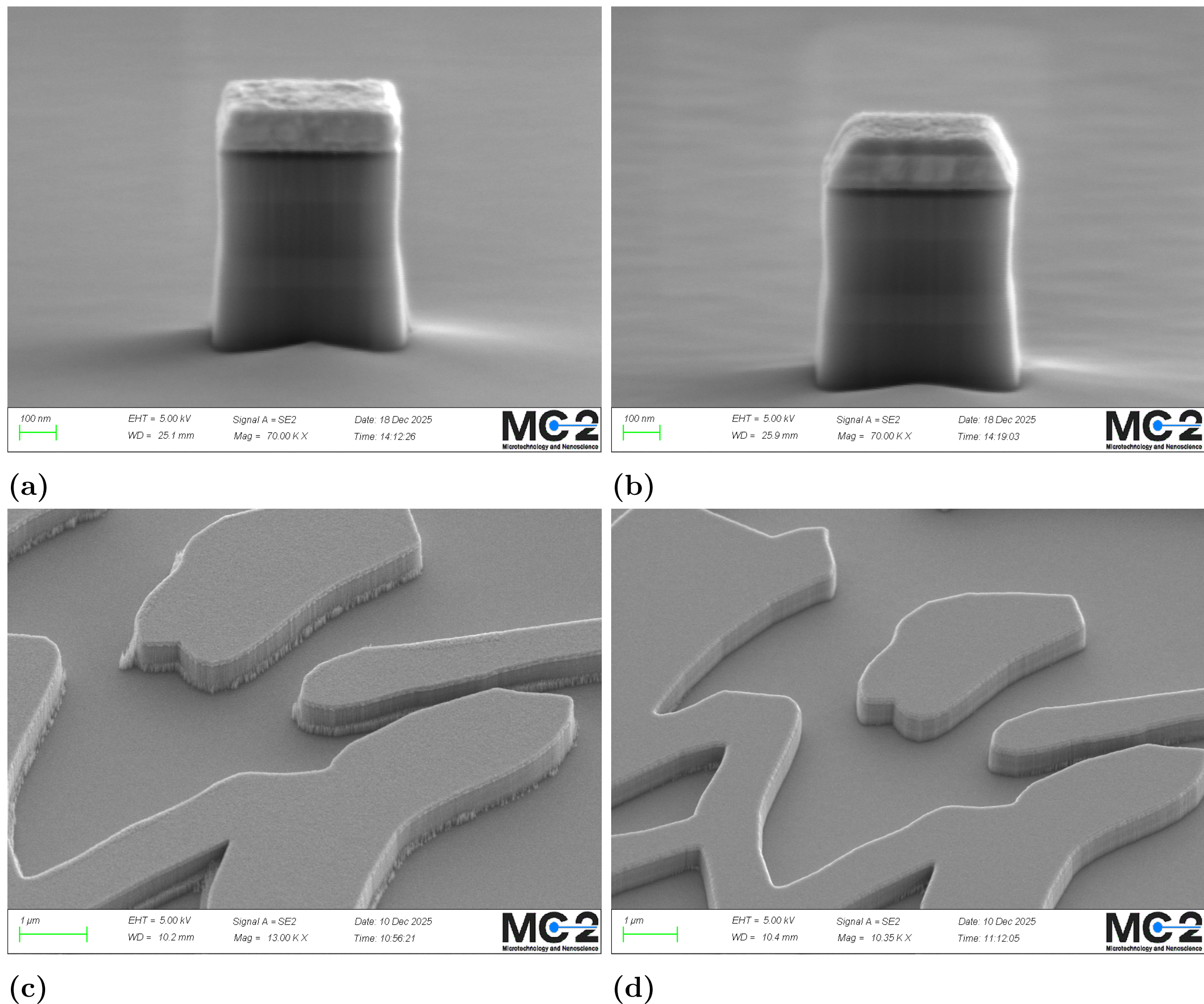
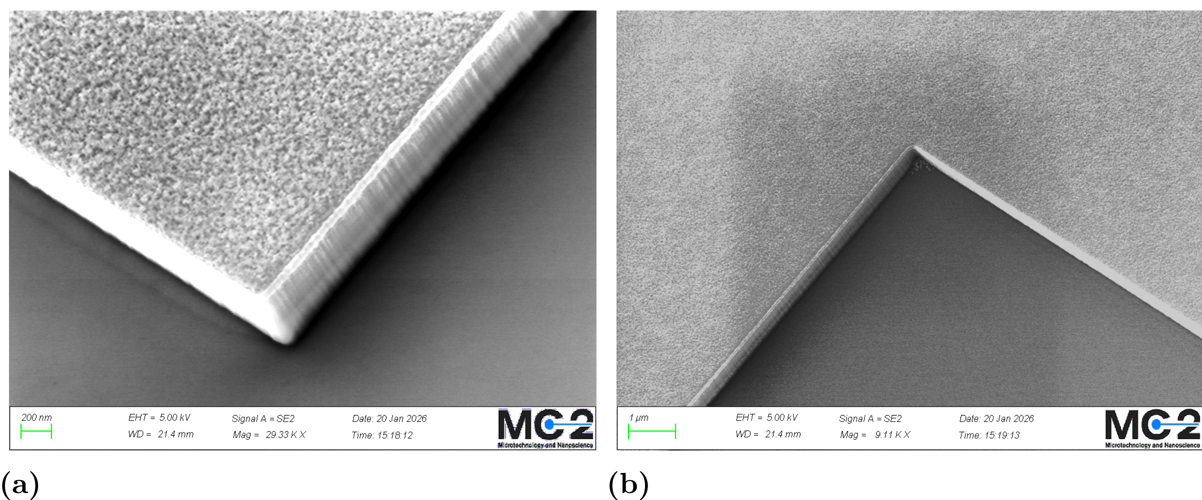


Figure 4.3: SEM images of 0.25 µm^2. FMBD-D anodes etched with hard mask material (a) Ni, (b) Cr and larger FMBD-D structures (c) Ni, (d) Cr.

Figure 4.3 show a double-FMBD substrate etched using the optimized recipe with a nickel (fig 4.3a) and a chromium (fig 4.3b) hard mask. As mentioned in chapter 3, both samples had 60 nm hard mask before etching. After etching the nickel-masked FMBD-D for 2 minutes and 14 seconds, approximately 15 nm nickel remained. For 2 minutes and 6 seconds of etching a chromium masked FMBD-D , 35 nm Cr remained. The selectivity towards the semiconductor (SC) for etch with the final recipe is therefore 12:1 for Ni and 22:1 for Cr, which for both materials is acceptable for etching structures of this height. Although, chromium is superior as a 60 nm Cr-mask would suffice for a etch to the depth of 1.3 µm, Ni is still advantageous because of it's superior conductivity in the case that mask remains after etching. As for the effect on resulting sidewall profile and surface, the small 500 nm wide structures shown in figure 4.3 are very similar and considered identical. While in figure 4.3c & 4.3d, which show larger and more complex shapes close together, a grass-like texture is visible on or close to the sidewalls of the Nickel sample. With this in mind, observe that the profile of metal stacks differ somewhat after etching

in figure 4.3a & 4.3b, where the Ni-stack has a near vertical profile and the Cr-stack is slightly sloped. After the deposition of the metal layers both of these should have had a slightly sloped profile. That the Ni-stack has more vertical sides after etch is somewhat characteristic to the mask pull-back defect described by T. Burman in his PhD thesis [10]. The grass-like texture on sidewalls is therefore concluded to be a result of mask failure near edges. Although, the resulting damage can be limited by adjusting process parameters, the mask pull-back issue itself is result of a issue with metal deposition [10]. In our case, the mask pullback issue was found to be related to which evaporator tool was used for metal deposition, and not hard mask material. As in the later tests shown in figure 4.4, a nickel mask deposited using the same tool as the sample in figure 4.3d, does not have the same problem.



(a) (b)

Figure 4.4: SEM images of (a) the protruding corner (b) the recessed corner, of a larger FMBD-S structure etched with a Ni hard mask deposited with the Lesker PVD tool

Why the edges of a Ni mask deposited with the Lesker Spectros tool 'pull-back' during etching is not yet understood. The current theory is that there is something with the deposition speed and/or temperature in the Lesker Spectros that causes differences in granularity which weakens sides of the mask. Though, this requires further investigation to be fully understood, and for future device fabrication, the Lesker PVD tool is strongly recommended. Nevertheless, nickel were adapted as the primary mask choice in this project, due to it's advantage as a conductor relative chromium, which in this case, is more advantageous than a higher selectivity. However, a combination of these where a Cr layer is deposited on top of the Ni could be optimal. Where for example, a 20/15 nm Cr/Ni mask for the FMBD-D, would reduce the overall mask thickness to 35 nm, and benefit from nickels conductive properties after the Cr layer is etched away.

4.1.2 EDX measurements

The EDX measurements done in this project proved to be quite unreliable due to factors such as the depth from which X-rays are emitted and the degree these gets absorbed by other layers. Though, results might still provide some insight into potential issues that require further research and analysis by more suitable tools. Two EDX measurements performed on the bottom contact near a etched anode is presented in table 4.2, where figure 4.5 displayed the EDX spectrum for Surface 1.

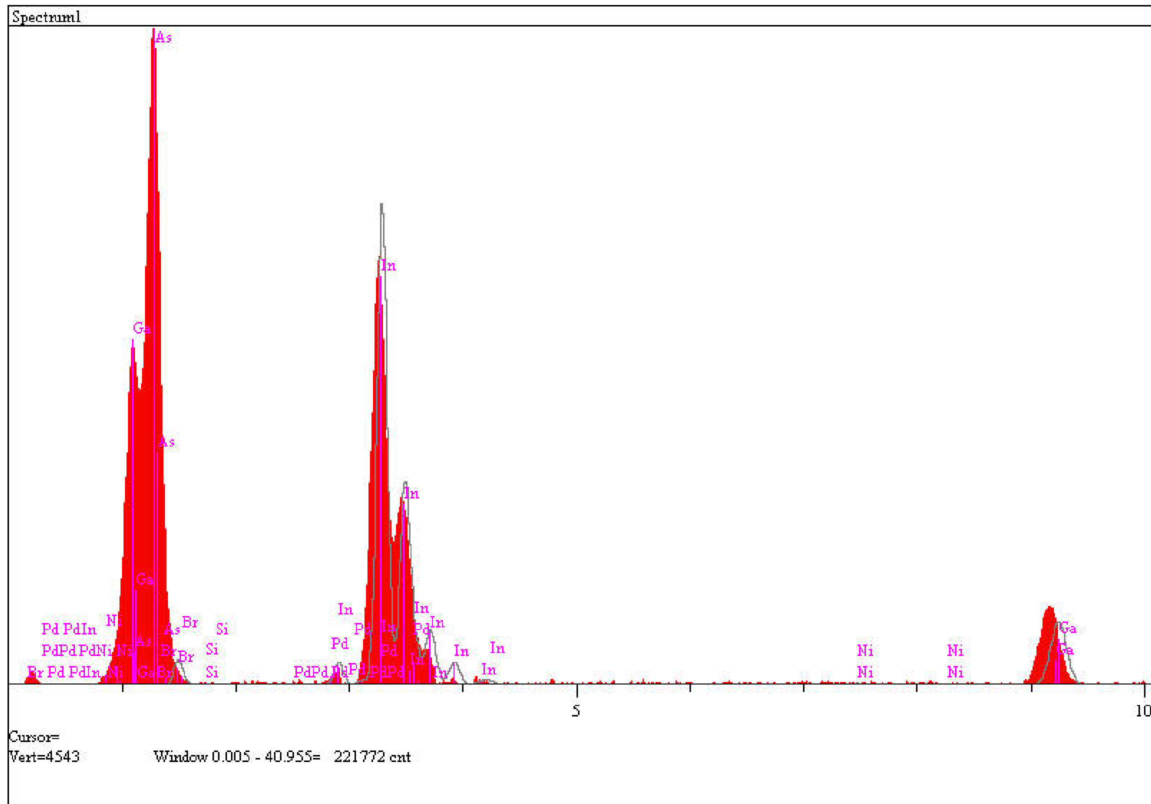


Figure 4.5: EDX spectrum of a measurement performed on the bottom contact near a FMBD-D anode.

	In	P	Ga	As	Br	Si	Ti	Pd	Au	Ni
Surface 1	53.905	*0.295*	15.927	26.121	*0.000*	*0.506*	*0.336*	*0.214*	2.260	*0.437*
Surface 2	57.472	*0.328*	14.499	23.384	*0.000*	*0.266*	*0.457*	*0.294*	2.988	*0.311*

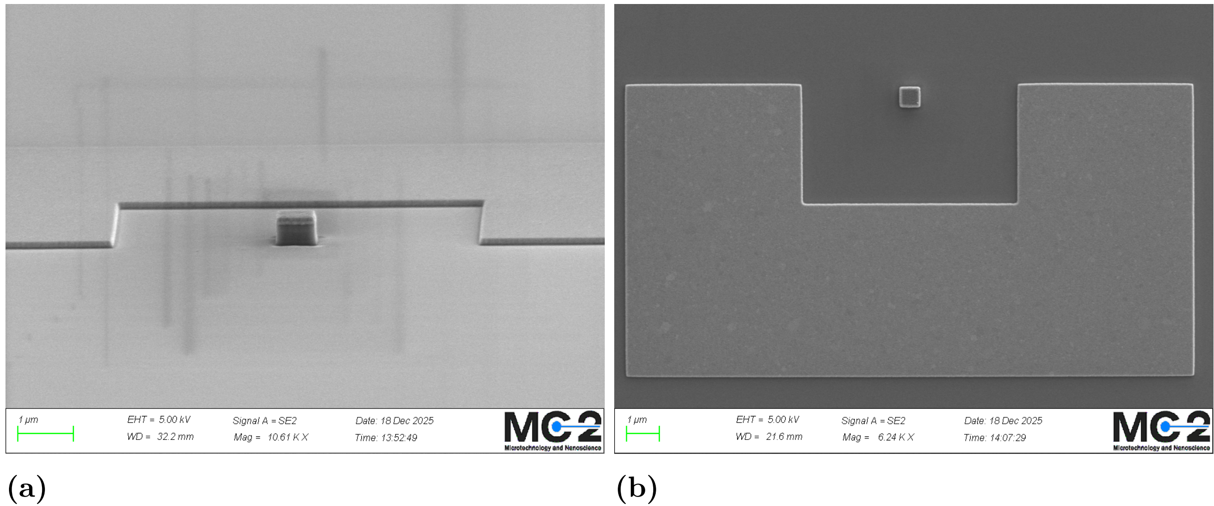
Table 4.2: Atomic compositions measured by EDX on the bottom contact near a FMBD-D anode. Where cursive values indicate a error equal or larger than the measurement.

The In content was significantly higher than the sum of P and Ga, these elements should exhibit the same ratio as $In_{0.53}Ga_{0.47}As$ at about 1:1:2 and InP is 1:1. The high In content may result from InP substrate, but the but the low phosphorus content contradicts this.

The high detected indium content could also indicate that $InBr_X$ by-products are left on the surface, but because the measurement showed 0% Br we can not confidently say if it does or not. The 0% Br measurement is also strange as two peaks in the EDX spectrum is observed to likely come from Br (around 0.3 and 1.5). Another possible explanation is that Ga and As has been etched away far more that In, this would indicate a difference in etch rate between these elements, which was previously observed by S. J. Pearton [22]. However, because this measurement has to many potential issues, the reason for the why such a high indium content is reported can not be fully understood at this time. Furthermore the the Ga:As ratio appeared to be a about 0.63:1 which exceeded than the 0.53:1 specified in $In_{0.53}Ga_{0.47}As$ composition. This may indicate that As is removed more relative Ga, but, again, this cannot be confirmed by this measurement alone. Lastly, traces of gold also appeared to be present, which was surprising because the hard mask covered most of the gold during etching. This result would imply that gold is redeposited during mask pull-back, but the 2.6 % Au content was considered, and could be because of a peak overlap. Nevertheless, these measurements indicate on some properties which would be interesting to investigate further, but is ultimately deemed not suited for this kind of material analysis. If some time was put towards manually defining peaks while using the software this measurement might be improved, for future analyses, a more suitable method such a photoelectron spectroscopy is recommend. Which would provide far more accurate data about the surface composition since X-rays would not be emitted from deep into the sample.

4.1.3 FMBD devices

Although we did not measure any FMBD devices due to their small size. Diodes on 100 mm^2 chips have been etched and some progress towards these measurable devices have been fabricated during the writing of this thesis. The following figure show SEM images of a 0.25 μm^2 FMBD-S anode with the ohmic contact acting as cathode deposited in proximity.



(a) **(b)**

Figure 4.6: SEM images of a 0.25 μm^2 FMBD-S anode with surrounding cathode.

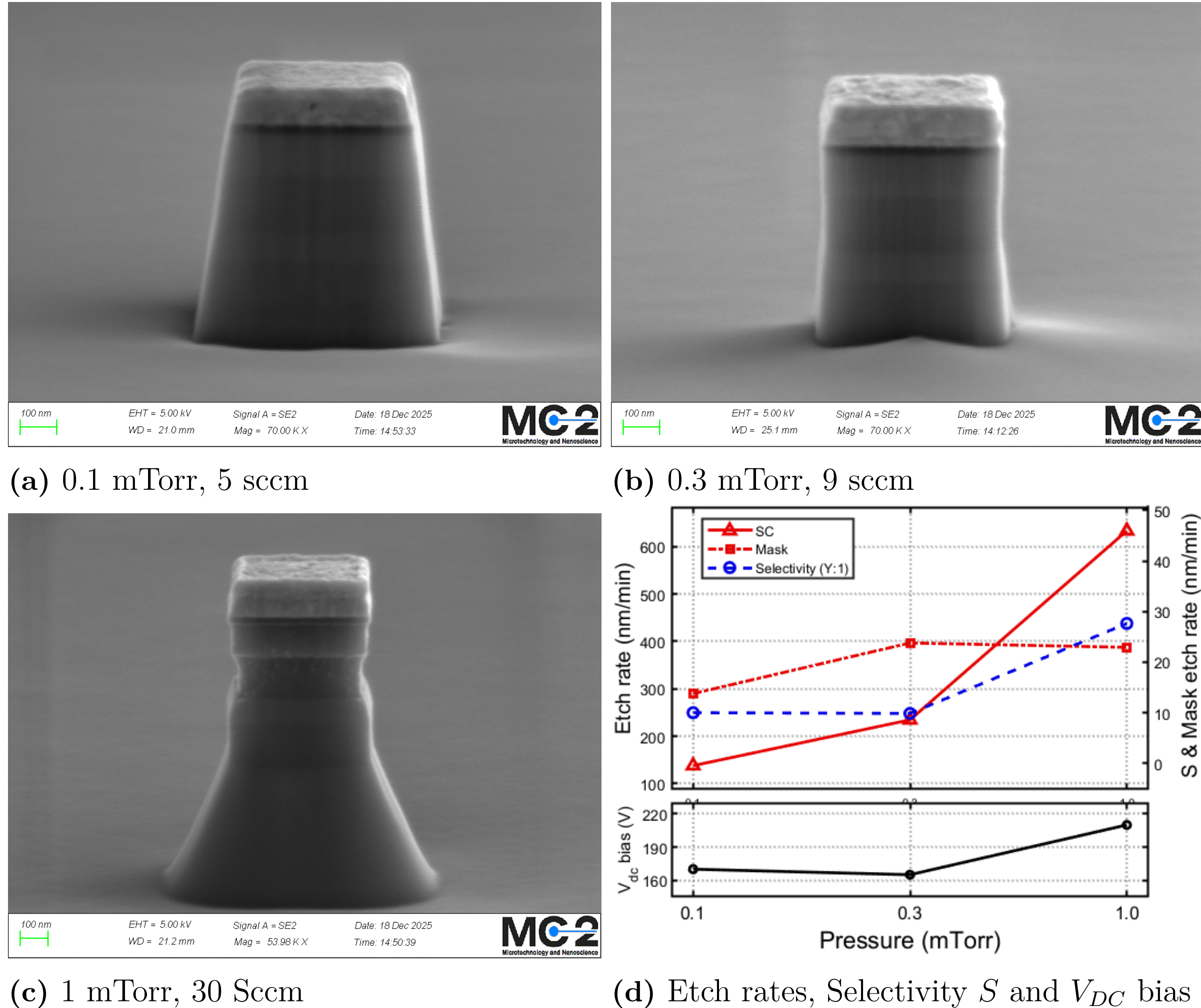
As mentioned earlier, the larger 100 mm^2 chips had flow rate adjusted to 13 sccm to account for the loading effect. With this adjustment, no visible difference is observed relative results presented in the previous sections. Furthermore, the layout seen in figure 4.6 is essentially a functioning device as both anode (metal-stack + hard mask) and cathode is present, which could be measured directly if probing such a small anode were possible. However, until a air-bride has been fabricated to contact the small anode, measurement by probing is not possible.

4.2 Influence of process parameters

This section compiles the experience gained during optimization and development of the recipe by discussing the effects each parameter had on etching characteristics. Observe that all Ni masked results in this section is fabricated with the Lesker spectros and therefore inhibit the mask pull back issue discussed earlier, although resulting damage is dependent on etch parameters.

4.2.1 Pressure

One of the most impactful parameters for overall etch profile was found to be the pressure. For the test results presented in this section, the gas flow rate was adjusted to maintain the same gas residence time between recipes, to study the effect of pressure with minimal change to plasma composition. A comparison of a etch with lower and higher pressure relative the optimized recipe (table 4.1) is presented below. Note that, for the 1 mTorr result, was etched beyond the stop point.



(a) 0.1 mTorr, 5 sccm

(b) 0.3 mTorr, 9 sccm

(c) 1 mTorr, 30 Sccm

(d) Etch rates, Selectivity S and V_{DC} bias

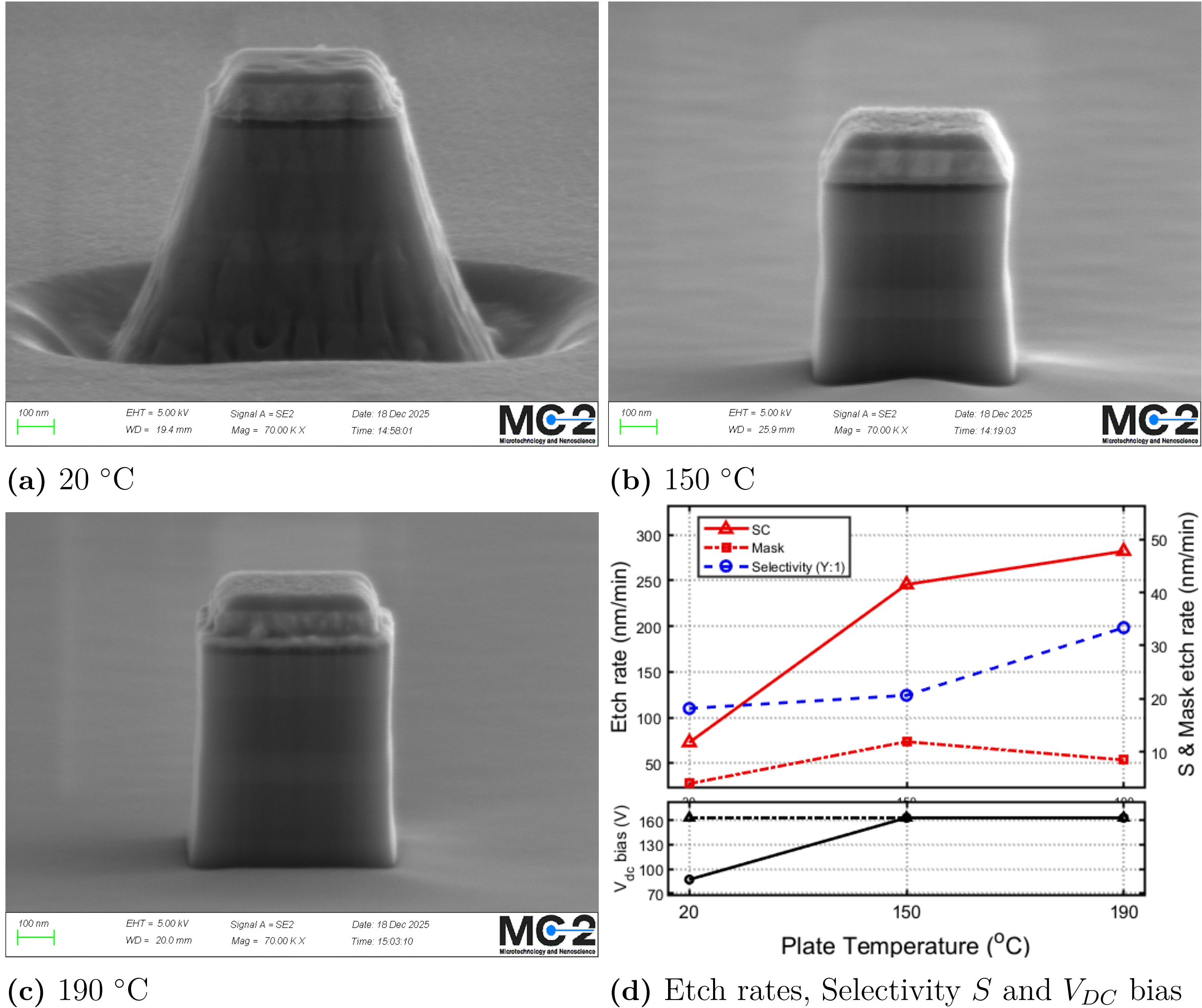
Figure 4.7: SEM images of 0.25 µm² FMBD-D anodes, etched with varying pressure and flow rate. Where 4.7b is the optimized recipe. Images are taken from an 80 degree angle with a magnification of 70K (a & b) and 54K (c). Figure 4.7d show selectivity, estimated etch rates, and measured DC bias in relation to RF-power

The tests displayed in Figure 4.7 demonstrate that, pressure has a significant effect on overall profile. At a pressure of 0.1 mTorr (fig 4.7a) the anode exhibited a sloped, and for 1 mTorr (fig 4.7c) a undercut is observed. An undercut at higher pressures has been well documented in similar studies, and is a result of the ions' mean free path

decreasing [9]. In this case, the undercut appear to have sharp edges at the InP/InGaAs interfaces, and this might indicate InGaAs etching slightly faster than InP, which which may explain why the optimized recipe feature a very small undercut in this layer [22]. At a pressure of 0.1 mTorr (fig 4.7a) the mean free path is increased resulting in greatly reduced lateral etching. This generally benefits high verticality, but because the process includes a mechanism to passivate the surface, some ion assisted horizontal etching appear to be needed for balance. Otherwise sidewalls became over-passivated and cause a sloped profile, which is what is observed in figure 4.7a. The sidewall surfaces does not seem to additional damage from pressure change in this interval. However the more etched InP layer seem to have small brighter spots on the surface, these are likely Indium droplets that could indicate poor desorption of In in relation to Ga and As. As for the surface in general little to no change is observed relative the optimized process. Furthermore, figure 4.7d show semiconductor etch rate to have a almost linear correlation with pressure. This behaviour was expected as the concentration of reactive species at any time is largely dependent on the pressure. However, from previous studies, we know that pressure also effect plasma potential and composition, which in turn effect the amount and ratio of reactive species and ions [23]. That this occurs can be somewhat confirmed as we see a higher V_{dc} bias for 1 mTorr in figure 4.7d, which indicate a decrease in plasma potential, and thus a decrease in the amount of ions generated in the plasma. Although, if the amount of ions was a crucial property, the etch rate would not increase as much as it does, indicating that the amount of radicals is a more limiting factor in this case. The selectivity is improved at higher pressures where it's estimated to be around 26:1, and etch rate of Ni in this case is 26 nm/min while etch rate for semiconductor is about 650 nm/min. This is again characteristic for a process limited by the amount of radicals, as mask etching is generally more dependent on the kinetic energy of ions which becomes lower as pressure increases. For lower pressures, ions should have more kinetic energy, and thus cause etch the mask more. This is not observed for 0.1 mTorr, as mask etch rate instead drops, which could indicate that mask etch rate also has become limited by the amount of radicals.

4.2.2 Temperature

This section outlines the effect of plate temperature relative to the optimized recipe. For these tests a 60 nm Chromium mask was used instead of 60 nm Nickel, otherwise all other material properties are the same as the double-FMBD stack used in section 4.2.1. Also note that for the chip etched at 20°C, a lower RF power of 50W was applied. A comparison of etch results for process recipes with a lower and higher plate temperature relative the optimized recipe (table 4.1) is presented below:



(a) 20 °C

(b) 150 °C

(c) 190 °C

(d) Etch rates, Selectivity S and V_{DC} bias

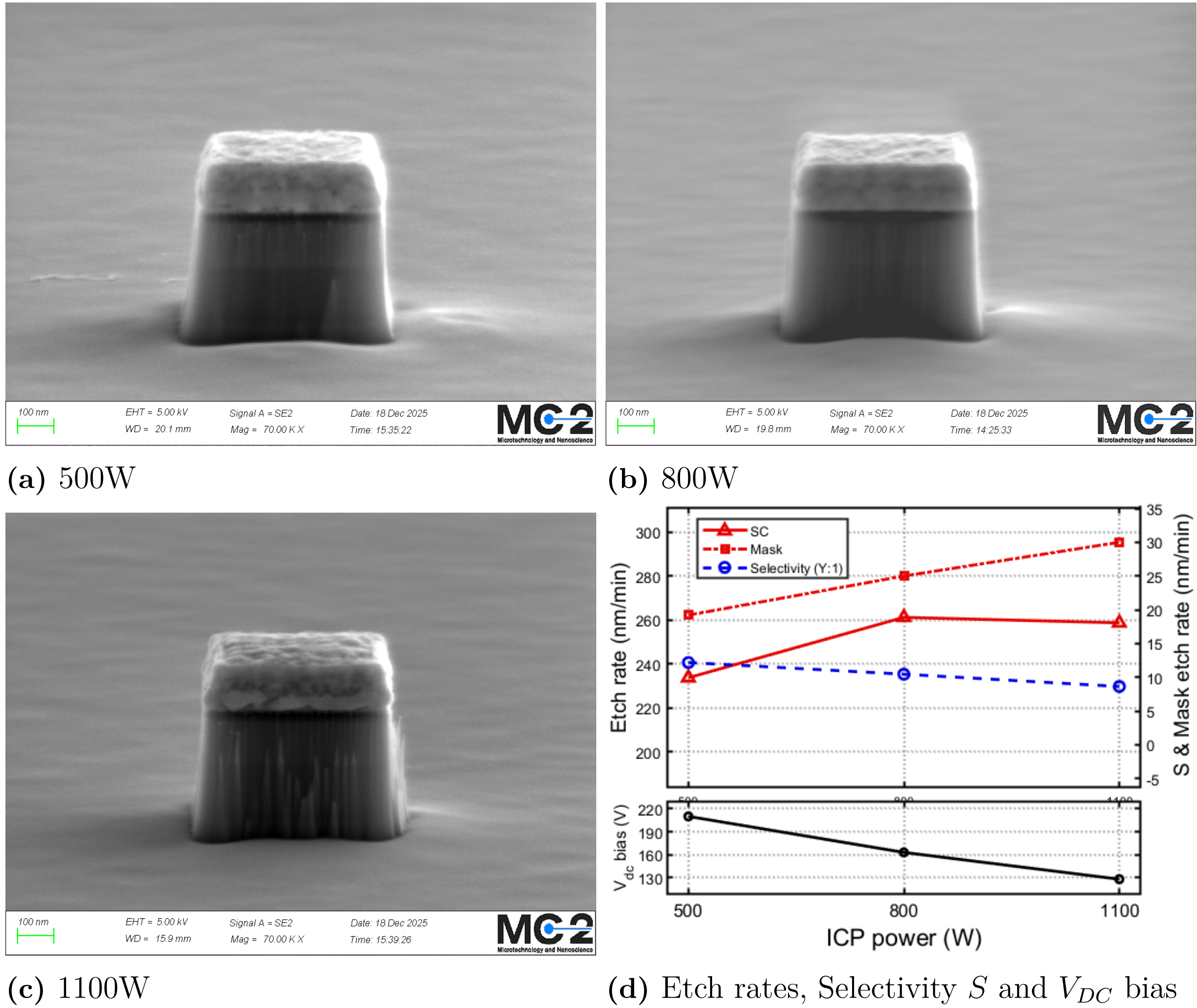
Figure 4.8: SEM images of 0.25 µm² FMBD-D anodes with a Chromium hard-mask, etched with varying plate temperatures. Where 4.8b is the developed recipe. Images are taken from an 80 degree angle with a magnification of 70K. Figure 4.7d show selectivity, estimated etch rates, and measured DC bias in relation to RF-power

For the sample etched at 20°C (fig 4.8a), the anodes have a highly sloped profile with significant trenching, which is a common result of a process with a high degree of passivation. This is because at 20°C $InBr_x$ by-products do not have the volatility to efficiently desorb from the surface, and instead acts as an additional passivation layer [24]. For

the higher plate temperatures, 150°C (fig 4.8b) and 190°C (fig 4.8c), this problem is solved and the profile feature vertical sidewalls. The small undercut in the first dark gray layer when etched at 150°C is seemingly reduced at 190°C. This may be a result of the difference in etch-rates for InGaAs and InP discussed earlier, and increasing the temperature as a means to combat this problem has previously been proposed by in a similar study [22]. Additionally, the footing is significantly reduced at 190°C, which is somewhat unexpected. This would indicate that footing is a result of less assisted reactions, and not only a difference in etchant density on the surface. Furthermore, surfaces of sidewalls and surroundings seems to be relatively smooth. The 20°C result appear to be slightly rougher, and the increased damage at the lower part of sidewalls is a common property of the trenching defect. Lastly, figure 4.8d show that etch rate drastically increases at higher temperatures, which indicate $InBr_x$ by-products being able to dissolve more effectively as temperature is increased. Going from 150°C to 190°C seem to have a small effect on the etch rate, suggesting that temperature is no longer a limiting factor in this range. For 20°C selectivity decreases as the etching of semiconductor material is limited by the additional InBr passivation, while the mask etch-rate remain largely unaffected. When increasing the temperature to 190°C, selectivity is improved as it is seen to benefit semiconductor etch rate but not the mask, which is likely because mask etch rate is more dependent on the physical component of etching. The higher temperature does however seem to cause the sloped outer part of the metal stack to be etched, which is not ideal and could cause further issues as underlying layers are exposed. Examining the V_{dc} bias, the lower value at 20°C is entirely attributed to the lower RF power, and adjusting for this, V_{dc} bias is seen to be constant and therefore unaffected by plate temperature.

4.2.3 ICP power

The ICP-power parameter is directly controlling the field sustaining the inductively coupled plasma, and thus the amount of ion and radicals that are being created. This section will discuss how a change in ICP-power effect etching, by comparing etching with lower and higher powers relative the optimized recipe.



(a) 500W

(b) 800W

(c) 1100W

(d) Etch rates, Selectivity S and V_{DC} bias

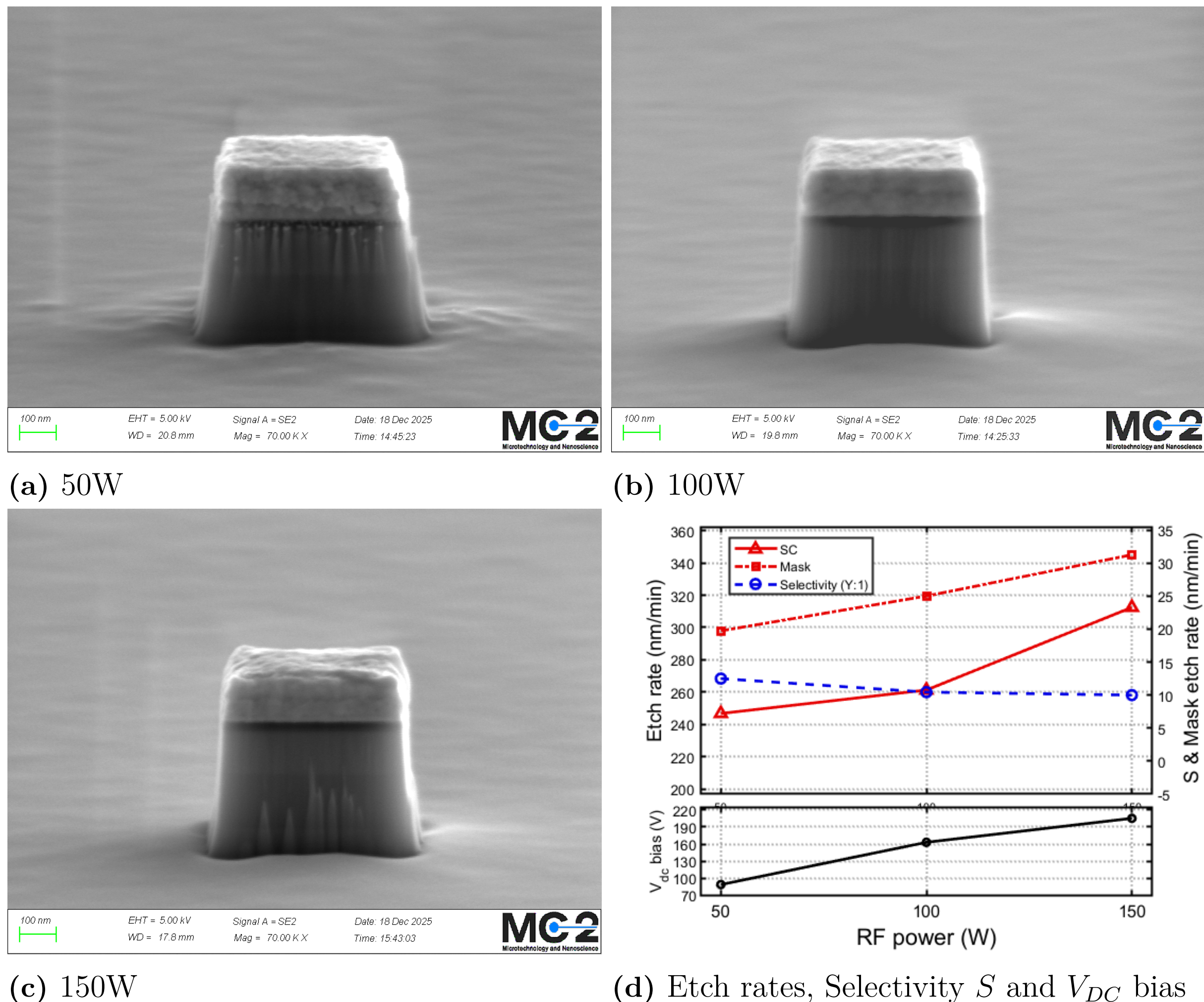
Figure 4.9: SEM images of 0.25 µm^2 FMBD-S anodes, etched with varying ICP-power. Where 4.9b is the optimized recipe. Images are taken from an 80 degree angle with a magnification of 70K. Figure 4.9d show selectivity, estimated etch rates, and measured DC bias in relation to RF-power

Results presented in 4.9 show no apparent effect on the mesa profile as a result of ICP power. But the sidewall texture for the anode fabricated at 1100 W (fig 4.9c) appear to have more damage related to mask pull-back, relative to tests at 500 (fig 4.9a) and 800 W (fig 4.9b. An increase in ICP-power generally means a higher degree of ionization, and that more ions are impacting the surface, which would explain the increased damage. This is reflected in the figure 4.9d as larger plasma potential would causes a the V_{DC} bias to be lower. Moreover, etch rate increases when the ICP power goes from 500 to 800 W, and at 1100 W the etch rate increase is reduced. This aligns with the saturation behaviour discussed in earlier papers, which would indicate that over 800 W, the etch-rate is becomes more limited by the amount of radicals and not the amount ions which assist reactions [6]. Selectivity has a slight downwards trend as ICP-power increases, and as the mask etch rate does not seem to saturate, it is reasonable to conclude that selectivity

does suffer when ICP-power is surpassed the saturation point.

4.2.4 RF power

RF-power directly effect the field that accelerated ions towards the substrate and the electrode potential. This section will discuss how a change in RF-power effect etching, by comparing a recipes with lower and higher powers relative the optimized recipe.



(a) 50W **(b)** 100W

(c) 150W **(d)** Etch rates, Selectivity S and V_{DC} bias

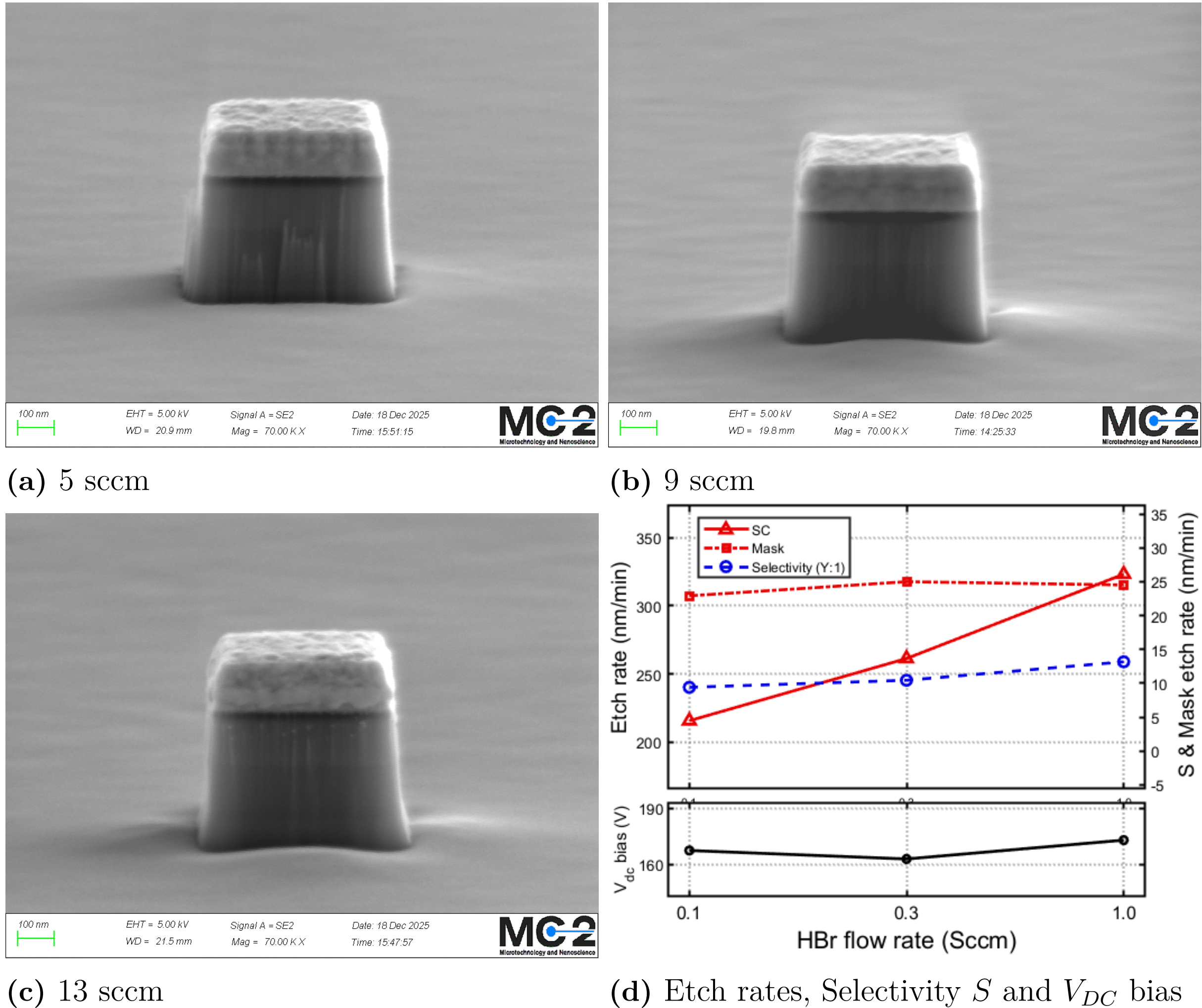
Figure 4.10: SEM images of 0.25 µm^2 FMBD-S anodes, etched with varying RF-power. Where 4.10b is the optimized recipe. Images are taken from an 80 degree angle with a magnification of 70K. Figure 4.10d show selectivity, estimated etch rates, and measured DC bias in relation to RF-power

At 50 W RF-power (fig 4.10a) the profile appear slightly sloped relative the optimized recipe (fig 4.10b).The slope is likely due to ions impacting the sidewall having less energy, and therefore balance is shifted so passivation slightly overpowers lateral etching. For the higher RF-power of 150 W (fig 4.10c) a slight increase in trenching is observed, otherwise the profile seem to be largely uneffected. Sidewall surface, or rather the amount damage

from mask pull-back also appear the be effected by RF-power. For a power of 150 W the sidewall receives more damage due to a increase in physical etching. While 50 W does not seems to be enough for the side to smoothly etch, which would also explain the slight slope. The overall surface also appears slightly rougher for 50 W, which would indicate a reduction to the uniformity when RF-power is lower. Furthermore, figure 4.10d show that both etch rates increase with RF-power, which is a expected outcome as the kinetic energy of ions increases, and likely caused by ions more effectively etching on their own. The selectivity appears to be gradually decreasing, but this trend is weak and within the measurement error so no confident conclusions can be drawn. Although this is expected as RF-power is higher, and likely causes more damage to the mask. Finally, the V_{dc} bias increases since the RF-power directly dedicate the electrode potential. Yet the relation is not completely linear, which could be a indication of the RF-power also having a slight effect on the plasma potential.

4.2.5 Flow-rate

The flow rate decides how mush process gas to feed into the chamber, and in turn how fast gas is pumped out to retain the set pressure. The section discusses the etching outcome as a result of a recipes with lower and higher flow-rates relative the optimized recipe.



(a) 5 sccm

(b) 9 sccm

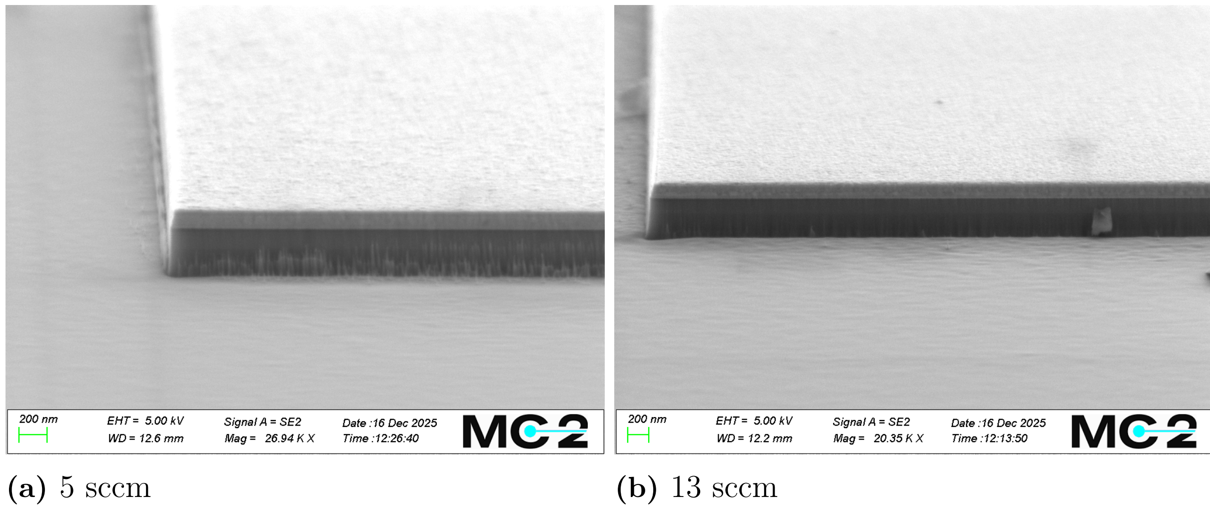
(c) 13 sccm

(d) Etch rates, Selectivity S and V_{DC} bias

Figure 4.11: SEM images of 0.25 µm^2 FMBD-S anodes, etched with varying HBr flow-rate. Where 4.11b is the developed recipe. Images are taken from an 80 degree angle with a magnification of 70K. Figure 4.11d show selectivity, estimated etch rates, and measured DC bias in relation to RF-power

From figure 4.11(a-c) no change to the profile as a result of HBr flow rate is observed. Etch rate (fig 4.11d) appear to increase linearly with flow rate. This is a strong indication that the etch rate is limited by the amount of available reactants (radicals), a conclusion which is further reinforced by the previous discussion about pressure and ICP-power. On the other hand, mask etch rate (fig 4.11d) does not appear to follow the same trend, which is likely due to mask etch rate being more dependent on amount of ions and their kinetic energy, and not so much the amount of available reactants, which is also similar

to the conclusions drawn when discussing pressure. As for V_{dc} bias, a slightly variation is recorded, and this would indicate that flow rate has a small impact on plasma composition and potential. While small, this could bring larger problems if a larger change in flow rate is required. Lastly, sidewall damage due to the mask pull-back appear to be worse for a lower flow-rate, as seen in figure 4.11a. This effect becomes more apparent when examining the larger structures displayed in figure 4.12.



(a) 5 sccm

(b) 13 sccm

Figure 4.12: A larger (625 µm^2) FMBD-S structure etched with (a) 5 sccm (b) 13 sccm.

The sidewall for a large structure etched with 5 sccm (fig 4.12a) have significantly more damage compared to the 13 sccm (fig 4.12b). This clearly shows that the degree of sidewall damage when mask pull-back is occurring is closely tied to flow-rate. The theory is that the ions that impact the surface sputter etch more, relative assisting radical reactions. When flow-rate is lower, radicals are refreshed less and by-products stay in the chamber for longer, which cause this there to be less radical etching to assist. Therefore, overall etching comes more from a purely physical component, which is harsher and damages the sidewalls more.

4.3 Etch performance for other heterostructures

In order to evaluate the performance of the optimized recipe for other heterostructures than the FMBD, 10x10 mm test samples have been fabricated from the the RTD and HBV layer stacks. These are fabricated using the Lesker PVD, with variations in mask composition and etched depths. For the RTD a 50 nm Ni mask was used, and endpoint detection was used to stop etching 240 nm into the material. The HBV had a combined 50/30 nm Cr/Ni mask as proposed in section 4.1.1 and was etched 1500 nm into the material.

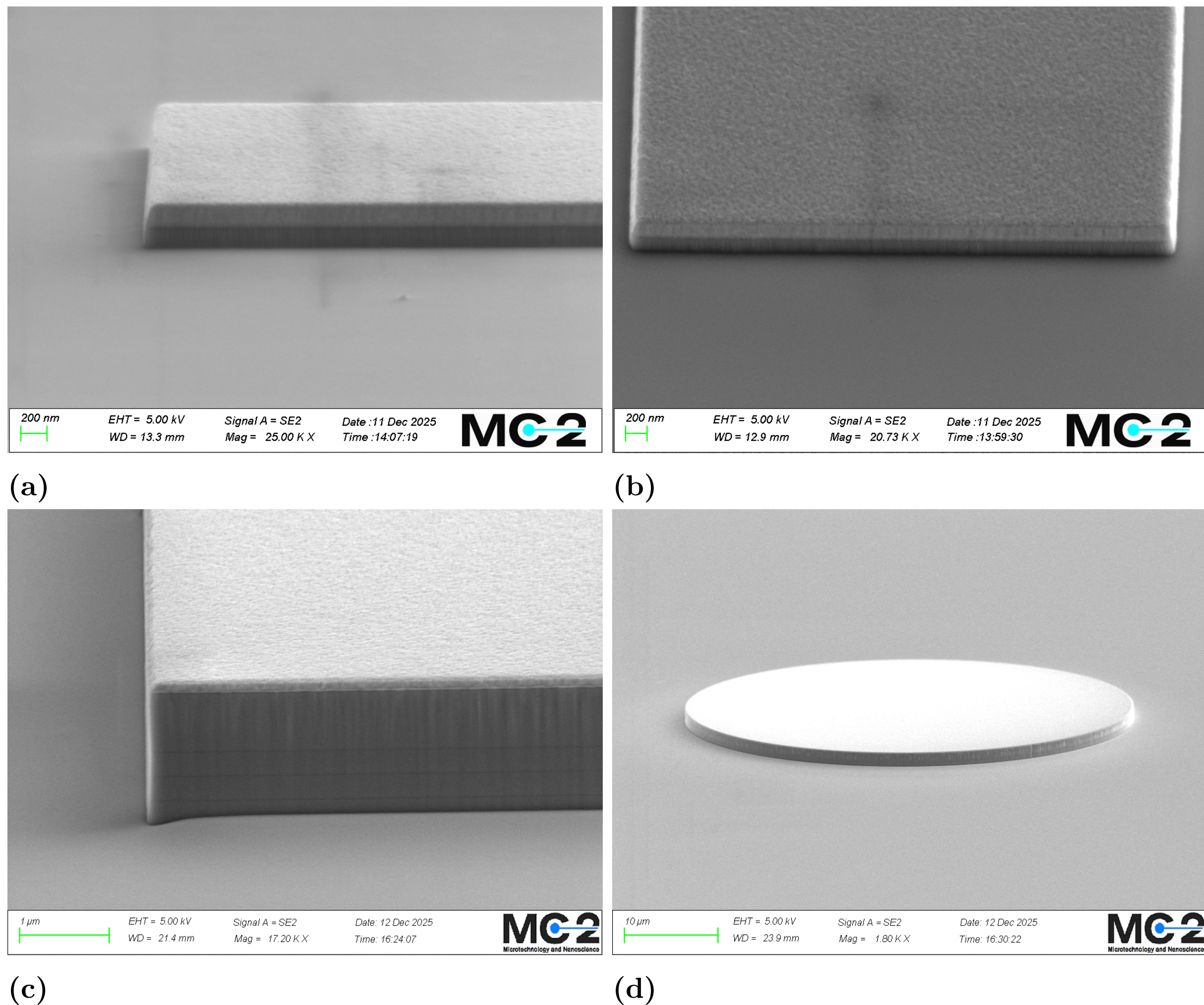
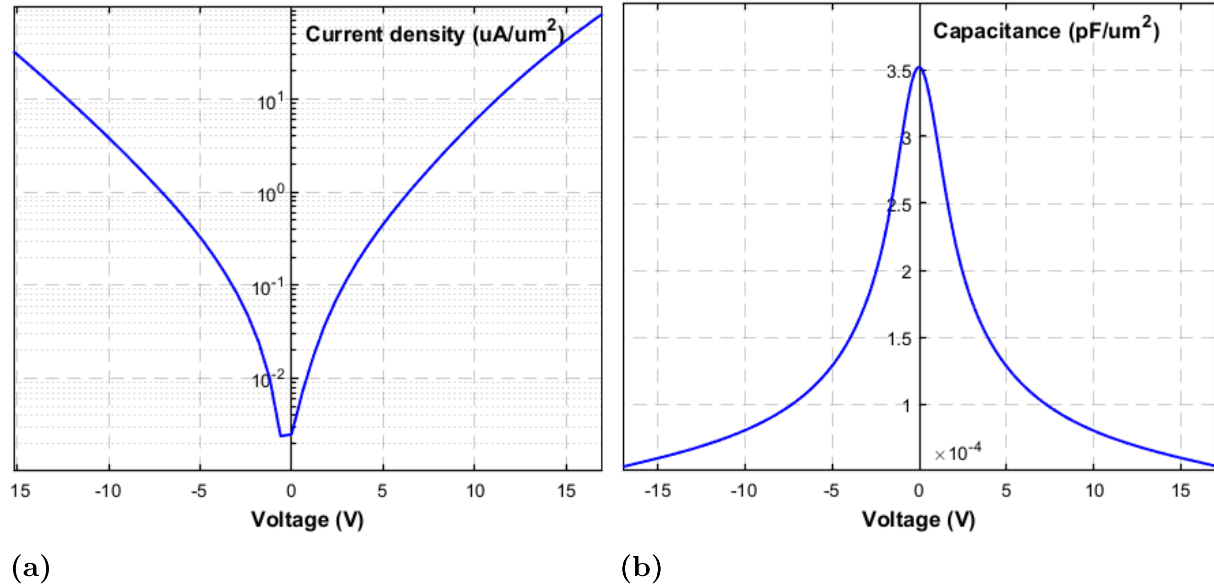


Figure 4.13: SEM images of structures etched in (a & b) RTD, (c & d) HBV -layer stacks using the optimized process recipe.

In figure 4.13, the recipe is observed to have etched both RTD and HBV -layer stacks well. These layer-stacks, unlike the FMBD, does not contain any InP, but this does not appear to have had an impact on overall etch performance, and the etch rate appeared to be the similar to the FMBD. That these has layers containing Al also does not seem to have impacted etching, although these layers could be to thin to cause identifiable issues. With the exception that the HBV appear to have increased footing, likely due to the deeper etch, the etch results appear to have a equally good quality as the FMBDs. Furthermore, in figure 4.13c three dark lines are visible, which are the InAlAs/AlAs barrier layers, and the fact that these are distinguishable is a indication that there is no thick passivation on the sidewalls. Therefore, these results shows that the optimized recipe presented in table 4.1 is not only a viable alternative for etching FMBDs, but also for the RTD and HBV, implying that the recipe is a suitable for InP/InGaAs based heterostructures in general.

4.3.1 Electrical characterisation

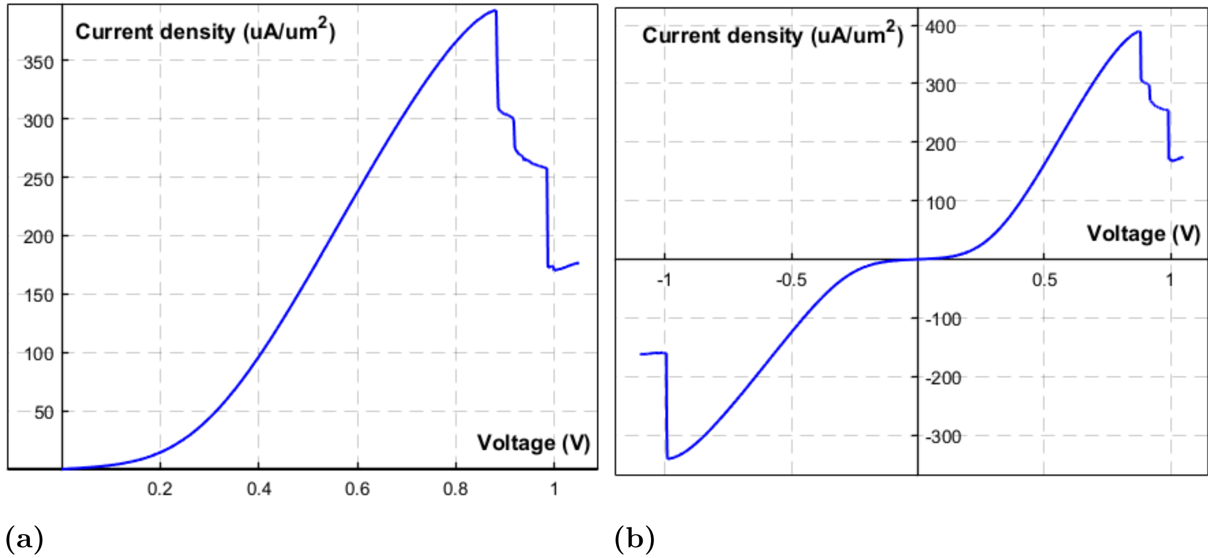
As the HBV does not require a small size in order to show it's characteristics a 180x180 µm HBV diode has been measured, with resulting I-V and C-V data presented below.



(a) **(b)**

Figure 4.14: I–V (a) and C–V (b) measurements for a 625 µm² HBV etched with the optimized process recipe, conducted at room temperature under dark conditions.

The I-V and C-V plots displayed in figure 4.14 show the same characteristics to what is expected form the theoretical curves shown in section 4.3. Even though no claims about performance relative a CH_4-fabricated device has could be made at this time. This is a good sign that the optimized recipe does not inflict excessive damage as it is shown to result in functioning devices, which is ultimately the most important aspect if the recipe is to be used in future device fabrication. Furthermore, fabrication of measurable 1x1 µm RTDs was completed during final stages of writing, with I-V measurements of these shown in figure 4.15.



(a) (b)

Figure 4.15: I-V measurements for a 1 µm^2 RTD fabricated using the optimized recipe, conducted at room temperature under dark conditions.

In figure 4.15, a non-linear I-V behaviour is observed in the region from (-)0.85-0.85 V, along with the current drop in the NDC region thereafter, which matches the characteristic behaviour of an RTD. Compared to the reference measurement (fig 2.6) the NDC region occurs at a lower voltage and the current seems to drop quite sharply and in more defined steps. That the NDC region occur at lower voltage indicate a lower series resistance in the system, which could mean better contact as a result of smoother surfaces. However, the cause of the difference in peak current and the defined steps observed in the NDC region require further investigation. Although, since both RTD and HBV devices fabricated and measured within this project show their respective characteristic behaviour, we conclude that the developed recipe suitable for etching InGaAs-based heterostructures.

5

Conclusions

In this thesis, a novel ICP-RIE dry etching recipe utilizing HBr gas has been developed for etching small (< 1 µm^2) devices with vertical sidewalls in multiple InP/InGaAs-based heterostructures. Sidewall angles are reported as high as 88.9 degrees, and surfaces appear smooth with few observed etch induced defects. Preliminary electric measurements were performed on two different types of devices confirming that the developed etching process yields fully functional devices. During recipe development, process pressure and plate temperature was found the be the most critical parameters, whereas HBr flow-rate, ICP- and RF power having a smaller effect on profile. For the proposed recipe, the etch rate was found to be primarily limited by the availability of reactive radicals, a factor that must be considered when etching larger device areas. Furthermore, both Nickel and Chromium has been demonstrated as suitable alternatives as hard mask materials for HBr-based ICP-RIE etching, and the use of a combined Ni/Cr hard mask is recommended for future device fabrication. The hard mask can be deposited in the same step as the device top-contact metallization, therefore enabling a simplified and self-aligned fabrication process. Additionally, the choice of evaporator used to deposit metal has shown to be be crucial in preventing mask pull-back during etching, which can otherwise lead to significant sidewall damage. Through systemic parameter effect evaluation it was shown that the extent of such damage can be mitigated by carefully adjusting the balance between ion- and radical-driven processes in the plasma. For future research, an extensive study of how etching parameters may affect the electrical properties, as well as a specialized investigation into surface roughness and chemical composition, would be highly valuable. As these aspects are only briefly addressed in this thesis. Indeed, at the time of writing, researchers within the department have already begun applying this recipe in their own fabrication processes, and publications featuring this recipe are anticipated in the near future.

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Appendix A

Fabrication process in detail.

Cleaning	5 min Acetone 70°C, repeat once with fresh acetone 5 min Isopropanol 70°C IPA spray rinse Dry with N_2
Spinning	5 min dehydration bake 170°C **MMA 8.5 EL10:** (400 nm) 60 sec 1500 ms acceleration 3000 rpm 1000 ms deceleration 5 min bake 170°C **PMMA A2:** (70 nm) 60 sec 1500 ms acceleration 3000 rpm 1000 ms deceleration 5 min bake 170°C
Lithography	**Raith EBPG 5200:** Small structures: 1 nA, 380 μC/cm^2, stepsize 0.005 μm
Development	Mix IPA:DI [10:1], stir for 30 sec 30 sec development with gentle stirring 30 sec rinse in beaker with pure IPA Check in microscope If not fully developed repeat procedure with shorter 8-10 sec dips until fully developed.

Ashing	O_2 plasma RIE 10 sec, 50 W, 100 mTorr
Oxide removal	Mix HCl:DI [10:1] by stirring on a 20°C hotplate for 5 min Dip the chip for 30 sec, using a Teflon holder (no stirring) 30 sec DI rinse Blow dry with N_2
Metal deposition	Clamp sample from both sides to improve heat transfer Pump chamber to 5x10^{-7} mTorr Deposit 20 nm Ti Deposit 20 nm Pd Deposit 75 nm Au Deposit * nm Ni/Cr (*thickness vary with etch depth)
Lift off	Acetone 70°C, wait for lift off assist with spray bottle or pipette as required Move chip to fresh beaker with Acetone 70°C IPA 70°C Dry with N_2 Check pattern in microscope
Pre-Etching	Repeat cleaning and ashing steps once more Prepare a DI and a IPA beaker on a hotplate (70°C) Etch a 'waste' InP/InGaAs chip for 2-3 min
Etching	Clean carrier wafer with Isopropanol and cleanroom wipes Load chip onto the carrier using a small drop of santovac oil Transfer wafter into the chamber using the loadlock After wafter is clamped onto the plate wait 3 min Adjust laser as required Etch 0-8 sec: 2 mTorr, 150°C, 1000 W ICP, 100 W RF, 9 Sccm HBr Etch 8- sec: 0.3 mTorr, 150°C, 800 W ICP, 100 W RF, 9 Sccm HBr 30 sec stir in DI 30 sec stir in Isopropanol Dry with N_2

Reflectance models

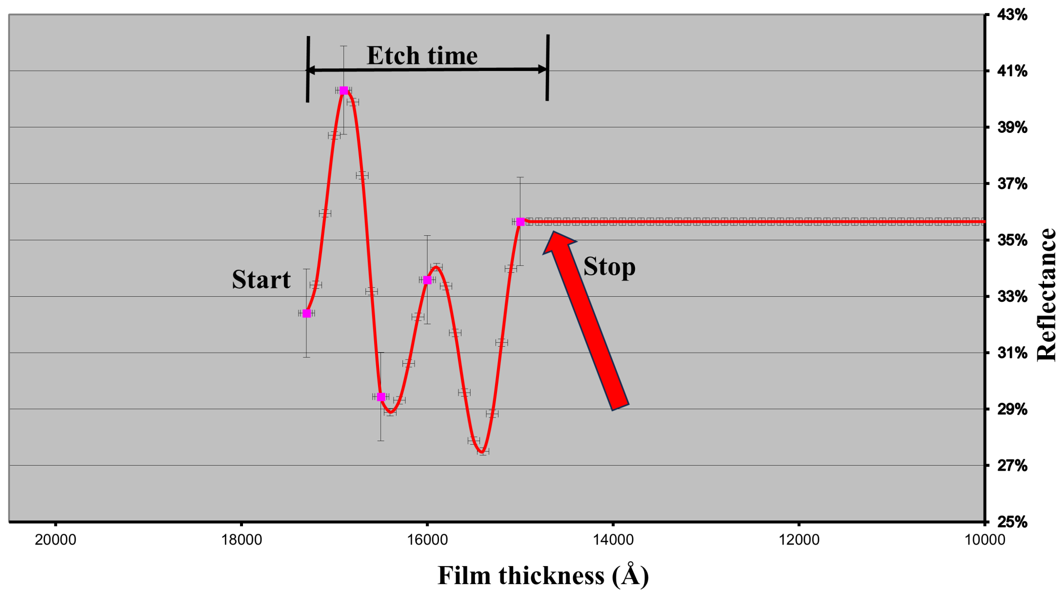


Figure 1: Calculated reflectance model for the FMBD-S. Etching is stopped right as the signal derivative hits zero for stop in the point indicated by the red arrow. Corresponding to a 310 nm deep etch.

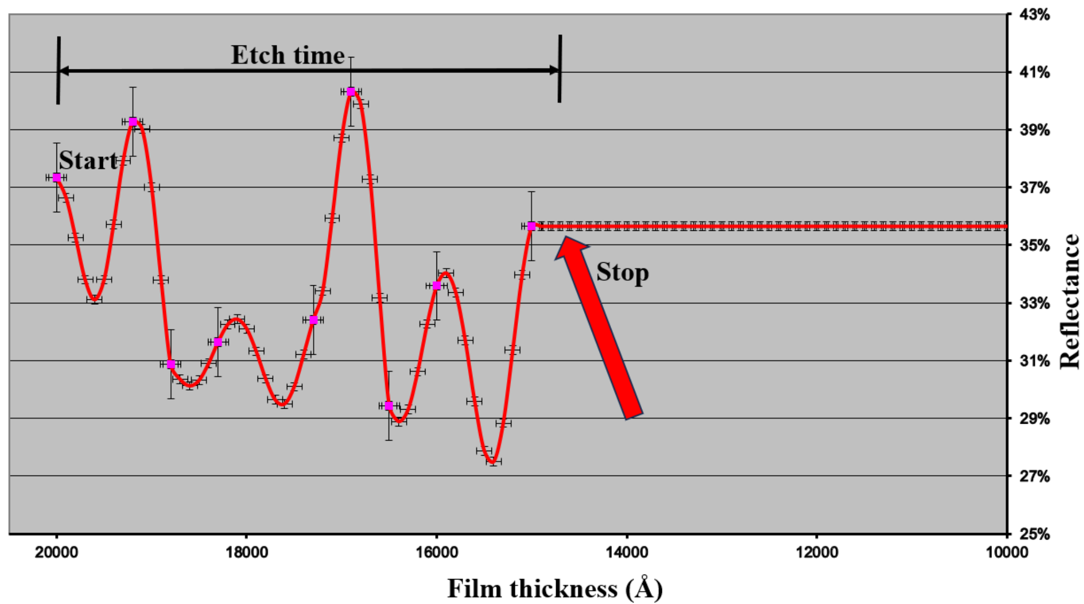


Figure 2: Calculated reflectance model for the FMBD-D. Etching is stopped right as the signal derivative hits zero for stop in the point indicated by the red arrow. Corresponding to a 540 nm deep etch.

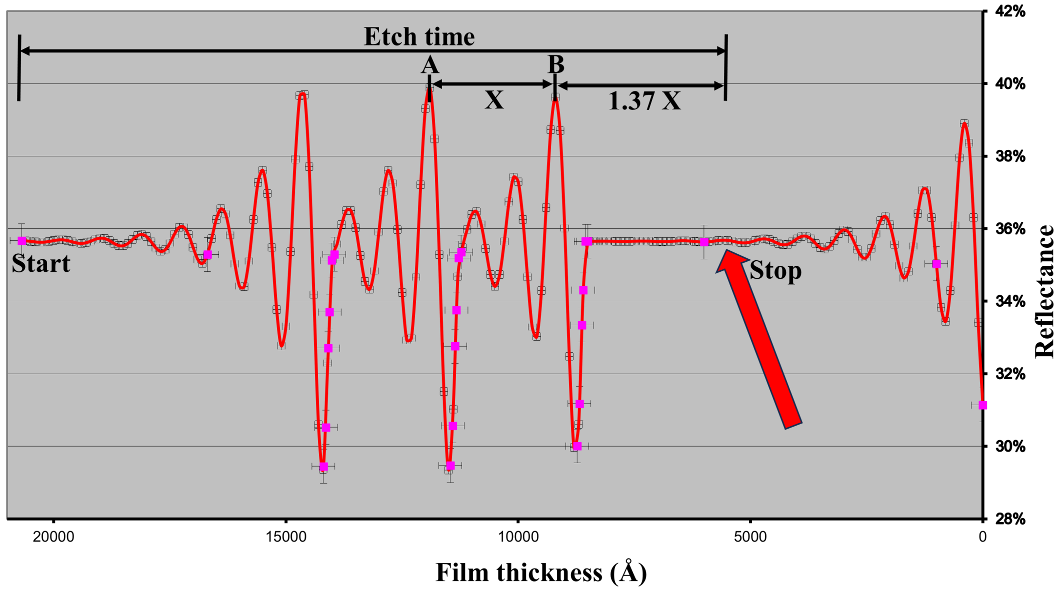


Figure 3: Calculated reflectance model for the HBV. Etching is aborted as the signal reaches the point indicated by the red arrow, which corresponds to a 1520 nm deep etch. This is point can be hard to identify while etching, and it is therefore recommended that one measures the time (X) from when the signal reaches point to point B, and then aborting $1.37 * X$ seconds after the signal reached point B.

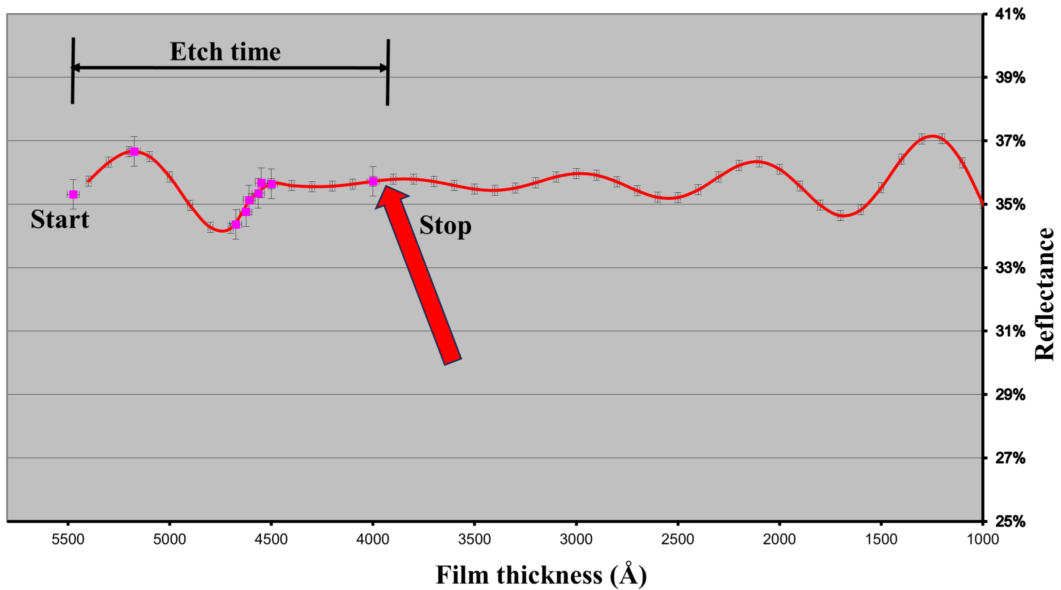


Figure 4: Calculated reflectance model for the RTD. Etching is aborted right before the signal reaches the top of the hill, as indicated by the red arrow. Corresponding to a 240 nm deep etch.

Appendix B

Figure 5: ICP-RIE system, Oxford PlasmaPro 100

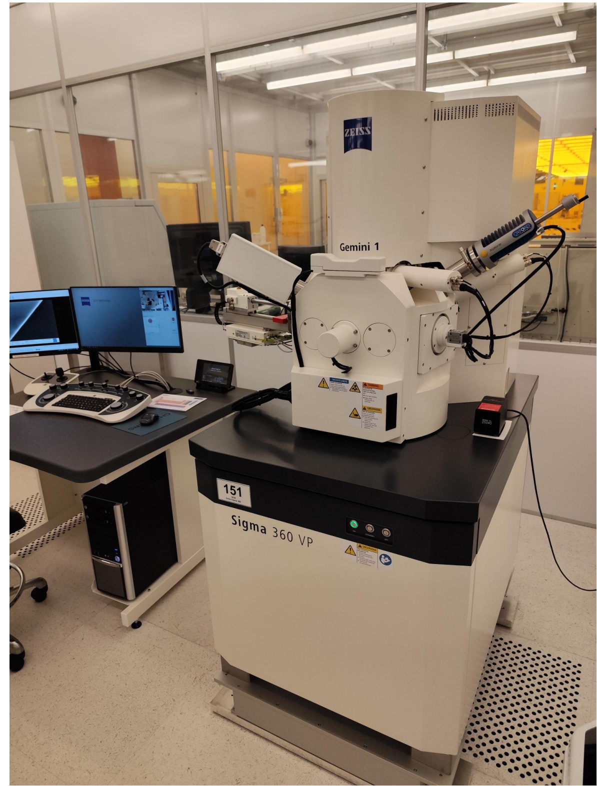
Figure 6: Electron beam lithography tool, Raith EBPG 5200

(a) Lesker PVD 225

(b) Lesker Spectros

Figure 7: Evaporators

(a) Zeiss Supra 60 VP, with EDX detector



(b) Zeiss Sigma 360

Figure 8: Scanning electron microscopes

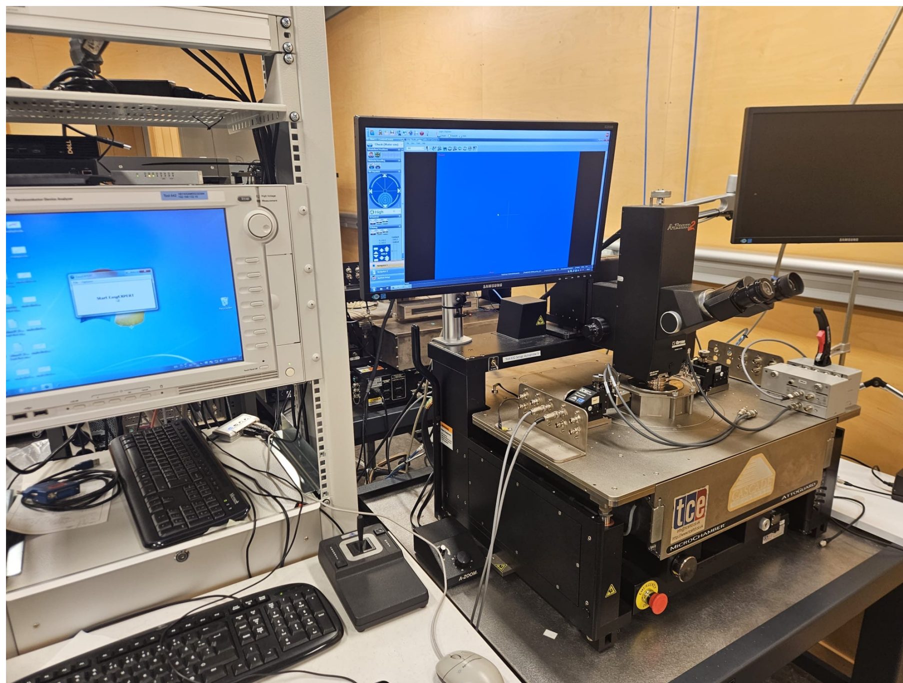


Figure 9: Probe station