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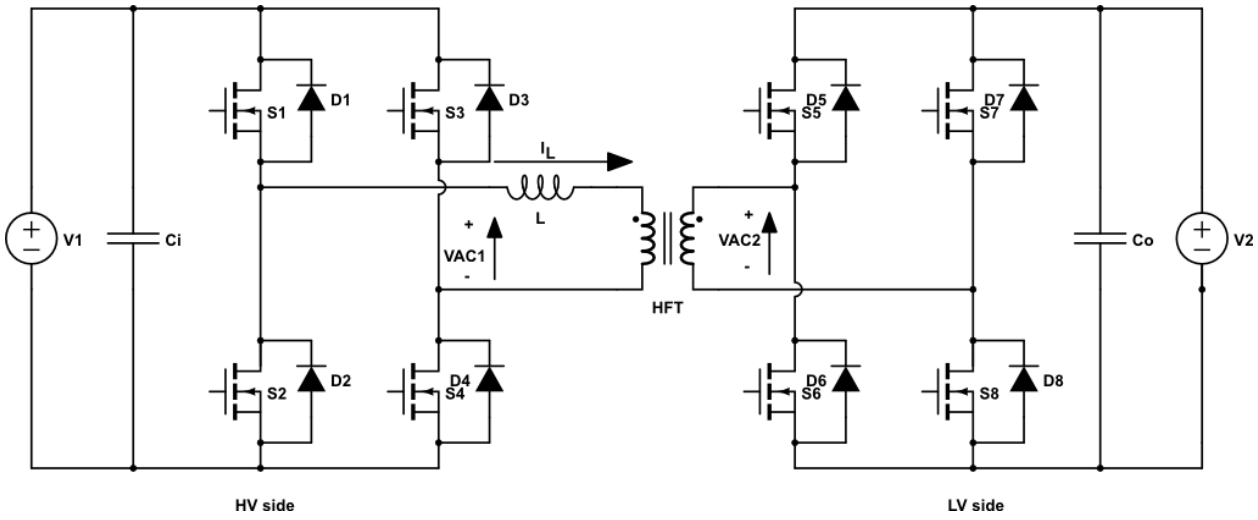


# Designing of a SiC Equipped DC/DC Converter for Hybrid Vehicles

*Master of Science Thesis*

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Department of Energy and Environment
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2019

# Designing of a SiC Equipped DC/DC Converter for Hybrid Vehicles

A Master of Science thesis in which dual active bridge DC/DC converter topology is designed and studied

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*Division of Electric Power Engineering*
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Investigate and Design of DC/DC Converter for Automotive Industry

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# Abstract

This thesis investigates a Dual Active Bridge (DAB) DC/DC converter which can be used for automotive applications to interface the battery with the DC link. The thesis starts with a qualitative study of different DC/DC converter topologies to select the best topology. After that, the operational principle of the DAB converter is analyzed using trapezoidal modulation, and theoretical analysis is made to design the components of the DAB converter. The converter is designed for an input voltage of 240 V and a nominal output voltage of 12 V with a rated power of 2 kW. The control strategy for the generation of pulses is addressed to achieve power transfer. The DAB converter is suitable for power flow control between the two DC buses due to its bidirectional power flow capability. The Power loss in the semiconductors and the efficiency are analytically calculated and compared for the Si MOSFET and SiC MOSFET for different switching frequencies. The results clearly show that a SiC MOSFET reduces the switching loss strongly and increases the conduction loss. In the case of a Si MOSFET, 53 % of the total loss is switching loss for 100 kHz but in the case of a SiC MOSFET, it reduces to 12 % and the efficiency also increases from 93.5% to 95 %. After selecting the core material and other parameters for high frequency transformer, the losses in the transformer are analyzed for the core loss and winding loss with different output voltages and switching frequencies. The result promotes high frequency operation to reduce the core loss. Moreover, the operating point where the transformer can operate with the minimum total transformer loss is identified. Finally, the thermal model for the converter is analyzed with selection of a proper heat sink.

Keywords: Dual Active Bridge, Bidirectional DC/DC Converter, Trapezoidal Modulation, High Frequency Transformer

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# Contents

# 1
# Introduction

## 1.1 Background

A huge number of vehicles used far and wide has caused and keep on causing major issues on human life and nature. The fundamental issues which are identified with conventional vehicles incorporate air pollution, a worldwide temperature alteration, and quick exhaustion of the world's oil assets. In recent times, Electric Vehicles (EV), Hybrid Electric Vehicles (HEV), and fuel cell electric vehicles are gaining popularity to replace conventional vehicles [1].

At present, in HEVs and EVs, a high voltage battery pack supplies energy to the electric traction system. The ordinary 12 V traction system is used to provide all the electric loads such as head and tail lights, heating fans, sound system, etc. In the other way, the high voltage bus sustains the traction inverter and engine. Since a double voltage control system is available in the electric vehicle, it is appropriate to transmit energy between the two voltage systems which exist in HEV and EV.

Due to wide availability and cost, Silicon (Si) has been the most commonly utilized material in power semiconductors such as MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) and IGBTs (Insulated Gate Bipolar Transistor). However, the growing requirements of the automotive industry, in terms of efficiency, have shifted the interest towards new technologies. These technologies do not show the limitations of Si, such as, lower operating temperatures and slower switching times. Silicon Carbide (SiC) and Gallium Nitride (GaN), allow higher switching frequencies, higher blocking voltage capability, higher maximum operating temperatures, higher thermal conductivity and lower voltage drop [2]. These characteristics make them suitable candidates for high power density and efficiency applications. These semiconductor material properties also affect the complete converter circuit in terms of cooling requirements, robustness and volume.

## 1.2 Purpose

The purpose of this thesis is to design an efficient DC/DC converter for automotive applications and to analyze its efficiency and power loss for different switching frequencies. The design process includes the transformer design for the converter and thermal model analysis for selected converter topology. In order to increase the efficiency from the conventional set up, a SiC will be investigated.

## 1.3 Limitations

Theoretical and simulation models have been investigated for the selected DC/DC converter topology based on previous work and a literature review for different switching frequencies. Analysis is made based on efficiency, semiconductor loss and transformer loss. To enumerate some constraints, the following limitations are set:

- This thesis does not include hardware design of the selected typology.
- The power transfer is controlled only by adjusting the inner and outer phase shift ratios.
- Loss is analyzed analytically by considering only the losses in the semiconductors and high frequency transformer, while capacitor and inductor losses are not included in this thesis.

## 1.4 Social, Ethical and Ecological Aspects

The project will take into consideration the sustainability and ethics of designing the DC/DC converters. The sustainability aspect of constructing the DC/DC converters consists of investigating how the materials and the different components will affect the environment. The study will take this into account both in the construction of the individual components and the assembly of the converters. To get more efficient electrified vehicles, all the parts in the power train need to be more effective and if possible more compact to get lighter vehicles and/or more space for the passengers.

The design of DC/DC converters in this thesis will be a suitable part of a power train in an electrified vehicle. It has considered the different automotive design constraints. However, to create more environmentally friendly transportation, it is important to consider that the vehicle itself is produced as sustainable as possible. Therefore, the sustainability aspect of the DC/DC converters needs to be investigated such as how the semiconductor materials and the different components affect the environment.

When the DC/DC converters are used, their operation should be sustainable. In addition, the production of the electricity for the converters should be sustainable. The two different semiconductor materials have been compared considering the ethical aspects of the DC/DC converter , and the IEEE's code of ethics has been followed.

The first code of ethics is "to be honest and realistic in stating claims or estimates based on available data". To address this, before any claims about the designed converter will be made, it is essential to do some research to have facts and back up the claims. To be honest about the results of the converters, to be clear on how it works and what problems will be encountered. Since if the problems of the converters are not identified and only known their benefits, it will result in technical problems when they are being used.

The second code of ethics is "to improve the understanding of technology, its appropriate application, and potential consequences". Before designing DC/DC con-

verters, some research is needed regarding the technology and about the semiconductor materials. After the research, the converters will be designed with the most optimized semiconductor materials by comparing two semiconductor materials for different switching frequencies.

In this way more understanding of the converters will be achieved and it will give the chance to know what to change and how to improve the converter.

# 2

# Qualitative Study of DC/DC Converters

DC/DC converters are used in several applications including automotive power supplies for the hybrid vehicles, personal computers, office equipment, telecommunications equipment, laptops, and DC motor drives.

In the configuration of HEV/EV power supplies, DC/DC converters are necessary for interfacing an energy component, batteries, and supercapacitors to the DC-link voltage. For interfacing an energy unit, DC/DC converters are utilized to increase the fuel cell voltage and regulate the DC-link voltage. In order to interface batteries or supercapacitor modules, bidirectional DC/DC converters are required. In different research papers various sorts of DC/DC power converters are proposed. It is possible to find insulated and non-insulated DC/DC converters topologies. Also, due to the vehicles converter requirements, the power converter structure must be reliable, lightweight, have a minimized size and high efficiency [3].

The purpose of this section is to present the different topologies of DC/DC converters, namely isolated and non isolated which are suitable for hybrid vehicles, each having their advantages and disadvantages. Based on different features of the DC/DC converters which are suitable for a HEV, different topologies will be compared and the best topology will be selected.

## 2.1 Features of DC/DC converter

Different DC/DC converters topologies, including converters with direct energy conversion (non isolated) and with intermediate storage components (isolated), have been published by different experts. However, in vehicle application, some structural consideration is needed [3].

- High efficiency,
- Light weight,
- Low electromagnetic interference,
- Small volume,
- Low cost,
- Low current ripple
- Voltage ratio of the converter,
- Soft switching

Based on these design considerations, features which are used for the comparison of different DC/DC topologies for a HEV are identified. These features are electromagnetic interference (EMI), current ripple, galvanic isolation, hard switched/soft switched, bidirectional/unidirectional, capacitor size, voltage ratio and stress on the switch.

**Electromagnetic Interference**

EMI is undesirable coupling of signals from one circuit to another, or to system coupling via conduction through parasitic impedance, power and ground connections. It is created due to high power, high $di/dt$ on the switches and diodes, fast transients (voltage and current), parasitic inductance and capacitance in current paths [3].

Power electronics converters are considered as a source of electromagnetic interference which is responsible for power system disturbances including voltage and frequency variations. For an electric vehicle, the limitation is based on the EMI regulations [3], [4], [5]. In this section, converters have been identified whether they can achieve the limitation or not without or with the EMI filter.

The power electronic interface which increase the low fuel cell voltage to a fixed DC bus voltage should also maintain the fuel cell input current ripple at a lower level in order to expand fuel cell or battery lifespan [4].

**Capacitor Size**

To compare the capacitor size for different topologies, a common voltage ripple of 1% for all converters are considered to calculate the new size of the capacitor in kJ/MVA. The capacitor size can be calculated as

$$C_1 = \frac{2E_{max,arm}}{(V_{r1}^2 - 1)V_c^2} \tag{2.1}$$

$$C_2 = \frac{2E_{max,arm}}{(V_{r1}^2 - 1)V_c^2} \tag{2.2}$$

where $C_1$ is the original capacitor size, $C_2$ is the new value of the capacitor size based on the common ripple voltage, $E_{max,arm}$ is the maximum energy across the arm, $V_{r1}$ is the original ripple voltage, $V_{r2}$ is common ripple voltage and $V_c$ is the voltage across the capacitor [6].

Various competitive topologies which are suitable for automotive application have been assessed based on the features discussed on Section 2.1. These topologies of DC/DC converter can increase or decrease the magnitude of DC voltage and/or invert its polarity. These topologies are divided into two categories, namely isolated and non isolated converters.

## 2.2 Non-isolated DC/DC Converters Topologies

Non-isolated DC/DC converter topologies are generally utilized in medium and high power applications. Especially, step-up converters such as the conventional boost [3], the bidirectional buck-boost [7], the interleaved boost converter [3], [5], [4], [8] and the floating-interleaved boost [9] are the most well known topologies for interfacing battery with the dc-link. This is because of their interesting features such as simplicity, simplified control, compactness and low cost. The boost converter produces an output voltage higher than its input voltage while the buck-boost converter inverts the polarity of the input voltage, it can boost or reduce the output voltage depending on the duty cycle. The voltage of a battery cell is normally low and it must be boosted to accomplish a several hundreds of volts on the DC-bus, consequently, the boost DC/DC converters are required.

One of the most important required characteristics of power converters is the current ripple reduction to increase the performance of the battery. The following equation gives the current ripples of basic DC/DC boost converter [3]:

$$\Delta I = \frac{V_i D}{2fL} \tag{2.3}$$

where $V_i$ is the input voltage, $D$ is the duty cycle, and $f$ and $L$ are the switching frequency and the inductance value respectively.

From (2.3), it can be seen that a small current ripples needs larger value of inductance. Hence, a large inductor volume makes the total volume of the conventional boost converter quite large. Another parameter which affects the current ripples is the switching frequency. However, it cannot be increased because the switching losses are proportional to the switching frequency. Based on this, the conventional boost converters have a low efficiency for a high conversion ratio, a low voltage gain and high volume of passive components.

To improve the voltage gain, compactness, and efficiency of the basic boost converter, several topologies based on the basic configurations of it are proposed in [3], [9], [5], [10], [11], [7], [10], [12]. When the converter are required to achieve high conversion ratio, floating topologies have many opportunities. The topologies based on the topology of the basic boost converter have several possibilities, including interleaving and higher voltage-gain of the entire converter. Table 2.1 shows that the features of this converters that have a high efficiency.

## 2.3 DC/AC/DC topologies: Isolated Converters

Isolated DC/DC converters have an intermediate AC phase made of a single phase inverter and a transformer. The transformer enables having a low voltage for the input converter and low currents for the output converter. The high voltage ratio is the main benefit of these converters [3]. The electrical isolation of the high frequency transformer is utilized to protect the power module/batteries stacks under overload

conditions. The AC stage can be half-bridge [13], [14], [9], or a full-bridge [3], [9], [15], [12], [16].

The operating frequency is fluctuated contrarily with volume and weight of the transformer, hence the addition of the transformer into the converter provide substantial enhancement. The soft-switching operation of the half-bridge isolated converter topology becomes possible by introducing additional components [9].

## 2.4 Comparison and Selection of Best Topology

The features of the converters which have high efficiency, both isolated and non isolated converter topologies are summarized in Table 2.1.

**Table 2.1:** Features of high efficiency DC/DC converter topologies

| Classification | Topologies | Features | Efficiency | Reference |
|---|---|---|---|---|
| Isolated | ZVZCS hybrid-switching full-bridge dc–dc converter | Provide wide ZVS range<br>Reduced size of capacitor and inductor<br>Minimal voltage stress | 98.1 | [16] |
| | High step-up soft-switched bidirectional DC/DC converter | Achieve soft switching in wider range<br>Reduced voltage stress | 97.7 | [17] |
| | Dual Active Bridge DC/DC converter | Reduced current and voltage ripple<br>High efficiency by operating switch in ZVS<br>Low switching loss<br>High voltage ratio | 98.5 | [12] |
| | Bidirectional coupled inductor boost converter | Reduced switching losses<br>Soft switching can be achieved<br>High power density | 99.8 | [11] |
| Non isolated | Multidevice interleaved boost converter (MDIBC) | Reduced stress across the switch<br>Reduced passive device<br>Medium voltage ratio | 97.3 | [5] |
| | Resonant Isolated Boost (RIB) converter | High voltage ratio<br>Low current ripple<br>Soft switching | 97.2 | [9] |
| | 3X dc-dc converter | Compact size and light weight<br>Flexible voltage ratio<br>Low voltage stress | 97.2 | [10] |
| | Bidirectional interleaved buck-boost converter with n phases | Low number of active and passive components<br>Low switching loss<br>Low voltage stress<br>Soft switching | 98.4 | [7] |
| | Four-phase interleaved Buck/Boost DC/DC converter | Reduced current ripple<br>High voltage ripple<br>Medium voltage ratio<br>Reduced size of passive components | 97.3 | [12] |

In this study, a total of 23 topologies are compared and from this 15 are non-isolated and 8 are isolated DC/DC converters which can be used for automotive applications. To select the best topology, the converters are compared based on the features which are described in Section 2.1 with calculation of the total point from each features as shown in Figure 2.1. Figure 2.2 shows the total result of the study for different converter topologies when considering the isolated converter as an advantage.

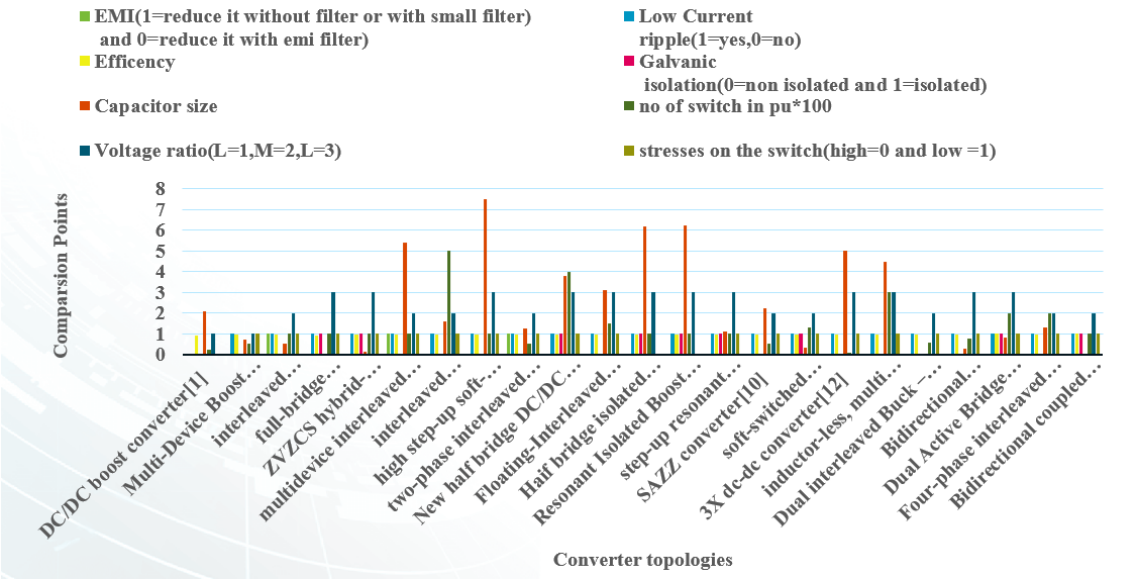



**Figure 2.1:** Comparsion of DC/DC converter topologies based on different features

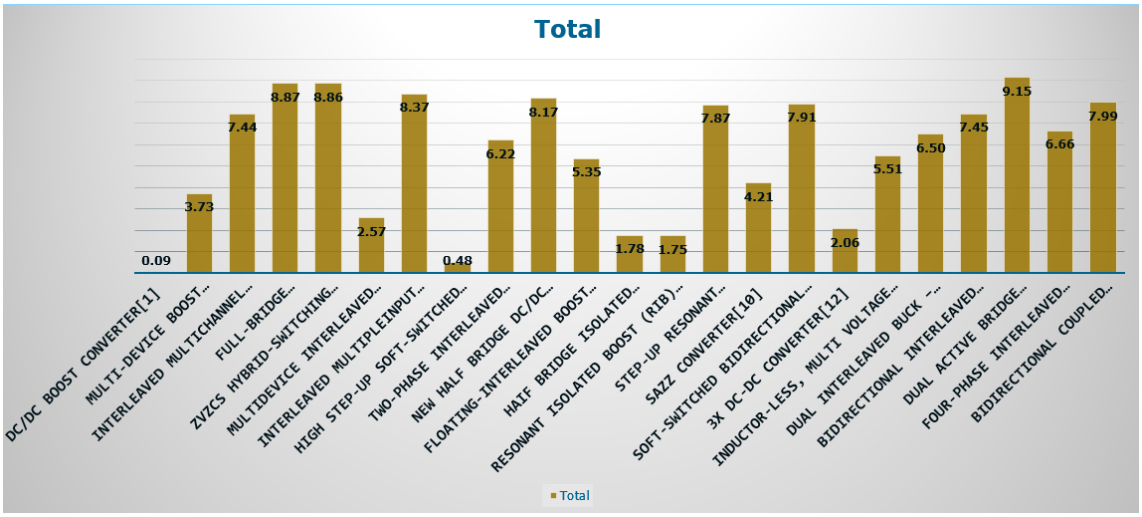



**Figure 2.2:** Total comparsion of DC/DC converter topologies with considering galvanic isolation as an advantage

Based on Figure 2.2, from non-isolated and isolated DC/DC converters topologies, the dual active bridge DC/DC converter has the highest total value compared to the other converter topologies, and it is considered as the best topology and selected for further study and design process.

# 3
# Theory

## 3.1 Design Overview

An electric vehicle that utilizes a mix of various energy sources such as fuel cells, batteries and supercapacitor is shown in Figure 3.1.

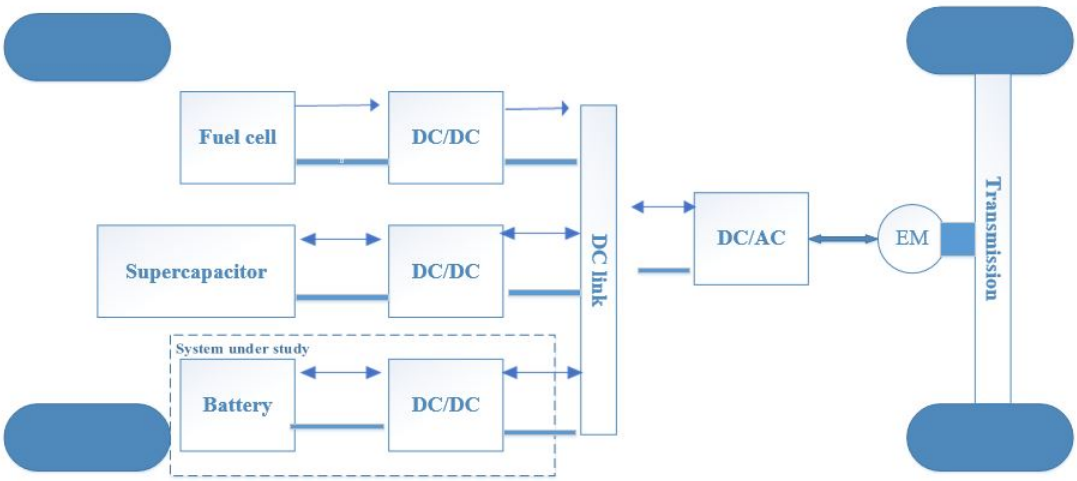



**Figure 3.1:** Electric vehicle drive system

In the fuel cell battery configuration, the fuel cell gives nearly a similar power all the time due to the fixed voltage of the battery. But in the battery/supercapacitor arrangement only a fraction of the energy exchange capability of the battery can be used since the battery has almost constant voltage [1]. By introducing DC/DC converters one can pick up the voltage variation of the devices and the power of each device can be controlled. From Section 2, the dual active bridge converter topology is selected for the design.

## 3.2 Dual Active Bridge (DAB) DC/DC converter

The basic topology of the DAB is characterized by two active bridges connected through a high frequency transformer as shown in Figure 3.2. As both of the bridges

are active, the power flow can be bidirectional [18].

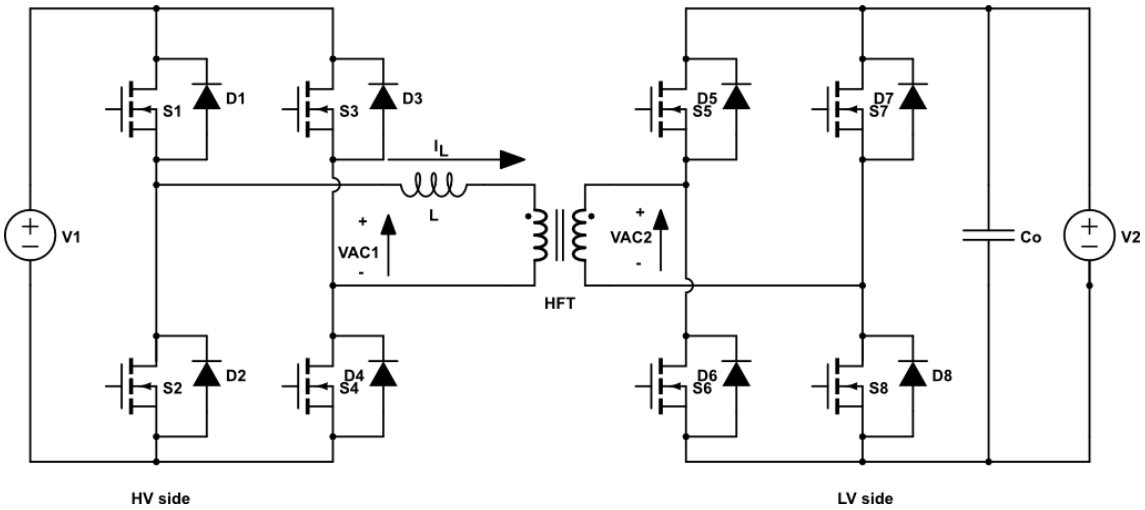



**Figure 3.2:** Dual active bridge topology schematic

A DAB comprises eight switches which are set on four legs in the full bridge circuit and high frequency transformer. Four switches are placed on the high voltage side and four switches are located on the low voltage side.

The high frequency transformer separated the high voltage side from the low voltage side. To accomplish soft switching, the leakage inductance of the transformer and parasitic capacitance are used with an appropriate switching pattern. This can be used to limit switching losses, increase switching frequency, and decrease the size and weight of transformer and passive components in the converter. The reduction of passive component, the evenly shared current in the switch and adaptable control technique are the fundamental benefit of the DAB converter [18].

### 3.2.1 Switching Pattern

The DAB converter has two voltage sourced full bridge circuit which are associated with the inductor and high frequency transformer. In order to transfer power, $V_{AC1}$ and $V_{AC2}$ must be provided by the full bridge circuit to the high frequency transformer and the converter inductor $L$. Hence, the voltage sources on the HV and LV side full bridge circuit can be replaced by voltage source, $V_{AC1}$ and $V_{AC2}$ to simplify the analysis as shown in Figure 3.3.

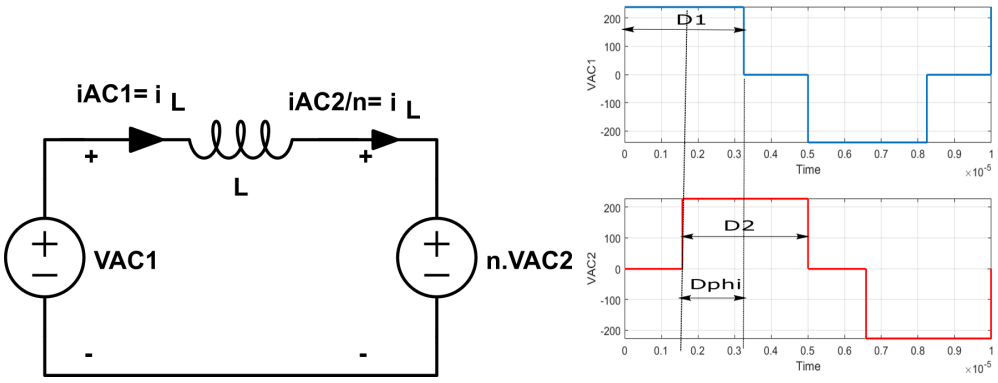



**Figure 3.3:** Simplified DAB circuit with voltage waveform

An appropriate control strategy of the switches is needed to have two square voltages waves on the high voltage and low voltage sides of the high frequency transformer, $V_{AC1}$ and $V_{AC2}$. $nV_{AC2}$ is the transferred voltage from the high voltage side to the low voltage side of the high frequency transformer.

The adaptable control approach can be accomplished by altering the duty cycles of the two sides of the transformer voltage which are $D_1$ and $D_2$, and the phase shift angle between the high voltage and low voltage side of the transformer. As can be seen from Figure 3.3, the duty cycle equivalent to the phase shift between the two sides of the transformer, $V_{AC1}$ and $V_{AC2}$ represented by $D_{phi}$. For this analysis, the voltage ratio is defined as

$$d = \frac{nV_o}{V_i} \tag{3.1}$$

where $V_i$ and $nV_o$ are the input and referred output voltage respectively. When $V_i >= nV_o$ then $d <= 1$ and the converter transfers positive power. If $V_i < nV_o$ then $d > 1$ and the converter transfers negative power.

The phase shift modulation is the most widely used modulation system to operate DAB with fixed switching frequency and the highest duty cycles, $D_1 = D_2$=1/2. It exclusively forms the phase shift $\phi$ between the two transformer voltages to control the transported power [19]. Since only one variable is required to control the transferred voltage, it is simple compared to the other modulation systems.

### 3.2.2 DAB Inductor Current

With the HV side full bridge, three different voltage levels are possible for $V_{AC1}(t)$,

- $+V_1$ for state I: $S_1, S_4$ on, $S_2, S_3$ off
- 0 for state II: $S_1, S_3$ on, $S_2, S_4$ off or for state III: $S_2, S_4$ on, $S_1, S_3$ off
- $-V_1$ for state IV: $S_2, S_3$ on, $S_1, S_4$ off

Similarly, $V_{AC2}(t)$ is equal to $+V_2$, 0, or $-V_2$ depending on the switching states of $S_5, S_6, S_7$, and $S_8$. The resulting voltage,

$$V_R(t) = V_{AC1}(t) - nV_{AC2}(t) \tag{3.2}$$

applied to the inductor of the simple DAB model (Figure 3.3), generates the current

$$i_L(t_1) = i_L(t_0) + \frac{1}{L}(\int_{t0}^{t1} V_R \, dt) \tag{3.3}$$

This inductor current equation works for all values of time with $t_0 < t_1$.

### 3.2.3 Circuit Operation

The trapezoidal modulation method is selected for this converter operation since it has lower rms current and less switching loss compared to phase shift modulation. For trapezoidal modulation, as for single phase shift modulation, the two transformer voltages $V_{AC1}$ and $V_{AC2}$ will be phase-shifted. In addition to that, two inner phase-shifts are introduced between the two legs of each full bridge. As shown in Figure 3.4, the primary side of $S_1$ and $S_3$ has a phase shift of $D_1$ and secondary side of $S_5$ and $S_7$ has a phase shift of $D_2$. This causes the duty cycle of $V_{AC1}$ and $V_{AC2}$ to change and introduces a time during which $V_{AC1}$ and $V_{AC2}$ will be zero.

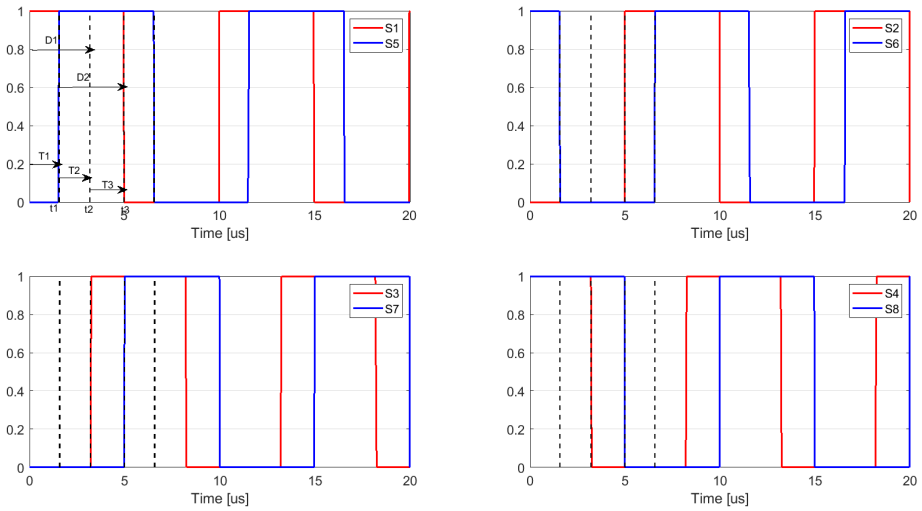



**Figure 3.4:** Switching signals for the gates $S_1$ to $S_8$

Figure 3.4 shows the gate control signals of a dual active full bridge converter. The activity of the circuit is accomplished by a suitable turn on/off a grouping of eight switches ($S_1$ to $S_8$).

### 3.2.4 Transferred Power, Phase Shift Angle and Duty cycles

The equations for the transferred power, phase-shift angle and other expressions for trapezoidal modulation are given in [19]. For the trapezoidal modulation typical voltages and current waveform are shown in Figure 3.5.

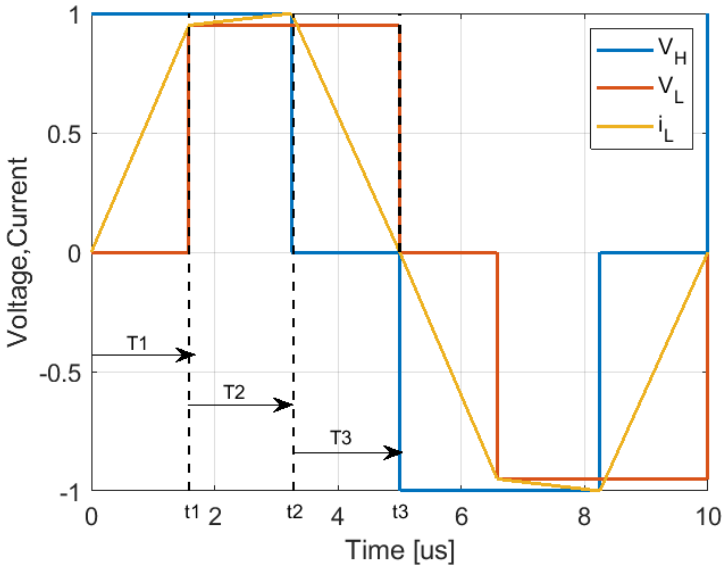



**Figure 3.5:** Transformer voltages and inductor current for trapezoidal current mode modulation

For the trapezoidal current mode modulation, three different time intervals can be identified. During $0 < t < t_1$, $V_{AC1}(t) = V_1$ and $V_{AC2}= 0$ and the absolute value of the inductor current, $|i_L(t)|$, increases from zero. At $t = t_1$, the voltage$V_{AC2}(t)$ changes to $V_{AC2}(t) = nV_2$ and remains constant during $t_1 < t < t_2$. During $t_2 < t < t_3(T_s/2)$, $V_{AC1}(t) = 0$ and $V_{AC2}(t) = V_2$ apply and $|i_L(t)|$ decreases back to zero.

The transferred power is given as,

$$P = sgn(\phi)\frac{nV_1V_2[2nV_1V_2(\pi^2 - 2\phi^2) - (V_1^2 + (nV_2)^2)(\pi - 2|\phi|)^2]}{4\pi^2 f_s L(V_1 + nV_2)^2} \tag{3.4}$$

The required phase shift angle $\phi$ and duration $T_1, T_2$ and $T_3$ are given as,

$$\phi = \pi/2\frac{sgn(P)}{V_1^2 + nV_1V_2 + (nV_2)^2}(V_1^2+(nV_2)^2-(V_1+nV_2)\sqrt{nV_1V_2[1 - \frac{4f_sL|P|(V_2)^2 + nV_1V_2 + (nV_2)^2}{(nV_1V_2)^2}]}) \tag{3.5}$$

$$T_1 = \frac{nV_2 - V_1 + 2V1\phi/\pi}{2f_s(V_1 + nV_2)} \tag{3.6}$$

$$T_2 = \frac{1 - 2\phi/\pi}{2f_s} \tag{3.7}$$

$$T_3 = \frac{V_1 - nV_2 + 2nV2\phi/\pi}{2f_s(V_1 + nV_2)} \tag{3.8}$$

By means of $T_1$ and $T_2$ the equations of the duty cycles of $V_{AC1}$ and $V_{AC2}$ can be derived as

$$D_1 = (1 - \frac{2T_3}{T_s})T_s/2 \tag{3.9}$$

$$D_2 = (1 - \frac{2T_1}{T_s})T_s/2 \tag{3.10}$$

$D_1$ and $D_2$ are not only representing the duty cycles, but also corresponding to the inner phase-shifts, i.e the phase-shifts between the two legs of the input and output bridge as shown in Figures 3.4.

## 3.3 Semiconductor Loss Determination

There are two types of losses in a semiconductor, namely conduction loss and switching loss. Switching losses are created when the switch is turned on and off whereas the conduction losses are created when it is conducting.

### 3.3.1 Conduction Loss

The RMS currents through the switches determine the respective conduction losses. In steady-state operation, every switch conducts current during half a switching cycle $T_s$ and the waveform of the inductor current $i_L(t)$ (Figure 3.5) repeats itself with negative sign after one half-cycle [i.e. $i_L(t) = i_L(t - (T_S/2)]$. Thus, each of the 4 switches on the HV side ($S_1$, $S_2$, $S_3$, and $S_4$) carries the RMS current $I_{s1}$ [19],

$$I_{s1} = \frac{I_L}{\sqrt{2}} \tag{3.11}$$

and each of the 4 switches on the LV side carries the RMS current

$$I_{s2} = \frac{nI_L}{\sqrt{2}} \tag{3.12}$$

where $n$ is transformer ratio and $I_L$ is the RMS value of $i_L(t)$.

According to (3.11), the switches on the HV side generate the total conduction losses

$$P_{s1,cond} = 4R_{s1}I_{s1}^2 \tag{3.13}$$

And according to (3.12) all switches on the LV side cause the total conduction losses

$$P_{s2,cond} = 4R_{s2}I_{s2}^2 \tag{3.14}$$

where $R_{s1}$ and $R_{s2}$ are the DC switch resistances of the selected MOSFETs for the high voltage and low voltage respectively which can be extracted from the data sheet.

Due to the diode forward voltage drop on the on time of MOSFET, the conduction loss can be found as,

$$
\begin{aligned}
p_{on\_state} &= \frac{1}{T}\int_0^{DT_s} i_{on}(V_{sd} + R_{s1}I_{s1})dt \\
&= \frac{V_{sd}}{T_s}\int_0^{DT_s} i_{on}dt + \frac{R_{s1}}{T_s}\int_0^{DT_s} i_{s1}^2 dt \\
&= V_{sd}I_{on,avg} + R_{s1}I_{s1}^2
\end{aligned}
$$

Consequently, the conduction loss on the primary and secondary side of the transformer is calculated as [18],

$$P_{s1,cond} = 4(R_{s1}I_{s1}^2 + V_{sd}I_{on,avg}) \tag{3.15}$$

$$P_{s2,cond} = 4(R_{s2}I_{s2}^2 + V_{sd}nI_{on,avg}) \tag{3.16}$$

where $V_{sd}$ is the diode voltage drop which is given in the MOSFET datasheet, $n$ is the transformer turn ratio and $I_{on,avg}$ is the average current when the MOSFET conduct.

### 3.3.2 Switching Loss

The switching loss for a semiconductor occurs when the switch is turned on and off [18]. The turn on and the turn of time is calculated based on the rise time and fall time of current and voltage as shown in Figure 3.6 as,

$$t_{on} = t_{ri} + t_{fv}$$

$$t_{off} = t_{fi} + t_{rv}$$

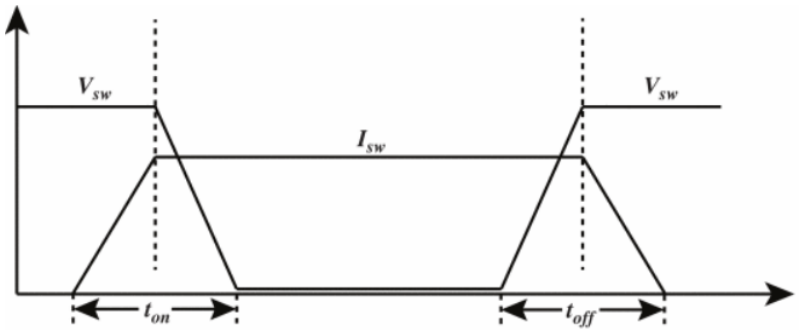



**Figure 3.6:** Typical MOSFET turn on and turn off transtion

In order to calculate the voltage rise time and current fall time using data sheets values, the rise time of voltage is derived as [20],

$$t_{rv} = \frac{Q_{gd}(V_{DS} - V_F)(R_g + R_{g\_app})}{(V_{DS\_D} - V_{F\_D})(V_{th} + \frac{I_{DS}}{g_{fs}})} \tag{3.17}$$

where $Q_{gd}$ is the gate drain charge, $V_{DS}$ is the drain source voltage, $V_F$ is the forward voltage, $R_g$ is the internal gate resistance, $R_{g\_app}$ is the external gate resistance, $V_{th}$

is the MOSFET threshold voltage, and $I_{DS}$ and $g_{fs}$ are the drain source current and the forward transconductance. All the parameters values can be extracted from the datasheet of the MOSFET.

And the fall time of current can be found as,

$$t_{fi} = (R_g + R_{g\_app})C_{iss}@V_{DS} ln[\frac{V_{GP}(1 + \frac{g_{fs}L}{R_g + R_{g\_app}C_{iss}@V_{DS}})}{V_{th}}] \tag{3.18}$$

where $C_{iss}$ is the input capacitance which is the summation of gate-drain capacitance and gate-source capacitance, $V_{GP}$ is the gate plateau voltage and $L$ is the inductance of the MOSFET.

Then, the turn off losses can be calculated as

$$P_{off} = V_d I_0 \frac{t_{fi} + t_{rv}}{2} f_s \tag{3.19}$$

where $t_{fi}$ and $t_{rv}$ are the fall time and the turn off delay respectively.

In the same way, the turn on losses can be calculated as

$$P_{on} = V_d I_0 \frac{t_{ri} + t_{fv}}{2} f_s \tag{3.20}$$

where $t_{ri}$ is the rise time and $t_{fv}$ is the turn on delay time. $V_d$ is the drain to source voltage when the MOSFET is turning on and $I_0$ is the drain current.

### 3.3.3 Active, Reactive Power and Efficiency

Active power is the actual transferred power which is calculated using (3.4). The reactive power is calculated based on the total loss, rated power and actual transferred power as

$$P_{reactive} = P_{rated} - P_{total\_loss} - P_{Trans\_act} \tag{3.21}$$

where $P_{rated} = 2kW$, $P_{total\_loss} = P_{conduction\_loss} + P_{switching\_loss}$ and $P_{Trans\_act}$ is the actual transferred power which is calculated using (3.4).

And the efficiency of the converter is calculated as

$$Efficiency = P_{Trans\_act}/P_{in} \tag{3.22}$$

where $P_{in} = P_{Trans\_act} + P_{total\_loss}$

## 3.4 Losses in the Transformer

The power loss in a transformer can be divided into two types i.e copper loss and iron loss. The total power loss in a transformer that takes place in the winding resistance of a transformer is known as the copper loss.

The iron loss highly relies upon the material that is picked for the transformer core, which is termed as hysteresis loss and eddy current loss. The hysteresis losses are related to the power which is required to magnetize and demagnetize of the core. On the other hand, the eddy current losses are the result of small currents that appear in the core due to the magnetic AC field.

### 3.4.1 Core Losses

There are a number of methods available in the literature, which discusses the magnetic loss determination [21]. These methods can be categorized into three main models.

- Hysteresis Models
- Loss separation approach
- Empirical methods

The Hysteresis models are based on the Jiles-Atherton or Preisach Models. One of them uses a macroscopic calculation whereas others introduced a statistical approach for the description of time and space distribution of a domain-wall motion [21]. The Loss separation model has introduce the contribution of three different effects of the magnetization losses which are static hysteresis loss, eddy current loss, and excess eddy current loss. Empirical approaches are based on the Steinmetz equation commonly known as curve-fitting expression for the measured data.

Although hysteresis models and loss separation models can be considered for adequate results they need extensive computations. On the other hand, the empirical methods based on the Steinmetz equations uses the manufacturers provided data with a simple expression to determine the magnetic losses.

**Original Steinmetz equation**

Steinmetz introduced a general expression to characterize the core losses which is usually used in the design of magnetic power devices namely transformers, electrical machines, and inductors. It is also known as the Original Steinmetz Equation (OSE), based on the curve fitting approach of the measured data under the sinusoidal excitation [21].

$$P_v = K f^{\alpha} \hat{B}_m^{\beta} \tag{3.23}$$

where $K, \alpha$ and $\beta$ are the coefficients based on the material characteristics. $\hat{B}_m$ is the peak magnetic flux density and $f$ is the frequency.

A major drawback of (3.23) is that it is only valid for sinusoidal waveforms [21]. However, power electronic converters inductors and transformers are usually subjected to non-sinusoidal rectangular waveforms having positive, negative and zero amplitudes. This results in the ramping up/down and constant flux in the core of the transformer [22].

It has also been proven that for a non-sinusoidal waveform, the losses are high compared to a sinusoidal waveform, though the frequency and peak flux density are the same [21]. The limitation of the OSE is overcomed by the introduction of the modified forms of Steinmetz equation which are useful for a wide variety of waveforms.

**Modified Steinmetz equation**

For the analytical estimation of the ferrite core losses in the transformer, the following modified Steinmetz equation for rectangular voltages [23], [21] is used.

$$P_{Fe} = C_m f^{\alpha} B^{\beta} (c_o - c_1 T_T + c_2 T_T^2) V_{Fe} \tag{3.24}$$

where $P_{Fe}$ is a power losses generated in the core [mW], $C_m, f, B$ are a polynomial coefficients, frequency and peak value of the flux density respectively. $T_T$ is a core temperature [°C], $c_0, c_1, c_2$ are temperature effect coefficients and $V_{Fe}$ is effective core volume [$cm^3$].

### 3.4.2 Copper Losses

In modern power electronic converters, a high switching frequency is used. This results in a reduced transformer and inductor size. This, however, introduces skin, proximity, and fringing flux effects [23]. Also because of non-sinusoidal current waveforms, additional copper losses occur due to harmonics.

The winding creates different resistances for each frequency component, it is therefore important to accurately estimate the resistance of the windings subjected to high frequency currents. The actual resistance of the winding to a high frequency current is called AC-resistance. Under high frequency excitation, the copper losses is given as,

$$P_{cu} = I_{rms}^2 R_{AC} \tag{3.25}$$

where $R_{AC}$ is the AC resistance of the windings and can be expressed as

$$R_{Ac} = F_{AC} R_{DC} \tag{3.26}$$

where $R_{DC}$ is the DC-resistance and $F_{AC}$ is the factor which shows the increase in the DC resistance due to skin and proximity effects caused by the high frequency components.

The DC resistance of the windings can be calculated approximately as

$$R_{DC} = \frac{\rho l}{A_{cond}} \tag{3.27}$$

where $\rho$ is the resistivity in ohms, $l$ is the length of conductor in $m$ and $A_{cond}$ is the cross sectional area of the conductor in $mm^2$.

The transformer primary winding loss is given by

$$P_{pri} = I_{pri,rms}^2 \, R_{AC\_pri} \tag{3.28}$$

The secondary transformer winding loss is

$$P_{sec} = I_{sec,rms}^2 \, R_{AC\_sec} \tag{3.29}$$

Then the total conduction loss of the transformer is given by

$$P_{cu} = P_{pri} + P_{sec} \tag{3.30}$$

## 3.5 Thermal Model

Due to the self-heating effect, the junction temperature of a power device is significantly higher than the ambient temperature. Hence, the maximum power loss of a power device is typically limited by the maximum junction temperature. Furthermore, the device switching and conduction losses are the cause to raise its junction temperature and an increasing junction temperature leads to more device losses [24]. The conduction losses of a power MOSFET and a diode can be calculated using the drain-source on-state resistance as (3.15) and (3.16).

For most power semiconductors, the device temperature usually has some influence on the on-state resistance due to the thermal runaway. In some cases, the power dissipated in this resistance causes more heating of the junction, which leads to higher junction temperature and this is called thermal runway as shown in Figure 3.7.

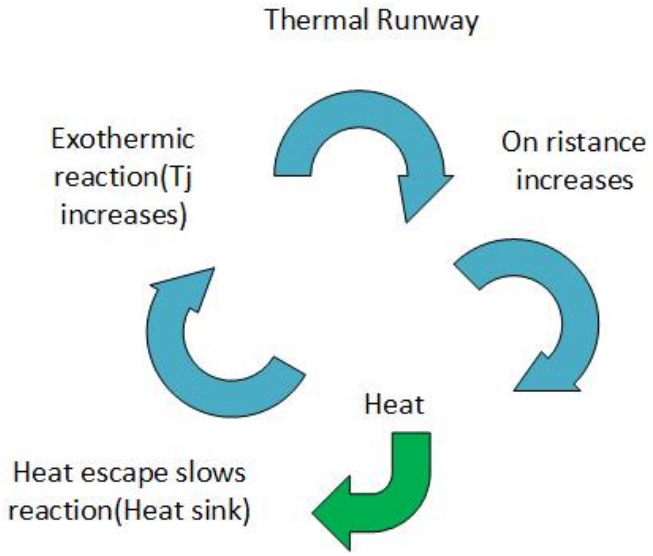



**Figure 3.7:** Diagram of Power MOSFETs thermal runaway

If a power MOSFET produces more heat than the heatsink can dissipate then the thermal runaway can damage the device. This problem can be reduced by lowering the thermal resistance between the transistor die and the heat sink [25].

The typical on-resistance of a MOSFET can usually be obtained from the data-sheet diagram as shown in Figure 3.8.

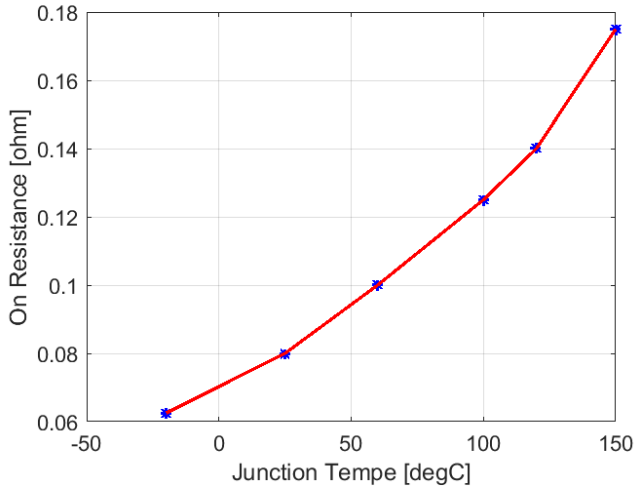



**Figure 3.8:** On-resistance with junction temperature

Figure 3.8 shows that the typical on-resistance of power device obtained from the datasheet which shows the relation between on resistance and junction temperature for the Si-MOSFET SPW47N60CFD.

### 3.5.1 Equivalent Thermal Model

The equivalent thermal model is fundamental in the analysis of thermal modeling. The heat flow can be modeled by analogously to an electrical circuit where heat flow is represented by the current, temperatures are represented by voltages, heat sources are represented by constant current sources, and absolute thermal resistances are represented by resistors as shown in Figure 3.9. Under the assumption of a one-dimensional heat flow, the thermal resistance ($Rth$) of a piece of material is generally given by

$$Rth = \frac{d}{\lambda A} \tag{3.31}$$

where $d$ is the length of the heat path, $A$ is the heat conducting area and $\lambda$ is the thermal conductivity of the material.

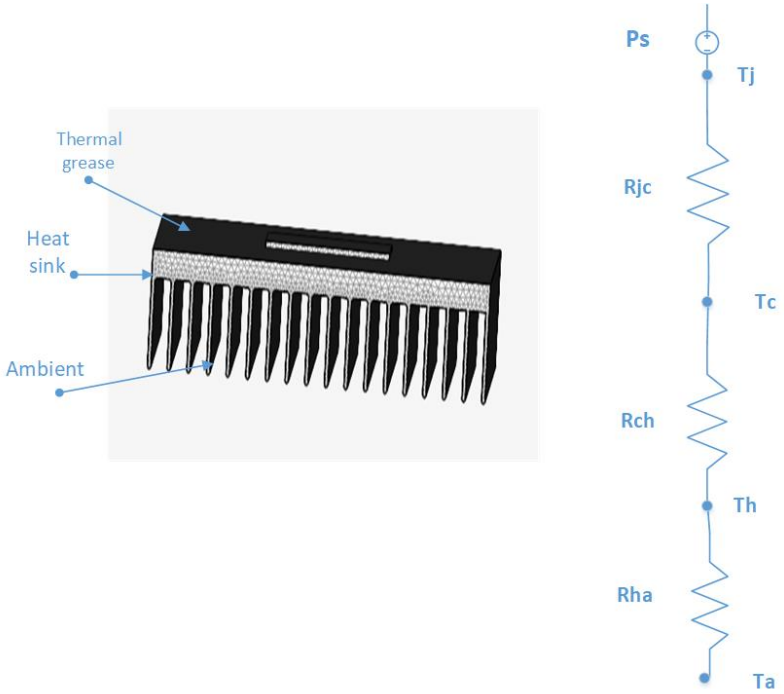



**Figure 3.9:** Equivalent thermal model

Figure 3.9 shows a typical heat sink which used for mounting the power device and its steady-state thermal equivalent circuit. For the thermal circuit to be stable, the following equation must be fulfilled,

$$T_j = P_{loss} Rth_{ja} + T_a \tag{3.32}$$

where $T_j$ is the device junction temperature, $T_a$ is the ambient air temperature, $P_{loss}$ is the device power loss, and $Rth_{ja}$ is the total junction-to-ambient thermal resistance.

The thermal resistance $Rth_{ja}$ can be divided in three parts:

$$Rth_{ja} = Rth_{jc} + Rth_{cs} + Rth_{sa} \tag{3.33}$$

Based on this theory, the thermal model for the converter is modelled in Section 4.5.

# 4
# Method

## 4.1 Design Specifications

For this thesis work, the specification for the DC/DC converter is shown in Table 4.1 and the selection of specific parameters will be discussed on the following sections.

**Table 4.1:** Specifications of the converter

| | |
|---|---|
| Input DC voltage | 240 V |
| Output DC voltage | 10 V-18 V |
| Nominal output voltage | 12 V |
| Output power | 2 kW |
| Output voltage ripple | 2% of output voltage |
| Switching frequency | 100 kHz |
| Efficiency | over 95% |

### 4.1.1 Operation Frequency

In a power conversion system, the high frequency operation is preferred to reduce weight and noise [19]. In order to analyze an appropriate switching frequency for the MOSFET and high frequency transformer, the losses in the MOSFET, high frequency transformer and volume of the transformer have been studied for different frequencies.

### 4.1.2 Leakage Inductance of the Transformer

The phase-shift angle of the DAB DC/DC converter varies from 0 to 90 degrees for positive power flow. Therefore, for the given design specification $P_o = 2$ kW, $V_1 = 240$ V, and $f_s = 100$ kHz, the phase-shifted angle $\phi$ is varied from 0 to 90 degrees to minimize the High Frequency Transformer (HFT) current associated with a given output voltage. The output voltage varies from 10V to 18V, which corresponds to the voltage ratio d varies from 0.8 to 1.5.

Voltage ratio is calculated using the transformer ratio by considering the nominal output voltage. For each value of $\phi$, the resultant leakage inductance for the power transfer and the HFT current are computed, respectively, using (3.4) and (3.3) as shown in Figure 4.1 and Figure 4.2.

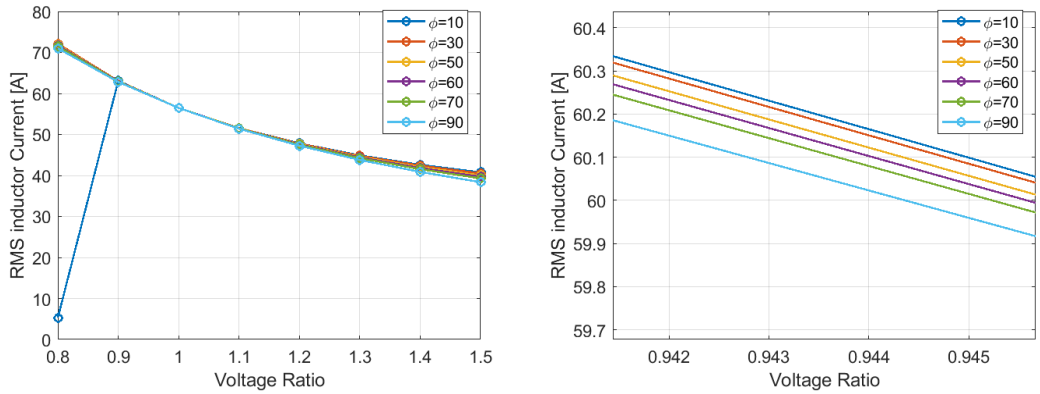
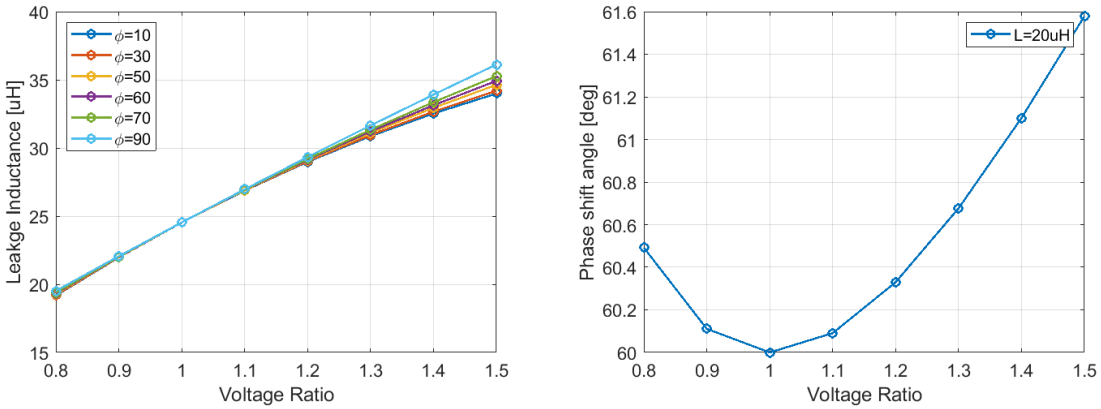



**Figure 4.1:** Variation of inductor current with phase shifted angle and voltage ratio, $V_i$=240 V, $P$=2 kW

From Figure 4.1, the optimum phase shift angle of 60 degree is selected which can result in optimum inductor current for a full range voltage ratio from 0.8 to 1.5.




**(a)** Leakage inductance versus voltage ratio for different phase shift angle

**(b)** Phase shift angle versus voltage ratio for L=20$\mu$H

**Figure 4.2:** Selection of leakage inductance

Figure 4.2 (a) illustrates the variation of the leakage inductance from 20$\mu$H to 35$\mu$H when the voltage ratio varies from 0.8 to 1.5 for the phase shifted angle of 60°. Since a leakage inductance of 20$\mu$H has a low current which is calculated using (3.3), for phase shifted angle of 60°, this inductance value will be used for 100 kHz. Using (3.5) the phase shift angle can be calculated for the selected leakage inductance of 20$\mu$H which is shown in Figure 4.2 (b). From the Figure 4.2 (b), for phase shifted angle of 60°, the voltage ratio is 1.

### 4.1.3 Output Capacitor

The output capacitor allows to stabilize the output voltage. A big capacitor allows to control a stable voltage with only low ripple. The allowed Voltage ripple is 2% of

the output voltage and the output capacitor is calculated as

$$C = \frac{50 I_{Load}}{V_o f} \tag{4.1}$$

where $I_{Load}$ is 166.6A for the rated power of 2 kW and output voltage of 12 V, f is switching frequency of 100 kHz. Based on this values the output capacitor is calculated as 6.9 mF.

## 4.2 Semiconductor Component Selection

Power semiconductor devices such as IGBTs and MOSFETs are key components in power electronic systems for a hybrid electric vehicle. Although the MOSFET is prefered for a higher swiching frequency, for a switching frequency less than 50kHz and a high rated voltage, IGBTs are typically selected [19].

On the high voltage side, in order to enable a high switching frequency and to achieve low losses, the SPW47N60CFD Si MOSFET has been selected due to its low on state resistance and fast switching speed [26]. It has a rated voltage of 600 V and the maximum conduction current is 46 A at 25 °C. In the case of using a SiC MOSFET, the SCT3080AL [27] has been selected for the high voltage side.

On the low voltage side, the maximum blocking voltage of each switch is 18 V. However, due to over-voltage spikes during turn off switching, a Si MOSFET with a rated voltage of 40 V is selected. Hence, the IRF2804 is chosen due to a low on state resistance of 2.2 mΩ. For the SiC MOSFET, the SCT3017ALHR is selected with a rated voltage of 650V and on-state resistance of 17 mΩ.

## 4.3 High Frequency Transformer Design

The DAB converter, as shown in Figure 3.2, comprises of two full bridges connected by a transformer and a coupling inductor. Each bridge is connected to a DC bus of a low and high voltage respectively. Each bridge is controlled to produce a square wave with high frequency at the AC terminals. The bidirectional energy flow is governed by the transformer and the coupling inductor, and flows from the bridge to produce the square wave.

The design of a high frequency transformer requires an appropriate selection of a ferrite core and considerations because of the skin effect impact. To make the isolated DC to DC converter minimized, the transformers should have the following characteristics [28].

- High turn ratio to match the voltage difference between the LV input and HV DC bus.
- High current handling capability.
- Compact size due to the limited space.

To design a high frequency transformer, four main steps are followed as shown in Figure 4.3.

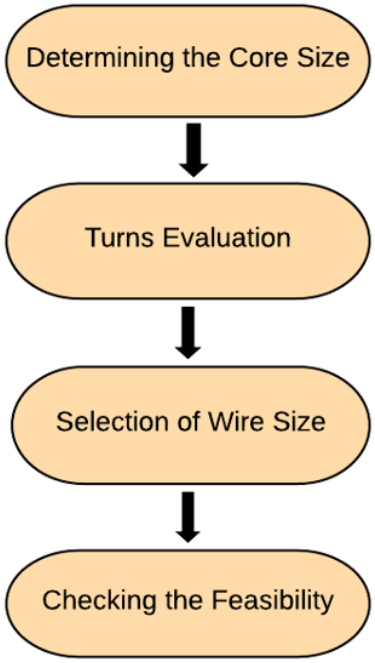



**Figure 4.3:** Flow Chart of High Frequency Transformer Design

### 1. Determining the Core Size

For the high frequency transformer, an E-type ferrite core is typically utilized as the transformer core. Moreover, as the initial step of the transformer design, the core selection can be made through an iterative process including trial solutions, but the equation below gives an approximation of the core area product, $A_P$, required for the application [22]. At that point, it was necessary to choose the core available from the catalog data, whose area product exceeds the calculated value. The area product $A_P$ of the high frequency transformer is

$$A_p = A_w A_e = (\frac{P_o}{K f_s B})^{(4/3)} cm^4 \tag{4.2}$$

where $A_e$ is the magnetic cross section ($cm^2$), $A_w$ is the window area ($cm^2$) for selected core size, $P_o$ is the output power of the DC/DC converter ($W$), $B$ is the variation of flux density ($T$), $f_s$ is the operating frequency of the DAB converter (Hz), and $K$ is the factor parameter.

Once $A_P$ is found, the transformer core size can be selected from the manufacturer's datasheet [29]. Figure 4.4 shows the selected E-type ferrite core geometry which can have different dimension for different core size and frequencies. After the core size has been found, the following core parameters need to be taken from the datasheet for further calculations of the mean length turn (MLT), core area and window area.

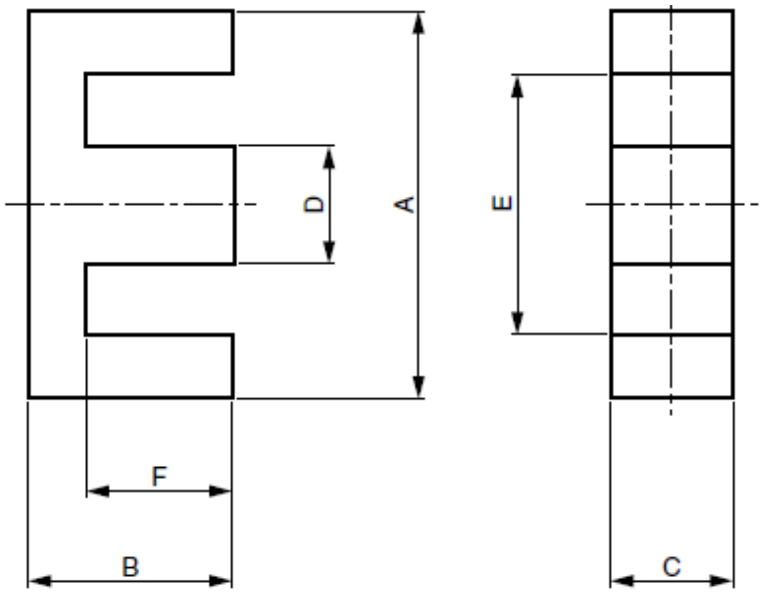



**Figure 4.4:** Geometric dimensions for E-type ferrite core

Based on the rating of the transformer and the switching frequency, the 3C96 ferrite material is selected due to their large flux cross-section area and winding window width. To select the core material, transformer core datasheet are used [29]. From the datasheet, it is possible to find the performance factor as a function of frequency for different ferrite materials. From this data, the 3C96 ferrite material has a high performance for frequencies between 25 kHz to 100 kHz.

Following this step, the turns of the primary and secondary sides are evaluated. Then, the wire crossectional area is calculated for the primary and secondary side to select the appropriate wire size. Based on these two steps, it was possible to calculate the total required area and compare the results with the window area of the selected core size for the specific frequency. If the window area is sufficient for the winding, this means that the selected core is an appropriate choice.

**2. Turns Evaluation**

The number of primary and secondary turns can be found by using Faraday's law,

$$N_1 = \frac{V_{in}}{K_f f B A_C} \tag{4.3}$$

$$N_2 = \frac{N_1 V_o}{V_{in}} \tag{4.4}$$

where $A_c$ is the core area for the selected core size , $B$=0.1-0.2 T, $K_f$=4 for copper and $f$=25 kHz-100 kHz

**3. Selection of wire Size**

To select the appropriate wire size, the wire area of primary and secondary side should be calculated. They can be calculated by using (4.5) and (4.6) as,

$$A_{w(p)} = \frac{I_p}{J} \tag{4.5}$$

$$A_{w(s)} = \frac{I_s}{J} \tag{4.6}$$

After the wire areas are determined, these values are utilized to find the appropriate wire gauge number (AWG), which can be selected from the table given in [30]. Since a high frequency transformer is being designed, as opposed to a low frequency transformer, it is highly recommended to use litz wires instead of solid wires. From [31], it is known that the litz wires reduce skin effect losses and consequently winding loss because they consist of multiple isolated strands and each strand has the diameter which is equal or smaller skin depth diameter which can be calculated as

$$D_{skin\_Depth} = 2\delta \tag{4.7}$$

where $D_{skin\_Depth}$ diameter of the single strand in wire and $\delta$ is skin depth which can be calculated as

$$\delta = \frac{6.62}{\sqrt{f}}K \tag{4.8}$$

where $f$ is an operating frequency of the transformer and $K$ is skin depth coefficient, which equals to 1 for the copper.

The MLT of the wire wound can be calculated as follows [31]:

$$MLT_{wire} = 2(C + D) + (\frac{E - D}{2})(2 - \pi) \tag{4.9}$$

where C, D and E are core dimensions that can be found in Figure 4.4.

Then, the primary and secondary DC winding resistances are used to calculate windings loss in the transformer. They can be calculated as follows [31]:

$$R_P = MLT.N_p.\frac{\mu\Omega}{cm}10^{-6}[\Omega] \tag{4.10}$$

$$R_s = MLT.N_s.\frac{\mu\Omega}{cm}10^{-6}[\Omega] \tag{4.11}$$

where $\frac{\mu\Omega}{cm}$ is the winding resistance of the conductor, which can be obtained from [30].

In this case, since the primary and secondary side of the transformer currents are 8.3 A and 166 A respectively. The wire areas are determined using (4.5) and (4.6) as 2.63 $mm^2$ and 45.6 $mm^2$ for the primary and secondary side with the consideration of current density of 3.8 $A/mm^2$. Consequently, the wire gauge number (AWG) is determined, which can be selected from the table given in [30]. From the table

AWG-15 and AWG-1 are selected for the primary and secondary side respectively which depends on the wire areas.

**4. Checking the Feasibility**

Once the ferrite core and winding area have been decided, it is then necessary to verify whether the transformer core window area is large enough to host the wires. The core size can be determined whether it has sufficient winding area or not for the winding using the following relation,

$$A_{w(p)}N_p + A_{w(s)}N_s < K_w A_W \tag{4.12}$$

where $k_w$ is winding factor which is 0.5 for transformer and $A_W$ is the window area for the selected core size.

Using this relation, if it is true, then the window area of selected core size is sufficient for the winding, otherwise the core size should be changed.

Based on the procedures which are discussed above, the core size for the frequencies of 25 kHz, 50 kHz, 75 kHz and 100 kHz are determined and presented in Table 4.2. Moreover, the following core parameters need to be taken from the data sheet for further calculations of core area, window area and volume of the core.

**Table 4.2:** Selected transformer core data [29]

| Frequency | 25 kHz | 50 kHz | 75 kHz | 100 kHz |
|---|---|---|---|---|
| Core size | EE 80/76 | EE 55/55B | EE 56/47 | EE 49/48 |
| B [T] | 0.2 | 0.16 | 0.13 | 0.1 |
| A [mm] | 80.1 | 55 | 56.6 | 49.07 |
| B [mm] | 38.1 | 27.8 | 23.6 | 23.77 |
| C [mm] | 19.8 | 25 | 18.7 | 15.62 |
| D [mm] | 19.8 | 17.2 | 18.7 | 15.62 |
| E [mm] | 62.2 | 37.5 | 38.1 | 31.37 |
| F [mm] | 28.2 | 18.5 | 14.8 | 15.24 |
| $A_c$ [mm$^2$] | 392 | 417 | 352 | 245 |
| $A_w$ [mm$^2$] | 1480 | 400 | 292 | 250 |
| $V_c$ [mm$^3$] | 69800 | 52000 | 36700 | 28200 |

Then, using the transformer core size which is given in Table 4.2, the MLT of wire is calculated using (4.9) and presented in Table 4.3. Moreover, the DC resistance and the length of the wire on the primary and secondary side are determined using (4.10) and (4.11).

**Table 4.3:** Transformer winding parameters

| Frequency | 25 kHz | 50 kHz | 75 kHz | 100 kHz |
|---|---|---|---|---|
| $MLT_{wire}$ [m] | 0.188 | 0.136 | 0.124 | 0.103 |
| Wire length (Primary) [m] | 7.52 | 2.72 | 2.48 | 2.06 |
| Wire length (Secondary) [m] | 0.376 | 0.136 | 0.124 | 0.103 |
| $R_p$ [m$\Omega$] | 49.3 | 17.8 | 16.2 | 13.5 |
| $R_s$ [m$\Omega$] | 0.142 | 0.051 | 0.046 | 0.038 |

The final stage of the design is the determination of the loss existing in the transformer for the specific core size and it is presented in Section 5.2.

## 4.4 Power Flow Controller (PFC)

A bidirectional DC/DC converter is used for the DC/DC conversion process. In the DAB, the converter has two full bridge circuits, one act as inverter and the other are as rectifier. To limit the negative inductor current in the DAB converter (Figure 3.5), the Double Phase Shift (DPS) control technique is selected for power transfer [32].

In DPS control, the HV and LV bridges produce a three-level AC output and are connected back-to-back via a transformer as shown in Figure 3.2. In Figure 3.2, $S_1, S_2, S_3$ and $S_4$, are HV-bridge switches and $S_5, S_6, S_7$ and $S_8$ are LV bridge switches. These switches operate according to trapezoidal modulation schemes with a phase shift in the LV and HV bridges as shown in Figure 3.4.

### 4.4.1 Operation of DAB Converter in DPS Control

In the DAB converter, there are two modes of operation for power transfer between the input and output side, namely forward mode and reverse mode. The three-level voltage waveforms of HV and LV bridges are shifted to either lag or lead, depending upon the mode of operation. The phase shift is lagging in forward operation and leading in the reverse operation. And the transmission of power between the input side and output side is controlled by adjusting $d_1$ and $d_2$ as shown in Figure 4.5.

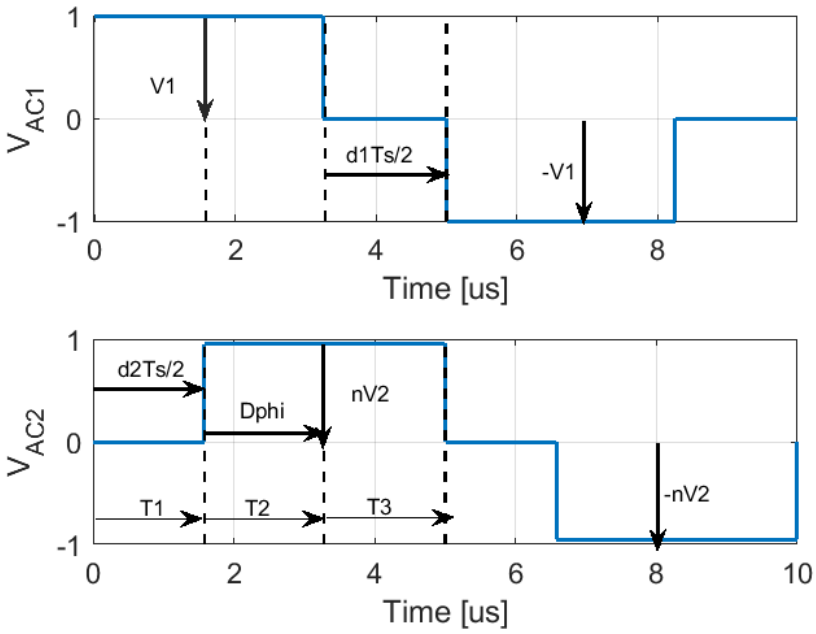



**Figure 4.5:** Operating principle of power flow control

For the dual phase shift control, there are two condtions: (a) $0<=d_1<=d_2<=1$, and (b) $0<=d_2<=d_1<=1$ , where, $d_1$ is inner phase shift duty ratio and $d_2$ is outer phase shift duty ratio. And the range of $d_1$ and $d_2$ should be between 0 and 1, while the summation of $d_1$ and $d_2$ should not be greater than or equal to 1 [32]. The power transfer depends upon the current flow through the inductor L. The inductor current increases or decreases according to the voltage across the inductor and its polarity.

### 4.4.2 Implementation of PFC

The instantaneous input and output current and voltage of the DAB converter is measured and fed back to the power flow controller to achieve closed-loop control operation. Figure 4.6 and Figure 4.7 show the implementation of the power flow controller for the dual active bridge converter in MATLAB/SIMULINK.

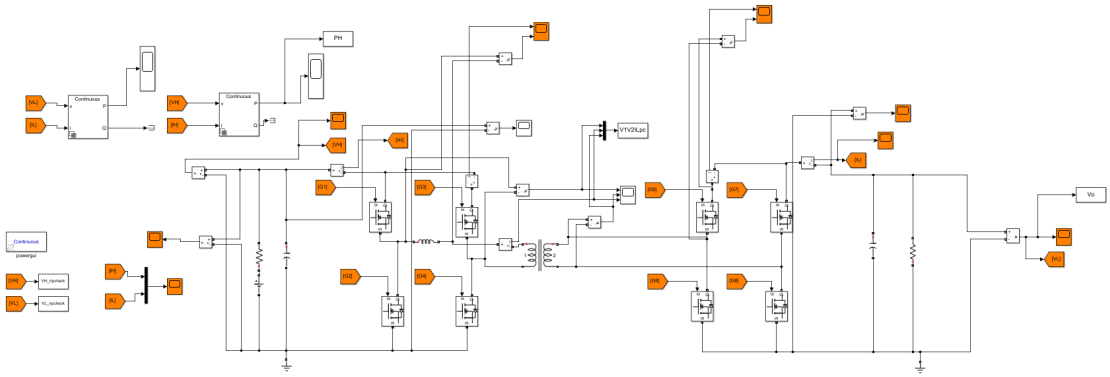


**Figure 4.6:** Dual active bridge circuit in MATLAB/SIMULIK

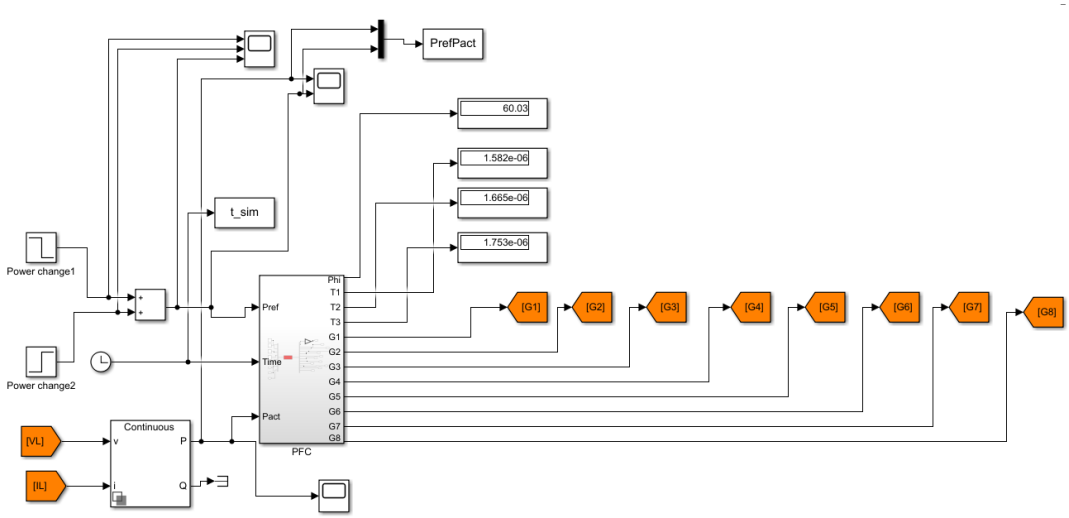



**Figure 4.7:** Power flow controller circuit

Figure 4.7 shows the power flow controller circuit which receive the actual transfered power ($Pact$) from the output side of the DAB circuit as output voltage and output current of the DAB. Then it is compared with the reference power, in this case with the rating power of 2 kW. Figure 4.8 shows the flow chart of the power flow controller (PFC). It shows the control algorithm and describes how the PFC generates control variables $d_1$ and $d_2$.

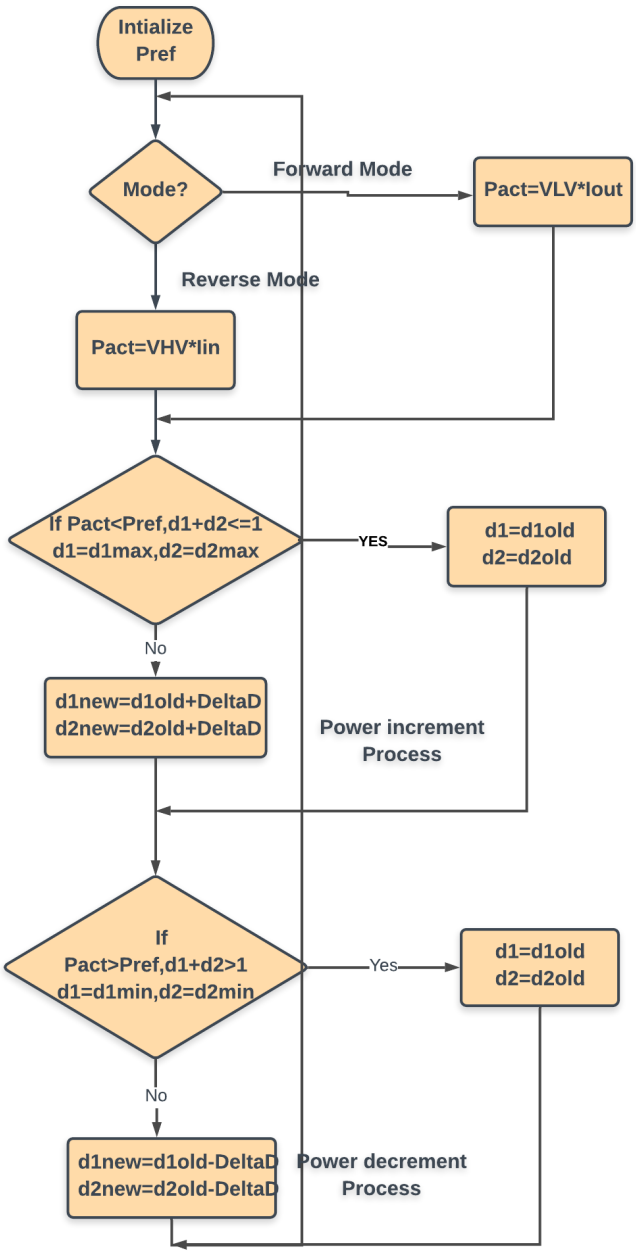



**Figure 4.8:** Flow chart of power flow controller

After initializing the reference power, the actual power transferred is calculated for the forward or reverse mode of operation, depending upon the mode of operation signal. The relation between the power levels determines the action of the PFC as shown in the flow chart of power flow controller.

In the controller, $d_{1max}$=$d_{2max}$ =0.5, $d_{1min}$=$d_{2min}$ =0 and $\Delta d$ is the step ratio of $d_1$ and $d_2$, which is chosen as 1 to 2% of $d_{1max}$ or $d_{2max}$. This scheme generates $d_1$ and $d_2$ as a consequence of sudden changes in the power reference.

## 4.5 Thermal Model for Heat Sink

The dominant heat generators in a DAB are the transformer, LV, and HV semiconductor bridges while the losses in the capacitors, control system, and semiconductor drivers are considerably lower. The losses generated in the semiconductor devices (conduction, and switching losses) have to be dissipated to the ambience via a heat sink, which usually significantly affects the system volume.

Losses in one semiconductor device are dissipated via the series connection of the internal thermal resistance of the device $Rth_{jc}$ and the thermal resistance of the electrical as insulating material between the devices and the heat sink $Rth_{ch}$ as shown in Figure 3.8. Therefore, the different losses shares of the devices sum up and are transferred via the heat sink to the ambient. The heat conduction of a semiconductor can be simulated as an electric circuits as shown in Figure 4.9.

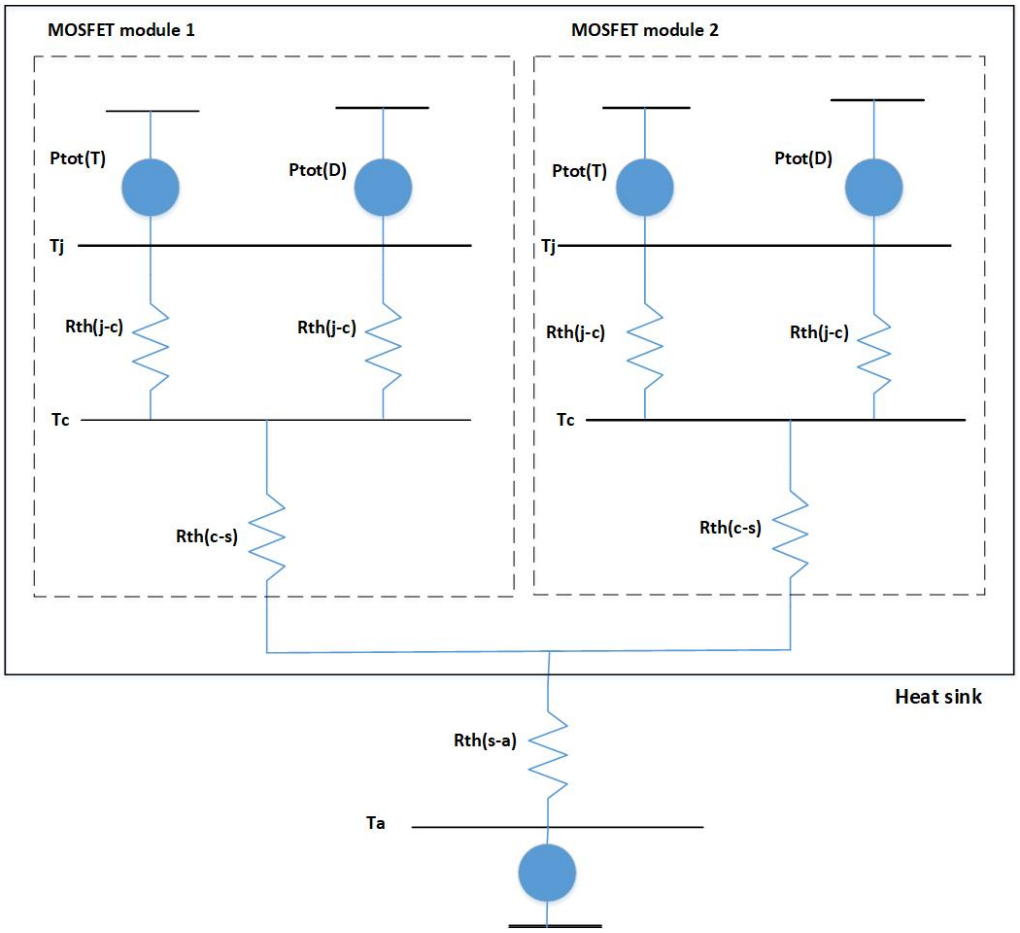



**Figure 4.9:** Thermal model for the DAB converter

The thermal model shown in Figure 4.9 is the same for both bridge heat sinks. Using the equivalent circuit, the heat sink, case, and junction temperature can be calculated using the following thermal equation. By knowing the power losses of each MOSFET and diode, the dissipated power in the thermal resistance is known.

Heat sink temperature

$$T_s = n_1(P_{tot}(T) + P_{tot}(D))Rth_{s\_a} + T_a \tag{4.13}$$

Case temperature

$$T_c = n_2(P_{tot}(T) + P_{tot}(D))Rth_{c\_s} + T_s \tag{4.14}$$

Junction temperature

$$T_j(T) = (P_{tot}(T) + P_{tot}(D))Rth_{j\_c} + T_c \tag{4.15}$$

where, $Rth_{j\_c}$ is junction-case, $Rth_{c\_s}$ is case-heat sink, $Rth_{s\_a}$ is heat sink-ambient thermal resistance, $n_1$ represents all components of power loss on the heat sink and $n_2$ is all components of power loss in the module.

As a starting point, assume an ambient temperature of 40°C. Using the manufacturer's datasheet, the maximum temperatures of the semiconductors is determined. Also set the junction-case thermal resistance, $Rth_{j\_c}$ and case-heat sink thermal resistance, $Rth_{c\_s}$.

Using the calculated losses, we can determine the thermal resistance that is required to keep the heat sink temperature. The calculated junction temperatures should not exceed the maximum values for $T_j(T)$ given from the manufacturer. For example, in case of the SPW47N6CFD MOSFET module, the maximum temperature $T_j(T)$ is 150°C.

For transferring the heat to the ambient, two types of air cooling are distinguished: forced air cooling and free (natural) convection cooling. The benefits of free convection include low cost of implementation, no need for fans, and the reliability of the cooling process. Compared to forced air cooling, however, free convection will need more heat sink volume to attain an equivalent temperature. In case of forced air, it can make a great difference in cooling efficiency. Heat sink to air thermal resistance can be improved by using suitable heat sinks. For both types of cooling, the thermal resistance of the heat sink $Rth_{hs}$ is determined based on analytical equations, and presented in Section 5.5.

# 5
# Results and Analysis

In the previous sections, a DAB converter has been designed and studied. In this section, the analytical results of semiconductor loss and efficiency comparison will be made with different switching frequencies for both Si MOSFETs and SiC MOSFETs. In addition, the losses in the transformer which are core loss and winding loss will be analysed for different frequencies.

Morover, from the simulation design, the power flow controller has been tested by changing the reference power level and changing the direction of the power flow.

## 5.1 Loss Comparison and Efficiency

The semiconductor losses consisting of switching loss and conduction loss for the Si MOSFET and SiC MOSFET are compared for the selected MOSFET. The selected MOSFET for the high voltage side and low voltage side is shown in Table 5.1 with their respective on state resistance.

**Table 5.1:** Selected Si MOSFET and SiC MOSFET

| Component(MOSFET) | Part no. | On resistance [Ω] at $T_j = 25°C$ | Quantity |
|---|---|---|---|
| HV Si MOSFET | SPW47N6CFD | 0.07 | 4 |
| LV Si MOSFET | IRF2804PbF | 0.002 | 4 |
| HV SiC MOSFET | SCT3080AL | 0.008 | 4 |
| LV SiC MOSFET | SCT3017ALHR | 0.017 | 4 |

The leakage inductance of the transformer are calculated for the rated power of 2 kW using (3.4) for different switching frequencies and presented in Table 5.2.

**Table 5.2:** Leakage inductance for different frequency

| Switching frequency | 25 kHz | 50 kHz | 75 kHz | 100 kHz |
|---|---|---|---|---|
| Leakage inductance | 98.1 $\mu$H | 49.1 $\mu$H | 32.7 $\mu$H | 20 $\mu$H |

The conduction loss is calculated based on the rms inductor current. The rms current is calculated from the instantaneous inductor current which is calculated using (3.3) as,

$$i_L(t_1) = i_L(t_0) + \frac{1}{L}(\int_{t0}^{t1} V_R\, dt), t_0 < t_1$$

$$= i_L(t_0) + \frac{1}{2L}(V_R(t_o) + V_R(t))$$

The resulting voltage $V_R$ and instantaneous inductor current is shown in Figure 3.5 for one full period.

Consider the switching frequency of 100 kHz to calculate the conduction loss. The rms inductor current is calculated using the inductor current waveform as 9.56 A for the rated power of 2 kW, and an input output voltage of 240 V and 12 V. Here, the actual transferred power is approximately 1.95 kW for the phase shift angle of 60° and leakage inductance of 20 $\mu$H. The time interval $T_1$, $T_2$ and $T_3$ are calculated using (3.6)-(3.8) as 0.5 $\mu$s, 1.6 $\mu$s and 2.9 $\mu$s respectively.

As a result, each of the 4 switches on the HV side carries the RMS current $I_{S1}$,

$$I_{s1} = \frac{I_L}{\sqrt{2}} = 6.7A$$

Similarily, each of the 4 switches on the LV side carries the rms current $I_{S2}$,

$$I_{s2} = \frac{nI_L}{\sqrt{2}} = 67.6A$$

The diode forward voltage $V_{sd}$ is extracted from the data sheet of the selected Si-MOSFET (Table 5.1) as 1V and 1.3V for the high voltage and low voltage side respectively.

Consequently, the primary conduction loss for the full bridge is calculated as

$$P_{s1,cond} = 4(R_{s1}I_{s1}^2 + V_{sd}I_{on,avg})$$
$$P_{s1,cond} = 4(0.07\Omega * 6.7A^2 + 1.0V * 0.0185A) = 12.87W$$

Similarily, the secondary conduction loss for the full bridge is calculated as

$$P_{s2,cond} = 4(R_{s2}I_{s2}^2 + V_{sd}nI_{on,avg})$$
$$P_{s2,cond} = 4(0.002\Omega * 67.6A^2 + 1.3V * 10 * 0.0185A) = 37.5W$$
$$Total_{cond\_loss} = 5.4W + 31.3W = 50.4W$$

Switching loss is calculated based on Section 3.3.2 using (3.17) to (3.20). Since the MOSFETs turn on at zero voltage in trapezoidal modulation, only the turn off energy is considered for calculating the switching losses.

First, the secondary side of the Si MOSFETs is considered to calculate the switching loss. From (3.19), the turn off energy can be calculated using the off time which is the summation of turn off delay time and fall time. The turn off delay time and fall time are approximately calculated using the datasheet [26], i.e 130ns and 110ns respectively under a voltage of 20 V and current of 75 A. As a result the turn off energy on the secondary side MOSFET is calculated as 24 mJ.

In the case of using a primary side MOSFET, the turn off delay time and fall time are approximately calculated as 100ns and 20ns respectively under a voltage of 400 V and current of 46 A. As a result the turn off energy on the primary side MOSFET is found as 12 mJ.

Then, the turn off losses on the secondary side in the case of 100 kHz is calculated as [33],

$$P_{sw\_turnoff\_sec} = \frac{E_{off\_sec} I_{pk\_sec} V_o f}{V_{nom} I_{nom} \pi} = 14.4W \tag{5.1}$$

where $E_{off\_sec}$ is the turn off energy on the secondary side, $I_{pk\_sec}$ is the peak current on the secondary side, and $V_{nom}$ and $I_{nom}$ are nominal voltage and current which are obtained from the datasheet as 20V and 75A respectively.

Correspondingly, the turn off loss on the primary side is found as,

$$P_{sw\_turnoff\_prim} = \frac{E_{off\_pri} I_{pk\_pri} V_i f}{V_{nom} I_{nom} \pi} = 0.58W \tag{5.2}$$

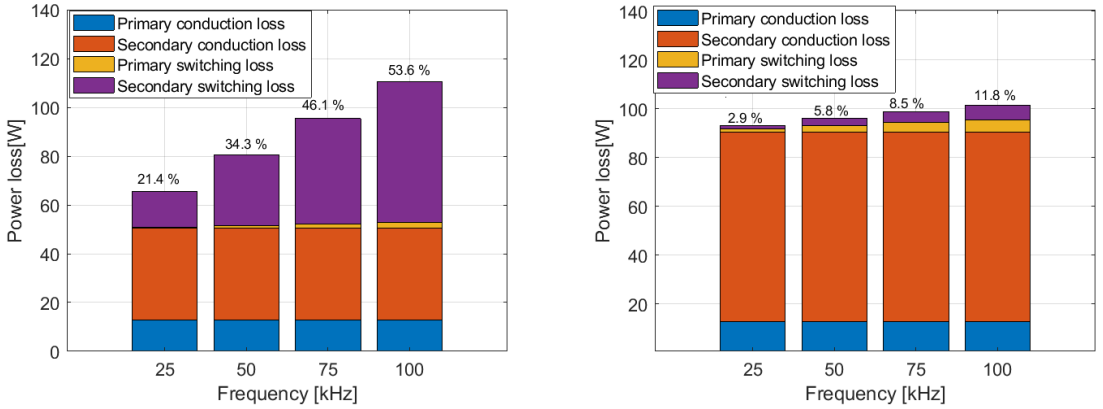
where $E_{off\_pri}$ is the turn off energy on the primary side which is calculated as 12 mJ, and $V_{nom}$ and $I_{nom}$ are nominal voltage and current which are obtained from the datasheet as 400 V and 46 A respectively.

Consequently, the total turn off switching losses in the primary and secondary side across all eight switches becomes 59.9 W.

In the case of using a SiC MOSFET, the conduction loss on the primary and secondary side is increases to 12.89 W and 78.65 W respectively. Since the secondary side of SiC MOSFET (SCT3017ALHR) has a higher on resistance and due to high current on the low voltage side, the conduction loss on the secondary side becomes higher compared to that of the Si MOSFET. The turn off energy on the primary and secondary side are found as 43 $\mu$J and 25 $\mu$J respectively. Consequently the turn off losses on the primary and secondary side MOSFETs are strongly decreases to 5.16 W and 6 W for the switching frequency of 100 kHz.

Each losses on the primary and secondary side is calculated for different switching frequencies and presented in Figure 5.1. Figures 5.1 (a) and (b) shows the comparison of conduction loss and switching loss for the frequencies, 25 kHz, 50 kHz, 75 kHz and 100 kHz for the Si MOSFET and the SiC MOSFET.

From Figure 5.1 (a), it can be seen that, the switching loss for the MOSFET increases as the switching frequency increases where as the conduction loss is almost equal for different switching frequencies. For instance, the switching loss for 25 kHz is 21% of the total loss whereas for 100 kHz, it increases to 54% of the total loss since the turn off losses in the primary and secondary side is directly affected by the frequency as can be seen from (5.1) and (5.2).




**(a)** Loss comparison for Si MOSFET **(b)** Loss comparison for SiC MOSFET

**Figure 5.1:** Loss comparison for Si MOSFET and SiC MOSFET

In the case of a SiC MOSFET, the switching loss increases as the switching frequency increases. This is the same case for a Si MOSFET. However, in the case of SiC MOSFET, it is substantially reduced due to a lower value of voltage rise time (turn off delay) and current fall time in the SiC MOSFET. Thus, the total loss is lower for the higher switching frequency of 75 kHz and 100 kHz. For instance, when the switching frequency is 100 kHz, the switching loss reduces from 53% to 12% of the total loss and conduction loss increases from 47% to 88% of the total loss. Thus, the Si MOSFET is better in terms of conduction power loss while switching power loss of SiC MOSFEET are significantly lower. As a result, the efficiency is improved in the case of SiC MOSFET for the switching frequency of 75 kHz and 100 kHz as shown in Figure 5.2.

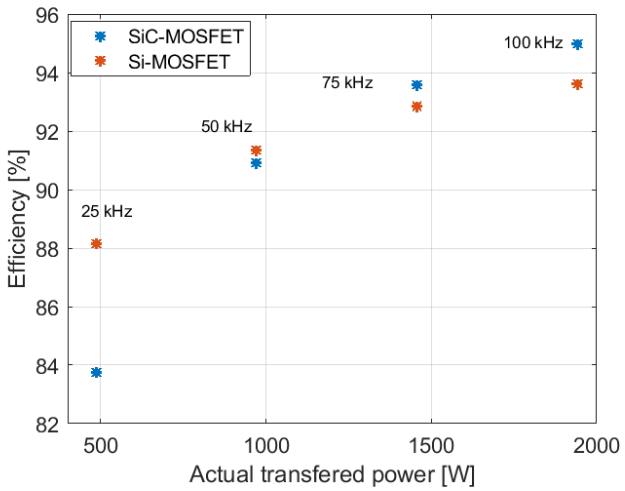



**Figure 5.2:** Efficiency comparsion for Si MOSFET and SiC MOSFET

Figure 5.2 shows the efficiency versus the actual power transferred for different switching frequencies. The efficiency is calculated analytically by considering only

the losses in the switching device using (3.22). From the efficiency comparison, as the switching frequency increases, the SiC MOSFET is more advantageous. For a switching frequency of 100 kHz, the efficiency is increased from 93.5% to 95% due to the reduction of switching loss using a SiC MOSFET.

## 5.2 Losses in the Transformer

In Section 4.3, a planar transformer is designed which is a high frequency transformer used in isolated power supplies and operate at high frequency. Its parameters are shown in Table 4.2 and 4.3 for a selected core set of E type Ferrite core and core material Ferrite 3C96. The primary (high voltage) and the secondary (low-voltage) side windings were made from copper tape with size AWG-15 and AWG-1 respectively.

Based on the geometrical dimensions and construction details of the core (Table 4.2) and the winding (Table 4.3), the losses in the core and winding are calculated for different frequencies and output voltages.

### 5.2.1 Power Loss in the Core

For the analytical estimation of the ferritie core losses in the transformer, the modified Steinmetz equation is used as (3.22) for the rectangular voltage.

$$P_{Fe} = (Core_{density}.core_{volume})$$

$$Core_{density} = C_m f^{\alpha} B^{\beta} (c_o - c_1 T_T + c_2 T_T^2)$$

where $Core_{density}$ is core loss density and the values for $C_m$, $\alpha, \beta$ and the polynomial coefficients $c_o, c_1$ and $c_2$ are given in Table 5.3 from the datasheet. $core_{volume}$ is the core volume which is presented in Table 4.2. $T_T$ is the operating temperature and it is considered as 100 °C.

**Table 5.3:** Parameters values of core material with different switching frequencies

| Parameter | Switching Frequencies | | | |
|---|---|---|---|---|
| | 25 kHz | 50 kHz | 75 kHz | 100 kHz |
| $C_m$ | 5.121 | 5.121 | 5.121 | 0.0827 |
| $c_0$ | 6.563 | 6.563 | 6.563 | 2.805 |
| $c_1$ | 0.1104 | 0.1104 | 0.1104 | 0.0366 |
| $c_2$ | 0.000548 | 0.000548 | 0.000548 | 0.000183 |
| $\alpha$ | 1.34 | 1.34 | 1.34 | 1.72 |
| $\beta$ | 2.665 | 2.665 | 2.665 | 2.827 |
| $B$ | 0.2 | 0.16 | 0.13 | 0.1 |

As can be seen from Table 5.3, the parameter values are the same for the frequencies from 25 kHz to 75 kHz and they are reduced strongly in case of a 100 kHz operating frequency for one type of core material, in this case it is 3C96. Based on the values of operating frequency and parameters values presented in Table 5.3 and 4.2, the core loss in the transformer is calculated and shown in Table 5.4 and Figure 5.3 for different frequencies and output voltages respectively.

### 5.2.2 Power loss in the Winding

In high frequency operation modes, the skin and proximity effects cause a significant increase in AC resistance and power losses in both windings. It is calculated based on (3.23)-(3.28),

$$P_{cu} = P_{pri} + P_{sec}$$

$$P_{pri} = I_{rms}^2 \, R_{AC-pri}$$

$$R_{Ac} = F_{AC} R_{DC}$$

where $R_{AC}$ is the AC resistance of the winding, $F_{AC}$ is the resistance factor and $R_{DC}$ is the DC resistance which is calculated in Section 4.3 as $R_p$ and $R_s$ for the primary and secondary side as presented in Table 4.3.

The rms current is calculated as,

$$I_{rms} = I_o \frac{1}{n} \sqrt{2D} \tag{5.3}$$

where $I_o$ is the output current, $n$ is the transformer turn ratio and $D$ is the duty cycle.

Consider the switching frequency of 100 kHz with an output voltage of 12 V. Based on the parameters of the core material which is given in Table 5.3, the core density is calculated as

$$Core_{density} = C_m f^{\alpha} B^{\beta} (c_o - c_1 T_T + c_2 T_T^2)$$

$$Core_{density} = 0.0827(100 * 10^3)^{1.72} * 0.1^{2.82}(2.8 - 0.0366 * 100 + 0.000183 * 100^2)/1000$$

$$Core_{density} = 51.42 mW/cm^3$$

Then, the losses in the core of the transformer is calculated using the core volume which is given in Table 4.2 as,

$$P_{Fe} = (Core_{density}.core_{volume})$$

$$P_{Fe} = (51.42 mW/cm^3 * 28.2 cm^3)/1000 = 1.45W$$

To calculate the winding loss in the transformer, the rms current and AC resistance for the primary and secondary side should be calculated. The DC resistance is calculated and presented in Table 4.3 as 13.5 $m\Omega$ and 0.038 $m\Omega$ for the primary and secondary side respectively. By considering the resistance factor as 1.2, the AC resistance is calculated as 16.2 $m\Omega$ and 0.0456 $m\Omega$ for the primary and secondary side respectively.

The rms current on the primary side is calculated using (5.3) as,

$$I_{rms} = I_o \frac{1}{n} \sqrt{2D} = 8A \tag{5.4}$$

where $I_o$ is the output current of 160 A, $n$ is the transformer turn ratio of 20 and $D$ is the duty cycle which is 0.5.

Then, the primary winding loss is calculated as

$$P_{pri} = I_{rms}^2 \, R_{AC\_pri}$$

$$P_{pri} = 8A^2 * 16.2 * 10^{-3}\Omega = 1.03W$$

Correspondingly, secondary winding is calculated as

$$P_{sec} = I_o^2 \, R_{AC\_sec}$$

$$P_{sec} = 160A^2 * 0.0456 * 10^{-3} = 1.16W$$

Total winding loss= 1.16 W+ 1.03 W= 2.19 W

As a result, the total transformer loss becomes 3.65 W.

Based on the parameters presented in Table 4.3, the losses in the transformer core and in the windings are calculated for different switching frequencies and presented in Table 5.4.

**Table 5.4:** Transformer loss for different switching frequencies

| Frequency | 25 kHz | 50 kHz | 75 kHz | 100 kHz |
|---|---|---|---|---|
| Core loss [W] | 3.84 | 4.00 | 2.43 | 1.45 |
| Primary winding loss [W] | 3.78 | 1.36 | 1.24 | 1.03 |
| Secondary winding loss [W] | 4.36 | 1.57 | 1.43 | 1.16 |
| Total Transformer loss [W] | 11.99 | 6.94 | 5.11 | 3.65 |

Table 5.4 presents the transformer loss for the selected core and transformer winding with different switching frequencies with an input output voltage of 240 V and 12 V respectively. As can be seen from this table, as the switching frequency increases the core loss and the winding losses in the transformer is reduced since as the switching frequency increases, the core size becomes smaller. Moreover, as the switching frequency increases the core parameter values and the operating flux density decrease as shown in Table 5.3, for a 100 °C operating temperature.

The transformer losses also calculated for the different output voltages 12 V to 48 V with the switching frequency of 100 kHz. Core loss of the transformer is calculated using modified steinmetz equation as discussed in Section 3.4.1. As the output voltage is varied between 12 V and 48 V, the flux density is calculated for each output voltage of the same core size of the transformer as,

$$B = \frac{V_o}{4fnA_{core}} \tag{5.5}$$

where $V_o$ is output voltage, $f$ is operating frequency, $n$ is number of turns on secondary and $A_{core}$ is area of the transformer core.

Consider the output voltage of 30 V, input voltage of of 240 V and switching frequency of 100 kHz. For this frequency, the selected transformer core parameters are

presented in Table 4.2. From this table the core area of the transformer is 245 $mm^2$ and number of turn on the secondary is 1. As a result, the flux density is calculated using (5.5) as 0.15 T.

Using the transformer core volume of 28200 $mm^3$ and other transformer parameters which is given in Table 5.3, the transformer core loss is calculated as

$$Core_{loss} = C_m f^{\alpha} B^{\beta} (c_o - c_1 T_T + c_2 T_T^2) core_{volume}$$

$$Core_{loss} = 0.0827(100*10^6)^{1.72} * 0.15^{2.82}(2.8 - 0.036*100 + 0.00183*100^2)28200*10^{-9}$$

$$Core_{loss} = 4.78W$$

The winding loss of the transformer are calculated based on the rms current and winding resistance of the transformer in the primary and secondary side which is presented in Table 4.3. For the frequency of 100 kHz, Table 4.3 shows that the DC resistance on the primary and secondary side are 13.5 $m\Omega$ and 0.038 $m\Omega$ respectively. The resistance factor is considered as 1.2 which describes the effect of conductor resistance due to skin effect, then the AC resistance on the primary and secondary side becomes 16.2 $m\Omega$ and 0.0456 $m\Omega$ respectively.

Using an output voltage of 30 V, input voltage of 240 V and rated power of 2 kW, the rms current on the primary and secondary side are calculated as 23 A and 66.6 A respectively. As a result, the primary winding loss of the transformer is calculated using (3.26) as

$$P_{pri} = I_{pri,rms}^2 \, R_{AC\_pri}$$

$$P_{pri} = 23A^2 * 16.2m\Omega = 8.56W$$

The secondary transformer winding loss is

$$P_{sec} = I_{sec,rms}^2 \, R_{AC\_sec} \tag{5.6}$$

$$P_{sec} = 66.6A^2 * 0.0456m\Omega = 0.2W$$

Consequently, the total transformer loss becomes 13.54 W.

Figure 5.3 shows the transformer loss distribution with an output voltage of 12 V to 48 V, and keeping the input voltage, and switching frequency as 240 V and 100 kHz respectively.

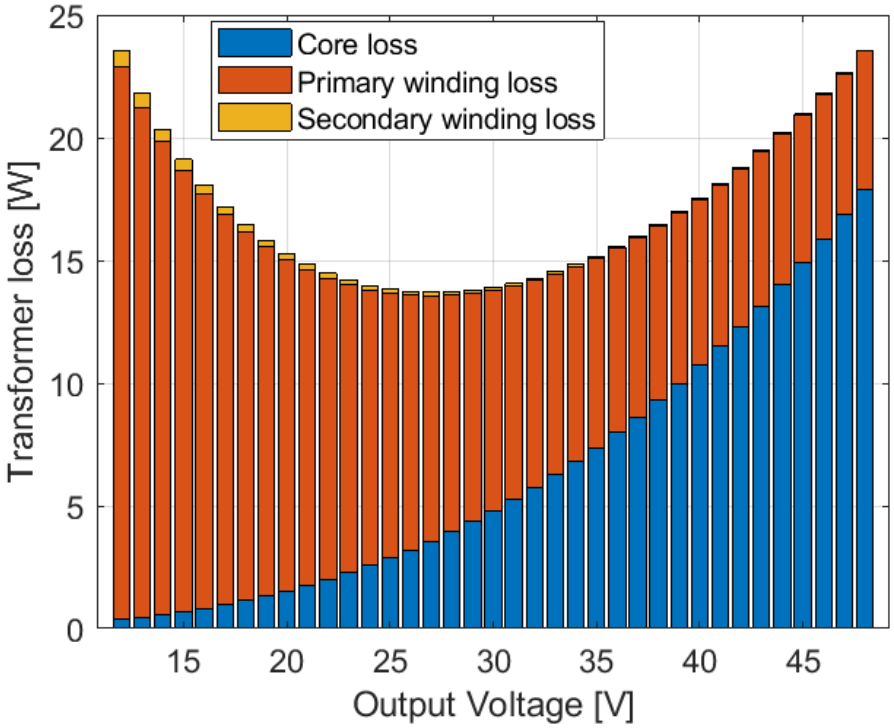



**Figure 5.3:** Transformer loss for different output voltage, 100 kHz and 2 kW

As can be seen from Figure 5.3, the core loss in the transformer is increased with an output voltage. However, the winding loss is decreased as the output voltage increased. Since the voltage to frequency ratio is directly proportional to the flux density, as the output voltage increase, the flux density also increased hence, the core loss in the transformer is increased.

However, in the case of winding loss as the output voltage increases, the output current for the rated power of 2 kW is reduced which leads to a decrease in the winding loss as the output voltage increase. The primary winding is more responsible for the losses in the transformer winding due to higher resistance on the primary side for the fixed frequency of 100 kHz as shown in Table 4.3. And it will be reduced strongly as the output voltage increases.

In case of a higher output voltage, the core loss is more responsible for the losses in the transformer since increasing an output voltage leads to an increase in the load which increases the core loss. From this figure, we can see also the operating point of the transformer where the transformer operate at a minimum total transformer loss. This operating point is at an output voltage of around 30 V for the fixed input voltage of 240 V and a rated power of 2 kW.

## 5.3 Power Step Response of the Controller

The dual active bridge converter is modeled in MATLAB/Simulink based on the designed parameters in Section 4.1. The designed duty cycle for the primary and

secondary transformer voltage is 0.3248 and 0.3419 respectively which is calculated based on the time $T_1$ and $T_3$ as in (3.9) and (3.10).

To achieve power flow control, the pulses have to be produced such that a phase shift is formed. Figure 5.4 show that the primary and secondary side of the transformer voltage with the inductor current for the rated power of 2 kW, input voltage of 240 V, output voltage of 12 V and with switching frequency of 100 kHz. Figure 5.5 (a) shows the output voltage of the converter for buck operation with a ripple voltage of 2 % of the output voltage. The ripple voltage is shown in Figure 5.6.

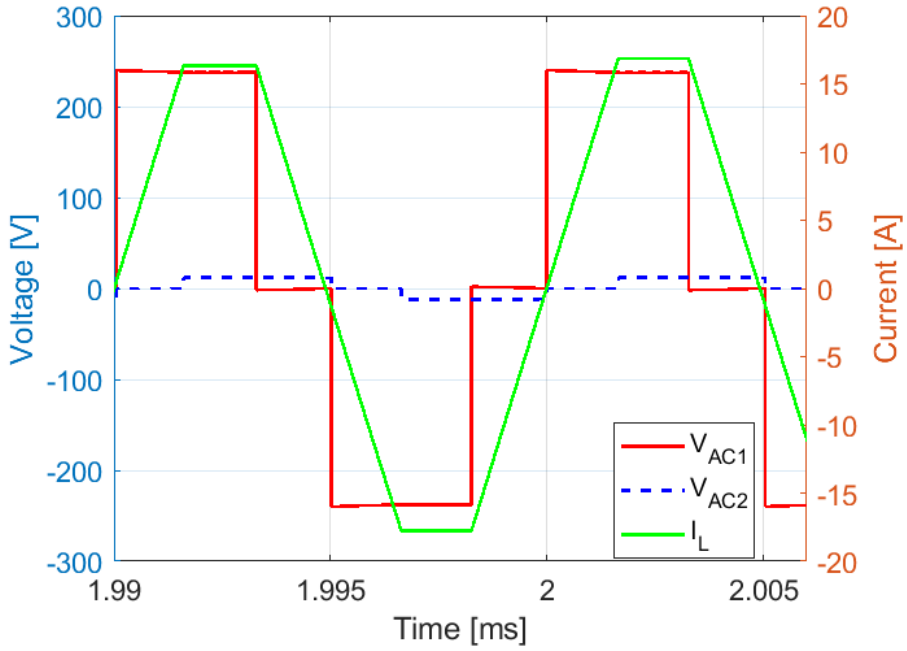
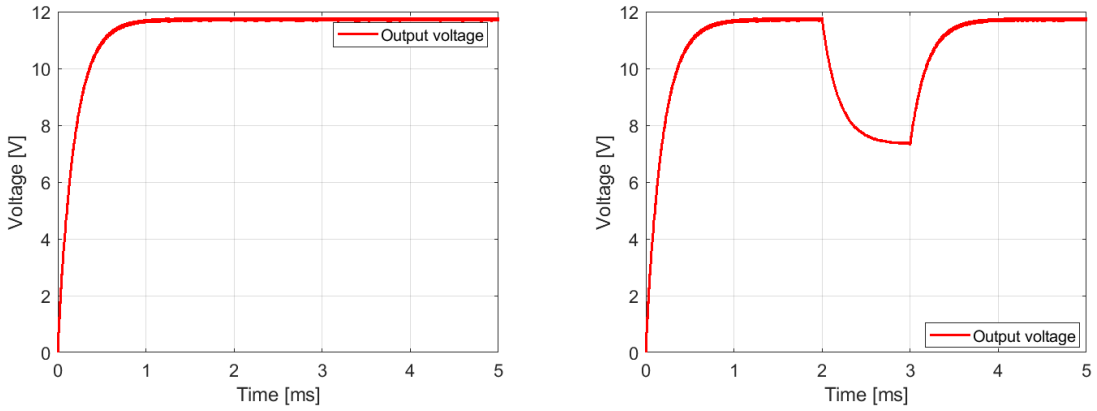



**Figure 5.4:** Input and output transformer voltage with inductor current




**(a)** For the rated power of 2 kW **(b)** When the power changes to 1.2 kW

**Figure 5.5:** Output voltage

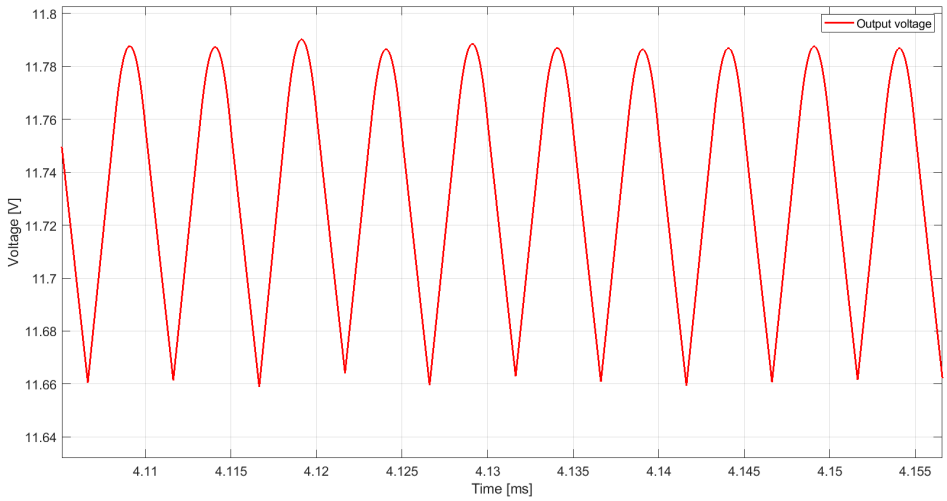
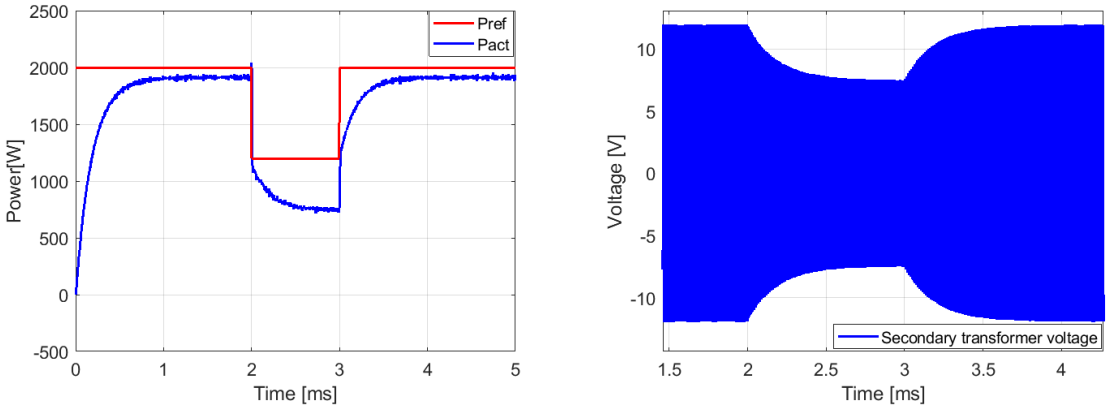



**Figure 5.6:** Output voltage ripple, $V_o = 12V$

When there is a sudden change of power, then the controller control the current flowing to the secondary transformer by changing the phase shift angle which leads to a change in $T_1$, $T_2$ and $T_3$. Figure 5.7 shows the step response of the power and output voltage. In order to perform the closed-loop operation of the DAB converter under DPS control, the reference power is kept at 2 kW.




**(a)** Power response **(b)** Voltage response

**Figure 5.7:** Step response of the controller

As shown in Figure 5.7 (a), the power reference is changed from the rated power of 2 kW to 1.2 kW at 2 ms and the actual power transferred reduced at 2 ms. This is achieved by reducing the phase shift angle since as the power is reduced the phase shift angle between the two voltages also changes (3.5). With the phase shift angle reduction, the time interval $T_1$, $T_2$ and $T_3$ was also reduced as (3.6)-(3.8) which can be observed in Figure 5.8.

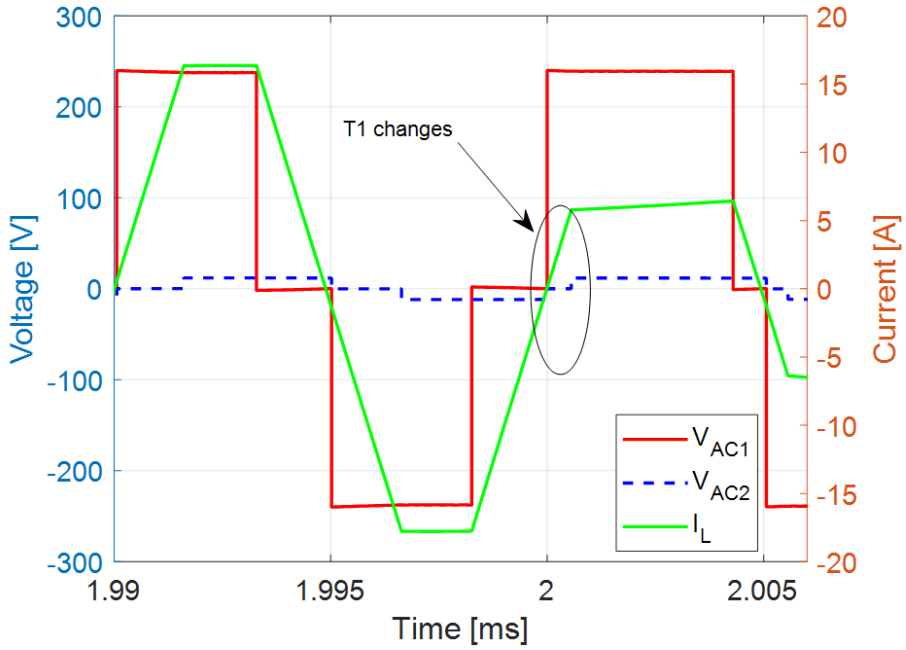


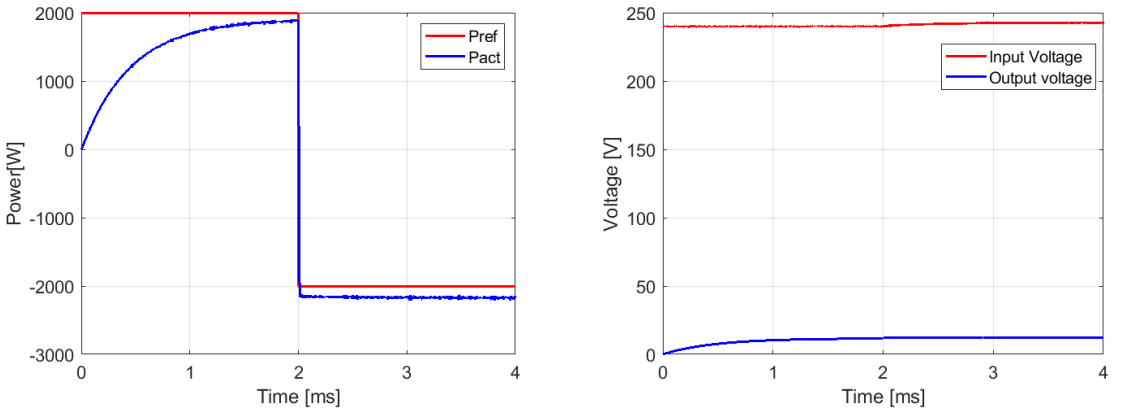

**Figure 5.8:** Transformer voltage and current waveforms when the power changes at 2 ms

At 2 ms the controller compares the actual and reference power and decides whether the process is a power increment or power decrement. In this case since the reference is lower, the process will be a power decrement through optimizing the values of $d_1$ and $d_2$. As a result, the peak amplitude of the inductor current decreased from 17.54 A to 6.975 A as shown in Figure 5.8. At 2 ms the output voltage also reduced from the nominal output voltage of 12 V to 7.39 V as shown in Figure 5.7 (b) and returned back to 12 V at 3 ms .

In order to enhance the closed-loop control strategy, the actual power has to follow the reference power. In the case an error occurs, further corrective action is initiated by the controller. Finally, the actual power tracks the reference power, which is shown in Figure 5.7 (a). The figure shows the tracking of the actual power to the reference when the step change of reference power occurs at 3 ms.

## 5.4 Power Reversal Response of the Controller

Since the dual active bridge DC/DC converter is bidirectional, the power flow can be positive or negative depending on the mode of operation. To achieve this the controller is tested by changing the direction of the power flow. Figure 5.9 (a) shows the actual power transferred and voltage response when the power change its direction at 2ms.




**(a)** Power response **(b)** Input and output Voltage response

**Figure 5.9:** Power reversal response when power changes its direction at 2ms

In Figure 5.10, it is shown that in order to change the power flow direction as shown in Figure 5.9 (a), pulses are produced to change the current direction. From this figure the current has changed its direction at 2ms. However, the phase shift angle and the time interval $T_1, T_2$ and $T_3$ are not changed.

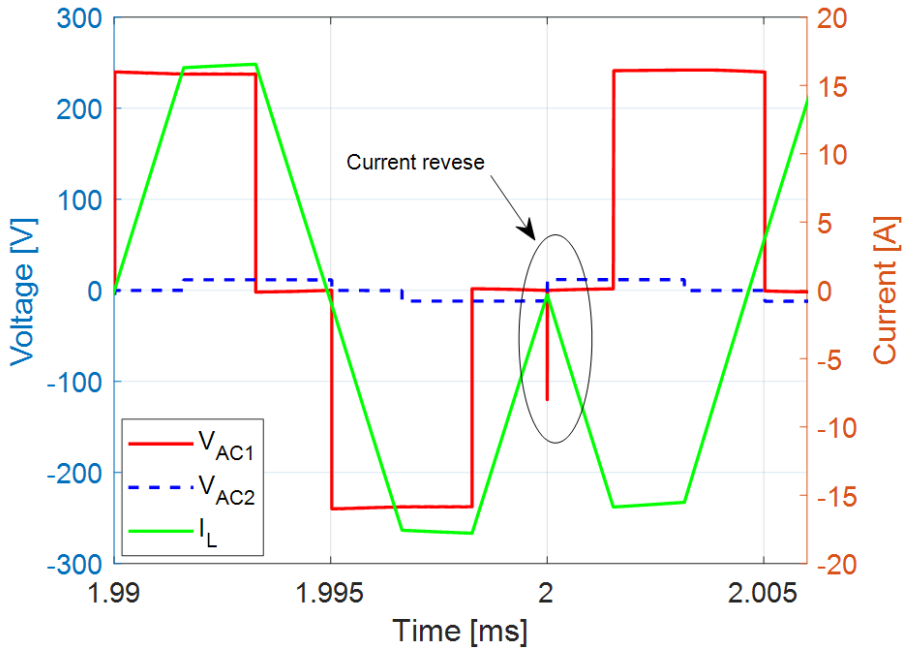



**Figure 5.10:** Transformer voltage and current waveform when the power direction reversed at 2ms.

From Figure 5.9 (b), it is clear that the controller kept the same input and output voltage when the power flow changed its direction. The control directs power between the two DC buses such that the leading bridge delivers power to the lagging bridge. The applied square waves to the bridges create a voltage differential across the energy transfer inductance and direct its stored energy.

## 5.5 Selection of Heat Sink

In the heat sink design, semiconductor junction temperatures, $T_j(T)$ should not exceed their designed temperature limits under worst case operating conditions. The heat sink temperature is selected as the reference point for the worst case operating point of the converter since it maintains a relatively constant temperature compared to the MOSFET and diode junctions.

The heat sink selection process involves calculating the MOSFET module losses under full load conditions for the chosen surface temperature of the heat sink with the desirable cooling method. Then, calculate the required heat sink-ambient thermal resistance, $Rth_{s\_a}$ to allow the heat sink to maintain the surface temperature at the full load.

For the analysis, one Si MOSFET (SPW47N60CFD) is considered and calculate its conduction loss with different on-resistance, since the dissipated power varies with on resistance and temperature as shown in Table 5.5.

**Table 5.5:** Power dissipation for different operating temperature

| Operating temperature [°C] | -20 | 25 | 60 | 100 | 120 | 150 |
|---|---|---|---|---|---|---|
| $R_{dson}$ [Ω] | 0.0625 | 0.08 | 0.1 | 0.125 | 0.14 | 0.175 |
| $P_{diss}$ [W] | 4.86 | 6.22 | 7.22 | 9.72 | 10.88 | 13.61 |

From the data sheet for the MOSFET the thermal resistance can be determined and shown in Table 5.6.

**Table 5.6:** Thermal resistance of SPW47N60CFD MOSFET

| $Rth_{j\_c}$ [k/W] | $Rth_{j\_a}$ [k/W] | $T_j$ [°C] |
|---|---|---|
| 0.3 | 62 | -55 to 150 |

Consider the thermal conductor interface material is silcon pad, hence $Rth_{cs}$=1.1 k/W and assume the worst case ambient temperature of 40 °C. The chip temperature can be calculated in steady state without the heat sink based on (3.29) and presented in Figure 5.11.

$$T_{jnh} = Rth_{j\_a}P_{diss} + T_a$$

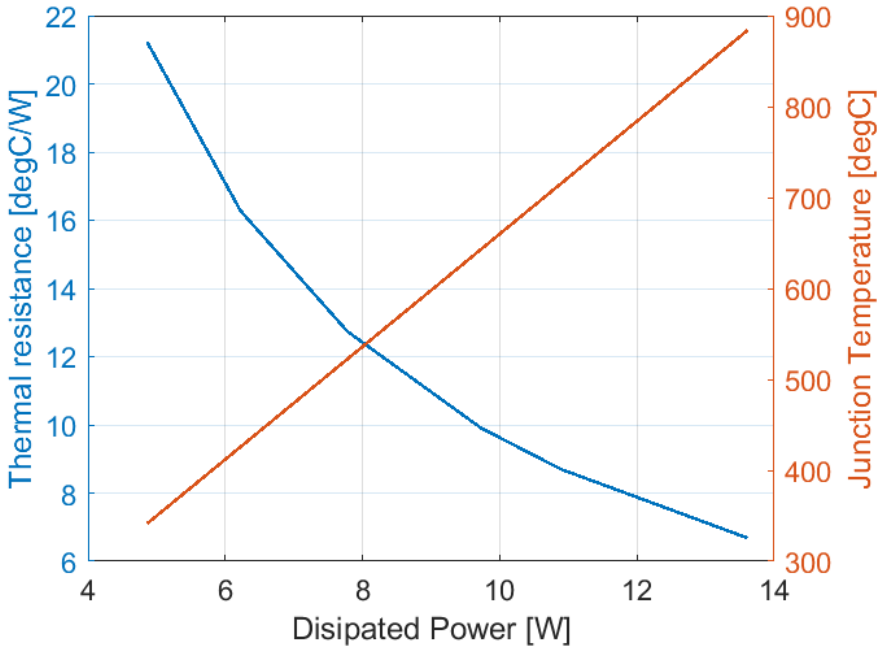



**Figure 5.11:** Thermal resistance and junction temperature for different dissipation of power

From Figure 5.11, it can be seen that the MOSFET chip temperature operates above 300 °C for different dissipated power. However, the maximum chip temperature for a regular MOSFET is approximately 175 °C. To be on the safe side, the temperature on the semiconductor is often designed so that the temperature is kept under this maximum temperature with the help of additional cooling. This has mainly to do that the life length of the chip is temperature dependent and a high temperature reduces the life length strongly.

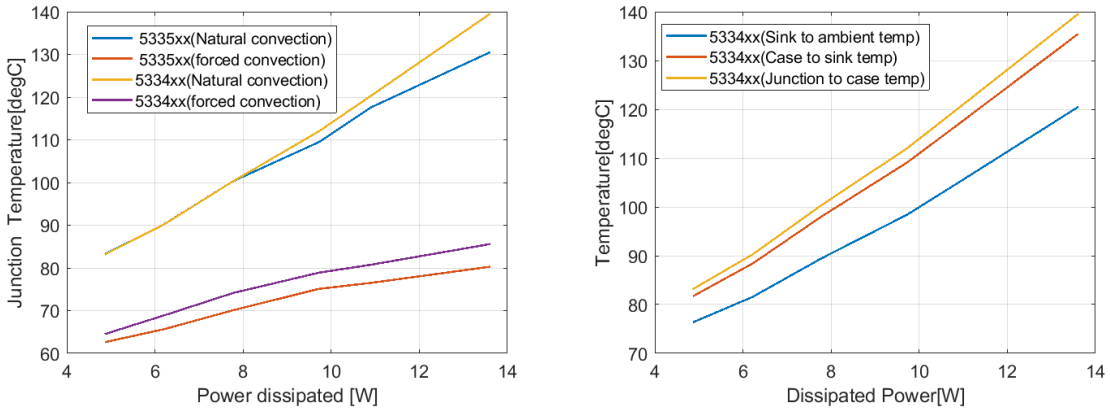
To lower this temperature, two different heat sinks are tried out which are 5334XX and 5335XX with large radial fins. The difference between this two heat sink is their height and they have height of 38.1 mm and 50.88 mm for 5334XX and 5335XX respectively. They have a thermal resistance lower than the maximum thermal resistance of the selected Si MOSFET. The thermal resistance for the selected heat sinks is calculated based on the data sheet values for both natural convection and forced convection for various power dissipation levels as shown in Table 5.7.

**Table 5.7:** Thermal resistance of heat sink for different power dissipation

| | | Power dissipated | | | | | |
|---|---|---|---|---|---|---|---|
| | | 4.86 | 6.22 | 7.22 | 9.72 | 10.88 | 13.61 |
| $Rth_{sa}[°C/W]$ | 5334XX(Natural) | 5.76 | 5.14 | 4.89 | 4.42 | 4.4 | 4.04 |
| | 5334XX(Forced) | 2.5 | 2.1 | 1.9 | 1.7 | 1.5 | 1.2 |
| | 5335XX(Natural) | 5.75 | 5.14 | 4.89 | 4.62 | 4.59 | 4.55 |
| | 5335XX(Forced) | 2.8 | 2.5 | 2.3 | 2.0 | 1.8 | 1.5 |

Based on the data from the data sheet and calculated values of thermal resistances

(Table 5.7) of the heat sink which is required to keep the heat sink temperature below 140 °C, the junction temperature is calculated and presented in Figure 5.12 (a).




**(a)** Junction temperature of two heat sinks with dissipated power

**(b)** Temperature with dissipated power for 5334XX

**Figure 5.12:** Temperature with dissipated power

In order to account for uncertainty, 30% of safety factor is applied, hence the calculated resistance values are multiplied with 1.3. Based on this thermal resistance the junction temperature is calculated as shown in Figure 5.12. From this Figure, it is noted that how the temperature is reduced when we have the heat sinks. Moreover, the junction temperature for the heat sink which have higher height can achieve lower junction temperature for the natural and forced convection. In addition, as can be seen from Figure 5.12 (a), in case of natural convection for both types of heat sinks, the junction temperature is high. This is because the thermal resistance of sink to ambient of natural convection is higher than that of forced convection.

For the forced convection, a fan is selected for the heat sink which is CEBF0140401605-00 and its volume is 5.5 $cm^3$. Figure 5.13 shows its thermal resistance with air velocity and area of the fan.

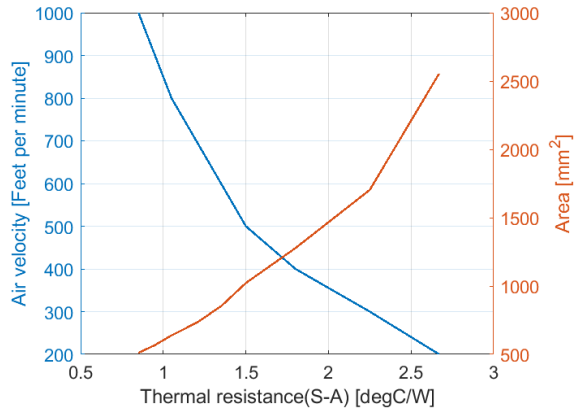



**Figure 5.13:** Thermal resistance and junction temperature for different dissipation of power

Considering the two bridge of the converter with Si MOSFET on resistance of 0.07Ω at $T_j$=25 °C. From Section 5.1, with maximum junction temperature of 150 °C, the total power dissipation is approximately 110 W at 100 kHz. Then, the required thermal resistance is calculated using (3.31).

As a result, $Rth_{sa}$=1.13 °C/W is the maximum required heat sink to ambient thermal resistance. Hence, it can allow the heat sink to maintain the surface temperature at full load. Based on this thermal resistance value, a heat sink 431 is selected for this power dissipation with dimensions as shown in Figure 5.14.

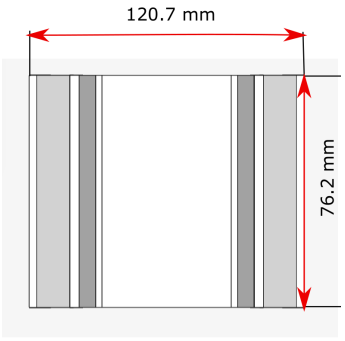



**Figure 5.14:** Geometric dimension of heat sink 431-series

For the natural and forced convection, the datasheet can be used to calculate the thermal resistance (sink-to-ambient) for the 431 series heat sink [34]. In the case of natural convection, the thermal resistance is calculated by dividing the surface temperature rises by the heat dissipated. This provides the required thermal resistance at that specific operating condition.

In this case, the heat dissipated is 110 W which results in a surface temperature rise above 90°C [34]. Dividing 90°C by 110W produces a sink-to-ambient thermal

resistance of 0.83°C/W. In the case of forced air, the thermal resistance sink to ambient is reduced to 0.45°C/W with air velocity of 210 LFM (Linear Feet per Minute). Based on this thermal resistance, the temperature of the junction, case and heat sink are calculated using (4.13)-(4.15) for both cases and presented in Table 5.8.

**Table 5.8:** Junction, case and sink temperature for natural and forced air

| Type | Junction temp [°C] | Case temp [°C] | Sink temp [°C] |
|---|---|---|---|
| Natural convection | 241 | 186.3 | 131.3 |
| Forced convection | 199.5 | 144.5 | 89.5 |

The natural convention is also simulated by FEM for the selected geometry of the heat sink and with the aluminium material as shown in Figure 5.15.

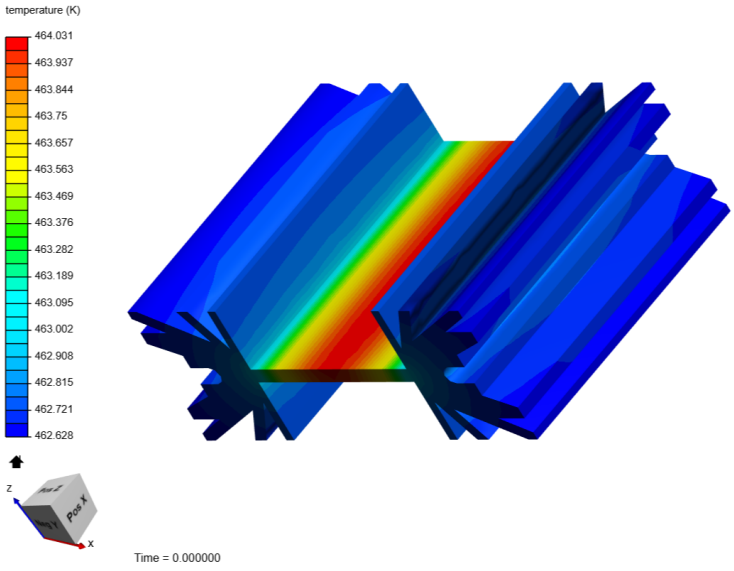



**Figure 5.15:** Temperature distribution of heat sink under natural convection.

Figure 5.15 show the temperature distribution of heat sink under natural convection.

# 6
# Conclusion

The main purpose of this study is to design a promising DC/DC converter topology to be used in an automotive application. After the qualitative study of different DC/DC converter topologies, the DAB is selected since it has a high efficiency and the best features of the investigated topologies.

The DAB converter is designed for the input voltage and nominal output voltage of 240 V and 12 V with a rated power of 2 kW and a switching frequency of 100 kHz. The design includes the transformer design to select the core material, and winding parameters. The closed-loop control of the DAB converter using DPS modulation has been used to control the wide range of power transfer. The various operating waveforms for different switching condition is discussed.

The power loss of the semiconductor is analyzed analytically for the conduction and switching loss for different switching frequencies using a Si MOSFET and SiC MOSFET. From the result, the SiC MOSFET reduced the switching loss strongly and increases the conduction loss. In the case of using a Si MOSFET, 53 % of the total loss is switching loss but in the case of using a SiC MOSFET, it reduced to 12 % for the switching frequency of 100 kHz. Hence, the Si MOSFET is better in terms of conduction power loss while switching power loss of SiC MOSFEET are significantly lower. Moreover, as the switching frequency increases, the SiC MOSFET is more advantageous and the core loss and the winding losses in the transformer is reduced.

## 6.1 Future Work

- The design and optimization of a closed-loop feedback control are needed to achieve a high performance regulation of the DAB bi-directional DC/DC converter.
- Analytical and simulation results are presented in this study. To verify these results further, hardware should be developed to determine the actual efficiency and power density.
- To further reduce the losses in the transformer, a transformer design optimization is needed.
- To increase the efficiency and reduce the loss in the converter, an EMI filter is needed.
- Thermal modeling should be verified further using FEM simulations and hardware modeling to accurately predict the heat sink effect on the junction temperature.

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