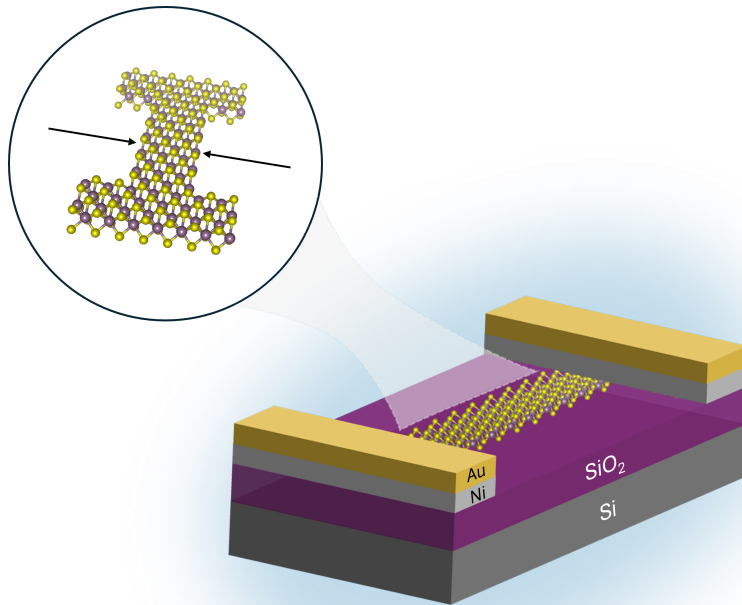




CHALMERS
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High-performance Transistors with Two-dimensional Semiconductor Nanoribbons

Width scaling of Mono- and Bilayer MoS₂ for Efficient and High-density Transistor Technologies

Master's thesis in Nanotechnology

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DEPARTMENT OF MICROTECHNOLOGY AND NANOSCIENCE

CHALMERS UNIVERSITY OF TECHNOLOGY
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Cover: Schematic of a monolayer MoS₂ nanoribbon field-effect transistor. The inset shows the representative width scaling of a two-dimensional semiconductor nanoribbon.

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Abstract

The progressive miniaturization of transistors has been the engine of the modern information revolution. While both gate lengths and channel thicknesses have been scaled into the sub-20 nm regime in state-of-the-art silicon gate-all-around nanosheet architectures, the channel width, the last unscaled dimension in transistors, has remained constrained above ~40-50 nm. This “width-scaling wall” arises from dangling-bond trap states, lateral charge depletion, and edge-roughness scattering that collectively suppress drive current as channel widths are reduced, fundamentally limiting the transistor integration density. Breaking this wall is one of the most consequential open challenges in semiconductor device physics.

This master’s thesis presents the experimental demonstration that two-dimensional semiconductor nanoribbon transistors overcome the width-scaling wall and operate in an edge-enhanced transport regime. A high-fidelity top-down lithographic nanofabrication strategy enabled the fabrication of monolayer and bilayer molybdenum disulfide (MoS₂) nanoribbon transistors with channel widths as narrow as 15 nm. In contrast to the conventional semiconductor scaling rule that associates degraded current density with reduced channel width, atomically thin monolayer and bilayer MoS₂ nanoribbon transistors in this work demonstrate enhancements in on-current density of up to 230% and 170%, respectively, followed by saturation for channel widths approaching 15 nm. These ultranarrow transistors achieve on/off ratios of 10⁶ with channel lengths as short as 50 nm. In addition, enhanced mobility and threshold-voltage stability suggest reduced edge scattering and depletion resulting from improved electrostatic control. The demonstrated monolayer and bilayer MoS₂ nanoribbon transistors achieve on-current densities up to ~300-400 $\mu\text{A}\mu\text{m}^{-1}$ in the 15-30 nm channel width regime. These findings provide an experimental foundation for channel width scaling to realize the ultimate scaling of high-performance transistor technologies.

Keywords: 2D semiconductors, Nanoribbons, Width scaling, High-performance transistors, MoS₂

List of Publications

The following article is based on the work in this thesis.

- (A) S. K. Mallik, A. Christiansen and S. P. Dash. "Breaking the width-scaling limit in high-performance atomically thin 2D nanoribbon transistors". *Manuscript under review* (2026).

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Tack!

Adrian Christiansen, Gothenburg, June 2026

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1

Introduction

Last year marked the 100th anniversary of Julius Edgar Lilienfeld’s patent for the first concept of a device capable of controlling electric currents, the field-effect transistor (FET) [1]. It would then take 22 years until the first working transistor was developed at Bell Labs in 1947. Since then, transistor technologies have shaped our modern society in ways that once seemed unimaginable, with the planar metal–oxide–semiconductor field-effect transistor (MOSFET) playing a particularly significant role [2, 3]. The subsequent geometric scaling of silicon (Si)-based MOSFETs and the development of complementary metal-oxide-semiconductor (CMOS) technology further enabled performance advancements of the efficient and high-density integrated circuits (ICs) of contemporary information and communication technologies (ICTs).

Around the time of the new millennium, the scaling of Si-based transistor technologies had hit a couple of rough patches, especially considering the challenges of mitigating short-channel effects (SCEs) [3]. The need for new materials and architectures was evident and a new era of equivalent scaling was beginning. The focus on new materials, especially the integration of insulators with high dielectric constants (κ), and more complex architectures drove successful innovations from the MOSFET to the fin field-effect transistor (FinFET) and eventually the gate-all-around (GAA) architecture [2, 4]. This facilitated the continued drive of the prediction of Gordon Moore, also known as Moore’s law, stating that the number of components per IC would double every two years [3–5].

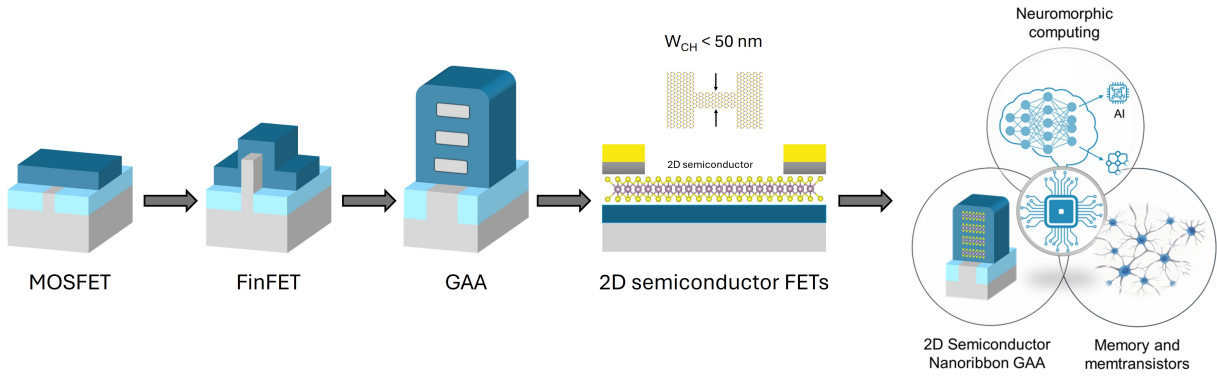


Figure 1.1: The evolution of scaled transistor technologies from the conventional MOSFET structure, to FinFET, GAA, and the modern atomically thin 2D semiconductor transistors. Showcasing the future possibilities of 2D semiconductors, in even more scaled and high-performing transistor technologies, memory and memtransistors, and neuromorphic applications.

Despite evident efforts in equivalent scaling, Si-based technologies are reaching their physical limits with further scaling posing challenges for high-performance transistors in the sub-nm regime [6–8]. The strong scattering effects at the channel-dielectric interface due to surface roughness and dangling bonds cause severe degradation of carrier mobilities and performance, breakdown of the electrostatics, and emerging SCEs. Additionally, scaling the gate oxide give rise to quantum tunnelling of charge carriers increasing leakage currents and degrading efficiency [9]. Furthermore, due to lower hole mobilities, p-type MOSFETs require channels that are two or three times wider than their n-type counterpart to compensate for drive current [10].

Two-dimensional (2D) semiconductors have been proposed as alternatives to Si-based transistors, with properties to facilitate the development of ultra-scaled high-performance devices [4, 11]. The 2D semiconductors of the transition metal dichalcogenide (TMD) family, a class of van der Waals (vdW) crystals, have an atomically thin body with no out-of-plane dangling bonds, optical transparency, and mechanical flexibility [12]. They show great electrostatic integrity when scaled and high performance in on-current, on/off ratio, mobility, and subthreshold swing/slope (SS). TMDs have the general formula MX_2 , where M is a transition metal (e.g. Mo, W, Ta, Nb, Re) and X is a chalcogen (e.g. S, Se, Te) [13, 14]. Representative 2D semiconductors of the TMDs are molybdenum disulfide (MoS_2), tungsten disulfide (WS_2), molybdenum diselenide (MoSe_2), and tungsten diselenide (WSe_2). Remarkable for these materials is the transition from an indirect band gap to a direct band gap as the number of layers are decreased

to one [13–15]. The 2D semiconductors MoS₂ and WSe₂ exhibit native n-type and p-type behaviour, respectively, and are widely investigated as candidates for high-performance transistor applications [14]. The atomically thin body, electrostatic integrity and direct band gap are not the only extraordinary properties of monolayer TMDs. They also exhibit physical phenomena such as strong spin-orbit coupling, spin-orbit splitting, coupling of spin and valley physics, well-pronounced valley degree of freedom, charge density waves, and gigantic exciton binding energy that governs their optical spectra [14, 16, 17].

Scaling the width of TMDs to the one-dimensional (1D) regime yields nanoribbons, which in the last couple of years have emerged as promising candidates for scaled and versatile devices [18, 19]. Their enhanced intrinsic catalytic reactivity, increased edge currents, and stable electrical transport properties show great potential for future ultra-scaled technologies. Although transistors exploiting the exotic features of monolayer and nanoribbon TMDs have been demonstrated, the relationship between further scaling of the channel width and performance is still unexplored for atomically thin TMDs. Hence, questions arise if, in contrast to the conventional scaling rule for semiconductors of suppressed drive current with reduced channel width, there might exist other types of scaling laws for 2D semiconductors, enabling high-performance device characteristics and novel technical applications.

The purpose of this master’s thesis is to develop ultra-scaled 2D semiconductor nanoribbons to achieve ultimate scaling for high-performance transistor technologies. Focusing on n-type MoS₂, this study aims to fabricate monolayer and bilayer MoS₂ nanoribbons integrated into a FET architecture. The fabrication will employ selected nanofabrication processes to achieve precise nanoribbon dimensions while maintaining material quality. Success in this effort will advance ultra-scaled computational networks and enable novel applications characterized by low power consumption, high efficiency, and extreme device density. This work contributes to addressing the remaining challenges in versatile, controllable, scalable, and applicable fabrication techniques for 2D semiconductor devices in the sub-50 nm channel width regime.

This thesis is organized into seven chapters. Chapter 1 outlines the background, current challenges, motivations, and purpose of this work. Chapter 2 presents the progressive scaling of state-of-the-art Si and 2D semiconductor nanoribbon transistors. Chapter 3 investigates structural and electronic properties of 2D semiconductor nanoribbons. Furthermore, it presents state-of-the-art synthesis of TMD nanoribbons. Chapter 4 describes the experimental methods used in this work and Chapter 5 presents the results of this study, including the high resolution fabrication of atomically thin MoS₂ nanoribbons and high-performance MoS₂ nanoribbon transistors. Chapter 6 discusses the results and provides a future outlook while Chapter 7 summarizes the key findings. The thesis also includes two appendices, with Appendix A containing detailed experimental methods and recipes and Appendix B presenting supplementary results.

2

Progressive Scaling of Transistors

In 1965 Gordon Moore predicted that the number of components per IC would double every year, later adjusted to every two years [4]. Since then, semiconductor technologies have been scaled in the physical device dimensions of MOSFETs and CMOS technology. FinFET structures hit the 10 nm technology node in 2017 and by 2024, advancements had brought the transistors down to the 3 nm enhanced node [20]. The evolution of the technology nodes are shown in Figure 2.1a. The most recent equivalent scaling of transistor technologies by the first commercial manufacturing of the GAA architecture by Samsung in 2022 [21], has enabled industries to develop scaled architectures nearing the few-nm regime. Industries such as Intel, Samsung, and TSMC report 2 nm-node technologies with their GAA RibbonFETs [22], second-generation MBCFET(GAA) technology [23], and N2 first-generation nanosheet transistors [24]. Additionally, IBM very recently introduced the first chip technology reaching the 0.7 nm technology node [25]. Although these accomplishments are impressive, it is important to note that the modern technology nodes do not represent the actual physical device dimensions [26].

In Si-based technologies, various physical dimensions have been scaled down to the few-nm regime, such as the channel thickness reaching 6 nm for state-of-the-art GAA nanosheet transistors, whereas the physical gate lengths have stagnated above 10 nm [5, 20], see Figure 2.1b. The width of the fin has been scaled to 5 nm, while still exhibiting a height of ~50 nm as of the latest FinFET technology node, see Figure 2.1c. Hence, the deviations from the technology nodes for the actual physical dimensions is quite evident, especially regarding the effective device width of 101 nm for state-of-the-art FinFET architectures, see Figure 2.1d.

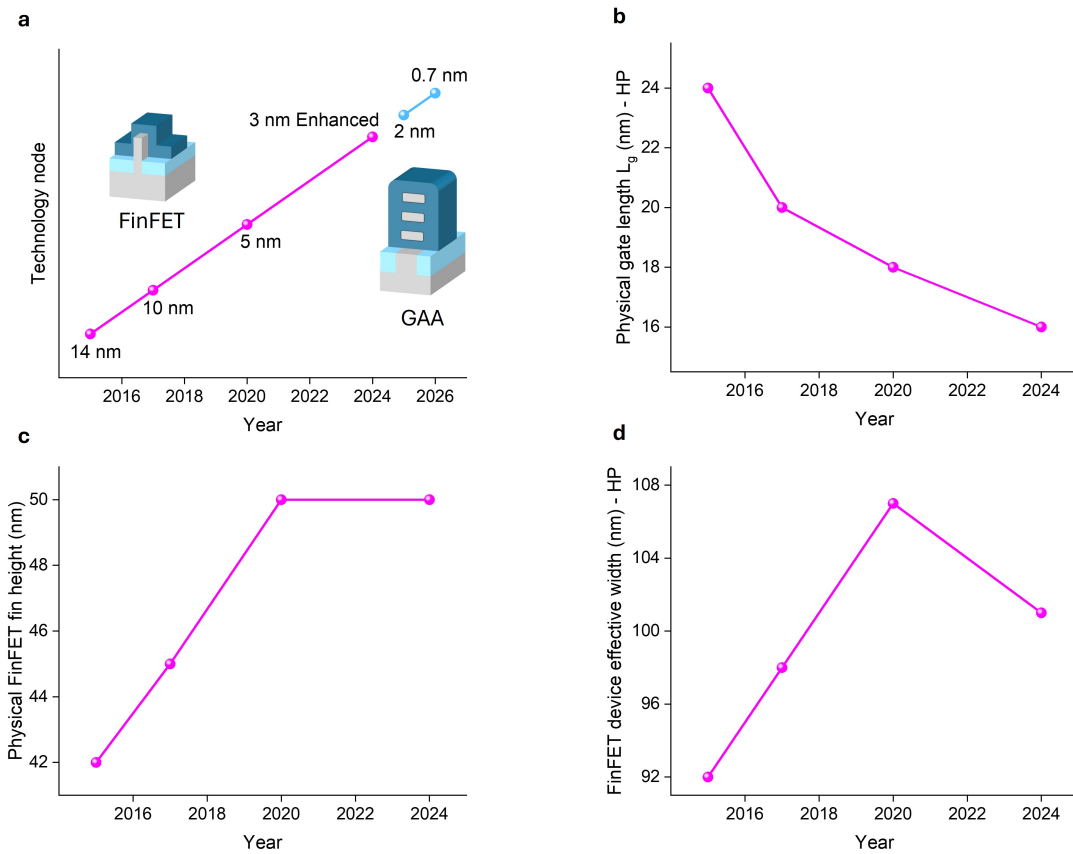


Figure 2.1: Historical scaling of state-of-the-art industry-manufactured Si transistor technologies for FinFET (magenta) and GAA nanosheet (blue) for high-performance (HP) devices. **(a)** Evolution of the technology nodes, 2015–2026. **(b)** Scaling of the physical gate length, 2015–2024. **(c)** FinFET fin height, 2015–2024. **(d)** Effective device widths for FinFETs, 2015–2024. The data are from [20, 25].

Scaling of the channel as well as the effective device widths are predicted to continue [20]. However, scaling the channel width further poses challenges due to dangling-bond trap states, lateral charge depletion, and edge-roughness scattering [3, 8]. Additionally, further scaling of the channel and gate thicknesses pose problems with mobility degradation and leakage currents [6, 7, 9, 27]. With the thinning of channel thickness below 4 nm in bulk Si on insulator (SOI), scattering of the charge carriers with surface roughness and dangling bonds, especially at the semiconductor-dielectric interface, cause extreme degradation of the mobilities for both electrons and holes, see Figure 2.2c. The ongoing scaling challenges of silicon transistors have highlighted the need for new materials for future transistor technologies [27, 28]. In this context, 2D semiconductors have attracted considerable interest as promising channel materials due to their high mobility, reduced surface scattering, and improved electrostatics [2, 4, 6, 29].

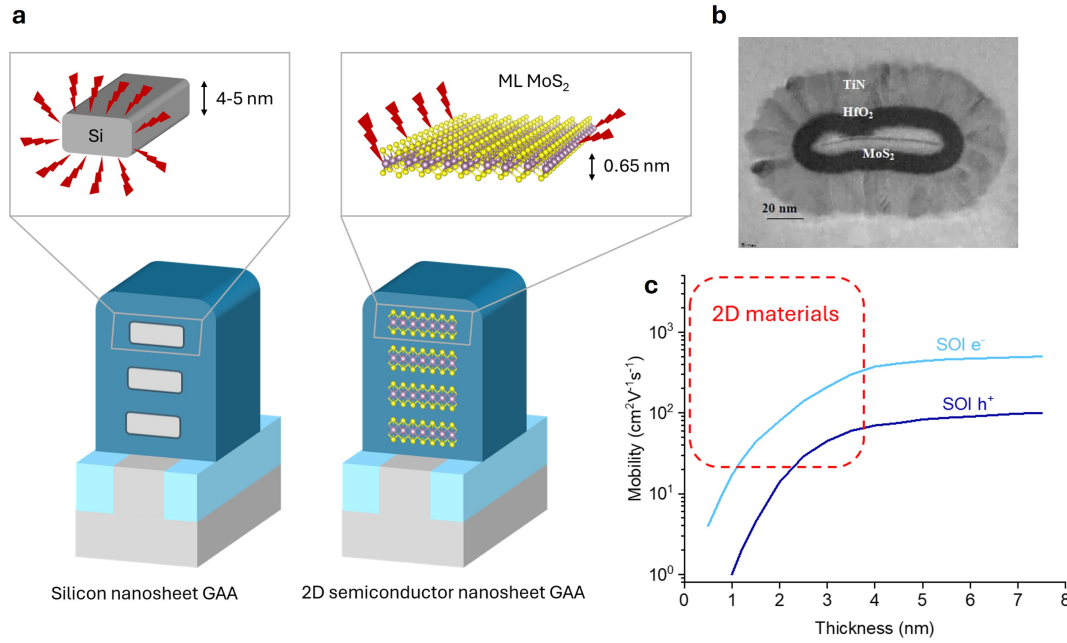


Figure 2.2: Introducing 2D semiconductors. **(a)** Comparison between Si nanosheet GAA with minimum thickness of 4-5 nm (left) and 2D semiconductor nanosheet GAA with atomically thin thickness of 0.65 nm, for MoS₂ (right). The red lightnings represent edge scattering of charge carriers due to dangling bonds and surface states, which is enhanced in Si due to terminated covalent bonds in all crystal directions. **(b)** First demonstrated GAA nanosheet FET with monolayer MoS₂ channels reported by Imec at the 2024 IEDM. Figure reproduced from [30]. **(c)** Mobility degradation of electrons (e⁻) and holes (h⁺) in Si on insulator (SOI) when scaling the channel thickness below 4 nm.

The interest in devices based on 2D semiconductors sparked when the first study of a monolayer TMD FET was published in 2011 by Radisavljevic et al. [31]. Although the advantages of 2D semiconductors are quite clear, there are still challenges of integrating them into more complex three-dimensional (3D) structures [28, 29]. Despite nanofabrication difficulties, Imec reported in 2024, at the international electron devices meeting (IEDM), the first functional stacked monolayer MoS₂ nanosheet transistor with a high- κ GAA architecture [30], see Figure 2.2b. The transition to 2D semiconductor materials can therefore facilitate further development of ultra-scaled 2D semiconductor nanosheet and nanoribbon GAA architectures as well as GAA complementary FET (CFET), incorporated with high- κ dielectrics such as hafnium dioxide (HfO₂) [11]. Figure 2.2a shows schematics of Si nanosheet GAA architecture in comparison with a 2D semiconductor nanosheet GAA architecture, highlighting the advantages of 2D semiconductors exhibiting thinner bodies with high mobilities and less surface scattering.

2. Progressive Scaling of Transistors

The first mechanical exfoliation and electrical characterization of graphene in 2004 [32], for which Andre Geim and Konstantin Novoselov received the Nobel prize in physics in 2010 [33], marked the beginning of the era of 2D materials research. Since then, 2D materials have enabled gate length scaling beyond beyond 1 nm [34], compared to earlier studies of state-of-the-art Si transistors reporting gate lengths of 10 nm [35] and 3 nm [36], see Figure 2.3b. Desai et al. utilized single-walled carbon nanotubes (SWCNTs) to scale the physical gate length to 1 nm, while demonstrating an SS of ~ 65 mV/dec [37], see Figure 2.3a and 2.3c. In 2022, Wu et al. demonstrated a vertical MoS₂ transistor with sub-1-nm gate lengths by incorporation of graphene as the gate [34], see Figure 2.3d. The effective channel length approaching 0.34 nm still exhibits an SS of ~ 121 mV/dec, see Figure 2.3e. Additionally, graphene can be utilized to scale the channel length of 2D semiconductors, as has been demonstrated in the work by Tian et al. [38]. They report a ~ 9 nm channel with low drain-induced barrier lowering (DIBL), demonstrating strong electrostatic control and suppressed SCEs in 2D semiconductor transistors.

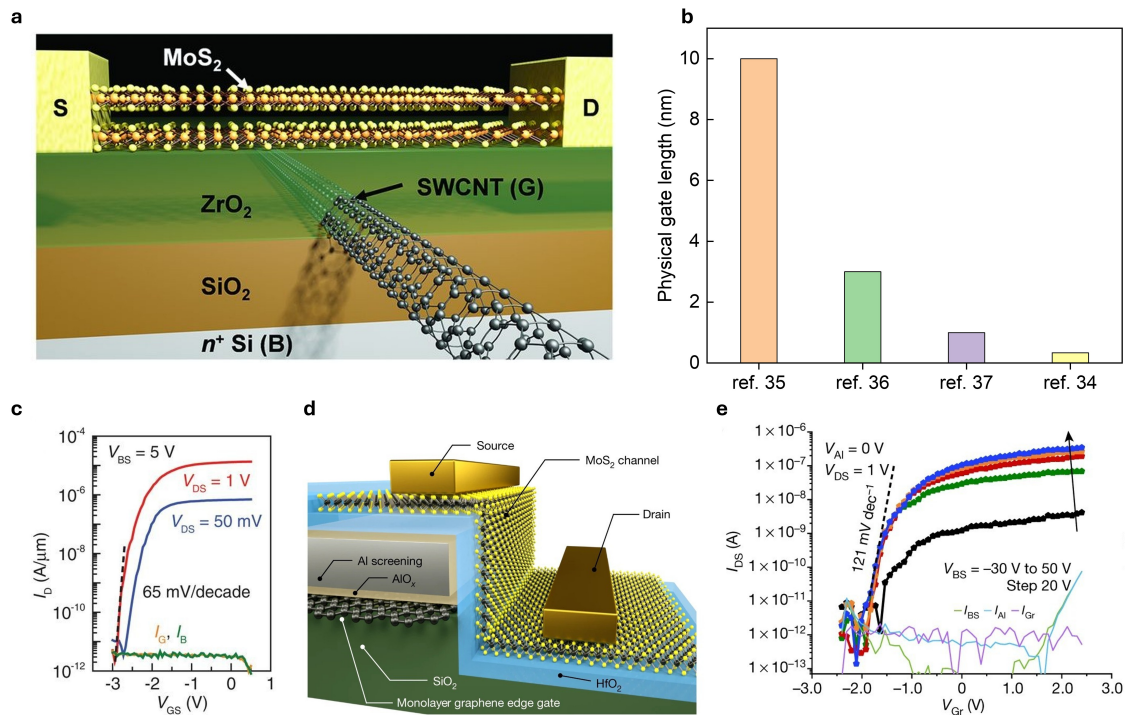


Figure 2.3: Scaling the physical gate lengths of state-of-the-art transistors. **(a)** Schematic of MoS₂ transistors gated by single-walled carbon nanotubes (SWCNTs). Figure reproduced from [37]. **(b)** Representative scaling of physical gate lengths. **(c)** Electrical characterization of the MoS₂ transistors with a SWCNTs as the gate electrode. Figure reproduced from [37]. **(d, e)** Schematic of graphene-gated vertical MoS₂ transistors and related electrical characterization. Figures reproduced from [34].

Among various 2D TMDs, MoS₂ FETs stand out as atomically scaled high-performance n-type transistors, reaching high on-state currents [7, 39, 40]. In a recent study, Sakib et al. reported an on-state current density of 460 $\mu\text{A}/\mu\text{m}$ for a trilayer MoS₂ device with a contact length of 30 nm and channel length of 35 nm [7]. However, p-type WSe₂ has emerged as a contender for high-performance transistors as well. In 2025, Ghosh et al. reported a high on-state current density of 421 $\mu\text{A}/\mu\text{m}$ for a nitric oxide (NO)-doped bilayer WSe₂ FET [41]. This year, Sun et al. reported an even higher on-state current density of 1245 $\mu\text{A}/\mu\text{m}$ for O₂-passivated monolayer WSe₂ FETs [42]. This high performance of 2D semiconductors when the thickness, and gate and channel lengths, are scaled is promising for beyond-Si transistor technologies [27]. Furthermore, scaling the width of the atomically thin semiconducting TMDs to the nanoribbon regime has in the last couple of years emerged as a promising strategy for scaled and versatile devices [18, 19].

Studies of the electrical transport properties in width-scaled TMD nanoribbon transistors have been conducted. Li et al. demonstrated bilayer MoS₂ nanoribbon transistors by nickel particle-enabled growth [16], see Figure 2.4a. These devices performed down to widths of 20 nm with an on-current density of 0.9 $\mu\text{A}/\mu\text{m}$, and degradation of the drive current for an 8 nm wide channel, see Figure 2.4b. In a study by Chen et al., monolayer MoS₂ nanoribbon transistors with a minimum channel width of 30 nm and on-current density of 0.3 $\mu\text{A}/\mu\text{m}$ were fabricated by scanning probe lithography [43], see Figure 2.4c and 2.4e. Furthermore, in a study by Hoque et al. they demonstrate nanoribbon transistors for 35 nm thick WS₂ [44]. By combining dry etching and anisotropic wet chemical etching they achieved working nanoribbon transistors with a minimum channel width of 18 nm, see Figure 2.4d and 2.4f. They measured on-current densities of approximately 18.9 and 0.58 $\mu\text{A}/\mu\text{m}$ for channel widths of 47 and 18 nm, respectively, and report a suppressed drive current with reduced channel width.

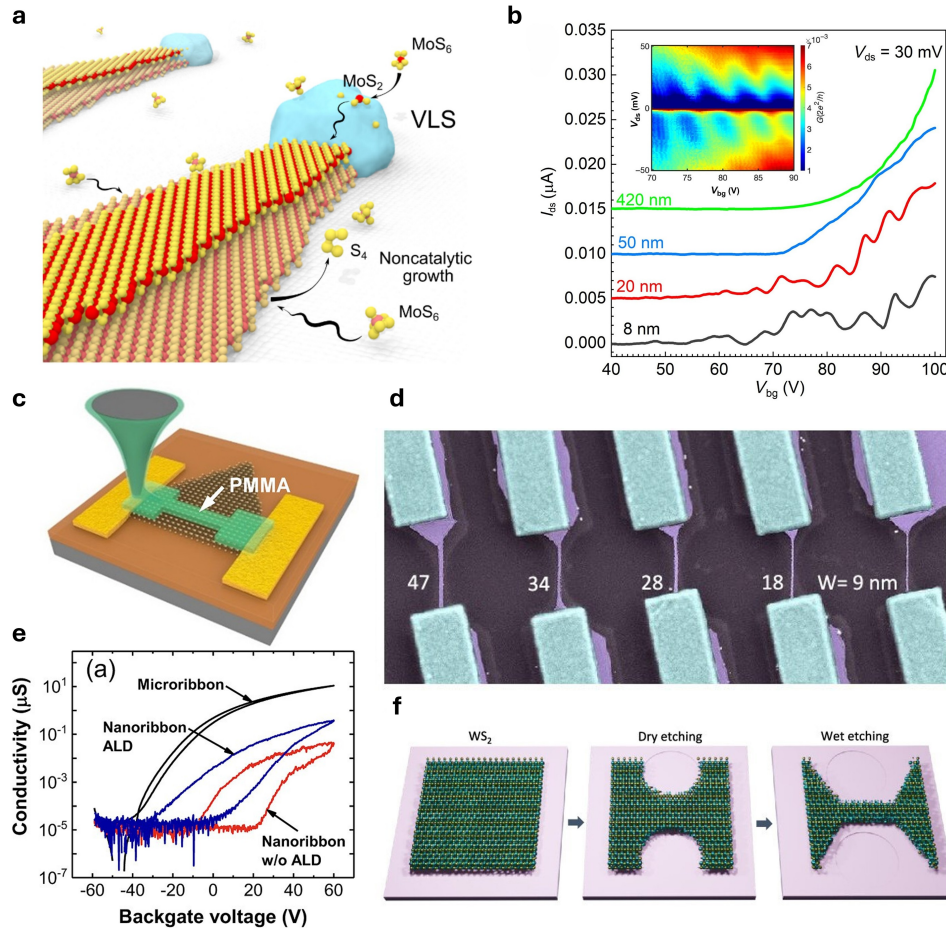


Figure 2.4: State-of-the-art scaling of 2D semiconductor nanoribbon transistors. **(a, b)** Schematic of nickel particle-enabled growth of bilayer MoS₂ nanoribbons and transfer characteristics of corresponding nanoribbon transistors. Figures reproduced from [16]. **(c, e)** Schematic of monolayer MoS₂ nanoribbons fabricated by scanning probe lithography and corresponding transfer characteristics. Figures reproduced from [43]. **(d, f)** SEM micrograph of WS₂ nanoribbons with widths from 9 to 47 nm, and a schematic of the fabrication process utilizing both dry etching and anisotropic wet chemical etching. Figures reproduced from [44].

The performance, i.e., maximum on-current density (I_D) and on/off ratio (I_{ON}/I_{OFF}) as a function of channel width (W_{CH}), of these fabricated devices as well as other nanoribbon transistors are shown in Figure 2.5a and 2.5b. Another study on monolayer MoS₂ nanoribbon transistors report on-current densities of approximately 38 $\mu\text{A}/\mu\text{m}$ for a channel width of 50 nm [45]. For thicker (6, 8, and 20 nm) MoS₂ nanoribbons of widths 60, 55, and 50 nm, on-current densities of approximately 16.4 [46], 2.5 [47], and 0.75 $\mu\text{A}/\mu\text{m}$ [48] have been reported, respectively.

Furthermore, there are reports of techniques to improve the performance of 2D semiconductor transistors. Studies have shown that resist residues heavily affect the performance of 2D semiconductor transistors, where methods like cleaning the surface with an atomic force microscopy (AFM) probe tip [50] or removing the resist residues by annealing [51] have been shown to improve the performance. Passivation of vacancies in the body and at the edges have been shown to improve performance as well, where edge-passivated 2D semiconductors have been shown to outperform corresponding non-passivated edges [51].

Atomically thin TMDs can not only enable further development in the scaling of high-performance transistor technologies, but have also been demonstrated in applications such as optoelectronics/photoreceptors [14, 52–54], photonics [54], photovoltaics [53], sensing [14], memory [55], memtransistors [56, 57], memristors [58–60], fuzzy logic hardware [61], logic electronics [48], artificial neurons [52, 62], neuromorphic computing [58], and artificial neural networks (ANNs) [56]. Hence, 2D semiconductors can enable further development of beyond Boltzmann and non von-Neumann computational frameworks capable of delivering ultra-low power operation [63].

3

Structural and Electronic Properties of Two-dimensional Semiconductor Nanoribbons

The structural and electronic properties of 2D semiconductors and their corresponding nanoribbons are presented in this chapter. It is divided into three sections, where the first expounds TMD nanoribbon edge effects and synthesis methods. This is followed by a description of the electronic structures of atomically thin MoS₂ nanoribbons, and finally the dynamics of 2D semiconductor-metal interfaces.

3.1 Nanoribbon Edge Structures and Synthesis Methods

For the majority of the semiconducting TMDs, three crystal phases are commonly observed [64]. The most thermodynamically stable and therefore most commonly found phase is the semiconducting 2H phase, which has trigonal prismatic Mo–S coordination and AB stacking. The metallic 1T phase and the semiconducting 3R phase are metastable. The 3R phase differs from the 2H phase in its ABC stacking sequence, while the 1T phase has octahedral Mo–S coordination with AA stacking, changing the electronic structure to a metallic behaviour.

Scaling down the thickness and width of materials enhances the impact of surface and edge states [65], and the same applies for 2D semiconducting TMDs. Figure 3.1 shows the edge structure configurations of monolayer MoS₂ as well as the electrochemical current along MoS₂ nanoribbons of varying widths, reproduced from the work of Ma et al. [66] where they did hydrogen evolution reaction (HER) current mapping to extract the current profile of the nanoribbons.

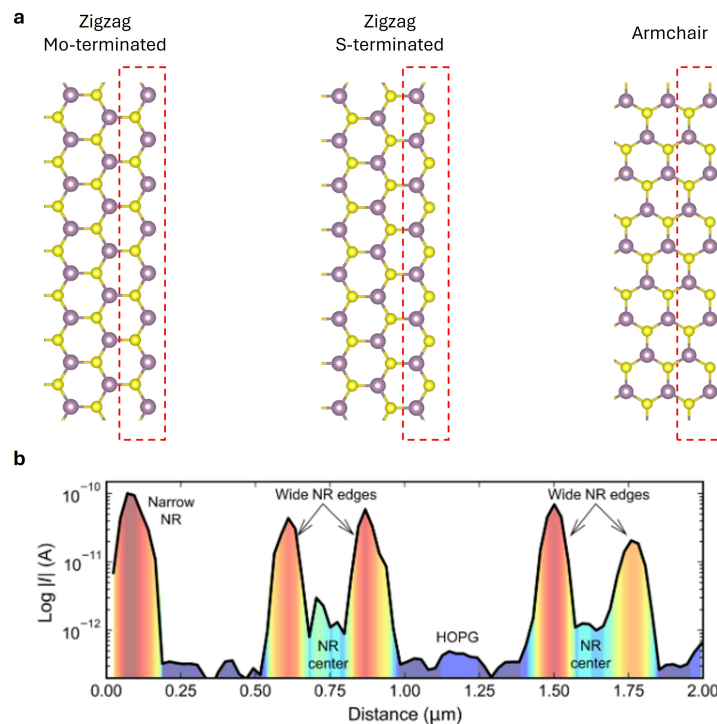


Figure 3.1: TMD sheet and nanoribbon edge termination configurations and their effects. **(a)** Edge-termination configurations for MoS₂ (as well as WS₂, MoSe₂, and WSe₂). The edges can either be zigzag-terminated, with Mo exposed at the edge (Mo-terminated) or S exposed at the edge (S-terminated), or armchair-terminated. **(b)** Current profile along MoS₂ nanoribbons with varying widths, acquired with HER current mapping. Figure reproduced from [66].

The edge structures of the 2H phase for 2D TMD materials such as MoS₂, WS₂, MoSe₂, and WSe₂ exist in two different configurations, namely zigzag-terminated and armchair-terminated [67–69]. The zigzag edges can be terminated by the transition metal (M-terminated) or by the chalcogen (X-terminated). Zigzag terminations are energetically more favourable than armchair, and show a more ferromagnetic and metallic behaviour than the bulk [67, 69]. Armchair-terminated nanoribbons on the other hand are non-magnetic and more semiconducting than zigzag edges, but still exhibit a smaller band gap than the bulk. Theoretical and experimental studies show that the edges of TMD nanoribbons exhibit higher catalytic reactivity and higher currents [66]. Hence, scaling nanoribbons will impose a high and homogeneous current profile over the entire nanoribbon, instead of only at the edges. In reality, the edges of TMD nanoribbons are naturally passivated by ambient chemical species [68, 70]. Common molecules such as oxygen (O₂) or water (H₂O) adsorb on the surface and edges of TMD nanoribbons, altering the edge structure and electronic environment.

Although atomically thin TMDs and their respective 1D nanoribbons exhibit extraordinary intrinsic properties, excellent for future applications, the method of synthesizing them in a controlled and versatile way is still challenging. Bottom-up approaches have been demonstrated to regularly result in narrow and thin TMD nanoribbons, often with a controlled edge-termination. It is not unusual to utilize templates, such as nanotubes or substrate lattices.

In the work of Tanaka et al. they demonstrated the growth of ultra-narrow MoS₂ nanoribbons within boron nitride nanotubes to an average width of 3.8 nm (1.4 – 8.9 nm), with varying thicknesses [67]. In the works by Cain et al. [71] and Wang et al. [72] they utilize carbon nanotubes (CNTs) to synthesize monolayer TaS₂ and MoS₂ nanoribbons with widths down to 2.5 and 1.3 nm, respectively. Tanaka et al. and Wang et al. identified the edges of their synthesized nanoribbons to be of zigzag-terminated nature, while Cain et al. reported a zigzag-like superstructure in their nanoribbons. Ma et al. reported a self-aligned lattice-guided growth on sapphire of monolayer MoS₂ nanoribbons below widths of 10 nm with zigzag-terminated edges [66]. Similarly, Chen et al. reported stable 1H-phase MoS₂ nanoribbons with zigzag edges down to widths of 13 nm by growth with molecular beam epitaxy onto a highly oriented pyrolytic graphite substrate [68]. There have also been reports of bottom-up approaches utilizing particle-assisted growth with nickel (Ni) nanoparticles [16] and nano-alloy seeds [73], reaching 10 nm wide bilayer MoS₂ nanoribbons and 7–10 nm wide monolayer MoS₂ and WSe₂ nanoribbons, respectively. Lastly, Schock et al. demonstrated synthesis of MoS₂ flakes as well as nanoribbons and nanotubes of a wide range of diameter by growth from vapour phase [74]. The nanotubes reached diameters of 20 nm, while the nanoribbons were at a minimum 20 nm thick and 155 nm wide. Although these techniques often yield a high density of ultra-narrow and thin TMD nanoribbons, they lack controllability and versatility in the fabrication, especially when utilized for transistor devices.

Top-down approaches on the other hand often utilize different variations of etching techniques to fabricate TMD nanoribbons from larger flakes. The larger flakes are commonly mechanically exfoliated or grown by chemical vapour deposition (CVD) [75]. As mentioned in Chapter 2, Hoque et al. demonstrated an approach where they combine dry plasma etching and anisotropic wet chemical etching to realize WS₂ nanoribbons of widths down to 9 nm and a thickness of 35

nm [44]. Canton-Vitoria et al. demonstrated a method where the CVD-growth of MoS_2 creates a dominating 1T-phase at the centre of the triangular flakes and a dominating 2H-phase at the edges [76]. They then utilized the higher oxidative reactivity for the 1T-phase compared to the 2H-phase to etch the middle with O_2 plasma etching, resulting in monolayer nanoribbons down to widths of 25 nm. Approaches using PMMA masks in the shape of the nanoribbons deposited on the surface of monolayer TMD flakes have also been demonstrated to yield nanoribbons with minimum widths of 40 nm [77] and 30 nm [43]. Top-down approaches utilizing templated etching with different kinds of nanostructures have also been demonstrated, such as nanowires [48] or organic nanostructure networks [18]. These kinds of techniques can result in ultra-narrow monolayer TMD nanoribbons, but lack control over the width, and versatility and simplicity in device design. The same disadvantage can be seen in the work by Saunders et al. where they demonstrated successful direct exfoliation of 20 nm wide monolayer nanoribbons from bulk vdW crystals [78]. Sasikala et al. demonstrated a longitudinal unzipping of the 1T'-phase and 2H-phase of monolayer TMDs resulting in nanoribbons with widths down to 10 nm [79]. However, this synthesis method is not suitable for nanoribbon device fabrication as the nanoribbons are randomly distributed in solution.

Combining lithography techniques with dry etching seems to be the best option when trying to reach the ultimate goal of atomically thin TMD nanoribbons in electronic devices. As early as 2012, Liu et al. demonstrated the fabrication of MoS_2 nanoribbon transistors by lithography and plasma dry etching [46]. However, their minimum thicknesses and widths were 6 nm and 60 nm, respectively. Early in 2019, Kotekar-Patil et al. managed to fabricate monolayer MoS_2 nanoribbon transistors by lithography and etching techniques, with minimum widths of 50 nm [45]. Very recently, Peña et al. demonstrated scaling of monolayer MoS_2 nanoribbon transistors to minimum widths of approximately 25 nm [49]. Another recent study, still under review, report fabrication of nanoribbons to widths of approximately 30-40 nm [80]. Notably, there is also a study demonstrating the scaling of MoS_2/WS_2 heterostructures to thicknesses below 10 nm and widths between 20 and 350 nm [81], showing the possibilities of scaled TMD nanoribbon structures beyond homostructures.

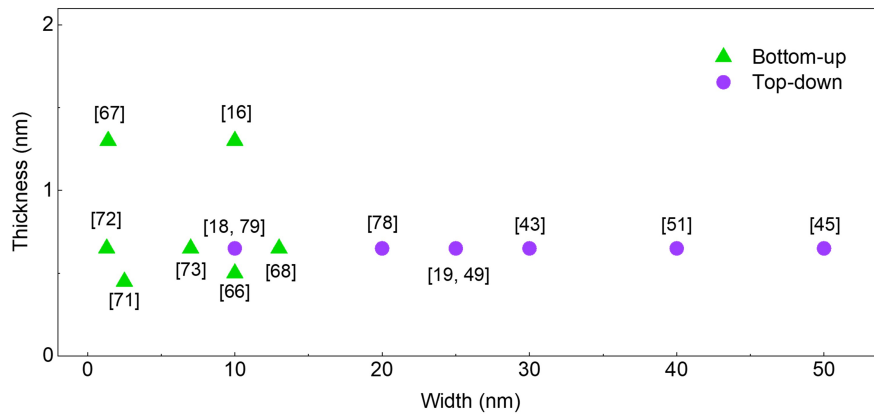


Figure 3.2: Comparison of minimum achieved thicknesses and widths for nanoribbons with a variety of state-of-the-art bottom-up (green triangles) and top-down (purple circles) approaches.

Minimum achieved thickness and width of nanoribbons for each state-of-the art nanoribbon fabrication method is shown in Figure 3.2. The comparison showcases the difference between bottom-up approaches (green triangles) and top-down approaches (purple circles). The bottom-up fabrication methods exhibit apparent advantages in reaching ultra-scaled widths and control in the edge configuration. The top-down approaches appear to have challenges in the scaling, especially for thinner flakes such as monolayer or bilayer. However, they are more versatile in the sense of device fabrication and width-control, important for studies of width-dependent transistor characteristics.

3.2 Electronic Structures

Theoretical electronic band structures for monolayer MoS₂, and the corresponding zigzag- and armchair-terminated edges are shown in Figure 3.3. The band structures are reproduced from the work of Dias et al. [15]. It also presents photoluminescence (PL) spectra of MoS₂ nanoribbons of varying widths from the works of Canton-Vitoria et al. [76] and Li et al. [73]. As mentioned in the Introduction, see Chapter 1, the band structure of the semiconducting TMDs transitions from an indirect band gap to a direct band gap in the K-point of momentum space when decreasing the number of layers to one [13, 14, 82]. This is due to quantum confinement effects when reducing the dimensionality from three to two. For MoS₂ it is widening from ~1.2-1.3 eV to ~1.8-1.9 eV. Edges and nanoribbons MoS₂ have been studied extensively as they offer an electronic structure that combines features of MoS₂ and graphene [83]. Studies often point to metallic or semi-metallic zigzag-terminated edges with a narrower band gap, whereas armchair-terminated edges remain with finite band gaps and semiconducting properties. Bollinger et al. predicted metallic edges in MoS₂ nanoribbons using electronic structure calculations [84]. The effect of short- and long-range disorder on MoS₂ zigzag nanoribbons has been studied by Ridolfi et al., where it was found that the metallic states are robust against structural disorder [85].

Additional studies include the work of Li et al. [69] where they through spin-polarized calculations predicted that zigzag MoS₂ nanoribbons are magnetic and are more stable than triangular nanoclusters, and Kim et al. [86] who found that armchair nanoribbons can be stabilized by hydrogen (H) adsorption and possess a semiconducting character with strong excitonic effects. However, in reality, strained crystal structures achieving the actual minimized energy states and passivation of the terminated bonds at the edges alter the electronic structure [68]. Experimental studies show blue-shifted PL spectra when decreasing the widths of monolayer MoS₂ nanoribbons [73, 76]. The aspect ratio of edges to body is increased when narrowing the width, resulting in a higher contribution from the edge states which causes the shift [82]. Although, the optical spectra might possibly be governed by excitonic effects as the scaled width results in reduced screening and enhanced electron-electron interactions [87].

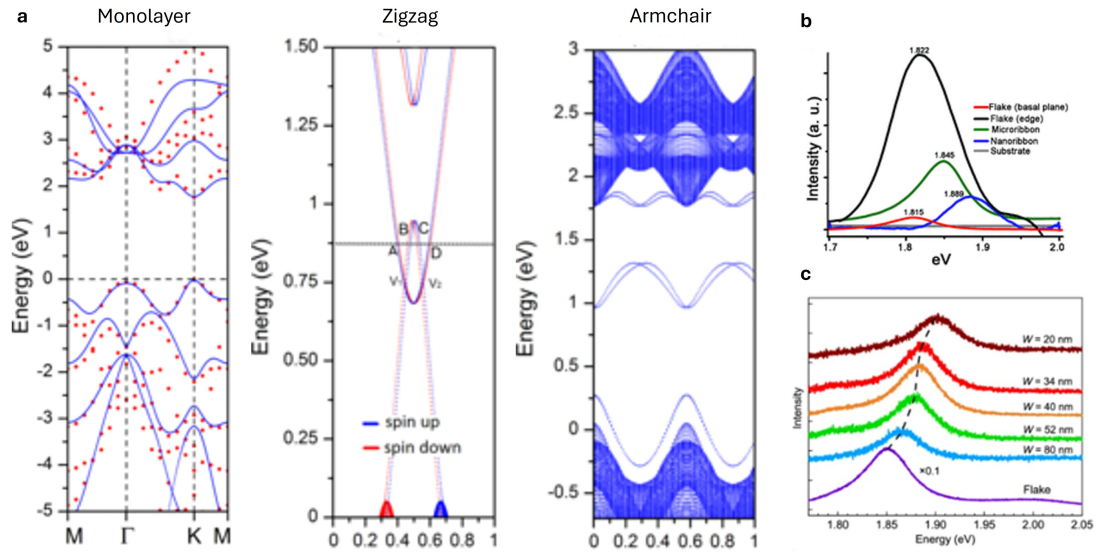


Figure 3.3: Theoretical electronic band structures of monolayer MoS₂ and its edges, as well as experimental PL spectra of monolayer MoS₂ nanoribbons of varying widths. **(a)** Electronic band structures calculated with DFT for monolayer MoS₂ (left), a zigzag-terminated edge on monolayer MoS₂ (middle), and an armchair-terminated edge on monolayer MoS₂ (right). Figures reproduced from [15]. **(b)** PL spectra of monolayer metallic/semiconducting MoS₂ with the 2H-phase at the edges. PL spectra were acquired for a flake (basal plane), flake (edge), microribbon, and nanoribbon. Figure reproduced from [76]. **(c)** PL spectra of monolayer MoS₂ for a flake, and nanoribbons of widths 20, 34, 40, 52, and 80 nm. Figure reproduced from [73].

3.3 Contact Engineering of Two-dimensional Semiconductors

For conventional bulk semiconductor-metal interfaces with overlapping orbitals creating covalent bonding, the injection of charge carriers (electrons or holes) heavily depends on the difference between the energy landscape of the metal and the semiconductor [88]. A heavily n-doped semiconductor with a shifted Fermi level (E_F) towards the conduction band (E_C) will exhibit a lower semiconductor work function (Φ_s). To achieve ohmic charge injection to and from the semiconductor, rather than rectifying behaviour, the metal work function (Φ_M) must be smaller than that of the semiconductor. For p-type semiconductors, the opposite condition applies. If Φ_M is greater than the electron affinity (χ) of an n-type semiconductor, a Schottky barrier (SB) will be created at the interface [63, 88]. The ideal Schottky barrier height (SBH) for an n-type semiconductor is presented in Equation 3.1.

$$\Phi_{Bn} = \Phi_M - \chi \quad (3.1)$$

The work functions of the elemental metals bismuth (Bi), silver (Ag), aluminium (Al), titanium (Ti), antimony (Sb), nickel (Ni), gold (Au), palladium (Pd), and platinum (Pt) are presented in Table 3.1.

Table 3.1: The elemental metals Bi, Ag, Al, Ti, Sb, Ni, Au, Pd, and Pt and their corresponding work functions (Φ_M). All values are taken from [89].

Element	Bi	Ag	Al	Ti	Sb	Ni	Au	Pd	Pt
Φ_M (eV)	4.25	4.26	4.28	4.33	4.55	5.09	5.10	5.12	5.65

Metal-contacting to 2D semiconductors work a bit differently as they lack out-of-plane dangling bonds [40]. Additionally, contact engineering to 2D semiconductors are highly challenging due to Fermi-level pinning and quantum tunnelling barriers [90]. Depending on the metal, the interface can either create a vdW gap, a reduced vdW gap or hybridized covalent bonding overlapping the band structures affecting the charge-injection mechanisms [40]. There are two mechanisms by which charge-injection into a 2D semiconductor, either by thermionic emission over the SB or tunnelling through the SB. The metal contact can also be situated at two different locations, either on the top/bottom or at the edge.

The electron affinities for some common TMDs (MoS_2 , MoSe_2 , MoTe_2 , WS_2 , WSe_2 , WTe_2) with varying thickness (1 layer to bulk) are between 3.65 eV and 4.38 eV [91]. Hence, an SB will almost always be present at the interface of metals on TMD semiconductors. However, Bi and Sb has been shown in multiple studies to form excellent ohmic contacts because of their semimetal properties [39, 74, 92]. Figure 3.4 shows schematics of a 2D semiconductor-metal interface in a top-contact configuration with the injection of an electron, as well as the energy band diagram of an interface with a vdW gap and SB showing the tunnelling of an electron through the quantum tunnelling barrier. Additionally, a schematic showcasing the injection of electrons from the Fermi level of metals exhibiting different Φ_M to the conduction band of an n-type semiconductor is presented.

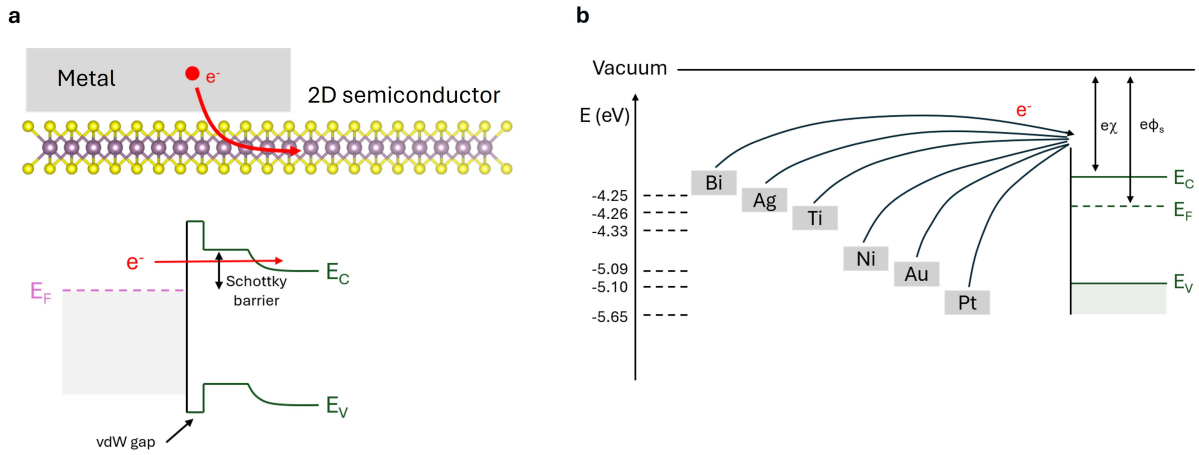


Figure 3.4: Schematics of electron injection from the contact metal to a 2D semiconductor when a vdW gap is present, as well as an energy diagram showcasing the importance of metal work functions. **(a)** Charge carrier injection of an electron into monolayer MoS_2 with equivalent energy band diagram of the tunneling of the electron through the interface. The Fermi level of the metal, conduction band of the semiconductor, and valence band of the semiconductor are denoted by E_F , E_C , and E_V , respectively. **(b)** E_C , E_F , and E_V are the semiconductor conduction band, Fermi level, and valence band, respectively.

Contact engineering in 2D semiconductors depends not only on metal work functions but heavily on the interaction between contact materials and the 2D semiconductor during and after metal deposition. In a study by Schauble et al., they uncovered the effects of contact deposition on monolayer MoS_2 [93]. Ti, Sc, and yttrium (Y) oxidize and react with the monolayer MoS_2 , negatively impacting the contact resistance. Ultra-thin Al oxidizes and dopes MoS_2 , while Ag, Au, and Ni introduce variational levels of damage on the monolayer MoS_2 during deposition. Additionally, Ag, Au, and Ni do not bond covalently with MoS_2 , but interacts via interlayer vdW interactions, creating a vdW gap. Although the latter metals can cause some degree of damage, it is important to note that some of the highest-performing contacts have been achieved using these metals.

Experimental Methods

The methodology of this work, conducted at Chalmers University of Technology, consisted of fabrication, measurements, characterization, and data analysis. The nanofabrication of the 2D semiconductor MoS₂ nanoribbon transistors was carried out at the MyFab Nanofabrication Laboratory. Electrical measurements on the fabricated devices were carried out at the Quantum Device Physics Laboratory. Characterization was performed at the MyFab Nanofabrication Laboratory as well as Chalmers Materials Analysis Laboratory (CMAL). The transistors were fabricated on 7x7 mm substrates diced from a 4-inch wafer, purchased from HQ Graphene, with p⁺⁺-doped Si and a 285 nm thick layer of SiO₂ as the gate dielectric. All device designs were prepared using AutoCAD 2026. An example of the designs is depicted in Figure 4.1. The template used for the AutoCAD base file, fitting the dimensions and markers for the 7x7 mm chips and serving as the starting point for all designs, was created by Dmitrii Khokhriakov.

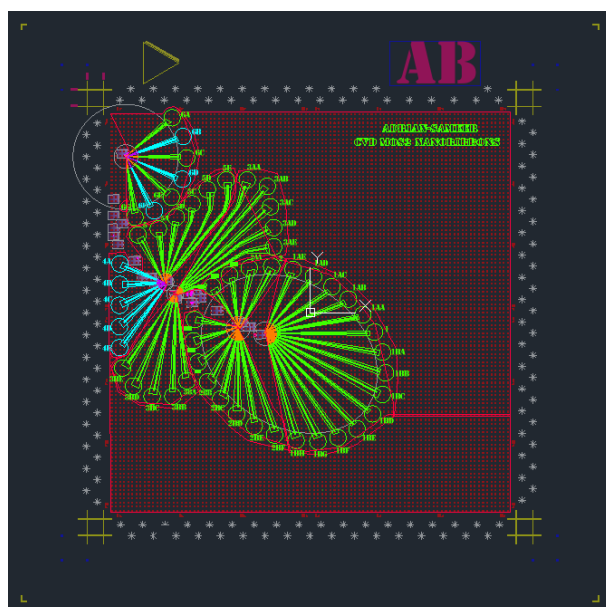


Figure 4.1: Example of an AutoCAD design for the fabricated devices.

4.1 Fabrication

Transistor devices based on MoS₂ were fabricated by top-down approaches, and by selecting important device parameters such as channel length (L_{CH}), channel width (W_{CH}), and contact materials. This section presents the nanofabrication methodology of this work, including the preparation of the 2D semiconductor materials, the fabrication of ultra-narrow nanoribbons, and the fabrication of the contacts. A more thorough description of the fabrication process with detailed recipes can be found in Appendix A.

4.1.1 Two-Dimensional Semiconductor Nanoribbons

Mono- and bilayer MoS₂ was prepared with mechanical exfoliation from bulk MoS₂, purchased from HQ Graphene. The exfoliation was carried out using Nitto tape and then transferred to a clean Si/SiO₂ substrate with PDMS tape. The Si/SiO₂ substrates with exfoliated MoS₂ were viewed with an optical microscope and areas with mono- and bilayer flakes were imaged. Selected images were then aligned in AutoCAD to create the designs of the nanoribbons.

The workflow of the nanoribbon fabrication can be seen in Figure 4.2. The electron beam (e-beam) resist AR-P 6200.13 1:2 was spin-coated at 6000 rpm for 60 seconds and then soft baked at 150 °C for 60 seconds on a hot plate. The designs were then defined with electron beam lithography (EBL) (Raith EBPG 5200, 100 kV acceleration voltage). Development was performed by submerging in n-amyl acetate for 90 seconds, followed by isopropyl alcohol (IPA) for 30 seconds. The chips were then gently blow dried with nitrogen (N₂) gas. Etching of the monolayer and bilayer MoS₂ was conducted using the Oxford Plasmalab 100 Inductively Coupled Plasma/Reactive Ion Etcher (ICP/RIE). The MoS₂ was etched for 5 seconds with a plasma consisting of trifluoromethane/argon (CHF₃/Ar) (50/40 sccm). During the plasma etching, the top layer of the AR-P resist may get hardened, making it difficult to dissolve. Therefore, O₂-plasma stripping (10 sccm, 50 W, 250 mTorr, 10 s) was performed with a PlasmaTherm RIE to etch away the top layer of the resist. The resist was then dissolved in acetone for 24 hours, followed by IPA for 5 minutes and gently blow dried with N₂ gas.

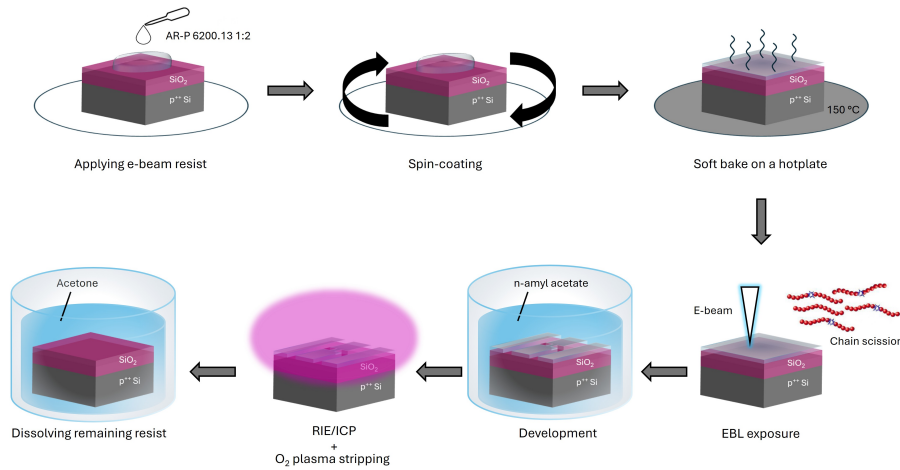


Figure 4.2: Workflow of the 2D semiconductor nanoribbon fabrication. This includes the spin-coating of the resist, soft baking, EBL exposure, development, etching and O₂-plasma stripping, and finally dissolution of the remaining e-beam resist.

4.1.2 Source and Drain Electrodes

The fabrication of the top-contacts was conducted by first spin-coating a bilayer resist stack on top of the chips. Figure 4.3 shows the workflow of the spin-coating. The bottom layer consisted of the e-beam resist P(MMA 8.5 MAA) EL8 and the top layer of the e-beam resist AR-P 6200.13 1:2. Both were spin-coated at 6000 rpm for 60 seconds, and then soft baked at 130 °C for 10 minutes on a hotplate.

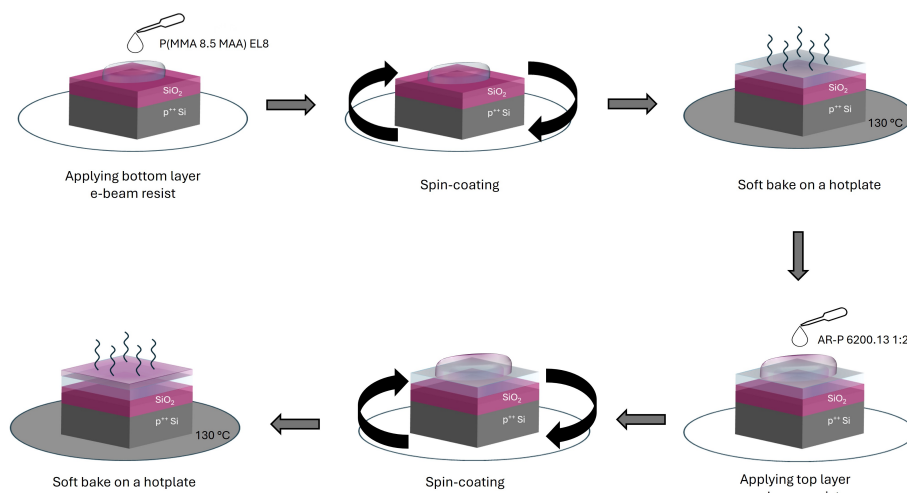


Figure 4.3: Workflow of the spin-coating of the bilayer P(MMA 8.5 MAA) EL8/AR-P 6200.13 1:2 resist stack for contact fabrication. Both resist layers were spin-coated at 6000 rpm for 60 seconds and then soft baked at 130 °C for 10 minutes.

The contact designs were defined on the spin-coated chip via exposure with EBL (Raith EBP 5200, 100 kV acceleration voltage). The exposure was divided into two different areas, high-resolution features and low-resolution features, with e-beam currents of 5 nA and 100 nA, respectively. Figure 4.4 shows the workflow of the remaining steps for the contact fabrication, with schematics for each step. The exposed areas were developed in n-amyl acetate for 50 seconds and then methyl isobutyl ketone (MIBK):IPA 1:1 for 1 minute and 10 seconds, followed by gentle blow drying with N₂ gas. Thin film deposition of the contacts were conducted with electron beam physical vapour deposition (EBPVD) using the e-beam thin film evaporator Lesker PVD 225, depositing 20/20 nm Ni/Au. Lift-off was performed by immersion in acetone for 30 minutes with gentle agitation by pipetting, followed by the chip being submerged in IPA for 5 minutes and then blow dried with N₂ gas.

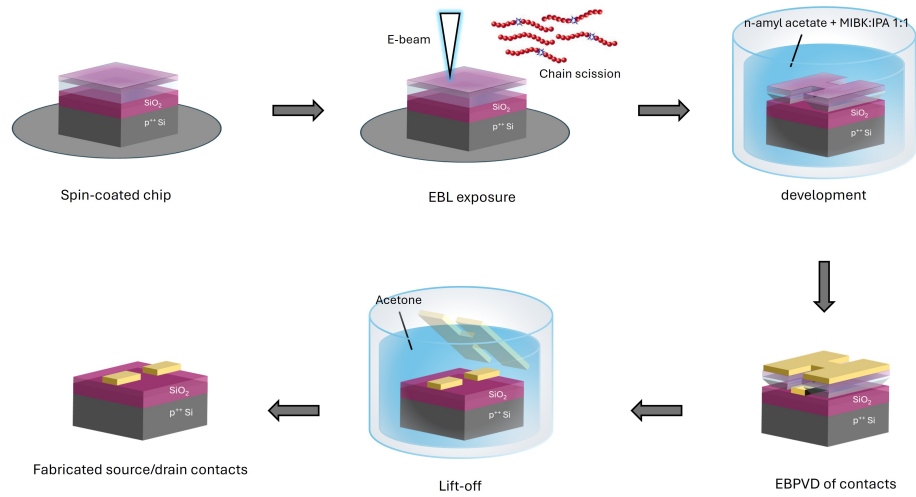


Figure 4.4: Workflow of the continued nanofabrication process for the contacts after completing the coating of the bilayer resist stack. This includes exposure with EBL, development in n-amyl acetate and then MIBK:IPA 1:1, followed by EBPVD of Ni and Au as the source and drain contacts, and then immersion in acetone for lift-off.

4.2 Measurements

Electrical measurements for transistor characterization were performed in room-temperature (~295 K) with a single channel source measure unit Keithley 2400 and a dual channel source measure unit Keithley 2612B. The chips were first attached to a bonding substrate with silver paint, see schematic in Figure 4.5. The bonding substrate consists of a gold plate in the middle,

with 16 bonding pads surrounding it, four on each side. These are connected to soldered pins that extend downwards on the backside. The contacts were then bonded with gold wires using an iBond5000 Wedge Model wire bonder. The gate was bonded to the central gold plate. The bond substrate was mounted in a holder and then put under vacuum ($\sim 10^{-4}$ mbar) with a turbo pump. Measurements were then conducted with a LabView program to control V_D and V_G and a switchbox to control which devices to measure. The drain was biased positively and the source negatively with respect to ground. The back-gate was biased positively relative to the source, which was connected to ground.

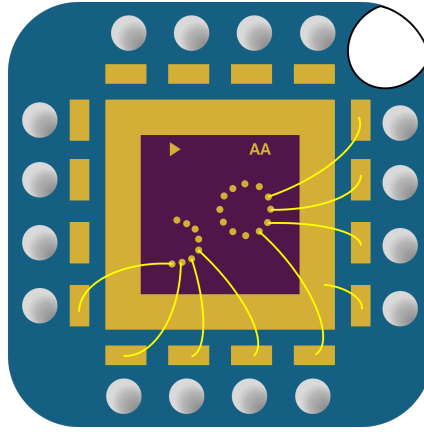


Figure 4.5: Schematic of the bonding substrate used for electrical measurements.

4.3 Material and Device Characterization

The characterization of the MoS_2 nanoribbons and nanoribbon FETs was performed with scanning electron microscopy (SEM), atomic force microscopy (AFM), and Raman spectroscopy. Continuous evaluation of the fabrication process was performed with an optical microscope. Evaluation of the width and length of the nanoribbons was conducted with the Zeiss Supra 60 VP, EOS Gemini 1, scanning electron microscope (SEM). Besides the evaluation, the electron microscope was also used to acquire micrographs of the devices. Characterization of the resist height, etching depth, and nanoribbon profile was performed with AFM using the Bruker dimension ICON scanning probe microscope (SPM). To identify the number of layers the devices were fabricated from, Raman spectroscopy was performed in CMAL with the scanning confocal Raman microscope system WITech alpha300 R with a 532 nm green laser.

4.4 Data Processing and Analysis

Acquired electrical measurement data was plotted and analysed with OriginPro 2023. Values for the electron field-effect mobility (μ_{FE}) and threshold voltage (V_{TH}) were extracted by fitting of the linear non-saturated region of the linear transfer characteristics. The transconductance ($g_m = \partial I_D / \partial V_G$) was extracted from the slope of the linear fit and used to calculate μ_{FE} [88], see Equation 4.1. For the 285 nm SiO₂, a value of $1.212 \cdot 10^{-8}$ F/cm² was used for the oxide capacitance, see Equation 4.2. V_{TH} was determined by extracting the intercept of the linear fit at $I_D = 0$. Gwyddion was used to process and analyse the AFM images. Height profiles were then extracted and plotted in OriginPro 2023. Processing and colouring of the SEM micrographs were performed using ImageJ. Structural images of MoS₂ were generated with the corresponding crystallographic information file (CIF) [94] in Vesta.

$$\mu_{FE} = \frac{g_m L_{CH}}{W_{CH} C_{ox} V_D} \quad (4.1)$$

where g_m is the transconductance, L_{CH} the channel length, W_{CH} the channel width, C_{ox} the oxide capacitance, and V_D the source-drain bias voltage.

$$C_{ox} = \frac{\epsilon_r \epsilon_0}{t_{ox}} = \frac{3.9 \cdot 8.854 \cdot 10^{-14} \text{ F/cm}}{285 \cdot 10^{-7} \text{ cm}} \approx 1.212 \cdot 10^{-8} \text{ F/cm}^2 \quad (4.2)$$

where ϵ_r is the relative permittivity of SiO₂, ϵ_0 the vacuum permittivity, and t_{ox} the thickness of SiO₂.

5

Ultra-narrow Two-dimensional Semiconductor Nanoribbon Transistors

This chapter presents the results of this work with thorough AFM and SEM characterization of the nanoribbons and electrical transport properties for the fabricated devices. The monolayer MoS₂ nanoribbons showcase vertical and straight etching profiles, as well as accurate widths when compared to design. Ultra-scaled nanoribbons down to a width of ~15 nm were also achieved. Raman spectroscopy measurements confirmed the nanoribbons to be mono- and bi-layer. The electrical characterization revealed higher current densities as the width is decreased from 50 nm to 30 nm for monolayer MoS₂ and 80 nm to 30 nm for bilayer MoS₂. The electrical transport properties are then slightly reduced and saturated at high on-current densities when decreasing the width beyond 30 nm for bilayer MoS₂.

5.1 Scaling the Width of Atomically Thin MoS₂

Width-scaled MoS₂ nanoribbons of widths ranging from 15 nm to 200 nm were fabricated with the optimized fabrication recipe, see Appendix A. Figure 5.1 shows AFM images depicting monolayer MoS₂ nanoribbons of ranging widths etched with the optimized ICP/RIE parameters, as well as the height of the resist measured with AFM. The nanoribbons exhibit accurate, straight, and vertical etch profiles. The height of the single-layer resist AR-P 6200.13 1:2 dilution in anisole spin-coated at 6000 rpm for 60 seconds with a rotational acceleration of 1500 rpm/s² was measured with AFM to be approximately 55 nm for the EBL doses 220, 240, and 260 $\mu\text{C}/\text{cm}^2$. This resulted in an aspect ratio of ~ 0.27 for the 15 nm wide nanoribbons and ~ 3.64 for the 200 nm wide nanoribbons.

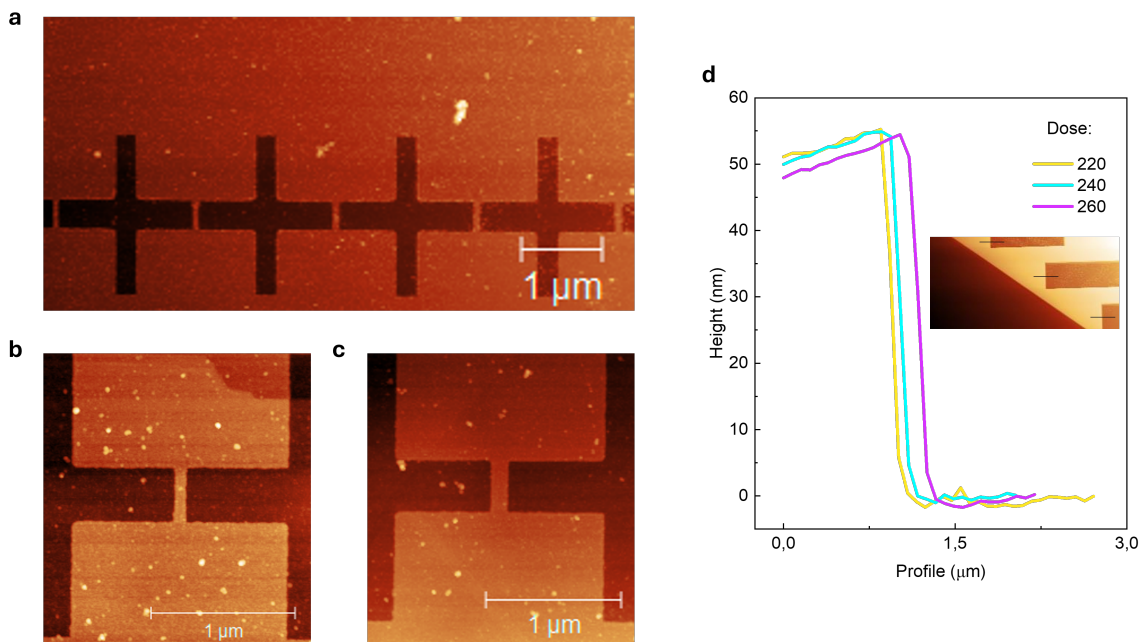


Figure 5.1: AFM characterization of MoS₂ nanoribbon fabrication. (a), (b), and (c) AFM images of fabricated nanoribbons of ranging widths with straight and vertical etching profiles. (d) Measured height profile of the e-beam resist AR-P 6200.13 1:2 spin-coated at 6000 rpm for 60 seconds, at an acceleration of 1500 rpm/s². Inset: AFM image of the location of the AFM characterization with the black lines marking the spots for the resist height measurements.

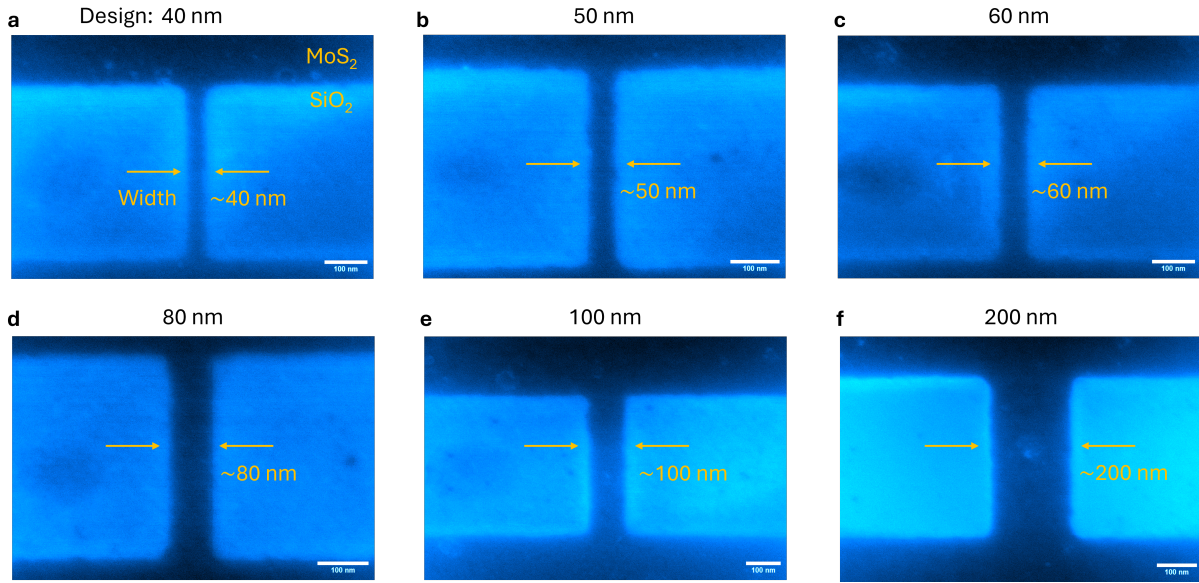


Figure 5.2: False-coloured SEM micrographs of monolayer MoS₂ nanoribbons showcasing accurate widths according to design and straight profiles. The widths of the nanoribbons are approximately (a) 40 nm, (b) 50 nm, (c) 60 nm, (d) 80 nm, (e) 100 nm, and (f) 200 nm. Scale bar = 100 nm.

Accurate fabrication of nanoribbons with widths according to design was achieved with the optimized process. Figure 5.2 shows false-coloured SEM micrographs of monolayer MoS₂ nanoribbons of lengths ~ 400 nm and approximate widths 40, 50, 60, 80, 100, and 200 nm. Each fabricated nanoribbon is approximately the same width as was intended according to design, with deviations reaching 2–3 nm at most. Additionally, acquired edge profiles are straight with minimal damage. These results showcase the accuracy and quality of the optimized 2D semiconductor nanoribbon fabrication.

The optimized fabrication recipe did not only successfully produce nanoribbons with accurate widths, but also managed to achieve sub-50 nm downscaling of the width. Figure 5.3 shows false-coloured SEM micrographs of ~ 400 nm long nanoribbons and sub-50 nm widths where monolayer MoS₂ nanoribbons with widths down to ~ 15 nm were successfully fabricated. The 30 and 40 nm wide nanoribbons exhibit straight edges, but as the width is decreased beyond 30 nm variations in the edge structures begin to emerge. Despite their ultra-narrow width sufficiently straight edges with a vertical etching profile. No nanoribbon exhibit damaged or broken parts. Nanoribbons with designed widths of 5 nm and 10 nm were fabricated on monolayer MoS₂ as well. These were characterized with SEM where it was observed that all of them were broken.

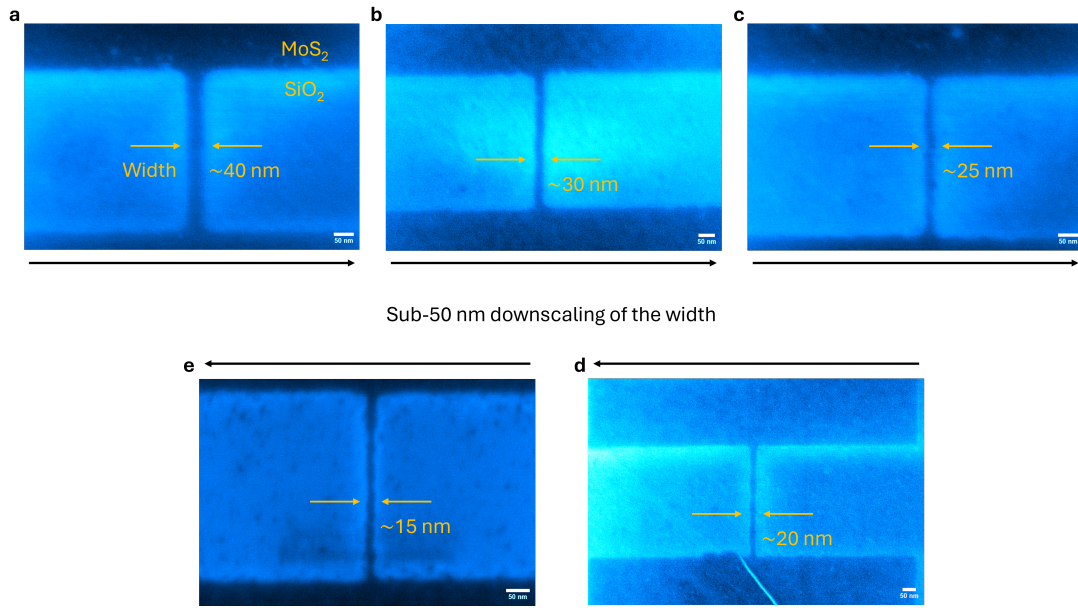


Figure 5.3: False-coloured SEM micrographs of monolayer MoS₂ nanoribbons showing the sub-50 nm downscaling of the nanoribbon widths. The widths were narrowed to approximately (a) 40 nm, (b) 30 nm, (c) 25 nm, (d) 20 nm, and (e) 15 nm. Scale bar = 50 nm.

Figure 5.4 shows the benchmarking of the MoS₂ nanoribbons achieved in this work against state-of-the-art lithographic top-down approaches on mono- and bilayer 2D semiconductors (2DSCs). The results of the nanofabrication of mono- and bilayer MoS₂ reaching 15 nm benchmarks the width scaling in this work (coloured stars) compared to earlier studies (blue spheres) utilizing lithography and etching to fabricate individual nanoribbons of atomic thicknesses.

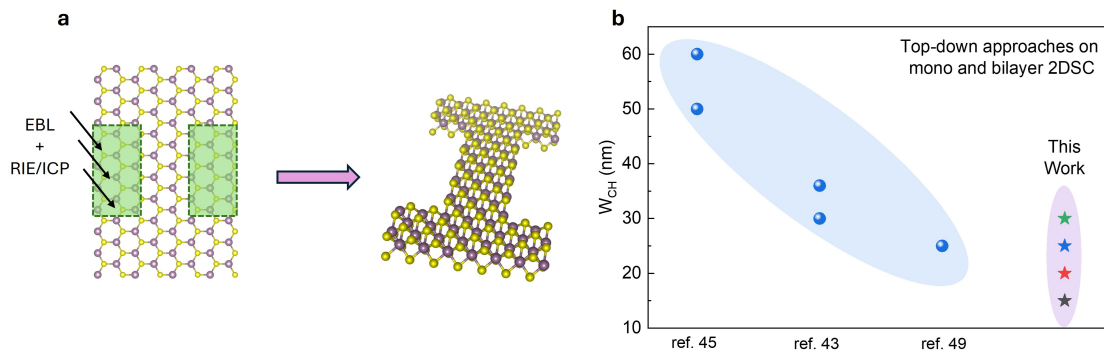


Figure 5.4: Benchmarking of the fabrication of width scaled monolayer and bilayer TMD nanoribbons. (a) Schematic nanoribbon fabrication utilizing EBL and RIE/ICP. (b) Earlier reported widths (blue spheres) versus this work (coloured stars).

5.2 Mono- and Bilayer MoS₂ Nanoribbon Transistors

Monolayer MoS₂ nanoribbon transistors with $W_{CH} \approx 30, 40, \text{ and } 50 \text{ nm}$ and $L_{CH} \approx 50 \text{ nm}$ were fabricated from mechanically exfoliated MoS₂. Figure 5.5 shows a schematic of the monolayer MoS₂ nanoribbon transistor with 20/20 nm Ni/Au contacts and Raman spectra acquired using a green (532 nm) laser excitation. The characteristic peaks of the in-plane (E_{2g}^1) and out-of-plane (A_{1g}) vibrational modes of MoS₂ are present at Raman shifts of approximately 387 cm^{-1} and 405 cm^{-1} , respectively. The separation between the Raman shifts was measured to be $\sim 18 \text{ cm}^{-1}$, and together with the distinct E_{2g}^1 - and A_{1g} -peaks, it was identified to be monolayer MoS₂.

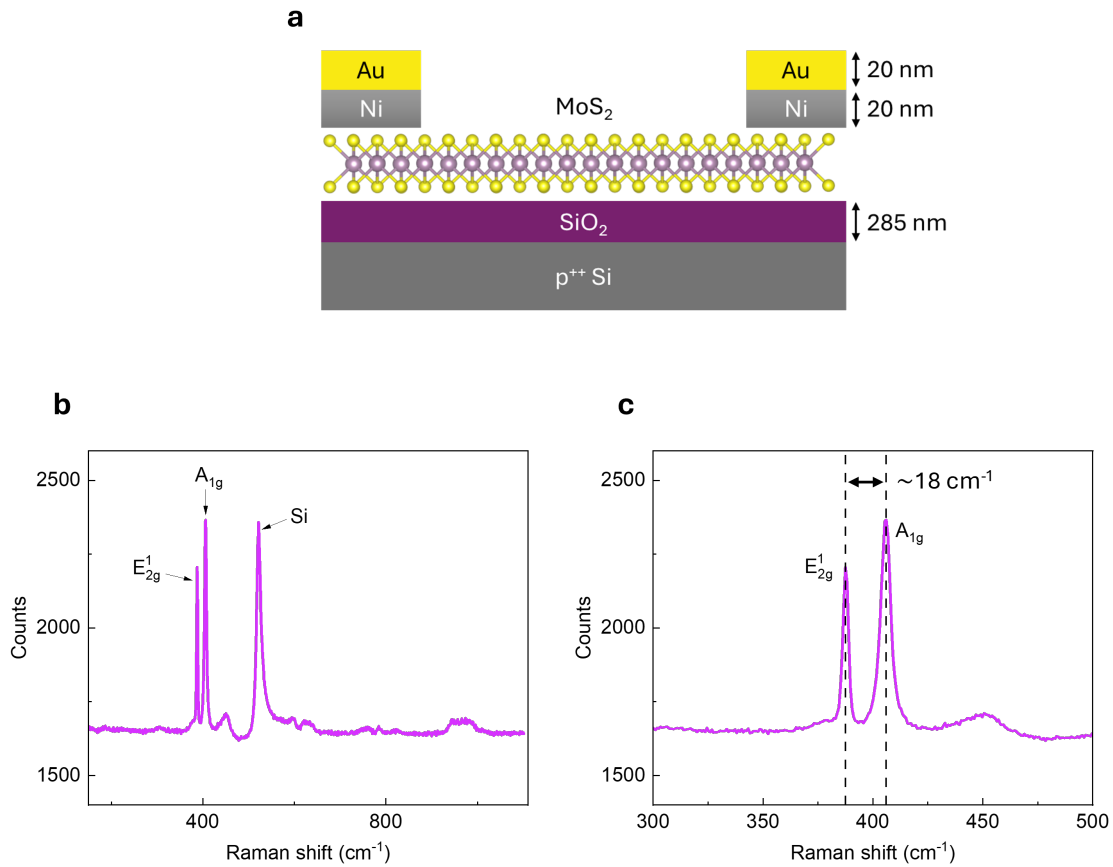


Figure 5.5: Schematic and Raman scattering spectra of the fabricated monolayer MoS₂ FETs. **(a)** Schematic of the monolayer MoS₂ nanoribbon FETs fabricated with 20/20 nm Ni/Au contacts. **(b)** Raman spectrum of monolayer MoS₂ showcasing the peaks of the E_{2g}^1 and A_{1g} vibrational modes, as well as the peak of the vibrational modes of the underlying Si. **(c)** Magnified Raman spectrum confirming monolayer MoS₂, identified by the $\sim 18 \text{ cm}^{-1}$ separation between the Raman shifts.

Electrical transport characteristics of the n-type monolayer MoS₂ nanoribbon FETs with $L_{CH} \approx 50$ nm and $W_{CH} \approx 30, 40,$ and 50 nm are shown in Figure 5.6. The transfer characteristics (I_D versus V_G), as well as the logarithmic transfer characteristics ($\log(I_D)$ versus V_G) at $V_D = 1$ V show, for all channel widths, a clear off-state for large negative biases of the gate voltage. As the gate voltage is increased, subthreshold conduction begins. Increasing V_G further, turn on the transistors and a steep switching from off-state to on-state is observed in the logarithmic transfer characteristics. This can be seen in the transition to the linear non-saturated region in the transfer characteristics as well. At $V_G = 70$ V and $V_D = 1$ V, the devices show a systematic increase of current density from ~ 35 to $110 \mu A/\mu m$ when narrowing the channel width from 50 to 30 nm, respectively. This corresponds to a mean percentage enhancement of 230%. In Figure 5.6c the maximum current density versus the channel width for different V_D biases between 50 mV and 1 V further shows that decreasing W_{CH} enhances the current density for the monolayer MoS₂ nanoribbon transistors. The output characteristics (I_D versus V_D) for the 30 nm and 50 nm wide channels, with an applied sweep of V_D between 0 V and 3 V, show a monotonic increase in current density when V_G is increased from -50 V to 60 V, indicating well-controlled gate-induced electrostatic doping in the channel. The 30 nm wide channel saturates for all V_G , with a shift of the saturation threshold towards higher V_D when V_G is increased. The 50 nm wide channel does not reach the saturation region, as can be seen by the linear behaviour of the output characteristics up until $V_D = 3$ V. Increasing the set biases of V_D from 50 mV to 1 V while sweeping V_G increases the on-state current, as can be seen in the transfer characteristics for the 30 nm wide channel in Figure 5.6f. Although the 30 nm-wide channel achieves higher current densities, it exhibits pronounced variations in the electrical transport, especially at large biases of V_D and V_G .

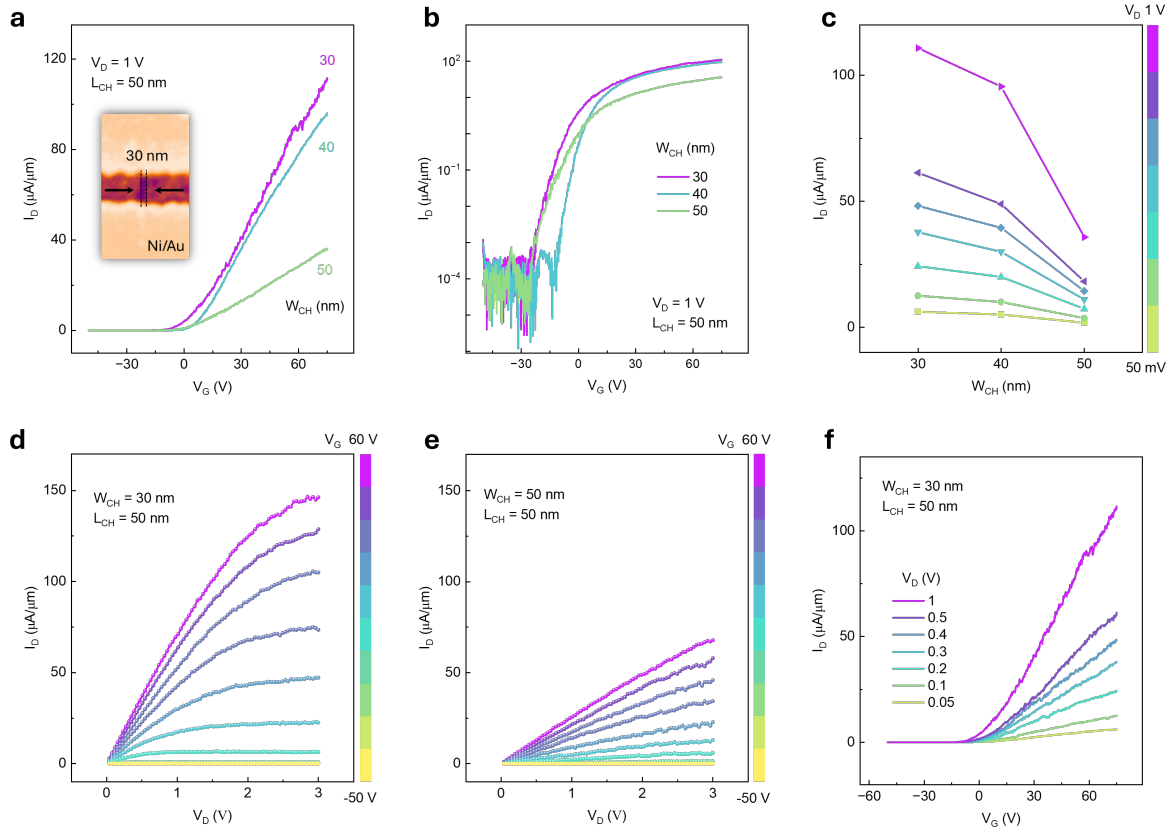


Figure 5.6: Electrical transport characteristics of the monolayer MoS₂ devices with channel widths ranging from 30 nm to 50 nm, and $L_{CH} \approx 50$ nm. **(a)** Transfer characteristics $V_D = 1$ V, showing the drain-source current density versus applied gate voltage from -50 V to 70 V, for the channel widths 30, 40, and 50 nm. The current density of the transistors is increased when decreasing the width of the channel. Inset: false-coloured SEM micrograph of a device with $W_{CH} \approx 30$ nm and Ni/Au contacts. **(b)** Logarithmic transfer characteristics at $V_D = 1$ V, showing the drain-source current density in logarithmic scale versus applied gate voltage, for the channel widths 30, 40, and 50 nm. **(c)** Drain-source current density versus channel width at different V_D ranging from 50 mV to 1 V, for a set $V_G = 70$ V. **(d)** Output characteristics from $V_D = 0$ V to 3 V for $W_{CH} \approx 30$ nm for applied gate voltages ranging from -50 V to 60 V. **(e)** Output characteristics from $V_D = 0$ V to 3 V for $W_{CH} \approx 50$ nm for applied gate voltages ranging from -50 V to 60 V. The scale of the y-axis is the same as that for the output characteristics of the 30 nm wide transistor. **(f)** Transfer characteristics at V_D ranging from 0.05 V to 1 V for the 30 nm channel width.

Bilayer MoS₂ nanoribbon FETs with $W_{CH} \approx 15, 20, 25, 30, 50, 60,$ and 80 nm and $L_{CH} \approx 200$ nm were fabricated from mechanically exfoliated MoS₂. Figure 5.7 shows a schematic of the bilayer MoS₂ nanoribbon transistor with 20/20 nm Ni/Au contacts, an optical image of the fabricated devices, and Raman spectra acquired using a green (532 nm) excitation laser. The characteristic peaks of the in-plane (E_{2g}^1) and out-of-plane (A_{1g}) vibrational modes of MoS₂ are present at Raman shifts of approximately 386 cm^{-1} and 407 cm^{-1} , respectively. The separation between the Raman shifts was measured to be $\sim 21\text{ cm}^{-1}$, and together with the distinct E_{2g}^1 - and A_{1g} -peaks, it was identified to be bilayer MoS₂.

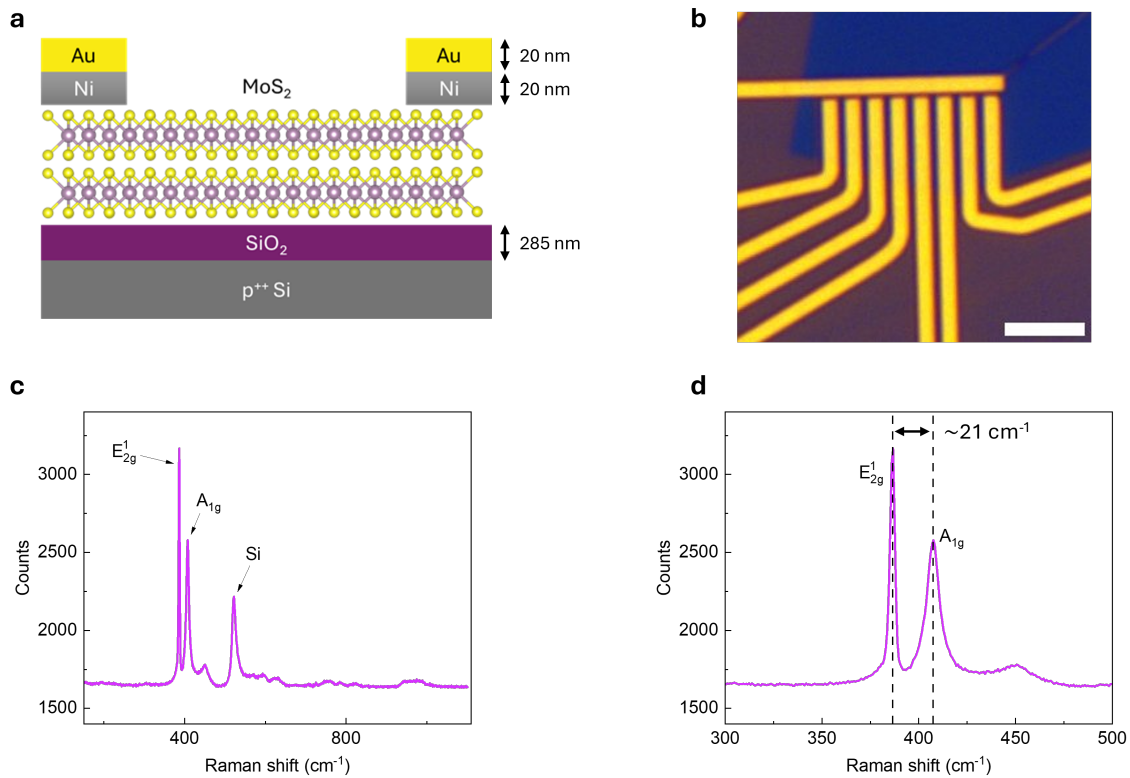


Figure 5.7: Schematic, optical image, and Raman scattering spectra of the fabricated bilayer MoS₂ nanoribbon FETs. (a) Schematic of the bilayer MoS₂ nanoribbon FETs fabricated with 20/20 nm Ni/Au contacts. (b) Optical image of the fabricated bilayer MoS₂ FETs. Scale bar = 5 μm. (c) Raman spectrum of bilayer MoS₂ showcasing the peaks of the E_{2g}^1 and A_{1g} vibrational modes, as well as the peak of the vibrational modes of the underlying Si. (d) Magnified Raman spectrum confirming bilayer MoS₂, identified by the $\sim 21\text{ cm}^{-1}$ separation between the Raman shifts.

Electrical transport characteristics of the fabricated n-type bilayer MoS₂ nanoribbon FETs with $L_{CH} \approx 200$ nm and $W_{CH} \approx 30, 50, 60,$ and 80 nm are shown in Figure 5.8. The transfer characteristics (I_D versus V_G), as well as the logarithmic transfer characteristics ($\log(I_D)$ versus V_G) at $V_D = 2$ V show, for all channel widths, an off-state for large negative biases of the gate voltage. As the gate voltage is increased, subthreshold conduction begins. Increasing V_G further, turn on the transistors and a steep switching from off-state to on-state is observed in the logarithmic transfer characteristics. This can be seen in the transition to the linear non-saturated region in the transfer characteristics as well. For the 30 nm wide channel measured at $V_G = 70$ V, maximum current densities of $\sim 300, \sim 330,$ and $\sim 395 \mu A/\mu m$ are achieved for $V_D = 2, 2.5,$ and 3 V, respectively. At $V_G = 70$ V and $V_D = 2$ V, the devices show a systematic increase of current density from ~ 125 to $300 \mu A/\mu m$ when narrowing the channel width from 80 to 30 nm, respectively. This corresponds to a mean percentage enhancement of 170%. In Figure 5.8c, the maximum current density versus the channel width for different V_D biases between 0.5 V and 3 V further shows the monotonic increase in I_D when decreasing W_{CH} for the bilayer MoS₂ transistors. The output characteristics (I_D versus V_D) for the 30 nm and 80 nm wide channels, with an applied sweep of V_D between 0 V and 3.5 V, show an increase in I_D when V_G is increased from -60 V to 60 V. The 30 nm wide channel exhibits velocity saturation for all V_G , with a positive shift in the saturation threshold. The 80 nm wide channel does not reach the saturation region, as can be seen by the linear behaviour of the output characteristics up until $V_D = 3.5$ V. Increasing the set values of V_D from 50 mV to 1 V while doing a sweep of V_G from -70 V to 70 V increases the on-state current, as can be seen in the transfer characteristics for the transistor with a 30 nm wide channel. Although the 30 nm-wide channel achieves higher current densities, it exhibits pronounced variations in the electrical transport, especially at large biases of V_D and V_G .

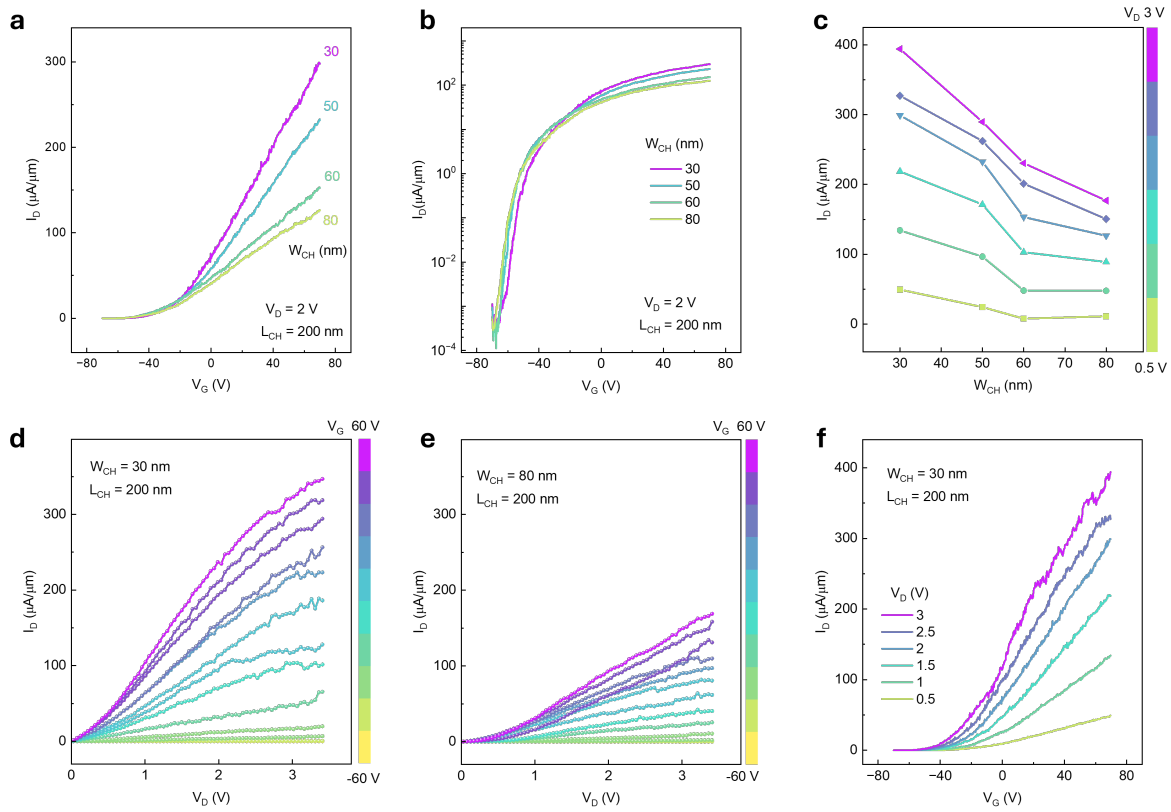


Figure 5.8: Electrical transport characteristics of the bilayer MoS₂ devices with channel widths ranging from 30 nm to 80 nm, and $L_{CH} \approx 200$ nm. **(a)** Transfer characteristics of fabricated transistors at $V_D = 2$ V and an applied gate voltage ranging from -70 V to 70 V for $W_{CH} \approx 30, 50, 60$, and 80 nm. **(b)** Logarithmic transfer characteristics at $V_D = 2$ V, showing the drain-source current density in logarithmic scale versus applied gate voltage, for the channel widths 30, 50, 60, and 80 nm. **(c)** Drain-source current density versus channel width at different V_D ranging from 0.5 V to 3 V. The current density is increased with decreasing channel width for all applied biases of V_D . **(d)** Output characteristics from $V_D = 0$ V to 3.5 V for the device with $W_{CH} \approx 30$ nm with applied gate voltages ranging from -60 V to 60 V. **(e)** Output characteristics from $V_D = 0$ V to 3.5 V for the device with $W_{CH} \approx 80$ nm with applied gate voltages ranging from -60 V to 60 V. The scale of the y-axis is the same as that for the output characteristics of the 30 nm wide transistor. **(f)** Transfer characteristics for the fabricated device with $W_{CH} \approx 30$ nm, with the gate voltage ranging from -70 V to 70 V, and $V_D = 0.5, 1, 1.5, 2, 2.5$, and 3 V.

Table 5.1 shows the approximate maximum on-current densities of the 30 nm channel width bilayer transistor at $V_G = 70$ V for $V_D = 0.5, 1, 1.5, 2, 2.5,$ and 3 V. The maximum on-current densities measured were $50, 135, 220, 300, 330,$ and $395 \mu\text{A}/\mu\text{m}$ for the source-drain voltages $0.5, 1, 1.5, 2, 2.5,$ and 3 V, respectively. Hence, the current density is systematically increased with increasing V_D , eventually hitting the highest measured on-current density in this work of approximately $395 \mu\text{A}/\mu\text{m}$.

Table 5.1: Approximate maximum current densities for the 30 nm channel width transistor at $V_G = 70$ V for $V_D = 0.5, 1, 1.5, 2, 2.5,$ and 3 V.

V_D (V)	0.5	1	1.5	2	2.5	3
I_D ($\mu\text{A}/\mu\text{m}$)	50	135	220	300	330	395

Electrical transport characteristics of the fabricated bilayer MoS_2 nanoribbon FETs with $L_{\text{CH}} \approx 200$ nm and $W_{\text{CH}} \approx 15, 20, 25,$ and 30 nm are shown in Figure 5.9. As can be seen below, successful fabrication of ultra-narrow nanoribbon transistors down to a channel width of ~ 15 nm exhibiting transistor characteristics was achieved. However, the results of the transfer characteristics show that scaling the channel width below 30 nm first decreases and then saturates the current density of the nanoribbon transistors. In Figure 5.9c the current densities are systematically decreased and then saturated at high on-current densities for the channel widths $25, 20,$ and 15 nm for all source-drain bias voltages. The saturation can also be seen in the output characteristics for the 20 nm and 15 nm wide channels, where both exhibit similar behaviour and maximum on-current densities at $V_D = 3.5$ V. In contrast to the 30 nm wide monolayer and bilayer channels, the 20 and 15 nm wide bilayer channels do not exhibit any clear saturation threshold and velocity saturation in the output characteristics. As the channel width is decreased, the transistors also begin to exhibit larger variations in I_D when sweeping both V_G and V_D .

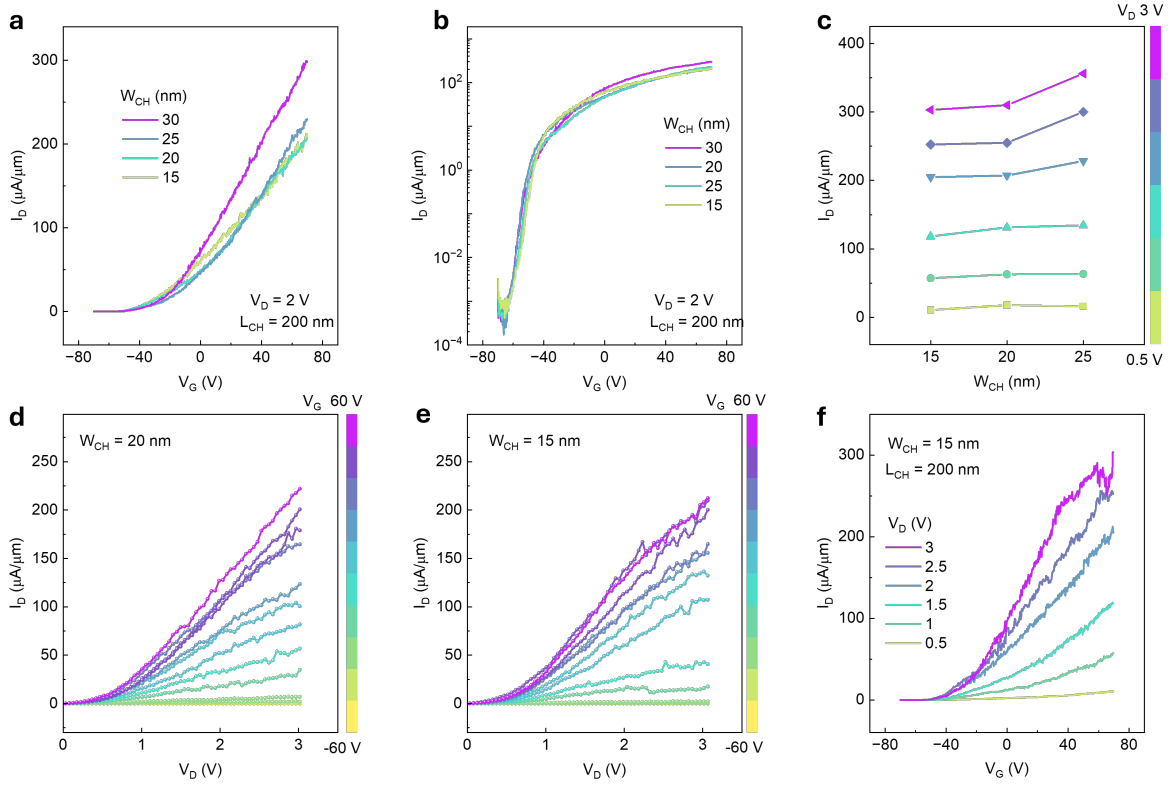


Figure 5.9: Electrical transport characteristics of the bilayer MoS₂ devices with $W_{CH} \approx 15$, 20, 25, and 30 nm, and $L_{CH} \approx 200$ nm. **(a)** Transfer characteristics of fabricated transistors at $V_D = 2$ V and an applied gate voltage ranging from -70 V to 70 V. **(b)** Logarithmic transfer characteristics at $V_D = 2$ V and an applied gate voltage ranging from -70 V to 70 V. **(c)** Drain-source current density versus channel width at different V_D ranging from 0.5 V to 3 V. **(d)** Output characteristics for the 20 nm wide channel with biases $V_D = 0$ V to 3.5 V and $V_G = -60$ V to 60 V. **(e)** Output characteristics for the 15 nm wide channel with biases $V_D = 0$ V to 3.5 V and $V_G = -60$ V to 60 V. **(f)** Transfer characteristics for the 15 nm wide channel at biases $V_D = 0.5, 1, 1.5, 2, 2.5$, and 3 V for $V_G = -70$ V to 70 V.

The field-effect mobility (μ_{FE}) and the threshold voltage (V_{TH}) as a function of W_{CH} for the fabricated mono- and bilayer devices are shown in Figure 5.10. The bilayer devices exhibit higher μ_{FE} than the monolayer devices across all widths, displaying a high carrier mobility of $\sim 32 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the 30 nm wide nanoribbon. The 25, 20, and 15 nm wide channels show a saturation and weak width-dependence of μ_{FE} with respect to W_{CH} . Additionally, the devices with channel widths greater than 25 nm show a decrease in μ_{FE} with increasing W_{CH} . The 30 to 80 nm wide bilayer nanoribbons exhibit a systematic positive shift in V_{TH} with decreasing width. In contrast, monolayer devices show a near-zero and weakly width-dependent V_{TH} , while the 15 to 25 nm wide bilayer nanoribbons show a slight negative shift with decreasing width.

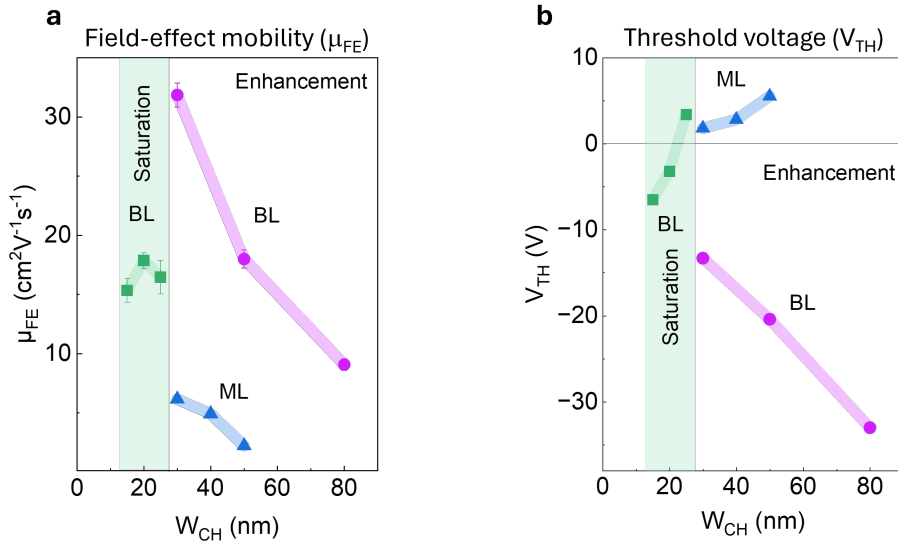


Figure 5.10: Width-dependent transport parameters of monolayer (ML) and bilayer (BL) MoS₂ nanoribbon FETs. (a) Field-effect mobility (μ_{FE}) as a function of W_{CH} for monolayer (blue), bilayer in the enhancement regime (magenta), and bilayer in the saturation regime (green) MoS₂ nanoribbon FETs. (c) Threshold voltage (V_{TH}) as a function of W_{CH} for monolayer (blue), bilayer in the enhancement regime (magenta), and bilayer in the saturation regime (green) nanoribbon FETs.

Figure 5.11 shows the benchmarking of maximum on-current density (I_D), as well as on/off ratios, as a function of W_{CH} for monolayer (ML) and bilayer (BL) MoS₂ nanoribbon FETs from this work (blue and magenta stars, respectively) against literature reports of MoS₂ and WS₂ nanoribbon devices with varying thicknesses (ML, BL, 6 nm, 8 nm, 20 nm, and 35 nm). The results from this work show high-performance mono- and bilayer MoS₂ FETs with enhancement in the on-current density when scaling the width, reaching higher on-current densities than previously reported. This work also reports a high current density-saturation when scaling the widths below 30 nm for bilayer MoS₂ nanoribbons. The fabricated devices exhibit high on/off ratios at 6 orders of magnitude ($\sim 10^6$), showcasing the highest on/off ratios reported for mono- and bilayer MoS₂ nanoribbon transistors. As can be seen in Figure 5.11a, the thicker 2D semiconductor nanoribbons show no enhancement, but rather reduction, in on-current density when scaling the width.

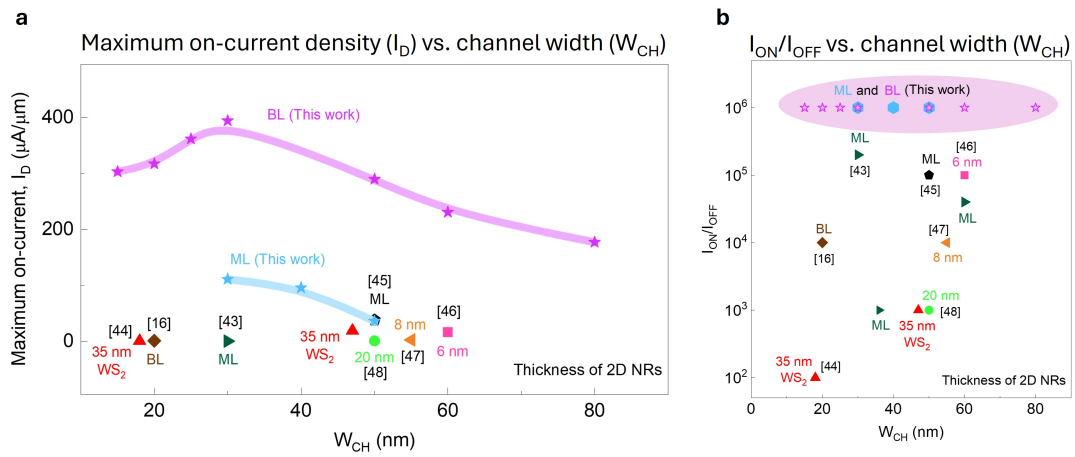


Figure 5.11: Benchmarking of maximum on-current density (I_D), as well as on/off ratios, as a function of W_{CH} for state-of-the-art MoS₂ and WS₂ nanoribbon (NR) FETs. **(a)** Maximum on-current density (I_D) as a function of W_{CH} . The benchmarking depicts the monolayer (ML) and bilayer (BL) MoS₂ nanoribbon FETs from this work (blue and magenta stars, respectively) against literature reports of MoS₂ and WS₂ nanoribbon devices with varying thicknesses (ML, BL, 6 nm, 8 nm, 20 nm, 35 nm; coloured symbols). **(b)** On/off ratios (I_{ON}/I_{OFF} , as a function of W_{CH} . The benchmarking depicts the monolayer (ML) and bilayer (BL) MoS₂ nanoribbon FETs from this work (blue hexagons and magenta stars, respectively) against literature reports of MoS₂ and WS₂ nanoribbon devices with varying thicknesses (ML, BL, 6 nm, 8 nm, 20 nm, 35 nm; coloured symbols).

6

Discussion

The high-resolution nanofabrication of MoS₂ nanoribbons and width-scaled transistors, as well as the electrical transport properties, are discussed in this chapter. Additionally, future studies are mentioned, both as a solution to the limitations of this work as well as suggestions to other technologies where the ultra-narrow nanoribbons and devices can be utilized.

6.1 High-resolution Nanofabrication

One of the most critical factors in achieving high-performance transistors is the nanofabrication process, where every step matters. As devices are scaled down to the atomic level, the risk of fabrication failure increases significantly, making it extremely challenging to develop reliable processes for ultra-scaled 2D semiconductor nanoribbons. The high-resolution nanoribbon fabrication recipe in this work was developed with a lot of literature research, as well as trial and error. One of the reasons for the successful fabrication is in the first step, the coating of the e-beam resist. First and foremost, the substrate needs to be clean to not damage the two-dimensional materials, keep dirt and dust from interfering with the final devices, and to avoid failure in the coating procedure. An uneven and dirty surface will result in an uneven coating of the resist, gravely affecting the rest of the processes. In the spin-coating process there are four key parameters of utter importance when developing a high-resolution recipe. They are choice of resist, rotational speed, soft baking temperature, and soft baking time. As described in the experimental methods of this work (see Section 4.1 or Appendix A), AR-P 6200.13 1:2 dilution in anisole was chosen as the resist, and spin-coated at 6000 rpm. This positive, high-resolution, and very etch resistant resist, when spin-coated at 6000 rpm, will produce a very thin layer on top of the substrate. When pushing the limits of resolution, a minimum aspect ratio of one between the resist height and the desired feature size is preferred. As shown in Figure 5.1, the resist was

measured with AFM to a thickness of approximately 55 nm and as mentioned in Section 5.1, this resulted in aspect ratios of ~ 0.27 and ~ 3.67 for the 15 nm and 200 nm wide nanoribbons, respectively. Although the aspect ratios are smaller than one for the nanoribbon widths below 55 nm, successful fabrication was achieved. The reason a thin resist is so important is because of the electron scattering during the EBL, see Figure B.1. As the primary electrons hit and interact with the resist, they immediately begin to scatter. A thicker resist results in more electron scattering in the resist, and therefore a higher risk of broadening the exposed areas compared to design, see Figure B.1 in Appendix B. Subsequently, the resolution of the fabrication will be worse. The extremely thin resist used in this work was therefore an active choice to limit electron scattering and broadening of the designs. Previous studies have also shown that soft baking time and temperature affects the resolution. Changing the temperature and time of the soft baking changes the rate of solvent evaporation and the amount of evaporated solvent, and can directly affect the properties of the polymers in the resist. Hence, different times and temperatures will affect the EBL exposure of the resist, which in turn affects the development. All of these matter when going down the road of high-resolution nanofabrication.

The EBL parameters were optimized with respect to the resist and its thickness, as well as the development time. The acceleration voltage of the Raith EBPG 5200 is set at 100 kV and is not a tunable parameter. However, the other parameters were varied and tested according to literature research. A low beam current of 500 pA and a beam step size of 2 nm was chosen to avoid broadening and produce super-straight edges during the exposure. The EBL dose was optimized to $240 \mu\text{C}/\text{cm}^2$, and it was found during the optimization that both lower and higher doses were insufficient in producing correct widths. The dose will define how long the e-beam stays in one spot before moving on to the next, and will therefore directly affect the amount of charge per unit area the resist is exposed with. Too high will enhance the electron scattering and too low will under-expose the resist. An under-exposed resist will result in wrongly developed patterns compared to design and leave resist residues affecting the other fabrication steps, as well as the device performance. After the exposure, the development time was optimized to 90 seconds in n-amyl acetate for the 55 nm thick resist exposed with the 500 pA beam current and $240 \mu\text{C}/\text{cm}^2$ dose. The 90 second development time was confirmed with SEM to produce the narrowest and most accurate widths according to design, see Figure 5.2 and 5.3.

The gentle etching recipe used in this work is one more reason for the high-resolution fabrication of the mono- and bilayer MoS₂ nanoribbons. To keep the resist from being etched laterally, and therefore broadening the designs, Ar was chosen at a comparable gas flow as CHF₃. Adsorbed Ar atoms on the resist walls will keep the resist from being etched laterally by CHF₃, see Figure B.1, while the Ar ions provide an anisotropic physical etching aligned with the electric field. This keeps the nanoribbons accurate according to design and results in the super-straight edges and vertical etching profiles achieved in this work, see Figure 5.1, 5.2, and 5.3. Moreover, including ICP in the process also helps produce the vertical and accurate etching profiles. Decreasing the forward power and instead increasing the ICP will lower the energy of the ion bombardment on the surface and at the same time induce a higher density of the ions in the plasma. This choice of etching recipe is one of the most crucial steps in the fabrication for producing narrow and accurate nanoribbons with high resolution.

Even though this work has shown a successful lithographic top-down approach of nanoribbons, bottom-up approaches still yield narrower widths. This, combined with the often controlled fabrication of certain edge structures might indicate that bottom-up approaches are superior. However, top-down approaches are favourable when fabricating electrical devices such as transistors. Bottom-up approaches often yield random distributions of nanoribbons with non-controllable widths and occasionally nanoribbons with width-gradients, two disadvantages when fabricating devices. Additionally, the substrates are often not compatible with device fabrication. Hence, compared to the more complex bottom-up approaches, top-down approaches are more versatile, scalable, and especially controllable regarding the nanoribbon widths.

To further scale 2D semiconductor nanoribbon devices an optimized high-resolution nanofabrication of the contacts is crucial. However, nanofabrication processing of thin materials with atomic thicknesses is extremely challenging. Especially for materials like TMDs with weak inter-layer vdW-interactions, increasing the risk of folding, delamination and breakage. When decreasing the widths of the MoS₂ sheets towards the sub-50 nm nanoribbon regime one has to be cautious when handling the chips. Processes such as the lift-off has to be conducted with extreme care, limiting agitation, heating, and vibrations. Development of a high-resolution contact nanofabrication process was attempted in this work, but with no success. A recipe for

a bilayer PMMA 495k A4/PMMA 950k A2 stack was developed and resulted in super-clean, straight and high-quality contacts, with a high-resolution gap of 30 nm. Unfortunately, lift-off issues were encountered, likely due to insufficient undercut and changes in the PMMA properties induced by the high-energy deposition of the metal films. Lift-off was possible under extreme agitation with a pipette, heated acetone, or sonication. Though successful, these methods are unsuitable, as they tend to induce breaking, folding, or delamination of weakly interacting 2D semiconductor materials. This issue is particularly pronounced for nanoribbons, which, due to their reduced interaction area with the substrate, exhibit even weaker van der Waals adhesion.

As is often the case in nanofabrication, process recipes can be continually refined, even after reaching optimal conditions. In this sense, the development is effectively ongoing, and the 2D semiconductor nanoribbon process developed in this work likely still allows for further optimization. However, if we for a moment believe that it is the best one it can be, there are still some aspects to improve. As discussed, the first step would be to develop a high-resolution contact recipe to decrease the channel length of the devices and improve the quality of the contacts. It would then be beneficial to anneal the chips in high vacuum after each fabrication step to ensure that there are no resist residues left on the surface. The annealing will also improve the semiconductor-metal interface, avoiding resistive contacts.

6.2 Effects of Width Scaling in Mono- and Bilayer MoS₂ Nanoribbon Transistors

Interestingly, this work presents a new type of enhancement regime when scaling the widths of mono- and bilayer MoS₂ transistors, see Figure 5.6 and 5.8. In thicker stacks of 2D semiconductors, the current density is, as expected, saturated or decreased when narrowing the width, consistent with the geometric aspects of the resistance. As the width is decreased the aspect ratio between the edges and the body is increased, enhancing the role of edge effects in the semiconductor channel. Due to the enhanced edge scattering effects and confinement of the charge carriers, thicker stacks of the 2D semiconductor nanoribbons experience decreased on-state currents, reduced current density and lower saturation currents. However, for thinner mono- and bilayer nanoribbons we see an enhancement of the on-state current density for ap-

plied biases when scaling the width. Hence, an increase in the charge carrier density at the same electric field bias is observed, consistent with enhanced gate-induced electrostatic doping and fringing field effects at the ribbon edges. These different charge carrier transport effects depending on thickness and width suggests there is a point in scaling the thickness and width of the 2D semiconductors where a transition occurs from dominating edge scattering to fringing field effects and enhanced gate-channel coupling dominating. This, in turn, enhances the gate-induced electrostatic doping and the current density in the 2D semiconductor nanoribbon channel is increased compared to wider channels. In addition, enhanced mobility and threshold-voltage stability in Figure 5.10 suggest reduced edge scattering and depletion resulting from improved electrostatic control. The bilayer nanoribbons exhibit a systematic positive shift in V_{TH} with decreasing width, consistent with enhanced gate-control and fringing field effects at the ribbon edges. In contrast, monolayer devices show a near-zero and weakly width-dependent V_{TH} , reflecting balanced electrostatic control without significant charge accumulation at the edges. Important to note is that the rather thick gate dielectric (285 nm SiO_2) might result in uncertainties when extracting parameters such as V_{TH} .

There are both similarities and differences in the output characteristics of the monolayer MoS_2 nanoribbon transistors in Figure 5.6d and 5.6e, and the bilayer MoS_2 nanoribbon transistors in Figure 5.8d and 5.8e. The enhancement in current density is seen in both cases when narrowing the width down to 30 nm, consistent with the transfer characteristics in both cases. The 30 nm wide channel in the mono- and bilayer transistors reach the saturation region and a high saturation current, indicating strong gate control over the entire nanoribbon. This is not the case for the 50 nm wide monolayer transistor and the 80 nm wide bilayer transistor under the same biases, where the larger widths barely reach the saturation region with much lower saturation currents. The positive shift of the saturation threshold with increased gate bias is consistent with both experimental and theoretical results for MOSFETs, and indicates a strong gate control over the nanoribbon channel. The bilayer 30 nm wide channel also outputs approximately twice the current density of the monolayer 30 nm wide channel. Despite the enhanced field-effect of the monolayer 50 nm channel, the bilayer 80 nm channel outputs a higher current density. This is not very surprising as increasing the number of layers enables more charge carriers to flow through the semiconductor channel.

The decrease and high-current saturation of the 25, 20, and 15 nm wide bilayer nanoribbons can be seen in the similar maximum on-currents as well as behaviour in the transfer and output characteristics in Figure 5.9. Additionally, this can be observed in the saturation of the field-effect mobility in Figure 5.10. This compared to clear increase of current density as the channel width is decreased from 80 to 30 nm suggests a transition from an enhancement regime to a saturation regime. Quite reasonable as it is not realistic for the current to approach infinity. This could possibly be due to the increased aspect ratio of the edges versus body, effectively increasing how the edges affects the total transport characteristics. Due to the more prominent metallic edge effects, it is harder to control charge carrier density in the channel with the electric field. Hence, the gate-induced electrostatic control over the channel is reduced and the transport mechanisms are not controlled in the same way as for wider nanoribbons. Additionally, the lack of velocity saturation of the charge carriers as well as negative shift in threshold voltage indicates prominent metallic edges and no edge-enhanced scattering in the channels.

This work has not only successfully fabricated MoS₂ nanoribbons of ultra-scaled size with accurate widths, but also shown physical phenomena/effects useful for future applications. The geometric and equivalent scaling of Si-based transistor technologies have come to a stop, with the electrostatic control beginning to break down. Since the first fabricated monolayer MoS₂ transistor, research in the area exploded, showing off the apparent advantages of 2D semiconductors. However, the scaling of the width has not been as heavily researched, with few works showing high-performance ultra-narrow nanoribbon transistors with 2D semiconductors. This work shows that it is not only possible to scale mono- and bilayer down to widths of 15 nm, but also that it is possible to fabricate extremely efficient and high-performance transistors with 2D semiconductor nanoribbons. The scaling of transistor technologies provide higher efficiency and device density. This, in turn, provides larger computational capabilities and faster computers.

The most important result of this work is that as the width of the nanoribbons are scaled from 80 nm to 30 nm for the bilayer MoS₂ and from 50 nm to 30 nm for the monolayer MoS₂, the current density is increased. This is a very interesting physics phenomenon, and very convenient for high-performance and energy efficient transistor technologies. As the transistors are scaled, allowing for higher device densities, one can at the same time achieve transistors that are more energy efficient and produce higher current densities. With these results, this work has shown a new type of width scaling rule for mono- and bilayer 2D semiconductors, see Figure B.2, unconventional in contrast to the scaling laws for Si.

6.3 Future

To improve statistical confidence and ensure more robust conclusions, additional devices should be fabricated and included in the analysis. As this work was limited to n-type monolayer and bilayer MoS₂, future studies should be conducted with both exfoliated and CVD-grown TMDs, such as MoS₂, WS₂, MoSe₂, and WSe₂. Devices with a range of nanoribbon widths and lengths should be fabricated and thoroughly studied. Moreover, a single- or dual-gate structure incorporated with a high- κ dielectric such as HfO₂ should be fabricated. This should be done for further scaling, better electrical transport and gate-control, and to extract SS as well as more accurate values of V_{TH} . SS was not extracted in this work due to the thick 285 nm SiO₂ resulting in undesired switching characteristics. Further measurements and evaluations of the semiconductor-metal interface is also needed. Measurements on varying channel lengths should be conducted to extract the contact resistance via the transfer length method. Temperature-dependent measurements should be done to study the electrical transport properties and to evaluate the semiconductor-metal interface by extracting the effective SBH by linear fit of the Arrhenius curves. Hence, these methods can also be used to analyse if the total contact resistance plays a role in the enhancement and saturation of the devices. Contact engineering should be conducted with metals such as Ag, Bi, Sb, and Ti to determine the best contact materials for high-performance nanoribbon transistors. To improve the performance, the devices should be annealed in high vacuum to remove resist residuals and improve the semiconductor-metal interface.

In this work, dry etching was chosen to fabricate the nanoribbons instead of wet chemical etching, since wet chemical etching is not feasible for mono- and bilayer TMDs. Therefore, we can not control whether the edges are in a zigzag configuration, with either Mo-termination or S-termination, or an armchair configuration. Lateral anisotropic etching and control over the edge termination and structure is only feasible with wet chemical etching. The edge structure will directly impact the electrical performance of the nanoribbons, something that is not taken into consideration in this work. Studies of the edges should be conducted to better understand their role in the electrical transport when reducing the width. For example, transmission electron microscopy (TEM), scanning tunneling microscopy (STM), Kelvin probe force microscopy (KPFM), and PL spectra. An evaluation of the edge-passivation should be conducted as well, to establish if edge-passivation at this scale can enhance the performance further. Finally, for a complete understanding of the physical phenomena, theoretical studies such as density functional theory (DFT) calculations should be performed.

This work has presented the incredible possibilities and applications of 2D semiconductor nanoribbon transistors in ultra-scaled, high-performance, and high-density computational architectures. However, further considerations remain. More complex architectures, e.g., 2D semiconductor nanoribbon GAA structures would enable an ultra-scaled 3D integration of high-performance nanoribbon transistors, with possibilities of scaling the gate and channel even further. The results of this work also innovates further progressive development for ultra-scaled and high-performance pn-junctions, CFET technologies, logic gates, parallel computing, and optoelectronics. The integration of graphene as the gate conductor can also facilitate further developments in scalable fuzzy logic hardware. Future studies of the nanoribbon electrical transport properties should be done to evaluate the possibilities of incorporating memtransistive and memristive behaviour. Ultra-scaled 2D semiconductor nanoribbons can then be used for high-density, energy efficient, and fast three-terminal modulated artificial neurons for neuro-morphic computing and in-memory computing applications.

7

Conclusion

The findings in this work establish a new ultra-narrow width-scaling principle for 2D semiconductors down to 15 nm with improved performance that is distinct from conventional semiconductors physics as well as an optimized nanofabrication approach to realize high-resolution fabrication of ultra-narrow atomically thin nanoribbons. By reducing the channel width of monolayer and bilayer MoS₂ nanoribbon transistors from 80 to 15 nm, an enhancement in on-current density and saturation at narrower transistors is observed. This directly reverses the degradation trend reported earlier in silicon and 2D semiconductors at comparable dimensions. The improvements in field-effect mobility and threshold-voltage stability reveal an edge-enhanced transport regime and suppressed edge depletion, reflecting an intrinsic electrostatic advantage of atomically thin nanoribbon channels. From a technological perspective, the enhancement in on-current density with narrower channels provide a path towards energy efficient and high-density logic. Combined with the demonstrated compatibility of the top-down lithographic approach, these findings provide an experimental foundation for channel width scaling for hyper-scaled electronics with two-dimensional semiconductor nanoribbons. Further experimental and theoretical studies of the nanoribbon edges are of particular interest to unravel the origin of the physics in ultra-narrow 2D semiconductor nanoribbon transistors.

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A

Fabrication Process with Detailed Recipes

Preparation of mono- and bilayer MoS₂

Cleaning of the bare substrates were done according to the description below.

1. Submerge in acetone at 50 °C for 10 minutes.
2. Submerge in room-temperature acetone for 5 minutes.
3. Submerge in room-temperature IPA for 5 minutes.
4. Blow dry with N₂ gas.
5. Perform an O₂–plasma stripping with a gas flow of 10 sccm, forward power of 50 W, and pressure of 250 mTorr for 20 seconds.

Exfoliation of MoS₂ was performed according to the description below.

1. Prepare three to four rectangular pieces of Nitto tape.
2. Use the Nitto tape to first exfoliate from the bulk crystal. Fold the tape against itself and exfoliate to get a larger area of thinner flakes. Use another piece of tape and press it against the first piece to exfoliate once more. Either continue the exfoliation by folding the tape in on itself or use the remaining pieces to exfoliate further. Stop when desired density and thickness of the flakes has been achieved.
3. Cut a square piece of PDMS tape of equal size as the substrate and peel off the thin protective plastic layer. With tweezers, apply the square PDMS tape to an area of interest on the Nitto tape with thin MoS₂. Gently rub the top of the PDMS square with a circular motion with the backside of the tweezers for 30 seconds.
4. Peel off the PDMS with the tweezers and apply it to the substrate. Gently rub the top of the PDMS in a circular motion for 30 seconds. With tweezers, carefully peel off the

PDMS. Check for thin flakes in an optical microscope. If desired thickness or density of flakes is not achieved, return to step three.

5. Immerse in room-temperature acetone overnight to remove PDMS residues on the surface. This will minimize the risk of spin-coating failure because of the PDMS residues. Submerge in IPA for 5 minutes after the overnight acetone cleaning and very gently blow dry with N_2 gas.

AutoCAD design process

Before designing the devices, images were taken of preferred areas with mono- or bilayer MoS_2 and WS_2 . When images of mono- and bilayer MoS_2 and WS_2 had been taken using an optical microscope, designs of the devices were done in AutoCAD 2026. Figure A.1 shows the workflow of the design process in AutoCAD, beginning with alignment of the images on the correct coordinates. The nanoribbon etch layer was then designed with nanoribbon widths mostly ranging from 15 nm to 200 nm, but could in some cases vary up to 10 μm , and were on purpose designed in the shape of a dog bone to mitigate delamination and folding, and ensure stability of the nanoribbons during the processing. The etching designs were extended until they hit the SiO_2 to ensure no parallel connections between the devices. Around the selected flakes another etching layer was designed, with the purpose to etch away unwanted dirt and thicker parts of MoS_2 . This was done to avoid lift-off failure, ensure proper adhesion of the contacts to the substrate and avoid unwanted connections between the contacts. The high-resolution feature contacts were then designed on top of the nanoribbon designs with channel lengths ranging from 50 nm to 200 nm, and up to 500 nm for contact resistance measurements. They were then connected to the final layer, the low-resolution feature contact layer. This layer was designed with circular contact pads and were assigned markers in the form of numbers and letters to locate and bond the devices.

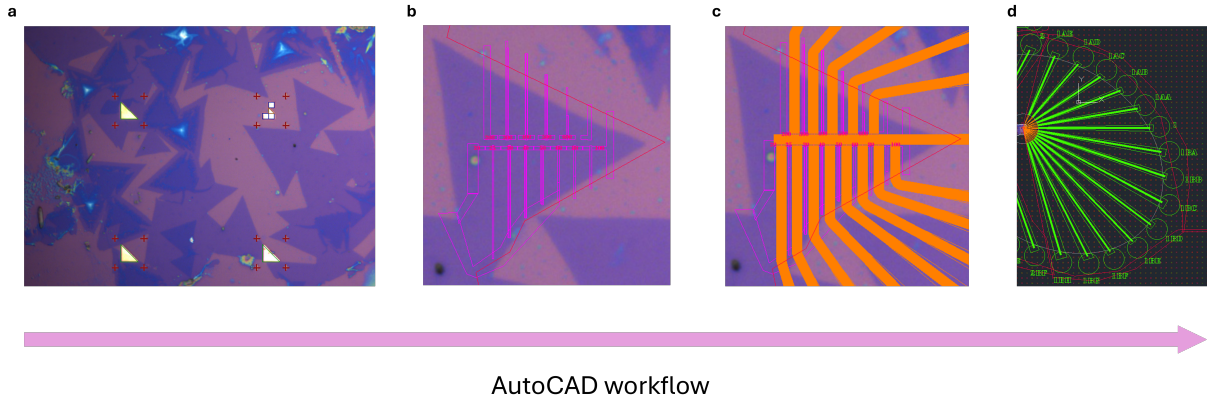


Figure A.1: Representative AutoCAD workflow for the design of ultra-narrow MoS₂ mono- and bilayer transistors. Acquired images of the samples were (a) aligned on the correct coordinates in the AutoCAD template, followed by (b) design of the nanoribbon etching layer, often ranging in widths between 15 nm and 200 nm. On top of the nanoribbons, (c) the high-resolution feature contacts were designed where channel lengths were usually varied between 50 nm and 200 nm. Finally, (d) the low-resolution feature contacts were designed with contact pads and contact markers (numbers and letters) to easily locate and bond the devices.

Nanoribbon fabrication

For the 2D semiconductor nanoribbon fabrication, the e-beam resist AR-P 6200.13 1:2 dilution in anisole was spin-coated with a Suss LabSpin6 spinner using the recipe below. The total acquired thickness of the resist was measured with AFM to be approximately 55 nm.

1. Spin-coat AR-P 6200.13 1:2 at an acceleration of 1500 rpm/s² and a rotational speed of 6000 rpm for 60 seconds.
2. Soft bake on a hot plate at 150 °C for 60 seconds.

The nanoribbons were then defined with EBL by patterning the etching layer of the AutoCAD design on the positive e-beam resist with the Raith EBPG 5200. The EBL was carried out with proximity error correction. Upon exposure, the polymers in the exposed area will undergo chain scission and become more soluble during the development. The optimized parameters used for the EBL exposure of the nanoribbon designs in this work are presented in Table A.1. These include the voltage, beam current, aperture, beam step size (BSS), and dose.

Table A.1: Parameters for the EBL exposure of nanoribbon designs using the Raith EBPG 5200.

Voltage	Beam current	Aperture	BSS	Dose
100 kV	500 pA	300 μm	2 nm	240 $\mu\text{C}/\text{cm}^2$

Development of the exposed areas was carried out by submerging the chip in room-temperature n-amyl acetate for 90 seconds. This was followed by immersion in IPA for 30 seconds and very gently blow drying with N_2 gas. The IPA will stop the development and support the resist walls from collapsing/folding, ensuring successful high-resolution fabrication.

When the development was complete, the dissolved areas were evaluated using an optical microscope. When complete development of all areas had been confirmed, the etching step began. The etching recipe was designed to create a gentle etching of the monolayers with straight edges and minimal over-etching into the SiO_2 . The etching was performed with an Oxford Plasmalab 100 ICP/RIE and the parameters are presented in Table A.2. This yielded an etching rate of approximately 0.9 nm/s. Hence, etching for 5 seconds resulted in 4 – 5 nm deep etching, enough to etch both mono- and bilayers while avoiding substantial over-etching into the SiO_2 substrate.

Table A.2: Parameters for the etching of mono- and bilayer MoS_2 and WS_2 using the Oxford Plasmalab 100 ICP/RIE.

CHF_3	Ar	Forward power	ICP	Pressure	Time
50 sccm	40 sccm	25 W	200 W	10 mTorr	5 s

During the etching process, the top of AR-P 6200.13 1:2 may get hardened, which results in an issue of removing the left-over resist. Therefore, an O_2 -plasma stripping was carried out with a PlasmaTherm RIE to etch the top layer for complete dissolution and to avoid resist residues. The parameters for the oxygen stripping are presented in Table A.3 below.

Table A.3: Parameters for the O_2 -plasma stripping using the PlasmaTherm RIE.

O_2	Forward power	Pressure	Time
10 sccm	50 W	250 mTorr	10 s

After the O₂-plasma stripping the chip was immersed in room-temperature acetone for 24 hours to dissolve the remaining resist. It was then submerged in IPA for 5 minutes and very gently blow dried with N₂ gas. The results of the nanoribbon fabrication were evaluated using an optical microscope. Characterization of the nanoribbons was carried out with AFM and SEM.

Fabrication of source and drain contacts

The bilayer resist stack for contact fabrication was spin-coated using a Suss LabSpin6 spinner according to the recipe below.

1. Spin-coat P(MMA 8.5 MMA) EL8 at an acceleration of 3000 rpm/s² and a rotational speed of 6000 rpm for 60 seconds.
2. Soft bake on a hot plate at 130 °C for 10 minutes.
3. Spin-coat AR-P 6200.13 1:2 at an acceleration of 3000 rpm/s² and a rotational speed of 6000 rpm for 60 seconds.
4. Soft bake on a hot plate at 130 °C for 10 minutes.

The contact designs were defined with EBL, which was carried out with proximity error correction. The exposure of the contacts was divided into two parts, one for high-resolution features and one for low-resolution features. The detailed parameters are presented in Table A.4 below.

Table A.4: Parameters for the EBL exposure of contact designs using the Raith EBPG 5200.

Parameter	Voltage	Beam current	Aperture	BSS	Dose
High-resolution	100 kV	5 nA	300 μm	5 nm	260 μC/cm ²
Low-resolution	100 kV	100 nA	300 μm	30 nm	260 μC/cm ²

Development of the exposed areas was performed by submerging the chips in room-temperature n-amyl acetate for 50 seconds followed by room-temperature MIBK:IPA 1:1 for 1 minute and 10 seconds, and then gently blow drying with N₂ gas. Complete development was checked with an optical microscope.

A. Fabrication Process with Detailed Recipes

Source and drain top contacts were deposited with EBPVD at high vacuum ($\sim 5 \cdot 10^{-7}$ Torr), depositing 20/20 nm Ni/Au. After metal deposition, the edges of the chips were scratched to improve the lift-off process. The chips were then immersed in room-temperature acetone for 30 minutes, with gentle agitation by pipetting to remove the redundant metal. The chips were then submerged in room-temperature IPA for 5 minutes to clean them from any metal and solvent residues. Finally, they were gently blow dried with N₂ gas.

B

Supplementary Results

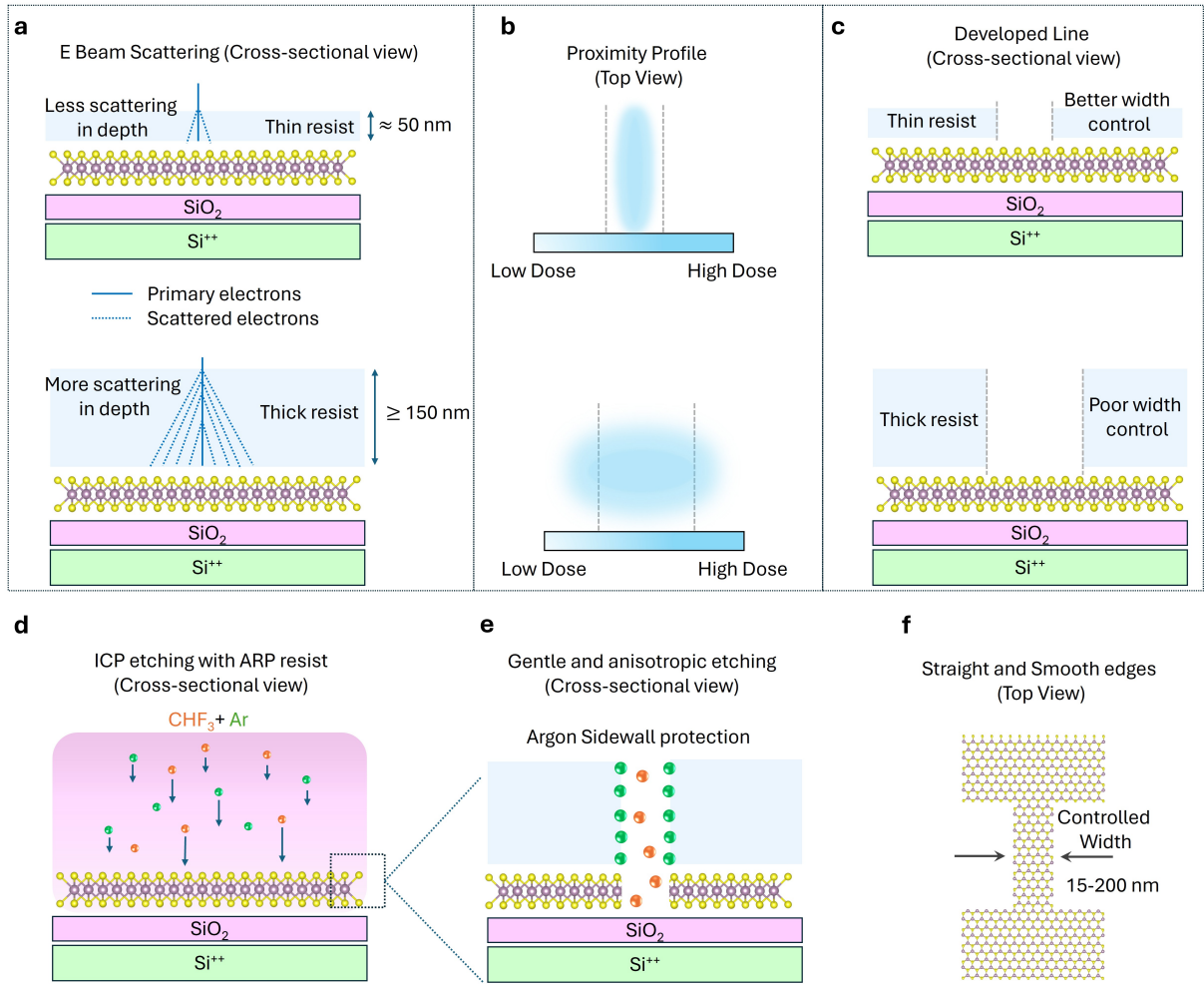


Figure B.1: Schematics explaining the optimized nanoribbon fabrication process. **(a)** Scattering effects depending on the e-beam resist thickness. **(b)** Proximity profile of the primary e-beam depending on the resist thickness. **(c)** Developed line in the e-beam resist depending on scattering effects in different thicknesses of the resist. **(d), (e)** Cross-sectional view of the gentle and anisotropic etching by Ar-adsorption on the resist walls. **(f)** An etched nanoribbon with a controlled width.

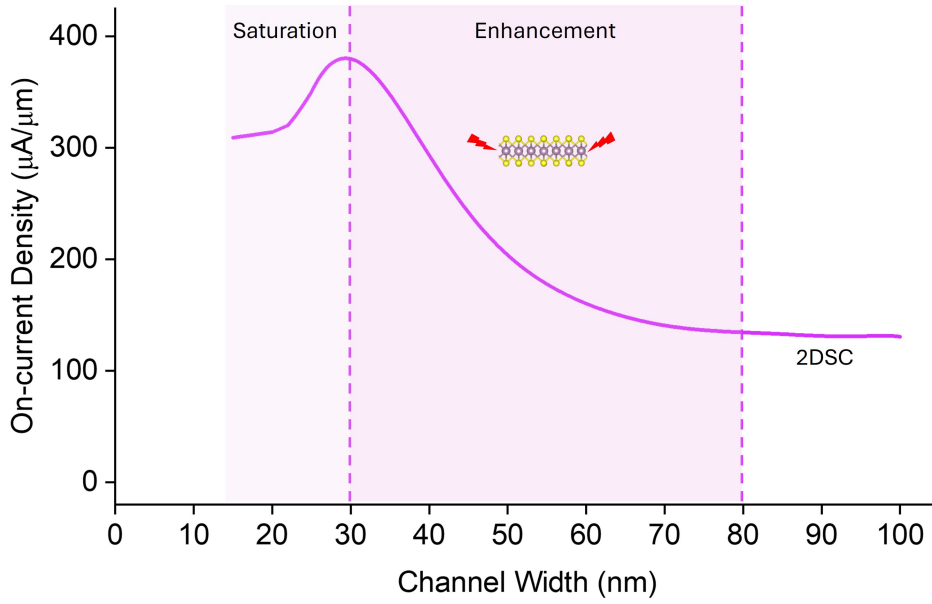


Figure B.2: Schematic showcasing the dynamics of scaling the width of 2D semiconductor nanoribbon transistors.

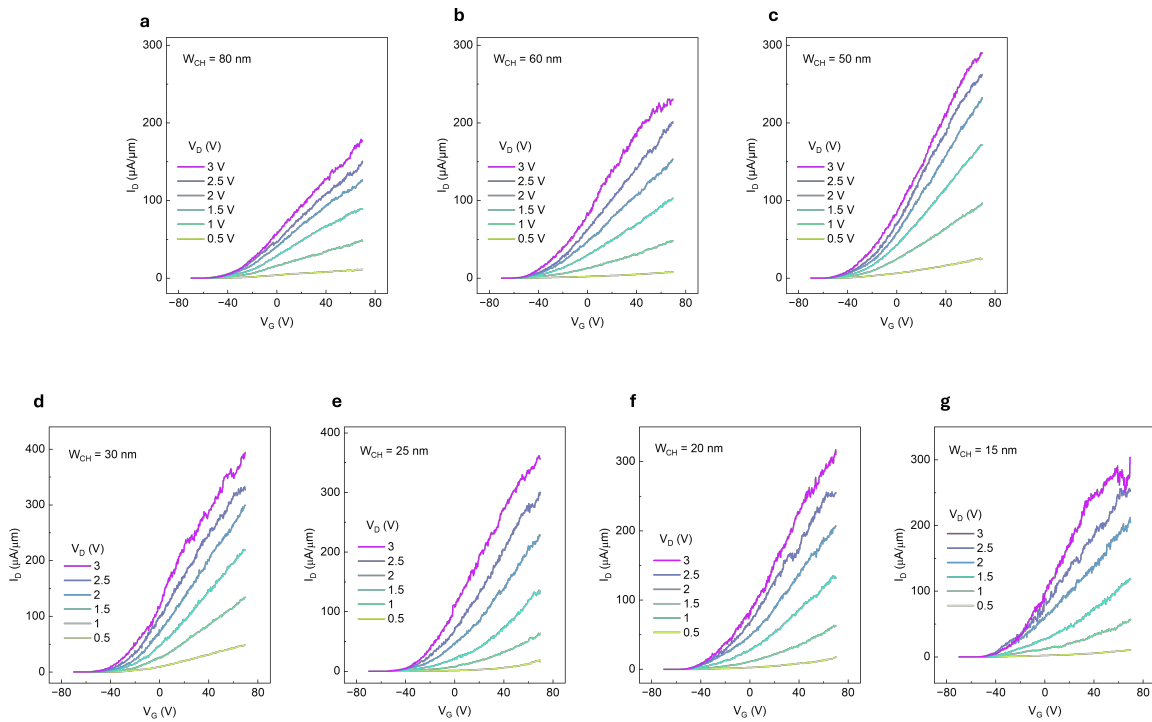


Figure B.3: Transfer characteristics for fabricated bilayer MoS_2 FETs. Channel lengths are 200 nm for all devices. The gate voltage bias sweep is between -70 V to 70 V for source-drain biases of 0.5, 1, 1.5, 2, 2.5, and 3 V. Channel widths are (a) 80 nm, (b) 60 nm, (c) 50 nm, (d) 30 nm, (e) 25 nm, (f) 20 nm, and (g) 15 nm.

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