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Integration of Fast Charger with the Powertrain of a Battery Electric Vehicle

Master's Thesis in Mobility Engineering

Fernando Dattwyler

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Fernando Dattwyler

Supervisor: Luca Boscaglia
Examiner: Yujing Liu

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Department of Electrical Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

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Chalmers University of Technology

Abstract

The transition toward sustainable transportation and the increasing adoption of electric vehicles (EVs) are driving the need for more efficient and compact fast-charging systems. This thesis investigates the integration of a fast charger with the powertrain of a battery electric vehicle by reusing existing traction components such as the inverter and electrical machine stator.

The work focuses on the experimental evaluation of integrated charging topologies, with particular attention to system efficiency, electrical behaviour, and power loss mechanisms under different operating conditions. The proposed system is based on interleaved boost converter configurations integrated with the vehicle powertrain, enabling reduced component count, lower system volume, and improved power density. An experimental test bench was developed including electrical machines, inverter hardware, measurement systems, and embedded control system. Both simulation and laboratory measurements were used to analyze switching losses, conduction losses, current ripple, and efficiency trends for different switching frequencies and phase-shift operating conditions.

The experimental results demonstrate the feasibility of integrated fast-charging systems for future electric vehicles and provide insights into the trade-offs between the studied topologies, quantifying efficiencies, losses, and ripple suppression, thereby establishing a technical baseline for full-scale systems. The results show a peak system efficiency of 94.4% for the three-phase interleaved boost topology (T1) and 93.9% for the two-phase configuration (T2). Rotor inclusion reduces the phase current ripple and does not exhibits vibrations or acoustic noise; however, it maintains similar system efficiency to T2.

Keywords: fast charging, electric vehicles, interleaved boost converter, power converter losses, electrically excited synchronous machine, permanent magnet synchronous machine

Acknowledgements

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Fernando Dattwyler
May 14th 2026, Varberg

Nomenclature

Below is the nomenclature of indices, sets, parameters, and variables that have been used throughout this thesis.

Acronyms

AC	Alternate Current
AFE	Active Front-End
BEV	Battery Electric Vehicle
BMS	Battery Management System
CAN	Controller Area Network
CC	Constant Current
CCM	Continuous Conduction Mode
CCS	Combined Charging System
CHAdeMO	CHArge de MOve (EV charging standard)
CV	Constant Voltage
DAB	Dual Active Bridge
DC	Direct Current
EESM	Electrically Excited Synchronous Machine
EM	Electric Machine
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EV	Electric Vehicle
FCS-MPC	Finite Control Set Model Predictive Control
GaN	Gallium Nitride
GB/T	Guo Biao/Tui (Chinese national standard)
ICE	Internal Combustion Engine
MCS	Megawatt Charging System
MHEV	Mild Hybrid Electric Vehicle
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MW	Megawatt

NACS	North American Charging Standard
OBC	On-Board Charger
PFC	Power Factor Correction
PHEV	Plug-in Hybrid Electric Vehicle
PI	Proportional-Integral
PLL	Phase-Locked Loop
PLC	Power Line Communication
PMSM	Permanent Magnet Synchronous Machine
PPP	Partial Power Processing
PSFB	Phase-Shift Full-Bridge
PWM	Pulse Width Modulation
SiC	Silicon Carbide
SOGI	Second-Order Generalized Integrator
SoC	State of Charge
SPICE	Simulation Program with Integrated Circuit Emphasis
SRF-PLL	Synchronous Reference Frame Phase-Locked Loop
SRM	Switched Reluctance Motor
SynRM	Synchronous Reluctance Machine
T1	Topology 1 (Three phase interleaved converter)
T2	Topology 2 (Two phase interleaved converter)
THD	Total Harmonic Distortion
V2G	Vehicle-to-Grid
V2H	Vehicle-to-Home

Symbols

a_n, b_n	Fourier cosine and sine coefficients
B_{pk}	Peak flux density [T]
C	Output filter capacitance [F]
C_{min}	Minimum output capacitance [F]
C_{oss}	MOSFET output capacitance [F]
$C_{\mathrm{oss}}^{\mathrm{eff}}$	Effective output capacitance [F]
D, D_n	Diode
d, d_k	Duty cycle (of phase k)
E_{on}, E_{off}	Turn-on and turn-off energy [J]
f	Frequency [Hz]

f_{sw}		Switching frequency [Hz]
f_s^*		Effective ripple frequency [Hz]
$g(d)$		Ripple factor function
I_{bat}		Battery charging current [A]
I_C		Capacitor current [A]
I_D, I_D		Drain current [A]
I_{DC}		DC current component [A]
$I_{fn^*,\text{in}}$		Fundamental input current at dominant harmonic [A]
$I_{fn^*,out}$		Fundamental output current at dominant harmonic [A]
$I_{fn^*,1}$, $I_{fn^*,3}$	$I_{fn^*,2}$,	Fundamental phase current at dominant harmonic [A]
I_{in}		Input current [A]
I_L, $I_{L,k}$		Inductor current (of phase k) [A]
$I_{n,rms}$		RMS value of n-th harmonic [A]
I_{out}		Output current [A]
ΔI_{pp}		Peak-to-peak current ripple [A]
I_{RMS}		Root-mean-square current [A]
I_{rr}		Peak reverse-recovery current [A]
j		Imaginary unit ($\sqrt{-1}$)
$\mathbf{J}(\mathbf{r}, t)$		Current density vector [A/m^2]
k		Steinmetz coefficient
k_h		Hysteresis loss coefficient
k_L		Inductance unbalance factor
k_R		Resistance unbalance factor
K_c		Eddy current loss coefficient
K_e		Excess loss coefficient
K_h		Hysteresis loss coefficient
L, L_k		Boost inductance (of phase k) [H]
L_b		Boundary inductance for CCM [H]
L_{eff}		Effective per-phase inductance [H]
L_{in}		Series input inductance [H]
L_{nom}		Nominal inductance [H]
N		Number of interleaved phases
n^*		Dominant harmonic order
n_{leg}		Number of active legs
$p_{M,losses}(t)$		Instantaneous MOSFET loss power [W]
P_{body}		Body diode conduction loss [W]

$P_{EM,core}$	Total core loss [W]
$P_{EM,eddy}$	Eddy current loss [W]
$P_{EM,cu}$	Copper loss of electric machine [W]
$P_{EM,cu}^{AC}$	AC copper loss [W]
$P_{EM,cu}^{DC}$	DC copper loss [W]
$P_{EM,losses}$	Electric machine losses [W]
P_{exc}	Excess (anomalous) loss [W]
P_{gate}	Gate drive loss [W]
$P_{EM,hys}$	Hysteresis loss [W]
P_{in}	Input power [W]
$P_{inv,cond}$	Inverter conduction losses [W]
$P_{inv,losses}$	Inverter losses [W]
$P_{inv,sw}$	Inverter switching losses [W]
$P_{L,core}$	Core loss of inductor [W]
$P_{L,cu}$	Copper loss of inductor [W]
$P_{losses,EM}$	Electric machine losses [W]
$P_{losses,inv}$	Inverter losses [W]
$P_{M,body}$	MOSFET body diode loss [W]
$P_{M,cond}$	MOSFET conduction loss [W]
$P_{M,C_{oss}}$	MOSFET output capacitance loss [W]
$P_{M,gate}$	MOSFET gate drive loss [W]
$P_{M,losses}$	Total MOSFET losses [W]
$P_{M,rr}$	MOSFET reverse-recovery loss [W]
$P_{M,sw}$	MOSFET switching loss [W]
P_{out}	Output power [W]
P_{rr}	Reverse-recovery loss [W]
P_{solid}	Solid (copper) loss in Maxwell [W]
P_{sw}	Switching loss [W]
$P_{syst,losses}$	Total system losses [W]
P_{th}	Power thermal limit for EM [W]
P_{total}	Total loss [W]
Q_g	Gate charge [C]
Q_{rr}	Reverse-recovery charge [C]
R_{bat}	Battery internal resistance [Ω]
R_{DC}	DC resistance [Ω]
$R_{DS,on}$, $R_{DS,on}$	MOSFET on-state resistance [Ω]
R_{ESR}	Equivalent series resistance of capacitor [Ω]

R_{nom}	Nominal resistance [Ω]
S, S_k	Controlled switch (of phase k)
$\overline{S_k}$	Synchronous diode (of phase k)
t	Time [s]
t_{dt}	Dead time [s]
t_f, $t_{f,i}$, $t_{f,v}$	Current/voltage fall time [s]
t_r, $t_{r,i}$, $t_{r,v}$	Current/voltage rise time [s]
t_{rr}	Reverse-recovery time [s]
T, T_{sw}	Switching period [s]
T_{cond}	Conduction interval [s]
T_{off}	Turn-off transition interval [s]
T_{on}	Turn-on transition interval [s]
V_{bat}	Battery voltage [V]
V_C	Output capacitor voltage [V]
V_c	Core volume [m^3]
V_{DC}, V_{DC}	DC bus voltage [V]
V_{DS}, V_{DS}	Drain-source voltage [V]
V_F	Body diode forward voltage [V]
V_{GS}, V_{GS}	Gate-source voltage [V]
V_{in}	Input voltage [V]
V_L	Inductor voltage [V]
$V_{M,H}$, $V_{M,L}$	High-side/low-side MOSFET voltage [V]
V_{out}	Output voltage [V]
α	Steinmetz frequency exponent
β	Steinmetz flux density exponent
ΔI_{in}	Input current ripple [A]
ΔI_{L_k}	Current deviation of phase k [A]
ΔI_{pp}	Peak-to-peak current ripple [A]
ΔV_C	Output capacitor voltage ripple [V]
$\Delta V_{C,max}$	Maximum allowable voltage ripple [V]
$\Delta\phi$	Phase shift between consecutive phases [rad]
η_{EM}	Electric machine efficiency
η_{inv}	Inverter efficiency
η_{system}	Overall system efficiency
θ	Phase shift angle [rad]
τ	Time delay between phases [s]
ω_s	Angular switching frequency [rad/s]

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Chapter 1

Introduction

1.1 Overview

In recent years, efforts for the transition to a sustainable transport system have intensified. The European Union (EU) aims to reduce transport greenhouse gas emissions by 90% in 2050, with an interim goal of 30 million zero-emission vehicles by 2030. Electric vehicles (EVs) are key to reducing emissions and fossil fuel dependence in road transport. This transition requires improvements in battery technology, electrical machines, power electronics, control systems, power train design, and charging infrastructure to enhance vehicle range, efficiency, and feasibility [1, 2].

The charging system is a main component of electric vehicle technology. Development on these systems are required to reduce charging times, increase power density and energy conversion efficiency without compromising safety or battery life. Consequently, research into new fast-charging architectures has become a central topic in power electronics for e-mobility [3, 4]. Fast chargers must accurately control voltage and current to ensure optimal battery charging their extending lifespan, while also supporting bidirectional power flow for vehicle-to-grid (V2G) and vehicle-to-home (V2H) functionalities. The need for fast chargers is driven not only by user convenience but also by broader energy-system integration, as EVs become part of the smart grid ecosystem [4, 5, 6].

Recent developments have explored integrated fast-charging systems, where the charger shares components with vehicle's powertrain stages, such as the traction inverter or the electrical machine's stator . This integration reduces volume, weight, and cost by using less material. However, challenges remain in thermal management, EMI mitigation, and striking the right balance between power density, cost, and efficiency [4, 7, 6].

Previous studies have demonstrated the feasibility of integrating the fast charger into the powertrain [8, 7, 9]. However, more conclusive results for industrial application require validation through experimental testing. Therefore, this thesis contributes studying the performance, losses and efficiency of a compact fast-charging system integrated with the powertrain through an experimental approach, focusing on electrical behaviour, system efficiency, and integration with the traction system during charging using optimal control for the system efficiency.

1.2 Scope of the Thesis

To investigate the performance, efficiency, and operational characteristics of the proposed system are set up four main goals.

- **Design and Implementation of Experimental Setup:** Build a prototype of a fast charger system including a power supply, machine stator winding, inverter, and load to emulate the EV battery. Ensuring that the setup allows controlled testing under different voltage, current, and power conditions.
- **Efficiency Analysis:** Measure the overall system efficiency under various operating points and identify major power losses contributors by using open loop control.
- **Electrical and Powertrain Integration Study:** Evaluate potential level of integration between the fast charger and the rotor/machine during charging process.
- **Recommendation for future designs:** Based on experimental results and scaled up simulations, suggest optimizations/changes of the system elements or operating points to reach higher efficiency. Provide insights for the integration of fast-charging systems into EV powertrains for future industrial applications.

1.3 Limitations

To ensure project feasibility and achieve the stated objectives within the available resources and time-frame, the following limitations are defined:

- **Measurement Range and Operating Conditions:** Tests will be conducted under controlled laboratory conditions within the rated voltage and current limits of the available equipment. Long-term endurance testing are not included.
- **Hardware and Software Constraints:** The experimental implementation will be limited by the specifications of the available inverter, sensors, data acquisition system, and control hardware. The software used for simulation includes ANSYS Maxwell, LTSpice, MATLAB, and PLECS.
- **Control and System Integration Scope:** The thesis will focus on the electrical performance and control parameters of the fast-charging system during charging. Broader system-level functions, such as V2G operation or battery management algorithms, will not be studied.
- **Time and Resource Constraints:** The project duration is limited to one semester, restricting the extent of experimental variations. The primary focus will remain on validating the fast charger's efficiency and operation. Additional optimization or redesign iterations are considered future work.

1.4 Thesis outline

The thesis is structured in the following form:

Chapter 2. This chapter presents the state of the art of charging technologies for electric vehicles, introducing and defining the fundamental concepts related to EV charging systems. Different charging approaches and architectures are discussed to provide the necessary background for the subsequent chapters.

Chapter 3. This chapter defines the methodology adopted to carry out the experimental work of the thesis. The electrical topology, system architecture, experimental setup, and the criteria used for efficiency evaluation are described in detail.

Chapter 4. This chapter analyses the proposed charging topologies to understand their operating principles and transfer functions.

Chapter 5. This chapter presents the main experimental results and provides a discussion of the system performance, efficiency, and observed behaviour under different operating conditions.

Chapter 6. This chapter summarizes the main conclusions of the thesis and outlines possible directions for future work and further development.

Chapter 2

State of Art

This chapter starts by introducing the definitions for electric vehicles and charging systems, followed by a comprehensive review of the current charging architectures, with a focus on integrated chargers. Then, the chapter explain some control strategies for these systems to end with the follow trends and challenges for the development of the charging systems.

2.1 Introduction to Electric Vehicles

An electric vehicle (EV) is a road vehicle propelled entirely or partially by one or more electric machines (EM), drawing energy from onboard rechargeable batteries instead of fuel like internal combustion engines (ICE) do. EVs have become an important element in reducing greenhouse gases, as they can eliminate tailpipe emissions during operation and achieve higher energy efficiency compared to traditional vehicles. However, the autonomy provided by the battery pack and the required recharging time remain challenges for a full transition, specially in locations with extreme weather where battery capacity is reduced by 50% [10, 11]. While EV is a broad term that can include trucks, motorcycles, scooters, etc., in this thesis the term will refer specifically to cars.

The main components of an EV powertrain include the battery pack, EMs, power electronics, control systems, and transmission among others. However, different configurations exist regarding how the powertrain's components are interconnected. Typical powertrains with their corresponding power flows are shown in Figures 2.1, 2.2, 2.3, and 2.4.

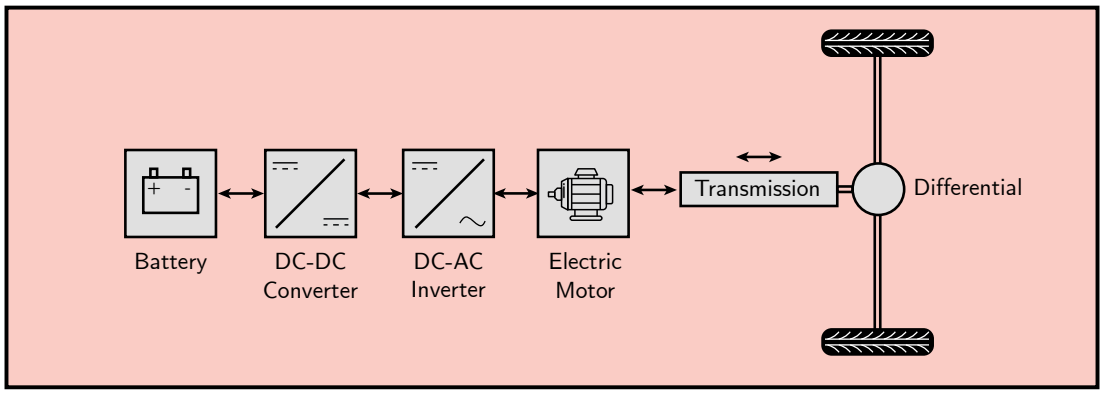

Figure 2.1: Battery electric powertrain

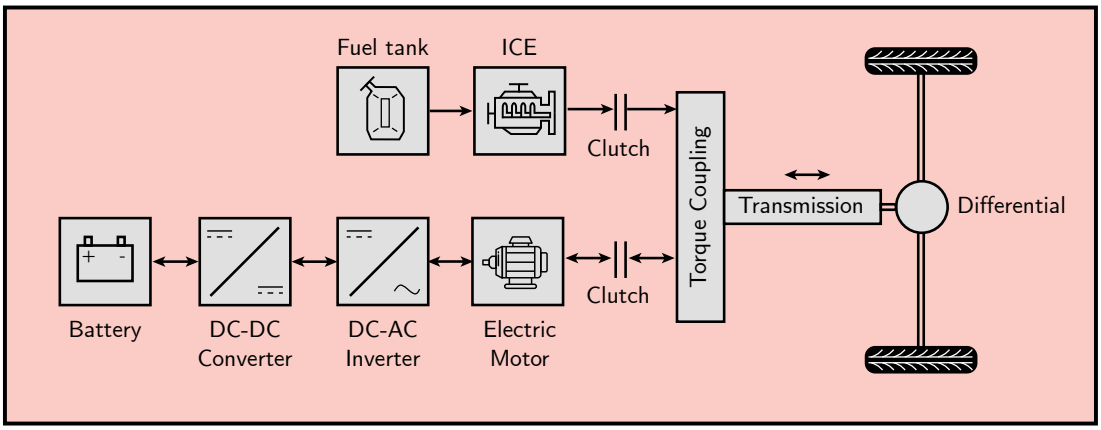

Figure 2.2: Parallel hybrid powertrain

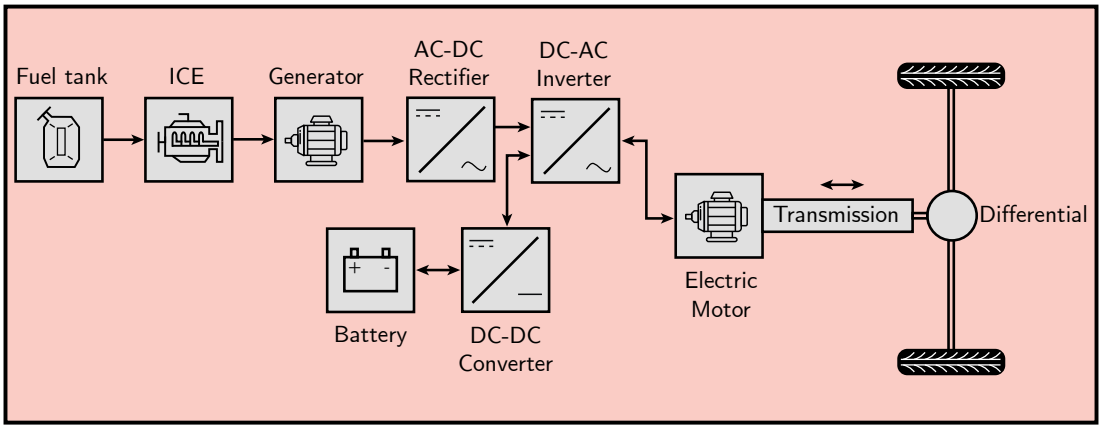

Figure 2.3: Series hybrid powertrain

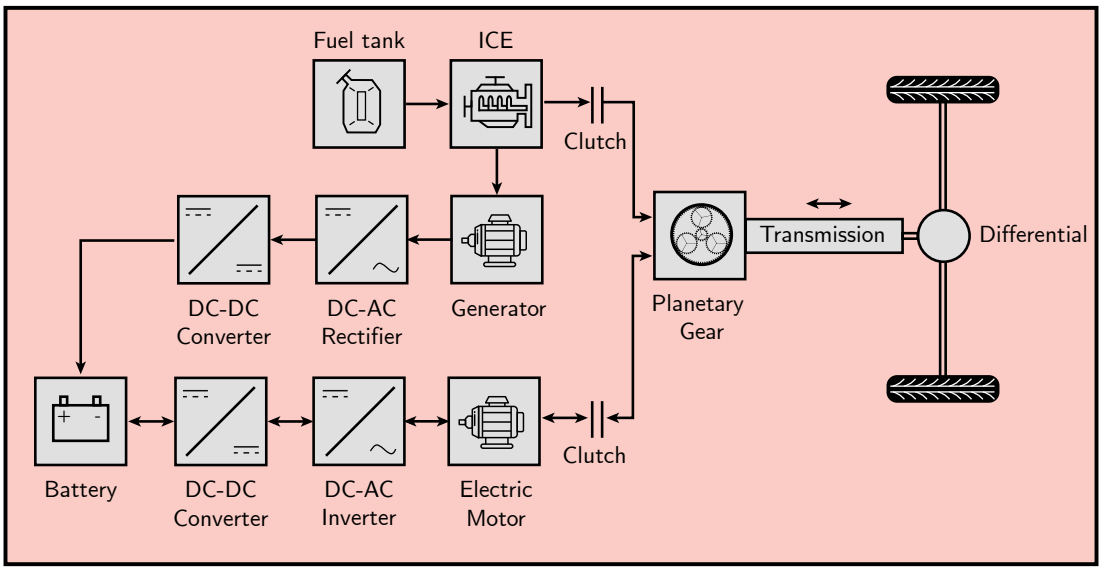

Figure 2.4: Series-parallel hybrid powertrain

EVs also can be classified by their level of electrification. Vehicles powered exclusively by electric energy are referred to as battery electric vehicles (BEVs), in which all traction energy is stored in an onboard battery pack. Representative examples include the Tesla Model Y, Volkswagen ID.4, and Nissan Leaf. Hybrid electric vehicles combine two distinct energy sources for propulsion, typically an internal combustion engine and electrical machine(s). Within this category, mild hybrid electric vehicles (MHEVs) employ small battery packs that cannot be externally charged and are mainly used to enable regenerative braking, provide torque assistance during short intervals, and improve compliance with emission regulations. In contrast, plug-in hybrid electric vehicles (PHEVs) are equipped with larger batteries that can be recharged from the electrical grid, allowing the vehicle to operate in all-electric mode over longer distances before the internal combustion engine is engaged.
In this context, batteries and charging systems become specially relevant for BEV and PHEV; this kind of vehicles depend on external charging stations to fully exploit their propulsion capabilities. As it can be seen in Figure 2.5 and 2.6, during the last decade the share of BEV and PHEV has increased, remarking the efforts to integrate these vehicles to the current and upcoming infrastructure [12].

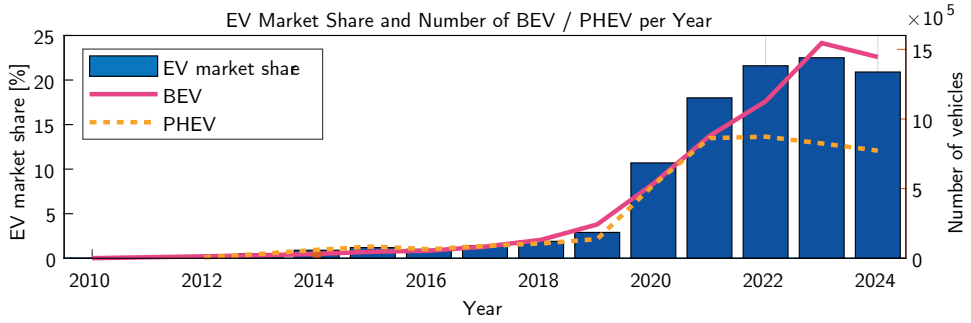

Figure 2.5: Trend of new registered electric cars in EU (Based on [12])

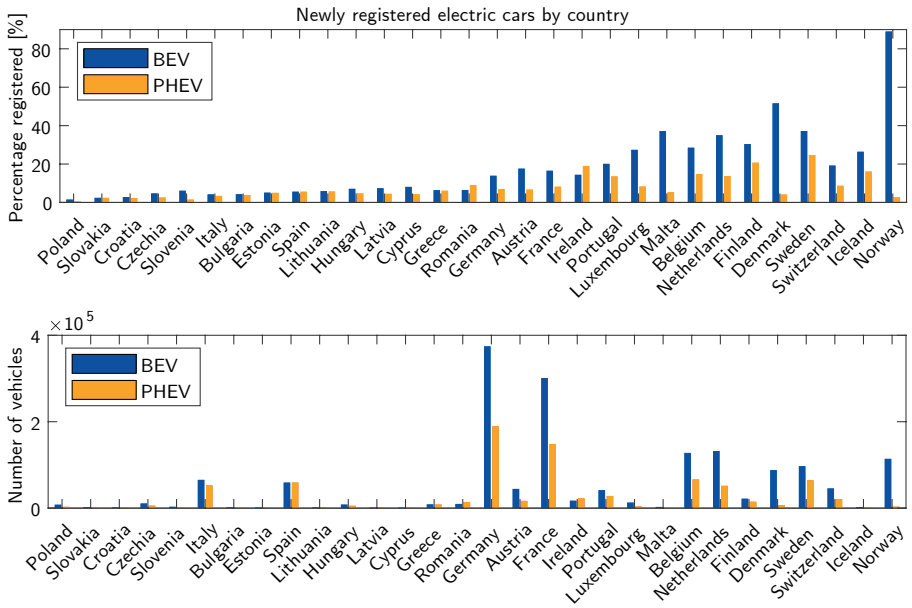

Figure 2.6: Newly registered electric cars by country in 2024 (Based on [12])

Lastly, Table 2.1 presents a list of popular electric vehicles in Europe, classified according to their level of electrification, battery capacity, and charging times. For BEVs, higher-voltage architectures are generally associated with higher allowable charging power. The differences in charging times from hours to minutes reflect ongoing efforts by manufacturers and infrastructure providers to develop high-power charging systems.

Table 2.1: Battery capacity, charging power, voltage architecture and manufacturer-declared charging times of selected electrified vehicles in Europe

Manufacturer & Model	**Battery (kWh)**	**Max DC (kW)**	**Arch. (V)**	**Slow charge (AC < 11 kW)**
Battery Electric Vehicles (BEV)				
Hyundai IONIQ 5 [13]	80	205	800	∼8h.45m
Kia EV6 Long Range AWD [14]	80	205	800	∼8h.45m
Tesla Model 3 Long Range [15]	79	125	400	∼8h.30m
Tesla Model Y Long Range [16]	77	130	400	∼8h.15m
Volkswagen ID.4 [17]	77	120	400	∼8h.15m
Skoda Enyaq iV [18]	77	125	400	∼8h.15m
Renault Megane E-Tech [19]	60	88	400	∼6h.30m
Volkswagen ID.3 Pure [20]	52	90	400	∼8h.30m
Nissan Leaf [21]	39	40	400	∼12h.45m
Fiat 500e Hatchback [22]	21.3	40	400	∼2h.30m
Plug-in Hybrid Electric Vehicles (PHEV)				
Toyota RAV4 (XA50) [23]	18.1	–	–	∼4 h*
Volvo XC60 Recharge [24]	18.8	–	–	∼5 h*
Volkswagen Passat GTE [25]	9.9	–	–	∼4 h*
BMW F30 3 Series [26]	7.6	–	–	∼5 h*
Mild Hybrid Electric Vehicles (MHEV)				
Audi A6 50 TDI MHEV [27]	0.5	–	–	N/A
BMW X5 MHEV [28]	0.4	–	–	N/A
Mercedes-Benz E 220 d MHEV [29]	<1	–	–	N/A

*Charging time declared by manufacturer using onboard AC charger (typically 3.6–7.4 kW).

2.2 Overview of EVs charging systems functionalities

The charging system enables the vehicle's battery to store energy from an external power source. It includes the electric hardware, control strategies, and communication functionalities necessary for energy transfer while meeting its operational constraints [6, 30, 31, 32]. Although there are different solutions for EV chargers, all of them have some core functionalities, which are presented in the following subsections.

2.2.1 Electrical protection

Electrical protection functions are needed to guarantee safe operation under normal and fault conditions, mitigating risks such as thermal runaway, fires, or explosions [6, 9]. These functions are responsible for detecting abnormal electrical behaviour and interrupting power transfer when necessary, in order to protect the user, vehicle, and electrical grid.

Particularly, IEC 61851-1 [33] and IEC 61851-23 [34] specify safety requirements for electric vehicle supply equipment, including protection against over-voltage, under-voltage, short-circuit conditions, insulation faults, and safe connection and disconnection procedures. Complementary safety protection against electric shock and automatic disconnection are defined in IEC 60364-4-41 [35]. Additionally, ISO 17409 [36] establishes safety requirements for the connection of electrically propelled road vehicles to external electric power supplies.

As a summary, electrical protection functionalities must include:

- Over-voltage protection
- Under-voltage protection
- Over-current and short-circuit protection
- Ground fault and residual current detection
- Isolation monitoring
- Pre-charge control and inrush current limitation
- Contactor control and safe disconnection

2.2.2 EMI / EMC filtering

The objective of the electromagnetic compatibility (EMC), is to ensure that the charging system operates without causing electromagnetic interference (EMI) or being susceptible to it. This is achieved through the implementation of input filtering, such as common-mode chokes, X/Y capacitors, shielding, and appropriate grounding strategies. EMC standards for charging systems are specified in IEC 61851-21-1 [37] and IEC 61851-21-2 [38], which define conducted and radiated emission limits as well as immunity requirements for on-board and off-board chargers. In addition, vehicle-level EMC requirements are addressed by standards such as CISPR 25 [39] and the ISO 11452 [40] series, which aim to limit electromagnetic disturbances and ensure the immunity of onboard communication systems and sensitive electronic components during charging operation.

The EMC functionalities include:

- Conducted EMI attenuation
- Radiated emission reduction
- Compliance with grid harmonic limits
- Protection of vehicle communication and sensors

2.2.3 Power Conditioning and Conversion

If the charging system is connected to an AC grid, the power conversion stage must comply grid power quality requirements. This is typically achieved through power factor correction implemented in the front-end converter. International standards such as IEC 61851-1 [33] and IEC 61851-23 [34] establish general requirements for controlled energy transfer. However, these standards do not explicitly define grid-side power factor or harmonic performance limits. Grid-related power quality constraints, including harmonic current emissions, are instead defined in IEC 61000-3-2 [41] and IEC 61000-3-12 [42], depending on the rated input current.

Accordingly, the power conditioning functionalities include:

- Near-unity power factor correction
- Low current total harmonic distortion (THD)
- Stable DC link generation

2.2.4 Output Power Control

The power transfer during the charging process must be controlled to ensure safe battery operation and preserve battery lifetime. IEC 61851-1 [33] defines general requirements for conductive EV charging systems, including guidelines for controlled energy transfer, safety functions, and permissible current levels communicated between the EV and the supply equipment. IEC 61851-23 [34] specifies requirements for DC charging stations, including output voltage and current limits, and system behaviour during steady-state and transient conditions.

2.2.5 Battery protection and communication

Battery protection functionalities are shared between the charging system and the battery management system (BMS). The charging process is supervised and controlled based on signals and charging limits provided by the BMS. High-level communication between the EVs and the charging system is typically implemented using power line communication (PLC) in accordance with the ISO 15118 [43] series, which defines application-layer protocols for communication handshake, charging control, and smart charging functionalities. For DC charging systems, lower-layer communication requirements are further specified in IEC 61851-24 [44]. Within the vehicle, internal communication between control units, including the BMS and other subsystems, commonly relies on automotive communication protocols such as ISO 11898 (CAN bus) [45] or Automotive Ethernet implementations aligned with relevant ISO Ethernet standards [43].

Based on these requirements, the main communication functionalities include:

- Handshake procedures and user or vehicle authorization.
- Set of charging parameters, including voltage and current limits.
- Monitoring of safety-related states and fault conditions during charging.

2.3 Classification for EVs charging systems

Charging systems can be broadly categorized according to their power level, charging speed, and power conversion topology as is shown in Figure 2.7.

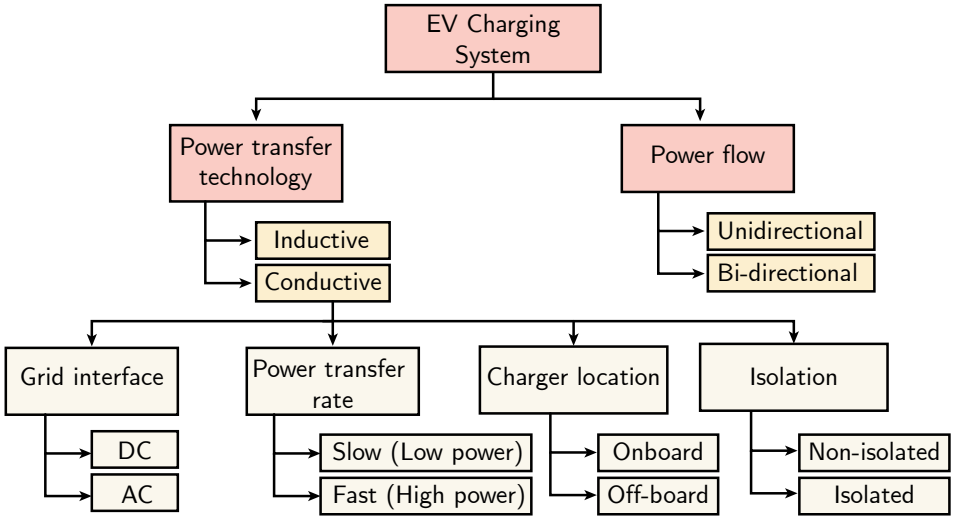

Figure 2.7: EVs Charging system classification

It is possible to start the classification with the difference between conductive and inductive charging. Conductive charging is the most established method for electric vehicles. In this approach, electrical energy is transferred from the grid to the vehicle through a direct electrical connection, typically via a cable and plug, compliant with standards such as IEC 61851 [6, 33]. Inductive charging, in contrast, is a form of wireless power transfer in which energy is transmitted from a ground-side coil to a vehicle-side coil through magnetic coupling, without direct electric contact. Standardization efforts for wireless charging are addressed in IEC 61980 [6, 46]. This technology is still under development but is characterized by user convenience and electrical isolation. However, inductive charging generally has lower efficiency and power density compared to conductive charging.

Additionally, chargers can be unidirectional or include bidirectional power flow capabilities, enabling vehicle-to-grid (V2G) and vehicle-to-home (V2H) functionalities. This allows EVs to return energy to the grid, which is required for integration into smart energy management system and support actions such as peak shaving in the demand response[3].

Depending on the grid interface, chargers can be connected to either an AC or DC power supply. AC charging standards are typically associated with slow charging that involves on-board systems. In contrast, DC fast charging relies on off-board chargers, as the high power required cannot be managed by on-board systems and would take up excessive space within the electric vehicle. As a result, this remains an area of ongoing development. [4].

In terms of power transfer rate, slow traditional chargers are typically used in residential or workplace environments due to their simplicity, cost-effectiveness, and compatibility with standard grid connections, which leads to longer charging times. In contrast, fast chargers operate at significantly higher power levels, using DC charging architectures, to reduce charging times [4]. However, fast charging introduces additional challenges due to high power flow and

thermal stresses on the battery and power electronics. A list of the charging standards are shown in Table 2.2, 2.3 and 2.4

Table 2.2: Standards for AC Electric Vehicle Charging (Based on [6])

Parameter	Charging Standard			
	SAE J1772	**IEC 61851**	**GB/T**	**NACS**
Charging mode / level	Level 1–2	Modes 1–3	AC charging	Mobile / Wall
Maximum AC voltage [V]	120–240	230 (1ϕ) / 400 (3ϕ)	220 (1ϕ) / 380 (3ϕ)	120–240
Maximum current [A]	80	32[a]	32	48[c]
Maximum power [kW]	19.2	22	12.8	11.5[c]
V2X capability	No[b]	No[b]	No[b]	No[b]
Region	US, JP, SK	EU, AU	CN, IN	North America

[a] Some high-power AC configurations for Mode 3 can reach 43 kW (requiring 63 A), though 32 A / 22 kW is the standard reference.
[b] While listed as "No" for basic AC conductive charging, bidirectional control is a future requirement being integrated via the ISO 15118 protocol.
[c] Tesla NACS AC charging supports up to 48 A (11.5 kW) for single-phase home or wall charging.

Table 2.3: Standards for DC Fast Charging Stations (Part I) (Based on [6])

Parameter	Charging Standard			
	CHAdeMO	**GB/T**	**CCS Type 1**	**CCS Type 2**
Output voltage [V]	50–1000	250–950	200–1000	200–1000
Maximum current [A]	400	250	400	400
Maximum power	400 kW	237.5 kW	200 kW	350 kW
Communication protocol	CAN	CAN	PLC	PLC
V2X capability	Yes	No	No	No
Compliant standards	IEEE 2030.1.1, IEC 62196-3	IEC 62196-3	SAE J1772, IEC 62196-3	IEC 62196-3
Region	Worldwide	China, India	United States, South Korea	Europe, Australia

Table 2.4: Standards for DC Fast Charging Stations (Part II) (Based on [6])

Parameter	Charging Standard		
	ChaoJi	**NACS**	**MCS**
Output voltage [V]	1000–1500	300–480	500–1250
Maximum current [A]	600	800	3000
Maximum power	900 kW	250 kW	3.75 MW
Communication protocol	CAN	CAN	PLC
V2X capability	Yes	No	Yes
Compliant standards	CHAdeMO, GB/T	IEC 62196-3	IEC 62196-3, IEC 61851-23
Region	Worldwide	Worldwide	Worldwide

As it was mention, battery chargers can be on-board or off-board, being the main difference where is located the power converter that handle the charge and the ownership of the charger [31], as it shown in Figure 2.8. Off-board charging systems include public charging stations, rapid chargers, inductive charging, and home charging stations. They are installed in both public environments, such as fuel stations, or private locations, like homes. Depending on the power level and system architecture, off-board chargers may operate in AC or DC mode. In this case, the external charger is responsible for battery voltage and current regulation, enabling straightforward integration with the electrical grid and shared charging infrastructure.
On-Board Charging Systems are integrated into the car, allowing direct connection to the home grid [9, 31]. This setup includes a power electronic converter that manages the voltage and current during the charging process. The main advantage is its flexibility, as the onboard charger (OBC) can adapt to various input sources, both AC and DC, and different voltage levels. This flexibility eliminates the need of searching an specific charger while be compliant with the vehicle's battery requirements. However, there are limitations of weight, space, and power that must be considered for inclusion in the car.

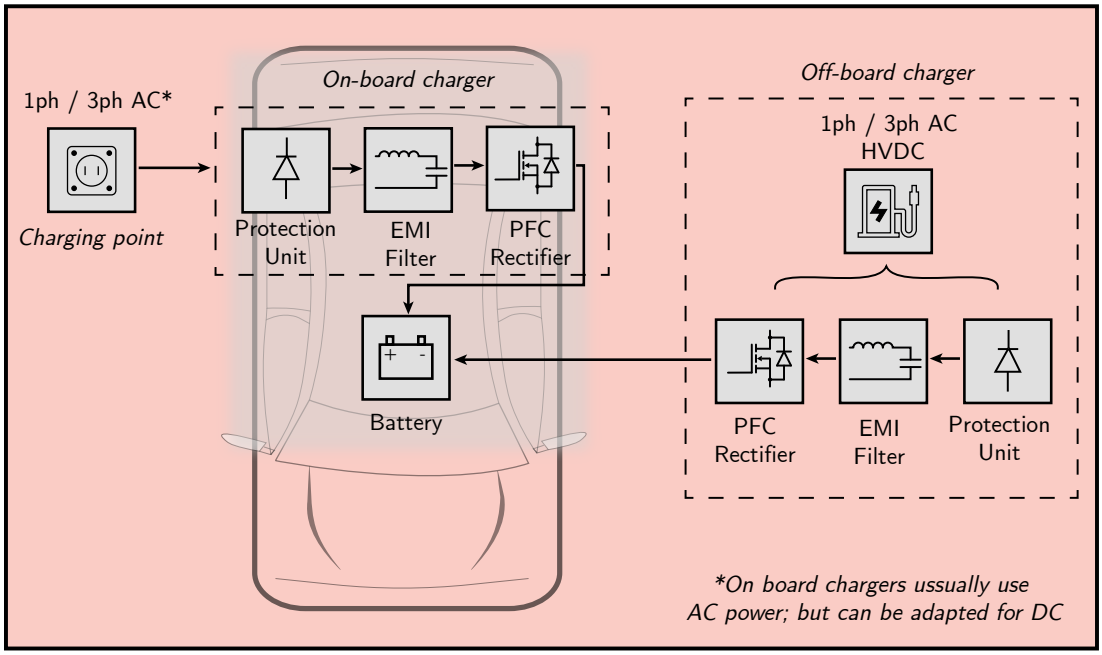

Figure 2.8: On-board and Off-board charging system diagram

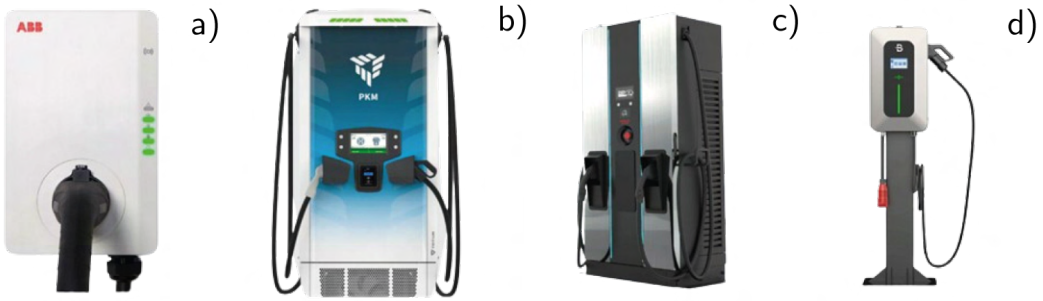

Figure 2.9: Commercially available off-board EV charging systems: (a) ABB Terra AC wallbox [47], (b) Tritium 150 kW DC charger [48], (c) PHIHONG DS150 Series EV charger [49], and (d) BENY IP65 22 kW wall-mounted DC charger [50].

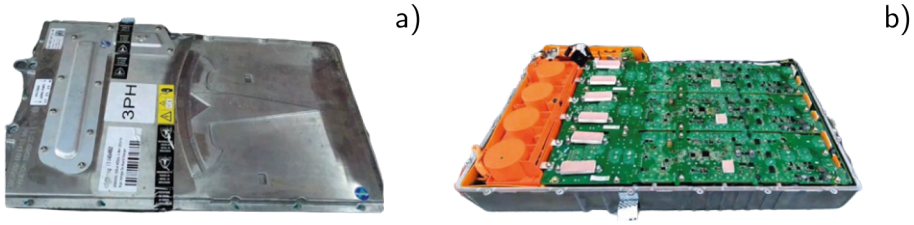

Figure 2.10: Tesla Gen 3 OBC: (a) closed enclosure view, (b) open enclosure view [51].

2.4 Battery chargers efficiency

Efficiency is one of the main metrics in charging systems, as it directly affects thermal management, achievable power density, and overall cost. This motivates the investigation of topologies that maximize energy conversion. Table 2.5 summarizes some representative off-board charger architectures. DC-connected systems frequently achieve higher efficiency compared to standalone AC-connected designs. High-power DC fast chargers, such as the Tritium PKM150, can reach up to 97% efficiency [48], outperforming AC-DC designs such as the ABB Terra HP, which achieves 95% [52] with the same power level. This performance gap is primarily driven by the DC conversion topology, which requires only a single centralized rectification stage. By sharing this stage among multiple charging units, the total number of power conversion stages is reduced, minimizing the cumulative energy losses found in AC-connected stations where each individual charger must include its own AC-DC conversion. Furthermore, the table shows that emerging reconfigurable topologies, such as the r-PSFB [53] and the reconfigurable DAB proposed by Zayed et al. [54] can achieve high efficiencies of 97.8% and above 97.5%, respectively, while addressing interoperability by handling a wide output voltage range (200,V to 1000,V), allowing a single infrastructure to serve both 400 V and 800 V charging systems. While non-isolated topologies such as the bidirectional T-type converter [55] can reach peak efficiencies of up to 98%, they are often limited to specific distribution applications because safety standards such as IEC 61851-23 mandate galvanic isolation for each port in multi-output simultaneous charging systems [34].

A compilation of representative OBC and integrated powertrain charger architectures is provided in Table 2.6. The data indicates that on-board systems exhibit significant performance variations based on their electrical topology and whether they incorporate galvanic isolation. Non-isolated topologies, such as the integrated fast charger proposed by Eull et al., achieve some of the highest reported peak efficiencies in current literature, exceeding 98.5% at 11,kW [56]. By removing the physical transformer, these systems eliminate the significant core and copper losses typically associated with galvanic separation. For instance, the integrated charger developed by Kushwaha et al. demonstrates that partial power processing (PPP) can reduce the converter's processed power rating substantially for an 11,kW application, achieving a total system efficiency above 97% [30]. The table also reflects the industry's transition toward higher-voltage vehicle architectures, with emerging designs such as that of Eull et al. targeting output voltage levels of 700–800,V to support faster charging with lower current-related conduction losses. Finally, integrated designs such as the Renault ZOE or the dual-motor topology proposed by Tong et al. may exhibit lower peak efficiencies compared to dedicated OBC solutions—reporting near 91% [57] and approximately 96.1-82% (depending on load and configuration) [58], respectively. However, these figures reflect early-stage implementations where neither the power converter nor the electrical machine has been fully co-optimized for the charging function, leaving room for efficiency improvement, and were primarily driven by the motivation to reuse existing traction components.

Table 2.5: Overview of off-board chargers efficiency

Name / Model	Electrical Topology	AC-DC / DC-DC	Isolation	Output Voltage	Power Rating	Efficiency
PHIHONG 150 Series [49]	-	AC-DC	Yes	200–950 V	150 kW	94%
ABB Terra HP [52]	3-ph Rectifier and Interleaved buck	AC-DC	Yes	150–920 V	150 kW	95%
Bidirectional T-type Converter [55]	3-Phase 3-Level T-type	AC-DC	No	400–1000 V	11–22 kW	98%
Swiss Rectifier [59]	Interleaved DC-DC Output	AC-DC	No	400 V	8 kW	96.5%
Enercon E-charger 600 [60]	3ph Rectifier and Phase-Shift Full-Bridge	DC-DC	Yes	200–920 V	350 kW	94%
Tritium PKM150 [48]	-	DC-DC	Yes	150–920 V	150 kW	97%
r-PSFB [53]	3-Winding Transformer PSFB	DC-DC	Yes	250–1000 V	11 kW	97.8%
Zayed et al. DAB [54]	Reconfigurable DAB	DC-DC	Yes	200–1000 V	10 kW	<97.5%

Table 2.6: Overview of on-board chargers efficiency

Name / Model	Electrical Topology	AC-DC / DC-DC	Isolation	Output Voltage	Power Rating	Efficiency
GaN Modular (Lu et al.) [61]	AC-link + DAB	AC-DC	Yes	200–450 V	22 kW	<97%
BRUSA NLG667 [62]	-	AC-DC	Yes	570–750 V	20.5 kW	<94%
PPP Integrated (Kushwaha et al.) [30]	Partial Power Processing	AC-DC	Yes	700–800 V	11 kW	<97%
Bidirectional Non-isolated Fast Charger Integrated (Eull et al.) [56]	Bidirectional VFCSS	AC-DC	No	700–800 V	11 kW	>98.5%
A Multi-Functional Integrated Onboard Charger for Dual-Motor (Tong et al.) [58]	AFE + Buck	AC-DC	No	288 V	∼5.1 kW	∼82.37%*
Single-Phase On-Board Integrated Battery Chargers (Subotic et al.) [63]	Multiphase inverter + Buck-Boost	AC-DC	No	600 V	500 W	81%
Renault ZOE [57]	Interleaved Boost	AC-DC / DC-DC	No	400 V	43 kW	<91.73%
3-Phase CLLC (Chen et al.) [64]	SiC-based Bidirectional Three-phase CLLLC	DC-DC	Yes	330–500 V	20 kW	<98.67%
(Tong et al.) [58]	Interleaved Buck	DC-DC	No	288 V	∼2.9 kW	<96.1%

2.5 Integrated Battery Chargers and Powertrain Integration

A different approach of on-board charging are integrated electric car chargers; these chargers reuse traction components while charging reducing system volume, weight, and cost by avoiding the need for specialised power electronic converters. During the charging process, the inverter switches are connected to operate as an AC–DC rectifier or a DC–DC boost converter, while the electric machine's intrinsic stator inductances serve as filter or energy storage elements [7, 8, 9, 56, 58, 63].

However, this integration introduces some challenges; one of those is the unintended generation of electromagnetic torque. If is not properly managed through control actions or splitting machine winding configurations, current ripple can cause the rotor to vibrate or to move while the vehicle is charged [30, 31, 32, 63, 65, 66]. Moreover, because traction motors are typically optimized for low-frequency AC current, the high-frequency current ripples resulting by the switching conversion can induce significant iron losses (hysteresis and eddy currents) and lead temperature rises, restricting the allowable fast-charging duration [8, 9, 56, 63]. The following sections will compile some topologies structures for AC-DC and DC-DC including their control schemes.

2.5.1 AC-DC topologies and control structure

These chargers are typically structured in two main stages. The first stage performs the grid-side AC-DC conversion, which can be implemented using the traction inverter operating as an active front-end (AFE) rectifier [30, 31]. This stage regulates the DC-link voltage and ensures proper current shaping, power factor correction. The second stage consists of a battery-side DC-DC converter, typically implemented as a buck–boost topology, in which the DC-link voltage is regulated to supply the battery with the required charging current and voltage. Some topologies are presented in Figure 2.11.

Control for AFE can be divided into several stages, starting with grid synchronization. This is done by a Phase-Locked Loop (PLL) that can be implemented with a Synchronous Reference Frame PLL (SRF-PLL) or a Second-Order Generalized Integrator (SOGI) . SRF-PLL is widely adopted due to its simplicity and satisfactory performance under balanced and low-distortion grid conditions [67, 68]. SOGI-PLL, on the other hand, provides enhanced filtering capabilities and robustness, making it particularly suitable for automotive charging applications where grid quality cannot always be guaranteed [67, 68], the block diagram for both schemes are presented in Figure 2.12.

For three-phase AC–DC on-board chargers, the front-end stage is commonly implemented as a three-phase active rectifier, which enables bidirectional power flow, high power factor, and low current distortion [6, 9, 69]. The control structure of such converters is organized in a cascaded manner, consisting of an outer DC-link voltage control loop and an inner grid current control loop, both operating based on the grid synchronization provided by the PLL. A broadly adopted approach for current regulation in three-phase rectifiers is the use of PI controllers in the synchronous reference frame (dq). By using the Clarke-Park transformation on the measured grid currents and taking the voltage as the reference frame, the current references become constant in steady state, allowing the use of simple PI controllers. In this scheme, the d-axis current is used to regulate the active power flow and maintain the DC-link voltage, while the q-axis current reference is set to zero to ensure unity power factor operation [6, 9, 69].

Beyond classical linear controllers, model-based and predictive control methods have also been

investigated for three-phase rectifiers in EV charging applications. Techniques such as finite control set model predictive control (FCS-MPC) directly select the optimal switching state based on a cost function that minimizes current error and switching losses [70]. These methods can offer fast dynamic response and multi-objective control capabilities, although at the expense of higher computational requirements.

After the grid-side current has been regulated through the PFC stage, the DC-link voltage serves as the intermediate energy storage between the AC input and the DC–DC stage,

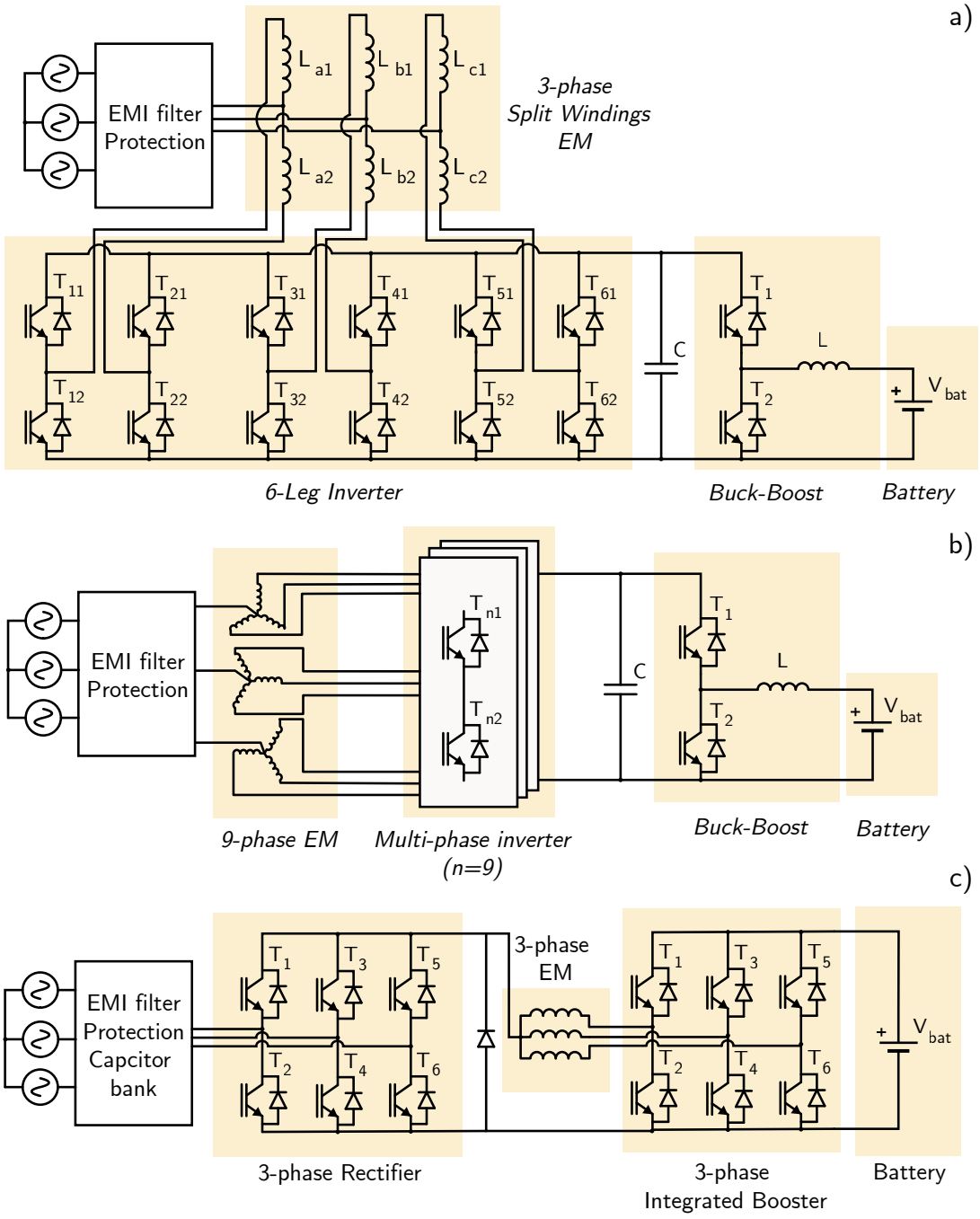

Figure 2.11: AC-DC topologies for integrated chargers

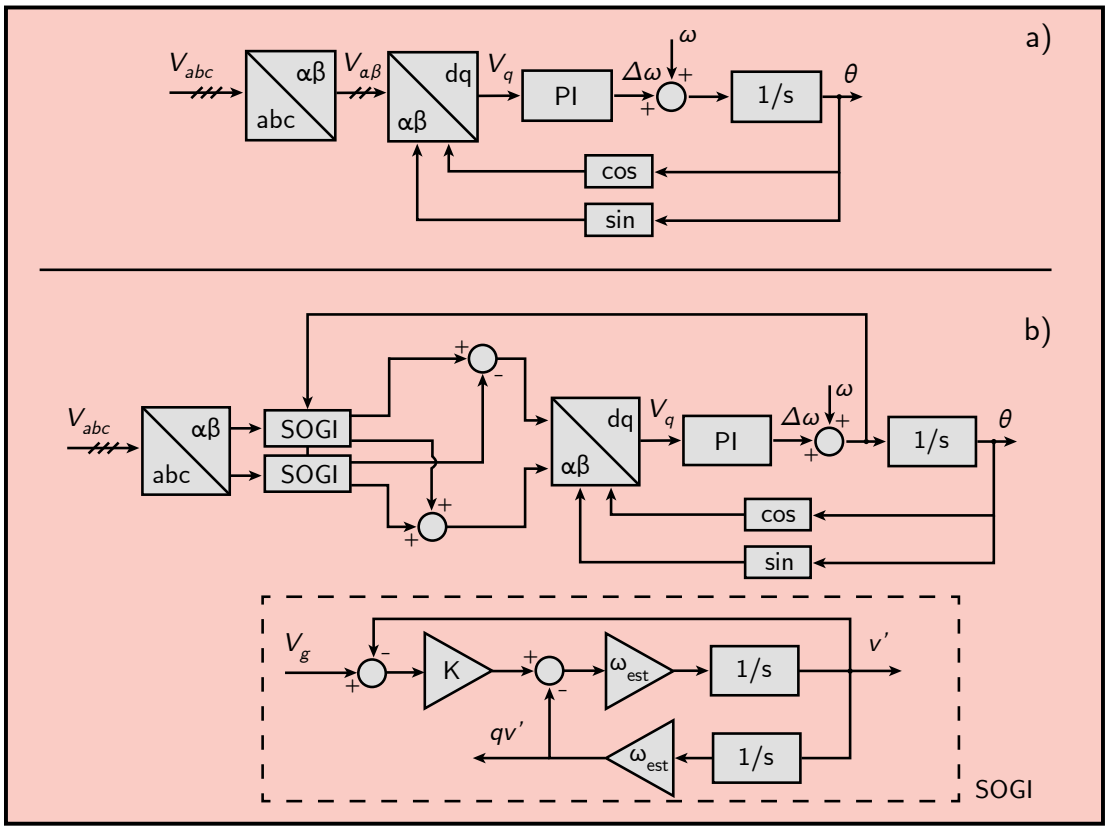

Figure 2.12: PLLs block diagrams a) SRF-PLL b) SOGI-PLL

and it must be maintained at a stable value. A voltage control loop regulates the DC-link voltage and generates a reference for the active power component of the input current (d-axis in the synchronous frame). This outer loop is usually implemented using a PI controller, which adjusts the magnitude of the current reference fed to the inner current control loop [6, 9, 69].

Then, the DC-DC is controlled with a similar cascade approach with a outer voltage loop controls the battery voltage during the charging giving the current reference for the inner loop [6, 9, 69]. Nonetheless the outer voltage loop can be skipped during a part of the charging process; this is explained further in the Section 2.6.

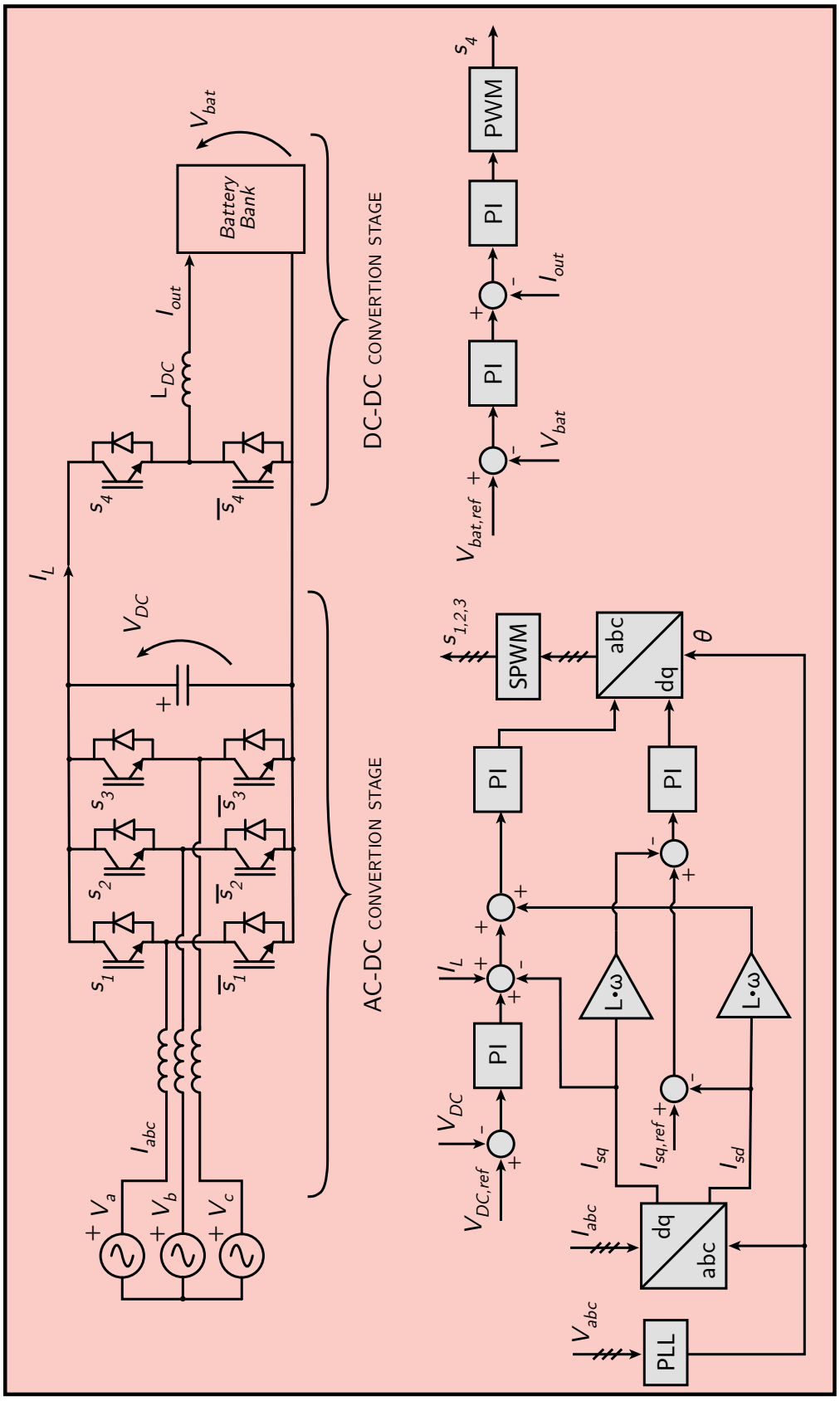

Figure 2.13: Control scheme for AC-DC charging system

2.5.2 DC-DC topologies

Integrated DC/DC chargers are designed to interface directly with a high-voltage DC charging bus, typically at 400 V or 800 V, and adapt this voltage to the requirements of the traction battery without an intermediate AC/DC conversion stage and enabling fast charge [32, 71, 72]. Similarly to the AC-DC chargers, these systems rely on the reconfiguration of the traction inverter and electrical machine to perform DC/DC conversion, using the inverter legs as controllable switches and the machine windings as energy-storage elements [32, 72].

Solutions with access to the motor neutral point utilize the inverter legs and stator windings to form multiphase boost or buck-boost converters [66, 72]. Open-winding machines combined with dual-inverter architectures enable bidirectional DC/DC operation by regulating zero-sequence current paths through the machine inductances while the rotor remains stationary [73, 70]. In addition, dual-wound synchronous machines exploit magnetic coupling between multiple winding sets to extend the achievable voltage conversion range, acting as an isolated transformer or generator during the charging process. Finally, reconfigurable buck/boost and multi-phase converter structures allow for the efficient handling of high charging currents and wide DC bus variations by adjusting the relay or contactor placement to match the specific voltage level of the external source [58].

When the electric machine is integrated into the boost process, it operates as a interleaved converter where the primary control objectives are minimizing current unbalances and ripples across the phases normally achieved with phased-shift PWM [8, 58], some examples are shown in Figure 2.14.

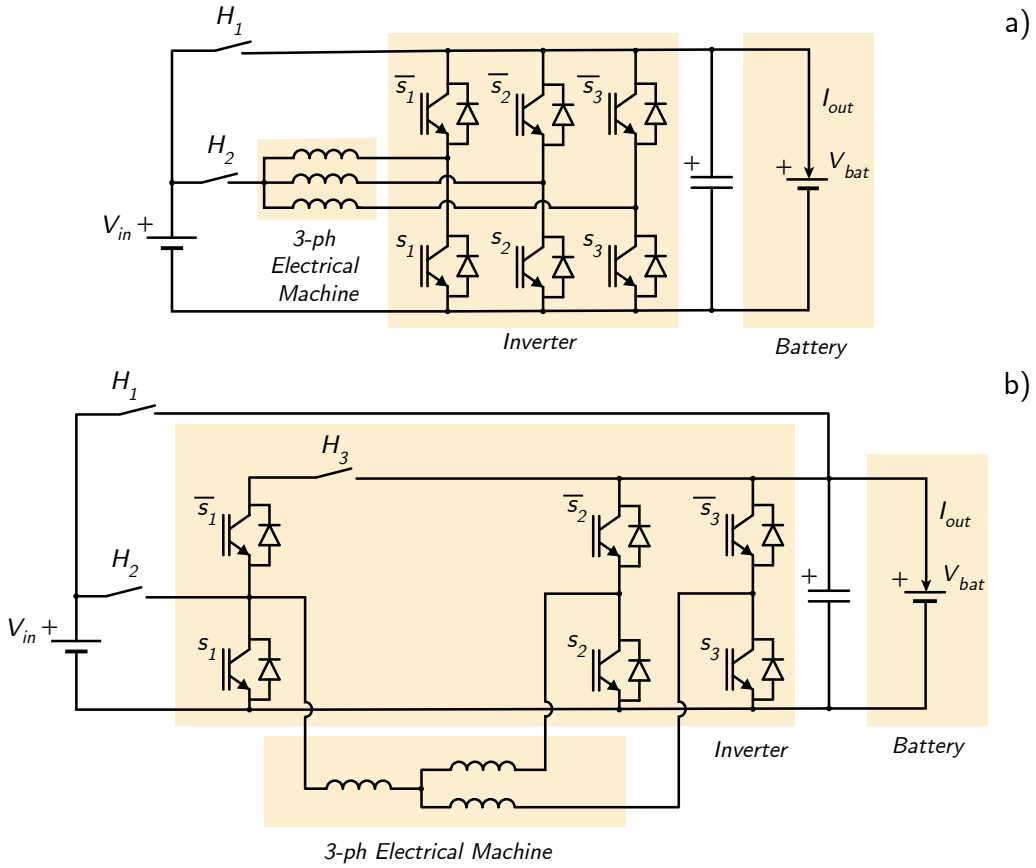

Figure 2.14: DC-DC topologies for integrated chargers

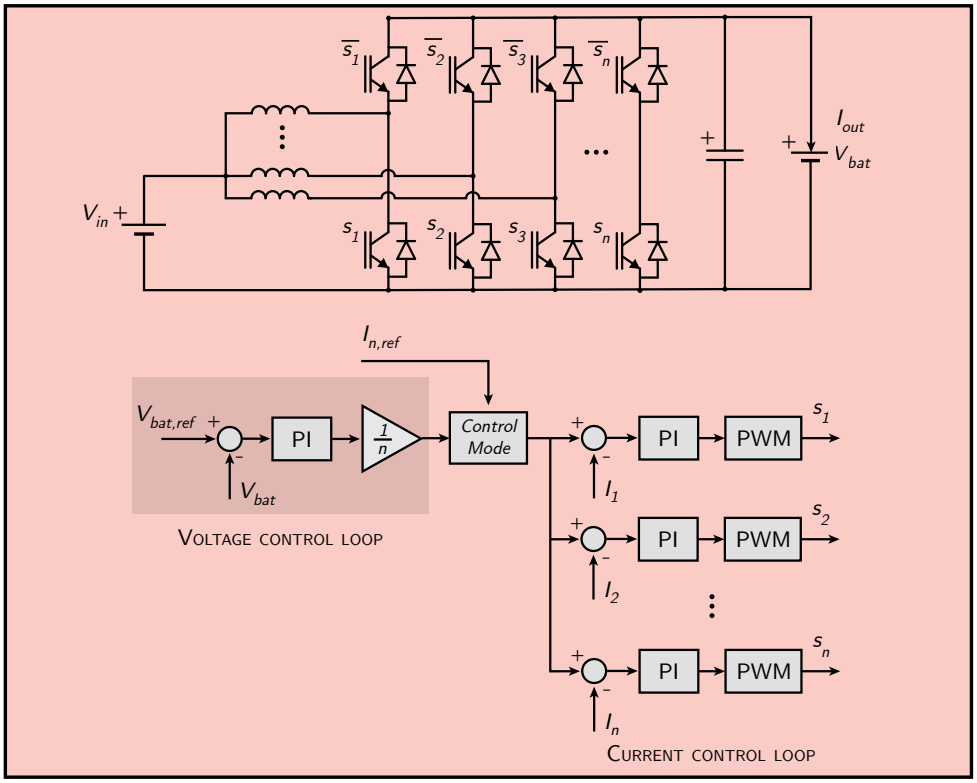

Figure 2.15: Control scheme for DC-DC charging system

2.6 Battery charging phase

Batteries are typically charged in two main phases: Constant Current (CC) and Constant Voltage (CV). During the CC phase, which begins when the battery is at a low state of charge (SoC), the control system maintains a constant current reference equal to the maximum allowable charging current specified by the Battery Management System (BMS) [31, 69]. As the battery voltage approaches a predefined threshold, usually set at 70–80% SoC, the charging controller switches to the CV phase to prevent overcharging and limit thermal stress. In the CV phase, the outer voltage control loop is activated to regulate the battery terminal voltage at its nominal value. The output of this voltage controller provides a dynamic current reference for the inner current loop, resulting in a gradual reduction of the charging current [31, 69].

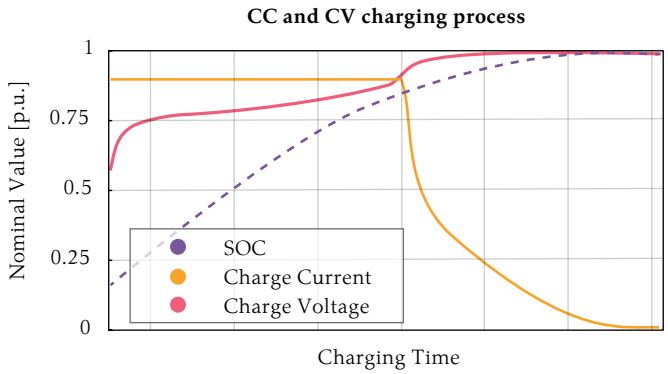

Figure 2.16: CC and CV charging process

2.7 Challenges & Future Directions

The future of EVs charging systems is shaped by the growth of EV adoption, battery development, and the transition toward higher voltage architectures. These developments demand charging solutions capable of delivering higher power with charging times on the order of 10–15 minutes, but being at the same time compatible with grid constraints, renewable energy integration, and emerging smart-grid functionalities. As a result, future charging infrastructures are expected to evolve toward bidirectional, intelligent, and digitally managed system [4, 6, 69, 74].

To meet these requirement, charging systems faces several challenges involving interdisciplinary work like:

- **Efficiency at high power levels:** High-power chargers aim to reach currents that can exceed 1 kA, resulting in significant conduction losses in both transmission and conversion stages. New semiconductor technologies based on SiC and GaN aim to reduce the losses associated with traditional silicon switches, together with new converter topologies that enable soft switching, resonant operation, or partial power processing [6, 56, 74].
- **Thermal management:** Higher currents lead to increased heat dissipation, which must be properly handled to avoid the risk of thermal runaway in the batteries during charging and to ensure system longevity. As a result, forced air convection is often insufficient, making liquid cooling solutions necessary [6, 74, 75].
- **Power density and compactness:** Chargers, and in particular on-board systems, face strict space and weight limitations that compete with vehicle cargo and passenger space. To address this, a common strategy is to increase the switching frequency to the range of 100 kHz to MHz, allowing the use of smaller inductors and transformers. Additionally, planar magnetics and matrix transformers enable low-profile designs that help increase the power density of charging units. However, increasing the operating frequency also increases switching losses and, consequently, the thermal requirements [6, 30, 31, 74].
- **Reliability:** Chargers must remain stable despite grid disturbances, such as unbalanced AC grids or voltage sags, which can deteriorate power quality. Converters based on modular or multilevel topologies must incorporate fault-tolerant architectures that enable bypassing faulty cells and ensure continuous operation. Moreover, the integration of bidirectional power flow must account for battery ageing and degradation due to increased cycling and power discharge events [6, 69].
- **Standards compliance:** The current standard landscape is fragmented, with different standards applied across regions, complicating the development of universal charging solutions for manufacturers. Additionally, the transition from 400 V to 800 V battery systems poses challenges, and as voltage levels continue to increase, chargers must be capable of adapting their output voltage over a wide range. Finally, standards such as IEC 61851-23 require galvanic isolation, whereas transformerless converters can achieve higher efficiency and lower cost, creating a trade-off between safety compliance and converter performance [6, 56, 69, 76].

Integrated on-board chargers present challenges that distinguish them from conventional standalone charging solutions.

- One of the primary concerns is galvanic isolation, which is generally required to comply with safety standards. However, implementing isolation in integrated charger architectures often requires bulky transformers or additional high-frequency isolated stages, reducing the benefits of integration. As a result, non-isolated solutions must rely on common-mode voltage control strategies to mitigate leakage currents [9, 56].

- Another issue is EMI, as high-frequency switching can generate common-mode currents that propagate through the vehicle powertrain. Although existing studies focus on predicting common-mode currents in single-vehicle systems to prevent nuisance tripping of leakage protection devices, closely related to this, limited attention has been given to scenarios where multiple EV chargers operate from a common DC bus, in which interactions between converters may influence common-mode currents and EMI behavior [6, 73, 74, 76].
- As discussed before, thermal coupling between the traction inverter and motor adds limitations, as high-frequency currents increase winding and core losses, potentially elevating rotor temperatures and limiting charging power or duration [8, 9, 56, 63].
- From a control perspective, integrated chargers require carefully designed control algorithms to manage hardware reconfiguration and ensure zero average electromagnetic torque during charging, while maintaining balanced phase currents and enabling smooth transitions between operating modes [31, 65, 69, 70, 72].
- Additional gaps exist in electric machine design optimization, as most traction motors are primarily designed for propulsion, with limited investigation into materials, winding layouts, or magnetic designs optimized for charging operation [58]. Additionally, integrated charging solutions based on Electrically Excited Synchronous Machines (EESM), Synchronous Reluctance Machines (SynRM), and Switched Reluctance Motors (SRM) remain underexplored, particularly concerning magnetic saturation, vibration, and acoustic noise [9, 32, 66].

Chapter 3

Methodology

This chapter defines the thesis workflow, including the activities executed in each phase. It then describes the experimental system, including schematics and diagrams indicating the components' interconnections, as well as how the tests were performed. After that, the main signal quantities used to evaluate the performance of each configuration are presented. Finally, methods for calculating losses in experimental tests and simulations are presented.

3.1 Thesis workflow

The work of this thesis focus on the obtention of experimental results for the efficiency and losses of an integrated fast charger. The main steps are shown in Figure 3.1 and listed below:

- The work begins with a pre-study phase, where a review of existing topologies for integrated fast charger systems is conducted to identify the motivations and requirements for the proposed solution. Based on this, preliminary simulations are carried out to estimate voltage and current levels under nominal operating conditions. These results are then used to define the main system components (stator, electric machines, inverter, power supply, and load) and the operating conditions for all tests.
- The test bench setup phase involves the preparation of electrical schematics and the definition of the physical layout of the system, including the placement of the power supply, inverter, and load. Custom cables are assembled to ensure proper electrical connections according to the test configurations, and measurement instruments (e.g., oscilloscope probes) are installed following the defined schematics.
- The experimental testing phase is initiated under low-voltage and low-current conditions to verify correct system operation and ensure safe functionality. Once validated, the operating conditions are adjusted to perform comparative tests, including topology changes, switching frequency sweeps and phase-shift variation.
- In the post-processing phase, main electrical quantities such as input and output power, inverter losses, EM losses, and winding currents among others are filtered and processed to evaluate overall system efficiency, as well as the individual efficiencies of the electric machine and inverter. This enables a detailed breakdown of system losses.
- Finally, an analysis phase is conducted in which the performance of the evaluated topologies is compared, with particular focus on current characteristics within the converter. This phase concludes with the main findings of the study, providing insights into the integration and performance of the proposed fast-charging system.

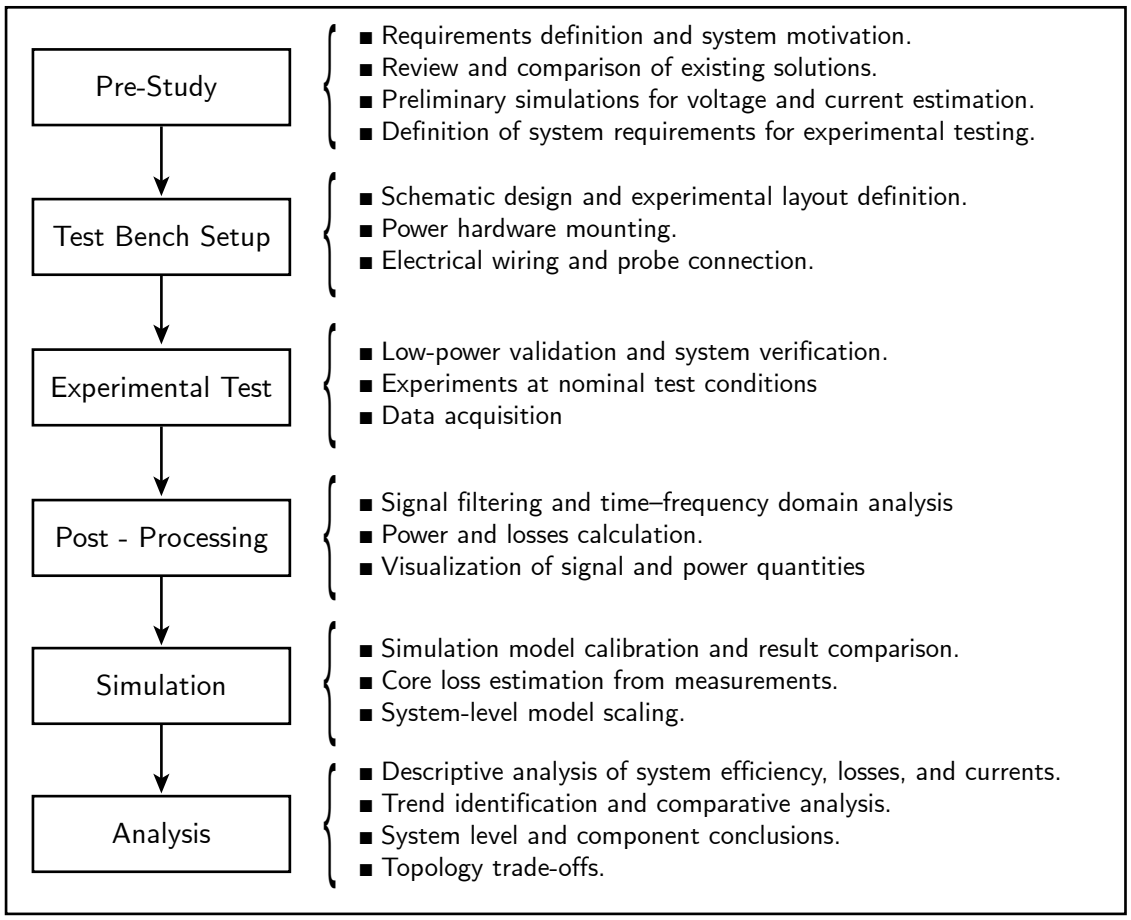

Figure 3.1: Thesis workflow

3.2 System Architecture

The system under study consists of an integrated EV charging setup composed of a DC power supply, an inverter, an electric machine (EM), and a load. The inverter used in this work is the CRD300DA12E-XM3, while the DC power supply and regenerative load are implemented using the SM1500 CP-30 bi-derectional power supply. The overall architecture is designed to evaluate efficiency and losses during power transfer operation, while allowing flexibility to switch between different topologies and EM configurations.

The inverter switches operate as the active devices of a boost converter, regulating the current through the stator windings and determining the output voltage. The load is configured to emulate a battery during charging, establishing a voltage level that the converter must overcome. The inverter is connected to a laptop via USB, and the duty cycle is controlled using an open-loop scheme. This setup enables control of the output voltage and, consequently, the amount of power delivered to the regenerative load.

Voltage and current waveforms are captured using probes, recorded, and visualized on an oscilloscope. These signals are then used to determine the loss distribution and overall system efficiency.

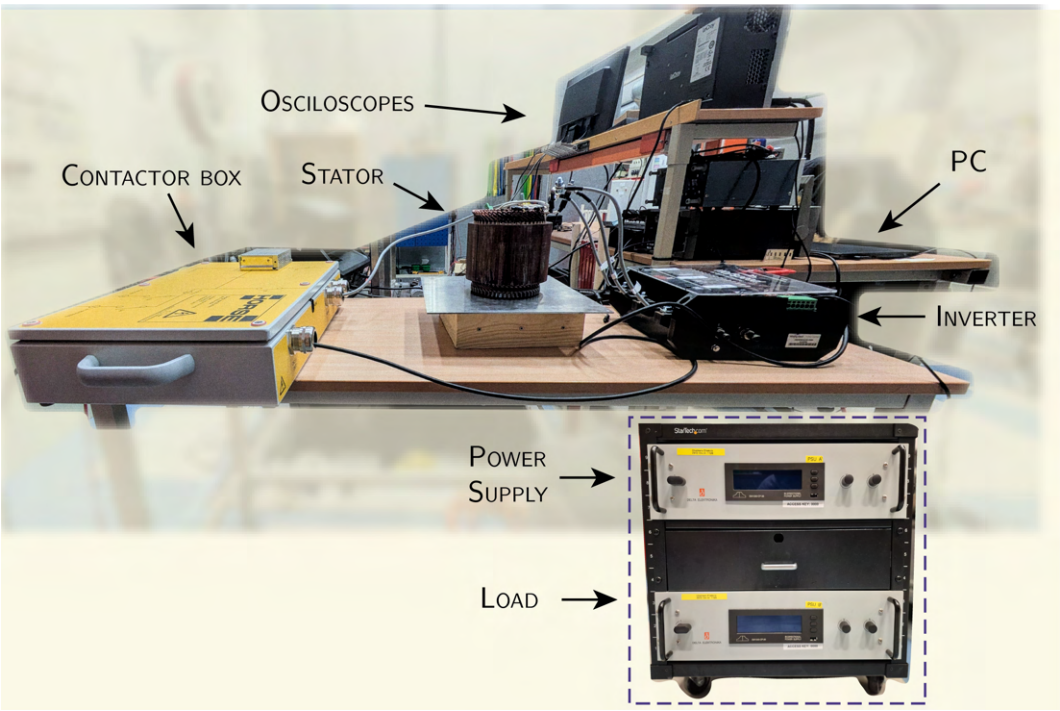

Figure 3.2: Test bench

3.2.1 Topology description and test conditions

Two converter topologies are compared under the same operating conditions and loads. The first topology is based on a three-phase interleaved boost converter, with the three phases connected directly to the input voltage. The second topology connects one of the windings directly to the input, making a two-phase interleaved boost converter. The main differences between the topologies are the current distribution and resulting losses. All the experiments are carried out with $V_{in} = 100\,\text{V}$, $V_{out} = 200\,\text{V}$ and $D = 0.52$.

The experiments begin by using the stator without the rotor as the inductance of the interleaved boost converter. Two sets of experiments are then carried out, considering the two topologies mentioned and shown in Figure 3.6. For each topology, a switching frequency sweep is performed from 10 kHz to 100 kHz in steps of 10 kHz, with the phase shift fixed at its theoretical optimum: 120° for T1 and 180° for T2. These angles correspond to the points at which the cancellation of circulating currents is maximized. In the second set, the phase shift is swept in six steps over the range 0°–120° for T1 and 0°–180° for T2, with the switching frequency fixed at 50 kHz.

Once the stator-only characterization is complete, a PMSM and an EESM, both built with the same stator, are tested. Since the neutral point is not accessible, only Topology 2 can be evaluated (with switching frequency equal to 50 kHz and phase shift equal to 180°). For the PMSM, only one fixed rotor position is tested, as the rotor settles at a fixed equilibrium position upon energization. For the EESM, three rotor positions are considered: an arbitrary reference at 0°, and additional positions at 15° and 30°, taking into account the 45° periodicity determined by the number of poles. Figure 3.3 shows the different connections for each test.

A summary of all the test is presented in Table 3.1.

Table 3.1: Summary of experimental test conditions ($V_{in} = 100V$, $V_{out} = 200V$ and $D = 0.52$).

Test	Topology	f_{sw} (kHz)	Phase shift	Swept variable	Rotor position
Stator only	T1 (3-phase)	10–100	120°	f_{sw}	–
	T1 (3-phase)	50	0°–120°	Phase shift	–
	T2 (2-phase)	10–100	180°	f_{sw}	–
	T2 (2-phase)	50	0°–180°	Phase shift	–
PMSM	T2 (2-phase)	50	180°	–	Fixed (0°)
EESM	T2 (2-phase)	50	180°	–	0°
	T2 (2-phase)	50	180°	–	15°
	T2 (2-phase)	50	180°	–	30°

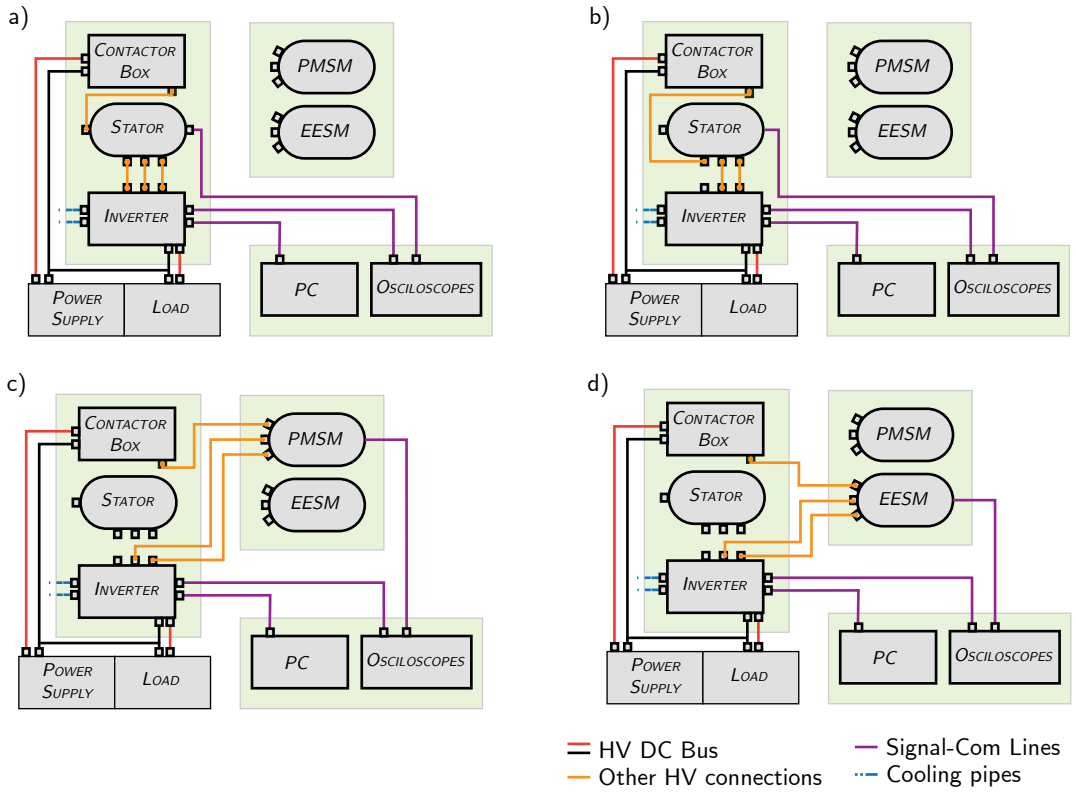

Figure 3.3: Different system connection for test configurations (a) T1 frequency and phase shift sweep, (b) T2 frequency and phase shift sweep, (c) T2 PMSM test, (d) T2 EESM position test

3.2.2 Measurement tools

The measurement tools used in the tests are listed in Table 3.2. The parameters of the CAB450M12XM3 power module are obtained from the manufacturer datasheet [77], while the stator resistance and inductance values are summarized in Tables A.1, A.2, A.3, and A.4.

Table 3.2: Instrumentation

Instrument	Model / Type	Measured Quantity
Fluke 2638A Hydra Series III	Data acquisition system	Stator temperature
LCR8110G	LCR meter	Stator inductance (L), Stator resistance (R)
LeCroy WaveSurfer 24MXs-B	Oscilloscope	Visualization and storage of in/out waveforms
Teledyne LeCroy MDA805A	Oscilloscope	Visualization and storage of phases/inverter waveforms
CP500 Current Probe	Current probe	I_{in}, I_1, I_2, I_3
CP150 Current Probe	Current probe	I_{out}
HVD3206 Differential Voltage Probe	Voltage probe	V_{in}, V_1, V_2, $V_{M,H}$, $V_{M,L}$

3.2.3 Electrical Machines and Stator

The stator used in the test is the same as those built in the PMSM and EESM, as shown in Figure . The position of the rotor is measured with a sticked label on the shaft, as shown in Figure 3.5.

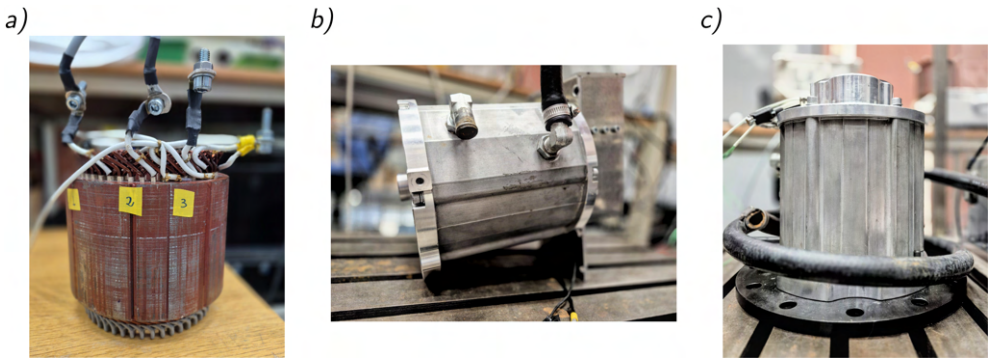

Figure 3.4: Used machines for the test (a) 360V 60 kW EM Stator (b) 360V 60 kW PMSM (c) 360V 60kW EESM

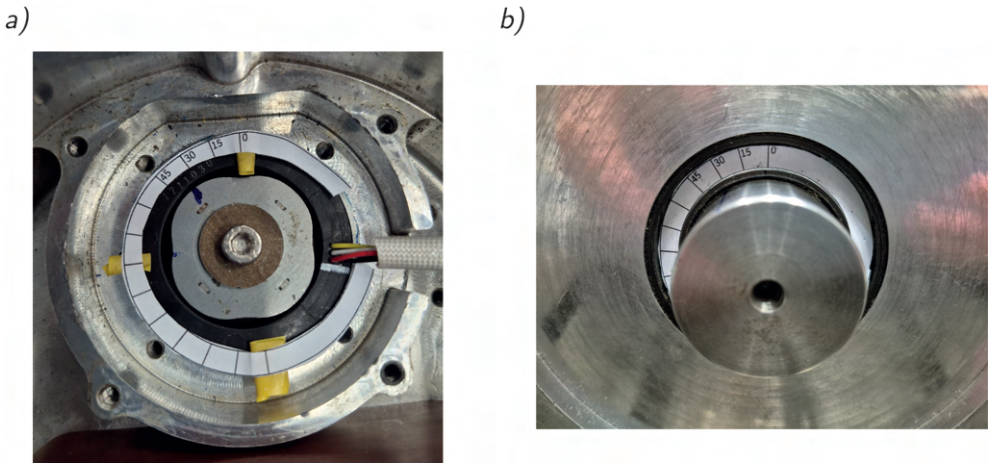

Figure 3.5: Rotor position measurement (a) PMSM shaft (b) EESM shaft

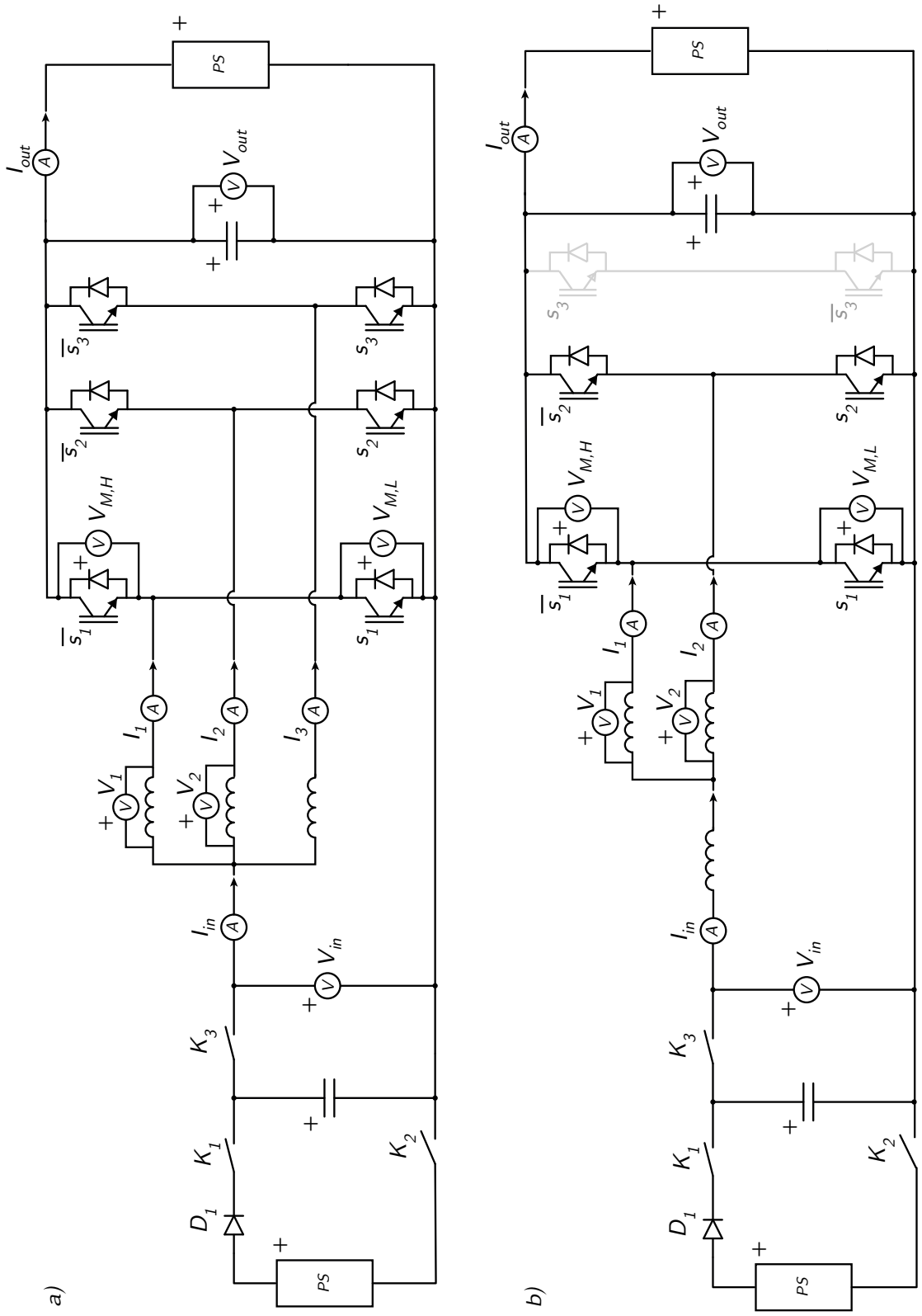

Figure 3.6: Electric schematic for the tested topologies (a) Three phase interleaved booster converter, (b) Two phase interleaved booster converter

3.3 Signal Quantities

The DC component of the current corresponds to the average value over one switching period and is defined as:

$$I_{\mathrm{DC}} = \frac{1}{T} \int_0^T i(t)\, dt \tag{3.1}$$

The RMS value represents the equivalent current that would yield the same power dissipation in a resistive element and is defined as:

$$I_{\mathrm{RMS}} = \sqrt{\frac{1}{T} \int_0^T i^2(t)\, dt} \tag{3.2}$$

For triangular waveforms, the RMS current can be expressed as:

$$I_{\mathrm{RMS}} = \sqrt{I_{\mathrm{DC}}^2 + \left(\frac{\Delta I_{\mathrm{pp}}}{2\sqrt{3}}\right)^2} \tag{3.3}$$

The peak-to-peak current ripple is defined as the difference between the maximum and minimum current values within one switching period:

$$\Delta I_{\mathrm{pp}} = I_{\mathrm{max}} - I_{\mathrm{min}} \tag{3.4}$$

To mitigate the influence of noise during measurements, the current ripple is evaluated in the frequency domain. The current signal is decomposed into its Fourier series, and the RMS value of the n-th harmonic is computed as:

$$I_{n,rms} = \frac{1}{\sqrt{2}} \sqrt{a_n^2 + b_n^2} \tag{3.5}$$

a_n and b_n are the cosine and sine Fourier coefficients of the n-th harmonic. The dominant harmonic is identified as the component with the highest RMS value, excluding the DC component ($n = 0$):

$$n^* = \arg\max_{n \geq 1} \left(I_{n,rms}\right) \tag{3.6}$$

3.4 Power loss model for power MOSFETs

The total power dissipated in a switching MOSFET can be separated into several terms depending on the grade of complexity. For the context of this thesis conduction and switching losses are the most relevant, even though a general model starts from the instantaneous drain-source voltage $V_{DS}(t)$ and drain current $I_D(t)$:

$$p_{M,losses}(t) = V_{DS}(t) \cdot I_D(t) \tag{3.7}$$

Then, the average power over one switching period $T_{sw} = 1/f_{sw}$ is

$$P_{M,losses} = \frac{1}{T_{sw}} \int_{T_{sw}} V_{DS}(t) \cdot I_D(t)\, dt \tag{3.8}$$

Ideal switch waveform can be divided into an on-interval, a turn-on transition and turn-off transition, expanding the integral expressed in Eq. 3.8 into conduction and switching losses as:

$$P_{M,losses} = \frac{1}{T_{sw}} \left[\underbrace{\int_{T_{cond}} V_{DS}(t) \cdot I_D(t)\, dt}_{P_{M,cond}} + \underbrace{\int_{T_{on}} V_{DS}(t) \cdot I_D(t)\, dt + \int_{T_{off}} V_{DS}(t) \cdot I_D(t)\, dt}_{P_{M,sw}} \right] \tag{3.9}$$

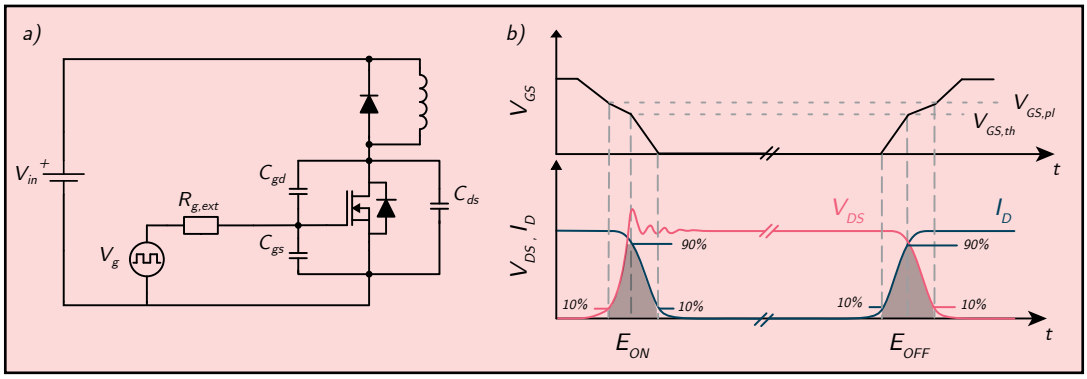

Figure 3.7: Mosfet transient definition (a) MOSFET double pulse test circuit (b) Transient switching waveforms

3.4.1 Conduction Losses

During the on-state the MOSFET conducts with a small voltage drop caused by the on-resistance. The drain-source voltage is [78]:

$$V_{DS}(t) = I_D(t) \cdot R_{DS,on} \tag{3.10}$$

With $R_{DS,on}$ assumed constant over the conduction interval. Substituting Eq. (3.10) into (3.9):

$$P_{M,cond} = \frac{1}{T_{sw}} \int_{T_{cond}} I_D^2(t) \cdot R_{DS,on}\, dt \tag{3.11}$$

It is important to remark that $R_{DS,on}$ increases the MOSFET junction temperature, so this dependency need to be included into a thermal model for long run estimations.

3.4.2 Switching Losses

By taking the $P_{M,sw}$ expression from Eq.(3.9), the turn-on and off time can be expressed as the rising and falling time for voltage and current. A common approximation used in literature, models the energy dissipated during a switching interval as a triangular waveform, assuming one quantity remains approximately constant throughout the transition [78]:

$$E_{on} = \frac{1}{2} \cdot V_{DS} \cdot I_D \cdot (t_{r,i} + t_{f,v}) \tag{3.12}$$

$$E_{off} = \frac{1}{2} \cdot V_{DS} \cdot I_D \cdot (t_{r,v} + t_{f,i}) \tag{3.13}$$

Then, the switching losses are averaged multiplying the energy losses times the switching frequency. This is a general expression used in both simulation and experiments:

$$P_{M,sw} = (E_{on} + E_{off}) \cdot f_{sw} \tag{3.14}$$

3.4.3 Extended Loss Model

The model presented in Eq.(3.9) omits some losses contributions that might be relevant in specific topologies or operation modes.

1. **Gate drive losses:** Each switching cycle, the gate capacitance must be charged to V_{GS} and discharged back to zero. The energy supplied by the gate driver per cycle is $Q_g \cdot V_{GS}$, and the associated average power is [78]:

$$P_{M,gate} = Q_g \cdot V_{GS} \cdot f_{sw} \tag{3.15}$$

   If the gate driver is supplied by a dedicated auxiliary power supply that is galvanically separated from the main power path, $P_{M,gate}$ does not contribute the converter's power stage efficiency and may be excluded from the loss calculation.

2. **Body diode conduction:** In bridge topologies, a dead time t_{dt} is inserted between the turn-off of one switch and the turn-on of its complementary switch to prevent short circuit. During t_{dt}, the load current freewheels through the MOSFET body diode at its forward voltage V_F, typically 0.7–1.2 V for silicon MOSFETs [78]:

$$P_{M,body} = V_F \cdot I_D \cdot t_{dt} \cdot f_{sw}, \tag{3.16}$$

3. **Reverse-recovery:** During turn-off, stored minority carriers in the body diode produce a reverse-recovery charge $Q_{rr} = \frac{1}{2} \cdot I_{rr} \cdot t_{rr}$, which must be swept out by the commutating switch, adding an average power loss of [78, 79]:

$$P_{M,rr} = Q_{rr} \cdot V_{DC} \cdot f_{sw}. \tag{3.17}$$

4. **Output capacitance.** The nonlinear output capacitance $C_{oss}(v_{\mathrm{DS}})$ stores energy as V_{DS} rises during turn-off. At hard turn-on, this energy is discharged through $R_{DS,on}$, constituting a loss that scales quadratically with bus voltage [78]:

$$P_{M,C_{oss}} = \frac{1}{2} \cdot C_{oss}^{\mathrm{eff}} \cdot V_{DC}^2 \cdot f_{sw}, \tag{3.18}$$

3.5 Power loss model for magnetic components

Losses in a magnetic component can be separated as:

$$P_{EM,losses} = P_{EM,cu} + P_{EM,core} \tag{3.19}$$

3.5.1 Copper Losses

Copper losses refer to the power dissipated in the winding conductors due to the Joule effect. Since the inductor current contains both a DC component and an AC ripple component, each contributes differently to the total loss, as higher frequency increases the effective resistance seen by the AC component (Skin effect [80]):

$$P_{EM,cu} = P_{EM,cu}^{DC} + P_{EM,cu}^{AC} \tag{3.20}$$

The DC copper loss is calculated from the DC current component and the winding DC resistance [80]:

$$P_{EM,cu}^{DC} = I_{EM,DC}^2 \cdot R_{EM,DC} \tag{3.21}$$

The AC copper loss accounts for skin and proximity effects, both of which increase the effective winding resistance with frequency [81]. The total AC loss is therefore evaluated as a sum over the relevant frequency components:

$$P_{EM,cu}^{AC} = P_{EM,\text{skin}} + P_{EM,\text{prox}} \tag{3.22}$$

$$P_{EM,cu}^{AC} = \sum_f I_{L,AC}^2(f) \cdot R_{L,AC}(f) \tag{3.23}$$

3.5.2 Core losses

Core losses arise refer as the losses generated by the variation of the magnetic flux through a magnetic material [81]. From the induction there are two main contributors the hysteresis and eddy currents.

$$P_{EM,core} = P_{EM,core}^{eddy} + P_{EM,core}^{hyst} \tag{3.24}$$

Hysteresis losses is generated from the work required to repeatedly reorient magnetic domains against internal material forces during each magnetization cycle. Because these processes are irreversible, part of the energy supplied is dissipated as heat. The dissipated energy corresponds to the area enclosed by the B–H loop, which represents the energy lost per unit volume in one cycle. When the excitation is periodic, the total loss scales with the frequency and with the extent of domain excursion, which is related to the peak flux density. This loss is therefore commonly approximated as [81, 82]:

$$P_{EM,core}^{hyst} = K_h \cdot f_s \cdot \Delta B^2 \cdot V_c \tag{3.25}$$

Eddy current losses in the iron are generated from currents by a time-varying magnetic flux, according to Faraday's law. These circulating currents flow in closed loops perpendicular to the flux, leading to Joule (ohmic) dissipation. A faster change in flux density increases the induced electric field, thereby driving stronger currents, while a larger flux excursion increases the magnitude of the induced voltages. As a result, the losses scale with the square of both the excitation frequency and the peak flux density. This loss is therefore commonly approximated as [81, 82]:

$$P_{EM,core}^{eddy} = K_c \cdot f_s^2 \cdot \Delta B^2 \cdot V_c \tag{3.26}$$

In real magnetic materials, hysteresis and eddy current losses occur simultaneously and are difficult to separate under arbitrary excitation. Instead, their combined effect is captured through the empirical Steinmetz equation, which relates the total dissipated power to the frequency and amplitude of the flux density [81, 80]:

$$P_{EM,core} = K \cdot f_s^{\alpha} \cdot \Delta B^{\beta} \cdot V_c, \tag{3.27}$$

k, α, and β are material-dependent parameters that implicitly account for the underlying loss mechanisms and are obtained from experimental characterization.

3.6 Experimental Losses and Efficiency Calculation

The system efficiency is defined as:

$$\eta_{system} = \frac{P_{out}}{P_{in}} \tag{3.28}$$

The input and output powers are calculated from voltage and current measurements as:

$$P_{in} = \frac{1}{T}\int_0^T V_{in}(t) \cdot I_{in}(t)\, dt \tag{3.29}$$

$$P_{out} = \frac{1}{T}\int_0^T V_{out,DC} \cdot I_{out}(t)\, dt \tag{3.30}$$

The inverter efficiency is defined as:

$$\eta_{inv} = 1 - \frac{P_{inv,losses}}{P_{in}} \tag{3.31}$$

The power dissipated in the inverter is estimated from measurements on a single leg and then scaled by the number of active legs ($n_{leg} = 3$ for T1, $n_{leg} = 2$ for T2):

$$P_{inv,losses} = (P_{inv,cond} + P_{inv,sw}) \cdot n_{leg} \tag{3.32}$$

$$\begin{aligned} P_{inv,sw} = \frac{1}{T}\Bigg[&\int_{T_{on,H}} V_{M,H}(t) \cdot I_1(t)\, dt + \int_{T_{off,H}} V_{M,H}(t) \cdot I_1(t)\, dt \\ &+ \int_{T_{on,L}} V_{M,L}(t) \cdot I_1(t)\, dt + \int_{T_{off,L}} V_{M,L}(t) \cdot I_1(t)\, dt \Bigg] \end{aligned} \tag{3.33}$$

$$P_{inv,cond} = \frac{1}{T}\left[\int_{T_{cond,H}} R_{ds,on} \cdot I_1^2(t)\, dt + \int_{T_{cond,L}} R_{ds,on} \cdot I_1^2(t)\, dt \right] \tag{3.34}$$

The EM efficiency is defined as:

$$\eta_{EM} = 1 - \frac{P_{losses,EM}}{P_{in}} \tag{3.35}$$

The electrical machine (EM) losses, limited to the stator contribution, are obtained from the power balance:

$$P_{losses,EM} = P_{in} - P_{out} - P_{losses,inv} \tag{3.36}$$

Additionally, the copper losses are calculated directly from the phase currents and resistances:

$$P_{EM,cu} = P_{EM,cu}^{DC} + P_{EM,cu}^{AC} \tag{3.37}$$

$$P_{EM,cu}^{DC} = I_{DC,1}^2 \cdot R_{DC,1} + I_{DC,2}^2 \cdot R_{DC,2} + I_{DC,3}^2 \cdot R_{DC,3} \tag{3.38}$$

$$P_{EM,cu}^{AC} = \sum_f \left(I_{AC,1}^2(f) \cdot R_{AC,1}(f) + I_{AC,2}^2(f) \cdot R_{AC,2}(f) + I_{AC,3}^2(f) \cdot R_{AC,3}(f) \right) \tag{3.39}$$

The rest of the losses according to Eq. (3.19) are reffered as core losses.

3.7 Simulation Losses and Efficiency calculation

To determine the losses in the simulation model, the MOSFET losses and EM losses are calculated separately, considering the current waveforms obtained from the experiments.

3.7.1 MOSFET SPICE simulation

In SPICE simulations, the MOSFET losses are evaluated directly from the instantaneous power defined in Eq. (3.7). The average dissipated power is then obtained numerically following Eq. (3.8). In practice, this is implemented by integrating the waveform over selected time intervals.

Consistently with the decomposition in Eq. (3.9), the total loss is separated into:

- **Conduction losses** $P_{M,cond}$, computed by integrating $p_{M,losses}(t)$ during the on-state interval T_{cond}, which is equivalent to Eq. (3.11).
- **Switching losses** $P_{M,sw}$, computed by integrating $p_{M,losses}(t)$ over the turn-on (T_{on}) and turn-off (T_{off}) transients, corresponding to the energy terms E_{on} and E_{off} used in Eq. (3.14).

3.7.2 Power loss model in ANSYS Maxwell

In ANSYS Maxwell for 2D simulations, the losses in magnetic components are computed directly from the electromagnetic field solution. Following the definition in Eq. (3.19), the copper losses are referred to as solid losses in Maxwell's terminology.

Solid losses are calculated from the current density distribution $\mathbf{J}(\mathbf{r}, t)$. The instantaneous volumetric power density is given by Joule's law, considering the material conductivity σ:

$$p_{\text{solid}}(\mathbf{r}, t) = \frac{|\mathbf{J}(\mathbf{r}, t)|^2}{\sigma} \tag{3.40}$$

The total average solid loss is obtained by integrating over the conductor volume V and over one switching period T_{sw}:

$$P_{\text{solid}} = \frac{1}{T_{sw}} \int_{T_{sw}} \int_V \frac{|\mathbf{J}(\mathbf{r}, t)|^2}{\sigma} \, dV \, dt \tag{3.41}$$

For the Electrical Steel model, Maxwell uses the three-term Bertotti loss separation formula, which separates the total core loss into hysteresis, classical eddy current, and excess (anomalous) contributions:

$$P_{\text{core}} = P_{\text{hys}} + P_{\text{eddy}} + P_{\text{exc}} \tag{3.42}$$

with:

$$P_{\text{hys}} = \int_{V_c} K_h \cdot f \cdot \Delta B^2 \, dV \tag{3.43}$$

$$P_{\text{eddy}} = \int_{V_c} K_c \cdot f^2 \cdot \Delta B^2 \, dV \tag{3.44}$$

$$P_{\text{exc}} = \int_{V_c} K_e \cdot f^{1.5} \cdot \Delta B^{1.5} \, dV \tag{3.45}$$

where K_h, K_c, and K_e are the hysteresis, eddy current, and excess loss coefficients, respectively.

3.8 System Scaling Methodology

The objective of the scaling method is to estimate the copper, core, and inverter losses of each converter topology at the nominal operating point. The methodology combines FEM simulations in ANSYS Maxwell, circuit simulations in PLECS, physical measurements, and analytical loss models. The method is summarised in the following steps:

1. The FEM machine model, including stator and rotor where it corresponds, is simulated in ANSYS Maxwell at several DC current levels to obtain the phase inductance as a function of current, $L(I_{DC})$, capturing the effect of magnetic saturation on the phase windings.

2. The same FEM model is excited with a 1 A_{rms} sinusoidal current at multiple frequencies to extract the frequency dependent winding resistance $R_{AC}(f)$ from the simulated solid conductor losses. The DC resistance R_{DC} is extracted at zero frequency from the same simulation. Both values are corrected by a end winding and temperature factor to account for the resistivity increase at the expected operating temperature.

3. The inductance profiles from Step 1 are used in the circuit simulation ran in PLECS. Both topologies are simulated under different operation points obtaining the current waveforms and MOSFET losses used to make the inverter loss look-up table, in addition to, identify the current ripple amplitude later used for the machine loss calculations.

4. The Steinmetz exponents α and β of the core loss model are extracted by fitting the eddy current and hysteresis loss components obtained from ANSYS Maxwell across a matrix of ripple current amplitudes and switching frequencies, as detailed in Section 3.8.2. The fitted exponents are then used to extrapolate core losses from a physically measured reference point to the nominal operating conditions.

5. Copper losses are computed independently from the frequency-dependent winding resistances and the harmonic decomposition of the scaled phase currents, as detailed in Section 3.8.1.

Steps 4 and 5 are independent of each other and are done once the ripple current scaling from Step 3 is established. Both topologies share the same stator and resistance data extracted in Steps 1 and 2, with differences in the current distribution and ripple waveforms that depend on the topology and the operating point.

3.8.1 Copper Loss Scaling

The total copper loss at the nominal operating point is computed from the frequency-dependent winding resistances extracted from ANSYS Maxwell and the harmonic decomposition of the scaled phase currents. The DC and AC contributions are evaluated separately considering Eqs. (3.38) and (3.39):

$$P_{EM,cu}^{DC} = I_{DC,1}^2 \cdot R_{DC,1} + I_{DC,2}^2 \cdot R_{DC,2} + I_{DC,3}^2 \cdot R_{DC,3}$$
$$P_{EM,cu}^{AC} = \sum_f \left(I_{AC,1}^2(f) \cdot R_{AC,1}(f) + I_{AC,2}^2(f) \cdot R_{AC,2}(f) + I_{AC,3}^2(f) \cdot R_{AC,3}(f) \right)$$

The AC resistance $R_{AC}(f)$ is obtained by interpolating the ANSYS Maxwell results shown in

Figure A.1 at each harmonic frequency present in the current spectrum. Since the $1\,\mathrm{A_{rms}}$ sinusoidal excitation produces a linear solid-loss result, the resistance is extracted directly as:

$$R_{AC}(f) = \frac{P_{solid}(f)}{1\,\mathrm{A_{rms}}^2} \tag{3.46}$$

The phase current ripple is scaled from a reference point (V_{ref}, D_{ref}, $f_{\mathrm{sw,ref}}$, L_{ref}) where the ripple amplitude is known from the PLECS circuit simulation. The scaling follows from the inductor current equation:

$$\Delta I_{pp}(V_{in}, f_{sw}, D, L) = \Delta I_{pp,ref} \cdot \frac{V_{in}}{V_{\mathrm{ref}}} \cdot \frac{D}{D_{\mathrm{ref}}} \cdot \frac{f_{\mathrm{sw,ref}}}{f_{sw}} \cdot \frac{L_{\mathrm{ref}}}{L(I_{DC})} \tag{3.47}$$

where $L(I_{DC})$ is the saturation dependent inductance evaluated at the nominal DC current, obtained by interpolating the ANSYS Maxwell magnetostatic results from Step 1. The scaled RMS ripple current is then decomposed into its harmonic components to evaluate Eq. (3.39).

3.8.2 Core Loss Scaling

Core losses at the nominal operating point are estimated by scaling the Steinmetz model from a reference operating point (f_1, I_1) to the target point (f_2, I_2). The Steinmetz model expresses core loss as a function of flux density B and frequency f:

$$P_{\mathrm{core}} = k \cdot f^{\,\alpha} \cdot B^{\,\beta}$$

At the target operating point, the machine experiences significant magnetic saturation due to high DC current, reducing the phase inductances. However, the AC ripple has a small amplitude compared to the DC bias, limiting flux variation to a narrow region around the DC operating point. So, the flux density varies proportionally to ripple current amplitude:

$$\Delta B \propto \Delta I_{pp} \tag{3.48}$$

This allows the Steinmetz model to be expressed in terms of the ripple current directly as:

$$\frac{P_{\mathrm{core},2}}{P_{\mathrm{core},1}} = \frac{f_2^{\alpha} \cdot B_2^{\beta}}{f_1^{\alpha} \cdot B_1^{\beta}} \propto \frac{f_2^{\alpha} \cdot I_2^{\beta}(V_{in}, f_{sw}, D, L)}{f_1^{\alpha} \cdot I_1^{\beta}(V_{in}, f_{sw}, D, L)} \tag{3.49}$$

The Steinmetz exponents α and β are extracted from ANSYS Maxwell simulations by sweeping the ripple current amplitude and switching frequency independently across the matrix listed in Table A.6. At the switching frequencies considered during the experimental tests, the eddy current losses are dominant over the hysteresis contributions. The exponents are therefore fitted to the eddy current loss component only, yielding a single-term Steinmetz model with exponents $\alpha \approx 1.96$ and $\beta \approx 2$.

3.8.3 Thermal Limit

Figures 3.8 and 3.9 show the stator copper and iron losses from ANSYS Maxwell simulations under traction operation. The shaded region marks the continuous operating area, where the machine can sustain continuous operation thermally. A total loss limit of $P_{\mathrm{th}} = 1.8\,\mathrm{kW}$ defines the thermal boundary for continuous charging.

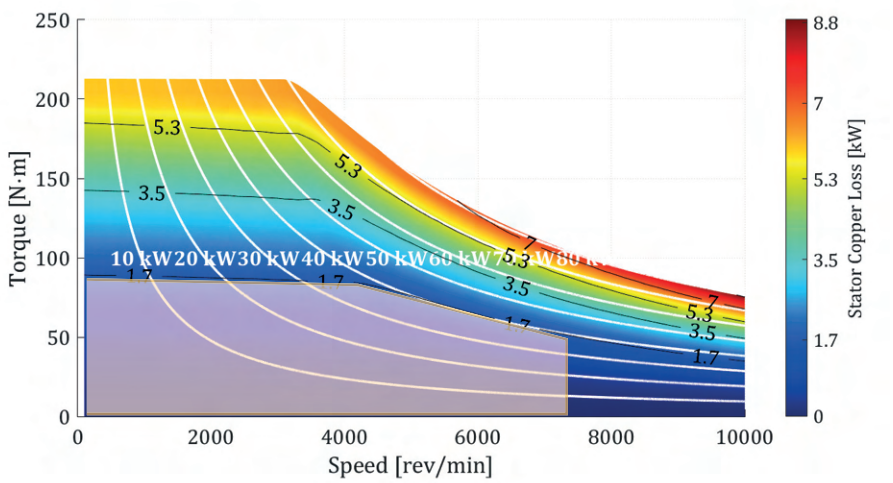

Figure 3.8: Stator copper losses as a function of operating point, obtained from ANSYS Maxwell. The shaded area indicates the continuous operating region.

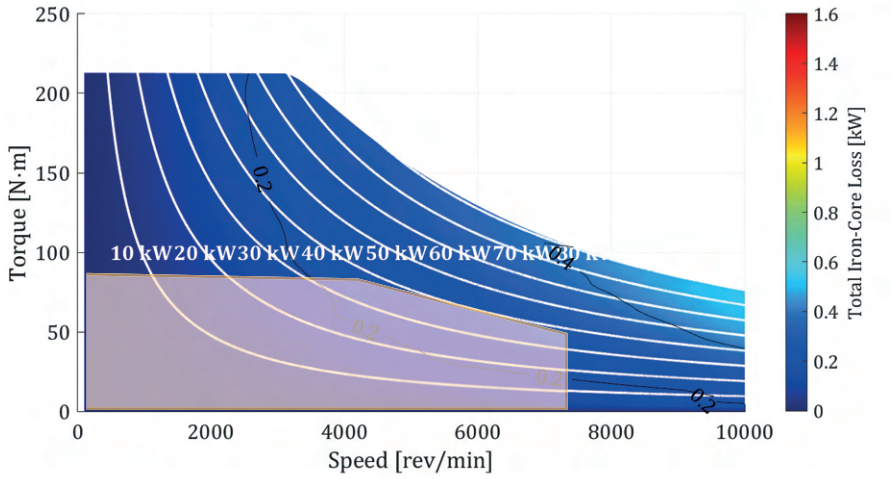

Figure 3.9: Stator iron losses as a function of operating point, obtained from ANSYS Maxwell. The shaded area indicates the continuous operating region.

3.8.4 Modelling Assumptions

The scaling methodology described relies on the following simplifying assumptions:

1. **Harmonic truncation:** The AC ripple current is approximated as a triangular waveform and decomposed into its 1st, 3rd, and 5th odd harmonics only. These three components capture the majority of the signal energy.

2. **Small-ripple linearity for core loss:** The AC ripple amplitude is small; so it is considered that the permeability is approximately constant at a certain input DC current. This justifies the proportionality $\Delta B \propto \Delta I_{\text{ripple}}$ used in the core loss scaling of Eq. (3.49).

3. **DC bias has negligible effect on core loss:** The ANSYS Maxwell simulation matrix in

Table A.6 includes a sweep of DC current at fixed ripple amplitude and switching frequency (Block 2). The eddy current loss remains essentially constant across the full range of I_{DC} values tested, confirming that the DC operating point does not influence the core loss and that the Steinmetz scaling in terms of ripple current alone is sufficient.

4. **Temperature-independent resistances:** The winding resistances R_{DC} and $R_{AC}(f)$ extracted from ANSYS Maxwell are corrected for the end winding length and a single temperature factor applied uniformly across all frequencies. Beyond this correction, the resistances are treated as temperature-independent, and no further variation with operating temperature is accounted for in the copper loss model.

5. **Inverter Loss Mode:** MOSFET switching and conduction losses are calculated using a three dimensional lookup table, interpolated over input voltage, switching frequency, and DC current. The loss data is based on the energy loss characterisation provided by the device manufacturer simulation model, so its accuracy is dependent on these values.

Chapter 4

Interleaved booster analysis

This chapter presents an analytical review of both topologies used in this thesis, starting with the single-phase boost converter and then extending the analysis for the interleaved topologies.

4.1 Single-phase boost converter

A single-phase boost converter for battery charging appliacations, consists of a DC input voltage source V_{in}, a boost inductor L, a controlled switch S, a diode D, an output filter capacitor C, and a battery load represented by a voltage source V_{bat} in series with an internal resistance R_{bat}. The battery as load imposes a voltage at the output terminal, which must be considered for the converter analysis.

During this analysis, the converter is assumed to operate in Continuous Conduction Mode (CCM), meaning the inductor current I_L never reaches zero within a switching period $T = 1/f_{sw}$.

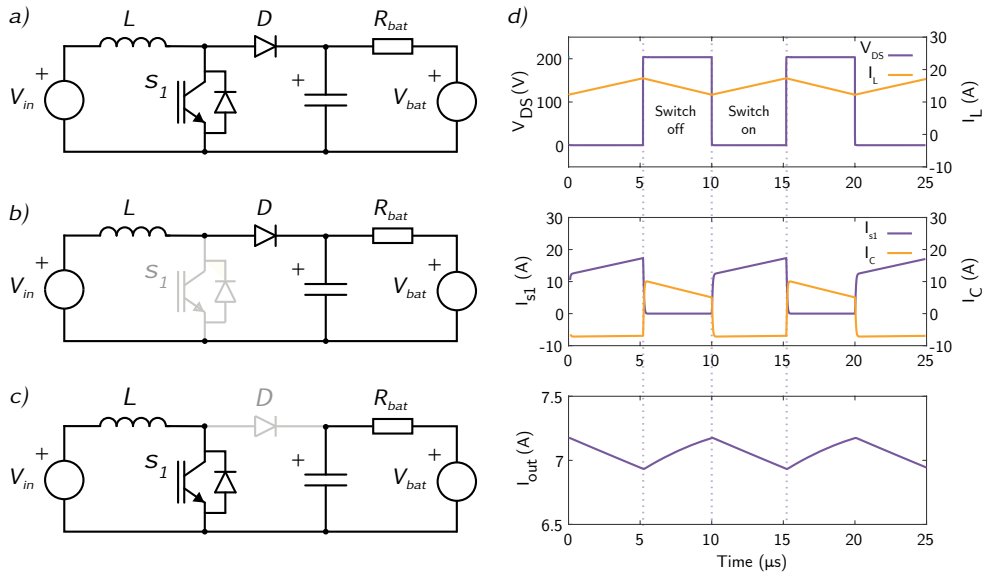

Figure 4.1: Single-phase boost converter (V_{in}=100V, V_{out}=200 V, D=0.52, f_{sw}=100 kHz). (a) Circuit topology, (b) Equivalent circuit during switch-off, (c) Equivalent circuit during switch-on, and (d) Relevant steady-state operating waveforms.

a) Switch-on interval ($0 \leq t < d \cdot T$)

When the switch S is turned on, the diode D is blocking and the input voltage V_{in} is applied directly across the inductor L. The inductor current increases linearly:

$$V_L = V_{in}, \qquad \frac{dI_L}{dt} = \frac{V_{in}}{L} > 0 \tag{4.1}$$

During this interval, the inductor is decoupled from the output. The battery charging current is maintained by the output capacitor C, which discharges through the battery internal resistance R_{bat} with a current equals to:

$$I_C = \frac{V_C - V_{bat}}{R_{bat}}. \tag{4.2}$$

b) Switch-off interval ($d \cdot T \leq t < T$)

When the switch S is turned off, the diode D conducts and the energy stored in the inductor is transferred to the output. The voltage across the inductor becomes:

$$V_L = V_{in} - V_C, \qquad \frac{dI_L}{dt} = \frac{V_{in} - V_C}{L} < 0 \tag{4.3}$$

Since $V_C > V_{in}$ in boost operation. The inductor current flows through the diode, simultaneously recharging the capacitor and supplying current to the battery. The inductor current decreases linearly until the switch is turned on again.

4.1.1 Voltage conversion ratio

Applying superposition on the inductor voltage for both cases, is it obtained the following expression:

$$V_{in} \cdot d \cdot T + (V_{in} - V_C)(1 - d) \cdot T = 0 \tag{4.4}$$

Solving for the output capacitor voltage V_C:

$$V_C = \frac{V_{in}}{1 - d} \tag{4.5}$$

It is important to note that Eq. (4.5) describes the voltage across the output capacitor V_C, not directly the battery voltage V_{bat}. The actual charging current delivered to the battery is determined by the difference $(V_C - V_{bat})$, scaled by the internal resistance:

$$I_{bat} = \frac{V_C - V_{bat}}{R_{bat}} \tag{4.6}$$

The operating point of the converter is therefore set by the duty cycle d and the battery's state of charge, which sets V_{bat}. As the battery charges and V_{bat} rises, the duty cycle must be adjusted accordingly to maintain the desired charging current.

4.1.2 CCM boundary condition

The converter operates in CCM if the inductor satisfies:

$$L > L_b = \frac{(1 - d)^2 \cdot R_{bat}}{2 \cdot f_{sw}} \tag{4.7}$$

4.1.3 Output voltage ripple

During the on-state interval, the capacitor alone sustains the battery charging current $(V_C - V_{bat})/R_{bat}$. The resulting voltage ripple across the capacitor is:

$$\Delta V_C = \frac{(V_C - V_{bat}) \cdot d}{R_{bat} \cdot C \cdot f_{sw}} \tag{4.8}$$

The minimum capacitance required to keep the ripple below a specified value $\Delta V_{C,max}$ is therefore:

$$C_{min} = \frac{(V_C - V_{bat}) \cdot d}{(\Delta V_{C,max} - I_{C,ripple} \cdot R_{ESR})\ R_{bat} \cdot f_{sw}} \tag{4.9}$$

Note that as the battery approaches full charge and $V_{bat} \rightarrow V_C$, the required capacitance decreases, since the charging current itself diminishes.

These steady-state relationships, particularly the voltage superposition of the inductor form the basis for the averaged state-space model developed in the Appendix B.

4.2 Topology I analysis (Three-phase interleaved boost converter)

The three-phase interleaved boost converter extends the single-phase topology by connecting three branches in parallel, sharing the same input voltage source V_{in}, the same output capacitor C and battery load (V_{bat}, R_{bat}). Each leg $k \in \{1, 2, 3\}$ consists of an inductor L_k, a controlled switch S_k, and a synchronous diode $\overline{S_k}$, as shown in Fig. 4.3. One feature of the interleaved topology is that the parallel branches can have a mutual phase shift to reduce the input and output ripple.

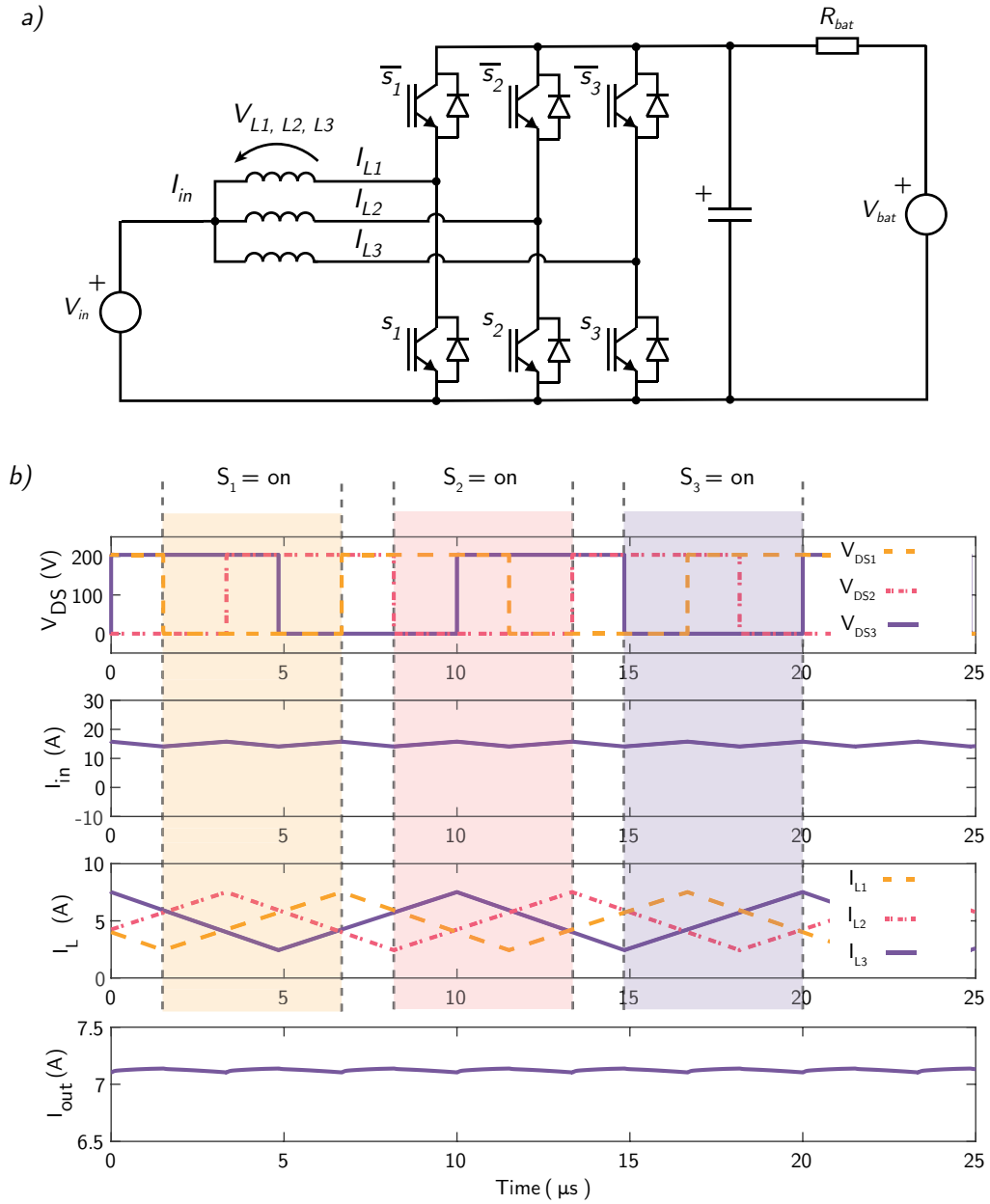

Figure 4.2: Three-phase boost converter (V_{in}=100V, V_{out}=200 V, D=0.52, f_{sw}=100 kHz). (a) Circuit topology, (b) Relevant steady-state operating waveforms.

4.2.1 Input Current Analysis

In a balanced scenario, considering the three-phase converter, the phase shift between consecutive phases is $\Delta\theta = 2\pi/3$. Additionally, all three phases share the same duty cycle d, so that:

$$d_1 = d_2 = d_3 = d, \qquad \theta_k = (k-1) \cdot \frac{2\pi}{3}, \quad k \in \{1, 2, 3\} \tag{4.10}$$

The total input current is the sum of the three inductor currents:

$$I_{\text{in}}(t) = I_{L_1}(t) + I_{L_2}(t) + I_{L_3}(t) \tag{4.11}$$

The optimal cancellation condition can be derived from (4.11). Each inductor current can be described by its Fourier decomposition; the n-th harmonic of the k-th leg is:

$$I_{L,k}^{(n)} = I_n \cdot e^{j \cdot \omega \cdot n \cdot t} \cdot e^{-j \cdot \frac{2\pi}{3} \cdot (k-1) \cdot n} \tag{4.12}$$

Taking only the phase term, the harmonic sum over all three legs is:

$$S_n = \sum_{k=1}^{3} e^{-j \cdot \frac{2\pi}{3} \cdot (k-1) \cdot n} \tag{4.13}$$

$$= \frac{1 - e^{j \cdot 2\pi \cdot n}}{1 - e^{j \cdot \frac{2\pi \cdot n}{3}}} \tag{4.14}$$

This sum is zero for every n that is not a multiple of three. Hence, the effective ripple frequency at the input is $f_{sw}^{*} = 3 \cdot f_{sw}$.

The input current ripple is determined by the piecewise function [83]:

$$\Delta I_{\text{in}}(d) = \frac{V_{\text{in}}}{L \cdot f_{sw}} \cdot g(d) \begin{cases} 3\,d\,(1 - 3d), & \text{if } d \leq \dfrac{1}{3} \\ (1 - d)\,(3d - 1), & \text{if } \dfrac{1}{3} \leq d \leq \dfrac{2}{3} \\ 3\,(1 - d)\,(3d - 2), & \text{if } \dfrac{2}{3} \leq d \leq 1 \end{cases} \tag{4.15}$$

4.2.2 Output Current Analysis

In this topology each branch delivers current to the output only during the off-time of its switch. The average diode current of leg k is therefore scaled by the complementary duty cycle $(1 - d_k)$, and the output capacitor current is:

$$I_C(t) = \sum_{k=1}^{3} I_{L_k}(t) \cdot (1 - d_k) - I_{out}(t) \tag{4.16}$$

The load is modelled as a battery represented by a voltage source in series with a resistance:

$$V_{out}(t) = V_{bat} + R_{bat} \cdot I_{out}(t) \tag{4.17}$$

The capacitor current is also related to the output voltage by:

$$I_C(t) = C\,\frac{dV_{out}(t)}{dt} \tag{4.18}$$

Combining (4.16)–(4.18), the governing equation for the output voltage is:

$$C\,\frac{dV_{out}(t)}{dt} = \sum_{k=1}^{3} I_{L_k}(t)\cdot(1-d_k) - \frac{V_{out}(t)-V_{bat}}{R_{bat}} \tag{4.19}$$

In steady state the output voltage is constant, so the capacitor current is zero, $I_C = 0$, and (4.19) reduces to:

$$\sum_{k=1}^{3} I_{L_k}(1-d_k) = \frac{V_{out}-V_{bat}}{R_{bat}} = I_{out} \tag{4.20}$$

As a power-balance condition, the total average current delivered to the output rail equals the load current. For the symmetric case where all three legs operate at the same operating point, $I_{L_k} = I_L$ and $d_k = d$ for all k, (4.20) simplifies to:

$$I_{out} = 3\cdot I_L\cdot(1-d) \tag{4.21}$$

4.2.3 Output Voltage Ripple

The voltage ripple arises within each switching period from the pulsed nature of the diode currents. During the on-time of leg k, its diode is blocked and the capacitor discharges into the battery load. Applying (4.18) and (4.17) during this interval:

$$C\,\frac{dV_{out}}{dt} = -\frac{V_{out}-V_{bat}}{R_{bat}} \tag{4.22}$$

Linearising over the on-time interval $\Delta t = d_k/f_{sw}$ under the small-ripple assumption $\Delta V_C \ll V_{out}-V_{bat}$, the peak-to-peak voltage ripple contributed by leg k is:

$$\Delta V_C = \frac{(V_{out}-V_{bat})\,d_k}{R_{bat}\,C\,f_{sw}} \tag{4.23}$$

In the symmetric case $d_k = d$, the three legs are interleaved with a phase shift of $120°$, so the effective ripple frequency seen by the capacitor is $3f_{sw}$ and the ripple is reduced by a factor of three compared to a single-phase converter:

$$\Delta V_C = \frac{(V_{out}-V_{bat})\cdot d}{R_{bat}\cdot C\cdot 3\cdot f_{sw}} \tag{4.24}$$

4.3 Topology II Analysis (Two-Phase Interleaved Boost Converter)

Similarly, Topology II consists of a two-phase interleaved boost converter with two identical branches sharing the same input voltage V_{in}. Each leg $k \in \{1, 2\}$ consists of an inductor L_k, a controlled switch S_k, and a synchronous diode $\overline{S_k}$.

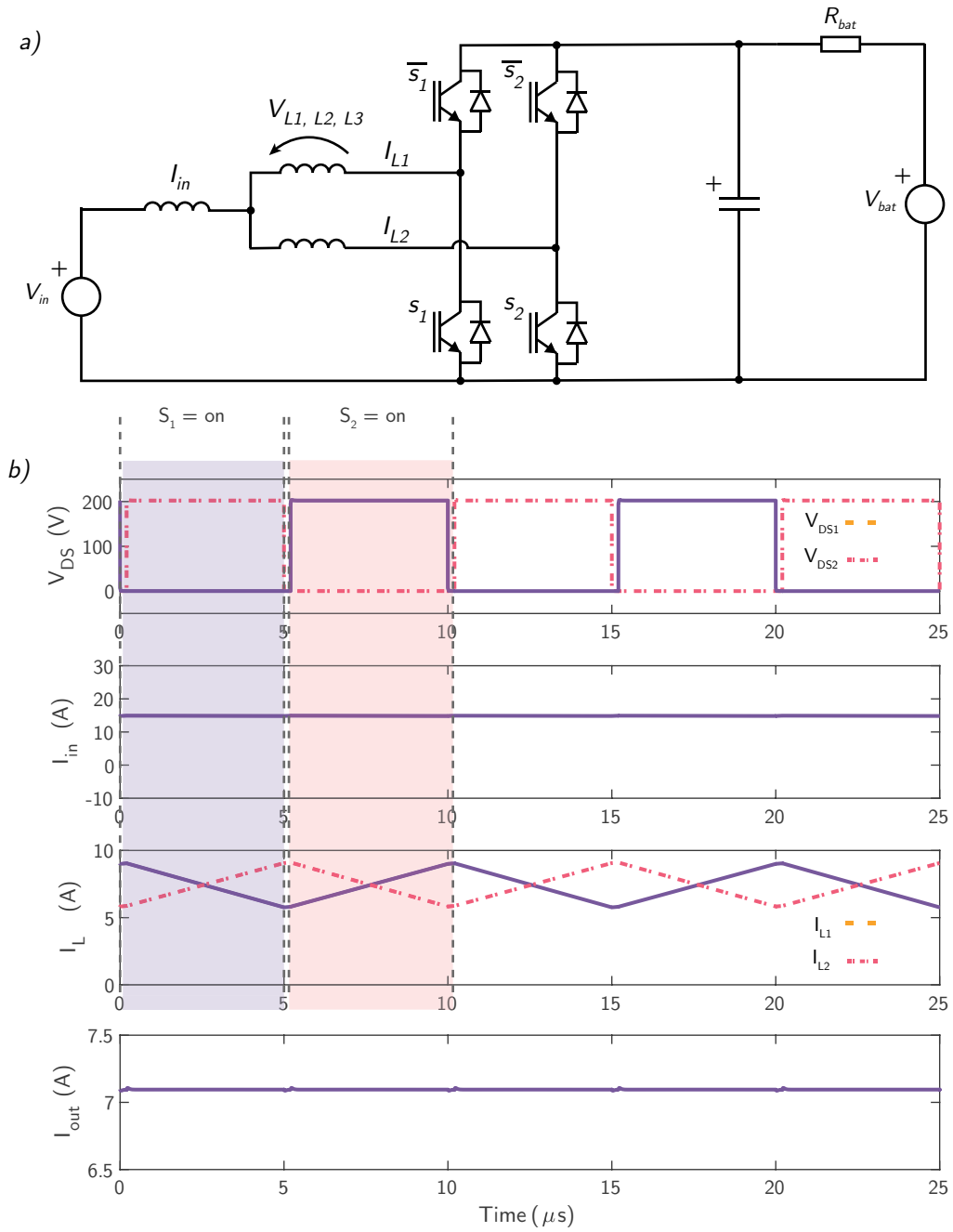

Figure 4.3: Two-phase boost converter (V_{in}=100 V, V_{out}=200 V, D=0.52, f_{sw}=100 kHz). (a) Circuit topology, (b) Relevant steady-state operating waveforms.

4.3.1 Input Current Analysis

The analysis follows the same Fourier approach used in Topology I (Section 4.2), now applied for two phases. In balanced operation both branches share the same duty cycle d, with a phase shift

of $180°$ between them:

$$d_1 = d_2 = d, \qquad \theta = \pi \tag{4.25}$$

The total input current is the sum of the two inductor currents:

$$i_{in}(t) = i_{L_1}(t) + i_{L_2}(t) \tag{4.26}$$

Substituting into the harmonic sum of (4.13) with $N = 2$:

$$S_n = \sum_{k=1}^{2} e^{-j\pi(k-1)n} = 1 + e^{-j\pi n} \tag{4.27}$$

The sum cancels all odd harmonics. Then, the effective ripple frequency at the input is therefore doubled:

$$f_{sw}^{*} = 2\, f_{sw} \tag{4.28}$$

The input current ripple follows the same piecewise structure as (4.15), for the two phase case [83]:

$$\Delta I_{in}(d) = \frac{V_{in}}{L \cdot f_{sw}} \cdot g(d) \begin{cases} d\,(1-2d), & d \le \dfrac{1}{2} \\ (1-d)\,(2d-1), & \dfrac{1}{2} \le d \le 1 \end{cases} \tag{4.29}$$

4.3.2 Output Current Analysis

The output stage of Topology II follows the same governing equations derived for Topology I. The capacitor current balance (4.16), the battery load model (4.17), and the capacitor relation (4.18) all apply unchanged; the only difference is that the sum now runs over $N = 2$ legs. The output voltage equation (4.19) therefore becomes:

$$C\,\frac{dV_{out}}{dt} = \sum_{k=1}^{2} I_{L_k}(t)\,(1-d_k) - \frac{V_{out}(t) - V_{bat}}{R_{bat}} \tag{4.30}$$

Setting $dV_{out}/dt = 0$ in (4.30), the power-balance condition (4.20) specialises to two legs:

$$\sum_{k=1}^{2} I_{L_k}(1-d_k) = \frac{V_{out} - V_{bat}}{R_{bat}} = I_{out} \tag{4.31}$$

For the symmetric case $I_{L,k} = I_L$, $d_k = d$, this reduces to:

$$I_{out} = 2\, I_L\,(1-d) \tag{4.32}$$

Applying the ripple derivation of (4.23) to two interleaved legs with a phase shift of $180°$, the effective switching frequency seen by the output capacitor is $2f_{sw}$, giving:

$$\Delta V_C = \frac{(V_{out} - V_{bat})\, d}{R_{bat}\, C \cdot 2 f_{sw}} \tag{4.33}$$

which is half the ripple of an equivalent single-phase converter, consistent with the interleaving benefit noted in (4.24).

4.3.3 Effective Per-Phase Inductance

The series input inductance modifies the effective inductance seen by each phase, and this modification depends on the phase shift angle. For this analysis, balanced operation is assumed, with two branches sharing the current from the input series inductor L_{in}. The two phase currents sum at the input node:

$$I_{in}(t) = I_{L,1}(t) + I_{L,2}(t) \tag{4.34}$$

Phase 2 is delayed relative to phase 1 by a fixed time shift $\tau = \theta/\omega_s$, where $\omega_s = 2\pi f_{sw}$ is the angular switching frequency and $\theta \in [0, \pi]$ is the inter-phase shift:

$$I_{L,2}(t) = I_{L,1}(t - \tau), \qquad \tau = \frac{\theta}{\omega_s} \tag{4.35}$$

The inductor L_{in} is in series with the supply and carries the total input current I_{in}. Writing KVL around the switching loop of phase k ($k = 1, 2$):

$$V_{in}(t) = L\,\frac{dI_{L,k}}{dt} + L_{in}\,\frac{dI_{in}}{dt} \tag{4.36}$$

The objective is to express dI_{in}/dt in terms of $dI_{L,k}/dt$ so that Eq. 4.36 collapses to a single effective-inductance equation.
The steady-state ripple current of a boost converter is triangular. For the purpose of analysing the dominant ripple component and the interleaving cancellation effect, each phase current is represented by its fundamental Fourier harmonic at the switching frequency f_{sw}:

$$\Delta I_{L,1}(t) = \hat{I}\cos(\omega_s t), \qquad \Delta I_{L,2}(t) = \hat{I}\cos(\omega_s t - \theta) \tag{4.37}$$

In phasor notation, Eq. 4.36 written for phase 1 becomes:

$$V_{in} = j\omega_s L\,\hat{I}_{L,1} + j\omega_s L_{in}\,\hat{I}_{in} \tag{4.38}$$

Substituting Eq. 4.34 into Eq. 4.38 and expressing $\hat{I}_{L,2} = \hat{I}_{L,1}\,e^{-j\theta}$ from Eq. 4.35:

$$V_{in} = j\omega_s\left[L\,\hat{I}_{L,1} + L_{in}\,\hat{I}_{L,1}(1 + e^{-j\theta})\right] \tag{4.39}$$

Factoring out $j\omega_s\hat{I}_{L,1}$:

$$V_{in} = j\omega_s\,\hat{I}_{L,1}\left[L + L_{in}(1 + e^{-j\theta})\right] \tag{4.40}$$

For Eq. 4.40 to represent a purely inductive voltage drop, the bracketed term must be real. Taking its real part:

$$L_{eff} = \Re\left[L + L_{in}(1 + e^{-j\theta})\right] \tag{4.41}$$

Expanding the last term using Euler's identity $\Re[e^{-j\theta}] = \cos\theta$:

$$L_{eff} = L + L_{in}(1 + \cos\theta) \tag{4.42}$$

Eq. 4.42 shows that L_{eff} seen per phase is modulated by the phase shift θ. At $\theta = 0$, the two phases are in phase, and the effective inductance increases to $L_{eff} = L + 2L_{in}$. At $\theta = \pi$, $L_{eff} = L$, meaning L_{in} does not contribute to reducing the phase ripple, and each phase sees only its own inductor. However, the effect is counteracting; if the phase ripple is reduced, the input ripple increases.

4.4 Current unbalance

In practice, perfect balance among the N phases is not guaranteed. Component tolerances in the inductors L_k, asymmetries in the gate drive signals, or differences in the on-resistance of the switches S_k can all lead to unequal current sharing. This is referred to as current unbalanced and it is characterised by the deviation of each phase current from the nominal average value:

$$\Delta I_{L_k} = I_{L_k} - \frac{I_{in}}{N}, \qquad k \in \{1, \ldots, N\} \tag{4.43}$$

where $N = 3$ for Topology I and $N = 2$ for Topology II. Current unbalance has some negative consequences:

- The ripple cancellation property is degraded. When the N legs do not carry equal currents, the partial cancellation of the switching harmonics is incomplete, increasing the input and output current ripple from the theoretical $N \cdot f_{sw}$ prediction.
- The thermal load is distributed unevenly across the converter legs. Over time, this accelerates component ageing and reduces converter reliability.
- Current unbalance introduces unexpected harmonics in the input and output current worsening the power quality.

It is important to note that current unbalance does not necessarily alter the output voltage V_C or the total charging current I_{bat}, since these are determined by the aggregate behaviour of all N legs. However, the *distribution* of that current among the legs is uncontrolled in the absence of a dedicated balancing strategy.

4.4.1 The unbalance as a degree of freedom

From a control perspective, both topologies introduce additional degrees of freedom with respect to the single-phase case. In the single-phase converter, the only control variable is the duty cycle d, which simultaneously determines the output voltage and the inductor current. In an N-phase interleaved converter, the N duty cycles $d_1, \ldots, d_N$ can in principle be set independently.

For Topology I ($N = 3$) there are two independent unbalance modes, since the three deviations ΔI_{L_k} are constrained to sum to zero. For Topology II ($N = 2$) there is a single unbalance mode, described by the scalar difference $I_{L_1} - I_{L_2}$.

This observation motivates a control architecture that regulates not only the output voltage V_C and the total charging current I_{bat}, but also actively monitors and corrects current unbalance among the legs.

4.4.2 Unbalance analysis

To quantify the deviation of the electrical parameters from their nominal values, an unbalance factor is defined for both the inductance and resistance as the ratio between the test value and the nominal value.

$$k_L = \frac{L_{\text{test}}}{L_{\text{nom}}}, \qquad k_R = \frac{R_{\text{test}}}{R_{\text{nom}}} \tag{4.44}$$

Based on the results shown in Tables 4.1 and 4.2, the following conclusions are obtained for each topology:

Topology T1

- **Inductance unbalance:** The peak-to-peak current ripple ΔI_{pp} is inversely proportional to the phase inductance. A phase with $k_L = 1.5$ reduces the ripple from 5.14A to 3.43A, while $k_L = 0.5$ increases it to 10.27A. The DC component and RMS value remain nearly unaffected by inductance variation, confirming that inductance primarily governs the ripple magnitude and not the DC current sharing.

- **Resistance unbalance:** The DC current is inversely proportional to the phase resistance. A phase with $k_R = 1.5$ draws significantly less DC current (5.85A vs. the nominal 8.02A), while $k_R = 0.5$ forces the phase to conduct a much higher DC current (12.71A). The current ripple ΔI_{pp} remains unchanged across all phases, confirming that resistance unbalance affects only the DC sharing. When both effects are combined (e.g., $k_R = 0.5$ on I_1 and $k_R = 1.5$ on I_3), the DC imbalance is further amplified, with I_1 reaching 13.56A and I_3 dropping to 4.79A.

- **RMS current:** In all T1 cases, the RMS value is dominated by the DC component, as the ripple contribution is comparatively small.

Topology T2

- **Current distribution:** Unlike T1, T2 exhibits an inherently asymmetric current distribution even under balanced conditions. Phase I_3 carries approximately twice the current of I_1 and I_2 (25.71A vs. 12.84A), with a nearly negligible ripple ($\Delta I_{pp} \approx 0.13A$). This asymmetry is intrinsic to the T2.

- **Inductance unbalance:** As in T1, the peak-to-peak ripple of the affected phase changes inversely with inductance (ΔI_{pp} increases for $k_L = 0.5$ and decreases for $k_L = 1.5$). However, inductance variation on I_1 or I_2 also produces a secondary effect on the unaffected parallel phase, slightly modifying its ripple. Phase I_3 remains largely unaffected in its DC component but shows a small increase in ripple, since $I_3 = I_1 + I_2$.

- **Resistance unbalance:** Resistance mismatch on I_1 or I_2 redistributes the DC current between those two phases, following the same inverse proportionality observed in T1. Phase I_3 continues to carry the sum of the other phases currents, not being affected to resistance changes in I_1 or I_2. When both $k_R = 0.5$ and $k_R = 1.5$ are applied simultaneously to I_1 and I_3, the DC unbalance across all phases is maximized.

- **RMS current:** As in T1, the RMS value in T2 is dominated by the DC component for all phases.

Both topologies confirm that inductance unbalance dictates ripple distribution while resistance unbalance governs DC current sharing, and that the RMS current is dominated by the DC component at this power level.

Table 4.1: Measured phase currents under inductance and resistance unbalance for T1 ($L_{nom} = 100\,\mu$H, $R_{nom} = 100\,m\Omega$)

I_i	k_L	k_R	I_{RMS} **(A)**	I_{DC} **(A)**	I_{pp} **(A)**
I_1	1	1	8.16	8.02	5.14
I_2	1	1	8.16	8.02	5.14
I_3	1	1	8.16	8.02	5.14
I_1	1.5	1	8.08	8.02	3.43
I_2	1	1	8.15	8.01	5.14
I_3	1	1	8.15	8.01	5.14
I_1	0.5	1	8.56	8.03	10.27
I_2	1	1	8.18	8.04	5.14
I_3	1	1	8.17	8.04	5.14
I_1	0.5	1	8.56	8.03	10.27
I_2	1	1	8.17	8.04	5.14
I_3	1.5	1	8.10	8.03	3.43
I_1	1	1.5	6.04	5.85	5.13
I_2	1	1	8.80	8.68	5.13
I_3	1	1	8.78	8.66	5.13
I_1	1	0.5	12.80	12.71	5.15
I_2	1	1	6.77	6.60	5.15
I_3	1	1	6.81	6.65	5.15
I_1	1	0.5	13.64	13.56	5.15
I_2	1	1	7.18	7.03	5.15
I_3	1	1.5	5.01	4.79	5.15

Table 4.2: Measured phase currents under inductance and resistance unbalance for T2 ($L_{nom} = 100\,\mu$H, $R_{nom} = 100\,m\Omega$)

I_i	k_L	k_R	I_{RMS} **(A)**	I_{DC} **(A)**	I_{pp} **(A)**
I_1	1	1	12.91	12.84	4.78
I_2	1	1	12.91	12.84	4.78
I_3	1	1	25.71	25.71	0.13
I_1	1.5	1	12.87	12.82	3.57
I_2	1	1	12.92	12.86	4.17
I_3	1	1	25.68	25.68	0.70
I_1	0.5	1	13.04	12.86	7.17
I_2	1	1	13.01	12.89	5.95
I_3	1	1	25.77	25.76	1.32
I_1	0.5	1	13.03	12.87	6.93
I_2	1	1	13.02	12.89	6.04
I_3	1.5	1	25.76	25.76	0.44
I_1	1	1.5	10.41	10.32	4.77
I_2	1	1	15.36	15.29	4.76
I_3	1	1	25.55	25.61	0.13
I_1	1	0.5	17.03	16.97	4.81
I_2	1	1	9.01	8.90	4.81
I_3	1	1	15.87	25.87	0.17
I_1	1	0.5	16.72	16.66	4.72
I_2	1	1	8.84	8.72	4.73
I_3	1	1.5	25.39	25.39	0.13

Chapter 5

Results

This chapter presents the experimental results for both converter topologies. It begins with a comparison of system efficiencies, followed by a breakdown of power losses. A current harmonic analysis show the ripple level of each topology. Then, is discussed the influence of the rotor inclusion on the converter. Finally, is presented the results for the scaled model at nominal operating conditions.

5.1 System efficiency analysis

Figure 5.1 presents the overall system efficiency for both topologies. In Figure 5.1 (a), T1 achieves a peak efficiency of 94.4% and T2 of 93.9%, a difference of 0.5% that is not a determining factor at this stage. Both topologies exhibit a similar trend with switching frequency; efficiency increases up to a mid-range value and then decreases, with T1 peaking in the 30–60 kHz range and T2 at a lower 20–40 kHz, indicating that T2 reaches its optimum at a lower switching frequency.

Regarding phase shift sensitivity shown in Figure 5.1 (b). T1 shows a clear dependence, with efficiency rising towards the theoretical cancellation angle and peaking at 93.63%. T2 exhibits a flatter response, with its peak of 95.19% occurring at 90° rather than the expected 180°. However, as shown in Section 5.3.1, operating T2 at 180° yields ripple cancellation benefits not captured by the efficiency figure alone.

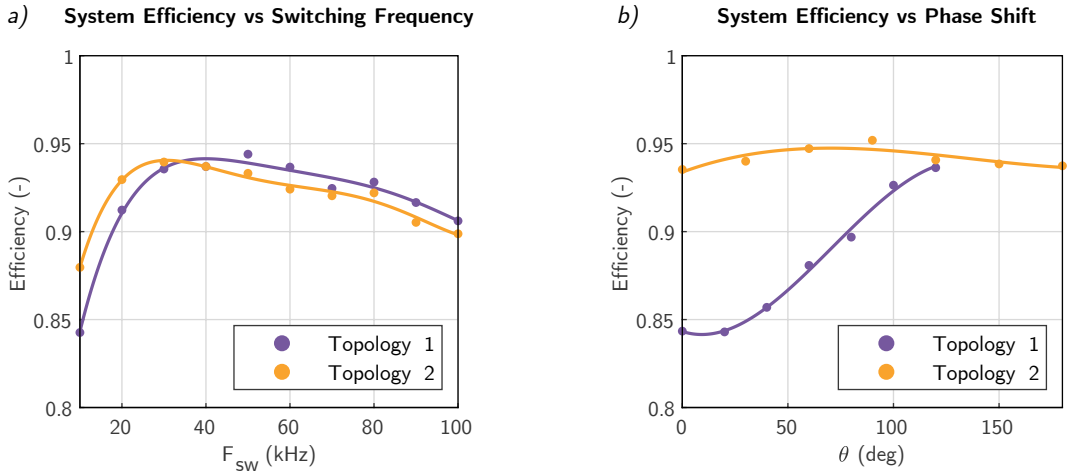

Figure 5.1: System efficiency as a function of (a) switching frequency and (b) phase shift for Topology 1 and Topology 2. Markers indicate measured data points; solid lines represent fitted curves.

5.2 Component efficiency analysis

Following the efficiency analysis, Figure 5.2 shows a breakdown of the efficiencies for the main components, the inverter and the electrical machine stator, referred to as (EM). The inverter efficiency decreases with switching frequency but remains within $\sim$ 97–99%, as shown in Figures 5.2 (a) and (b). Figures 5.2 (c) and (d) show that over the phase shift sweep, inverter efficiency is rather constant at approximately 98.5%.

Figures 5.2 (a) and (b), shows the relation of EM stator efficiency and the switching frequency. It efficiency follows the same trend as the system efficiency, specially before 30 kHz point where the switching losses from the inverter start being noticeable. The lowest efficiency is reached at 10 kHz with 85.7% and 88.5% and a peak efficiency of 95.9% and 95% for T1 and T2 correspondingly. Regarding the phase shift sweep, T1 EM stator efficiency depend on phase shift, increasing from 86.3% to 93.5 % as the phase shift approaches the maximum cancellation angle of 120°. T2 EM stator shows a different trend being rather flatter with an efficiency of $\sim$ 95%.

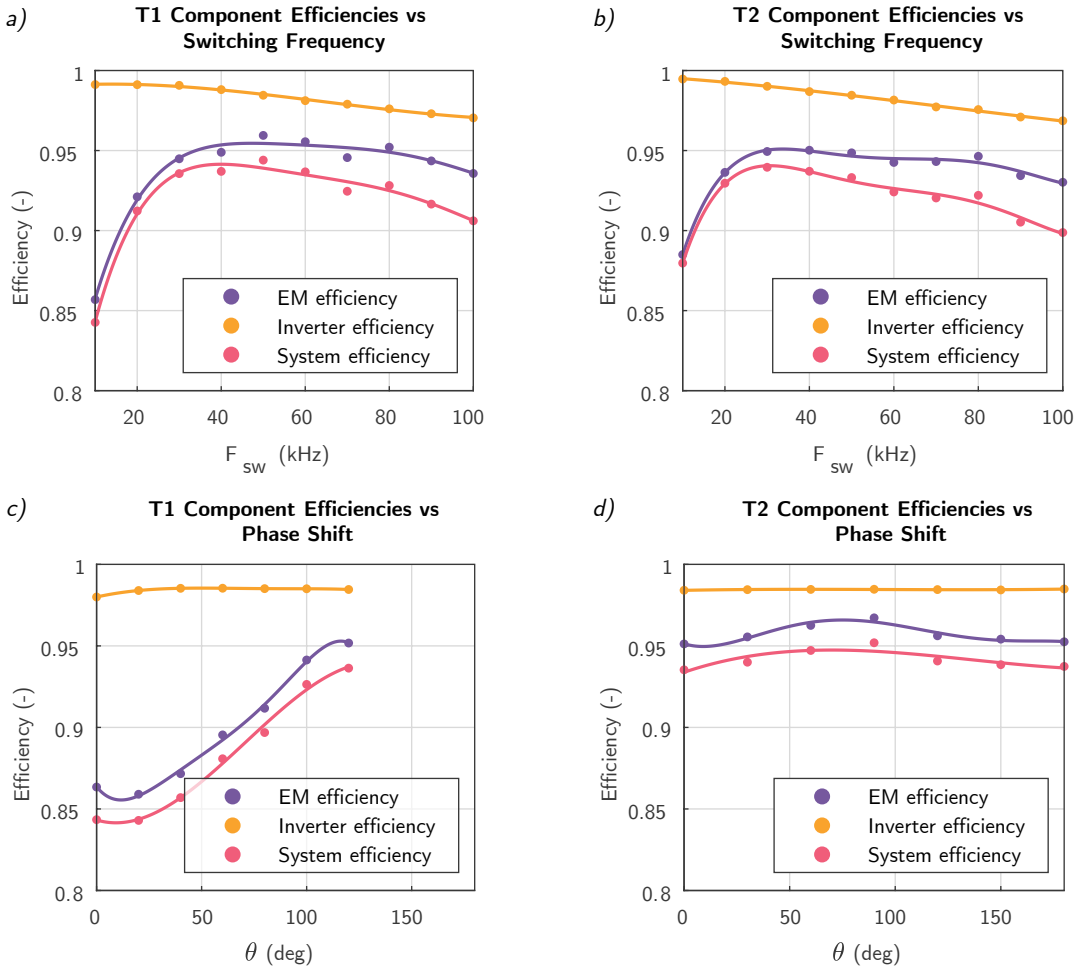

Figure 5.2: Component efficiency as a function of (a-b) switching frequency and (c-d) phase shift for Topology 1 and Topology 2. Markers indicate measured data points; solid lines represent fitted curves.

5.2.1 Electrical machine losses analysis

Figure 5.3 show the EM stator copper losses and trends for both topologies as functions of switching frequency and phase shift. On the frequency sweep, EM stator copper losses are dominated by AC losses in both topologies, especially at low switching frequencies (10 kHz).

- For T1, AC losses reach 327 W and then continuously decrease until 60 kHz, reaching around 82 W, where the increase in resistance due to the skin effect is counteracted by the ripple reduction; DC losses are nearly constant at around 7 W and have a negligible impact on the trend.
- T2 behaves similarly, with AC losses reaching 190 W at 10 kHz and continuously decreasing until 50–60 kHz, where losses flatten at around 40 W. DC losses are nearly constant at around 30 W and become comparable to the AC losses after 60 kHz.

For the phase shift sweep:

- T1 EM stator copper losses are dependent on the phase shift, with AC losses decreasing from 357 W to 88 W as the phase shift reaches the maximum cancellation angle of 120°, and DC losses remain constant at approximately 7 W.
- T2 presents a different behaviour; AC losses increase with the phase shift, since the effective inductance per phase varies as a function of the phase shift, as analysed in Section 4.3.3. When the phase currents are in phase the phase ripple is reduced, and losses are 19 W, whereas at 120° the input ripple is cancelled but the phase ripple increases, generating losses of 41 W, and DC losses remain constant at 29 W.

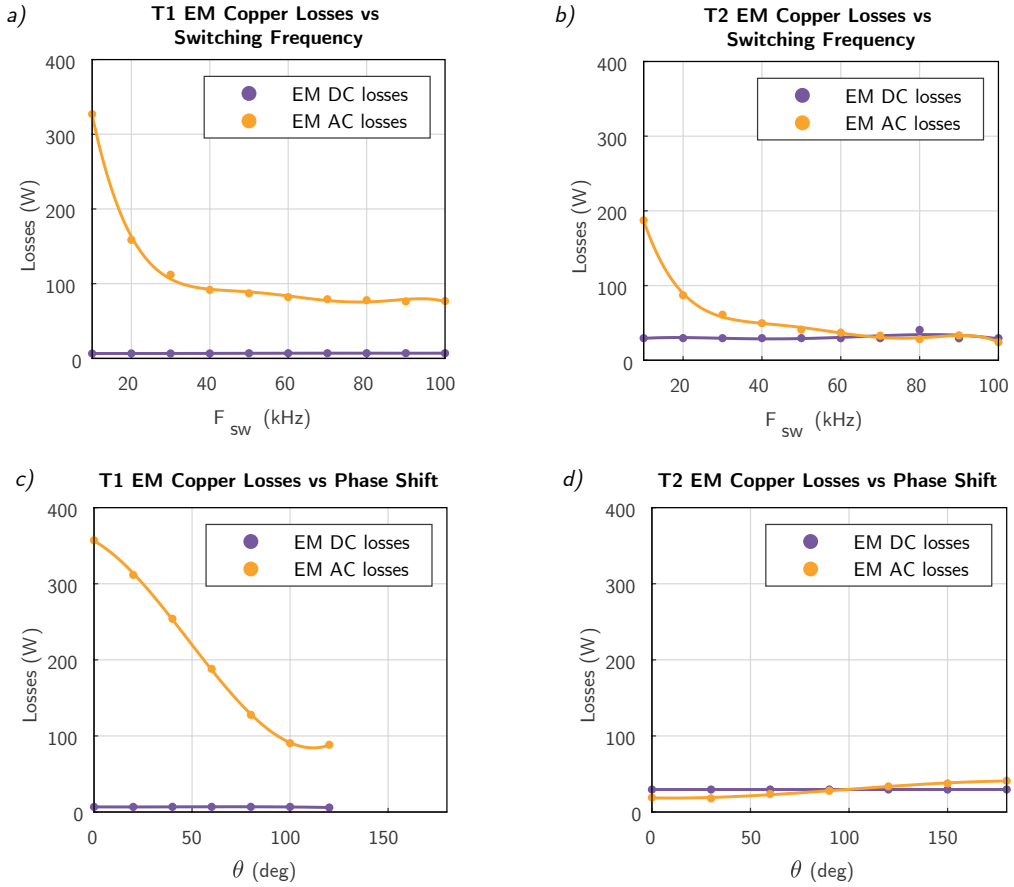

Figure 5.3: EM Stator losses as a function of (a-b) switching frequency and (c-d) phase shift for Topology 1 and Topology 2. Markers indicate measured data points; solid lines represent fitted curves.

5.2.2 Inverter Losses Analysis

Figure 5.4 (a) and (b), show that switching losses are dominant at this power level for the inverter. They increases linearly with frequency from $\sim$ 18 to 74 W in the range of 10-100kHz for both topologies. Conduction losses also decrease with the swithcing frequency as the current ripple reduces and then the AC current component; after 50kHz the DC current component is predominant and the losses remains constant and below 1W.

In the phase shift sweep, switching losses remain the dominant contribution, although their variation becomes flatter compared to the switching frequency sweep.

- For T1, switching losses are higher at low phase shift due to reduced ripple cancellation. Overall, switching losses are around 39 W, while conduction losses remain below 1 W.

- For T2, both switching and conduction losses remain constant across the phase shift range. Switching losses are close to 40 W, and conduction losses are approximately 1.5 W.

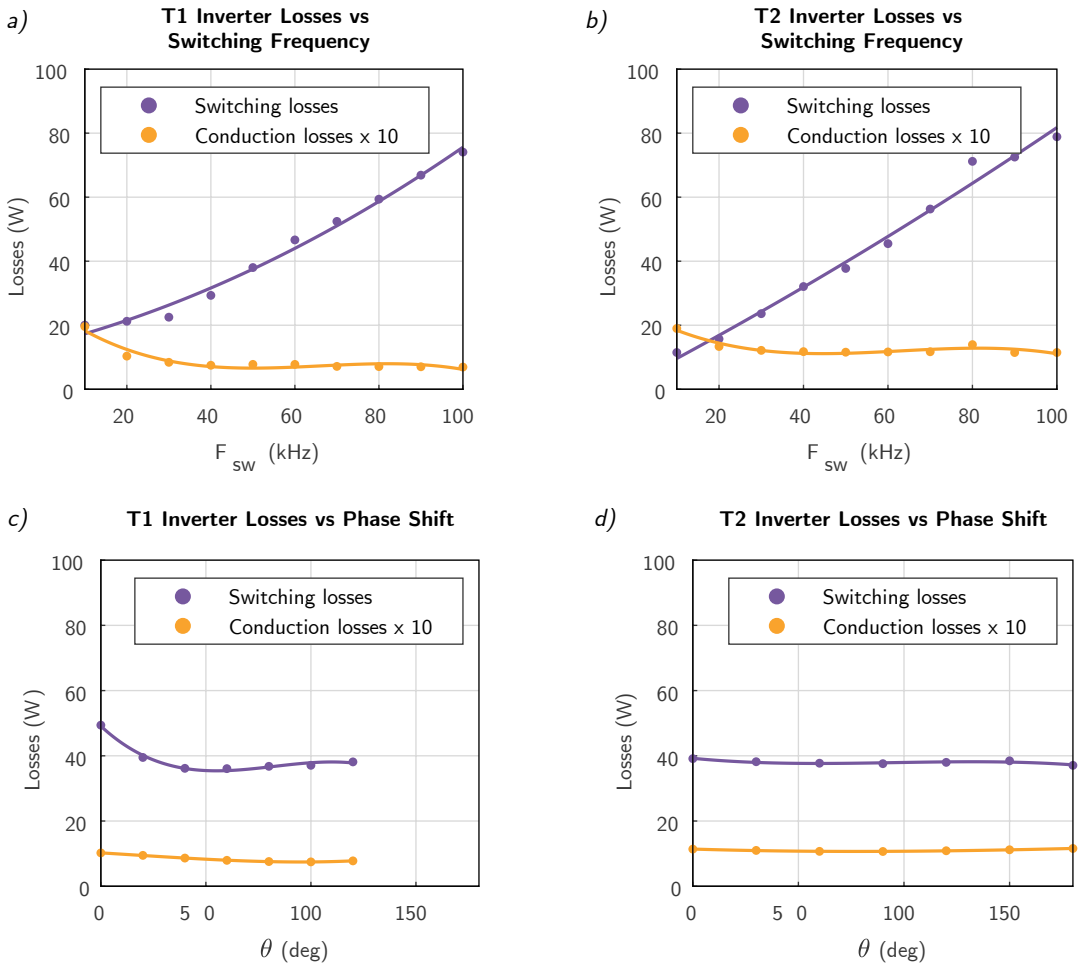

Figure 5.4: Inverter efficiency as a function of (a-b) switching frequency and (c-d) phase shift for Topology 1 and Topology 2. Markers indicate measured data points; solid lines represent fitted curves.

5.3 Current Analysis

Currents through the converter are shown in Figures 5.5 and 5.6. A separate analysis is presented for the input, phase, and output currents for T1 and T2.

5.3.1 Input current

Figure 5.5 (a) shows the highest harmonic component of the input current $I_{fn^*,\text{in}}$, which is used in this analysis as a measure of current ripple. As expected from the average inductor voltage–current relationship ($\Delta I = \frac{V_{in} \cdot D}{f}$), the fundamental follows a $1/f$ trend with switching frequency, decreasing from 8.7 A at 10 kHz to 0.9 A at 100 kHz. Over the phase shift sweep, the fundamental falls from 16.5 A at $0°$ to 1.8 A at $120°$. Figure 5.5 (b) shows the same $1/f$ frequency dependence for T2, but at a substantially lower magnitude of only 0.22 A at 10 kHz compared to 8.7 A in T1. Over the phase shift sweep, the fundamental decreases from 1.5 A at $0°$ to approximately 0 A at $180°$, following a similar trend to T1 but at a consistently lower level.

5.3.2 AC phase currents

The balance of the fundamental current among the three phases is shown in Figures 5.5 (c) and (d). Over the frequency sweep in T1, the phase currents follow the same $1/f$ trend and remain well balanced. Over the phase shift sweep, the balance is best at $0°$ and $120°$, and worsens at intermediate angles The fundamental phase currents for T2, are well balanced and follow the $1/f$ trend, reaching comparable values to T1 at the corresponding frequencies. The series winding fundamental current is negligible, reaching a maximum of only 0.22 A at 10 kHz. Over the phase shift sweep, a redistribution of AC content is observed: at $0°$, increased effective inductance on phases 1 and 2 suppresses their fundamental to 0.82 A, while at $180°$ the value rises to 2.35 A, closely matching the T1 value of 2.31 A. The series winding current follows the opposite trend, decreasing from 1.5 A at $0°$ to 0.04 A at $180°$ as cancellation is maximised as shown in Figures 5.6 (c) and (d).

5.3.3 DC phase currents

The DC phase currents as a function of the switching frequency are presented in Figures 5.5 (e) and (f). An imbalance is observed when the switching frequency is increased. The spread between phases grows from 8.37–8.85 A at 10 kHz to 7.72–10.30 A at 100 kHz; however for T2 this effect is not observed. Figures 5.6 (e) and (f) show that, over the phase shift the DC phase current remain constant for both topologies, where a mild unbalance is noted for T1 but associated to the switching frequency rather the phase shift.

5.3.4 Output current

The output current ripple as a function of switching frequency is shown in Figures 5.5 (g) and (h). In T1, by increasing the switching frequency, the ripple decreases but not monotonically; isolated peaks appear at certain frequencies, likely associated with the excitation of circuit parasitics that redistribute spectral content beyond 50 kHz. The main reduction occurs below 30 kHz, where the fundamental drops from 1.4 A at 10 kHz to 0.2 A at 30 kHz, with little further improvement at higher frequencies. In T2, the same $1/f$ behaviour is observed, but the ripple reaches a negligible value of 0.02 A beyond 30 kHz.
The effect of phase shift modulation on the output ripple is shown in Figures 5.6 (g) and (h). In T1, a monotonic reduction is produced, from 1.34 A at $0°$ to 0.22 A at $120°$, following a trend similar to the input current. In T2, the ripple is suppressed to 0.01 A at $180°$. Taken together, both frequency

and phase shift control in T2 prove highly effective at reducing input and output current ripple, easing the design requirements for input and output filters and lowering the associated losses.

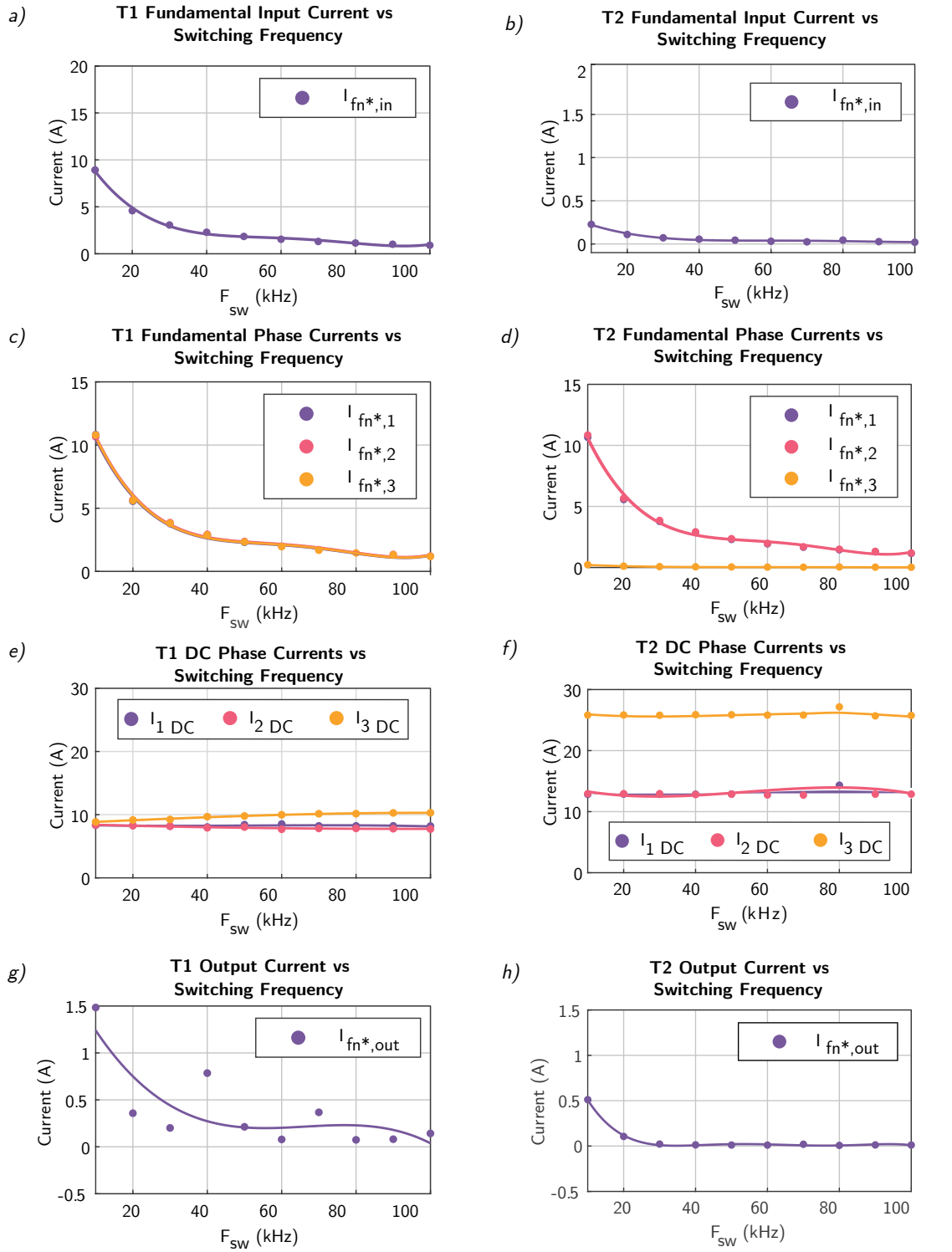

Figure 5.5: Current analysis as a function of switching frequency F_{sw}; T1 (left column) and T2 (right column). (a, b) Input fundamental current; (c, d) AC fundamental phase currents; (e, f) DC phase currents, (g, h) fundamental output current . Markers indicate measured data; solid lines represent fitted curves.

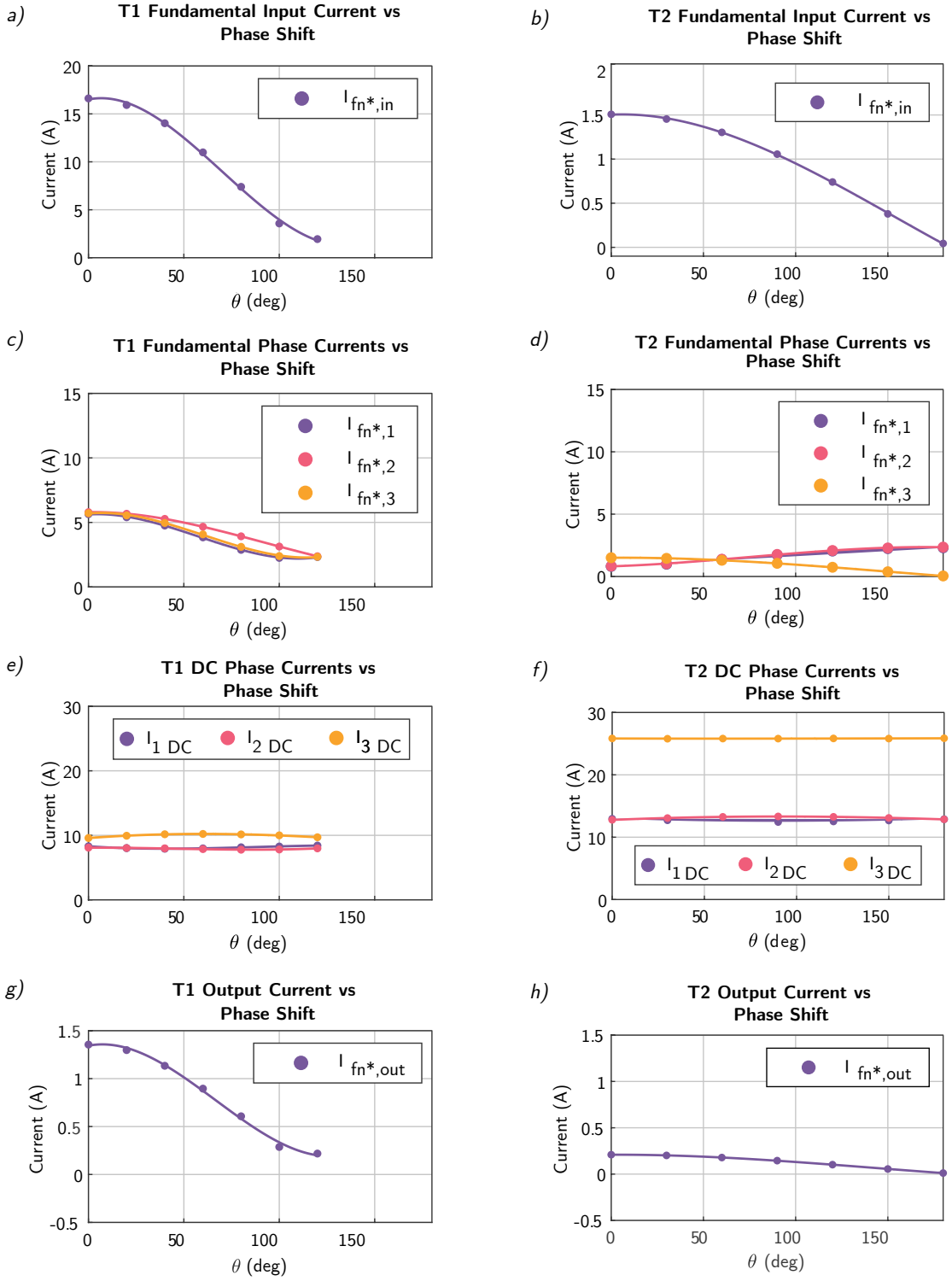

Figure 5.6: Current analysis as a function of phase shift θ; T1 (left column) and T2 (right column). (a, b) Input fundamental current; (c, d) AC fundamental phase currents; (e, f) DC phase currents, (g, h) fundamental output current . Markers indicate measured data; solid lines represent fitted curves.

5.4 Inclusion of the rotor

As shown in Table 5.1, the inverter efficiency is 98.4% in all cases, so any variation in system efficiency is attributable to losses in the EM. Additionally, AC losses are consistently lower for all rotor configurations compared to the stator-only case, indicating that the presence of a rotor reduces the current ripple flowing through the windings.

5.4.1 Current Ripple

As expected from the T2 topology, $I_{fn^*,\text{in}}$ magnitude remains low across all configurations, ranging from 0.044 A in the stator-only case to 0.120 A for EESM position 3.

The stator-only case shows the highest phase current fundamentals, with $I_{fn^*,1} = 2.298$ A and $I_{fn^*,2} = 2.358$ A, yet remains the most balanced configuration, with an difference among the phases of only 0.060 A (2.6%). The introduction of a rotor reduces these values across all cases. The PMSM yields the lowest fundamentals at 0.358 A and 0.368 A, with a difference of only 0.011 A (3.0%), indicating good inductance balance.

The EESM configurations show a stronger sensitivity to rotor position. The imbalance reaches 0.091 A (22.9%) at position 1, decreases to 0.047 A (8.4%) at position 2, and rises again to 0.102 A (21.9%) at position 3. This variation suggests that certain rotor angles produce a more asymmetric effective inductance between the two interleaved branches, degrading current sharing. The position dependence is consistent with the AC loss variation observed in Table 5.2.

The output fundamental current is negligible in the stator-only case at 0.011 A, consistent with effective interleaving cancellation in the absence of rotor-induced asymmetry. For all rotor configurations, it rises to approximately 0.35 A regardless of machine type or rotor position.

Table 5.1: Summary of efficiencies and power for different machine types

Machine	η_{inv}	η_{EM}	η_{sys}	$P_{EM,cu}^{DC}$ (W)	$P_{EM,cu}^{AC}$ (W)
Stator T2	0.984	0.948	0.933	42.64[a]	40.99
EESM (pos 1)	0.984	0.961	0.945	40.28	2.07
EESM (pos 2)	0.984	0.950	0.934	40.41	3.05
EESM (pos 3)	0.984	0.952	0.936	40.47	2.95
PMSM	0.984	0.958	0.942	40.48	1.82

[a] The stator DC copper loss values are scaled from 2.5 kW to 3 kW.

Table 5.2: Fundamental currents for different machine types

Machine	Stator	PMSM	EESM pos 1	EESM pos 2	EESM pos 3
$I_{fn^*,in}$ (A)	0.0443	0.0752	0.0750	0.0747	0.1202
$I_{fn^*,1}$ (A)	2.2978	0.3577	0.4347	0.5636	0.4655
$I_{fn^*,2}$ (A)	2.3578	0.3684	0.3441	0.5162	0.5679
$I_{fn^*,out}$ (A)	0.0112	0.3517	0.3345	0.3508	0.3575

5.5 Topology decision at the experimental power level

At the tested point ($V_{in} = 100V$,$V_{out} = 200V$,$P_{in} = 2.5kW$), T2 is the preferred solution. Both topologies achieve comparable peak system efficiencies (94.4% vs. 93.9%), so efficiency alone does not differentiate them. The decisive advantage of T2 lies in its lower current ripple; the input fundamental is reduced by more than an order of magnitude relative to T1 (0.22 A vs. 8.7 A at 10 kHz), and the output ripple reaches only 0.02 A beyond 30 kHz. This directly relaxes the sizing of input and output filters, reduces AC copper losses in the electrical machine stator, and makes system behaviour less sensitive to the choice of phase shift angle. The near-flat efficiency response of T2 over the phase shift sweep is also operationally attractive, as it add robustness against inductances variation over the operation. The only metric where T1 holds a clear advantage is DC copper losses ($\sim$7 W vs. $\sim$35–40 W), but at this power level that penalty is outweighed by the ripple and filter benefits of T2. Additionally, T2 offers a practical integration advantage, since does not require access to the neutral point, a terminal that is not typically available in traction machines. These considerations make T2 the preferred solution at low power level.

5.6 Efficiency trends for scaled up model

Figures 5.7 (a), (b), (c) and (d) show the system efficiency as a function of input power for both topologies considering three switching frequencies and $V_{in} = 400$ V for the stator and EESM machine cases respectively.

- Considering the stator case. Due to the dominance of DC copper loss over the inverter and AC loss contributions, efficiency in both converter configurations rises from low power to plateaus in the 40–80 kW range before keep near the peak efficiency or declining. Additionally, it has been noted that while T2 performs better at low power, T1 is more efficient at high power.

- The efficiency trends for the EESM case are similar to those for the stator, giving a good indicator on how rotor inclusion can affect the efficiency for charging applications. While T2 shows a noticeable decrease beyond 80 kW, falling from 93% to 90% at 204 kW. T1 peaks at about 94% and stays rather constant up to 204 kW. This difference is again related to T2 DC copper losses which are 4.5 times greater than T1.

5.6.1 Loss breakdown for scaled up model

Figures 5.8 and 5.9 show the distribution of the losses across all operating points. One important finding is that the addition of the rotor shifts the loss contribution from AC copper losses to core losses. This is explained by two competing effects. On one side, the rotor increases the total machine inductance, which reduces the AC ripple current amplitude and consequently the AC copper losses; however, the additional magnetic material introduced by the rotor increases the total core loss, which becomes the dominant contribution across the entire power range.

- In the stator case, DC copper losses grows to become the dominant contribution at high power operation, as expected from the I^2R scaling. AC copper losses are predominant in the low power operation and inverter losses become relevant as the switching frequency increases.

- In EESM, core losses becomes a great contributor of the total losses in both topologies, accounting for 30-65% of total losses depending on the operating point. This is caused by

rotor iron losses, which have complex behaviour. When the inductance reaches saturation, the current ripple increases, resulting in higher AC losses.

This result has an important practical implication. The machine losses dominate the system losses. From these, DC copper losses and core losses are the biggest contributors, so control strategies and new machine designs should focus on how to reduce DC resistance and minimize the phase current ripple at high voltage.

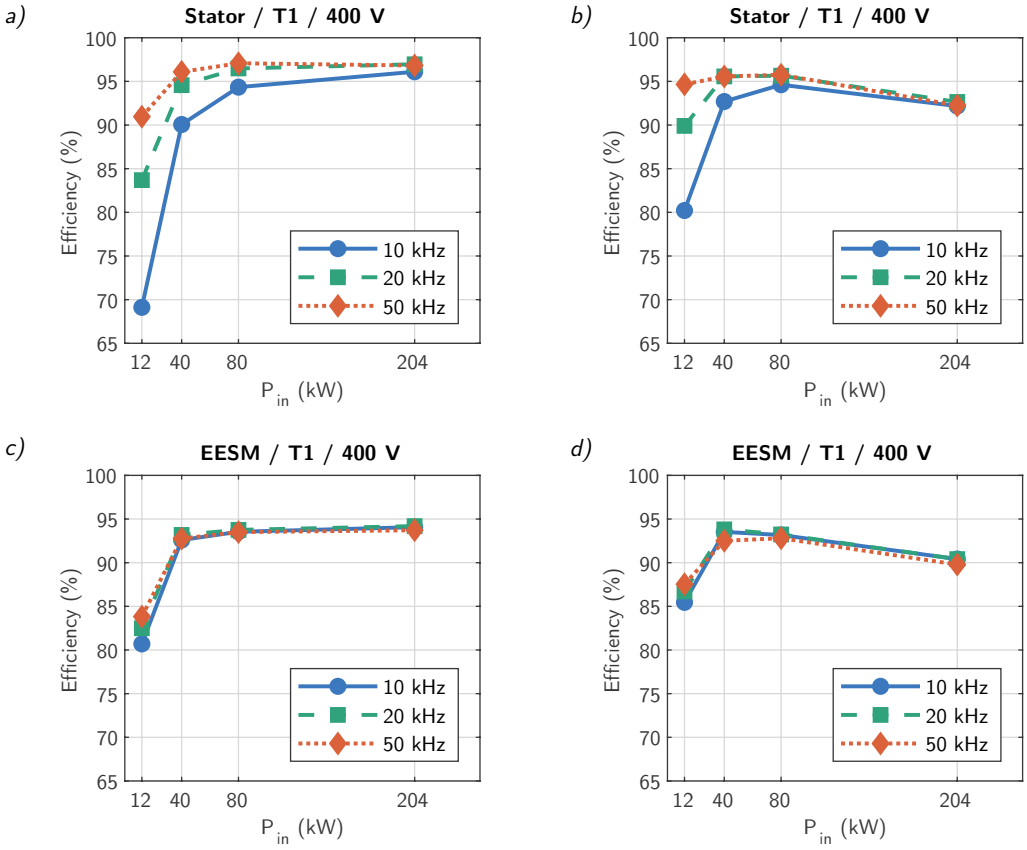

Figure 5.7: Efficiency trend for the only-stator scaled up models

5.6.2 Effect of switching frequency at higher power

For the stator case, increasing the switching frequency from 10 to 20 kHz produces efficiency improvements at low power, where AC copper losses represent a larger fraction of the total. The gain from 20 to 50 kHz is progressively smaller as the converter operates with higher input power, being consistent with the experimental results as shown in Figure 5.7.

For the EESM case, increasing the switching frequency does not produce noticeable changes in system efficiency, since eddy current losses dominate the total losses and the increase in switching frequency has a counteracting effect. Higher switching frequencies produce proportionally lower current ripple, but both variables have a power factor close to two, compensating for their variation. This means that, for the same power level, core losses will be similar at different switching frequencies as shown in Figure 5.9.

Additionally, since the current ripple is already small (<3 A at 400 V), the reduction in AC copper losses with higher switching frequency has a negligible effect on the total losses. This indicates

that increasing the switching frequency beyond 20 kHz is not justified for the EESM configuration from an efficiency point of view, and the choice of switching frequency should instead be guided by current ripple, current harmonics, or acoustic noise requirements.

5.6.3 Thermal Operating Limit

The thermal limit of the machine is set at a combined copper and iron loss of $P_{\mathrm{th}} = 1.8\,\mathrm{kW}$. This limit is evaluated against the EESM results charging scaled up model.

From Figure 5.9, the total machine losses at 40 kW input already exceed 2.5 kW for both topologies at all switching frequencies, surpassing the threshold. Continuous operation is therefore limited to input powers below 40 kW, placing the thermal boundary in the 12–40 kW range. Both topologies reach this limit in this boundary, since the core loss contribution is predominant independently of the topology and driven primarily by the ripple current amplitude rather than the winding configuration. This means that for reaching the nominal charging power is needed a dedicated cooling system.

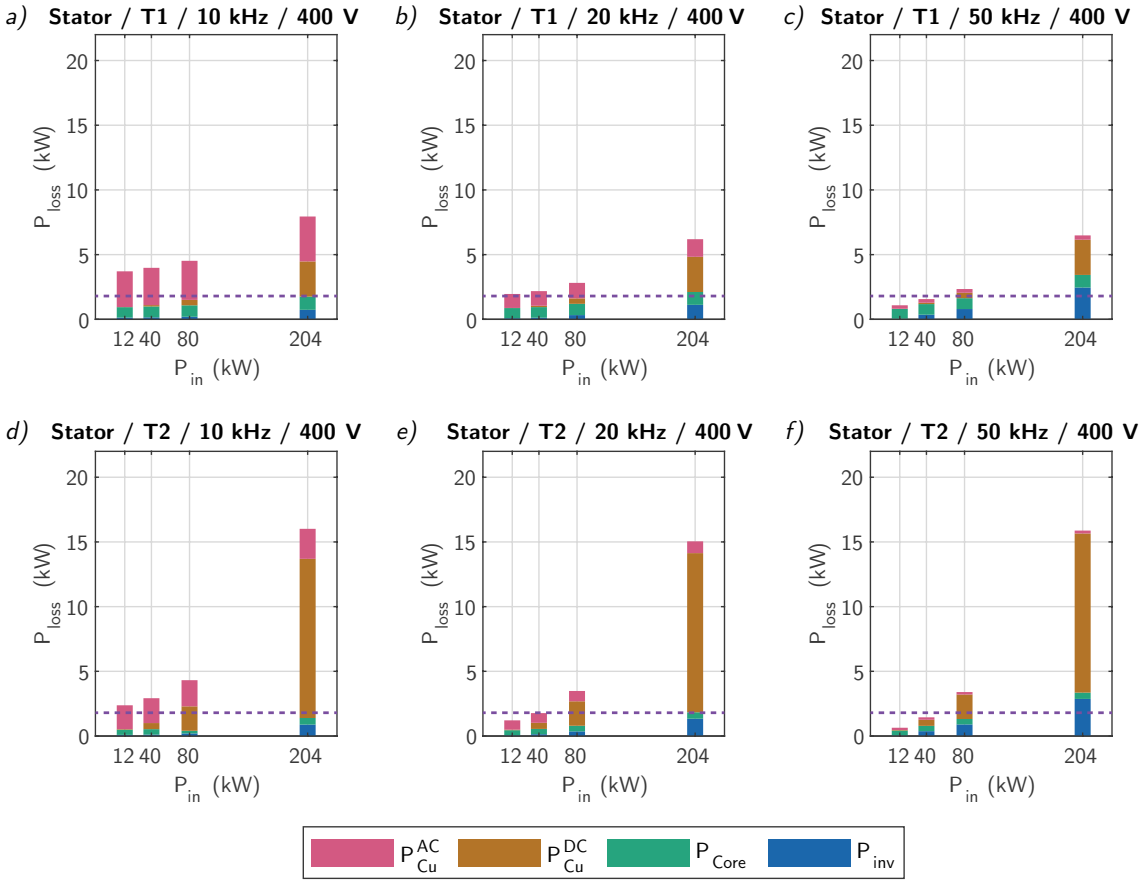

Figure 5.8: Power losses breakdown for the stator-only scaled up model, dashed purple line indicate the machine thermal limit for continuous operation

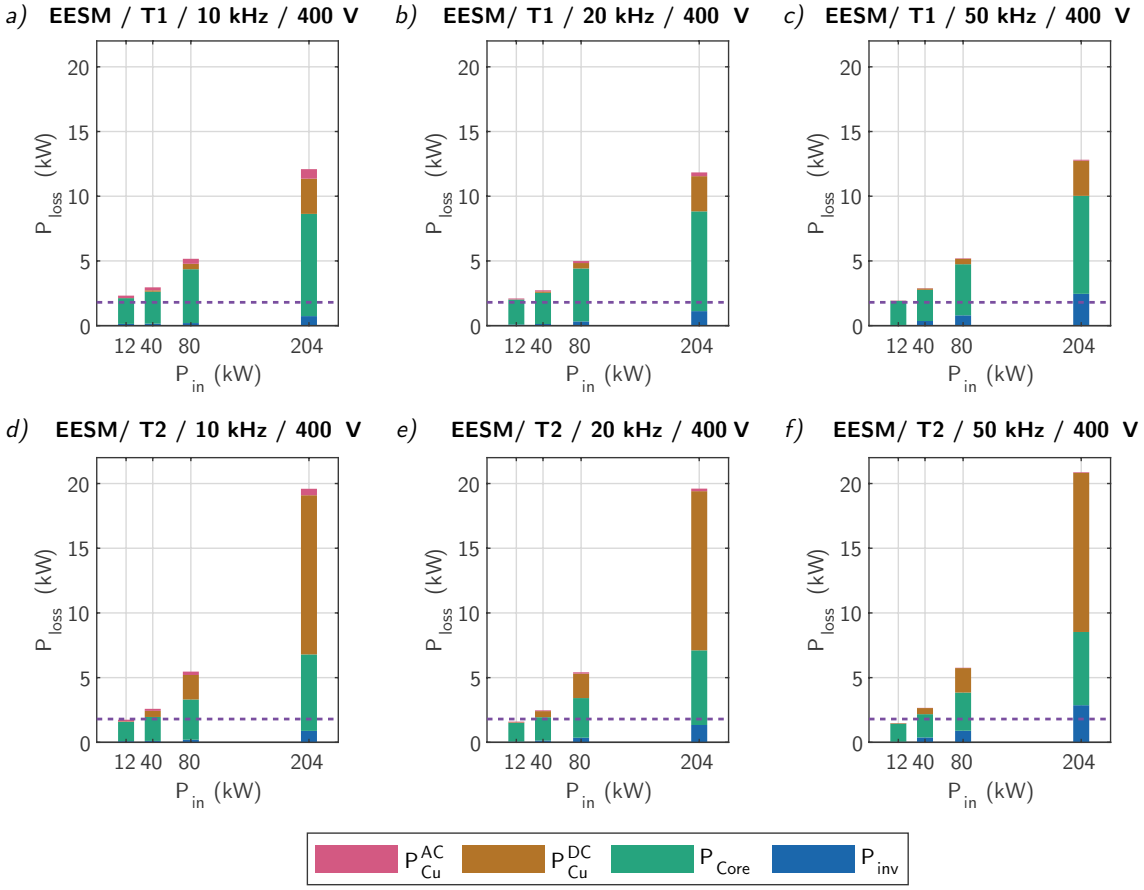

Figure 5.9: Power losses breakdown for EESM scaled up model, dashed purple line indicate the machine thermal limit for continuous operation

5.7 Topology selection overview

Table 5.3 summarises the key performance metrics of both topologies. It compiles the main experimental results and includes a final block with scaled-up simulation results.

Table 5.3: Performance comparison of the two converter topologies at the experimental operating point and simulated scaled-up conditions. Advantage indicators (**A**: advantage, **D**: disadvantage, –: draw) refer to T1 relative to T2.

Metric	T1: 3-phase interleaved	T2: 2-phase series-winding	T1
Efficiency at experimental conditions			
Peak system efficiency	94.4 %	93.9 %	**A**
Peak EM efficiency	≈ 95.9 %	≈ 95 %	**A**
Inverter efficiency	97–99 %	98–99 %	–
Ripple and filter requirements			
Input current ripple	Higher; sensitive to f_{sw} and θ	Lower; near-independent of f_{sw} and θ	**D**
Output current ripple	0.22 A ($f_{\mathrm{sw}} \geq 30$ kHz)	0.02 A	**D**
Filter sizing requirement	Moderate	Relaxed	**D**
Copper losses			
AC copper losses	High at low f_{sw}; phase shift dependent	Generally lower; nearly independent of the phase shift	**D**
DC copper losses	Low (≈ 7 W)	High (≈ 35–40 W)	**A**
Hardware integration			
Neutral-point access required	Yes	No	**D**
Phase shift sensitivity	High	Low	**D**
Scalability to higher power			
AC losses scaling	Higher. 1.5 times higher than T2	Lower. Improves efficiency at low power.	**D**
DC copper loss scaling	Mild (low baseline ≈ 7 W)	Significant (high baseline ≈ 35–40 W). 4.5 times higher than T1	**A**
Thermal stress	Lower DC copper losses, good scalability	Higher $I^2 R_{\mathrm{DC}}$ may constrain scalability	**A**
Efficiency at low power	≈ 83 %; improves with higher switching frequencies	≈ 87 %; improves with higher switching frequencies	**D**
Efficiency at rated power	≈ 94 %; stable up to 204 kW	Decreases from ≈ 93 % to ≈ 90 % at 204 kW	**A**

Chapter 6

Conclusion

This thesis has experimentally investigated the integration of a fast charger with the powertrain of a battery electric vehicle, using the traction inverter and electrical machine stator as active components of an interleaved boost converter. Two topologies were evaluated: a three-phase interleaved configuration (T1) and a two-phase with a series winding configuration (T2). The work characterised system efficiency, power loss contributions, current ripple behaviour, and the effect of rotor inclusion across a range of switching frequencies and phase-shift angles, establishing a quantitative experimental baseline for both topologies.

The experimental results confirm the feasibility of this fast charging system. Both T1 and T2 achieve comparable peak system efficiencies of 94.4% and 93.9%, respectively, demonstrating that efficiency alone does not differentiate the topologies at the tested power level. The decisive differences lie in current ripple behaviour, copper loss distribution, and practical integration constraints.

T2 exhibits lower input and output current ripple. Its input fundamental is reduced by more than an order of magnitude relative to T1 at 10 kHz (0.22 A versus 8.7 A), and its output ripple falls below 0.02 A beyond 30 kHz. Its near flat efficiency response across the full phase shift range makes system behaviour more robust. These properties directly relax input and output filter requirements and reduce AC copper losses in the electrical machine stator. T2 also offers a practical integration advantage over T1 in that it does not require access to the machine neutral point, a terminal not typically exposed in traction machines. At the experimental power level, these advantages make T2 the preferred topology. Additionally, the rotor inclusion experiments under T2 confirmed that all tested configurations; PMSM and EESM at three rotor positions, reduce phase current ripple relative to the stator only case. No mechanical vibrations or acoustic noise were observed during charging, supporting the viability of static charging with the rotor present. In addition, system efficiency was not significantly altered by rotor inclusion.

The scalability analysis reverses this preference at higher power. T1 maintains lower DC copper losses, while T2 incurs losses 4.5 times higher due to its series winding configuration, with both scaling quadratically with current. The loss breakdown for the scaled-up model shows that this trend grows to dominate T2 losses, where T2 efficiency falls from approximately 93% to 90% at 204 kW, while T1 remains near 94%. For the EESM case, core losses account for 30–65% of total system losses depending on operating point and frequency, becoming an important loss mechanism for both topologies. A key finding is that, because both the ripple current and the Steinmetz core-loss exponents are approximately equal ($\alpha \approx \beta \approx 2$), increasing switching frequency in the EESM configuration do not produces huge improvements in efficiency, since the reduction in

ripple amplitude is compensated by the increase in frequency contribution. This result implies that switching frequency selection in EESM-based charging systems should be guided by ripple, harmonics, or acoustic noise requirements rather than efficiency. The thermal analysis further shows that, with EESM, total machine losses already exceed the 1.8 kW continuous limit at input powers below 40 kW, placing strict constraints on full power continuous operation without active cooling.

The results presented here constitute a validated experimental baseline that supports further development of integrated fast chargers, informs machine design decisions for charging-optimised powertrains, and provides a directly comparable dataset for the two topologies across their relevant operating conditions.

6.1 Future Work

The results and limitations of this thesis identify several directions for further research and development:

- **Closed-loop control implementation:** All experiments in this thesis were conducted under open-loop conditions. Implementing closed-loop current and voltage control is essential for stable operation across the full power range, and it requires selection of current and voltage sensors with adequate bandwidth and accuracy.

- **Improved electrical machine loss modelling:** The present loss analysis focuses on copper losses and does not include iron (core) losses in the electrical machine stator. Accurate iron loss estimation requires extraction of the Steinmetz equation parameters for the specific electrical steel used in the stator laminations for high frequencies. Incorporating these losses into the model would improve the accuracy of the scalability analysis and the efficiency predictions at higher switching frequencies and power levels.

- **Full-power testing at nominal operating conditions:** The experimental results were obtained at a reduced power level. Validation at the nominal power level expected for the target application is necessary to confirm the scalability analysis presented in Section 5.5.2, to verify the thermal behaviour of the system under sustained charging conditions.

- **Thermal characterisation and management:** A dedicated thermal study is needed to quantify temperature rise in the inverter switches, electrical machine windings for the high power operation.

- **EMI and common-mode current analysis:**. High-frequency switching in an integrated charger generates common-mode currents that can propagate through the vehicle powertrain and the grid. An electromagnetic interference study, including conducted and radiated emissions characterisation, is required to assess standards compliance.

Appendix A

Measurements

Table A.1: Measured stator's inductances and resistances vs frequency

f	L_1 (μH)	L_2 (μH)	L_3 (μH)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)
1	0	0	0	0.0296	0.0293	0.0290
20	123.83	122.47	123.55	0.03538	0.03504	0.03492
50	121.68	120.71	121.30	0.03485	0.03426	0.03411
100	121.37	120.39	120.98	0.03500	0.03468	0.03452
200	121.96	120.26	120.85	0.03597	0.03565	0.03549
500	120.97	119.96	120.56	0.04263	0.04224	0.04213
1000	120.21	119.23	119.81	0.06491	0.06437	0.06434
2000	117.65	116.69	117.26	0.14185	0.14082	0.14106
5000	109.22	108.33	109.06	0.43536	0.43189	0.43323
10000	102.21	101.35	101.83	0.77520	0.77122	0.77176
15000	99.40	98.56	99.02	1.0390	1.0360	1.0369
20000	97.85	97.00	97.49	1.3044	1.3012	1.3028
25000	96.90	96.05	96.54	1.5825	1.5812	1.5820
30000	96.17	95.32	95.81	1.8727	1.8729	1.8725
35000	94.71	94.71	95.20	2.1776	2.1792	2.1784
40000	95.11	94.25	94.74	2.4935	2.5000	2.4983
45000	94.74	93.87	94.35	2.8204	2.8290	2.8277
50000	94.43	93.56	94.05	3.1609	3.1737	3.1671
55000	94.18	93.30	93.79	3.5131	3.5321	3.5208
60000	94.04	93.14	93.63	3.8802	3.9024	3.8915
65000	93.95	93.06	93.56	4.2610	4.2883	4.2727
70000	93.93	93.03	93.52	4.6526	4.6889	4.6702
75000	94.00	93.08	93.58	5.0672	5.1059	5.0850
80000	94.09	93.15	93.66	5.4952	5.5395	5.5150
90000	94.39	93.43	93.94	6.4033	6.5491	6.4260
100000	94.91	93.92	94.43	7.3888	7.4546	7.4144
120000	96.62	95.44	96.07	9.6599	9.7508	9.6827
150000	100.39	99.16	99.74	14.0300	14.1500	14.0480
200000	112.30	110.66	111.36	26.2360	26.2380	26.1120

Table A.2: PMSM inductances between phases vs frequency

f (Hz)	$L_3 - L_2$ (μH)	$L_2 - L_1$ (μH)	$L_3 - L_1$ (μH)
20	1160	1870	974
10000	1034	1740	850
50000	723	1110	606
60000	667	991	563

Table A.3: EESM position 1 inductances between phases vs frequency

f (Hz)	$L_3 - L_2$ (μH)	$L_2 - L_1$ (μH)	$L_3 - L_1$ (μH)
20	1810	2068.5	1840
10000	1600	1870	1400
50000	831	1118.6	960
60000	857	988	744

Table A.4: EESM position 2 inductances between phases vs frequency

f (Hz)	$L_3 - L_2$ (μH)	$L_2 - L_1$ (μH)	$L_3 - L_1$ (μH)
20	2060	1830	1950
10000	1870	1390	1630
50000	1110	825	974
60000	988	740	869

Table A.5: EESM position 3 inductances between phases vs frequency

f (Hz)	$L_3 - L_2$ (μH)	$L_2 - L_1$ (μH)	$L_3 - L_1$ (μH)
20	1850	1940	2120
10000	1415.8	1590	1910
50000	835	954	1130
60000	749	852	1000

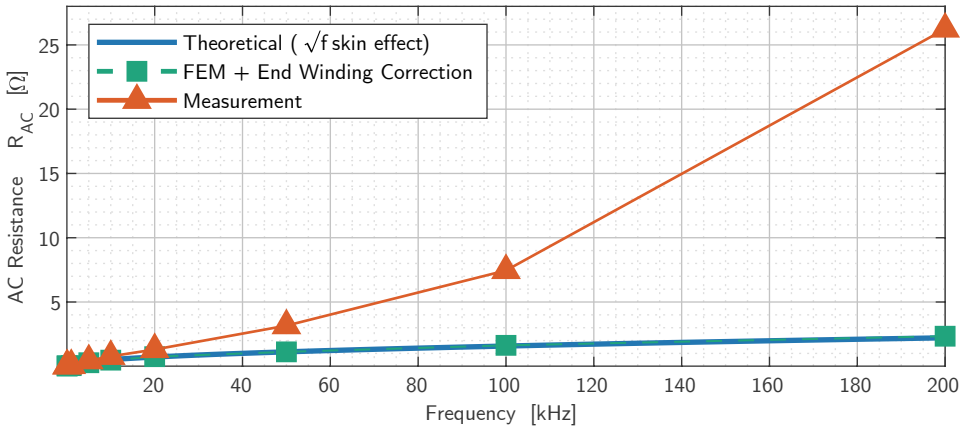

Figure A.1: AC winding resistance comparison between measurement (orange), ANSYS Maxwell FEM simulation (green) and theoretical skin effect trend (blue).

Table A.6: ANSYS Maxwell core loss simulation matrix used for Steinmetz exponent extraction

$I_{\text{ripple,rms}}$ [A]	I_{DC} [A]	f_{sw} [Hz]	$P_{\text{EM,eddy}}$ [W]	$P_{\text{EM,hyst}}$ [W]
10	170	500	0.07749	0.04360
20	170	500	0.30987	0.17347
50	170	500	1.87000	1.03000
100	170	500	7.95000	3.98000
50	10	500	1.75000	1.04000
50	33	500	1.83000	1.00000
50	66	500	1.89000	1.04000
50	170	500	1.87000	1.03000
50	170	100	0.36500	0.06400
50	170	500	1.87000	1.03000
50	170	1000	28.91000	2.83000
50	170	5000	620.0000	25.8200

A.1 Efficiency and power losses measurements

Table A.7: Power and efficiency measurements for T1 frequency sweep ($V_{in} = 100V$, $V_{out} = 200V$, $\theta = 120°$)

f_{sw} (kHz)	P_{in} (W)	P_{out} (W)	P_{loss} (W)	$P_{\mathrm{inv,losses}}$ (W)	$P_{\mathrm{EM,losses}}$ (W)	η_{sys} (-)	η_{inv} (-)	η_{EM} (-)
10	2514.29	2132.39	381.90	21.99	359.90	0.8481	0.9913	0.8569
20	2519.35	2298.27	221.08	22.27	198.81	0.9122	0.9912	0.9211
30	2520.52	2358.18	162.33	23.35	138.98	0.9356	0.9907	0.9449
40	2520.69	2361.83	158.86	30.07	128.78	0.9370	0.9881	0.9489
50	2512.48	2371.81	140.66	38.79	101.87	0.9440	0.9846	0.9595
60	2519.52	2360.02	159.50	47.42	112.07	0.9367	0.9812	0.9555
70	2526.43	2335.84	190.59	53.14	137.44	0.9246	0.9790	0.9456
80	2509.63	2329.35	180.28	60.08	120.20	0.9282	0.9761	0.9521
90	2503.21	2294.29	208.92	67.58	141.34	0.9165	0.9730	0.9435
100	2526.57	2289.29	237.28	74.78	162.50	0.9061	0.9704	0.9357

Table A.8: EM losses breakdown for T1 frequency sweep ($V_{in} = 100\,\mathrm{V}$, $V_{out} = 200\,\mathrm{V}$, $\theta = 120°$)

f_{sw}	$P_{\mathrm{EM,losses}}$	$P_{EM,cu}^{DC,1}$	$P_{EM,cu}^{DC,2}$	$P_{EM,cu}^{DC,3}$	$P_{EM,cu}^{AC,1}$	$P_{EM,cu}^{AC,2}$	$P_{EM,cu}^{AC,3}$	$P_{EM,cu}^{DC}$	$P_{EM,cu}^{AC}$	$P_{EM,cu}$	Other Losses
10	359.90	2.06	2.07	2.32	106.97	110.60	109.43	6.45	327.00	333.45	26.45
20	198.81	2.04	2.03	2.49	51.78	54.10	52.72	6.55	158.60	165.15	33.66
30	138.98	1.98	1.98	2.52	36.60	38.34	37.10	6.48	112.03	118.52	20.46
40	128.78	1.91	1.86	2.77	29.99	30.96	30.62	6.54	91.57	98.12	30.67
50	101.87	2.10	1.91	2.84	28.73	30.04	28.35	6.85	87.12	93.97	7.90
60	112.07	2.15	1.75	2.95	27.17	28.21	26.64	6.85	82.01	88.86	23.21
70	137.44	2.00	1.81	3.05	26.30	27.36	25.43	6.86	79.09	85.94	51.50
80	120.20	2.00	1.81	3.05	26.03	26.83	24.97	6.87	77.83	84.70	35.50
90	141.34	2.00	1.79	3.13	25.67	26.18	24.35	6.92	76.20	83.12	58.23
100	162.50	1.99	1.77	3.14	25.98	26.48	24.20	6.90	76.66	83.56	78.94

Table A.9: Power and efficiency measurements for T1 phase-shift sweep ($V_{in} = 100V$, $V_{out} = 200V$, $f_{sw} = 50kHz$)

θ (°)	P_{in} (W)	P_{out} (W)	P_{loss} (W)	$P_{\mathrm{inv,losses}}$ (W)	$P_{\mathrm{EM,losses}}$ (W)	η_{sys} (-)	η_{inv} (-)	η_{EM} (-)
0	2518.95	2124.54	394.40	50.42	343.98	0.8434	0.9800	0.8634
20	2521.58	2125.63	395.95	40.44	355.51	0.8430	0.9840	0.8590
40	2520.74	2160.14	360.60	37.02	323.58	0.8569	0.9853	0.8716
60	2519.52	2219.14	300.37	36.86	263.52	0.8808	0.9854	0.8954
80	2520.89	2260.91	259.98	37.53	222.46	0.8969	0.9851	0.9118
100	2527.76	2341.67	186.09	37.83	148.26	0.9264	0.9850	0.9413
120	2525.32	2364.58	160.74	38.91	121.83	0.9364	0.9846	0.9518

Table A.10: EM losses breakdown vs phase shift

Phase shift	$P_{\text{EM,losses}}$	$P_{EM,cu}^{DC,1}$	$P_{EM,cu}^{DC,2}$	$P_{EM,cu}^{DC,3}$	$P_{EM,cu}^{AC,1}$	$P_{EM,cu}^{AC,2}$	$P_{EM,cu}^{AC,3}$	$P_{EM,cu}^{DC}$	$P_{EM,cu}^{AC}$	$P_{EM,cu}$	Other Losses
0	343.98	2.04	1.94	2.72	116.51	122.50	118.08	6.69	357.08	363.78	-19.80
20	355.51	1.90	1.91	2.92	98.71	109.92	103.00	6.73	311.63	318.37	37.15
40	323.58	1.86	1.89	3.06	77.37	93.72	82.87	6.80	253.95	260.75	62.84
60	263.52	1.88	1.83	3.09	54.14	74.82	59.26	6.80	188.23	195.03	68.49
80	222.46	1.96	1.79	3.04	33.90	56.49	37.31	6.80	127.70	134.50	87.96
100	148.26	2.02	1.80	2.96	24.75	40.08	25.64	6.78	90.47	97.26	51.01
120	121.83	2.10	1.88	1.88	29.14	29.14	30.11	5.86	88.40	94.26	27.57

Table A.11: Power and efficiency measurements for T2 frequency sweep ($V_{in} = 100V$, $V_{out} = 200V$, $\theta = 180°$)

f_{sw} (kHz)	P_{in} (W)	P_{out} (W)	P_{loss} (W)	$P_{\text{inv,losses}}$ (W)	$P_{\text{EM,losses}}$ (W)	η_{sys} (-)	η_{inv} (-)	η_{EM} (-)
10	2515.01	2212.39	302.62	13.38	289.24	0.8797	0.9947	0.8850
20	2516.35	2339.14	177.21	17.06	160.15	0.9296	0.9932	0.9364
30	2514.79	2362.76	152.03	24.82	127.21	0.9395	0.9901	0.9494
40	2527.69	2368.53	159.15	33.26	125.90	0.9370	0.9868	0.9502
50	2520.75	2352.20	168.55	38.90	129.65	0.9331	0.9846	0.9486
60	2528.80	2336.92	191.88	46.65	145.23	0.9241	0.9816	0.9426
70	2526.35	2325.20	201.15	57.47	143.68	0.9204	0.9773	0.9431
80	2975.39	2743.36	232.03	72.59	159.44	0.9220	0.9756	0.9464
90	2535.40	2295.19	240.21	73.68	166.53	0.9053	0.9709	0.9343
100	2546.83	2289.00	257.83	80.02	177.81	0.8988	0.9686	0.9302

Table A.12: EM losses breakdown for T2 frequency sweep ($V_{in} = 100V$, $V_{out} = 200V$, $\theta = 120°$)

f_{sw}	$P_{\text{EM,losses}}$	$P_{EM,cu}^{DC,1}$	$P_{EM,cu}^{DC,2}$	$P_{EM,cu}^{DC,3}$	$P_{EM,cu}^{AC,1}$	$P_{EM,cu}^{AC,2}$	$P_{EM,cu}^{AC,3}$	$P_{EM,cu}^{DC}$	$P_{EM,cu}^{AC}$	$P_{EM,cu}$	Other Losses
10	289.24	4.87	4.96	19.73	91.89	95.26	0.19	29.56	187.35	216.91	72.33
20	160.15	4.90	4.96	19.75	42.72	44.27	0.09	29.61	87.07	116.69	43.46
30	127.21	4.88	4.96	19.68	29.92	30.87	0.23	29.52	61.01	90.54	36.67
40	125.90	4.90	4.85	19.83	24.43	24.79	0.36	29.58	49.59	79.17	46.73
50	129.65	4.91	4.90	19.81	20.31	20.49	0.19	29.62	41.00	70.61	59.04
60	145.23	5.00	4.80	19.72	18.37	18.26	0.40	29.52	37.03	66.55	78.68
70	143.68	5.07	4.78	19.72	16.22	16.27	0.44	29.58	32.93	62.50	81.18
80	159.44	6.07	7.97	26.57	13.75	14.51	0.04	40.61	28.29	68.90	90.54
90	166.53	5.00	4.90	19.53	19.53	13.55	0.27	29.42	33.34	62.77	103.76
100	177.81	5.02	4.90	19.64	11.82	12.22	0.14	29.56	24.17	53.73	124.08

Table A.13: Power and efficiency measurements for T2 phase-shift sweep ($V_{in} = 100V$, $V_{out} = 200V$, $F_{sw} = 50kHz$)

θ (°)	P_{in} (W)	P_{out} (W)	P_{loss} (W)	$P_{\text{inv,losses}}$ (W)	$P_{\text{EM,losses}}$ (W)	η (-)	η_{sys} (-)	η_{EM} (-)
0	2534.32	2370.41	163.91	40.27	123.65	0.9353	0.9841	0.9512
30	2533.90	2381.88	152.02	39.28	112.74	0.9400	0.9845	0.9555
60	2526.40	2393.03	133.37	38.80	94.57	0.9472	0.9846	0.9626
90	2529.80	2408.17	121.63	38.65	82.98	0.9519	0.9847	0.9672
120	2527.25	2377.48	149.77	39.08	110.70	0.9407	0.9845	0.9562
150	2525.56	2370.18	155.38	39.58	115.80	0.9385	0.9843	0.9541
180	2530.60	2372.20	158.40	38.23	120.18	0.9374	0.9849	0.9525

Table A.14: Power and efficiency measurements for EESM at different rotor position ($V_{in} = 100V$, $V_{out} = 200V$, $F_{sw} = 50kHz$, $\theta = 180°$)

Pos	P_{in} (W)	P_{out} (W)	P_{loss} (W)	$P_{\text{inv,losses}}$ (W)	$P_{\text{EM,losses}}$ (W)	η (-)	η_{sys} (-)	η_{EM} (-)
Pos 1	2990.79	2826.78	164.00	47.85	116.16	0.9452	0.9840	0.9612
Pos 2	2997.61	2800.30	197.31	47.55	149.76	0.9342	0.9841	0.9500
Pos 3	2993.16	2803.54	189.62	47.90	141.72	0.9366	0.9840	0.9527

Table A.15: EM losses breakdown for different positions

Position	$P_{\text{EM,loss}}$	$P_{EM,cu}^{DC,1}$	$P_{EM,cu}^{DC,2}$	$P_{EM,cu}^{DC,3}$	$P_{EM,cu}^{AC,1}$	$P_{EM,cu}^{AC,2}$	$P_{EM,cu}^{AC,3}$	$P_{EM,cu}^{DC}$	$P_{EM,cu}^{AC}$	$P_{EM,cu}$	Other Losses
Pos 1	116.16	6.92	6.77	26.59	0.84	0.70	0.54	40.28	2.07	42.36	73.80
Pos 2	149.76	6.92	6.76	26.74	1.32	1.23	0.50	40.42	3.05	43.32	106.44
Pos 3	141.72	6.93	6.74	26.80	0.95	1.47	0.54	40.47	2.96	43.43	98.29

Table A.16: Power and efficiency measurements for PMSM at the fixed rotor position ($V_{in} = 100V$, $V_{out} = 200V$, $F_{sw} = 50kHz$, $\theta = 180°$)

Pos (°)	P_{in} (W)	P_{out} (W)	P_{loss} (W)	$P_{\text{inv,losses}}$ (W)	$P_{\text{EM,losses}}$ (W)	η (-)	η_{sys} (-)	η_{EM} (-)
Pos 1	2990.23	2817.57	172.66	47.75	124.91	0.9423	0.9840	0.9582

Table A.17: EM losses breakdown for Position 1

$P_{\text{EM,loss}}$	$P_{EM,cu}^{DC,1}$	$P_{EM,cu}^{DC,2}$	$P_{EM,cu}^{DC,3}$	$P_{EM,cu}^{AC,1}$	$P_{EM,cu}^{AC,2}$	$P_{EM,cu}^{AC,3}$	$P_{EM,cu}^{DC}$	$P_{EM,cu}^{AC}$	$P_{EM,cu}$	Other Losses
124.91	6.90	6.64	26.94	0.59	0.74	0.49	40.48	1.82	42.30	82.61

A.2 Current measurements

Table A.18: Current measurements for T1 frequency sweep ($V_{in} = 100\,\mathrm{V}$, $V_{out} = 200\,\mathrm{V}$, $\theta = 120°$)

Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	f_{sw} (kHz)
I_{in}	25.9707	27.4943	31.3757	8.9194	10
I_1	8.3385	13.8685	43.8322	10.6465	10
I_2	8.3716	14.0484	44.5022	10.8280	10
I_3	8.8568	14.3022	44.2337	10.7896	10
I_{out}	10.5961	10.7004	4.2870	1.4838	10
I_{in}	25.9949	26.4081	16.2880	4.5882	20
I_1	8.2926	10.1080	22.8859	5.5498	20
I_2	8.2725	10.1649	23.2612	5.6661	20
I_3	9.1651	10.8683	22.9685	5.6097	20
I_{out}	11.4913	11.4976	1.2839	0.3578	20
I_{in}	25.9020	26.0876	10.7336	3.0660	30
I_1	8.1820	9.0818	15.7196	3.7758	30
I_2	8.1724	9.1141	15.8510	3.8636	30
I_3	9.2350	10.0550	15.6502	3.8114	30
I_{out}	11.7908	11.7932	0.8510	0.2010	30
I_{in}	25.9395	26.0430	7.7904	2.2942	40
I_1	8.0439	8.5854	12.0914	2.8659	40
I_2	7.9250	8.4999	12.0243	2.9365	40
I_3	9.6827	10.1436	11.8491	2.8910	40
I_{out}	11.8091	11.8108	0.7850	0.7850	40
I_{in}	26.1118	26.1789	6.3851	1.8482	50
I_1	8.4146	8.7542	9.5950	2.3017	50
I_2	8.0423	8.4174	9.7488	2.3676	50
I_3	9.7881	10.0873	9.5337	2.3266	50
I_{out}	11.8591	11.8613	0.9008	0.2129	50
I_{in}	25.8335	25.8806	5.2131	1.5455	60
I_1	8.5218	8.7631	8.0660	1.9414	60
I_2	7.6934	7.9748	8.1874	1.9965	60
I_3	9.9827	10.1928	8.0109	1.9597	60
I_{out}	11.8002	11.8008	0.4178	0.0787	60
I_{in}	26.0226	26.0565	4.6312	1.3125	70
I_1	8.2192	8.4056	6.8835	1.6673	70
I_2	7.8233	8.0301	7.0460	1.7150	70
I_3	10.1458	10.2985	6.8474	1.6759	70

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Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	f_{sw} (kHz)
I_{out}	11.6791	11.6850	1.1552	0.3674	70
I_{in}	26.0262	26.0520	3.7989	1.1494	80
I_1	8.2179	8.3626	6.1172	1.4623	80
I_2	7.8270	7.9877	6.1756	1.5054	80
I_3	10.1560	10.2750	5.9917	1.4759	80
I_{out}	11.6467	11.6470	0.4103	0.0741	80
I_{in}	25.9748	25.9951	3.3005	1.0160	90
I_1	8.2228	8.3385	5.3837	1.3018	90
I_2	7.7776	7.9073	5.5059	1.3425	90
I_3	10.2768	10.3711	5.3407	1.3164	90
I_{out}	11.4714	11.4718	0.3702	0.0810	90
I_{in}	25.8905	25.9067	3.5302	0.9098	100
I_1	8.1951	8.2905	4.9674	1.1757	100
I_2	7.7224	7.8292	4.9422	1.2101	100
I_3	10.3049	10.3812	4.7660	1.1830	100
I_{out}	11.4464	11.4473	0.4477	0.1423	100

Table A.19: Current measurements for T1 phase-shift sweep ($V_{in} = 100V$, $V_{out} = 200V$, $F_{sw} = 50kHz$)

Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	θ (°)
I_{in}	25.9533	30.8926	57.4635	16.6168	0
I_1	8.2995	10.0657	21.1118	5.6355	0
I_2	8.0884	9.9845	21.7673	5.7931	0
I_3	9.5828	11.1851	20.8585	5.7106	0
I_{out}	10.6228	10.7174	5.0072	1.3549	0
I_{in}	25.9628	30.4903	48.8628	15.9280	20
I_1	8.0185	9.6799	16.9833	5.3971	20
I_2	8.0281	9.8477	18.3313	5.6695	20
I_3	9.9343	11.3882	17.7609	5.5420	20
I_{out}	10.6282	10.7080	4.0120	1.2975	20
I_{in}	25.9783	29.5257	40.4880	14.0246	40
I_1	7.9183	9.2427	13.8011	4.7538	40
I_2	7.9806	9.5717	16.5680	5.2732	40
I_3	10.1654	11.3155	15.4655	4.9581	40
I_{out}	10.8007	10.8659	4.0694	1.1339	40
I_{in}	25.9523	28.1950	31.7598	10.9865	60
I_1	7.9747	8.8635	11.1959	3.8387	60
I_2	7.8658	9.1502	14.7737	4.6648	60
I_3	10.2138	11.0069	12.9568	4.0748	60
I_{out}	11.0958	11.1326	2.9974	0.8955	60
I_{in}	25.9437	26.9848	23.2122	7.3934	80
I_1	8.1462	8.6472	8.8605	2.8714	80
I_2	7.7715	8.7141	13.1457	3.9210	80
I_3	10.1422	10.6141	10.3250	3.1038	80
I_{out}	11.3044	11.3238	2.4425	0.6071	80
I_{in}	26.0505	26.3307	14.7830	3.5725	100
I_1	8.2654	8.5837	8.4860	2.2486	100
I_2	7.8078	8.4326	11.3577	3.1276	100
I_3	9.9955	10.2913	8.8289	2.3904	100
I_{out}	11.7083	11.7140	1.5249	0.2870	100
I_{in}	25.9931	26.0675	6.6098	1.9415	120
I_1	8.4142	8.7572	9.6152	2.3137	120
I_2	7.9783	8.3589	9.7676	2.3767	120
I_3	9.6980	10.0017	9.5281	2.3343	120
I_{out}	11.8230	11.8253	0.9521	0.2183	120

Table A.20: Current measurements for T2 frequency sweep ($V_{in} = 100V$, $V_{out} = 200V$, $F_{sw} = 50kHz$)

Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	f_{sw} (kHz)
I_{in}	25.7196	25.7211	1.7358	0.2271	10
I_1	12.8236	16.7267	37.1297	10.6545	10
I_2	12.9448	16.9450	37.6065	10.8482	10
I_3	25.8196	25.8211	1.7358	0.2271	10
I_{out}	11.1620	11.1741	1.4601	0.5112	10
I_{in}	25.8320	25.8324	0.6702	0.1100	20
I_1	12.8694	14.0380	19.7157	5.5631	20
I_2	12.9436	14.1489	19.8970	5.6698	20
I_3	25.8320	25.8324	0.6702	0.1100	20
I_{out}	11.6957	11.6962	0.3608	0.1059	20
I_{in}	25.7881	25.7882	1.3025	0.0713	30
I_1	12.8367	13.3887	13.7343	3.7754	30
I_2	12.9468	13.5170	13.7158	3.8542	30
I_3	25.7881	25.7882	1.3025	0.0713	30
I_{out}	11.8137	11.8137	0.1923	0.0219	30
I_{in}	25.8831	25.8833	1.1129	0.0555	40
I_1	12.8598	13.1797	10.6144	2.8640	40
I_2	12.8016	13.1367	10.4118	2.9254	40
I_3	25.8831	25.8833	1.1129	0.0555	40
I_{out}	11.8427	11.8427	0.1799	0.0130	40
I_{in}	25.8697	25.8698	1.7159	0.0443	50
I_1	12.8796	13.0860	8.2338	2.2978	50
I_2	12.8631	13.0807	8.5034	2.3578	50
I_3	25.8697	25.8698	1.7159	0.0443	50
I_{out}	11.7610	11.7610	0.1599	0.0112	50
I_{in}	25.8086	25.8087	0.5040	0.0315	60
I_1	12.9952	13.1411	7.1421	1.9371	60
I_2	12.7343	12.8891	7.1308	1.9770	60
I_3	25.8086	25.8087	0.5040	0.0315	60
I_{out}	11.6845	11.6845	0.1674	0.0104	60
I_{in}	25.8119	25.8120	1.1358	0.0247	70
I_1	13.0901	13.1962	6.4090	1.6580	70
I_2	12.7107	12.8251	6.4121	1.6973	70
I_3	25.8119	25.8120	1.1358	0.0247	70
I_{out}	11.6260	11.6260	0.1995	0.0198	70
I_{in}	30.0104	30.0104	0.5442	0.0448	80

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Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	f_{sw} (kHz)
I_1	14.3228	14.3970	5.6774	1.4500	80
I_2	16.4164	16.4855	5.5490	1.4973	80
I_3	30.0104	30.0104	0.5442	0.0448	80
I_{out}	13.7171	13.7171	0.6857	0.0072	80
I_{in}	25.6844	25.6844	0.5053	0.0273	90
I_1	12.9928	13.0566	4.6241	1.2792	90
I_2	12.8677	12.9363	4.5436	1.3213	90
I_3	25.6844	25.6844	0.5053	0.0273	90
I_{out}	11.6259	11.6259	0.1938	0.0124	90
I_{in}	25.7578	25.7579	1.3258	0.0199	100
I_1	13.0222	13.0737	4.1908	1.1516	100
I_2	12.8700	12.9255	4.0839	1.1893	100
I_3	25.7578	25.7579	1.3258	0.0199	100
I_{out}	11.1751	11.1751	0.1155	0.0110	100

Table A.21: Current measurements for T2 phase-shift sweep

Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	θ (°)
I_{in}	25.8384	25.8831	8.1998	1.5076	0
I_1	12.9581	12.9857	4.6934	0.8125	0
I_2	12.7808	12.8093	4.5572	0.8278	0
I_3	25.8384	25.8831	8.1998	1.5076	0
I_{out}	11.8521	11.8540	0.8258	0.2094	0
I_{in}	25.6435	25.6850	4.7317	1.4540	30
I_1	12.7095	12.7503	4.3097	0.9881	30
I_2	13.0674	13.1086	3.9490	1.0082	30
I_3	25.7935	25.8348	4.7317	1.4540	30
I_{out}	11.9094	11.9112	0.5985	0.2017	30
I_{in}	25.8192	25.8521	4.7931	1.3030	60
I_1	12.5061	12.5829	5.2556	1.3567	60
I_2	13.2630	13.3385	4.8332	1.3860	60
I_3	25.8192	25.8521	4.7931	1.3030	60
I_{out}	11.9651	11.9665	0.5532	0.1787	60
I_{in}	25.8130	25.8349	3.3703	1.0560	90
I_1	12.4342	12.5568	6.1329	1.7321	90
I_2	13.3300	13.4493	5.7504	1.7687	90
I_3	25.8130	25.8349	3.3703	1.0560	90
I_{out}	12.0409	12.0418	0.6190	0.1453	90
I_{in}	25.8410	25.8521	2.0965	0.7403	120

Continued on next page

Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	θ (°)
I_1	12.5241	12.6905	7.0258	2.0371	120
I_2	13.2669	13.4312	6.6662	2.0848	120
I_3	25.8410	25.8521	2.0965	0.7403	120
I_{out}	11.8874	11.8879	0.3938	0.1019	120
I_{in}	25.8197	25.8229	1.2133	0.3790	150
I_1	12.6758	12.8735	7.8928	2.2332	150
I_2	13.0919	13.2927	7.6212	2.2880	150
I_3	25.8197	25.8229	1.2133	0.3790	150
I_{out}	11.8510	11.8511	0.4070	0.0551	150
I_{in}	25.8697	25.8698	1.7159	0.0443	180
I_1	12.8796	13.0860	8.2338	2.2978	180
I_2	12.8631	13.0807	8.5034	2.3578	180
I_3	25.8697	25.8698	1.7159	0.0443	180
I_{out}	11.8610	11.8610	0.1599	0.0112	180

Table A.22: Current measurements for EESM at different rotor position

Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	Position
I_{in}	29.9726	29.9732	1.5173	0.0750	1
I_1	15.2940	15.3005	1.7106	0.4347	1
I_2	15.1186	15.1231	1.7974	0.3441	1
I_3	29.9726	29.9732	1.5173	0.0750	1
I_{out}	14.1341	14.1382	1.3848	0.3345	1
I_{in}	30.0528	30.0533	1.3464	0.0747	2
I_1	15.2900	15.3008	2.0981	0.5636	2
I_2	15.1146	15.1242	2.2620	0.5162	2
I_3	30.0528	30.0533	1.3464	0.0747	2
I_{out}	14.0017	14.0062	1.4121	0.3508	2
I_{in}	30.2896	30.2903	1.5455	0.1202	3
I_1	15.3035	15.3109	1.7800	0.4655	3
I_2	15.0916	15.1031	2.3830	0.5679	3
I_3	30.2896	30.2903	1.5455	0.1202	3
I_{out}	14.0179	14.0227	1.5090	0.3575	3

Table A.23: Current measurements for PMSM at the fixed rotor position

Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	Position
I_{in}	30.1656	30.1661	1.3822	0.0752	aligned
I_1	15.2692	15.2737	1.5365	0.3577	aligned

Continued on next page

Signal	I_{DC} (A)	I_{RMS} (A)	ΔI_{pp} (A)	I_{fn^*} (A)	Position
I_2	14.9818	14.9870	1.8330	0.3684	aligned
I_3	30.1656	30.1661	1.3822	0.0752	aligned
I_{out}	14.0880	14.0926	1.1156	0.3517	aligned

A.3 Oscilloscope waveforms

A.3.1 T1 frequency sweep waveforms

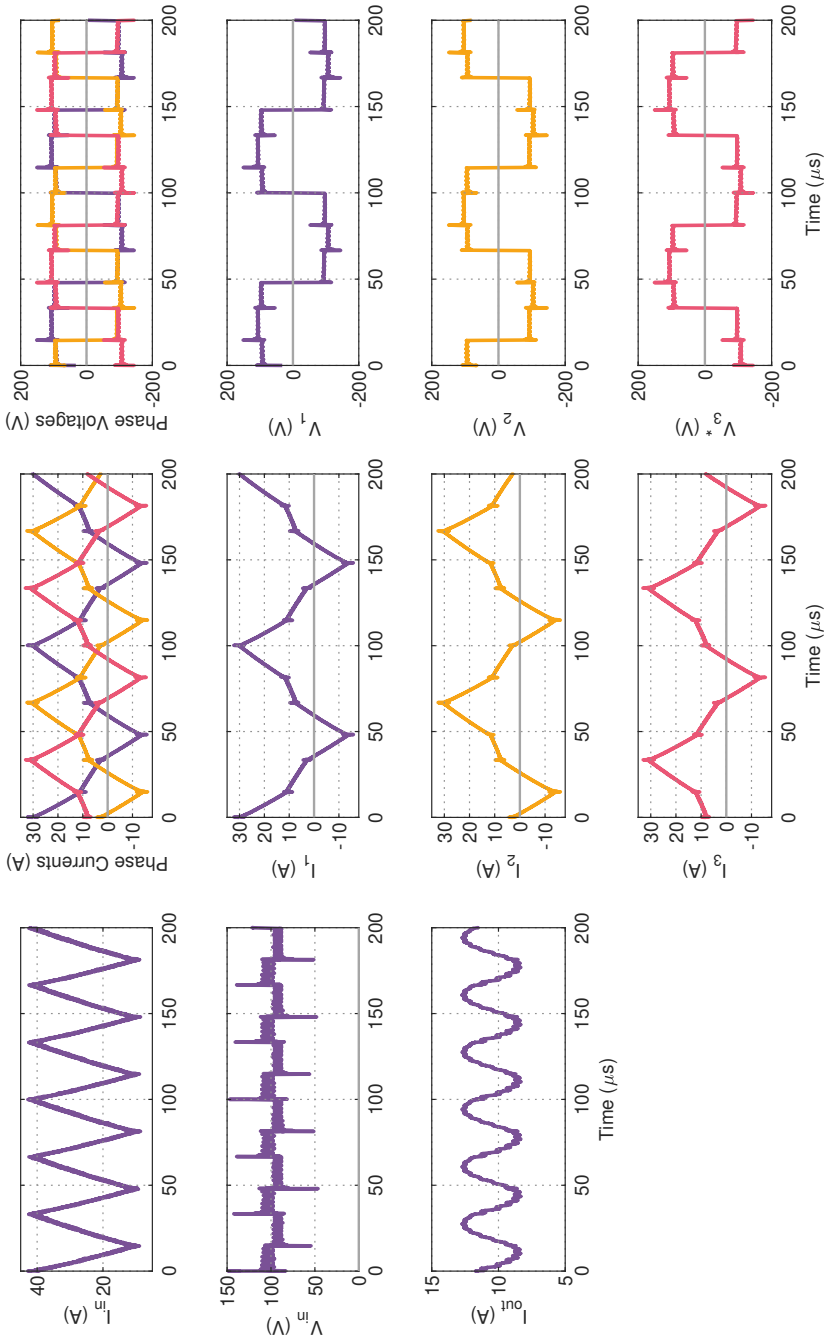

Figure A.2: T1 frequency sweep $F_{sw} = 10kHz$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

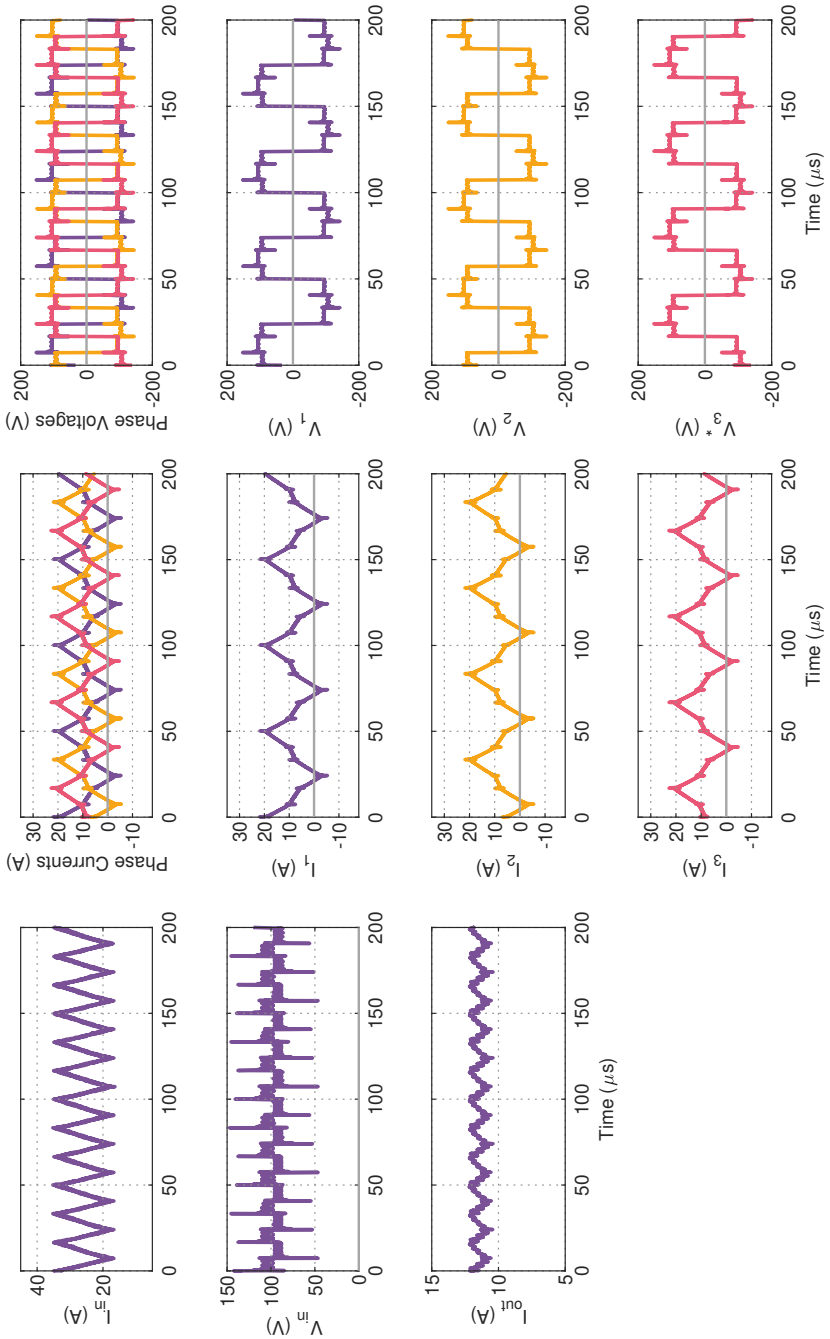

Figure A.3: T1 frequency sweep $F_{sw} = 20kHz$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

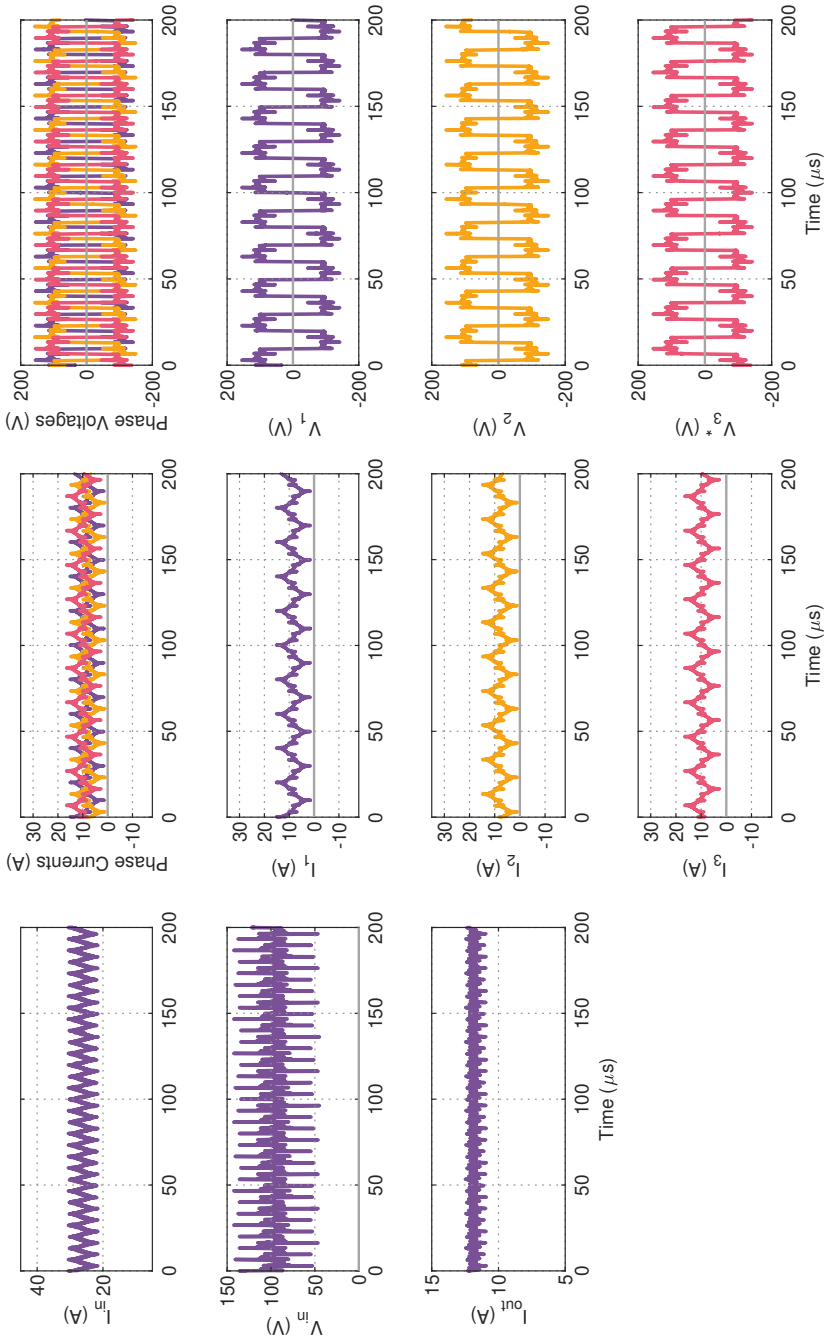

Figure A.4: T1 frequency sweep $F_{sw} = 50kHz$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

A.3.2 T1 phase shift sweep waveforms

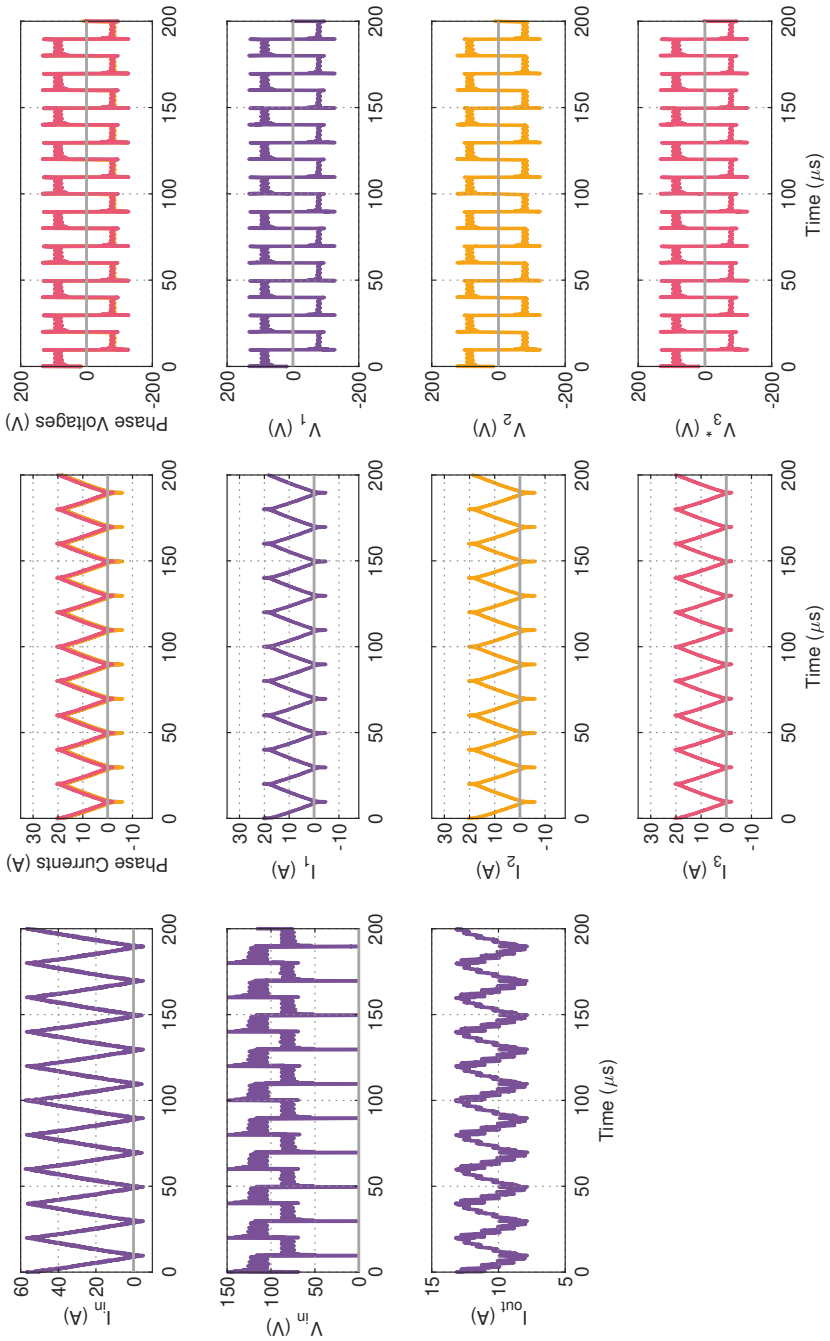

Figure A.5: T1 phase shift sweep $\theta = 0°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

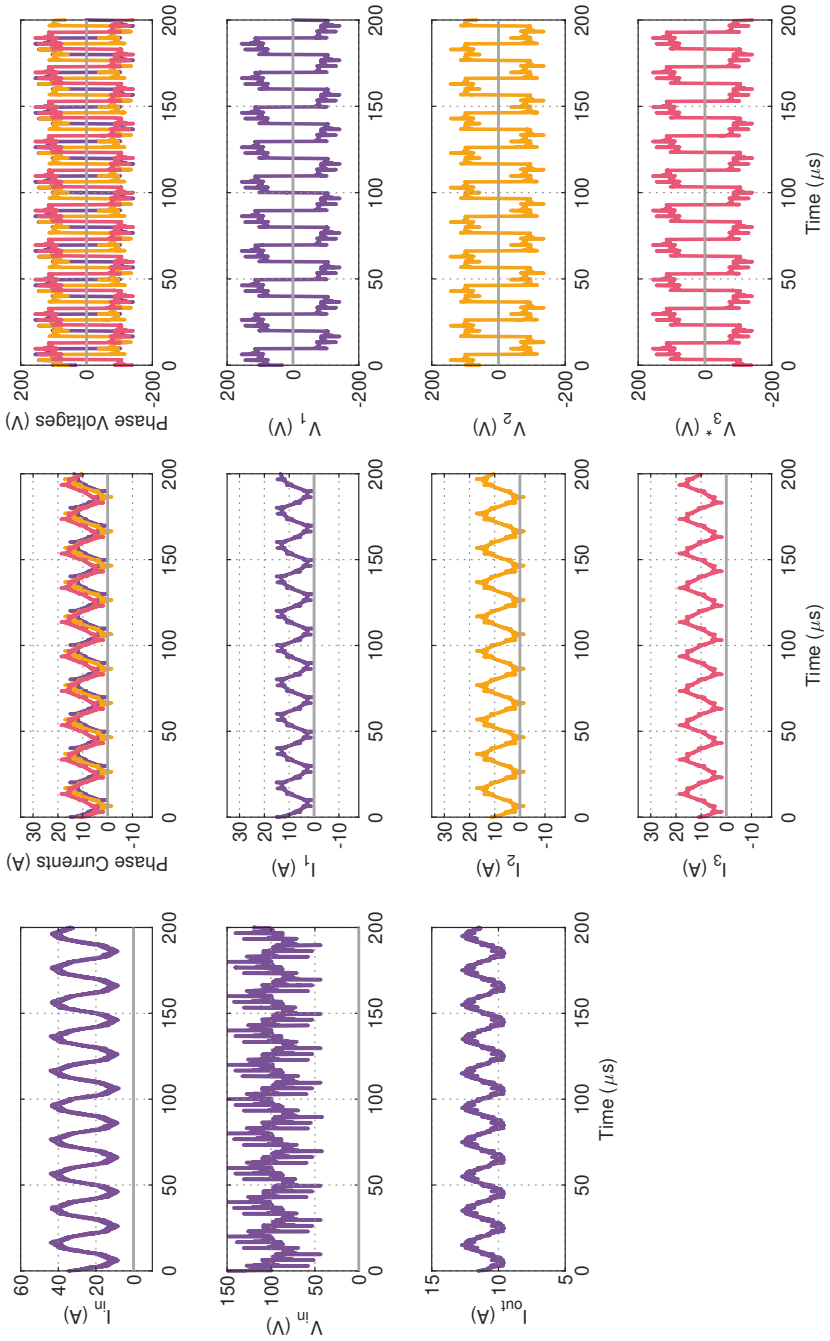

Figure A.6: T1 phase shift sweep $\theta = 60°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

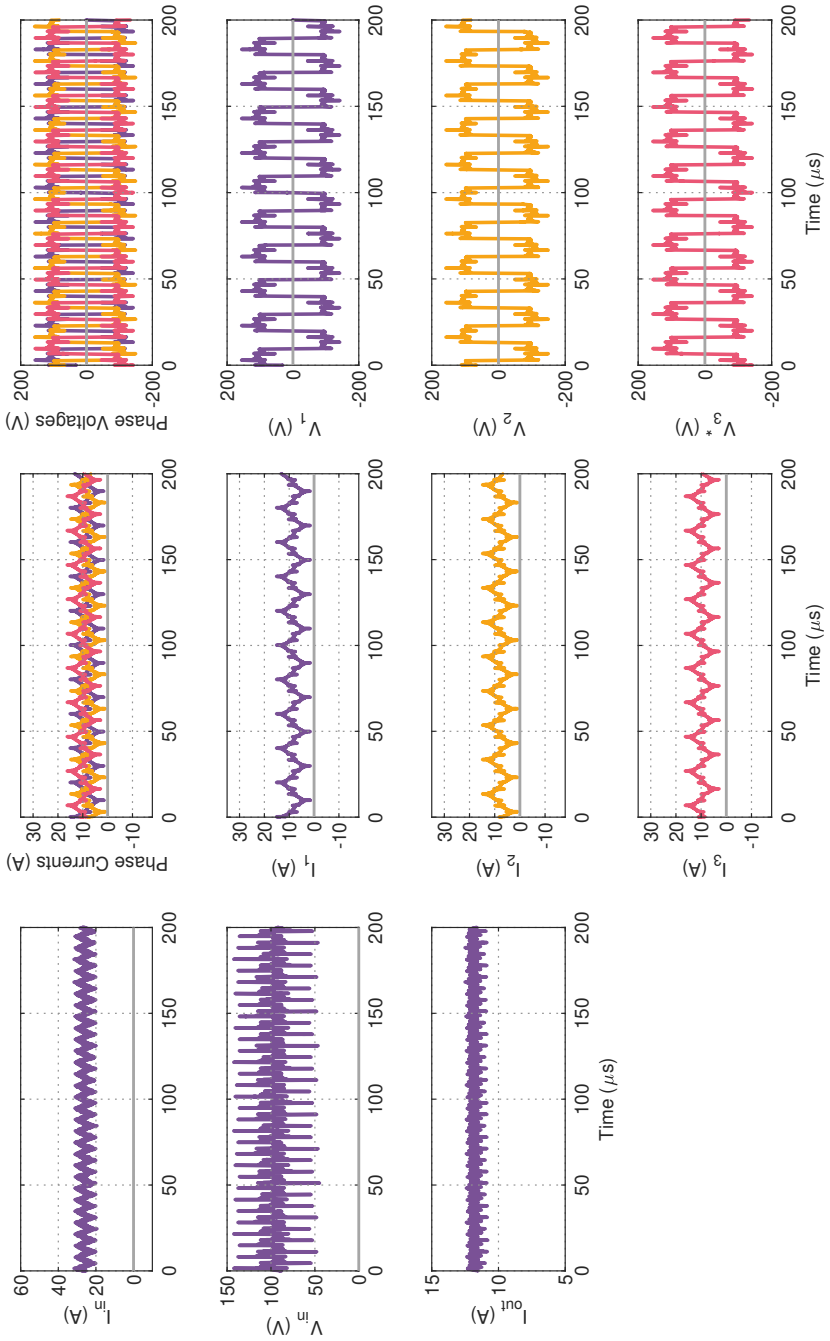

Figure A.7: T1 phase shift sweep $\theta = 120°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

A.3.3 T2 frequency sweep waveforms

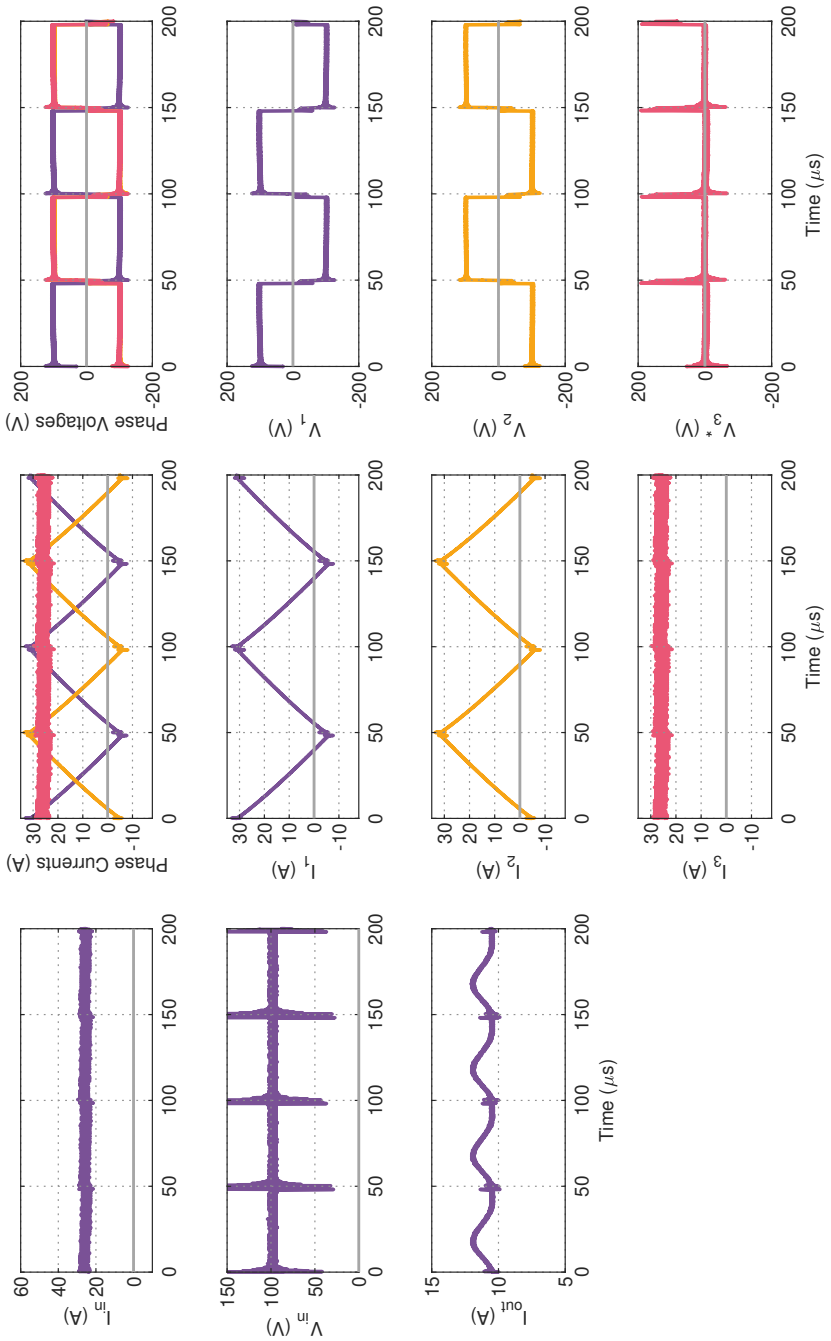

Figure A.8: T2 frequency sweep $F_{sw} = 10kHz$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

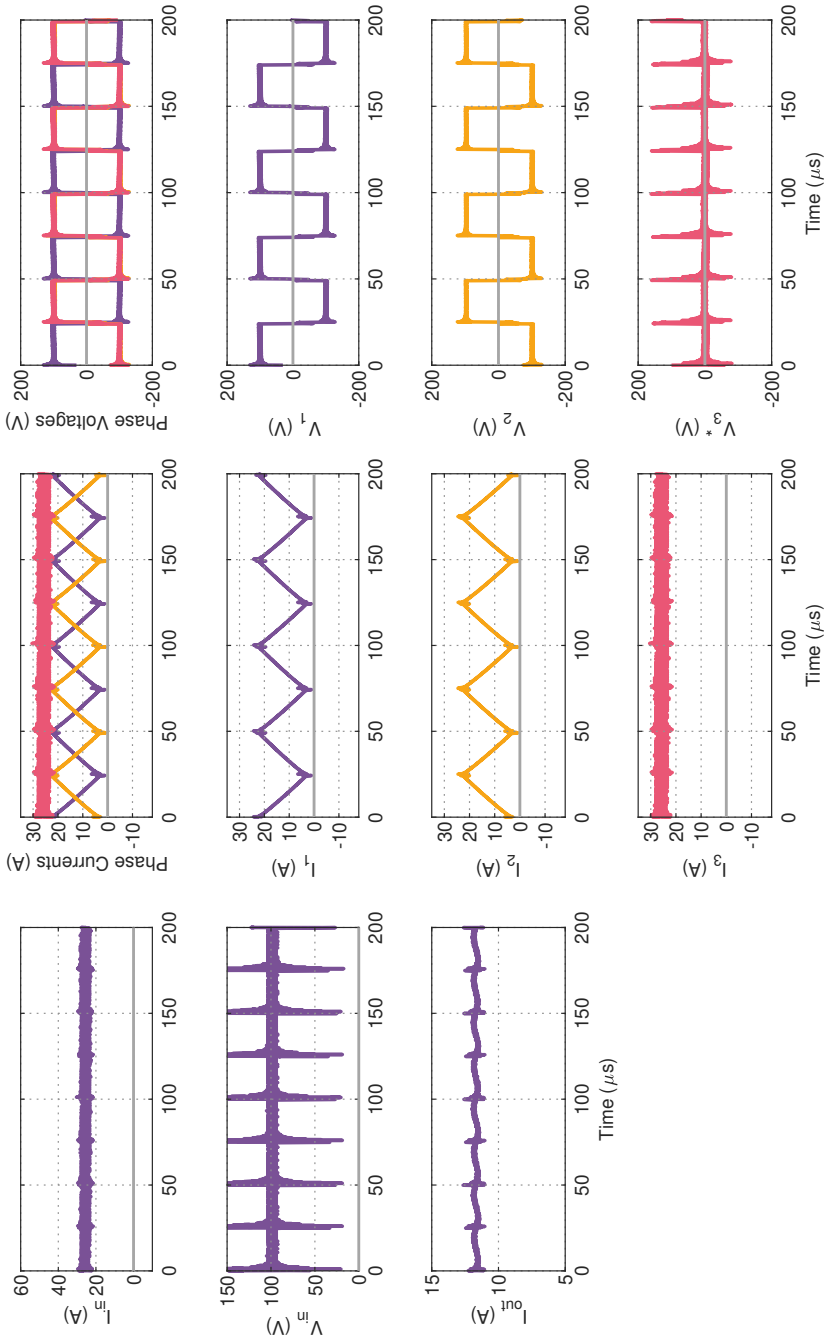

Figure A.9: T2 frequency sweep $F_{sw} = 20kHz$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

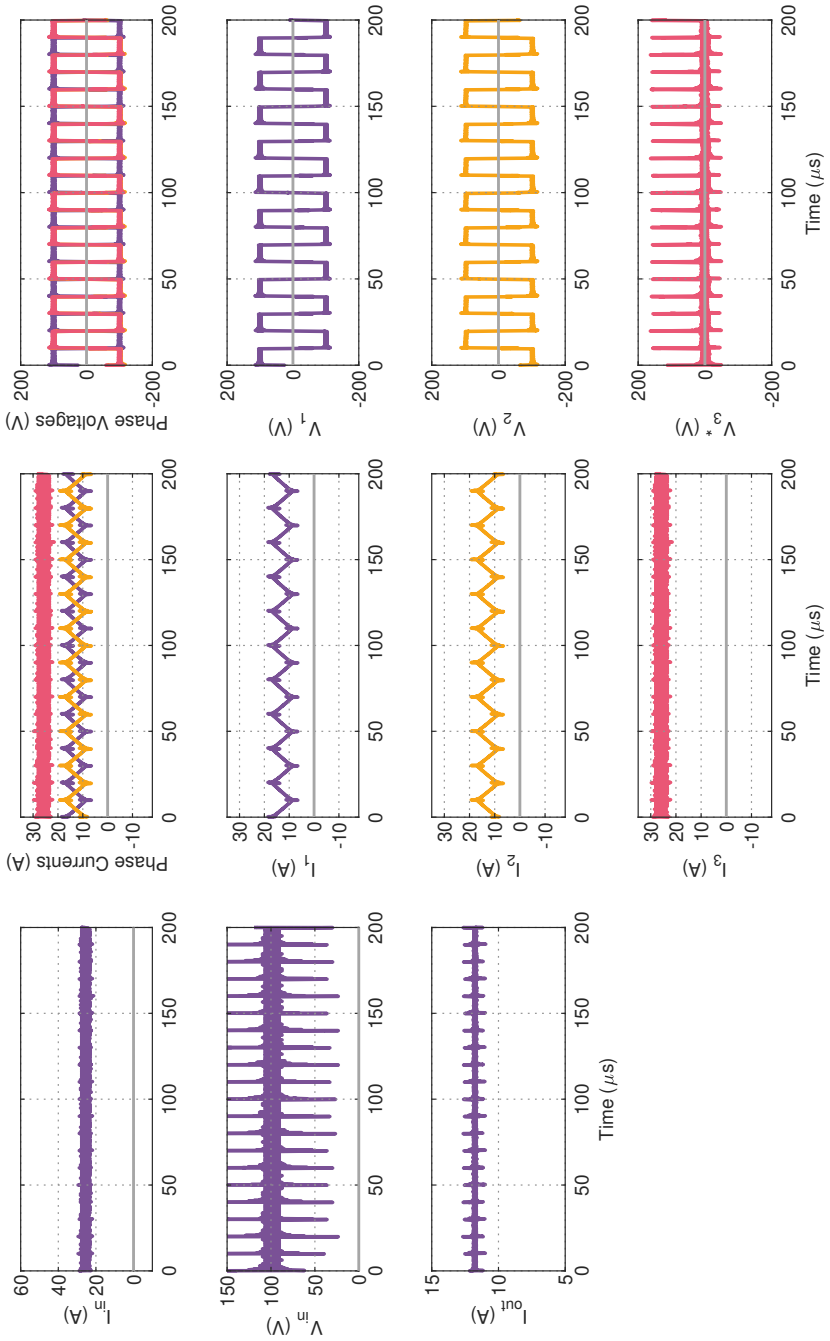

Figure A.10: T2 frequency sweep $F_{sw} = 50kHz$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

A.3.4 T2 phase shift sweep waveforms

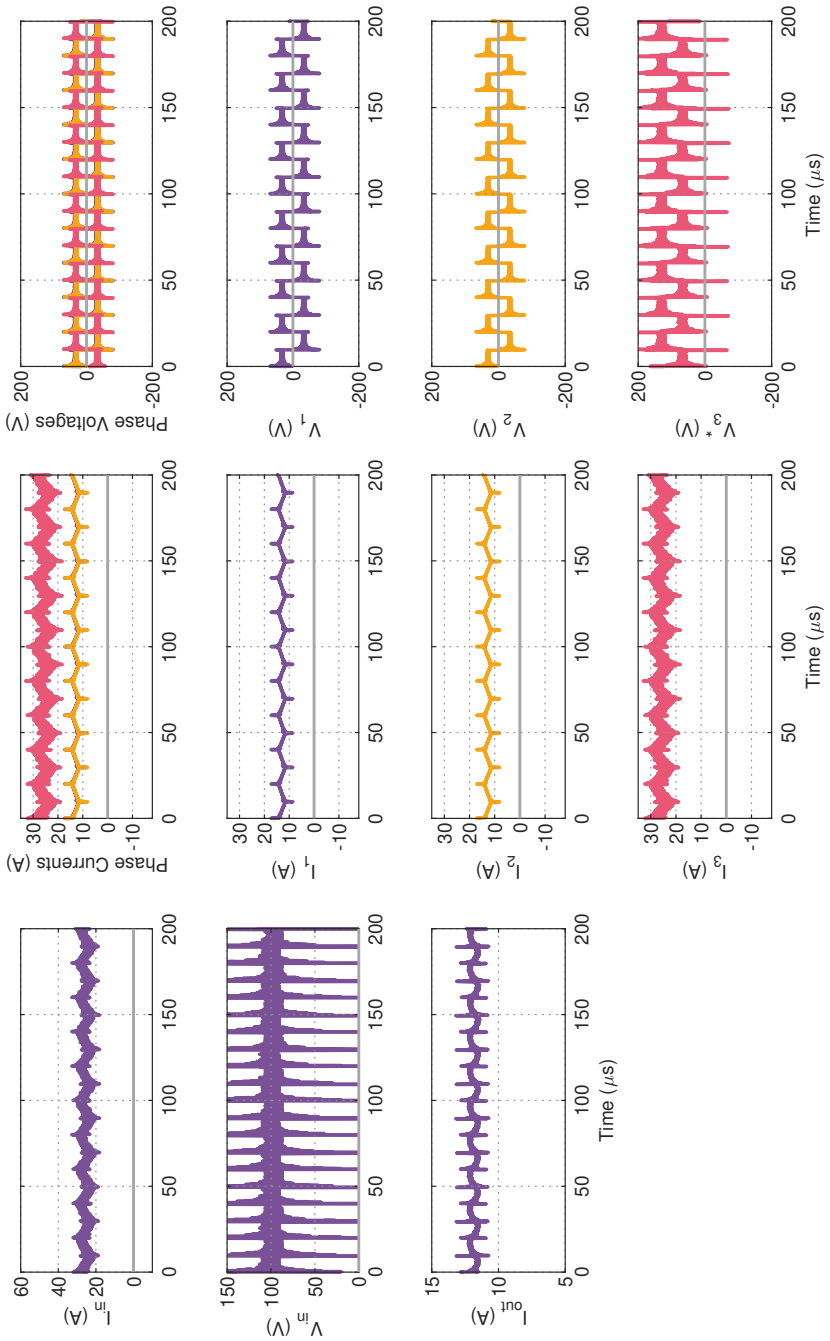

Figure A.11: T2 phase shift sweep $\theta = 0°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

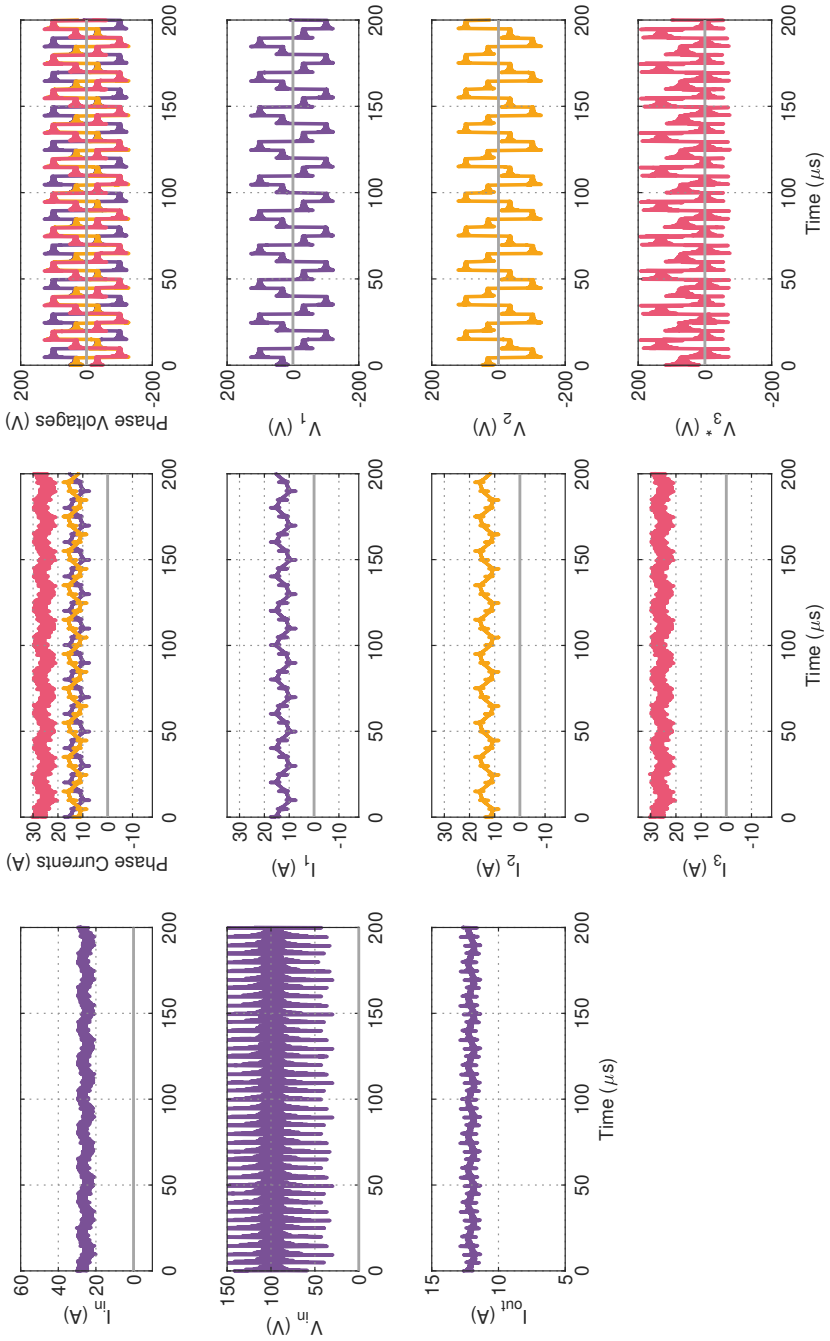

Figure A.12: T2 phase shift sweep $\theta = 90°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

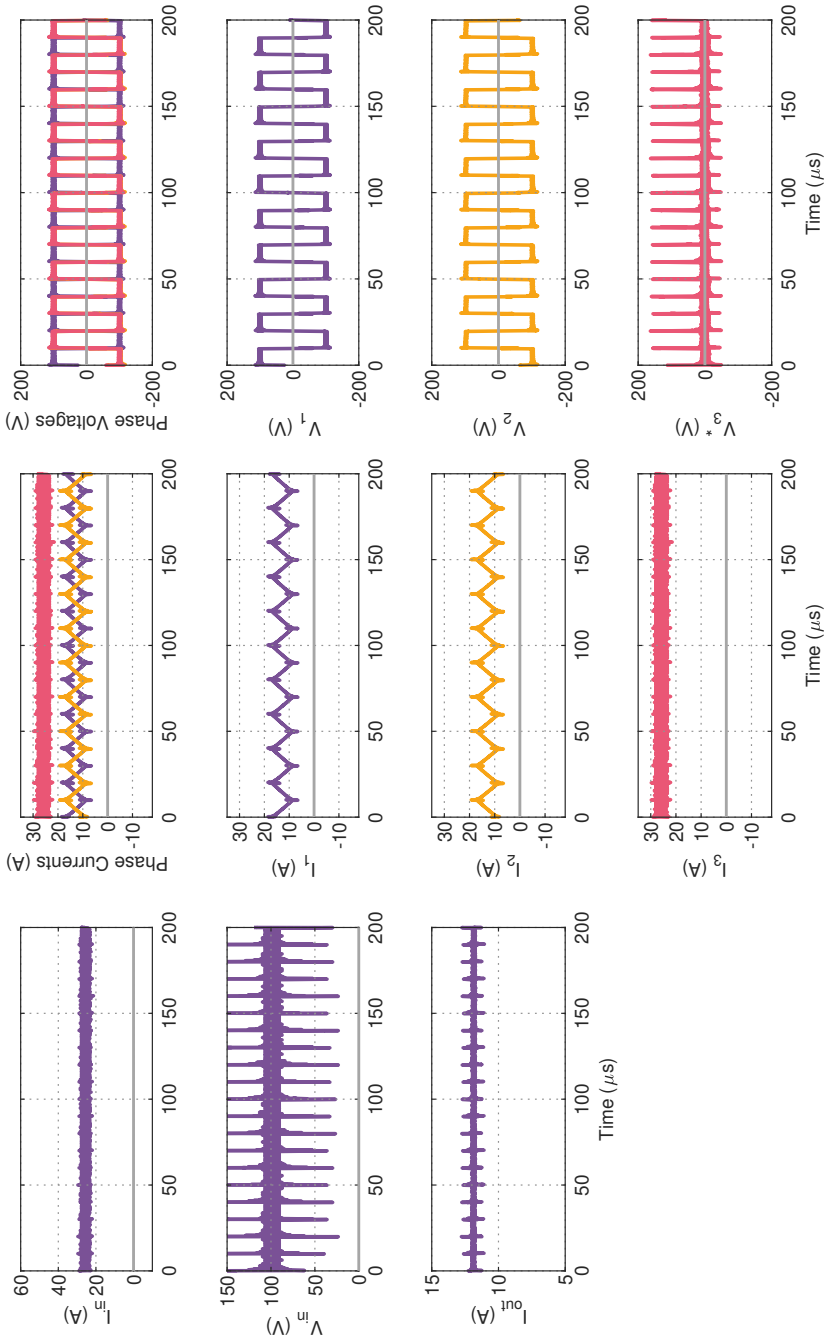

Figure A.13: T2 phase shift sweep $\theta = 180°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

A.3.5 Rotor inclusion waveforms

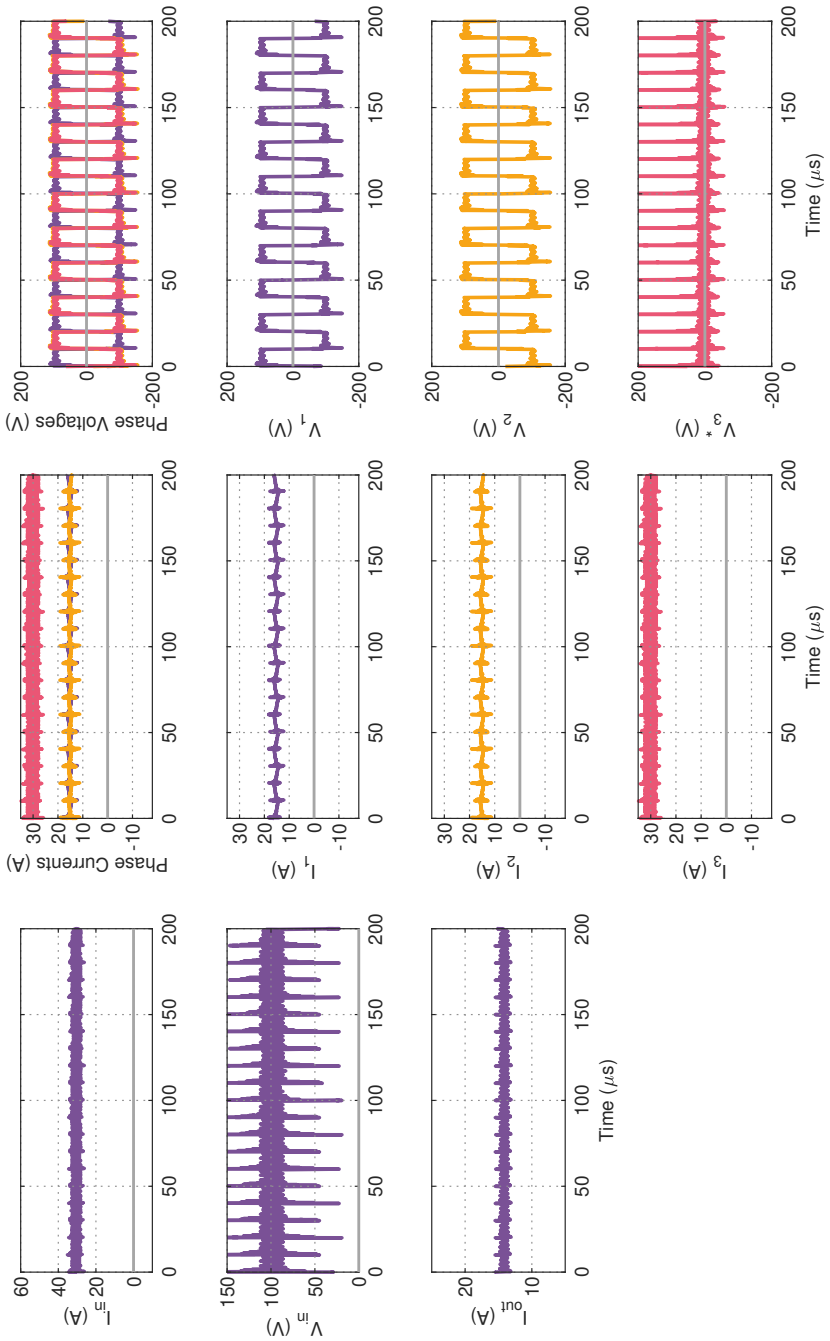

Figure A.14: EESM position 1 $F_{sw} = 50kHz$, $\theta = 180°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

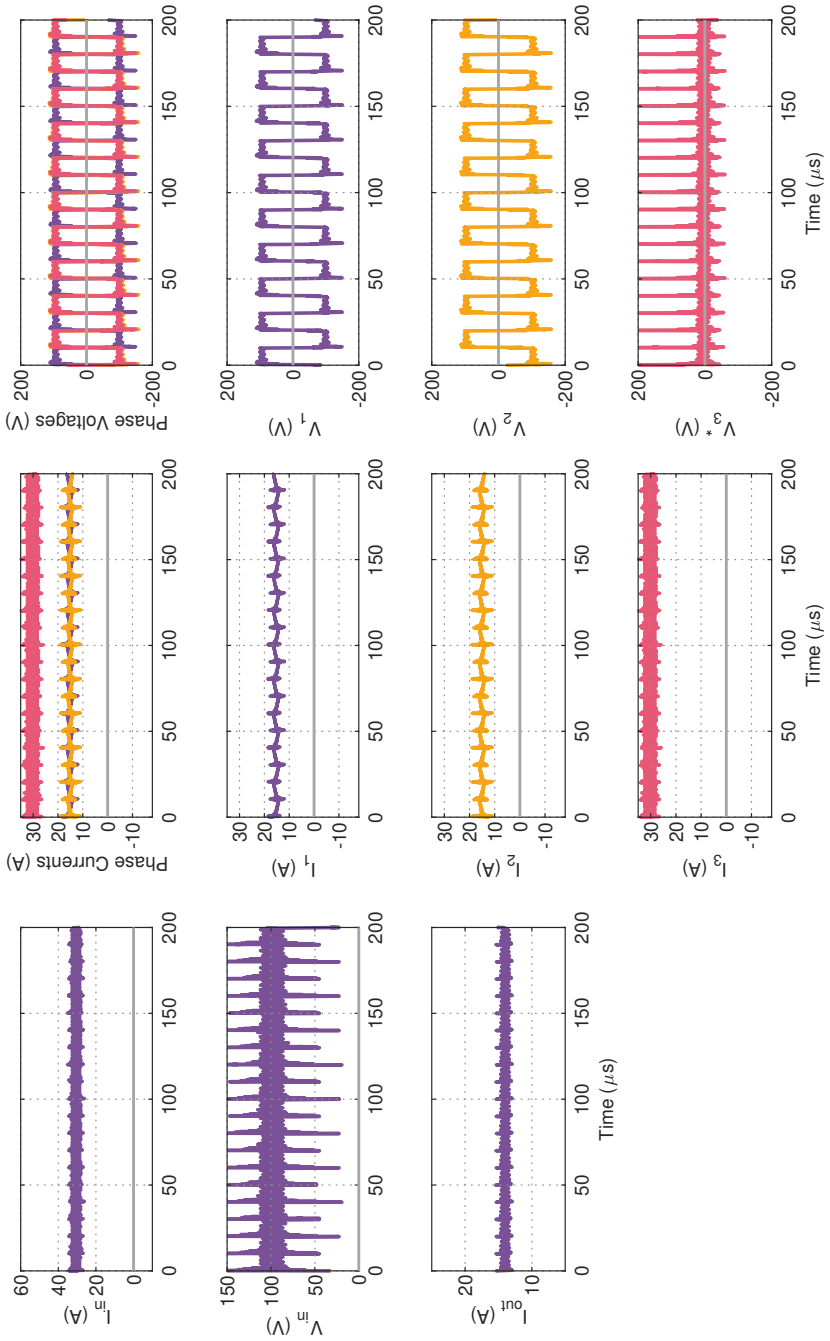

Figure A.15: EESM position 2 $F_{sw} = 50kHz$, $\theta = 180°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

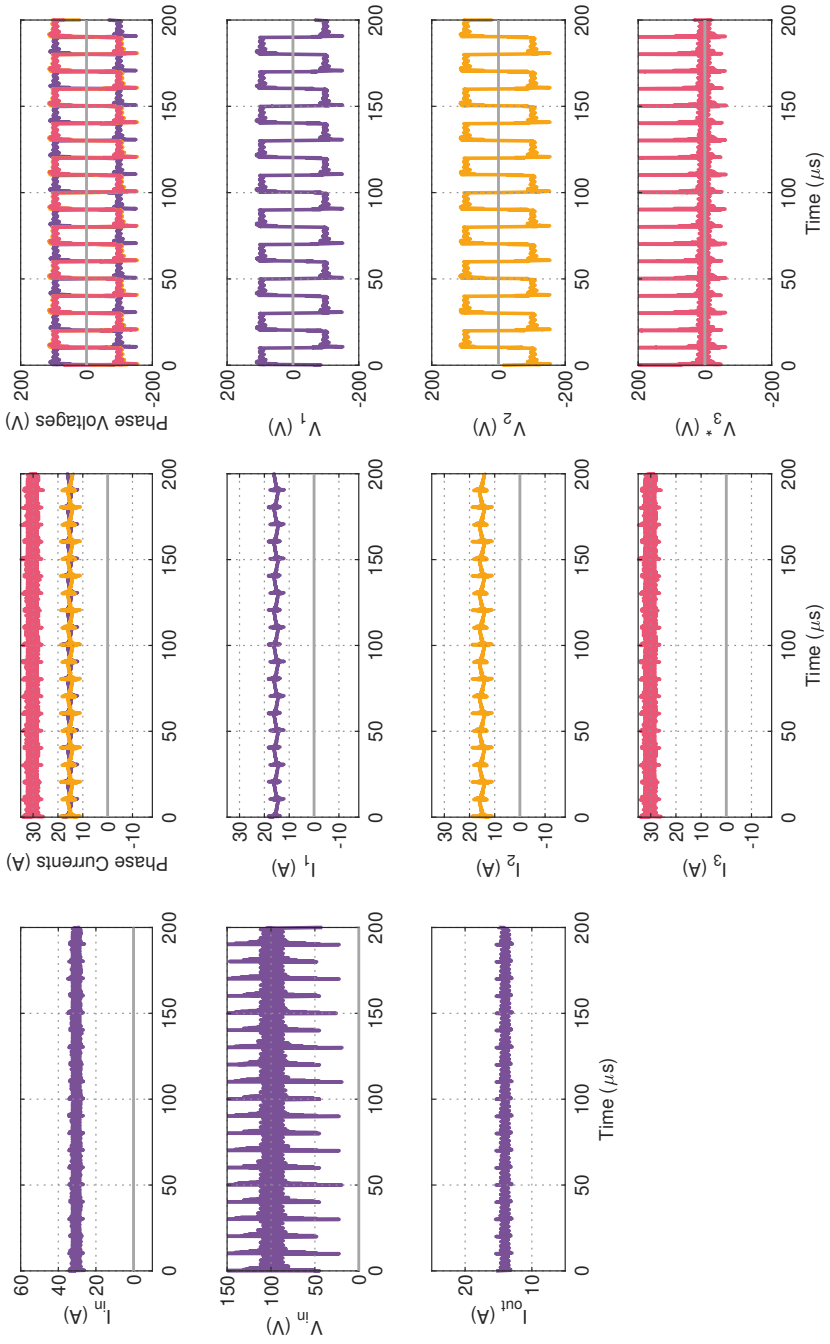

Figure A.16: EESM position 3 $F_{sw} = 50kHz$, $\theta = 180°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

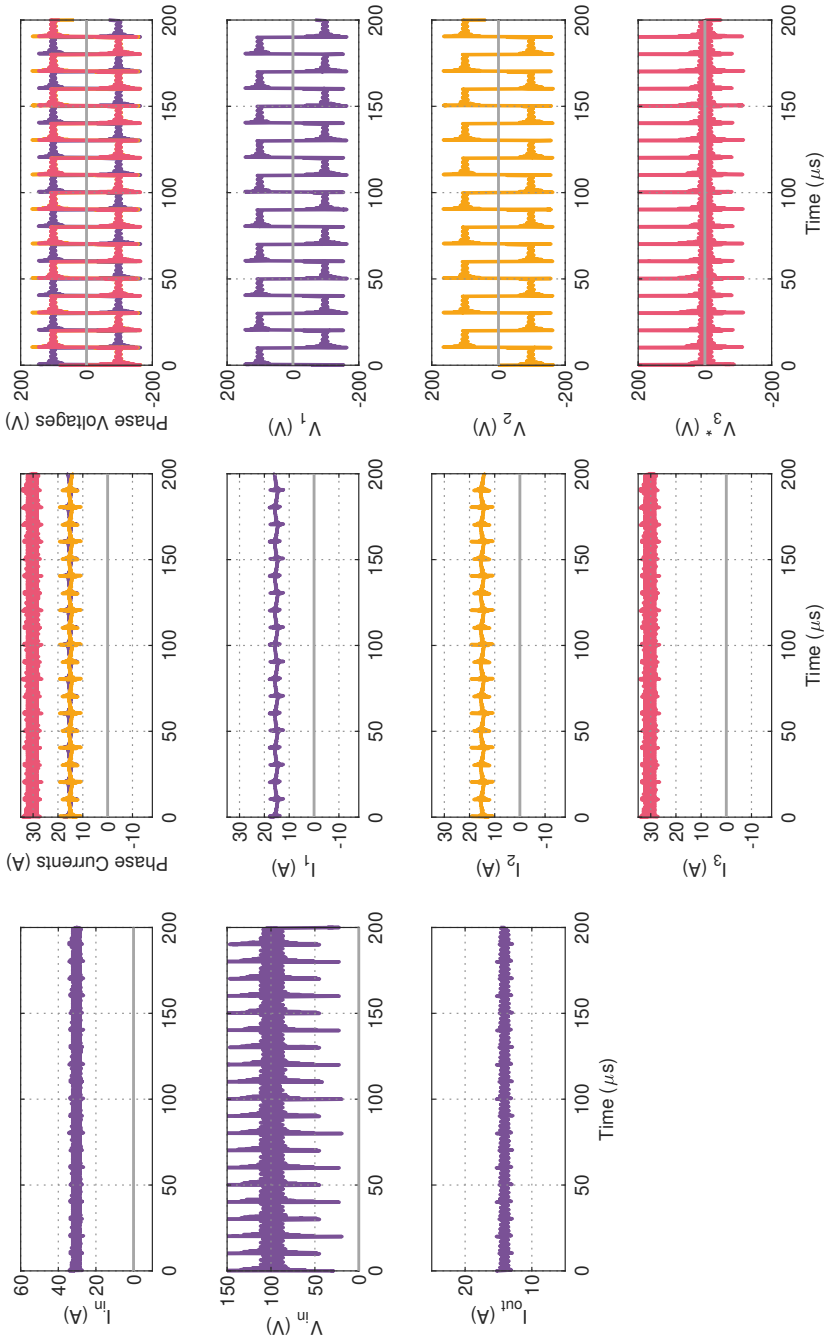

Figure A.17: PMSM fixed pos $F_{sw} = 50kHz$, $\theta = 180°$, $V_{in} = 100V$, $V_{out} = 200V$, $D = 0.52$

Appendix B

Average state space model

B.1 One phase average state space model for a booster converter

A single-phase booster DC–DC converter can be described by a state-space model by assuming that, in steady-state operation, its duty cycle remains constant and that the current through the inductor never discharges completely (the booster operates in continuous current mode operation).

The analysis starts by considering the boost converter in its two states, when the switch is turned on and off. When the switch is turned on, the input current charges the inductor, the diode is not conducting, and the battery is supplied by the output capacitor for a fraction of the period d.

$$\begin{aligned} \frac{dI_L}{dt} &= \frac{V_{in} \cdot d}{L} \\ \frac{dV_C}{dt} &= -\frac{1}{C}\left(\frac{V_C - V_{bat}}{R_{bat}}\right) \cdot d \end{aligned} \tag{B.1}$$

When the switch is turned off, the diode conducts and the inductor discharges, supplying the output capacitor and the battery for a fraction of the period $(1-d)$.

$$\begin{aligned} \frac{dI_L}{dt} &= \frac{(V_{in} - V_C) \cdot (1-d)}{L} \\ \frac{dV_C}{dt} &= \left(\frac{I_L}{C} - \frac{1}{C}\frac{V_C - V_{bat}}{R_{bat}}\right) \cdot (1-d) \end{aligned} \tag{B.2}$$

By using superposition, both states described by the equations B.1 and B.2 are coupled, forming the large-signal averaged model.

$$\begin{aligned} \frac{dI_L}{dt} &= \frac{V_{in}}{L} \cdot d + \frac{(V_{in} - V_C)}{L} \cdot (1-d) \\ \frac{dV_C}{dt} &= \left(-\frac{1}{C}\frac{V_C - V_{bat}}{R_{bat}}\right) \cdot d + \left(\frac{I_L}{C} - \frac{1}{C}\frac{V_C - V_{bat}}{R_{bat}}\right) \cdot (1-d) \end{aligned} \tag{B.3}$$

The state variables of the system are declared as:

$$x = \begin{bmatrix} I_L \\ V_C \end{bmatrix}, \quad \dot{x} = \begin{bmatrix} \dot{I}_L \\ \dot{V}_C \end{bmatrix} = \begin{bmatrix} f_1(I_L, V_C, d) \\ f_2(I_L, V_C, d) \end{bmatrix} \tag{B.4}$$

Where the duty cycle d is considered as the control input, and the battery voltage V_{bat} is treated as an external disturbance. The resulting state-space representation of the system can be written as:

$$\begin{aligned} \dot{x} &= A \cdot x + B \cdot u \\ y &= C \cdot x \end{aligned} \tag{B.5}$$

For control design purposes, the large-signal averaged model is linearized around a steady-state operating point. Each variable is decomposed into its steady-state value and a small perturbation:

$$I_L = I_{L,Q} + \hat{i}_L \tag{B.6}$$
$$V_C = V_{C,Q} + \hat{v}_C \tag{B.7}$$
$$d = d_Q + \hat{d} \tag{B.8}$$
$$V_{bat} = V_{bat,Q} + \hat{v}_{bat} \tag{B.9}$$

The resulting small-signal model is given by:

$$\dot{\hat{x}} = A_Q \cdot \hat{x} + B_Q \cdot \hat{d} \tag{B.10}$$
$$\hat{y} = C \cdot \hat{x} \tag{B.11}$$

The terms for the A and B matrix are obtained by taking the result of the first order Taylor expansion evaluated at the operating point for each differential equation that described each state variable. This is expressed as:

$$\begin{aligned} A_{Q_{1,1}} &= \left.\frac{\partial \dot{I}_L(I_L, V_C)}{\partial I_L}\right|_{x=x_{ss}}, \quad A_{Q_{1,2}} = \left.\frac{\partial \dot{I}_L(I_L, V_C)}{\partial V_C}\right|_{x=x_{ss}} \\ A_{Q_{2,1}} &= \left.\frac{\partial \dot{V}_C(I_L, V_C)}{\partial I_L}\right|_{x=x_{ss}}, \quad A_{Q_{2,2}} = \left.\frac{\partial \dot{V}_C(I_L, V_C)}{\partial V_C}\right|_{x=x_{ss}} \end{aligned} \tag{B.12}$$

$$A_Q = \begin{bmatrix} 0 & -\frac{1-d_Q}{L} \\ \frac{1-d_Q}{C} & -\frac{1}{R_{bat}C} \end{bmatrix}, \quad B_Q = \begin{bmatrix} \frac{V_{C0}}{L} \\ -\frac{I_{L0}}{C} \end{bmatrix} \tag{B.13}$$

The obtained small-signal model is linear and time-invariant, making it suitable for classical and modern control design techniques such as PI, pole placement, or LQR. The duty-cycle perturbation $\hat{d}$ acts as the control input, while the output voltage perturbation $\hat{v}_C$ is typically selected as the controlled variable.

B.2 Three-Phase Interleaved Boost Converter Model

The averaged state-space model derived for the single-phase boost converter, is extended to a three-phase interleaved boost converter by considering three identical inductors operating in parallel at the input and sharing a common output capacitor and load.

Each phase is driven with the same duty cycle magnitude but with a fixed phase shift of $120°$ between the PWM signals.

$$\begin{aligned} \frac{dI_{L,k}}{dt} &= \frac{V_{in}}{L} - \frac{(1-d_k)}{L} V_C, \quad k = 1, 2, 3 \\ \frac{dV_C}{dt} &= \frac{1}{C} \sum_{k=1}^{3} (1-d_k) \cdot I_{L,k} - \frac{V_C - V_{bat}}{R_{bat} \cdot C} \end{aligned} \tag{B.14}$$

The output voltage dynamics depend on the sum of the inductor currents, while each inductor current is described by the same differential equation.

The state vector is defined as

$$x = \begin{bmatrix} I_{L1} & I_{L2} & I_{L3} & V_C \end{bmatrix}^T \tag{B.15}$$

With the linearized states:

$$I_{Lk} = I_{Lk,Q} + \hat{i}_{Lk}, \quad k = 1, 2, 3 \tag{B.16}$$

$$V_C = V_{CQ} + \hat{v}_C \tag{B.17}$$

$$d = d_Q + \hat{d} \tag{B.18}$$

The averaged state-space model can be written as:

$$A_Q = \begin{bmatrix} 0 & 0 & 0 & -\frac{1-d_{1,Q}}{L} \\ 0 & 0 & 0 & -\frac{1-d_{2,Q}}{L} \\ 0 & 0 & 0 & -\frac{1-d_{3,Q}}{L} \\ \frac{1-d_{1,Q}}{C} & \frac{1-d_{2,Q}}{C} & \frac{1-d_{3,Q}}{C} & -\frac{1}{R_{bat} \cdot C} \end{bmatrix}, \quad B_Q = \begin{bmatrix} \frac{V_{C,Q}}{L} & 0 & 0 \\ 0 & \frac{V_{C,Q}}{L} & 0 \\ 0 & 0 & \frac{V_{C,Q}}{L} \\ -\frac{I_{L1,Q}}{C} & -\frac{I_{L2,Q}}{C} & -\frac{I_{L3,Q}}{C} \end{bmatrix} \tag{B.19}$$

The interleaved structure introduces redundancy in the inductor current states, allowing the system to be decomposed into common-mode and differential-mode dynamics.

Appendix C

Three-Phase Interleaved Boost Converter Control

C.1 Current Control

The current controller can be run standalone without considering the voltage dynamics. The model is obtained from the linearized system by removing the rows and columns related to the output voltage.

$$A_Q = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \quad B_Q = \begin{bmatrix} \frac{V_{C,Q}}{L} & 0 & 0 \\ 0 & \frac{V_{C,Q}}{L} & 0 \\ 0 & 0 & \frac{V_{C,Q}}{L} \end{bmatrix}, \quad C = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{C.1}$$

C.1.1 PI Controller

From this reduced model, the transfer function for each inductor current is:

$$\frac{\hat{i}_{Lk}(s)}{\hat{d}_k(s)} = C \cdot (sI - A_Q)^{-1} \cdot B_Q \tag{C.2}$$

Since $A_Q = 0$ and B_Q is diagonal, this simplifies to:

$$H(s) = \frac{\hat{i}_{Lk}(s)}{\hat{d}_k(s)} = \frac{V_{C,Q}}{L \cdot s} \tag{C.3}$$

Taking a PI controller of the form:

$$C(s) = K_p + \frac{K_i}{s} \tag{C.4}$$

The closed-loop characteristic polynomial is:

$$P(s) = 1 + H(s) \cdot C(s) \tag{C.5}$$

Substituting $H(s)$ gives:

$$P(s) = s^2 + \frac{V_{C,Q} \cdot K_p}{L} s + \frac{V_{C,Q} \cdot K_i}{L} \tag{C.6}$$

Finally, the PI gains can be calculated by placing the poles according to a desired bandwidth ω_n and damping ξ:

$$k_p = \frac{2 \cdot \xi \cdot \omega_n \cdot L}{V_{C,Q}}, \qquad k_i = \frac{\omega_n^2 \cdot L}{V_{C,Q}} \tag{C.7}$$

C.1.2 State-Feedback with Integral Action

Alternatively, considering non-ideal inductors and slow variations in the capacitor voltage, the state-feedback controller can be augmented with the integral of the current error to ensure zero steady-state error with a state space implementation. This expresses the system and controller as a multi-input multi-output (MIMO) system, highlighting its scalability and compatibility with observer-based control techniques. To achieve this, the integral of the current errors is defined as additional states:

$$z = \begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix}, \quad z_k = \int (I_{L,k}^{ref} - I_{L,k}) dt \tag{C.8}$$

So, the augmented state vector is:

$$x_a = \begin{bmatrix} I_{L1} & I_{L2} & I_{L3} & z_1 & z_2 & z_3 \end{bmatrix}^T \tag{C.9}$$

And the control input vector is:

$$u = \begin{bmatrix} d_1 & d_2 & d_3 \end{bmatrix}^T \tag{C.10}$$

Using the current-only linearized model, the augmented dynamics can be written as:

$$\dot{x}_a = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \end{bmatrix}}_{A_a} x_a + \underbrace{\begin{bmatrix} \frac{V_{C,Q}}{L} & 0 & 0 \\ 0 & \frac{V_{C,Q}}{L} & 0 \\ 0 & 0 & \frac{V_{C,Q}}{L} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{B_a} u + \underbrace{\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}}_{E} x_{ref} \tag{C.11}$$

Where $x_{ref} = [I_{L1}^{ref}, I_{L2}^{ref}, I_{L3}^{ref}]^T$.

The control law is:

$$u = u_Q - K_a \cdot x_a \tag{C.12}$$

Where the gain matrix has the following structure:

$$K_a = \begin{bmatrix} k_p & 0 & 0 & k_i & 0 & 0 \\ 0 & k_p & 0 & 0 & k_i & 0 \\ 0 & 0 & k_p & 0 & 0 & k_i \end{bmatrix} \tag{C.13}$$

Substituting the control law into the augmented system yields the closed-loop dynamics:

$$\dot{x}_a = (A_a - B_a \cdot K_a) \cdot x_a + E \cdot x_{ref} \tag{C.14}$$

The closed-loop system matrix becomes:

$$A_{cl} = \begin{bmatrix} -\frac{V_{C,Q}}{L}k_p & 0 & 0 & -\frac{V_{C,Q}}{L}k_i & 0 & 0 \\ 0 & -\frac{V_{C,Q}}{L}k_p & 0 & 0 & -\frac{V_{C,Q}}{L}k_i & 0 \\ 0 & 0 & -\frac{V_{C,Q}}{L}k_p & 0 & 0 & -\frac{V_{C,Q}}{L}k_i \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \end{bmatrix} \tag{C.15}$$

The characteristic polynomial associated with each phase is identical and given by:

$$P(s) = det(s \cdot I - A_{cl}) \tag{C.16}$$

$$\left(s^2 + \frac{V_{C,Q}}{L} \cdot k_p \cdot s + \frac{V_{C,Q}}{L} \cdot k_i\right)^3 = 0 \tag{C.17}$$

Thus, the controller gains are selected by imposing a desired natural frequency ω_n and damping ratio ξ, with the same formulation as the PI approach:

$$k_p = \frac{2 \cdot \xi \cdot \omega_n \cdot L}{V_{C,Q}}, \qquad k_i = \frac{\omega_n^2 \cdot L}{V_{C,Q}} \tag{C.18}$$

C.1.3 LQR

While pole placement allows explicit tuning of the closed-loop poles, the same augmented formulation can be naturally used for optimal control. In particular, the Linear Quadratic Regulator (LQR) provides a systematic way to compute the feedback gains. The LQR controller is obtained by minimizing the quadratic cost function:

$$J = \int_0^\infty \left(x_a^T \cdot Q \cdot x_a + u^T \cdot R \cdot u\right) \, dt \tag{C.19}$$

where the weighting matrices are chosen as:

$$Q = \begin{bmatrix} q_i \cdot I_3 & 0 \\ 0 & q_z \cdot I_3 \end{bmatrix}, \quad R = r \cdot I_3 \tag{C.20}$$

The values of q_i, q_z, and r are application dependent, but they can be related to physical constraints of the system. High values of q_i and q_z emphasize fast current regulation and steady-state accuracy, respectively, while high values of r penalize excessive control effort and reduce duty-cycle activity. A practical normalization of the weighting parameters can be obtained as:

$$q_i = \frac{1}{\Delta I_{max}^2}, \qquad q_z = \frac{1}{\Delta z_{max}^2}, \qquad r = \frac{1}{\Delta d_{max}^2} \tag{C.21}$$

The optimal state-feedback control law is defined as:

$$u = u_Q - K_a \cdot x_a \tag{C.22}$$

where the gain matrix is computed as:

$$K_a = R^{-1} \cdot B_a^T \cdot P \tag{C.23}$$

and P is the unique positive semi-definite solution of the Algebraic Riccati Equation:

$$A_a^T \cdot P + P \cdot A_a - P \cdot B_a \cdot R^{-1} \cdot B_a^T \cdot P + Q = 0 \tag{C.24}$$

Due to the symmetry of the interleaved system and the selected weighting matrices, the resulting gain matrix has the following structured form:

$$K_a = \begin{bmatrix} k_x & 0 & 0 & k_z & 0 & 0 \\ 0 & k_x & 0 & 0 & k_z & 0 \\ 0 & 0 & k_x & 0 & 0 & k_z \end{bmatrix} \tag{C.25}$$

It can be noted that the gain matrix have the same structure as the state feedback regulator, being the last one a particular solution from the optimal controller.

C.2 Cascade Voltage and Current Control

Battery chargers operate in two modes: Constant Current (CC) and Constant Voltage (CV). During constant voltage operation, an outer voltage loop with integral action is required in order to eliminate steady-state error and ensure accurate voltage tracking. Starting from the linearized model in (B.19), an additional state is introduced to represent the integral of the voltage error:

$$\dot{z}_v = V_C^{ref} - V_C \tag{C.26}$$

Similarly, integral states for the inductor currents are defined as:

$$\dot{z}_i = I_{Li}^{ref} - I_{Li}, \qquad i = 1, 2, 3 \tag{C.27}$$

The augmented state vector becomes:

$$x_a = \begin{bmatrix} I_{L1} & I_{L2} & I_{L3} & V_C & z_1 & z_2 & z_3 & z_v \end{bmatrix}^T \tag{C.28}$$

And the control input vector is:

$$u = \begin{bmatrix} d_1 & d_2 & d_3 \end{bmatrix}^T \tag{C.29}$$

The augmented linearized model can then be written in compact form as:

$$\dot{x}_a = \begin{bmatrix} A & 0 \\ -C_r & 0 \end{bmatrix} x_a + \begin{bmatrix} B \\ 0 \end{bmatrix} u + \begin{bmatrix} 0 \\ I \end{bmatrix} r \tag{C.30}$$

Where:

$$C_r = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{C.31}$$

And the reference vector is defined as:

$$r = \begin{bmatrix} I_{L1}^{ref} & I_{L2}^{ref} & I_{L3}^{ref} & V_C^{ref} \end{bmatrix}^T \tag{C.32}$$

C.2.1 Voltage Control

Once the inner current loop is designed as exposed in Section C.1 and sufficiently faster than the voltage dynamics ($\omega_{n,i} > 5\,\omega_{n,v}$), it can be approximated by its closed-loop behavior. Assuming identical controllers for the three phases, the total current that charges the capacitor is:

$$i_{tot} = i_{L1} + i_{L2} + i_{L3} \tag{C.33}$$

The capacitor voltage dynamics are:

$$C\frac{d\hat{V}_C}{dt} = \hat{i}_{tot} - \frac{\hat{V}_C}{R_{bat}} \tag{C.34}$$

In practical high-voltage battery systems, R_{bat} is small ($m\Omega$ range). Consequently, the associated pole is typically much larger than the designed voltage-loop bandwidth.

$$\frac{1}{C \cdot R_{bat}} \gg \omega_{n,v} \tag{C.35}$$

Therefore, the battery-induced dynamics are much faster than the voltage-control dynamics and can be neglected in the controller design. Under this assumption, the plant simplifies to:

$$G_v(s) \approx \frac{1}{s \cdot C}. \tag{C.36}$$

The controller output corresponds to the duty-cycle command of the converter. The PWM stage converts duty-cycle variations into an equivalent average voltage applied to the power stage. Linearizing around the operating point:

$$\hat{V}_C(s) = K_{PWM} \cdot \hat{d}(s). \tag{C.37}$$

Since the inner current loop is much faster than the voltage loop, the total injected current follows the controller command, yielding

$$\hat{I}_{tot}(s) \approx K_{PWM} \cdot C_v(s) \cdot \hat{G}(s). \tag{C.38}$$

Consequently, the effective plant seen by the voltage controller is

$$H_v(s) = \frac{K_{PWM}}{s \cdot C}. \tag{C.39}$$

C.2.2 PI Controller

The voltage controller PI form is:

$$C_v(s) = K_{p,v} + \frac{K_{i,v}}{s}. \tag{C.40}$$

The closed-loop characteristic polynomial is

$$P_v(s) = 1 + H_v(s) \cdot C_v(s). \tag{C.41}$$

In its expanded form:

$$P_v(s) = s^2 + \frac{1}{C}K_{p,v} \cdot s + \frac{K_{i,v}}{C}. \tag{C.42}$$

The gains are obtained by matching the polynomial to a desired second-order characteristic equation

$$s^2 + 2 \cdot \xi_v \cdot \omega_{nv} \cdot s + \omega_{nv}^2. \tag{C.43}$$

Equating coefficients:

$$K_{p,v} = \frac{2 \cdot \xi_v \cdot \omega_{n,v} \cdot C}{K_{pwm}} \tag{C.44}$$

$$K_{i,v} = \frac{\omega_{n,v}^2}{K_{pwm}} \tag{C.45}$$

Appendix D

Two-Phase Interleaved Boost Converter Control

D.1 System Model

The two-phase interleaved boost converter consists of two parallel boost legs sharing a common output capacitor. Operating with a 180° phase shift between carriers, it reduces input current ripple and inductor size. Applying state-space averaging and linearizing around the operating point $(I_{L,Q},\, V_{C,Q},\, D_Q)$, the small-signal model is:

$$\dot{\hat{x}} = A\,\hat{x} + B\,\hat{u}, \qquad \hat{x} = \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_C \end{bmatrix}, \quad \hat{u} = \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} \tag{D.1}$$

$$A = \begin{bmatrix} 0 & 0 & -\frac{1-D_Q}{L} \\ 0 & 0 & -\frac{1-D_Q}{L} \\ \frac{1-D_Q}{C} & \frac{1-D_Q}{C} & -\frac{1}{RC} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{V_{C,Q}}{L} & 0 \\ 0 & \frac{V_{C,Q}}{L} \\ -\frac{I_{L,Q}}{C} & -\frac{I_{L,Q}}{C} \end{bmatrix} \tag{D.2}$$

D.2 Current Control

Removing the voltage row/column from the linearized model yields the current-only subsystem:

$$A_Q = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad B_Q = \begin{bmatrix} \frac{V_{C,Q}}{L} & 0 \\ 0 & \frac{V_{C,Q}}{L} \end{bmatrix}, \quad C = I_2 \tag{D.3}$$

Because $A_Q = 0$ and B_Q is diagonal, each phase has the identical integrating plant:

$$H(s) = \frac{\hat{i}_{Lk}(s)}{\hat{d}_k(s)} = \frac{V_{C,Q}}{L \cdot s}, \qquad k = 1, 2 \tag{D.4}$$

D.2.1 PI Gains

A PI controller $C(s) = K_p + K_i/s$ closes the loop around $H(s)$. Matching the closed-loop polynomial to the standard second-order form $s^2 + 2\xi\omega_n s + \omega_n^2$ gives directly:

$$K_p = \frac{2\,\xi\,\omega_n\,L}{V_{C,Q}}, \qquad K_i = \frac{\omega_n^2\,L}{V_{C,Q}} \tag{D.5}$$

D.2.2 State-Feedback with Integral Action

Integral states $z_k = \int (I_{Lk}^{\text{ref}} - I_{Lk})\,dt$ are appended to eliminate steady-state error. The augmented state and dynamics are:

$$x_a = \begin{bmatrix} I_{L1} \\ I_{L2} \\ z_1 \\ z_2 \end{bmatrix}, \quad \dot{x}_a = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix}}_{A_a} x_a + \underbrace{\begin{bmatrix} \frac{V_{C,Q}}{L} & 0 \\ 0 & \frac{V_{C,Q}}{L} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{B_a} u + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}}_{E} x_{\text{ref}} \tag{D.6}$$

With the structured gain matrix:

$$K_a = \begin{bmatrix} k_p & 0 & k_i & 0 \\ 0 & k_p & 0 & k_i \end{bmatrix} \tag{D.7}$$

The closed-loop system matrix $A_{cl} = A_a - B_a K_a$ yields the characteristic polynomial (identical for both phases):

$$\left(s^2 + \frac{V_{C,Q}}{L}\,k_p\,s + \frac{V_{C,Q}}{L}\,k_i\right)^2 = 0 \tag{D.8}$$

The gains are therefore selected identically to the PI case:

$$k_p = \frac{2\,\xi\,\omega_n\,L}{V_{C,Q}}, \qquad k_i = \frac{\omega_n^2\,L}{V_{C,Q}} \tag{D.9}$$

D.3 Cascade Voltage and Current Control

During Constant Voltage (CV) operation an outer voltage loop is added. Integral states for both current errors and the voltage error are appended:

$$x_a = \begin{bmatrix} I_{L1} & I_{L2} & V_C & z_1 & z_2 & z_v \end{bmatrix}^T \tag{D.10}$$

The augmented model follows the same compact form as in the three-phase case, with the output matrix $C_r = \text{diag}(1, 1, 1)$ selecting the three regulated variables.

D.3.1 Voltage Loop Plant and PI Gains

Once the inner current loop is designed with bandwidth $\omega_{n,i} > 5\,\omega_{n,v}$, it is approximated as unity gain. The two-phase total current is $i_{\text{tot}} = i_{L1} + i_{L2}$, and the effective plant seen by the voltage controller is:

$$H_v(s) = \frac{K_{\text{PWM}}}{s\,C} \tag{D.11}$$

where the battery resistance pole $1/(C\,R_{\text{bat}}) \gg \omega_{n,v}$ is neglected. A PI voltage controller $C_v(s) = K_{p,v} + K_{i,v}/s$ yields the closed-loop polynomial:

$$P_v(s) = s^2 + \frac{K_{p,v}}{C}\, s + \frac{K_{i,v}}{C} \tag{D.12}$$

Matching to the desired natural frequency $\omega_{n,v}$ and damping ξ_v:

$$K_{p,v} = 2\,\xi_v\,\omega_{n,v}\,C, \qquad K_{i,v} = \omega_{n,v}^2\,C \tag{D.13}$$

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