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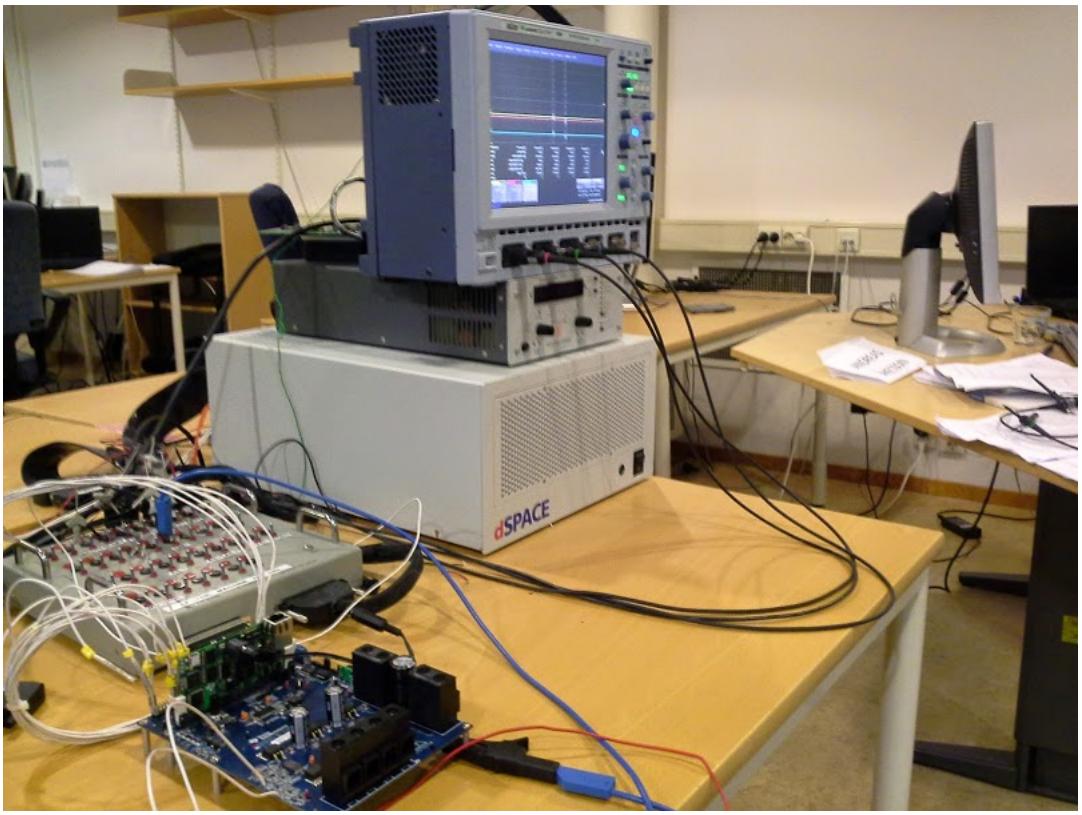

Evaluation of microcontroller architectures for PMSM control

Master of Science Thesis

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Department of Energy and Environment
Division of Electric Power Engineering
Chalmers University of Technology
Göteborg, Sweden 2015

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Cover:
Illustration of dSpace kit integrated with micro-controller evaluation board.

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Abstract

Due to hybridization of vehicles, electrical motors like permanent magnet synchronous motors (PMSM) are playing a major role in the automotive industry. In order to upgrade the micro-controller used for the prototype of the PMSM control in Volvo Group Truck Technology, a study on available micro-controllers presently on the market and to evaluate a few of the suitable micro-controllers is necessary. In this thesis a evaluation of Texas instrument micro-controllers TMS320F28377D and TMS570LS1227 are performed. In the first part of the thesis, a digital control algorithm has been implemented in the Matlab simulink and effect of various digital control parameters like ADC resolution, PWM resolution, ratio of switching frequency to electrical frequency of stator current etc. has been discussed. Based on the simulation minimum requirements of PWM and ADC resolution has been found to be 10 bit. Also the simulation results showed that for the drive system under consideration the ratio f_{sw}/f_{elec} should be 40 or more to have a better torque control.

In the second part of the thesis the best available micro-controllers suitable for PMSM control has been listed and the two of the most suitable micro-controllers TMS320F28377D and TMS570LS1227 has been selected for further evaluation. In the third part of the thesis, the digital control algorithm has been implemented in both the selected micro-controllers and the motor control performance has been evaluated using the hardware in the loop simulation with the real time motor model implemented on a dSpace system. The CPU utilization for the ISR in TMS570LS1227 for a switching frequency of 20 kHz and a CPU clock frequency of 80 MHz is measured to 30.2%. But for TMS320F28377D, the CLA executes the ISR. So its CPU utilization is almost 0% and its CLA utililization is 23.8% with the same switching frequency of 20 kHz and the CLA clock frequency of 80 MHz. The fault response time for the micro-controllers to block the gate pulses has been found to be sufficient to protect both the PMSM and the VSC. The fault response time has been measured to be 20 ns for TMS570LS1227 and 60 ns for TMS320F28377D. Also the effect of PWM and ADC resolution on the motor control has been compared with the simulated results and found to have the same effect on the real system. The real system torque response do not look like the designed first order response due to the presence of the additional impedance in the hardware connecting the micro-controller evaluation board and dSpace.

Though both the evaluated controllers is suitable for PMSM control, TMS570LS1227 has been developed by Texas Instrument with safety features that helps to achieve ASIL-D. But it doesn‘t have any special units to perform mathematical operation fast and to take care of some of the critical tasks independent of the CPU. TMS320F28377D has, a fast processing mathematical unit and a CLA to take care of critical tasks independent of the CPU. Though it has some safety features to achieve ASIL-D, it is not assured that it will be possible to achieve, unless application developers work on it. Based on the evaluation of the micro-controllers a suitable architecture that provides the powerful control performance and safety features that helps in achieving ASIL-D has been suggested.

Index Terms: PMSM, PWM resolution, ADC resolution, TMS570LS1227, TMS320F28377D, Digital control, SVPWM.

Acknowledgements

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Last but not least, a word thank you just not sufficient for my whole family, who understands me and helped me to continue my studies after few year of my professional career.

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Rathinavel Jeyabalan
Göteborg, Sweden, 2015

Contents

Chapter 1

Introduction

1.1 Problem background

Electric mobility is one of the essential element to design a sustainable passenger and freight transport. Several studies show that the global transport capacity will continue to increase and the global vehicle stock would be double by 2030. This accompanied with rising gas prices and stricter emission regulations have increased the importance of electric hybrid vehicles [21]. Volvo Group Truck Technology (GTT), Advanced Technical Research(ATR) division identify this as an important area and are currently involved in several electro mobility projects. The Europian union project COSIVU (COmpact, Smart and reliable drIVe Unit for commercial electric vehicle) is one of those projects [12].

The project COSIVU aims at investigating new system architectures for the electric drive-trains by developing a prototype of a smart, compact and durable single wheel drive unit. The drive unit has a compact transmission, full SiC power electronics (switches and diodes), a novel control and health monitoring module with wireless communication and an advanced ultra-compact cooling solution. The project's main approach is in substituting the central drive train by compact and smart drives attached to the individual wheels, controlled by a central vehicle computer. This will reduce the heavy transmission units and improve the drivability and performance of the vehicle, together with reduction in space and weight. The main focus of the COSIVU project will be on a smart system consisting of power, control and communication modules integrated into the next generation type of traction system in VOLVO truck commercial vehicles [12].

As a part of the COSIVU project, VOLVO GTT, ATR has developed a prototype of a permanent magnet synchronous motor (PMSM) control system for a single wheel drive unit, similar to the one shown in Figure 1.1. The control system receives torque reference (T_e^*) from the user and based on that it calculates the required stator current (i_s^*) of the PMSM. The signals from the resolver sin_{res} and cos_{res} is used to estimate the electrical position and speed of the PMSM rotor, θ and ω respectively. The measured PMSM stator current (i_s) is compared with i_s^* and the error is given to the current controller block. The current controller is a proportional and integrator (PI) controller which calculates the required PMSM stator voltage ($u_{s,ictrl}^*$) to minimize the error. The voltage calculation block compensates $u_{s,ictrl}^*$ for the estimated disturbances in the system and re-calculate the required PMSM stator voltage to u_s^*. The dc link voltage u_{dc} is used to limit u_s^* to keep it within the maximum voltage that converter could produce. The limited u_s^* is used to generate the gate signals t_a, t_b and t_c for the power electronic converter using the space vector pulse width modulation (SVPWM) technique. The gate signals are used to ON/OFF the semiconducting switches in the voltage source converter, which provides the three phase voltage to the PMSM stator. The detailed description of the control algorithm and the SVPWM technique will be described in Chapters 2 and 3.

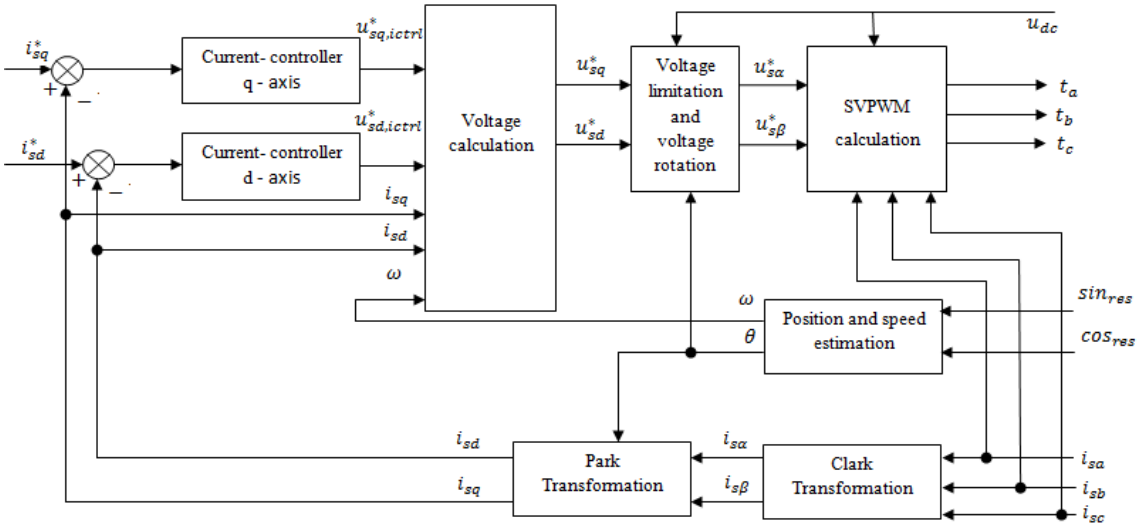


Figure 1.1: An overview of the PMSM control developed by VOLVO GTT,ATR.

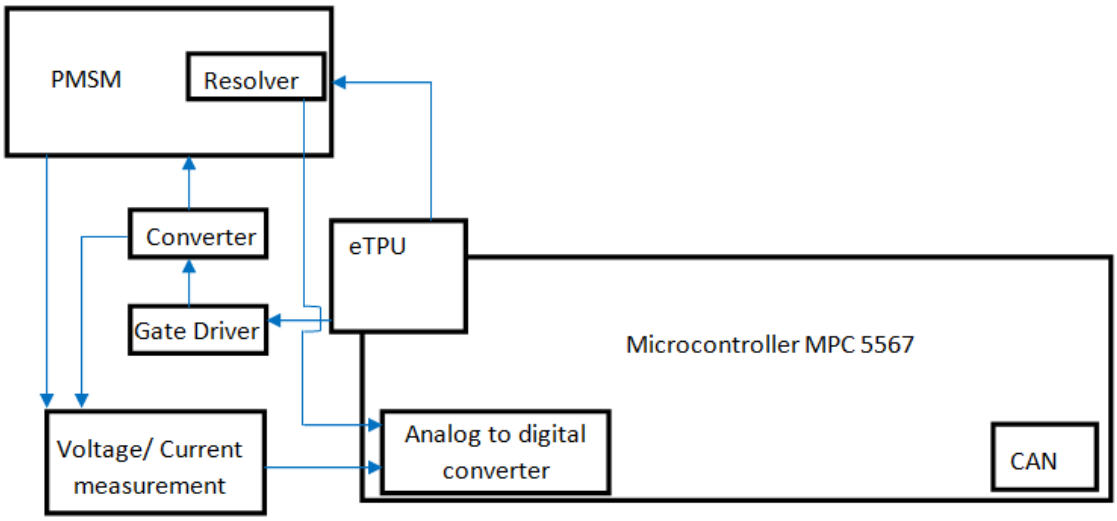


Figure 1.2: Existing micro-controller architecture overview

The simple overview of the existing micro-controller architecture for the PMSM control system prototype at Volvo is shown in Figure 1.2. The prototype system has been implemented using the micro-controller MPC5567 and an enhanced time processing unit (eTPU). The eTPU is mainly used for the time critical activities like gate signal generation and resolver excitation signal generation. The resolver output signals and other required signals are measured with the micro-controller analog to digital converter. The existing prototype has many issues like non availability of a proper compiler and timing issues with the eTPU. The supplier also has stopped supporting the eTPU. Another limitation with the present system is that the CPU of the MPC5567 is almost fully utilised when the switching frequency of the converter is 8 kHz. Volvo wants to increase the switching frequency for the new converter based on silicon carbide (SiC). In-order to achieve that, a processor with higher capacity is required.

Due to the development in electronics, there is a large number of micro-controllers available for motor control applications, but there is no defined methodology to choose the best micro-controller architecture that provides the best motor control performance. This master thesis will evaluate the suitable micro-controller architectures for this application.

1.2 Aim

The aim of this thesis is to suggest the important micro-controller properties to be verified while selecting the micro controller for the permanent magnet synchronous motor (PMSM) control in the automotive applications. The aim is also to list the various micro-controller architectures suitable for the PMSM control based on their datasheet properties and to evaluate the selected micro-controller architectures on its PMSM control performance.

1.3 Method

In the first part of the thesis, the micro-controller properties that affects the PMSM torque control in the automotive application will be discussed and it will be used as a selection criteria for the micro-controllers. The required micro-controller properties for this thesis can be divided into two, based on the PMSM control requirements and based on the automotive specific requirements given by VOLVO.

As described in Section 1.1 the micro-controller receives signals from the PMSM rotor position sensor and the stator current measurement system. The accuracy of measuring the rotor position and the stator currents will play an important role in the PMSM control performance. Also the micro-controller gives out the gate signals generated based on the pulse width modulation (PWM) technique. The resolution of the PWM determines the smallest variation in the voltage that could be obtained from the voltage source converter. So the resolution of the PWM is one of the parameter to be considered for the micro-controller selection. The clock frequency of the micro-controller which controls the PMSM should be high enough to make the central processing unit (CPU) of the micro-controller to compute all the necessary calculations required for the PMSM torque control at a faster rate. In addition to the high clock frequency, if there is a fast mathematical unit or co-processor unit that can help the CPU to run the PMSM control faster and/or to handle the functions other than the PMSM control like communication, temperature monitoring etc, will make the micro-controller more efficient. The micro-controller properties that affects the PMSM control are

- CPU clock frequency.
- Resolution of the PWM.
- Accuracy of the analog to digital converter (ADC) which measures the PMSM stator current.
- Accuracy of the PMSM stator position measurement module.
- Fast mathematical unit or co-processor to support the CPU.

The present VOLVO prototype is having the license from the service provider ARCCORE, who provides support for implementing AUTOSAR (AUTomotive Open System ARchitecture) in the micro-controllers. Also VOLVO aims at achieving ASIL - D (Automotive Safety Integrity Level D) as per ISO 26262 for their future products. So in this thesis automotive specific requirements for the micro-controllers are considered as

- Possibility of making the micro-controllers to be in compliant with Automotive safety integrity level D (ASIL D) as per ISO 26262 [1].
- AUTOSAR support from ARCCORE [2].

In-addition to this, availability of the micro-controller debugging tools, customer support, documentation for the motor control specific to the micro-controller and the availability of free licenses for the compiler with the evaluation kit are also considered as selection criteria for the micro-controllers. The mathematical model for the digital PMSM control will be designed in MATLAB/Simulink and the model will be used to estimate the minimum PWM resolution and ADC resolution required to have a good torque control. Also the model will be used to show the effects of the error in the rotor position measurement. Based on the results, a few of the available

micro-controllers in the market that are suitable for the PMSM torque control in the automotive application will be listed. Two of the listed micro-controllers, which satisfies most of the selection criteria will be selected for the evaluation purpose.

In the second part of the thesis, the selected micro-controllers will be evaluated for the PMSM control. To reduce the cost and time, instead of evaluating the micro-controllers with a actual motor, VOLVO is making use of the real time simulation environment called dSpace to act as a PMSM. The selected micro-controllers‘ evaluation boards will be purchased and the same will be modified to interface with the existing dSpace system in VOLVO. The PMSM torque control algorithm will be developed using C language to evaluate the micro-controllers.

Each of the micro-controllers are first evaluated for the time to complete the execution of the PMSM torque control. Based on the execution time and the suitability of the micro-controllers with respect to the automotive requirement, a micro-controller architecture suitable for the PMSM torque control will be suggested. Also the estimated minimum PWM resolution and ADC resolution for the PMSM control using the simulation, will be verified using the selected micro-controllers.

1.4 Scope

The scope of the thesis includes ordering of new micro-controller evaluation boards, implementing the PMSM control and making arrangement to evaluate the control performance with various micro-controller architectures. The scope does not include evaluation of the PMSM control using various control techniques, as the control is implemented based on Figure 1.1, which is already developed and standardised by Volvo. The power electronics converter and the PMSM will be simulated in Simulink and used for evaluation purpose. So while implementing in the actual system the motor control performance may deviate from the obtained results in the thesis. But the deviation will be mainly due to the parameter variations and losses in the actual system, so it is independent of the type of micro-controller architecture.

Achieving ASIL D in the motor control is not the part of this thesis. But it will be considered as one of the selection criteria while selecting the micro-controller architecture. This may affect the result of this thesis, as when a system implemented with ASIL D there is a chance that the processor utilisation may increase. But during the evaluation, processor utilisation will be verified for its capability to handle the additional tasks required to achieve ASIL D.

Chapter 2

PMSM and its control

The electric motor is one of the main components of electric hybrid vehicles. The selection of the suitable electric motor is significantly important for a hybrid vehicle. Following are the major characteristics of the motors for the electric vehicles [38]:

- High power density.
- High torque at acceleration and high speed during cruise.
- Wide speed range including constant torque and constant power region.
- Fast torque response.
- High reliability and robustness.
- Low cost.

Induction machines and PMSM will satisfy most of the major requirements for the electric vehicles [38]. Based on internal cost and performance requirements, Volvo prefers PMSM for their truck application.

PMSM is a sinusoidally excited brushless motor [44]. The Sinusoidal air gap flux is obtained by the design of the rotor magnets and the armature windings [49]. PMSMs are classified into surface mounted and interior mounted PMSM based on the location of the permanent magnets in the rotor. The maximum speed limit of inner rotors with surface mounted magnets is usually lower than that of interior mounted, as the magnets are usually glued to the rotor [49]. In this thesis a interior mounted non salient PMSM is considered for the following discussions.

2.1 Mathematical model

In the electric vehicles, the electric motor has to be controlled to achieve the torque and speed requested by the driver. A well defined mathematical model of the whole system is required to develop a control system for the torque and speed control. Following assumptions has been made to derive the mathematical model of the PMSM [47] [53] [45]:

- No zero component in the three phase quantities, considering that the neutral is not grounded and the stator windings are perfectly designed to act as a balanced three phase load.
- Flux density in the air gap is assumed to be sinusoidally distributed so that the mathematical model can be derived similar to an ideal three phase system.
- Linear magnetisation characteristics is assumed to represent the variation of the flux as linear quantity without saturation.
- As the losses in the PMSM stator iron core is low and also to have a simple model, the iron loss is assumed to be zero.

- Resistance and inductance are assumed to be independent of temperature and frequency. This assumption will minimize the complexity of the model as the number of variables is reduced.

These assumptions will be helpful to obtain a simple and linear mathematical model of the PMSM which could be used to design the torque controller. The assumptions will not affect the results of this thesis as any modification that are required in the control algorithm could be implemented in the actual system with additional few lines of programming. The corresponding effect on the micro-controller performance will be the same in all the micro-controllers.

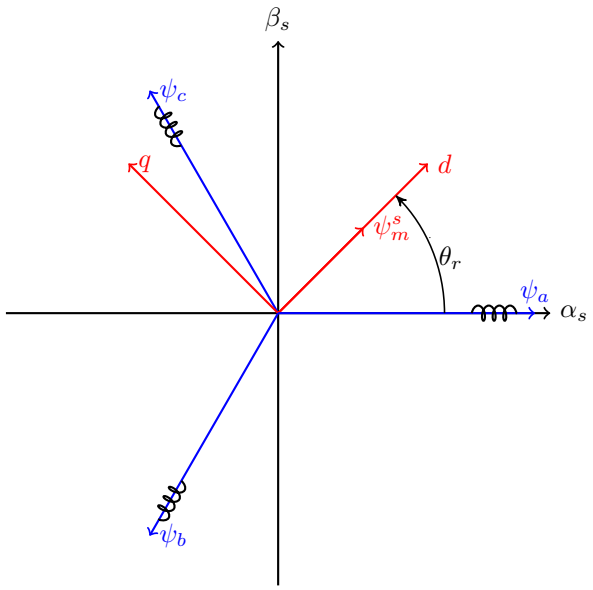


Figure 2.1: Vector representation of the PMSM stator flux in the $\alpha\beta$ and dq co-ordinate systems

The inductance of a PMSM varies according to the rotor position. So the voltage equations of a PMSM can be represented as a time varying differential equations. The time varying differential equations could be converted into a time invariant differential equations in dq co-ordinates using the park and clarke transformations. The time invariant differential equations helps to develop the control algorithm similar to the DC motor control [53] [45].

In Figure 2.1 ψ_a, ψ_b and ψ_c represents the direction of the flux linkage of the three phase stator windings. $\alpha_s\beta_s$ is the two phase stationery coordinate system in stator reference frame and α_s axis is aligned with phase-a. Ψ_m^s is the rotor flux in the stator reference frame which is assumed to be perfectly oriented with the d axis of the dq rotating coordinate system. The dq system rotates at the rotor speed ω_r and making the angle θ_r with the α_s-axis.

Any of the three phase quantities voltage, current or flux can be represented in the two phase $\alpha\beta$ co-ordinate system using the clarke transformation equation [53] [45]

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = K \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{2.1}$$

where K is a transformation scaling constant, (f_a, f_b, f_c) are any of the three phase quantities voltage, current or flux and (f_α, f_β) are the two phase equivalent to the three phase quantities. K is a transformation scaling constant which can take any value other than zero. In this thesis, amplitude invariant transformation is assumed, so the value of K is 1 [45].

The two phase $\alpha\beta$ co-ordinate system can be transformed into a dq co-ordinate system which rotates at the same frequency (ω_1) as that of the three phase system. The transformation to rotating co-ordinate system is done by using the park transformation equation [53] [45]

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = K \begin{bmatrix} cos(\theta_1) & sin(\theta_1) \\ -sin(\theta_1) & cos(\theta_1) \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \tag{2.2}$$

where $\theta_1 = \int \omega_1 dt$ and (f_d, f_q) are the three phase quantity equivalent in the rotating co-ordinate system. As the rotating co-ordinate system is rotating at the same speed as that of the three phase system, in the rotating co-ordinate system the three phase quantities are time-invariant.

If the three phase quantity f is assumed to be the stator voltage (u) of the PMSM, then the stator voltage in the dq coordinate system with the assumptions described in the initial part of this section is given by [39]

$$u_{sd} = R_s i_{sd} + L_s \frac{di_{sd}}{dt} - (\underbrace{\omega_r L_s i_{sq}}_{Cross\ coupling\ term}) \tag{2.3}$$

$$u_{sq} = R_s i_{sq} + L_s \frac{di_{sq}}{dt} + (\underbrace{\omega_r L_s i_{sd}}_{Cross\ coupling\ term}) + (\underbrace{\omega_r \psi_m}_{Back\ emf\ term}) \tag{2.4}$$

where L_s is the equivalent stator inductance of the PMSM, R_s is the stator resistance of the PMSM, ψ_m is the permanent magnet flux of the PMSM rotor, (u_{sd}, u_{sq}) are the stator voltage and (i_{sd}, i_{sq}) are the stator current of the PMSM in the dq co-ordinate system. The cross coupling term introduces a disturbance during the control of the motor, as the control of the d-current is affecting the q-current and vice versa. Similarly the back emf term also introduces a disturbance in the control as increase in speed, will increase the amount of voltage required to produce the same current [45].

The electromagnetic torque T_e produced by the non-salient PMSM is given by [43]

$$T_e = \frac{3np}{2} \psi_m i_{sq} \tag{2.5}$$

T_e can also be expressed in terms of the load angle (δ) which is the difference between the total flux linkage (ψ_s) and the permanent magnet flux (ψ_m) as [43]

$$T_e = \frac{3np}{2L_s} \psi_m \psi_s \sin\delta \tag{2.6}$$

where np is the number of pole pairs in the PMSM. Equations (2.5) and (2.6) show that either by varying i_{sq} or δ, T_e can be controlled.

2.2 Overview of control methods

Vector and scalar control are the two broad categories of controlling the PMSM. Scalar control of the PMSM is also called Voltage/Hz control, in which magnitude of the voltage (V) is varied according to the frequency (f) in a constant ratio V/f. This method is open loop control as it does not uses any feedback such as rotor position or speed. So Voltage/Hz method does not have control over the torque [34] [48]. The V/f method is simple but its dynamic performance is poor and it will introduce high torque ripple [43].

Direct torque control (DTC) and field oriented control (FOC) are few of the vector control methods. In the direct torque control method, the stator flux will be adjusted based on the applied stator voltage. The change in the stator flux, changes the load angle (δ) and T_e as in (2.6). As the torque control is directly based on the electromagnetic state of the motor, similar to the DC motor, this method is called direct torque control. The main advantage of this technique is good dynamic torque control performance [43].

In the FOC, a decoupled control of the torque and flux can be achieved by converting the measured three phase current into the dq co-ordinate system using the park and clarke transformations. This transformation also helps to implement the control algorithm similar to the DC motor control. Considering the rotor flux is perfectly oriented, (2.5) shows that by varying the q-current T_e can be controlled. Generally the d-current is used only when the PMSM is operated in the field weakening region otherwise it is kept zero and the rotor flux will be constant due to the presence of the permanent magnet. When a negative d-current is injected, the effective flux and the u_{sq} required to produce the same i_{sq} is reduced as per (2.4). This helps the PMSM to increase the speed without reaching its voltage limit. As the FOC involves more mathematical transformations,

its control algorithm is complex compared to the DTC and V/f method [35]. But the FOC has a good steady state performance compared to the other control methods [43].

2.3 Rotor position sensor

As described in Section 2.2, converting the three phase stator current to the dq co-ordinates using the clarke and park transformation is very important for the field oriented control. The park transformation requires the position of the PMSM rotor as shown in (2.2). The inaccuracy in the estimated rotor position results an error in the determination of the d-current and q-current, which in turn affects the torque control as the torque is dependent on the q-current as shown in (2.5).

There are different types of PMSM rotor position sensors available, like hall effect sensors, incremental encoders and resolvers as examples. The incremental encoder provides the digital counts defining the position of the rotor. It needs the exact alignment before the motor starts to find the actual position. The electrical speed of the rotor can be give by [28]

$$\omega_r(N) = \frac{\theta_r(N) - \theta_r(N-1)}{T_{sample}} \tag{2.7}$$

where $\omega_r(N)$ is the electrical rotor speed at sample N in radians per second, T_{sample} is sampling period in second, $\theta_r(N)$ is the electrical rotor position at sample N and $\theta_r(N-1)$ is the electrical rotor position at sample N-1 in radians.

For the hall effect sensor, the rotor is divided into six sectors (k) based on its magnetic axis and the sensor detects when the rotor magnetic axis enters each 60^o sector. Then the electrical speed of the rotor in the sector k ($\hat{\omega}_{r,k}$) can be given by [40]

$$\hat{\omega}_{r,k} = \frac{\pi/3}{\triangle t_{k-1}} \tag{2.8}$$

where $\triangle t_{k-1}$ is the time interval taken by the rotor to cross the previous sector $k-1$. The estimated instantaneous electrical rotor position $\hat{\theta}_{r,k}(t)$ within the sector k is given by

$$\hat{\theta}_{r,k}(t) = \theta_{r,k} + \omega_{r,k}(t - t_k) \; with \; \theta_{r,k} \leq \hat{\theta}_{r,k}(t) \leq \theta_{r,k} + \frac{\pi}{3} \tag{2.9}$$

where $\theta_{r,k}$ is the initial angle of the rotor in the sector k measured from a fixed axis reference.

The resolvers are considered as a inductive position sensor which have their own rotor and stator windings. The resolver rotor is mounted on the motor shaft and the resolver stator is fixed to the motor shield. The resolver rotor windings are excited with a high frequency excitation signal (U_{ext}). The two resolver stator windings are placed in quadrature to each other such that the amplitude of its induced voltages are proportional to *sin* and *cosine* of the motor rotor electrical position (θ_r), when the resolver rotor is excited with U_{ext}. The amplitude of the induced voltages in the resolver stator windings can be given by

$$U_{\sin\theta_r} = KU_{ext}\sin\theta_r \tag{2.10}$$

$$U_{\cos\theta_r} = KU_{ext}\cos\theta_r \tag{2.11}$$

where $U_{\sin\theta_r}$ and $U_{\cos\theta_r}$ are the two resolver stator winding outputs and K is the transformation ratio of the resolver windings. Equations (2.10) and (2.11) can be used to extract the rotor position θ_r using various techniques [15].

2.4 Pulse width modulation

The simplified circuit of the voltage source converter (VSC) that is used to power the PMSM drive system is shown in Figure 2.2. The mechanical switches S_A, S_B and S_C represents the semiconductor switches, which could either take + or − position. U_{dc} is the DC input voltage and U_A, U_B and U_C are the three phase voltage output of the VSC. Assuming that the positive position

of the switches is referred as 1 (ON) and the negative position is referred as -1 (OFF), the eight possible different states of the VSC at any point of its operation can be shown as in Table 2.1. The voltage vectors U_0 to U_7 are the VSC three phase voltages in the $\alpha\beta$ co-ordinates in each of the eight different states. In Figure 2.3 the eight voltage vectors are shown in the $\alpha\beta$ co-ordinate system together with U_{ref}, which is an example reference voltage to be generated from the VSC in the $\alpha\beta$ co-ordinates.

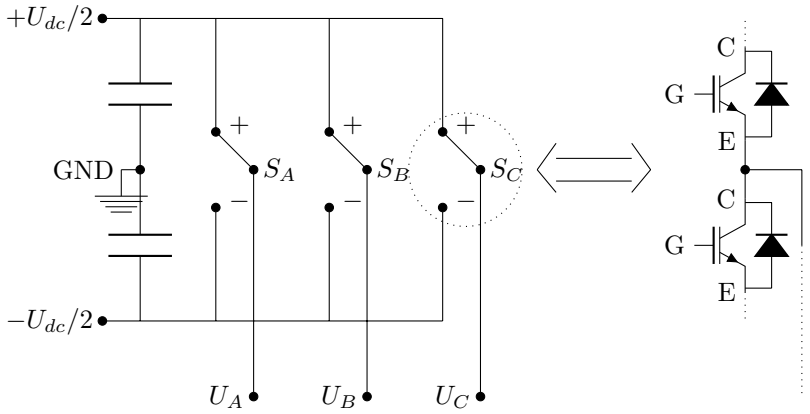


Figure 2.2: The simplified circuit of the VSC. The mechanical switches S_A, S_B and S_C represents the semiconductor switches, here represented as two IGBTs with anti-parallel diodes.

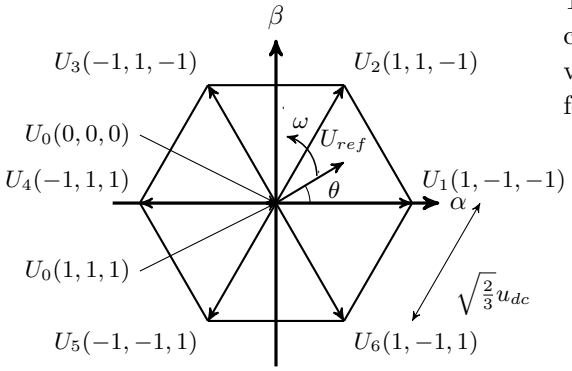


Figure 2.3: The VSC output voltages in the $\alpha\beta$ co-ordinate system for the eight different switching states, and an example reference voltage vector U_{ref}.

Table 2.1: Description of the position of the mechanical switches and the corresponding output voltage of the VSC in the $\alpha\beta$ co-ordinate system for different switching states

Switch state X	**Switch position (S_A, S_B, S_C)**	**VSC output voltage in $\alpha\beta$**
0	(-1, -1, -1)	U_0
1	(1, -1, -1)	U_1
2	(1, 1, -1)	U_2
3	(-1, 1, -1)	U_3
4	(-1, 1, 1)	U_4
5	(-1, -1, 1)	U_5
6	(1, -1, 1)	U_6
7	(1, 1, 1)	U_7

PMSM control requires the semiconductor switches to change its states in a sequence to vary the motor input power as per the control requirement. Pulse width modulation (PWM) technique is one of the widely adopted methods to control the semiconductor switches in the eight different states. The two major types of PWM for three phase inverters are sinusoidal PWM (SPWM) and space vector PWM (SVPWM) [52].

The switching pulses in SPWM is generated based on the intersection between a triangular carrier wave with three 120^0 separated sinusoidal reference waveform. The maximum fundamental peak AC output line-to-line voltage of the VSC using SPWM is given by $\hat{U}_{AB1} = m\sqrt{3}\frac{U_{dc}}{2}$ where m is the ratio of the peak of sinusoidal reference to the peak of triangular carrier wave. Using the same U_{dc}, the peak voltage $\hat{U}_{AB1}$ can be increased by 15.5% when a third zero sequence harmonic is injected to the sinusoidal reference wave [52].

In SVPWM, the duration of the switching pulses are mathematically calculated instead of comparing the phase voltage reference with the carrier wave. Assuming that the U_{ref} is constant for one switching period in Figure 2.3 and it rotates at the speed of ω radians per second in the positive rotating direction. To generate the average output voltage of the VSC equal to U_{ref} in

any switching period, at-least three switching states are used. The two states nearest to U_{ref} is always used to generate the required voltage for the time period of t_1 and t_2. t_1 is the switching time period of the switching state behind the U_{ref} and t_2 is for the switching state after the U_{ref} in Figure 2.3. The third switching state is the zero voltage vector state, either of switching states 0 or 7 or both can be used for the total time period of t_0. There are different methods in choosing the sequence of the switching states based on the applications [52]. The general algorithm of calculating the duration of t_1, t_2 & t_0 is as follows [52]:

- Compute $\theta = arg(U_{ref})$.
- Find the sector and possible combination of the switching states using Table 2.2.
- Calculate the duration of the switching pulse t_1, t_2 & t_0 as [46] [52]

$$\begin{aligned} t_1 &= mT_{sw} \sin\left(\frac{\pi}{3} - \theta + \frac{(n-1)\pi}{3}\right) \\ t_2 &= mT_{sw} \sin\left(\theta - \frac{(n-1)\pi}{3}\right) \\ t_0 &= T_{sw} - t_1 - t_2 \\ m &= \frac{\sqrt{3}|U_{ref}|}{U_{dc}} \end{aligned} \tag{2.12}$$

  where n is the sector number and $0 \leq m \leq 1$ to avoid over modulation.

- Generate the switching sequences as per the application requirement

Table 2.2: Selection of the sector and possible combination of the switching states based on the value of arg (U_{ref})

arg (U_{ref})	**Sector**	**Nearest switching states**
$0° - 60°$	I	1,2
$60° - 120°$	II	2,3
$120° - 180°$	III	3,4
$180° - 240°$	IV	4,5
$240° - 300°$	V	5,6
$300° - 0°$	VI	6,1

The main advantage of this method is the freedom of selecting the switching sequence to reduce the switching losses. There are many different type of switching sequence selections that are discussed in various papers [50] [13] but this is out of the scope for this thesis. One of the widely accepted methods of sequence selection is to generate the center aligned PWM, based on the method described in [13]. In this method, the ON durations for each of the phases are calculated based on

$$\begin{aligned} t_{aON} &= \frac{t_0}{2} \\ t_{bON} &= t_{aON} + t_1 \\ t_{cON} &= t_{bON} + t_2 \end{aligned} \tag{2.13}$$

The ON duration of the switches has to be selected based on Table 2.3. The switching sequence at which each of the switches will be switched ON/OFF can be obtained by comparing the ON durations of the three phases with a triangular waveform as shown in Figure 2.4.

Table 2.3: The ON duration of the switches S_A, S_B, S_C for different sectors

	Sector I	**Sector II**	**Sector III**	**Sector IV**	**Sector V**	**Sector VI**
S_A	t_{aON}	t_{bON}	t_{cON}	t_{cON}	t_{bON}	t_{aON}
S_B	t_{bON}	t_{aON}	t_{aON}	t_{bON}	t_{cON}	t_{cON}
S_C	t_{cON}	t_{cON}	t_{bON}	t_{aON}	t_{aON}	t_{bON}

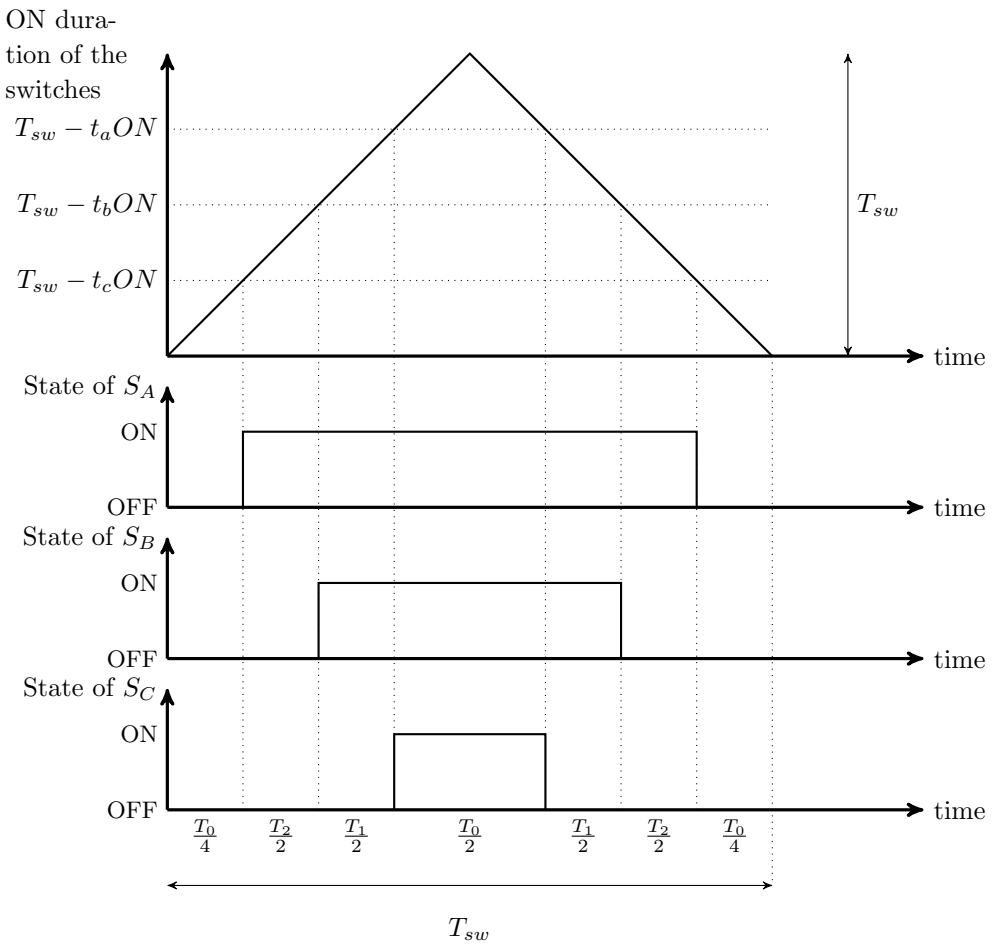


Figure 2.4: Switching sequence of the switches S_A,S_B and S_C when the voltage reference is in the sector IV

Chapter 3

Digital control parameters and algorithm of PMSM control

In the initial part of this chapter some of the importance of the digital control parameters that affects the PMSM control like floating and fixed point representation of the data, sampling frequency, resolution of the PWM and resolution of the analog to digital converter will be discussed. Then the digital control algorithm for the PMSM control that is used in this thesis will be described.

3.1 Resolution of the PWM

Resolution of the PWM is used to determine the smallest variation in time that can be brought in PWM. The smallest time variation determines the resolution of the voltage from the three phase converter which helps in the motor control. So fixing the resolution of the PWM is one of the critical parameter in the digital motor control.

Resolution of the PWM can be calculated based on [17]

$$\frac{2^{res}}{f_{OSC}} = \frac{1}{f_{PWM}} \tag{3.1}$$

where res is the resolution of the PWM in bits, f_{OSC} is the clock frequency of the oscillator and f_{PWM} is the PWM frequency. The PWM frequency will be selected based on the type of the semiconductor switch used in the VSC, electromagnetic interference, noise and the power loss requirement. As per [41], the PWM should at least be of 8 bit resolution to have reduced harmonics in the output voltage.

3.2 Sampling frequency

In-order to transfer the real world signals to the digital world, sampling of the analog signals at the required interval is an important factor. In the motor control, sampling of the position sensor signals and the stator current feedback is the most critical signals to be sampled. The stator current sampling instant should be chosen in such a way that the signal do not have any disturbances due to commutation of the switches. The best time to sample the stator current for the converter operating using the SVPWM technique is in the middle of the duration when the zero vector is applied [42]. The duration of the zero vector should atleast be more than the settling time of the current after the switch in ON. Also the sampled signal should be processed and the PWM duty cycle has to be updated based on the control requirement within the next PWM cycle. In-order to do so, the sampling frequency should at least be equal to the frequency of the PWM.

3.3 Resolution of the analog to digital conversion

Analog to digital conversion (ADC) is required in the PMSM control for the measurements like the stator current feedback, DC bus voltage, position sensor signal etc. The accuracy of the ADC

for the current measurement will affect the accuracy of current control which in turn gives poor torque control and the accuracy of the ADC for the position sensor signals results in a error-nous calculation of the d and q current which causes a poor torque control. So the resolution of the analog to digital converter plays a major role in determining the torque control performance of the motor control.

3.4 Floating and fixed point data

Fixed point data is used to represent the numbers with constant number of digits after the decimal point like 567.89, 56.78 etc. Whereas the floating point data is used to represent 0.56568, 5678000000, 0.000005678 etc. The fixed point data representation is sufficient for the motor control, but care should be taken during the development of algorithm with proper scaling factor. If the floating point data is used the development of the algorithm is much easier but the cost of the micro-controller supporting the floating point operation without too high CPU load. With the present developments in the micro-controllers there are many controllers with the floating point data support is available, which makes the work of the algorithm developer easier [3].

3.5 Digital control algorithm

In this thesis, FOC designed based on the internal model control (IMC) [45] with the incremental encoder position feedback and the gate signal generation based on the SVPWM technique will be implemented in a micro-controller for the evaluation purpose. The flow chart of the digital FOC algorithm for the PMSM is shown in Figure 3.1. When the micro-controller is powered up and starts running, the micro-controller peripherals like the PWM module, the ADC module and the encoder module will be initialized. Then the PMSM control parameters like the proportional and integral constant for the current controller, the maximum voltage, the maximum current and DC link voltage of the VSC will be initialized. Then the micro-controller will wait for the "motor drive enable" command from the user. Once the micro-controller receives the "motor drive enable" command, the low priority control loop will be executed. Any time during the control process, if the fault occurs the system will block the PWM and waiting for the "motor drive enable" command from the user. The low priority control loop described in Figure 3.1 is mainly used to get input from the user. The PMSM stator q current reference (i^*_{sq}) is calculated based on (2.5) using the torque request (T^*_e) input from the user in the low priority control loop. The PMSM stator d current reference is always assumed to be zero and the field weakening algorithm is not considered for the evaluation purpose.

3.5.1 Measuring the stator currents

The timing diagram representing the sequence of occurrences of the events ADC start of conversion (SOC) interrupt, ADC sample and hold (SH), ADC conversion, ADC end of conversion (EOC) interrupt, interrupt service routine (ISR) and PWM duty cycle update are shown in Figure 3.3. The micro-controller PWM module is configured to generate the ADC SOC interrupt at the centre of the PWM cycle (T_1 and T_3). The ADC module starts sampling the PMSM stator current i_{sa} and i_{sb} simultaneously after receiving the SOC interrupt. At the end of the sample and hold time specified in the ADC register, the sampled currents are converted into its binary equivalent and stored in the micro-controller memory. After the ADC conversion event is completed, the end of conversion (EOC) interrupt is generated to initiate the interrupt service routine (ISR) in the high priority control loop. The steps in the ISR and the signals exchanged between the micro-controller, the VSC and the PMSM are shown in Figure 3.2.

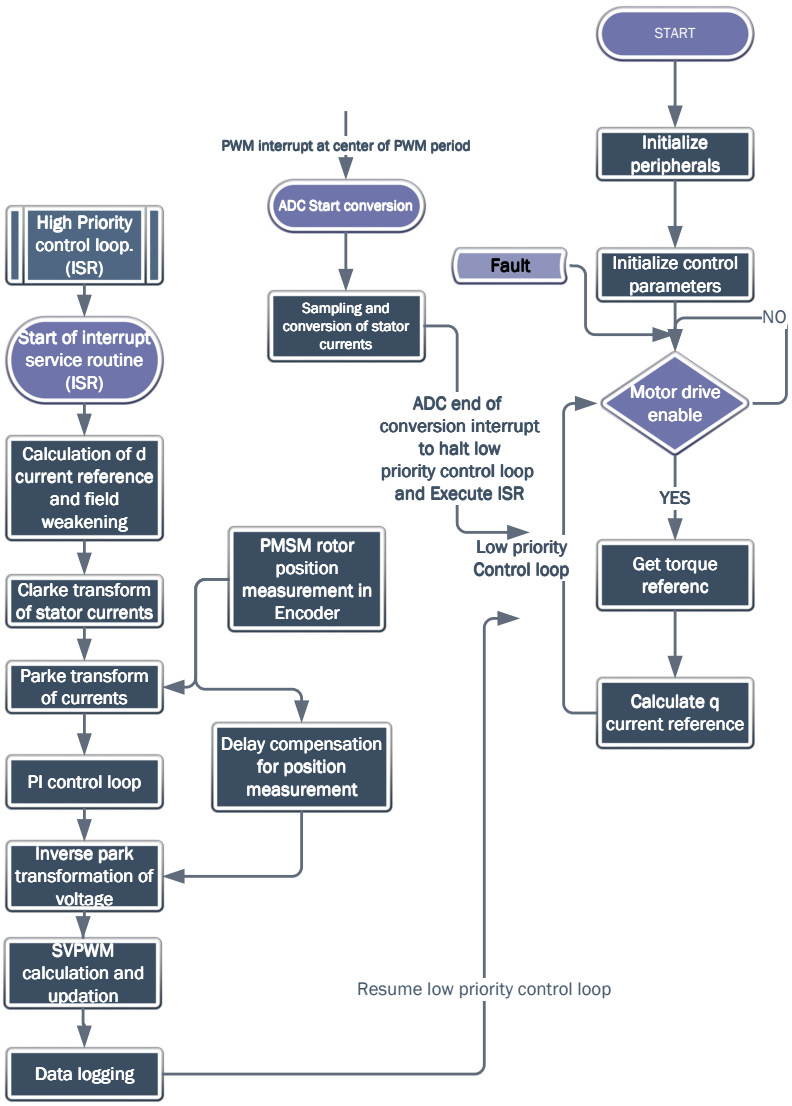


Figure 3.1: General PMSM digital FOC algorithm

The measured stator currents i_{sa} and i_{sb} are converted to the $\alpha\beta$ co-ordinates using the clarke transformation. The PMSM is a balanced load as per the assumptions described in Chapter 2. So the sum of the stator currents of the PMSM is zero and the stator current i_{sc} can be represented in terms of the stator current i_{sa} and i_{sb} as [53]

$$i_{sc} = -(i_{sa} + i_{sb}) \tag{3.2}$$

The amplitude invariant clarke transformation to convert the measured stator currents to the $\alpha\beta$ co-ordinates can be written using (3.2) and (2.1) as

$$\begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \end{bmatrix} \tag{3.3}$$

The stator currents in the $\alpha\beta$ co-ordinates are converted to the dq co-ordinates using the park transformation [53]

$$\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} \cos\theta_r & \sin\theta_r \\ -\sin\theta_r & \cos\theta_r \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} \tag{3.4}$$

where θ_r is the electrical position of the rotor.

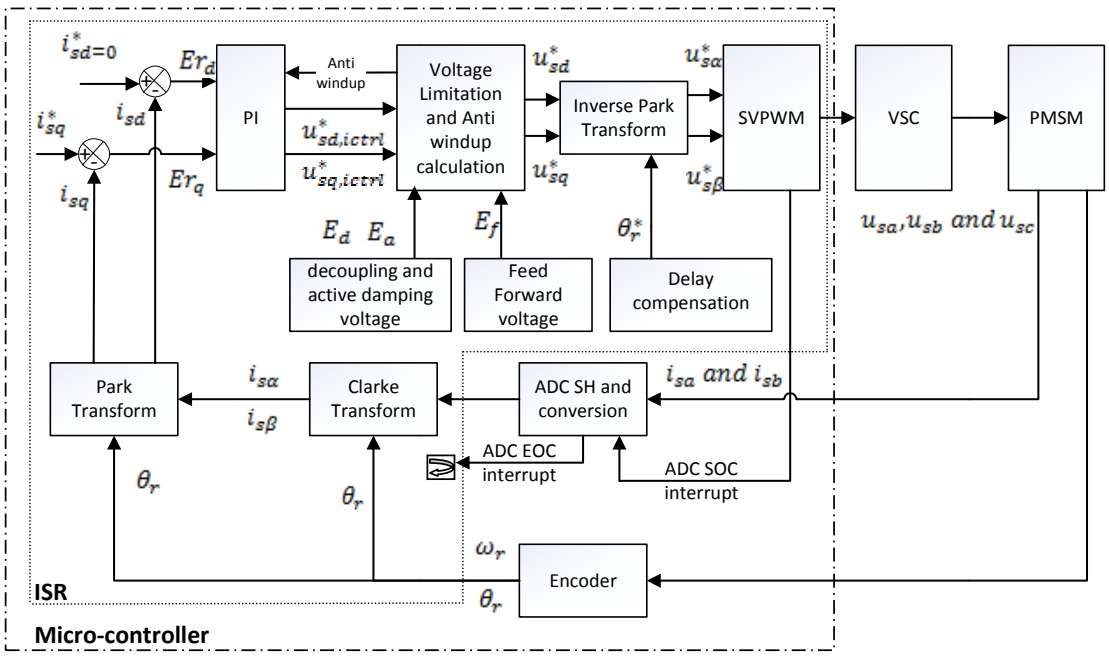


Figure 3.2: Overall representation of the PMSM control including the algorithm implemented in the micro-controller and the signals exchanged between the micro-controller, the VSC and the PMSM

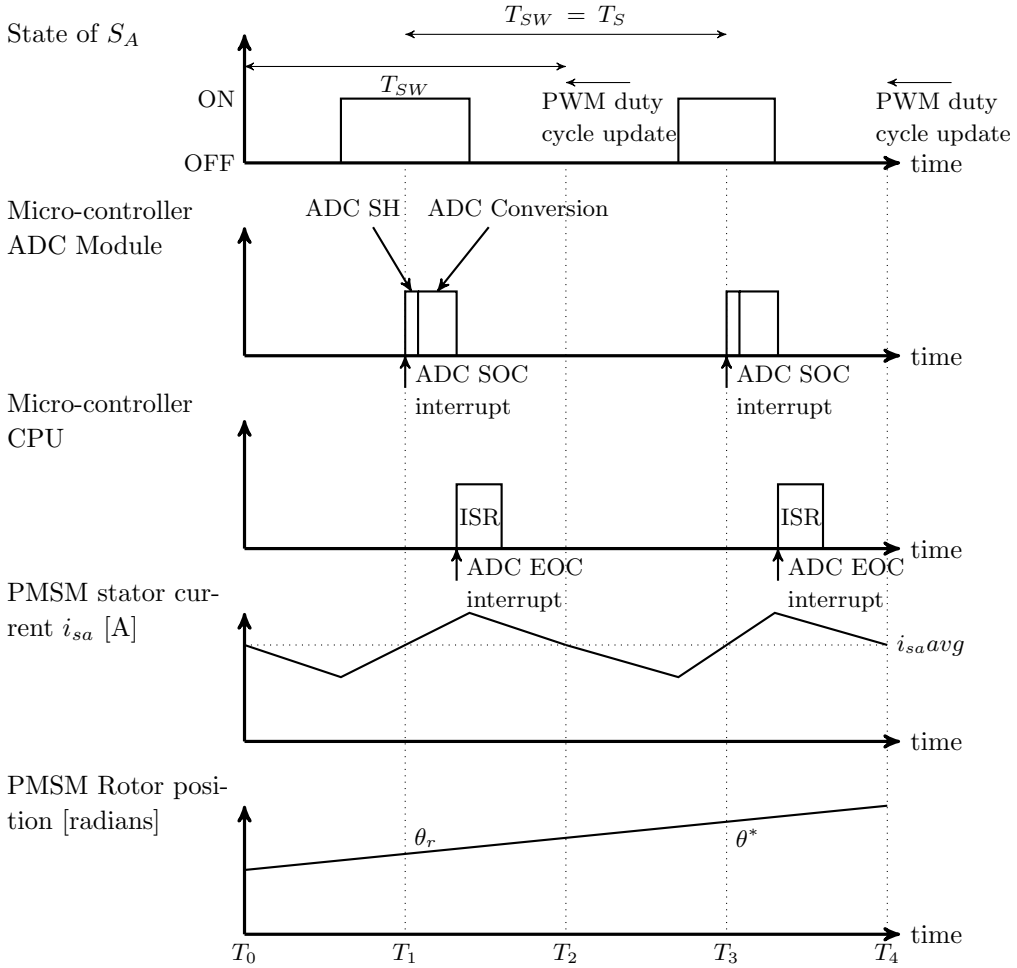


Figure 3.3: Timing diagram representing the sequence of occurrences of the events SOC interrupt, ADC SH, ADC conversion, EOC interrupt, ISR and PWM duty cycle update

3.5.2 Current PI control

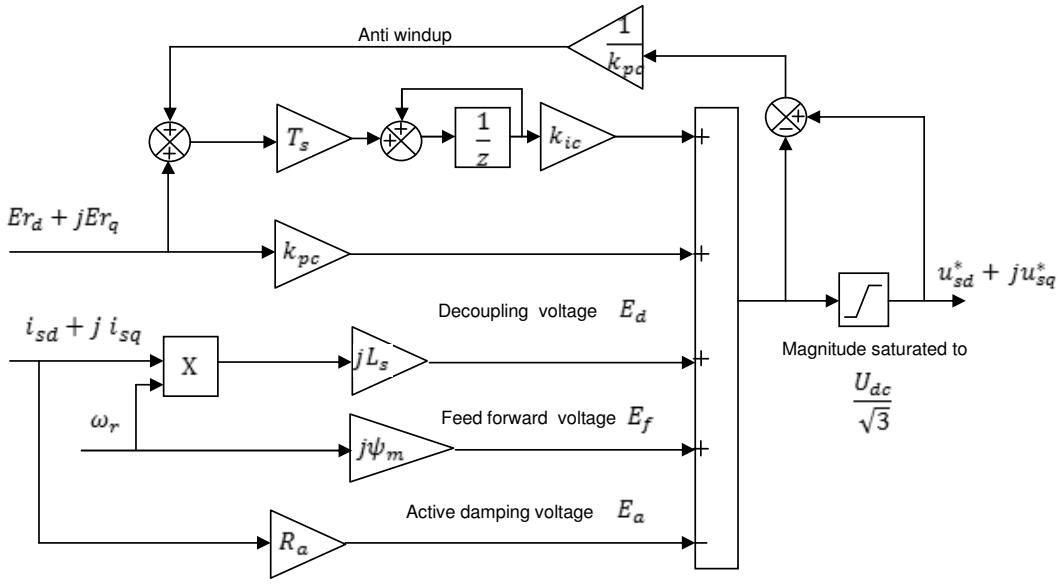


Figure 3.4: PMSM Current PI controller

Figure 3.4 shows the internal function of the blocks 'PI' and 'Voltage limitation and Anti-windup calculation' described in Figure 3.2. When there is a sudden increase in the current reference to the PI controller, the controller tries to ask for more voltage to achieve the required current set-point. As the magnitude of the output voltage reference in the dq co-ordinates ($u^*_{sd,ctrl}$ and $u^*_{sq,ctrl}$) from the current controller is limited to the maximum voltage rating of the VSC ($U_{dc}/sqrt(3)$), there is a chance that the voltage output is saturated during the control process, which causes the accumulated error to be more than zero when the actual current increases equal to the set-point. So the PI controller takes additional time to reduce the error, which may results in a overshoot and the system will not behave as a first order system. So to avoid the overshoot when the current controller output voltage reference is above $U_{dc}/sqrt(3)$, an anti windup designed using the back calculation method is used in the PI control loop [45].

The term $E_f = j\omega_r\psi_m$ in Figure 3.2 is the estimated back emf, this voltage is feed forwarded and added to the voltage output from the current controller to reduce the disturbance in the current controller. Similarly the term $E_d = (j\omega_r\hat{L}_s - Ra)(i_{sd} + ji_{sq})$ in Figure 3.2 is the term correspond to decoupling voltage of the estimated cross coupling factor and it is added to avoid the influence of the d current on the q voltage and vice versa. The active damping voltage $E_a = (i_{sd} + ji_{sq})R_a$ is added to reduce the disturbance in the control due to the error in the estimated parameters of the PMSM. R_a is the active damping resistance and $\hat{L}_s$ is the estimated stator inductance of the PMSM.

3.5.3 Delay compensation for the calculated stator voltage

The output from the block 'Voltage limitation and Anti-windup calculation' in Figure 3.2 is transformed to $\alpha\beta$ coordinates using the inverse park transform as below

$$\begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \end{bmatrix} = \begin{bmatrix} \cos\theta^* & -\sin\theta^* \\ \cos\theta^* & \sin\theta^* \end{bmatrix} \begin{bmatrix} u_{sd} \\ u_{sq} \end{bmatrix} \tag{3.5}$$

where θ^* is the PMSM electrical rotor position compensated for the delay inside the micro-controller. In Figure 3.3 the stator current (i_{sa}) is sampled at T_1 and the current controller in the ISR is trying to achieve the stator current equal to the current reference by modifying the stator voltage. The stator voltage can be modified by changing the duty cycle of the PWM gate signals, but the duty cycle can only be updated at the start of next PWM switching period T_2.

After the duty cycle is updated, the average stator current ($i_{sa}avg$) will be increased/decreased and the i_{sa} will be approximately equal to the required reference current only at T_3 due the PMSM inductance. During the period between T_1 and T_3, the PMSM rotor position must have been changed and that must be estimated accurately to have a better current control as the inverse park transformation is dependent on the rotor position. So the measured electrical rotor position θ_r should be converted to θ^* using (3.6) to compensate for the delay occurred in achieving the required stator current reference.

$$\theta^* = \theta_r + (D\omega_r T_s) \tag{3.6}$$

where T_s is the sampling period and D is the delay factor which takes values 1.5 or 1 [37]. D is 1, if the current is sampled at the center (T_1) of the PWM period as the time difference between the sampling instant (T_1) and T_3 is T_s. D is 1.5, if the current is sampled at the start (T_0) of the PWM period, as the time difference between the sampling instant (T_0) and T_3 is $1.5T_s$. In this thesis, it is considered that the current is sampled at the center of the PWM period, so the delay factor of 1 is used. The output from the inverse park transformation block will be used to generate the PWM gate signals based on the SVPWM algorithm described in Chapter 2.4 and given to the VSC.

3.5.4 Tuning of the current controller

The tuning of the controller can be done by assuming that the current controller is always operated within the voltage limits of the VSC and all the estimated machine parameters $\hat{\psi_m}$, $\hat{L_s}$ and $\hat{R_s}$ matches with its actual value. So the current controller doesn't required anti-windup. The current controller described in Figure 3.4 without anti-windup can be represented using the S-function based block diagram as shown in Figure 3.5.

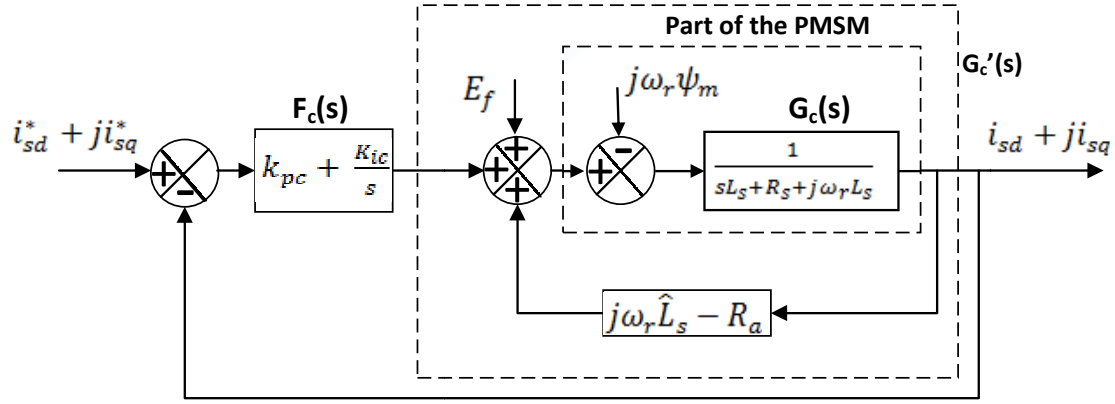


Figure 3.5: S-function based block diagram representation of the current PI controller without anti-windup

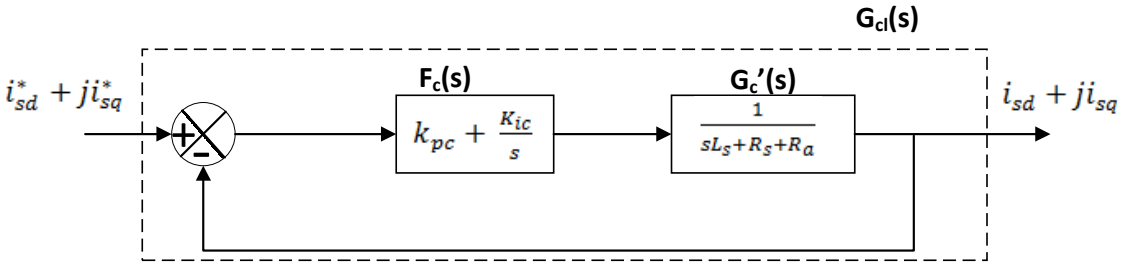


Figure 3.6: Simplified S-function based block diagram representation of the current PI controller with perfectly estimated machine parameter and without anti-windup

In Figure 3.5 $F_c(s)$ is the PI controller. By assuming that the parameters are perfectly estimated $G'_c(s)$ in Figure 3.5 can be written as [45]

$$G'_c(s) = \frac{1}{SL_s + R_s + R_a} \tag{3.7}$$

and the same has been shown in Figure 3.6. The control parameters k_{pc} and k_{ic} can be determined by assuming the closed loop control system $G_{cl}(s)$ to be the first order low pass filter and the bandwidth of $G'_c(s)$ is selected to be same as that of the current controller $F_c(s)$ [45]. Using the assumptions $G_{cl}(s)$, $G'_c(s)$ and $F_c(s)$ can be written as

$$G_{cl}(s) = \frac{\alpha_c/s}{1 + \alpha_c/s} = \frac{F_c(s)Gc'(s)}{1 + F_c(s)Gc'(s)} \tag{3.8}$$

$$F_c(s) = \alpha_c L_s + \frac{\alpha_c(R_s + R_s)}{s} = k_{pc} + \frac{k_{ic}}{s} \tag{3.9}$$

$$G'_c(s) = \frac{1/L_s}{s + (R_s + R_a)/L_s} = \frac{g\alpha_c}{s + \alpha_c} \tag{3.10}$$

where α_c is the bandwidth of the current controller and g is the gain of the closed loop control system. From (3.8), (3.9) and (3.10) the control paramters can be estimated as

$$\begin{aligned} R_a &= \alpha_c \hat{L_s} - \hat{R_s} \\ k_{pc} &= \alpha_c \hat{L_s} \\ k_{ic} &= \alpha_c(\hat{R_s} + R_a) \end{aligned} \tag{3.11}$$

Chapter 4

Simulation of digital control and SVPWM

To analyse the importance of the parameters like ADC resolution, PWM resolution and PWM updation delay during the digital control, a mathematical model is developed in MATLAB simulink. The results of the analysis is discussed in this chapter.

4.1 The impact of PWM resolution on the SVPWM with a RL-Circuit load

A simple three phase RL-load connected to a SVPWM controlled VSC has been simulated in MATLAB Simulink to analyse the effect of the PWM resolution on the total harmonics distortion (THD) and on the fundamental value of the voltage output from the VSC (U_0). A RL-load is considered for this simulation instead of a PMSM, just to avoid the dynamics involved with motor control. This doesn't affect the final result as the voltage output will be same and independent of the type of load used, PMSM or RL-circuit. The VSC is implemented with ideal switches in-order to only see the effects of the PWM resolution.

For all the simulation in this section, the DC bus voltage of the converter is $U_{dc} = 400$ V and the load resistance is $R = 0.4\ \Omega$ and the inductance is $L = 1.1\ \mu$H. According to (2.12) the maximum value of m is 1 and $|U_{ref}|_{max} = 0.5577U_{dc}$. The simulation has been done with the U_{ref} of 10% ($m = 0.1732$), 20% ($m = 0.3464$) and 55% ($m = 0.9526$) of the U_{dc}. Also the switching frequency (f_{sw}) for the simulation has been chosen such a way that it is 10, 20 and 100 times the fundamental frequency (f_{fund}). Both m and f_{sw} has been chosen to represent the low speed and high speed operation of the PMSM.

Table 4.1: The smallest average phase voltage output from the VSC for different PWM resolution in one switching period when the $U_{dc} = 400$ [V].

PWM Resolution	**Smallest average phase voltage output from the VSC in one switching period [V] (U_{dc} is 400 V)**
6 bit	6.25
8 bit	1.5625
10 bit	0.3906
12 bit	0.0977
16 bit	0.0061

The PWM resolution determines the smallest time variation that can be brought in the PWM gate signals as discussed in Chapter 3.1. It also decides the smallest output voltage of the VSC.

Table 4.1 shows that the smallest average phase voltage output that can be obtained from the VSC for different PWM resolution in one switching period. Table 4.2 and Table 4.3 show the THD and the U_0 respectively for different PWM resolutions (PWM_{res}), U_{ref}, switching frequencies and fundamental frequencies. The number of the switching pulses during the fundamental period is the major factor that determines the voltage harmonics. When the PWM_{res} is varied only the time of switching will get affect but not the number of switchings. So the change in the PWM_{res} has a very small affect on the value of the THD when the fundamental frequency and U_{ref} is constant. When the DC voltage at the VSC is constant, the reduction in the output fundamental voltage increases the magnitude of the voltage harmonics as the voltage waveform is distorted more with voltage pulses of short time with same peak in one fundamental period [51]. So the THD increases when both the U_{ref} and U_0 is reduced as shown in Table 4.2.

Table 4.3 shows that the U_0 almost matches with the U_{ref} for the PWM_{res} 8, 10 and 12 bits except for the 500 Hz switching frequency. The SVPWM gate pulse generator receives only the instantaneous voltage references to generate the gate pulse not the fundamental voltage reference. So the SVPWM generator has to receive more number of instantaneous voltage references within one fundamental period, so that the fundamental output voltage will be approximately equal to the U_{ref}. When the switching frequency is reduced, the total number of instantaneous voltage request and the number of voltage pulses in one fundamental period will also reduce. This makes the fundamental value of the VSC output voltage (U_0) deviates from its U_{ref} at 500Hz irrespective of the PWM_{res} and U_{ref} as shown in Table 4.3. When the PWM_{res} is 6 bit, $|U_{ref}|$ is not able to achieve in most of the cases with different switching frequency, PWM_{res} and U_{ref}. So to achieve the best voltage output, the resolution of 8 or 10 bits is minimum required with high switching frequency.

Table 4.2: THD of VSC output voltage in % for different PWM resolutions, switching frequencies, fundamental frequencies and U_{ref}. The DC bus voltage is $U_{dc} = 400$ V

(a) 5 kHz Switching frequency

$\mathbf{\lvert U_{ref}\rvert / U_{dc}}$	**0.55** ($U_{ref} = 220$ **V**)				**0.2** ($U_{ref} = 80$ **V**)			**0.1** ($U_{ref} = 40$ **V**)	
$\mathbf{f_{fund}}$ **[Hz]**	**59**	**50**	**52**	**47**	**50**	**52**	**47**	**59**	**47**
6 bit PWM$_{res}$	57.24	54.97	55.57	54.92	169.5	169.31	169.2	250.12	245.34
8 bit PWM$_{res}$	56.03	55.76	55.67	55.6	164.45	164.53	164.2	264	250.65
10 bit PWM$_{res}$	56.28	55.62	55.57	55.51	164.27	164.42	165.39	254	253.11
12 bit PWM$_{res}$	56.53	55.61	55.59	55.58	164.86	164.28	164.58	254	254.15

(b) 2 kHz Switching frequency

$\mathbf{\lvert U_{ref}\rvert / U_{dc}}$	**0.55** ($U_{ref} = 220$ **V**)				**0.2** ($U_{ref} = 80$ **V**)			**0.1** ($U_{ref} = 40$ **V**)	
$\mathbf{f_{fund}}$ **[Hz]**	**59**	**50**	**52**	**47**	**50**	**52**	**47**	**59**	**47**
6 bit PWM$_{res}$	56.99	55.95	55.57	55.39	168.5	170.2	169.45	247.16	248.46
8 bit PWM$_{res}$	56.26	56.05	56.41	55.71	162.3	165.32	164.7	250.22	254.28
10 bit PWM$_{res}$	55.20	56.28	55.93	55.74	164.22	166.01	165.58	249.82	253.49
12 bit PWM$_{res}$	56.28	56.43	56.16	55.75	164.2	164.37	164.99	255.96	253.77

(c) 500 Hz Switching frequency

$\mathbf{\lvert U_{ref}\rvert / U_{dc}}$	**0.55** ($U_{ref} = 220$ **V**)				**0.2** ($U_{ref} = 80$ **V**)			**0.1** ($U_{ref} = 40$ **V**)	
$\mathbf{f_{fund}}$ **[Hz]**	**59**	**50**	**52**	**47**	**50**	**52**	**47**	**59**	**47**
6 bit PWM$_{res}$	66.87	58.53	66.51	66	168.72	176.89	179.87	261.06	254.34
8 bit PWM$_{res}$	67.77	59.09	68	64.23	163.66	173.74	171.14	283.25	271.71
10 bit PWM$_{res}$	66.97	57.83	68	65.09	161.26	171.95	168.09	270.74	265.15
12 bit PWM$_{res}$	66.4	59.71	67	65.81	161.12	173.74	170.26	274.29	264.37

Table 4.3: U_0 in [V] for different PWM resolutions, switching frequencies, fundamental frequencies and U_{ref}. The DC bus voltage is $U_{dc} = 400$ V

(a) 5 kHz Switching frequency

$\|\mathbf{U_{ref}}\|/\mathbf{U_{dc}}$	**0.55** ($U_{ref} = 220$ **V**)				**0.2** ($U_{ref} = 80$ **V**)			**0.1** ($U_{ref} = 40$ **V**)	
$\mathbf{f_{fund}}$ **[Hz]**	**59**	**50**	**52**	**47**	**50**	**52**	**47**	**59**	**47**
6 bit PWM$_{res}$	218	220.9	220	220.9	76.34	76.45	76.23	40.61	42.58
8 bit PWM$_{res}$	219.6	219.6	220	219.5	80.09	80.01	79.98	38.46	40.94
10 bit PWM$_{res}$	219.7	219.8	220.7	220	80.19	80.06	79.34	39.84	39.99
12 bit PWM$_{res}$	219.2	219.9	220.2	220.2	79.88	80.11	79.95	39.9	39.8

(b) 2 kHz Switching frequency

$\|\mathbf{U_{ref}}\|/\mathbf{U_{dc}}$	**0.55** ($U_{ref} = 220$ **V**)				**0.2** ($U_{ref} = 80$ **V**)			**0.1** ($U_{ref} = 40$ **V**)	
$\mathbf{f_{fund}}$ **[Hz]**	**59**	**50**	**52**	**47**	**50**	**52**	**47**	**59**	**47**
6 bit PWM$_{res}$	219.2	219.2	220.4	220.2	76.95	76.32	76.38	41.92	41.59
8 bit PWM$_{res}$	220.3	219.7	219	219.7	81	79.75	80.01	41.12	39.98
10 bit PWM$_{res}$	221.7	219.3	219.9	219.8	80.23	79.2	79.95	40.74	39.99
12 bit PWM$_{res}$	220.1	219.1	219.3	219.8	80.26	80.02	80.06	39.22	39.73

(c) 500 Hz Switching frequency

$\|\mathbf{U_{ref}}\|/\mathbf{U_{dc}}$	**0.55** ($U_{ref} = 220$ **V**)				**0.2** ($U_{ref} = 80$ **V**)			**0.1** ($U_{ref} = 40$ **V**)	
$\mathbf{f_{fund}}$ **[Hz]**	**59**	**50**	**52**	**47**	**59**	**50**	**52**	**47**	**47**
6 bit PWM$_{res}$	214.1	217.4	210	208.3	78.77	74.09	72.58	40.84	41.93
8 bit PWM$_{res}$	212.8	216	207.8	212.3	81.59	76.63	78.58	35.52	37.17
10 bit PWM$_{res}$	214.5	217.5	208	210.2	83.86	77.25	78.65	38.11	38.71
12 bit PWM$_{res}$	215	215.5	208	208.9	82.99	76.54	79.45	37.35	39.3

4.2 SVPWM with PMSM simulation

The current PI controller, the VSC and the PMSM described in Figure 3.2 has been modelled using simulink and the model is used to evaluate the impact of the PWM updation delay, PWM resolution and ADC resolution on the torque response of the PMSM control system. The PMSM machine parameters used in the simulation for the PMSM model described in (2.3), (2.4) and (2.5) are

$R_s = 0.0273$	Stator Resistance [ohm]
$L_s = 0.738e-3$	Stator Inductance [H]
$\psi_m = 102.9e-3$	Flux Linkage in airgap due to permanent magnet
$J_m = 0.0419$	Motor inertia $[kgm^2]$
$B = 0.01$	Viscous Damping Coefficient
$n_p = 8$	Number of pole pair
$n_s = 1335$	Synchronous speed in rpm.

The current control simulink block is shown in Figure 3.4 and its parameter used for the simulation are

$K_{ic} = 738$	Integration constant for current controller
$K_{pc} = 0.738$	Proportional constant for current controller
$R_a = 0.7107$	Active damping resistance.

Voltage and current limitation settings are kept as

$I_{srated} = 400$	Maximum converter current in [A]
$\|U_{dq}\|_{max} = U_{dc}/sqrt(3)$	Maximum converter output voltage in [V]

and the DC bus voltage is kept constant for all simulations in this section, $U_{dc} = 600$ V. During all the simulation, i^*_{sd} is kept zero so that the system doesn‘t required to be in field weakening mode.

4.2.1 Impact of PWM resolution

The impact of the resolution of the PWM gate signals on the torque step response has been analysed using the developed simulink model. Table 4.4 shows the PWM resolution and its corresponding smallest average phase voltage output from the VSC when the U_{dc} is 600 V and the smallest time variation in the PWM signals when the PWM signal frequency (f_{sw}) is 8 kHz. The two test cases for this simulation are chosen to operate the PWM at the ends of the modulation index:

- Low speed (100 rpm) and low torque (100 Nm) operation of the PMSM which makes the SVPWM to function with lower modulation index, approximately $m = 0.05$.
- Rated speed (1335 rpm) and high torque (300 Nm) operation of the PMSM which makes the SVPWM to function with near to maximum modulation index, approximately $m = 0.9$.

Table 4.4: The smallest average phase voltage output from the VSC for different PWM resolutions ($U_{dc} = 600$ [V]).

PWM Resolution	**Smallest average phase voltage output from the VSC [V] (U_{dc} = 600 V)**	**Smallest time variation in the PWM signals [μs] (f_{sw} = 8 kHz)**
6 bit	9.375	1.95
8 bit	2.344	0.489
10 bit	0.5859	0.122
12 bit	0.1465	0.031
16 bit	0.0091	0.0019

Figure 4.1 and Figure 4.4 shows the torque step response for the different PWM resolutions. The figures also show that the peak to peak torque ripple reduces with increased PWM resolution and the same has been measured after 0.15 s and listed in Table 4.5. The ripple in the torque is due to the switching and due to the difference in the voltage error introduced by the different PWM resolution. The reduction in the torque ripple from the 6 bit operation to 16 bit operation is high when the Te_{ref} is 100 Nm compared to its operation at 300 Nm. When the Te_{ref} is 100 Nm, the stator voltage will be very low with low modulation index and when the Te_{ref} is 300 Nm, the stator voltage will be comparatively high with high modulation index. The resolution will introduce a constant error to the output voltage for all the ranges of the voltage, so the percentage of error will be low for the higher voltage and high for the lower voltage. As the error percentage is high when the Te_{ref} is 100 Nm, it causes more difference in the ripple when the resolution is increased and the same is not the case when the Te_{ref} is 300 Nm as the error percentage in low.

In Figures 4.2 and 4.5, the rise time for the torque step is almost same for all the PWM resolution, except for the 6 bit and 8 bit operation during the torque step of 100 Nm at 100 rpm. This is because during the lower modulation index (U_{ref} is low), $|U_{ref}|$ will not match with the output voltage as per Table 4.3, which causes the difference in the response compared to the high resolution operation. But the same effect cannot be seen in 300 Nm operation as it is operating at the higher modulation index (U_{ref} is high). Also more than 10 bits of resolution has not provided any considerable reduction in the torque ripple as shown in Table 4.5, so the minimum of 10 bit resolution is sufficient to achieve good torque control performance with reduced ripple for this system.

Table 4.5: T_e peak to peak ripple in Nm for different PWM resolutions

PWM Resolution	**6 bit**	**8 bit**	**10 bit**	**12 bit**	**16 bit**
Te_{ref} = 100Nm, 100 rpm	9.2	4.38	2.13	1.32	1.17
Te_{ref} = 300Nm, 1335 rpm	19.96	17.2	17.16	17.02	16.9

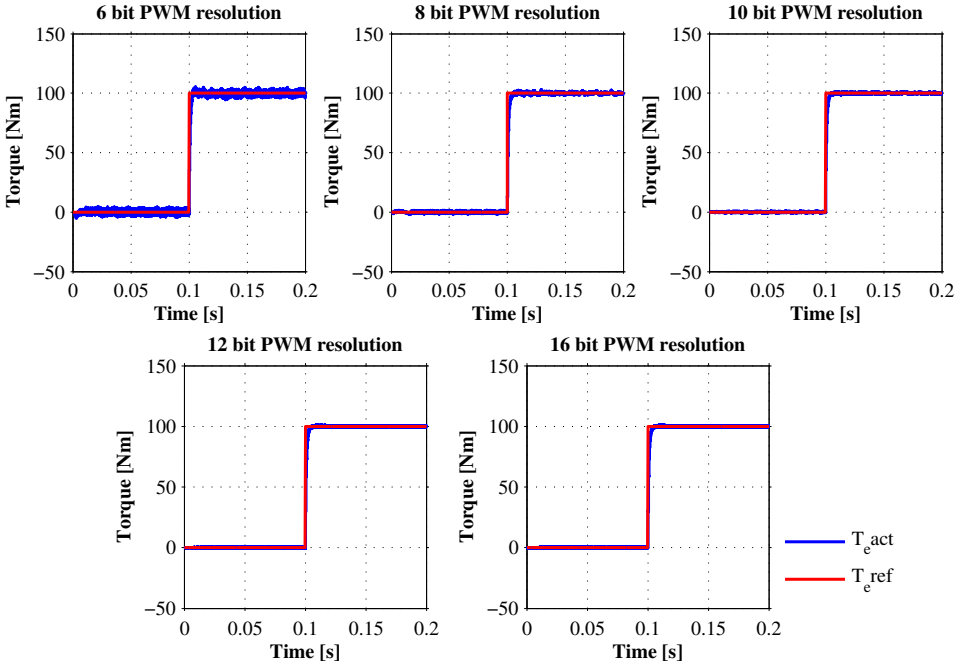


Figure 4.1: T_e step response with f_{sw}=8 kHz, 100 rpm and T_eref = 100Nm for different PWM resolutions

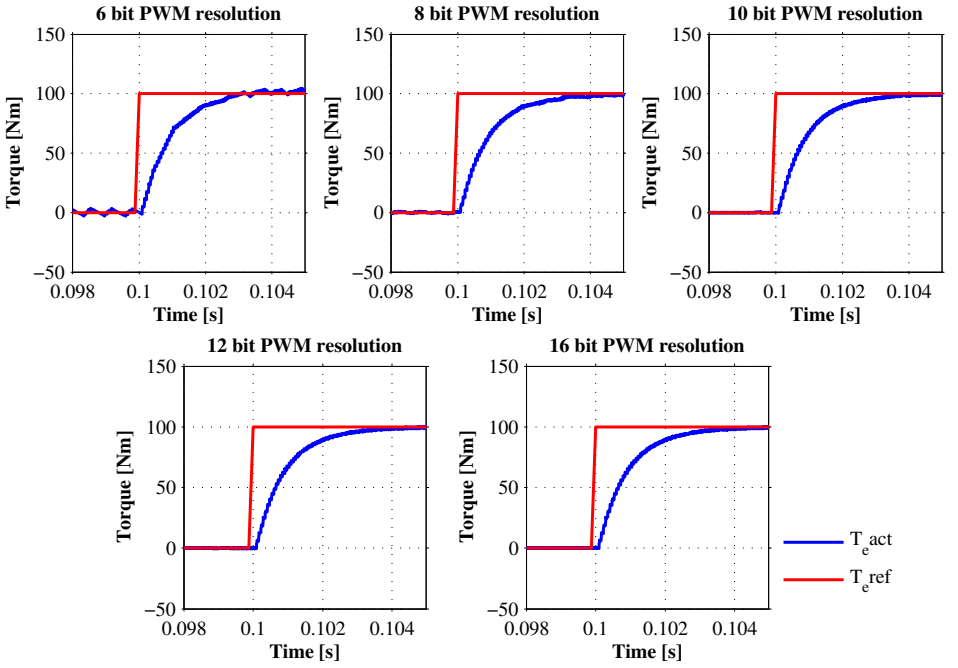


Figure 4.2: Rise time for T_e step response with f_{sw}=8 kHz, 100 rpm and T_eref = 100 Nm for different PWM resolutions

As described in Figure 2.4, $T_0/4$ is the time at which the switch S_A turns ON. Figure 4.3 shows the effect on $T_0/4$ during the torque step when the PWM resolution is 6 bit and 16 bit. In Figure 4.2, the step response of the torque for the 6 bit PWM resolution is not look like the designed first order response. When the resolution is 16 bit, a very small time variation of 0.0019 μs can be brought in on the ON time of the switches and the same results in the variation of the VSC output voltage in steps of 0.0091 V as shown in Table 4.4. But when the resolution is 6 bit, due to the minimum possible time variation of 1.95 μs the VSC output voltage cannot be varied in steps

less than 9.375 V. Also the stator voltage ($|U_{dq}|$) required to operate the motor at 100 rpm and 100 Nm torque is 10 V. So to obtain the required voltage, only a few time steps could be produced by the torque controller. This makes the torque response to deviate from the required first order response. But when the motor speed is at 1335 rpm and T_eref = 300 Nm, the controller could produce comparatively more number of time steps to achieve the required stator voltage $|U_{dq}|$ of 240 V. So the effect is not viewable in Figure 4.5.

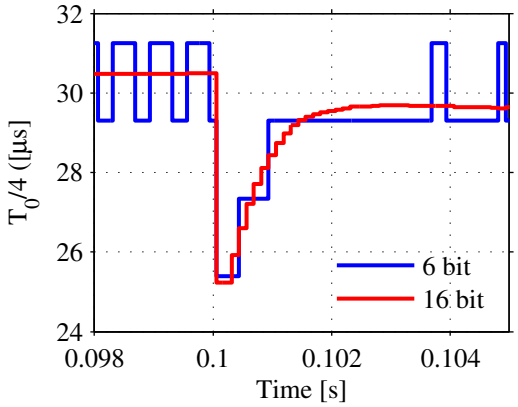


Figure 4.3: Effect of the PWM resolution on the start of the ON time of the switch S_A ($\frac{T_0}{4}$) during the torque step at 0.1 s with f_{sw}=8 kHz, 100 rpm and T_eref = 100 Nm

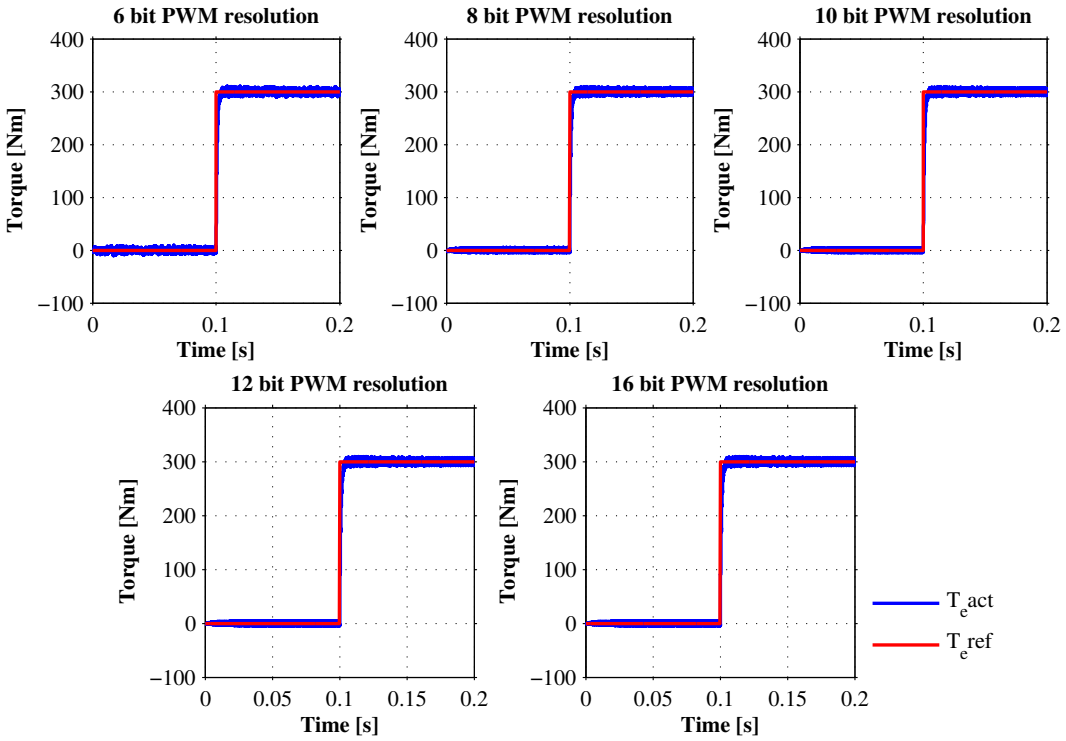


Figure 4.4: T_e step response with f_{sw}=8 kHz, 1335 rpm and $T_eref = 300Nm$ for different PWM resolutions

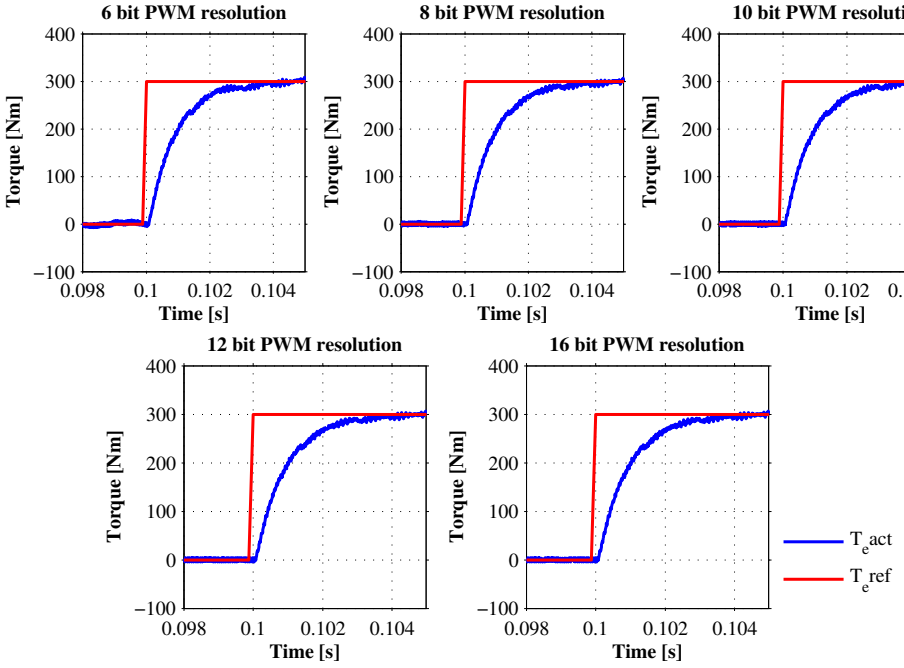


Figure 4.5: Rise time for T_e step response with f_{sw}=8 kHz, 1335 rpm and $T_eref = 300Nm$ for different PWM resolutions

4.2.2 Impact of the ratio f_{sw}/f_{elec} on the torque response

The ratio between the switching frequency and the fundamental electrical frequency of the stator flux will have an impact on the torque response. All the simulation has been done at less than 3000 rpm and 100 Nm torque reference just to operate below the field weakening region. For all cases, the rotor speed and the controller bandwidth is kept constant and the switching frequency is modified to obtain the required f_{sw}/f_{elec} ratio. Figure 4.6 shows the result of the simulation with different f_{sw}/f_{elec} ratios at 1000 rpm and the experiment at 2000 rpm and 3000 rpm also gave the similar results. Table 4.6 shows the peak to peak torque ripple content after the step command, for different f_{sw}/f_{elec} ratios and different motor speeds.

If the ratio f_{sw}/f_{elec} is low, then the number of switching of the VSC within one fundamental period is reduced. This makes a constant stator voltage pulse is applied to the motor for a longer time. It increases the stator current ripple as well as the torque ripple as shown in Table 4.6. Also as the motor under consideration is having low inertia ($J_m = 0.0419\ Kgm^2$) and the rotor position is unknown for longer period due to the low f_{sw}/f_{elec} ratio, the transient response will not be as good as for the high f_{sw}/f_{elec} ratio. The same can be noticed in Figure 4.6 at 0.1s to 0.17s for the ratio f_{sw}/f_{elec} equal to 20 and 30.

Figure 4.8 shows the torque response with 10 times increased motor inertia (J_m=0.419 Kgm^2) for different f_{sw}/f_{elec} ratio. It clearly shows that the torque response is improved during the period 0.1s to 0.17s for the ratio f_{sw}/f_{elec} equal to 20 and 30. The experiment has been repeated with decreasing the fundamental electrical frequency of the stator flux and keeping the switching frequency constant. Figure 4.7 shows that the experiment gives almost similar result to the experiment with constant fundamental frequency. These results clearly show that the torque response is better with atleast f_{sw}/f_{elec} ratio of 40 for the motor under consideration.

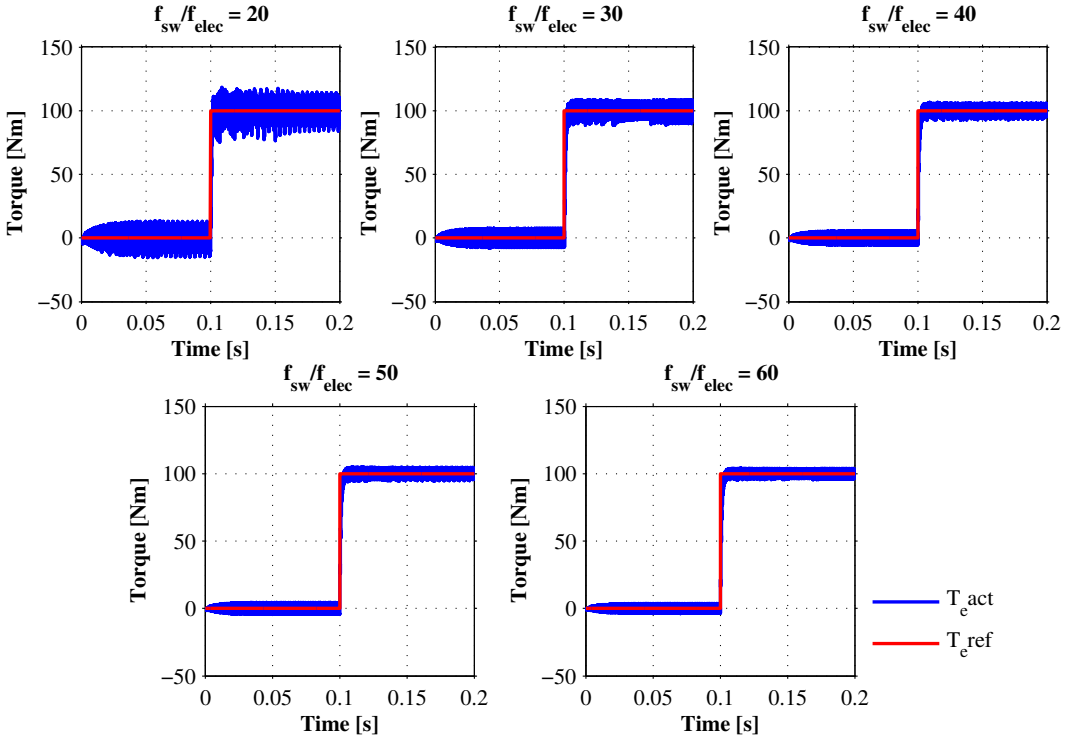


Figure 4.6: T_e step response with 1000 rpm, $T_eref = 100$ Nm and $J_m = 0.0419\ Kgm^2$ for different f_{sw}/f_{elec} ratios (f_{elec} is kept constant while changing the ratio).

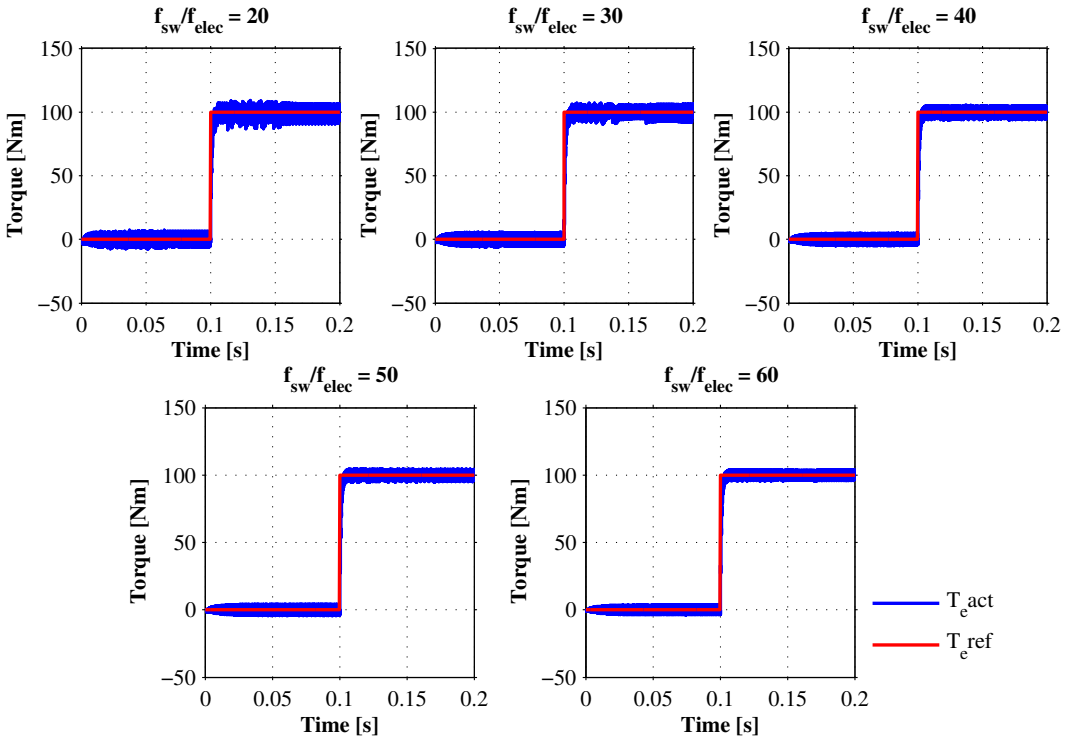


Figure 4.7: T_e step response with $f_{sw} = 8$ kHz, $T_eref = 100$ Nm and $J_m = 0.0419\ Kgm^2$ for different f_{sw}/f_{elec} ratios (f_{sw} is kept constant while changing the ratio).

Table 4.6: T_e peak to peak ripple measured after the step (0.1 s) for T_eref of 100 Nm for different f_{sw}/f_{elec} ratios and different motor speeds in Nm (f_{elec} is kept constant while changing the ratio)

f_{sw}/f_{elec}	**20**	**30**	**40**	**50**	**60**
1000 rpm	40.75	19.68	13.23	10.1	8.30
2000 rpm	26.53	15.44	10.029	7.57	6.08
3000 rpm	21.48	12.51	8.12	6.13	4.93

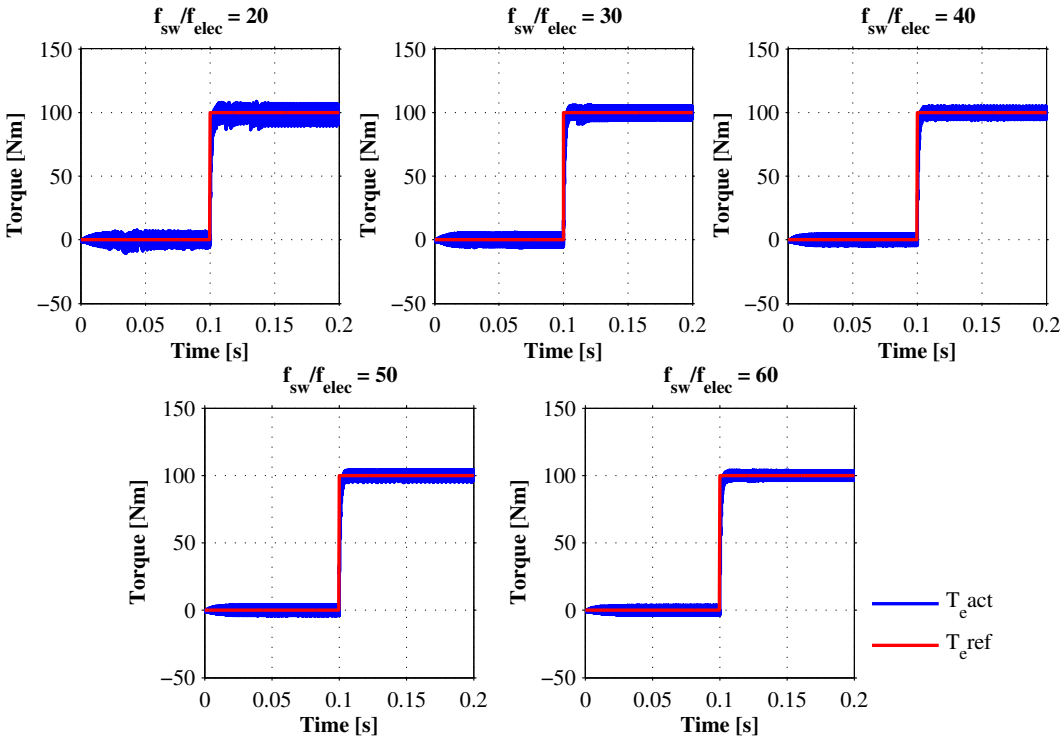


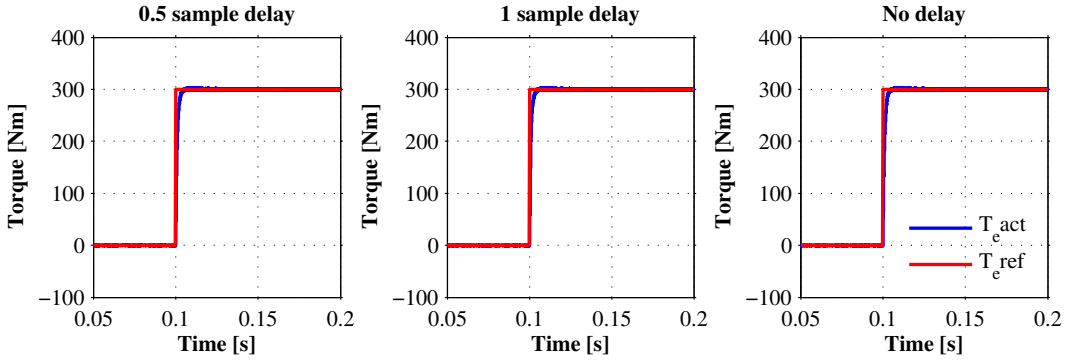
Figure 4.8: T_e step response with 1000 rpm, $T_eref = 100$ Nm and $J_m = 0.419\ Kgm^2$ for different f_{sw}/f_{elec} ratios (f_{elec} is kept constant while changing the ratio).

4.2.3 Impact of PWM updation delay

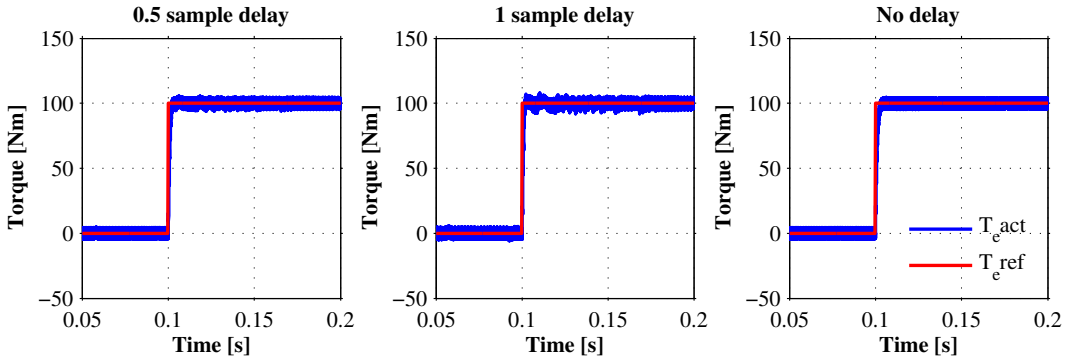
In a digital controller, there is always a delay between the time at which the sample is taken and when the PWM duty cycle is updated, as shown in Figure 3.3. There are two possible PWM updation is possible in the digital controller

- Sample at the beginning of the switching period and update PWM duty cycle at the start of the next switching period
- Sample at the center of the switching period and update PWM duty cycle at the start of the next switching period

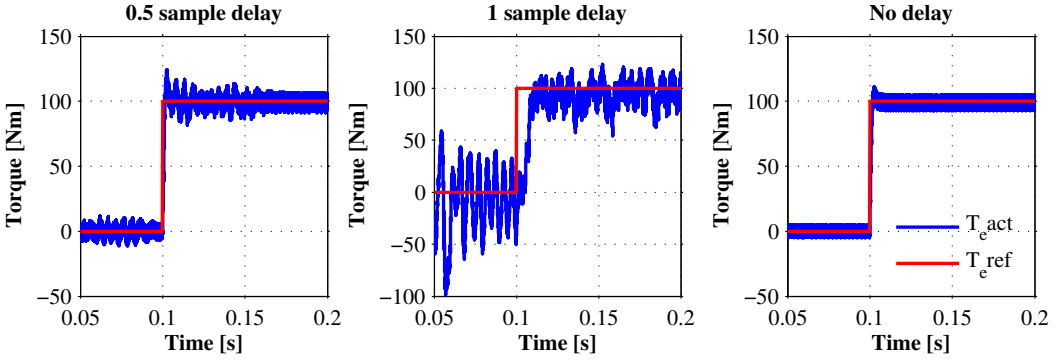
Sampling at the center of the switching period introduces half sample delay and requires a faster digital controller to calculate the new duty cycle within the half sample period as shown in Figure 3.3. Sampling at the start of the switching period introduces one sample delay and it will provide more time for the controller to calculate the new duty cycle. But the rotor position will be unknown for the one sample delay time, if the sampling is done at the start of the switching period. For the motor with low inertia, the dynamics of the motor will be high and any disturbances that happens between one sample delay of time cannot be controlled efficiently. So Volvo recommended to consider the sampling at the center of the switching period.



(a) 100 rpm and $T_eref = 300Nm$



(b) 1335 rpm and $T_eref = 100Nm$



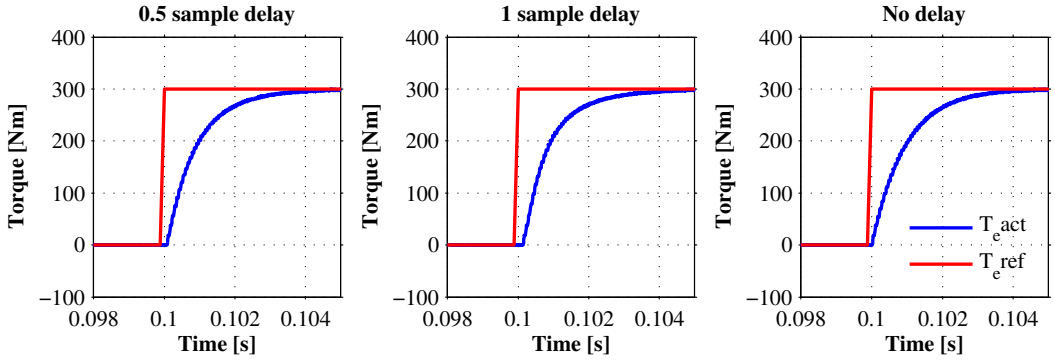
(c) 3000 rpm and $T_eref = 100Nm$

Figure 4.9: T_e step response with f_{sw}=8 kHz and without delay compensation for different speeds and PWM updation delays

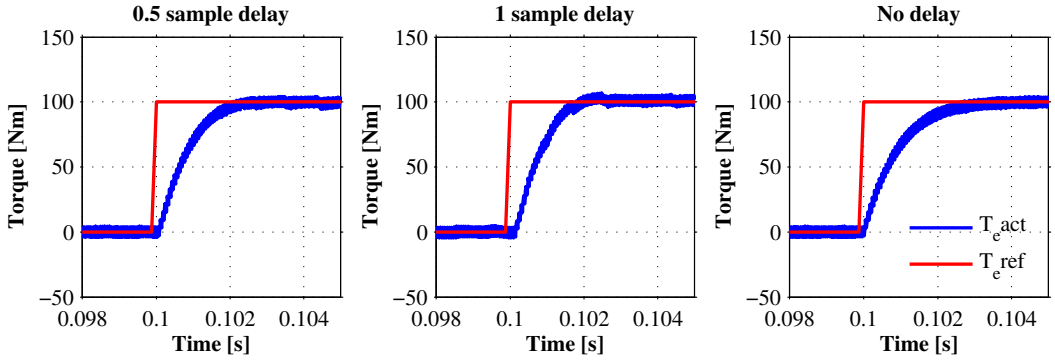
The impact of PWM updation delay on the torque control is simulated for different rotor speeds without delay compensation for the stator voltage calculation and the comparison of the results with a immediate duty cycle update are shown in Figure 4.9 and Figure 4.10. In the figures, 'No delay' is the ideal case in which the PWM duty cycle is updated immediately after the sampling. '1 sample delay' and '0.5 sample delay' represent the cases with one sample and half sample delay between the sampling and the PWM duty cycle update time respectively. Figure 4.9 shows the variation of the ripple content in the torque response and Figure 4.10 shows the rise time of the torque response for different speed and torque reference.

The results show that when the system is operating at a constant switching frequency, for the lower rotor speed the impact of update delay is negligible compared to the higher rotor speed. As discussed in Section 4.2.2, at higher speed the torque response will be poor when the moment of inertia of the motor is low and the f_{sw}/f_{elec} ratio is less. Together with that, at higher speed

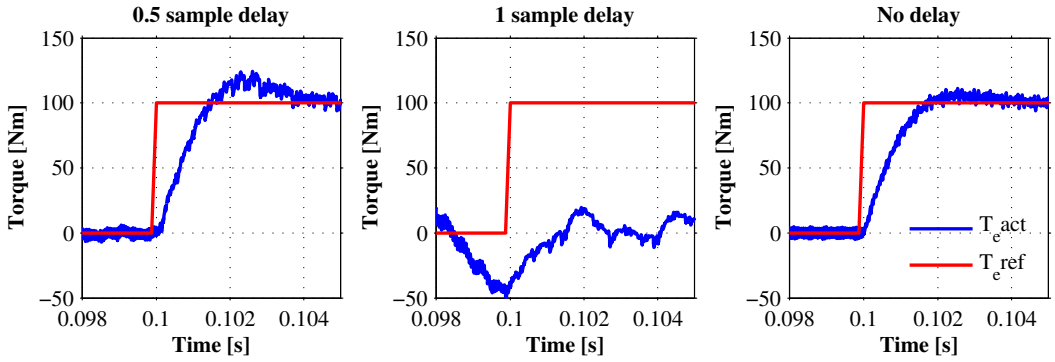
the rotor position changes at a higher rate and if the delay compensation for the stator voltage calculation is not available then the calculated stator voltage will be deviated from the required stator voltage as described in Chapter 3.5.3. This causes the poor torque response at the higher rotor speed.



(a) 100 rpm and $T_eref = 300Nm$



(b) 1335 rpm and $T_eref = 100Nm$

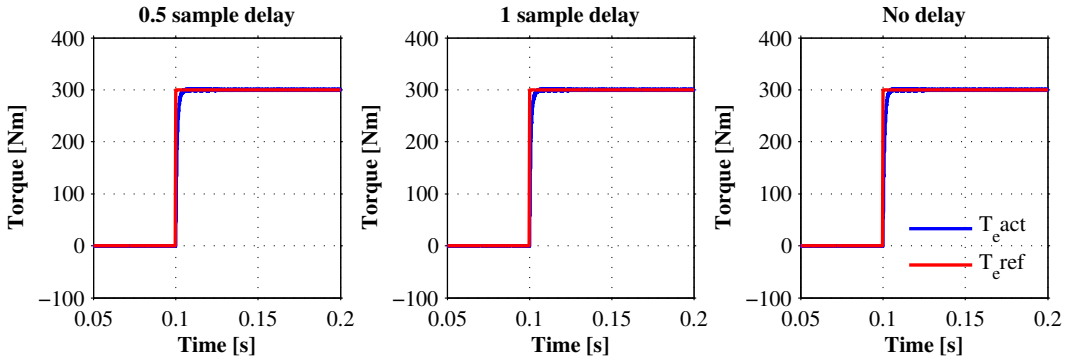


(c) 3000 rpm and $T_eref = 100Nm$

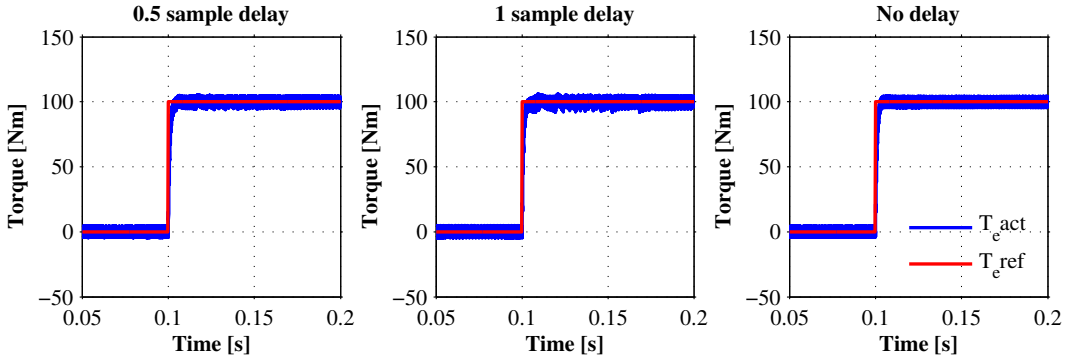
Figure 4.10: Rise time for T_e step response with f_{sw}=8 kHz and without delay compensation for different speeds and PWM updation delays

When the delay compensation is introduced, the torque response is comparatively improved as shown in Figures 4.11(c) and 4.12(c). For the case of 0.5 sample delay $D = 0.5$ in (3.6), for the one sample delay $D = 1$ and for the no delay case $D = 0$. At low speed the torque response with and without delay compensation gives almost the same response as shown in Figures 4.9(a), 4.10(a), 4.11(a) and 4.12(a). When the speed is low, the rotor position do not changed so much before the PWM duty cycle gets updated, so the effects is negligible in this case. The delay compensation has

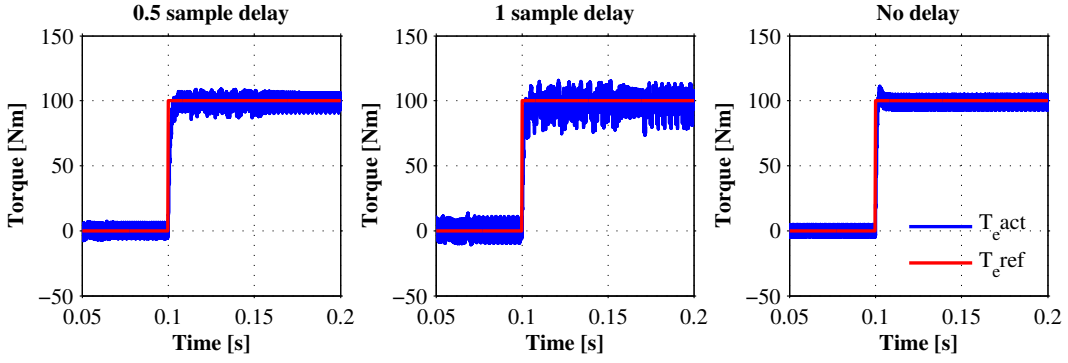
improved the torque response a little at the rated speed of 1335 rpm which could be noticed at the time 0.101 s to 0.102 s in Figure 4.10(b) and Figure 4.12(b) and at the time 0.11 s to 0.13s in Figures 4.9(b) and 4.11(b).



(a) 100 rpm and $T_eref = 300Nm$



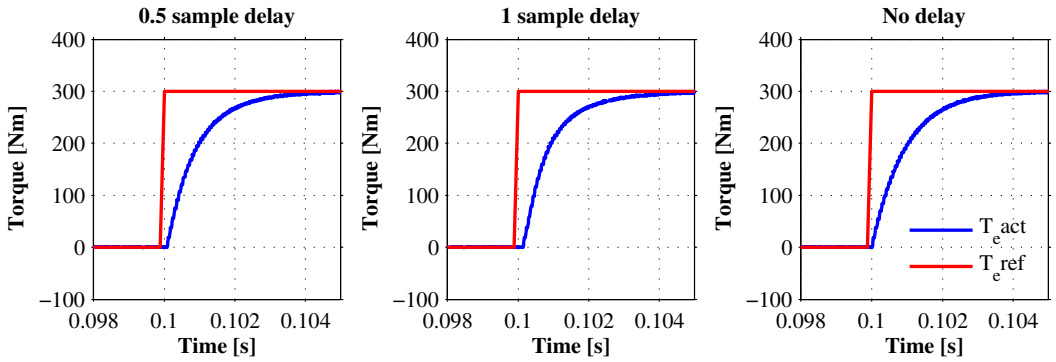
(b) 1335 rpm and $T_eref = 100Nm$



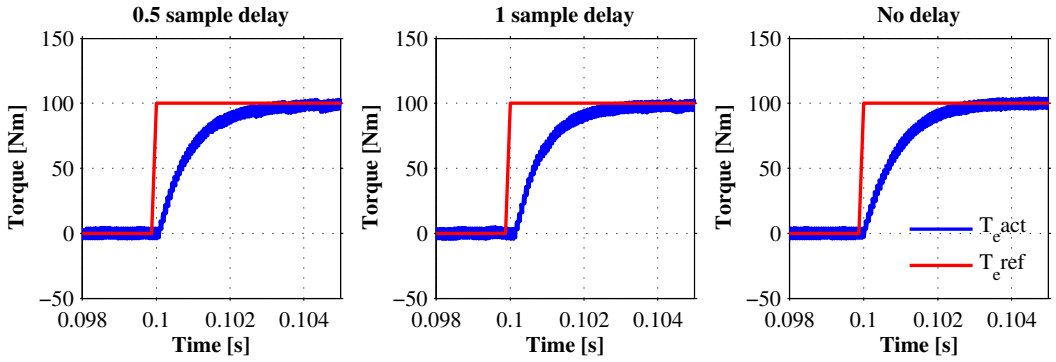
(c) 3000 rpm and $T_eref = 100Nm$

Figure 4.11: T_e step response with f_{sw}=8 kHz and with delay compensation for different speeds and PWM updation delays

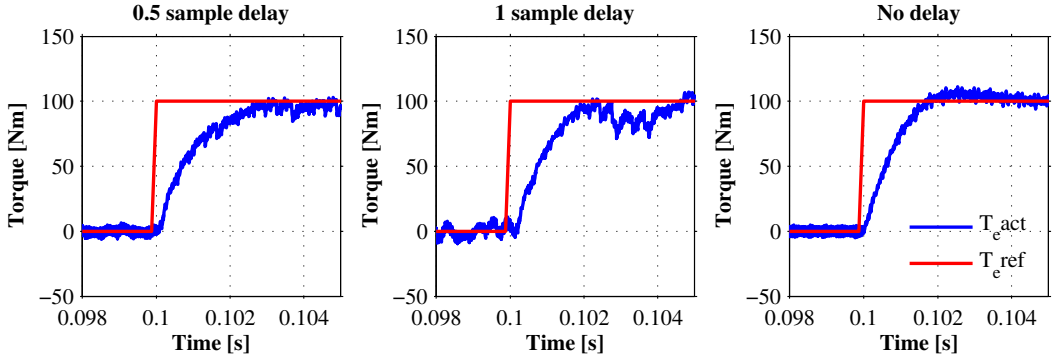
In all the cases, the torque response for one sample delay is worse than the half sample delay. For the case 'No delay at 3000 rpm during both with and without delay compensation an overshoot can be noted in Figures 4.9(c) and 4.11(c) at 0.1 s. This is because of the bandwidth selected for the control. The bandwidth can be increased to remove the overshoot at higher speed, but the effect with respect to with and without delay compensation will be same. As the main aim is to discuss only on the impact of PWM updation delay, more analysis by varying different bandwidth has not been done in this thesis.



(a) 100 rpm and $T_eref = 300Nm$



(b) 1335 rpm and $T_eref = 100Nm$



(c) 3000 rpm and $T_eref = 100Nm$

Figure 4.12: Rise time for T_e step response with f_{sw}=8 kHz and with delay compensation for different speed and PWM updation delay

4.2.4 Impact of ADC resolution

The resolution of the ADC for the current feedback will have an effect on the current controller. The maximum peak current of the VSC (I_{srated}) is 400 A and the nominal operating torque of the motor under consideration is 300 Nm, which corresponds to the stator q current of 240 A. In the simulation, the full scale resolution of the ADC converter is set to I_{srated} (400 A). As mentioned earlier the d current is always kept zero and the simulation has been carried out with the q current equals to 10 % of the I_{srated} ($I_q = 40A$) and with the q current corresponds to the nominal operating torque ($I_q = 240A$). Table 4.7 shows the least measurable current by the ADC for different ADC resolutions.

Table 4.7: The least measurable current by the ADC for different ADC resolutions

ADC Resolution	**Least measurable current (Resolution in [A])**
6 bit	6.25
8 bit	1.5625
10 bit	0.390625
12 bit	0.09765625
16 bit	0.006103515625

Table 4.8: i_q peak to peak ripple measured after the step (0.1 s) for different ADC resolutions in [A] at 1335 rpm, f_{sw}=8 kHz and U_{dc}=600 V

ADC Resolution	**6 bit**	**8 bit**	**10 bit**	**12 bit**	**16 bit**
$T_e$ref=50 Nm, $I_q$ref=40 A	12.5383	8.95	7.99	7.81	7.81
$T_e$ref=200 Nm , $I_q$ref=162 A	14.3	11.8	10.7	10.6	10.59
$T_e$ref=250 Nm , $I_q$ref=202 A	16.1	12.2	12.1	12.1	12.1
$T_e$ref=250 Nm , $I_q$ref=222 A	18	13.4	12.8	12.9	12.9
$T_e$ref=300 Nm , $I_q$ref=240 A	16.47	13.68	13.86	13.81	13.75

Table 4.8 and Figures 4.13 and 4.14 show that the ripple content in the q current is almost same for all the ADC resolution except for the 6 bit and 8 bit operation. The ripples in the current are due to the switching and also due to the least measurable current by the ADC. As the switching frequency is same, the ripple due to the switching will also be the same for all the ADC resolution. But when the resolution is decreased the least measurable current increases, it creates the difference in the error between the reference current and the feedback current for all the ADC resolution. This difference in error causes the additional ripple in the current when the ADC resolution is modified. When the resolution is 10 bit or more, the least measurable current is in mA so the difference in the ripple are unnoticeable compared to the lower resolutions. So to have the current control with less ripple its better to have at least 10 bit resolution for the investigated system.

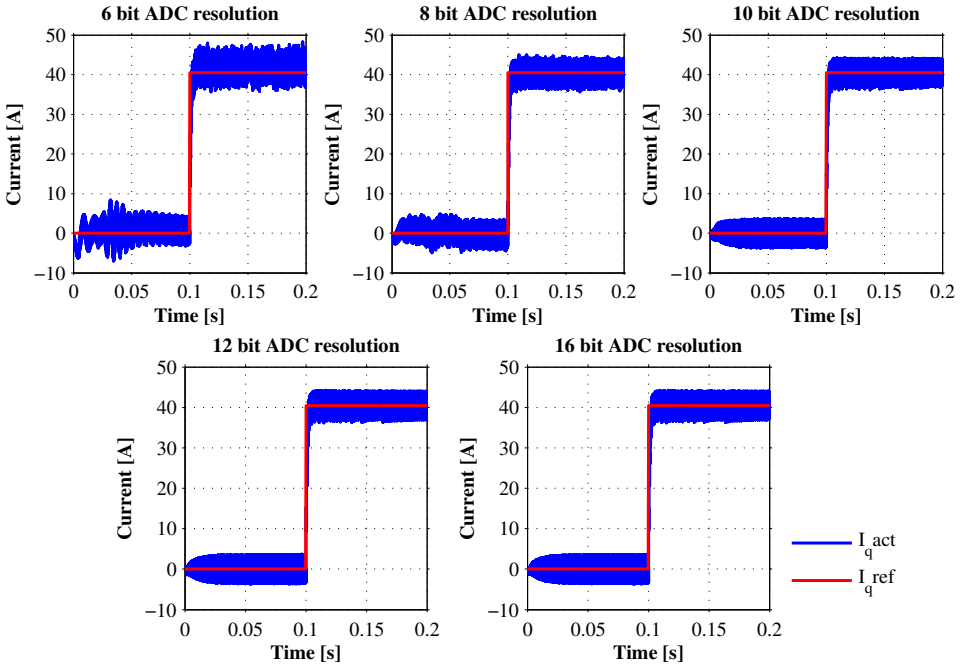


Figure 4.13: I_q step response with 1335 rpm and $T_eref = 50Nm$ with f_{sw}=8 kHz for different ADC resolutions

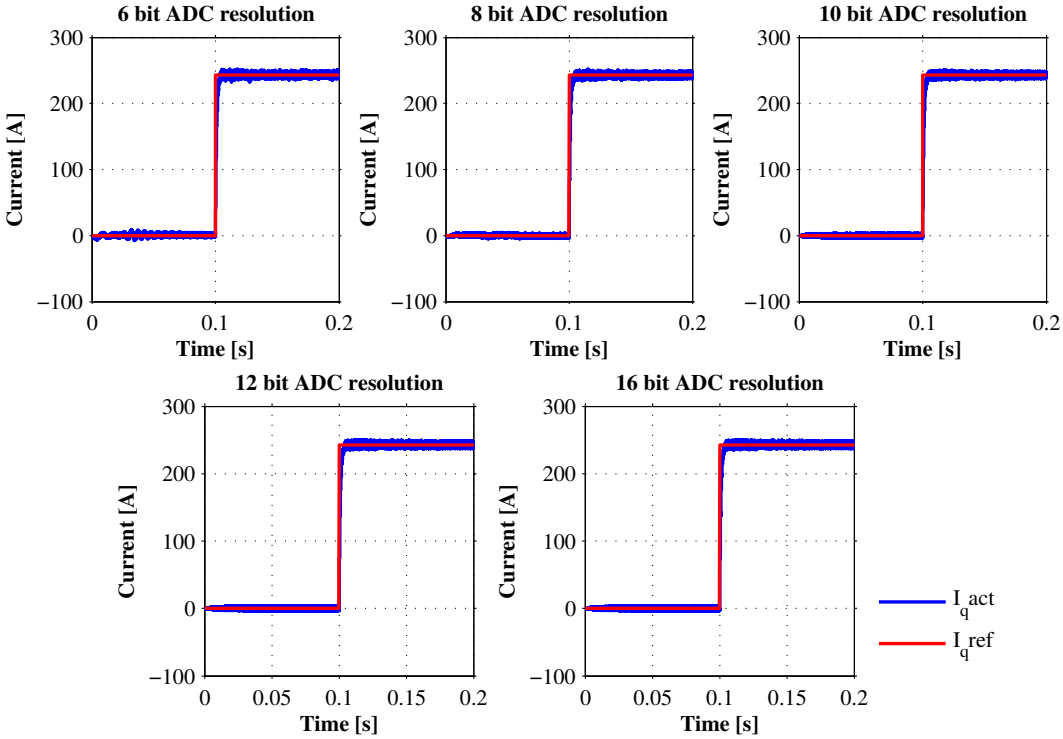


Figure 4.14: I_q step response with 1335 rpm and $T_eref = 300Nm$ with f_{sw}=8 kHz for different ADC resolutions

Chapter 5

Selection of micro-controller for evaluation and the evaluation methods

5.1 Required peripheral specification

Based on the simulation done and other inputs from Volvo the minimum required peripheral specification for the micro-controller should be:

1. Volvo aims at increasing the switching frequency upto 20 kHz. This requires the PWM frequency (f_{PWM}) to also be 20 kHz. Based on the simulation results in Chapter 4.2.1 the minimum PWM resolution should be 10 bit. So as per (3.1), the oscillator frequency (f_{OSC}) for the PWM should be minimum 20.5 MHz.

2. To have a good performance of the current controller, the minimum resolution of the ADC converter should be 10 bit, as discussed in Chapter 4.2.4. As mentioned in Chapter 3.5.1 atleast two of the phases of the stator current has to be measured for the current control. If both the phases of the stator currents has not been sampled simultaneously, it will create an error in the current measurement. So the micro-controller should have minimum two sample and hold circuit that works simultaneously. The ADC start of conversion interrupt should be generated at the center of the PWM period as discussed in Chapter 3.5.1, so the micro-controller should have the option to generate it.

3. The simulation results in Chapter 4.2.2 shows that if the f_{sw}/f_{elec} goes below 40, there is more ripple in the torque and when it goes near 20, the ripple is too high and the control becomes very difficult. For example if the maximum fundamental frequency (f_{elec}) of the motor is 400 Hz, the switching frequency should be atleast 16 kHz for the better control. If the ratio f_{sw}/f_{elec} is below 40 the switching frequency need to be varied based on the special control technique like synchronous switching whenever the system needs to run for higher speed. This requirement needs a shadow register arrangement in the digital controller to update the PWM frequency in the middle of control loop. This feature will also be used to reduce the switching loss and electromagnetic interference [54].

Other than the above mentioned specifications, properties described in Chapter 1.3 will also be considered for the selection of micro-controllers.

5.2 Justification of selected micro-controllers

The selection criteria for the micro-controller has been discussed in Chapter 1.3. Many of the micro-controllers in today‘s electronic market will have the required clock frequency, ADC and PWM resolutions. But the three selection criteria listed below are varying between manufactures:

- Possibility of achieving ASIL-D as per ISO 26262.
- Special hardware or Co-processors to handle the time critical tasks and to handle tasks which requires to utilise more of CPU capacity.
- Possibility of having ARC CORE based AUTOSAR support.

The micro-controller selected for further evaluation are shown in Tables 5.1 and 5.2. Table 5.1 shows the important characteristics of the selected micro-controllers and Table 5.2 shows the availability of the development environment and the debugging tools. The only micro-controller that satisfies most of the criteria is Texas Instruments' TMS570LS12x [27]. As per the data sheet it has the lock-step architecture and in-built memory test unit which helps it to achieve the ASIL-D. It also has a high end timer unit (HET) to handle the timer based functions like pulse capturing independent of the CPU. Though the HET unit is not so useful in motor control, it may reduce the CPU load for handling other functions [27].

STM's SPC56EL70L5 [23] and Freescale's MPC5643L [26] have many features that helps to achieve ASIL-D, but the AUTOSAR support is not available from ARC CORE. Also both the controllers are having similar characteristics and both do not have any special hardware that is specific for motor control like co-processor for the time critical operation etc. SPC56EL70L5 have very few motor control specific documents, as it is very new in the market. MPC5643L which is almost similar to SPC56EL70L5, has very good application specific documents but price of the evaluation boards are high as noticed in Table 5.2. Also the evaluation kit for SPC 56EL70L5 is available with all necessary software compared to the MPC5643L, which makes it to be preferred over the MPC5643L.

Toshiba's TMPM374FWUG [24] micro-controller has a special hardware that is specifically designed to take care of the motor control. But it does not have CAN or AUTOSAR support and it has less possiblity to achieve ASIL-D. Also it is primarily used for home appliances. Though TMPM354F10TAFG [29] is an unreleased product, it has all features of TMPM374FWUG together with CAN and possibility to achieve ASIL-D. Also it is designed especially for automotive applications. Evaluating TMPM374FWUG would be helpful for deciding on the usability of the higher end product TMPM354F10TAFG, when it is released on the market.

For Texas Instruments' Delfino TMS320F28377 [31] and Piccolo TMS320F28069M [32], there is no support for AUTOSAR based on ARC CORE and it is also difficult to make them in compliant with ISO 26262 compared to TMS570LS12x, SPC 56EL70L5 and MPC5643L as it does not have lock-step architecture and in-buit memory test unit. But both the micro-controllers have control law accelerator (CLA) which is an independent 32 bit floating point math accelerator. The CLA helps in reduction of the sample to output delay and to provide improved support for multiple control loops. TMS320F28377 has dual core processor, built in self test (BIST), error correction code (ECC) on flash, ECC on RAM and facility to detect missing clock [31]. These properties helps in achieving the ASIL-D, so TMS320F28377 is preferred compared to TMS320F28069M.

Infineon XMC4400 is not considered for the evaluation purpose though it is having some better properties than TMPM374FWUG. Because Infineon XMC4400 doesn't have any special properties compared to the other micro-controllers that makes it interesting for evaluation of motor control performance [33]. But the upcoming AURIX series Infineon is having the possibility to achieve ASIL-D with the help of its Tri-core and other protection unit in the controller. It will be interesting to evaluate, once it is fully released in the market.

Based on the above discussion, the below micro-controllers would be interesting to evaluate:

1. Texas Instruments' Hercules TMS570LS12x
2. Texas Instruments' Delfino TMS320F28377
3. Toshiba's TMPM374FWUG
4. STM's SPC 56EL70L5

Considering the time available for the thesis, out of the four micro-controller selected only the first two micro-controllers TMS570LS1227 and TMS320F28377D has been chosen for evaluation in this thesis.

Table 5.1: Comparison of Micro-controllers for PMSM motor control

	Possibility of achieving ASIL D	**Support for AUTOSAR**	**ADC**	**PWM**	Co- Processor / Special Hardware for Motor control
Hercules TMS570LS12x [27]	Yes, with the help of the lock-step architecture as per the data-sheet.	Full support from ARC CORE	Conversion time 600nS@30MHz	enhanced PWM with minimal CPU overhead is available	High end timer for time critical task. Operates independent of CPU
SPC 56EL70L5 [23]	Yes, with the help of the lock-step architecture as per the data-sheet.	Full support from VECTOR	Conversion time of 1108nS @60MHz	Cross Triggering unit to synchronise PWM and ADC conversion	none
MPC5643L [26]	Yes, with the help of the lock-step architecture as per the data-sheet.	Full support from VECTOR	Conversion time of 983nS @60MHz	Cross Triggering unit to synchronise PWM and ADC conversion	none
TMPM374FWUG [24]	Difficult, as it doesn‘t have lock-step architecture, built in self test (BIST) etc.	AUTOSAR basic software for OS is available from VECTOR	Conversion time of 2 micro second @40MHz	Dedicated PWM channel for motor control	Hardware implemented for most of the calculation in motor control via vector engine and programmable motor driver
TMPM354F10-TAFG [29] (under development)	Yes, with the help of tightly coupled fault supervisor.	AUTOSAR basic software for OS is available from VECTOR may support this also as it is Cortex M3 processor	No information	Dedicated PWM channel for motor control	Hardware implemented for most of the calculation in motor control via vector engine and programmable motor driver. Inbuilt hardware for resolver to digital conversion
Delfino TMS320F28377 [31]	Compared to piccolo it has more features like Dual core processor, ECC on Flash, ECC on RAM, Missing clock detection and BIST which helps to achieve ASIL D.	MCAL driver for CAN communication is available with VECTOR	ADC conversion time minimum 286ns. Upto 3.5 MSPS. Four simultaneous sample and hold.	High resolution PWM module is available	It has control law accelerator (CLA) an independent 32bit floating point math accelerator. The CLA helps in reduction of the sample to output delay and to provide improved support for multiple control loops.
Piccolo TMS320F28069M [32]	Difficult compared to Delfino as it doen‘t have BIST, ECC on RAM, lock-step architecure etc.	MCAL driver for CAN communication is available with VECTOR	ADC conversion time minimum 289ns. Upto 3.46 MSPS. Simultaneous dual sample and hold	High resolution PWM module is available.	It has control law accelerator (CLA) an independent 32bit floating point math accelerator. The CLA helps in reduction of the sample to output delay and to provide improved support for multiple control loops.

Table 5.2: Microcontroller software development environment and debugger [4] [5] [6] [7] [8] [9] [10]

	Estimated product release date	**Integrated development environment (IDE)**	**Compiler**	**Debugger**	**Evaluation Board**
Hercules TMS570LS12x	September 2012 as per press release.	CCS(Free with Evaluation kit)	Code composer studio (CCS)	JTAG interface kit available with evauation kit. Also lauter batch TRACE32 PowerDebug will support this.	1. Control Board - TMDX570LS12CNCD - Not comes with CCS -USD 149 2. Evaluation Board - DRV8301-LS12-KIT - with power stage, motor, debugger, CCS- USD 599
SPC56EL70L5	Datasheet first release on Nov 2012. On Sep 2013, major changes have been updated in datasheet.	SPC5Studio (Free)	GNU compiler collection (GCC)	Many options are available with lauterbatch	Control Board-SPC56EL70L5DISP -with JTAG interface - USD 121
MPC5643L	There is application note dated march 2011.	Code Warrior (Free for <128KB) and winIDEA(Free)	GCC	Many options are available with lauterbatch. Also available with P&E. Freemaster software is free to download for real time debug	1. MTRCCBB5643L - 389 USD. 2. MTRCKTSPS5643L- with motor and power stage - USD 2410.3.PE micro Development kit (USD 1000)(it is only debugger and development softwares . Control board not included in package)
TMPM374FWUG	First data sheet release date August 2011.	Keil MDK ARM and IAR. Keil Free version support upto 32KB	Not described in document. As its ARM core, it may be possible with GCC	Many options are available with lauterbatch. Segger J-link Jtag comes with Evaluation kit	BMSKTOPASM374(TEE) - with JTAG debugger - ŨSD 200
TMPM354(under development)	Yet to release. It is an automotive version of TMPM374FWUG				
Delfino TMS320F28377	Dec 11 2013, as per press release	CCS(Free with Evaluation kit)	CCS	JTAG interface kit available with evauation kit	TMDXDOCK28377D -With development environment CCS and debugger - USD 219
Piccolo TMS320F28069M	Jan11 ,2011, as per press release	CCS(Free with Evaluation kit)	CCS	JTAG interface kit available with evauation kit	DRV8312-69M-KIT - with motor, power stage, development environment CCS & Debugger - USD 299

5.3 dSpace real time environment

Testing the new micro-controller in an actual drive system could potentially have a risk of faulty operation of the drive system, leading to damage of the hardware and loss of time and money. To avoid this, a real time motor model based on (2.3) and (2.4) has been developed by Volvo in MATLAB simulink. The developed model is downloaded to the real time simulation environment dSpace and the dSpace system acts as the real hardware of the drive system (VSC, PMSM, incremental encoder and load). The dSpace is a real time simulation environment, which can be used as a tool to simulate engines in automobiles, electrical motors, real time control system etc. [11]. Volvo uses the dSpace AC motor control solution DS5202 FPGA base board for their real time simulation of electrical motors. Figure 5.1 shows the simple overview of the dSpace system.

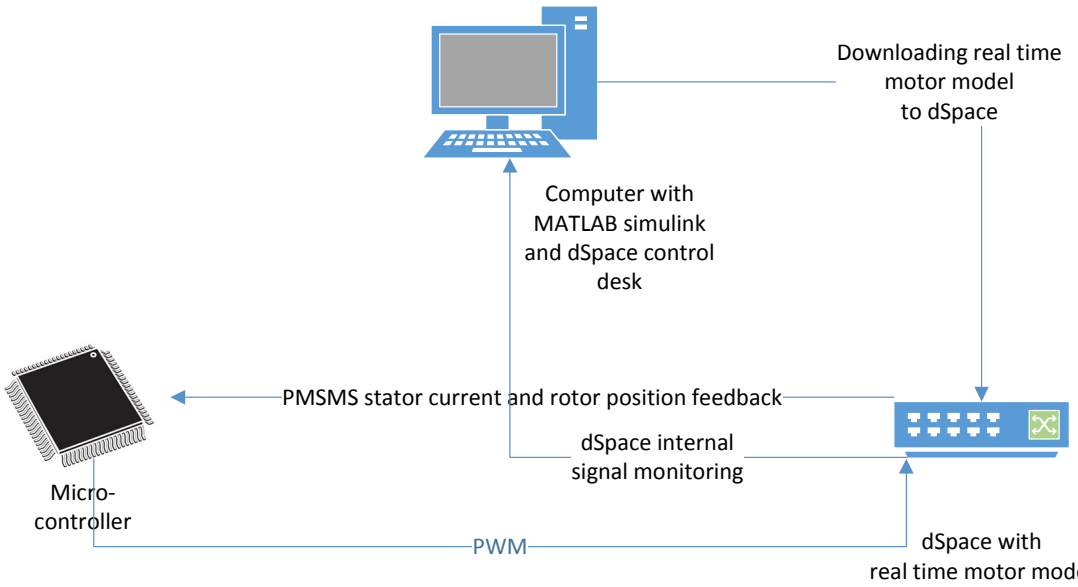


Figure 5.1: Overview of the dSpace system together with the micro-controller in the hardware in the loop simulation environment.

The micro-controller together with the dSpace system forms the hardware in the loop simulation environment used to evaluate the micro-controller for motor control. When the dSpace is running, the value of the PMSM stator current, stator voltages, PWM signals, rotor position etc. can be monitored using dSpace control desk software, installed on the same computer configured with MATLAB simulink for real time model development. The dSpace system will receive the PWM gate signal as a input from the micro-controller under test and the duty cycle of the PWM signals is measured. From the duty cycles the stator voltage requested by the digital controller is calculated and it is given as input to the real time PMSM model. The dSpace system outputs the stator current feedback and position sensor feedback to the micro-controller. The real time PMSM model is configured as a function call subsystem, which is executed based on the interrupt generated at the center of the PWM period.

5.4 Micro-controller architecture evaluation method

The methods used to evaluate the parameter listed in Chapter 1.3 is discussed in this section.

5.4.1 CPU utilization

The CPU utilisation time for the main torque control loop can be calculated by measuring the execution time of the code corresponding to it. Below are the few methods to calculate the execution time for the torque control code [18] [16]:

- Measuring the time duration between toggling a digital output pin. In this method whenever the code starts executing a digital output is set and the same output is reset at the end of the code. A Oscilloscope could be used to measure the duration of the digital output value, which gives the execution time for the particular code. This type of approach is general and can be used for many controllers.

- A Hardware counter in the real time interrupt module can be used to count the clock cycle required to execute the code.

- If availabe a PMU (performance monitoring unit) integrated with CPU can be used to count the clock cycles. The PMU will have a programmable counter, which could be configured to start and stop as per the user requirement. If the counter is configured to start at the beginning of the torque control loop and stop at the end of the control loop, CPU utilization can be estimated.

Some type of application codes may not have constant execution time, due to the presence of interrupts, so the execution time needs to be measured for several times to get the worst case value. The CPU utilization for a switching frequency (f_{sw}) in percentage is given by

$$CPU\ utilization = 100 * ISR\ execution\ time * f_{sw} \tag{5.1}$$

5.4.2 ADC module

The micro-controller ADC module has to be evaluated for the ADC sampling instant, ADC conversion time, ADC resolution, quality of the ADC measurement and the configurability of the registers corresponding to the ADC. The ADC resolution can be measured by injecting a constant DC voltages to the analog input and measure the values inside the digital controller. The quality of the ADC measurement can be evaluated by checking the presence of noise in the measured ADC values. The noise in the ADC signals can be reduced if the ADC module has differential ended input channels [14].

To verify whether the micro-controller is sampling at the exact instant that the controller is configured to is very important. Because the stator current feedback from the PMSM should be sampled exactly at the centre of the PWM period in-order to measure the average current accurately. If pin toggling is used to detect the ADC start of sampling, once the SOC interrupt has been occurred, a set of code has to be executed to generate the digital output. So there will be a delay to execute the code and getting the digital output in the oscilloscope.

The simplest method is to provide a constant dc voltage to the ADC input and measure the voltage on the analog input pin of the micro-controller using a oscilloscope. Whenever the ADC is started sampling, there will be a small dip in the voltage due to the presence of the sampling capacitor in the ADC module as illustrated in Figure 5.2. Figure 5.2 shows only the approximate shape of the voltage curve during the ADC sampling window time, the actual curve may vary depends on the value of the sampling capacitor and the ADC input impedance. The time at which the voltage dip starts is the start of the sampling. The voltage should become stable without any oscillation before the center of the PWM period (T_2). The ADC sampling window time should be set to equal to the time between the center of the PWM period and the start of the sampling, so that the ADC holds the voltage at the center of the PWM period during the ADC conversion period. At least two phases of the stator current should be sampled simultaneously to have a better control over current as discussed in Chapter 3.5.1. This also can be verified using the same approach as measuring the sampling instant.

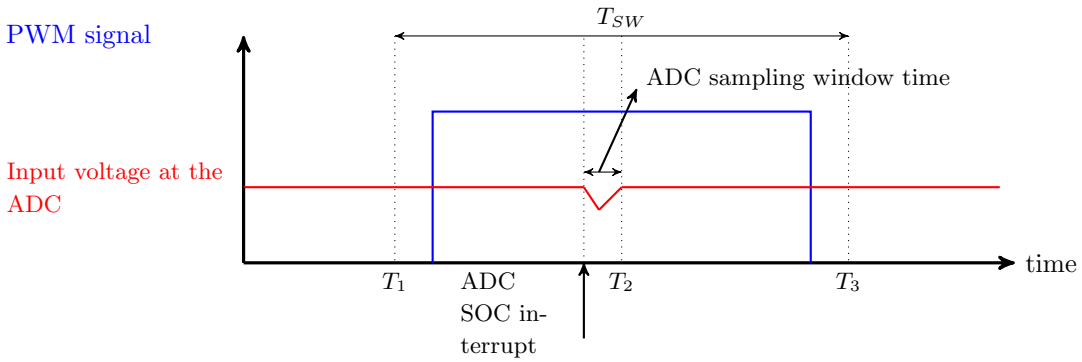


Figure 5.2: Approximate illustration of the effect on the voltage at the input of the ADC module, due to the sampling capacitor when the sampling started at the ADC SOC interrupt.

The ADC sample and conversion time can be measured similar to the execution time calculation discussed in Chapter 5.4.1 by monitoring the time difference between ADC start of conversion interrupt from the PWM module and ADC end of conversion interrupt from the ADC module. The ADC module should have the registers to configure the below mentioned features:

- As described above the ADC module should have registers and hardware features to implement differential ended input channel.
- The ADC module should have the hardware facility to detect an error in the ADC channel like the open and the short circuit of its channel terminal and the registers to indicate the same.
- As discused in Chapter 3.5.1 atleast two ADC channel is required and both should operate simultaneously. So the ADC module registers should have the facility to initiate the ADC SOC interrupt simultaneously for both the channel.
- The ADC module should have the registers to generate the ADC EOC interrupt a few CPU cycles earlier that the actual ADC conversion ends, to initiate the ISR earlier. This facility will make sure that the ISR to start execute exactly after the conversion ends.

5.4.3 PWM module

The micro-controller PWM module has to be evaluated for the PWM resolution, time required by the PWM gate signals to get blocked when the fault occurs and the configurability of the registers corresponding to the PWM gate signal generation. The PWM resolution can be measured by defining a fixed duty cycle and verifying the correctness of the ON/OFF period of the switching pulses using a oscilloscope. The experiment can be repeated for different duty cycles to find the worst case result. But the PWM resolution can be verified directly from the datasheets and the actual resolution will be almost equal to the datasheet values.

The time for the controller to set all the PWM signals to low state or high impedance state, when a external fault occurs is one of the important parameter to be verified. This can be done by connecting a digital input of the micro-controller to a external source of signal and configure the digital input to trigger the fault indication in the controller. By monitoring the PWM pulses and the configured digital input using a oscilloscope the fault response time can be measured. The PWM module should have the registers to configure the below mentioned features:

- A register to store the PWM duty cyle calculated at the end of the ISR and load the same to the duty cycle register at the start of the next PWM period. If this facility is not available then the CPU has to wait until the next PWM period to store the calculated PWM duty cycle and the CPU will be idle for longer time. So the CPU utilization will get increase.
- A register to configure the dead time for the each PWM channels. The dead time of the PWM signal is important for the VSC to avoid short circuit fault during its operation [55].

- A register to block the PWM signal when there is a fault detected in the system.
- As described in Section 5.4.2, the ADC should start sample before the center of the PWM period, to compensate for the effect due to sampling capacitor. So the PWM module should have a register to generate the ADC start of conversion interrupt before the center of the PWM period.

5.4.4 Encoder module

The encoder module has to be evaluated for the position measurement accuracy and configurability of the registers corresponding to the position measurement. The position measurement accuracy can be verified by keeping a constant speed in the motor and measuring the speed and angle variation inside the micro-controller. Constant speed in the motor can be simulated by implementing only the real time encoder model in the dSpace system and giving constant speed input to the encoder block in the model. The encoder output from the dSpace system can be measured using the micro-controller and the same could be converted to its equivalent position and speed measurement inside the micro-controller. The encode module should have the registers to configure the below mentioned features:

- The registers should be able to configured in such a way that the encoder counter value should get reset whenever the index signal is detected. This avoids the requirement of the rotor position alignment before the start of the motor.
- The register storing the encoder count should be accessible by the CPU when the ISR is getting executed, without halting the processor.

Chapter 6

Evaluation of Texas instrument TMS570LS1227 and TMS320F28377D

In this chapter, the hardware description and setup for the evaluation of the micro-controllers TMS570LS1227 and TMS320F28377D are explained. The experiments and the comparison of the results of the evaluation along with the simulation results are also discussed.

6.1 Hardware description and setup

6.1.1 Hardware description of the micro-controller and evaluation board

Table 6.1: **Hardware description of TMS570LS1227 and TMS320F28377D**

	TMS570LS1227	**TMS320F28377D**
Evaluation Board	• DRV8301LS12 EVM kit • The kit is included with the control card for TMS570LS1227 with limited access to pins , driver circuit to trigger the MOSFET based VSC and PMSM	• Experimenter kit TMDX-DOCK28377D. • This kit includes the control card for TMS320F28377D with access to all the pins of the micro-controller.
Processor core	• It is a ARM CORTEX-R4F, 32 bit RISC processor. • It has 180 MHz dual CPU running in lock step mode, which makes its suitable for safety critical application.	• It belongs to the Texas instrument's C28x series of C2000 family of micro-controller. • It has 200 MHz dual CPU.
ADC Module	It has two ADC modules, each can be configured single ended mode, 12 bit or 10 bit.	It has four ADC modules, each can be configured in differential mode 16 bit or 12 bit and single ended mode 12 bit .
PWM Module	High resolution PWM modules with dead band control is available.	
Encoder	A dedicated enhanced encoder unit is available to read to the PMSM rotor position.	

Continued on next page

Table 6.1 – continued from previous page

	TMS570LS1227	TMS320F28377D
CLA	Not available	• Each CPU is having a independent processing unit named Control law accelerator (CLA) to perfom the critical mathematical operations independent of the CPU. • It is operated at the same clock speed as the CPU. • The CLA can start executing its codes either based on software interrupts or interrupts from the ADC, PWM and encoder modules. • The CLA codes can be written using C language. • The CLA can access PWM, ADC and encoder module without help of CPU and it has 16 KB RAM.

A short description of the hardware details of the micro-controllers used for evaluation in this thesis in the motor control point of view is presented in Table 6.1 [20] [31] [27] [25]. Detailed description of the each modules will be discussed in corresponding sections.

6.1.2 Hardware connection between dSpace and TMS570LS1227

The kit DRV8301LS12 EVM includes a gate driver circuit to control the motor [20]. In this thesis the gate driver circuit is not required by the dSpace to trigger the inverter model. Therefore the driver circuit in the kit has been disabled using software configuration. The used interface between the dSpace system and the DRV8301LS12 EVM is shown in Figure 6.1 and Table 6.2.

In Table 6.2 PWM A, B and C corresponds to the switching signals for the switches S_A, S_B and S_C described in Figure 2.2. PWM A(PWM B/ PWM C) upper and lower signal is to make S_A (S_B/S_C) to position 1 and -1 respectively. Current A and B is the PMSM stator phase current i_{sa} and i_{sb} respectively. Encoder A and B are the quadrature encoder signals 90^o out of phase. Encoder index is the signal corresponds to completion of one mechanical rotation of rotor [28].

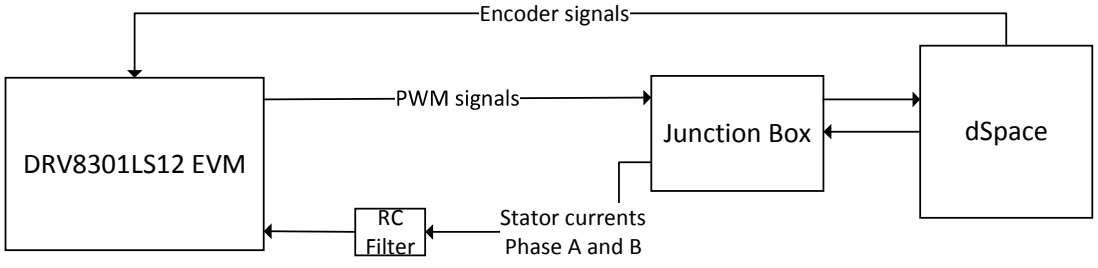


Figure 6.1: Interface between dSpace and DRV8301LS12 EVM

Table 6.2: DRV8301LS12 EVM and dSpace connection interface

Signal	dSpace	Junction Box	DRV8301LS12 EVM	Range
DRV8301LS12 EVM to dSpace				
PWM A upper	P4a:20	900B1:9	J5:25	0 or 2.5V
PWM A lower	P4a:21	900B1:10	J5:23	0 or 2.5V
PWM B upper	P4a:22	900B1:7	J5:28	0 or 2.5V
PWM B lower	P4a:23	900B1:8	J5:24	0 or 2.5V
PWM C upper	P4a:24	900B1:5	J5:26	0 or 2.5V
PWM C lower	P4a:25	900B1:6	J5:22	2.5V
GND	P4a:1, 2	900B1:20	J5:39	
GND	P4a:3, 4	900B1:16	J5:19	
GND	P4a:5, 6	900B1:18	J5:20	
GND	P2a:8	900B1:28	J5:40	
dSpace to DRV8301LS12 EVM				
Current A	P2a:41	900B1:32		0 to 3.3 V= -400 to 400 A
Current B	P2a:9	900B1:31		0 to 3.3 V= -400 to 400 A
Encoder A	P1:20		J4:1	0 or 5 V
Encoder B	P1:22		J4:2	0 or 5 V
Encoder Index	P1:24		J4:3	0 or 5 V
GND	P1:1		J4:5	

In order to reduce the high frequency noise in the current measurements, the Current A and Current B signals are connected to a low pass filter before connecting it to the analog input of DRV8301LS12. The low pass filter is having a cut off frequency of 100 kHz with a resistor of $R = 330\ \Omega$ and capacitor of $C = 4.7\ nF$. The low pass filter circuit is shown in Figure 6.2. The output of the filter has been connected to test points TP 25 and TP 24 on the DRV8301LS12 EVM evaluation board [22] [19]. The resistor R133 and R134 on the evaluation board has been removed to isolate the internal signals from the stator current inputs.

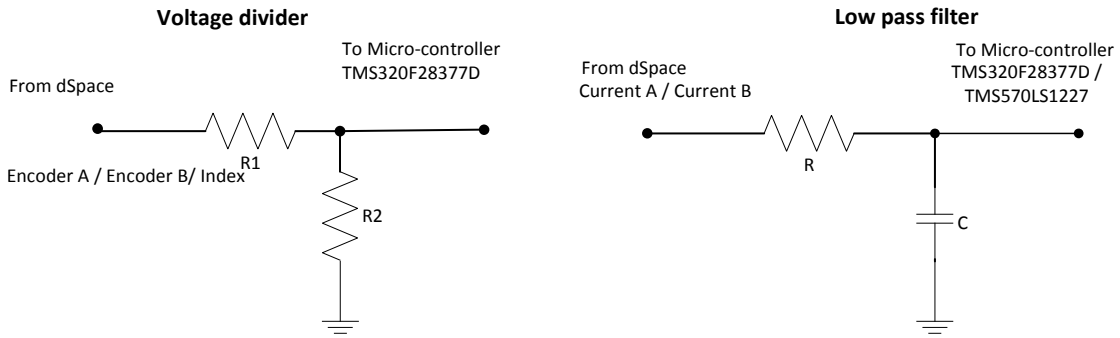


Figure 6.2: Low pass filter and voltage divider circuits. The low pass filter is used for both the micro-controllers but the voltage divider is used only for TMS320F28377D.

6.1.3 Hardware connection between dSpace and TMS320F28377D

The interface between the dSpace system and TMDXDOCK28377D is shown in Figure 6.3 and Table 6.3. The signal description in Table 6.3 is same as described in Section 6.1.2, except for that the signals are connected to different pins on the TMDXDOCK28377D evaluation board. The low pass filter used for the current measurement signals is same as the one used for TMS320F28377D.

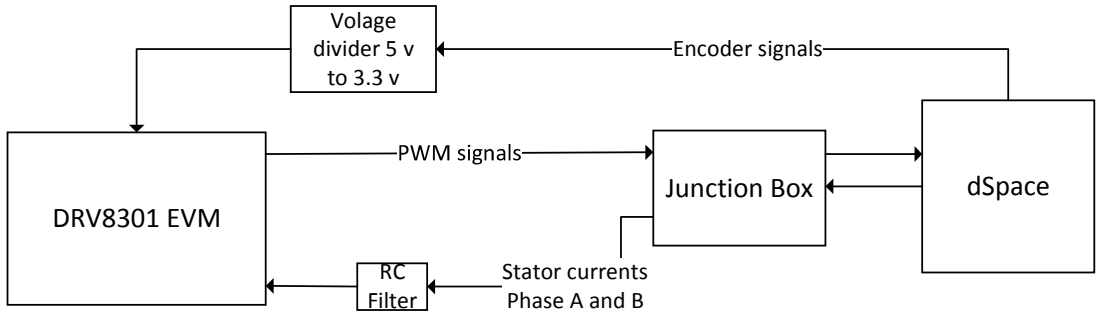


Figure 6.3: Interface between dSpace and TMDXDOCK28377D

Table 6.3: TMDXDOCK28377D and dSpace connection interface

Signal	dSpace	Junction Box	TMDXDOCK28377D	Range
TMDXDOCK28377D to dSpace				
PWM A upper	P4a:20	900B1:9	49	0 or 2.5V
PWM A lower	P4a:21	900B1:10	51	0 or 2.5V
PWM B upper	P4a:22	900B1:7	53	0 or 2.5V
PWM B lower	P4a:23	900B1:8	55	0 or 2.5V
PWM C upper	P4a:24	900B1:5	50	0 or 2.5V
PWM C lower	P4a:25	900B1:6	52	0 or 2.5V
GND	P4a:1, 2	900B1:20	GND	
GND	P4a:3, 4	900B1:16	GND	
GND	P4a:5, 6	900B1:18	GND	
GND	P2a:8	900B1:28	GND	
dSpace to TMDXDOCK28377D				
Current A	P2a:41	900B1:32		0 to 3.3 V= -400 to 400 A
Current B	P2a:9	900B1:31		0 to 3.3 V= -400 to 400 A
Encoder A	P1:20			0 or 5 V
Encoder B	P1:22			0 or 5 V
Encoder Index	P1:24			0 or 5 V
GND	P1:1		GND	

The voltage limit of the encoder signal pins on the TMDXDOCK28377D evalauation board is only 3.3 V, but the output from the dSpace system is 5 V, so a voltage divider circuit has been designed to reduce 5 V to 3.3 V for the encoder A, B and index signals. Figure 6.2 shows the voltage divider circuit with R1 = 22 kΩ and R2 = 39 kΩ. The Outputs of the voltage dividers for are connected to pins 68, 70 and 74 respectively on the TMDXDOCK28377D evaluation board [25].

6.1.4 Peripheral configuration of the evaluation board

As discussed in Chapter 5, the PWM gate signal frequency should be 20 kHz, the PWM resolution should be at least 10 bit and the PWM clock frequency should be at least 20.5 MHz. The existing dSpace system has a limitation with the maximum PWM signal frequency of 8 kHz. So the evaluation has been done with the PWM gate signal frequency of 8 kHz and the PWM signal clock frequency is arbitrarily chosen as 80 MHz. This gives the PWM gate signal resolution of approximately 13 bits as per (3.1), which is more than the required specification. The dead time for the PWM signal can be configured in multiples of 0.01 μ in both the micro-controllers. But it has been configured to zero to have a good comparison with the simulation. The required minimum ADC resolution is 10 bit as per Chapter 5, the maximum ADC resolution available in both the selected micro-controllers is 12 bit. So the ADC resolution of 12 bit is used for the evaluation purpose. For the TMS570LS1227 micro-controller, the ADC SOC interrupt is configured to generate at the

center of the PWM period and the ADC EOC interrupt is configured to generate at the end of the ADC conversion as described in Chapter 3.5.1. But for the TMS320F28377D micro-controller, the ADC EOC interrupt has been configured to be generated at one CPU cycle before the end of the ADC conversion as described in Chapter 5.4.2 and the ADC SOC is configured to generate at the center of the PWM period similar to the TMS570LS1227 micro-controller. The ADC EOC interrupt configuration is different in the TMS320F28377D micro-controller, as it has the additional facility in its hardware compared to the TMS570LS1227 micro-controller. The encoder module of both the micro-controllers has been configured in such a way that the encoder counter value will get reset on every index pulse from the encoder and the counter value can be read by the CPU any time during the ISR execution. Also both the micro controllers has been configured to perform the motor control as per the sequence described in Chapter 3.5.1.

Table 6.4: Peripheral configuration - TMS570LS1227 and TMS320F28377D

	TMS570LS1227	**TMS320F28377D**
CPU clock	80 MHz	
PWM clock	80 MHz	
PWM period	8 KHz	
PWM count mode	up down count mode	
Action on fault	All PWM signals to low	
ADC clock	26.67 MHz	20 MHz
ADC sample and hold window	6 ADC cycle	9 CPU cycle
ADC resolution	12 bit	
ADC SOC interrupt	Generated at the center of the PWM period	
ADC EOC interrupt	Generated at the end of ADC conversion and initiate ISR in CPU	Generated one CPU cycle before the end of ADC conversion and initiate ISR in CLA
ADC channel for i_{sa} and i_{sb}	Channel 1 of Group 1 ADC module 1 and 2	Channel 1 of ADC module 1 and 2
Quadrature encoder lines for one mechanical revolution	1000	

6.2 CPU utilization

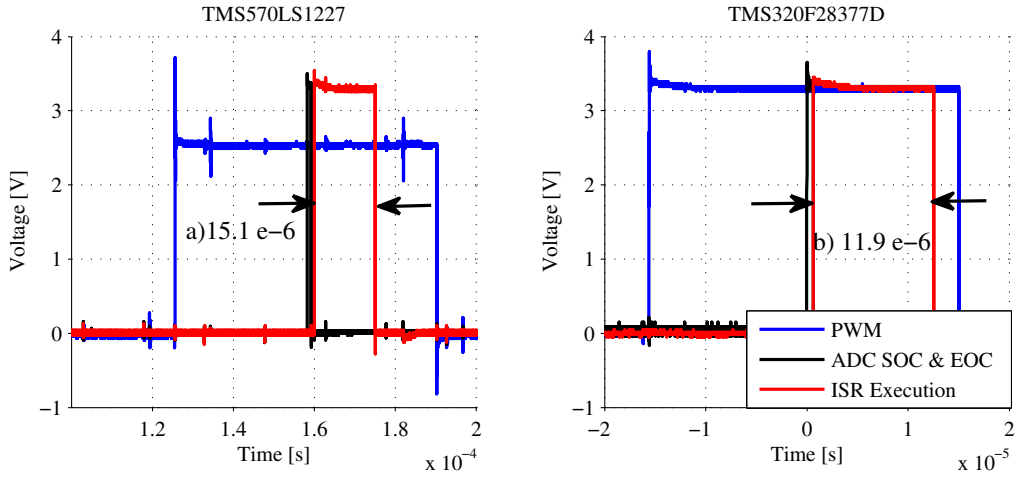


Figure 6.4: ISR Execution time - TMS570LS1227 and TMS320F28377D

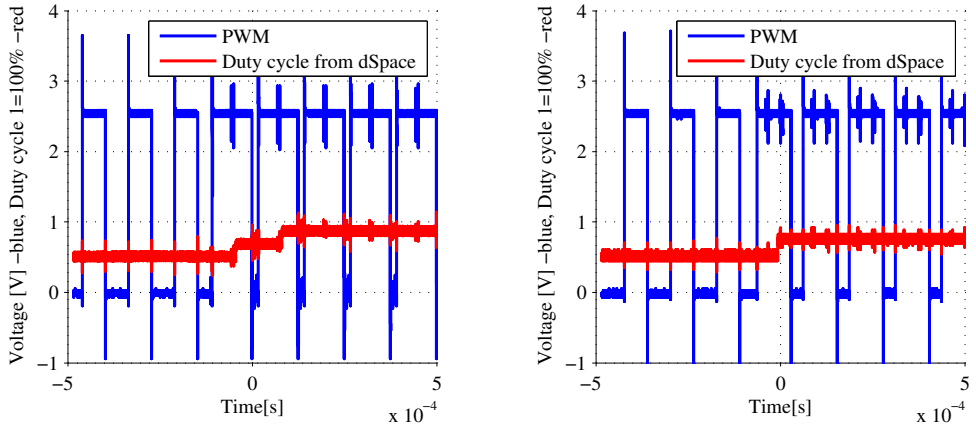
The PMSM current control algorithm is implemented as a ISR in the CPU of TMS570LS1227 and as a ISR in the CLA of TMS320F28377D. As the CLA has limited program memory of 4 kB in RAM the same algorithm but with different C code is implemented in both controllers. The C code for TMS570LS1227 has a lot of functions, and its mathematical libraries are also different, so it takes little more time to execute the ISR. The section a) and b) of Figure 6.4 shows that the ISR execution time for TMS570LS1227 and for TMS320F28377D are 15.1 μs and 11.9 μs respectively. TMS570LS1227 also has a real time interrupt module which can be used for measuring the ISR execution time and that gives 15 μs.

The CPU utlization for the ISR in TMS570LS1227 for a switching frequency of 8 kHz calculated based on (5.1) to 12.08%. The maximum switching frequency Volvo expects to operate the VSC at, is 20 kHz. The CPU utilization at 20 kHz will be 30.2%, but this can be further reduced if the CPU clock frequency is increased to its maximum of 180 MHz. In TMS320F28377D only the CLA is used for the ISR, leaving the CPU almost free to take care of other functional requirements. Due to this the CPU utilization is almost 0% and the CLA utlization is 23.8% at a switching frequency of 20 kHz and the CLA clock frequency of 80 MHz.

6.3 Delay in the dSpace system

As discussed in Chapter 5.3 the dSpace system receives the PWM gate signals as a input from the controller and it should be able to measure the duty cycle of the PWM signals. Depending on the way in which the PWM signal is sampled by the dSpace system, there will be a delay in measuring the actual duty cycle and it should be considered in-addition to the delay compensation for the voltage at the current controller output described in Chapter 3.5.3.

The PWM module in dSpace can be configured in normal sampled or over sampled mode. In the normal sample mode, dSpace measures the duty cycle of the PWM by sampling the PWM at its rising edge, falling edge and the center of the PWM period and calculating the time difference between them. In oversampled mode, it will take additional samples between two consecutive PWM center, based on its oversampling factor. In both modes, the PWM duty cycle is updated at the center of the PWM period [36].



(a) Normal sampled PWM in dSpace

(b) Over sampled PWM in dSpace

Figure 6.5: Delay in detecting the PWM duty cycle in dSpace. In (a) duty cylce changes from 0.5 to 0.8 at -0.05 ms and in (b) duty cycle changes from 0.5 to 0.7 at -0.05 ms

In normal sample mode during the first center of the PWM (T_c) after the actual duty cycle changes, the time difference between the previous falling edge and the rising edge is used for calculation of the duty cycle. As this time difference corresponds to the two PWM signal cycle, one with old duty cycle and the another with new duty cycle, the duty cycle measured by dSpace at T_c is the average of the old and new duty cycle. This gives the additional sample delay to detect

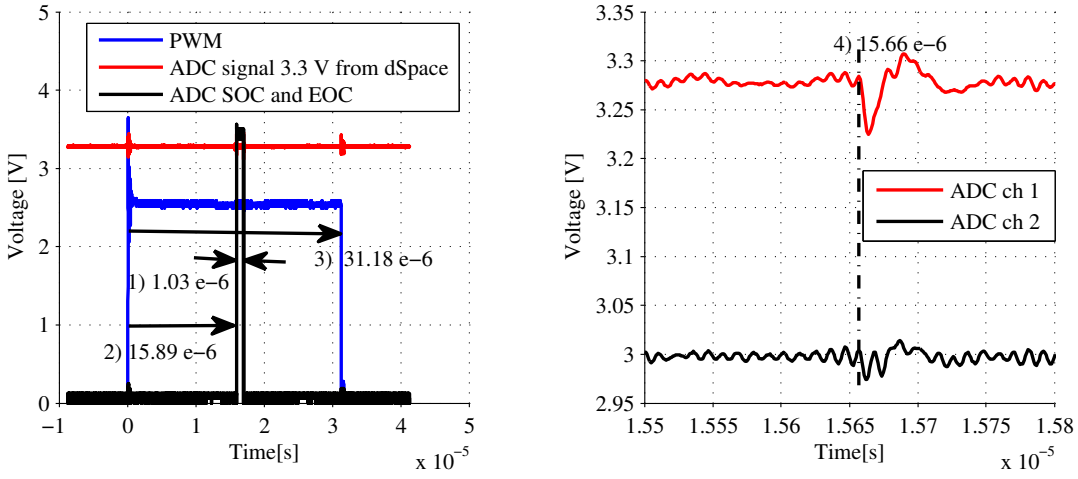
the actual duty cycle, as shown in Figure 6.5.

If a oversampling factor of two is set for the PWM module in dSpace, PWM is sampled twice between the centers of the two consecutive PWM period. Then the time between the rising edge and the sample before the PWM center is used for the duty cycle updation. This helps to detect the change in duty cycle faster compared to the normal sample mode, as shown in Figure 6.5. For higher rotor speed, its recommended to use oversampling mode [36].

6.4 ADC module

6.4.1 ADC sampling instant and conversion time

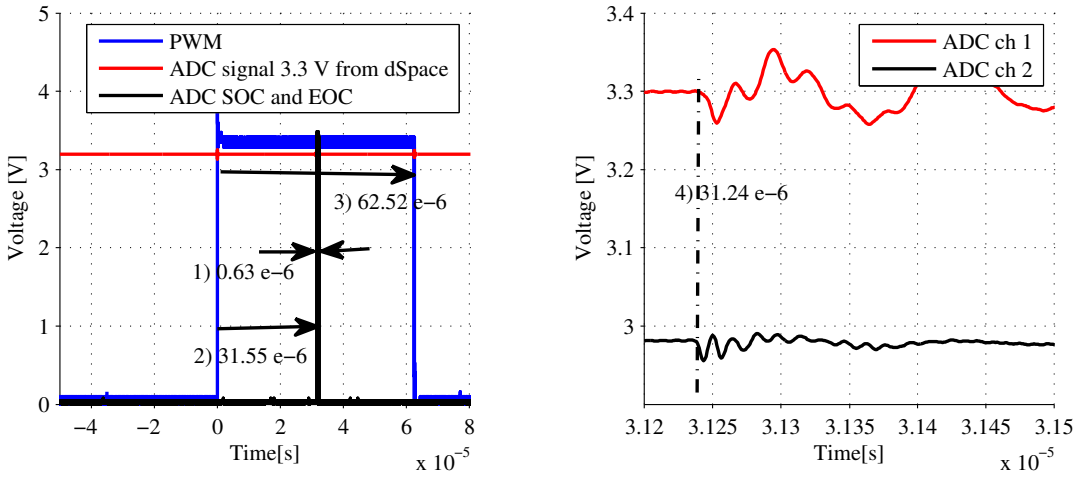
To verify the ADC sampling instant and conversion time, a constant voltage has been injected from dSpace to the ADC channel of the micro-controller. The variation in the input voltage due to sampling as described in Chapter 5.4.2, is monitored with a oscilloscope along with the PWM signal and a signal which is programmed to toggle for ADC SOC and EOC.



(a) Conversion time

(b) Start of the sample

Figure 6.6: ADC conversion time and sampling instant for TMS570LS1227



(a) Conversion time

(b) Start of the sample

Figure 6.7: ADC conversion time and sampling instant for TMS320F28377D

The time marked 1) in Figure 6.6 and 6.7 shows the ADC conversion time of the TMS570LS1227 and the TMS320F28377D micro-controllers and they are respectively measured to be 1.03 μs and 0.63 μs. TMS320F28377D has shorter ADC conversion time compared to TMS570LS1227, even though its ADC clock frequency is lower than of TMS570LS1227. Both the micro-controllers, has the capability to increase the ADC clock upto 50 MHz, which reduces the conversion time further.

The small voltage fluctuation at the time instant marked 4) in Figure 6.6 and 6.7 shows the instant at which the ADC sampling starts. The time instant marked 2) in both the figures shows that the signal toggled for ADC SOC appears little later than the actual sampling instant shown at 4). This is due to the delay inside the micro-controller.

The time marked 4) in Figure 6.6 shows that the actual start of the ADC conversion for TMS570LS1227 is at 15.66 μs, which is slightly longer than the actual center of the PWM, 31.18 μs/2 = 15.59 μs. But the time marked 4) in Figure 6.7 shows that the start of the ADC conversion for TMS320F28377D is at 31.24 μs, which is approximately equal to the middle of the PWM period 31.26 μs.

In-order to sample exactly at the centre of the PWM period, the ADC SOC interrupt can be generated slightly earlier than the actual PWM center in TMS570LS1227 by configuring the PMW SOC source register‘s comparator value slightly lower than its value at the PWM center. As discussed in Chapter 5.4.2, both the ADC channels need to be sampled simultaneously. The time instant 4) of both the figures also shows that both the ADC channels starts sampling at the same time.

6.4.2 Quality of the PMSM stator current measurement using the ADC module

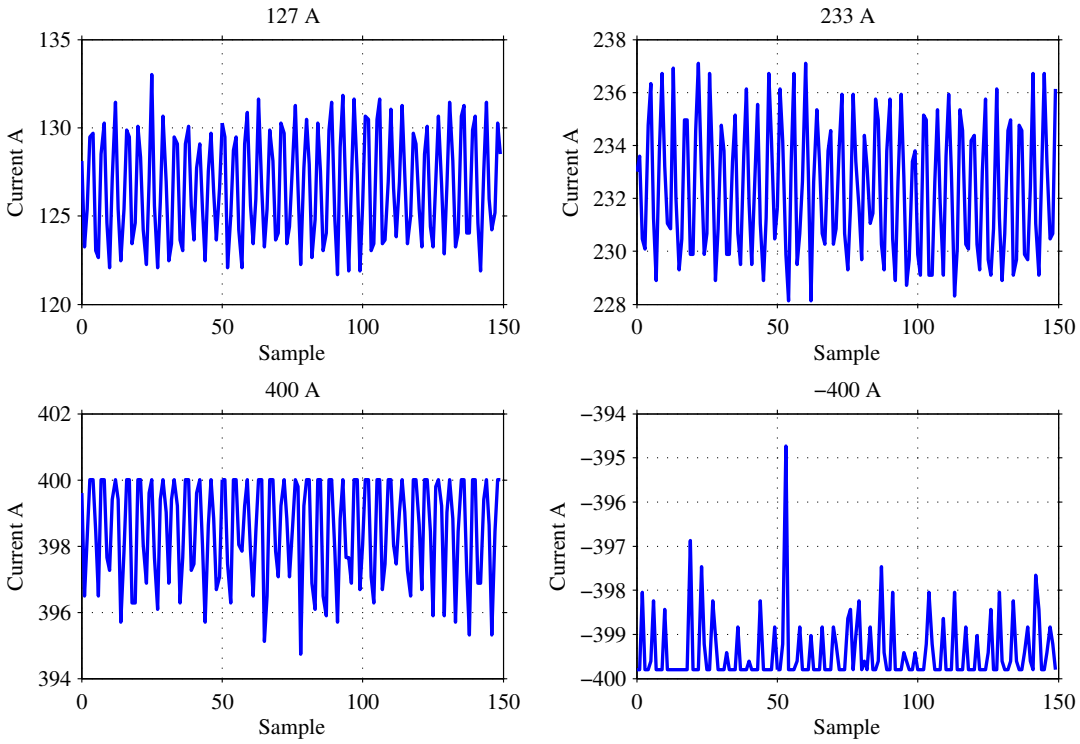


Figure 6.8: Quality of the ADC measurement using TMS570LS1227 for different stator currents

To measure the quality of the current measurement, a constant current has been kept in the dSpace and the same has been measured with the micro-controller. Figures 6.8 and 6.9 shows the readings inside the micro-controller at different current levels. One sample in the X-axis equals 125 μs. Figure 6.8 shows that TMS570LS1227 has more noice in the ADC channel. This may be due to grounding problems in the system, as the whole system has three different sources of supply one for each

subsystem dSpace, micro-controller and evaluation circuit. The long connecting cable from dSpace to the evaluation kit may also influence the same. Maximum 8 A of fluctuations observed at 400 A and - 400 A in Figure 6.8, which is 1% of the overall range of -400 A to 400 A. For TMS320F28377D, Figure 6.9 shows that the fluctuations in the current measurement is comparatively lower, which may be due to the reason that its power supply for both evaluation and micro-controller are from the USB of the testing computer. So the number of sources that is feeding the connected system is reduced. Figure 6.8 and 6.9 doesn‘t shows noice beyond -400 A and 400 A, as that is the highest limit configured in the micro-controller.

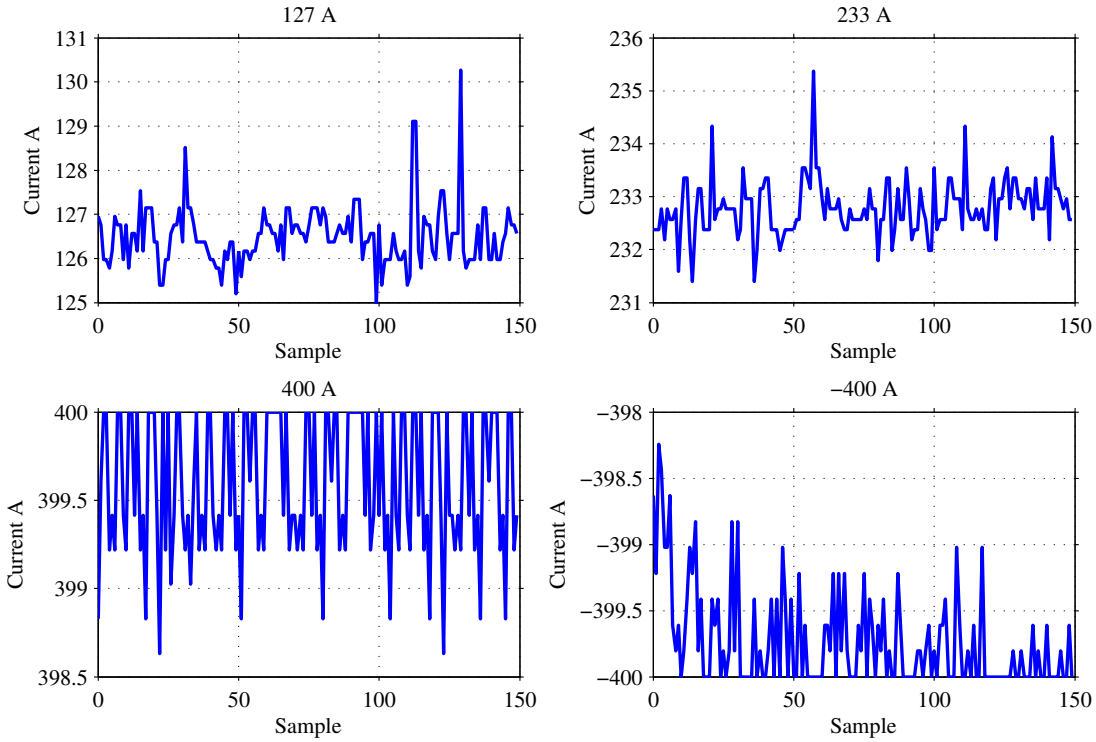


Figure 6.9: Quality of the ADC measurement using TMS320F28377D for different stator currents

6.5 Quality of the PMSM rotor position measurement using the encoder module

Both TMS570LS1227 and TMS320F28377D has the same type of encoder module. To test the quality of the rotor position measurement, a constant speed for the PMSM is kept inside dSpace as described in Chapter 5.4.4 and the readings of the encoder in the micro-controller is plotted in Figures 6.10 and 6.11 for different rotor speeds. One sample in the X-axis equals 125 μs. Figures 6.10 and 6.11 show that the position is varying as a smooth triangular signal for all the rotor speeds and there is no wobbling in the encoder reading. Also the frequency of the each triangular waveform for a particular speed, is same as the electrical frequency corresponds to the speed. If there is a problem with the position measurement, the waveform will not have perfect triangular waveform and its frequency will not match with the constant speed set in dSPace.

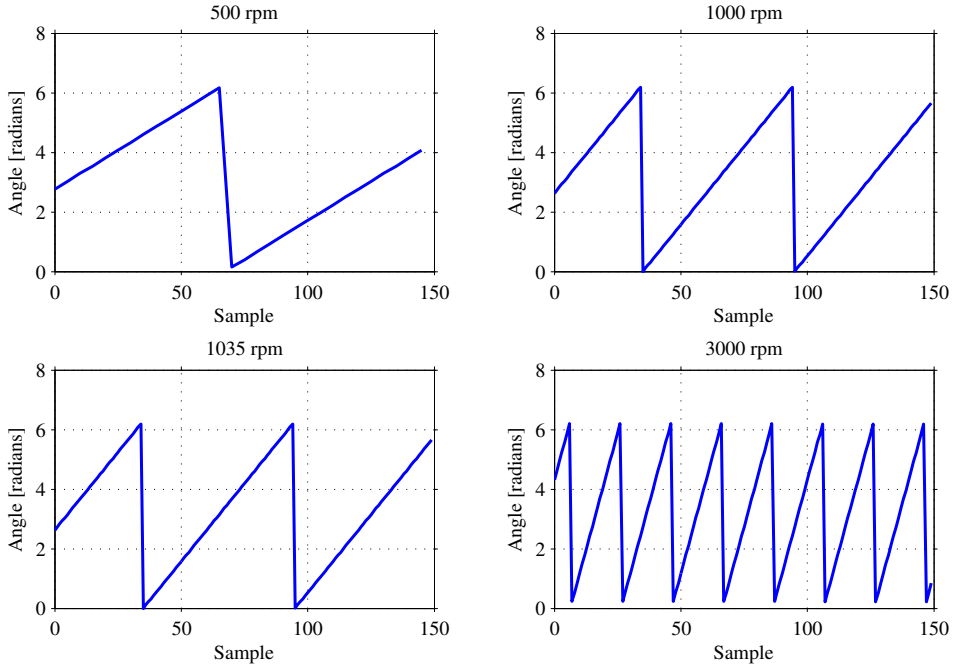


Figure 6.10: PMSM position measurement using TMS570LS1227

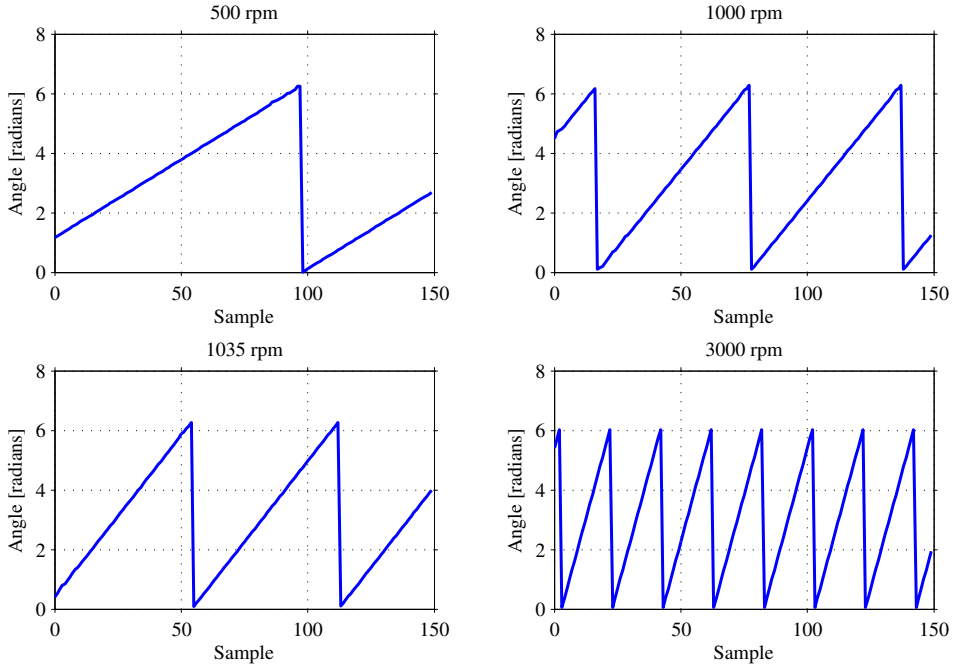


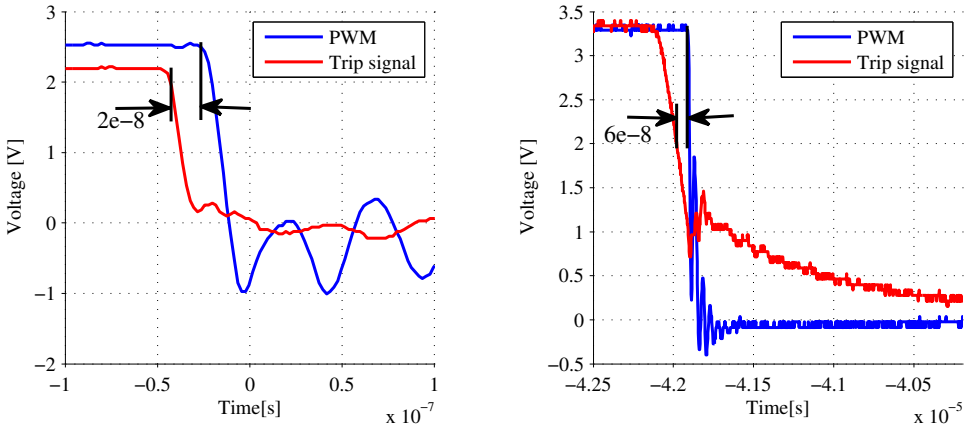
Figure 6.11: PMSM position measurement using TMS320F28377D

6.6 Fault response time of the PWM gate signals

The PWM module of the micro-controller is configured to block the gate pulse, once the fault signal is detected. Figure 6.12 shows the active low fault signal to the micro-controller and PWM output from the micro-controller. The micro-controllers TMS570LS1227 and TMS320F28377D detect active low at its digital input channel when the voltage is below 0.3 V and 0.7 V respectively as per its datasheet [27] [31]. From Figure 6.12 it can be noticed that for TMS570LS1227 and TMS320F28377D it takes 20 ns and 60 ns respectively to block the gate pulse after the fault

signals falls below 2 V. 2 V is selected just to make a fair comparison between both the micro-controllers. The rate of fall of both the trip signals is not the same, as it depends on the impedance at the digital input of the micro-controller. Though the active low signals is detected inside the micro-controller TMS570LS1227 below 0.3 V (below 0.7 V for TMS320F28377D), to measure the actual fault response time in the system its better to measure it from the time at which the fault signal voltage starts decreasing from the reference value.

Volvo is expecting to operate the PMSM upto 6000 rpm. The electrical frequency of the PMSM at 6000 rpm is 800 Hz, which means that the electrical cycle period is 1.25 ms. The micro-controllers are not used to detect the actual fault in the drive system. The actual faults like over-current fault or earth fault is detected using a external device/relay and the micro-controller is just receiving a signal indicating the presence of a fault. In both the micro-controllers, the fault signals is detected in less than 1/20000 of the electrical cycle time of 1.25 ms. Though there is no reference document regarding the fault response time for the micro-controller to block the gate pulse, the time measured is considerably lower compared to the electrical cycle time of the motor under consideration. So both the micro-controllers have a good fault response time.



(a) TMS570LS1227 (b) TMS320F28377

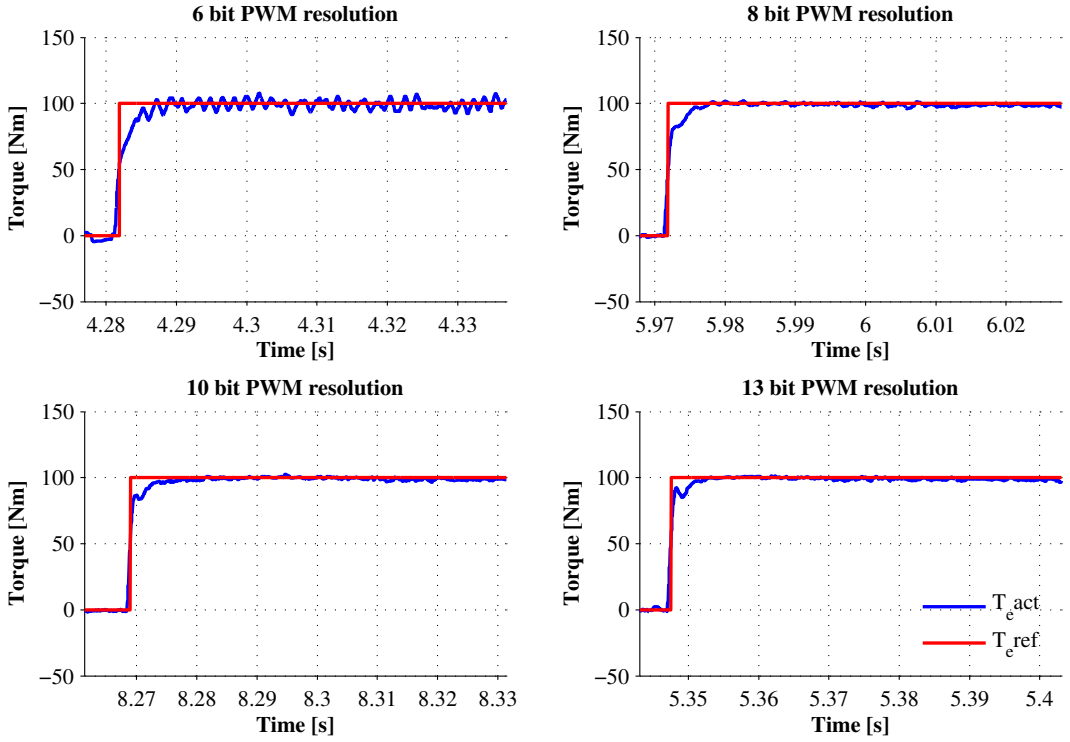
Figure 6.12: Fault response time with the micro-controllers TMS570LS1227 and TMS320F28377

6.7 Comparing measurements with simulation results

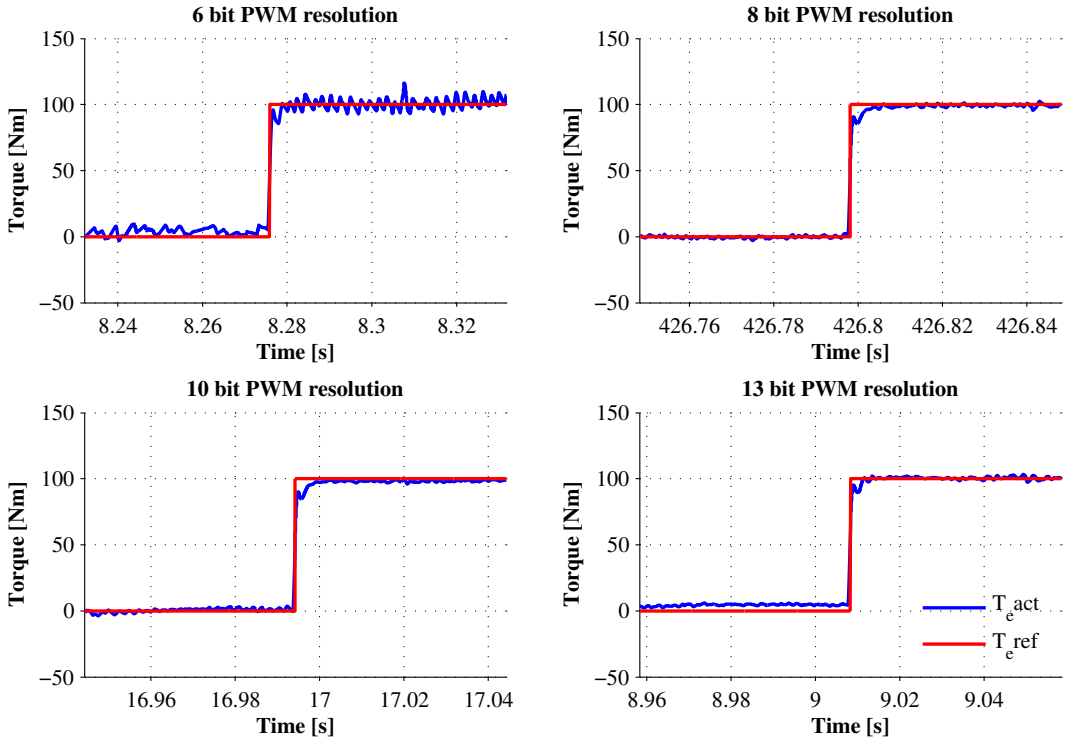
Both micro-controllers has been operated under the same conditions as that of the simulations described in Chapter 4 and the results from the measurements are discussed here.

6.7.1 Impact of PWM resolution

The resolution of the PWM has been varied by modifying the PWM clock frequency for both the micro-controllers and the results are shown in Figures 6.13 and 6.14. The result shows that the torque control is perfect for all the resolution except for 6 bit resolution. In Figures 6.13 and 6.14, for 6 bit PWM resolution the ripple around the torque reference is high compared to other higher resolution. The figures also show that for the PWM resolution 10 bits and 13 bits, the torque ripple is very less and there is no visible improvement in the torque response for the resolution above 10 bits as discussed in Chapter 4.2.1. The torque step response is not following the designed first order response and also there is a slight variation in the response time of the torque in the real experiment compared to its simulation in Chapter 4. This is due to the presence of additional impedance in the hardware system connecting dSpace and the micro-controller evaluation board. The output impedance of dSpace analog channel, input impedance of the evaluation board analog channel and the length of the wire connecting dSpace and the evaluation board for the stator current feedback make the step response to deviate from the fist order response.

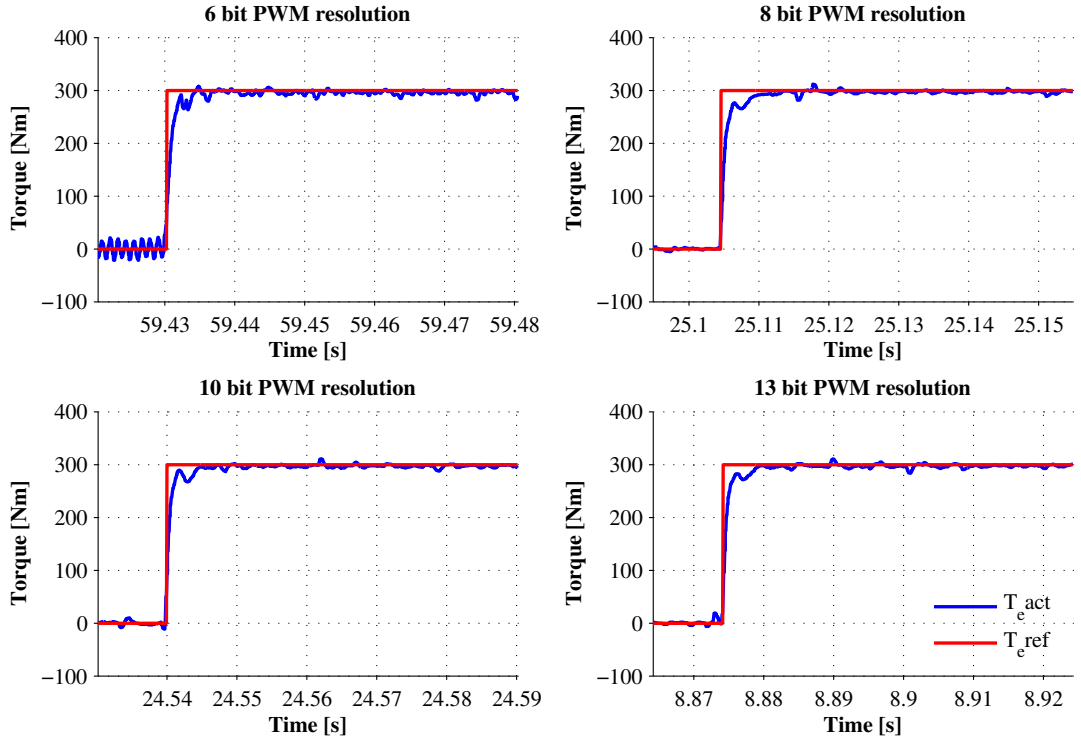


(a) TMS570LS1227

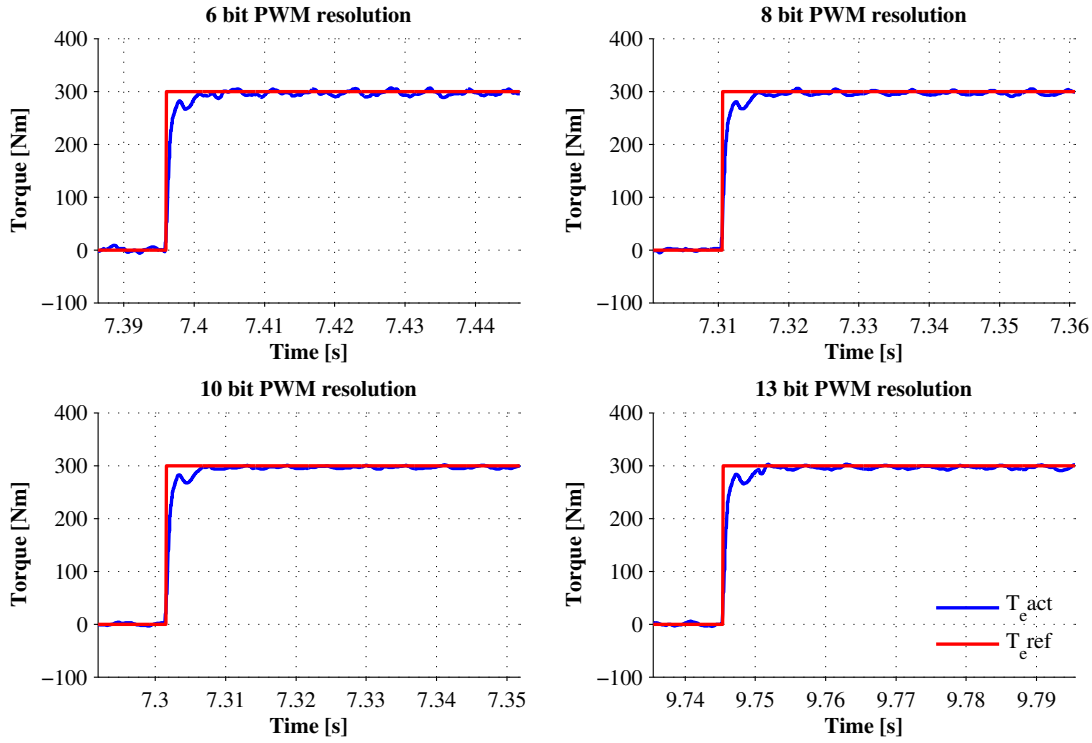


(b) TMS320F28377D

Figure 6.13: T_e step response with f_{sw}=8 kHz, 100 rpm and $T_eref = 100Nm$ for different PWM resolution



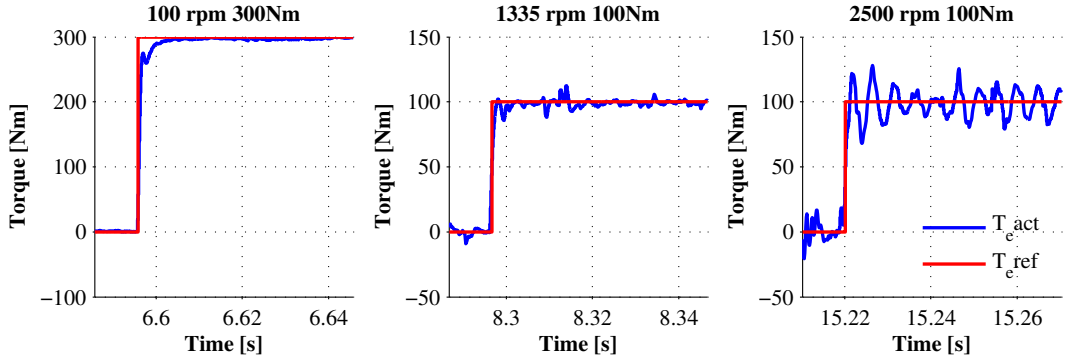
(a) TMS570LS1227



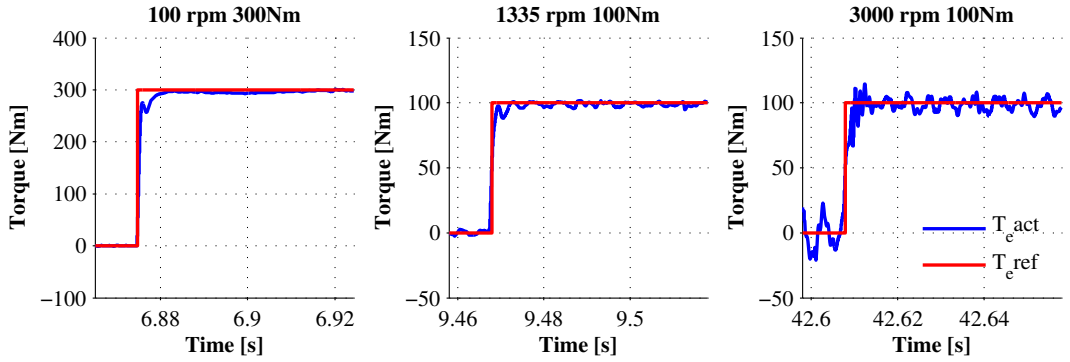
(b) TMS320F28377D

Figure 6.14: T_e step response with f_{sw}=8KHz, 1335 rpm and $T_eref = 300Nm$ for different PWM resolution

6.7.2 Impact of PWM updation delay



(a) TMS570LS1227



(b) TMS320F28377D

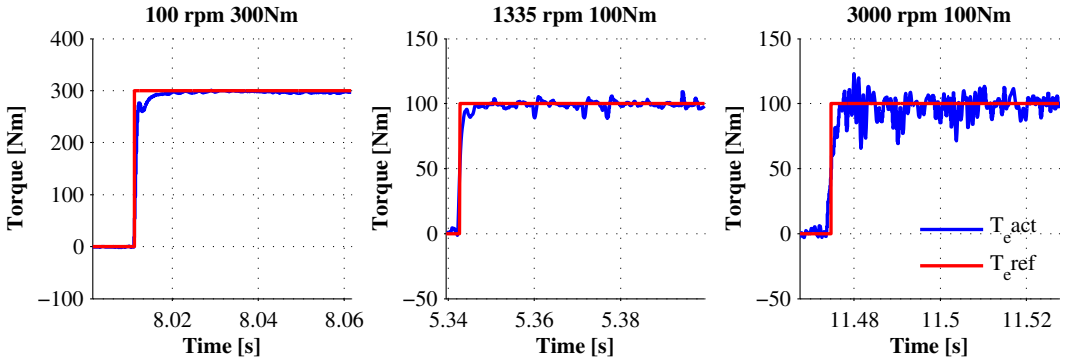
Figure 6.15: T_e step response f_{sw}=8 kHz for different rotor speeds, with the stator voltage delay compensation 1.3 sample

The rotor position compensation is required to have a perfect control of the PMSM as discussed in Chapter 3.5.3. Just to have ease of testing, instead of implementing the compensation in the micro-controller, the angle compensation has been done at the dSpace level. The offset for the rotor position angle used for the transformation of the 3-phase stator voltage to the dq-coordinates has been adjusted in dSpace to match u_{sd} and u_{sq} request in the micro-controller with the same in dSpace. For both the micro-controller there is a difference of 1.8 sample for the position measurement. This is not exactly 1 sample or 1.5 sample as stated in Chapter 3.5.3, because of the additional delay from dSpace to measure the duty cycle of the gate signals as described in Chapter 6.3.

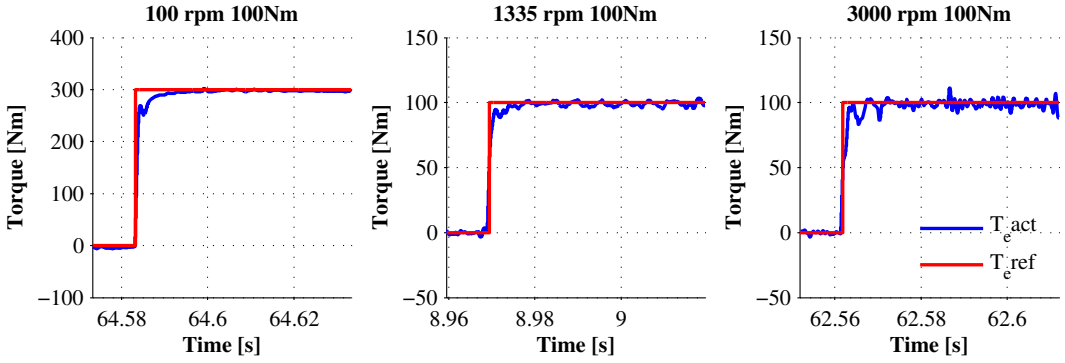
Figure 6.16 shows the torque response with compensation implemented for 1.8 sample delay and Figure 6.15 shows the torque response with compensation implemented for 1.3 sample delay. Figure 6.15 shows that, in TMS570LS1227 the torque is not able to follow the reference at 2500 rpm itself, but for TMS320F28377D the torque response is comparatively better upto 3000 rpm. This is because the ISR execution time is longer in TMS570LS1227 compared to TMS320F28377D, so it introduces the additional delay in updating the PWM duty cycle. When the delay compensation is 1.8 sample, both the micro-controllers is able to control the torque upto 3000 rpm as shown in Figure 6.16. If the compensation is reduced below 1.3 samples, the system is not able to control the torque if the speed is above 1000 rpm.

The figures showing the torque response with the delay compensation less than 1.3 sample has not been shown in this thesis, as the response is poor and the torque is deviating completely from the reference torque. Figures 6.16 and 6.15 show that, the delay compensation of 1.3 sample delay introduces more torque ripple for the higher speeds compared to the 1.8 sample delay compensation. These results show that at higher speeds the rotor position compensation should be more accurate

to have a better torque response and it is similar to the results discussed using simulations in Chapter 4.2.3.



(a) TMS570LS1227



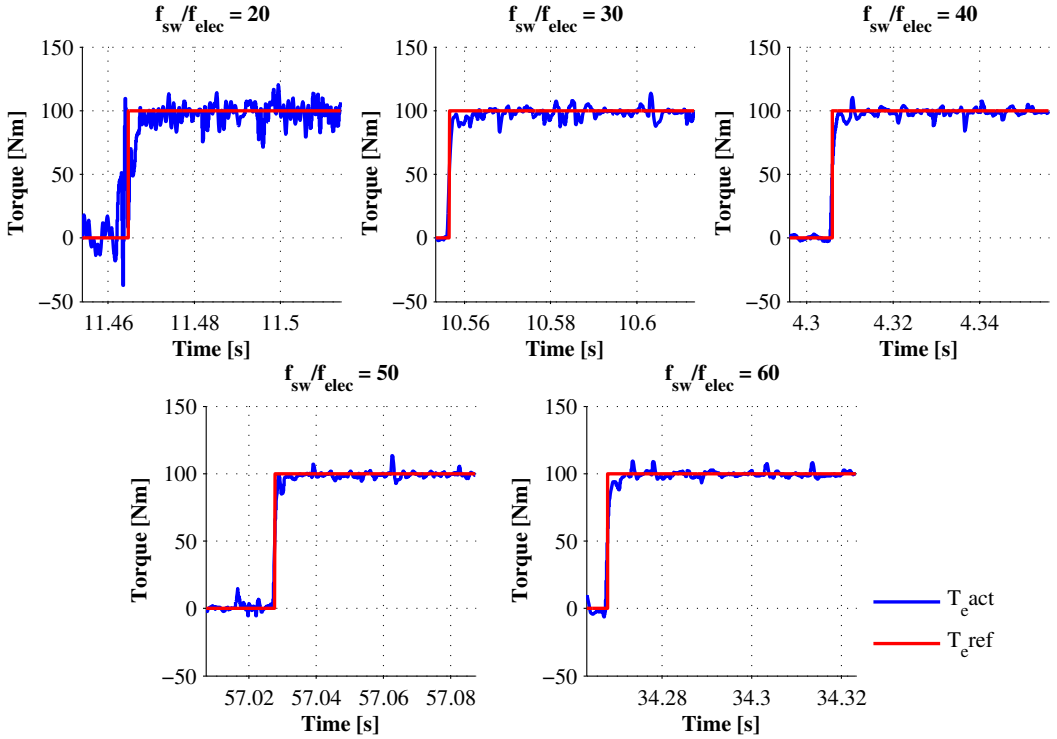
(b) TMS320F28377D

Figure 6.16: T_e step response f_{sw}=8 kHz for different rotor speeds, with the stator voltage delay compensation of 1.8 sample

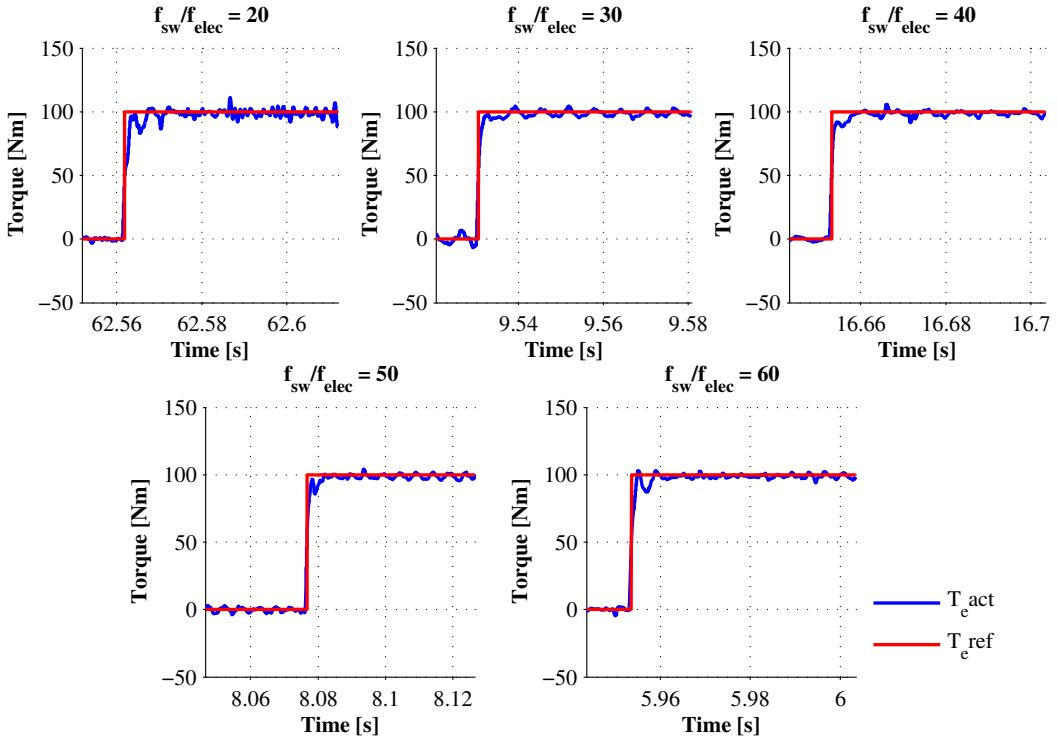
6.7.3 Impact of ratio f_{sw}/f_{elec}

By keeping f_{sw} at constant 8 kHz, the speed of the PMSM has been varied and the torque response of the system for both the micro-controllers is shown in Figure 6.17. f_{sw} is not varied as in the simulation Chapter 4.2.2, due to limitations in dSpace settings. The result shows that, for the ratio f_{sw}/f_{elec} below 30, there is a visible increase in the ripple content. The results also shows that, when the ratio is increased above 30 the ripple reduced slightly. This result matches with the simulation results shown in Chapter 4.2.2. The increase in ratio f_{sw}/f_{elec}, decrease the amount of torque ripple and vice versa.

In figure 6.17(a), When $f_{sw}/f_{elec} = 30$, the torque step response is not perfect with some oscillations around 10.58 s. This is similar to the simulation results for the ratio $f_{sw}/f_{elec} = 30$. But the same effect is not visible in 6.17(b), it may be due to the fact that the micro-controller TMS320F28377D has better ADC performance and lower execution time compared to TMS570LS1227. So its better to chose the ratio f_{sw}/f_{elec} 40 and above to have better performance with all type of micro-controllers for the motor under consideration.



(a) TMS570LS1227



(b) TMS320F28377D

Figure 6.17: T_e step response f_{sw}=8 kHz, with different f_{sw}/f_{elec}

6.7.4 Impact of ADC resolution

The resolution of ADC has been changed and the step response for I_q has been measured for both the micro-controllers. Figure 6.18 and 6.19 shows the step response for I_q with different ADC resolution. Table 6.5 and 6.6 shows the ripple content in the I_q during different resolution.

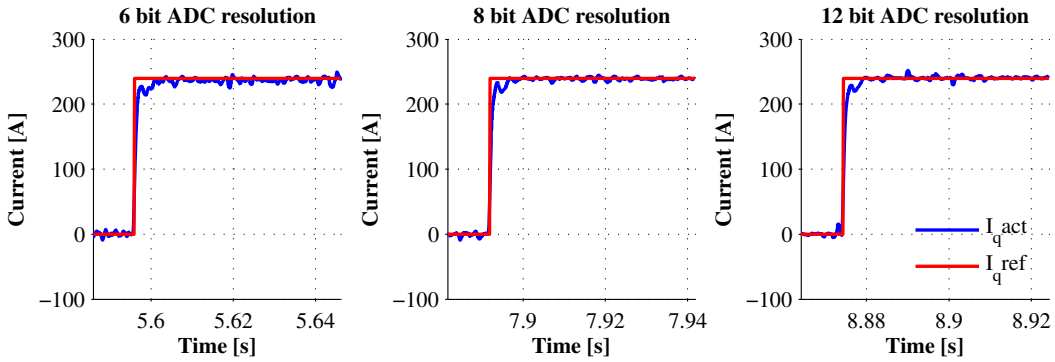
The ripple is measured as worst case peak to peak current, after eliminating the outliers. The results are very similar to the one described in Chapter 4.2.4 and for a particular set-point, the amount of ripple will increase considerable amount only when it is below 8 bit. Tables 6.5 and 6.6 show that when T_eref is 300 Nm, the current ripple with the TMS570LS1227 is noticeably high compared to the ripple with TMS320F28377D. This is because of the more fluctuation in the current measurement with TMS570LS1227 as discussed in Section 6.4.2.

Table 6.5: i_q peak to peak ripple for different ADC resolution in [A] at 1335 rpm - TMS570LS1227

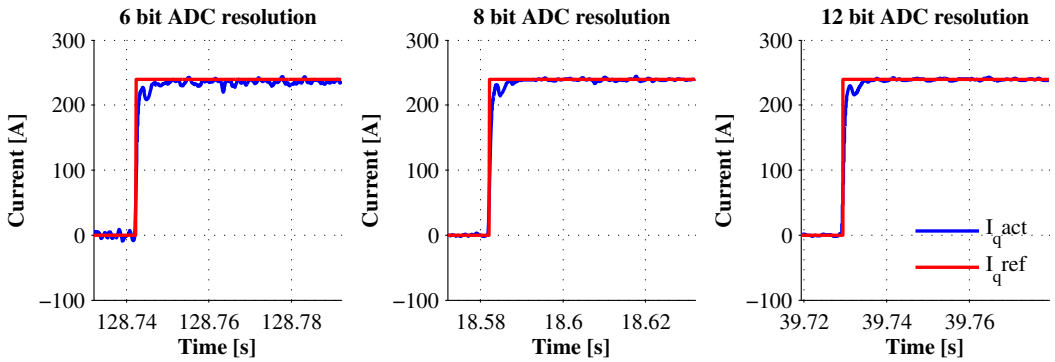
ADC Resolution	**6 bit**	**8 bit**	**12 bit**
$T_e$ref=50 Nm, $I_q$ref=40 A	11.39	8.66	8.31
$T_e$ref=300 Nm , $I_q$ref=240 A	24.6	12.2	13.1

Table 6.6: i_q peak to peak ripple for different ADC resolution in [A] at 1335 rpm - TMS320F28377D

ADC Resolution	**6 bit**	**8 bit**	**12 bit**
$T_e$ref=50 Nm, $I_q$ref=40 A	15.66	8.29	8.65
$T_e$ref=300 Nm , $I_q$ref=240 A	21.8	7.4	6.2

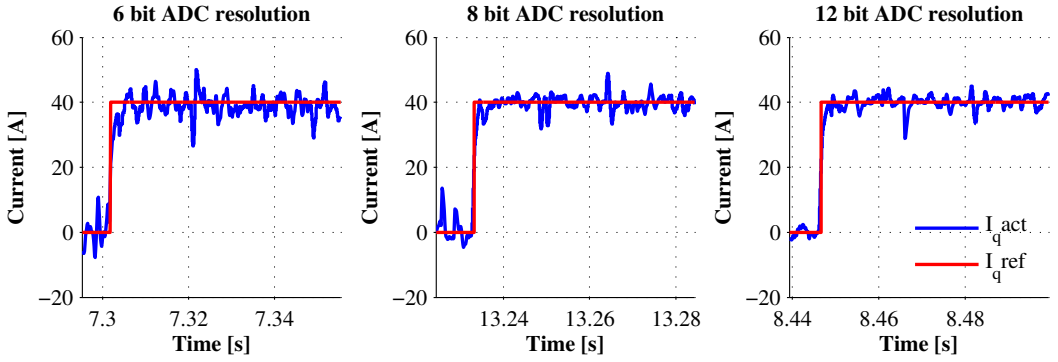


(a) TMS570LS1227

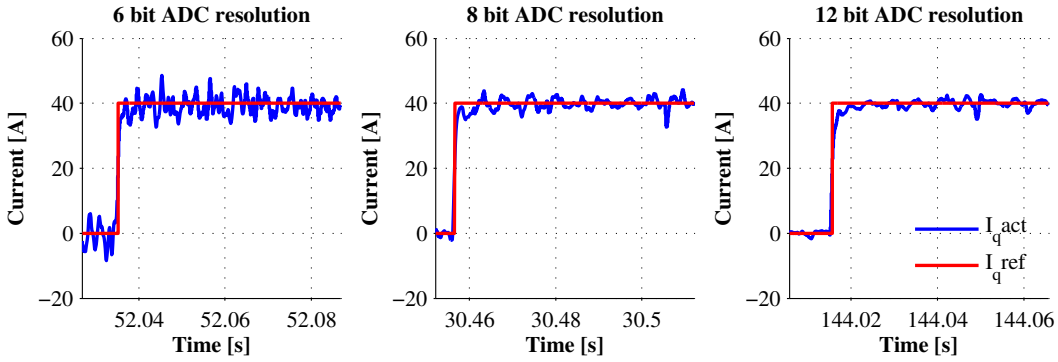


(b) TMS320F28377D

Figure 6.18: I_q step response with 1335 rpm, $T_eref = 300Nm$ and f_{sw}=8KHz - different ADC resolution



(a) TMS570LS1227



(b) TMS320F28377D

Figure 6.19: I_q step response with 1335 rpm, $T_eref = 50Nm$ and f_{sw}=8KHz - different ADC resolution

6.8 Code developing and debugging

Code composer studio 5.5 is used for developing the code and debugging the micro-controller and XDS100V2 is the debugger used for this thesis. Both the evaluation boards used for this thesis are having the full license to use developing and debugging environment. Also the board DRV8301LS12 EVM came with the software Halcogen, which is very useful in the initial hardware configuration. Halcogen provides user interface to all the modules in the controller, the user has just to select the module and click the required configuration. Code for the selected hardware will be automatically generated using Halcogen. This type of option is not available for code developing in TMS320F28377D.

XDS100V2 is a low cost debugger available with Texas. If XDS560 debugger is used acomplete system trace is possible in TMS570LS1227 [30]. TMS570LS1227 has a debug access port(DAP) which allows the direct access to entire memory without halting the processor. Similarly TMS320F28377D micro-controller's real time debug support the programmer to halt and debug the system, while critical user defined real time tasks are running in parallel.

Chapter 7

Observations and conclusions

7.1 Observations

The observations about the micro-controllers TMS570LS1227 and TMS320F28377D about its performance and architecture other than those described in previous sections will be discussed in this section.

7.1.1 TMS320F28377D

TMS320F28377D has the advantage of having the CLA and the same has been used to completely take care of the ISR in this thesis. As discussed in Section 6.2 the CLA has problem with allocating program memory in the RAM, though it has 16 kB memory only 4 kB was possible to utilize for its program. But this could be solved by studying more on the RAM memory configuration or by only using the CLA to take care of parts of the ISR and leaving the CPU to do the remaining job. By reducing the tasks of the CLA, program size would reduce and thereby the need of more memory. Even though the CLA has a huge advantage of taking the biggest load of the CPU the codes in the CLA cannot access the Trigonometric Math Unit (TMU) and Viterbi Complex Unit (VCU), which is meant to do some complex mathematical calculation at a very high speed.

Another advantage of TMS320F28377D is that all the supporting units like CLA, TMU and VCU can be programmed using C language itself, which gives the easy solution for the application developers. It also has safety features like Error Correction Code (ECC) on Flash , ECC or parity on RAM, missing clock detection, hardware built in self test for CPU and programmable built in self test for memory. Though these features are not evaluated during this thesis, this may help to achieve ASIL-D.

7.1.2 TMS570LS1227

TMS570LS1227 doesn‘t have any special units like TMS320F28377D to enhance the speed of the processor except for a high end timer unit. But its performance is sufficient enough to handle the motor control. As discussed in Section 6.2, it has a CPU utilization of 30.2% at 20 kHz of switching frequency and 80 MHz CPU clock frequency. The CPU utlization will be reduced to almost half 15%, if the CPU clock is increased to 160 MHz, which makes this controller suitable to handle other functions like communications together with the motor control. The high end timer unit (HET) is an independent timer unit in the CPU, which will be used when there is a need of pulse measurement or if a very high speed PWM is required. But it is not very useful with respect to the motor control since the PWM gate signal frequency is low.

TMS570LS1227 is designed to achieve ASIL-D, as per Texas instrument‘s description about the product. It has dual processors in a lock step architecture, hardware built in test for CPU and SRAM, Error correction code (ECC) for flash and SRAM, parity on peripheral memory, voltage monitoring unit and clock failure detection. These features help to build the system to achieve the ASIL-D safety standard. But those features are not evaluated in this thesis.

7.2 Results from present work

The simulations of the digital control of a PMSM discussed in Chapter 4 and experimental results in Chapter 6 shows that

- PWM and ADC resolution of 10 bits is the minimum required to have a good torque control performance.
- The ratio between the switching frequency and the fundamental stator frequency, f_{sw}/f_{elec} should be 40 or more to have a better torque control.
- The PWM updation delay compensation has to be accurate to have a good control at high speed operation.

for the studied drive system.

The evaluation of the two micro-controllers TMS570LS1227 and TMS320F28377D has been discussed in Chapter 6. It shows that, with respect to the performance of the ADC module, the PWM module and the encoder module both micro-controllers perform almost the same. Except for the ADC module of TMS320F28377D that has some advantage on its conversion time, compared to the other. But as discussed in Section 6.4.1, that can be improved byu increasing its clock frequency.

The advantage of TMS320F28377D is that the whole motor control can be implemented or part of the motor control can be implemented in the CLA module, which reduces the CPU load. This helps the CPU to efficiently handle the other functions like communication. So if PMSM control is only taken into consideration for the selection of the micro-controller, TMS320F28377D will be the best choice among the two.

But in the automotive industry, safety standards has to be met. Though in this thesis, safety of the micro-controller is not evaluated, as per the data sheets of Texas Instruments, TMS570LS1227 is built in such a way that the architecture helps the application developers to achieve ASIL-D. But TMS320F28377D almost has all safety features mentioned in data sheets of TMS570LS1227 except the lockstep architecture. If the application developer comes with a solution to achieve ASIL-D in TMS320F28377D, it will be the most suitable micro-controller for PMSM control in a automotive environment, else it is better to chose TMS570LS1227, as safety has higher priority.

In general, the best suitable micro-controller architecture for the automotive PMSM control applications, should combine the features of TMS570LS1227 and TMS320F28377D. The description of the general architecture that combines the above two micro-controller is shown below

CPU

- Dual CPU in lockstep architecture to meet the safety requirement easily.
- Minimum clock frequency required with respect to PWM resolution is 20.5 MHz, but to have faster ISR for motor control computation, it is better to have minimum of 160 MHz as per Chapter 7.1.
- Similar to TMU and VCU, mathematical processing units to do critical tasks faster.
- Floating point unit for easy programming without worrying about scaling.
- Hardware built in test for CPU and RAM, ECC for memory unit, parity on peripheral memory, voltage monitoring unit and clock failure detection

Co-processing unit

- Independent control units like CLA to handle critical tasks without the help of CPU.
- Co-processing unit should have access to the ADC, PWM and Encoder registers, to avoid the delay due to transfer of data between CPU and co-processor.
- Compiler for co-processing unit should also be in either C or C++ instead of assembly level coding, which ease the life of the application developer.
- Facility to calculate the execution time of the code inside the co-processing unit should be available.
- Debugging of the Co-processing unit should be possible with the same debugging tool used for CPU.
- It would be advantage to have a facility to access the fast mathematical processing unit in co-processor also, but it is not necessary.

PWM module

- PWM resolution should be minimum of 10 bits.
- Dead time should be configurable for the PWM signals.
- ADC start of conversion interrupt should be able to initiate at any time during the whole period of the PWM, by configuring the proper registers.
- Hardware interrupts with fault condition, should be directly linked with the PWM module to block the PWM gate signals under fault conditions.
- Shadow registers should be available in the PWM module to update the PWM period during any time of the motor operation.

ADC module

- At least 10 bit resolution. ADC channel with differential ended mode is an advantage.
- At least two ADC modules is required. Both the modules should be able to initiate SOC simultaneously based on the interrupt from the PWM module.
- ADC end of conversion interrupt should be generated little earlier than actual conversion ends, to initiate ISR earlier. As it will make sure that the ISR to start executing exactly after the conversion ends.
- ADC channel error detection facilities like channel open and channel short.

PMSM rotor position detection module

- Either dedicated high resolution encoder module or resolver to digital conversion module should be available for accurate rotor position measurement. Resolver signals can also be connected to ADC channel and calculate the rotor position, but instead if it has a dedicated module it will reduce the CPU load.

7.3 Future work

The present work is mainly focused on evaluating the micro-controller architecture for the PMSM control implementation, but it could be extended to check its communication processing capability, safety features to achieve ASIL-D and verify whether it is completely suitable for the automotive applications. The present work doesn‘t involve the optimization of the codes of the control algorithm. Optimizing the control algorithm may reduce the CPU load and memory. Different types of PMSM control algorithms can implemented to operate the PMSM at the lower f_{sw}/f_{elec} ratio and check the micro-controller‘s ability to perform.

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