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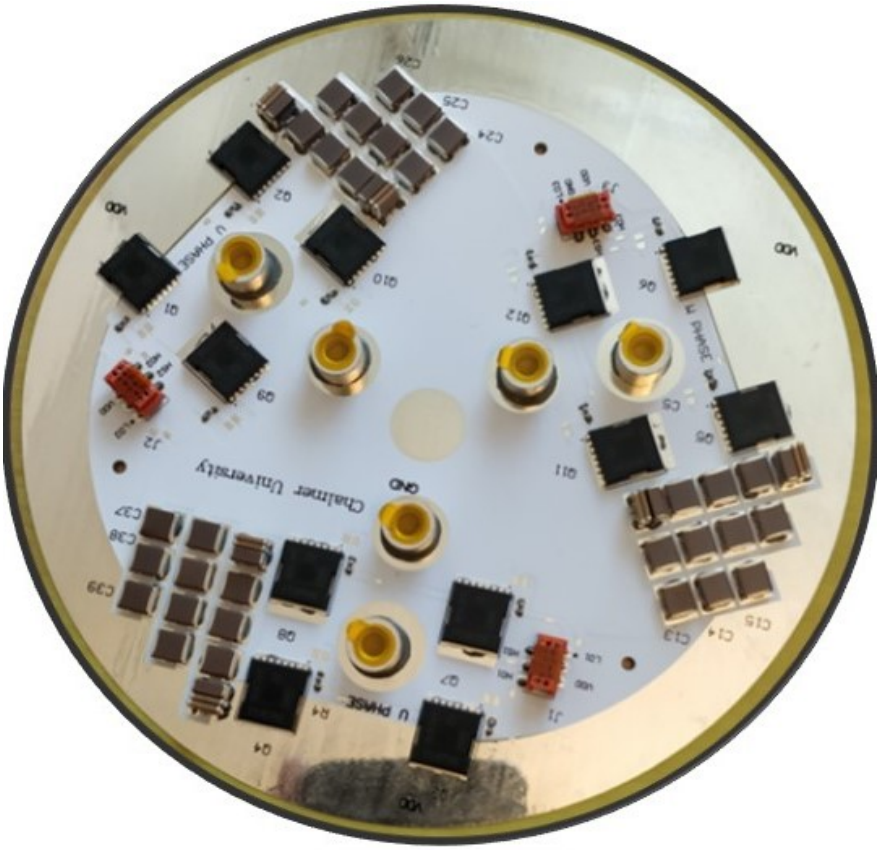

Design and Characterization of a 48V Inverter for Mild Hybrid Vehicle Application

Master's thesis in Electric Power Engineering

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Department of Electrical Engineering
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Gothenburg, Sweden 2019

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Master's Thesis 2019
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Abstract

This thesis deals with the design, construction and characterization of a 48V three-phase inverter for a mild-hybrid vehicle application. The inverter prototype is designed to operate at a peak power of 20kW and continuous power of 10kW, to achieve these high current levels paralleling of MOSFET's has been carried out. The prototype is designed to be directly integrated to the Traction Motor. Printed circuit boards for the inverter and the gate drivers are designed to be compact and modular. Different design considerations like appropriate placement of the DC link and the placement of gate drivers close to the MOSFET's has been done in this thesis to improve the performance of the inverter. The thermal analysis of the inverter is evaluated using COMSOL and finally the inverter is built and tested using a static load.

The inverter has been tested to deliver a continuous output power of 10kW at a switching frequency of 100kHz. Calorimetric analysis is carried out to measure the losses. Finally, the practically obtained results are compared with the theoretically predicted results and validated.

Keywords: Inverter, PWM, Mosfets, Calorimetric, Losses, Design, Capacitor bank, COMSOL, %, A, kW, Temp

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Akshay Santosh & Poovattil Tomy Biju Jude, Gothenburg, August 2019

Acronyms

AC Alternating Current. 51
ADC Analog to Digital Converter. 19

BSG Belted Starter Generator. 3

DC Direct Current. 1, 4

EM Electric Machine. 1
ESR Equivalent Series Resistance. 13

ICE Internal Combustion Engine. 1, 3
IGBT Insulated Gate Bipolar Transistor. xi, 5
IMS Insulated Metal Substrate. 21

MLCC Multi-Layer Ceramic Capacitor. 37
MOSFET Metal Oxide Semiconductor Field Effect Transistor. 1

PCB Printed Circuit Board. 14
PDE Partial Differential Equations. 16
PMSM Permanent Magnet Synchronous Machine. 3
PWM Pulse Width Modulation. 4

RMS Root Mean Square. 13

SMD Surface Mount Device. 1

Contents

1
Introduction

1.1 Background

In recent years there is a constant increase in the demand and usage of passenger vehicles which results in increased CO_2 emission. There is a need to control this excessive CO_2 emission which is possible by electrification or using cleaner fuels like Hydrogen in vehicles. Due to this, the government has implemented strict regulations on the automobile manufacturers and in-turn the automotive industry is moving towards rapid electrification. One of the many approaches in this electrified revolution is the mild hybrid.

The passenger car industry is moving towards 48V mild-hybrid systems. The mild hybrid system consists of an oversized Electric Machine(EM) which is integrated with an Internal Combustion Engine(ICE) through a belt-drive, gearbox, motor controller with integrated power electronics. Along with an efficient battery system, this mild hybrid system can prove to be more efficient by utilizing the EM and ICE for coasting, power assist, and regenerative braking. Further using the 48 V system gives an advantage to handle a higher power requirement in the other functional units inside the vehicle, like the use of a completely electric air conditioning system, which can reduce the direct load on the engine and enable cooling during queues without running the ICE. Also, other units like the cooling pump and infotainment systems can run from this 48 V system. To achieve an efficient mild hybrid system there is a need to optimize the power electronics and reduce the losses by having an efficient cooling system and choosing the right semiconductor devices for this application.

1.2 Previous Work

From various research efforts within this field it is seen that it is possible to use a parallel MOSFET combination when designing a modular compact and efficient inverter as a single MOSFET has lower turn on resistance compared to a MOSFET module [1] [2] [3] [4]. The major concern when considering paralleling SMD MOSFETS is the cooling. Some researches have dealt with these concepts, but there were major flaws in the design such as the placement of the DC link, cooling structure and most importantly the placement of the driver circuit for the MOSFET's [5]. To conclude, all these steps were considered in our project from the start to avoid similar design flaws. Additionally this project work deals with the characterization of the inverter to analyze the various losses calculated theoretically with the practical measurements and compared using calorimetric measurement, furthermore the thermal behaviour is modelled and simulated using COMSOL.

1.3 Aim

The aim of this master thesis is to design and build a low voltage inverter for a 48 V mild hybrid vehicle and to predict the losses theoretically and compare it practically. Also, to create a thermal model of the inverter and predict the thermal behaviour for different coolant flow rates theoretically using simulation tools and verify it practically by using Calorimetric measurements.

1.4 Scope

As the inverter will be a part of the Hybrid vehicle and will be very close to the electric machine the ambient temperature is expected to be higher due to the close proximity of the components and lack of space, thus controlling the temperature becomes very crucial for a continuous operation, hence there is a need for an efficient cooling system. The designing of the cooling plate and the material used for it is not the scope of this thesis. However it will consider the different flow rates and types of coolant used as calorimetric measurements is one of the major focus of this thesis. In this thesis the inverter current is controlled in open loop.

2

Theory

2.1 48V Mild Hybrid system

The electrified vehicles system can be subdivided into different types like full electric, plug-in hybrid, micro hybrid and mild hybrid system. The mild hybrid system is a 48V system which consists of a 48V battery, inverter/Motor controller and a 48V (PMSM) Permanent magnet synchronous machine. This PMSM machine is commonly known as the BSG(Belt driven starter Generator) machine. This BSG machine is connected in parallel to the Internal Combustion Engine through a belt or sometimes through gears, it is used to crank the ICE during starting of the vehicle and later used as a generator during normal operation to charge the 48V battery for the other other systems in the car that run on 48V like the Cooling system etc. Also this system has a 48V to 12V DC/DC converter to charge the 12V battery and operate the other systems like the safety and lighting system of the vehicle. This BSG machine is also used to produce power during breaking as regenerative break to produce power and charge the battery, It also can assist the engine to some extent to produce extra power during some high power demand situations from the vehicle. Since the load is high the unit is liquid cooled. Figure 2.1 provides an overview of the general 48V system.

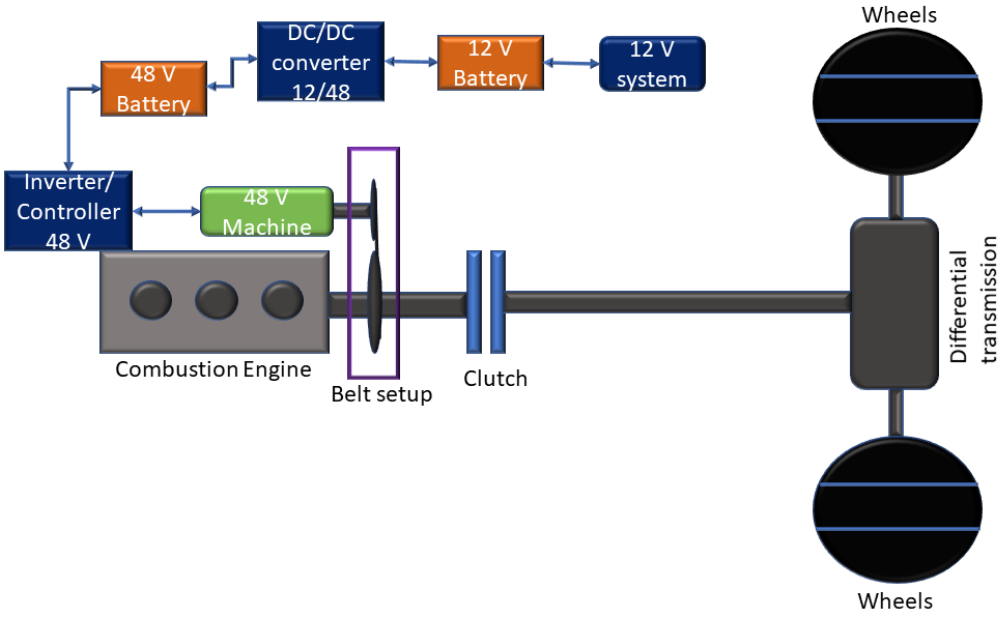


Figure 2.1: Schematic of a three phase inverter

2.2 Three phase Inverters

Three phase inverters are used to supply three phase load for eg. motors. A three phase inverter has three inverter legs combined, where each leg has two mosfets as shown in Figure 2.2. Each of the three legs produces an output which is displaced by 120 degrees from each other. The output of the each leg depends on the DC link voltage,V_d and the modulation index (the switch status). The output voltage is almost independent of the output load current as one of the two switches in a leg is always on at any instant[6].

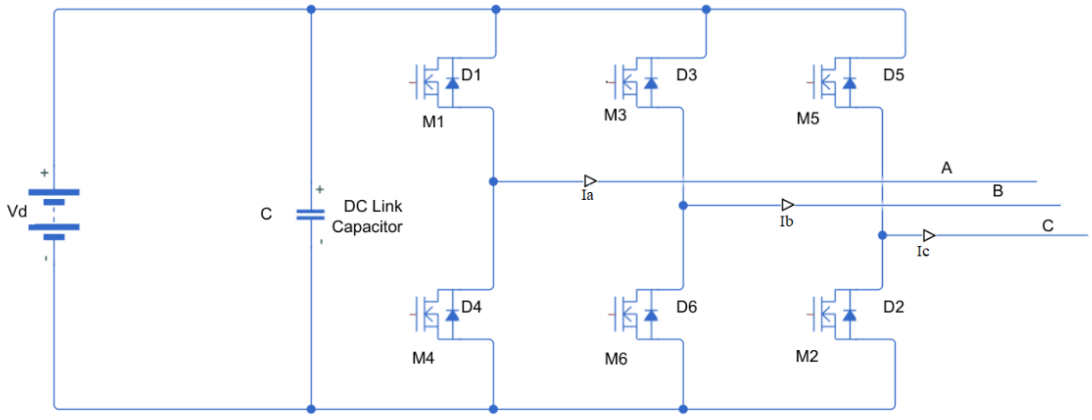


Figure 2.2: Three Phase Inverter

Pulse width modulation(PWM) switching technique is used here to control the duration each switch should be open. A triangular wave is compared with three sinusoidal waves which are 120degree phase shifted from each other. Based on the PWM switching pattern each switch has a duty ratio, D which decides if a switch should be open or close [6].

To generate a switching signal a triangle signal(V_{tri}) is compared with a control signal($V_{control}$) as shown in Figure 2.3. The resultant of the comparison decides which switch in a phase leg that should be opened or closed. If we consider one first leg of the inverter in Figure 2.2. When $V_{control} < V_{tri}$ the switch M4 is on and the switch M1 is off. In most applications the switching frequency is chosen below 6kHz or higher than 20kHz, so that it is above the audible range[6].

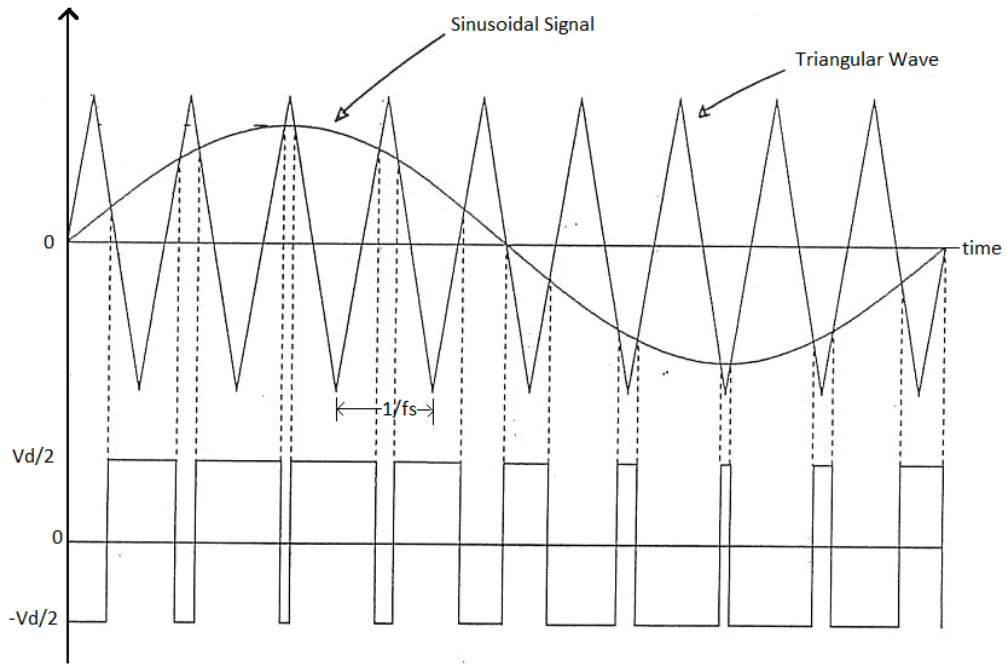


Figure 2.3: Pulse width modulation for one phase

2.3 Switching devices

MOSFET's and IGBT's are the most commonly used power electronic switching devices used in the power converters[6]. The IGBT can operate at ratings such as 1700V, 1200A and up to a switching frequency of less than 20kHz[6]. The MOSFET's can operate up to 1000V and a higher switching frequency up to 100kHz [6]. In the upcoming sections the important features of the IGBT and MOSFETs are outlined.

2.3.1 IGBT

Bipolar Junction Transistors have lower conduction loss at on state but longer switching time at at turn-off. MOSFET's have faster turn on and turn off, but they have a higher conduction loss.BJT and MOSFET combined monolithically on the same silicon wafer have led to the development of insulated gate bipolar transistor(IGBT).

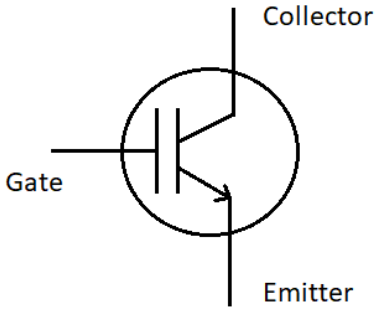


Figure 2.4: Symbol of IGBT

The IGBT has an emitter, collector and gate as shown in Figure 2.4 [6].IGBT's has a similar structure to the vertically diffused MOSFET's. The major difference between the IGBT and MOSFET is the presence of p^+ layer forms the drain of the IGBT [6].The doping level,doping density, thickness of the layer and the type of doping affects the charactersitcs of the device.
The gate-source voltage(V_{GS})controls the state of the device.When $V_{GS(th)} > V_{GS}$ no inversion layer is created between the drain to the source and the device is in off state.When V_{GS} exceeds $V_{GS(th)}$ an inversion layer is created and the device is turned on.

2.3.2 MOSFET

The Metal Oxide field effect transistor(MOSFET) is a majority carrier device i.e. the MOSFET is faster than bipolar devices and is used in fast switching applications[6]. MOSFET's are generally used for low voltage and medium voltage applications and operate at very high switching frequency.They have three terminals gate(g),drain(d) and source(s).

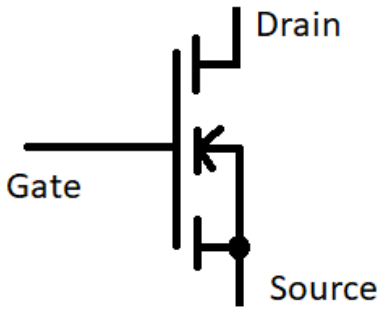


Figure 2.5: MOSFET symbol

When a voltage is applied between gate and source the MOSFET is closed and the current flows from the drain to the source terminal with an ON state resistance($R_{ds,on}$)

between them. The MOSFET has an anti-parallel diode known as body diode, Due to the presence of this, The MOSFET does not block negative voltage. The power MOSFET has a vertical structure as shown in Figure 2.6.

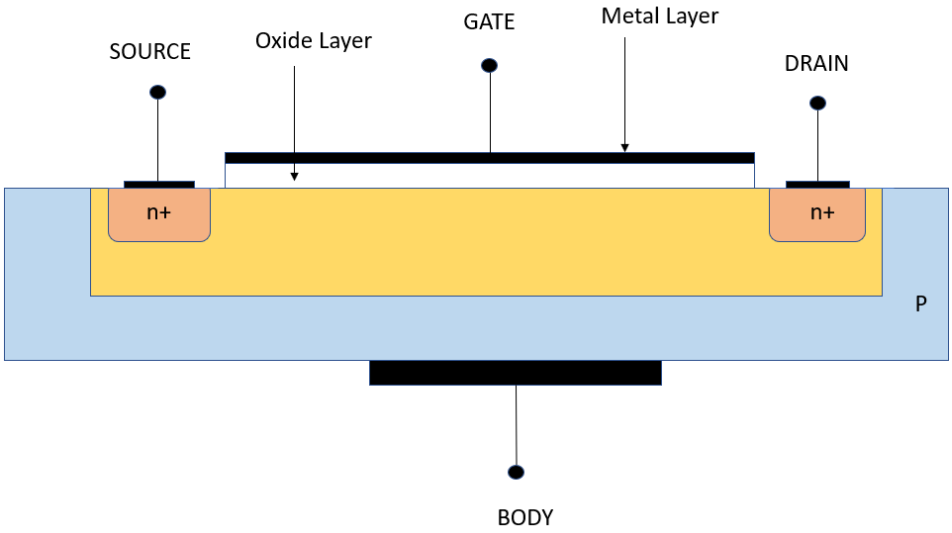


Figure 2.6: Vertical diffused MOSFET

The thickness and the width of the gate determines the amount of current that flows for a given gate to source voltage[6].For current to flow through the MOSFET a voltage is to be applied which biases the gate positive with respect to the source, thereby converting the silicon surface under the gate to be n-type channel that connects the source to the drain, Thus enabling the current to flow through the MOSFET [6].

The output characteristics of the MOSFET describes drain current (I_d) as a function of drain-source voltage(V_{ds}) with gate-soucre voltage(V_{gs}) as the parameter.The output characteristics can be divided in to three regions, Cutoff region, ohmic region and active region as shown in Figure 2.7.

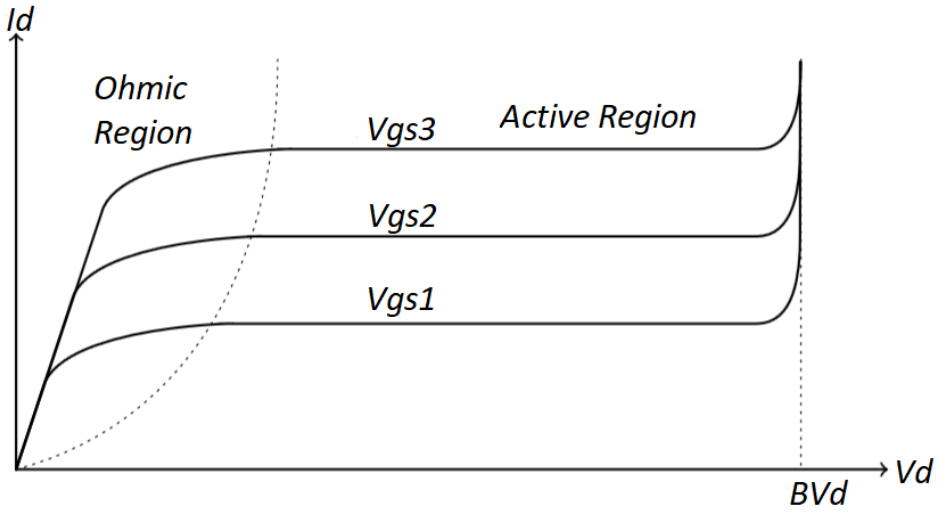


Figure 2.7: Output characteristics of a MOSFET

When the gate-source voltage(V_{gs}) is less than the threshold voltage ($V_{GS(th)}$) the MOSFET is in cutoff region. When the MOSFET is fed with a large gate source voltage (V_{gs}) it is said to be in ohmic region. In the active region the drain current(I_d) behaves like it has reached saturation and is dependent only on gate source voltage(V_{gs}). When V_d reaches a certain level, The MOSFET leaves the active region and an avalanche breakdown occurs. This is referred to as breakdown voltage(BV_d) and is the voltage rating of the MOSFET. In an inverter application during ON state it is desirable to operate the inverter in ohmic region due to low losses and in the active region during turn on and turn off [6].

2.3.2.1 Mosfet loss calculation

Since MOSFET is the switching device used in this project, the losses in it during the different operating stages is crucial to determine the overall efficiency of the inverter. The inverter is operated in four quadrant operation. The conduction losses through MOSFET and anti-parallel diodes can be elaborated through Table 2.1 and Figures 2.12,2.13,2.11,2.10

Table 2.1: Four quadrant operation for the inverter

4 quadrant operation				
No.	**Load V**	**Load I**	**Conduction**	**Sub-figure reference**
1^{st}	> 0	> 0	TA	(a)
2^{nd}	> 0	< 0	DA,TA	(b)
3^{rd}	< 0	> 0	DB,TB	(c)
4^{th}	< 0	< 0	TB	(d)

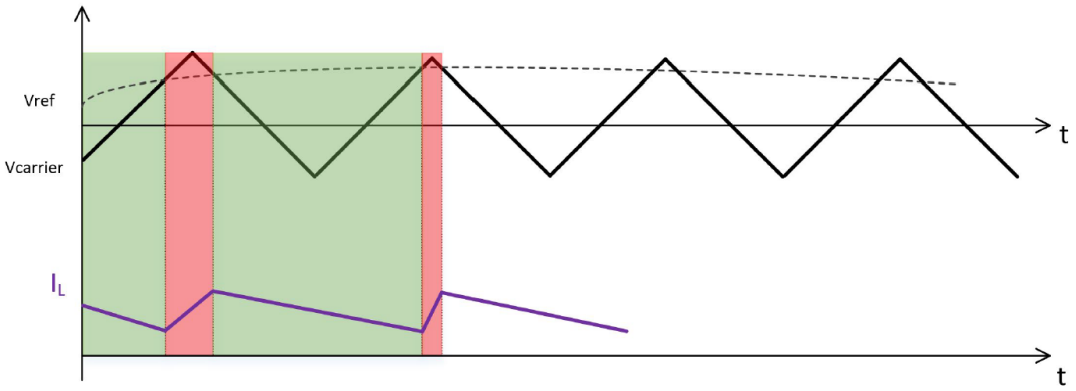


Figure 2.8: Illustrative figure of how the switching pattern is generated with reference wave,carrier wave and load current [7]

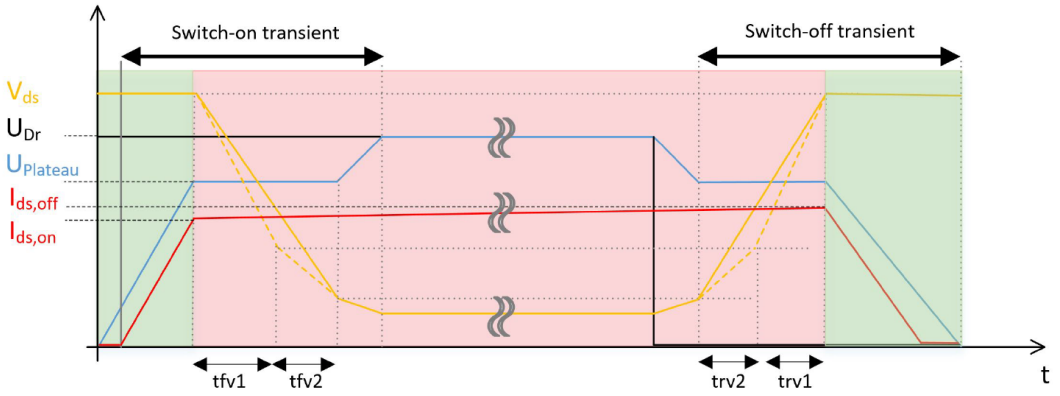


Figure 2.9: Zoomed in view of the turn-on and turn-off of mosfet switching, showing the drain-to-source voltage Vds, gate-to-source voltage Vgs, gate drive signal UDr and the drain-to-source current Ids[7]

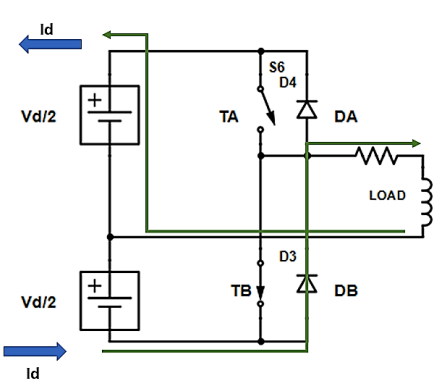


Figure 2.10: (a) Load voltage and current is positive

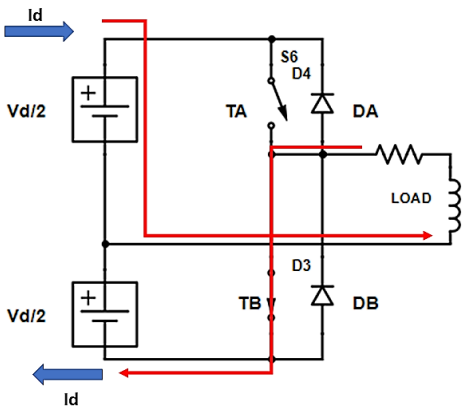


Figure 2.11: (b) Load voltage is positive and current is negative

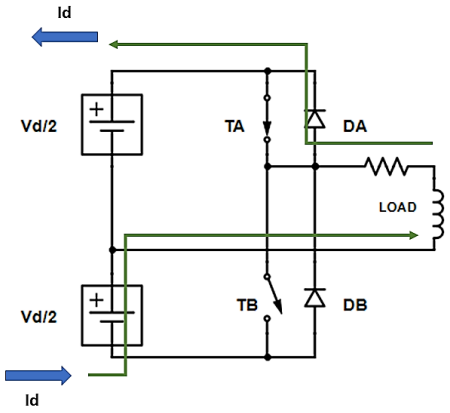


Figure 2.12: (c) Load voltage is negative and current is positive

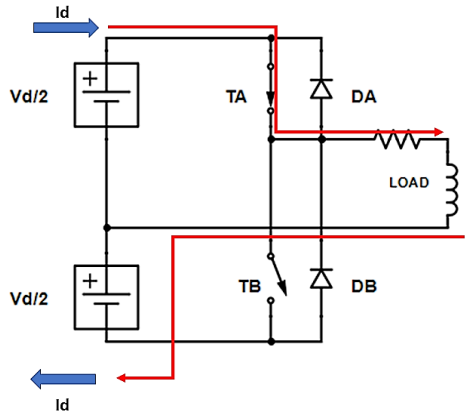


Figure 2.13: (d) Load voltage and current is negative

The losses in a MOSFET can divided into conduction losses and switching losses, the conduction losses in a MOSFET can be described using the expression [8]

$$P_{cond,M} = R_{ds,on} I_{ds,rms}^2 \tag{2.1}$$

where $R_{ds,on}$ is the on-state resistance of the transistor and $I_{ds,rms}$ is the RMS current through drain source of the MOSFET during one switching period [6].

The switching losses are more complex and can be calculated with the following expression, one for the MOSFET's switching loss and one for the anti-parallel diode

$$P_{sw,M} = (E_{on,M} + E_{off,M}) f_{sw} \tag{2.2}$$

$$P_{sw,D} = (E_{on,D} + E_{off,D}) f_{sw} \approx E_{on,D} f_{sw} \tag{2.3}$$

where $E_{on,M}$ is the MOSFET turn-on energy, $E_{off,M}$ is the MOSFET turn-off energy, similarly $E_{on,D}$ and $E_{off,D}$ are the turn-on and turn-off energy of the diode respectively. The $E_{off,D}$ can be neglected from (2.3) due to the fact that the majority of its loss is due to the reverse recovery in the diode, which can bee seen later that it is considered in the turn-on of the complementary MOSFET. The turn-on and turn-off energy of MOSFET can be written as

$$E_{on} = V_{ds} I_{ds,on} \frac{t_{ri} + t_{fv}}{2} + Q_{rr} V_{ds} \tag{2.4}$$

$$E_{off,M} = V_{ds} I_{ds,off} \frac{t_{ri} + t_{rv}}{2} \tag{2.5}$$

where V_{ds} is the DC supply voltage of 48 V from the battery. $I_{ds,on}$ and $I_{ds,off}$

are approximated to be the current flowing through one switch when it is on, these currents might differ a bit but they are assumed to be the same in the calculations here, hence $i_{ds,off} = I_{ds,on}$ [7]. Q_{rr} is the reverse recovery current through the diode, $_{ri}$, t_{fi}, t_{rv} and t_{fv} are the rise and fall times for current and voltage respectively. The current's switching times are given in the data sheet of the MOSFET whereas for the voltage rise and fall time it is calculated according to Figure 2.9 with the following formula,

$$t_{fv} = \frac{t_{fv1} + t_{fv2}}{2} \tag{2.6}$$

$$t_{fv1} = (V_{ds} - R_{ds,on} I_{ds,on}) R_g \frac{C_{gd1}}{(U_{Dr} - U_{plateau})} \tag{2.7}$$

$$t_{fv2} = (V_{ds} - R_{ds,on} I_{ds,on}) R_g \frac{C_{gd2}}{(U_{Dr} - U_{plateau})} \tag{2.8}$$

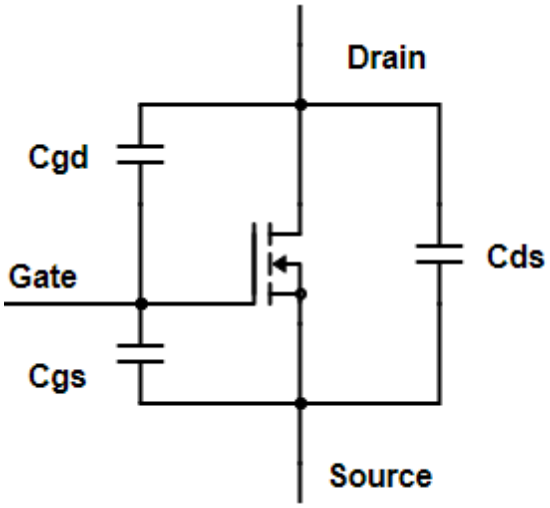


Figure 2.14: Schematic of the n-channel MOSFET

where U_{Dr} is the voltage of the gate signal of 10V, C_{gd1} and C_{gd2} are the gate drain capacitance for the blocking voltage of 48 V which can be calculated using the following relation

$$c_{gd1} = C_{rss} \tag{2.9}$$

$$C_{gd2} = C_{iss} - c_{gd1} \tag{2.10}$$

where C_{rss} and C_{iss} are the reverse transfer capacitance and input capacitance respectively which can be found from the data sheet of the MOSFET.The $R_{ds,on} I_{ds,on}$ gives the onstate voltage drop. R_g is the gate resistance and $U_{plateau}$ is the clamped voltage level where the miller effect takes place. For some transistors, this parameter is given in its data-sheet but for other it need to be calculated. Equation (2.7), which gives the t_{fv}, is a two-point approximation due to the complex dependency of

the non-linear gate-drain capacitance during turn-on, as well as for turn-off. This calculation combined with the fact that the drain-source voltage is assumed to have linear form, give the worst-case analysis for switching losses calculation.

$E_{on,D}$ is the diode tun-on and can be calculated as

$$E_{on,D} = \frac{1}{4} Q_{rr} U_{D,rr} \tag{2.11}$$

where $U_{D,rr}$ is thew voltage across the anti-parallel diode using the reverse recovery, it can be approximated to be equal to the supply voltage of V_{ds} for the worst case scenario.
Voltage rise time is calculated using the following formula,

$$t_{rv} = \frac{t_{rv1} + t_{rv2}}{2} \tag{2.12}$$

$$t_{rv1} = (V_{ds} - R_{ds,on} I_{ds,on}) R_g \frac{C_{gd1}}{U_{plateau}} \tag{2.13}$$

$$t_{rv2} = (V_{ds} - R_{ds,on} I_{ds,on}) R_g \frac{C_{gd2}}{U_{plateau}} \tag{2.14}$$

where $U_{plateau}$, R_g, C_{gd1} and C_{gd1} are the same as in (2.7) and (2.8). Summing up the overall switching losses can be calculated as the sum of switching losses in MOSFET and Switching losses in Anti-parallel diodes for one switching cycle

$$P_{total} = P_{sw,M} + P_{sw,D} \tag{2.15}$$

2.4 DC link Capacitor Design

In a three phase inverter a DC Link capacitor,C is used as shown in Figure 2.2. The role of the DC link capacitor is to maintain a stiff DC voltage across the power supply. Placing the DC link capacitor close to the switches helps in reducing the stray inductance and improving the switching behaviour. The DC link capacitor must be designed to be able to withstand ripple current.The desired DC link capacitor can be determined using the following formula, [9]

$$I_{avg} = \frac{3}{4} I_{a,peak} m_a cos(\phi) \tag{2.16}$$

$$I_{c,rms} = I_{a,rms} \sqrt{[2m_a(\frac{\sqrt{3}}{4\pi} + cos(\Phi)^2(\frac{\sqrt{3}}{\pi} - \frac{9}{16} m_a))]} \tag{2.17}$$

$$C_{dc} = \frac{0.7(I_{a,peak} - I_{dc}) m_a}{V_{dc,pk-pk} f_{sw}} \tag{2.18}$$

where f_{sw} is the switching Frequency, $\Delta V_{pp} max$ is the maximum allowed ripple volt-

age and I_0 is the peak output phase current.

To calculate the power loss in a Capacitor bank it is necessary to know the ESR of the capacitor bank. To calculate the ESR value the dissipation factor which is mentioned the data-sheet of the capacitor is used along with the following formula,

$$ESR = \frac{tan\delta}{2\pi fC} \tag{2.19}$$

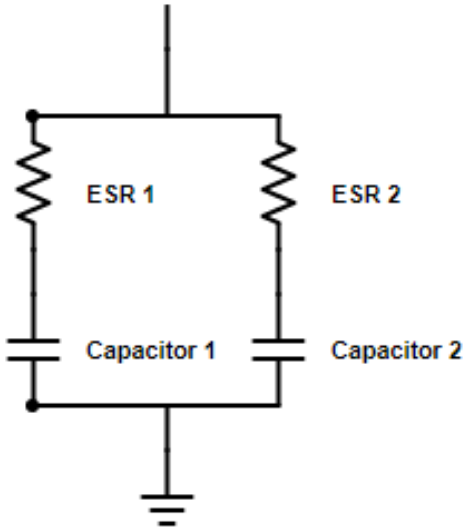


Figure 2.15: Schematic of ESR in capacitor

$$P_C = R_C I^2_{c,rms} \tag{2.20}$$

where P_C is the Power loss in Capacitor, R_C is the ESR resistance of the capacitor and $I_{c,rms}$ is the RMS current through the capacitor which is calculated using (2.17).

2.5 PCB Thermal Loss Estimation

The Thermal model of the PCB power dissipation can be described in terms of equivalent circuit of Thermal resistance of each layer of the PCB in terms of (°C/ W). The different layers of the PCB can be seen in Figure 2.16

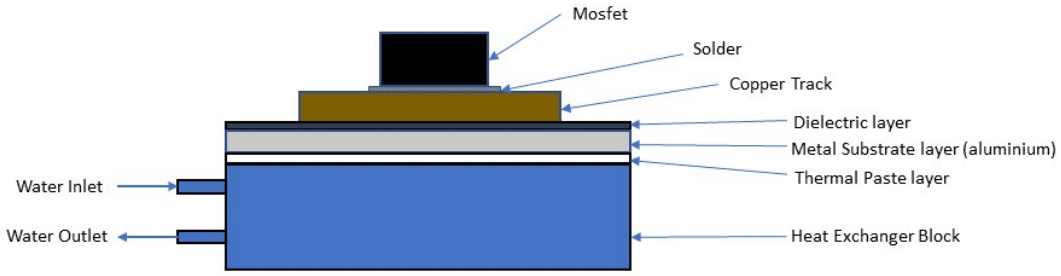


Figure 2.16: Layers of PCB

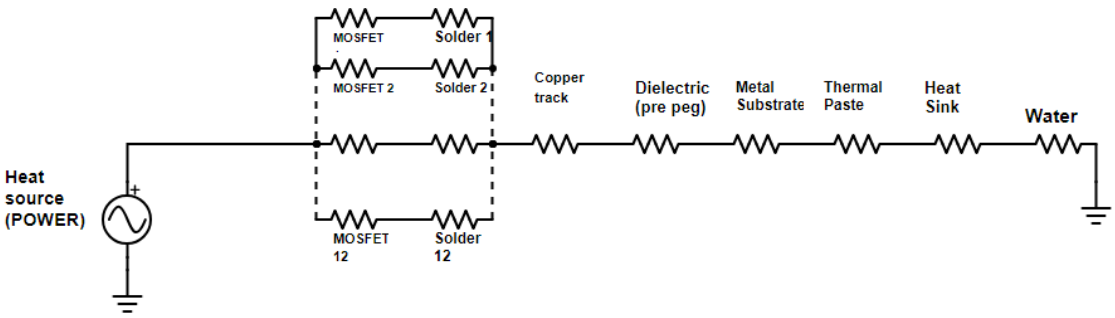


Figure 2.17: Thermal model

The temperature distribution through the PCB can be found using the simplified Thermal model shown in Figure 2.17. The thermal resistance of all the MOSFETS and Solder for each MOSFET are assumed to be in Parallel to full heat source which is calculated as the overall losses. The following simplifications are made to design the rest of the thermal circuit components.

- For simplicity the Dimension of the Track is assumed to be the same as the dimension of the PCB itself
- Pre-preg is the dielectric layer in between the copper tracks and the metal substrate. This is also assumed to be the same dimension as that of the PCB. The thickness is defined by the PCB manufacturer. Which is 0.15mm in this case.
- The Metal substrate also has the same dimension of the PCB. The thickness is 2mm which is the standard.
- The thermal paste is applied between the PCB and the Cooling plate (Heat sink). Hence it is assumed to have the same dimension of the PCB, the thickness of thermal paste is assumed to be as per general standards.
- The Heat sink dimension's are as per the manufacturer specification.

The other layers of the PCB like the Copper track, Dielectric Layer, Metal substrate, Thermal paste, Heat sink and Water thermal resistance are assumed to in

series with the Heat source.

The steady state temperature of the MOSFET can calculated using the expression

$$T_j = P_{tot}(R_{th,jc}+R_{th,solder}+R_{th,copper}+R_{th,die}+R_{th,Metal}+R_{th,cp}+R_{th,hs})+T_w \quad (2.21)$$

where P_{tot} is the Total power loss in the inverter, $R_{th,jc}$ is junction to case thermal resistance of the MOSFET,$R_{th,solder}$ is thermal resistance of the solder used to solder the MOSFET to the PCB, $R_{th,copper}$ is the junction to case thermal resistance of the PCB copper track, $R_{th,die}$ is the junction to case thermal resistance of the Dielectric material which the T-prepreg in this case between the Copper layer and the Metal substrate layer, $R_{th,Metal}$ is the junction to case thermal resistance of the Metal substrate layer(Aluminium in this case), $R_{th,cp}$ is the junction to case thermal resistance of the cooling paste applied between the Metal substrate layer and the Heat ex-changer (heat sink), $R_{th,hs}$ is the junction to case thermal resistance of the heat ex-changer block (heat sink) and T_w is the inlet water temperature. The heat is mainly produced by the MOSFET's and PCB tracks. Since the MOSFET's are close to each other there will be some mutual transfer of heat between the MOSFET's and the PCB track. This mutual transfer of heat is not Theoretically calculated due to the lack of time.

2.6 Calorimetric Measurements

Calorimetry is a technique to measure the amount of heat exited or absorbed during operation of the test object. The aim is to obtain a more accurate result from measurements by measuring losses as heat dissipated from the test object. A calorimetric setup could consist of a thermally insulated container filled with fluid, a thermometer for monitoring temperature and a device for stirring the fluid [10]. Calculations from calorimetry hinge on the first law of thermodynamics, which states that energy cannot be created or destroyed. Applied to calorimetry, this means that any heat produced during the operation of a test object must be transferred to the calorimetric liquid or, more specifically, to the heat ex-changer. Therefore, if we can measure the heat absorbed by the heat ex-changer, then we know the amount of heat given off by the test object. Test objects in this project is the inverter. The total power loss can be calculated as

$$P_{loss} = P_{Hex} + P_{wall} + P_{stray} - P_{fan} \quad (2.22)$$

P_{stray} and P_{fan} are neglected in our calculations as there is no circulation fan inside the box and stray losses are assumed to be zero.

- Power loss at walls of the box (P_{wall})

$$P_{wall} = \frac{T_{test} - T_{amb}}{R_{thwall}} \quad (2.23)$$

$$R_{thwall} = \Sigma \frac{d_{wall}}{\lambda_{wall} A_{wall}} \tag{2.24}$$

where,
T_{test}- Temperature of Test object
T_{amb} - Temperature of ambient
R_{thwall} - Thermal Resistance of the wall
λ_{wall} - Thermal conductivity of material
A_{wall} - Area of wall

- Power loss at Heat ex-changer (P_{Hex})

$$P_{Hex} = C_p V \rho \Delta T \tag{2.25}$$

where,
C_p- Specific heat capacity of Fluid
V - Flow rate
ρ - Mass density of fluid
ΔT - Temperature rise between inlet and outlet Temperature

Using these set of formulas, the power loss in the test object can be calculated thermally.

2.7 COMSOL Simulation

COMSOL multiphysics is a modeling environment that is used to solve scientific and engineering problems described as partial differential equations(PDE). Using this software multiphysics studies can be carried out. Physical parameters like material characteristics, loads, power supply, heat source, etc can be set for each model. COMSOL multiphysics processes the modified PDE without programmer's knowledge of mathematics and numerical analysis [11].COMSOL can be used in various domains like acoustics,biology,heat transfer,electromagnetism,fluid mechanics,diffusion,etc.

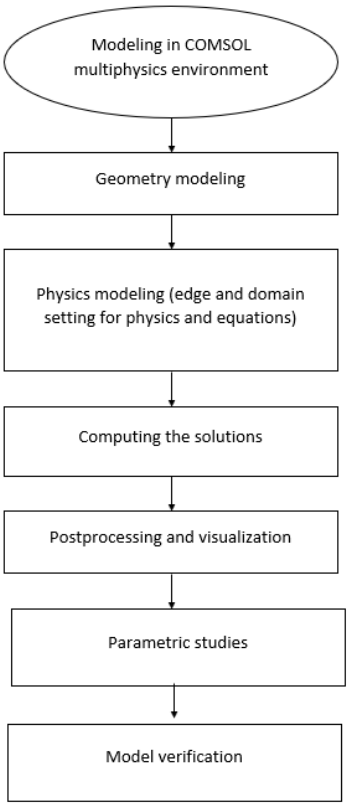


Figure 2.18: Flow of COMSOL modeling

3

Case Setup

3.1 Machine Parameters

The machine for which this inverter is designed is a 48V and 50kW peak power traction motor designed for a commercial vehicle application [12]. Since this power level is too high for this project, the inverter is designed by downsizing the machine to 20kW peak power and 10kW continuous power. The machine parameters are shown in Table 3.1

Table 3.1: Machine Parameters

Parameters	**50kW machine**	**units**
pole pairs	5	-
DC bus voltage	48	V
Peak power	50	kW
Maximum speed	12000	RPM
Base Speed	4500	RPM
Peak Torque	110	Nm

3.2 Inverter Topology

A traditional three phase inverter topology, which was presented in Figure 2.2 was chosen in this project. Since the power level is high, paralleling of the MOSFET's was chosen. Also, using MOSFET's gives the possibility to a use higher switching frequency for operation which helps in reducing the DC bus capacitors.

3.3 Gate driver and Control circuit

The gate driver circuit is designed using UCC27201ADDA IC as it is capable of driving both High and low MOSFET's using a single IC and also possible to drive two MOSFET's in parallel, It can be seen in Figure 3.2. A micro-controller from Texas instruments, the C2000 family, model TMS320F28379D LaunchPad is adopted to generate PWM signal of the required switching frequency of 100 kHz. Simulink blocks are used to generate the PWM signal in the form of C language code. This is then executed in Code Composer Studio 6.2.0, a recommended software which is used to link the micro-controller with a computer in order to achieve the required PWM signal to drive the MOSFET's. A Pre-Gate drive board as can be seen in Figure 3.1 was designed so that the LaunchPad could be just mounted on it for a neater and simpler solution. This Pre-gate driver board also had the Under voltage and over voltage protection to prevent damages. In order to have more control over the live variation of the modulation index ADC (Analog to digital) interrupt was

used where an external variable resistor was used as an ADC input to vary the modulation Index.

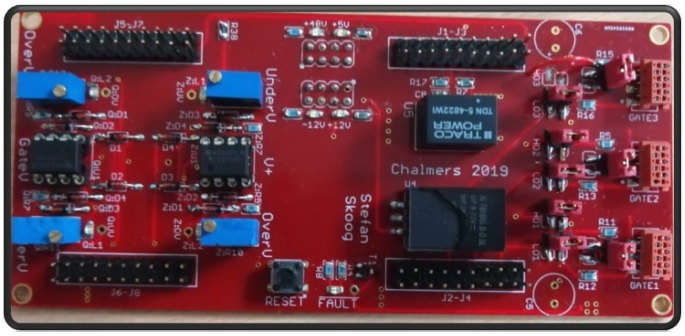


Figure 3.1: Pre-Gate Driver Board

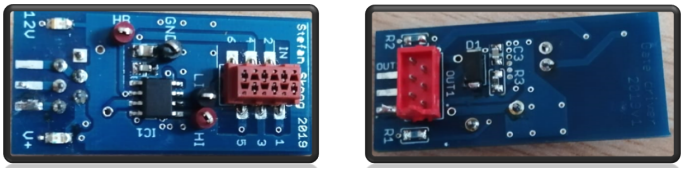


Figure 3.2: Gate Driver Board

3.4 Design of Inverter

To design a three phase inverter for such a high power rating, it is very important to consider certain design aspects. The following design aspects were mainly considered while designing the inverter.

1. Selection of Switching Device
2. Type of Printer Circuit Board(PCB)
3. DC link Capacitors
4. Copper track thickness
5. Gate Driver

3.4.1 Selection of Switching Devices

The first step in designing the inverter is to decide which kind of switching device is to be used based on the load requirement and various other parameters. The are two main options for switching devices are MOSFET and IGBT. Since the operating voltage is very low and the switching frequency is very high (100kHz), it is decided to go with MOSFET's over IGBT's. Generally IGBT's work at higher voltage and lower switching frequency. It was better to use MOSFETS for this application. There were two different options in MOSFETS as well. As the peak current demand is very high it is decided to use two MOSFET's in parallel so that it can handle the High currents. Table 3.3 shows the different MOSFETS found in the market based on the requirements of this project. It is chosen to use IAUT300N10S5N015 MOSFET for this thesis as it has the lowest R_{dson} compared to the other MOSFETs, which would result in a lower power loss.

Table 3.2: Parameters for building the Inverter

Parameters	Value	Units
DC Voltage	48	V
Input Current	430	A

Table 3.3: MOSFET options

Part No.	Manufacturer	Type	V_{ds}	I_{dson}	R_{dson}
FDBL86062F085	ON Semiconductor	SMD(H-PSOF)	100V	300A	2mΩ
CSD19536KTT	Texas Instruments	SMD(TO-263-3)	100V	272A	2.4mΩ
IXFT320N10T2	IXYS	SMD(TO-268-3)	100V	320A	3.5mΩ
MMIX1F420N10T	IXYS	SMPD-24	100V	334A	2.6mΩ
IAUT300N10S5N015	**Infenion**	**HSOF-8-1**	**100V**	**300A**	**1.5mΩ**

3.4.1.1 Type of PCB

Once the MOSFET was selected it was necessary to decide which type of PCB we would use to manufacture the inverter. There are different kinds of PCB's. Figure 3.3 shows the different types of PCB's available in market

1. Single sided PCB
2. Double sided PCB
3. Multi layer PCB
4. Insulated Metal substrate(IMS) PCB

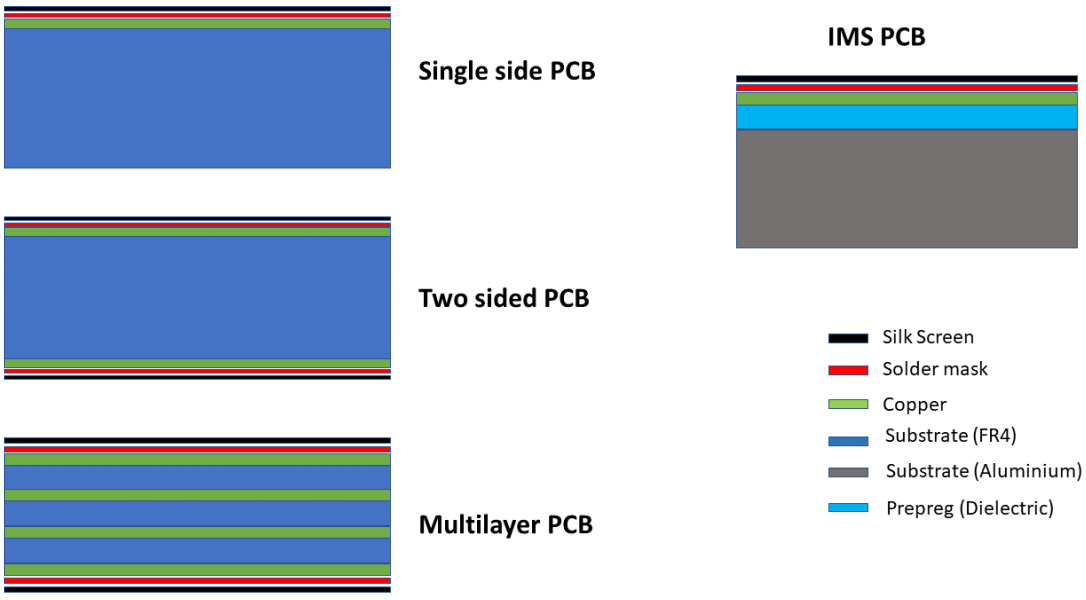


Figure 3.3: Types of PCB's

Since it was chosen to use surface mounted MOSFET's the best way of cooling theses were only by using IMS PCB boards. The IMS PCB has an aluminium layer as the base instead of FR4, over which a thin layer of dielectric (prepreg) is placed and

over this prepreg the copper tracks are made. Where as in a normal PCB the base layer is a thinner FR4 layer over which the copper tracks are made. This concept of having Aluminium substrate helps in providing better cooling for surface mounted components. Hence an Aluminium substrate PCB was used in this thesis project.

3.4.1.2 DC link capacitors

The next step after deciding the PCB is to decide which type of capacitors that will be used for the DC link. Non polarised MLC (Multi-layer ceramic chip) capacitors have a lower ESR [13] which helps in reducing the losses. Also the stray inductance's can be reduced by placing these capacitors very close to the MOSFET's. Based on the calculations in Section 4.2 the following capacitors were shortlisted as can be seen in Table 3.4 and out of these the (C5750X7S2A226M280KB) capacitor was selected because it is close to the requirement and was available in the market. Using the equations from Section 2.4 it is calculated that the needed capacitance was 331.3 μF. This is achieved by using 45, 22μF capacitors in parallel as the effective capacitance of these 22 μF at 50V is only 8.8 μF, This can be seen from Figure 3.4 which is provided by the capacitor manufacturer. The peak to peak voltage ripple is expected to be within 5 percent by using this DC link Design.

Table 3.4: Capacitors considered

Part No.	Capacitance	Effective cap.	ESR
CKG57KX7S2A156M335JJ	15μF	14.4μF	5.16 mΩ
C5750X7S2A156M250KB	15μF	14.36μF	3.156 mΩ
C5750X7S2A226M280KB	**22μF**	**21μF**	**2.119 mΩ**
C5750X7S2A106K230KB	10μF	9.38μF	4.52 mΩ

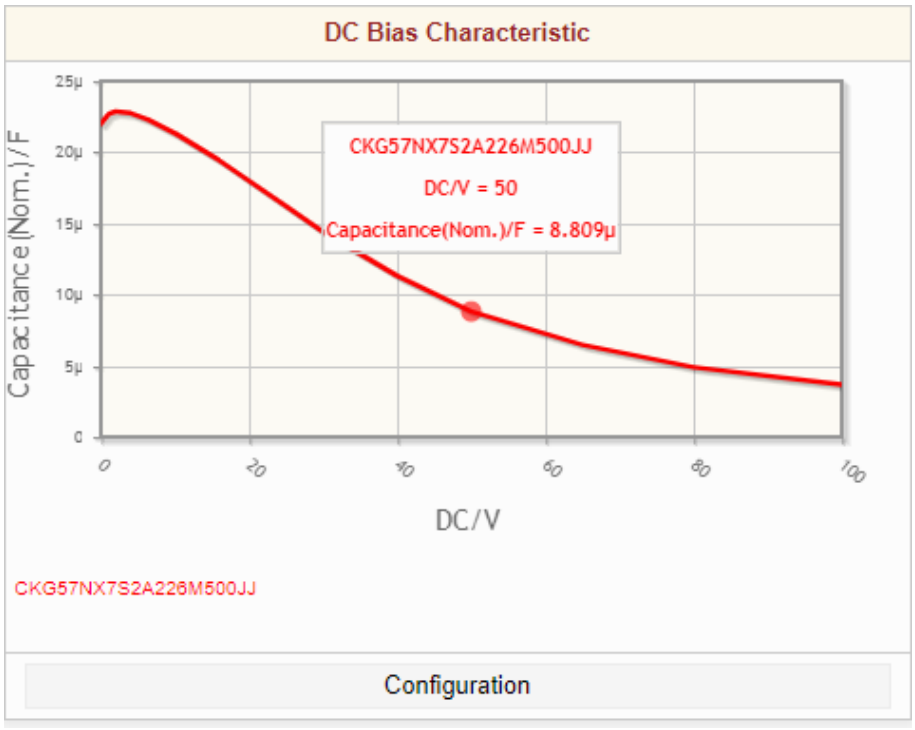


Figure 3.4: Capacitance value vs voltage

3.4.1.3 Copper track Thickness

Due to the very high current required by the input specification, the copper track thickness needs to sized accordingly. The thickness of copper needs to be as high as possible so that the power loss in the track can be reduced. Table 3.5 shows the different copper track thicknesses available in the market for IMS PCB.

Table 3.5: PCB track thickness

oz/ft^2	0.5	1	2	3	4
μm	17.5	35	70	105	140

According to calculations most appropriate copper thickness is 4oz/ft^2 (140mum). But due to the unavailability of the this copper thickness with the manufacturer (PCB Way) it is decided to use 3oz/ft^2 copper tracks instead. It is discussed in the Section 4.1.3 about the losses in the tracks for the different thickness and how it was managed to reduce the losses in the PCB by soldering extra copper wire to the DC+ track which would increase the area and consequently reduce the resistance and losses in the PCB tracks.

3.4.1.4 Gate Driver

The Gate driver design is a key factor in the overall inverter design to make it efficient. Since the gate Driver design was not a part of the project scope initially, it was planned to use the gate driver designed for last year's thesis [7]. But once the PCB was ready and tested with the gate driver it was seen that there was a lot of

ringing and distortions due to the stray inductance caused by the long cable length between the driver circuit and the Mosfet. It is discussed in Section 5.3.1. So it was decided to design and manufacture smaller individual gate driver for each phase which could be connected very close to the Mosfet's. Help was sought from Stefan Skoog to design the Gate Driver PCB.

3.5 Work approach

To effectively complete the project on time the following work approach procedure was followed.

- Selection of components based on requirement (Machine parameters)
- Designing of the Theoretical loss model considering the Mosfet loss,track loss, DC link loss and gate driver loss.
- Designing the PCB
- Designing and simulating the Thermal Model of the Inverter PCB in COMSOL Multi-physics
- Build test boards to test driver circuit and parallel MOSFET operation
- Manufacturing of PCB
- setup the cooling circuit
- Testing of the Actual PCB with different loads
- Temperature measurements
- Efficiency calculations
- Comparison of Theoretical and practical values

3.6 Case Setup's

Multiple test circuits were made to test the Driver circuit, parallelling of MOSFET and finally a test circuit was made using the actual MOSFETs, to check the magnitude of the turn ON and turn OFF ringing. The different test circuits build are discussed below.

3.6.1 Case Setup 1

Test Circuit 1 was a single leg circuit that was made with the standard TO-220-FP package MOSFET (IPA045N10N3 G) which has a maximum I_D current of 64 A and an R_dson of 4.5 mΩ. This was made basically to test the Gate Driver circuit. The circuit was made in such a way that the Existing gate driver could be directly connected to operate the MOSFETs, without modifying the Gate driver PCB. The circuit can be seen in the Figure 3.5.

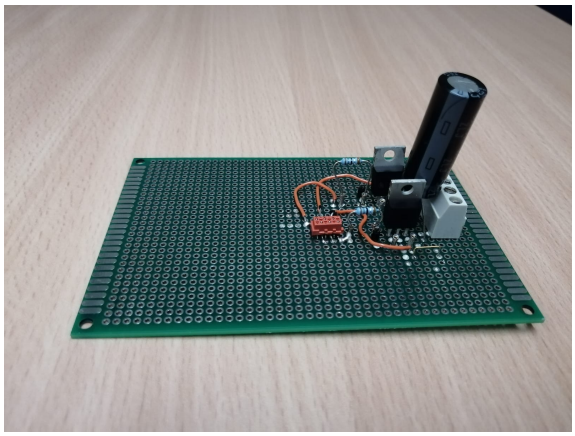


Figure 3.5: Case setup 1- Single leg circuit to test gate driver

3.6.2 Case Setup 2

Test Circuit 2 as seen in Figure 3.6 was made to test the parallel MOSFET operation with the existing gate driver circuit. The same MOSFETs as used in the first test case was used. Again, only a single leg circuit with two MOSFETs in parallel was built for testing.

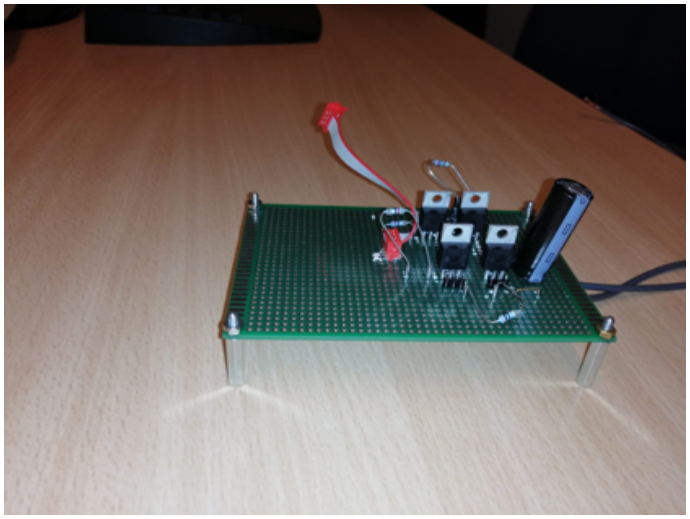


Figure 3.6: Case setup 2 - Single leg with parallel MOSFET's

3.6.3 Prototype Inverter PCB

Taking all the Design aspect as discussed in Section 3.4 into consideration multiple PCB designs were made and finally after a lot of fine tuning the PCB as shown in Figure 3.7,3.8 was designed using Altium PCB Designer software and manufactured.

3.6.3.1 Design process

While designing the inverter PCB the most important precaution to be taken is the Placement of the DC link as close as possible to the MOSFET's, the more the distance between the capacitor increases more will be stray inductance and cause

a lot of ringing. The other constrains strictly followed is to keep the gate driver at a minimum distance from the MOSFET. To fix this issue, small individual gate driver PCB were designed which would be directly mounted on the power board using connectors. Since it was decided to manufacture individual gate drivers, there was a need to design a new control and protection circuit. Texas Launch XL was decided to be used to generate the PWM switching signals for the gate drivers. To make things look compact and reduce the number of jumper wires, a pre-gate driver PCB is designed. This pre-gate driver PCB has the protection circuits and also was designed in such a way that the Texas Launch XL controller could be directly mounted on it. The pre-gate-driver was connected to the gate-drivers using patch cables. The power to drive the controller, gate driver and protection circuits were taken from the inverter power board through the gate driver. This reduced complexity and the need to use additional external power supplies. Figure 3.9 show the Gate driver boards(blue PCB's), Power board (white circular PCB), Pre-gate driver PCB (red PCB).

3.6.3.2 Manufacturing process

The PCB's were sent to PCB manufacturers to be manufactured. Since all the components of the power board are SMD components, reflow over soldering was used to solder the components to the PCB. This process is quite easier compared to the conventional hand soldering, especially for the SMD components. The gate driver PCB and pre-gate driver PCB's were hand soldered. The PCB's were checked under a microscope to see that there is no bridging of solder anywhere.

3.6.3.3 Difficulties encountered

There were several problems faced while trying to fix the PCB when some problem occurred. While trying to de-solder one of the MOSFET when found broken, it was a very difficult task as the PCB was an IMS PCB. The only way to de-solder the MOSFET was by heating the MOSFET from the top and bottom of the PCB with a hot air gun at 400 degree Celsius for almost 2 minutes constantly. The following problems were encountered.

1. The Entire PCB started getting too hot causing difficulties to handle the PCB
2. Connector close to the MOSFET started to melt as it was made out of plastic and is not designed to handle the high temperature.
3. The capacitors near the MOSFET also started to get de-soldered.
4. Some damage was done to the dielectric layer as proper precautions were not taken the first time during de-soldering.

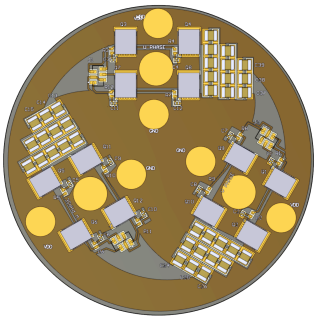


Figure 3.7: Altium PCB design

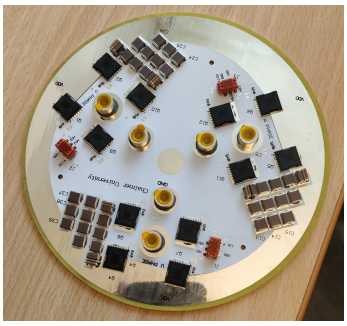


Figure 3.8: Prototype PCB

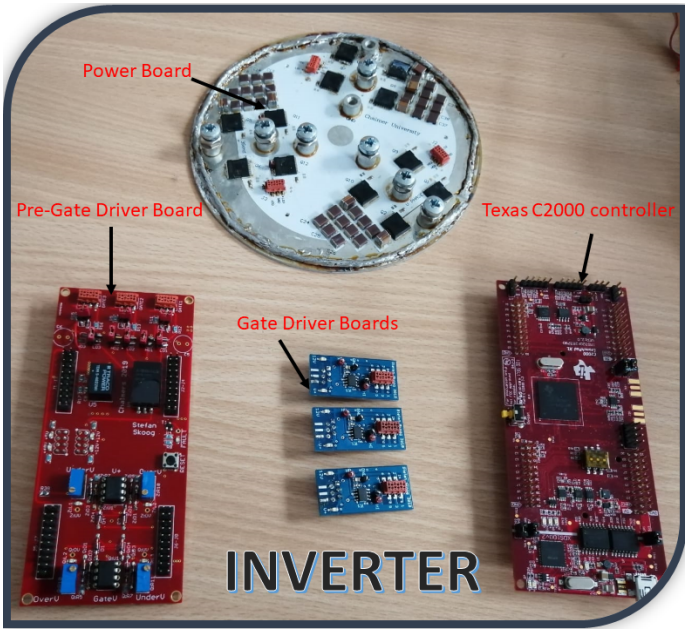


Figure 3.9: Inverter PCB's

3.7 Cooling system

The Cooling system was custom made by using locally available components. Water is used as the cooling fluid. The following were the main components in the cooling system are shown in Table 3.6. The actual setup can be seen the Figure 3.10

Components	Ratings/Dimensions
Cooling Plate	21cm*21cm
Water Pump	24V
Radiator Fan	24V
Temp Sensor	PT100

Table 3.6: Cooling system components

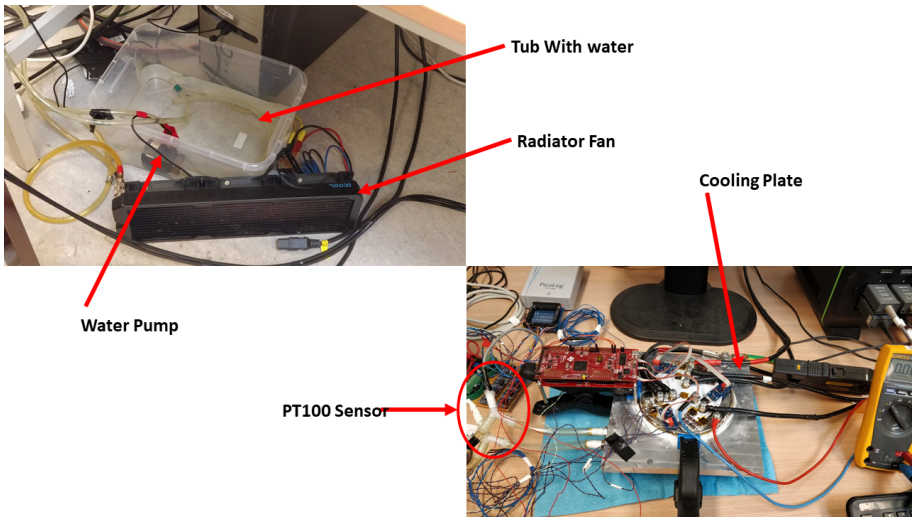


Figure 3.10: Cooling system

3.8 Measurement Bench Setup

The power level to be reached in this project was around 20kW. But since there were no loads available at 48V a step-up transformer of 48V to 380V was used. Three phase resistive load and Heating element were connected to the secondary side of the transformer as load. The Measurement setup (Bench Setup) which can be seen in Figure 3.11 can be depicted as a block diagram as can be seen in Figure 3.12 where the Input voltage and current is measured directly after the power supply. The output was measured after the cable, since it was easier to connect the measurement probes rather than connecting them directly on the PCB.

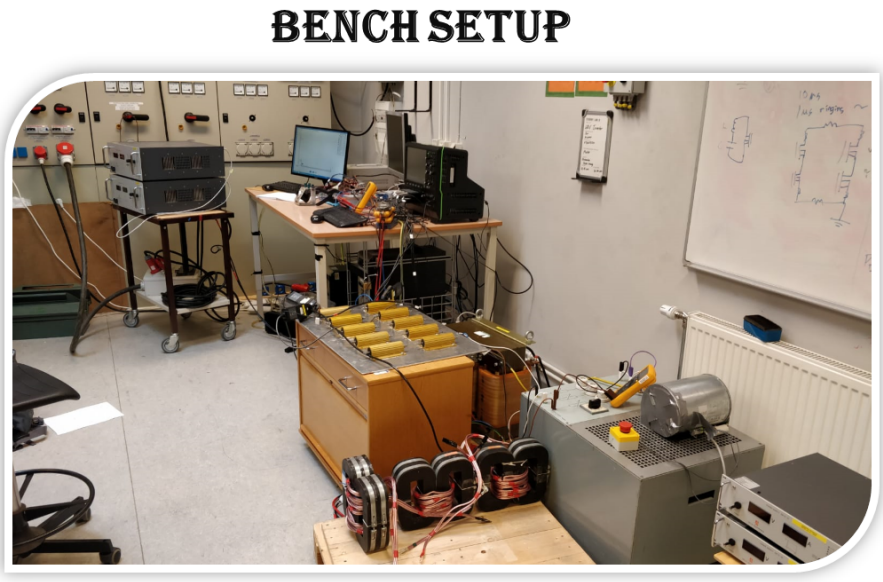


Figure 3.11: Bench Setup

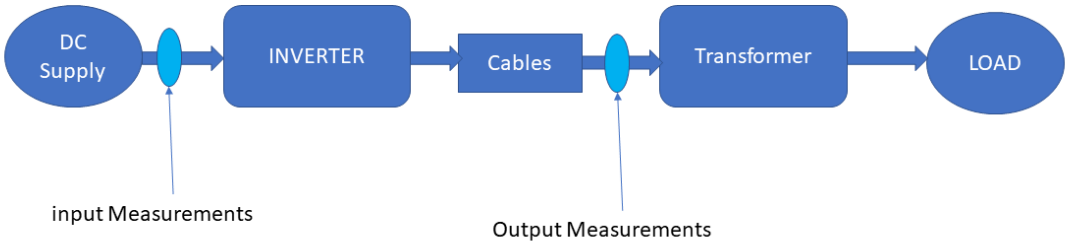


Figure 3.12: Bench Block diagram

3.9 Measurement Instruments

The different instruments that are used to setup the measurement rig are discussed in this section.

3.9.1 LeCroy Oscilloscope

The LeCroy MDA800A as seen in Figure 3.13 is used for the voltage and current measurements in that project. This is an 8 channel oscilloscope with inbuilt motor drive analyzer, hence it can measure the Three phase voltages and currents and also the DC input voltage and currents to give the overall efficiencies other important information's. It has an accuracy of ±1% based on the probes used [14].

Figure 3.13: LeCroy Oscilloscope

3.9.2 LeCroy Voltage Probes

Differential voltage probes are used as the voltage magnitude between two different potential points needs to be measured. The differential probe used is AP032. It has an accuracy of ±2% [15]. Figure 3.14 shows the differential probes used in this project.

Figure 3.14: Differential Probe

3.9.3 LeCroy Current Probes

The current probe used for this project is CP500 since the maximum expected current is 420A. This has good accuracy with a maximum error of 1% [16]. Figure 3.15 shows the current probes used in this project.

Figure 3.15: Current Probe

3.9.4 DC Power Supply

Two SM30-200 (6kW) were used in series to achieve 200A of current and 48V voltage. The two supplies are connected in series and made to work in master slave configuration. [17]. Figure 3.16 shows the power supply used.

Figure 3.16: DC Power Supply

3.9.5 Transformer

There was a need to step-up up the output voltage as most of the load's available were designed for higher voltages. Hence a 37V/400A to 370V/40A step-up transformer is used. The primary side in connected in delta connection to the output of the inverter and secondary side is connected in star connection to the 3 phase load. Figure 3.17 shows the step-up transformer used in this project.

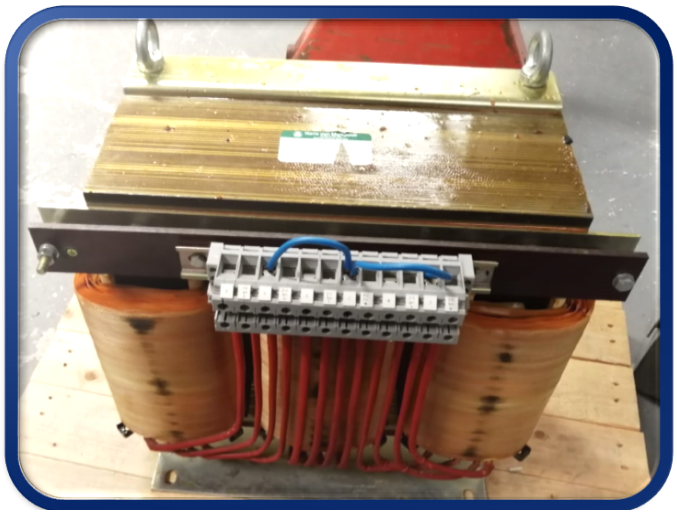


Figure 3.17: Step-Up transformer

3.9.6 Loads

Two different loads are used in this project. They are

- Three Phase Resistive Load (3kW)
- Heating Element Load (9kW)

Initially the 3kW loads are used for the initial lower power operating points. Later for higher powers the 9kW heating element load are used. Figure 3.18 shows the 9kW heating element load and Figure 3.19 shows the 3kW three phase resistive load used in this project.

Figure 3.18: 9kW Heating Element

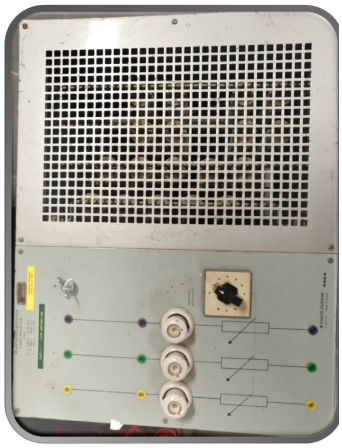


Figure 3.19: 3kW Resistive load

3.9.7 PicoLog Data Logger

PicoLog 1216 data logger is used to measure and record the water temperatures and the temperatures of the Mosfet's. Two different sensors were used to measure the temperatures directly.

- PT100 Sensor
- Two wire Thermocouple

The PT100 sensor was used to measure the inlet and outlet water temperatures. PT100 temperature sensors have a accuracy of 0.3 ° C (Class B). To measure the Mosfet temperature the two wire thermocouple's are used. These thermocouple's generally have an accuracy of ±0.01 ° C. Figure 3.20 shows the PicoLog data logger used in this project to record the temperature readings.

Figure 3.20: PicoLog Data Logger

4

Theoretical Results

4.1 Theoretical Loss calculation

This section covers the selection of DC link capacitor,loss in the capacitor and MOSFET, also discusses about the various other losses in PCB such as the track loss.

4.1.1 Mosfet loss calculations

The MOSFET losses during switching and conduction is calculated using the formulas discussed in Section 2.3.2.1. The losses in the MOSFET at 100kHz and 50kHz switching frequency considering a peak RMS Phase current of 420 A through each phase of the inverter are as mentioned in Table4.1
$I_{ph,rms}$ = 420 A
$R_{ds,on}$ = 0.0015/2 Ω
The Resistance is considered to be half of the actual resistance since two MOSFET'S are considered parallel here and assumed to operating perfectly at the same time.

Table 4.1: MOSFET losses at 100kHz and 50kHz

Frequency	**MOSFET Conduction (W)**	**MOSFET Switching (W)**
100kHz	1026	82.4
50kHz	1026	41.2

4.1.2 DC Link capacitor bank Losses

The DC Link capacitor bank values is calculated using the formulas as discussed in the Section 2.4 . The capacitors values for different frequencies are mentioned in the Table 4.2 and Figure 4.1.

Table 4.2: DC link Capacitor bank and Losses

Frequency (kHz)	**Total Capacitance required (μF)**	**Capacitor selected (μF)**	**Nominal capacitance at 48V**	**No of Cap. used**	**Actual Capacitance value (μF)**
100	331.3	22	8.809	45	**396.4**
50	662.5	22	8.809	76	**669.5**

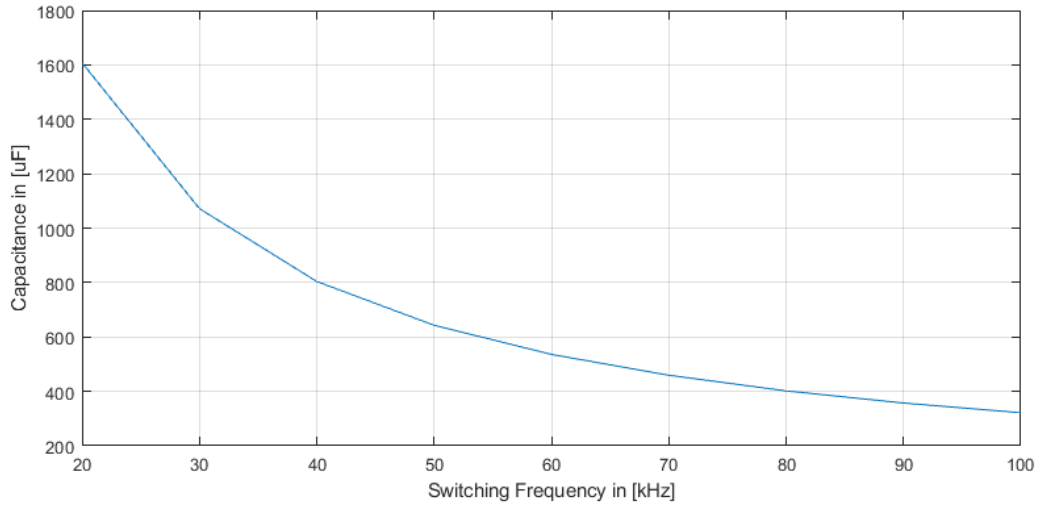


Figure 4.1: Capacitor bank values for different Frequencies at 100V

The capacitor loss is calculated using Peak RMS current value of 420 A. The Capacitor losses are shown in Table 4.3

Table 4.3: DC link Capacitor bank and Losses

Frequency (kHz)	**ESR (mΩ)**	**No of Cap. used**	**Total ESR (mΩ)**	**Losses (W)**
100	5.044	45	0.112	**19.8**
50	5.532	76	0.073	**12.84**

4.1.3 Losses in PCB Tracks

The losses in the PCB due to the copper tracks and connectors also contribute the the overall efficiency of the Inverter. The track is made of copper hence the losses can be calculated using the formula

$$P_{track} = R_{track} I_{rms}^2 \tag{4.1}$$

Where 'R$_{track}$' is the resistance of the track and 'I$_{rms}$' is the RMS current flowing through the track. The Resistance on the copper track depends on the length and Area of copper, this can be calculated using the formula

$$R_{track} = \frac{\rho l}{A} \tag{4.2}$$

From the Design of the PCB as shown in the figure the length and area of copper is calculated to determine the losses in the PCB tracks. It can be seen from the figure that the three legs are at 120 degrees angles from each other. To simplify the tracks can be divided into two parts

- DC+ track
- Phase output track
- DC- track

Using this information and the measurement's made form the design the losses are calculated, assuming that the maximum I$_{rms}$ current is 420 A. But as can be seen

from the Figure 4.2 there are three DC+ and DC- entry into the PCB, Thus an assumption is done on how much current the Track will carry. The assumptions are as follows

- DC+ track each segment between two half bridge is expected to carry only around 30% of the I_{rms} current. Thus Current through DC+ track is 126 A
- The DC- track also like the DC+ track is expected to carry around 30% of the I_{rms} current. Thus Current through DC- track is 126 A
- Each Phase track is expected to carry the entire I_{rms} current. Thus Current through Phase track is 420 A
- Also since the DC+ track is split into three sectors. The length of DC+ track used in calculation is 132[mm] which is the length of one segment. Thus the actual loss in DC+ track is multiplied by 3.

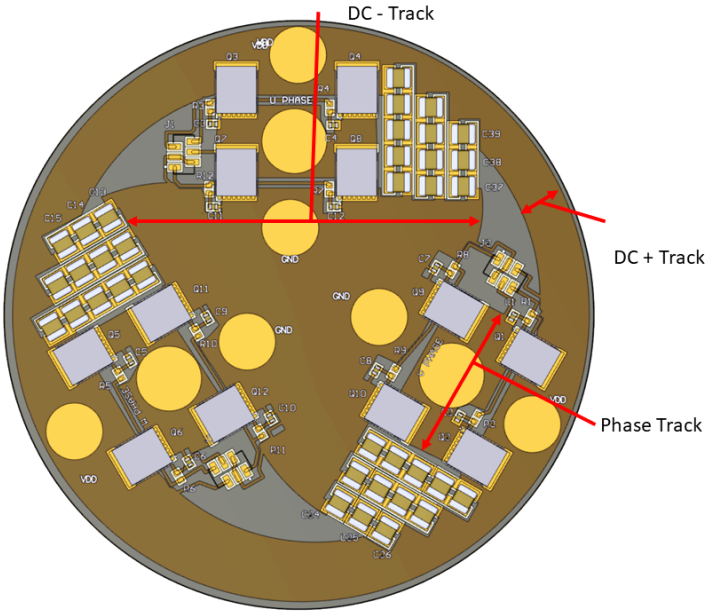


Figure 4.2: Inverter PCB design

Since the available copper thickness for printing in market was only 3Oz which is (105um or 0.105mm), The PCB in this project uses 3Oz copper thickness, This is not enough to handle such high currents, In order to solve this problem the only possible way is to increase the area of copper, since the thickness of copper track could not be increased it was planned to solder extra Copper wire over the DC+ track to increase the effective thickness of copper, thereby increasing the Area of Copper track which in-turn reduces the Resistance and consequently the power loss in the track is also reduced. A 4 [mm^2] copper wire was used for this. Considering these assumptions the track losses are calculated. It can be seen in the Table 4.4.

Table 4.4: PCB Track Losses

Thickness (mm)	L (mm)	W (mm)	ρ	A (mm^2)	R (mΩ)	Losses (W)
DC + Track						
0.035	132	12	0.0168	0.42	5.28	83.8
0.070	132	12	0.0168	0.84	2.64	42
0.105+2.257	**132**	**2.257**	**0.0168**	**5.33**	**0.416**	**6.6**
0.140	132	12	0.0168	1.68	1.32	21
Phase Track						
0.035	15	11	0.0168	0.385	0.655	115.5
0.070	15	11	0.0168	0.77	0.327	57.7
0.105	**15**	**11**	**0.0168**	**1.16**	**0.217**	**38.3**
0.140	15	11	0.0168	1.54	0.164	29
DC - Track						
0.035	78.7	70	0.0168	2.45	0.54	8.6
0.070	78.7	70	0.0168	4.9	0.27	4.3
0.105	**78.7**	**70**	**0.0168**	**7.35**	**0.18**	**2.86**
0.140	15	11	0.0168	9.8	0.135	2.14

4.1.4 Total Losses

Summing up all the losses calculated in the above sections. The overall losses of the inverter with the MOSFET losses, track loss, DC link loss, connector losses it is calculated as below. All the losses in this table are calculated using Ideal conditions, also current magnitude of 420A is considered to estimate the losses for 20kW peak operating point. Hence the efficiency is expected to be higher than the actual efficiency of the Inverter.

FREQUENCY	COMPONENTS	LOSS (W)
100kHz	MOSFETS (conduction + switching)	1108.4
	DC Link	19.76
	Track Loss	144.12
	Power terminal	3.46
	Gate driver & controller	14
OVERALL		1289.7 (Efficiency 93.55%)
50kHz	MOSFETS (conduction + switching)	1067.2
	DC Link	12.88
	Track Loss	144.12
	Power Terminal	3.46
	Gate driver & controller	14
OVERALL		1241.6 (Efficiency 93.8%)

Figure 4.3: Overall loss estimation

The results of Table 4.3 mainly compares between 50Hz and 100Hz switching frequency. It can be clearly seen form Table 4.3 that operating at 50kHz switching

frequency would have a better efficiency compared to 100kHz. But due to the main fact that the DC link size would increase by going down in switching frequency, from Table 4.2 it is evident that large number of capacitors would be needed for lower switching frequency. Due to the lack of availability of MLCC capacitors in the market and the complexity of adding so much capacitors to the PCB, it was decided to use 100kHz Switching frequency.
For proper comparison between Practical and Theoretical loss, The theoretical losses are calculated for each operating point by using the actual practical Rms phase current magnitudes. The values are shown in the Table 4.5. These values are later compared with the practical measurement values in Section 5.5.

Table 4.5: Theoretical Loss Calculation

Input Power (kW)	Current (A)	Conduction Loss (W)	Switching Loss (W)	Other Losses (W)	Total Losses (W)	Theoretical Efficiency (%)
2.27	59.1	29.4	18.5	17.2	65	97.1
6.46	186.36	204	41.15	45.35	290.5	95.5
8.30	210.34	260	45.4	54	359.4	95.67
9.02	220.36	287.86	47.18	58	393	95.64

The Figure 4.4 Shows the Output Voltage and Figure 4.5 shows the Output current waveform from Matlab Model of the Inverter at 20kW output power.

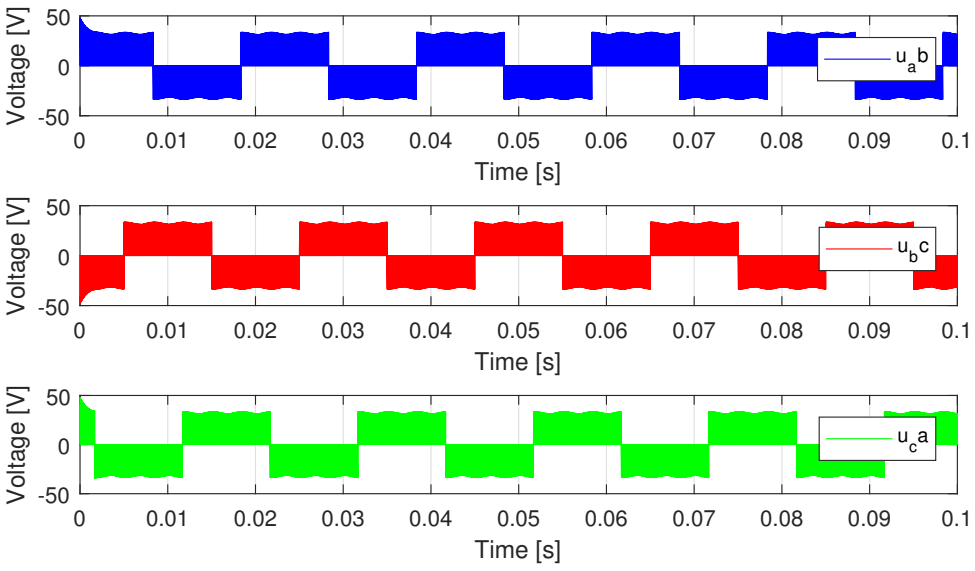


Figure 4.4: Three Phase Voltage from simulation

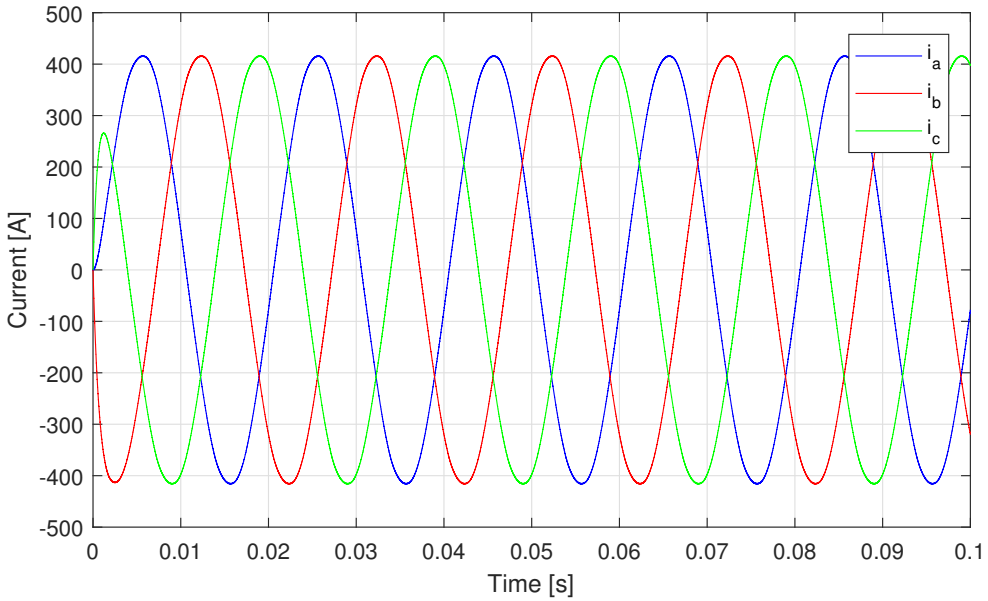


Figure 4.5: Three Phase Current from simulation

Table 4.5 shows the theoretical loss estimation using the current values from the practical measurements in-order to compare the theoretical losses with the practical losses. The other losses include all the capacitor loss, track loss, terminal loss and driver and control circuit loss. The capacitor loss and terminal losses are calculated based on the equations discussed in Section 4.1.3. The Driver and control circuit loss was calculated by running the inverter without connecting the load, it was found to be 14 W.

Table 4.6: Expected Theoretical Losses for higher Powers

Input Power (kW)	Current (A)	Conduction Loss (W)	Switching Loss (W)	Other Losses (W)	Total Losses (W)	Theoretical Efficiency (%)
12	252	357.7	52.78	71.32	500	95.8
16	336	657.3	67.62	116	841	94.7
20	420	1026	82.4	173.2	1282	93.6

In Table 4.6 the losses and efficiency of the Inverter is calculated assuming ideal currents for the different power levels. From the table it can be seen that the maximum efficiency of the inveter at 20kW power is around 93.6 %.

4.1.5 Thermal Analysis

The thermal power dissipation through the different layers of the PCB are calculated using the thermal model as discussed in the Section 2.5. The various temperature differences and thermal resistances of each layer can be seen in Table 4.6. The actual area of the MOSFET is considered for the thermal resistance calculation of the MOSFET and the solder. For rest of the components the ares of the PCB is

considered. The dimensions and other design parameters of the PCB are discussed in Section 3.4. Table 4.6 shows the thermal resistance. The thickness of Thermal Grease is assumed to be 0.05mm based on some application notes by Semikron [18]. The other material thickness are considered from the actual manufactured PCB.

R_{TH}	LAYER (MATERIAL)	THICKNESS(mm)	AREA (mm^2)	THERMAL CONDUCTIVITY(W/mK)	R_{TH} VALUE (K/W)
R_{th} MOSFET	Silicon	2.3	1.158*e-4		0.033
R_{th} Solder	Sn(60)/Pb(40)	0.81	1.158*e-4	50	0.01167
R_{th} Track	Copper	0.105	1697	400	0.0000155
R_{th} Dielectric	FR4	0.15	1697	0.3	0.0295
R_{th} IMS	Aluminium	2	1697	238	0.000495
R_{th} Thermal Paste	HTC thermal Grease	0.065	1697	1.3	0.02946
R_{th} Heat Sink	Aluminium	30	1697	238	0.00286
			TOTAL R_{TH}		**0.107**

Figure 4.6: Equivalent Thermal Resistance calculation

The temperature rise due to one MOSFET power loss can be calculated from the thermal resistance value as

$$Temp = R_{therm} P_{loss} \tag{4.3}$$

from the total power loss as calculated in (4.1). The overall temperature rise for 20kW operation (peak power) is estimated to be 137.2 ° C approximately.

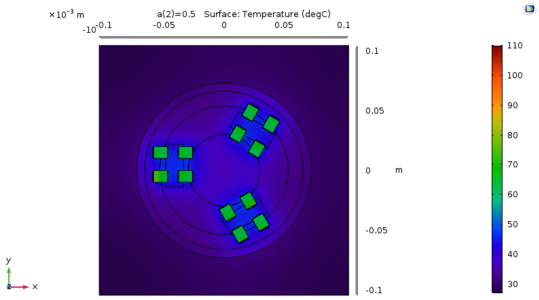
4.2 COMSOL Analysis

The thermal model of the actual inverter PCB was made in COMSOL Multi-physics considering the different thickness and thermal resistance as discussed in Section 4.1.5. This Thermal model is expect to recreate the actual PCB and help in determining the temperature on the MOSFET'S based on the different layers on the PCB theoretically. The following assumptions were made during the simulation.

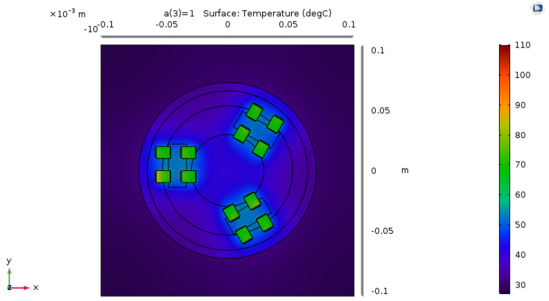
- Convective heat flux is used as cooling at the bottom of the cooling plate.
- The Mosfet is considered to be made of three layers. The top layer is silica glass, middle layer is silicon and bottom layer is copper
- Thermal Paste thickness is made to vary as we do not know the exact thickness which we would apply
- All the other material thicknesses are taken as per the designed PCB and standards from the Manufacturer (PCB way China)
- since the actual structure of the cooling plate is known it is just assumed to be a block of aluminium. dimensions are measured from the actual cooling block
- The DC link losses are not taken into account in these simulations due to complexity.

Figure 4.7 illustrates the thermal behaviour of the PCB at the 9kW operating point for different thickness of the thermal grease. By doing this we can determine the

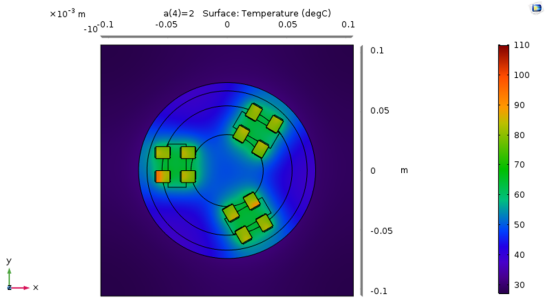
thickness of the thermal grease that is applied on the practical PCB.The obtained simulation results are compared with the results obtained from the practical temperature measurement.The value which matches or is close to the practical measurement could be considered as close value to the actual value of thickness of the applied thermal grease on the PCB.



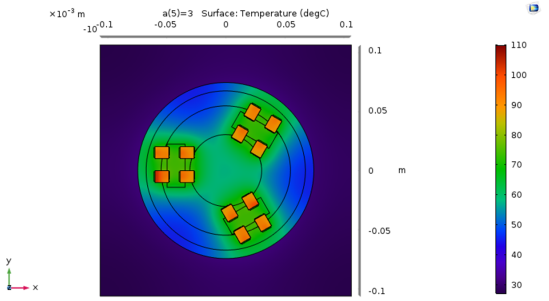
((**a**)) Thickness 0.005mm



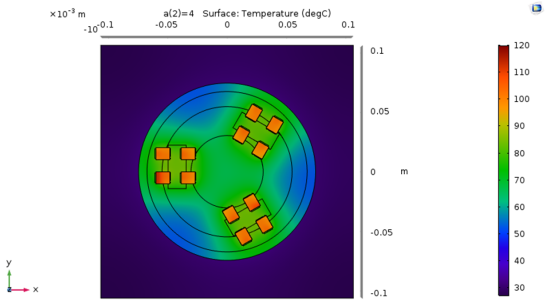
((**b**)) Thickness 0.1mm



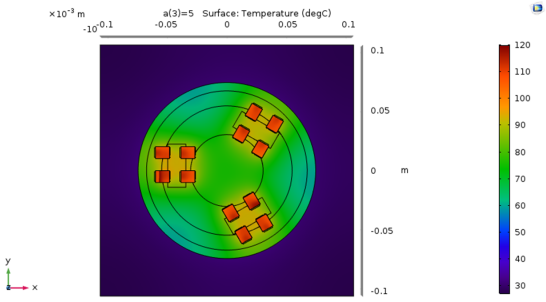
((**c**)) Thickness 0.2mm



((**d**)) Thickness 0.3mm



((**e**)) Thickness 0.4mm



((**f**)) Thickness 0.5mm

Figure 4.7: Temperature of MOSFET's due to variation in the thickness of thermal Grease

The obtained simulation results are tabulated in Table 4.7 When this is compared with the practical temperature of the PCB at 9kW operating point it matches with the simulation result at 0.3mm thickness. SO it was assumed that the temperature of the applied thermal grease on the PCB was 0.3mm. Therefore, the simulations of

the remaining operating points were carried out at 0.3mm thickness of the thermal grease.

Table 4.7: Temp for different thermal grease thickness

Thickness of Thermal Paste	MOSFET Max. Temp.
0.05 mm	80 ° C
0.1 mm	87 ° C
0.2 mm	95 ° C
0.3 mm	100 ° C
0.4 mm	110 ° C
0.5 mm	120 ° C

The Figures 4.8,4.9,4.10 4.11 represents the temperature characteristics of the PCB at 2kW, 6kW, 8kW and 9kW operating points respectively.
The design and layout of all the PCB is same. The parameters that are varied to obtain these results are the heat flux of the PCB at different operating points and also the heat flux at different parts of the PCB like the MOSFETs , DC+ track, DC- track and the phase track. The values that are assigned as the heat flux is actually the losses at these different points on the PCB for the corresponding operating points. From the figures it can be seem that there is an increase in the temperature at the different operating point due to the increase of current at different operating points.

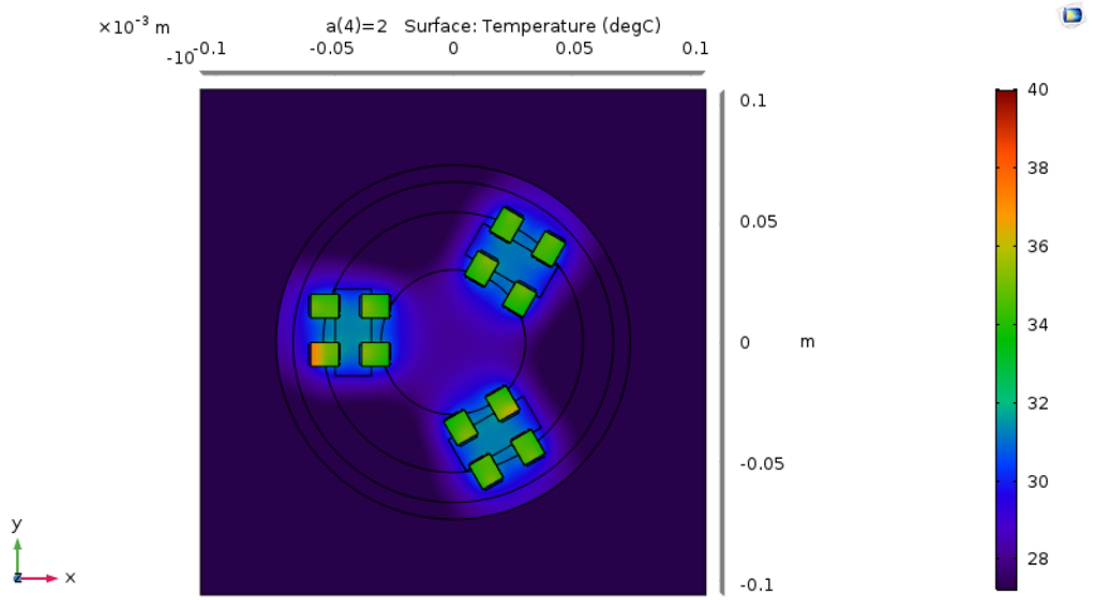


Figure 4.8: Temp at 2kW

Figure 4.8 presents the temperature variation on the different parts of the PCB for 2kW operating point. The maximum observed temperature on the Mosfet is 37° C.

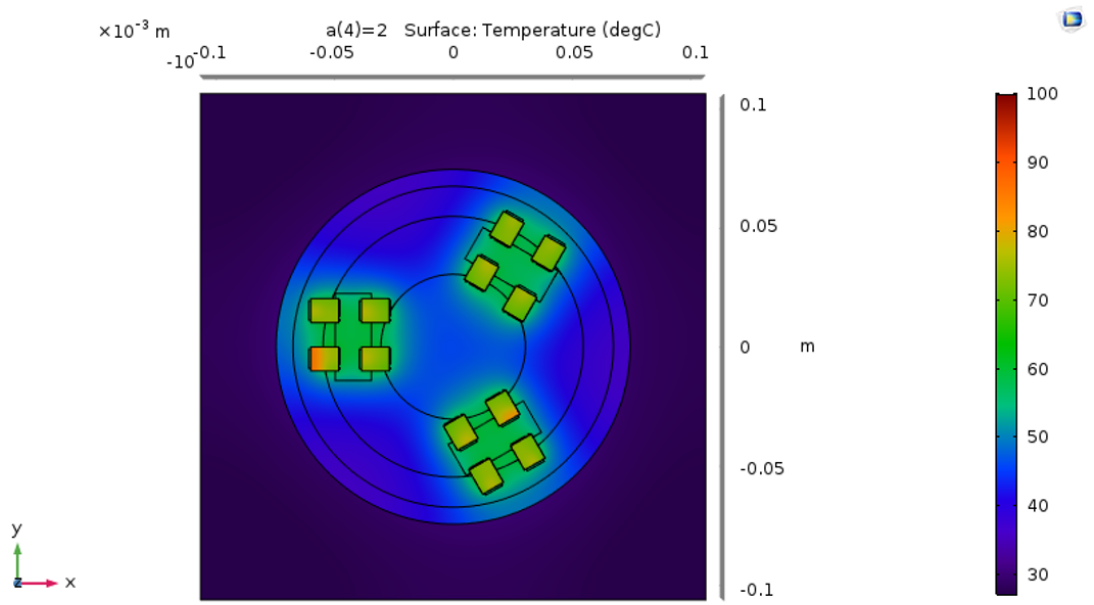


Figure 4.9: Temp at 6kW

Figure 4.9 presents the temperature variation on the different parts of the PCB for 6kW operating point. The maximum observed temperature on the Mosfet is 85° C.

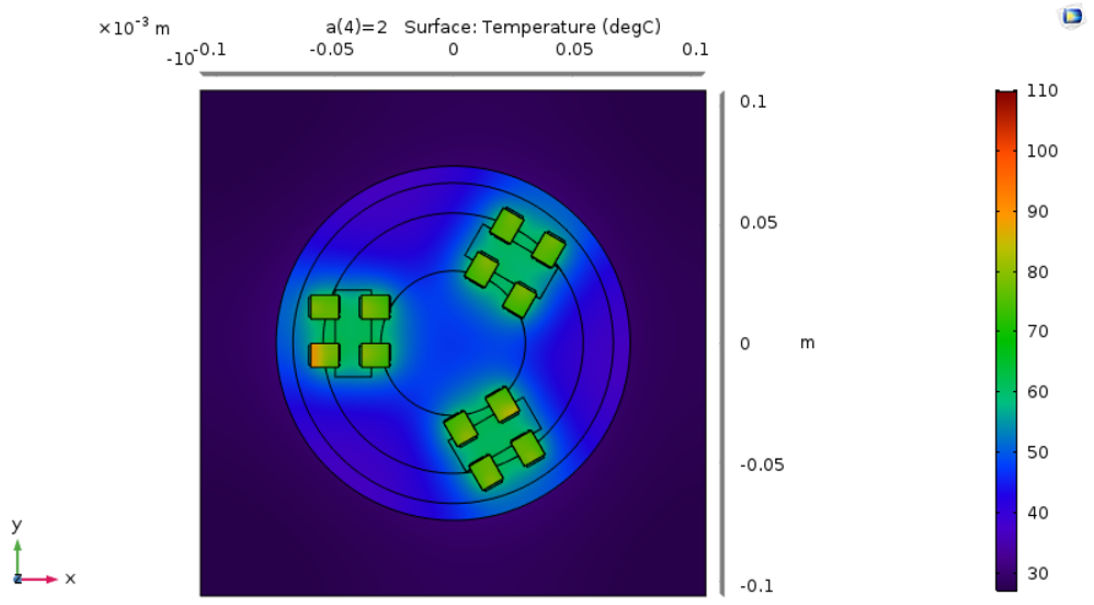


Figure 4.10: Temp at 8kW

Figure 4.10 presents the temperature variation on the different parts of the PCB for 8kW operating point. The maximum observed temperature on the Mosfet is 92° C.

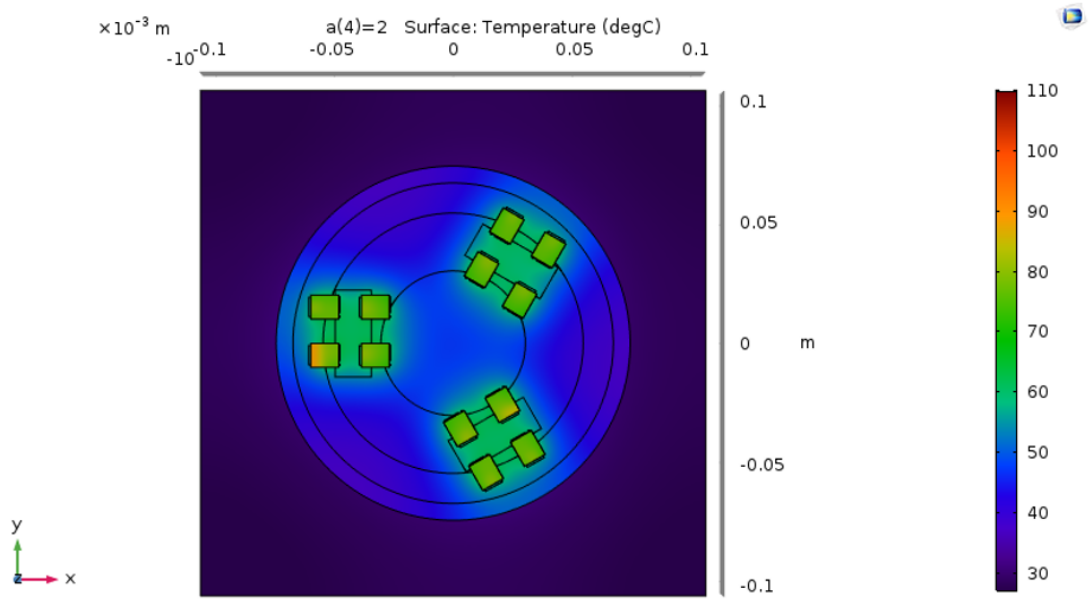


Figure 4.11: Temp at 9kW

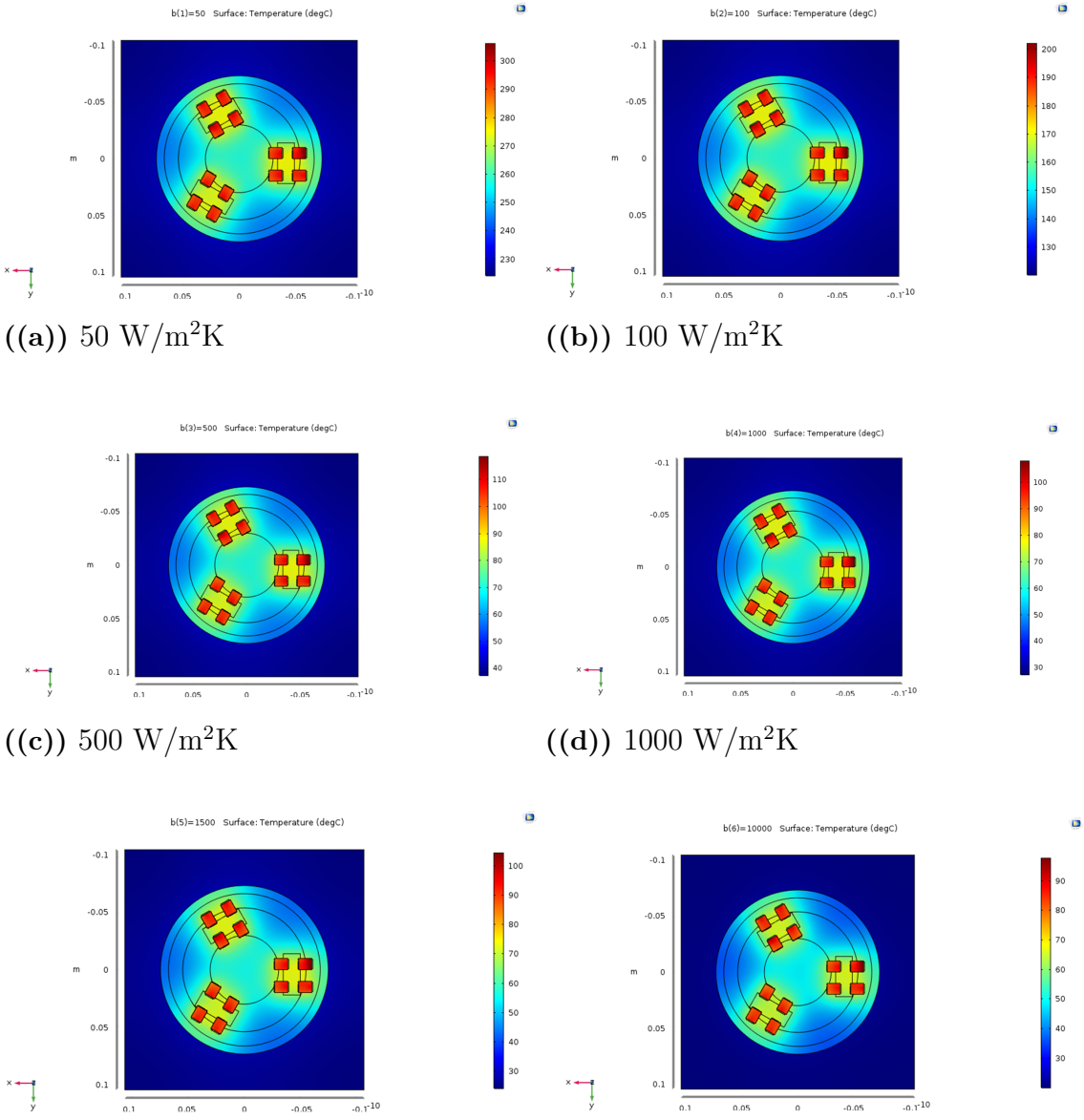
Figure 4.11 presents the temperature variation on the different parts of the PCB for 9kW operating point. The maximum observed temperature on the Mosfet is 100° C.

The legends in the plots are kept constant to facilitate an easy understanding of the variation of the temperature in different plots at different operating points. The ambient temperature in the simulation is kept at 20° C, Thus the ΔT value can be calculated. These are shown in Table 4.8

Table 4.8: Max MOSFET Temperature at different Operating Points

Power Rating (kW)	Max Mosfet Temp.(° C)	ΔT (° C)	Theoretical Temp.(° C)
2	38	16	36.6
6	85	65	83
8	98	72	96.8
9	104	80	102.6

For further analysis the 9kW operating point is selected. The Thickness of the thermal grease is kept constant at 0.3mm, as it was estimated that this thermal thickness in the actual setup was 0.3mm. The heat transfer coefficient for convective heat flux is varied. The General value for Forced convection heat transfer for water varies from 50 - 10000 (W/m^{2}K) [19]. The simulation results are presented in Figure 4.12.



((a)) 50 W/m^{2}K **((b))** 100 W/m^{2}K

((c)) 500 W/m^{2}K **((d))** 1000 W/m^{2}K

((e)) 1500 W/m^{2}K **((f))** 10000 W/m^{2}K

Figure 4.12: Heat Transfer Coefficient variation for water

From Figure 4.12 it can be clearly see that the minimum and the maximum temperature of the whole setup up changed but the Rise in Temperature (ΔT) remained constant for all the different Heat transfer coefficients. Thus it is seen that this parameter variation actually does not affect the thermal model as such. It only affects the measurement range.

5

Practical Results

5.1 Case Setup 1

A RL(resistive and Inductive) load was connected to the singe phase circuit to test the existing driver circuit. The Setup can be seen from Figure 5.1 The first plot in Figure 5.2 shows the High Gate signal(Blue) and Low Gate signal(Black), it could be seen that the High gate pulse is around 10V (58 -48V) because the High gate voltage is measured across the Gate source of the higher MOSFET which takes into account the DC input voltage as the source point is floating and not grounded. Whereas the low gate pulse measures around 10V, as it is measures the lower MOSFET gate voltage directly with ground as reference. The second graph shows the output Voltage and output current measured across the load. It was seen that the output voltage was almost 50V and current was 1.5A.

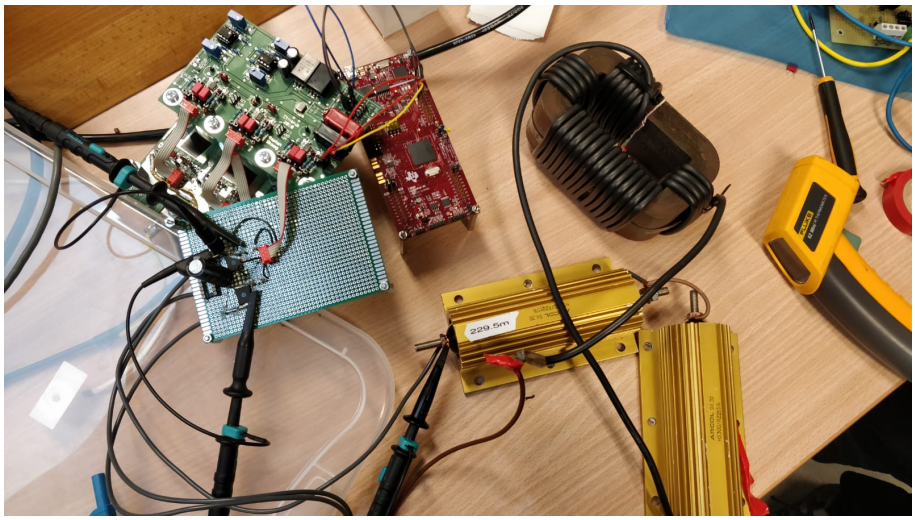


Figure 5.1: Measurement Test setup for Driver circuit

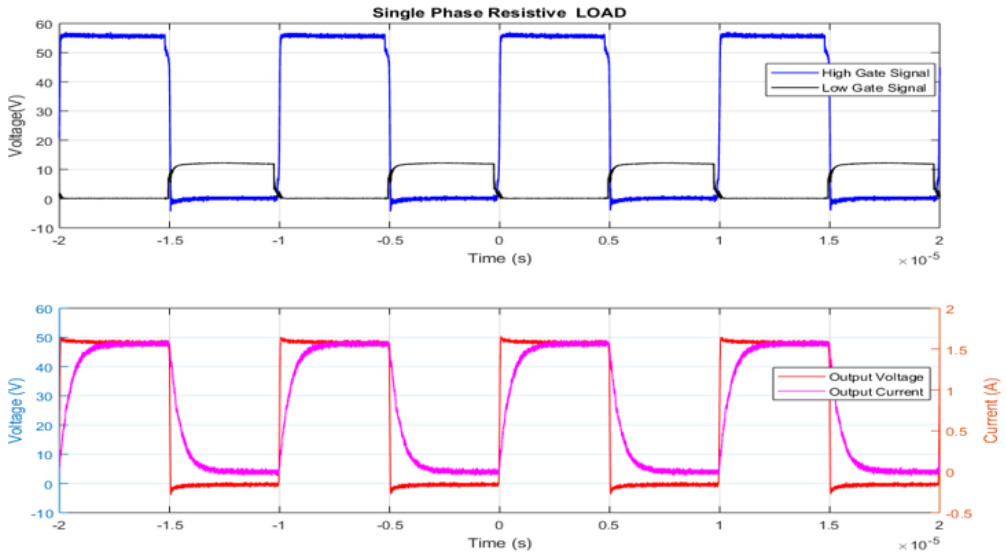


Figure 5.2: High, low gate signals and Output Voltage and Current waveforms

5.2 Case Setup 2

This Circuit was to test if the Gate driver could drive two MOSFET in parallel. From Figure 5.3 it is be seen that Gate driver could drive the parallel MOSFET's. There was no significant delays between the turn on and turn off of the two MOSFET's. The Blue line shows the Drain source Voltage of the First MOSFET and Red line shows the Drain source voltage of the Second MOSFET.

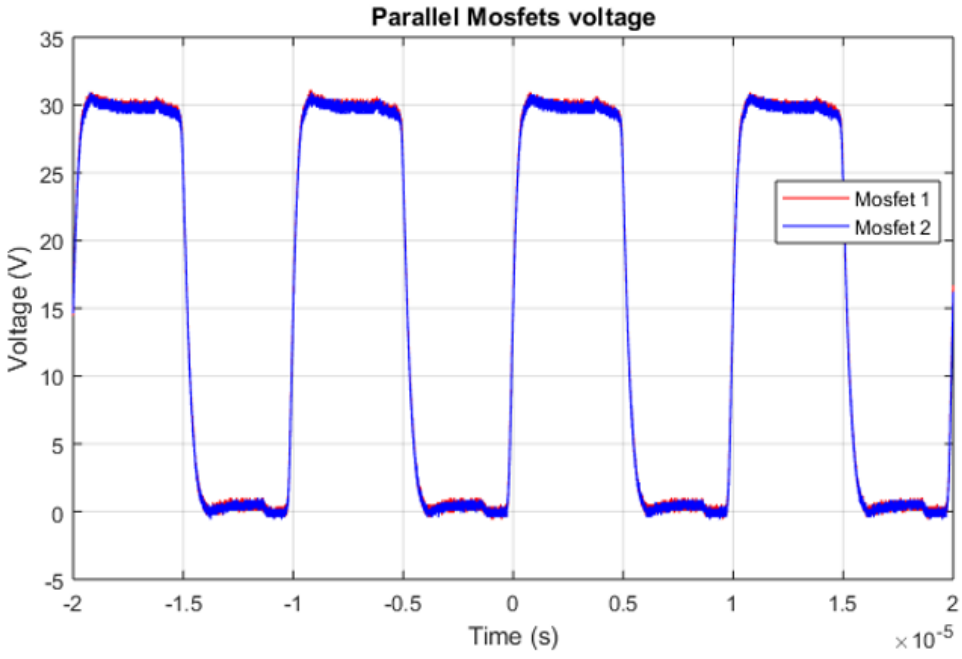


Figure 5.3: Gate signal of Parallel MOSFET's

5.3 Prototype Inverter

This section discusses about the different tests and measurements done on the Prototype inverter.

5.3.1 Gate Driver Test

The first test was done on the gate driver circuit board. This testing was done to compare the effect of the line impedance between the gate driver and the inverter board. Figure 5.4 shows the gate pulse from the old driver board and the new driver board.

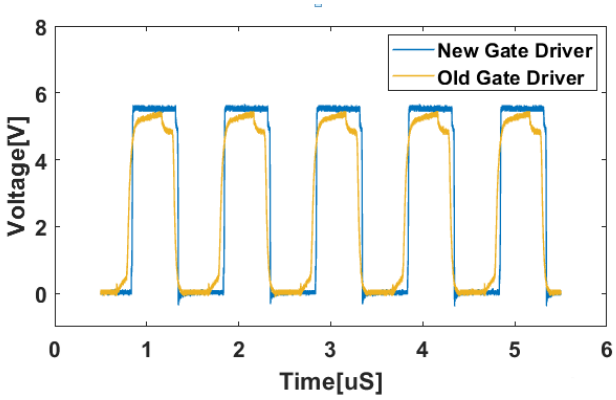


Figure 5.4: Inverter setup

From the Figure 5.4 it is evident that there are more distortions in the old gate driver waveform compared to the new gate driver board as the distance between the old gate driver is greater than the new gate driver. This increased distance will lead to increased line impedance. Figure 5.5 and Figure 5.6 shows the inverter setup with the old gate driver and the new gate driver respectively,

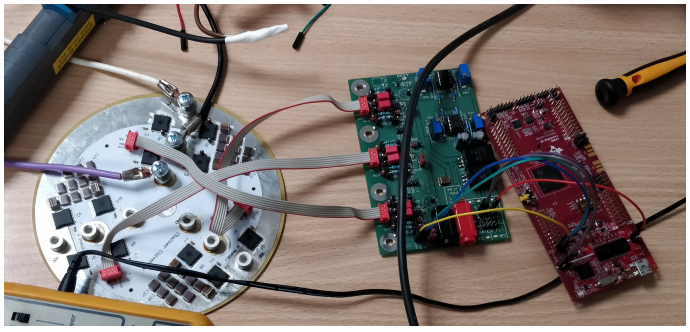


Figure 5.5: Inverter setup connected to old gate driver

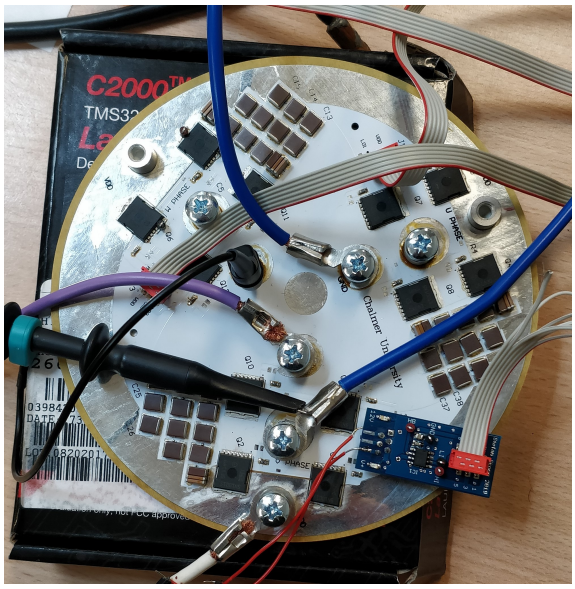


Figure 5.6: Inverter setup connected to new gate driver

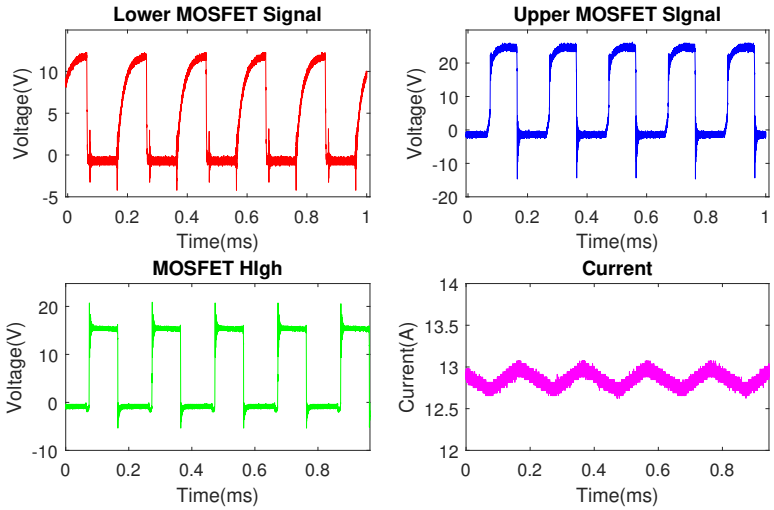


Figure 5.7: Old driver board Gate pulse signals

Figure 5.7 shows the gate pulse signals of the old gate driver boards. The old gate driver setup was used to run this prototype as it is evident from the plots that there are lot of ringing, which is due to the line inductance of the cable from the gate driver to the prototype PCB. From the plot it is evident that there are lot of voltage and current ripple. The voltage ripples can be minimized by properly designing the DC link capacitor bank and the current ripple can be reduced by having a low pass filter.

5.3.2 Electrical Measurements

The results of all the electrical measurements done are explained in this Section. Figure 5.8 shows the Measurement setup. Figure 5.9 shows in detail the different parts of the bench setup for easier understanding.

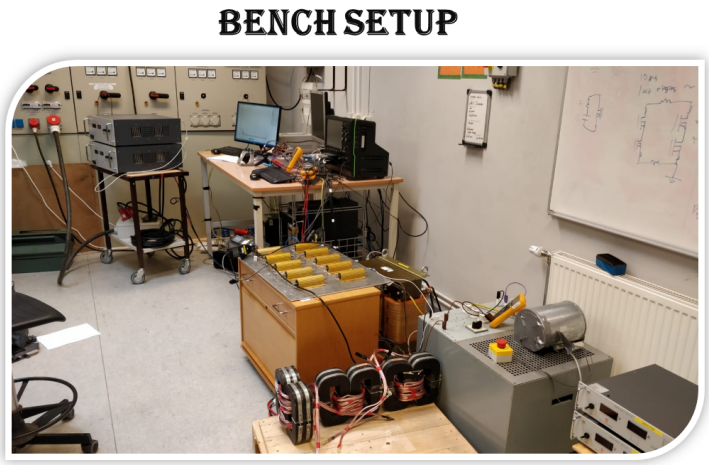


Figure 5.8: Bench Setup

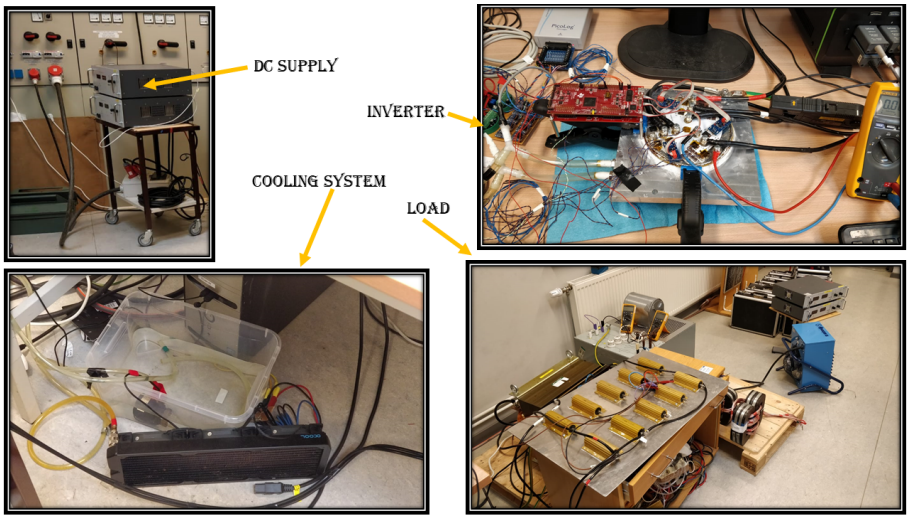


Figure 5.9: Split view of Bench setup

The prototype PCB was soldered and assembled in order to carryout the measurements and to move forward with the verification of the inverter. The inverter consists of two MOSFET's in parallel which comprises of four MOSFET's per leg as shown in Figure 5.10 .

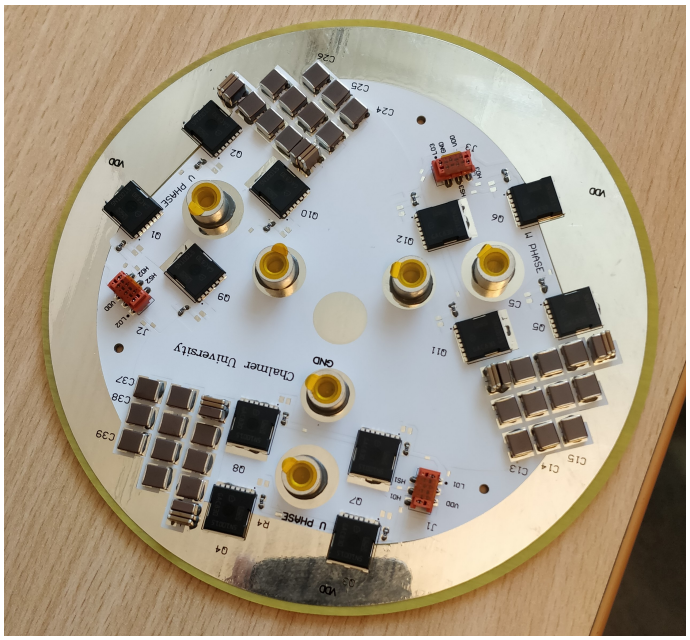


Figure 5.10: Inverter setup

The driver circuit PCB and the micro-controller along with the inverter and the cooling block setup is shown in Figure 5.11.

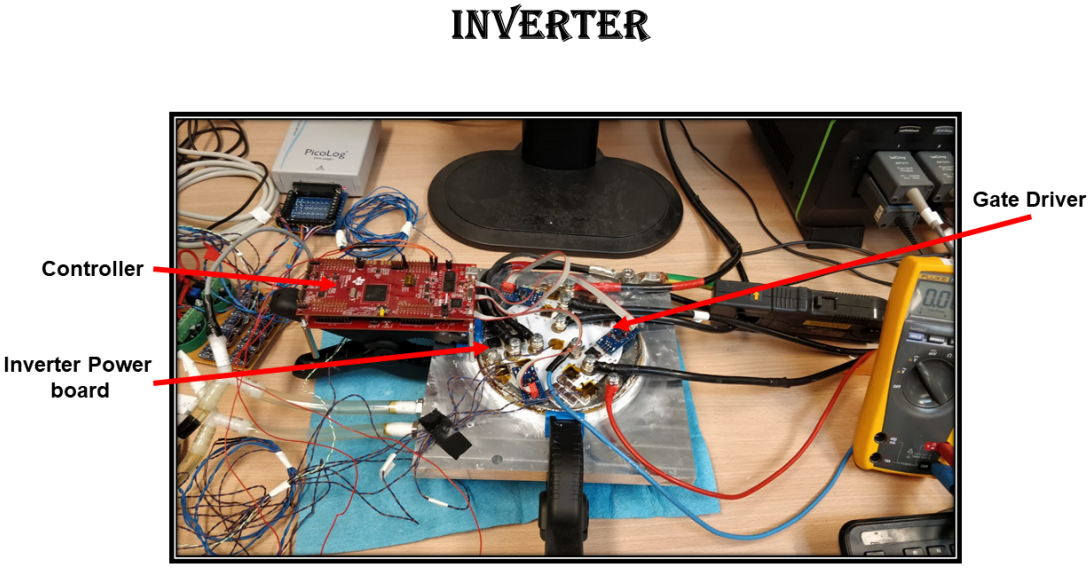


Figure 5.11: Prototype Inverter PCB

The Figure 5.12 illustrates the bench setup which is used to carry out the electrical measurements.

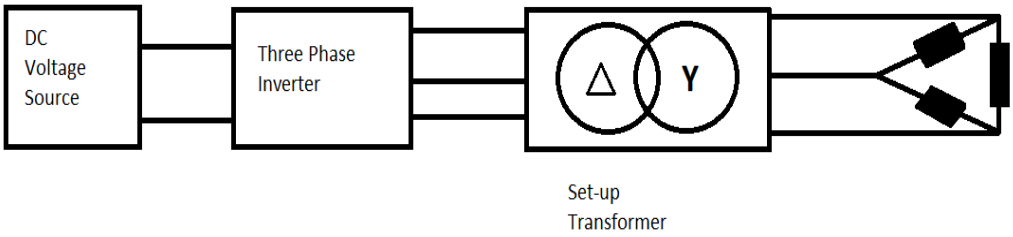


Figure 5.12: The measurement schematics

The inverter was designed to deliver a continuous operating power of 10kW. To test this, the load is connected to the star connected secondary of the transformer through a three phase resistive load in series as in Figure 5.12. The inverter converts the DC power from the source to AC power and this is delivered to a three phase load through a Δ - Y connected set-up transformer which has an approximate turns ratio of 10. The inverter is not directly operated at the 10kW continuous operation point instead it is operated at different operating point for some time and it is gradually increased to reach the continuous operation point. The actual load setup can be seen in Figure 5.13.

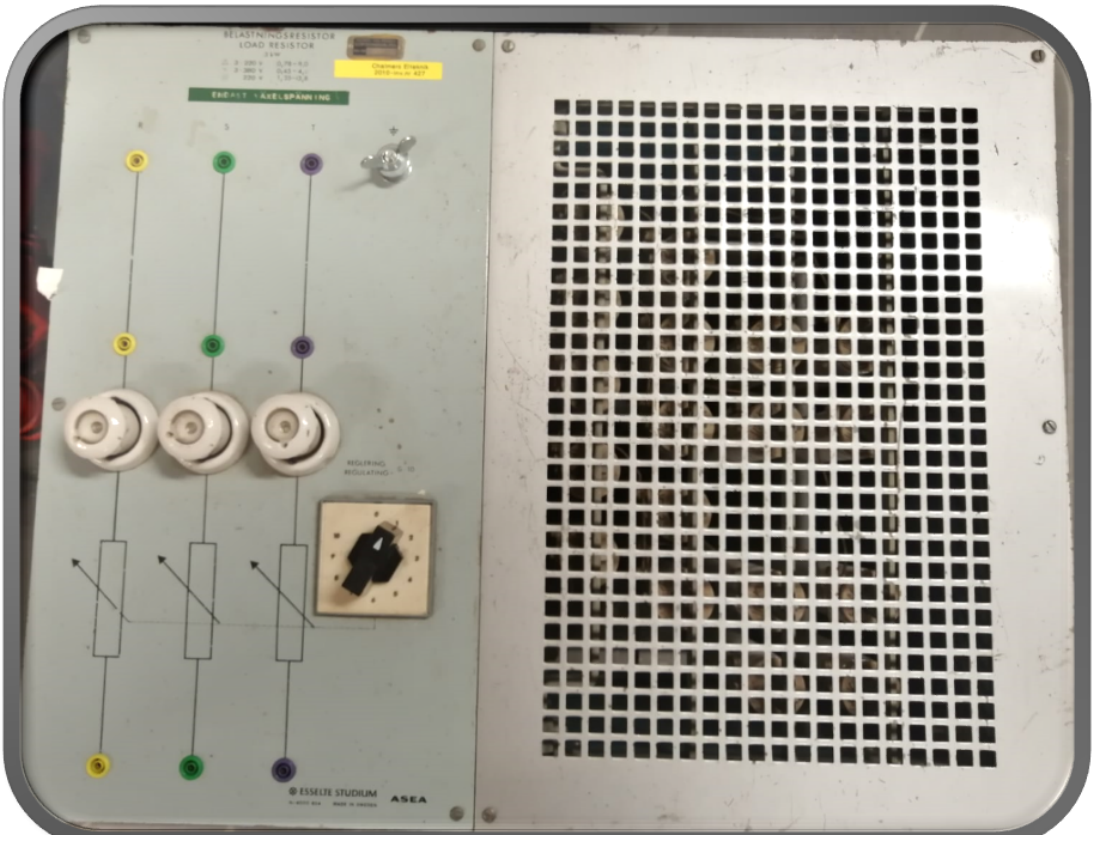


Figure 5.13: Load setup

5.3.2.1 2kW load

The Figure 5.14 is the capture from the LeCroy Oscilloscope MDA800A as discussed in section 3.9.1. The first plot at the top-left shows the three phase currents measured just after the inverter on the primary side of the transformer, The second plot at the top-right shows the Input DC current waveform, The third plot bottom-left shows the three phase to phase voltages and the fourth plot on the bottom-right shows the DC Input voltage. All these measurement were taken at the 2kW operating point with a switching frequency of 100kHz and an input voltage of 48V. It can be seen that the input current is around 48A. The output current is around 56A. The input power from the source is 2.27kW and the output power that the load pulls is equal to 2.15kW. The efficiency at this operating point is 94.7%, with the losses in the cable. Later in section 5.3.2.4 the actual inverter efficiency for all the operating points are calculated.

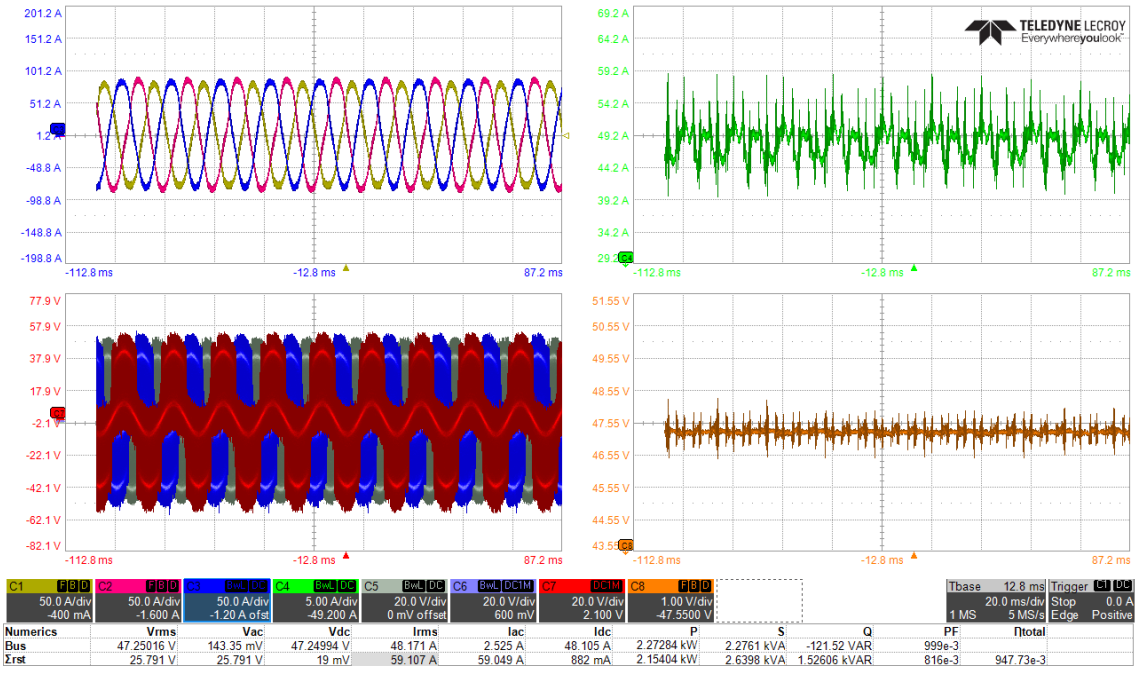


Figure 5.14: Snapshot of Oscilloscope waveforms at 2kW

Figure 5.15 shows the zoomed version of the three phase currents at 2kW operating point when an input voltage of 48V. The current waveform is sinusoidal with minimum ripple.

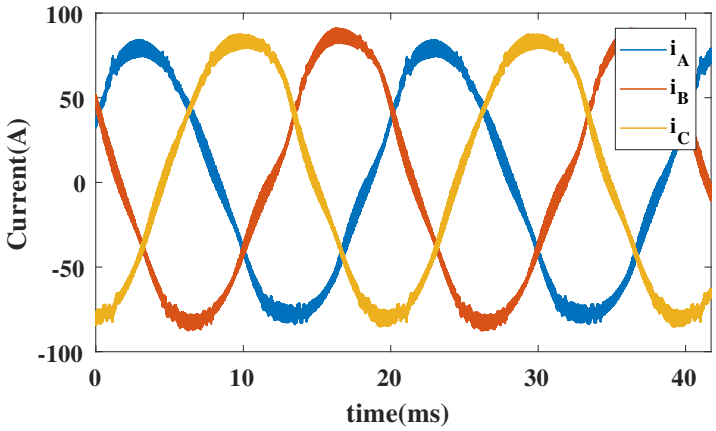


Figure 5.15: Phase currents at 2kW

Figure 5.16 shows the zoomed version of three phase voltage at 2kW operating point when a supply voltage of 48V is applied.

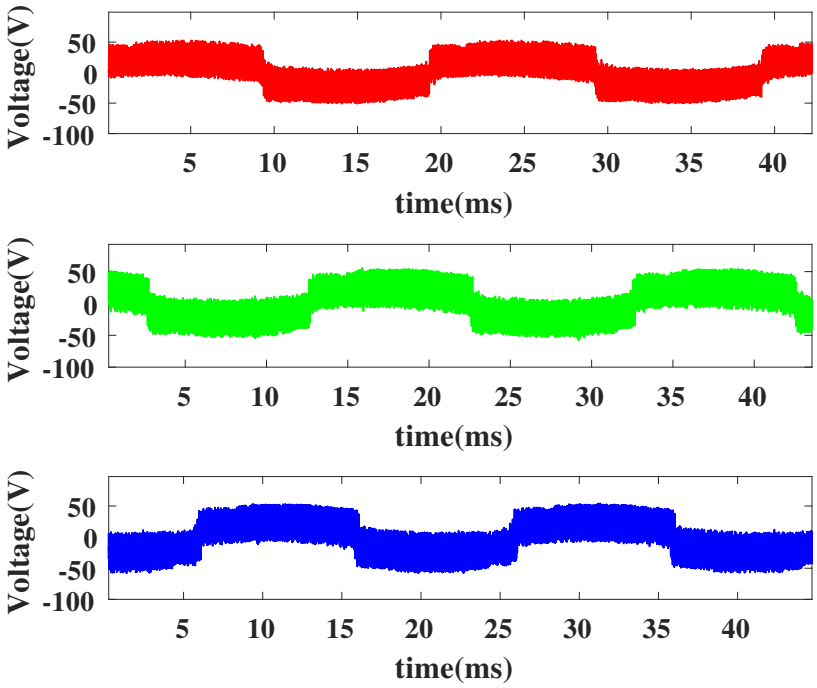


Figure 5.16: Phase to phase voltages at 2kW

The Voltage and current are measured at the output of the inverter just before the transformer. The Table 5.1 shows the input and output voltage, current, power and Efficiency values for the 2kW operating points measured using Lecroy oscilloscope.

Table 5.1: Measurement values for 2kw operating point

Udc [V]	Idc [A]	Pdc [kW]	U line RMS [V]	Irms[A]	Pac[kW]	Eff.[%]
47.25	48.17	2.27	25.7	59.107	2.15	94.7

5.3.2.2 6kW load

Figure 5.17 shows a capture from the LeCroy oscilloscope at the 6kW operating point. The first plot at the top-left shows the three phase currents measured just after the inverter on the primary side of the transformer, The second plot at the top-right shows the Input DC current waveform, The third plot bottom-left shows the three phase to phase voltages and the fourth plot on the bottom-right shows the DC Input voltage. At an input voltage of 48V, switching frequency of 100kHz the input current is 135A. The load pulls a current of 186A. The input power from the source is 6.45kW and the output power that the load pulls is equal to 5.68kW. The efficiency at this operating point is 88%. There is a reduced efficiency in this case due to the increase in temperature in the cables. This leads to increased losses in the cable. Later in section 5.3.2.4 the actual inverter efficiency for all the operating points are calculated.

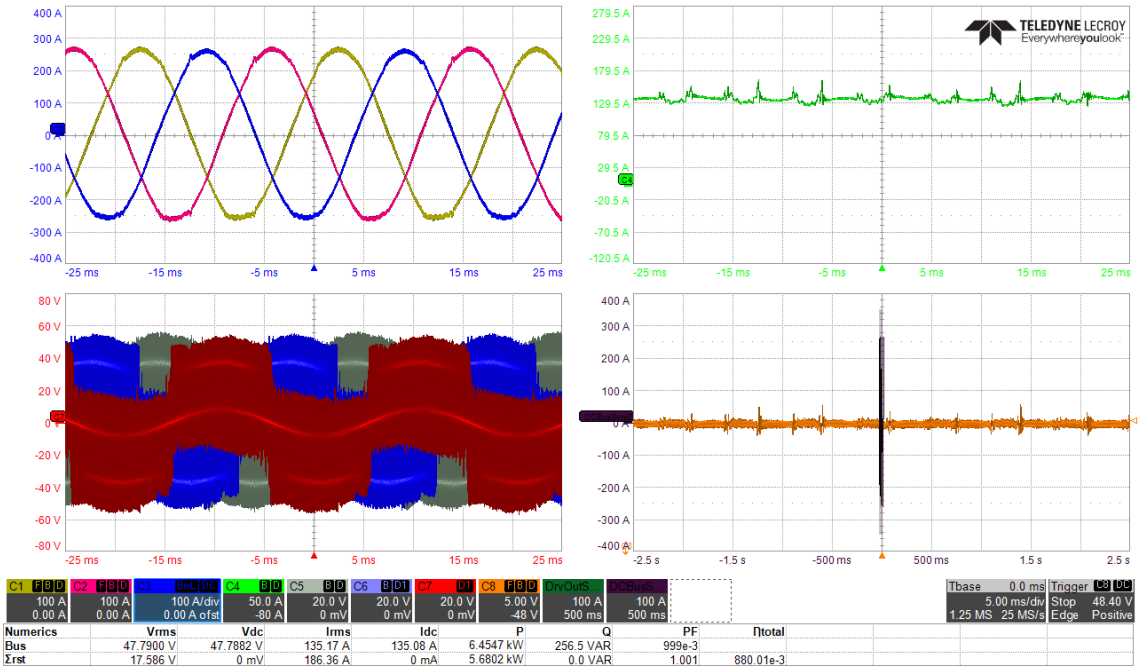


Figure 5.17: Snapshot of oscilloscope waveforms at 6kW

Figure 5.18 shows the zoomed version of three phase current and at 6kW operating point when a supply voltage of 48V is applied. The waveform is quite sinusoidal with less ripple.

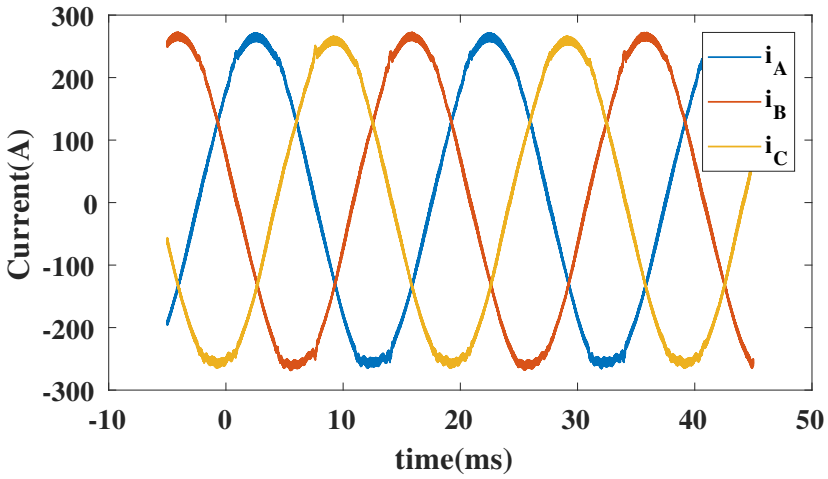


Figure 5.18: Phase currents at 6kW

Figure 5.19 shows the zoomed version of three phase voltage at 6kW operating point when a supply voltage of 48V is applied.

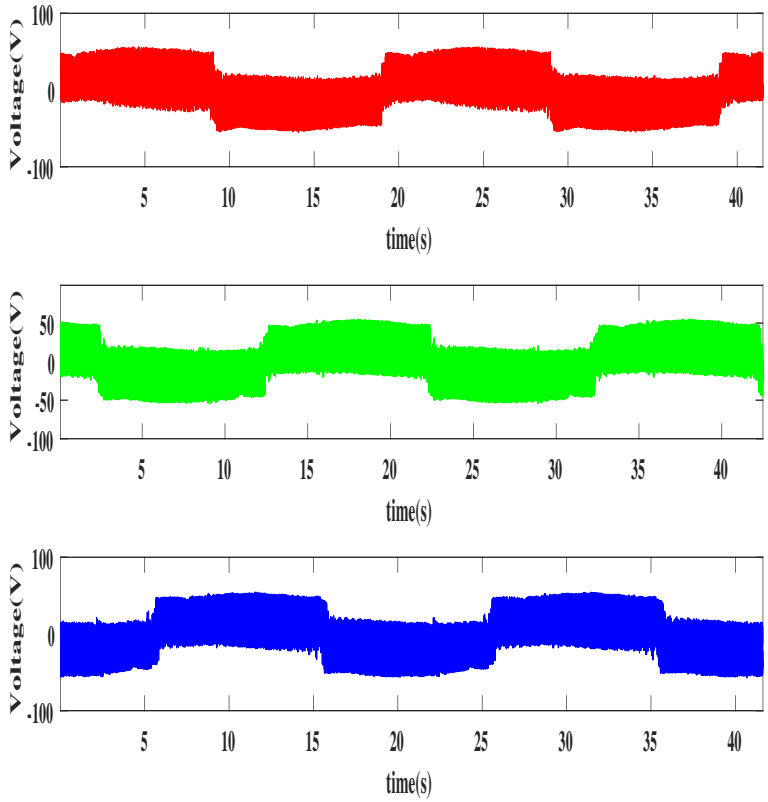


Figure 5.19: Phase to Phase voltages at 6kW

The Voltage and current are measured at the output of the inverter just before the transformer. Table 5.2 shows the input and output voltage, current, power and Ef-

ficiency values for the 6kW operating points measured using Lecroy oscilloscope

Table 5.2: Measurement values for 6kW operating point

Udc [V]	Idc [A]	Pdc [kW]	U line RMS [V]	Irms[A]	Pac[kW]	Eff.[%]
47.79	135.08	6.45	17.58	186.36	5.68	88

5.3.2.3 9kW load

Figure 5.20 is the capture from the LeCroy Oscilloscope at the 9kW operating point. The first plot at the top-left shows the three phase currents measured just after the inverter on the primary side of the transformer, The second plot at the top-right shows the Input DC current waveform, The third plot bottom-left shows the three phase to phase voltages and the fourth plot on the bottom-right shows the DC Input voltage. At an input voltage of 48V , switching frequency of 100kHz and the input current is 200A. The load pulls a current of 220A. The input power from the source is 9kW and the output power that the load pulls is equal to 8kW. The efficiency at this operating point is 88.7%. There is a reduced efficiency in this case due to the increase in temperature in the cables. This leads to increased losses in the cables. Later in section 5.3.2.4 the actual inverter efficiency for all the operating points are calculated.

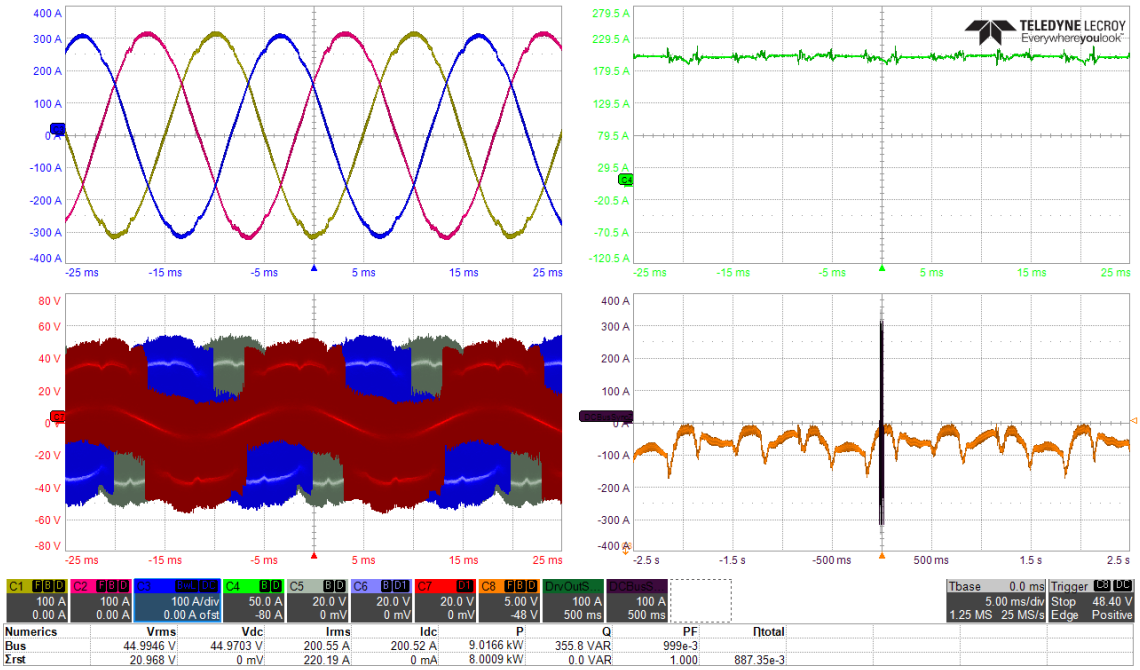


Figure 5.20: Snapshot of Oscilloscope waveforms at 9kW

Figure 5.21 shows the zoomed version of three phase current at 9kW operating point when a supply voltage of 48V is applied.

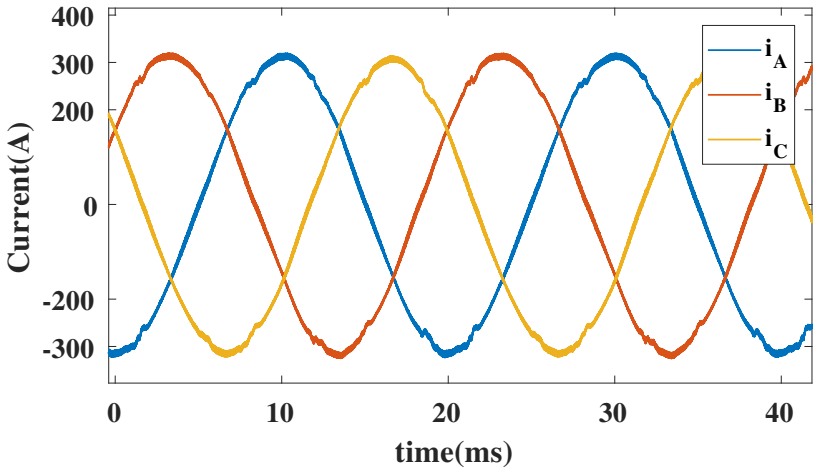


Figure 5.21: Phase Currents at 9kW

Figure 5.22 shows the zoomed version of three phase voltage at 9kW operating point when a supply voltage of 48V is applied

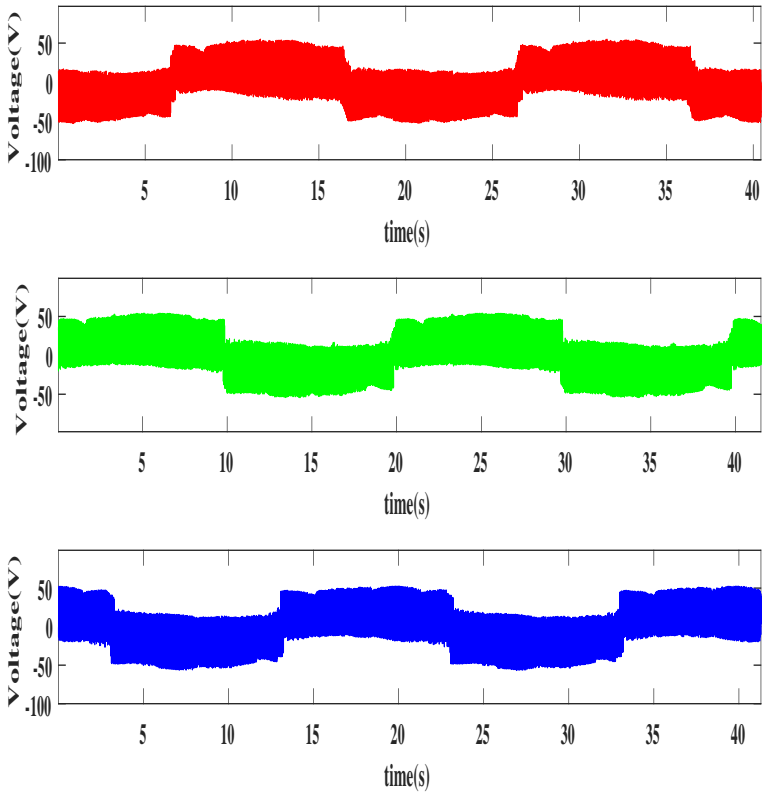


Figure 5.22: Phase to phase Voltages at 9kW

The Voltage and current are measured at the output of the inverter just before the transformer. Table 5.3 shows the input and output voltage, current, power and Ef-

ficiency values for the 9kW operating points measured using Lecroy oscilloscope.

Table 5.3: Measurement values for 9kW operating point

Udc [V]	Idc [A]	Pdc [kW]	U line RMS [V]	Irms[A]	Pac[kW]	Eff.[%]
45	200.55	9.01	20.96	220.2	8	88.7

5.3.2.4 Actual Loss estimation

As can be seen from the Bench block diagram in Figure 5.23 the output power is measured after the cables, which means that the output power includes the loss in the cable as well. So in-order to calculate the efficiency of the inverter, the loss in the inverter had to be calculated which could be done only by calculating the losses in the cable. the losses and efficiency of the inverter at different power level which was measured are shown in the Table 5.4 & 5.5. This losses and efficiencies values are compared with the theoretical values in section 5.5.1

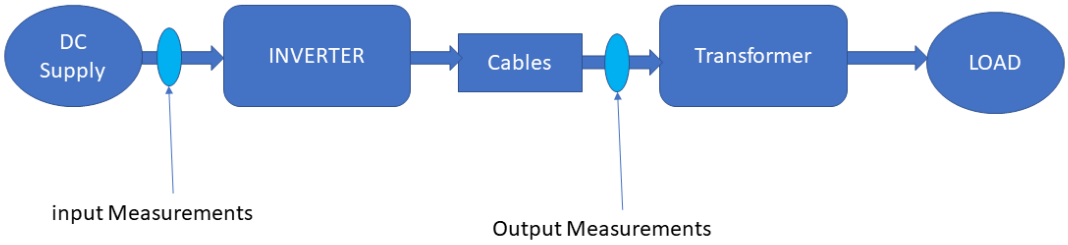


Figure 5.23: Block Diagram of Measurement setup

Table 5.4: Practical Loss Calculation

Input Power (kW)	Current (A)	Cable Resis-tance (mΩ)	Cable Loss (W)	Output Power (kW)	Total Loss (W)	Inv. Loss (W)
2.27	59.1	3.65	38.3	2.15	119	80.74
6.46	186.36	4.5	468	5.68	775	306
8.30	210.34	4.7	623.8	7.30	997	373
9.02	220.36	4.25	619	8.00	1020	401

Table 5.5: Practical Efficiency

Input Power (kW)	Inverter Loss (W)	Efficiency (%)
2.27	80.74	96.4
6.46	306	95.26
8.30	373	95.5
9.02	401	95.55

5.3.3 Thermal Measurements

The Temperature of the MOSFET's were measured using a thermocouple and recorded using Picolog data acquisition software. The maximum temperature of the MOSFET's are noted and tabulated in Table 5.6 which would be used to compare with the thermal calculations made using COMSOL multi-physics to see if the thermal model we built is in close approximation with the Practical inverter PCB. The comparison between the theoretical and practical thermal values are done in section 5.5.2 The Temperature logged by the Picolog can be seen from Figure 5.24 & 5.25.

Table 5.6: Mosfet Temperature

Operating Point (kW)	MOSFET Temperature (°C)
2	31.77
6	93.82
8	108.1
9	111.5

5.4 Calorimetric measurements

The calorimetric measurements could not be conducted as planned due to the lack of time. The following are limitations with which the calorimetric measurements are done.

- The measurements are not done in thermally steady state condition.
- The ambient temperature is also not accurate as it was not done in a calorimetric box.
- Since it is not done inside a calorimetric box there is some convective heat transfer to the ambient which could not be measured.
- The sensors were not calibrated properly due to lack of time.

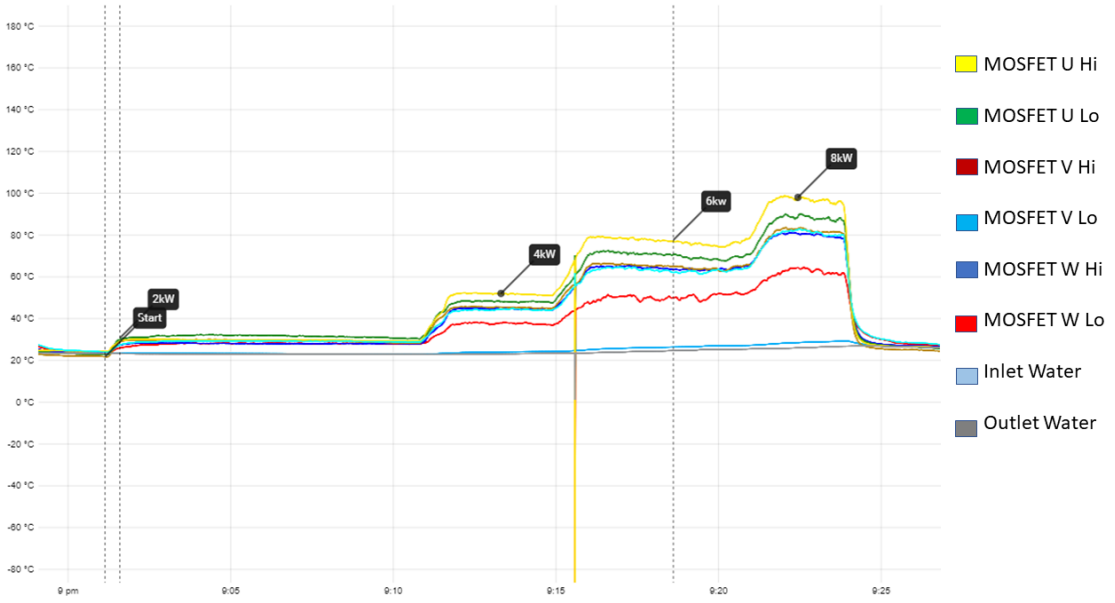


Figure 5.24: Temperature plot for Picolog

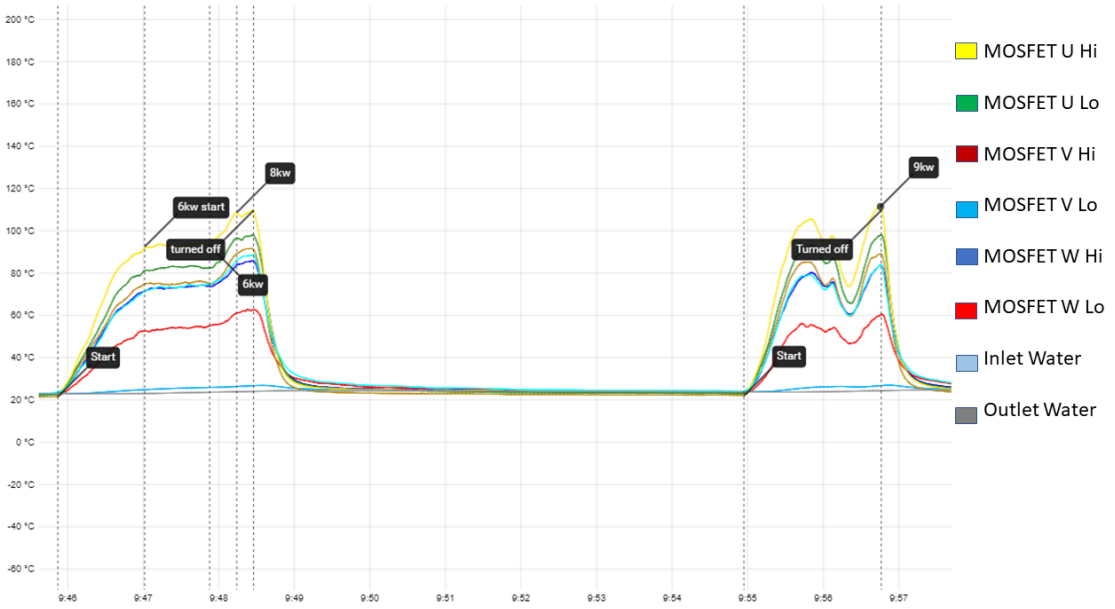


Figure 5.25: Temperature plot for Picolog

From the above two Figures 5.24 & 5.25 the water inlet and outlet temperature is noted down for the different operating points. Using these difference in the temperature values the power loss is calculated using the equations defined in Section 2.6. The Power loss calculated is summarised in Table 5.7.

Table 5.7: Calorimetric Power loss

Power (kW)	Flow Rate (L/min)	OutTemp (°C)	InTemp (°C)	ΔT	Power Loss (W)
2	2	23.21	22.71	0.5	69.8
6	2	25.76	23.70	2.1	293
8	2	25.99	23.59	2.4	335
9	2	26.71	24.16	2.55	356

5.5 Comparison of theoretical and practical

In this section comparisons are done between the various theoretical and practical measurements to validate the Theoretical loss models.

5.5.1 Electrical Measurements

A comparison between the theoretical and practical losses was done to see if the theoretical loss model of inverter matched with the practical inverter Loss measurement. It can be seen that there is around 16 W difference in the theoretical and practical power loss values. The reason for this could be the following.

- Copper track resistance is expected to increase due to the temperature increase because of the high currents. Which would mean that the power loss in the

track will increases
- The gate driver losses are also expected to vary with temperature, which also is not considered in the calculation

Overall it could be seen that there is around 0.1 - 0.7% difference between the practical and theoretical efficiency values, This can be seen from the Table 5.8.

Table 5.8: Comparison between Theoretical & Practical Loss

Input Power (kW)	Theoretical Loss (W)	Practical Loss (W)	Difference (W)	Theoretical Eff. (%)	Practical Eff. (%)
2.27	65	80.74	15.7	97.1	96.4
6.46	290.5	306	15.5	95.5	95.26
8.30	359.4	373	13.6	95.5	95.6
9.02	388.4	401	12.6	95.7	95.55

5.5.2 Thermal Measurements

A comparison between the Theoretical and practical Temperatures on the MOSFET's is done. Taking the Theoretical temperature values from from Section 4.2 and Practical Temperature values from Section 5.3.3. It is consolidated in Table 5.9.

Table 5.9: Comparison between Theoretical and Practical MOSFET Temperatures

Operating Point	Theoretical Temp.	Practical Temp.	Difference
2 kW	37 °C	32 °C	5 °C
6 kW	85 °C	94 °C	9 °C
8 kW	92 °C	108 °C	16 °C
9 kW	100 °C	112 °C	12 °C

Form Table 5.9 it can be seen that the difference in MOSFET temperature between the Theoretical and Practical values are quite similar and the maximum difference is around 16 °C, This could be explained by the following reasons

- The Heat transfer form the Power cables to the MOSFET's.
- The Heat transfer from the Driver circuit.
- Ambient Temperature practically is not the same as theoretical assumption.

So it can be assumed that the Theoretical Thermal model is quite similar to practical model. To make this thermal model more accurate all the above mentioned details need to be taken into account in the thermal model.

5.5.3 Electrical Vs Calorimetric

Here a comparison between the losses measured using the practical measurements and calorimetric measurements are done. The Practical loss values are taken from

Section 5.5.1, The calorimetric values are taken from section 5.4. These values are consolidated in the Table 5.10.

Table 5.10: Comparison between Practical and calorimetric losses

Operating Point (kW)	**Practical Losses (W)**	**Calorimetric Losses (W)**	**Difference (W)**
2	80.74	69.8	11
6	306	293	13
8	373	335	38
9	401	356	45

Due to the lack of time the calorimetric measurements could not be done inside a calorimetric box. As a consequence it can be seen that the difference in losses is very high, this is due to the fact that some of the heat got transferred through natural convection from top side of the PCB, hence not all the heat was transferred through the cooling water. Also considering the fact that the thermal grease between the PCB and the Heat sink was not applied properly which means that the thermal Resistance between the PCB and the Heat sink increased which means that some heat was lost there and could not be transferred to the Water. All these together contribute to the high difference in Power loss values between Practical and Calorimetric measurements.

6

Conclusion

6.1 Accomplishments

The final prototype of the inverter is realised within the time scope and is working as expected. The peak power measurement's were unfortunately not carried out due to a damage caused on the PCB due to a control error, however, the inverter achieved close to the continues intended operating point of 10kW. A maximum RMS current of 220.36 A is recorded during the 9kW operation. It is possible to achieve the peak operating point as the data-sheet of the MOSFET shows that each MOSFET can handle up-to 300A each, there are two in parallel. By improving the Power Cables and Connectors it is possible to achieve this operating point.

The theoretical loss analysis model is realised as intended. Most of the losses that occurred in the practical measurements is accounted for in the theoretical model and it was seen that the practical and theoretical results were close to each other. There is some small difference in the loss calculations which were due to some uncertainties in the operating conditions. This is not studied in detail due to the lack of time.

The thermal loss analysis model is realised as intended as well. It is seen that the thermal values predicted by the theoretical model was close to the practical measured values. Some losses like the DC link loss and thermal loss due to mutual thermal interactions between the components and other external components like the heat transfer from driver circuit and cables were not accounted for in the thermal analysis model due to lack of time.

The calorimetric loss analysis was not realised as expected due to the lack of time. But still attempts were made to perform simple open calorimetric measurements. There were a lot of deviations in the calorimetric loss values from the practical loss values. This was due to the fact that the calorimetric measurements are quite sensitive and need to be conducted in a controlled environment, which could not be done due to lack of time and resource.

6.2 Sustainable Development and Ethics

The EU has set strict CO_2 emission standard for cars and vans. To meet this standard the car manufacturers are shifting from combustion engine cars to electrified cars. The mild hybrid concept is one such alternative solution from the car manufacturers to achieve these targets. One interesting topic to discuss is whether these vehicles will run on electricity produced by unsustainable sources like fossil fuels

or burning coal. As the number of electric car increases the demand for electricity will increase and this will lead to pressure on the national grid to produce more energy, if the non renewable sources are used to produce energy this might again lead to carbon dioxide emission. The motors and batteries used in the cars contains neodymium magnets and Lithium respectively. The extraction of these metal have proven to be unsustainable and puts pressure on the environment. A comparison between the electric cars and the conventional cars proves that electric cars doesn't emit harmful gases like Notorious Oxide, sulphur dioxide and lead that are emitted by combustion engine cars. The electric cars produce less noise compared to combustion engine cars. Renewable energy such as wing, hydro etc. should be used to produce the energy required to meet the demands of the electric vehicles.

6.3 Future Scope

The most important future activity are as follows:

- A More detail COMSOL analysis specially designing the water flow in the heat sink and analysing various flow rates.
- Proper calorimetric measurements inside the calorimetric box and properly calibrated sensors.
- Proper connectors to connect the power cables. The one chosen for this project was too small due to unavailability of components.
- Manufacturing a PCB with thicker copper tracks to reduce the losses.
- Using GanFET's to make the inverter more compact and efficient.
- Validate electrical measurement's using more precise equipment's like yokogawa power analyzer.
- Including the DC capacitor losses into the COMSOl Analysis.
- More precaution while applying thermal paste to make it a very fine layer.
- Better cooling system if the power levels needs to go higher.
- Proper cooling for driver circuits.

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A

Appendix 1

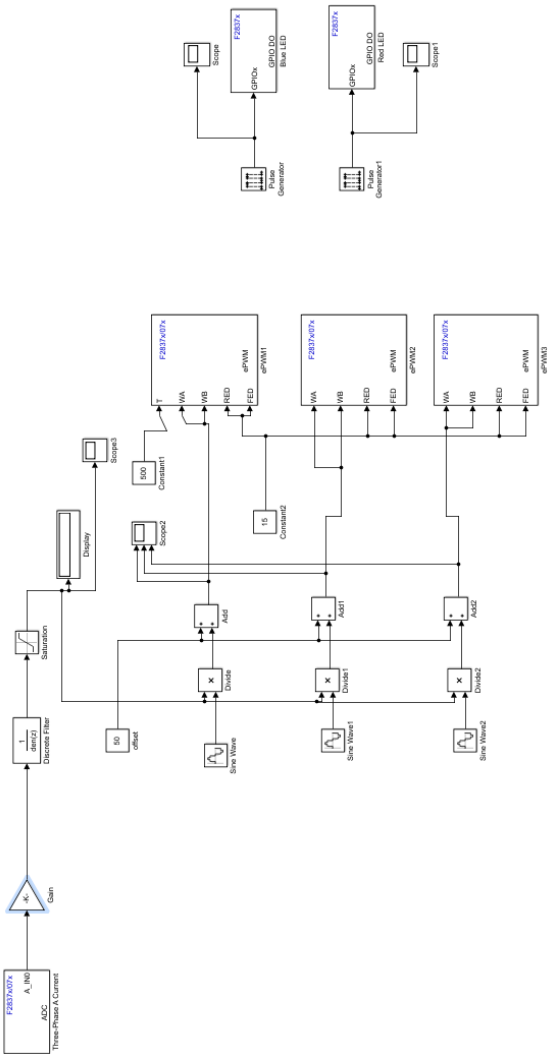


Figure A.1: TI Control circuit

TEXAS INSTRUMENTS
UCC27200, UCC27201
SLUS746C – DECEMBER 2006 – REVISED APRIL 2016

UCC2720x, 120-V Boot, 3-A Peak, High Frequency, High-Side and Low-Side Driver

1 Features

- Drives Two N-Channel MOSFETs in High-Side and Low-Side Configuration
- Negative Voltage Handling on HS (–5 V)
- Maximum Boot Voltage of 120 V
- Maximum VDD Voltage of 20 V
- On-Chip 0.65-V VF, 0.6-Ω RD Bootstrap Diode
- Greater than 1 MHz of Operation
- 20-ns Propagation Delay Times
- 3-A Sink and 3-A Source Output Currents
- 8-ns Rise and 7-ns Fall Time With 1000-pF Load
- 1-ns Delay Matching
- Undervoltage Lockout for High-Side and Low-Side Driver
- Specified from –40°C to 140°C

2 Applications

- Power Supplies for Telecom, Datacom, and Merchant Markets
- Half-Bridge Applications and Full-Bridge Converters
- Isolated Bus Architecture
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- High-Voltage Synchronous-Buck Converters
- Class-D Audio Amplifiers

3 Description

The UCC2720x family of high-frequency N-channel MOSFET drivers include a 120-V bootstrap diode and high-side and low-side drivers with independent inputs for maximum control flexibility. This allows for N-channel MOSFET control in half-bridge, full-bridge, two-switch forward, and active clamp forward converters. The low-side and the high-side gate drivers are independently controlled and matched to 1 ns between the turnon and turnoff of each other.

An on-chip bootstrap diode eliminates the external discrete diodes. Undervoltage lockout is provided for both the high-side and the low-side drivers forcing the outputs low if the drive voltage is below the specified threshold.

Two versions of the UCC27200 are offered. The UCC27200 has high noise immune CMOS input thresholds while the UCC27201 has TTL compatible thresholds.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC2720x	SOIC (8)	3.91 mm × 4.90 mm
	SO PowerPAD™ (8)	3.90 mm × 4.89 mm
	VSON (8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram

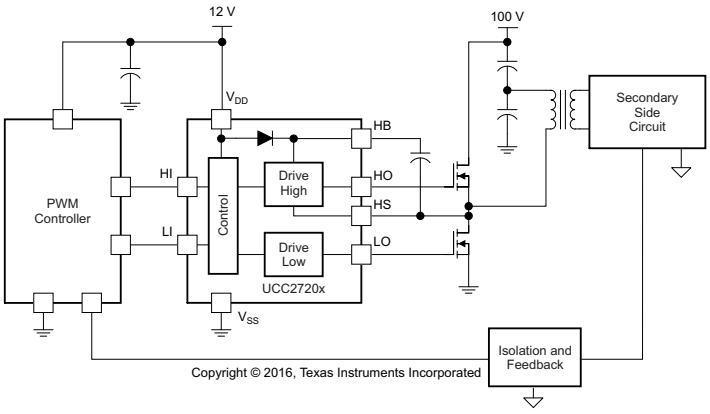


Figure A.2: Gate Driver IC

IAUT300N10S5N015

OptiMOS™-5 Power-Transistor

AEC Qualified

RoHS

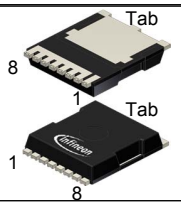
Product Summary

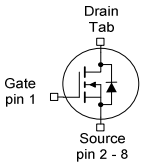
V_{DS}	100	V
$R_{DS(on)}$	1.5	mΩ
I_D	300	A

Features

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested

P/G-HSOF-8-1





Type	Package	Marking
IAUT300N10S5N015	P/G-HSOF-8-1	5N10015

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25°C, V_{GS}=10V[1)]	300	A
		T_C=100 °C, V_{GS}=10 V[2)]	247	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C	1200	
Avalanche energy, single pulse[2)]	E_{AS}	I_D=150 A	652	mJ
Avalanche current, single pulse	I_{AS}	-	300	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25 °C	375	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Figure A.3: Infenion MOSFET

Input Power	Current	Other Loss	Mosfet Conduction	Mosfet Switching	Total Losses theor	Eff Theor	Eff Prac
20kW (20000)	420 A	181.3 W	1026 W	82.4 W	1289.7 W	93.55 %	93.0 %
18kW (18000)	378 A	149.5 W	835 W	75 W	1059 W	94.7 %	94.1 %
16kW (16000)	336 A	121 W	657.3 W	67.6 W	846 W	94.7 %	94.1%
14kw (14000)	294 A	96 W	510.3 W	60.2 W	666.5 W	95.2 %	94.6 %
12kw (12000)	252 A	74.2 W	375.7 W	52.8 W	502.7 W	95.8 %	95.2 %

Figure A.4: Expected results for higher power operating points