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Design and performance comparison of Two-level and Multilevel Converters for HVDC Applications

Master's Thesis in Electric Power Engineering

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Switchyard of the Trans Bay Cable HVDC Project in San Francisco.
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Reference to more extensive information [www.energy.siemens.com], [www.transbaycable.com]

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Abstract

The purpose of this thesis is to compare a two-level and a multilevel converter for HVDC substation. For this study, both topologies were designed with different modulation strategies and compared on the basis of size, power losses and impact on power quality.

The model of a basic substation was built in MATLAB, and a 450MVA converter was modeled for different topologies and modulation techniques. Further, the total losses of the converter were computed using different voltage/current ratings of the modules in order to derive a performance comparison. In addition to the evaluation of losses, the impact on the power quality was also analyzed for the multilevel converters.

The results of the thesis revealed that, if harmonic emission without the need of external filters is the main criteria then, a twenty-three level converter with a modular structure could be used. The value of the output current THD in case of the twenty-three level converter is 0.52% which is well within the power quality standards and excludes the use of filters.

The losses for a three level modular converter were found to be lower than the two-level converter (0.59% versus 1.14%). Also, the use of a 4.5kV module presented the lowest losses compared to other module ratings (2.5kV-6.5kV), for all converter topologies.

Keywords: HVDC, Voltage Source Converters, Modular Multilevel Converter, Selective Harmonic Elimination, Total Harmonic Distortion.

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We would like to thank our supervisors Professor Torbjörn Thiringer and Dr. Massimo Bongiorno for giving us their timely input and guidance throughout the project.

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Table of Contents

Notations

Symbols

E_{off}	Turn-off energy	[J]
E_{on}	Turn-on energy	[J]
L	Inductance	[H]
M	Modulation index	-
P_{cond}	Conduction loss	[W]
P_{switch}	Switching loss	[W]
R	Resistance	[Ω]
R_{on}	On-state resistance of the IGBT	[Ω]
$\hat{U}_1$	Amplitude of the fundamental voltage component	[V]
U_{dc}	DC voltage	[V]
V_{ce}	On-state voltage drop of the IGBT	[V]
V_f	Forward voltage of the IGBT	[V]
f	Frequency	[Hz]
f_1	Fundamental frequency	[Hz]
f_{sw}	Switching frequency	[Hz]
i	Current	[A]
m_a	Amplitude modulation	-
m_f	Frequency modulation	-
n	Number of levels	-
t	Time	[sec]
v	Voltage	[V]
v_c	Capacitor voltage	[V]
v_{conv}	Converter output voltage	[V]
v_{grid}	Grid voltage	[V]
α	Firing angle	[deg]
δ	Power angle	[deg]
ω	Angular frequency	[rad]

Abbreviations

CSC	Current Source Converter
Dn	Individual Harmonic Distortion
HVDC	High Voltage Direct Current
IGBT	Insulated-gate Bipolar Transistor
M2C	Modular Multilevel Converter
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
PWM	Pulse Width Modulation
SHE	Selective Harmonic Elimination
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
SOA	Safe operating Area

1. Introduction

1.1. Background

With the continued increase of power and voltage levels, stress on cost effective solutions and stringent guidelines for power quality, multilevel converters have emerged as a technically viable solution for accomplishing acceptable standards. The term 'Multilevel' has been coined to emphasize the ability to increase the instantaneous voltage levels in steps, accomplished by addition of components in series. The basic topologies that have been studied so far are namely: Diode Clamped, Flying Capacitor, Cascaded H-bridge and the Modular Topology. Although the different topologies offer a variety of advantages, they however, also possess some limitations with further increase in voltage levels.

1.2. Previous Work

Recent advances in technology have realized the diode clamped topology to have a considerable reduction in switching losses and the ability to control the harmonic content. Currently several projects by ABB have also been implemented utilizing this topology. Along with the inherent advantages, the diode clamped topology also suffers from the use of additional components leading to more power losses, implying higher costs. On the other hand, the flying capacitor topology, which offers more flexibility in voltage synthesis in comparison to the diode clamped, suffers from the use of large number of capacitors with increasing levels and the complexity of control and high losses [1]. The cascaded H-bridge topology has the inherent advantage of utilizing minimum number of components and the ease of connecting the individual H-bridges in series to generate a stepped voltage waveform. However, it requires the use of isolated dc sources and hence its applications are somewhat limited. Further modifications to the existing topologies have resulted in a Hybrid approach for VSC transmission. The hybrid arrangements have distinct advantages over their classical counterparts and present a wide scope for application in HVDC transmission.

Another important topology that has currently been implemented by Siemens in HVDC is the Modular multilevel converter or M2C [2]-[3]. The modular approach is simpler than the cascaded H-bridge in terms of its extension to higher number of levels. With higher levels of a modular multilevel converter, the filter requirement at the output is greatly reduced, as the THD levels are extremely low.

1.3. Purpose

The purpose of this study is to analyze the operation of a Two-level converter and the modular multilevel converters considering PWM and selective harmonic elimination modulation strategy. Important objectives are to establish the effects of increase in the switching frequency and the number of levels on the power losses, size of the converter and the filter requirements in order to obtain the desired output current THD.

2. Introduction to VSC-HVDC

2.1. Features

Classical HVDC or Current sourced converters (CSC) involves the use of thyristor technology for transfer of power. Currently, the CSC technology is widely used for bulk transmission of power. VSC-HVDC being relatively new compared to CSC possesses some important features such as:

- Use of IGBT's which offer a faster response.
- Independent control of active and reactive power.
- Black start capability.
- Can be connected to weak ac grids.
- Bi-directional power transfer by changing the direction of current.

VSC-HVDC poses as a viable solution for large projects considering the overall cost associated.

Figure 1 shows the main components of a standard VSC-HVDC station up till the point of common coupling (PCC) [5]. On the dc side, a dc capacitor is provided to stabilize the dc voltage. With higher switching frequencies, the size of the dc capacitor is reduced, as with every switching action of the valves the direction of current in the capacitor reverses, thereby reducing the effective ripple. The converter unit comprises of series connected IGBT's with antiparallel diodes which provide a high voltage withstand capability. The presence of a coupling reactance or phase reactor helps to stabilize the ac current and reduce the current harmonics arising due to the switching operation of the converter. The ac side is also provided with ac filters to remove high frequency harmonics from the output.

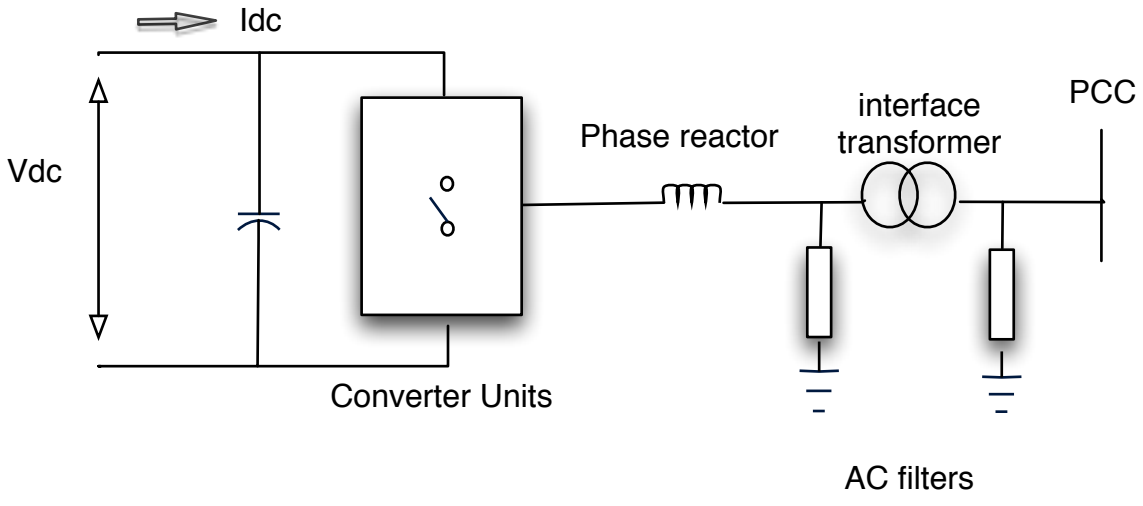

Figure 1: A typical VSC-HVDC station showing the various components

2.2. Devices (IGBT's/Diodes)

With recent advances in semiconductor technology, IGBT's and diodes of a rating up till 6.5kV have been introduced. In HVDC applications, since the valves experience the entire dc voltage, the rating of the components required is high. The diodes in the module must have a rating comparable to that of the IGBT, as in case of DC short circuit faults or during VSC energizing they will experience a large inrush current.

In the voltage source converter, a series chain of IGBT modules are used which can withstand the high voltages in an HVDC system. Also high number of parallel-connected devices is used in order to withstand higher power levels. For example, the number of valves used in a 150kV HVDC light project has been around 300 valves [5]. A typical module comprising of an IGBT with an antiparallel diode is shown in Figure 2 below.

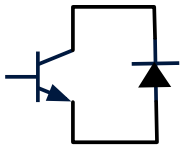

Figure 2: Module comprising of an IGBT and a Diode

A series chain of such modules also poses a requirement of good voltage sharing capabilities among the individual modules. In this project it has been assumed that the modules possess sufficient voltage-sharing capabilities. Voltage sharing can be achieved, for instance, by means of adding a resistor in parallel per module.

Also, during operation, the modules are not stressed equally and there exists a temperature difference or a gradient among the different modules. This temperature difference causes a delay in the response of the IGBT's during turn-off and turn-on. Keeping in view such factors, a snubber capacitor and a di/dt inductor are normally provided for effective voltage sharing. With high switching frequencies the power losses in the valves also increases. A di/dt limiting inductor is also provided to limit the turn-on losses [5].

During normal operation of the VSC, the IGBT should continue operating even if there exists a faulty module. This means that the faulty IGBT should act as a short circuit so that it does not impede the normal operation.

2.3 Industry of VSC-HVDC

In the last years two major companies have been at the forefront of the research and development of VSC-HVDC implementing both two-level and multilevel converters. HVDC Light® and HVDC PLUS® were released as product names of VSC-HVDC technologies from the companies ABB and Siemens respectively [6]-[7].

The most noticeable difference of the two technologies is the topology implemented for multilevel converters. So far ABB has used diode-clamped three-level converters, and Siemens has now developed the modular multilevel topology, which provides the benefit of increase in instantaneous voltage steps by use of higher number of submodules per converter

arm. For example, the 400MW Trans Bay cable project carried out by Siemens in 2010 utilizes 200 submodules per converter arm [30].

3. Voltage Source Converters

3.1. Two-level Converter

3.1.1. Features

The two-level converter has been widely used for a range of power levels. Some examples include the Gotland HVDC light, commissioned in 1999 in Sweden (50MW, ±80kV) and Hellsjön (3MW, ±10kV) [8]. The schematic of the topology is shown in Figure 3 below. It is capable of producing two output voltage levels namely $+U_{dc}$ and $-U_{dc}$. The crude ac waveform obtained has a high harmonic content [9].

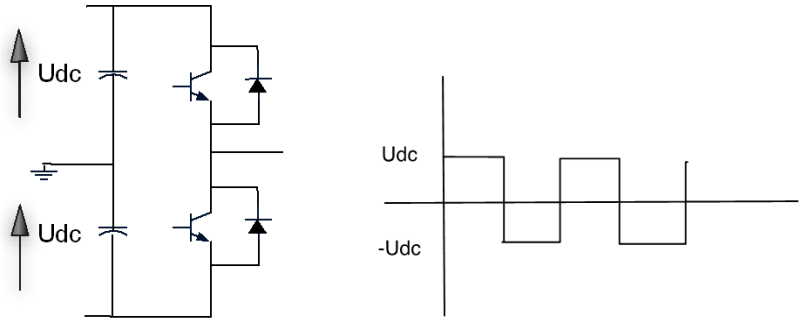

Figure 3. Single Phase leg of a Two level Converter and the ac output waveform.

Some advantages of a two-level converter include:

- Simple circuitry.
- Small size of dc capacitors.

Although the two-level topology offers some advantages there are certain limitations that also need to be considered, such as:

- The valves experience a very high voltage and hence they need to be rated with high blocking voltage capabilities.
- The crude ac waveform obtained contains a lot of unwanted harmonics. The switching frequency can be increased to push the harmonics to higher frequencies using PWM, but this leads to higher switching losses in the converter.

With increase in power ratings, more number of switches needs to be added in series. Simultaneous switching of a series chain of IGBT's becomes complex, as there may occur a delayed switching owing to heating of the devices. Hence, the concept of multi-level converters was introduced. It gave flexibility in switching the devices independently and at lower frequencies. Different topologies have been developed and a lot of research is being done in improving the overall performance of the converter to provide an output of high quality [1], [10].

3.2. Multilevel Topologies

3.2.1. NPC Diode Clamped Converter.

Figure 4 shows the schematic of the NPC and the 3 level output waveform.

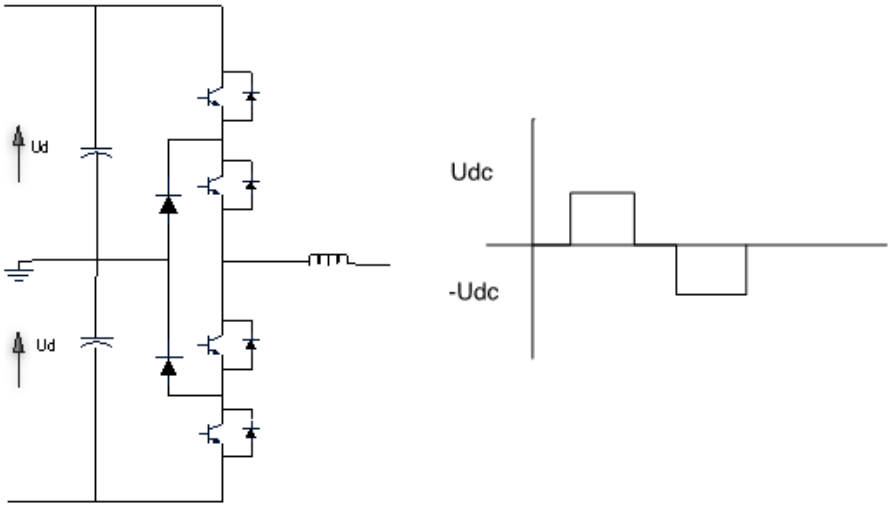

Figure 4. Phase leg of a 3 level Neutral point Clamped (NPC) Converter and its ac output waveform.

An n level diode clamped converter comprises of n-1 capacitors on the dc bus and produces n levels of phase voltage and 2n-1 levels of output line voltage. Some additional features include:

- High voltage rating of blocking diodes is required.
- Unequal device rating leading to different current ratings of devices.
- The output waveform has a better harmonic content compared to the Two - level.
- Suffers from capacitor voltage unbalance problem.
- The number of clamping diodes required increases with increase in the number of levels and increases complexity.

An example of implementation of this topology is Eagle Pass USA, commissioned in 2000 (36MW, ±15.9kV) [8].

3.2.2. Capacitor-Clamped or Flying capacitor Converter.

A single phase of a 3 level capacitor clamped converter is shown in Figure 5.

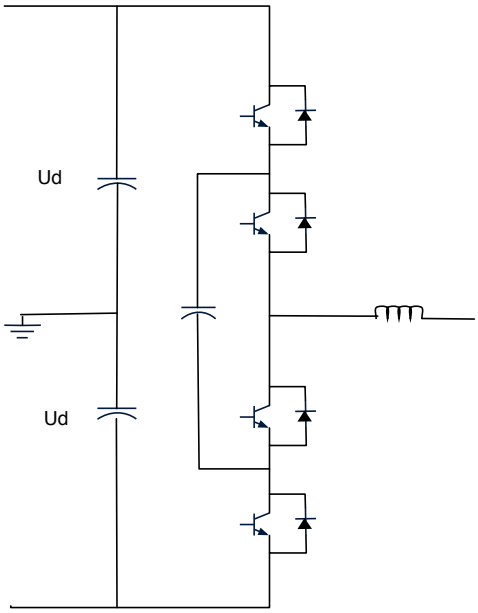

Figure 5. Capacitor Clamped or Flying capacitor Converter.

Compared to the diode clamped, the capacitor clamped converter comprises of a large number of capacitors called 'floating capacitors'. As the number of levels increases, the number of capacitors also increases. The use of such large number of capacitors does provide ride through capabilities during outages, but in turn also increases complexity in control and cost. Hence, this topology finds its use in large motor drives applications [5] [1]. The voltage synthesis in case of the capacitor clamped converter has more flexibility than the diode clamped converter. This topology also suffers from unequal duty problem of the switches.

3.2.3. Cascaded Multi-Level Inverter

A single phase of an n- level cascaded H-bridge structure with separate DC sources is shown in Figure 6.

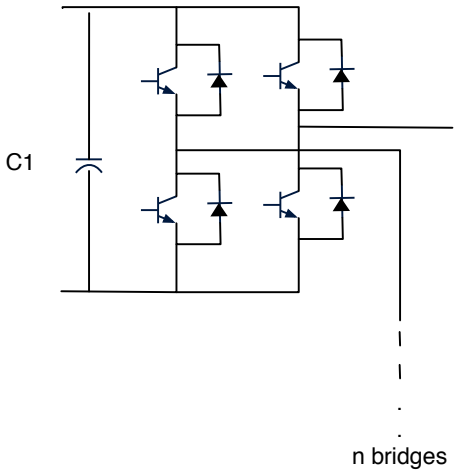

Figure 6. Single phase cascaded H-Bridge structure.

A single H-bridge structure is capable of producing three voltage levels, namely $+U_{dc}$,*0*, $-U_{dc}$. A series connection of these individual bridges yields a staircase output waveform wherein each step corresponds to each individual bridge. To obtain higher levels in the output waveform, more H-bridges need to be connected. Typically for an n level converter, (n-1)/2 H-bridges are required per phase. Some of the advantages associated with this topology are summarized below [11]:

- It requires the least number of components compared to the other topologies for the same voltage level required.
- It possesses a modularized circuit layout and does not require any extra diodes or clamping capacitors.

The disadvantage of such a topology is the requirement of separate DC sources hence making it difficult for extending to higher levels.

3.2.4. Modular Multilevel Inverter (M2C)

Figure 7 shows a single-phase leg of a 3 level modular Topology.

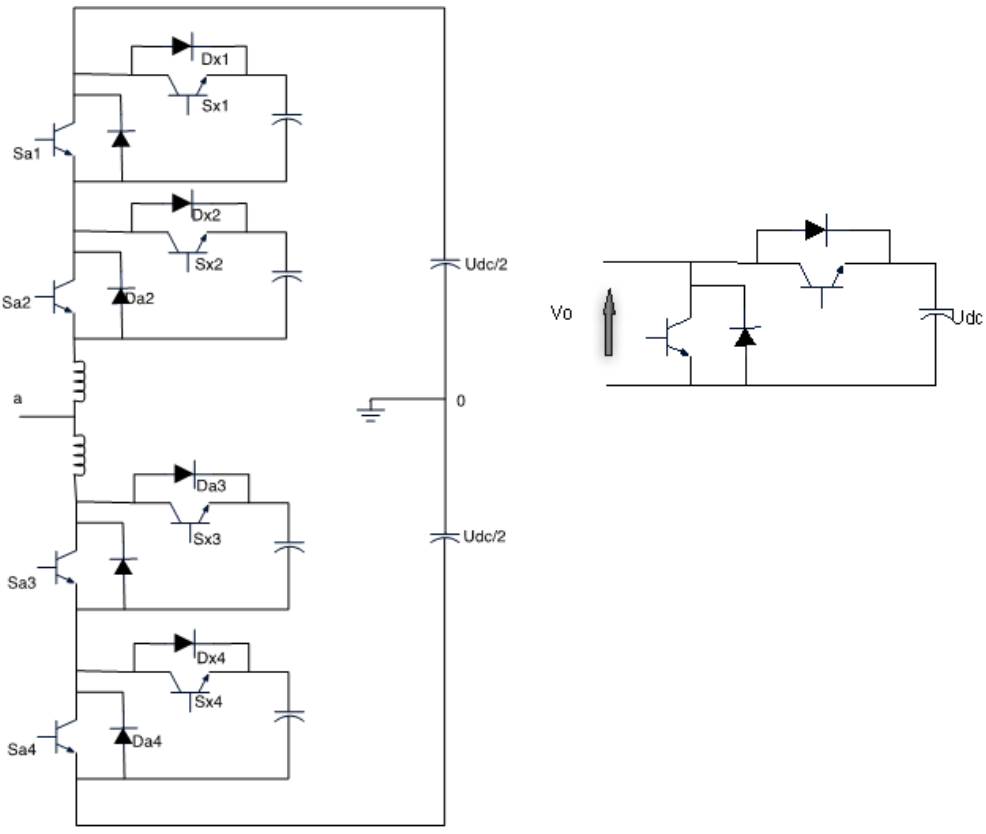

Figure 7. Phase leg of a 3 level Modular structure and the structure of one cell.

The modular topology is simpler than the cascaded H-bridge structure. A single cell comprises of two switches; the main switch and the auxiliary switch. The output voltages obtained from a single structure are $+U_{dc}$ and *0*. No $-U_{dc}$ state is possible as the case with cascaded H-bridge structure. During the 0 level state, the capacitors charge or discharge

depending upon the direction of the load current and hence a slight imbalance is created. The voltages of the capacitors are controlled by controlling the switching-in of the different cells during the 0 voltage output. The inductances in the arms provide a path for the circulating currents during the balancing process and limit the inrush currents. The modular nature of this topology offers an advantage as higher levels and hence higher voltages can be achieved by stacking the cells together. With higher number of sub-modules, the M2C can be operated without the use of filters, which is a significant advantage over its other multilevel counterparts [2].

3.3. Control and Modulation Strategies

3.3.1. Sinusoidal Pulse Width Modulation (SPWM)

Figure 8 shows the SPWM strategy.

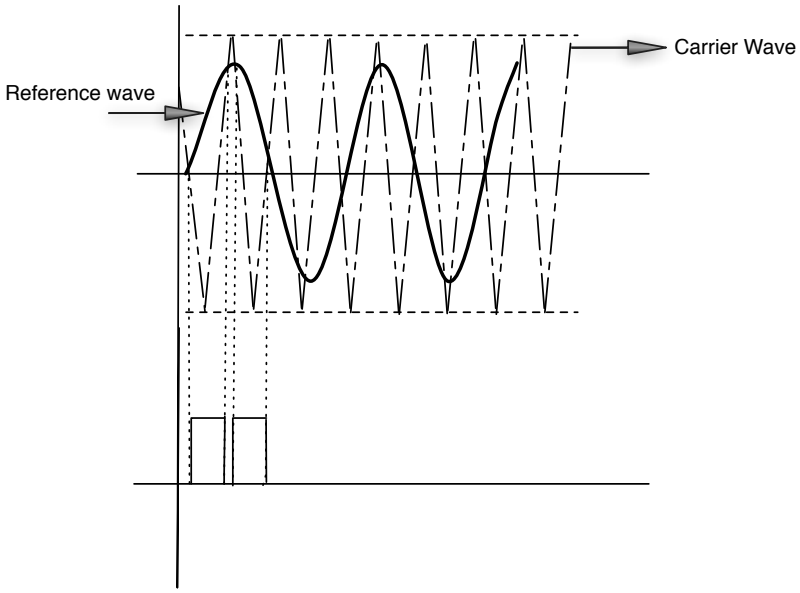

Figure 8. Pulse Width Modulation.

In the sinusoidal pulse width modulation or SPWM, a carrier wave (triangular wave) is compared with the reference wave [9]. The reference wave corresponds to the desired fundamental frequency at the output and the triangular wave determines the frequency with which the valves are switched. When the reference wave is higher than the carrier wave, a switching pulse is generated and the switch is turned on. Likewise, during the period when the carrier wave is greater than the reference, the switch is off. By changing the frequency of the carrier wave, higher switching frequencies can be obtained. The carrier frequency should always be an odd multiple of 3 as this provides a half and quarter wave symmetry thereby eliminating the even harmonics and generation of symmetrical three-phase voltages. The frequency modulation index f is defined as the ratio of the switching frequency and the fundamental frequency.

$$m_f = \frac{f_{sw}}{f_1} \tag{1}$$

3.3.2. Selective Harmonics Elimination (SHE)

Figure 9 shows the implementation of the SHE method for three delay angles (α1, α2, α3) per quarter wave.

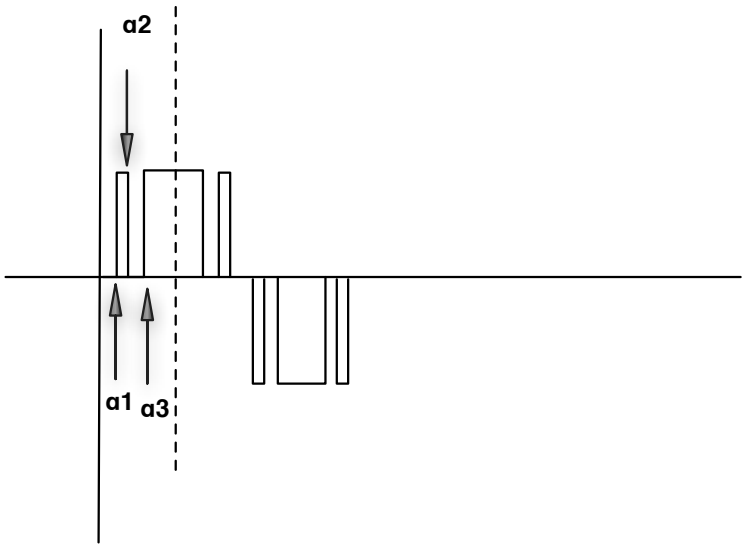

Figure 9. Selective Harmonic Elimination.

The selective harmonic elimination method is used to eliminate selected harmonics from the voltage wave and also control the fundamental output. In this method, at any fundamental switching frequency, a voltage reversal or a chop is provided. With every n chops or voltage reversals, one chop is used for controlling the fundamental and the rest n-1 chops are used for eliminating the harmonics. The delay angles $\boldsymbol{\alpha_{1-n}}$ are calculated solving a set of non-linear equations [12]. For instance, to control the fundamental and simultaneously eliminate fifth and seventh harmonics we will need three values of α (α1, α2, α3). Figure 9 shows three chops in the voltage wave in a quarter wave period. The values of α can be obtained from the set of non-linear equations as shown below:

$$\cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) = \frac{4}{\pi}\mathrm{M}$$

$$\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) = 0$$

$$\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) = 0$$

3.4. Power Quality- Standards

The IEEE Standard 519 describes the recommended requirements for power quality and harmonic control, focused on the point of common coupling (PCC) for both consumers and suppliers [13]. This standard establishes the distortion limits for different PCC voltage levels.

Two important indexes described in the standard are the individual harmonic distortion (Dn) and the total harmonic distortion (THD). The individual harmonic distortion of a specific harmonic relates its value as a percentage of the fundamental, and the THD is the root mean square of all individual harmonic distortions.

Although the allowable Dn and THD can be relatively high for low and medium voltage levels at PCC, this is not the case for FACTS and HVDC installations, because they are usually rated at high power and have a high impact on the power systems. Then more harmonic control is required in HVDC substations.

The common values that are used as limit in HVDC systems are: 1% for each individual harmonic distortion, and 2% for the THD taking up to the 50^{th} harmonic [14].

4. Design aspects of Voltage-Source Converters for HVDC applications

4.1 Two-level Converter

4.1.1 Description of the case: Setup in MATLAB

The representation of the HVDC substation is shown in the base case of Figure 10. In this basic model, a two-level converter operated as an inverter delivers active and reactive power to the grid at the point of common coupling (PCC). The rated power of the converter is 450 MVA, and the DC voltage is ±150 kV.

The converter station is connected to a strong grid through a 1:1 transformer, which has a 0.15pu reactance in this case. The grid is represented by an infinite bus with a rated voltage of 53kV-rms (75kV-peak). Some resistance is also included with a value of 0.015pu.

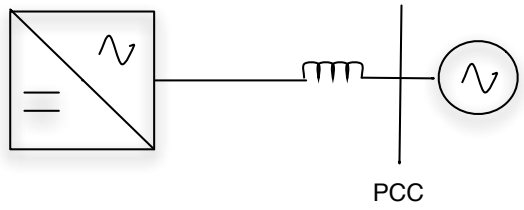

Figure 10. Base Case.

The MATLAB-Simulink interface is used for modeling. As shown in Figure 11, the converter output voltages are built by comparing three-phase reference voltages with a triangular wave. The current flowing in the system is determined by the difference of the converter voltage and grid voltage, and the magnitude of the reactor. At rated power operation, the converter output current is 2.8 kA.

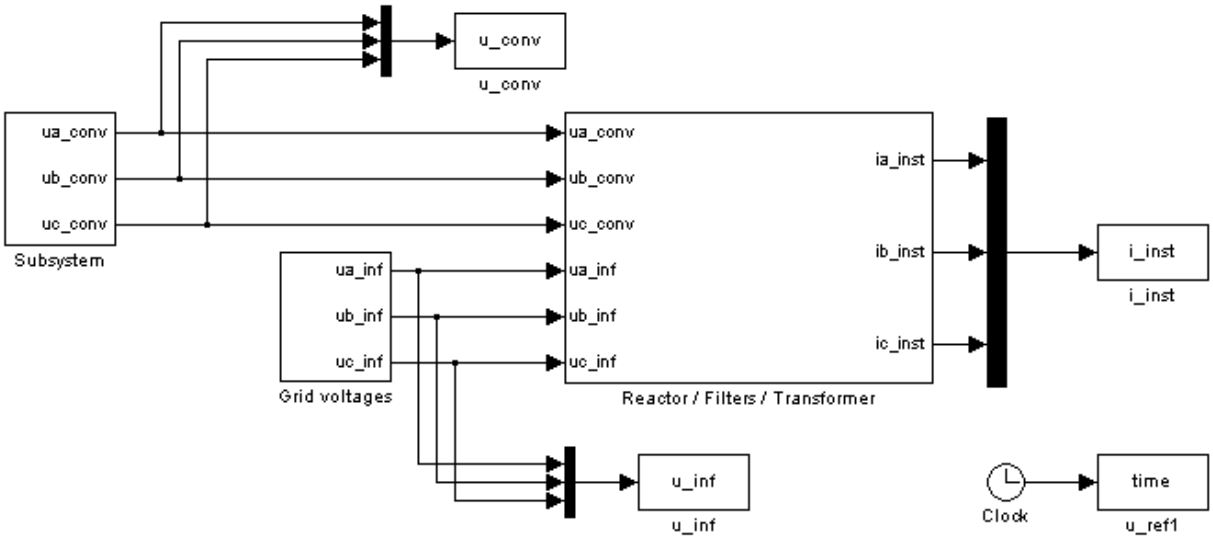

Figure 11. Simulink Model of the base case.

4.1.2 Modulation.

Different modulations strategies can be used to operate the two-level converter. In our model for HVDC applications, PWM and selective harmonic elimination (SHE) will be considered. Figure 12 shows how the converter can be controlled using PWM. In this case we have an amplitude modulation index of 0.8 and a power angle of 8.75 deg. The power angle can be varied to obtain different operation points on the converter capability curve with particular values of active and reactive power output.

Figure 12 presents the operation at a switching frequency of 450 Hz (frequency modulation mf=9). Three-phase voltage reference waveforms are compared with the triangular wave (carrier wave) and a PWM output is obtained. The grid voltage is shown in green.

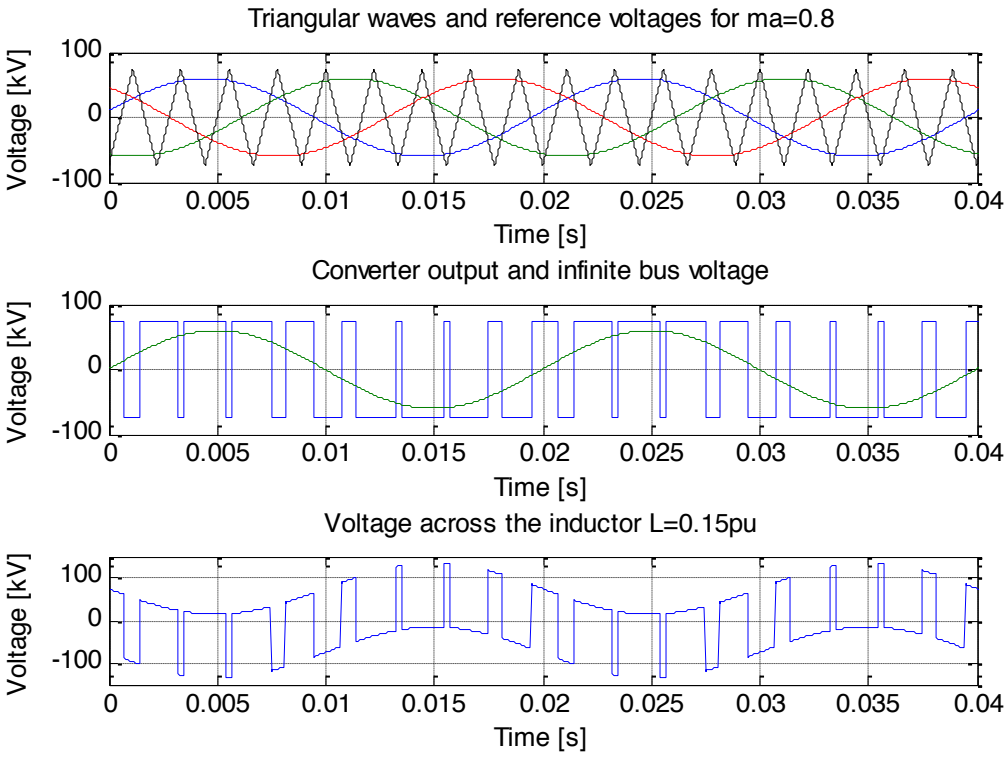

Figure 12. Example of the control of the converter using PWM.

Similarly, the selective harmonic elimination method will generate a voltage waveform varying from $U_{dc/2}$ *to* $-U_{dc/2}$, but for this strategy, the switching angles are calculated previously.

Three-phase currents are generated according to the differential equations relating voltage and current across a series connection of a resistor-inductor.

$$v_{conv} = v_{grid} + Ri + L\frac{di}{dt} \tag{2}$$

The instantaneous current calculation model for phase A is shown below in Figure 13.

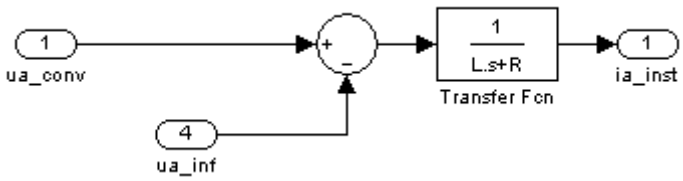

Figure 13. Instantaneous current calculation for phase A

4.1.3 Devices.

For simulation purposes the IGBT/diode modules have been chosen from the family of products of ABB Hipak TM [15]-[18].

The design and operation of the components of the converter, as well as the rating and operating parameters of power semiconductors are based in guidelines [19]-[20]. For calculating the power losses and the number of components required i.e. IGBT's, diodes, the waveforms obtained from MATLAB-Simulink and the datasheet parameters will be used [21]. The MATLAB model generates the number of components required for different levels of the multilevel converter and shows the power losses.

An assumption of working temperature of the IGBT has been taken as 125˚C and the working voltage of +55% overvoltage handling capability respectively.

4.1.4 Results.

Figure 14 shows the results for the PWM modulation when operating at rated power.

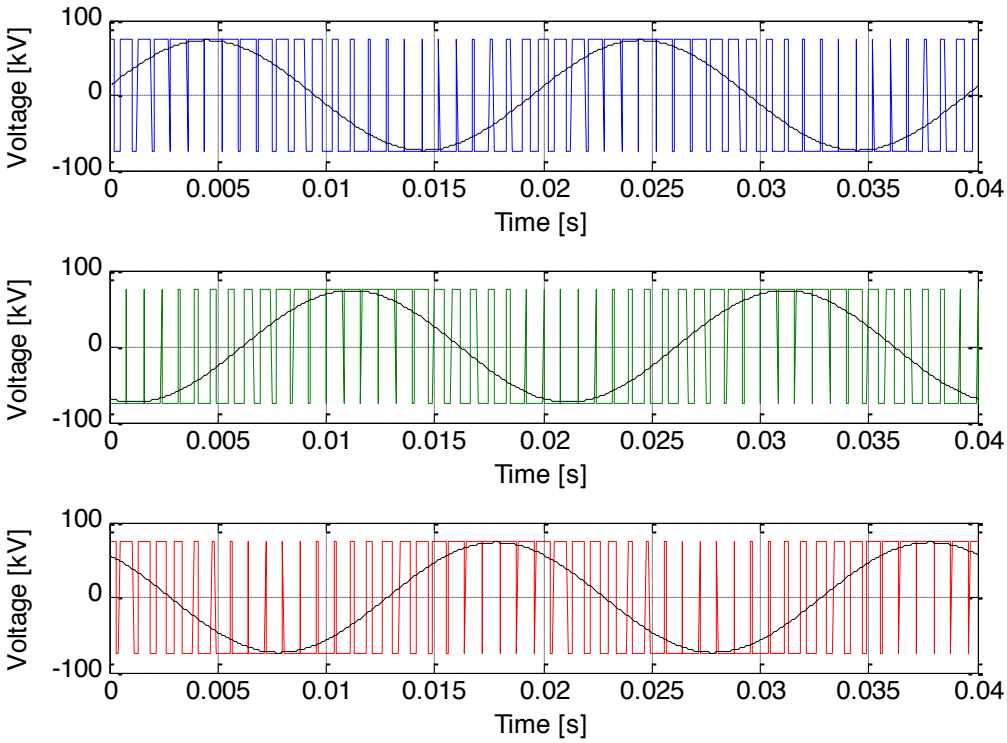

Figure 14. Three-phase instantaneous and fundamental voltages in the converter using PWM.

The chosen operating point for the simulation is the rated power. The output voltage is adjusted to be 53kV. It means that the amplitude of the ac voltage signal is 75kV, which is also half of the DC link voltage. For the PWM case the switching frequency is chosen to be 1250Hz in order to decrease the current ripple. The current waveform is plotted in Figure 15 for the PWM modulation.

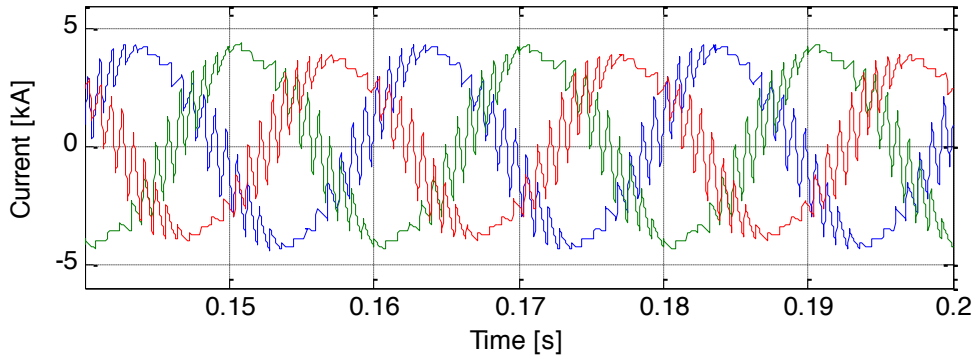

Figure 15. Three-phase currents for PWM.

When the converter is modulated using selective harmonic elimination (SHE), the three-phase voltages will look like in Figure 16. The switching frequency is 1150Hz in this case. The firing angles were computed following the SHE algorithm. A more detailed explanation and application of this modulation method is done in the further sections.

The current waveforms for the SHE case are shown in Figure 16. There are significant differences that can be noticed when comparing these waveforms with the PWM ones.

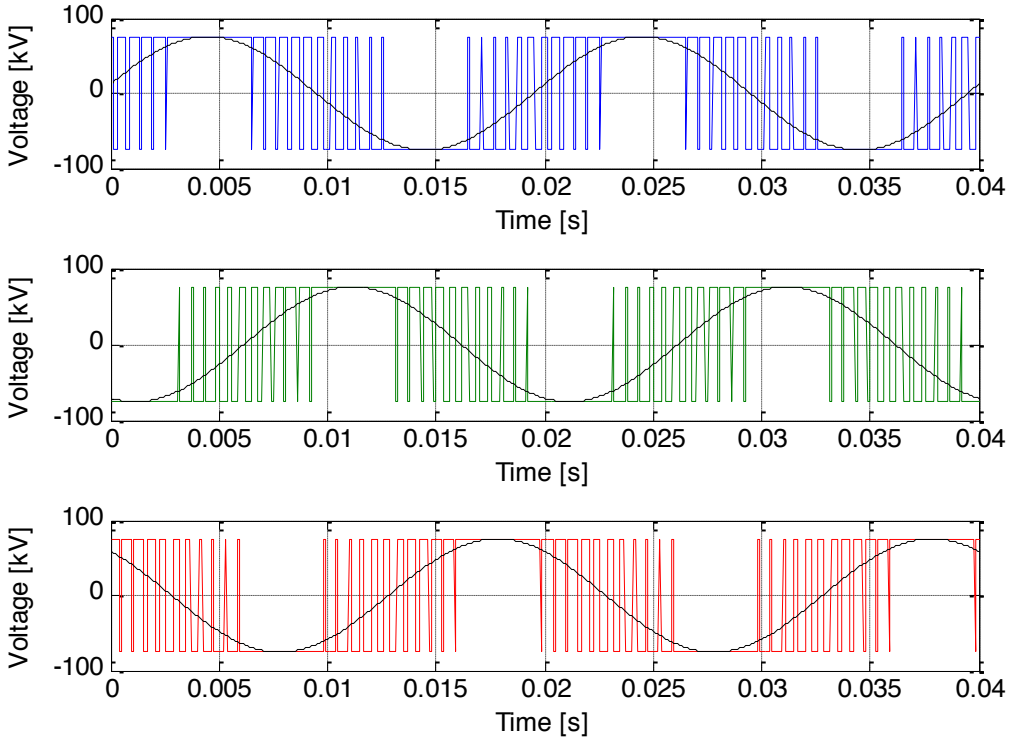

Figure 16. Three-phase instantaneous and fundamental voltages in the converter using SHE.

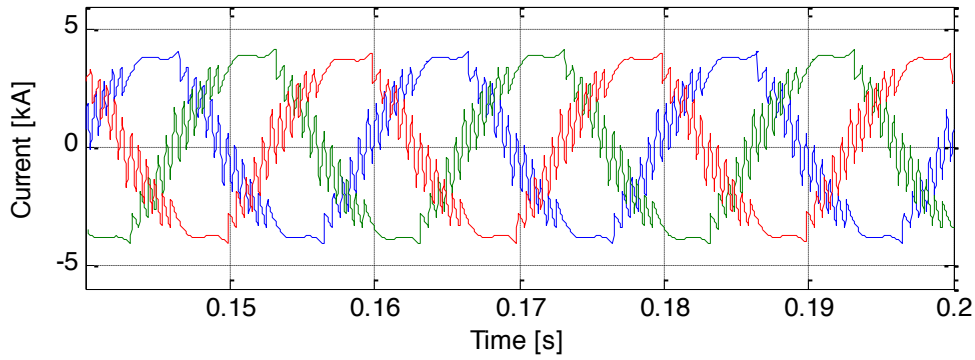

Figure 17. Three-phase currents for SHE.

Although a high switching frequency is used in the two cases, the three-phase currents contain a considerable amount of ripple, and a high total harmonic distortion (THD) is expected in both PWM and SHE simulations.

The THD of the current is directly related to the switching frequency of the converter as it affects the ripple. From Figure 18 we can see the values of the THD for both voltage and current signals when we increase the switching frequency.

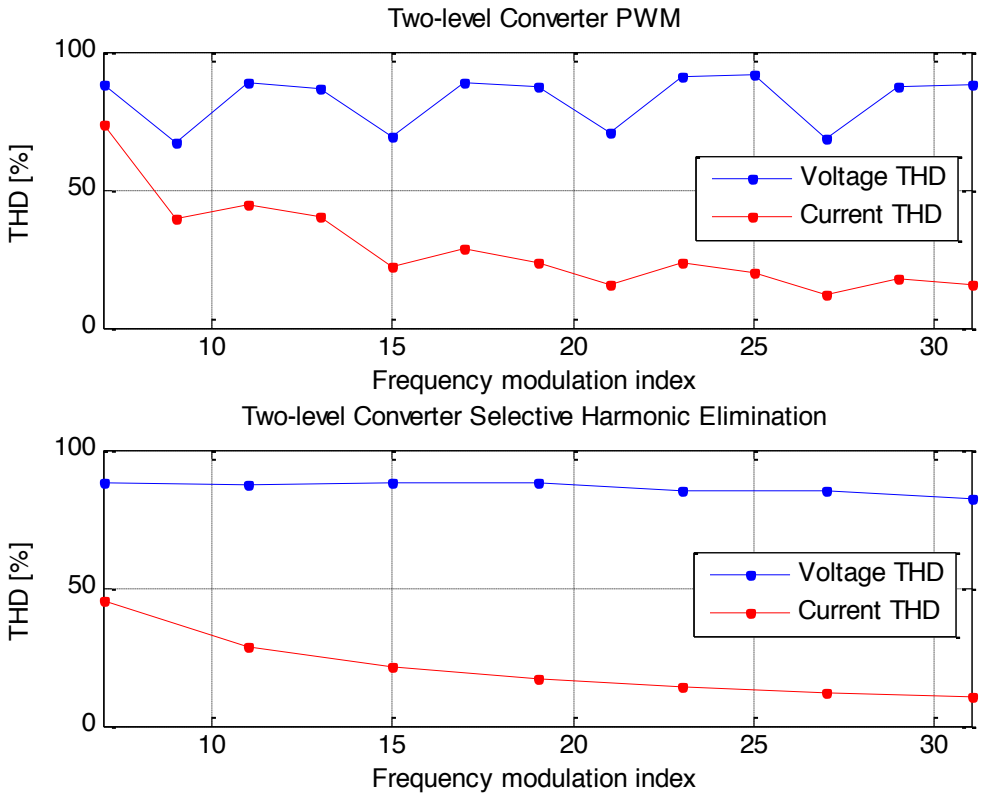

Figure 18. THD variation for a range of switching frequencies.

Although the results are different for PWM and SHE, there are common things to be noticed. The THD of the voltage signal is not improved when the switching frequency is increased. The reason is that the voltage harmonics are still there, but they were just shifted up in the

frequency harmonic spectrum. On the other hand, the current harmonics are reduced more and more when the frequency increases. This is achieved with the drawback that the switching losses increase considerably.

The current THD is relatively lower for SHE as there is a criteria that can be used for harmonic cancellation. But an interesting phenomenon can be seen when the switching frequency is chosen to be a triplen multiple of the fundamental: the current THD goes down to values equal to those of the SHE. The reason is that the most dominant harmonics have been cancelled out. It allows for us to conclude that there is no better or worse modulation strategy for the two-level converter as long as the frequency modulation is a multiple of three.

4.1.5 Power Losses

For the purposes of evaluating the power losses, the module chosen for the simulation is rated at 6.5kV and 750A [18]. The transfer characteristics for the IGBT and the diode are shown in Figure 19. A worst case temperature of 125°C is chosen for the simulation.

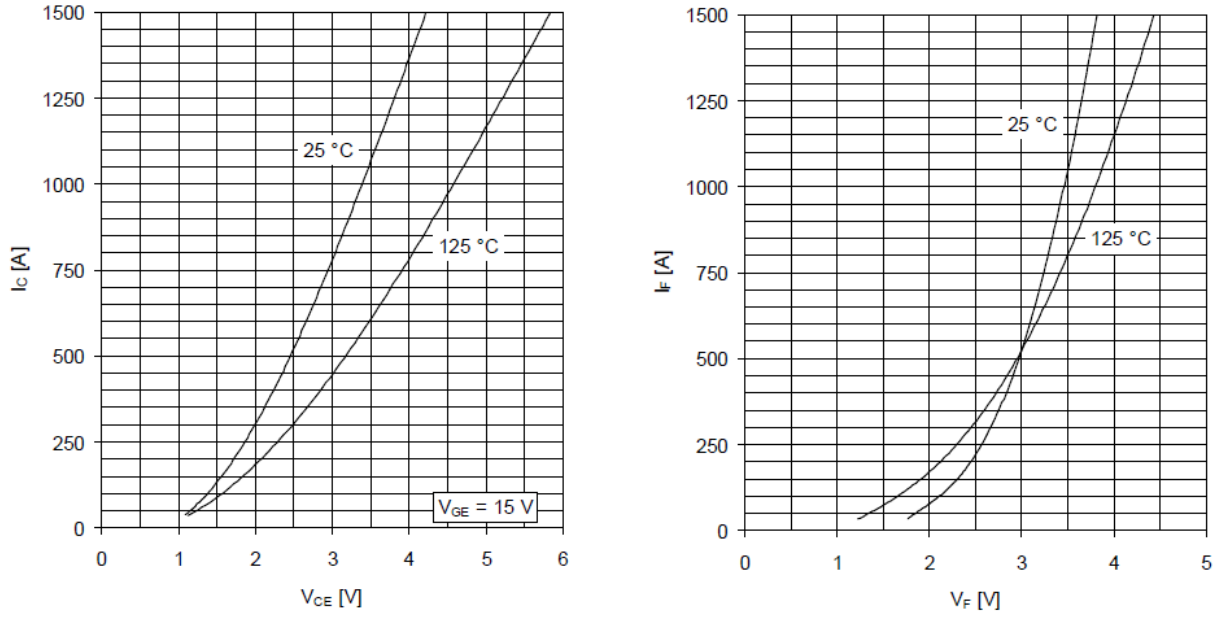

Figure 19 Transfer characteristics for IGBT (Vce Vs Ic) (Left) and Transfer characteristics for the Diode (Vf Vs If) (Right). (Source: ABB)

The total losses in the converter comprise mainly of switching losses and the conduction losses in the IGBT and diode. The diode turns on rapidly compared to the IGBT and hence the switching energy of the diode during turn-on can be neglected. But due to reverse recovery characteristics, the turn-off energy of the diode has to be considered.

In the two-level converter, the instantaneous current through the devices are calculated using the switching function concept [22]. Based on this procedure, losses are also modeled and calculated.

- Conduction losses

The on-state conduction loss for the IGBT is given as:

$$\mathrm{Pcond} = \frac{1}{\mathrm{T}}\int_{0}^{\mathrm{T}} \mathrm{V_f}\, \mathrm{i(t)dt} \tag{3}$$

$$\mathrm{V_f(t)} = \mathrm{V_{ce(0)}} + \mathrm{R_{on} i(t)} \tag{4}$$

where, $V_f(t)$ is the forward voltage drop of the IGBT

$V_{ce(0)}$ is the on-state voltage drop and R is the resistance. Similarly, the conduction losses of the diode can also be calculated by replacing (3) and (4) with the on-state resistance and voltage drop of the diode. The conduction losses for the IGBT/diode are calculated using PWM for m_f=25 and the results are presented in Table 1 and Figure 20.

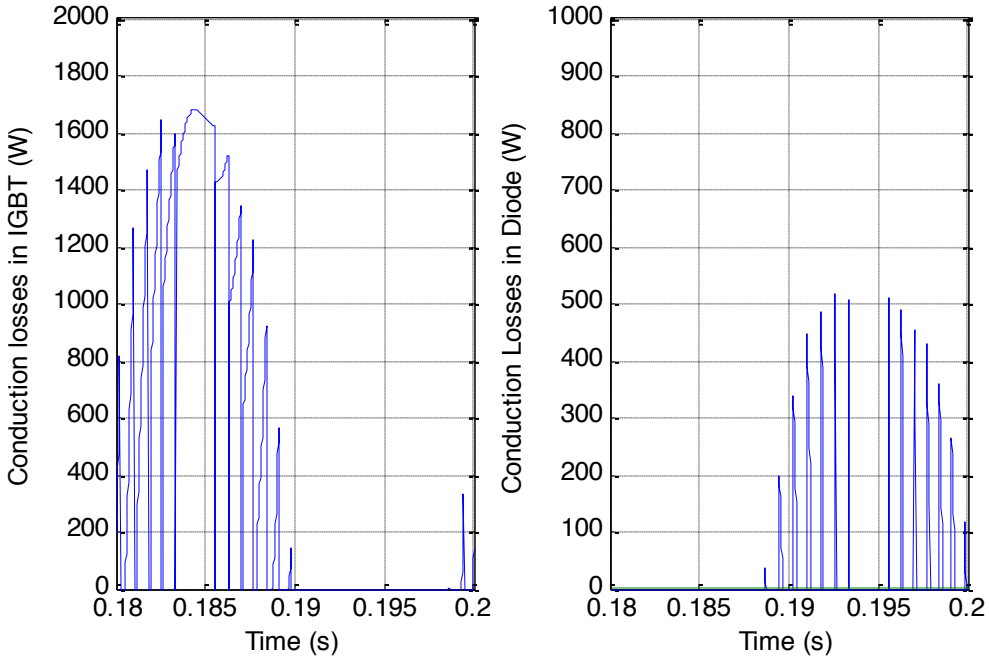

Figure 20. Conduction losses in the IGBT and the diode.

- Switching losses

With the use of PWM, the switching times of the IGBT's are determined and when they turn off the diodes take up the current. The increase in switching frequency causes the IGBT's to switch more often and resulting in losses during turn-on and turn-off. The switching loss of an IGBT is given by:

$$\mathrm{Pswitch} = (\mathrm{E_{on}} + \mathrm{E_{off}})\mathrm{f_{sw}} \tag{5}$$

Where, E_{on} is the energy during turn-on and E_{off} is the energy during turn-off and f_{sw} is the switching frequency.

Using the dependence of collector current on the switching energy as given in the datasheet, the value of the switching losses can be found. The switching energies with the current are depicted in Figure 21.

Figure 22 and Figure 23 show the switching losses in the IGBT and the diode respectively.

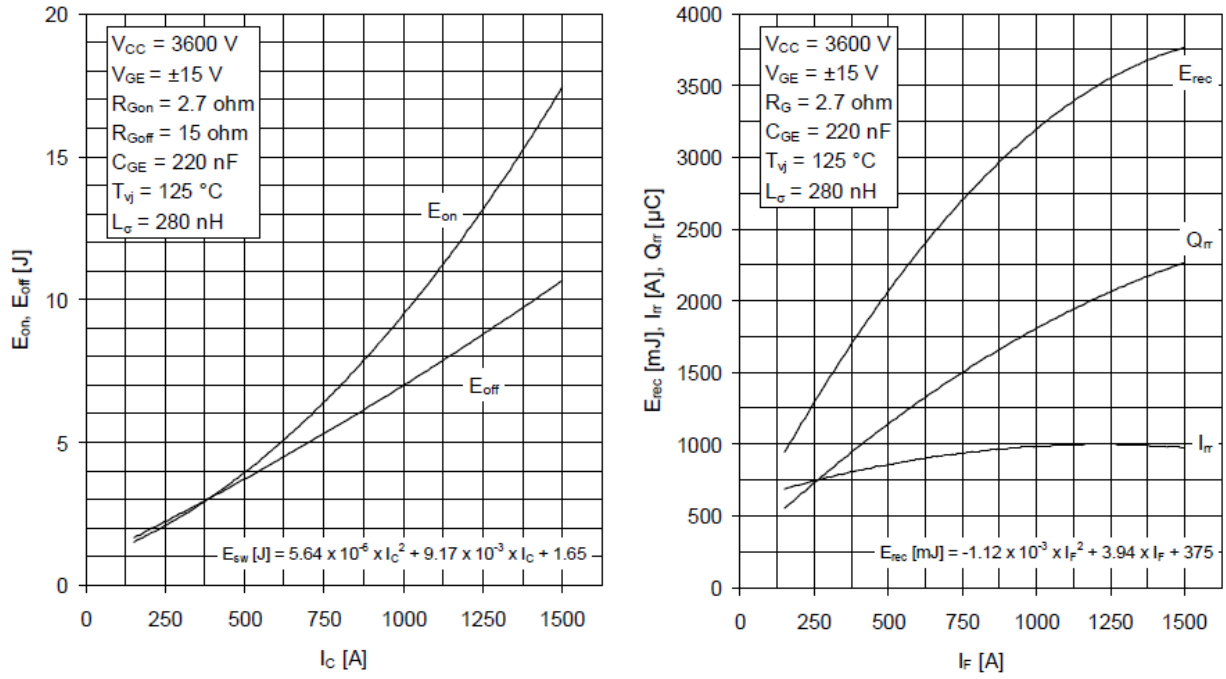

Figure 21. (a) Switching energy vs collector current and (b) Reverse recovery energy vs forward current in the diode. (Source: ABB)

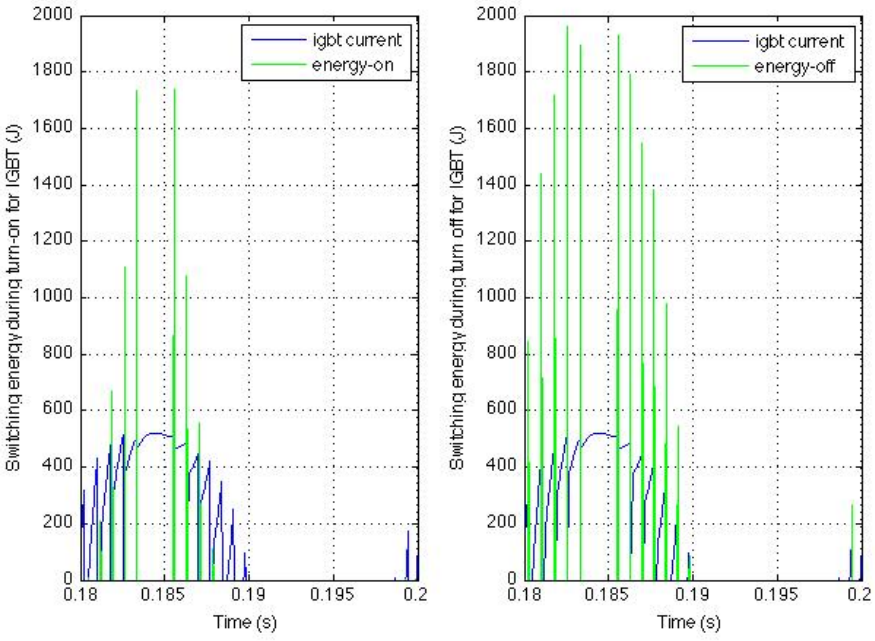

Figure 22. Switching energy during turn-on and turn off with the current through the IGBT

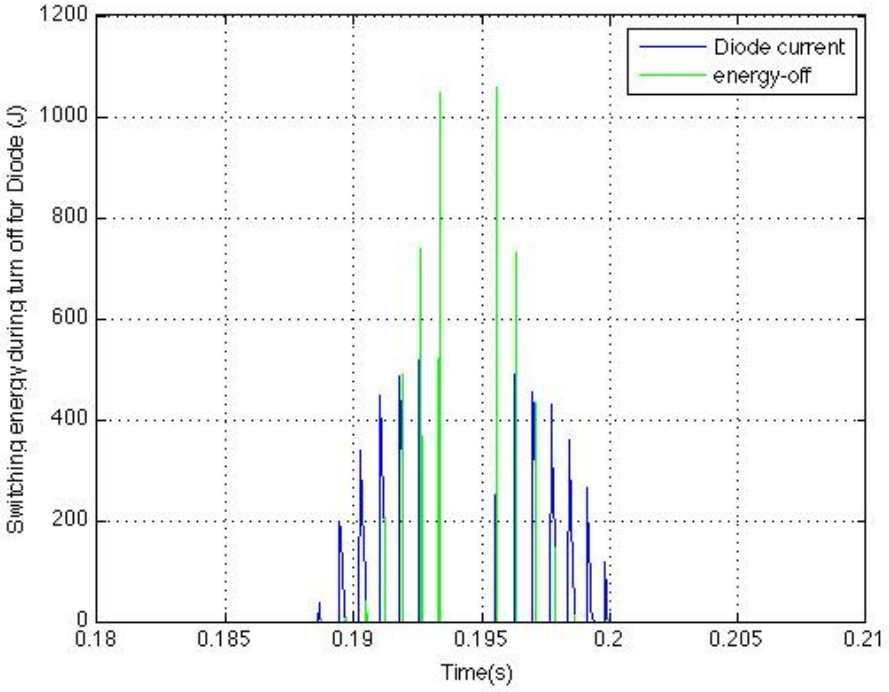

Figure 23. Losses during turn-off along with the diode current

- Number of components

In case of the two-level converter, each half leg experiences a DC voltage of 75kV and the current entering the phase leg is 2.828kA rms. According to the 6.5kV module datasheet, the SOA restricts the operation of the module at voltage levels higher than 4.4kV. Hence, for calculating the number of components required in series, an overvoltage factor of 55% is taken which gives an operating voltage of 3.6kV for the IGBT. Also, assuming sufficient voltage sharing capabilities the numbers of modules in series are calculated as

$$N_{Series} = \frac{U_{dc-link} * 1.55}{3.6kV} \approx 33 \tag{6}$$

For calculating the number of modules in parallel, a 50% overcurrent rating (I_{rms}=375A) for the 6.5kV module is assumed. The number of modules in parallel is calculated as

$$N_{parallel} = \frac{I_{rms-leg\ current}}{I_{rms\ rating\ of\ 6.5kV\ module}} \approx 8 \tag{7}$$

The total number of components in the two-level converter can now be calculated as

$$Total\ modules = 6\ N_{Series}\ N_{parallel} = 1584$$

The losses are calculated and tabulated as shown in Table 1.

Table 1: Losses in a Two level Converter

Power loss calculation using PWM for Two level Converter						
S.no.	Frequency Modulation Index (Mf)	Average Conduction Losses(KW)	Average Switching losses (KW)	Total Losses (MW)	% Loss	Total number of components
1.	27	499.2823	3.7789	6.7767	1.52%	1584
Power loss calculation using SHE for Two level Converter						
S.no.	Frequency Modulation Index (Mf)	Average Conduction Losses(KW)	Average Switching losses (KW)	Total Losses (MW)	% Loss	Total number of components
1.	27	421.0098	3.4559	6.1410	1.38%	1584

From the above results we can see that with the use of PWM the average switching losses are higher compared to using selective harmonic elimination for the same number of components and power rating. With the use of SHE, we can observe an increase in the conduction losses, as lesser switching events occur.

4.2 Three-level Converter

4.2.1 Modeling of the three level converter

The converter station is modeled using the three-level converter. Unlike the two-level case, a low-switching frequency modulation strategy is used. The model is simulated taking only into account the effect of the reactance only and without any filters.

In order to simulate the operation for multilevel converters, one topology should be chosen. In this thesis the simulations are carried out with the modular multilevel converter (M2C). A lot of inherent features of this topology make it suitable for HVDC [23]. Furthermore it can be operated at low switching frequencies, resulting in low losses and acceptable harmonic content.

Selective harmonic elimination allows us to eliminate specific harmonic components from the line voltage, and at the same time, control the fundamental component. The number of harmonics to be eliminated will depend directly on the number of times we chop the waveform. For every m chops in the voltage waveform we can eliminate m-1 harmonics and also control the fundamental. Higher number of pulses gives better harmonic performance, but also causes an increase in switching losses.

The number of delay angles (N) is defined for one quarter of the period. The whole period is built by reflecting this quarter wave and then duplicating it. This is done in order to get an odd-quarter-wave, which will simplify the Fourier analysis as shown below. Also, the number of delay angles (N) should be chosen such that the wave is at a positive voltage level at quarter time period of $\omega t = \frac{\Pi}{2}$ [24]-[25]. Hence, for all the simulations using SHE method the delay angle is chosen as an odd number. This will lead to a higher fundamental component for the line voltage and less harmonics.

4.2.2 Modulation: Selective Harmonic Elimination.

All periodical waveforms can be expressed as a Fourier series, which can be represented as the sum of sinusoidal functions with different frequencies.

$$f(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty}(a_n \cos(n\omega t) + b_n \sin(n\omega t)) \tag{8}$$

For odd quarter-waves a_n=0 for all n, so we do not have any cosine component; and b_n=0 for even n. From this, the created line voltage function will be simplified to:

$$u_{a0}(t) = \sum_{n=1}^{\infty}(b_n \sin(n\omega t)) = b_1 \sin(\omega t) + b_3 \sin(3\omega t) + b_5 \sin(5\omega t) + b_7 \sin(7\omega t) + \dots$$

$$b_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(t) \sin(n\omega t)\, d(\omega t)$$

As it is shown in the equation, b_n is the amplitude $\hat{U}_n$ of the harmonic n, and it is expressed for odd n. The expansion and calculation of the amplitude of the harmonics will depend on the number of firing angles (N). The analysis is presented for N=3. Three firing angles (α1, α2 and α3) will allow us to control three components; the fundamental component and the two lower order harmonics.

$$\hat{U}_n = \frac{4}{\pi}\left[\int_{\alpha_1}^{\alpha_2} \frac{U_{dc}}{2} \sin(n\omega t)\, d(\omega t) + \int_{\alpha_3}^{\frac{\pi}{2}} \frac{U_{dc}}{2} \sin(n\omega t)\, d(\omega t)\right]$$

$$\hat{U}_n = \frac{2U_{dc}}{n\pi}\left(-\cos n\alpha_2 + \cos n\alpha_1 - \cos n\frac{\pi}{2} + \cos n\alpha_3\right)$$

$$\cos n\alpha_1 - \cos n\alpha_2 + \cos n\alpha_3 = \hat{U}_n \frac{n\pi}{2U_{dc}} \tag{9}$$

The modulation index (M) for three-level converters is defined as the ratio between the amplitude of the fundamental and the half of the DC voltage. This will vary depending on the operation of the converter (desired output voltage).

From (9), the three unknown quantities, the three delay angles, create a system of three equations. Using the selective harmonic elimination (SHE) criteria, the fundamental is set to the desired modulation index, and the other two harmonics are eliminated (set to 0). In this case the third harmonic is not eliminated because we need the zero sequence to increase the available output voltage. Also, the third harmonic and its multiples will not circulate in the secondary side of the transformer, for instance, if a Dyn transformer is used. Hence, the fifth and seventh harmonics are eliminated using the equations below.

$$\cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) = \frac{4}{\pi}M \tag{10}$$

$$\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) = 0 \tag{11}$$

$$\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) = 0 \tag{12}$$

The system of equations presented in (10) to (12) can be solved for different values of modulation index. This equation system is non-linear, so numerical methods are required to find the angles. Algorithms and examples of numerical methods are shown in [26]. Figure 24 shows the firing angles for a range of desired values of modulation index (M). The model using three firing angles is explained as Case A.

A second case is also presented with an increase in the number of firing angles to five (α_1 to α_5). In this case (9) will be expanded to create a system of five equations, which will allow the elimination of four harmonics while simultaneously controlling the amplitude of the fundamental. The eleventh and thirteenth harmonic are also chosen to be eliminated in this case as the ninth harmonic is a multiple of three. This is presented as Case B. When the 5x5 equation system of Case B (not shown here, as it just requires the same procedure as Case B) is set and solved for different values of M, the firing angles are shown in Figure 25.

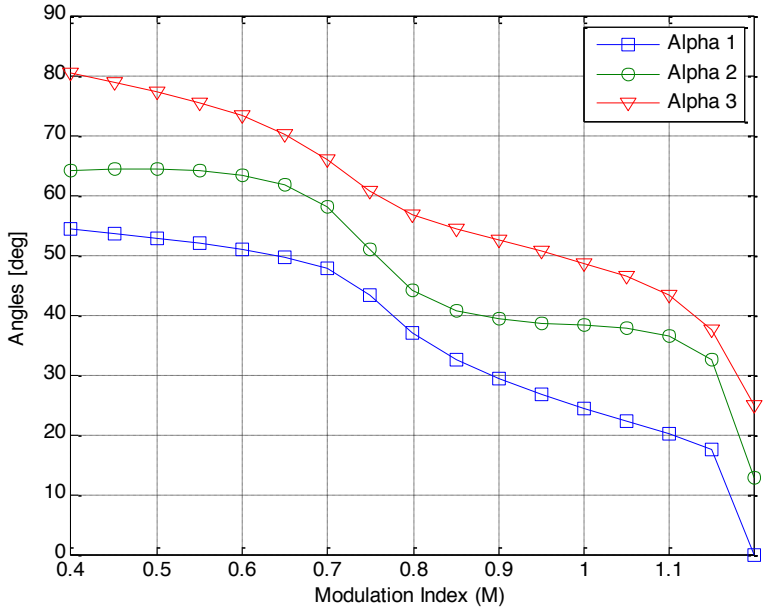

Figure 24. Case A: Three delay angles

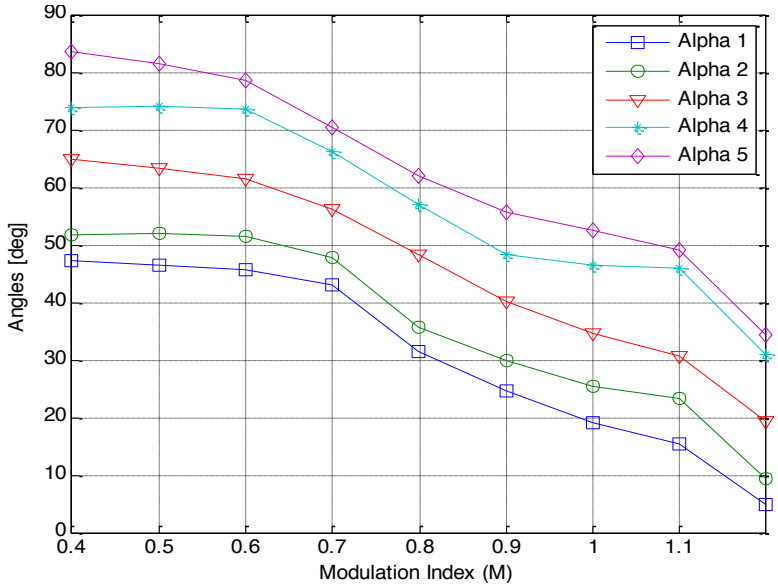

Figure 25. Case B: Five firing angles.

One important aspect to be noticed is the effect of elimination of the third harmonic. This harmonic component is carrying the zero-sequence component. When the third harmonic is chosen to be eliminated in the equation system, then any single solution is found for operation at values of M higher than 1.

4.2.3 Results

The output voltage of the converter for both Case A and Case B are shown in Figure 26 and Figure 27 respectively for M=1, which gives a fundamental voltage with an amplitude of 75kV, as we can also see in the plots.

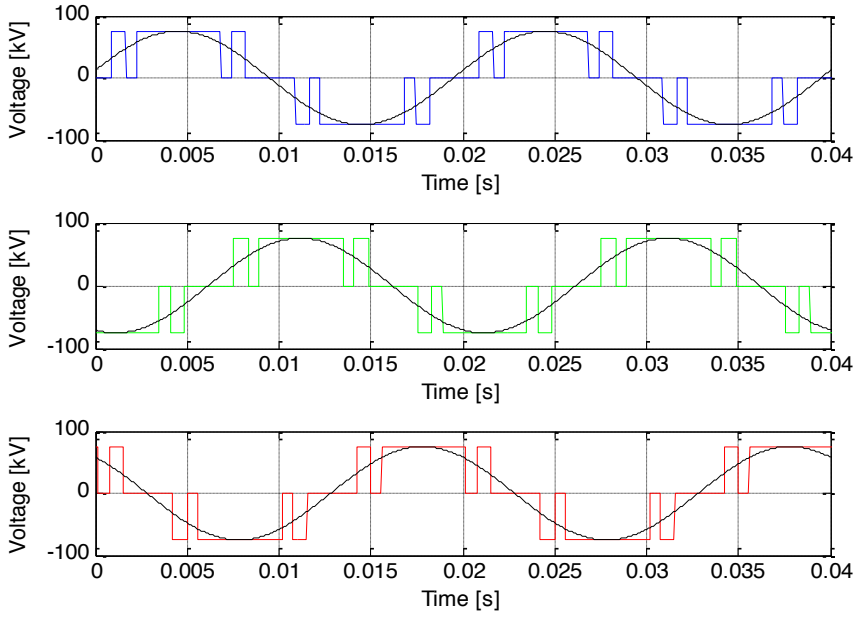

Figure 26. Three-phase voltages of three-level converter for case A.

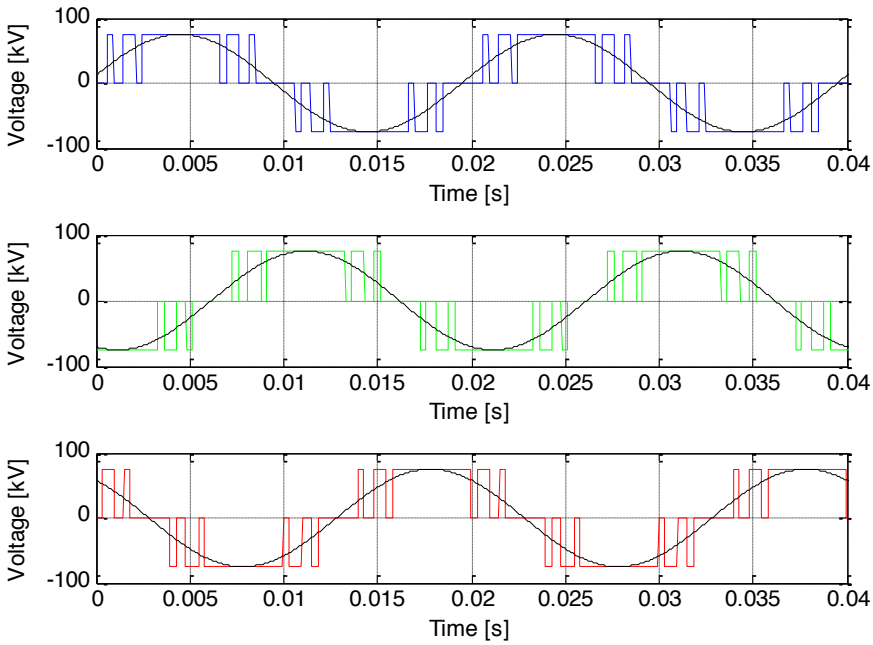

Figure 27. Three-phase voltages of three-level converter for case B.

Although the switching pattern is different, the fundamental voltage remains the same because it was set with the same value for both equation systems.

The active and reactive power control as well as the output voltage control of the converter is achieved by controlling the power angle (δ) and the modulation index respectively. In Figure 26 and Figure 27 the converter output voltage leads the grid voltage by 8.75° (which is the reference). This is chosen in order to deliver the nominal current, and hence operate at rated power.

Current waveforms in steady state operation assuming infinitely large capacitor, which depend on the transfer reactance (reactor-transformer), are presented in Figure 28 for the two different cases (A & B). As expected, lower ripple is achieved for higher number of switching events. Then we also anticipate less harmonic content for Case B.

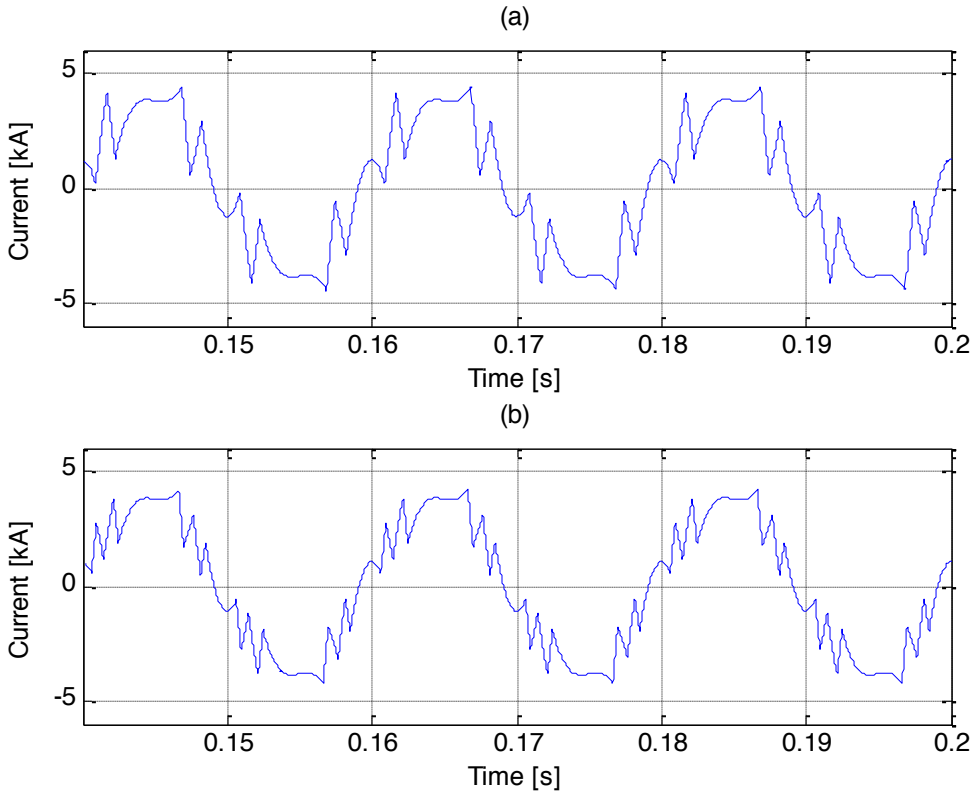

Figure 28. Line current in phase a for (a) Case A and (b) Case B.

Fourier analysis is performed to analyze the harmonic content of the voltage and the current injected to the grid. The results are shown in Figure 29 for Case A. The frequency spectrum demonstrates the accuracy of the SHE method, as fifth and seventh harmonic do not appear in the waves.

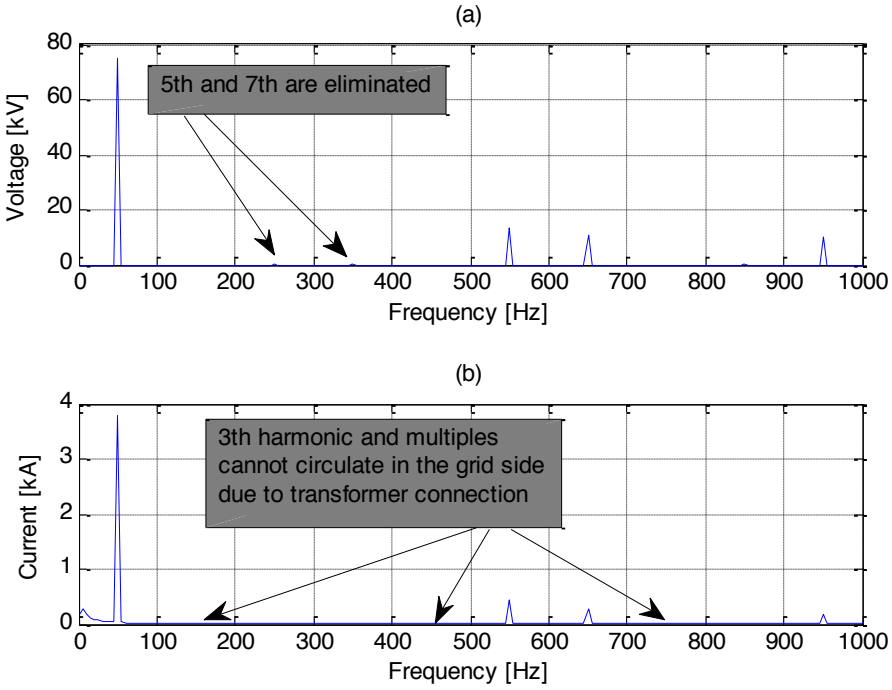

Figure 29. (a) Harmonic spectrum of the line voltage and (b) harmonic spectrum of the current for case A.

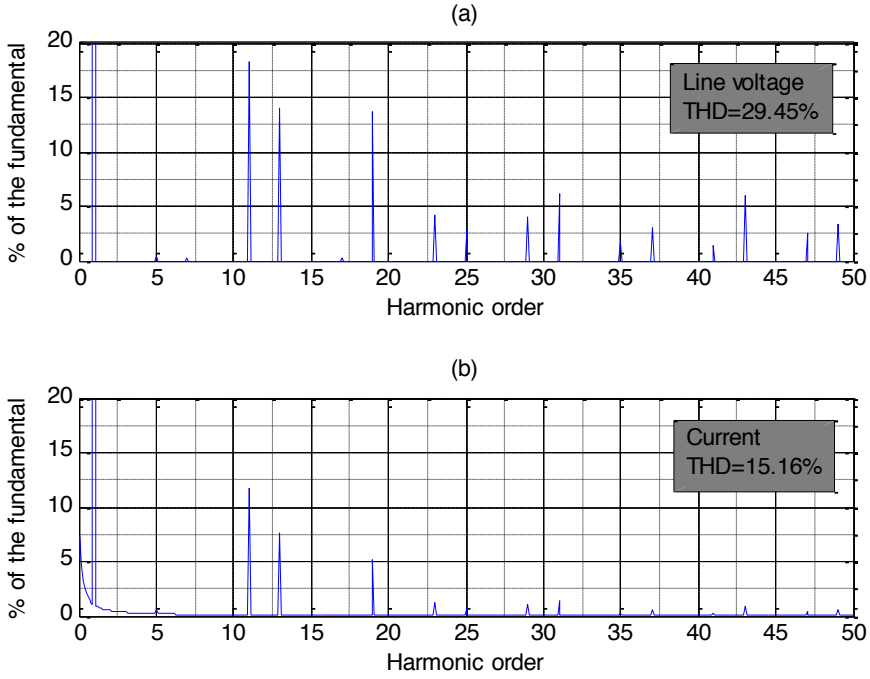

Figure 30. (a) Individual voltage harmonic distortion and (b) individual current harmonic distortion for case A.

For Case B we see in Figure 31 that the fifth, seventh, eleventh and thirteenth order harmonics are eliminated. However, the voltage THD does not seem to vary that much from the other case. THD for Case A is 29.45% and for Case B it is 30.78%. This is mainly because higher order harmonics have higher amplitudes when we increase the number of switching events.

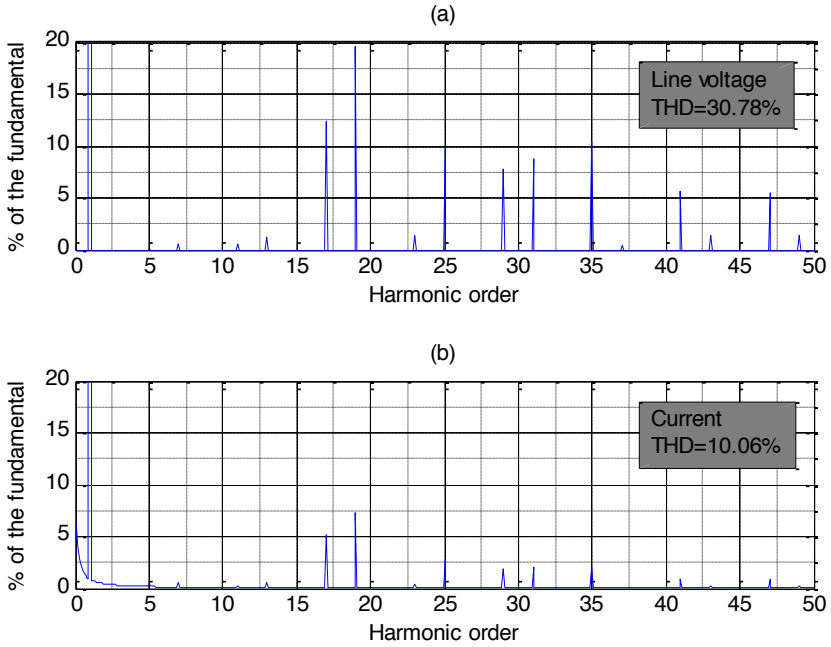

Figure 31. (a) Individual voltage and (b) current harmonic distortion for case B.

The effect of increasing the firing angles is just noticeable in the current, which reduces the THD to one third of its value in case B (from 15.16% to 10.16%), when we increase the switching events from three to five.

When the three-level converter is connected to the grid without any filtering device, it does not fulfill any harmonic requirement in any of the simulated cases (A and B). A lot of harmonics in the voltage present are in the range of 10% of the fundamental and the THD is very high, so tuned filters and high-pass filters are needed.

4.2.4 Capacitor balancing algorithm.

In the 3 level modular multilevel converter, as described in section 3.2.4, the upper and lower capacitors are charged and discharged continuously depending upon the direction of current when the output voltage is zero. The zero voltage output can be achieved by 4 switch states or switching sequences [27]. In the MATLAB simulation, initially the sequences are fixed for subsequent zero voltage periods and the switches are gated depending upon the direction of current. The instantaneous capacitor voltages (Vc1, Vc2, Vc3, and Vc4) are obtained using the SIMULINK model as shown in Figure 32 below. The value of each of the capacitors is chosen as 1mF and is rated for a voltage of 75kV (=Udc/2). The capacitor voltages, if not monitored, will continue to increase/decrease and cause an unbalance among the different sub-modules, leading to additional stresses on the switches and high circulating currents in the arms.

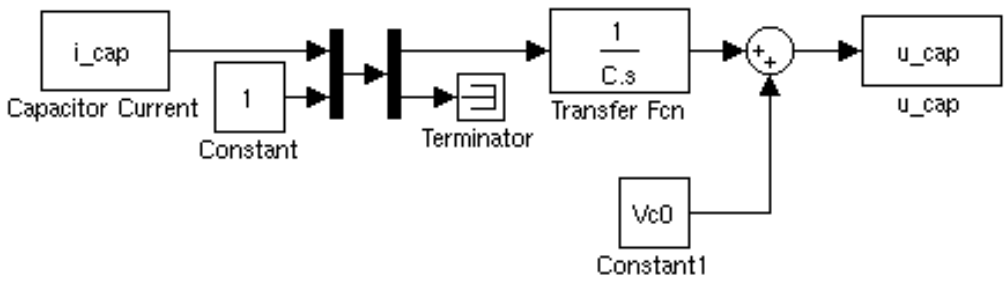

Figure 32. Instantaneous calculation of Capacitor Voltages

To balance the capacitor voltages a general capacitor-balancing algorithm used is presented below:

Capacitor balancing algorithm:

(i) The maximum and minimum values of the voltages of the upper capacitors and the lower capacitors are monitored.

(ii) Depending upon the magnitude of the capacitor voltages, during the positive half cycle the upper capacitor retaining the minimum voltage is charged and the lower capacitor with the maximum instantaneous voltage is simultaneously discharged.

(iii) Similarly, during the negative half cycle of the current the upper capacitor with the maximum instantaneous voltage is discharged and the lower capacitor with the minimum voltage is discharged.

Two cases (A & B) have been considered, taking into account the effect of the use of more notches in the voltage wave.

Case A: With 3 delay angles

In case A the simulation is carried out using 3 chops in the voltage wave providing an opportunity to control the fundamental component and eliminating two harmonics (5^{th} & 7^{th}). Applying the capacitor balancing algorithm to Case A the waveforms obtained are shown in Figure 33. From the figure we can see that the upper and lower capacitor voltages continue to oscillate around 75kV. It can also be observed that the waveforms for (Vc1, Vc3) and (Vc2, Vc4) are inverse of each other or in other words during the period of voltage zero these capacitor pairs alternately charge and discharge supplying power to the load. The maximum voltage increase that occurs on the upper capacitors Vc1 is around 1.1kV and for Vc2 it is 1.23kV. This increase in the voltage implies higher voltage stresses on the switches, which should be accounted for during the choice of rating for the devices.

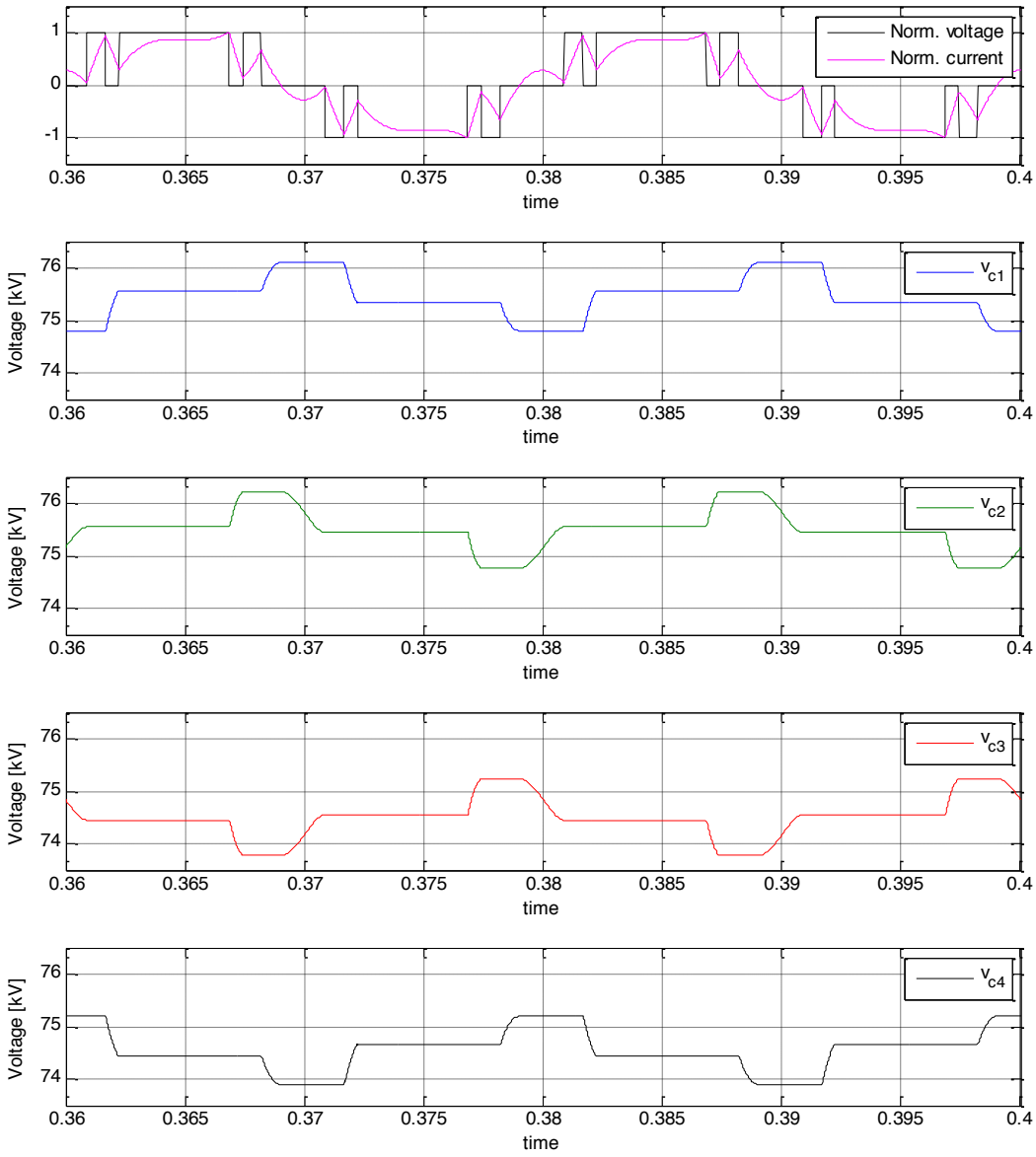

Figure 33. Results of Capacitor Balancing for Case A

Case B: With 5 delay angles

In case B the simulation is carried out using 5 chops in the voltage wave, which means that the fundamental component can be controlled along with the elimination of 4 other harmonics from the voltage wave. The waveforms for this case are shown in Figure 34.

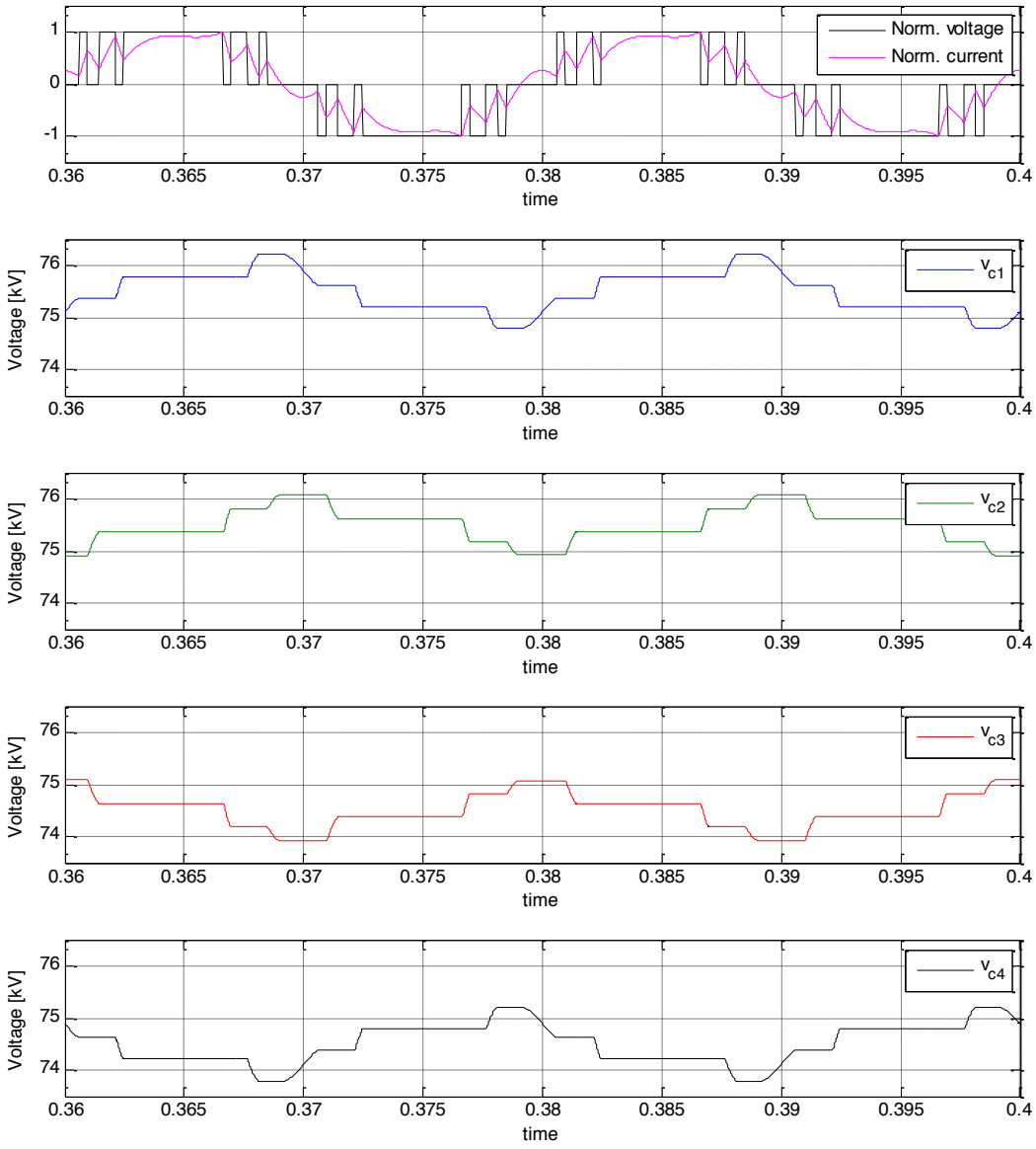

Figure 34. Showing the waveforms for the capacitor Voltages for Case B

Also, from Figure 34 we can see the effect of the capacitor balancing algorithm applied to the instantaneous values of the capacitor voltages. From case (a) & (b), initially the upper capacitor voltages show an increase and the lower capacitor voltages a decrease from the initial voltage level. As the capacitor balancing technique is applied we can see that the voltages on the capacitors vary instantly and continue to oscillate around the specified value.

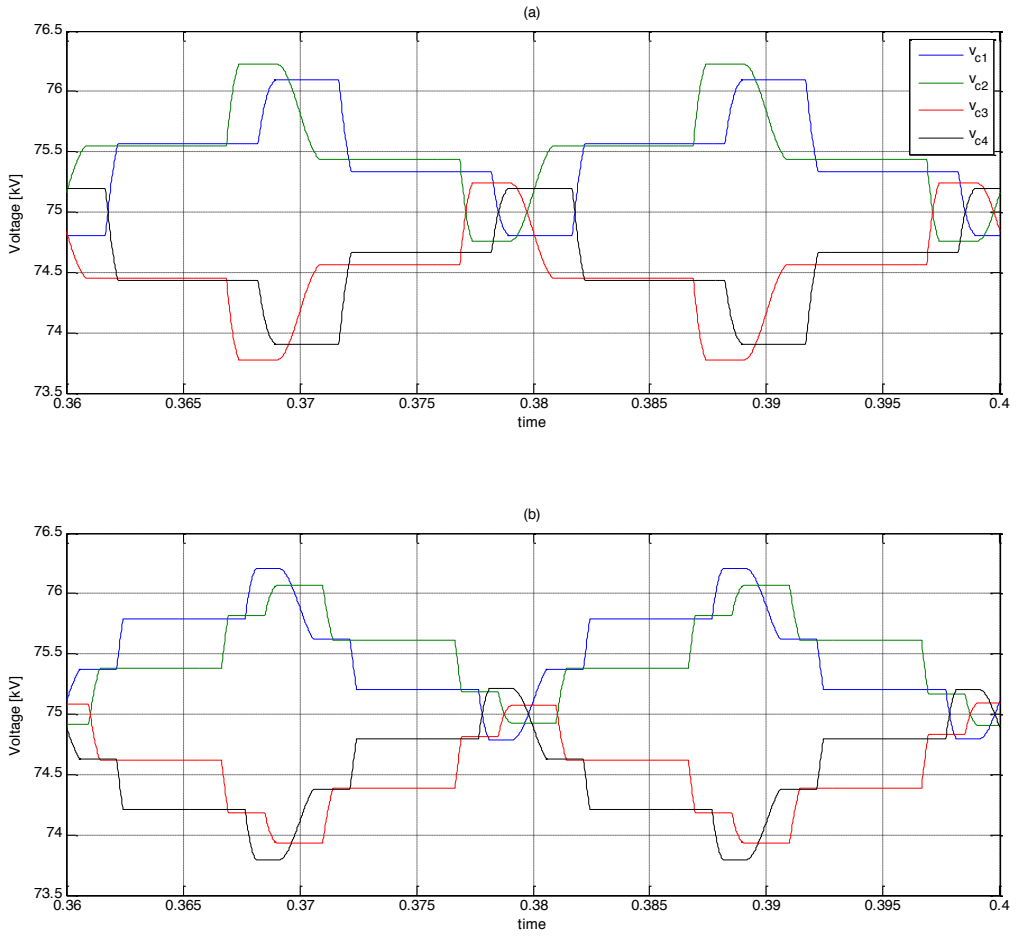

Figure 35. Showing the effect of introducing the balancing algorithm on (a) Case A (b) Case B.

4.2.5 Losses.

The losses for the three-level modular multilevel converter are calculated using the equations as in section 4.1.5. It is important to emphasize the effect of the capacitor-balancing algorithm in the calculation of the losses in the multilevel converters. The current through each sub-module (and hence through specific IGBTs and diodes) will depend on the switching pattern determined by the algorithm.

Once the currents through the devices are determined, the losses are computed for both Case A and Case B. In Figure 36 the losses for other cases are also presented, when the number of switching events is increased.

From Figure 36 we can see that as the number of firing angles is increased, and hence the switching frequency, the losses also increase. The figure only presents the losses when using the 6.5kV module. For other modules the calculated values for the losses are different, but the relation between losses and switching frequency remains unchanged.

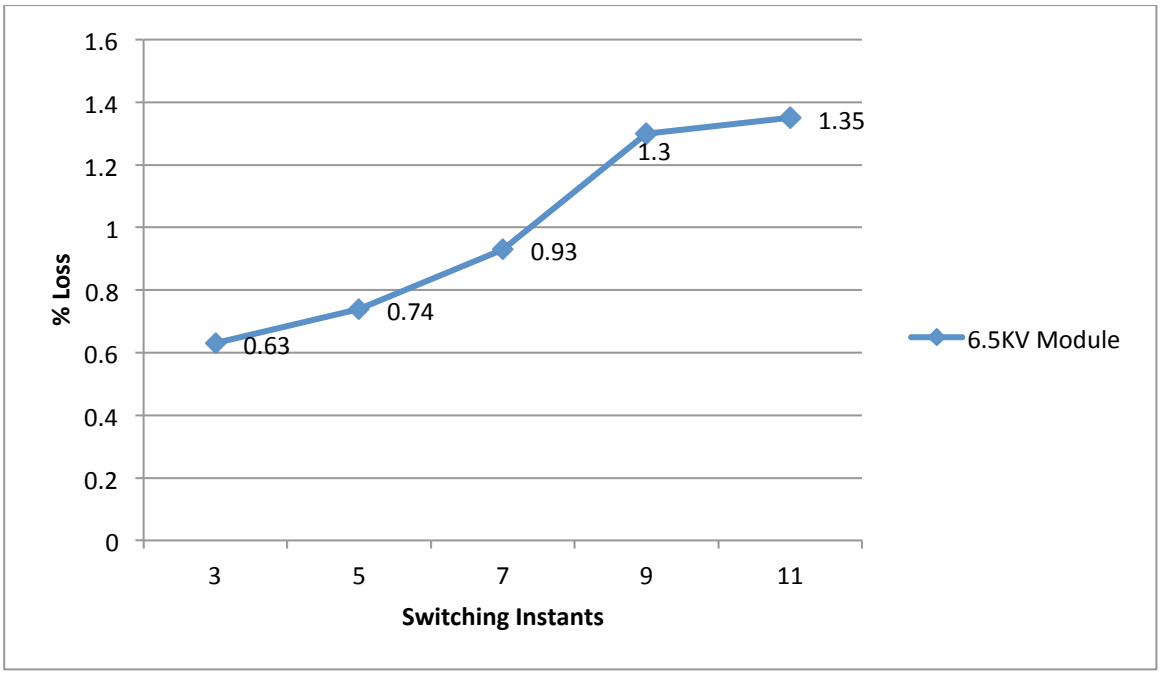

Figure 36. Variation of loss percentage with increase in delay angles for 6.5 kV module for three level converter.

Table 2 presents the values of the conduction and the switching losses for the increase in the number of delay angles when using

Table 2. Variation of conduction and switching losses with increase in delay angles

Delay Angles	**3**	**5**	**7**	**9**	**11**
Average conduction losses (KW)	159.3673	154.4959	154.2363	153.0304	154.59
Average switching losses (KW)	280.9880	366.5488	497.6316	757.8734	794.3495
Total converter losses (MW)	2.7901	3.3013	4.1302	5.7715	6.0125
%loss	0.63	0.74	0.93	1.3	1.35

From the above table we can see that the switching losses increase continuously with the increase in the delay angles and hence the losses also increase. The conduction losses however do not show much variation as it mainly depends on the on-state resistance of the module.

4.3 Five-level Converter

4.3.1 Modeling of the five level converter

The third kind of converter to be modeled for an HVDC substation is the five-level modular multilevel converter. The five-level comprises of eight sub-modules per phase leg, four in

each arm. The increase in sub-modules allows smaller voltage steps. Although the number of components is increased, each sub-module will be charged with a capacitor voltage of one quarter of the DC link, so the voltage they have to withstand will be less.

The expected harmonic performance is much better than in the three-level converter, because the smaller voltage steps will lead to less current ripple.

Like the three-level converter, the five-level converter is switched using selective harmonic elimination. In this case we will use fundamental frequency switching control, which makes the control even simpler. This means that for each quarter of the period, the voltage waveform will step twice (hence sub-modules will be switched only once per fundamental period). Due to this matter less switching losses are also expected.

When implementing the SHE algorithm for the five-level converter, just two firing angles must be calculated as there are only two switching events each quarter of the period. This gives a non-linear system with two equations and two unknown variables, hence two harmonics to be controlled [28]. In our simulation they are the fundamental (set according to the desired modulation index) and the fifth harmonic (set to zero) as it has higher amplitude after the fundamental.

After the fourier series calculation, the systems of equations are presented in (13) and (14).

$$\cos(\alpha_1) + \cos(\alpha_2) = \frac{\pi}{4}\left(\frac{\hat{U}_1}{U_{dc}/4}\right) = \frac{\pi}{4}M \tag{13}$$

$$\cos(5\alpha_1) + \cos(5\alpha_2) = 0 \tag{14}$$

In the five–level converter, the modulation index is the ratio between the amplitude of the fundamental and one quarter of the DC link voltage. When the system is solved for different values of M, the angles are computed and plotted as in Figure 37.

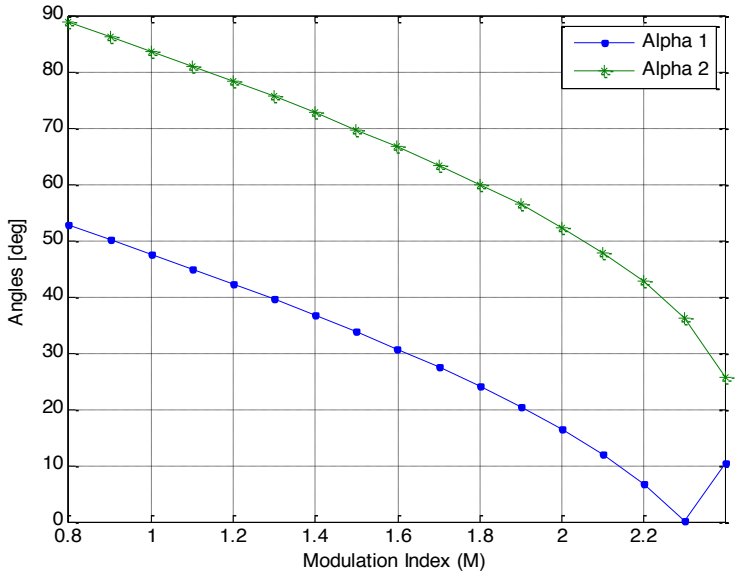

Figure 37. Delay angles for eliminating fifth harmonic and control of fundamental in five-level converter.

4.3.2 Results

In order to operate with a fundamental of 75kV peak voltage, we will choose the angles for a modulation index M=2. The line voltage waveforms are showed in Figure 38 for the three phases.

Due to the smaller voltage steps and the fundamental frequency switching control, the five-level converter waveforms have significant improvements when compared with three-level cases.

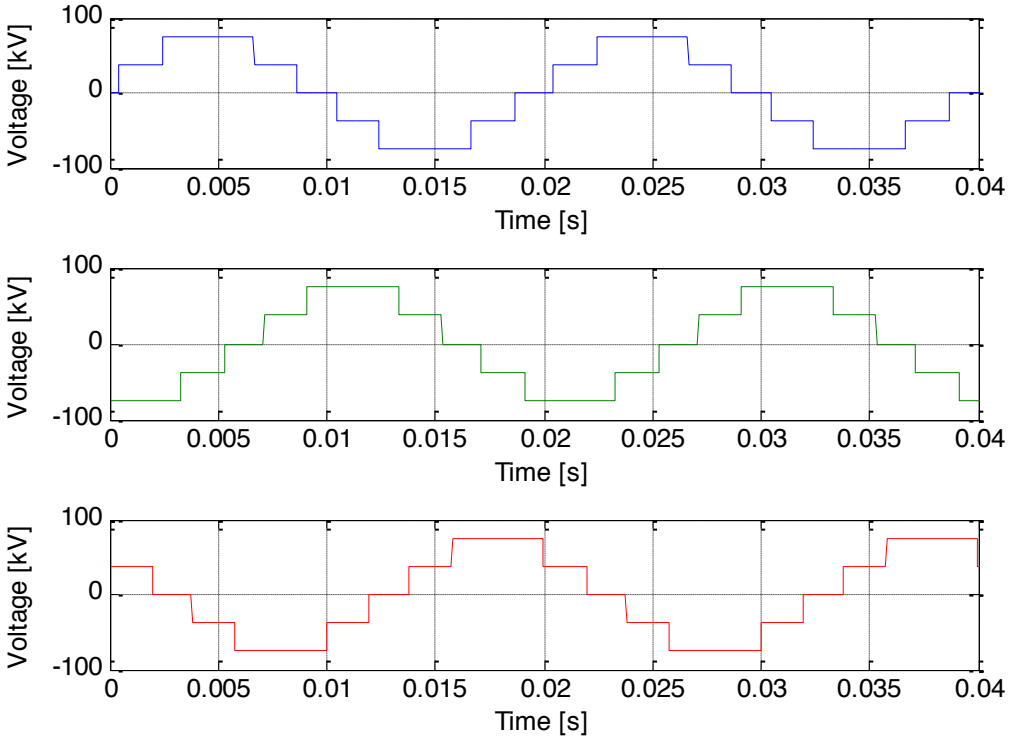

Figure 38. Three-phase voltages of five-level converter.

The current waveform in the five-level converter is much smoother than in three-level case for the same power operating point. This is shown in Figure 39. On analyzing the harmonic analysis results, we can observe in Figure 40, that a good performance of the converter is achieved in terms of distortion as seen from the grid side.

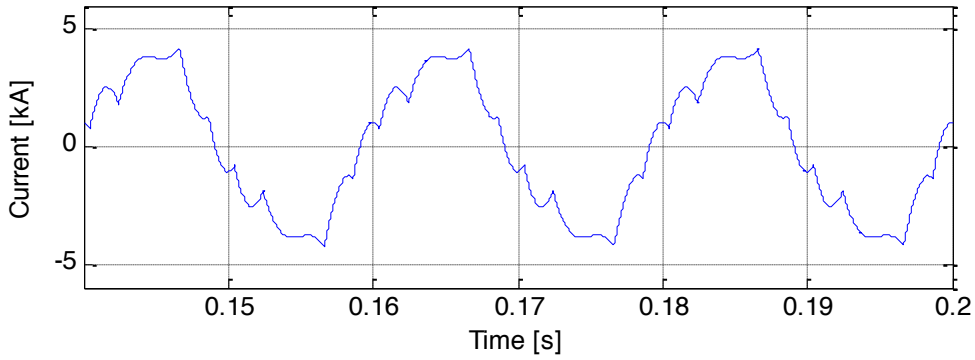

Figure 39. Line current in phase a in five-level converter.

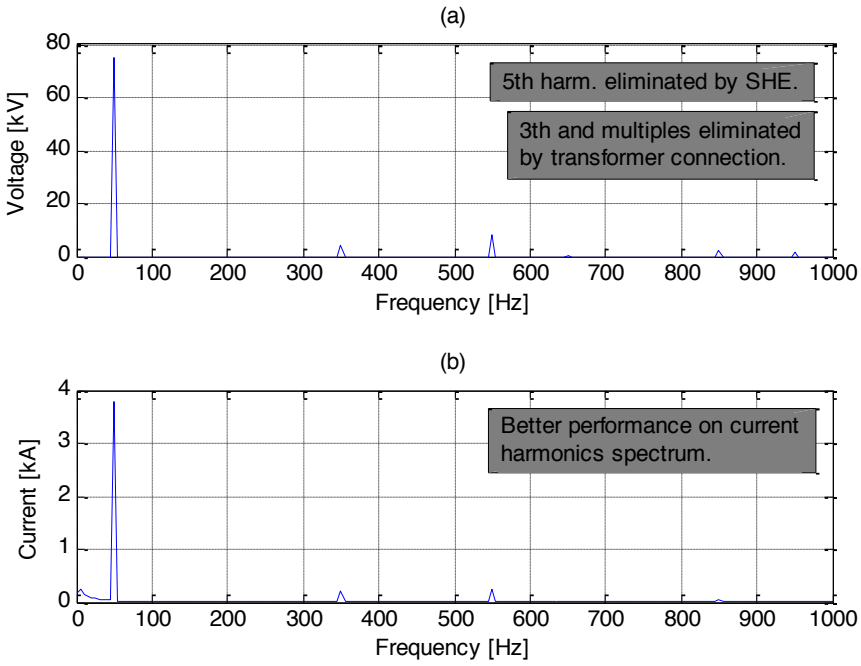

Figure 40. Fourier analysis for voltage and current at the grid side.

In terms of voltage harmonics, there is a remarkable improvement when using a five-level converter. The THD goes down to 13.72%, which is less than the half of the three-level converter case. The current harmonic distortion is also small, with a THD value of 8.92%. But again, for the five-level converter the voltage and current waveforms are not inside the distortion limits, and some filtering circuits will be required.

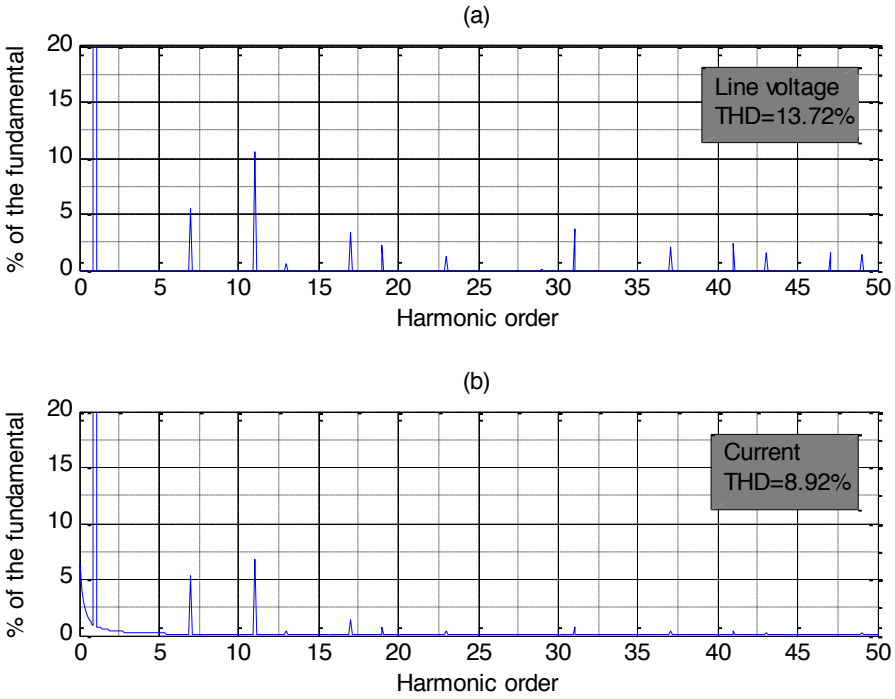

Figure 41. Individual voltage and current harmonic distortion in five-level converter.

5. Analysis and Performance Comparison of Two-level and Multilevel Converters.

5.1 Performance comparison of Two-level Converter using PWM and SHE.

With the number of components being the same in a two-level converter and using different modulation strategies along with different rating of modules, an interesting result can be observed. From Figure 42 we can see that with the use of PWM and for a range of ratings of modules, the number of components as well as the total loss varies. The use of higher number of components for a lower rating of module (2.5kV module) is justified, as the blocking voltage for each module is lower. The total loss, and hence the percentage losses, are also lower as the switching energies are lower compared to the other modules.

Another interesting result that can be observed is for the module rated 4.5kV. From Table 3 it can be seen that the number of components required are lesser for this module compared to the 6.5kV module. Also, according to the datasheet [17], the 4.5kV module has a higher current rating (1200A) compared to 6.5kV module (750A), which implies lesser number of components connected in parallel. From Figure 43, the difference in the average conduction and switching losses can also be observed. There exists a slight difference in the average losses for the two modules (4.5kV & 6.5kV), which is due to the switching energy specified in the datasheet. The difference in conduction losses can be attributed to the difference in the on-state resistance of the modules. Thus we can conclude that for the same power rating the choice of the rating of the module will depend on the criteria that is selected; either a compromise on the size of the converter or on the power losses.

Table 3: Total number of components in the converter for different module ratings

S.No	Rating of Modules (kV)	Current rating of Modules (A)	Total number of modules in converter
1	2.5	1200	2790
2	3.3	1200	1950
3	4.5	1200	1260
4	6.5	750	1584

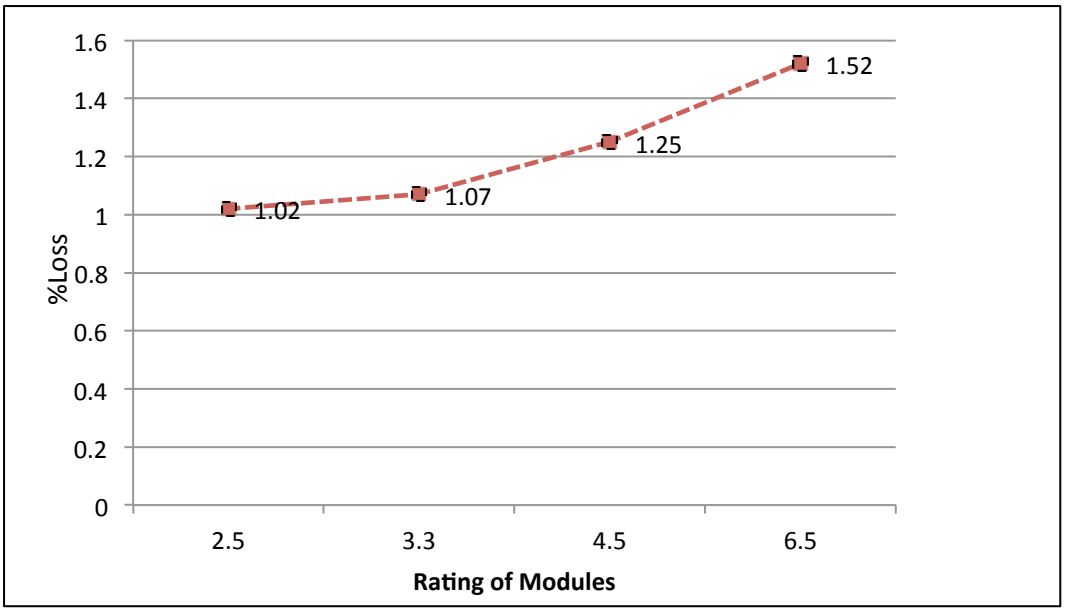

Figure 42. Variation of %loss for different module ratings: using PWM.

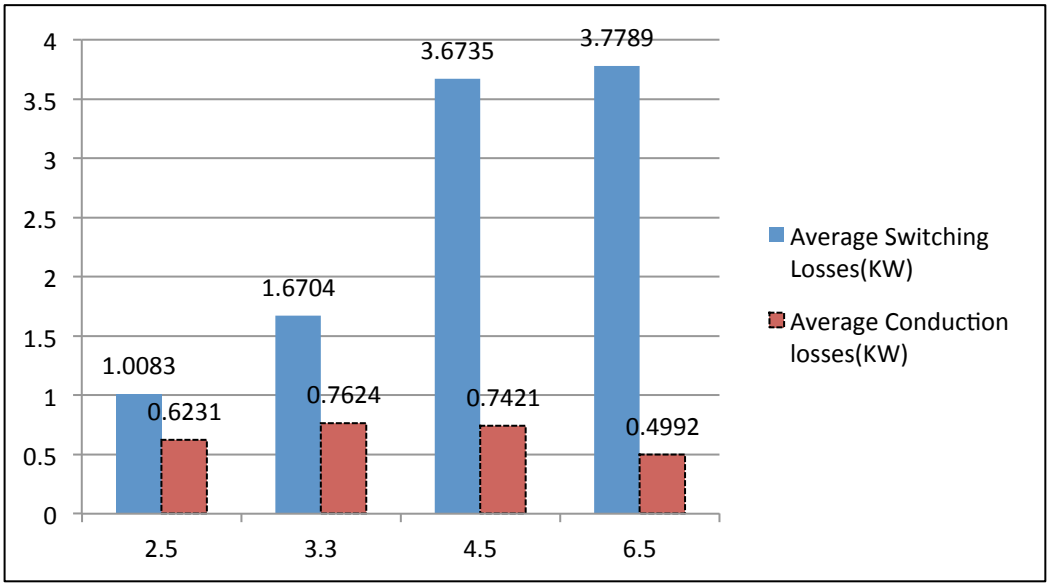

Figure 43. Variation of average switching losses and conduction losses for different module ratings: using PWM.

In case of using SHE for a two-level converter as shown in Figure 44 and Figure 45, we can observe that for the same number of components as the previous case for PWM, the losses are relatively lower which is mainly due to fewer switching.

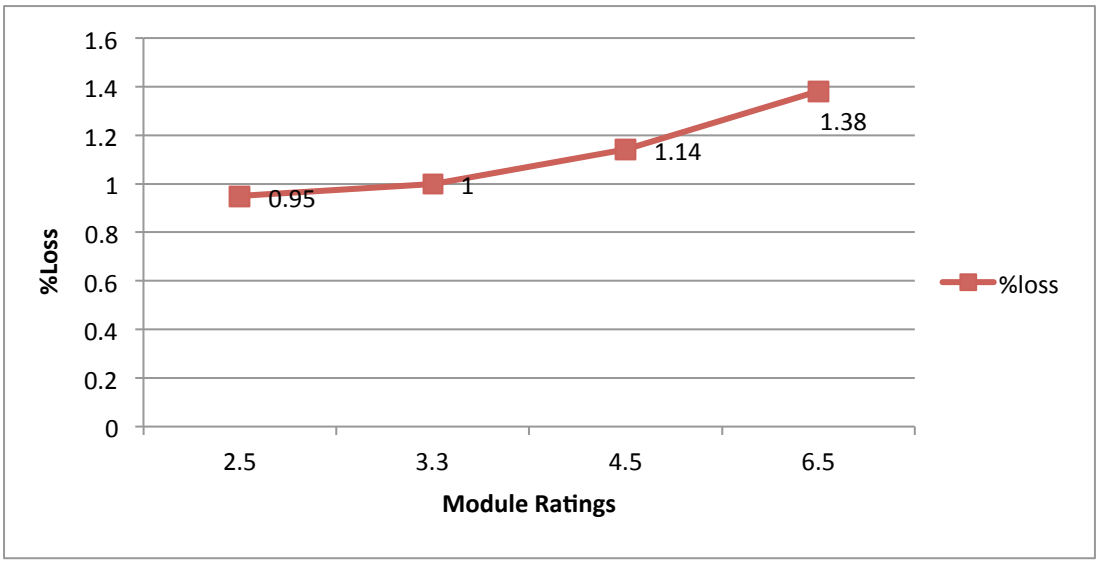

Figure 44. Variation of %loss for different module ratings: using SHE

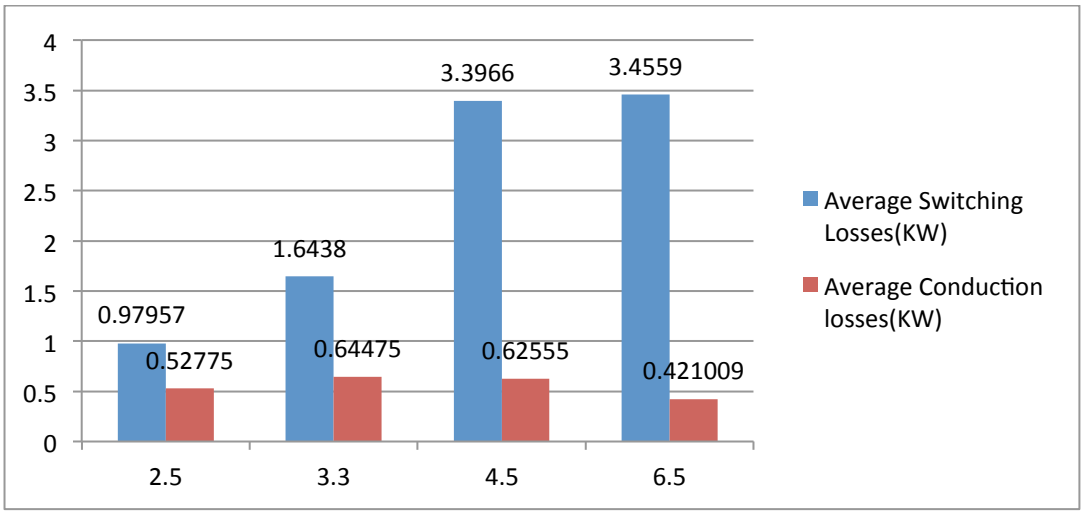

Figure 45. Variation of average switching losses and conduction losses for different module ratings: using SHE.

5.2 Performance comparison for the three-level Converter.

Figure 46 shows the variation of the losses in the converter with the increase in number of firing angles for a range of module ratings. As the number of delay angles increases, the components are switched more often leading to an increase in losses. In case of three-level converter, the losses for 6.5kV module are the highest compared to the 4.5kV module. This increase is mainly due to the higher number of components required in case of using a 6.5kV module, since it has a lower current rating compared to the 4.5kV module, as explained in the section 5.1 above. Also from the datasheet [18], we can see that the energy during turn-on and turn-off specified are higher for 6.5kV module compared to the 4.5kV module.

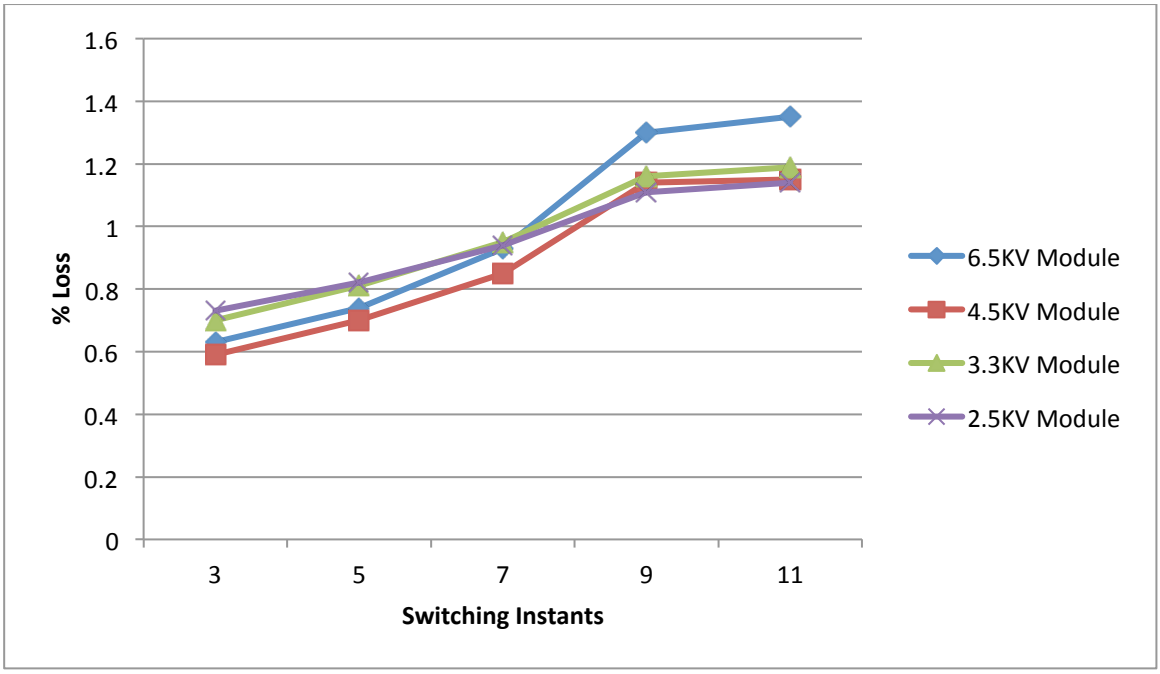

Figure 46. Variation of %loss with increase in delay angles for different module ratings.

In general, the use of 4.5kV is recommended instead of 6.5kV module because of the same reasons as explained in the previous section. But of course, when the size of the converter is an important matter, other important factors have to be taken into account.

The effect of the switching frequency in the three-level converter is summarized in the upper part of the Figure 47. Definitely, the increase in switching frequency is not an attractive solution anymore in order to fulfill the power quality requirements at PCC. This strategy will increase the losses in a drastic way. On the other hand, the increase in number of levels is expected to have a better effect as we will see in the next section.

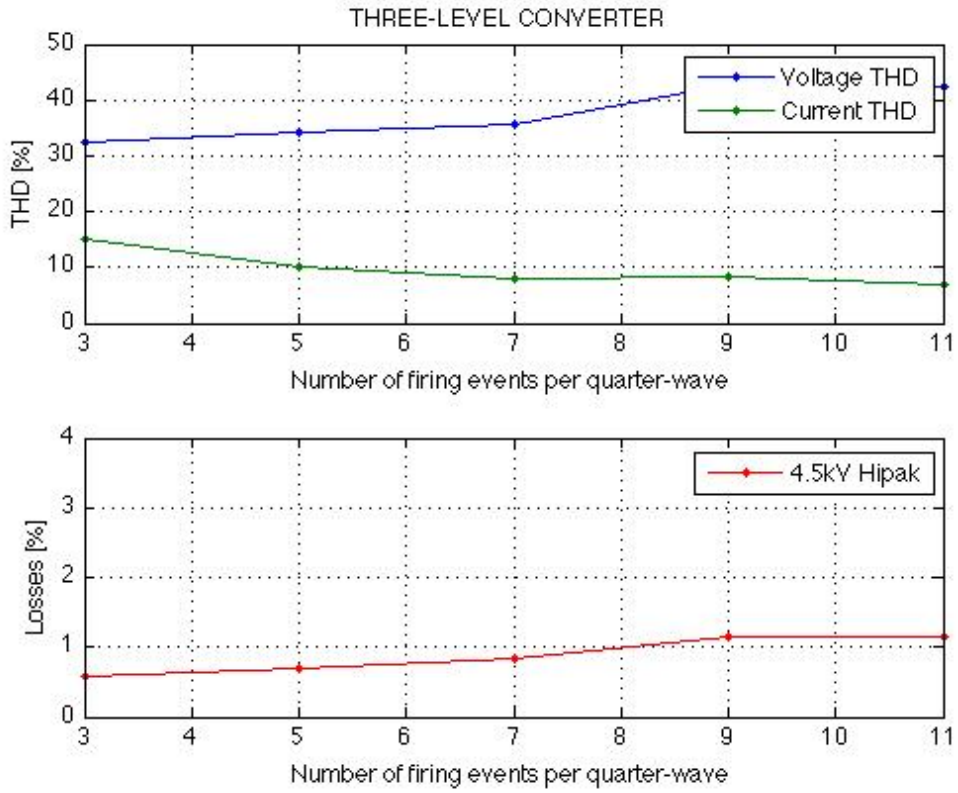

Figure 47. Characteristics of the three-level converter

5.3 Performance comparison for higher-level converters:

Finally, the simulations for higher level converters were carried out using SHE with fundamental frequency switching control. The simulation results from the seven-level converter to the twenty-three-level converter are presented in detail in the appendix. The obtained angles from the equation system are also presented.

The values of the voltage and current THD were plotted vs. the number of levels in Figure 48. Unlike the increase of the switching frequency, the increase of number of levels does represent a huge improvement in terms of distortion elimination.

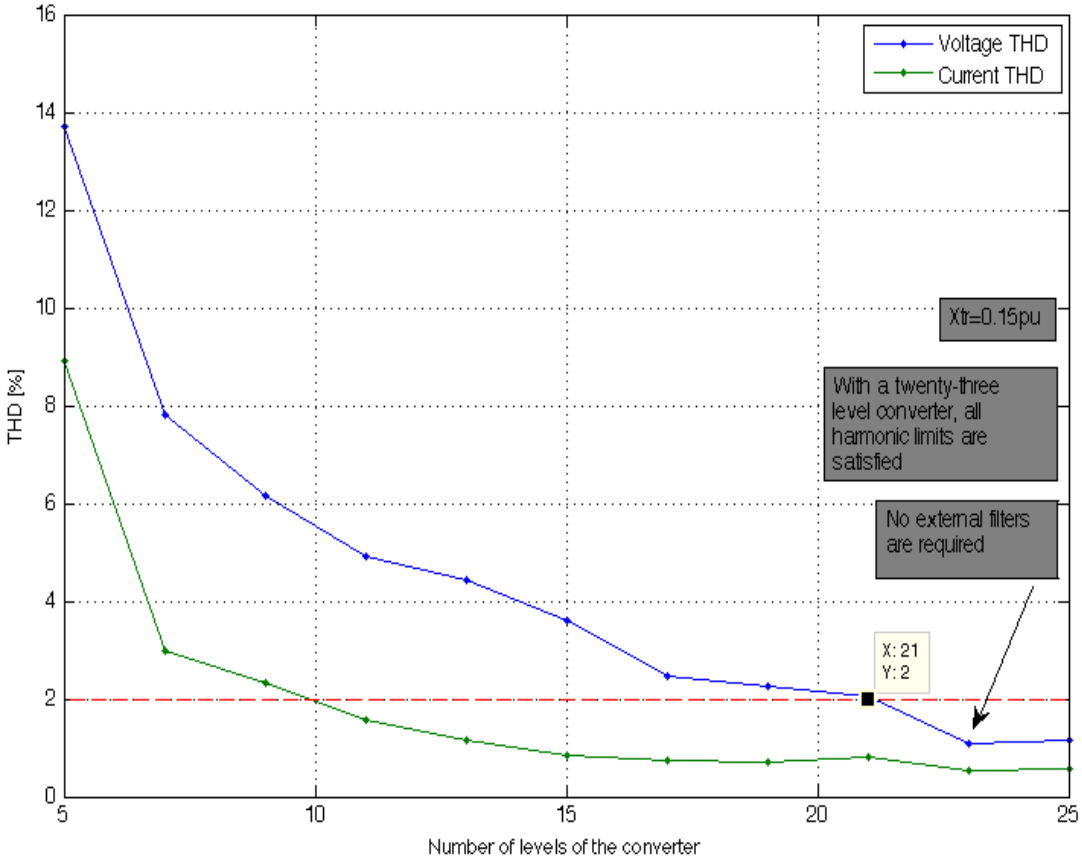

Figure 48. Voltage and current THD Vs the number of levels of the converter.

It is shown that with a converter with more than twenty-one voltage levels it is possible to connect the converter directly to the grid without the need of any external filter. The voltage THD with a twenty three-level converter is about 1.10%.

In terms of current THD, the situation is even better. For this simulation (with a total transfer reactance of 0.15pu of the transformer) the current quality requirements are already fulfilled for an eleven-level converter. It means that it is not necessary to have a big reactance. However, since the reactance has a filtering effect, a reduction in its value will cause an increase in the current ripple. Hence, for simulation purposes the value of the reactance is chosen as 0.15pu[29].

Another interesting aspect in the modeling of multilevel converters is the amount of energy stored in the converter. The energy stored is an indicative of the ride through capability [5] along with the size and cost of the capacitor. The equation for the energy stored in the capacitor is given as

$$E = \frac{1}{2} C U^2 n \tag{13}$$

where, E is the energy stored in the capacitor, C is the capacitance, U is the DC voltage and n is the number of capacitors in the converter topology. The value of energy has been calculated assuming a capacitance of 1mF and voltage rating of 75kV for all simulations of the two-level and multilevel converter.

The energy storage for the two, three and five level is shown in Table 4.

Table 4: Energy Stored in the Converter

S.No	Number of Converter levels	Number of Capacitors in the Converter(n)	Energy Storage (KJ)
1.	2	2	5.6
2.	3	12	33.75
3.	5	24	67.5

From the above results we can see that the energy stored in the converter mainly depends on the number of capacitors as all the modules in the case of the modular topology (three and five-level) are rated for 75kV. The five-level modular converter has higher number of capacitors and hence higher value of energy stored in the converter. The energy stored in the two-level is the least, as a half –bridge topology has been considered and the simulations have been carried out assuming two lumped capacitances with a voltage rating of 75kV. Higher energy storage leads to better ride-through capabilities but with a compromise on the large size of the capacitor and the associated cost for the same voltage and power rating. If cost is the main aspect, then the capacitor voltage rating can be reduced but will lead to an increase in the number of components and lower energy storage in the converter. Therefore, depending on the criteria of either cost, size or energy storage, the choice of topology will also vary.

6. Conclusions and Future Work

6.1 Conclusions

In this thesis, different topologies and modulation strategies were analyzed for the same voltage and power level.

For the same module rating of 6.5kV(750A), first the results for the two-level converter using PWM and SHE modulation strategies were analyzed. It was found that, using PWM strategy the total losses in the two-level converter are higher (1.52%) compared to SHE (1.38%). The decrease in losses in SHE was due to the lesser switching events. In terms of power quality, both the modulation techniques did not fulfill the requirements at the PCC, necessitating the use of either more filter requirements or the use of higher switching frequencies that imply higher losses. It was also observed that, the values for current THD, in the case of the two-level converter using PWM, are comparable to SHE for values of frequency modulation index as an odd multiple of three. Using higher switching frequency PWM did not have a profound effect on the voltage harmonics of the two-level converter, as the harmonics were just shifted further in the frequency spectrum, but it lead to an increase in the power losses. It was also realized that the choice of module rating affected the performance of the two-level converter. The use of SHE modulation strategy resulted in lower values of total losses, for the range of module ratings, compared to the PWM strategy. Amongst the different ratings of the modules, the use of 2.5kV module gave the lowest losses for both modulation techniques, but it also highlighted the aspect of size of the converter. The 6.5kV module gave lesser components compared to 2.5kV (1584 versus 2790) but then caused an increase in the total losses. Taking into account all the above factors, it can be concluded that although two-level converter offers simplicity in design it does not offer an acceptable output in terms of THD. If power quality is the main criteria, then going further in levels can lead to a better performance.

The three-level converter using the modular topology was simulated for the same voltage and power rating as the two-level converter. With higher levels, the use of PWM does not offer significant benefit as we have increased losses hence, SHE modulation strategy was utilized and the results were compared for increasing delay angles. It was found that, with the use of five delay angles, the current THD reduced to 10.16% compared to 15.16% for three delay angles in the voltage wave. In addition to the better result in terms of current THD, more harmonics were also eliminated with increase in delay angles. The voltage THD, in turn, did not show much improvement as the harmonics were shifted to higher frequencies. Further, different ratings of modules were compared and 4.5kV(1200A) module was chosen over 6.5kV(750A) as it yielded better results in terms of number of components, total power losses and overall size of the converter. The 4.5kV module gave lower losses of 0.59% for three delay angles compared to five delay angles, which had a loss percentage of 0.70%. It can be concluded that the use of higher delay angles although leads to a better harmonic performance but the increase in total losses also needs to be considered as the number of switching events increase in the three-level converter. Further, although the three-level converter presents improved results compared to the two-level converter in terms of power

quality and power losses, it still does not fulfill the requirements at the PCC. In order to achieve power quality standards, an alternative to increasing the number of delay angles in the three level converter is to increase the number of levels, which would lead to lesser switching of components per fundamental period and also provide opportunity to cancel out more harmonics with the use of SHE.

The five-level modular converter was simulated and it was found that, the voltage THD is reduced to 13.72% compared to 30.78% in the case of three-level converter with five delay angles. The current THD is also reduced to 8.92% compared to 10.16% of the three-level converter. It can be concluded that by increasing the number of levels to five, offers significant advantage in terms of power quality, compared to increase in the number of delay angles in the three-level converter which leads to increase in switching events.

For the same power and voltage rating, higher levels of the modular topology, were also simulated. Higher levels, implies the use of more number of submodules to generate intermediate steps in the instantaneous voltage wave to make it more sinusoidal. It was found that, with a twenty-three level converter the voltage THD reaches a value of 1.10% and satisfies the power quality standards (IEEE Standard 519). In addition to lower values of the THD, the twenty-three level converter does not require the use of external filters and can be connected directly to the grid.

The choice of topology for a particular voltage and power rating depends on a lot of factors. Depending on the criteria chosen, either power quality or reduced costs, different results can be obtained. With power quality as the main criteria, it was realized that with the use of higher number of levels, such as a twenty-three level converter, a good harmonic performance is achieved with no requirement of filters. Also, lesser switching per component leads to lower losses and energy storage for ride through capabilities is available. If however, the size and associated costs are considered, then using lesser voltage steps for the converter along with filters may be justified. In addition to power quality issues and cost, another factor that needs to be considered is the complexity of control. The use of higher levels although gives improved performance in terms of power quality and saving in cost of filters, but the complexity of the control in switching components simultaneously and the voltage imbalance of the capacitors, which overstresses the switches, also needs to be taken into account.

6.2 Future Work

The next step of this study should be the expansion of the model. It would be interesting to model a more realistic HVDC substation and analyze the combined effect of converter technology, modulation and filter design.

The impact of the capacitor size on the performance of the converter should be studied, as well as the impact of the inductor size on the current THD. The algorithm and control system of the capacitor balancing in a modular converter can also be studied for higher levels.

In the thesis all the simulations were done for rated power and rated voltage of the converter, but the operation at different voltage and power levels have to be investigated due to its effect on the efficiency of the converter.

In general, the cost in terms of investment and operation is an interesting factor to be studied, and it is the most important from the companies' point of view.

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Appendix

Simulation results for higher-level converters.

SEVEN-LEVEL CONVERTER

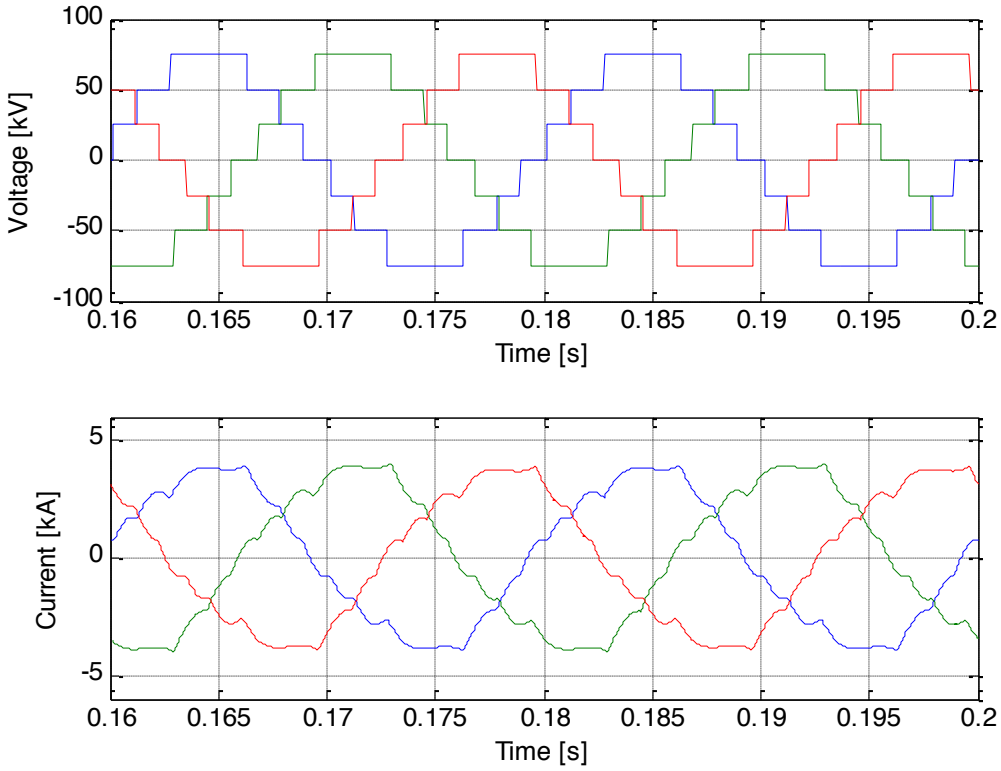

Figure A 1. Voltage and current waveforms in a seven-level converter.

Table A 1

THD Voltage	THD Current	Firing angles (deg)
0.0780	0.0299	11.6826 31.1804 58.5792

NINE-LEVEL CONVERTER

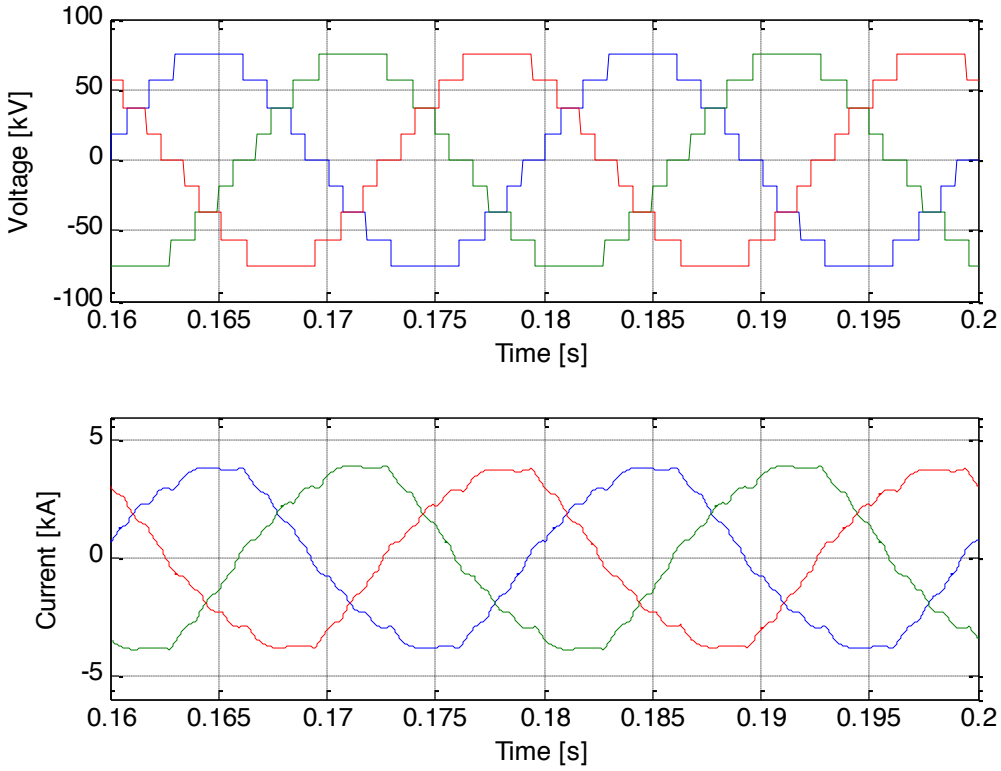

Figure A 2 Voltage and current waveforms in a nine-level converter.

Table A 2

THD Voltage	THD Current	Firing angles (deg)
0.0617	0.0234	10.0153 22.1448 40.7545 61.7706

ELEVEN-LEVEL CONVERTER

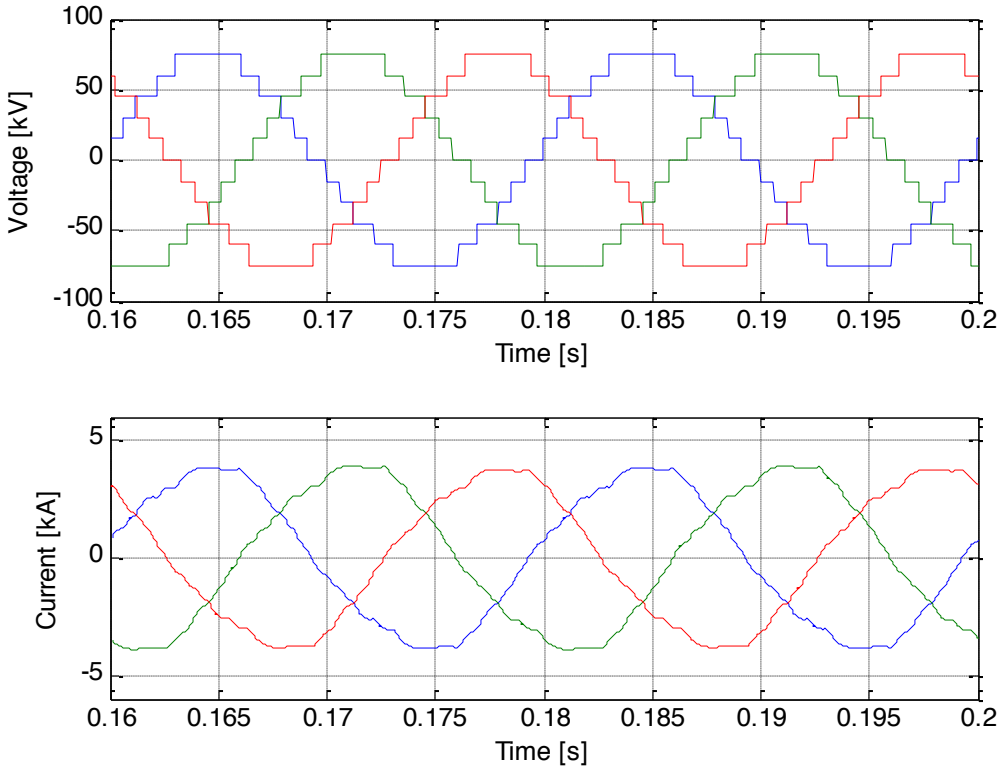

Figure A 3 Voltage and current waveforms in an eleven-level converter.

Table A 3

THD Voltage	THD Current	Firing angles (deg)
0.0492	0.0157	7.8610 19.3717 29.6506 47.6815 63.2144

THIRTEEN-LEVEL CONVERTER

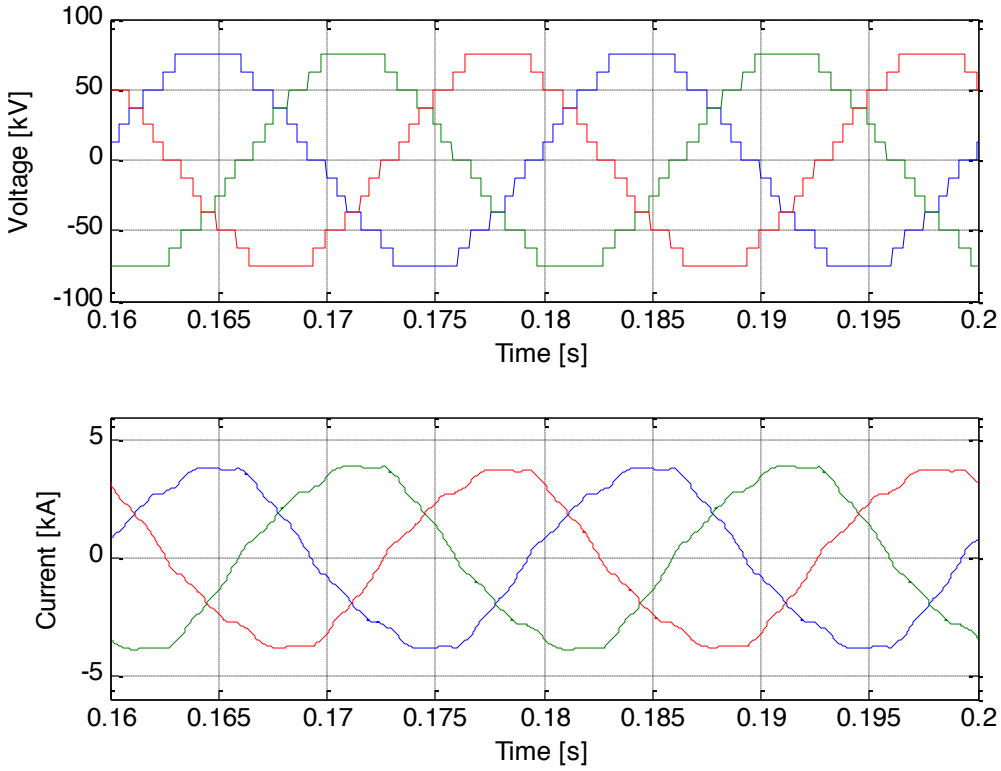

Figure A 4 Voltage and current waveforms in a thirteen-level converter.

Table A 4

THD Voltage	THD Current	Firing angles (deg)
0.0442	0.0114	7.7750 16.7590 24.4481 36.5604 53.1361 63.2202

FIFTEEN-LEVEL CONVERTER

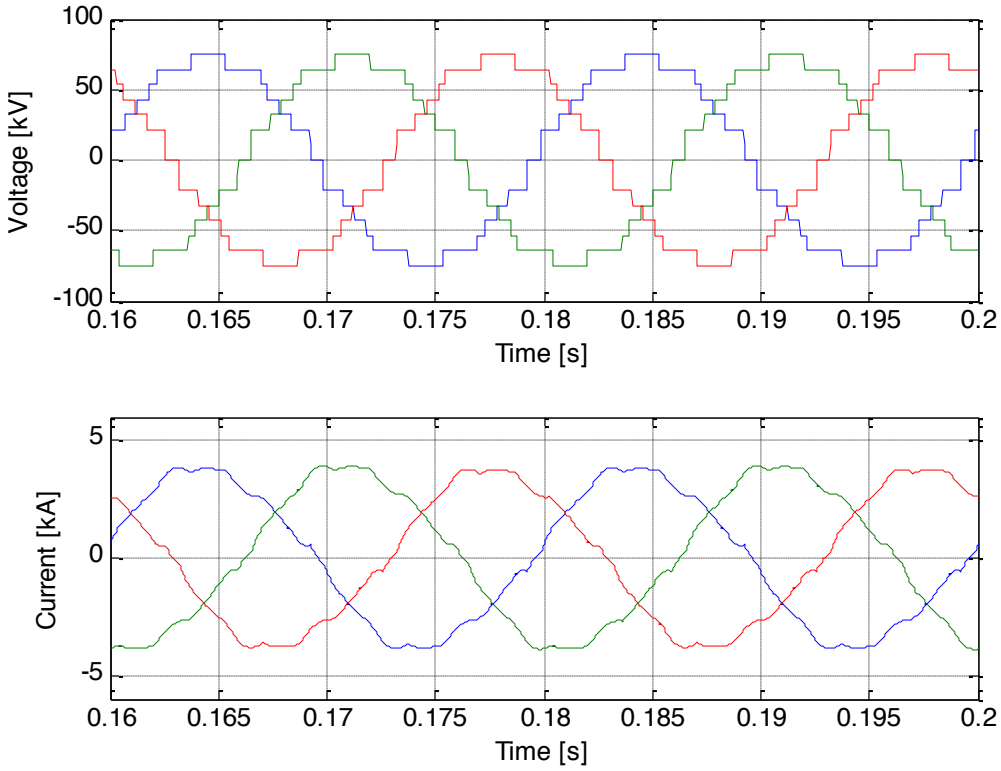

Figure A 5 Voltage and current waveforms in a fifteen-level converter.

Table A 5

THD Voltage	THD Current	Firing angles (deg)
0.0359	0.0083	5.6093 5.8384 21.3942 31.0429 40.7373 46.8966 75.8252

SEVENTEEN-LEVEL CONVERTER

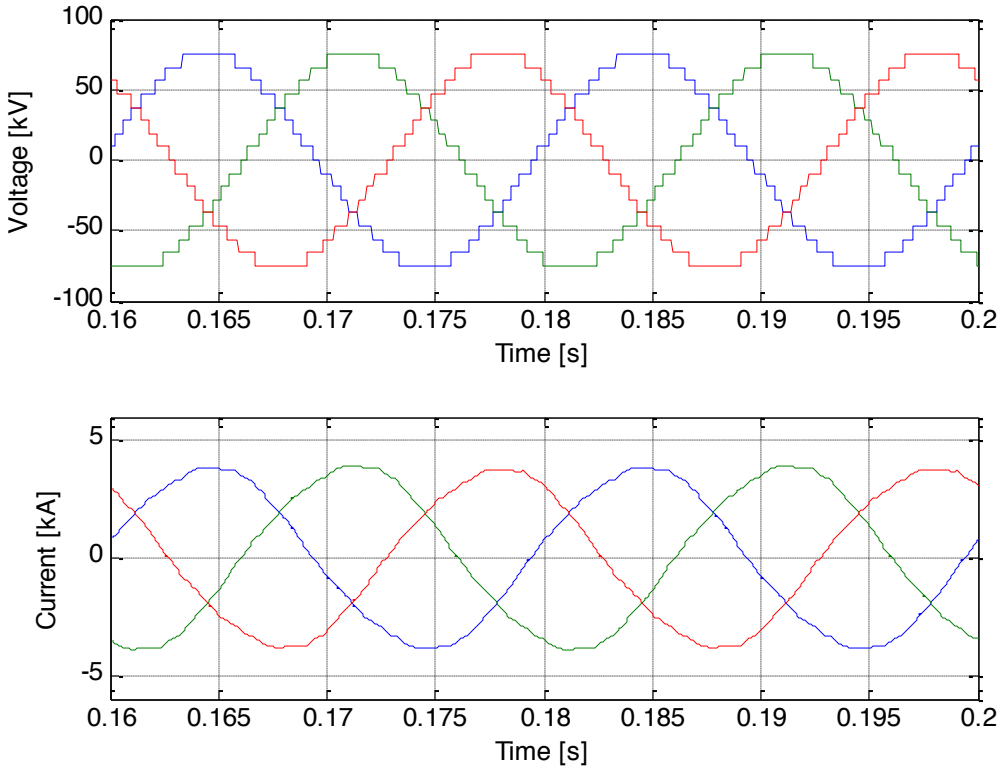

Figure A 6 Voltage and current waveforms in a seventeen-level converter.

Table A 6

THD Voltage	THD Current	Firing angles (deg)
0.0245	0.0073	2.5267 12.8629 19.4863 25.9779 34.5322 46.0372 54.5112 68.3424

NINETEEN-LEVEL CONVERTER

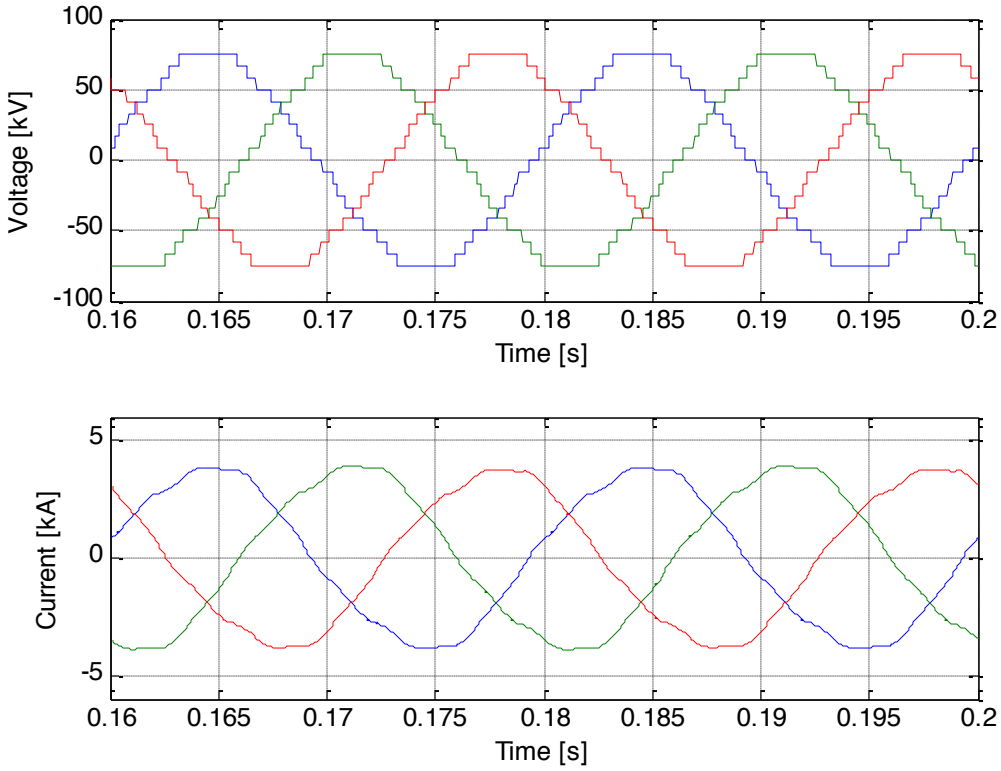

Figure A 7 Voltage and current waveforms in a nineteen-level converter.

Table A 7

THD Voltage	THD Current	Firing angles (deg)
0.0227	0.0069	4.6639 13.3098 16.8106 23.7033 29.7365 38.7262 50.5120 57.7198 65.9532

TWENTY ONE-LEVEL CONVERTER

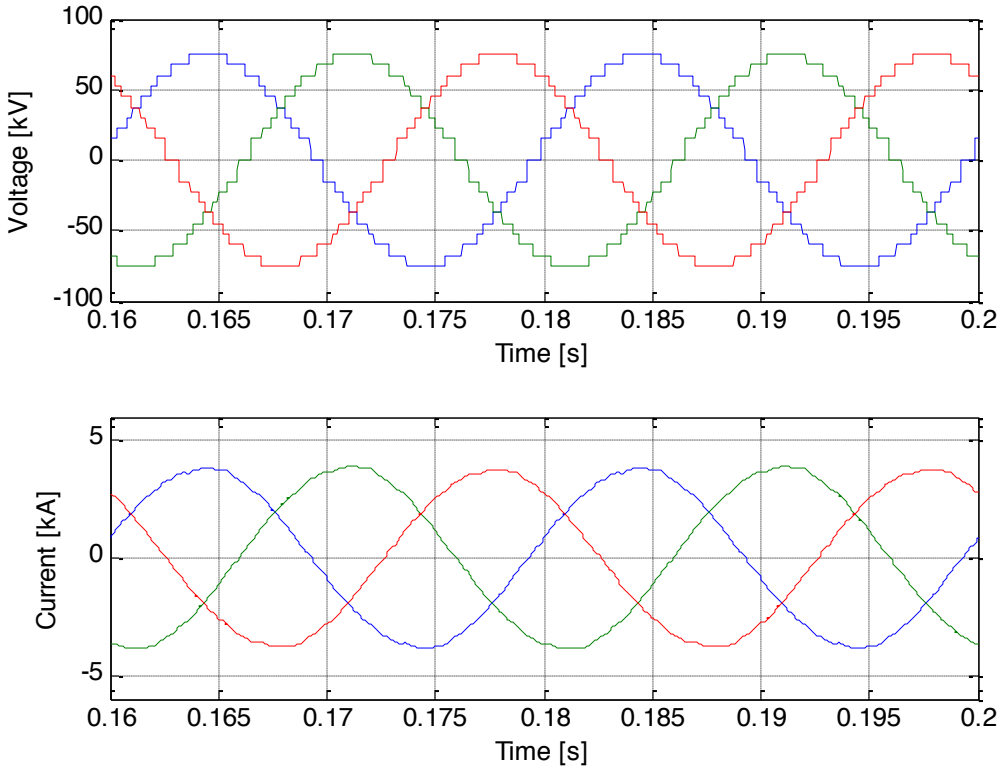

Figure A 8 Voltage and current waveforms in a twenty one-level converter.

Table A 8

THD Voltage	THD Current	Firing angles (deg)
0.0204	0.0080	5.7181 5.8213 14.9313 22.1620 26.7915 34.1655 42.5364 47.6128 59.6048 74.3642

TWENTY THREE-LEVEL CONVERTER

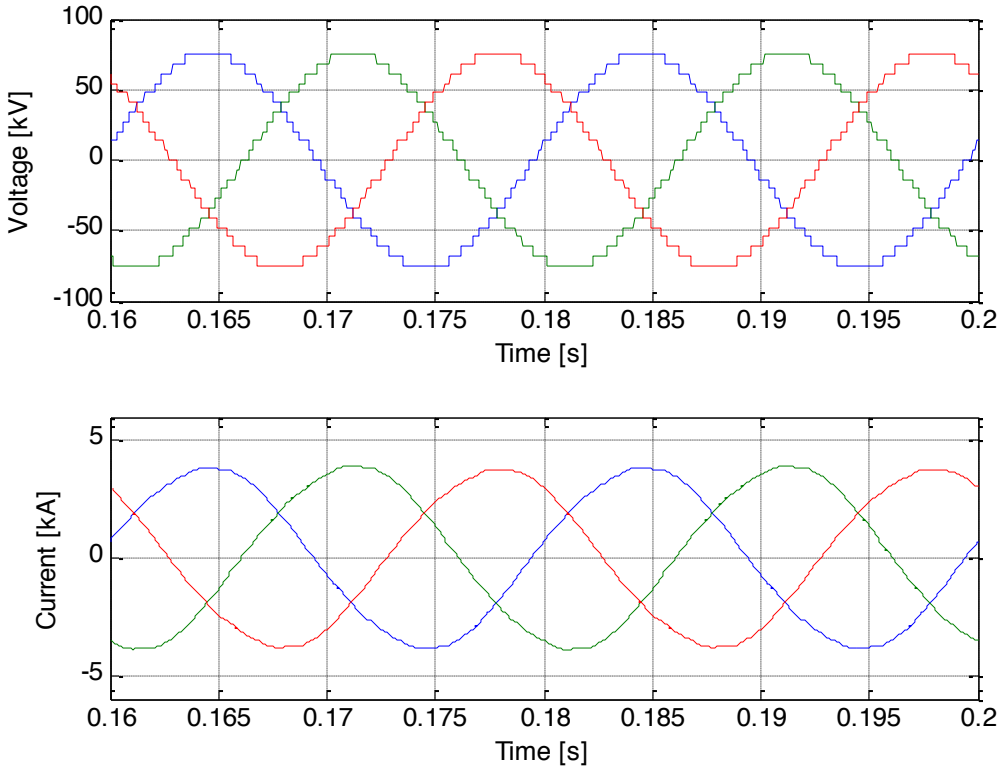

Figure A 9 Voltage and current waveforms in a twenty three-level converter.

Table A 9

THD Voltage	THD Current	Firing angles (deg)
0.0110	0.0052	3.6555 6.8468 15.0172 19.5665 24.4768 29.9485 36.8011 45.3840 50.4031 59.9142 71.2129