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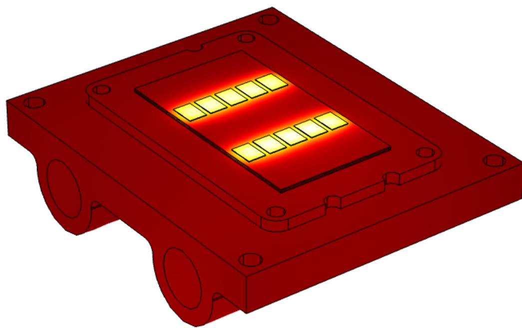

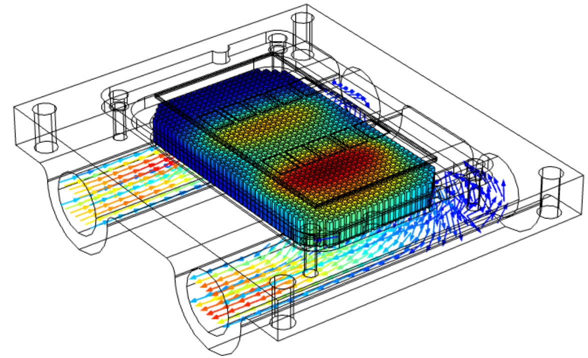

Thermal transport investigation of SiC Power Semiconductor Modules

Master of Science Thesis in Electric Power Engineering

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Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2020

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Abstract

Since power modules like other electronic devices are shrinking in size and the power demand is still high, there is a growing demand for better cooling technology in the automotive industry. Because the modules for three-phase inverters are becoming smaller in size and power loss is still high, extra pressure is being placed on the packaging system of the module and the cooling system to perform at a higher level. Therefore in this thesis work, an investigation was conducted regarding the heat distribution of the material Graphene when implemented as a sheet layer in a power module packaging system, as well as Graphene fins in a liquid cooling system.

The investigation was conducted around the CAB450M12XM3 SiC power MOSFET module to improve its thermal distribution between the packaging layers when Graphene is introduced, using the software COMSOL Multiphysics. Moreover, the thermal distribution of a cold plate before and after Graphene fins were introduced. The investigation was carried out in a three-phase study. The first phase included creating a thermal model for the power module CAB450M12XM3 in COMSOL and verify it with the datasheet value of the thermal resistance. The second phase of the work involved choosing a cooling strategy for the module and implement it in COMSOL. In the third and last phase of the work, Graphene was implemented as a layer and as fins to help spread and distribute the heat better than the current solution.

Our findings can be split into three sections, where each section of the results correspond to one of the phases conducted. The results obtained from the first phase showed that the CAB450M12XM3 has a seven-layer packaging system, with the base plate included. In this work, the calculated power loss calculation indicated that each switch has a power dissipation of 570 W. The simulation results showed a lower thermal resistance value than the presented value in the datasheet. This was proven to be due to the heat spreading effect and the thermal coupling. However, the error percentage was low and could be considered similar to the actual module and therefore qualified for further analysis. Results from the second phase indicated that a liquid cooled cold plate is the most optimal cooling strategy for a power module. The thermal resistance of the cold plate obtained from the simulation was very close to the datasheet value. Moreover, the results showed that the fin shapes of the heat sink influences its total thermal resistance. Lastly, the Graphene investigation showed that a Graphene layer below the copper layer improves the thermal distribution and decreases the working temperature by approximately 2%. The Graphene fins showed an improvement as well with 1-2% difference.

Keywords: Thermal distribution, Graphene, Power module, SiC MOSFET, liquid

cooled cold plate, COMSOL Multiphysics

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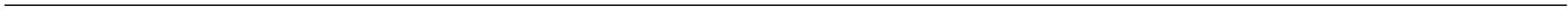
Finally, we would like to express our sincere gratitude to the Department of Electric Power Engineering at Chalmers for their support throughout the project.

Abdullah Al-Safi & Yasin Sharifi
Gothenburg, June 2020

List of abbreviations

AIN	Aluminum Nitride
DBC	Direct Bonded Copper
DDCP	Deep Drilled Cold Plate
FEM	Finite Element Method
FTCP	Formed Tube Cold Plat
IGBT	Insulated Gate Bipolar Transistor
MCCP	Machined Channel Cold Plated
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PFCP	Pocketed Folded-Fin Cold Plates
RMS	Root Mean Square
Si3N4	Silicon Nitride
SiC	Silicon carbide
TIM	Thermal Interface Material



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1
Introduction

1.1 Background

Packaging technology in power modules is one of the key issues in a power electronics system, which can affect the system performance dramatically. Compact high-temperature power modules with appropriate cooling systems are attractive for the automotive industries. Thus, a novel thermal design of a power module to achieve an adequate cooling system would be of interest. Nowadays, SiC (Silicon Carbide) and insulated gate bipolar transistor (IGBT) modules have been utilized in several application areas such as electric cars, wind turbines, and high voltage DC systems.

1.2 Aim

The aim of this project is to build a base SiC power module design including a cold plate in COMSOL Mulitiphysics. Thereafter, to investigate the thermal dissipation from the power module when Graphene film is introduced as a layer close to the chips as well as to a modified heat sink when copper fins have been replaced with Graphene fins. Finally to investigate the impact of various fin designs on the thermal distribution.

1.3 Scope

This project will focus on the thermal design concept and simulation of heat dissipation from the SiC power module to the modified heatsink. Introducing Graphene with high in-plane thermal conductivity to the power module and heat sink to enhance the heat spreading on the surface of the module and decreases the temperature of the hot spots. The Graphene film is applied as a layer on the power module. Moreover, investigating the thermal transport from top to down when replacing aluminium fins with Graphene fins. The simulation analysis in this project is done by using software COMSOL Multiphysics.

Having mentioned all the above, the objective of this thesis is:

- Determine the power losses of a SiC power module.

- Build a 3D thermal model of the power module and cold plate and verify it with the datasheet for further analysis.
- Investigate the thermal distribution from the power module and cold plate.
- Create variations of fin designs on the cold plate to improve the heat dissipation from the chips.
- Evaluate the Graphene material when used with the power module packaging technology, as well as replacement of aluminium fins.

2

Component and Modelling Theory

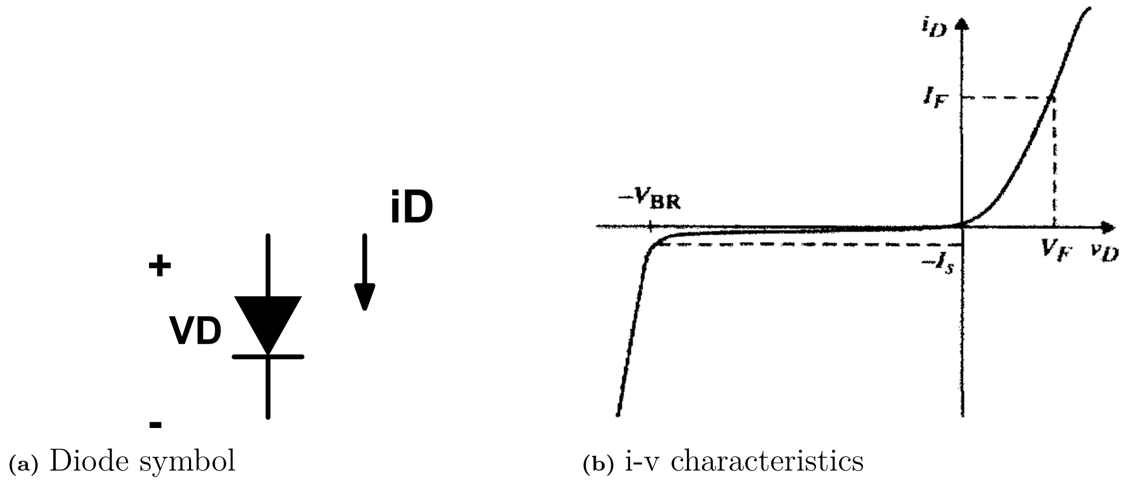
This chapter will go through all theory that was used in this work to achieve the specified objectives. Subjects included such as devices in the power module, power module's packaging system, thermal modeling and heat transfer in solids, cooling strategy as well as the properties of the material Graphene.

2.1 Power devices

This section will go through the working principle of power semiconductor devices that are included in inverter modules. Since this thesis is investigating a MOSFET power module, it is necessary to go through the working principle of the MOSFET, and the diodes. To understand the working principle one has to look at the equivalent circuit and the i-v (current-voltage) characteristics of each device.

2.1.1 Power Diode

There are two main types of power diodes, rectifier diodes, and fast recovery diodes. Rectifier diodes are used with a grid frequency of 50/60Hz. While fast recovery diodes are used with higher frequencies ranging up to 20kHz. The equivalent circuit for the diode can be derived by approximating the forward characteristic is the imaginary line that ranges between 25-80% in figure 2.1b. The forward voltage drop V_d can be specified as the distance between the two points, origin and the straight line's intersection with the x-axis. The forward resistance of the diode can be identified through the slope of the straight line. By identifying the parameters named above, the diode can be represented as resistance with a voltage source connected in series. [1]



(a) Diode symbol

(b) i-v characteristics

Figure 2.1: Symbol and i-v characteristics for a diode [2]

Therefore, the power losses can calculated as follow,

$$P_{diode} = (R_D i(t) + V_D) i(t) = R_D i(t)^2 + V_D i(t) \tag{2.1}$$

$$P_{diode}(t) = \frac{1}{T}\int_0^T R_D i(t)^2 + V_D i(t) dt = R_D i_{RMS}^2 + V_{D(avg)} \tag{2.2}$$

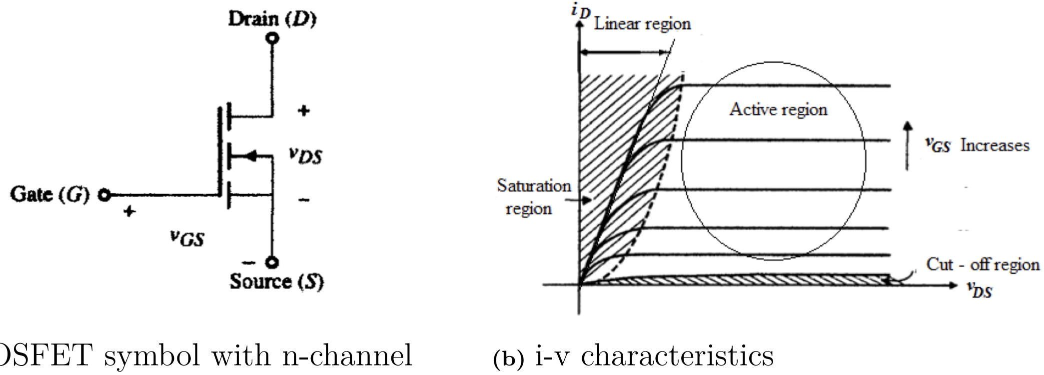
The analytical equation for conduction losses is,

$$P_{cond,diode} = \frac{1}{2}(V_D \frac{I}{\pi} + R_D \frac{I^2}{4}) - m * cos(\phi)(V_D \frac{I}{8} + \frac{1}{3\pi} R_D I^2) \tag{2.3}$$

where m is the modulation index, $cos(\phi)$ is power factor. V_D and R_D are obtained through the i-v forward characteristics of the diode.

2.1.2 Power MOSFET

Metal-oxide-semiconductor field-effect transistors (MOSFET) is a device with three terminals, gate, source, and drain, see figure 2.2a. Figure 2.2b shows the i-v characteristics of an N-channel MOSFET, as it can be observed from the figure that the MOSFET does not have a forward voltage drop. The MOSFET is in a blocking phase when there is a positive voltage V_D between the drain and source and the threshold voltage is larger than V_G. The i-v characteristics have the form of a straight line for low values of V_D. When the gate voltage V_G is defined $R_{DS(on)}$ is specified. [1]



(a) MOSFET symbol with n-channel (b) i-v characteristics

Figure 2.2: Symbol and i-v characteristics for a MOSFET with n-channel [2]

For simplicity the MOSFET can be modeled as a resistor only R_{on} and the on-state power loss equation can be obtained through the relations

$$P_{MOSFET}(t) = R_{on}i^2(t) \tag{2.4}$$

$$P_{loss-MOSFET} = \frac{1}{T}\int_0^T R_{on}i^2(t)dt = R_{on}i^2_{RMS} \tag{2.5}$$

Since there is no voltage source connected in series with the resistance in the MOSFET equivalent model, the reverse conduction losses are not taken into account. The analytical equation for the conduction losses can be derived as,

$$P_{cond-MOSFET} = \int_0^{\frac{T}{2}} R_{on}(Isin(\omega t))^2\tau(t)dt \tag{2.6}$$

R_{on} is the ON-state resistance and $\tau(t)$ is the duty cycle taken from the pule pattern be calculated from eq.2.7.

$$\tau(t) = \frac{1}{2}(1 + msin(\omega t + \phi)) \tag{2.7}$$

Now by suubsitiuting (2.7) in (2.6), the conduction losses for a MOSFET can be written as

$$P_{cond-MOSFET} = R_{on}I^2(\frac{I}{8} + \frac{m * cos(\phi)}{3\pi}) \tag{2.8}$$

2.1.3 Switching losses

The MOSFET's maximum achievable switching frequency is dependent on the switching losses. The switching losses occur during the turn-ons and turn-offs of the switch and the anti-parallel diode. In turn, the switching losses are dependent on the switching energy, similar to other devices, the energy loss can be calculated through the

product of voltage and current as, [1]

$$E_{ON} = \int_{t_{ON}} V_D(t)i(t)dt \tag{2.9}$$

$$E_{OFF} = \int_{t_{OFF}} V_D(t)i(t)dt \tag{2.10}$$

$$E_{SW} = E_{On} + E_{OFF} \tag{2.11}$$

According to [1], the off-state leakage current for a power MOSFET is very low and therefore the blocking losses can be neglected. The analytical equation for the switching losses is

$$P_{SW(MOSFET)} = f_{SW}E_{SW}(\frac{1}{\pi}\frac{i}{I_{ref}})(\frac{V_{DC}}{V_{ref}}) \tag{2.12}$$

Finally, the switching losses for the diode is calculated in same manner by identifying the switching energy losses. The switching losses for the diode can be calculated by

$$P_{SW(Diode)} = f_{SW}E_{SW(Diode)}(\frac{1}{\pi}\frac{i}{I_{ref}})(\frac{V_{DC}}{V_{ref}}) \tag{2.13}$$

2.2 Power electronics module

Power electronic devices have the task of transforming one form of electrical energy to another. The transformation could be AC-DC, DC-AC, and DC-DC. The transformation of AC-AC is easily done with a transformer. Due to the saturation of the core, DC-DC transformation is done through power electronic devices instead of a transformer. An AC/DC devices are called rectifiers and DC/AC devices are called converters or inverters. [1]

Power converters consist of three main components:

- Active components, the mechanisms that control the power flow (on and off) within the device. The device has two states, on-state when conducting and off-state when forward or reverse blocking. The device can only operate in one state at a time.
- Passive components are components that temporarily store energy within the device. Inductors, capacitors, and transformers are examples of such components. These components are constructed for the operating frequency, cooling method, voltage, level of integration, and the type of insulation material that has been used.
- Control unit, components that control the flow of energy within the device in such a way that the current and voltage follow the reference signals that

ensure the appropriate behavior of the converter. Examples of such components are, analog and digital devices, processors, signal converters, and sensors.

Electric vehicles and hybrid electric vehicles are both supplied with energy through either battery or supercapacitor. These types of energy sources provide a DC voltage which creates an obstacle since the electric motor requires an AC source. Therefore, an inverter is needed to transform the energy source from DC to AC.

2.3 Packaging of power devices

Power devices can have multiple types of packaging. Depending on the voltage and current rating as well as the overall use of the application, the type of packaging can vary. One can define the packaging system as everything surrounding the actual die. The packaging system serves multiple purposes, such as a form of protection for the die and acts as a support structure. Moreover, the packaging system helps enhance the thermal performance of the device by keeping the junction temperatures low and guarantees that the device reaches the desired lifetime. In general, there are a certain number of requirements that a packaging system has to meet [1]:

- High reliability, to reach a long lifetime.
- The high electrical conductivity of the components, to decrease undesirable electrical properties such as parasitic resistance, capacity, and inductivity.
- Supplementary insulation between switches, and insulation between the heatsink and electrical circuit. This is for power modules.

2.3.1 Structure of the power modules

The packaging of a power module contains multiple configurations of switches and diodes, half-bridges, and three-phase inverters being the common ones. To increase the abilities to handle current switches and diodes in the module are connected in parallel. IGBT:s and MOSFET:s are widely used in power modules, which one to use is dependent on the use of the application.[3]

Figure 2.3 shows a cross-sectional view of a typical packaging layout for a power module. On top are the silicon chips which are soldered on a substrate called ‘’ direct bonded copper” (DBC). The DBC acts as electrical insulation and consist of three layers, two copper layers, and a ceramic insulation substrate. The ceramic substrates task is to isolate the current-carrying parts in the module. The DBC layer is attached to the baseplate by a second solder layer. The baseplate forms mechanical support around the module and acts as a heat spreader by increasing the heat dissipating area. Lastly, a heatsink is attached to the baseplate with a Thermal Interface Material (TIM). The heat sink helps bring down the temperature of the module to the desired levels and the TIM layer adds additional support to it by filling the small air vacuums wit grease instead of air. Because air has a low heat conductivity value. Multiple TIM options are used today in the industry, the most

common is thermal grease[3]

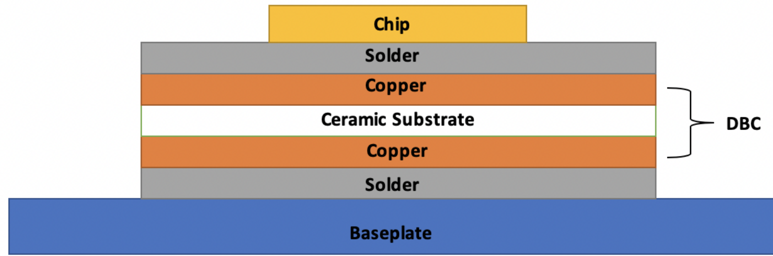


Figure 2.3: All the material layers in a power module.

2.4 Theory of thermal models

A thermal problem can be transformed into an electrical problem by exchanging the electrical and thermal parameters. This is because of the equivalence of the differential equations, all procedures done on an electrical network can be shifted to thermal networks. The electrical and thermal parameters that are equivalent to each other are presented in the table 2.1. To calculate the thermal problem, one has to solve the electrical equivalent circuit.[1]

Table 2.1: Equivalent thermal and electrical parameters.

Electrical Parameters	**Thermal Parameters**
Voltage (V)	Temperature difference (ΔT)
Current (I)	Heat Flux (P)
Charge (Q)	Thermal Energy (Q_{th})
Resistance (R)	Thermal Resistance (R_{th})
Capacitance (C)	Thermal Capacitance (C_{th})

The thermal impedance (Z_{th}) can be represented and calculated by different thermal resistances and capacitances according to

$$Z_{th} = \frac{T_j - T_a}{P} = \frac{\Delta T}{P} \tag{2.14}$$

where T_j represents the junction temperature of the power semiconductor, T_a is the ambient temperature or the temperature of the case and P is the power losses from the semiconductor chips.

Two types of thermal models can describe a power module with a lump of parameters, Cauer and Foster models. Each one of the models can be represented with an equivalent circuit consisting of a heat source and multiple thermal impedances, see figures 2.4 & 2.5. Both models represent a network of thermal resistors R_{th} and thermal capacitances C_{th}, each link of R_{th} and C_{th} represents one layer of the typical

power module packaging material. In the cauer model, the thermal resistances and capacitances are connected in a shunt. Since the power losses are produced in the system it will make the temperature rise in the nodes and the thermal energy will be stored in the capacitances. The stored energy in the capacitor is proportional to the temperature difference to the condition before the power losses were inserted into the system. Thus, this model describes the physical aspects of the power module.[1]

The Foster model on the other hand has the thermal resistances and capacitances connected in parallel. This type of RC-link can be replaced without affecting the transient response of the system. Where in the Cauer model, the replacement of R and C will affect the transient response of the system, as when the real system would do if the layers are exchanged. Therefore, in this thesis, the Cauer model was used.[1]

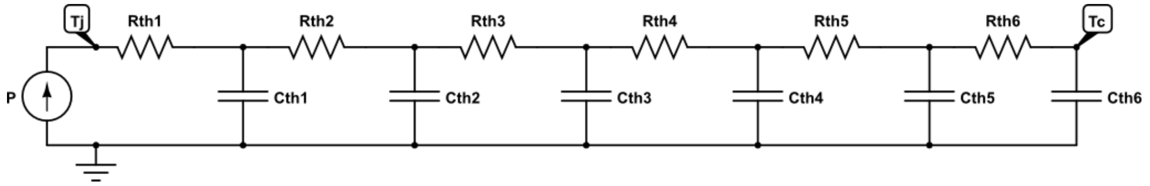


Figure 2.4: Equivalent circuit for Cauer model

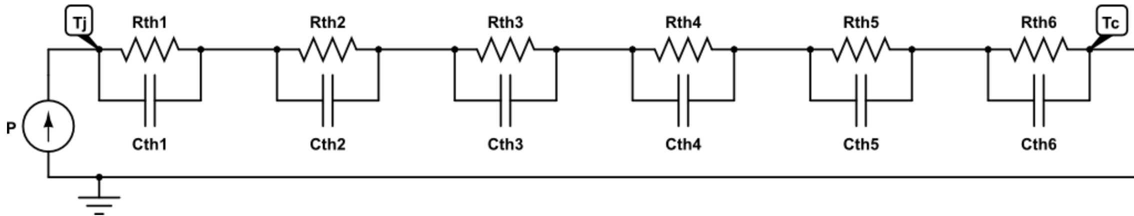


Figure 2.5: Equivalent circuit for Foster model

To calculate the thermal resistance and capacitance theoretically using the Cauer model, one has to identify a couple of parameters first. The two equations used for calculating R_{th} and C_{th} are

$$R_{th} = \frac{d}{AK} \tag{2.15}$$

$$C_{th} = c\rho dA \tag{2.16}$$

$$\tau_{th} = R_{th}C_{th} \tag{2.17}$$

where R_{th} denotes the thermal resistance [K/W], C_{th} is the thermal capacity [J/K], τ_{th} represents the time constant, d is the thickness [m], A is the total area of the layer [m^2], K is the thermal conductivity [W/(mK)], c is the specific heat capacity [J/(kgK)] and ρ is the specific density [kg/m^3] of the material.

To take the heat spreading effect into consideration, the area A of each layer needs to be calculated with a heat spreading angle, θ. The total area A(z) of the layer is now a function of the length in the z-direction and can be calculated as

$$A(z) = (a + 2ztan(\theta))(a + 2ztan(\theta)) \tag{2.18}$$

where a and b are the side length in the x-y direction, z is the length (thickness) in the z-direction and θ is the heat spreading angle.

2.4.1 Transient thermal impedance

The transient thermal impedance $Z_{th(x-y)}$ is defined as the change in temperature between the point x (T_x) and the point y (T_y) as a function of time divided by the change of power dissipation over time. Since there will be multiple reference points within the power module the thermal impedance can be described with a matrix. The thermal impedance matrix can be written as

$$Z_{th} = \begin{bmatrix} Z_{th(11)} & ... & Z_{th(1j)} & ... & Z_{th(1n)} \\ . & . & . & . & . \\ . & . & . & . & . \\ . & . & . & . & . \\ Z_{th(i1)} & ... & Z_{th(ij)} & ... & Z_{th(in)} \\ . & . & . & . & . \\ . & . & . & . & . \\ . & . & . & . & . \\ Z_{th(n1)} & ... & Z_{th(nj)} & ... & Z_{th(nn)} \end{bmatrix} \tag{2.19}$$

All elements included in the thermal impedance matrix can be obtained by measurements or finite element analysis (FEA) simulations through

$$Z_{th} = \frac{T_j(t) - T_a}{P(t)} \tag{2.20}$$

The thermal transient performance is normally described by a Foster model. From measurements and FEA simulations, an expression for the thermal impedance can be derived

$$Z_{th(x-y)} = R_{th1}(1 - e^{\frac{-t}{\tau_{th1}}}) + R_{th2}(1 - e^{\frac{-t}{\tau_{th2}}}) + ... = \sum_{i=1}^{n} R_{thi}(1 - e^{\frac{-t}{\tau_{thi}}}) \tag{2.21}$$

where n is the number of R_{th}/C_{th} pairs and τ_{th} is the time constant.

2.5 Heat transfer in solids

The phenomenon transportation of heat can be described as the transportation of thermal energy as a result of a gradient in temperature. The heat flux is described by Fourier's law

$$q = -k \bigtriangledown T \tag{2.22}$$

which defines the theory behind heat conduction. The equation states that thermal conductivity is proportional to the magnitude of the temperature gradient, q flows from higher temperatures to lower temperatures. q is the heat flux measured in (W/m^2), k is the thermal conductivity (W/m K) and $\bigtriangledown$ is the gradient.[4]

Since the goal is to model a realistic system using COMSOL, the heat flux, or also named the heat convection must be taken into consideration. The heat convection can either be natural or forced, is added to the boundaries of the system, and is dependent on the geometry and its length. When natural convection is implemented, the system is cooled through natural air. The steady-state heat flux density is defined by

$$q_s = h(T_S - T_m) \tag{2.23}$$

when convective cooling/heating is involved. h is the heat transfer coefficient $W/(m^2K)$, T_s is the surface temperature and T_m is the media temperature.

In this study there are different materials involved, the heat conduction or heat diffusion must be taken into consideration as well. The heat diffusion is described by

$$\rho C \frac{\delta T}{\delta t} = \bigtriangledown k(T) \bigtriangledown T + q_v \tag{2.24}$$

where ρ is the density, C is the heat capacity, $\frac{\delta T}{\delta t}$ is the difference of temperature over time, and $\bigtriangledown T$ is the gradient temperature.

2.6 Power module cooling

Since power modules are high power electronic devices there will be extreme heat flux stresses on the cooling system. The high stresses on the cooling system cannot be solved with air cooling. By using air cooling, a heat spreader is needed to carry the heat from the device to the air-cooled surfaces. The heat spreaders come in many shapes and sizes depending on where and how they are used, they are mostly known as heat sinks. The heat spreaders are only sufficient at low heat fluxes. At higher heat fluxes the heat spreader will have less of an impact since the thermal resistance in the heat spreader will become unacceptably large compared to the

difference in temperature between the base and the coolant. That means it would require very large heat spreaders to cool down a high-power module and thus this solution becomes unattractive and a more advanced solution is required. It appears that in the high power module industry when the power dissipation level has reached 1500 W and even lower levels, the cooling process is liquid-based [5].

2.6.1 Liquid cooled cold plate

When the abilities of air cooling to cool down the electronic device are not enough, there is a shift towards a liquid-based cooling system. The reason for it is the liquid material properties which make this type of cooling a better choice for high temperatures. The heat transfer coefficient for liquid-based cooling is significantly higher when compared to forced air convection. In comparison the heat transfer coefficient for forced air convection is 100 W/m^2K while for liquid is around 10 000 W/m^2K[6].

The liquid cooling system is considered to be a closed-loop system with multiple components contributing to the cooling process. The main components in the system are a cold plate, heat exchanger, pumps and tubes. The cold plate is the component that is attached to the power module with TIM. The purpose of the heat exchanger is to cool down the liquid when it's been through the cold plate. The heat exchanger transfer heat into the environment and this is done by adding an extra fan to provide adequate airflow to the heat exchanger. More components can be added to the system such as liquid reservoirs, valves and filters[7].

2.6.2 Cold plate models

Multiple cold plate models are being used in the industry today with different materials and fluid flow channels. Selecting a cold plate model will be dependent on the size of the module and the heat dissipation caused by the chips. The cold plate models are classified into four groups, as described below[5].

Formed Tube Cold Plate (FTCP). This is the simplest cold plate model with the coolant channels that are simply soldered or attached to the cold plate with a thermal epoxy material. This model does not offer a high performance because of its simple design and therefore its use is rather limited.

Deep Drilled Cold Plate (DDCP). When the power dissipation reaches high levels, this becomes one of the better alternatives. Since with higher power dissipation the thermal resistance of the plate and tubes becomes extremely high. In this model, the channels or deep holes are drilled into the cold plate itself. The channels and holes are arranged with end caps to create a flow path for the liquid through the plate. The shape of the flow path is dependent on the placement of the power modules.

Machined Channel Cold Plated (MCCP). This model is more enhanced compared

to the previous ones, mostly used when high thermal performance is required. In this model design the channels are machine-cut inside the plate and a cover is later attached to the top of the plate where the modules will be placed. The big advantage of this model is that the channels can be shaped with multiple patterns to enhance the thermal performance of the plate. The width of the channels can be changed as well to increase the fluid follow which will later decrease the thermal resistance of the plate.

Pocketed Folded-Fin Cold Plates (PFCP). This is a more enhanced version of MCCP, where the heat transfer coefficient and the surface area are improved by introducing fins in the fluid passage. The fins can be soldered inside the plate or below the cover. The fins can be shaped in multiple ways depending on the performance required from the cold plate.

With all the models mentioned above there is an inlet and outlet where the fluid flows. Which model to choose as a cooling system will depend on four factors, total heat removed, heat flux, pressure drop and cost. The cost can vary significantly between the models depending on the size and the material used.

2.6.3 Fin models

Likewise the cold plate model there are multiple fin models to choose from. The basic type is straight fins with rounded, triangular or squared edges. More advanced options are herringbone, lanced, offset, lanced and offset, ruffled, lazily ruffled and perforated fins. Similar to their varying shape design the performance of each fin design is not equal. At low velocities of flow rate the performance of the square and round-shaped fins is approximately the same[5].

2.7 Graphene material

The growth of power electronics towards minimizing the size of the devices produces severe thermal dissipation problems that threaten the performance and reliability of the devices. Therefore, this problem is considered to be one of the big challenges the power electronics industry is facing. One way that this problem is being solved is by introducing heat spreading materials that will move extreme heat away from the devices and later reduce the operating temperature of the device. For this to be possible, the heat spreading material must have a very high thermal conductivity level. Moreover, the material needs to be thin, strong, and flexible for it to be combined with the rest of the components included the power electronic devices [8].

Graphene is said to be a material that arises to the challenges named above but where does it come from. To begin with, there are two kinds of Carbon crystals, Graphite and Diamond. While the first-named is plentiful the other is very precious, however, they are both made of Carbon. Normally Graphite is used to make elec-

trodes while it can be used as an electrical insulator. Even though both materials are made of carbon, they are very different from each other and that can be seen in their atomic structure. For Diamond, every carbon atom is surrounded by four other carbon atoms and creating a tetrahedron. The Diamond crystal mesh is in 3D-space is created though the periodical repetition of the tetrahedron. In comparison, Graphite has a layered structure and with each layer the carbon atoms are organized in hexagons. Each carbon atom is enclosed by three other atoms creating a layer, the plane of layers that forms the structure of Graphite is called the basal plane. What gives Graphite the upper hand is the strong carbon bonds within each layer, stronger than the bonds in Diamond. On the other hand, the bonds between each layer, known as Van der Waals bonds, are weaker compared to Diamond. Because of this weakness Graphite appears to be ‘’soft” and easy to peel off[9][10].

A single layer of carbon atoms of Graphite is known as Graphene, which has outstanding properties compared to other materials. As an example, the mechanical strength is better than in diamond, and due to the decrease in scattering affect the electrons in Graphene move very fast. The electrons make up the electricity in Graphene, by allowing the electrons to move at very rapid speeds.

Because of its two-dimensional shape, it is known to be the thinnest and strongest material produced. It would take an excessive amount of force to break through a sheet of Graphene. Even though the bonds between the material’s carbon atoms are very strong, the material itself is very flexible. Graphene can be twisted, pulled, or curved without breaking [11].

Moreover, Graphene is a brilliant heat conductor with very high thermal conductivity levels. The thermal conductivity levels are very much dependent on the thickness of the layer. This can be explained by three reasons. The first one is the grain size, the Graphene layer is composed of separate Graphene sheets that contain great amounts of defects that increases the phonon scattering and thus limit the thermal conductivity. The second reason is alignment because Graphene being very flexible, wrinkles, and layer misfits will be very hard to avoid during the sheet formation. A bad alignment structure could strongly harm the thermal performance of Graphene. The third reason is phonon interfacial scattering, where the bonding layer between the Graphene layers could lead to high phonon interfacial scattering. This will later lead to a decrease in thermal conductivity. As one study shows that by decreasing the thickness the thermal conductivity increases. Table 2.2 shows the thermal conductivity levels for each thickness used.

Table 2.2: Thermal conductivity for Graphene with different thicknesses.[8]

Thickness (μm)	Thermal conductivity (W/mK)
0.8	3200 $\pm$ 330
1	2942 $\pm$ 308
2	2527 $\pm$ 230
3	2461 $\pm$ 197
4 - 6	2250 $\pm$ 220

Although the material itself is outstanding it does come with a challenge, the process of producing a single layer of atoms for its properties to be measured is enormously difficult. Therefore, one has to be realistic when implementing the material in simulations to draw better conclusions.

3

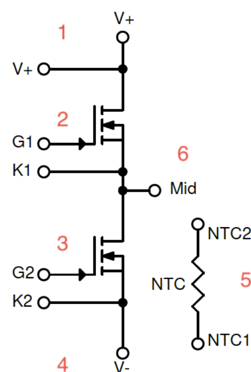
Thermal modelling set-up of the power inverter module

This chapter will go through the build-up process and simualtions for the thermal model of the the power module CAB450M12XM3 in COMSOL Multiphysics. As well as the Cauer thermal model for comparison purposes.

3.1 Description of the module CAB450M12XM3

The power module under investigation is the newest generation three-phase power inverter (CAB450M12XM3) manufactured by Wolfspeed and used for vehicle applications. The module is a third-generation SiC MOSFET with a 1200V half-bridge structure and a current rating of 450A. The module has the thermal characteristics of SiC power devices, which gives it the advantage of operating at a temperature of 175 C. The thermal resistance per switch position is 0.11 K/W. The physical device and its electrical diagram are shown in figures 3.1a and 3.1b. From the electrical diagram in figure 3.1b, one can see that the highest voltage reference is at point 1 and the lowest voltage reference is at point 4. Points 2 and 3 indicate the two SiC MOSFETS. Point 6 shows the output terminal. Lastly, point 5 displays the NTC device which is a temperature sensor.

(a) Overview of the module



(b) Electrical diagram of the module

Figure 3.1: Power module CAB450M12XM3 [12].

The module is covered with a package housing that covers most of the device besides the base-plate where on the backside a heatsink can be attached. Then there is a top cover that covers the electrical components inside and acts as a form of protection. The package housing and the top cover are both made of plastic. By unveiling the top cover, there is thermal gel covering the module from the inside and is acting as an insulator. Beneath the thermal gel lays all the electrical components. In total there are two switches connected in parallel and each switch has five chips. The layout of the electrical component can be seen in figure 3.2.

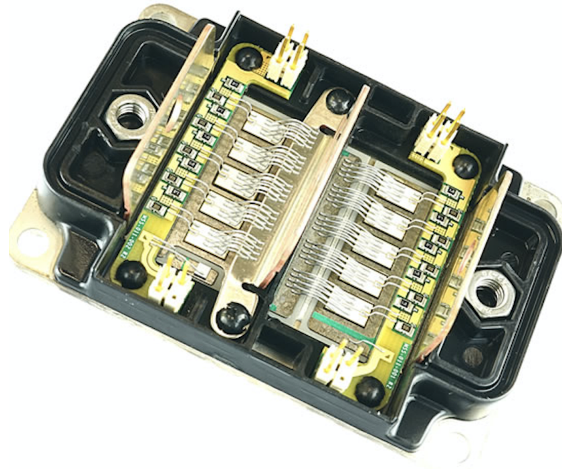


Figure 3.2: Inside view of the power module CAB450M12XM3 [13].

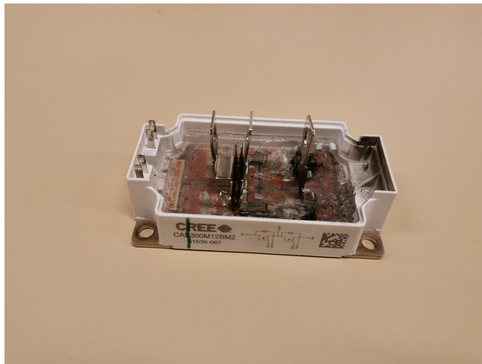
The thermal packaging aspects of the module is mostly unknown due to secrecy. However, it is stated in the datasheet that a silicon Nitride insulator has been used and the base plate is made of copper. For further information a reference model was used from the same manufacturer, the module is presented in the next chapter.

3.2 Reference module CAS300M12BM2

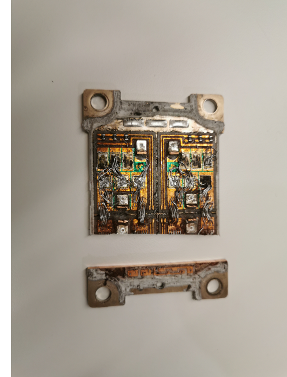
The power module CAS300M12BM2 is an older module in Wolfspeed / Cree series of SiC Power Modules. The device is a 1200V, all silicon-carbide half-bridge module. A cross-sectional and SEM/EDS analysis were done on this module to extract information such as what material has been used as insulation and their respective thickness. From the datasheet, it is known that the base plate is made of copper and an Aluminum Nitride insulator has been used.

By conducting an Energy Dispensive X-Ray Spectroscopy (EDS) which is a chemical micro-analysis technique in combination with scanning electron microscopy (SEM), structures with a very small thickness can be analyzed. The EDS method identifies the x-rays released from the sample throughout the bombardment process with an electron to illustrate the element arrangement of the analyzed volume. However, before conducting the analysis, a cross-sectional piece was cut off the module to

make the analysis possible to implement. Figure 3.3 illustrates the cross-sectional piece[14].



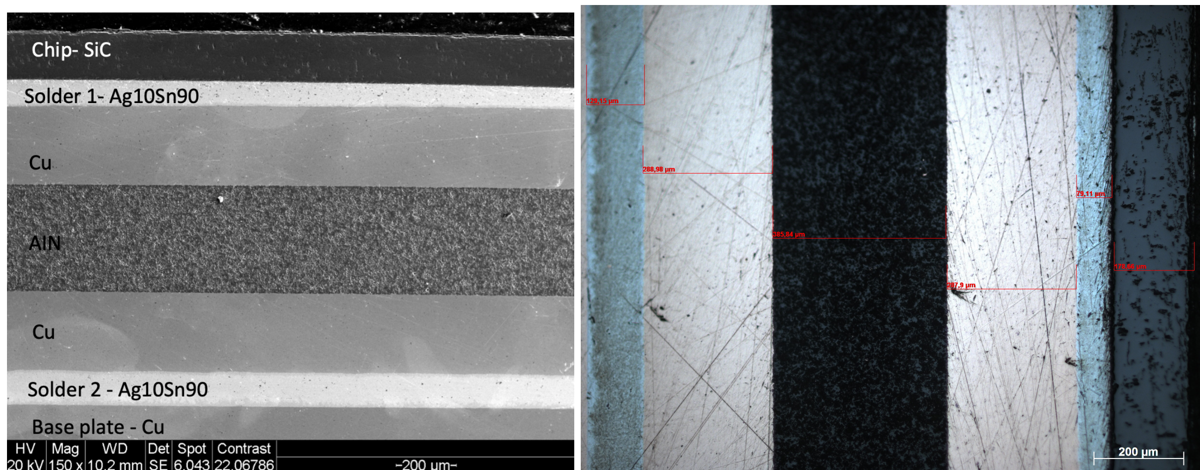
(a) Before removal of casing



(b) After removal of casing and cut for EDS analysis

Figure 3.3: Reference model CAS300M12BM2.

After the implementation of the analysis, the results are shown in figure 3.4. The results are in line with the datasheet, the chip is all silicon-carbide, the base plate is made of copper and an Aluminum Nitride insulator has been used as one of the DBC layers. For the other two DBC layers they are made of copper. The analysis shows the solder $Sn_{90}Ag_{10}$ has been used for both solder layers. In terms of thickness, figure 3.4b and table 3.1 summarizes the thickness for each layer.



(a) Insulation materials

(b) Material thickness

Figure 3.4: Materials and their respective thickness for power module CAS300M12BM2.

Table 3.1: Material thickness for CAS300M12BM2.

Material	Thickness (um)
SiC	178.66
Ag10Sn90 (Solder 1)	79.11
Cu (DBC)	287.9
AIN (DBC)	386.64
Cu (DBC)	288.98
Ag10Sn90 (Solder 2)	129.15

3.3 Power modules loss calculation

The power module CAB450M12XM3 has a nominal voltage of 600 V and a nominal current of 450 A. The total power loss for one switch is amounted by the conduction and switching losses of 5 MOSFETs and 5 body diodes. From the analytical equations presented in section 2.1, the power loss for the module with the system variables presented in table 3.2 and components parameter values presented in table 3.3, the total power loss could be calculated.

Table 3.2: The table demonstrates the input variable for the system.

Parameter	**Value**	**Description**
I_{ref}	450	Nominal current A
V_{ref}	600	Nominal voltage V
ma	0.084	Modulation index
ϕ	1.77	Power factor
I_{RMS}	400	RMS current
I_{peak}	565.7	Peak current
f_{sw}	10 kHz	Switching frequency
V_{DC}	300	DC voltage

Table 3.3: The table demonstrates the input MOSFET and Diod parameter for the power loss calculation.

Parameter	**Value**	**Description**
$R_{DS(on)}$	2.6 mΩ	MOSFET Drain-Source On-state Resistance
E_{ON}	11 mJ	Turn-ON switching energy, $T_j = 25°C$
E_{OFF}	10.1 mJ	Turn-OFF switching energy, $T_j = 25°C$
E_{Diod}	0.25 mJ	Diod switching energy
V_D	3.35 V	Diod Source-Drain voltage
R_D	2.96 mΩ	Body diod resistance

The results can be seen in table 3.4, where the total power loss amounts to 570.86 W for one switch and that equals to 114W per chip.

Table 3.4: The results obtained from the power loss calculation.

Power loss	MOSFET	Diod
Conduction losses	102.53 W	425.61 W
Switching losses	42.21 W	0.5 W
Total losses	570.86 W	

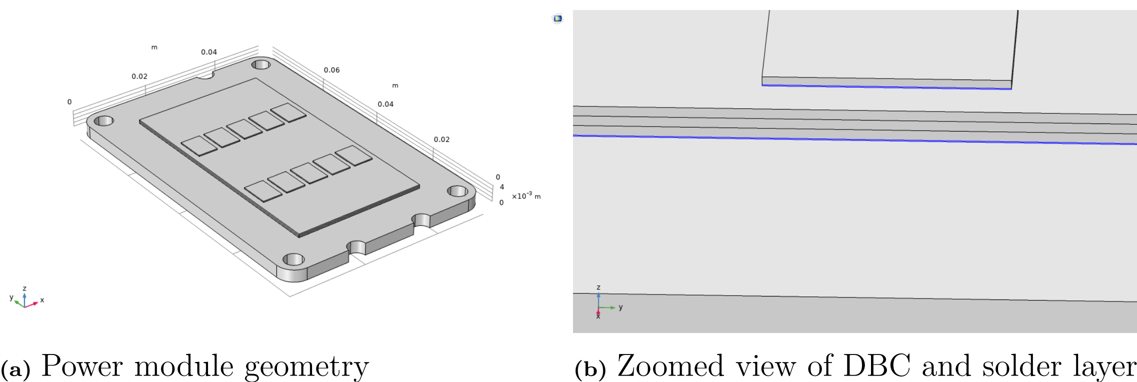
3.4 COMSOL model

COMSOL Multiphysics is a software environment for modeling and simulating physical systems using the finite element method (FEM). The software includes various modules for different physics. The main feature with COMSOL is the multiphysics capabilities, and when physics of different modules depend on each other, they can also be coupled together using multiphysics interfaces. In this study, COMSOL Multiphysics 5.4 is used for modeling the power module and for investigating the heat transfer and temperature distribution.

3.4.1 Geometry of the module

To create a thermal model of the power module in COMSOL Multiphysics, one of the first steps is to build the geometry. The geometry of the power module has been made based on information provided in the datasheet, extracted data from the inside view of the power module, and the measured data from the reference module.

The Datasheet contains information about the package and baseplate dimensions. The inside view of the power module reveals the position of the chips. The extracted information from the reference module reveals the dimension of each layer, such as the DBC and solder layer. To be able to simulate and visualize thermal distribution over different parts of the power module, the geometry in 3D-domain has been modeled. The result of geometry is shown in figure 3.5.



(a) Power module geometry

(b) Zoomed view of DBC and solder layer

Figure 3.5: Geometry view of the CAB450M12XM3 power module built in COMSOL

The geometry inserted in COMSOL Multiphysics is a simplified representation of the real module, consisting of stacked blocks based on the corresponding dimensions of the power module, to reduce the complexity of the simulation. For that reason, the package housing, terminal pins, and terminal leads and wire bonding have not been modeled. The dimension of each layer is shown in table 3.5. Die and Diesol represents the dimensions of the chips and chip's solder layer beneath respectively. The four DBC blocks represents the DBC layers, including the solder layer above the basplate.

Table 3.5: Dimension of each layers of the power module

Layer	Width x (mm)	Depth y (mm)	Height z (mm)
Die	5	7	0.17866
Diesol	5	7	0.07911
DBCUcu	33	10	0.28898
DBCSiN	33	10	0.38584
DBCLcu	33	10	0.28898
DBCsol	33	10	0.12915
Baseplate	53	80	3.00000

3.4.2 Materials of the module

The materials used in the COMSOL model are selected according to the information provided in the datasheet and the data provided from the reference module. According to the manufacturer, the baseplate has copper (Cu) as material. Further, the Ceramic material used in DBC substrate is Silicon Nitride (Si_3N_4). The chips material is Silicon Carbide (SiC). On top of the baseplate, there is a layer of solder, which holds the DBC layer. The upper layer of the DBC having again a solder that holds the Silicon chip. There is no information available about the solder layer materials in the datasheet. Hence, in this project, the result of EDS-analysis from section 3.2 has been used. The solder layer material approximates as $Sn_{90}Ag_{10}$. Material properties for the module layers, which are essential for the thermal analysis are presented in table 3.7.

Table 3.7: Properties of the materials of the power module

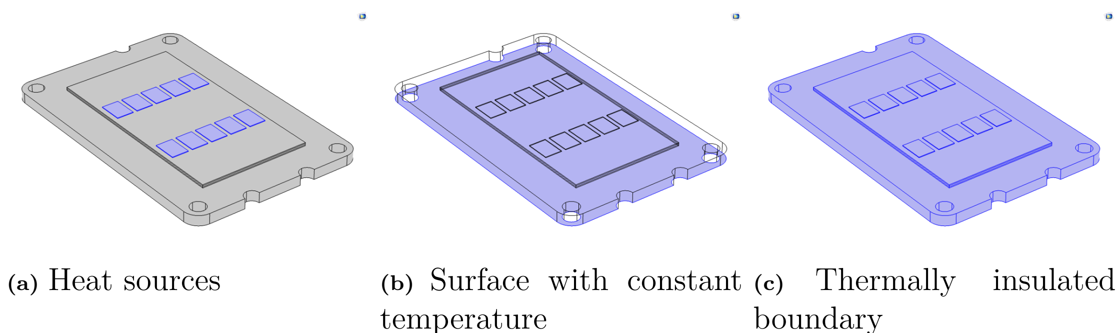
Layer	Material	Thermal conductivity, K (W/(mK))	Density, $\rho(kg/m^3)$	Heat capacity, C (J/(kgK))
Die	SiC	490	3216	690
Solder layer	$Sn_{90}Ag_{10}$	50	9000	150
DBC ceramic	Si_3N_4	20	3100	700
Copper/ Baseplate	Cu	400	8940	385

3.4.3 Boundary conditions of the module

To achieve a good estimation of the heat transport, boundary conditions needed to be applied. The boundary conditions are implemented by considering all chips as heat sources, to simulate heat injection to other layers. In section 3.3, the power loss in one switch is calculated to 570.86 W. Since there are five parallel connected chips in one switch, the power loss for each chip is calculated to 114 W. This value is used for the simulations.

The bottom surface of the baseplate is set to have a convective heat flux as a boundary condition. To mimic the heatsink, an "external forced convection" with "plate, averaged transfer coefficient" is selected. For the cooling method, a liquid flow of water with a velocity of one meter per second and a temperature of 65 °C has been applied. All other boundaries are set to have a convective heat flux with a heat transfer coefficient of 10 W/(m^2K), which is the convection of low-speed flow of air over a surface [15].

The two-solder layers, Die solder layer, and the DBC solder layer were applied in the model by the Thermal Contact feature in COMSOL through their equivalent thermal resistance. The physical representation of these thin layers in the module would create a mesh trouble since this layer is thin, an accurate mesh on these layers is difficult to achieve. Figure 3.6 shows the boundary condition for the selection of heat sources 3.6a, bottom surface of the baseplate 3.6b and, thermally insulated boundaries 3.6c.



(a) Heat sources (b) Surface with constant temperature (c) Thermally insulated boundary

Figure 3.6: Boundary conditions of the power module

3.4.4 Mesh of the module

Since the different layers in the module are very thin, and accurate mesh needs to be achieved, for this simulation, a user-controlled mesh has been used to customize meshing in the areas which are of interest. As the focus of this simulation is on thermal distribution through chips and the DBC layer, a manually refined mesh is applied in these areas, which means that the different layers have been applied with different mesh settings. A free tetrahedral mesh has been applied to the geometry. However, the mesh has been customized and refined with an extra-fine free tetrahedral mesh in the chips and DBC areas to minimize the error in the numerical

solution and obtain a reasonable heat flux distribution. The result of the meshing is shown in the figure 3.7.

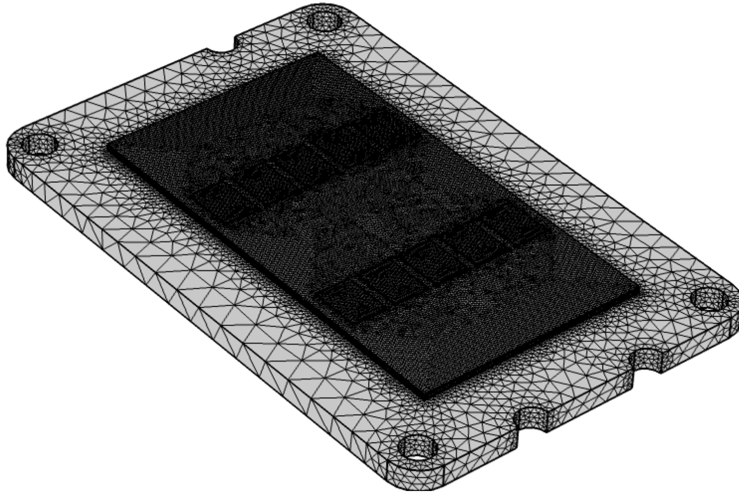


Figure 3.7: Mesh visualization of the power module

3.4.5 Physics settings and Study selection

To evaluate the temperature distribution through the power module and simulate heat transfer conduction, the physics module "Heat Transfer in Solids" was utilized with a stationary study. Although for the transient analysis of the maximum junction temperature (T_j) of the MOSFET, a time-dependent study is selected. Furthermore, the problem is simulated for a time interval of 0-1 second, and a reference temperature of 65 °C is selected.

3.4.6 Base simulations

The base simulations include plotting and analyzing time variations of the temperature inside the different layers of the power module, temperature profiles across it and within boundary layers of the power module. Calculating the thermal resistance of the power module. Comparing and verifying the result with the given thermal resistance in the datasheet.

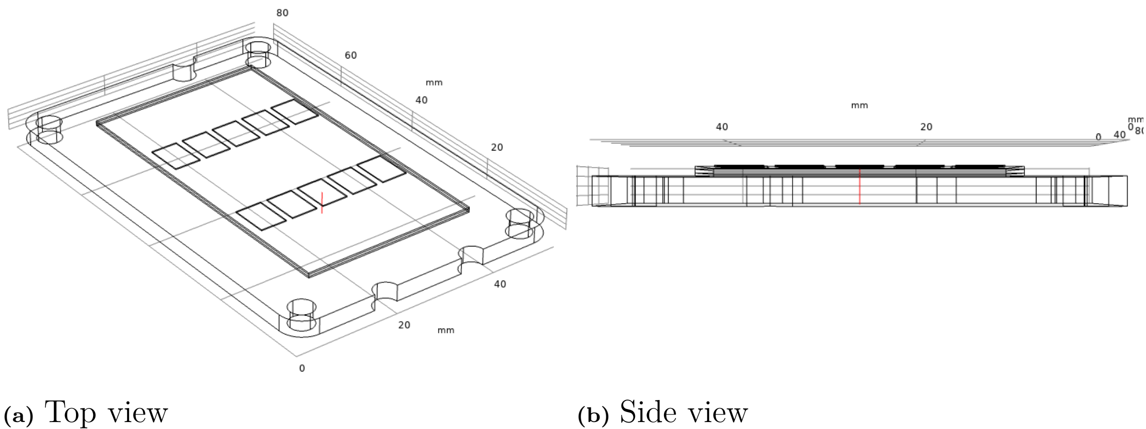
3.4.6.1 Simulation of untuned model

Since there are unknown variables such as which material that has been used and its thickness, the untuned model was built on typical values found in multiple sources. To simplify the model even further, the solder layers were excluded from the simulation because both solder layers are very thin, and it would create mesh trouble in the simulation. Therefore, only the chip, DBC layers, and the baseplate are included in this simulation. The materials that have been used and their respective thickness can be seen in table 3.9.

Table 3.9: The table shows materials and thickness of the layers that were implemented in the untuned model[16].

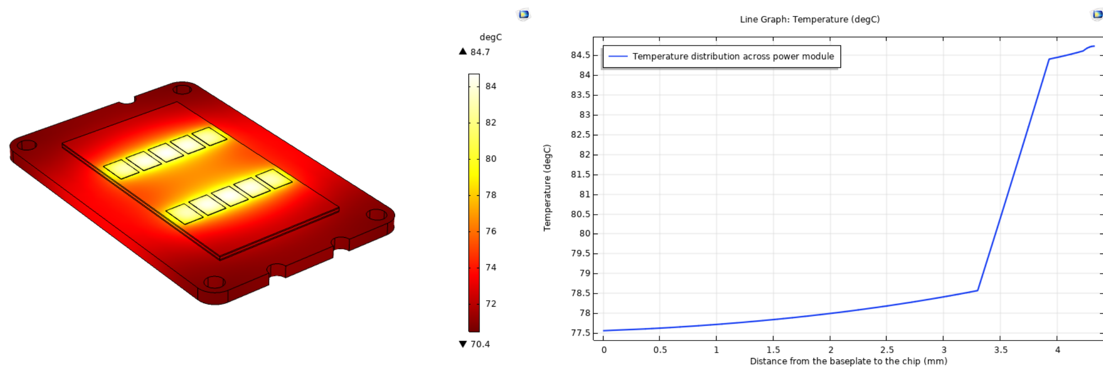
Layer	**Material**	**Thickness**
Chip	SiC	100 um
DBC	Cu	0.3 mm
DBC	AL_2O_3	0.63 mm
Baseplate	Cu	3 mm

By running the simulation, the obtained results can be seen in figure 3.9, where the temperature distribution across the module and its layers are plotted. The distribution is measured as a cut-line from the middle chip to the baseplate, figure 3.8 shows the 3D cut-line. The reason for choosing the middle chip is because it is where the most heat will be concentrated. It can be seen that the maximum temperature is close to 85°C and the lowest temperature is 70°C. Thus, the thermal resistance that was obtained from the simulation is equal to 0.078 K/W, which is 0.032 K/W lower than the real model (0.11 K/W).



(a) Top view (b) Side view

Figure 3.8: Figure shows the cut-line goes through module for temperature measurements.



(a) Temperature distribution across the power module

(b) Temperature distribution across all the layers

Figure 3.9: The figures demonstrates the temperature distribution across the power module for the untuned model.

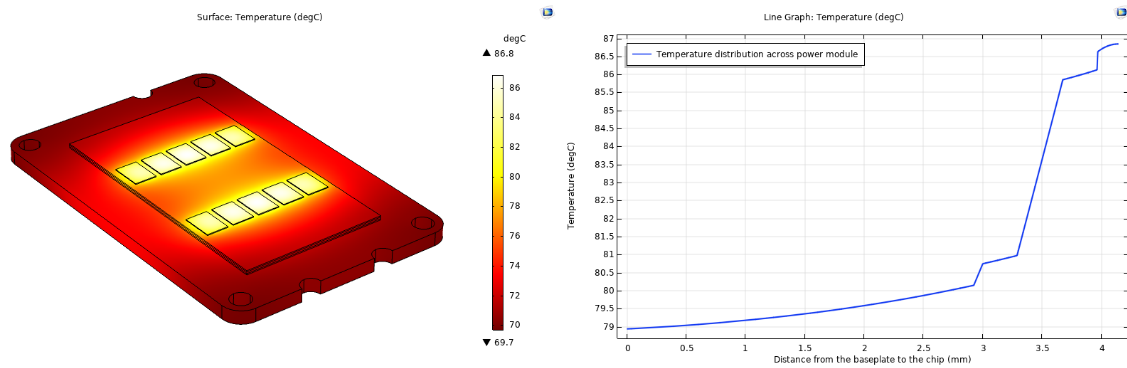
3.4.6.2 Simulation of tuned model

The tuned model is an attempt to make the COMSOL model as close as possible to the real model (CAB450M12XM3). With help from the reference module, explained in section 3.2, the thickness value of each layer could be adjusted in COMSOL. In this tuned model, two solder layers were added, one below each chip and the second between the DBC layers and baseplate. The DBC insulating material was changed to Si_3N_4. All the adjusted values can be seen in table 3.10.

Table 3.10: The table shows materials and thickness of the layers that were implemented in the tuned model.

Layer	**Material**	**Thickness**
Chip	SiC	178 um
DBC	Cu	0.3 mm
DBC	Si_3N_4	386 um
Solder (below the chip)	$\mathrm{Sn}_{90}Ag_{10}$	79 um
Solder (below the DBC layers)	$\mathrm{Sn}_{90}Ag_{10}$	129 um
Baseplate	Cu	3 mm

The obtained results from the tuned model simulation are shown in figure 3.10. It can be noticed that there is a slight increase in temperature, this model reaches a maximum temperature of 87°C. The lowest temperature which is found around the edges of module is approximately 70°C. The thermal resistance was calculated to be 0.0945 K/W which is an increase by 0.0158 compared to the untuned model, a 15% closer to the real model.



(a) Temperature distribution across the power module

(b) Temperature distribution across all the layers

Figure 3.10: The figures demonstrates the temperature distribution across the power module for the tuned model.

The difference between the tuned and untuned models can be noticed more clearly in figure 3.11. The adjusted thickness and the added solder layers have increased the temperature by a couple of degrees. There is a 2.5°C difference in baseplate temperature and approximately 2°C difference in chip temperature.

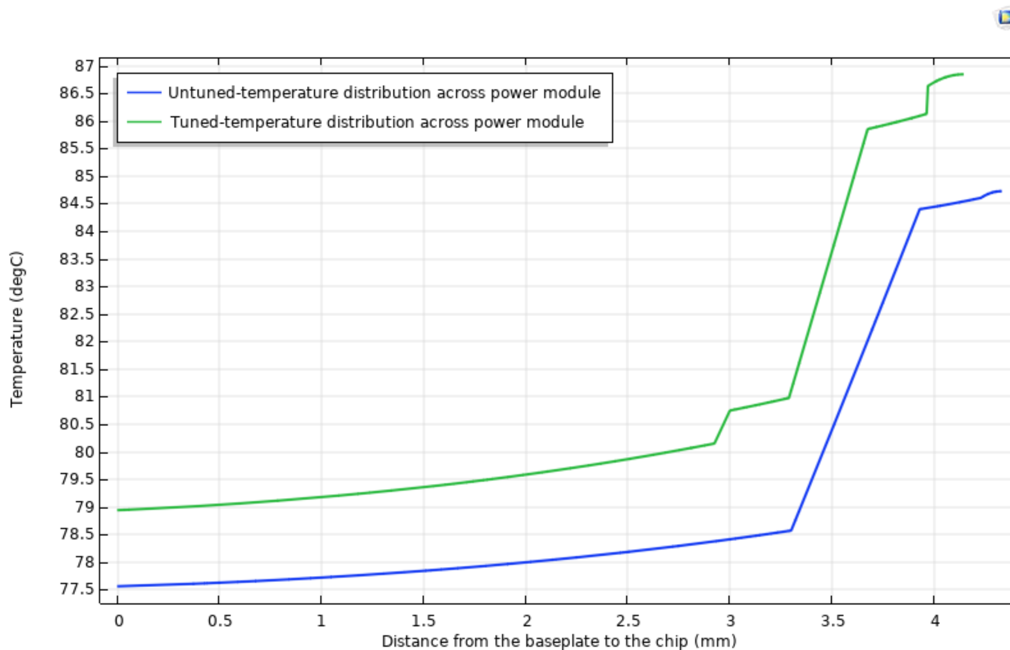


Figure 3.11: Comparison of temperature distribution between the tuned and untuned models

Even though the thermal resistance obtained from the tuned model is lower than the value from the datasheet there is a conflicting effect that needs to be considered. In power modules the mutual chip heating (thermal coupling) and heat spreading will have an impact on thermal resistance. The thermal resistance value will be

lower than the actual measured value shown in the datasheet. Since there are multiple uncertainties with heat spreading, thermal coupling, and the impurities at the surface of the layers, which all have not been considered in the model, it is of no surprise that the thermal resistance is lower than the value in the datasheet.

3.5 Cauer Thermal Model

An equivalent Cauer Thermal Model using Simulink/Simscape was built in order to investigate heat transfer through an individual layer of the power module. The thermal model was also used for simulating thermal effects and estimate cooling requirements for the power module (CAB450M12XM3).

3.5.1 Cauer model parameter calculations

The Cauer model parameters R_{th} and C_{th} were calculated using (2.15) and (2.17). For the first simulation, both the heat spreading effect and the thermal coupling were not taken into account. The material characteristics for each layer are obtained from the table 3.7. R_{th}, C_{th} and τ were calculated for each layer and later added together for the total value. The results can be seen in table 3.11.

Table 3.11: Material characteristics that are included in the investigated power module.

Layer	**Thickness**	**Area** $[m^2]$	R_{th}	C_{th}	τ
Die	178.66e-6	3.5e-05	0.00851	0.06938	0.000590
Solder layer 1	79.11e-6	3.5e-05	0.04521	0.00374	0.000169
Copper layer 1	288.98e-6	0.002	0.00036	1.96939	0.000719
DBC Ceramic Substrate	385.84e-6	0.002	0.00974	1.65780	0.016153
Copper layer 2	288.98e-6	0.002	0.00036	1.96939	0.000719
Solder layer 2	129.15e-6	0.002	0.00130	0.34522	0.000450
Copper layer 3 (baseplate)	3e-3	0.0042	0.00177	43.78097	0.077443
Total value			0.07	49.80	

3.6 Thermal analysis of junction temperature with COMSOL test model and Cauer model

In this section a thermal analysis of the junction temperature is discussed, while taking into account the heat-spreading angle and the thermal coupling. To prove that the thermal coupling and the heat spreading effect have a large impact on the thermal resistance of the module and overall results, a small test model was simulated in COMSOL and Cauer model in Simscape. The two models were compared

with each other after each investigation.

3.6.1 Comsol test model and Cauer model

Considering the transient temperature response in COMSOL will be computationally heavy, a smaller test model will be used for the transient thermal analysis. The results from the test model are compared with the results obtained from the Cauer model.

To prove that the thermal coupling and the heat spreading effect have a large impact on the thermal resistance of the module, a small test model was simulated in COMSOL. The test model had the same number of layers and thickness, as well as the material used. The difference from the previous models is the area and volume, see figure 3.12.

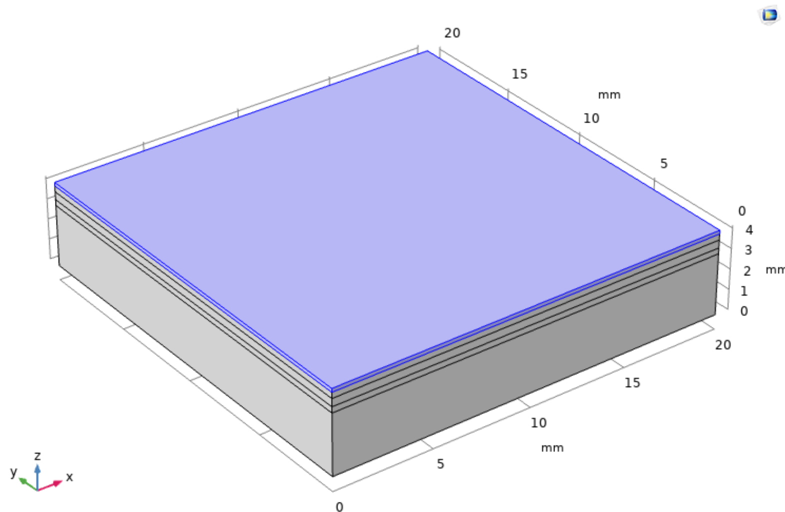
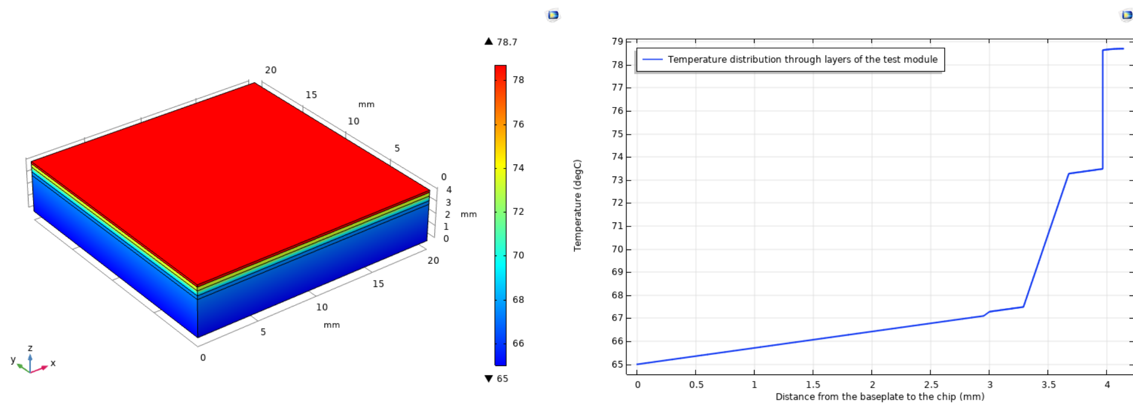


Figure 3.12: Test model geometry

The model was simulated with a time-dependent study to see the thermal transient response. The results were quite different compared to the previous models, see figure 3.13. In this case, the test model reached a higher temperature, just below 79°C, and the thermal resistance was calculated to 0.1106 K/W.



(a) Temperature distribution across the test model

(b) Temperature distribution across all the layers

Figure 3.13: The figures demonstrates the temperature distribution across the test model

To have a glance at the transient temperature of the power module, a Cauer model was built in Simscape with the help of element blocks. The element blocks symbolize heat transfer through a single layer of the power module. Layers such as the chip, solder, DBC, and the baseplate. Figure 3.14 shows the equivalent circuit of the Cauer model created in Simscape. The model does not consider the thermal coupling and heat spreading effects. This is a ladder network where element blocks are connected in series and each connection represents a single layer. The temperature behavior of the model is from the junction temperature (T_j) and the baseplate temperature (T_c). To run the simulation test, the thermal resistance and the time constant values for each layer are needed as inputs. The values that have been used for this simulation can be seen in the table 3.12. Lastly, the power loss value of 114 W was used as an input for this simulation.

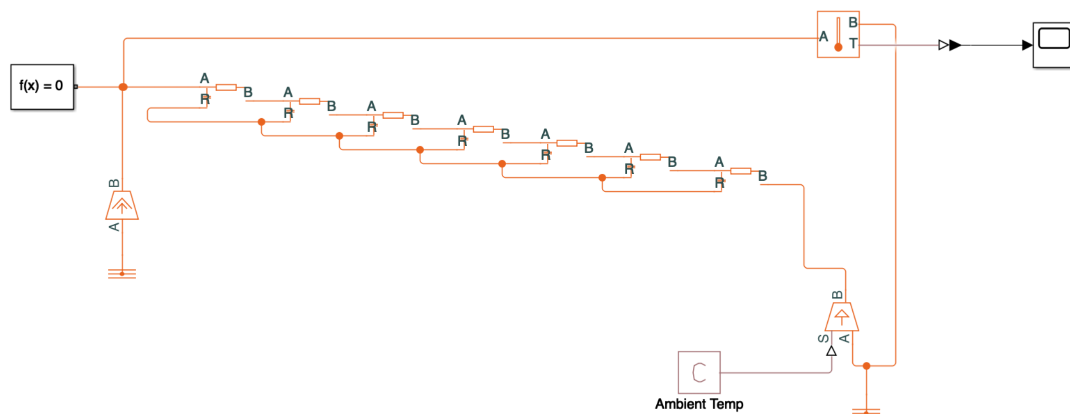


Figure 3.14: Simulation buildup in Simscape

Table 3.12: Material characteristics that are included in the investigated test model (without heat-spreading angle).

Layer	Thickness	Area $[m^2]$	R	C	\tau
Die	178.66e-6	4e-4	0.00372	0.15858	0.000590
Solder layer 1	79.11e-6	4e-4	0.00396	0.04272	0.000169
Copper layer 1	288.98e-6	4e-4	0.00181	0.39786	0.000719
DBC Ceramic Substrate	385.84e-6	4e-4	0.04823	0.33491	0.016153
Copper layer 2	288.98e-6	4e-4	0.00181	0.39786	0.000719
Solder layer 2	129.15e-6	4e-4	0.00646	0.06974	0.000450
Copper layer 3 (baseplate)	3e-3	4e-4	0.01875	4.13028	0.077443
Total value			0.08	5.53	

The result of both simulations are shown in figure 3.15, which shows the transient junction temperature of the model. It can be seen that the temperature rises fairly quickly and later stabilizes just below 73°C. Since no heat-spreading and thermal coupling is occurring in both models the results from both simulations were identical. The highest acceptable junction temperature is the boundary that makes sure the module is working within the safe area and exceeding this value will cause a failure in the module. Therefore, having an estimation of the maximum junction temperature during operation to understand operating conditions, especially during the design phase of the module.

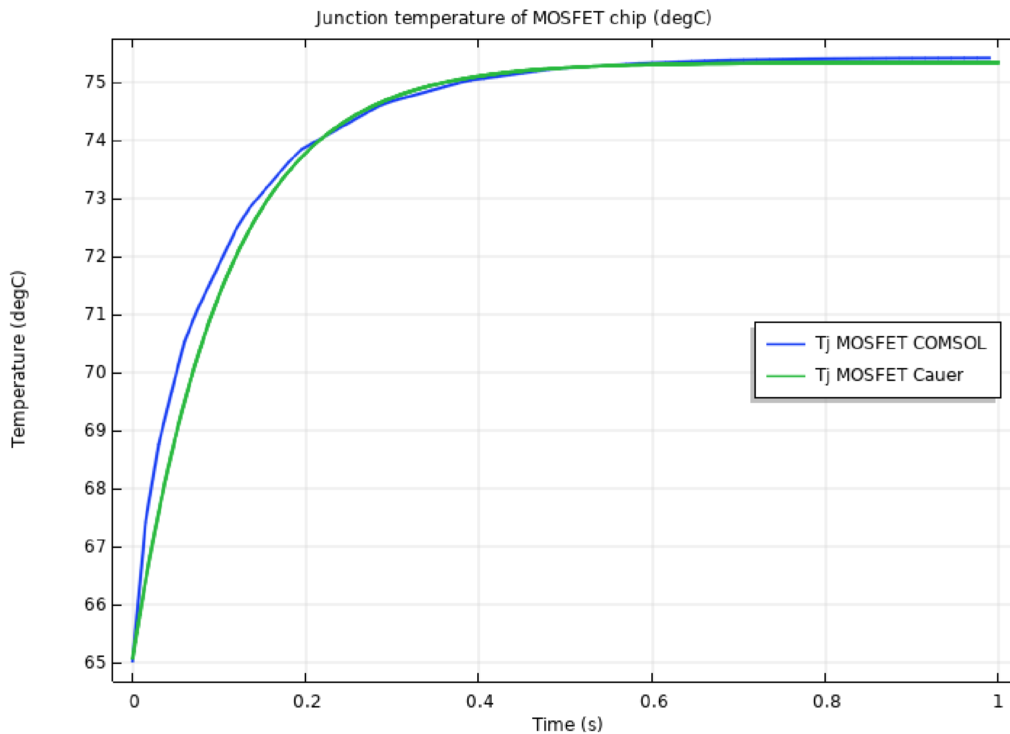


Figure 3.15: Transient junction temperature of MOSFET.

3.6.2 Taking heatspreading into account

The model above does not consider the heat spreading effect. Therefore, the model is not accurate and needs corrections to make the the results more reasonable. To consider and demonstrate the heat spreading effect, a new test model was simulated with a time-dependent study to see the thermal behavior over time. To study the effect of heat spreading, the size chip and its solder layer was reduced but the thickness of all layers stayed the same. From the simulation results shown in figure 3.16, the heat fluxes can be seen with a spreading effect flowing from the chip to the DBC layers.

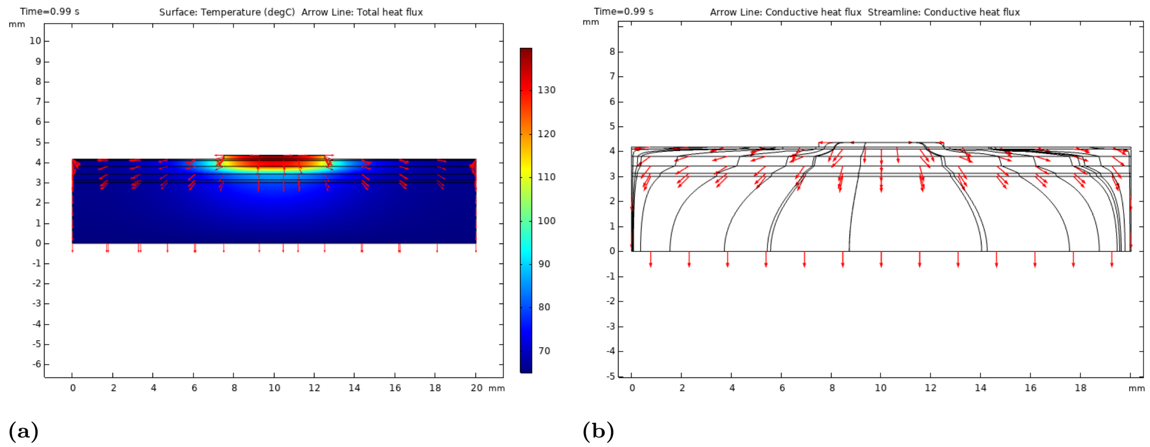


Figure 3.16: The figures demonstrates flow direction of the heat flux.

As it can be seen, the heat fluxes spread with a certain angle ϕ, which is called as the effective heat spreading angle. This angle determines the direction of heat flow and the effective area. Therefore, a heat spreading angle need to be considered in the Cauer model to calculate the temperature response. Applying the heat spreading angle using (2.18) presented in section 2.4, the effective area in each layer has been modified as it can be seen in table 3.13. The effective area has in turn affected the R_{th} and C_{th} as well as τ_{th} values in the Cauer model. The heat spreading angle (θ) was estimated to be 40°for all layers except the solder layers. Since the solder layers are not considered heat spreading layers, θ is 0°.

Table 3.13: Updated Cauer parameter with heatspreading angle

Layer	**Thickness**	**Area** $[m^2]$	R_{th}	C_{th}	τ_{th}
Die	178.66e-6	4.1211e-04	0.00362	0.1637	0.000593
Solder layer 1	79.11e-6	4.0000e-04	0.00396	0.0427	0.000169
Copper layer 1	288.98e-6	4.1963e-04	0.00172	0.4346	0.000748
DBC Ceramic Substrate	385.84e-6	4.2633e-04	0.04527	0.3571	0.016153
Copper layer 2	288.98e-6	4.1963e-04	0.00172	0.4346	0.000748
Solder layer 2	129.15e-6	4.0000e-04	0.00646	0.0697	0.000450
Copper layer 3 (baseplate)	3e-3	6.2671e-04	0.01197	6.7384	0.080640
Total value			0.07	8.2410	

The result of simulation with and without considering heatspreading compare to the COMSOL simulation is shown in figure 3.17. As it can be see, the modified Cauer model is very close to the COMSOL model.

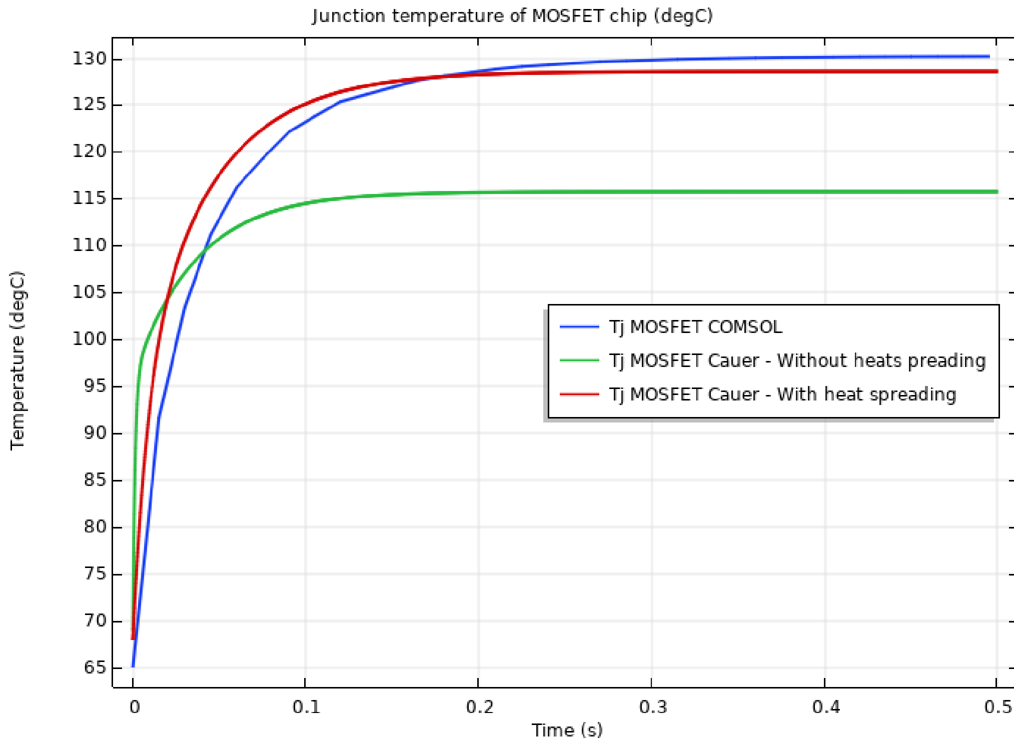
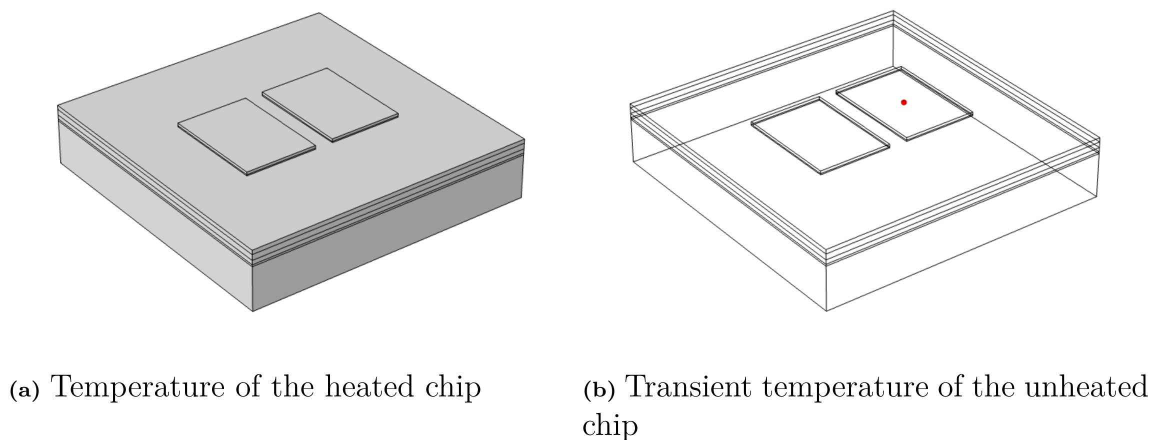


Figure 3.17: Comparison simulation result in case with considering heat spreading effect

3.6.3 Taking thermal coupling into account

The previous test models only consider the self-heating process of the module that is caused by the single operating chips. Though in the case of two or multiple chips are positioned close to each other, the thermal coupling effect occurring between the chips will heat the module to higher temperatures. The thermal coupling effect

is most noticeable if the gap distance between the chips is less than 3mm, and for power module CAB450M12XM3 the gap distance is 1.25mm. Similar to the previous cases, a test model was created to observe the thermal coupling effect. However, with this test model, two chips were included and only one of them is acting as the heat source. While one chip is heated up, the temperature of the chip next to it will be measured to determine the coupling effect, see figure 3.18 for the geometry and measuring point.

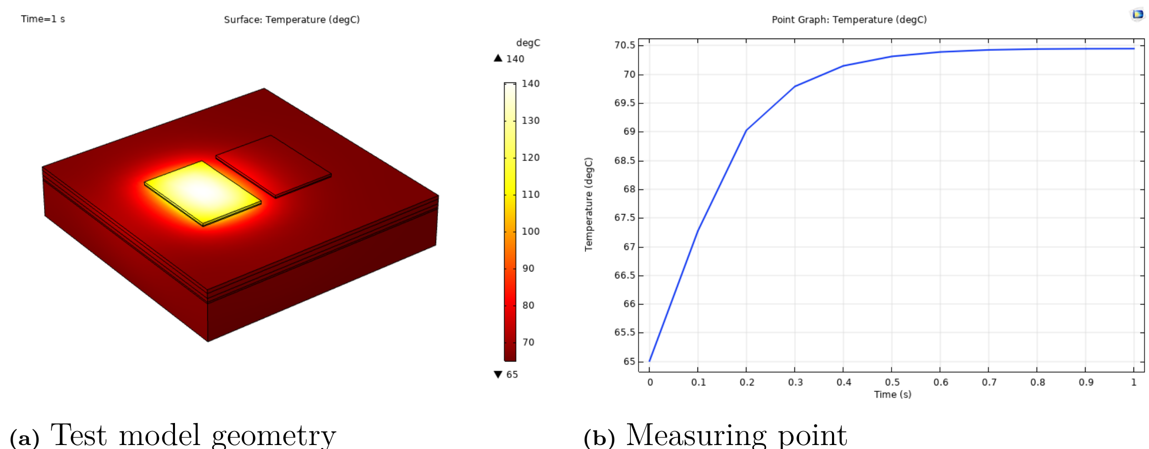


(a) Temperature of the heated chip

(b) Transient temperature of the unheated chip

Figure 3.18: The figures the test model created for thermal coupling analysis.

The simulation results are shown in figure 3.19, the thermal coupling effect can be noticed. While the heat source chip is reaching a temperature of 140°C the chip beside it is reaching a steady-state temperature of approximately 70°C. From figure 3.19b, it can be seen that the temperature response of the chip has the characteristics of an exponential curve, this means that the curve can be represented with one Foster RC link.



(a) Test model geometry

(b) Measuring point

Figure 3.19: The figures the test model created for thermal coupling analysis.

For the second correction, the coupling thermal impedance between the chips can be obtained by using 2.14. Since the curve in figure 3.19b can be represented with a one Foster RC link, the values of R and C can be calculated as well. Through the curve fitting tool in MATLAB, the values of R and C are obtained and added as a Foster link to the Simscape model, see figure 3.20. The simulation result with the added correction is shown in figure 3.21. The thermal coupling effects made an approximately 10% difference in the transient temperature response.

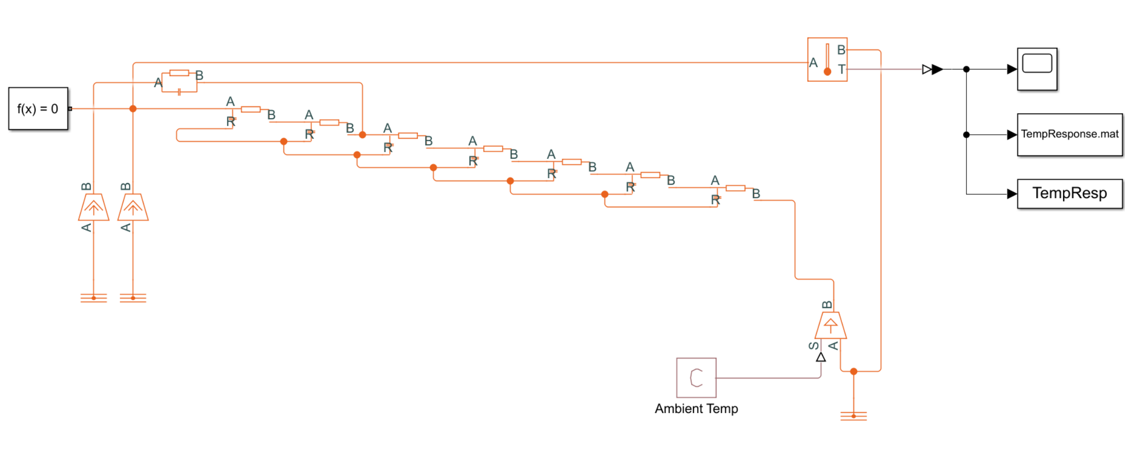


Figure 3.20: Simulation buildup in Simscape adding thermal coupling

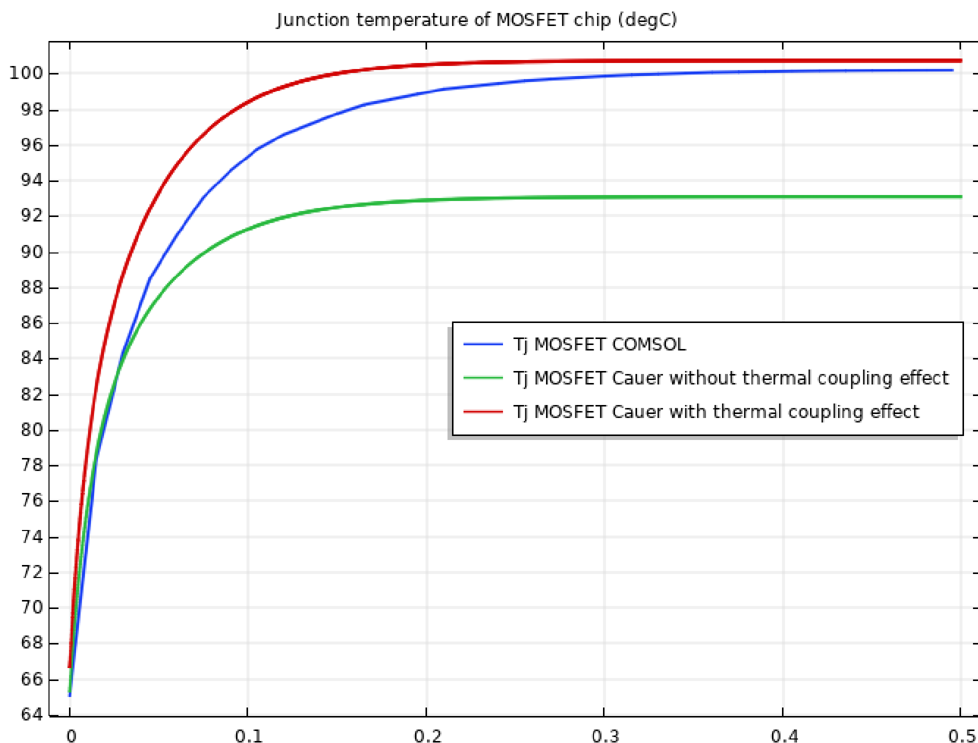


Figure 3.21: Simulation result of considering thermal coupling effect

3.7 Modified Cauer and COMSOL model

In this section, the COMSOL model and the Cauer model for the power module are simulated and compared with each other. Even though materials, their respective thickness, and the area are the same, results obtained from the Cauer and COMSOL models are different. Mostly due to the Cauer model not representing the thermal coupling and heat spreading effects accurate enough. As shown in figure 3.22, there is a 2-3°C difference between the COMSOL and Simscape simulations when both the thermal coupling and heat spreading effects are not considered.

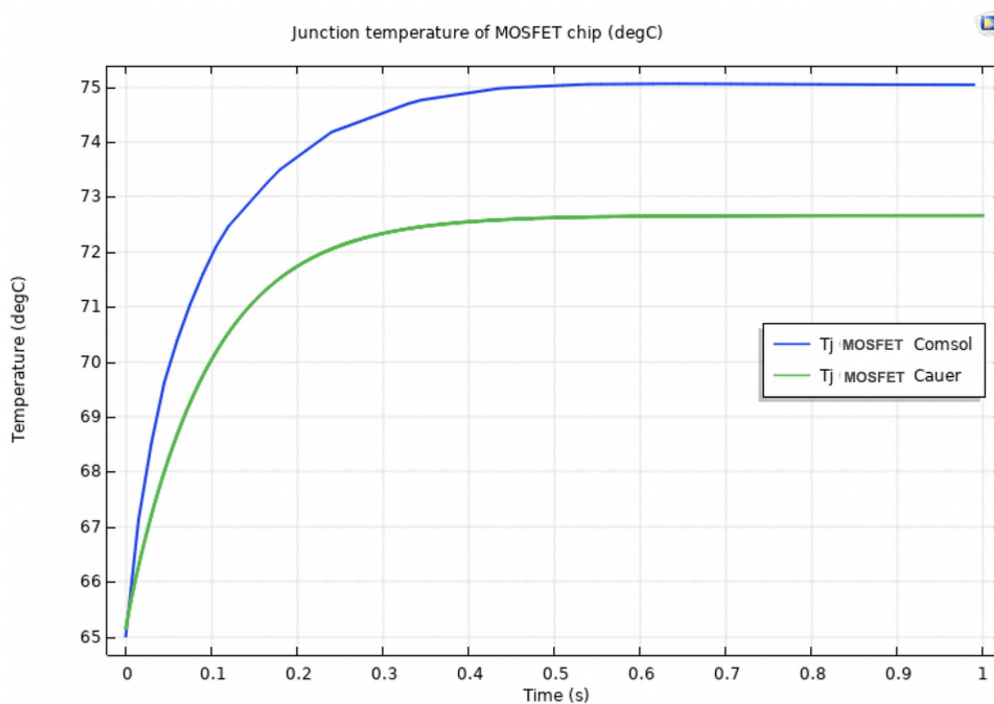


Figure 3.22: Junction temperature of MOSFET, COMSOL and Cauer mdoel without concidering heatspreading and thermal coupling effect

However, when the Simscape model is improved by adding the thermal coupling and heat spreading effects, the difference between the two is very small and can be considered acceptable, see figure 3.23. The small error is due to the estimation of the heat spreading angle of 40°not representing the conditions in COMSOL accurate enough.

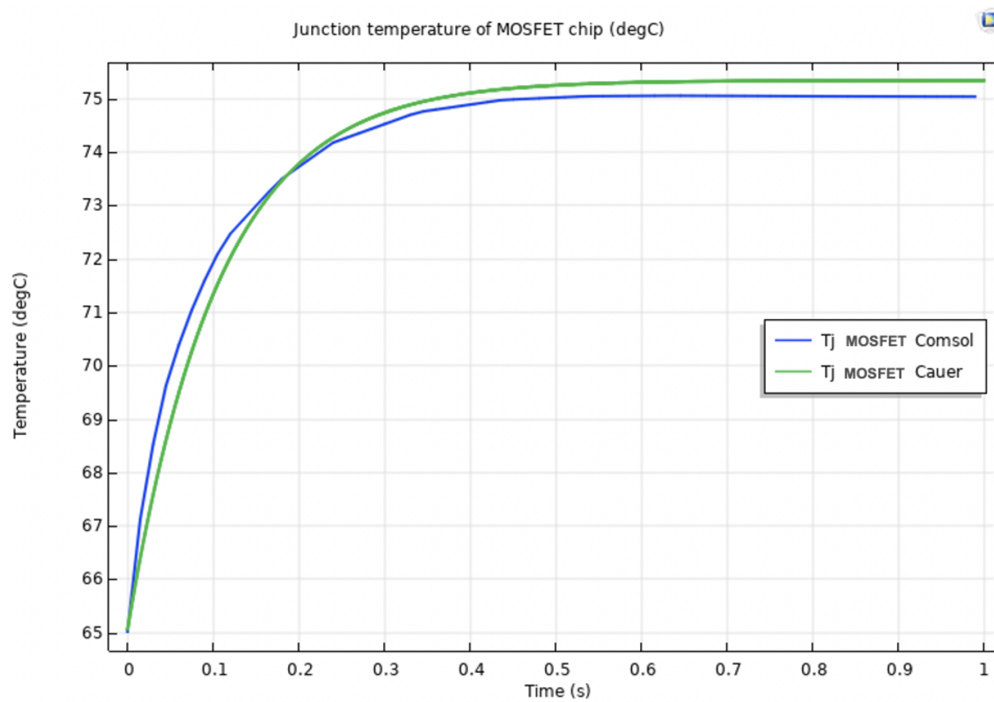


Figure 3.23: Junction temperature of MOSFET, COMSOL and Cauer model added heat+spreading and thermal coupling effect

4

Investigation of cold plate

This chapter will go though the selection and implementation of a cold plate model for the module CAB450M12XM3. Moreover, the optimization of fins shape and dimension will be discussed in this chapter as well.

4.1 Selection of heatsink model

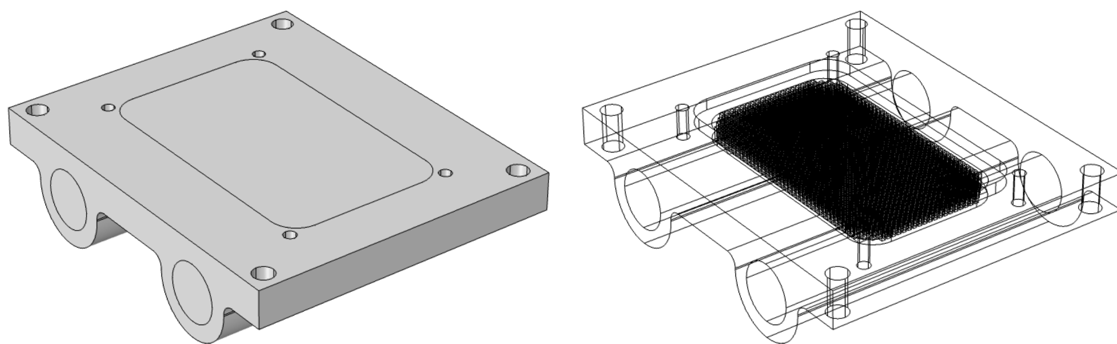
The selected cold plate model to cool down the power module CAB450MX12 is of the type PFCP. This model was chosen because it's the most enhanced option of the four models. Moreover, the model has fins which will make it possible to study the effect of Graphene when fins are replaced with the Graphene material. The design of the cold plate will be identical to Wieland Microcool's 3000 series cold plate model. The model's name is CP3012 and is made for the Wolfspeed XM3 module. The CP3012 cold plate is made of aluminum and has an MDT (Micro deformation technology) inside that decreases the thermal resistance, lowers the pressure drop, and a balanced parallel flow of liquid, see figure 4.1.

Figure 4.1: CP3012 cold plate designed by Wieland Microcool [17]

The cold plate has an inlet and outlet where the liquid flows from one side to the other. The cold liquid will pass the middle side of the plate going through multiple fins attached beneath the cover plate. The power module is placed on top of the cover which is welded on the plate.

4.2 Geometry set-up of cold plate

The cold plate is designed for a three-phase inverter with three power modules. However, the focus in this thesis is on a single power module, and therefore the design was modified to fit a single module only. The geometry is built according to the dimension given in the CP3012 datasheet[17]. More detailed information about the dimension can be found in appendix A. The result of geometry is shown in figure 4.2.



(a) Geometry of cold plate (b) Geometry inside view

Figure 4.2: Geometry of Cold plate for one Power module

The pin fin plate has an in-line pin fin with a gap distance of 0.5 mm. The fins are cubic with a side length of 1 mm and 4 mm length. The pin fin plate is shown in figure 4.3. This set-up, according to the manufacturer, has the best performance.

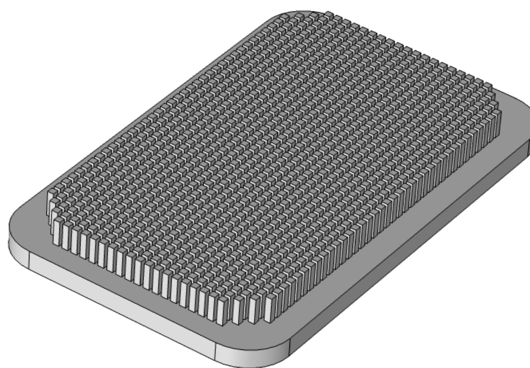


Figure 4.3: Pin fin plate with inline pin fins

4.3 Materials of the cold plate

The material used for the cold plate is aluminium. This material is also used in the COMSOL model to verify the cold plate parameters. For this simulation, the fluid type is selected to be 50/50 water and ethylene glycol, same as the coolant used for testing power module in datasheet. The fluid parameters such as heat capacity, density and thermal conductivity are temperature dependent.

TIM is usually used between the power module and the cold plate in order to enhance the thermal coupling between them. This thermal paste layer has a thickness of $75\mu m$. Since the thermal paste layer is very thin an accurate mesh on the layer can not be achieved with some normal level of meshing. Therefore, it is represented by its equivalent thermal resistance in the COMSOL model. Properties of the materials can be found in table 4.1

Table 4.1: Properties of the materials of the cold plate

Material\Material properties	Thermal conductivity k (W/(mK))	Density ρ(kg/m^3)	Heat capacity c (J/(KgK))
Aluminium	237	2700	904
TIM	5	2250	N/A

4.4 Boundary Conditions of the cold plate

The boundary conditions are implemented by applying that the cold plate has a fluid flow rate of 10 litres/minute. The reason to choose a flow rate of 10 litres/minute was that it is an average flow rate for liquid-cooled cold plate and also it was a value that could be compared to the data sheet. The inlet temperature (fluid temperature) is set to have a reference temperature of 65°C, which were a condition of the system. For other boundaries, the same condition as the power module applied to the cold plate is used. Namely, to have a convective heat flux with a heat transfer coefficient of 10 W/(m^2K), excluding the top surface of the cold plate.

The simulation was done with a constant temperature, meaning the cold plate and the power module were not simulated together due to the COMSOL file being excessively large. Instead, when simulating the cold plate a representation of the power module was used by making a constant heat that comes from the baseplate of the module and through the cold plate. The heat is later distributed to the fins below the cover and lastly to the circulating liquid.

4.5 Mesh of the cold plate

A free tetrahedral mesh was applied to the entire geometry of the cold plate. However, the mesh has refined with finer mesh in the interest area such as in fins and liquid domain to see a better distribution of temperature. The quality of the mesh impacts the accuracy of the model and the result. The even finer mesh is more accurate than the currently applied mesh, but the computational power required increases as there are more elements in the mesh.

Because of the complexity of the geometry, the denser mesh would result in long computational time. Therefore it is satisfied with a finer mesh of the model. This means that the mesh resulted in lower quality is some regions. But those regions were not in the primary interest of study. The overall quality of the mesh was considered as a sufficiently good, and the model was verified by comparing it to measured data from the cold plate datasheet. The result of meshing is shown in figure 4.4.

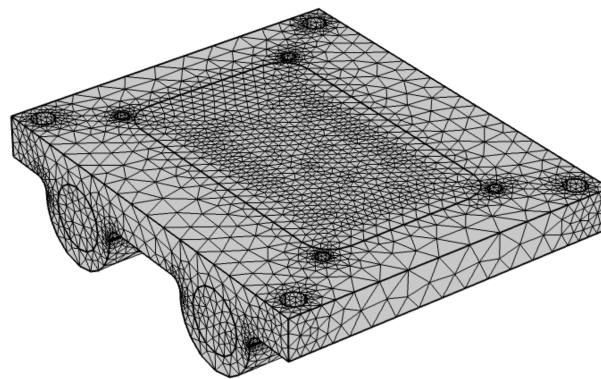


Figure 4.4: Mesh of the cold plate

4.6 Physics settings and Study selection

Different physical phenomena need a particular module in COMSOL Multiphysics. When two or more physics are involved in the problem, several models are needed in the analysis to get an estimate of the solution. Since this problem deals with both the heat transfer in the solid and fluid, the Conjugate Heat Transfer, the Laminar Flow multiphysics interface is used. The module simulates the coupling between heat transfer and fluid flow. The multiphysics module consists of two modules, namely the “Heat Transfer in Solid and Fluids” as well as “Laminar Flow.” These modules evaluate the temperature transport and the generated heat fluxes in the cold plate and in the fluid.

For the major part of the analysis, when the temperature field at thermal equilibrium is the focus, the stationary study has been used. However, a Time-Dependent

solver has been applied for the transient analysis part of the study when the problem is changing over time.

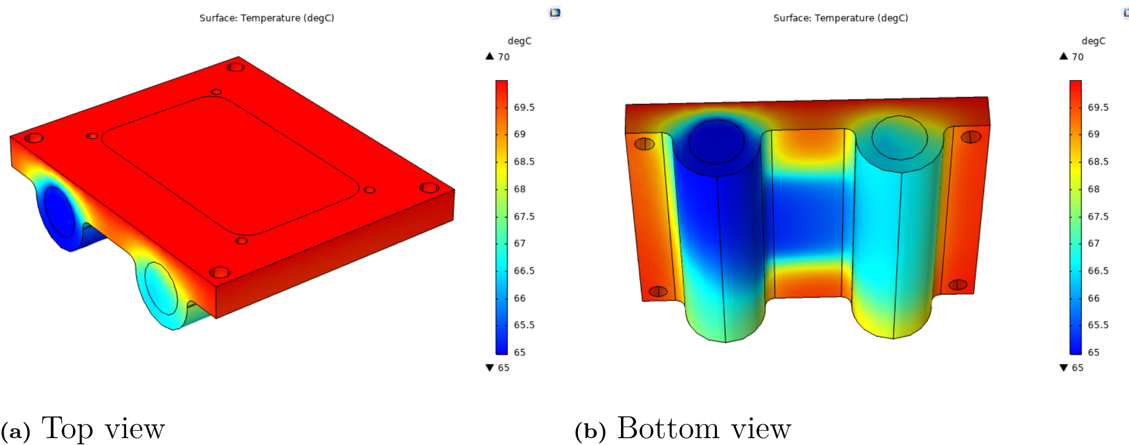
4.7 Simulation results

In this section, two methods of calculating the thermal resistance of the cold plate were investigated. The first one is without a cold plate and assumed a constant temperature at the surface of the cold plate. The second one is with the power module.

4.7.1 Simulation with a constant temperature

After the geometry of the cold plate was completed and the boundary conditions were set according to the previous section, the model could be simulated. The objective of this simulation was to determine the thermal resistance and compare it with the value found in the datasheet (0.0078 K/W) for a flow rate of 10 liter/min[17]. Since the thermal resistance changes with the flow rate of the fluid, it was decided to simulate the model with a flow rate of 10 liters/min for the reason to compare it with an exact value from the datasheet. The simulation was based on a constant heat placed on top of the cold plate with a temperature of 70°C. The constant temperature was acting as the heat coming from a power module.

The results from the first simulation can be seen in figure 4.5, the hottest points are located on top of the cold plate where the power module would normally be mounted. The coolest points seem to be located in the area between the inlet and the middle side of the cold plate where the fins are located. It is obvious that the outlet has a higher temperature than the inlet, this indicates that the fluid is absorbing the heat coming from the top and through the fins.



(a) Top view **(b)** Bottom view

Figure 4.5: The figures demonstrates the temperature distribution across the coldplate with a constant temperature of 70°C.

Moreover, the flow and velocity of the fluid are of importance as well because it is an indication of how easy it is for the fluid to flow from one side to the other. Figure 4.6 demonstrates the flow of the fluid from the inlet to the outlet of the cold plate and it can be noticed that there is a decrease in velocity. Since the fins act as resistance, the flow will slow down to some degree.

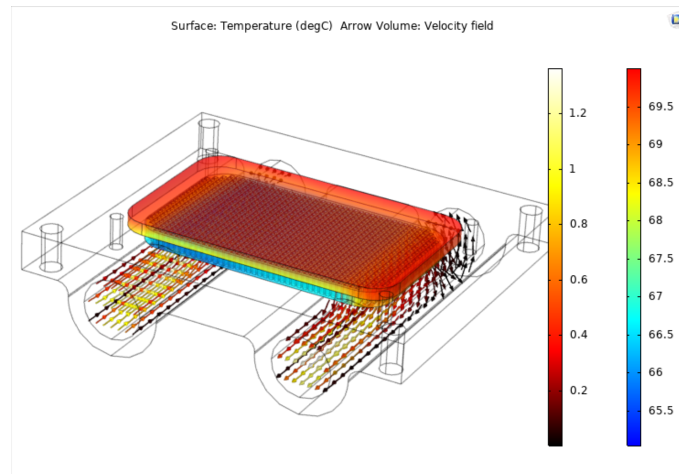
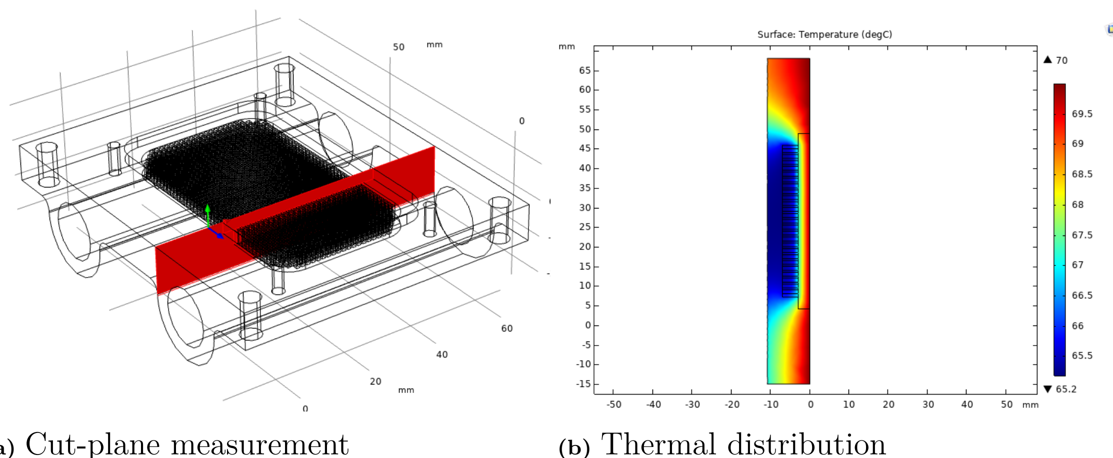


Figure 4.6: The figures demonstrates the fluid flow across the cold plates channels and the temperature distribution with a cut-plane view.

The thermal distribution for is this simulation is measured with a cut-plane that goes through the whole cold plate, from the top and down through the fins. The thermal distribution can bee seen in figure 4.7, where the fins and the cooled fluid seems to distribute the heat from the middle of the plate.



(a) Cut-plane measurement (b) Thermal distribution

Figure 4.7: Cut-plane measurement and it's thermal distribution results

The thermal resistance for this simulation was calculated to be 0.0066 K/W which is lower than the value shown in the datasheet for 10 liters/min flow, 0.0078 K/W. This may be due to quality of mesh and also the geometry of the cold plate that adjusted for single power module. However, the value calculated is still relatively

close to the actual value, and therefore the COMSOL model can be considered similar to the real model.

4.7.2 Simulation with the power module

This simulation of the cold plate had two targets, one to see if the model built in COMSOL had the same parameters as the datasheet in terms of thermal resistance. Second, which is the most important part of this simulation was to see if the working temperature of the module had decreased to acceptable levels. The results from figure 4.8, show that the cold plate has an impact on the temperature of the module and reducing it to approximately 74.4 °C.

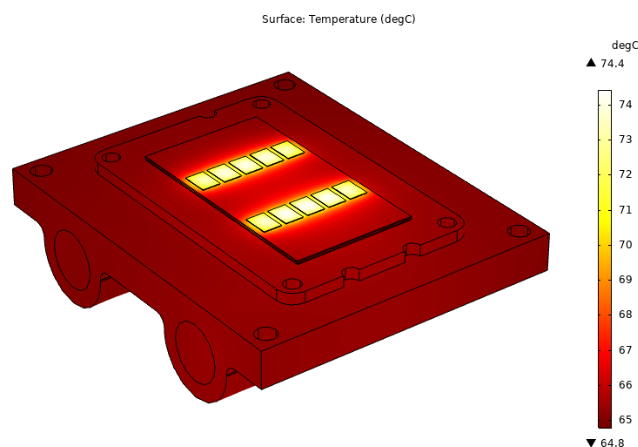
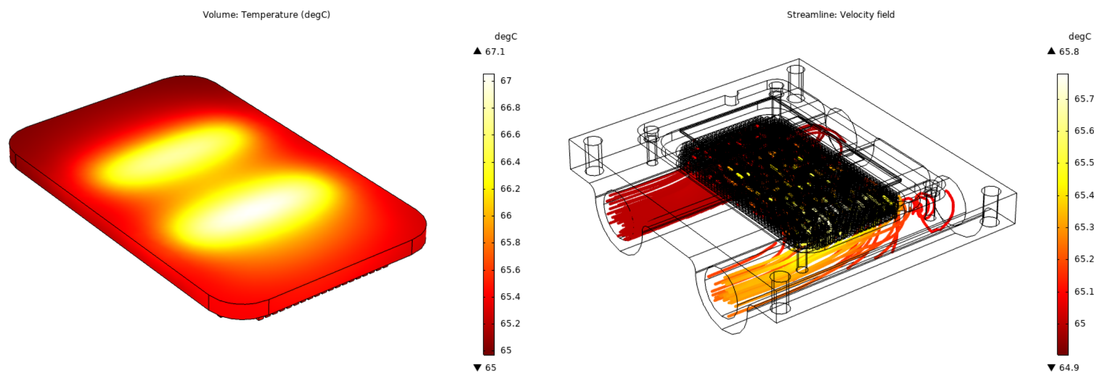


Figure 4.8: Temperature distribution across power module and cold plate

In terms of flow rate and velocity the results were the same as the previous simulation without the power module where there is a reduction in velocity when the fluid reaches the outlet, see figure 4.9. The temperature distribution on the Pin fin plate can be seen not evenly distributed. This is due to the difference between the outlet and inlet temperature, on the outlet side of the cold plate the temperature is higher.

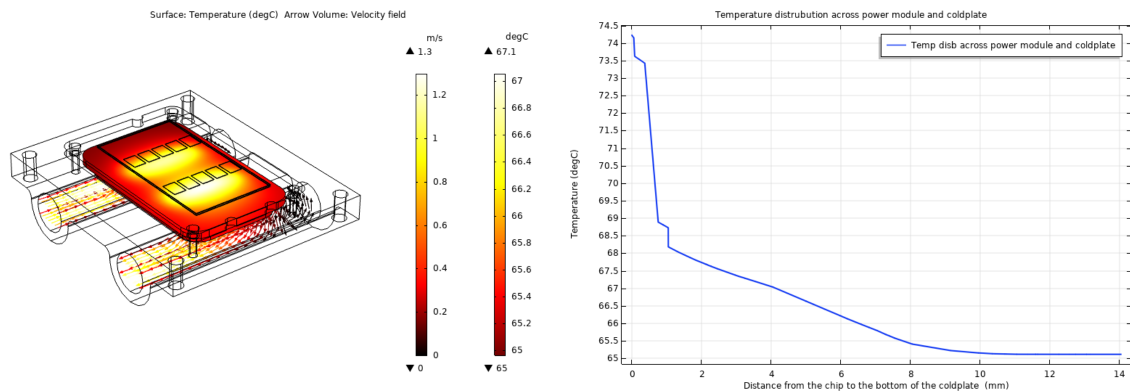


(a) Temperature distribution on Pin fin plates

(b) Velocity field and temperature distribution of liquid

Figure 4.9: The figures demonstrates the temperature distribution and fluid velocity across the coldplate and power module.

It can be noticed in figure 4.10 that the cold plate is spreading the heat effectively from the chips down to the fluid. However, the thermal resistance for this case was calculated to be 0.013 K/W which is higher than the datasheet value. Therefore, calculating the thermal resistance with a constant temperature seems to give a more accurate result for the cold plate.



(a) Liquid velocity

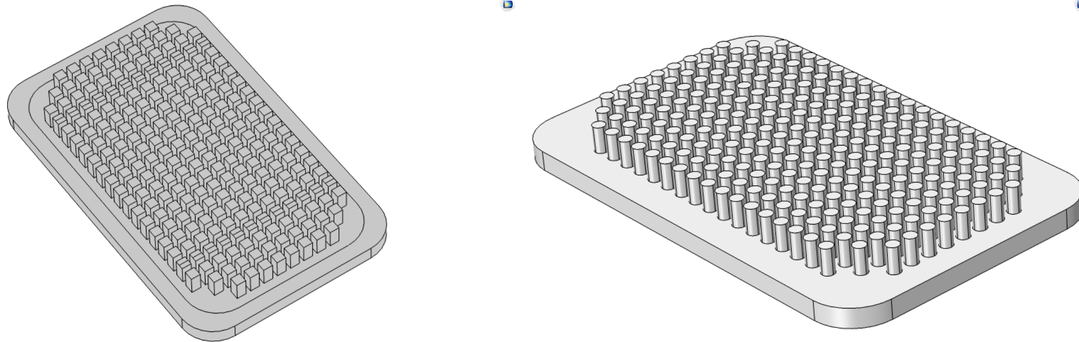
(b) Temperature distribution across power module and cold plate

Figure 4.10: The figures demonstrates the temperature distribution across the coldplate and power module.

4.7.3 Optimization of fins shape and dimension

To investigate the effects of fins shape and dimension on the flow and heat transfer characteristics, the cold plate with different fin shapes cubic and cylindrical are investigated, see the geometry of the fins in figure 4.11. The parametric monitoring is mainly focused on the cold plate thermal resistance, outlet fluid temperature, maximum cold plate surface temperature in fins area and inlet pressure. It should

be noted that, higher thermal cooling performance results in decreased thermal resistance of the cold plate as well as extends the lifetime of the power module.

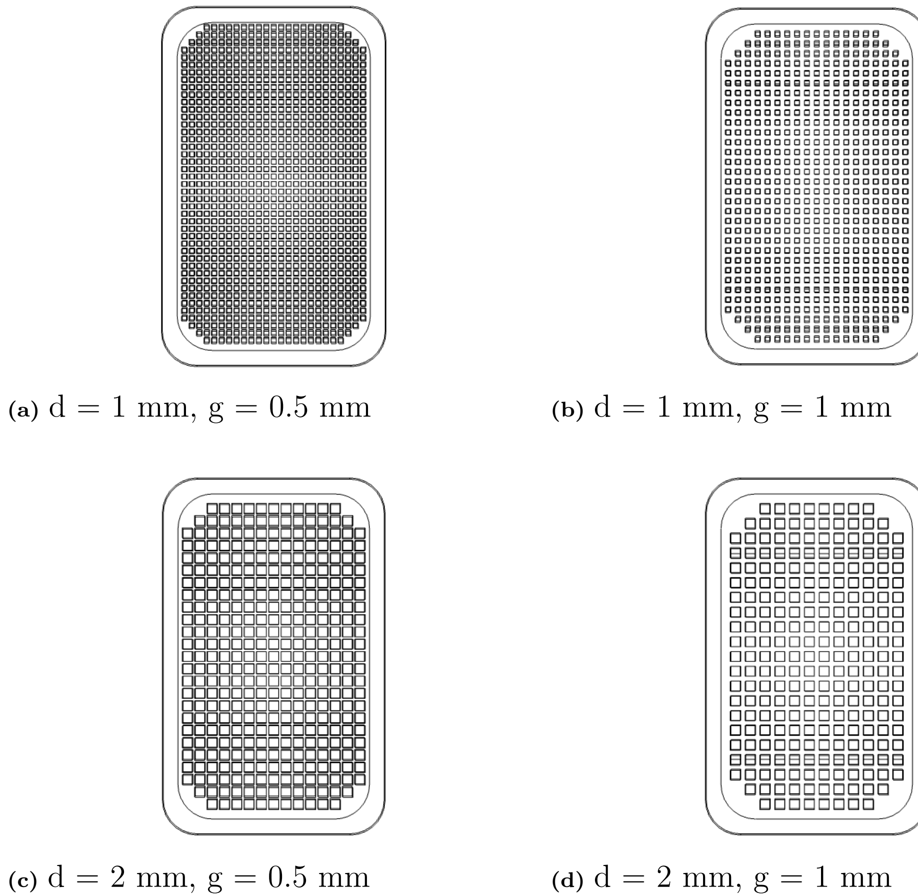


(a) Cubic structure

(b) Cylindrical structure

Figure 4.11: Pin fin plate with different fin configurations

In this study, four combinations of varying the fins diameter and gap distance have been considered. The cubic pin fin has a dimension of d mm × 4mm (W × L), where the d is diameter and varies between 1 mm and 2 mm. As well as, fin spacing, varies between 0.5 mm, 1 mm and 2 mm. Therefore the number of fins varies in each combination. Different fins configurations are shown in figure 4.12.



(a) d = 1 mm, g = 0.5 mm (b) d = 1 mm, g = 1 mm

(c) d = 2 mm, g = 0.5 mm (d) d = 2 mm, g = 1 mm

Figure 4.12: Different fins (d = diameter and g = gap distance) configurations

The boundary condition for this experiment is the same as for the verification part of the cold plate. Namely, a flow rate capacity of 10 liter/min is used for liquid to circulate the 50/50 water and ethylene glycol flowing through the cold plate and fins. The cold plate top surface has a constant temperature of 70 °C, and the all other boundaries of the cold plate is cooled with a heat flux coefficient of 10 W/(m^2K). The result of simulation and the investigated parameter are shown in table 4.3.

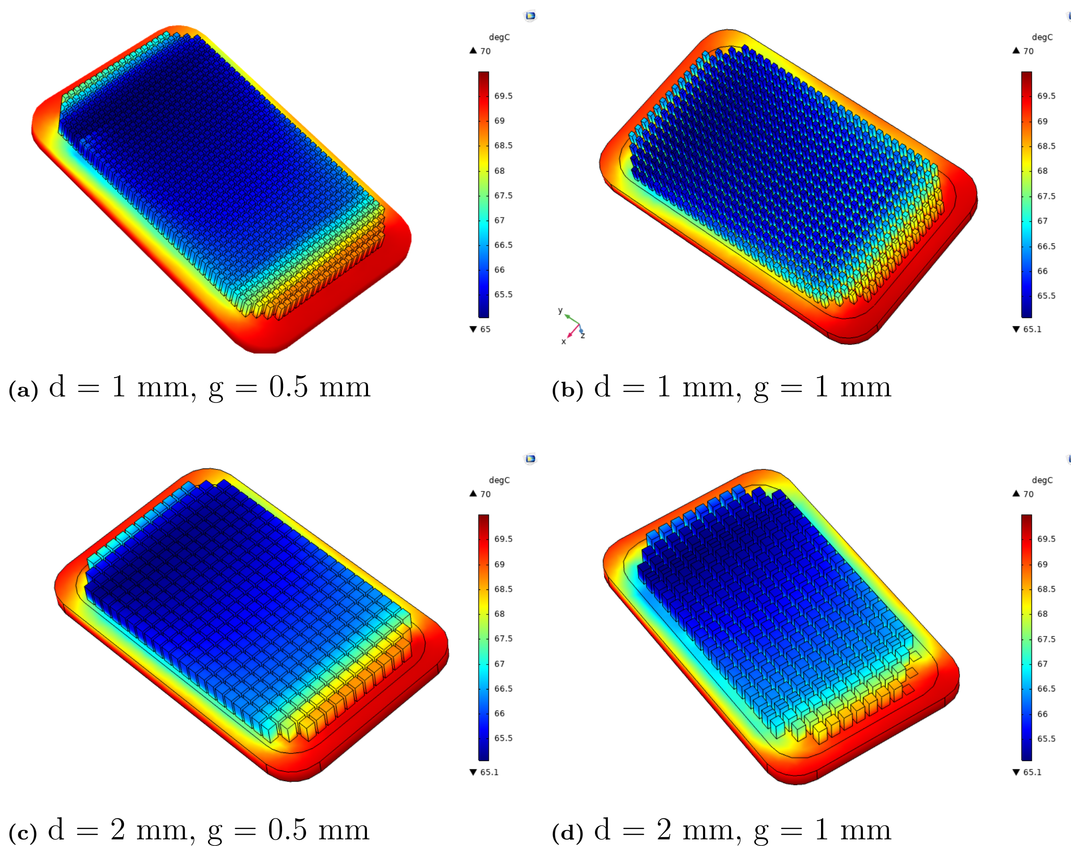
Table 4.3: Investigation of fins dimension, d is diameter and g is gap distance

Investigated parameter\ Fins diameter and gap	d = 1 mm g = 0.5 mm	d = 1 mm g = 1 mm	d = 2 mm g = 0.5 mm	d = 2 mm g = 1 mm
Cold plate Thermal Resistance [mK/W]	6.5198	6.9209	6.3885	5.9407
Outlet Fluid Temp [degC]	67.029	66.919	67.062	67.203
Max Coldplate Surface temp (in fin area) [degC]	69.619	69.527	69.514	69.360
Inlet Pressure Liquid (Pa)	31136	9184.4	34453	9341

From the table, it can be concluded that the bigger gap distance results in higher thermal resistance, lower outlet fluid temperature and maximum cold plate surface temperature in fins area. This is due to that the number of fins has been decreased and thus the contact surface area. Although this result in a lower pressure drop of liquid.

On the contrary, when the diameter of the fins has increased, the thermal resistance of the cold plate, as well as maximum cold plate surface temperature in fins area, has decreased. Also, the outlet fluid temperature increased, which means that the liquid absorbs more heat from the fins. This is due to that the contact surface area has increased, but this case would result in a higher pressure drop.

The results showed that the fin shapes of the heat sink influencing its total thermal resistance. The result can also be confirmed with the measured data from the cold plate data sheet, that the lower gap distance would have the best performance but higher pressure drop. The lowest thermal resistance achieves when the cubic fins have a diameter of 2 mm and a gap distance of 1 mm. This combination also have the lowest liquid pressure drop. The temperature distribution for each configuration is shown in figure 4.13



(a) d = 1 mm, g = 0.5 mm

(b) d = 1 mm, g = 1 mm

(c) d = 2 mm, g = 0.5 mm

(d) d = 2 mm, g = 1 mm

Figure 4.13: Temperature distributions in pin fin plate with different fin configurations (d = diameter and g = gap distance)

The same study has been carried out for the case with the cylindrical fins. The result showed that cylindrical fin has a higher thermal performance by lowering the thermal resistance of the cold plate compared to cubic fins. But the changes are small. It should be noted that the mesh of the fins geometry has a significant impact on the result. A denser mesh would result in a smooth surface of cylindrical fins, but it increased the computational time significantly.

4.8 Transient thermal analysis

In section 4.7.1 and 4.7.2, the cold plate thermal resistance was determined and verified by COMSOL simulation. To continue to build up the Cauer model for further transient analysis, the cold plate part must also be calculated and implemented in the model. Using the same procedure as it described in section 2.4, the value of the cold plate thermal resistance, as well as the thermal time constant, has determined to 0.0069 [K/W] and 18.7 [s] respectively.

4.8.1 Transient junction temperature

The transient junction temperature was plotted using both COMSOL and Simscape. The Cauer model in Simscape was updated with thermal components of the TIM, coldplate and liquid. The added components were inserted in the ladder network and simulated as in previous transient simulations. The results from the transient simulation are shown in figure 4.14. For the Cauer model, in this case, it was required two order of foster link to match the COMSOL model. As in previous simulations there is a small difference between the two models. It takes some more time for the cauer model to reach a steady-state compared to the COMSOL model. Moreover, the two models have slightly difference in steady-state temperature. The difference between the models can be explained due to the many uncertainties such as liquid parameters, surface contact area, heat transfer coefficient, and TIM material properties.

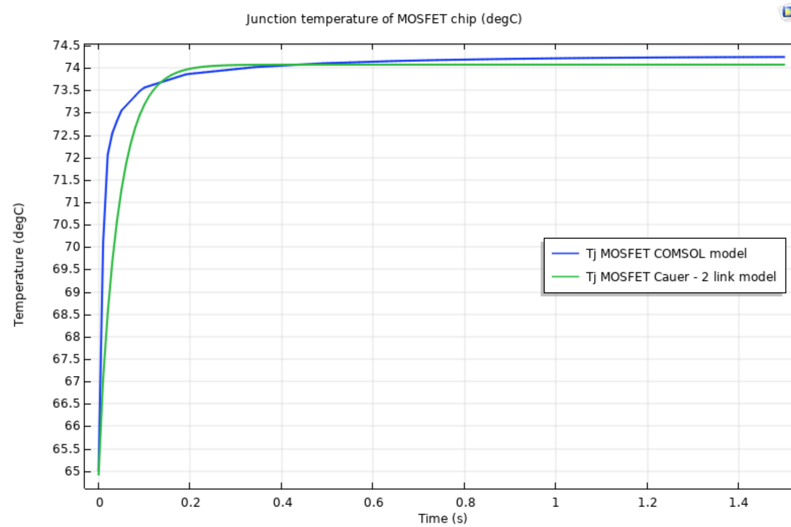
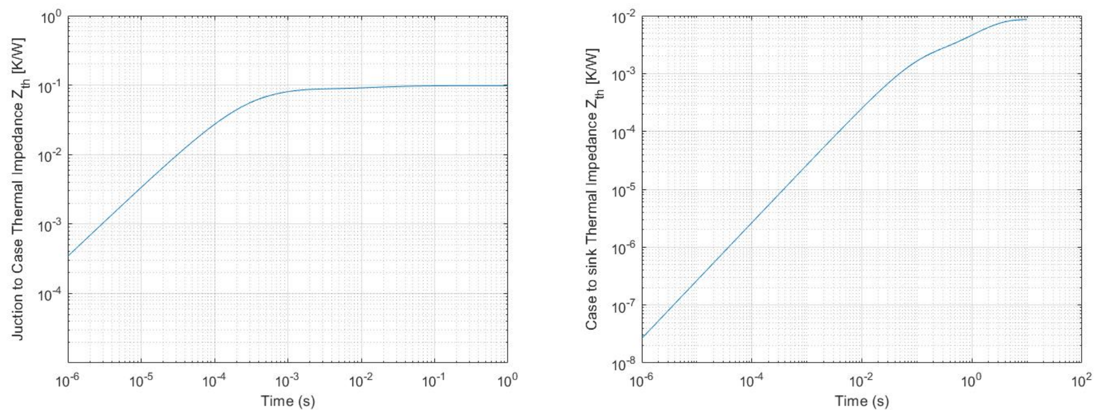


Figure 4.14: MOSFET junction temperature, cold plate with power module

4.8.2 Transient thermal impedance

As is discussed in section 2.4, the thermal behavior of the power module can be predicted using the Cauer thermal model. The Cauer parameters (thermal resistance, thermal capacity, and time constant) obtained by calculations based on geometric parameters and thermal properties of each layer as presented in section 3.5.1 and 3.11.

Thermal impedance is used to model the dynamic thermal behavior of the semiconductor element. By using the calculated Cauer parameters and the presented theoretical formula for thermal impedance in section 2.4.1, the transient thermal impedances $Z_{th_{j-c}}$ and $Z_{th_{c-s}}$ are plotted. The transient thermal impedance curve of the power module is shown in figure 4.15a based on the Cauer thermal network model. The result is verified with the power module datasheet. Moreover, the transient thermal impedance curve of the cold plate is shown in figure 4.15.



(a) Thermal impedance of the power module **(b)** Thermal impedance of the cold plate

Figure 4.15: Transient Thermal impedance obtained from the Cauer model in MatLab/Simscape.

5

Investigation of the material Graphene

In this section, the impact of graphene as one sheet layer close to the chip on the power module, and replacement of aluminium fins towards graphene fins in the cold plate is investigated. The goal was optimizing the thermal capacitance and resistance of the heatsink and transport the heat down to the cooling liquid.

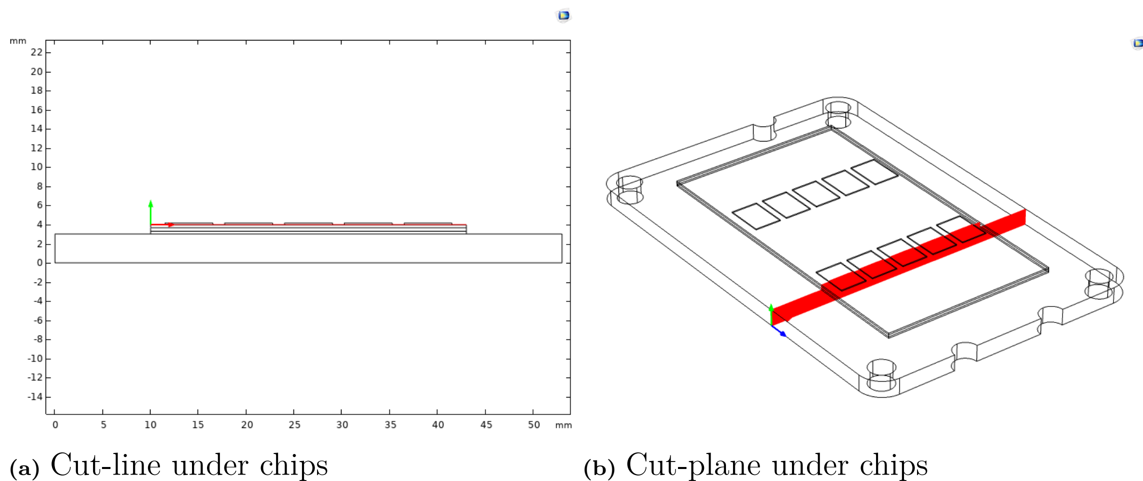
5.1 Effect of Graphene layer on the power module

Since the material Graphene is a very good heat spreader, the most logical place to implement the Graphene layer would be as close to the heat source as possible. That place would be below the chips, however, since the Graphene material has an insulating ability, it would weaken electrical conductivity [18]. Thus, an ideal place for the Graphene layer would be below the first copper layer, above the SiN layer.

To prove this theory where the best results are achieved when the Graphene layer is placed as close to the chips as possible. Two cases were studied, one where the Graphene is directly placed below the chips and one where the Layer is placed above the SiN layer. The thickness of the Graphene layer was $2\mu m$ with a thermal conductivity of 2500 W/(mK) in x- and y-direction. The thermal conductivity in z-direction is set to be 14 W/(mK) [8]. Material properties of the Graphene are shown in figure 5.1. The material Graphene has a contact resistance to the other surfaces, this resistance set to be 10^{-6} K/W [8]. The simulations were done with only the power module and without the cold plate. The temperature was measured in two ways, one through a cut-line, one that goes through the module horizontally below the chips and the other through a cut-plane that goes through the chips horizontally as well. Figure 5.2 shows both cut-lines that were used in these simulations.

	Property	Variable	Value	Unit	Property group
✓	Density	rho	2267	kg/m³	Basic
✓	Thermal conductivity	{k11, k22...	{2500,2500,14}	W/(m·K)	Basic
✓	Heat capacity at constant pressure	Cp	720	J/(kg·K)	Basic

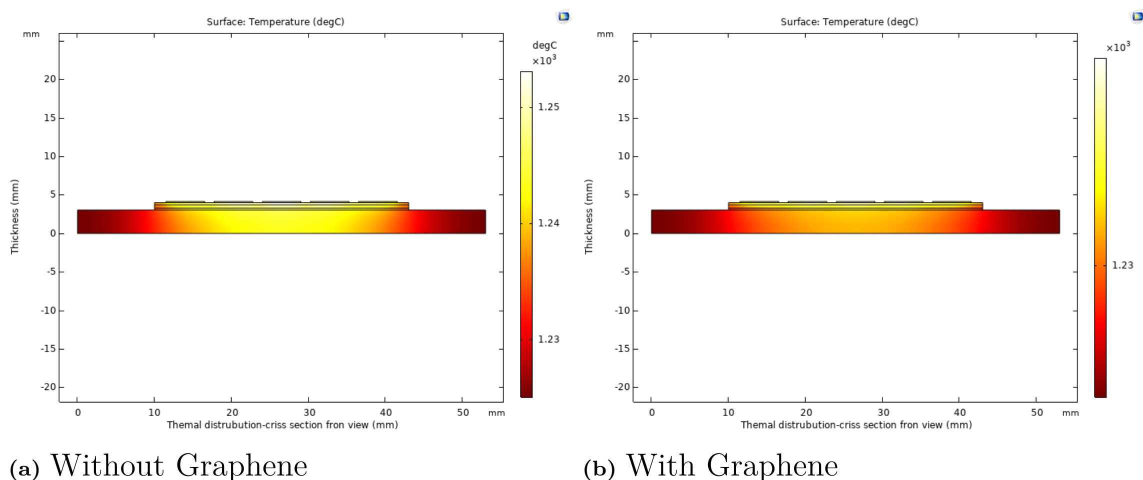
Figure 5.1: Properties of material Graphene



(a) Cut-line under chips (b) Cut-plane under chips

Figure 5.2: Figure shows the cut-line and cut-plane that were used to measure the temperature distribution.

Before making a comparison between the two cases, a comparison between the results with Graphene and without had to be made to make sure there was an actual improvement. There was a noticeable difference as expected. In figure 5.3, it can be noticed that the heat distribution is better with Graphene than without. In this simulation the Graphene layer is placed below the chips. With Graphene, the heat is more distributed across the baseplate, and in the case without the heat is more concentrated in the middle where the chips are located. The distribution across each layer can be seen more clearly in figure 5.4. The temperature reduction when Graphene is introduced amounts to be around only 14-15°C, which is a 2% improvement compared to without Graphene. However, the temperature distribution is more flat which means that each layer is absorbing more heat and that is the most interesting part. This has led to a decrease in thermal resistance as well which now is equal to 0.064 K/W. It is a reduction by 30.3% compared to the case without Graphene (0.0945 K/W).



(a) Without Graphene (b) With Graphene

Figure 5.3: Temperature distribution with and without Graphene.

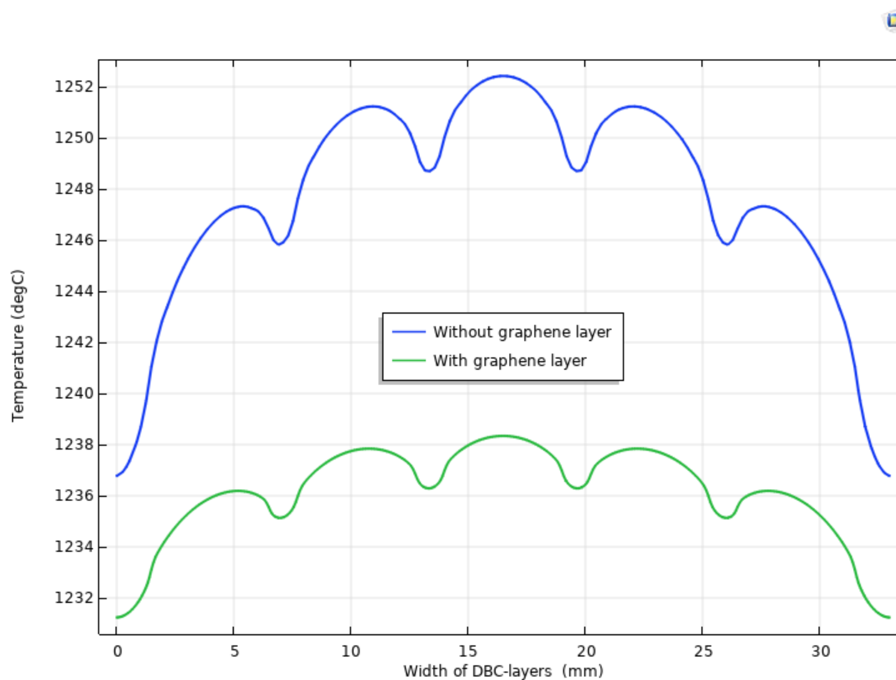
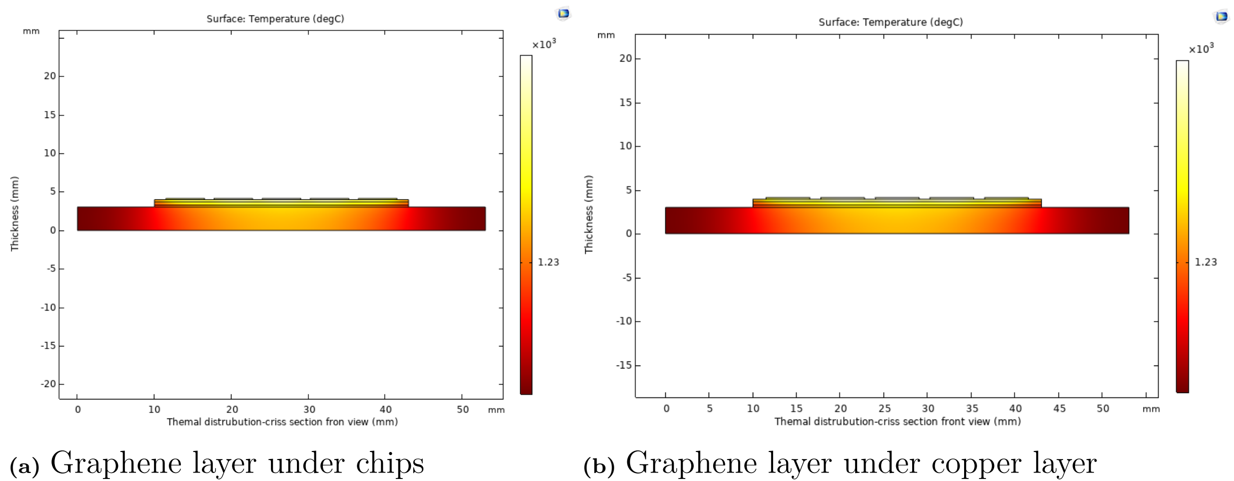


Figure 5.4: Temperature distribution across each layer, with and without Graphene.

Moving to a more realistic simulation, which is the second case where the Graphene layer is below the copper layer, the results are still positive. However, there is a small but noticeable difference in the distribution of heat. Figure 5.5 shows a comparison between the results obtained from the two cases. It can be observed that the heat distribution is better when the Graphene layer is closer to the chips. But the improvement is still very small and the reduced temperature only amounts to 1-2°C. The most noticeable difference is between the chips as figure 5.6 demonstrates. There is a small dip in temperature with the Graphene layer below the chips. Because there was no high temperature reduction between the two cases the thermal resistance was still at the same level.



(a) Graphene layer under chips

(b) Graphene layer under copper layer

Figure 5.5: Tepmerature distibution for Graphene layer under the chips and under the copper layer.

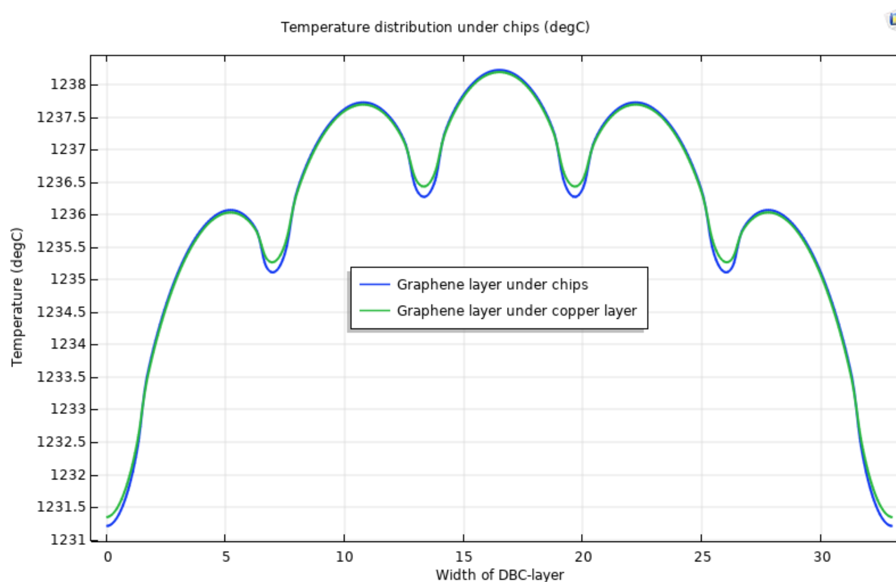
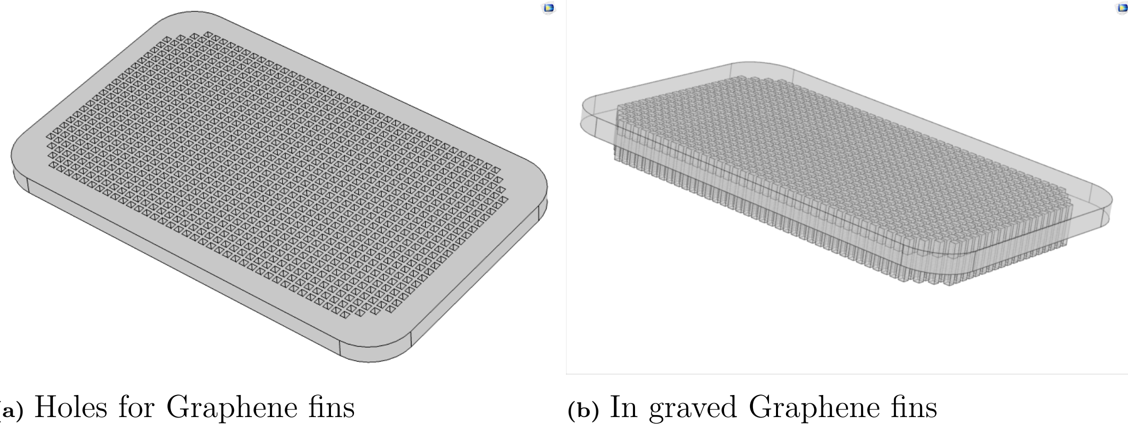


Figure 5.6: Temperature distribution across each layer with Graphene bleow the chips and below the copper layer.

5.2 Effect of Graphene fins on the cold plate

An alternative way of implementing Graphene is by substituting the fins material with Graphene. In reality this is a very challenging task to implement physically because normally the Graphene layers are thin and hard to shape in certain ways. However, in this investigation it was assumed that shaping the Graphene material in a cubic fins shape is possible. To make this investigation more realistic the Graphene fins needed to be attached to the plate in a certain way. The fins were in graved in the plate with a 2.25 mm depth and a 4 mm fin length that is sticking out of the plate, see figure 5.7. The thermal conductivity of Graphene in this case is set to

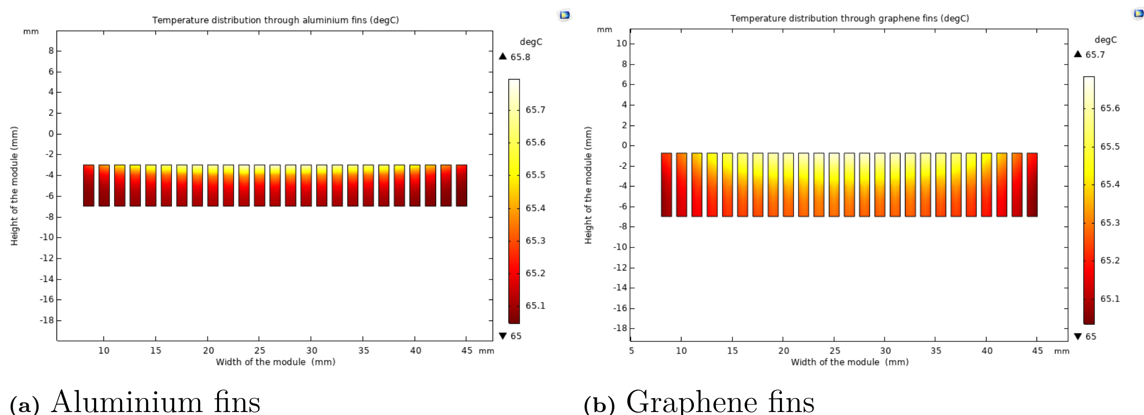
have a 14 W/(mK) in x- and y-direction, and 2500 W/(mK) i z-direction.



(a) Holes for Graphene fins (b) In graved Graphene fins

Figure 5.7: Geometry for the Graphene fins

The simulations with Graphene fins were done in the same manner as previous simulations to have a reasonable comparison with previous results. The simulations, in this case, were mainly focused on the fins and the heat distribution around them. The results were quite clear in this case as well, with Graphene the heat is absorbed and distributed more than Aluminium fins. Figure 5.8 displays a comparison between normal Aluminum fins and Graphene fins. In the figure, the Graphene fins are longer than the Aluminum fins but the length of the fins that are pointing out of the plate is the same (4 mm). The fins seen in the figure are exactly below the chips which means they are absorbing the most heat out of the rest. There is not much difference in a reduced temperature, but the Graphene fins are absorbing more heat and distribute it further to the liquid. This means the system has gained a better overall heat distribution than before.

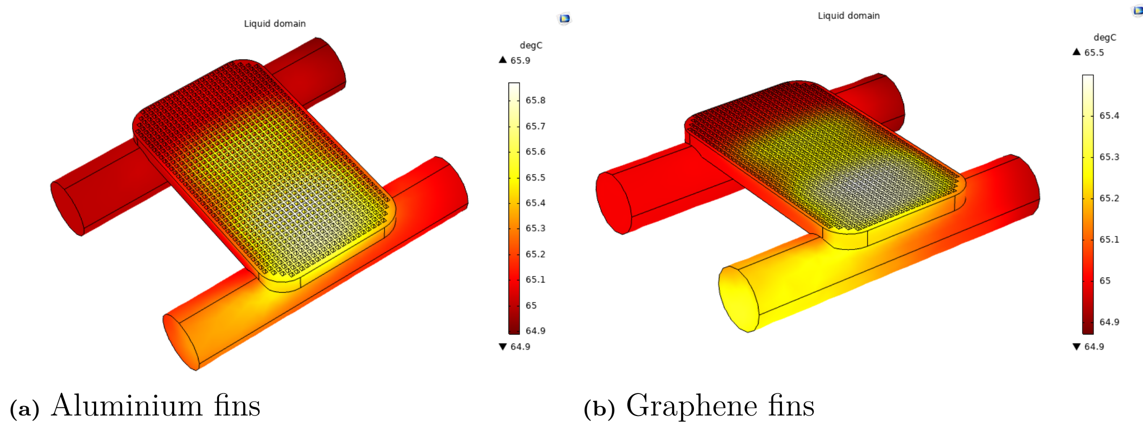


(a) Aluminium fins (b) Graphene fins

Figure 5.8: Temperature distribution with Graphene and Aluminum fins.

A closer look at the liquid temperature can be seen in figure 5.9 which shows a liquid domain plot for the Graphene and Aluminum fins. The focus here is on the outlet

temperature where with Graphene there was an increase by approximately 0.4°C. The thermal resistance for this case was calculated to be 0.0084320 K/W, which is a decrease by 39.3% compared to the case without Graphene fins.



(a) Aluminium fins

(b) Graphene fins

Figure 5.9: Liquid domain temperature distribution with Graphene and Aluminum fins.

5.3 Application of Graphene layer and fins simulation

Since the material Graphene was showing positive effects on the thermal distribution and reduction of temperature it would be interesting to combine both strategies demonstrated in sections 5.1 and 5.2. In this simulation, a Graphene layer and Graphene fins were included at the same time with the same settings and set-up as the previous simulations. With both the Graphene layer and fins combined, there was a reduction in temperature by 1.7 °C and an overall 2% improvement compared to the case where Graphene is not used. However, the fluid temperature remained at approximately the same level with only 0.3°C difference, see figure 5.11. In terms of thermal resistance, it was noticed that there is a decrease of 40.2% compared to the case where no Graphene is used. The now calculated thermal resistance amounts to 0.0083206 K/W.

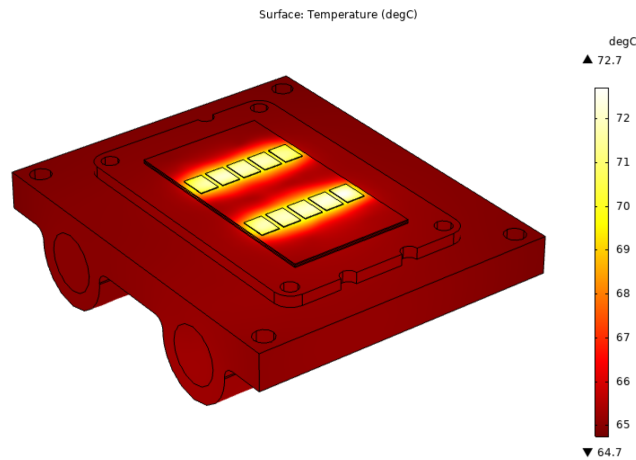
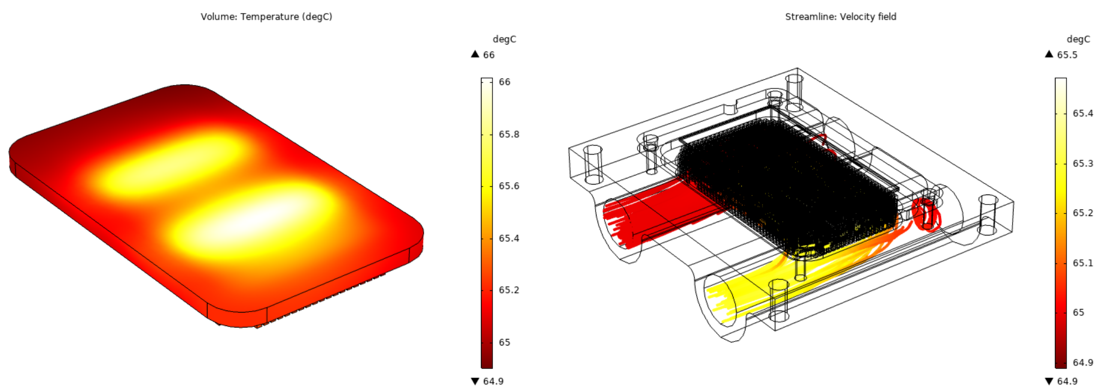


Figure 5.10: Temperature distribution across power module and cold plate when the Graphene layer and fins has been applied

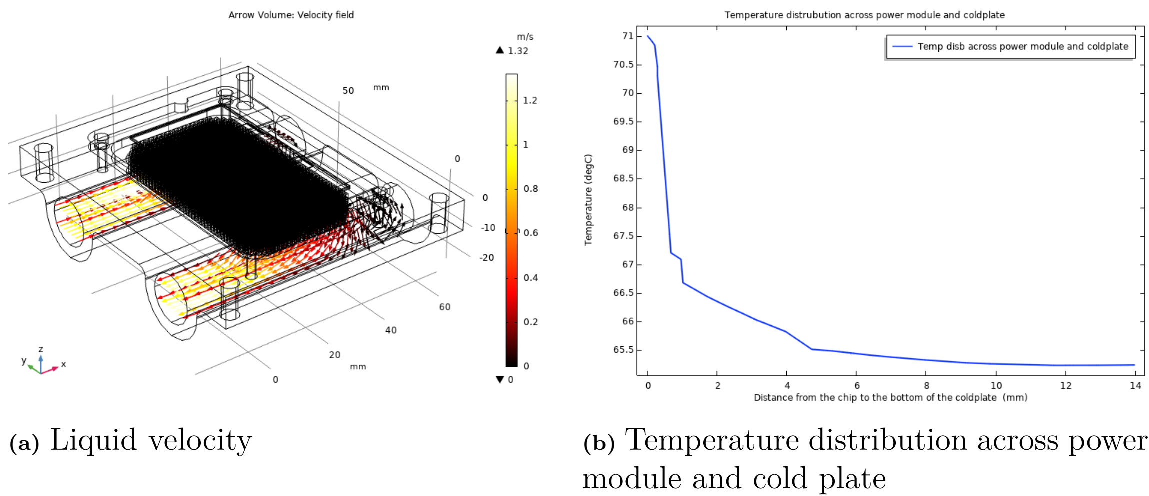


(a) Temperature distribution on Pin fin plates

(b) Velocity field and temperature distribution of liquid

Figure 5.11: The figures demonstrates the temperature distribution and fluid velocity across the coldplate and pin fin plates.

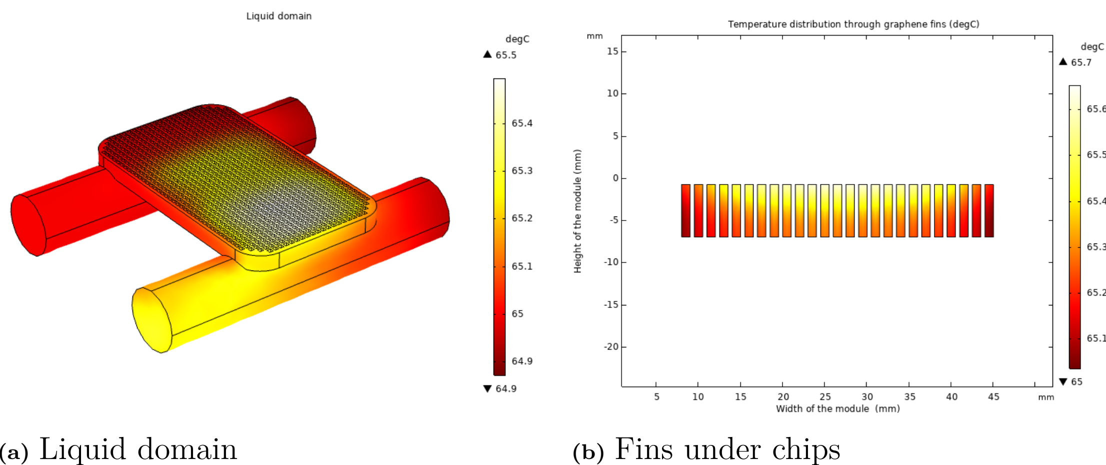
As it can be seen in figure 5.12b, the maximum junction temperature of the power module has decreased by 3.3 °C compare to the case without Graphene layer and fins 4.10b.



(a) Liquid velocity

(b) Temperature distribution across power module and cold plate

Figure 5.12: The figures liquid velocity field and temperature distribution across the cold plate and power module.



(a) Liquid domain

(b) Fins under chips

Figure 5.13: The figures demonstrate temperature distribution through liquid domain and fins.

As a comparison with results found in section 4.7.2, the simulations with Graphene indicates shows that there is a decrease in thermal resistance by up to 40.2%. Between the second and third cases in table 5.1, there is no significant difference. With Graphene fins and layer there is still a very small decrease, however, the thermal resistance decreases by 1.32% compared to when only Graphene fins are used.

Table 5.1: Thermal resistance of different case simulation

Simulation Case	Thermal resistance R_{th} [K/W]
Cold plate with Aluminium fins and power module	0.013893
Cold plate with Graphene fins and power module	0.0084320
Cold plate and Power module with Graphene fins and layer	0.0083206

5.4 Transient thermal simulations

For the transient analysis when Graphene is added there are noticeable results as well. However, the difference was only noticed in the COMSOL model and not in the Simscape model, see figure 5.14. With the COMSOL model there was a 2% difference, the temperature dropped by 1-2°C. In the Simscape model, there was no difference in result compared to previous simulations. That can be explained by the thermal conductivity, the Cauer model only considers the thermal conductivity in the z-direction and not in XY-direction. Since Graphene has its highest thermal conductivity in XY-direction the results will not differ by significant values.

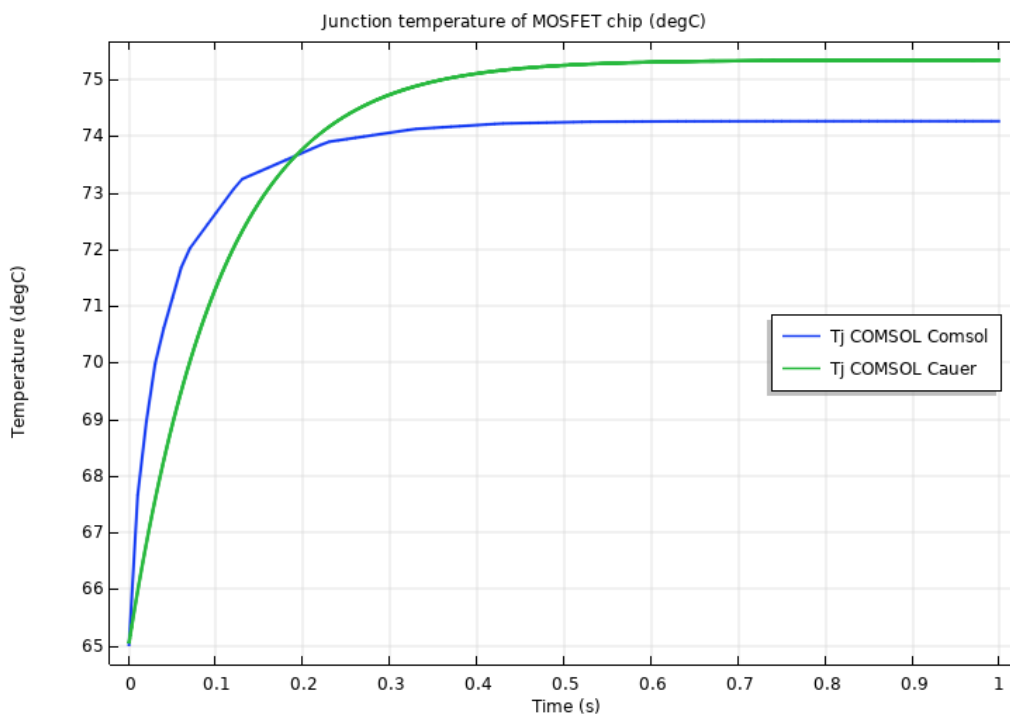


Figure 5.14: Junction temperature after application of Graphene layer below the copper layer

6
Conclusion

In this thesis work, an investigation was conducted regarding the heat distribution of the material Graphene when implemented in as a layer in a power module packaging system, as well as Graphene fins in a liquid cooled cold plate. The investigation was mainly focused around the power module CAB450M12XM3 where a thermal model was created using the software COMSOL Multiphysics. The overall work of the thesis was carried out in a three-phase strategy.

The first phase of the work was concentrated on creating a thermal model for the power module CAB450M12XM3 in COMSOL. Before beginning the creation of the module in COMSOL the total power loss of the device had to be identified. The power loss represented the heat source and through theoretical calculation was found to be 570 W per switch. Since most of the packaging system of the module was relatively unknown, a more simple theoretical thermal model was created using the Cauer thermal model. By using typical values for each layer the Cauer model showed a thermal resistance of 0.07 K/W and a steady-state temperature of 76 °C. The COMSOL model as the Cauer model had to represent the packaging system of the actual model in terms of the insulation layers and the overall thermal resistance of the module. Through a literature study and by cutting a cross-section piece of a similar power module (CAS300M12BM2) it was estimated that the CAB450M12XM3 consists of six layers in total, including the baseplate. The materials for layers were found to be all-silicon carbide, $Sn_{90}Ag_{10}$, SiN, and copper. The thicknesses of the layers were found to be almost equal to typical values found in various kinds of literature. Two versions of the model were created in COMSOL untuned and tuned, where the untuned was built on typical thickness values and the tuned was built on values found from the module CAS300M12BM2 and other findings. Through simulations in COMSOL the thermal resistance for untuned and tuned models found to be 0.078 and 0.094 K/W respectively. The tuned model did come up short compared to the datasheet value of thermal resistance (0.11K/W). However, this was due to the thermal coupling and heat spreading effect and was proven through a small test model which had a thermal resistance of 0.1 K/W.

The second phase of the work included choosing a cooling strategy for the module and implement it in COMSOL. Through a literature study regarding cooling techniques for power modules in automotive vehicles it was found that the most optimal solution is liquid cooling. Since all liquid cooling includes a cold plate the type PFCP was chosen due to its being the most advanced and it included fins which were crucial for the last phase of the work. A cold plate model, CP3012, was chosen

due to that it met the requirements mentioned earlier. The model was replicated in the same manner as the power module, where the thermal resistance needed to match the one presented in the datasheet. After the model was created in COMSOL, a minor investigation regarding the type of fins and gap distance could give the best results and it was found that the lowest thermal resistance was achieved when the cubic fins have a diameter of 2 mm and a gap distance of 1 mm. After the adjustments to the fins were made the model was ready for the Graphene simulations.

In the third and last phase of the work, Graphene was implemented as a layer and as fins to help spread and distribute the heat better than the current solution. Graphene was simulated as a thin layer (2 um) below the chips and below the copper layer, separately. The results showed that with Graphene there is an improvement in heat distribution between the layers and overall reduction in temperature by 2% and a reduction in thermal resistance by 30.3% for the case when a Graphene layer is implemented. Moreover, through simulations it was proven that implementing Graphene as close to the chip as possible will give the best thermal distribution. Almost similar results were achieved when Graphene was introduced as fins in the cold plate. A better thermal distribution could be noticed due to the fins absorbing more heat than before. However the thermal resistance in this case reduced by 39.9% compare to the case of aluminium fins. Moreover, when both Graphene fins and layer were implemented, the results showed a decrease of junction temperature of 3.3°C and reduction in thermal resistance by 40.2% compared with the case when Graphene was not used.

7 Discussion

7.1 Sustainability aspects

Today the automotive industry is going through a shift, where there is a decrease in combustion engine vehicles and an increase in electric and hybrid vehicles manufactured. This is mainly due to the movement towards a better and more sustainable transportation. Since power inverters are required in electric and hybrid vehicles to transform the DC power supplied by the battery to AC power supplied to the motor.

The most commonly used power electronic switches today in the automotive industry are Silicon-based (Si) IGBTs. Since there are many challenges and limitations with IGBT modules, such as switching frequencies and the maximum allowable operating temperature, the industry is shifting more towards all Silicon-Carbide (SiC) MOSFETs [19]. The advantage with SiC MOSFETs is the reduction in switching losses which amounts to 70-80% compared to those of Si IGBTs [20]. In turn, this makes the SiC MOSFET a better and more sustainable solution compared to using a Si IGBT. However, SiC MOSFETs have the disadvantage of being too costly and therefore it is only used when one wants to enhance the performance of the inverter considerably.

7.2 Ethical aspects

To evaluate the possible risks and consequences of this master thesis project an ethical analysis has been made. The ethical analysis was conducted based on the methodology and the results of the project. Discussing the moral reasoning behind the choices based on scientific background. This ethical analysis has been made based on the IEEE codes of ethics [21], and some code of ethics has been followed during the project.

In the last couple of years, it has been noticed that electric vehicles are becoming increasingly popular. There is a lot of research going on power electronics to make the electric car even more efficient. Therefore, there is need for improvements made in the area of thermal distribution of power modules. This will consequently reduce the power loss and increase the efficiency of the electric vehicle, which in turn affect people's lives in order for them to have a society free of toxic gases.

This master thesis project has its core focus in advancing the technology and components used in an electric vehicle to increase efficiency by improving the thermal distribution through a power module. In addition, to develop a thermal model and investigate the opportunity to enhance the thermal distribution through the power module by introducing Graphene.

While carrying the project an attempt has been made according to the code of ethics, to be honest, and realistic when presenting the real data from the measurement as well as limitations. The result from this project is the guidelines for future power electronic development companies as well as for research centres to use more efficient and sustainable power electronic devices. This can be considered as the positive impact that outweighs the negative factors, in turn this can be seen as an indication that this project was ethically correct to conduct.

7.3 Future work

This section gives some thought to what could be further analyzed and investigate in future work.

- In this project, a 3D COMSOL model for a single power module has been build. However, the model can expands and develop to build a thermal model for a 3 phase system, in other word for three power module including cold plate in the future.

- The effect of two fins shapes cubical and cylindrical on the thermal resistance of the power module has been investigated in this project. More shapes such as conical, herringbone, lanced, offset, lanced and offset, ruffled, lazily ruffled and perforated fins could be simulated in the future.

- Time-dependent simulation of COMSOL model can be performed. Consequently, transient thermal analysis and transient thermal impedance can be carried out.

- Increasing the quality of the mesh, to improve the accuracy of the results. However, this requires a powerful computer and longer computational time.

- Implementing material Graphene as a sheet layer and fins showed a promising result. Other possibilities can be investigated such as applying graphene as a thin layer around the fins.

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A

Appendix 1

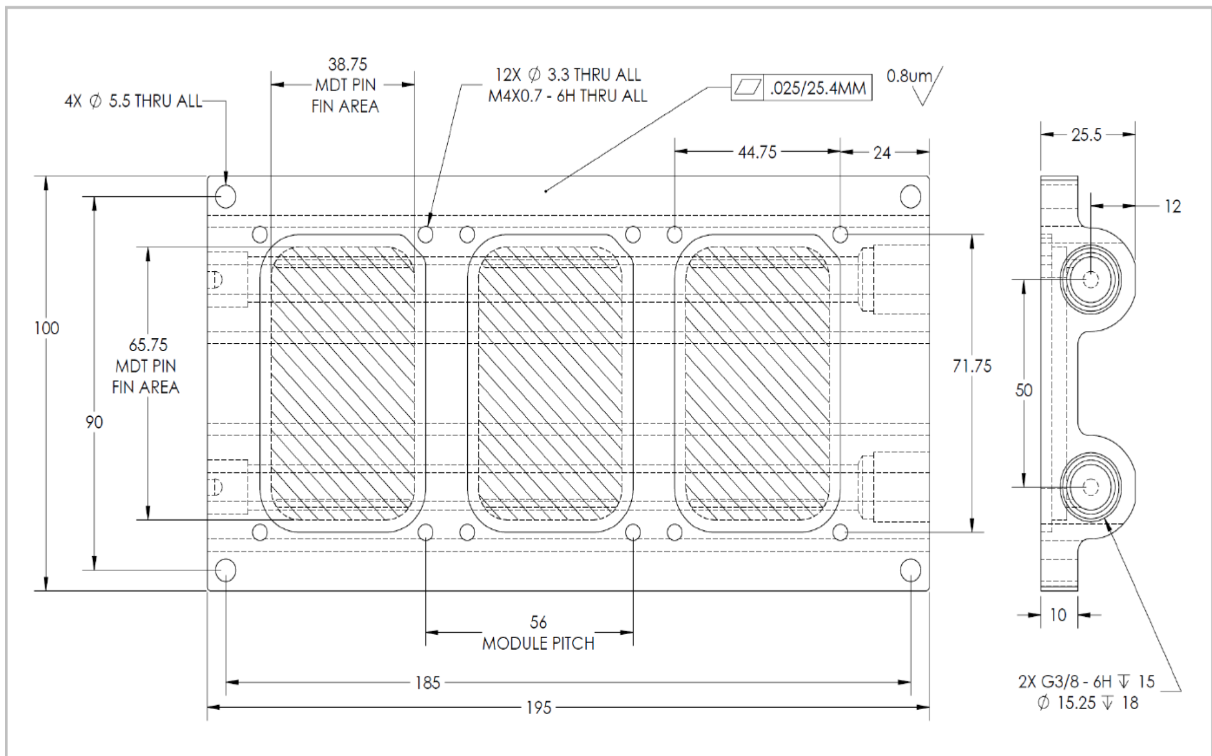

Figure A.1: Dimension of the CP3012 cold plate