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Modelling and analysis of Shunt-connected Voltage Source Converter for voltage dip mitigation

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THESIS FOR THE DEGREE OF MASTER SCIENCE

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To my beloved parents

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Abstract

Distribution Static Synchronous Compensator (D-STATCOM) is a Custom Power Device based on a Voltage Source Converter (VSC) shunt connected to the grid. By injecting a controllable current, it can improve the quality of the load current, e.g. compensating harmonic currents or fluctuating currents. If a D-STATCOM is equipped with an energy storage, the system is also called Energy Storage Equipment STATCOM (E-STATCOM).

This thesis focuses on the E-STATCOM for mitigating voltage dips. A short description of power quality problems has been done, with particular attention a in-depth study on voltage dip problem and its solution has been conducted. Afterwards the control system for the E-STATCOM has been derived. The vector current- and voltage-controllers have been designed and their behaviour has been studied. The impact of controller bandwidths and of model parameters has been investigated. The dual vector current- voltage-controllers (DVCC DVVC) have been designed in order to improve the performance con the control system also under unbalanced conditions. All results are verified in MATLAB and simulated in PSCAD/EMTDC.

The system has been tested to mitigate both balanced and unbalanced voltage dips, with several types of loads.

Index Terms: Power Electronics, Power Quality, Current Controller, Voltage Controller, Voltage Dip (Sag), Voltage Source Converter (VSC), shunt compensation, dual vector controller, PLL.

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Paolo Cilona
Gothenburg, Sweden
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Contents

Chapter 1

Introduction

1.1 Background and motivation

Power quality phenomena include all possible situations in which the waveform of the supply voltage or load current deviate from the sinusoidal waveform at rated frequency with amplitude corresponding to the rated rms value for all three phases of a three-phase system. But poor quality of the current taken by many customers together will ultimately result in low quality of the power delivered to other customers: e.g. both harmonics and unbalanced currents ultimately cause distortion and, respectively, unbalance in the voltage as well. [1]

Among power quality problems voltage dips are one of most important. Voltage dips are sudden drops in voltage with duration between half a cycle and some seconds, mainly caused by short circuits and starting of large motors. The interest in voltage dips is due to the problems they cause on several types of equipment. As an example adjustable-speed drives, process-control equipment, and computers are especially notorious for their sensitivity. Some pieces of equipment trip when the rms voltage drops below 90% for longer than one or two cycles. Such a pieces of equipment might trip tens of times a year. The cost to US industry of voltage dips is estimated to be 10 billion US$ per year. The cost of a single severe voltage dip to one semiconductor manufacturer in Singapore is estimated to be 1 million Singapore$ per event. [2]

Voltage dips at equipment terminal can be due to short-circuit faults hundreds of kilometers away in the transmission system. To solve this problem, several different Custom Power devices have been proposed. The term Custom Power has been defined as "the concept of employing power electronic (static) controllers in 1 kV through 38 kV distribution systems for the purpose of supplying a compatible level of power quality necessary for adequate performance of selected facilities and processes". A "Custom Power Controller" is thus defined, accordingly, as "an active power electronic switch or inverter with the ability to perform current interruption and voltage regulating functions in the distribution system to improve power quality".

Many of which have at their heart a Voltage Source Converter (VSC) connected to the grid. Voltage dips can be mitigated by injecting a controllable current into the grid with a shunt-connected VSC. This device is called distribution STATCOM or D-STATCOM. If a D-STATCOM is equipped with an energy storage, the system is also called Energy Storage Equipment STATCOM (E-STATCOM). The E-STATCOM is used as active filter and voltage regulation.

By injecting a current in the point of connection, a shunt-connected VSC can also boost the voltage in that point during a voltage dip. The VSC must be controlled properly to inject the necessary current into the grid in order to compensate for the voltage dip. Since some sensitive loads can shut down because of a dip that lasts some hundreds of ms, the speed of response of the device is a decisive factor for successful compensation. Moreover, most voltage dips are unbalanced, and therefore another requirement for successful dip compensation is a fast detection of the grid voltage unbalance and a high-performance control of the VSC [3].

1.2 Aim and outline of this thesis

The aim of this thesis is to improve, analyze and test, via simulation, control algorithms for shunt-connected VSC, for mitigation of balanced and unbalanced voltage dips. The first part of this work has a focus on power quality problems and in particular on voltage dip, and its main mitigation methods. In the second part a detailed analysis of shunt-connected VSC will be carried out. In Chapter 4 the control system for shunt-connected VSC will be derived, both for balanced and unbalanced conditions. In Chapter 5, the control system will be tested in order to mitigate balanced and unbalanced voltage dips for different kinds of load.

Chapter 2

Power Quality and Custom Power

2.1 Introduction

Even a few years back, the main concern for customer was the reliability of electric power supply. Here we indicate as reliability the continuity of electric supply. It is not only reliability that the consumers wants these days, quality is also very important. Both electric utilities and consumers are becoming increasingly concerned about the quality of electric power. For example, a consumer that is connected to the same bus that supplies a large motor load may have to face a severe dip in his supply voltage every time the motor load is switched on. This may be unacceptable to most customers. There are also very sensitive loads such as hospitals, processing plants, air traffic control, financial institutions and numerous other data processing and service providers that required clean and uninterrupted power. In several processes such as semiconductor manufacturing or food processing plants, a batch of product can be ruined by a voltage dip of very short duration. Such customers are very concern of such dips since each event will result in an economical loss.

There are three major reasons for the increased concern on power quality [4]:

- Newer-generation load equipment, with microprocessor-based controls and power electronic devices, is more sensitive to power quality variations than was equipment used in the past.
- The increasing emphasis on overall power system efficiency has resulted in continued growth in the application of devices such high-efficiency, adjustable-speed motor drives and shunt capacitors for power factor correction to reduces losses. This is resulting in increasing harmonic levels on power systems and has many people concerned about the future impact on system capabilities.
- End-users have an increased awareness of power quality issues. Utility customers are becoming better informed about such issues as interruptions, dips, harmonics and switching transients and are challenging the utilities to improve the quality of power delivered.

The reason for the increased interest in power quality can be summarized as follows [5]:

- **Metering:** Poor power quality can affect the accuracy of utility metering.
- **Protective relays:** Poor power quality can cause protective relays to malfunction.
- **Downtime:** Poor power quality can result in increased costs due to the preceding effects.
- **Electromagnetic compatibility:** Poor power quality can result in problems with electromagnetic compatibility and noise.

2.2 Characterization of electric power quality

The term electric power quality broadly refers to maintaining a near sinusoidal power distribution bus voltage at rated magnitude and frequency. In addition, the energy supplied to a customers must be uninterrupted from the reliability point of view.

Ideal power quality for the source of energy to an electrical load is represented by the three-phase waveforms of voltage shown in Figure 2.1 . The amplitude, frequency, and any distortion of the waveforms must remain within prescribed limits. When the voltages shown in Figure 2.1 is applied to electrical loads, the load currents will have frequency and amplitudes dependent on the impedance or other characteristics of the load. If the waveform of the load current is also sinusoidal, the load is termed "linear". If the waveform of the load current is distorted, the load is termed "nonlinear". The load current with distorted waveform can produce distortion of the voltage in supply system, which is an indication of poor power quality [5].

Most PQ problems occur in distribution systems. In most metropolitan cities, the distribution feeders run underground in the central business districts. In most other places, the feeders run overhead. As a result these lines can easily come in contact with trees. Furthermore, they are likely to be hit by lightning or suffer from interference from birds and smaller animals, causing arching, momentary transients in voltages or voltage dip/swell.

A single customer can impose its harmonics and the effect of unbalanced loads on other customers. Furthermore, switching on of a large induction motor can cause a large inrush current to flow in that circuit causing a voltage dip in other parts of the system. Based on the above discussions, we can summarize that there are two different categories of causes for the deterioration in PQ [2]. The first category contains natural causes such as

- Faults or lighting strikes on distribution feeder.
- Falling of trees or branches on distribution feeders during stormy conditions.

- Equipment failure.

The second category contains the man made causes that may be due to load or feeder line operation. Some of these causes are

- Transformer energization, capacitor or feeder switching.
- Power electronic loads, adjustable speed drives (ASD) etc.
- Arc furnaces and induction heating systems.
- Switching on or off of large loads.

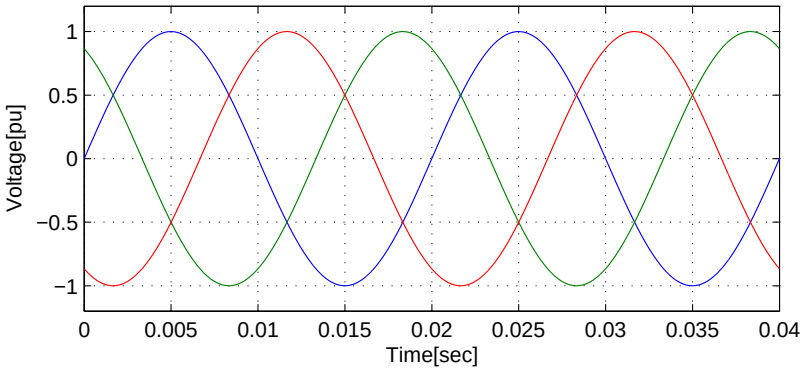

Figure 2.1: Ideal three-phase voltage waveform.

The PQ standards vary among countries. However, it is needless to say that poor quality affects almost all consumers. It is therefore important to list the terms and definitions that are used with power quality. In particular, we shall consider the following

- **Transients** A transient is that part of change in a system variable that disappears during transition from one steady-state operating condition to another. Transients can be classified into two categories: impulsive transients and oscillatory transients. According to IEEE Std.1159-1995 [6], an impulse transients is a sudden non-power frequency change in the steady-state condition of voltage or current that is unidirectional in polarity (primarily either positive or negative) while, an oscillatory transient is a sudden, non-power frequency change in the steady-state condition of voltage or current that includes both positive or negative polarity value.
- **Short duration voltage variations** Any variation in the supply voltage for duration not exceeding one minute is called a short duration voltage variation. Usually such variations are caused by faults, energization of large loads that require large inrush currents and intermittent loose connection in the power wiring. Short duration variations are further classified as voltage dips, voltage swells and interruptions. According to IEEE Std.1159-1995 [6], a voltage dip

is defined as a decrease between 0.1 to 0.9 pu in the RMS voltage at the power frequency with duration from 0.5 cycles to 1 minute. Voltage swells are defined as the increase of a fundamental frequency voltage for a short duration. Voltage swells are not as common as voltage dips. An interruption occurs when the supply voltage decreases to less then 0.1 per unit for a period of time not exceeding 1 minute.

- **Long duration voltage variations** These are defined as the rms variations in the supply voltage at fundamental frequency for periods exceeding 1 minute. These variations are classified into over-voltages, under-voltages and sustained interruptions. An over-voltage (or under-voltage) is a 10% or more increase (or decrease) in rms voltage for more than 1 minute. When the supply voltage is zero for a period of time in excess 1 minute, the long duration voltage variation is called sustained interruption.

- **Voltage unbalance** This is the condition in which the voltages of the three phases of the supply are not equal in magnitude. Furthermore, they may not even be equally displaced in time. Severe unbalance (grater than 5%) can result during single phasing conditions when the protection opens up one phase of a three-phases supply.

- **Waveform distortions** This is the steady-state deviation in the voltage or current waveform from an ideal sine wave. These distortions are classified as DC offset, harmonics and notching. The presence of a load drawing DC current results in a DC component of the current in the secondary of a distribution transformer. This current will cause a DC bias in the sinusoidal flux of a transformer core. This increased peak value of the flux may push the transformer towards saturation.

  Power electronic loads like UPS, adjustable speed drives etc usually cause harmonics in power system. A measure of harmonic content in a signal is the total harmonic distortion (THD). The percentage THD in a voltage is given by

$$THD[\%] = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \cdot 100 \tag{2.1}$$

  where V_n denotes the magnitude of the n^{th} harmonic voltage and V_1 is the magnitude of the fundamental voltage.

  Notching is a periodic voltage distortion due to operation of power electronic converts when current commutates from one phase to other. During this period there is a momentary short circuit between the two phases that distorts voltages. The maximum voltage during notches depends on the system impedance.

- **Voltage fluctuations** These are systematic random variations in supply voltages. A modulation of the amplitude in the supply voltage is called voltage

flicker. This is caused by rapid variations in current magnitude of loads such as arc furnaces.

Figure 2.2 shows a typical power disturbance.

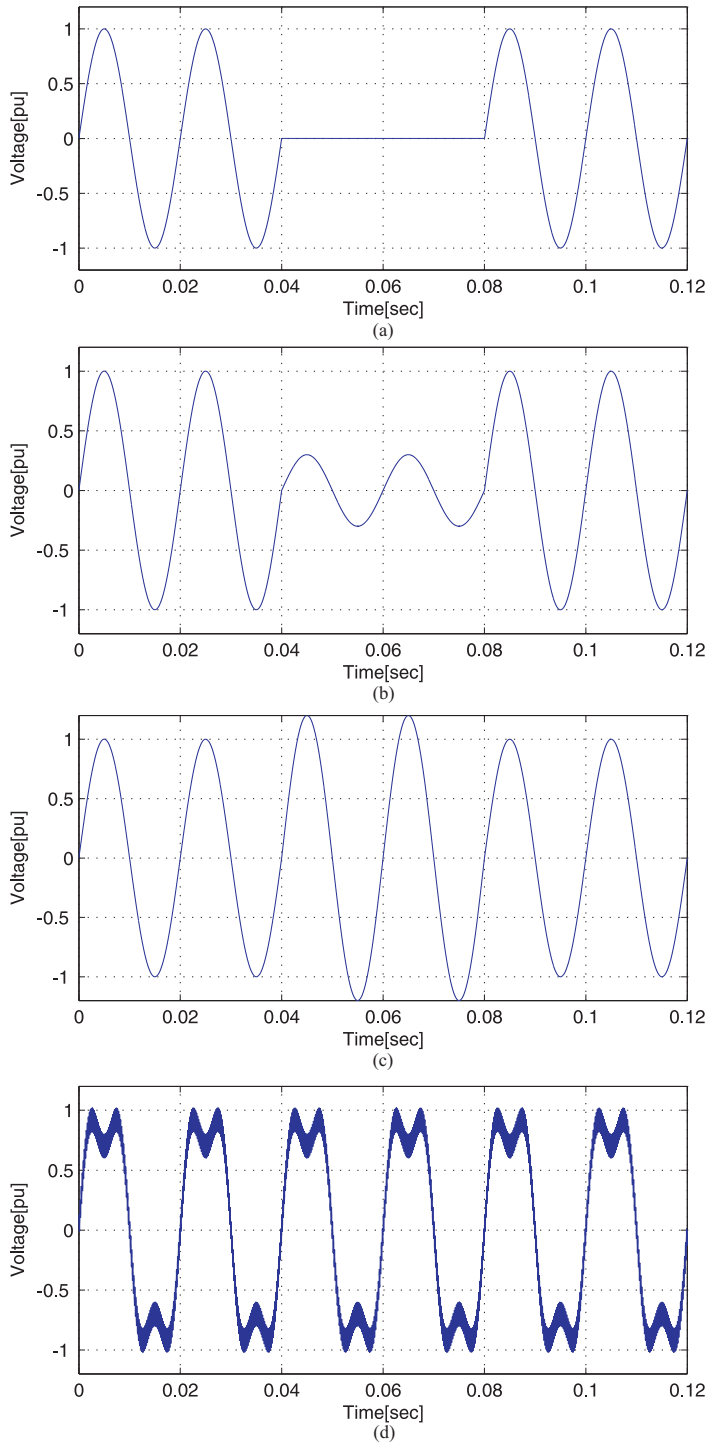

Figure 2.2: Typical power disturbances.(a)Interruption, (b)Dip, (c)Swell and (d)Harmonics

Following table reports a summary of PQ problems and their causes [2]

Table 1.1 Power quality problems and their causes

Broad Categories	Specific Categories	Methods of Characterization	Typical Causes
Transients	Impulsive	Peak magnitude, rise time and duration	Lightning strike, transformer energization, capacitor
	Oscillatory	Peak magnitude, frequency components	Line or capacitor or load switching
Short duration voltage variation	Sag	Magnitude, duration	Ferro-resonant transformer, single line-to-ground faults
	Swell	Magnitude, duration	Ferro-resonant transformer, single line-to-ground faults
	Interruption	Duration	Temporary (Self-clearing) faults
Long duration voltage variation	Under-voltage	Magnitude, duration	Switching on loads, capacitor de-energization
	Over-voltage	Magnitude, duration	Switching off loads, capacitor energization
	Sustained interruptions	Duration	Faults
Voltage unbalance		Symmetrical components	Single-phase loads, single-phasing condition
Waveform distortion	Harmonics	THD, Harmonic spectrum	Adjustable speed drives and other non-linear loads
	Notching	THD, Harmonic spectrum	Power electronic converters
	DC offset	Volts, Amps	Geo-magnetic disturbance, half-wave rectification
Voltage flicker		Frequency of occurrence, modulating frequency	Arc furnace, arc lamps

2.3 Power Quality Problems

Of the term and definitions of PQ that are listed in the previous section, some of the major concerns of both customers and utility are

- **Poor load power factor** Consider a distribution system in which a source is supplying an inductive load through a feeder. The feeder has a resistance of R_s and a reactance of X_s. The feeder current is denoted by I_s, the voltage is denoted by V_l and the power factor angle is denoted by θ_l. Now suppose the load power factor is poor,i.e., the load has a large X/R ratio. Then the load angle will be large. This implies that the reactive component of the current is large and hence the magnitude of the load current is also large. This will not be only cause a significant drop in the feeder voltage but there will also be a large decreasing of the active power for the load. Therefore, to operate the feeder in an optimal condition, the power factor at the load should be maintained near unity. In a ideal situation, the load power factor should be unity. However this may always not be achievable.

- **Harmonic contents in loads** Power electronic loads are the major source of harmonic generation in power system. Consider an example where a new main frame computer system has been installed in a multistoried office building. At the same time, to protect the computer, a very large uninterrupted supply (UPS) has also been installed. The UPS employs power electronic switches and as a result in can cause interferance to the loads that are connected in parallel with the UPS. Assuming that all the loads of a office building are placed on the same bus and that the AC filter of the UPS is not adequate, the UPS can cause screens of many smaller computer to flicker or roll and can even cause these computers to freeze. It can also cause other electronic circuits to malfunction. For example, it can change the timing sequence of the elevator control circuit.

- **Notching in load voltages** With rectifier loads there are commutation periods where the line to line voltage falls o zero. This effect is due to the finite inductance in the supply. Thus this causes a finite time for the current to fall to zero in one phase and transfer to another.

- **DC offset in load voltages** There are two main implications of the presence of a DC current in an electricity supply system. Usually at distribution level, a supply voltage system is equipped with a transformer that changes the voltage levels in accordance with the need of the consumers. It was mentioned earlier that a DC current can offset the flux excursions in a distribution transformer. As a result the magnetic core of a transformer gets heavily saturated resulting in excessive heating and distortion. The other aspect of DC current is the earth path. The return path for a DC current can often involve current through the earth. This will sometimes involve the DC current passing through buried structures such as pipes or reinforced steel. The DC current greatly enhances corrosion of metallic structures as it carries the metallic ions in the direction of the current flow.

- **Unbalanced loads** An unbalanced load produces the voltage unbalance. The larger the unbalanced current, the larger is the unbalance. The voltage unbalance can be decomposed into a positive sequence voltage, negative sequence and zero sequence voltage. This results in a torque reduction and in a vibration at the shaft.

- **Disturbance in Supply Voltage** As we have discussed before there can be various form of a disturbances in supply voltage such as interruption, distortion, over-voltage/under-voltage, dip/swell, flicker etc. These can have an adverse impact on the customers. For example, even small duration voltage interruption can cause relay tripping, thereby completely stopping a process line. Even a short duration outage can cause defects in the process. A few cycle voltage dip can force motors to stop thereby running a process.

2.4 Power Electronic Application in Power Distribution Systems

Custom power provides an integrated solution to the present problems that are faced by the customers and power distributors. Through this technology the reliability of the power delivered can be improved. The custom power devices are basically of two types: reconfiguring type and compensating type. The network reconfiguring equipment can be GTO based or thyristor based. They are usually used for fast current limiting and current braking during faults. They can also prompt a fast load transfer to an alternate feeder to protect a load from voltage dip/swell or fault in the supplying feeder. The following devices are members of the family of network reconfiguring devices [2]

- **Solid State Current Limiter (SSCL)** This is a GTO based device that inserts a fault current limiting inductor in series with the faulted circuit as soon the fault is detected. The inductor is removed from the circuit once the fault is cleared. The following figure shown a schematic diagram of SSCL

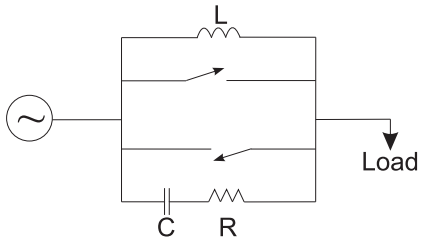

Figure 2.3: Schematic diagram of a SSCL.

- **Solid State Circuit Breaker (SSCB)** This device can interrupt a fault current very rapidly and can also perform auto-reclosing function. It has almost the same topology as that of an SSCL ezcept that the limiting inductor

iss connected is series with an opposite poled thyristor pair. This device, based on a combination of GTO and thyristor switches, is much faster than its mechanical counterpart.

- **Solid State Transfer Switch (SSTS)** This is usually a thyristor based device that is used to protect sensitive loads from dip/swell. It can perform a sub-cycle transfer of the sensitive load from a supplying feeder to an alternate feeder when a voltage dip/swell is detected in the supplying feeder. An SSTS can also be connected as a bus coupler between two incoming feeder. The following figure shown a schematic diagram of SSTS

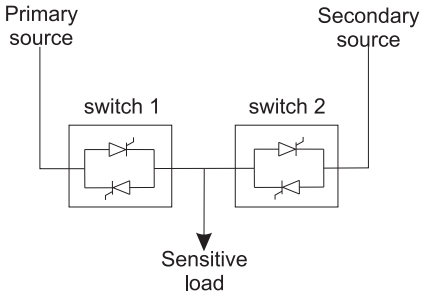

Figure 2.4: Schematic diagram of a SSTS.

The compensating devices are used for active filtering, load balancing, power factor correction and voltage regulation. The active filters, which eliminate the harmonic currents, can be connected in shunt. The active filters, which eliminate the harmonic voltages, can be connected in series. Some of these devices are used as load compensator, in this mode they correct the unbalance and distortions in the load currents such that compensated load draws a balanced sinusoidal current from the AC system. Some other are operated to provide balanced, harmonic free voltage to the customers. The family of compensating devices has following members

- **D-STATCOM** This is a shunt-connected VSC which structure is shown in the following figure. This can perform load compensation, power factor correction, harmonic filtering, etc. when connected at the load terminals.

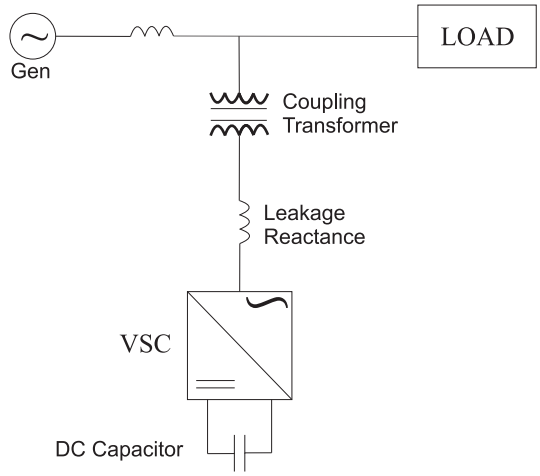

Figure 2.5: A D-STATCOM connected to a power system.

It can also perform voltage regulation when connected to a distribution bus. In this way it can keep the bus voltage constant against any unbalance or distortion in the distribution system. D-STATCOM is derived from STATCOM used in the transmission system; they have a similar structure. D-STATCOM must be able also to inject a unbalanced and harmonically distorted current to eliminate unbalance or distortions in the load current or the supply voltage.

- **Dynamic Voltage Restorer (DVR)** This is a series-connected VSC (also called Static Series Compensator (SSC)) which structure is shown in Figure 2.6 . The main purpose of this device is to protect sensitive load from dip/swell. This is accomplished by rapid series voltage injection to compensate for the drop/rise in the supply voltage. Since this series device, it can also be used as a series active filter. The DVR may have to inject unbalanced voltages to maintain the voltage at the load terminal in case of an unbalanced dip in the supply side. Furthermore when there is a distortion in the source voltage, the DVR may also have to inject a distorted voltage to counteract the harmonic voltage.

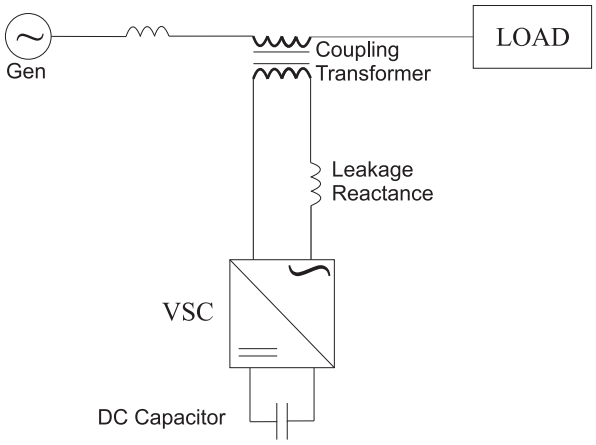

Figure 2.6: A DVR connected to a power system.

- **Unified Power Quality Conditioner (UPQC)** This is a very versatile device that can inject current in shunt and voltage in series simultaneously in a dual control mode (see Figure 2.7). Therefore it can perform both the functions of load compensation and voltage control at the same time. As in the case of D-STATCOM or DVR, the UPQC must also inject unbalanced and distorted voltages and currents.

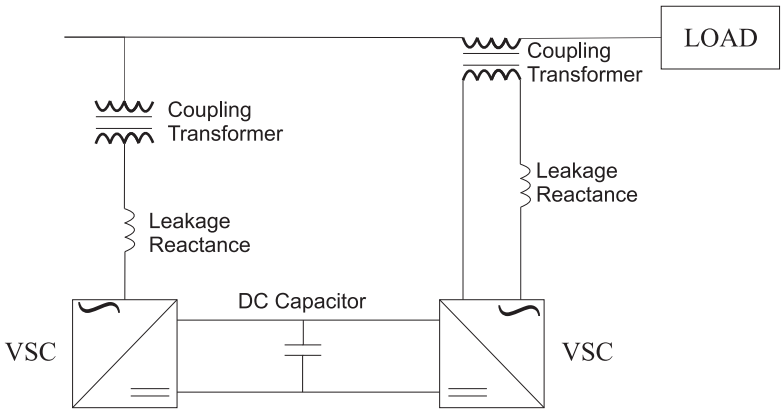

Figure 2.7: Schematic diagram of a UPQC

2.5 Conclusions

In this chapter a small description about power quality problems has been carried out. Moreovea small introduction about power electronic applications in power distribution systems has been presented. This work will focus on voltage dips mitigation through a shunt-connected VSC converter. The next chapter will present an overview of voltage dips and different solutions for voltage dip mitigation.

Chapter 3

Voltage Dips and Mitigation Methods

Power quality and reliability are essential for proper operation of industrial processes that involve critical and sensitive loads. Short-duration power disturbances, such as voltage dips, swells and short interruptions, are major concerns for industrial customers.

Due to wide usage of sensitive electronic equipment in process automation, even voltage dips which last for only few hundreds of milliseconds way cause production stops with considerable associated costs; these costs include production losses, equipment restarting, damaged or low-quality product and reduced customer satisfaction.

The high costs associated with these disturbances explain the increasing interest towards voltage dip mitigation methods. The cost of the mitigation intervention has to be compared with the loss of revenue and takes into account all economic factors involved.

This chapter will present an overview of voltage dips and different solutions for voltage dip mitigation, like power system improvements, load immunity and installation of mitigation devices will be treated.

3.1 Analysis of voltage dip

According to IEEE Std.1159-1995, a voltage dip is defined as a decrease between 0.1 to 0.9 pu in the RMS voltage at the power frequency with duration from 0.5 cycles to 1 minute. Typically the dip is characterized through the remaining voltage during the event. This is then given as a percentage of the nominal voltage. Thus, a 70% dip in a 230 V system means that the voltage dropped to 161 V. As mentioned in the previous chapter, a voltage dip can be caused by different events that can occur in the power system like transformer energizing, switching of capacitor banks, starting of large induction motors and short-circuit faults in the transmission and

distribution system. In this report, only voltage dips due to short-circuit will be considered [3].

Faults on the feeder can be initiated by [2]

- Lightning strike.
- Tree or branches falling on conductors.
- Animals across lines.
- Wind causing conductors to clash together.
- Digging equipment breaking cables.

The statistic of overhead lines indicate that

- 70% of the faults are single line to ground.
- 15% of the faults are double line to ground.
- 10% of the faults are line to line.
- 5% of the faults are three phase faults.

To quantify the dip magnitude in radial systems, the voltage divider model, shown in Figure 3.1 can be used, where Z_g is the grid impedance and Z_f is the fault impedance between the point of common coupling (PCC) and the fault [3]. The PCC is the point from which both the fault and the load are fed.

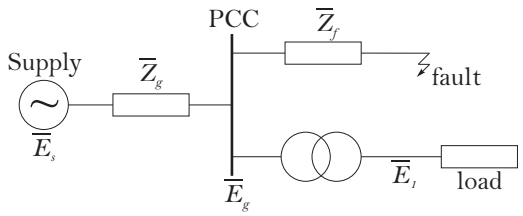

Figure 3.1: Single-line diagram to display voltage division during voltage dips.

The voltage at the PCC is found from:

$$\overline{E}_g = \frac{\overline{Z}_f}{\overline{Z}_f + \overline{Z}_g}\overline{E}_s \tag{3.1}$$

From (3.1) it is possible to observe that the voltage dip magnitude depends on the fault location(since the impedance on the distance between the point in the power system where the fault occurs and the PCC) and the grid impedance. This equation can be used to calculate the dip magnitude as a function of the distance to the fault.

Therefore, if $Z_f = zd$, with z the impedance of the feeder per unit length and d the distance between the fault and the PCC, leading to [7]:

$$\overline{E}_g = \frac{zd}{zd + \overline{Z}_g}\overline{E}_s \tag{3.2}$$

From this equation we can obtain the distance at which a fault will lead to a dip of a certain magnitude E. If we assume equal X/R ratio of source and feeder, we get the following equation:

$$d_{crit} = \frac{\overline{Z}_g}{z} \times \frac{E}{1-E} \tag{3.3}$$

This distance is often called "critical distance". Suppose that a piece of equipment trips when the voltage drops below a certain level(the critical voltage). The definition of critical distance is such that each fault within the critical distance will cause the equipment to trip. The critical distance has been calculated for different voltage levels, using typical fault levels and feeder impedances. The data used and the results obtained are summarize in Table 3.1 for the critical voltage of 50%. Note how the critical distance increases for higher voltage levels. A customer will be exposed to much more kilometres of transmission lines than of distribution feeder [7].

Table 3.1 Critical distance for faults at different voltage levels

Nominal Voltage	Short-Circuit Level	Feeder Impedance	Critical Distance
400 V	20 MVA	230 $m\Omega/km$	35 m
11 kV	200 MVA	310 $m\Omega/km$	2 km
33 kV	900 MVA	340 $m\Omega/km$	4 km
132 kV	3000 MVA	450 $m\Omega/km$	13 km
400 kV	10000 MVA	290 $m\Omega/km$	55 km

A short circuit in the power system not only causes a drop in a voltage magnitude, but also change in the phase angle of the voltage. This sudden change in phase angle is called a "phase-angle jump". The phase-angle jump is visible in the time-domain plot of the dip as a shift in voltage zero-crossing between the pre-event and the during-event voltage. With reference to Figure 3.1 and (3.1), the phase-angle jump is the argument of $\overline{E}_g$, thus the difference in argument between Z_f and $Z_g + Z_f$. If impedances Z_g and Z_f have equal X/R ratio, there will be no phase-angle jump in the voltage at PCC. The phase-angle jump is given by

$$\psi = \arg(\overline{E}_g) = \arctan\left(\frac{X_f}{R_f}\right) - \arctan\left(\frac{X_f + X_g}{R_f + R_f}\right) \tag{3.4}$$

Depending on the type of fault (three-phase, phase-to-phase with or without ground involved, single-phase to ground), the resulting voltage dip at the PCC can be one of six types reported in Figure 3.2 [8].

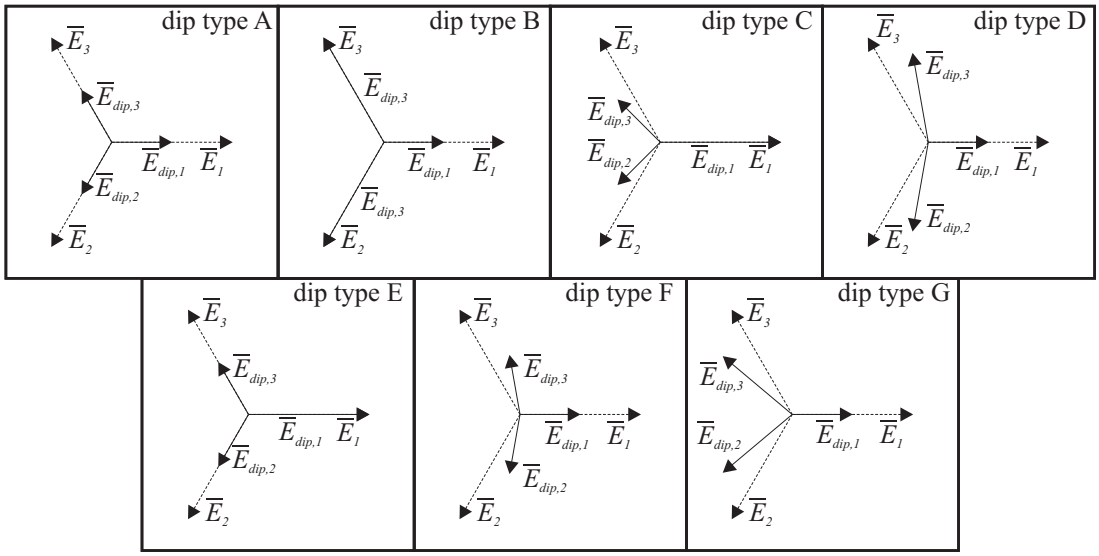

Figure 3.2: Voltage dip classification "A" to "G". Phasors three-phase voltage before (dotted) and during fault (solid) are displayed.

The load is usually supplied through a distribution transformer, connected in Δ/Y. The transformer swaps the phases and removes the zero-sequence component because of the delta connection. This results in a transformation of the dip characteristic as listed in Table 3.1 (right column). It can be concluded that voltage dips that affect the load downstream a Δ/Y-transformer can only be of type A, C, D and F. The voltage dip type A is a drop in a voltage in all three phase (balanced dip). The voltage dip type C is characterized by a drop in two phases with the third phase voltage almost undisturbed. The voltage dip type D is characterized by a larger drop in one phase and smaller drops in the other two phases. The voltage dip type F is in fact a particular case of type C and D [9]. However, in some applications, such as control of VSC connected to the grid, it can be preferable to characterize the voltage dip in terms of the remaining positive-sequence voltage and the unbalance, expressed as magnitude of negative-sequence voltage in percentage of the pre-fault voltage [3]. Therefore, this characterization will not be used in this report.

Table 3.1 Voltage dip classification and propagation through Δ/Y-transformers.

Fault	Dip seen at PCC	Dip seen by the load
3-phase fault	Type A	Type A
1-phase fault	Type B	Type C
2-phase fault	Type E	Type F
phase-to-phase	Type C	Type D

If the voltage amplitude of three phases are unequal, the resulting voltage vector can be expressed as the sum of two vectors interpreted as positive- and negative-sequence component vectors. The magnitude of the positive sequence (E_p) and the negative sequence (E_n) of the grid voltage for dip types "A" through "G" are calculated using synchronous coordinate (see Appendix A.) and summarized in Table 3.3, where is the phase-to-phase RMS grid voltage. It shown that dips "C" and "D" have the same positive and negative sequence magnitudes. The same applies

for dips "E", "F" and "G". However they may affect the system in different ways according to Table 3.4, at which the positive and negative sequence components in the $dq-$coordinate system have been calculated. It shows that dips "C" and "D" result in different negative sequence $dq-$components. The same also holds for dip types "F" and "G", while dips "E" and "G" are exactly the same since they both result in the same positive and negative sequence components. This classification is useful in understanding the effect of unbalanced voltage dips on the system [10].

Table 3.3 Positive and negative sequence magnitudes of grid voltage for dip types "A" through "G".

Dip type	E_p	E_n
A	EE_g	0
B	$\frac{E}{3}\sqrt{4+4E_g\cos\psi+E_g^2}$	$\frac{E}{3}\sqrt{1-2E_g\cos\psi+E_g^2}$
C, D	$\frac{E}{2}\sqrt{1+2E_g\cos\psi+E_g^2}$	$\frac{E}{2}\sqrt{1-2E_g\cos\psi+E_g^2}$
E, F, G	$\frac{E}{3}\sqrt{1+4E_g\cos\psi+4E_g^2}$	$\frac{E}{3}\sqrt{1-2E_g\cos\psi+E_g^2}$

Table 3.4 Positive and negative sequence components of grid voltage in $dq-$coordinates for dip types "A" through "G".

Dip type	e_{dp}	e_{qp}	e_{dn}	e_{qn}
A	$EE_g\cos\psi$	$EE_g\cos\psi$	0	0
B	$\frac{E}{3}(2+E_g\cos\psi)$	$\frac{E}{3}E_g\sin\psi$	$-\frac{E}{3}(1-E_g\cos\psi)$	$-\frac{E}{3}E_g\sin\psi$
C	$\frac{E}{2}(1+E_g\cos\psi)$	$\frac{E}{2}E_g\sin\psi$	$\frac{E}{2}(1-E_g\cos\psi)$	$\frac{E}{2}E_g\sin\psi$
D	$\frac{E}{2}(1+E_g\cos\psi)$	$\frac{E}{2}E_g\sin\psi$	$-\frac{E}{2}(1-E_g\cos\psi)$	$-\frac{E}{2}E_g\sin\psi$
E	$\frac{E}{3}(1+2E_g\cos\psi)$	$\frac{2E}{3}E_g\sin\psi$	$\frac{E}{3}(1-E_g\cos\psi)$	$\frac{E}{3}E_g\sin\psi$
F	$\frac{E}{3}(1+2E_g\cos\psi)$	$\frac{2E}{3}E_g\sin\psi$	$-\frac{E}{3}(1-E_g\cos\psi)$	$-\frac{E}{3}E_g\sin\psi$
G	$\frac{E}{3}(1+2E_g\cos\psi)$	$\frac{2E}{3}E_g\sin\psi$	$\frac{E}{3}(1-E_g\cos\psi)$	$-\frac{E}{3}E_g\sin\psi$

3.2 Voltage dip mitigation

There are various mitigation methods for the voltage dip. Thus we can distinguish three main categories:

- Power System Improvements
- Increasing Equipment Immunity
- Mitigation Devices

3.2.1 Power System Improvements

Power system improvements include the mitigation through intervention on the power system, considering both changes in the electrical components of the system and in its structure.

Reducing the number of faults Reducing the number of short-circuits in a system not only reduces the dip frequency, but also the frequency of long interruptions. This is thus a very effective way of improving the quality of the supply and many customers suggest this as the obvious solution when a voltage dip problem occurs [7]. Fault prevention actions may include the institution of tree trimming policies, the addition of lightning arresters, insulator washing and the addition of animal guards. Insulation on transmission systems cannot withstand the most severe lightning strokes, but lines which are often subject to lightning-induced faults should be carefully investigated for improvement of the insulation level. Faults due to lightning can be reduces by lowering the ground resistance at the foot of the tower for overhead static wires. Other measures include the use of recently introduced special wires, which are covered by a thin layer of insulation material, or the installation of additional shielding wires, placed in such a way that they are more likely to be hit by a lightning stroke than the phase conductors. A considerable reduction in the number of faults per year can otherwise be achieved by replacing overhead lines by underground cables, which are less affected by adverse weather. The fault rate of an overhead line is much higher than that of an underground cable, but in case of fault the repair time of the latter is longer [11].

Changing the power system By implementing changes in the supply system, the severity of the event can be reduced. However, the costs may become very high, especially for transmission and subtransmission voltage levels. In industrial systems, such improvements more often outweigh the costs, especially when already included in the design stage. Some examples of mitigation methods are given in [7]. Other improvements in the power system design include:

- Install a generator near the sensitive load. The generators will keep up the voltage during a dip. The reduction in voltage drop is equal to the percentage contribution of the generator station to the fault current.

- Split buses or substations in the supply path to limit the number of feeders in the exposed area.
- Install current-limiting coils at strategic places in the system to increase the electrical distance to the fault. The drawback for this method is that this may make the event worse for other customers.
- Feed the bus with sensitive equipment from two or more substations. A voltage dip in one substation will be mitigated by the in feed from the other substations. The more independent the substations are, the more mitigation effect.

Reducing the fault-clearing time Reducing the fault clearing time does not reduce the depth of the dips, but only their duration. The ultimate reduction of fault clearing time is achieved by using current-limiting fuses or modern static circuit breakers, able to clear a fault within half-cycle. Additionally, several types of fault-current limiters have been proposed that do not actually clear the fault, but significantly reduce the fault current magnitude within one or two-cycles. One important restriction of all these devices is that they can only be used for low- and medium-voltage levels systems. The maximum operating voltage is a few tens of kilovolts [7]. The fault-clearing time is not only the time needed to open the breaker, but also the time needed for the protection to make a decision. To achieve a proper reduction in fault-clearing time, it is necessary to reduce any grading margins, thereby possible allowing for a certain loss of selectivity. Some caution has to be taken, however, when applying these new protection devices in existing distribution systems. If only some of the protective devices were replaced with fast acting breakers, it would not be possible to co-ordinate them with previously existing downstream protective devices [11].

3.2.2 Increasing Equipment Immunity

Case studies and power quality surveys show that sensitive equipment include both low-power electronics (computers, process-control devices, consumers-electronics) and high-power electronics (for AC and DC drives). It has been reported that an installation using only electromechanical control could tolerate a dip down to 60% voltage without problems, while a completely automated factory could be disrupted by a dip to 85% [11]. Improvement of equipment voltage tolerance thresholds appears at the most effective solution against voltage dips in the long term. This is especially true for short-duration and shallow dips which can hardly be mitigated by means of the utility-side solutions. Unfortunately, customers can only require a specific voltage tolerance level for very large industrial equipment, and these are usually tailored for specific applications. In most cases, the customer has no direct contact with the manufacturer and can in no way intervene to modify equipment sensitivity to voltage disturbances [11].

3.2.3 Mitigation Devices

Customer solutions usually involve power conditioning for sensitive loads. Different devices are currently available for the mitigation of power quality problems. The installation of these devices is getting more and more popular among industrial customers due to the fact that it is that only place where the customers has control over the situation. There are several methods that can be used.

Motor-generator sets Motor-generator sets stores energy in a flywheel. It consists of a motor supplied by the grid, a synchronous generator supplying the load and the flywheel, all connected to the common axis (as shown in Figure 3.3). The rotational energy stored in the flywheel can be used to perform steady-state voltage regulation and to support voltage during disturbances. This system has high efficiency, low initial costs and enables long-duration ride through (several seconds) but can only be used in industrial environments, due to its size, noise and maintenance requirements [11].

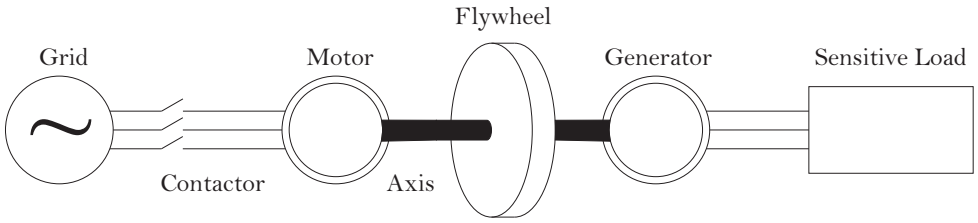

Figure 3.3: Three-phase diagram of motor-generator set with flywheel to mitigate voltage dips.

Transformer-based mitigation devices A Constant Voltage, or ferro-resonant, Transformer (CVT) works in a similar manner to a transformer with a 1:1 turns ratio which is excited at a high point on its saturation curve, thus providing an output voltage which is not affected by input voltage variations. In the actual design, as shown in Figure 3.4 , a capacitor is needed to set the operating point above the knee of saturation curve during normal operation. This solution is suitable for low-power, constant loads: variable loads can cause problems, due to the presence of this tuned circuit on the output.

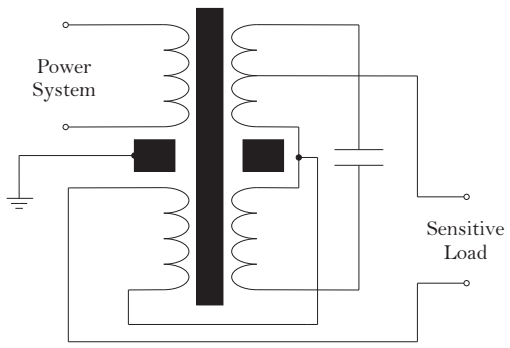

Figure 3.4: Typical circuit for a ferro-resonant transformer.

Electronic tap changers (Figure 3.5) can be mounted on a dedicated transformer for the sensitive load, in order to change its turns ratio according to change in the input voltage. They can be connected in series the distribution feeder and placed between the supply and the load. Part of the secondary winding supplying the load is divided into a number of sections, which are connected or disconnected by fast static switches, thus allowing regulation of the secondary voltage in steps. This should allow the output voltage to be brought back to a level above 90% of the nominal value, even for severe voltage dips. Thyristor-based switches which can only be turned on once per cycle are used, therefore the compensation is accomplished with a time delay of at least one half cycle.

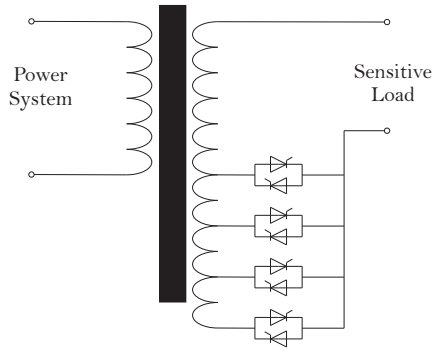

Figure 3.5: Transformer with electronic tap changers.

Autotransformer Switched by Hysteresis Voltage Control AC converters consist of two solid-state switches per phase and require reactive elements such as a capacitor and an inductor. Since the current in the AC converters flows in both directions, static switches and diodes are serially connected to allow both directions current. A new compensation scheme with a new control method is used [12]. The scheme configuration is shown in Figure 3.6. In this configuration an autotransformer is used as a boosting transformer instead of a two-winding transformer. The autotransformer does not offer electrical isolation between primary side and secondary side but has advantages of high efficiency with small volume.

This voltage dip supporter works for only a few seconds and remains in the off-state most of its operation time. Since the switch remains in the off-state for most of the time and must withstand the voltage across it. Therefore, the voltage across the switch becomes an important factor. The voltage across the switch in the off-state is equal to one half of the input voltage.

The model consists of the single IGBT switch in a bridge configuration, a thyristor bypass switch, output filters, an autotransformer, and the system controller. In normal conditions, the IGBT switch is off and the power flows through anti-parallel thyristor as a bypass switch. This bypass switch connects the input power to the load unless the dip condition is present. When voltage dip occurs, the bypass switch turns off and the switching command turns on the IGBT switch. Utilizing autotransformer, the IGBT improves the output voltage in such a way that the voltage

across the load remains constant.

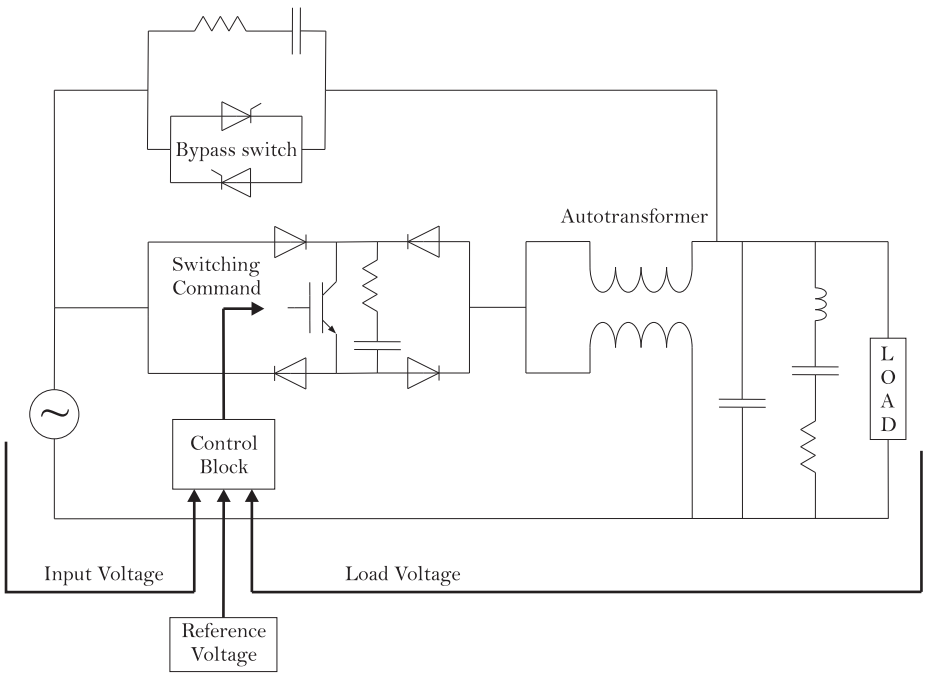

Figure 3.6: Overall structure of voltage dip compensator.

To prevent the switching noise effect of IGBT and thyristor on the load current and voltage waveforms, two filters (a capacitor filter and a notch filter) utilized. To keep the power switches safe, an RC snubber circuit is designed. The snubber circuit of IGBT switch consists of a resistor and a capacitor. The snubber suppresses the peak voltage across the IGBT switch when the IGBT turns off. When the IGBT switch turns off, the current flowing in the IGBT in the on-state instantly diverts to the snubber circuit. The energy stored in the current path is transferred into the snubber capacitor and resistor.

Static Transfer Switch The Static Transfer Switch (STS) consists of two three-phase static switches, each constituted in turn of two antiparallel thyristor per phase, as shown in Figure 3.7, where the single-line diagram of an STS is displayed [3]. The usual configuration of the STS, shown in Figure 3.7, consists of [1]:

- two three-phase static switches, each constituted in turn by by two-antiparallel thyristors per phase, which actually perform the fast transfer of power between the two sources;
- two three-phase mechanical bypass switches, which are operated as standard mechanical switches to perform a slower back-up transfer, when the STS cannot operate due to overload conditions or when it is out of service for maintenance or testing;
- isolating switches, needed to disconnect the STS from the distribution system for maintenance and testing.

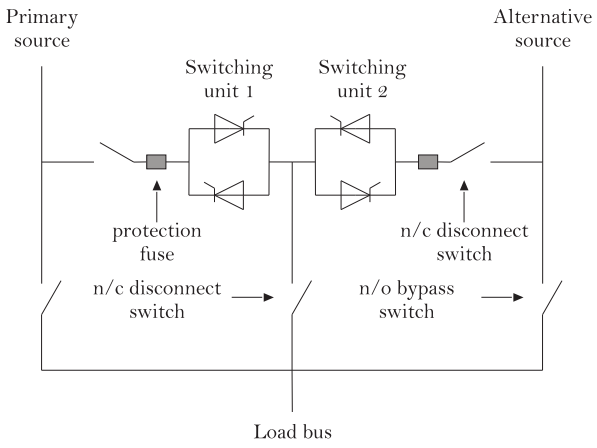

Figure 3.7: Single-line diagram of Static Transfer Switch (STS).

The STS has to transfer the load from the preferred source to the alternative source automatically and rapidly when a reduced voltage is established in the preferred source and while the alternative source meets certain quality requirements. Formerly available only for low voltages, STS systems are now advertised for higher voltages and protected load ratings, which make them for high-power industrial applications: they would be capable to protect loads up to 35 MVA supplied at a voltage of 35 kV. Ratings of a commercial STS are reported in Table 3.5 [1]

Table 3.5 Ratings of commercial STS system.

Model	Voltage Class	Continuous Current Rating	Power
DSTSIS200	15 kV	200 kA	5 MVA
DSTSIS600	15 kV	600 kA	15 MVA
DSTS2S200	25 kV	200 kA	8 MVA
DSTS25600	25 kV	600 kA	26 MVA
DSTS35200	35 kV	200 kA	11 MVA
DSTS3S600	35 kV	600 kA	35 MVA

Transfer under normal operating conditions may also be needed in particular cases and must be allowed. However, the need for transfer usually arises because of an upstream fault causing a reduction of the preferred source voltage for a limited time interval, after which the load is switched back to the main supply. It has been observed that, with this arrangement, the load current flows continuously through the thyristors and this causes high losses and heating [13].

Uninterruptible Power Supply An Uninterruptible Power Supply (UPS) consists of a diode rectifier followed by an inverter, as shown in Figure 3.8 [3] [11]. The energy storage is usually a battery connected to the DC link. During normal operation, the power coming from the AC supply is rectified and then inverted to feed the load. The battery remains in standby mode and only keeps the DC-bus voltage constant. During a voltage dip or an interruption, the energy released by the battery

keeps the voltage at the DC bus constant. Depending on the storage capacity of the battery, it can supply the load for minutes or even hours. Low cost, simple operation and control have made the UPS the standard solution for low-power, single phase equipment, like computers. For higher-power loads the costs associated with losses due to the two conversions and maintenance of the batteries become too high and, therefore, a three-phase, high power UPS is not economically feasible.

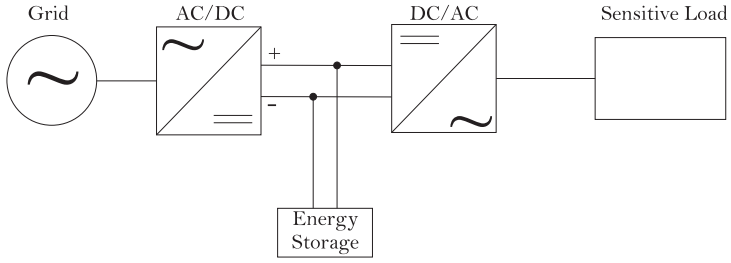

Figure 3.8: Single-line diagram of Uninterruptible Power Supply (UPS).

Series-connected VSC The basic idea is to inject a voltage $\underline{e}_c(t)$ of desired amplitude, frequency and phase between the PCC and the load in series with the grid voltage. A single-phase diagram of the main components of the SSC is depicted in Figure 3.10. The SSC injects by means of three single-phase transformers three voltages in the grid, synchronized in such a way that the load voltage magnitude and phase are constant at any instant to maintain the operation of the load [14].

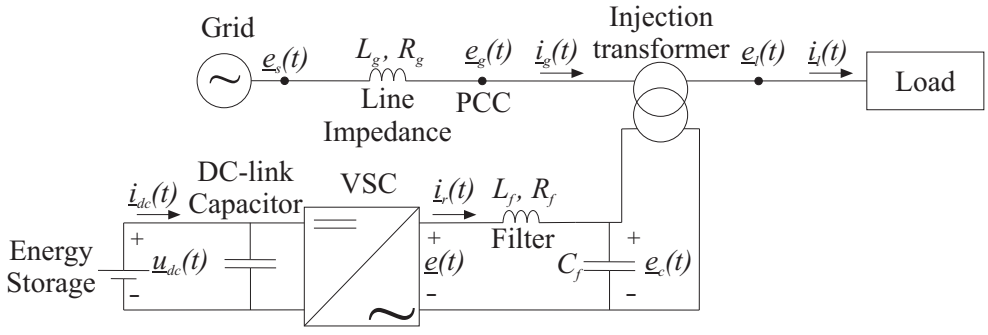

Figure 3.9: Single-line diagram of SSC.

The SSC in mainly used for voltage dip mitigation. The device maintains the load voltage $\underline{e}_l(t)$ to the pre-fault condition by injecting a voltage of appropriate amplitude and phase. Figure 3.11 shows the phasor diagram of the series injection principle during voltage dip mitigation, where $\overline{E}_c$ is the phasor of the voltage injected by the compensator, $\overline{I}_l$ is the phasor of the load current and where φ is the angle displacement between load voltage and current, $\overline{E}_{g,dip}$ is the grid voltage phasor during the dip and ψ is the phase angle jump.

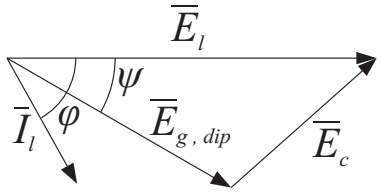

Figure 3.10: Mitigation of voltage dips using SSC.

The dynamic performance of the SSC is important to start compensation without a sensible delay. Thus, the response time of the dip detection and voltage compensation must be short; consequently, the bandwidth of the control algorithm should be high.

In the single-line diagram of the SSC, shown in Figure 3.10, the grid voltage, current and angular frequency are denoted by $\underline{e}_g(t), \underline{i}_g(t)$ and ω, respectively. R_g and L_g denote the equivalent resistance and inductance of the grid, $\underline{u}(t)$ and $\underline{i}_r(t)$ are the voltage and current of the VSC. The load voltage is denoted by $\underline{e}_l(t)$. At the point of common coupling (PCC), the SSC is connected to the power system. The LC-filter consists of a series inductor with inductance L_f and resistance R_f and a shunt capacitor with capacitance C_f. The energy storage provides the required power to compensate the identified voltage dip.

In order to be able to restore both magnitude and phase of the load voltage to the pre-fault conditions, the SSC has to inject both active and reactive power [3]. Assuming that the load voltage and the current in pre-fault condition are both equal to 1 pu, the power injected by the device during voltage dip mitigation is equal to

$$\begin{aligned} \overline{S}_{inj} = \overline{E}_c \overline{I}_l^* = (\overline{E}_l - \overline{E}_{g,dip})\overline{I}_l^* = (1 - \overline{E}_{g,dip} e^{\jmath\psi}) e^{\jmath\varphi} = \\ = \cos\varphi + \jmath \sin\varphi - (E_{g,dip}\cos(\varphi+\psi) + \jmath E_{g,dip}\sin(\varphi+\psi)) \end{aligned} \tag{3.5}$$

Observe that the power absorbed by the load is given by

$$\overline{S}_{load} = P_{load} + \jmath Q_{load} = \overline{E}_l \overline{I}_l^* = e^{\jmath\varphi} = \cos\varphi + \jmath\sin\varphi \tag{3.6}$$

Therefore, the active and reactive power injected by the SSC are given by

$$P_{inj} = \left[1 - \frac{E_{g,dip}\cos(\varphi+\psi)}{\cos\varphi}\right] P_{load} \tag{3.7}$$

$$Q_{inj} = \left[1 - \frac{E_{g,dip}\sin(\varphi+\psi)}{\sin\varphi}\right] Q_{load} \tag{3.8}$$

Figure 3.12 and 3.13 display the active and the reactive power injected by the SSC during voltage dip mitigation for different phase-angle jump (0°, 15°, 30°, 45°) under the assumption of load impedance $\overline{Z}_l$ equal to 1 pu with power factor 0.8 inductive.

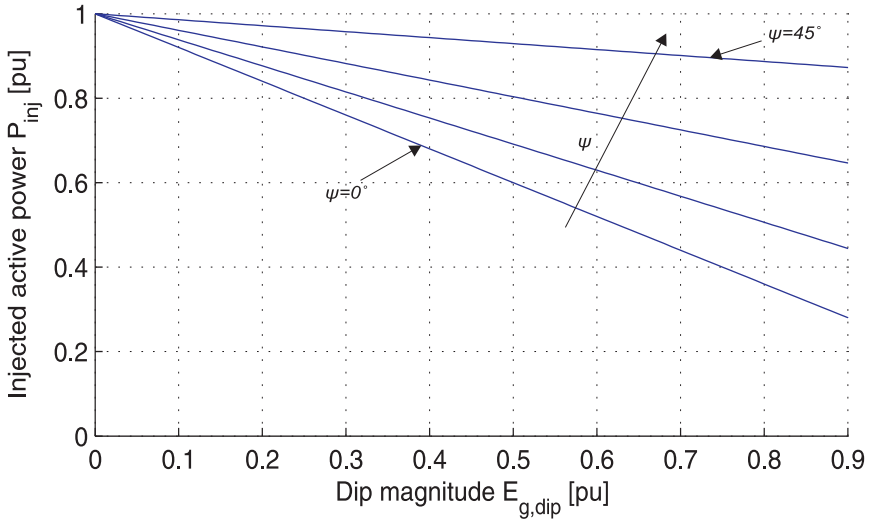

Figure 3.11: Active power injected vs. dip magnitude during voltage dip mitigation for different phase-angle jump.

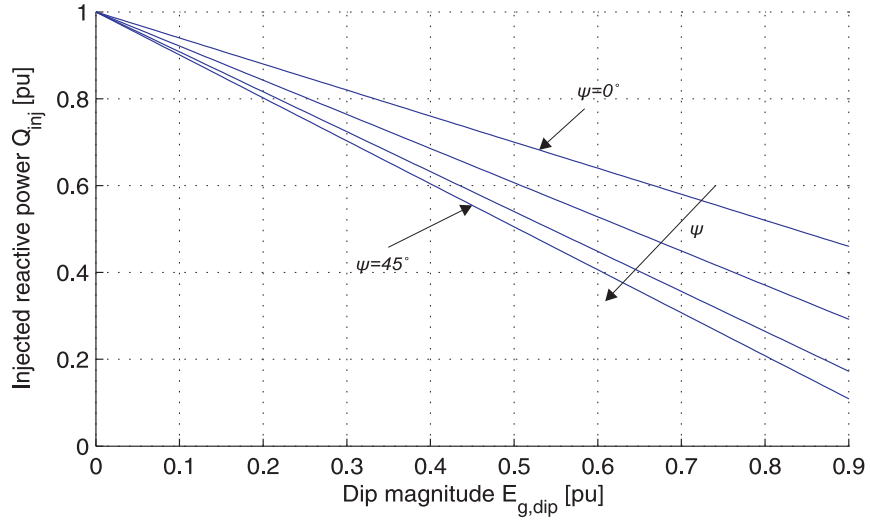

Figure 3.12: Reactive power injected vs. dip magnitude during voltage dip mitigation for different phase-angle jump.

The maximum injected voltage is limited by the size of the converter and the rating of the series transformer. The voltage rating of the converter is chosen on the basis of the maximum dip to compensate for. Existing SSCs are usually sized for 50% maximum voltage injection with duration of 500 ms.

Shunt-connected VSC The typical configuration of a shunt-connected VSC with energy storage (as seen also called E-STATCOM) is shown in Figure 3.14. The device consists of a VSC, an injection transformer, an AC filter and a DC-link capacitor.

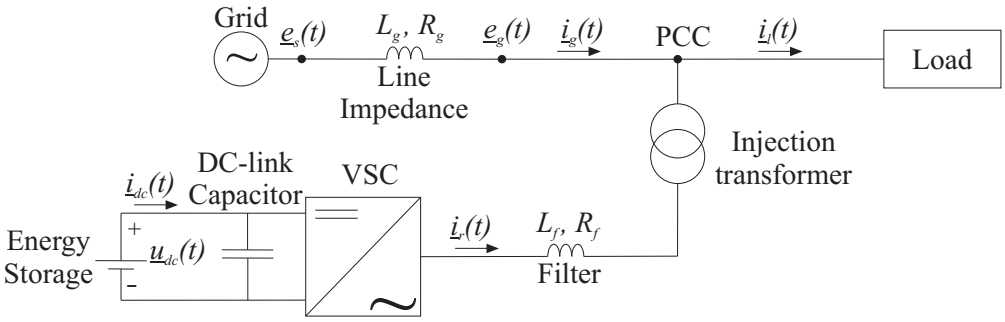

Figure 3.13: Single-line diagram of shunt-connected VSC.

The grid voltage and current are denoted by $\underline{e}_s(t)$ and $\underline{i}_g(t)$, respectively. The voltage at the point of common coupling (PCC), which is also equal to the load voltage, is denoted by $\underline{e}_g(t)$ and the load current by $\underline{i}_l(t)$.

The converter acts as a controllable current source connected in parallel with the load. The system can instantaneously compensate voltage dips by regulating the load voltage using the injected current from the converter and the voltage drop across line inductance, as shown in the phasor diagram in Figure 3.15. The voltage phasor at PCC is denoted by $\overline{E}_g$, Z_g is the line impedance, $\overline{E}_{g,dip}$ is the grid voltage phasor during the dip and ψ is the phase-angle jump of the dip.

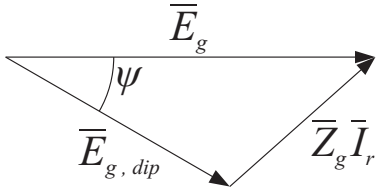

Figure 3.14: Mitigation of voltage dips using shunt-connected VSC.

From the diagram it is possible to understand that when the shunt-connected VSC is used to mitigate voltage dips, it is necessary to provide an energy storage for injection of active power in order to avoid phase-angle jumps of the load voltage. If only reactive power is injected, it is possible to maintain the load voltage amplitude $\overline{E}_g$ to the pre-fault conditions but not its phase. Therefore, the voltage dip mitigation capability of a shunt-connected VSC depends on the rating of the energy storage, on the grid impedance Z_g and on the rating in current of the VSC. To restore the load voltage to the pre-fault conditions (without introducing phase-jump), the following condition must be fulfilled [3]

$$\overline{E}_g = \overline{E}_{g,dip} + \overline{Z}_g\overline{I}_r \tag{3.9}$$

Observe that if the line impedance is small to achieved the mitigation the current $\underline{i}_r(t)$ must be big (major cost of the system), instead if the line impedance is big to

achieve the mitigation the current $\underline{i}_r(t)$ must be small (minor cost of the system). But if the line impedance is big, the voltage at PCC will be more variable with the consequence that the system will be more sensitive by the faults. Active and the reactive power injected by the device can be calculated in per unit as

$$P_{inj} = \frac{\cos\varphi_l}{Z_l} - \frac{E_s(E_{s,dip}\cos(\varphi_g - \varphi_s) - \cos(\varphi_g - \varphi_s + \psi))}{E_{s,dip}Z_g} \tag{3.10}$$

$$Q_{inj} = -\frac{\sin\varphi_l}{Z_l} + \frac{E_s(E_{s,dip}\sin(\varphi_g - \varphi_s) - \sin(\varphi_g - \varphi_s + \psi))}{E_{s,dip}Z_g} \tag{3.11}$$

where the source voltage, the load impedance and the line impedance are expressed as $\overline{E}_s = E_s e^{\jmath\varphi_s}$, $Z_l = Z_l e^{\jmath\varphi_l}$ and $Z_g = Z_g e^{\jmath\varphi_g}$, respectively.

Figures 3.16 and 3.17 show the amount of active and reactive power, respectively, injected by the shunt-connected VSC to maintain the voltage at its pre-fault value. In order to compare the SSC and the E-STATCOM, we consider the case of mitigation of voltage dips with magnitude higher than 50% (i.e., the remaining voltage is equal or higher than 50% of the rated voltage). The load impedance Z_l has been set to 1 pu with power factor of 0.8, while different values for the line impedance Z_g (from 0.1 pu to 0.5 pu in steps of 0.1 pu) have been considered. For the grid impedance, it has been assumed that X_g=0.995Z_g and $R_g = 0.1X_g$, which results in an impedance angle of 84.29°. It is interesting to observe that, since the line impedance is mainly reactive ($R_g < X_g$), the amount of active power injected is significantly smaller than the reactive power. Moreover, the injected power increases for smaller values of the line impedance. This is not surprising, since smaller line impedance means a stronger grid. Thus, it will be necessary to inject a larger amount of current to increase the voltage at the PCC.

As it is possible to observe, the amount of reactive power is bigger than the use of SSC. Actually if the grid impedance is equal to 0.1 pu the amout of reactive power required is not smaller than 1.0 pu.

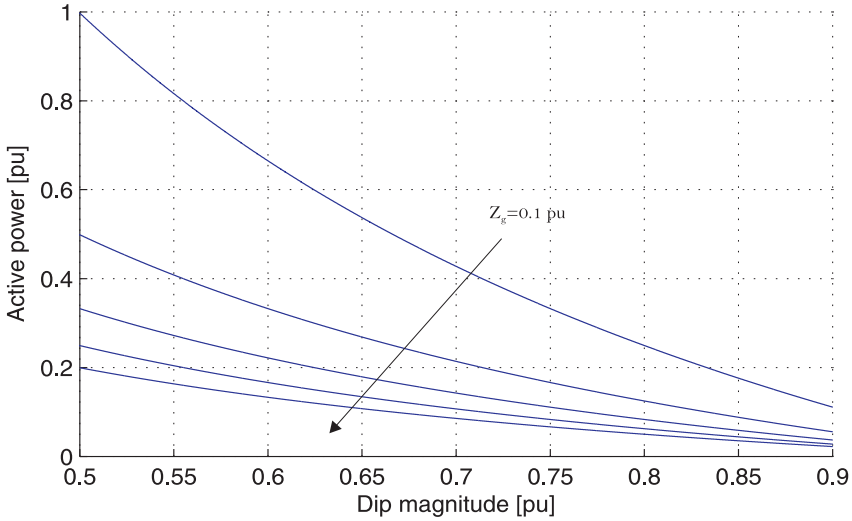

Figure 3.15: Active power injected by shunt-connected VSC vs. dip magnitude during voltage dip mitigation for different line impedances $\overline{Z}_g$.

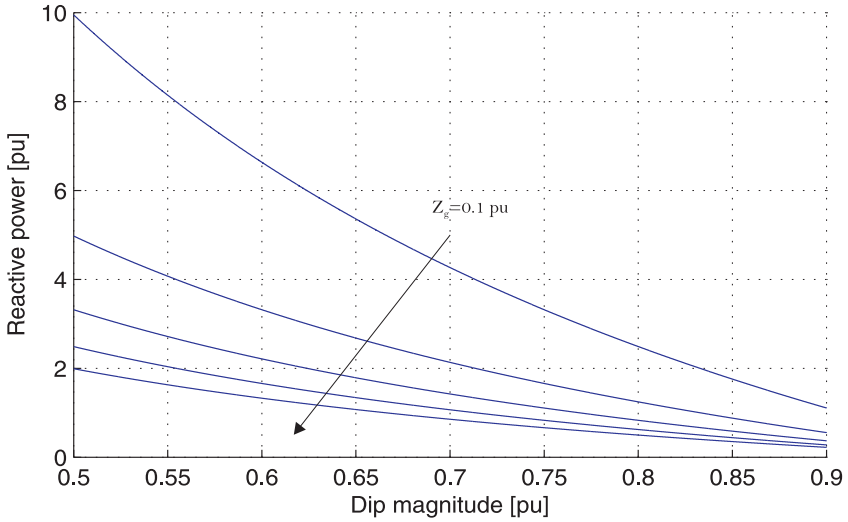

Figure 3.16: Active power injected by shunt-connected VSC vs. dip magnitude during voltage dip mitigation for different line impedances $\overline{Z}_g$.

3.3 Conclusion

In this chapter, a brief overview of voltage dips, with their origin and classification has been given. Different methods for voltage dip mitigation have been described. The installation of mitigation devices at the system-equipment interface appears as the most attractive short-term solution for customers, who rarely have the chance to request either specific tolerance levels for equipment or an improved power supply. A summary of the cost and capability of the most common devices is shown in Table 3.3 [15].

Table 3.3 Comparison of Custom-Power Equipment for Correcting Dips.

Device	Cost, U.S. $	Capability
Shunt-connected VSC	50-200 $/kVA$	dips to 70%
Static transfer switching	500-1000 $/A$	
Series-connected VSC	150-250 kVA	dips to 50%
UPS	750-1500 kVA	

Among the mitigation methods presented, the use of custom power devices seems the most efficient. In particular among the custom power the SSC is the most used for voltage dip mitigation. But the use of SSC presents some problems.

If a fault occurs at downstream of the device, the fault current goes through the VSC, therefore the components must be designed properly considering these events. Another problem is due to the transformer saturation. When a voltage dip is detected, the SSC injects a voltage into the mains by applying a voltage on the secondary side of the injection transformer. The flux in the injection transformer is constituted by an AC term that varies with the grid frequency and a DC term that depends on the angle of the grid voltage at the beginning of the dip. If the initial phase of the injected voltage is equal to $\pi/2 + n\pi$, with n any integer, the transformer flux can reach up to twice the steady-state value. Therefore, if the transformer is not properly designed, saturation can occur and the magnetizing current can become very large. As a result, the VSC can be damaged due to overcurrent. To avoid saturation under all conditions, the transformer has to be sized to handle two times the normal steady-state flux requirement at maximum RMS injection voltage without saturating [16]. Another problem is that if during the dip a feeder, where there is the sensitive load, is open by the protection, SSC can't work not supplying the sensitive load.

The E-STATCOM does not have all these problems. It is mainly used as a active filter, but if the cost of the power electronic components will became smaller than today and if the power required by the E-STATCOM will be easily available, this system can replace the SSC for voltage dip mitigation.

In the next chapter, the E-STATCOM, and especially its control system, will be described in detail.

Chapter 4

Control System for Shunt-Connected VSC

4.1 Introduction

In the previous chapter, different voltage dip mitigation methods have been described. In this chapter a specific on about the control system for Shunt-Connected VSC for voltage dips mitigation will be carried out. The control system consists of two controllers: a vector current-controller and a vector voltage-controller. These controllers will be connected in cascaded under the assumption that the inner loop (vector current controller) is much faster than the outer loop (vector voltage controller). Stability analysis considering the impact of the controller bandwidths and the impact of the model parameters will be carried out.

Improvements of the standard control system in order to control positive and negative sequence independently will be presented by a dual vector current- and voltage-controller.

4.2 Description of electrical system

To derive the control system, it is necessary to describe how the shunt-connected VSC acts to mitigate voltage dips. The electrical system is shown in Figure 4.1. The grid voltages are denoted by $e_{sa}(t)$, $e_{sb}(t)$ and $e_{sc}(t)$. The line impedance is modelled as a resistance R_g and inductance L_g. The voltages at the point of common coupling (PCC) are denoted by $e_{ga}(t)$, $e_{gb}(t)$ and $e_{gc}(t)$. The injection transformer impedance has a resistance R_{tr} and inductance L_{tr}. The inductance and resistance of the AC-filter reactor are denoted by R_f and L_f respectively. A capacitor C is added in between the filter reactor at the VSC output and the transformer, with the twofold purpose of making the voltage at the PCC more stable and filtering the harmonic voltage components in the VSC output voltage.

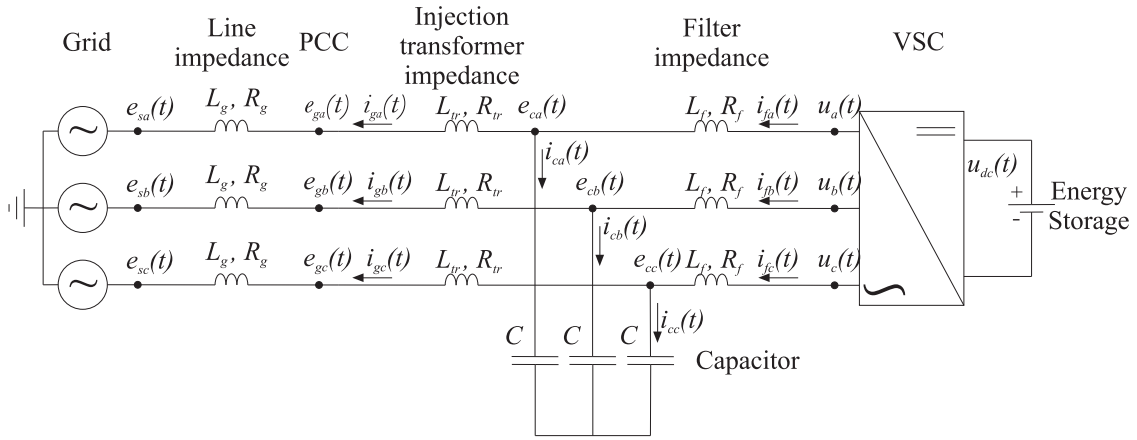

Figure 4.1: Main electrical circuit of Shunt-connected VSC.

As a result, the filter inductor, the capacitor and the transformer inductor make an LCL-filter. The control objective is to maintain the voltage at the PCC constant. By observing the electrical scheme, if the transformer impedance is neglectable, it is possible to reach this purpose by maintaining the voltage across the capacitor constant.

Figure 4.2 shows a three-phase VSC. The valves in the phase-legs of the VSC (usually insulated gate bipolar transistors, IGBTs) are controlled by the switching signals $sw_a(t)$, $sw_b(t)$ and $sw_c(t)$. The DC-link voltage is denoted by $u_{dc}(t)$. The switching signal can be equal to ± 1. When $sw_a(t)$ is equal to 1, the upper valve in the phase a is turned on while the lower valve in the same leg is off. Therefore, the potential $v_a(t)$ is equal to half of the DC-link voltage ($u_{dc}(t)/2$). Vice versa, when the switching signal is equal to -1, the upper valve is off and the lower one is on and, thus, $v_a(t)$ is equal to $-u_{dc}(t)/2$.

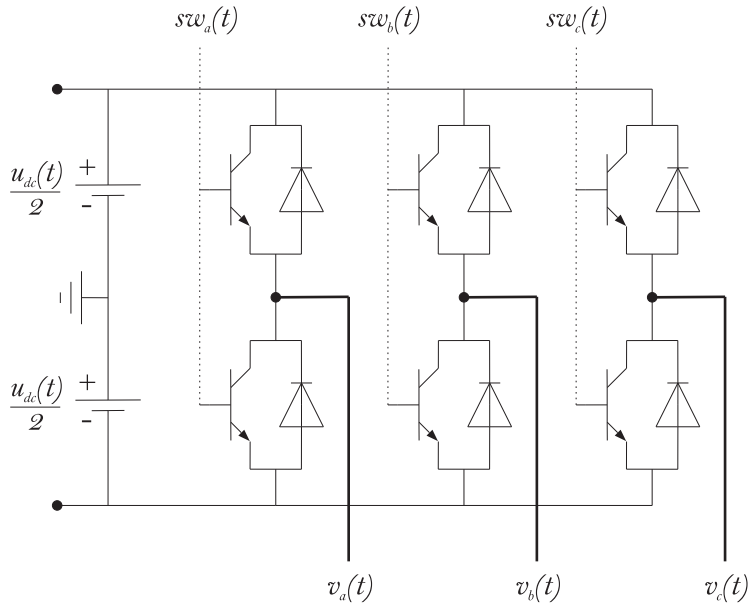

Figure 4.2: Three-phase Voltage Source Converter (VSC).

It is possible to describe the three-phase system of the inverter output voltage as an equivalent two-phase system, with two perpendicular axes, denoted as α and β. It is convenient to consider these axes as the real and imaginary axes in a complex plane. With the complex two-phase representation, the three-phase/two-phase transformation is given by

$$\underline{v}^{(\alpha\beta)}(t) = v_\alpha + \jmath v_\beta = K\left(v_a + v_b e^{\jmath\frac{2\pi}{3}} + v_c e^{\jmath\frac{4\pi}{3}}\right) \tag{4.1}$$

where K is a scaling constant. The complex quantity $\underline{v}^{(\alpha\beta)}(t)$ is called space vector. The scaling constant K can be chosen arbitrarily. Depending on the application, one choice can be more convenient than another. There are three standard selections (Appendix A); in this work K is equal to $\sqrt{3/2}$ (power-invariant transformation). The three switching signals sw_a, sw_b and sw_c can be combined in eight ways. The resulting voltage vectors for these combinations draw a hexagon in $\alpha\beta$ plane. Figure 4.3 shows the eight realizable voltage vectors and their switching combinations for the two level VSC. As an example, a vector $\underline{v}(sw_a, sw_b, sw_c)$ with switching states $sw_a = 1$, $sw_b = -1$ and $sw_c = 1$ is represented as (1,-1,1). Due to the selected parameter K, the maximum modulus of the voltage vector is

$$\underline{v}(t) = \sqrt{\frac{2}{3}} \cdot u_{dc} \tag{4.2}$$

which is attained for all switching states except (1,1,1) and (-1,-1,-1), which both yield to the zero vector. The maximum sinusoidal output voltage of the VSC corresponds to the maximum circle inside the hexagon. The radius of the circle is the maximum line-to-line voltage

$$|\underline{v}_{max}| = |\underline{v}| \cos\left(\frac{\pi}{6}\right) = \sqrt{\frac{2}{3}}\frac{\sqrt{3}}{2} \cdot u_{dc} = \frac{u_{dc}}{\sqrt{2}} \approx 0.707 u_{dc} \tag{4.3}$$

To obtain the switching signals for the VSC, Pulse Width Modulation technique (PWM) has been adopted. The maximum output voltage amplitude from the VSC when using sinusoidal PWM is given by [17]

$$\underline{v}(t) = \sqrt{\frac{2}{3}} \cdot \frac{u_{dc}}{2} \approx 0.61 u_{dc} \tag{4.4}$$

shown in Figure 4.3 with the dot circle.

Therefore, by using PWM the VSC it is not utilized to its maximum. It is possible to use several methods for increasing the maximum output voltage with the same DC-Link. As an example, waveforms of zero-sequence can be added to the sinusoidal reference voltage to the PWM. One common choice is to add a 3rd harmonic of 25% the amplitude of the fundamental frequency component to all reference signals [18].

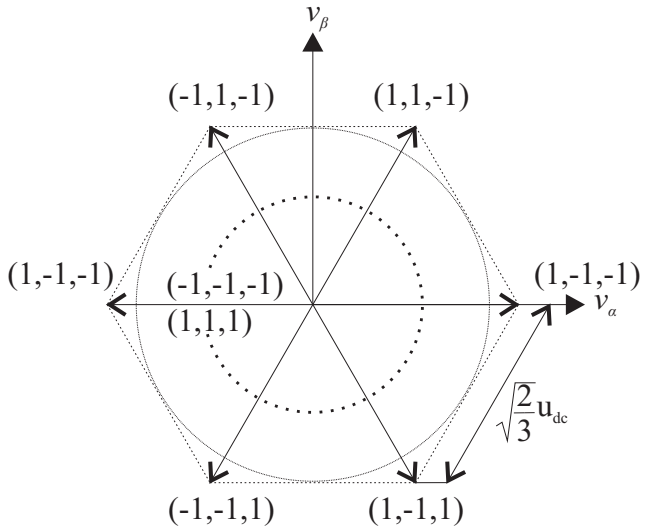

Figure 4.3: Space-vector diagram.

The following figure shows the method used to increase the maximum output voltage.

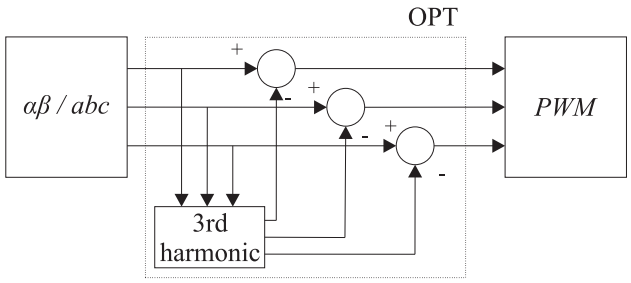

Figure 4.4: Block diagram for increasing the maximum output voltage.

The 3rd harmonic is calculated

$$H_3 = \frac{\max(u_a^*, u_b^*, u_c^*) + \min(u_a^*, u_b^*, u_c^*)}{2} \tag{4.5}$$

If the same deviation H_3 is subtracted from all reference signals (Figure 4.5), a zero-sequence component is added. The resulting three-phase voltages are depicted in Figure 4.6. It is possible to observe that the maximum output voltage increases by 15.5% without increasing the DC-link. The principle drawback of this method is that a 3rd harmonic is injected into the grid. This is avoided by not connecting the AC side of the VSC to ground.

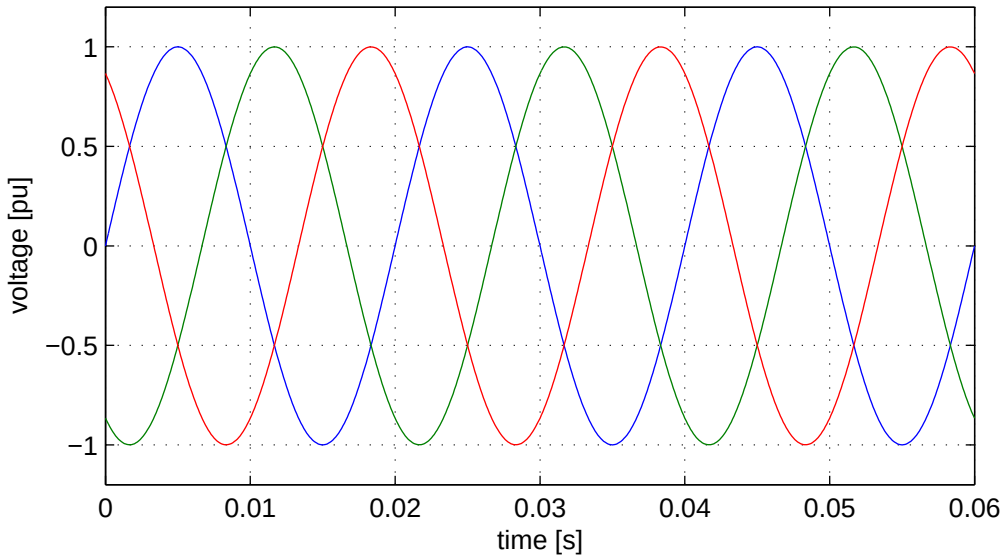

Figure 4.5: Three-phase voltage system without 3rd harmonic injection.

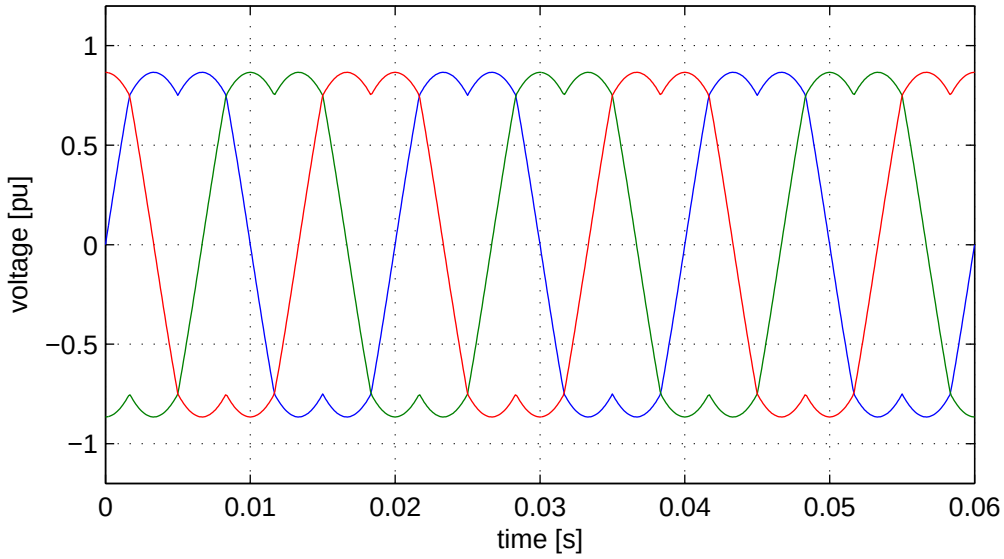

Figure 4.6: Three-phase voltage system with 3rd harmonic injection.

4.3 Control System

As mentioned earlier in this chapter, the control system consists of two controllers: a vector current-controller and a vector voltage-controller. These controllers will be connected in cascaded under the assumption that the inner loop (vector current controller) is much faster then the outer loop (vector voltage controller). The vector voltage controller produces a reference signal proportional to the output VSC current in order to maintain the voltage above the capacitor constant to the desired value, while the vector current controller produces a reference signal proportional to the VSC output voltage in order to track the reference VSC output current. Figure 4.7 shows the block diagram of the implemented control system.

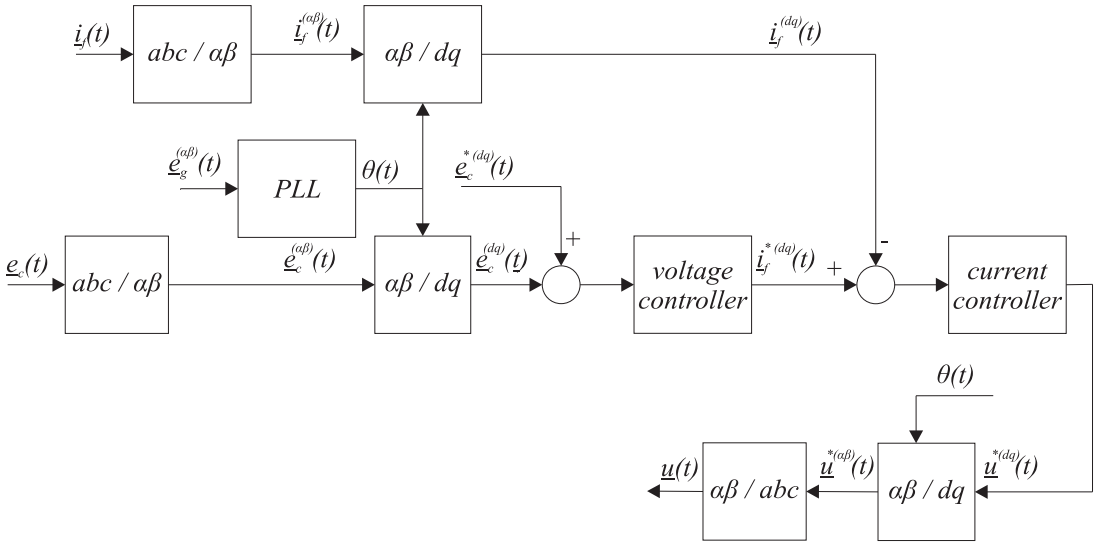

Figure 4.7: Block diagram of the implemented control system.

The control system will be derived in the synchronous coordinate, applying the equations in Appendix A. In this way a three-phase system can be expressed by a two-phase system whose components will appear as DC quantities, in steady-state. As seen in Appendix A in order to obtain the $dq-$ coordinates, voltages and currents will be transformed to fixed coordinate $\alpha\beta$ and then to synchronous coordinate $dq-$. To calculate the $dq-$ coordinates it is necessary calculate the transformation angle θ(t) (Figure 4.8) that will be calculate with a Phase-Looked Loop (PLL).

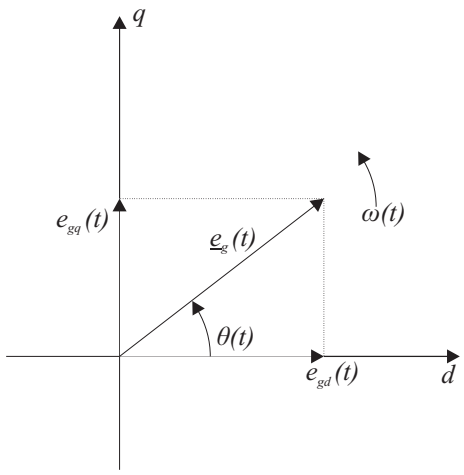

Figure 4.8: Vector $\underline{e}_g(t)$ in $dq-$ coordinates.

The dq transformation is not only useful for analysis, but also for implementation of control algorithms, since it is easier to design controllers for DC quantities instead of AC quantities.

One of the most important advantages in using DC quantities is for correct operations of PI controller. The transfer function of a the PI controller is given by

$$G(s) = k_p + \frac{k_i}{s} \tag{4.6}$$

where k_p is the proportional gain and k_i is the integral gain.
The proportional gain acts like a simple amplitude gain and it works properly at any frequency. The integral gain works properly only with DC quantities. To have an idea of the integral response, we can consider the block diagram shown in Figure 4.9. The error ε is given by

$$\varepsilon = u - \varepsilon(\frac{1}{s}) \Rightarrow u = \varepsilon\left(1 + \frac{1}{s}\right) = \varepsilon\left(\frac{s+1}{s}\right) \tag{4.7}$$

thus the transfer function between the input and the error $G(s)$ is given by

$$G(s) = \frac{\varepsilon}{u} = \frac{s}{s+1} \tag{4.8}$$

By applying a unitary step input and a unitary ramp input, the final values of the error $\varepsilon(t)$ are given respectively by

$$\varepsilon(\infty) = \lim_{t\to\infty} u(t)G(t) = \lim_{s\to 0} s \cdot u(s)G(s) = \lim_{s\to 0} s\frac{1}{s}\frac{s}{s+1} = 0 \tag{4.9}$$

$$\varepsilon(\infty) = \lim_{t\to\infty} u(t)G(t) = \lim_{s\to 0} s \cdot u(s)G(s) = \lim_{s\to 0} s\frac{1}{s^2}\frac{s}{s+1} = 1 \tag{4.10}$$

From (4.9) it is possible to observe that the integrator cancels the error when a constant input (a step input) while from (4.10) it is possible to observe that the integrator doesn't cancel the error with a variable input (a ramp input).

In the following, the main components of control system depicted in Figure 4.7 will be described in detail. The adopted coordinate transformation are described in Appendix A.

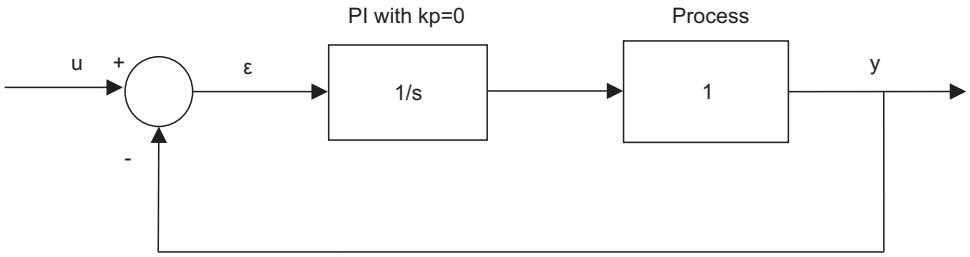

Figure 4.9: Block diagram with PI controller and Process.

4.3.1 PLL-Type estimator

As shown in Figure 4.7, in order to derive the control system in the $dq-$ coordinates it is necessary calculate the grid-voltage angle θ(t), given by

$$\theta(t) = \int_0^\tau \omega(t)dt + \theta_0 \tag{4.11}$$

with θ_0 the grid voltage angle at t=0. Therefore,

$$\frac{d\theta(t)}{dt} = \omega(t) = \dot{\theta} \tag{4.12}$$

where ω(t) is the angular frequency.

It is possible to calculate θ(t) in several ways. If the frequency is constant and known exactly and if $\theta_0 = 0$, θ(t) is given by

$$\theta(t) = 2\pi ft = \omega t \tag{4.13}$$

but obviously, in a real system the frequency is never constant, thus $\theta(t)$ will be affected by an error. Another way is to monitor one phase of the grid voltage and calculate the frequency from two subsequent zero crossing. However the measure is always affect by noise making difficult the calculation of the zero crossing without filtering. Furthermore, in a three-phase system $\theta(t)$ is calculated in one phase losing information about the other two phases.

Another way, used in this work, is to use a PLL-type estimator. The PLL calculates the angle $\theta(t)$ needed to align the grid voltage vector $\underline{e}_g^{(dq)}(t)$ with one of

the $dq-$coordinates. If the $d-$coordinate is aligned with the grid voltage vector the system is called "voltage oriented system", while if $q-$coordinate is aligned with the grid voltage vector the system is called "flux oriented system". Thus $\theta(t)$ is calculated by adding a correction term ($\gamma\varepsilon$) to the synchronous frequency, in order to set one of the vectors components equal to zero in steady state. The PLL-type estimator is given

$$\dot{\theta} = \omega_s + \gamma\varepsilon \tag{4.14}$$

where ω_s is the nominal frequency, γ is gain parameter and ε is the error signal.

Combining (4.14) with (4.12), the angle error (indicated with the symbol$\tilde{}$) is given by

$$\dot{\tilde{\theta}} = \dot{\theta}_s - \dot{\theta} = -\gamma\varepsilon \tag{4.15}$$

In this work $d-$component is aligned with the grid voltage vector, thus the error signal coincides with e_{gq}

$$\varepsilon \equiv e_{gq} = e_{g\alpha}\sin(-\tilde{\theta}(t)) + e_{g\beta}\cos(-\tilde{\theta}(t)) \tag{4.16}$$

For small $\tilde{\theta}$ $\sin(-\tilde{\theta}(t)) \approx -\tilde{\theta}(t)$ while $\cos(-\tilde{\theta}(t))$ is constant, therefore the error signal becomes

$$\varepsilon = -e_{g\alpha}\tilde{\theta}(t) \tag{4.17}$$

It is possible to observe that $\dot{\tilde{\theta}}$ converges to zero faster as γ is increased. This gain should not be made larger than necessary for good tracking of θ, since this would lead to high amplification of harmonics. The synchronization loop bandwidth is $\alpha_e = \gamma\hat{E}_g$, thus the gain selection is given by

$$\gamma = \frac{\alpha_e}{\hat{E}_g} \tag{4.18}$$

where $\hat{E}_g$ is the estimated grid voltage magnitude.

Here, the bandwidth of the PLL is set to $\alpha_e = 0.1\omega$, therefore the gain selection is

$$\gamma = \frac{0.1\omega}{\sqrt{e_{g\alpha} + e_{g\beta}}} \tag{4.19}$$

The active and reactive power are given (see Appendix A.) by (A.18) and (A.19)

$$P = e_d i_d \tag{4.20}$$

$$Q = -e_d i_q \tag{4.21}$$

thus the digital implementation of whole control system is easier moreover if q-component is set equal zero, the d-component of the current will be proportional to

the active power whereas the q-component of the current will be proportional to the reactive power in steady-state.

Figure 4.10 shows the block diagram of the adopted PLL implemented in continuous time domain.

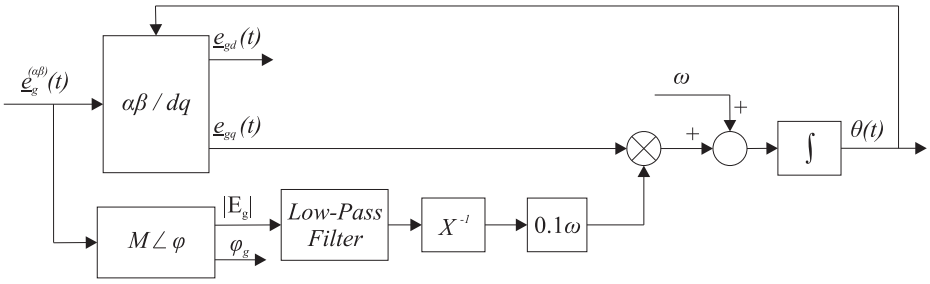

Figure 4.10: Block diagram of adopted PLL.

Figure 4.11 shows the Bode diagram of PLL for two different bandwidths. Increasing its bandwidth, the PLL will be faster. The bandwidths of the PLL have been set equal to 30 rad/s (sys1) and 300 rad/s (sys2). Note that for sys1 the frequency components in the input signal above 6 Hz will be attenuated in the output signal while for sys2 is above 60Hz. In Chapter 3 it has been seen that the voltages dips are mostly unbalanced, which results in a double-frequency component in the measured signals (see Appendix A). From Figure 4.11 it is possible to observe that a input signal at 100 Hz will be attenuated by 90% with sys1 and by 20% with sys2. This means that to ensure a good rejection to the negative sequence component, it is convenient to select the bandwidth of the PLL $\leq$ 30rad/sec.

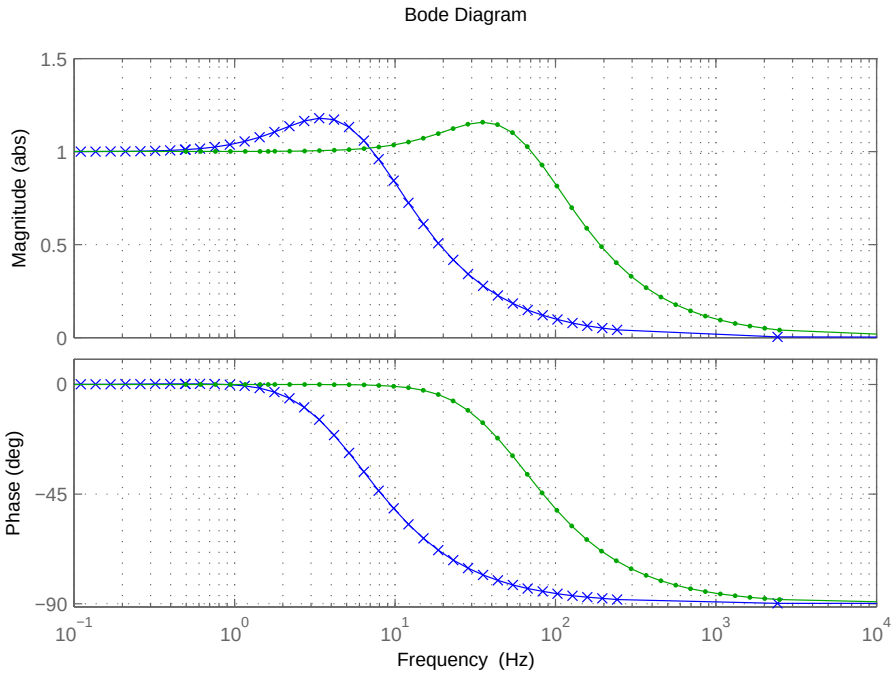

Figure 4.11: Bode diagram of PLL for two different bandwidths. Marker "x" denotes α_e= 30 rad/sec, marker "◊" denotes α_e= 300 rad/sec

4.3.2 Vector Current-Controller(VCC)

From the electrical scheme shown in Figure 4.1, with the signal reference given in the figure, applying Kirchhoff's voltage law (KVL), the following differential equations can be obtained

$$\begin{aligned} u_a(t) - R_f i_{fa}(t) - L_f \frac{di_{fa}(t)}{dt} - e_{ca}(t) = 0 \\ u_b(t) - R_f i_{fb}(t) - L_f \frac{di_{fb}(t)}{dt} - e_{cb}(t) = 0 \\ u_c(t) - R_f i_{fc}(t) - L_f \frac{di_{fc}(t)}{dt} - e_{cc}(t) = 0 \end{aligned} \tag{4.22}$$

Equation (4.22) can be written in the fixed $\alpha\beta-$ coordinate system as

$$\underline{u}^{(\alpha\beta)}(t) - R_f \underline{i}_f^{(\alpha\beta)}(t) - L_f \frac{d\underline{i}_f^{(\alpha\beta)}(t)}{dt} - \underline{e}_c^{(\alpha\beta)}(t) = 0 \tag{4.23}$$

Under the assumption of perfect knowledge of the grid-voltage angle (neglecting the dynamic of PLL) the $\alpha\beta-$ to $dq-$transformation is applied.The VSC voltages, the capacitor voltages and the VSC currents in the rotating $dq-$coordinate system are

equal to

$$\begin{aligned} \underline{u}^{(dq)}(t) &= e^{-\jmath\theta(t)}\underline{u}^{(\alpha\beta)}(t) \\ \underline{e}_c^{(dq)}(t) &= e^{-\jmath\theta(t)}\underline{e}_c^{(\alpha\beta)}(t) \\ \underline{i}_f^{(dq)}(t) &= e^{-\jmath\theta(t)}\underline{i}_f^{(\alpha\beta)}(t) \end{aligned} \tag{4.24}$$

Equation (4.23) can thus be transformed into

$$\begin{aligned} &\underline{u}^{(dq)}(t)e^{\jmath\theta(t)} - R_f\underline{i}_f^{(dq)}(t)e^{\jmath\theta(t)} - L_f\frac{d}{dt}(\underline{i}_f^{(dq)}(t)e^{\jmath\theta(t)}) - \underline{e}_c^{(dq)}(t)e^{\jmath\theta(t)} = \\ &= \underline{u}^{(dq)}(t) - R_f\underline{i}_f^{(dq)}(t) - e^{-\jmath\theta(t)}L_f(\frac{d}{dt}(\underline{i}_f^{(dq)}(t)e^{\jmath\theta(t)} + +\underline{i}_f^{(dq)}(t)\jmath\omega e^{\jmath\theta(t)}) + \underline{e}_c^{(dq)}(t) \end{aligned}$$

$$\underline{u}^{(dq)}(t) - R_f\underline{i}_f^{(dq)}(t) - L_f\frac{d\underline{i}_f^{(dq)}(t)}{dt} - \jmath L_f\omega\underline{i}_f^{(dq)}(t) - \underline{e}_c^{(dq)}(t) = 0 \tag{4.25}$$

Equation (4.25) can be split up into two equations representing the $d-$ and $q-$component separately and considering that $\jmath i_{fd} = -i_{fq}$ and $\jmath i_{fq} = i_{fd}$

$$\begin{aligned} u_d(t) &= e_{cd}(t) + R_f i_{fd}(t) + L_f\frac{di_{fd}(t)}{dt} - \omega L_f i_{fq}(t) \\ u_q(t) &= e_{cq}(t) + R_f i_{fq}(t) + L_f\frac{di_{fq}(t)}{dt} + \omega L_f i_{fd}(t) \end{aligned} \tag{4.26}$$

Assuming that the switching frequency is very high and that not saturation of VSC occurs, the VSC can be modelled as an ideal three-phase voltage source. Therefore, the output voltages of the VSC can be considered sinusoidal and equal to the reference voltages (u_a^*, u_b^*, u_c^*), (4.25) can by rewritten as

$$\underline{u}^{*(dq)}(t) - R_f\underline{i}_f^{(dq)}(t) - L_f\frac{d\underline{i}_f^{(dq)}(t)}{dt} - \jmath L_f\omega\underline{i}_f^{(dq)}(t) - \underline{e}_c^{(dq)}(t) = 0 \tag{4.27}$$

This equation corresponds to the block diagram depicted in Figure 4.12.

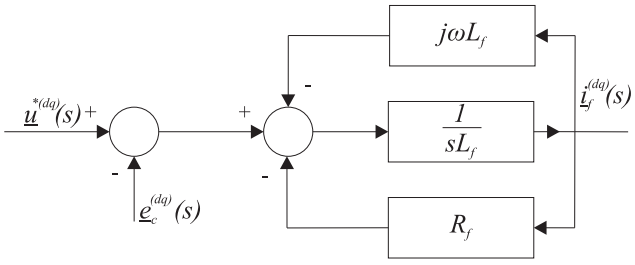

Figure 4.12: Block diagram of the main electrical circuit.

Equation (4.25) will be used to derive the current controller in the next section (Controller Design). Figure 4.13 shows the schematic diagram of the algorithm of the current controller that can be summarized as follows:

1. Measure and sample grid voltages and filter currents with sampling frequency f_s.
2. Transform all quantities from the three-phase coordinate system to the fixed $\alpha\beta-$coordinate system, using the transformation angle $\theta(t)$, obtained from the PLL.
3. Calculate the reference voltage vector $\underline{u}^{*(dq)}(t)$ using the current controller.
4. Transform the reference voltage vector from the rotating $dq-$coordinate system to the three-phase coordinate using the same transformation angle $\theta(t)$.
5. Inject a zero sequence voltage into the control signals by the block "OPT"
6. Calculate the duty-cycle in the "PWM" block and send the switching pulses to the VSC valves.

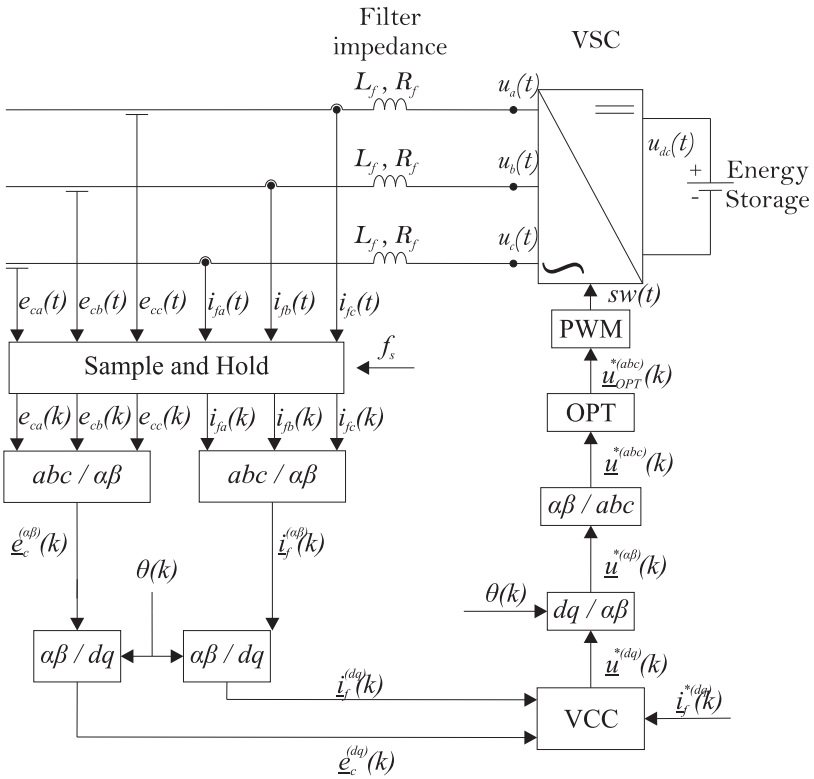

Figure 4.13: Schematic diagram showing VSC, grid, filter and controller.

Controller design

By applying the Laplace transformation to (4.27), it is possible to obtain the complex transfer function $G(s)$ of the system shown in Figure 4.12 from $(\underline{u}^{*(dq)} - (s)\underline{e}_c^{(dq)}(s))$ to $\underline{i}_f^{(dq)}(s)$, given by

$$G(s) = \frac{1}{(s + \jmath\omega)L_f + R_f} \tag{4.28}$$

Using the complex transfer function (4.28), the system can be expressed with the block diagram shown in Figure 4.14. The voltage vector $\underline{e}_c^{(dq)}(t)$ is modelled as a disturbance which subtracts from the input signal $\underline{u}^{*(dq)}(t)$. The current vector $\underline{i}_f^{(dq)}(t)$ is measured and compared with the reference $\underline{i}_f^{*(dq)}(t)$. The error signal $\varepsilon_c = \underline{i}_f^{*(dq)}(t) - \underline{i}_f^{(dq)}(t)$ forms the input of the current controller (denoted as $F(s)$ in the figure), which generates the voltage reference $\underline{u}^{*(dq)}(t)$.

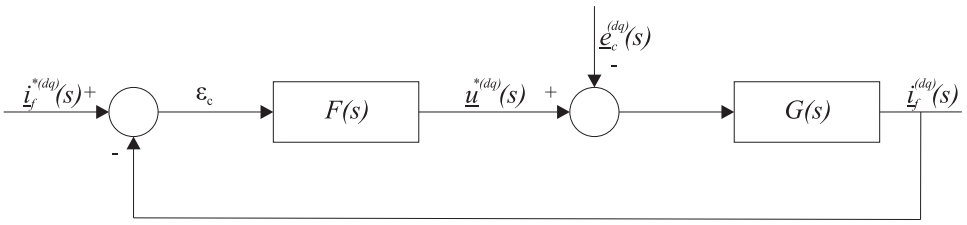

Figure 4.14: Block diagram of the electrical dynamics.

Equation (4.26) represent two cross-coupled first-order subsystems. The cross coupling is initiated by the term $\jmath\omega L_f \underline{i}_f^{(dq)}$ in (4.27), since multiplication by $\jmath$ maps the $d-$axis on the $q-$axis and vice versa

$$\jmath\underline{i}_f^{(dq)}(t) = \jmath(i_{fd} + \jmath i_{fq}) = -i_{fq} + \jmath i_{fd} \tag{4.29}$$

The first step in the controller design is to cancel this cross coupling term. This is easily done, provide that the inductance L_f is known with fairly good accuracy, by adding a decoupler term $\jmath\omega L_f$ to the inner feedback loop, as shown in the following figure

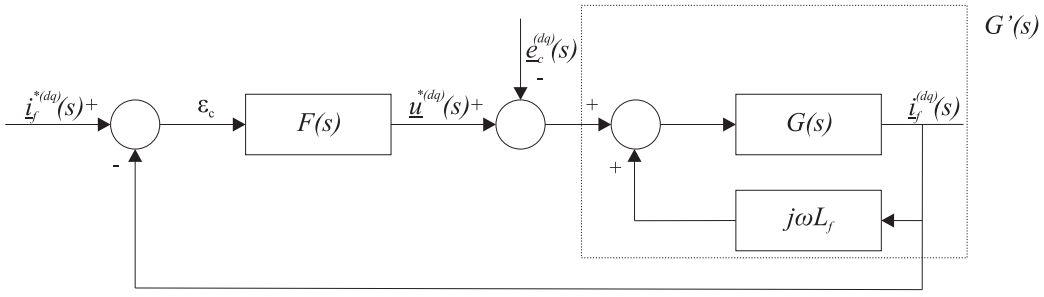

Figure 4.15: Block diagram of the electrical dynamics with an inner decoupling loop.

Considering the subsystem $G'(s)$ the transfer function is given by

$$\begin{aligned} G'(s) = \frac{G(s)}{1 - G(s)(\jmath\omega L_f)} &= \frac{\dfrac{1}{(s+\jmath\omega)L_f + R_f}}{1 - \dfrac{1}{(s+\jmath\omega)L_f + R_f}\jmath\omega L_f} = \\ &= \frac{\dfrac{1}{(s+\jmath\omega)L_f + R_f}}{\dfrac{(s+\jmath\omega)L_f + R_f - \jmath\omega L_f}{(s+\jmath\omega)L_f + R_f}} = \frac{1}{R_f + sL_f} \end{aligned} \tag{4.30}$$

It is possible to observe that the cross-coupling term is cancelled.

The transfer function $G'(s)$ is a first-order complex-valued system (representing two non-interacting first-order system in the d and q directions, respectively). Therefore, a PI regulator (Proportional-Integral control) is appropriate for control

$$F(s) = k_{pc} + \frac{k_{ic}}{s} \tag{4.31}$$

The next step is to select the controller parameter k_{pc} and k_{ic}. If the filter parameters are known it is logical to use this knowledge for selecting suitable k_{pc} and k_{ic}. The controller is designed to have the features of a low-pass filter; thus the closed-loop transfer function $G_{cc}(s)$ from $\underline{i}_f^{*(dq)}(t)$ to $\underline{i}_f^{(dq)}(t)$ is imposed to be equal to

$$G_{cc}(s) = \frac{\alpha_{cc}}{s + \alpha_{cc}} = \frac{\alpha_{cc}/s}{1 + \alpha_{cc}/s} \tag{4.32}$$

where α_{cc} is the closed-loop system bandwidth. In Figure 4.16 is shown the step response for a low-pass filter

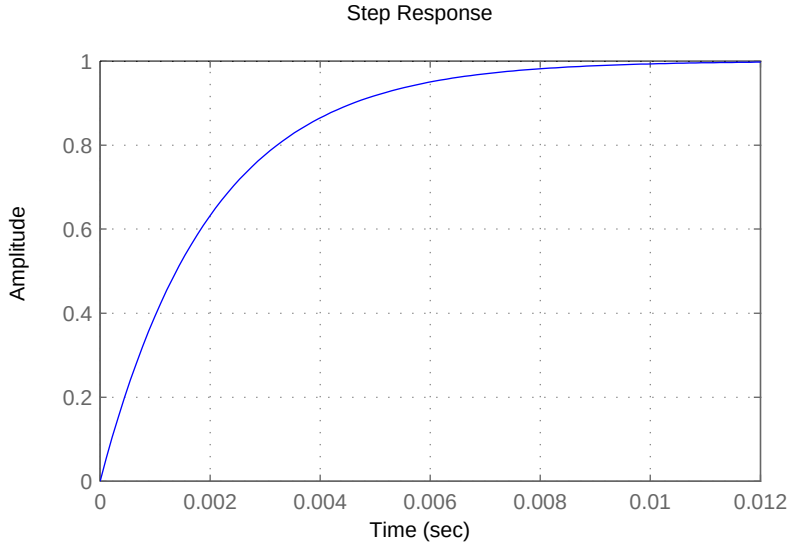

Figure 4.16: Step response of Low-Pass filter.

If the disturbance $\underline{e}_c^{(dq)}(s)$ is equal to zero, from Figure 4.15 $G_{cc}(s)$ is also equal to

$$G_{cc}(s) = \frac{F(s)G'(s)}{1 + F(s)G'(s)} \tag{4.33}$$

so, if $F(s)G'(s) = \alpha_{cc}/s$, the desired closed-loop system is obtained. This yields

$$F(s) = \frac{\alpha_{cc}}{s} G'^{-1}(s) = \frac{\alpha_{cc}}{s}(sL_f + R_f) = \alpha_{cc}L_f + \frac{\alpha_{cc}R_f}{s} \tag{4.34}$$

which leads to

$$\begin{aligned} k_{pc} &= \alpha_{cc}L_f \\ k_{ic} &= \alpha_{cc}R_f \end{aligned} \tag{4.35}$$

Imposing at the system a specific rise time t_{rc} (time required for the output signal to go from 10% to 90% of the final value [19]), it is possible to calculate the closed-loop system bandwidth [20]

$$\alpha_{cc} = \frac{\ln 9}{t_{rc}} \tag{4.36}$$

Improvement of Current Controller

Previously in order to design the current controller, it has been made the assumption that the disturbance $\underline{e}_c^{(dq)}(s)$ is equal to zero. Obviously, this voltage can't be equal to zero. A straightforward remedy of disturbance rejection is to add the term $\widehat{\underline{e}}_c^{(dq)}(t)$ (estimated capacitor voltage) to the output of the current controller [20], as shown in Figure 4.17. If $\widehat{\underline{e}}_c^{(dq)}(t)$ coincides with $\underline{e}_c^{(dq)}(t)$ the influence of $\underline{e}_c^{(dq)}(t)$ is cancelled; while if $\widehat{\underline{e}}_c^{(dq)}(t)$ doesn't coincide with $\underline{e}_c^{(dq)}(t)$ the influence of $\underline{e}_c^{(dq)}(t)$ is reduced but not cancelled.

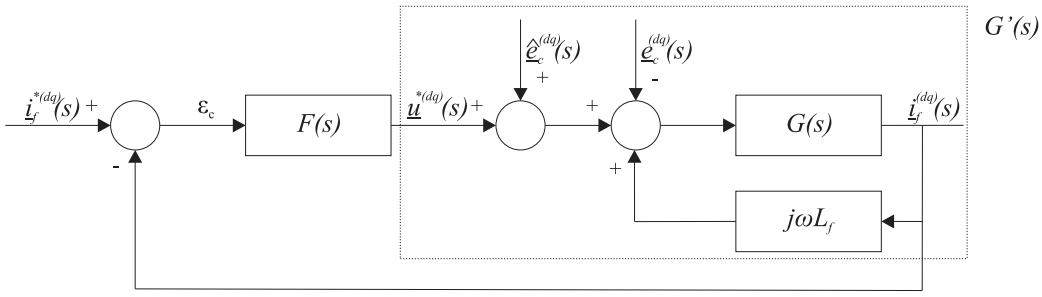

Figure 4.17: Block diagram of the electrical dynamics with an inner decoupling loop and feed forward of voltage vector.

In this work all the signals are estimated and all these are exactly equal to the actual signals, therefore $\widehat{\underline{e}}_c^{(dq)}(s) \equiv \underline{e}_c^{(dq)(s)}$. The PI controller can be rewritten as follows

$$\underline{u}^{*(dq)}(s) = \widehat{\underline{e}}_c^{(dq)}(s) + \jmath\omega L_f \underline{i}_f^{(dq)}(s) + k_{pc}\varepsilon_c + \frac{k_{ic}\varepsilon_c}{s} \tag{4.37}$$

The damping of the system depends from the value of the filter resistance. Normally, in order to limit the losses in the system, this resistance is very small and the system results not much damped. In order to increase the damping, a resistance can be added. However, the resistor causes losses in all operating conditions and increases the amount of active power during voltage dip mitigation. An alternative method [21] is to add a fictitious resistance in the inner feedback loop as shown in Figure 4.18, using an "active resistance" R_a. This technique, which may also be called "active damping", was proposed in [22].

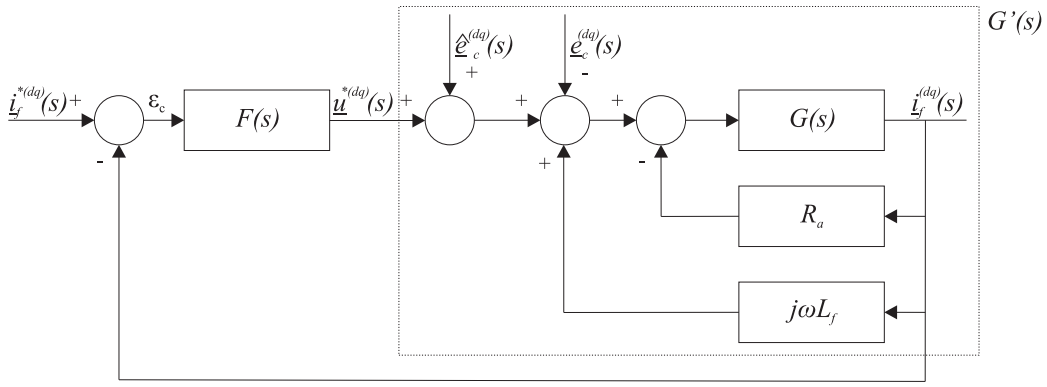

Figure 4.18: Block diagram of the electrical dynamics with an inner decoupling loop, a feed forward of voltage vector and "active damping".

The modified transfer function $G'(s)$ is now

$$G'(s) = \frac{1}{R_f + R_a + sL_f} \tag{4.38}$$

Observe that, although the fictitious resistance is not physically inserted in the system, the controller "sees" an increased filter resistance.

The PI controller $F(s)$ can now be designed as

$$F(s) = \frac{\alpha_{cc}}{s} G'^{-1}(s) = \frac{\alpha_{cc}}{s}(sL_f + R_a + R_f) = \alpha_{cc}L_f + \frac{\alpha_{cc}(R_a + R_f)}{s} \tag{4.39}$$

That is,

$$\begin{aligned} k_{pc} &= \alpha_{cc}L_f \\ k_{ic} &= \alpha_{cc}(R_a + R_f) \end{aligned} \tag{4.40}$$

Regarding the selection of R_a, it is useful to make the modified transfer function $G'(s)$ as fast as the total closed-loop system with bandwidth α_{cc}. Then R_a should be selected such that $(R_f + R_a)/L_f = \alpha_{cc}$, giving

$$R_a = \alpha_{cc}L_f - R_f \tag{4.41}$$

Therefore, the final expression for the vector current controller is given by

$$\underline{u}^{*(dq)} = \underline{e}_c^{(dq)} + \jmath\omega L_f \underline{i}_f^{(dq)} + \varepsilon_c k_{pc} + \varepsilon_c \frac{k_{ic}}{s} - R_a \underline{i}_f^{(dq)} \tag{4.42}$$

4.3.3 Vector Voltage-Controller(VVC)

From the electrical scheme shown in Figure 4.1, with the signal reference given in the figure, applying Kirchhoff's current law (KCL), the following differential equations can be obtained

$$\begin{aligned} i_{fa}(t) &= C\frac{de_{ca}(t)}{dt} + i_{ga}(t) \\ i_{fb}(t) &= C\frac{de_{cb}(t)}{dt} + i_{gb}(t) \\ i_{fb}(t) &= C\frac{de_{cb}(t)}{dt} + i_{gb}(t) \end{aligned} \tag{4.43}$$

Equation (4.43) can be written in the fixed $\alpha\beta-$ coordinate system as

$$\underline{i}_f^{(\alpha\beta)}(t) = C\frac{d\underline{e}_c^{(\alpha\beta)}(t)}{dt} + \underline{i}_g^{(\alpha\beta)}(t) \tag{4.44}$$

The $\alpha\beta-$ to $dq-$transformation is applied. The same PLL previously described is used to calculate the transformation angle $\theta(t)$; (4.44) can thus be transformed into

$$\underline{i}_f^{(dq)}(t) = C\frac{d\underline{e}_c^{(dq)}(t)}{dt} + \underline{i}_g^{(dq)}(t) + \jmath\omega C\underline{e}_c^{(dq)}(t) \tag{4.45}$$

Equation (4.45) can be split up into two equations representing the $d-$ and $q-$component separately as

$$\begin{aligned} i_{fd}(t) &= C\frac{de_{cd}(t)}{dt} + i_{gd}(t) - \omega Ce_{cq}(t) \\ i_{fq}(t) &= C\frac{de_{cq}(t)}{dt} + i_{gq}(t) + \omega Ce_{cd}(t) \end{aligned} \tag{4.46}$$

Equation (4.45) will be used to derive the voltage controller in the following section. Figure 4.19 shows the schematic diagram of the algorithm of the voltage controller that can be summarized as follows:

1. Measure and sample grid voltages and injection currents with sampling frequency f_s

2. Transform all quantities from the three-phase coordinate system to the fixed $\alpha\beta-$coordinate system, using the transformation angle $\theta(t)$, obtained from the PLL

3. Calculate the reference current vector $\underline{i}_f^{*(dq)}(t)$ for the vector current controller.

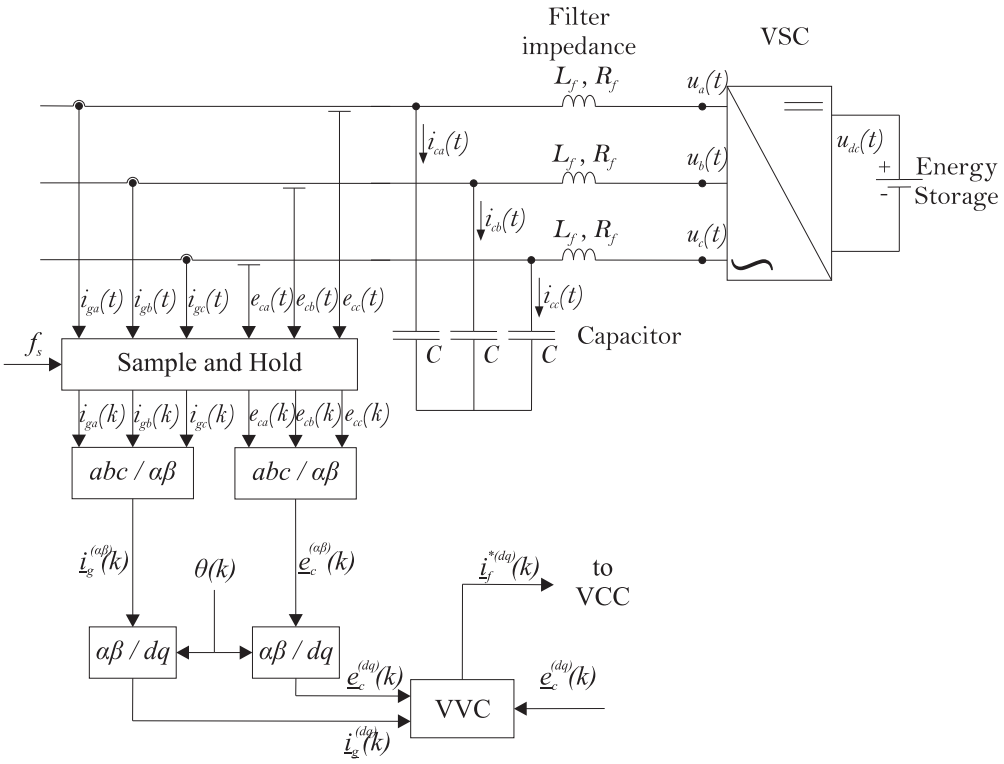

Figure 4.19: Schematic diagram showing VSC, grid, filter and voltage controller.

Controller design

In this section the design of VVC will be carried out. It is important to notice that the voltage controller design can be done under the assumption that the current controller is infinitely fast. Thereby it is possible say that the current reference, at the output of the voltage controller is the actual current in the line. The system can be expressed with the block diagram shown in Figure 4.20. The current vector $\underline{i}_g^{(dq)}(t)$ is modelled as a disturbance which subtracts from the input signal $\underline{i}_f^{*(dq)}(t)$. The voltage vector $\underline{e}_c^{(dq)}(t)$ is measured and compared with the reference $\underline{e}_c^{*(dq)}(t)$. The error signal $\varepsilon_v = \underline{e}_c^{*(dq)}(t) - \underline{e}_c^{(dq)}(t)$ forms the input of the voltage controller, which generates a signal proportional at the current reference $\underline{i}_f^{*(dq)}(t)$.

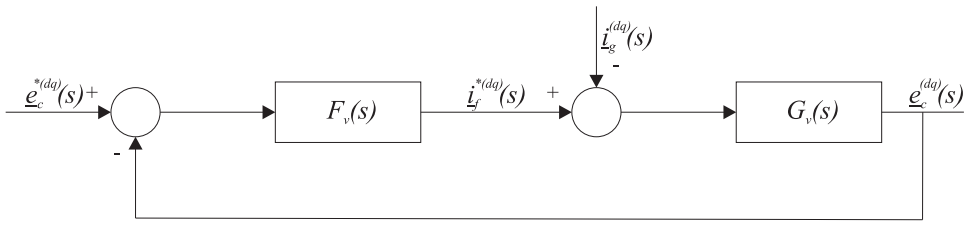

Figure 4.20: Block diagram of the electrical dynamics.

Following the same proceedings seen for controller design of the current controller, we obtain the complex transfer function $G_v(s)$ given by

$$G_v(s) = \frac{1}{C(s + \jmath\omega)} \tag{4.47}$$

The first step in the controller design is to cancel this cross coupling term; as seen before, if the capacitance C is known with fairly good accuracy, a decoupler term $\jmath\omega C$ can be added at inner feedback loop.

To cancel the influence of the $\underline{i}_g^{(dq)}(t)$, a term $\widehat{\underline{i}}_g^{(dq)}(t)$ (estimated injected current) can be added to the output of the voltage controller, in this case this term coincides with the current vector $\underline{i}_g^{(dq)}(t)$ measured (as seen before).

Also in the design of this controller, it is possible to use the "active damping" technique adding a fictitious conductance in the inner feedback loop, using an "active conductance" G_a. The following figure shows the block diagram of the system.

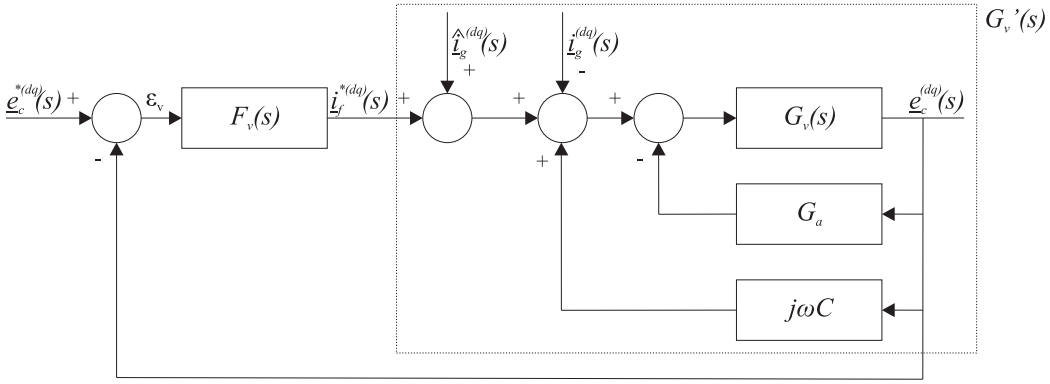

Figure 4.21: Block diagram of the electrical dynamics with an inner decoupling loop, a feed forward of voltage vector and "active damping".

Regarding selection of G_a, as seen before, can be selected as

$$G_a = C\alpha_{cv} \tag{4.48}$$

The modified transfer function $G'_v(s)$ is given by

$$G'_v(s) = \frac{G_v(s)}{1 - G_v(s)(\jmath\omega C - G_a)} = \frac{1}{Cs + G_a} \tag{4.49}$$

By observing the transfer function $G'_v(s)$, it is possible to say that this is a first-order complex valued system (representing two non-interacting first-order system in the d and q directions, respectively), PI control is appropriate

$$F_v(s) = k_{pv} + \frac{k_{iv}}{s} \tag{4.50}$$

The controller is designed to have the features of a low-pass filter; therefore

$$F_v(s) = \frac{\alpha_{cv}}{s} G'^{-1}_v(s) = \alpha_{cv} C + \frac{\alpha_{cv} G_a}{s} \tag{4.51}$$

which leads to

$$\begin{aligned} k_{pv} &= \alpha_{cv} C \\ k_{iv} &= \alpha_{cv} G_a \end{aligned} \tag{4.52}$$

where α_{cv} is the voltage controller. Observe that, without active damping term the system equations would lead to a pure P-controller. This is due to the fact that a lossless capacitor is considered in this design.

The PI controller can be rewritten as follows

$$\underline{i}_f^{*(dq)}(s) = \widehat{\underline{i}}_g^{(dq)}(s) + \jmath\omega C \underline{e}_c^{(dq)}(s) + \varepsilon_v k_{pv} + \varepsilon \frac{k_{iv}}{s} - G_a \underline{e}_c^{(dq)}(s) \tag{4.53}$$

4.4 Saturation and integration anti-windup

The VSC is capable to deliver voltages within the hexagon that is spanned by the six active voltage vectors represented in the $\alpha\beta-$coordinate system (see Figure 4.3). In transient state, the output voltage of the current controller may become large especially when having a large filter inductor. If the reference voltage vector is located in the region within the hexagon but outside the maximum circle that can be inscribed within it (see Figure 4.3) overmodulation occurs and that results in low-frequency current harmonics [23]. When the reference voltage vector output from the current controller exceeds the hexagon, which is the maximum voltage boundary of the PWM inverter limited by the DC-link voltage, then saturation occurs. If saturation occurs the VSC will not be able to deliver the demanded voltage leading to reduce performance of the system.

If saturation occurs, the output voltage of the current controller will be limited to the boundary of the hexagon and the output voltage will be smaller compared with the demanded one. In this case, if a controller with an integral part is used, the current error will be integrated and, as a consequence, the integration term can become very large, due to the fact that the output voltage cannot be increased to reduce the current error. This phenomenon is called "integrator windup" [24].

The saturation occurs if $\underline{u}_{abc}^*(t) \leq -\frac{u_{dc}}{2}$ or $\underline{u}_{abc}^*(t) \geq \frac{u_{dc}}{2}$. A countermeasure to avoid integrator windup is to inhibit the integration whenever the output of the VSC saturates.

4.5 Stability analysis

The performance of the entire system depends on the setting of the controller parameters. Therefore, a stability analysis is important to determine the stability margin and of course the performance. To ensure stability and a good damping of the system, the poles of the closed-loop system should be located in the gray area

shown in Figure 4.22 in the continuous time domain.

The behaviour of the system depends mainly on the values of the controllers bandwidth and on the values of the model parameters. In this section the study of the impact of these factors will be carried out. In particular, an analytical study of the poles location it will be carried out. The obtained analytical results will be validated through real-time simulations.

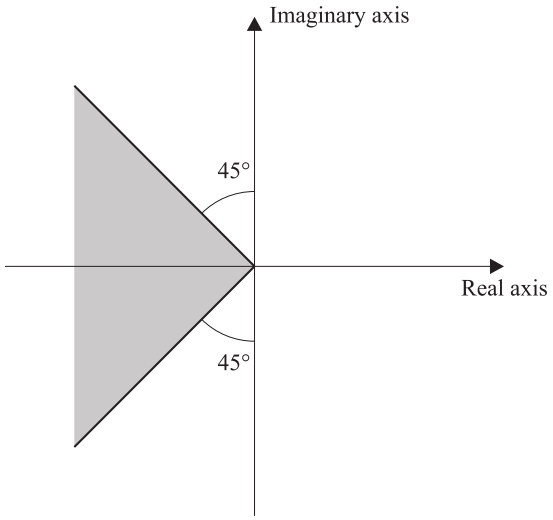

Figure 4.22: Desired poles locus in continuous time domain.

4.5.1 Impact of the controllers bandwidth

To ensure a high performance of the control system, the controller bandwidths must be set as high as possible.

The control system is made by two controllers in a cascade control structure. Previously, in Section 4.3.3, it has been made the assumption that the current controller (inner loop) is infinitely fast, but in a real installation there is a limitation about the bandwidth selection of this controller. Actually this bandwidth can be set at most equal to the sampling frequency f_s (deadbeat controller). To avoid problems like the "One-sample delay compensation" [25], the current controller bandwidth is here set equal to 1/5 of the sampling frequency. As a rule of thumb, in a cascade control structure the bandwidth of the outer loop should be 1/10 or less of the bandwidth of the inner loop. In this section the impact of the choice of the voltage controller bandwidth will be investigated. System parameters are reported in Table 4.1.

Table 4.1 System parameters.

Grid voltage	$E = 400V = 1pu$	Base Power	$S = 59.3kVA = 1pu$
Grid frequency	$f = 50$Hz	Capacitor	$C = 202.64\mu F$
Filter resistance	$R_f = 0.0248\Omega$	Filter Inductance	$L_f = 2mH$

To investigate the impact of voltage controller bandwidth, the control system has been analyzed increasing its bandwidth from 1/10 to 1/5 and 3/10 of the current controller bandwidth. The stability analysis can be done in the continuous time domain because the variation of the bandwidth causes the same effects for the continuous time domain and for the discrete time domain.

Figure 4.23 shows the pole-zero placement of the control system for voltage controller bandwidth variation. It is possible to observe that when decreasing the bandwidth difference between outer and inner loop poles and zeros move in the direction of the imaginary axis, decreasing the real part and increasing the imaginary part.

For clarity the poles and the zeros near the imaginary axis have been plotted separately in Figure 4.24. It is possible to observe that the poles and the zeros move in the direction of the imaginary axis, decreasing the real part and increasing the imaginary part.

From this analysis it is possible to conclude that increasing the bandwidth of the voltage controller, that represents the outer loop, the control system decreases its stability margin.

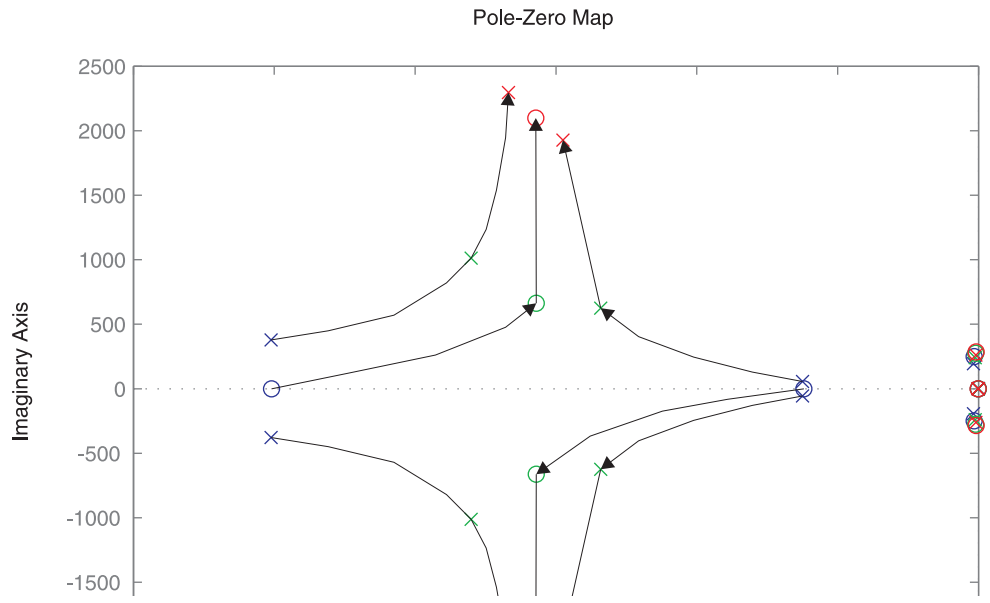

Figure 4.23: Pole Zero placement of the control system for α_{cv}/α_{cc} variation.

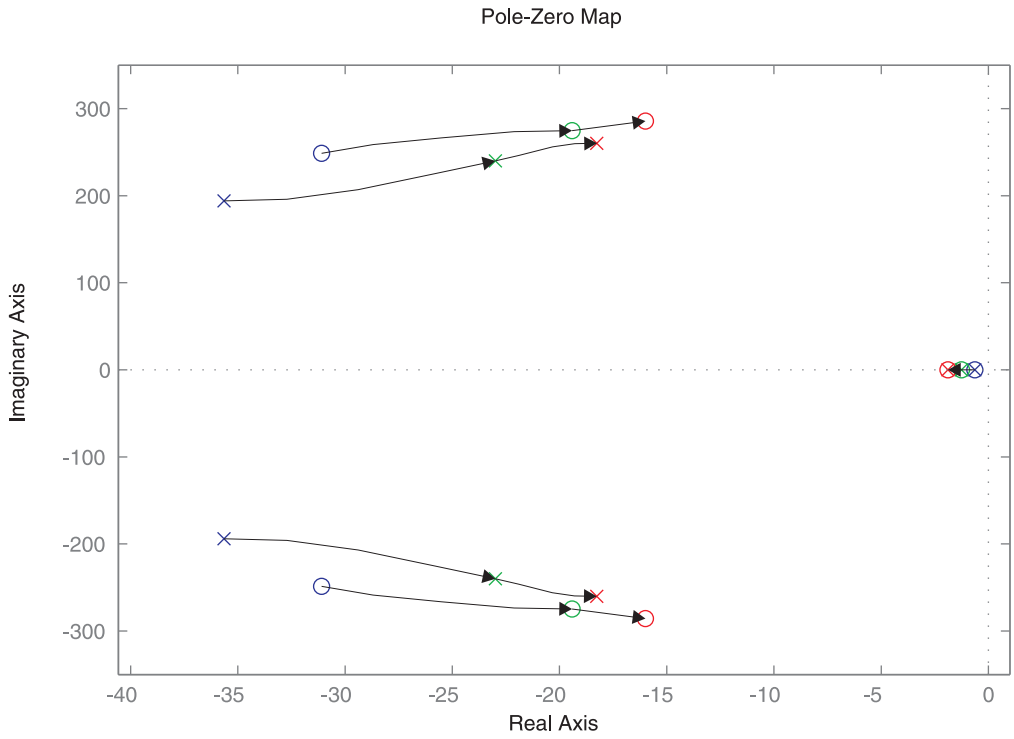

Figure 4.24: Pole Zero map of the control system for α_{cv}/α_{cc} variation - Zoom in on imaginary axis.

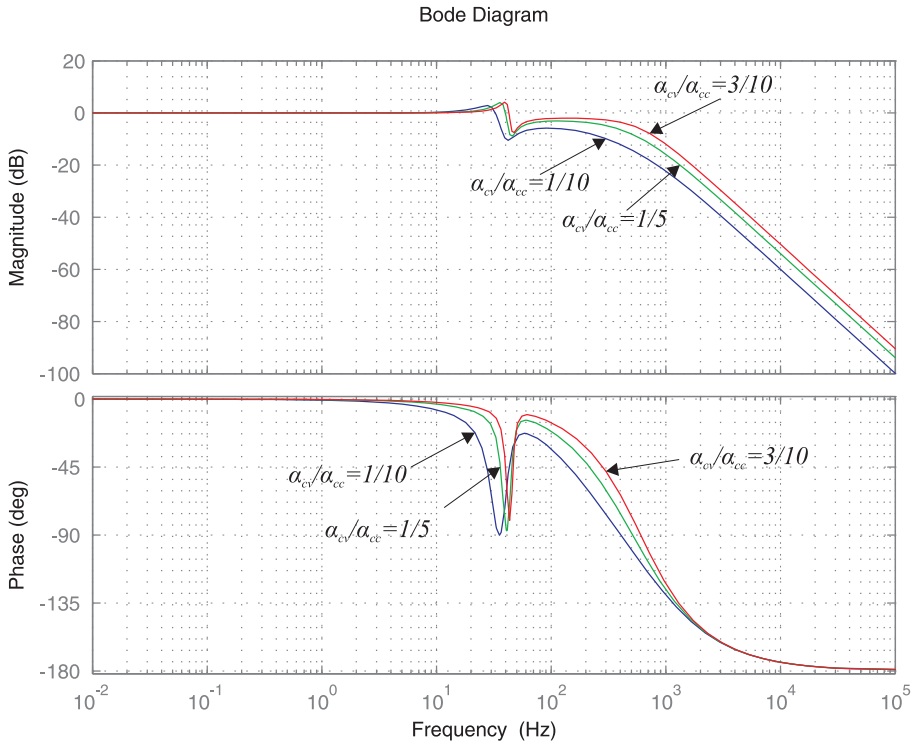

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Figure 4.25: Bode diagram of control system for α_{cv}/α_{cc} variation.

Figure 4.25 shows the Bode diagram of the control system. By increasing the ratio α_{cv}/α_{cc} for the three considered cases it is possible to observe that for α_{cv}/α_{cc}=1/10 m_{φ}=98.1° at frequency of 32.6 Hz; for α_{cv}/α_{cc}=1/5 m_{φ}=96° at frequency of 39.9 Hz; for α_{cv}/α_{cc}=3/10 m_{φ}=101° at frequency of 42.8 Hz.

For this analysis, the system has been modelled by using MatLab by MathWorks. To investigate the dynamic performance of the system, the response to a unity step input has been considered. The obtained results are then validated using the simulation program PSCAD/EMTCD by Manitoba, where the control system has been implemented by using Fortran 90 language [26].

Figures 4.26(a),(c) and (e) show the step response of the analyzed control system where using MatLab while Figures 4.26(b),(d) and (f) show the step response of the analyzed control system when using PSCAD/EMTDC. A unit step in the $d-$component of the reference capacitor voltage has been applied at $t = 0.0$ s and the response of the transfer function from reference to actual $d-$voltage over the capacitor is depicted. As shown, the obtained results with the two programs are exactly the same. This means that the stability analysis carried out corresponds to the real behaviour of the system. From the figures it is possible to notice that increasing the voltage controller bandwidth the performance of the control system increase, the overshoot and the damping decrease.

The controllers have been designed like a low-pass filter, but from the step response, it is possible to observe that the response of the control system is different from the response of a low-pass filter. This difference is due to the assumption during the derivation that the current controller bandwidth is infinitely large while the current controller bandwidth selected is limited. Figures 4.27 to 4.29 show the same step response of the analysed control system for $\alpha_{cc}/f_s = 1$, $\alpha_{cc}/f_s = 5$ and $\alpha_{cc}/f_s = 20$, respectively. The bandwidth of the voltage controller is kept constant and equal to 2π100 rad/sec. As shown, increasing the current controller bandwidth, the response of the system is much similar at that of low pass filter.

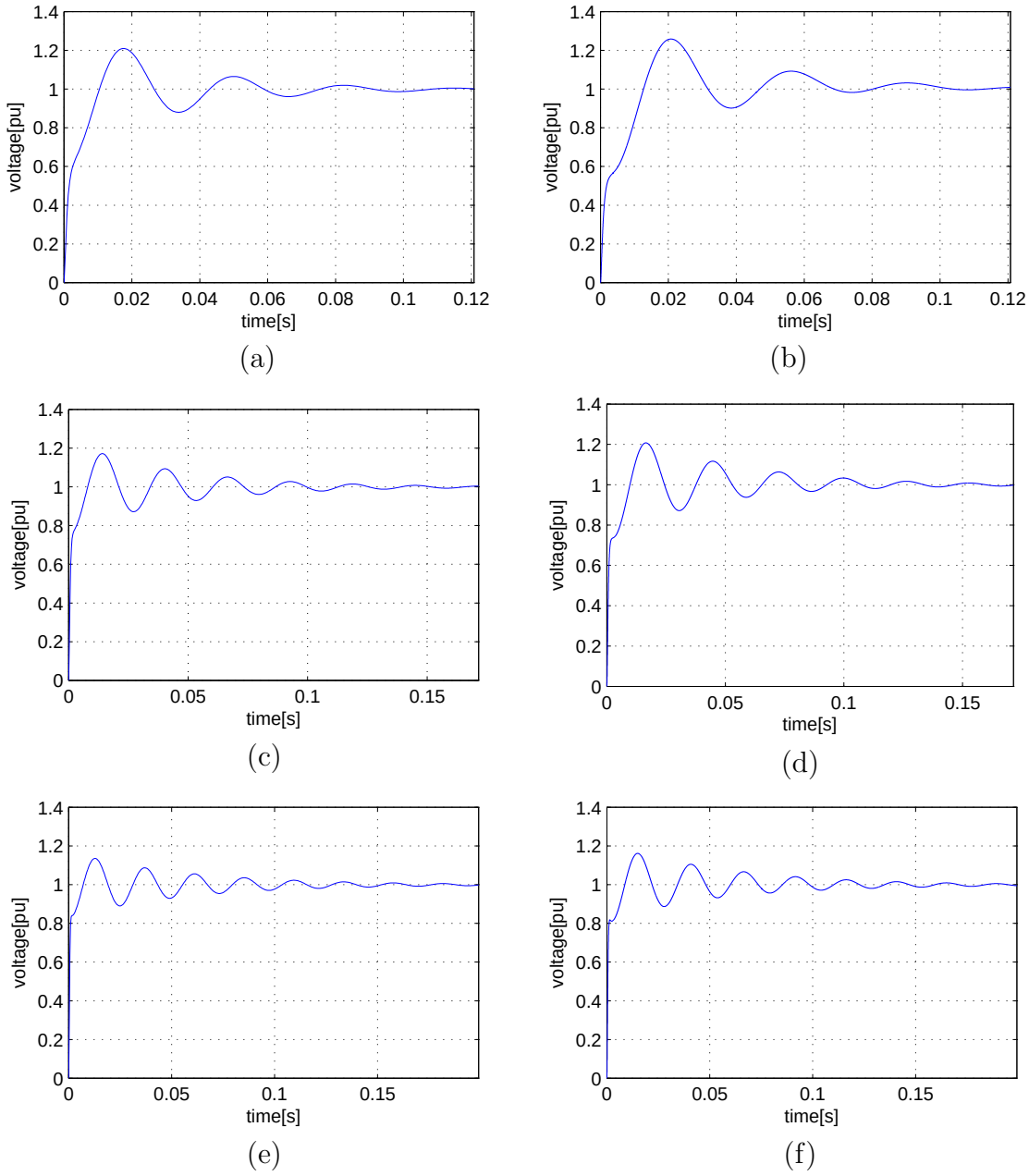

Figure 4.26: Simulated $d-$step response for α_{cv}/α_{cc} variation: (a),(c) and (e) with MatLab; (b),(d) and (f) with PSCAD/EMTDC.

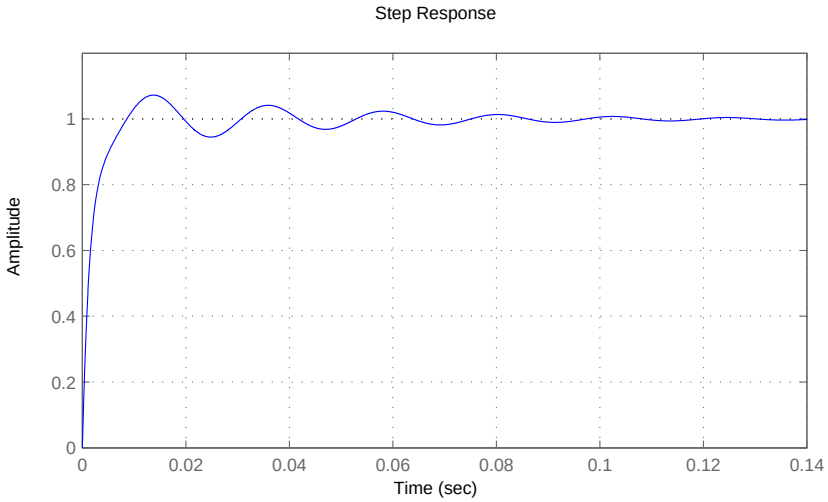

Figure 4.27: Simulated $d-$step response for $\alpha_{cc}/f_s = 1$.

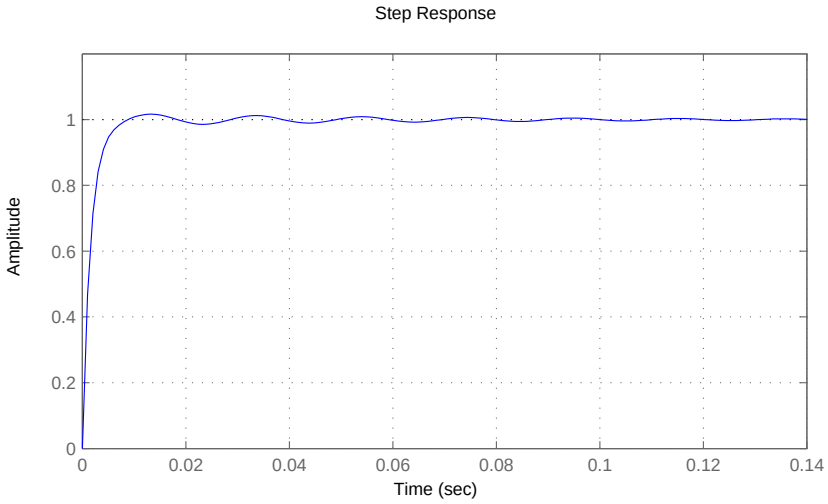

Figure 4.28: Simulated $d-$step response for $\alpha_{cc}/f_s = 5$.

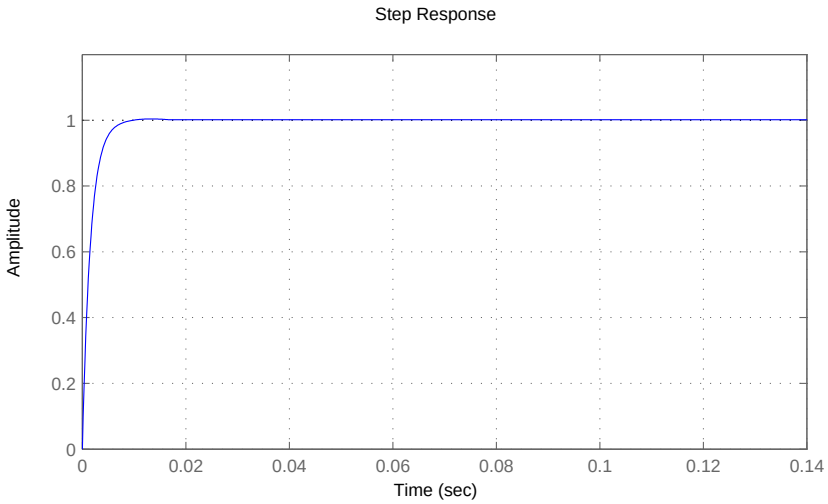

Figure 4.29: Simulated $d-$step response for $\alpha_{cc}/f_s = 20$.

4.5.2 Impact of model parameters

In the previous analysis, it has been assumed that the estimated system parameter coincide with the actual values. However, in a real system, the values of these parameters are not known exactly. Moreover, some of the parameter values change during operation, due to ageing or to temperature changes. In this section it will be studied the impact of model parameters on the control system, in particular to variations of the filter inductance. Since the filter resistance is usually negligible compared with its reactance, the response of the closed-loop system is insensitive to its variation [3]. Also, the active damping will reduce the effect of resistance variation [20].

The system is instead sensitive to variations of the filter inductance. Actually, a inaccurate knowledge of this parameter involves a wrong calculation of the output reference and a wrong value of the proportional gain k_{pc}. Figure 4.30 shows pole-zero placement of the closed-loop system when the estimated filter inductance $\widehat{L}_f$ varies from 60% to 140% of the actual filter inductance L_f, the VVC bandwidth and the VCC bandwidth are respectively set equal to $2\pi100$ rad/sec and $2\pi1000$ rad/sec.

It is possible to observe that underestimating the filter inductance some poles and zeros move in the direction of the imaginary axis, increasing the imaginary part, while some poles and zeros move in opposite direction increasing the imaginary part. Overestimating the filter inductance some poles and zeros move in the direction of the imaginary axis, increasing the imaginary part, while some poles and zers move in the opposite direction decreasing the imaginary part.

For clarity the poles and the zeros near the imaginary axis have been plotted separately in Figure 4.31. It is possible to observe that the poles and the zeros move in the opposite direction of the imaginary axis, decreasing the imaginary part.

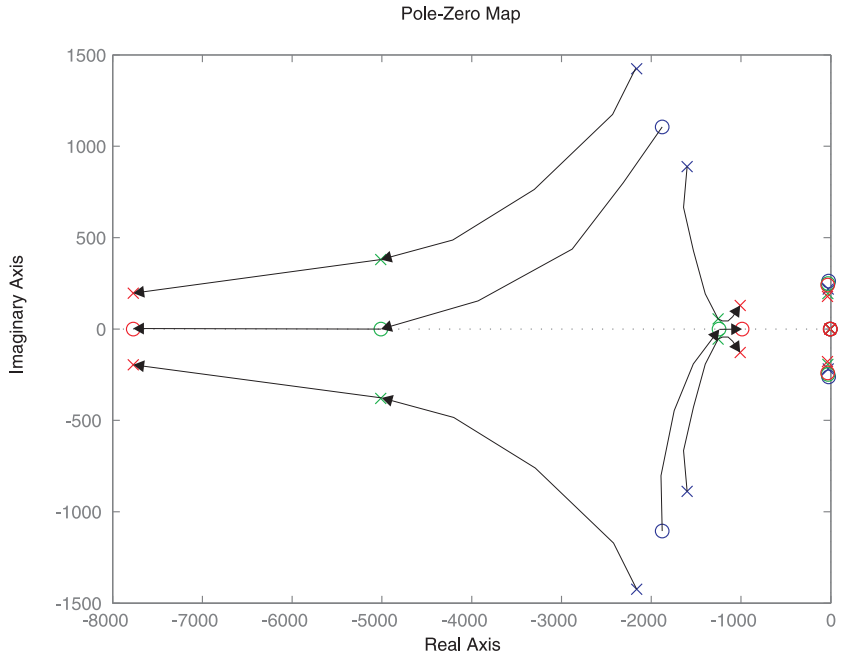

Figure 4.30: Pole-zero placement for $\widehat{L}_f = 0.6L_f$, $\widehat{L}_f = 1.0L_f$ and $\widehat{L}_f = 1.4L_f$.

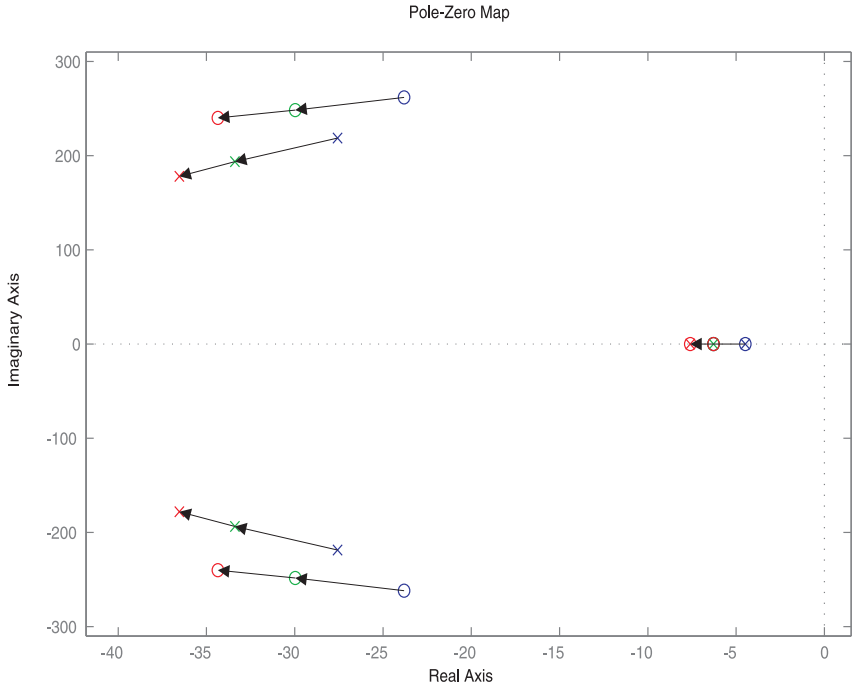

Figure 4.31: Pole zero placement of control system for $\widehat{L}_f = 0.6L_f$, $\widehat{L}_f = 1.0L_f$ and $\widehat{L}_f = 1.4L_f$. - Zoom in on imaginary axis.

To properly represent the behaviour of an actual system, it is of importance to consider that the controller will operate in discrete time, since it will be implemented in a control computer. This will have an impact on the system stability. During the sampling time the control system works with constant values while the electrical system evolves to new values. Thus the controllers performance will be affected. Considering this and considering the effects of the inaccurate knowledge of filter inductance, the stability analysis will be carried out in a discrete time domain.

To ensure stability and a good damping of the system, the poles of the closed-loop system should be located within the gray region inside a unit circle, as shown in Figure 4.32.

Figure 4.33 shows the pole-zero placement of the closed-loop system when the estimated filter inductance $\widehat{L}_f$ varies from 60% to 140% of the actual filter inductance L_f.

The trajectory of some poles has been plotted separately for clarity (see. Figure 4.34). From this figure, it is possible to observe that an underestimation of L_f results in a well-damped closed-loop system. On the other hand, an overestimation of L_f result in poorly-damped system and an overshoot in the step response can be observer. This overshoot increases with the overestimation error. Therefore, it can be concluded that, in order to obtain a well-damped system, it is better to underestimate the filter inductance $\widehat{L}_f$.

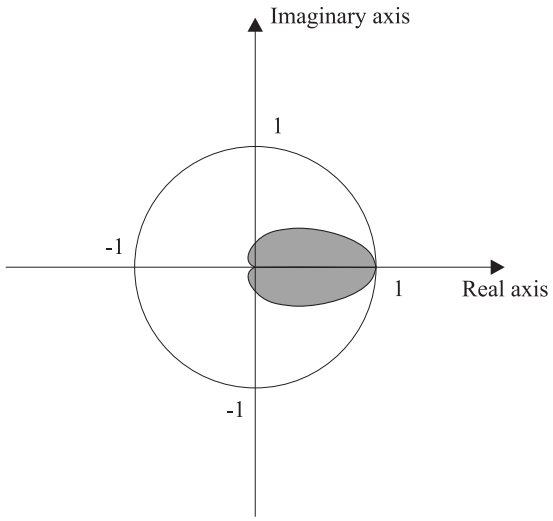

Figure 4.32: Desired poles locus in discrete time domain.

Figure 4.35 shows the Bode diagram of the control system, with variation of $\widehat{L}_f$ of 0.6, 1.0 and 1.4. By increasing of $\widehat{L}_f$ it is possible to observe that the gain margin $|m_a|$ increases while the phase margin m_φ decreases, in particular: for $\widehat{L}_f$=0.6L_f $|m_a|$=25.4 dB at frequency of 6.21 10^3 rad/sec while m_φ=110° at frequency of 217

rad/sec; for $\widehat{L}_f$=1.0L_f $|m_a|$=26.2 dB at frequency of 7.73 10^3 rad/sec while m_φ=93° at frequency of 206 rad/sec; for $\widehat{L}_f$=1.4L_f $|m_a|$=27.1 dB at frequency of 9 10^3 rad/sec while m_φ=88.6° at frequency of 199 rad/sec.

When the inductance is underestimated, the current controller produces a voltage reference smaller of that necessary and the response is slower; when the inductance is overestimated, the current controller produces a voltage reference larger of that necessary causing an overshoot and in this case the response is faster.

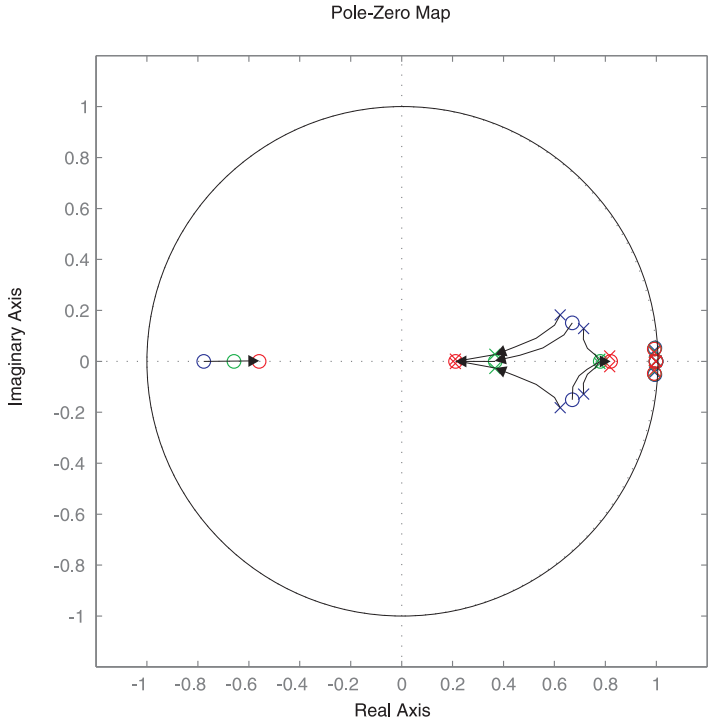

Figure 4.33: Pole-zero placement for $\widehat{L}_f = 0.6L_f$, $\widehat{L}_f = 1.0L_f$ and $\widehat{L}_f = 1.4L_f$.

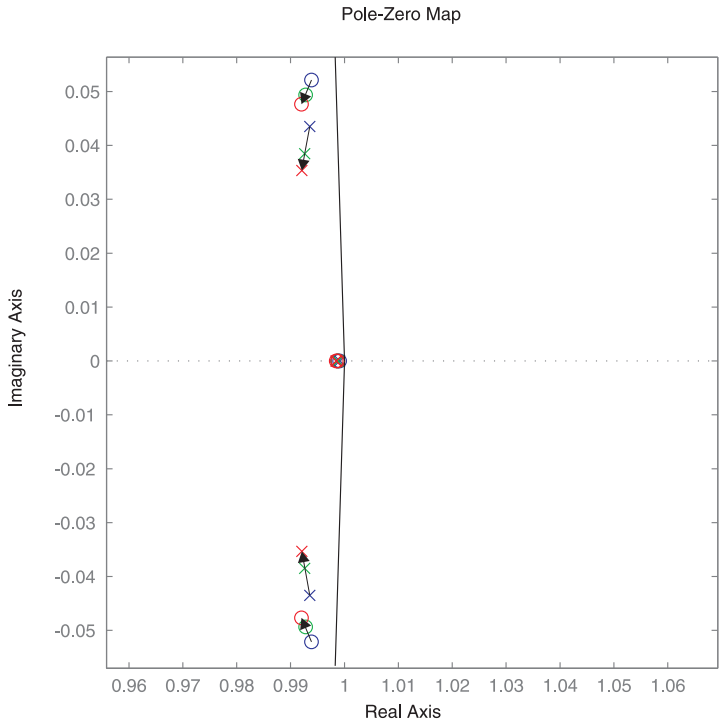

Figure 4.34: Pole zero placement of control system for $\widehat{L}_f = 0.6L_f$, $\widehat{L}_f = 1.0L_f$ and $\widehat{L}_f = 1.4L_f$. - Zoom in on imaginary axis.

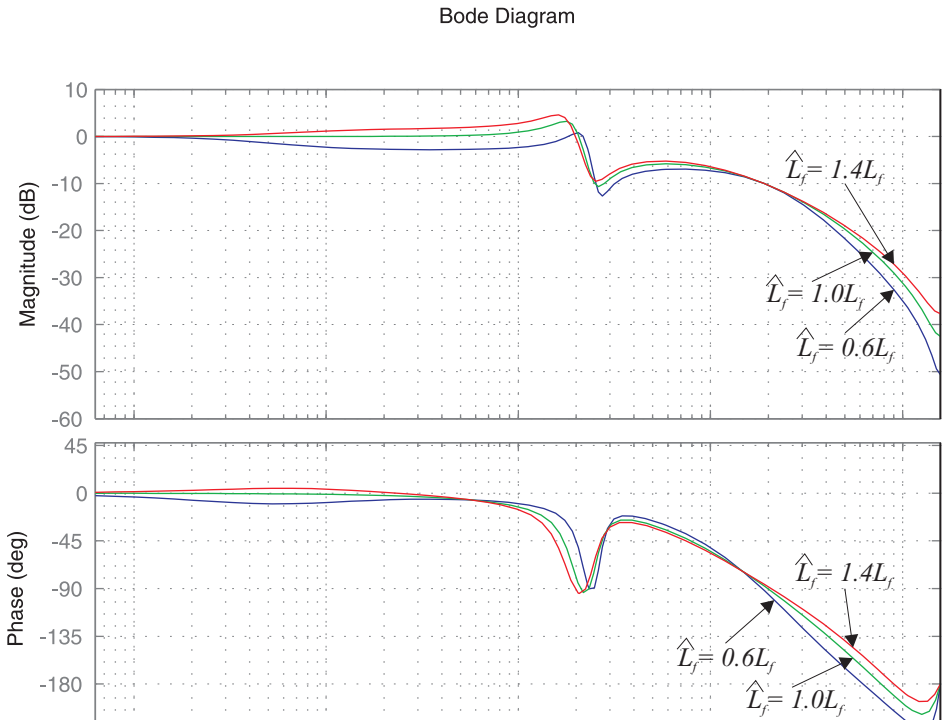

Figure 4.35: Bode diagram of control system for $\widehat{L}_f = 60\%L_f$, $\widehat{L}_f = 100\%L_f$ and $\widehat{L}_f = 140\%L_f$.

Figures 4.36(a) and (c) show the step response of the analyzed control system where using MatLab while Figures 4.36(b) and (d) show the step response of the analyzed control system when using PSCAD/EMTDC. A unit step in the $d-$component of the reference capacitor voltage has been applied at $t = 0.0$ s and the response of the transfer function from reference to actual $d-$voltage over the capacitor is depicted. As shown, the obtained results with the two programs are exactly the same. This means that the stability analysis carried out corresponds to the real behaviour of the system. As expected, when the filter inductance is underestimated the system is well damped, while the overestimated filter inductance provides an oscillatory step response with an initial overshoot of 0.41 pu.

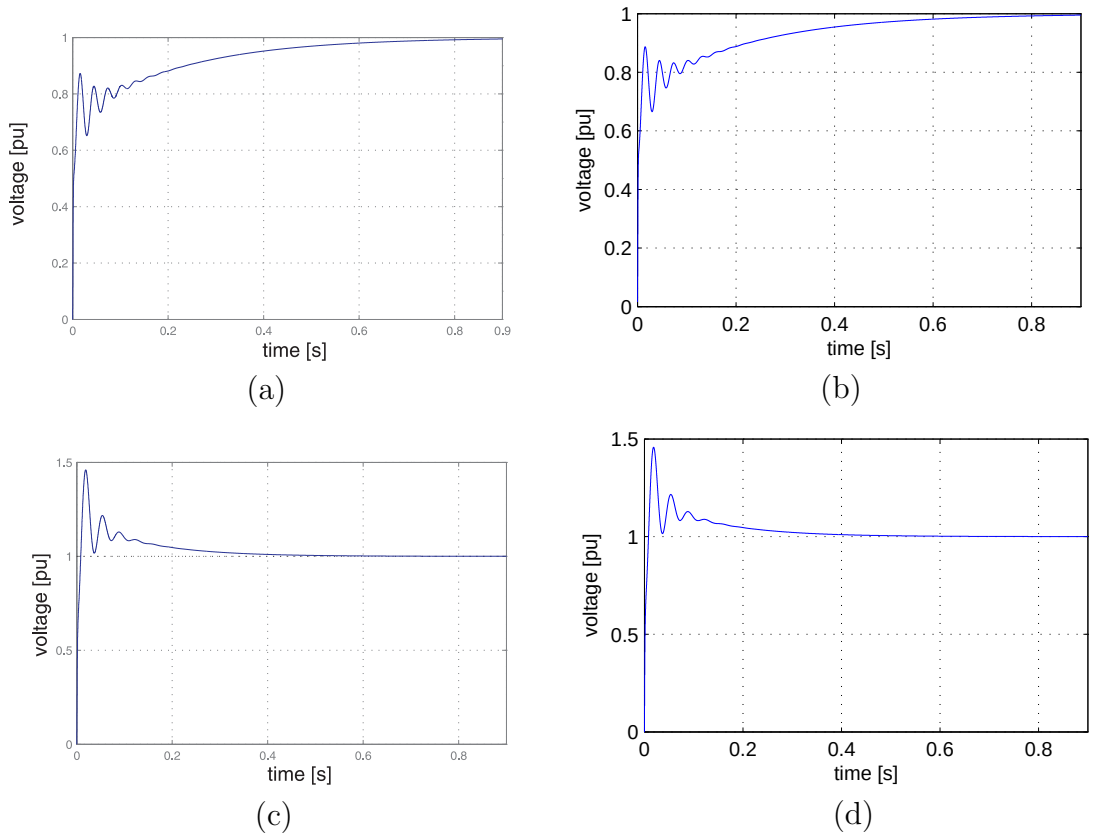

Figure 4.36: Simulated d-step response for $\widehat{L}_f$=140%L_f: (a) and (c) with MatLab; (b) and (d) with PSCAD/EMTDC.

4.6 Dual Cascade Controller

In the Chapter 3 it has been said that the majority of the voltage dips are unbalanced. Voltage unbalance, or three-phase unbalance, is the phenomenon in three-phase systems, in which the rms value of the voltages and/or the phase angle between consecutive phases are not equal. In this case according with Fortuscue's theorem, a set of three unbalanced phasors $\overline{E}_a$, $\overline{E}_b$ and $\overline{E}_c$ can always be resolved into three balanced systems of phasors:

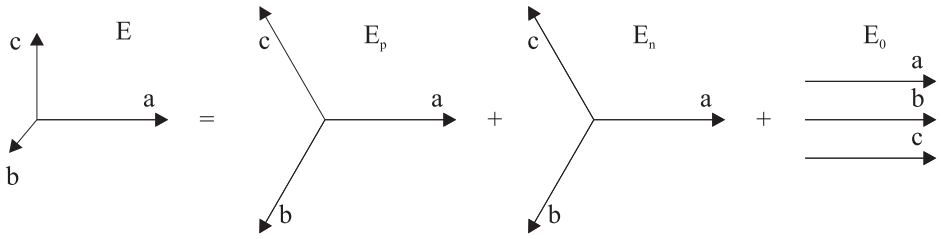

Figure 4.37: Fortuscue's theorem.

- Positive phase-sequence components system, formed by three phasors of equal magnitude E_p and displaced 120° counter clockwise from each other;
- Negative phase-sequence components system, formed by three phasors of equal magnitude E_n and displaced 120° clockwise from each other;
- Zero phase-sequence components system, formed by three phasors of equal magnitude E_0 and equal phase.

The sequence components can be calculated by

$$\overline{V}_p = \frac{1}{3}\left(\overline{V}_a + \alpha\overline{V}_b + \alpha^2\overline{V}_c\right) \tag{4.54}$$

$$\overline{V}_n = \frac{1}{3}\left(\overline{V}_a + \alpha^2\overline{V}_b + \alpha\overline{V}_c\right) \tag{4.55}$$

$$\overline{V}_0 = \frac{1}{3}\left(\overline{V}_a + \overline{V}_b + \overline{V}_c\right) \tag{4.56}$$

where $\alpha = e^{\jmath 2\pi/3}$ gives a phase shift of 120°.

Since the negative sequence appears, the controllers should track the 100 Hz negative sequence commands. In this condition the performance of the system will be deteriorated. To overcome this problem, the dual vector current- voltage- control (DVCC and DVVC) has been proposed in [27]. It is constituted by two separate control system implemented in the positive and in the negative synchronous reference frame (SRF) respectively (see also Appendix A.) [27].

Therefore, it is necessary to estimate positive and negative sequence component in the measured signals.

It is possible to use the traditional method, based on phasors but the main drawback is that this calculation requires at least one half period at the line frequency (10 ms at 50 Hz), thus being considered not fast enough for the performance required for the control system. To avoid the large delay introduced by this method, the space vectors have been used.

In the general case of unsymmetrical grid, the grid voltage vector $\underline{e}_g^{(\alpha\beta)}(t)$ can be written as

$$\underline{e}_g^{(\alpha\beta)}(t) = \underline{e}_{gp}^{(\alpha\beta)}(t) + \underline{e}_{gn}^{(\alpha\beta)}(t) = E_{gp}e^{\jmath(\omega t+\varphi_p)} + E_{gn}e^{-\jmath(\omega t+\varphi_n)} \tag{4.57}$$

where E_{gp} and E_{gn} are the amplitudes of positive and negative phase sequence voltage vectors, respectively, and φ_p and φ_n are their phase displacements. If a delay T is applied to the measured voltage vector, (4.57) becomes

$$\underline{e}_g^{(\alpha\beta)}(t-T) = E_{gp}e^{\jmath[\omega(t-T)+\varphi_p]} + E_{gn}e^{-\jmath[\omega(t-T)+\varphi_n]} \tag{4.58}$$

Assume that the applied delay is equal to one-fourth of a line period (T_g) of the grid voltage

$$T = \frac{T_g}{4} = \frac{1}{2}\frac{\pi}{\omega} \tag{4.59}$$

Substituting (4.59) into (4.58), the delayed voltage vector is given by

$$\begin{aligned}\underline{e}_g^{(\alpha\beta)}(t-T_g/4) = E_{gp}e^{\jmath(\omega t-\pi/2+\varphi_p)} + E_{gn}e^{-\jmath(\omega t-\pi/2+\varphi_n)} = \\ -\jmath\big[E_{gp}e^{\jmath(\omega t+\varphi_p)} - E_{gn}e^{-\jmath(\omega t+\varphi_n)}\big]\end{aligned} \tag{4.60}$$

Combining (4.57) and (4.60), it is possible to extract the positive and negative component from the measured signal. This method is also called Delayed Signal Cancellation (DSC) method.

$$\begin{aligned}\underline{e}_{gp}^{(\alpha\beta)}(t) &= \frac{1}{2}\left(\underline{e}_g^{(\alpha\beta)}(t) + \jmath\underline{e}_g^{(\alpha\beta)}\big(t-\frac{T_g}{4}\big)\right) \\ \underline{e}_{gn}^{(\alpha\beta)}(t) &= \frac{1}{2}\left(\underline{e}_g^{(\alpha\beta)}(t) - \jmath\underline{e}_g^{(\alpha\beta)}\big(t-\frac{T_g}{4}\big)\right)\end{aligned} \tag{4.61}$$

where $\underline{e}_{gp}^{(\alpha\beta)}(t)$ and $\underline{e}_{gn}^{(\alpha\beta)}(t)$ are the voltage vectors of the positive and negative phase-sequence of the grid voltage and T_g is the period of the grid voltage [28]. The principle of the DSC technique can be understood by using the vector diagram shown in Figure 4.38. In the fixed $\alpha\beta$-coordinate system, the positive phase-sequence vector rotates with the grid frequency counterclockwise, while the negative rotates with the

same frequency clockwise. Delaying the grid voltage vector $\underline{e}_g^{(\alpha\beta)}(t)$ by a quarter of period yields

$$\underline{e}_{gp}^{(\alpha\beta)}(t) = \jmath \underline{e}_{gp}^{(\alpha\beta)}\left(t - \frac{T_g}{4}\right) \tag{4.62}$$

$$\underline{e}_{gn}^{(\alpha\beta)}(t) = -\jmath \underline{e}_{gn}^{(\alpha\beta)}\left(t - \frac{T_g}{4}\right) \tag{4.63}$$

Delaying the signal and by applying a 90° phase-shift, in appropriate direction, gives a vector composed by the same positive sequence component and a negative sequence component which is equal in value but opposite gain. Therefore, if this signal delayed by $T_g/4$ is subtracted from the measured grid voltage at time t, the positive sequence voltage will be removed, while if this signal is added the negative sequence voltage will be removed.

Applying Eqs.(4.61) correspond to averaging the input signal over a quarter of period, which gives a robust response. The drawback of this detection method is that it requires a quarter of cycle at the fundamental frequency for estimation.

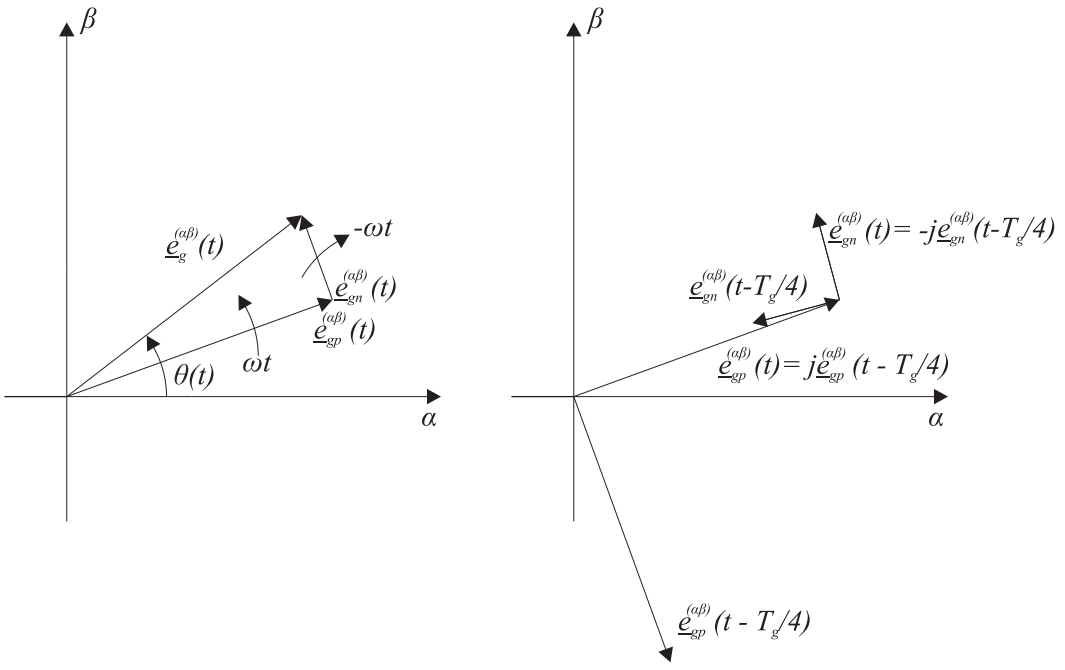

Figure 4.38: Vector diagram describing principle of DSC technique.

Equations 4.61 is then transformed to the $dq-$coordinate system in positive and negative SRF respectively as

$$\begin{aligned} \underline{e}_g^{(dqp)}(t) &= e^{-\jmath\theta(t)}\underline{e}_{gp}^{(\alpha\beta)}(t) \\ \underline{e}_g^{(dqn)}(t) &= e^{\jmath\theta(t)}\underline{e}_{gn}^{(\alpha\beta)}(t) \end{aligned} \tag{4.64}$$

The algorithm can also be described by a block diagram shown in Figure 4.39

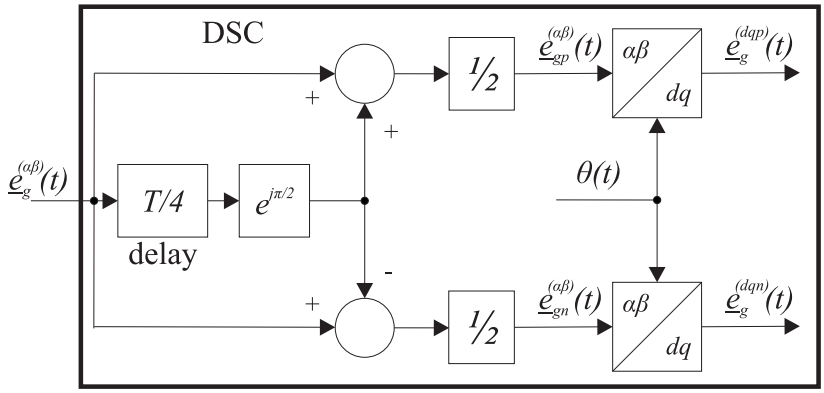

Figure 4.39: Block diagram of the separation of the *positive*− and *negative*−sequence components of the grid voltage.

Figure 4.40 shows the block diagram of the dual cascade controller

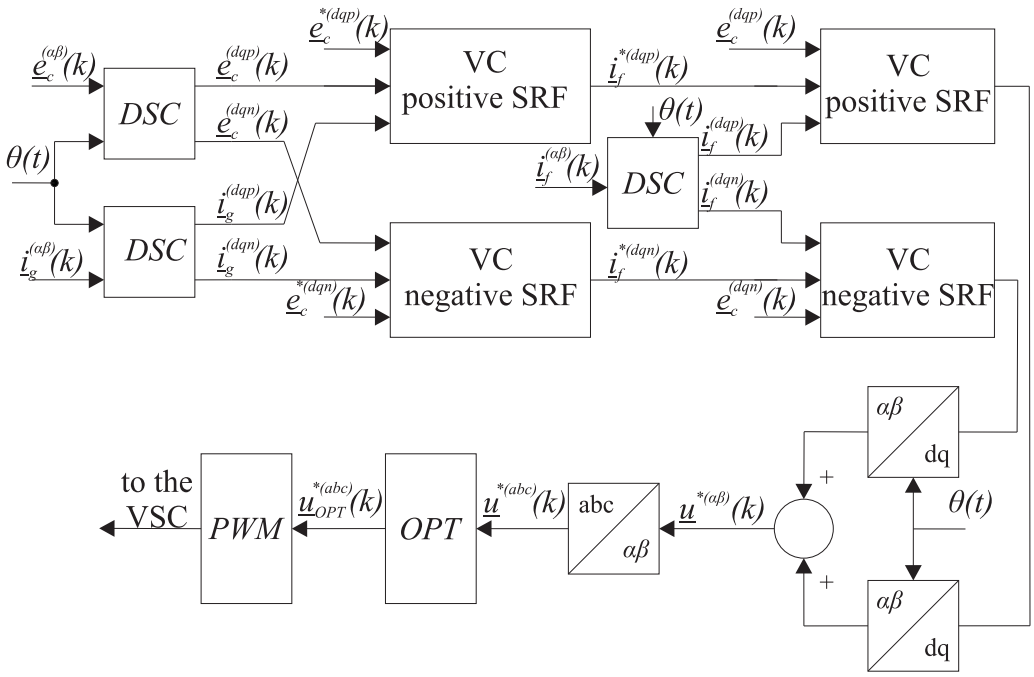

Figure 4.40: Block diagram of dual cascade controller.

Figure 4.41 shows that at time $t = 0.4s$ a two-phase to ground fault occurs in the grid causing an unbalanced 80% voltage dip with an unbalance of 4% and lasts for 100 ms. Due to the presence of a negative-sequence component during the dip, the grid voltages in the $dq-$coordinate system, without DSC, are affected by a 100 Hz oscillation, as shown in Figure 4.42. In Figure 4.43 and 4.44 is shown the grid voltages in the $dq-$coordinate system with DSC in the corresponding SRFs; it is possible to observe that after a transient, the components remain to constant value. This transient last a quarter of period of the grid frequency and it is the delay introduced by the DSC.

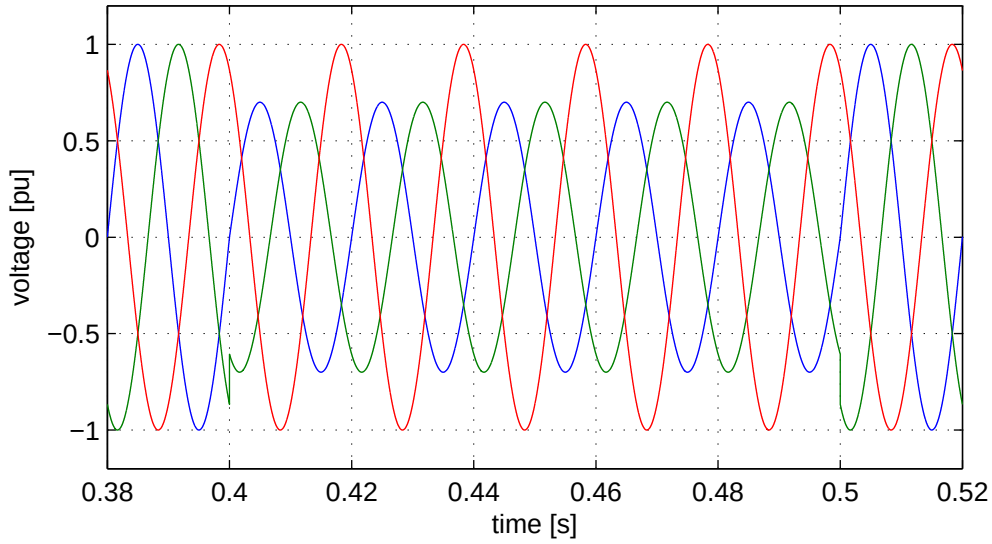

Figure 4.41: Simulated three-phase grid voltages during 70% voltage dip.

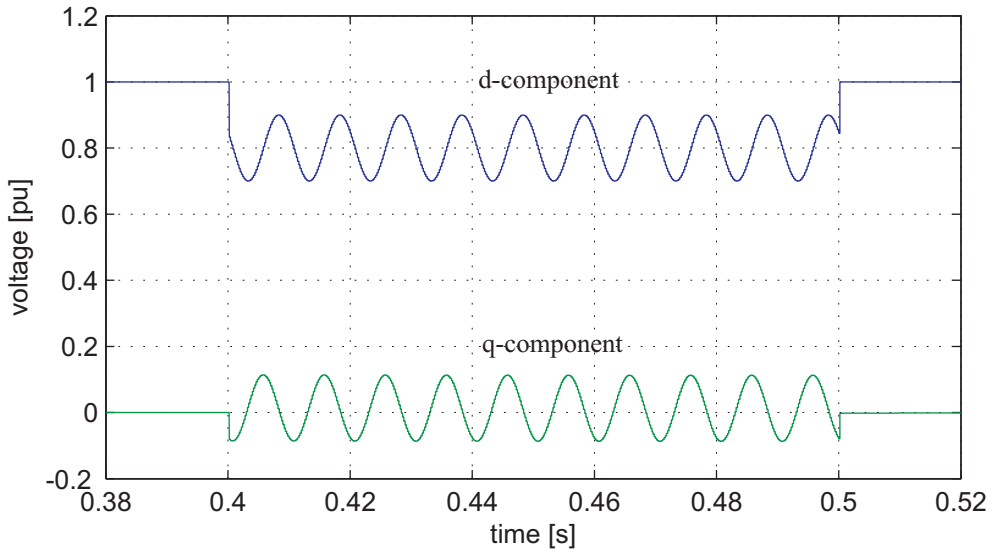

Figure 4.42: Simulated grid voltages in $dq-$system during 70% voltage dip without DSC.

Figure 4.45 shows the simulation result with DVCC and DVVC under balanced grid voltage when applying a step in the positive sequence $d-$voltage. At time $t = 0.2s$ a step in the positive sequence $d-$voltage has been applied, it is possible to notice a delay of a quarter of period of the grid frequency, caused by DSC, that lengthens the duration of the transient decreasing thus the performance of the control system.

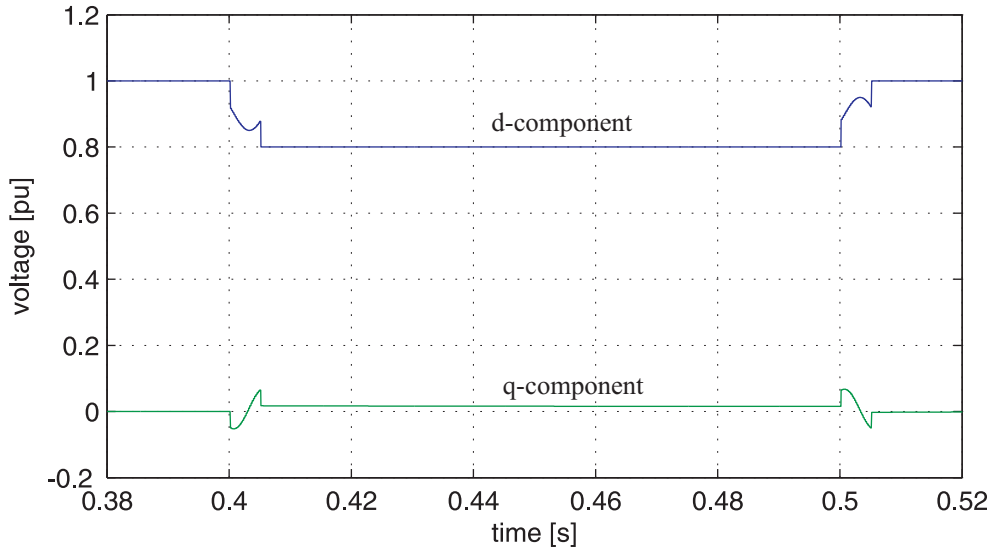

Figure 4.43: Simulated grid voltages in $dq-$system during 70% voltage dip with DSC - Positive SRF.

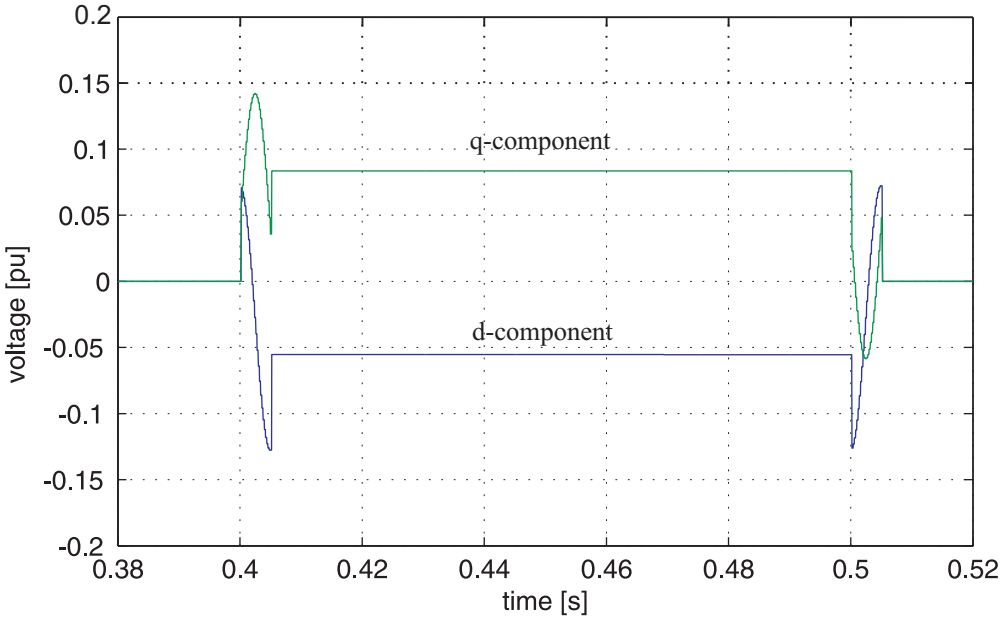

Figure 4.44: Simulated grid voltages in $dq-$system during 70% voltage dip with DSC - Negative SRF.

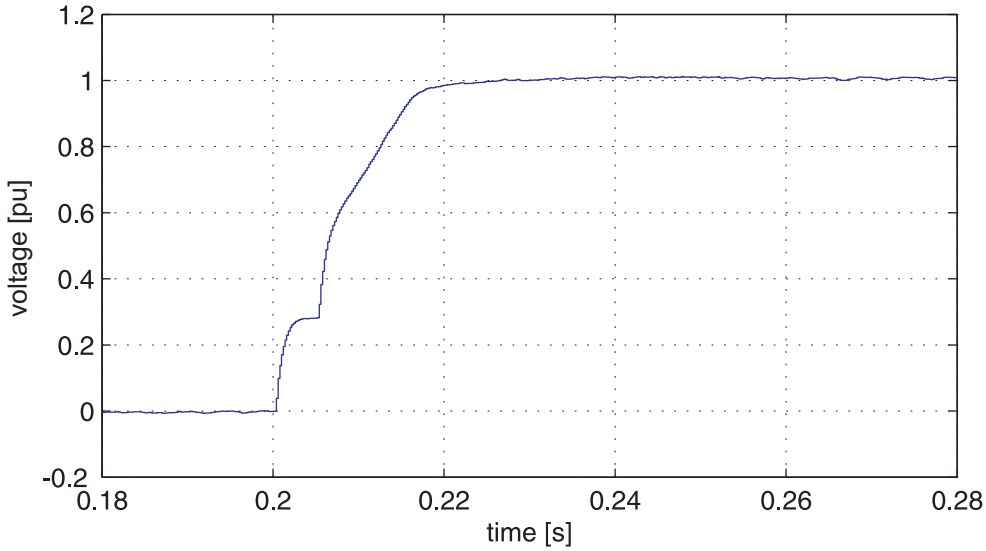

Figure 4.45: Simulated step in the positive sequence $d-$voltage.

4.7 DC-link model

In the actual installation the control system has to be completed with the DC controller. This controller regulates the energy exchange between the DC-side and the AC-side, moreover it regulates that the voltage across the DC-Capacitor is constant. All this is not the scope of this work.
The energy storage has been simulated with an ideal DC source and its discharge has been modelled introducing a high-pass filter on a d-component (active component) of current $\underline{i}_f(t)$ for positive sequence. A high-filter has a step response shown in Figure 4.47, thus it well simulates the discharge of the energy storage.

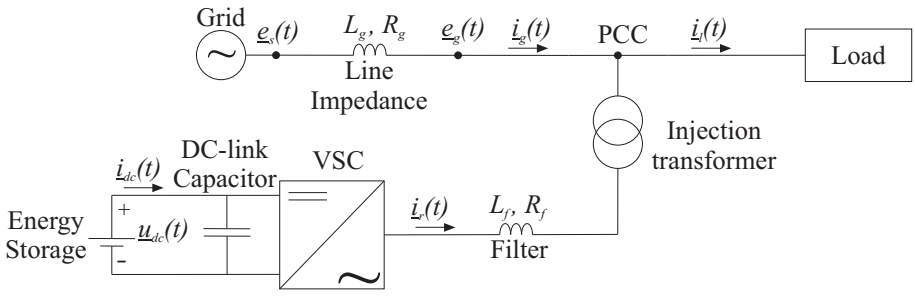

Figure 4.46: Single-line diagram of shunt-connected VSC.

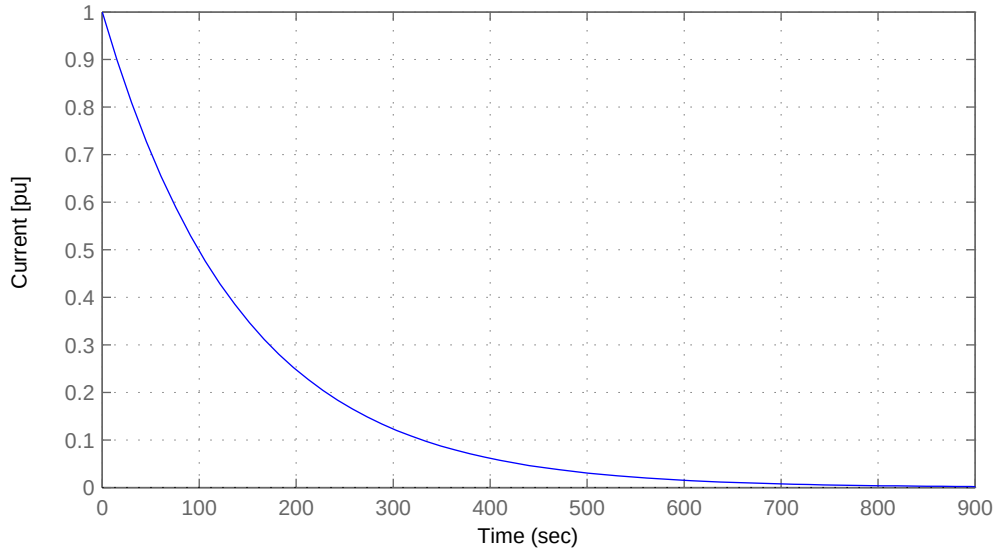

Figure 4.47: High-pass filter step response.

4.8 Conclusions

In this chapter the control system for the E-STATCOM for voltage dip mitigation has been derived. The vector current controller (VCC) and the vector voltage controller (VVC) have been designed and their behaviour has been studied. Steps in the reference voltage have been applied in order to test the dynamic performance of the system. The impact of controller bandwidths has been investigated.

Furthermore, the impact of inaccurate knowledge system parameters has been investigated. It has been shown that overestimated filter inductance leads to an increased overshoot that, for protection reasons, must be avoided. The purpose of this thesis is to compensate voltage dip. In the previous chapter it has been shown that the majority of the voltage dips are unbalanced. In this chapter has been shown a DSC method to extract the sequences. It has been demonstrated that, without DSC, the $dq-$voltages under unbalanced grid voltage are affected by an oscillation at double the power frequency. The dual cascade controller, where both voltages and currents are separated into their sequence components and two separate current controllers and two separate voltage controllers, is used. It shows a lower response due to delay introduced by the sequence separation.

In the next chapter the control system will be tested for voltage dip mitigation; simulations under balanced and unbalanced voltage dips will be carried out.

Chapter 5

Simulation Results

5.1 Introduction

In the previous chapter the control system for E-STATCOM has been presented. The control system has been derived for both balanced and unbalanced grid voltage conditions. This chapter will present the simulation results for the E-STATCOM when mitigating voltage dips. The control system will tested under symmetrical an unsymmetrical voltage dips when protecting a fixed RL-load and an induction motor.

The system has been tested by using the PSCAD/EMTCD and the control system has been implemented by using Fortran 90 language.

5.2 Mitigation of symmetrical voltage dips

The scheme used is displayed in Figure 5.1. System parameters are shown in Table 5.1. The transformer impedance is equal to 1 mH.

Table 5.1 System parameters.

Grid voltage	$E = 400$V=1pu	Base Power	$S = 59.3$kVA=1pu
Grid frequency	$f = 50$Hz	DC-link	$U_{dc} = 1.6$kV
Grid resistance	$R_g = 0.05\Omega$	Grid Inductance	$L_g = 2.1$mH
Filter resistance	$R_f = 0.0248\Omega$	Filter Inductance	$L_f = 2$mH
Load resistance	$R_l = 10.0\Omega$	Load Inductance	$L_l = 23.9$mH
Capacitor	$C = 720\mu$F		

The control system parameters are shown in Table.5.2. The three-phase grid voltages at the PCC are displayed in Figure 5.2 when E-STATCOM is off-line.

At $t = 0.5$ s, a three-phase fault occurs causing a 70% balanced voltage dip with 10^o phase-angle jump and lasts for 300 ms. All three phases drop from 1 pu to 0.7 pu. The grid voltages in the $dq-$coordinate system are displayed in Figures 5.3 and 5.4.

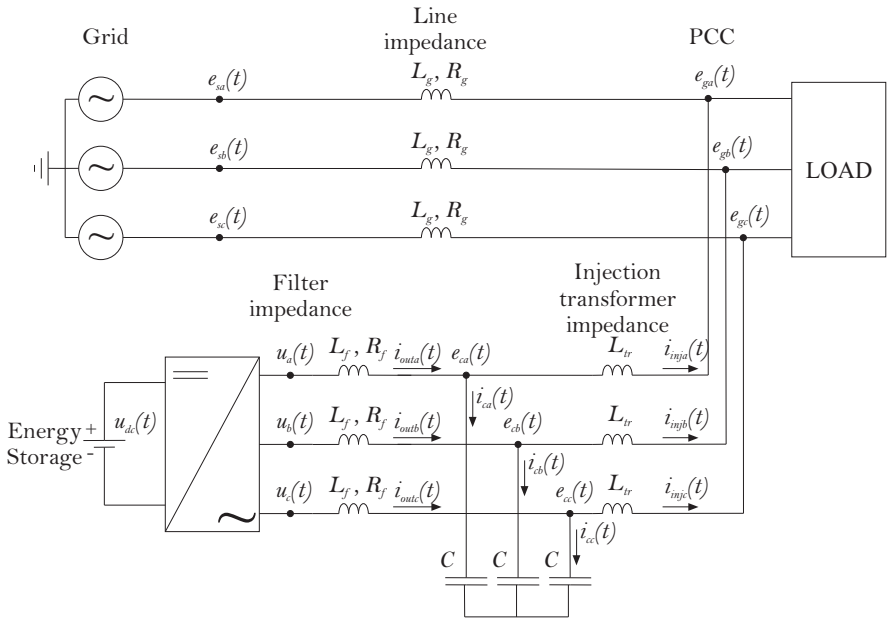

Figure 5.1: Scheme of shunt-connected VSC for voltage dip mitigation.

As shown, at $t = 0.5$ s the positive sequence d-component makes a step down from 1 pu to 0.7 pu, while, due to the phase-angle jump, the q-component goes from 0 pu to 0.01 pu, and then due to the PLL operations goes back to 0 pu. The negative sequence components of the grid voltage are both equal to zero before, during and after the dip, except a small transient due to the DSC.

Table 5.2 Controller parameters.

Voltage Controller.			
Bandwidth	$\alpha_{cv} = 2\pi 600 rad/sec$	Active damping	$G_a = 0.0027\Omega^{-1}$
Proportional gain	$k_{pv} = 2.71$	Integrator gain	$k_{iv} = 10.23$
Current Controller.			
Bandwidth	$\alpha_{cc} = 2\pi 1400 rad/sec$	Active damping	$R_a = 0.0\Omega$
Proportional gain	$k_{pv} = \alpha_{cc} 17.6$	Integrator gain	$k_{iv} = 0.0$

Figure 5.5 shows the resulting three-phase voltage over the capacitor, while Figures 5.6 and 5.7 show the voltage over the filter capacitor in $dq-$coordinate system when E-STATCOM is on-line. As it is possible to observe the voltage, after a small transient not visible in the figure due to the scaling, is kept constant to the pre-fault value. Figure 5.8 shows the resulting three-phase grid voltages, Figures 5.9 and 5.10 show the grid voltage in $dq-$coordinate system when E-STATCOM is on-line. From the figures it is possible to observe that, during the dip, the voltages are not constant and equal to 1 pu. This is due to the fact that in this simulation model the transformer impedance is not negligible as assume during the derivation of the voltage controller. In this simulated case , the grid voltages are acceptable because the RMS value is greater than 0.9 pu. However, it is important to observe that if the severity of the voltage dip increases and/or the grid impedance decreases, the voltage above the filter capacitor will be restored at pre-fault value but the voltage at PCC will be smaller than 0.9 pu.

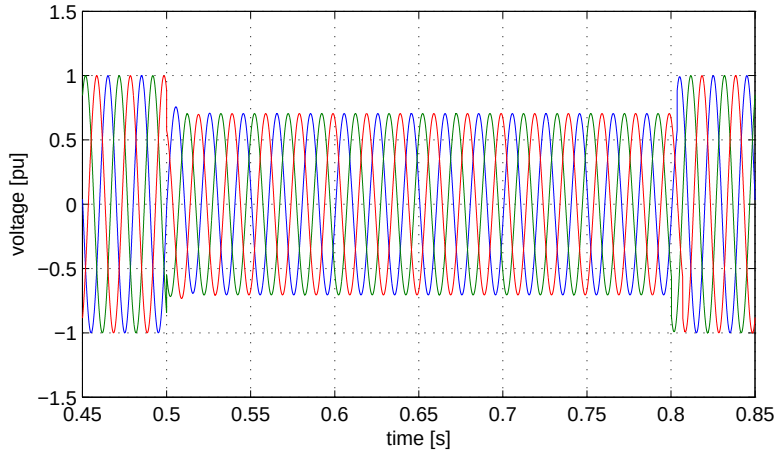

Figure 5.2: Simulated three-phase grid voltages during 70% balanced voltage dip with 10° phase-angle jump.

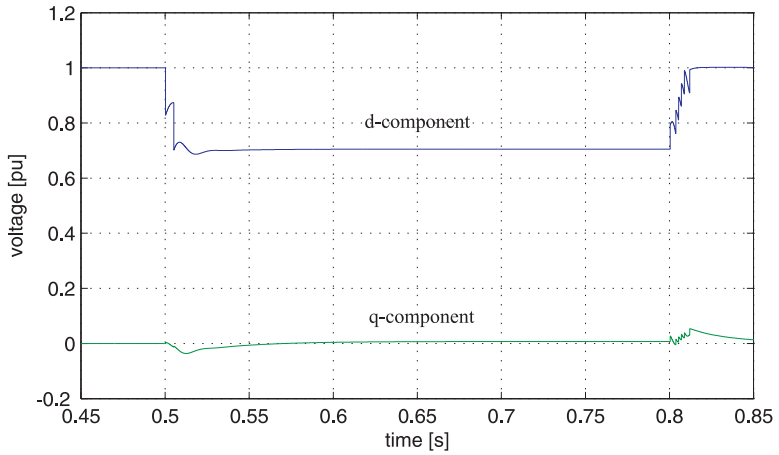

Figure 5.3: Simulated grid voltages in $dq-$coordinate system during 70% balanced voltage dip with 10° phase-angle jump. Positive sequence in positive SRF.

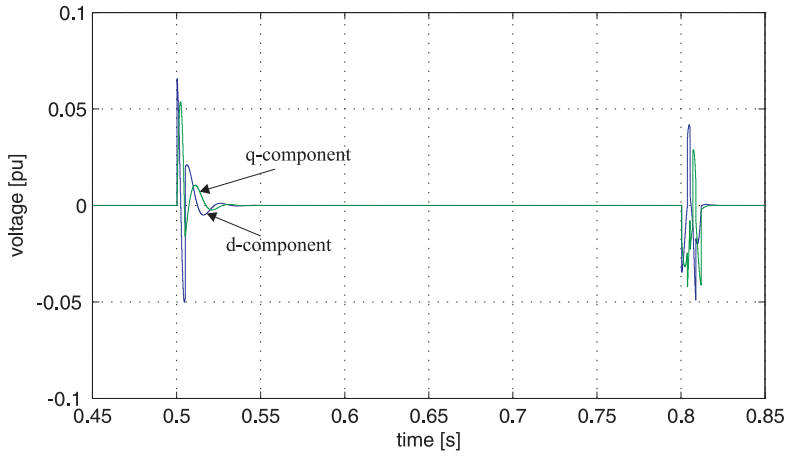

Figure 5.4: Simulated grid voltages in $dq-$coordinate system during 70% balanced voltage dip with 10° phase-angle jump. Negative sequence in negative SRF.

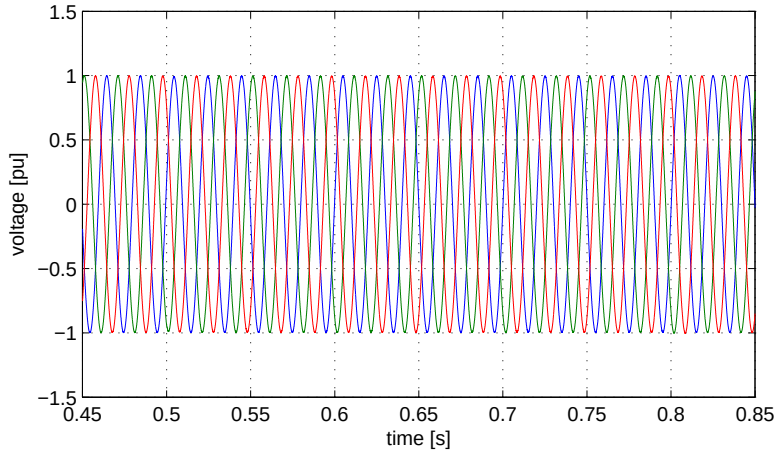

Figure 5.5: Simulated three-phase voltages over the capacitor during voltage dip. Voltage dip mitigation is used.

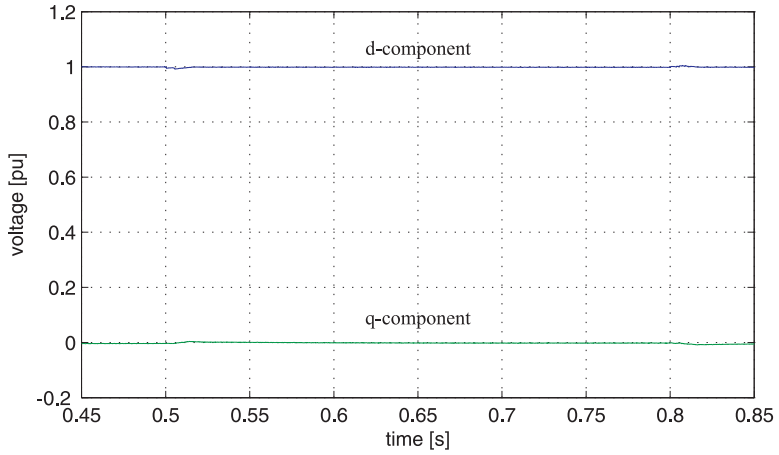

Figure 5.6: Simulated voltages over the capacitor in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used. Positive sequence in positive SRF.

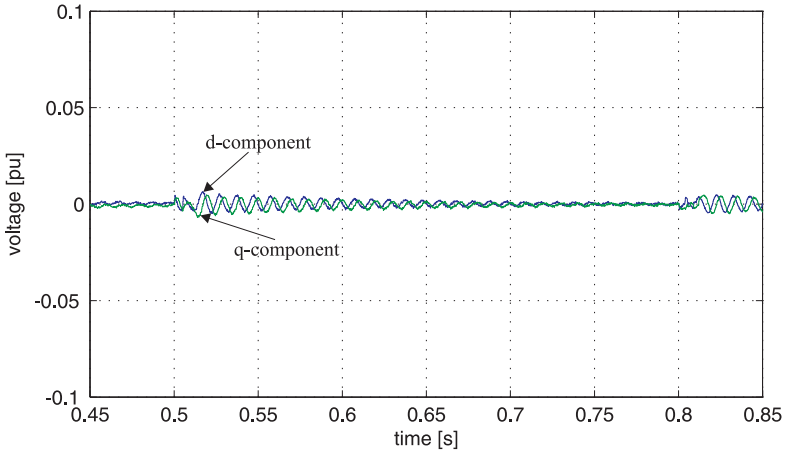

Figure 5.7: Simulated voltages over the capacitor in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used. Negative sequence in negative SRF.

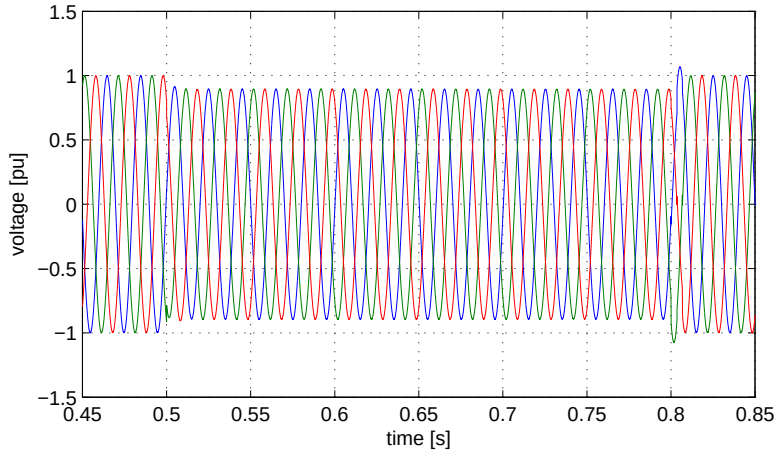

Figure 5.8: Simulated three-phase grid voltages during voltage dip. Voltage dip mitigation is used.

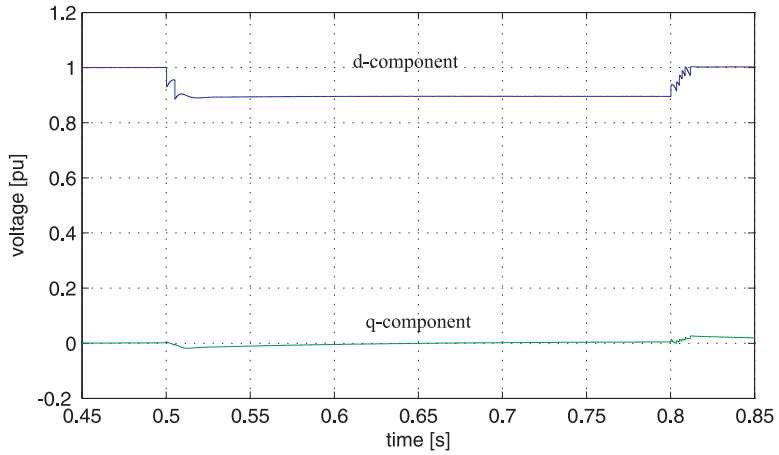

Figure 5.9: Simulated grid voltages in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used. Positive sequence in positive SRF.

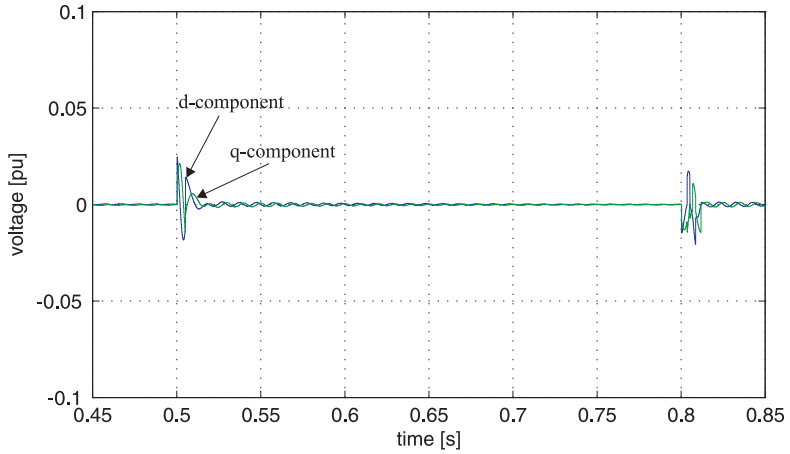

Figure 5.10: Simulated grid voltages in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used. Negative sequence in negative SRF.

5.3 Mitigation Improvement

In the previous section it has been shown that, being the transformer impedance not negligible, the grid voltage cannot be maintained to its pre-fault value. To restore the grid voltages at pre-fault values, the voltages over the capacitor must be incremented to take into account the voltage drop over the injection transformer. It is possible to write that

$$\begin{aligned} \underline{e}_{cp}^{(dq)}(t) &= \underline{e}_{gp}^{*(dq)} + L_{tr}\frac{d\underline{i}_{gp}^{(dq)}(t)}{dt} + \jmath\omega L_{tr}\underline{i}_{gp}^{(dq)}(t) \\ \underline{e}_{cn}^{(dq)}(t) &= \underline{e}_{gn}^{*(dq)} + L_{tr}\frac{d\underline{i}_{gn}^{(dq)}(t)}{dt} - \jmath\omega L_{tr}\underline{i}_{gn}^{(dq)}(t) \end{aligned} \tag{5.1}$$

where $e_{gp}^{*(dq)}$ and $e_{gn}^{*(dq)}$ are the pre-fault grid voltages in $dq-$coordinate system.

Assuming steady-state compensation and splitting up into two equations representing the $d-$ and $q-$component separately, (5.1) can be written as

$$\begin{aligned} e_{cdp}^{*}(t) &= e_{gdp}^{*} - \omega L_{tr} i_{gqp}(t) \\ e_{cqp}^{*}(t) &= e_{gqp}^{*} + \omega L_{tr} i_{gdp}(t) \\ e_{cdn}^{*}(t) &= e_{gdn}^{*} + \omega L_{tr} i_{gqn}(t) \\ e_{cqn}^{*}(t) &= e_{gqn}^{*} - \omega L_{tr} i_{gdn}(t) \end{aligned} \tag{5.2}$$

Figures 5.11 to 5.19 show the grid voltages, the capacitor voltages and the VSC output currents in a three-phase system and $dq-$coordinate system, respectively when the new reference values as in (5.2) are used. The grid voltages in $dq-$coordinate after a transient, due to DSC and to control system response, remain constant at pre-fault values. As expected, compared with the previous case (see Figures 5.6 and 5.7), the voltages over the capacitor in $dq-$coordinate system are increased during the dip. In particular the $d-$component in positive SRF makes a step from 1.0 pu to 1.2 pu, while the $q-$component in positive SRF makes a step from -0.05 pu to 0.05 pu; the negative value of $q-$component before the dip is due to the difference between the argument of the vector $\overline{E}_g$ and the argument of the vector $\overline{E}_c$.

Although acceptable in steady state, from the obtained results it is possible to note that the assumption of steady-state compensation results in a not high dynamic performance of the control system. In order to increase the performance it is necessary to consider and implement the derivative terms in (5.1), which was neglected in (5.2). However, implementation of the derivative terms causes some problems in a control algorithm; eq.(5.3) represents an approximation of derivative term (forward difference - Euler's method)

$$\frac{dx(t)}{dt} \approx \frac{x(k) - x(k-1)}{T_s} \tag{5.3}$$

From eq.(5.3), the derivative term is sensitive to variation of the input, even if the input is constant the presence of the ripple and of the noise, it results in a wrong calculation of the derivative term.

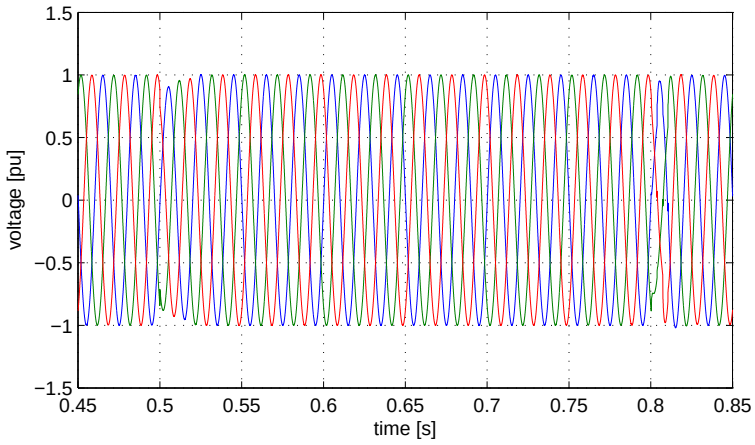

Figure 5.11: Simulated three-phase grid voltages during voltage dip. Voltage dip mitigation is used with new voltage references.

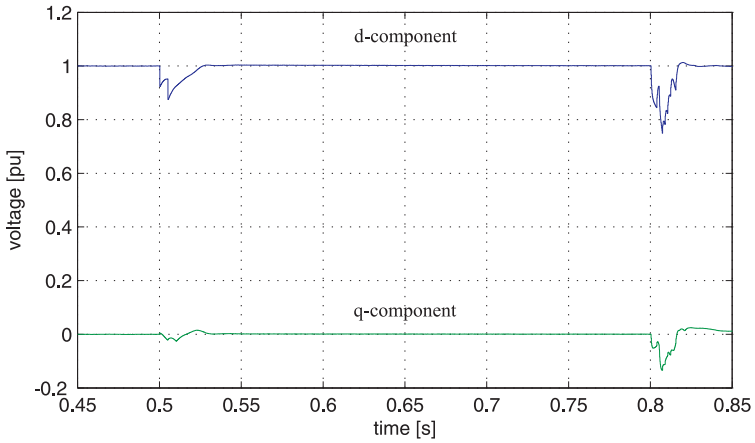

Figure 5.12: Simulated grid voltages in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references. Positive sequence in positive SRF.

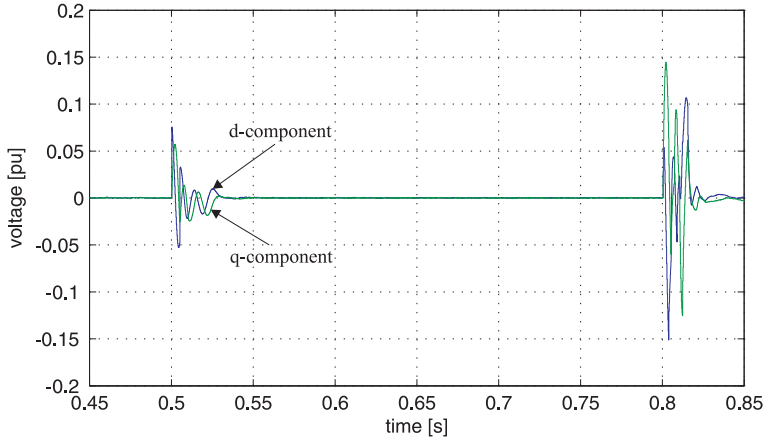

Figure 5.13: Simulated grid voltages in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references. Negative sequence in negative SRF.

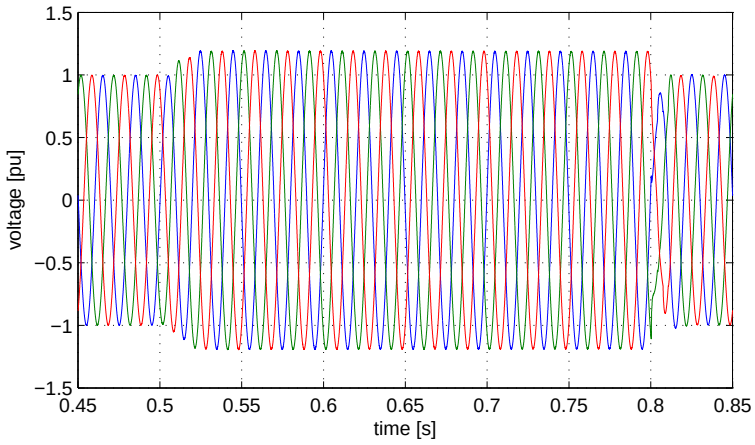

Figure 5.14: Simulated three-phase voltages over the capacitor during voltage dip. Voltage dip mitigation is used with new voltage references.

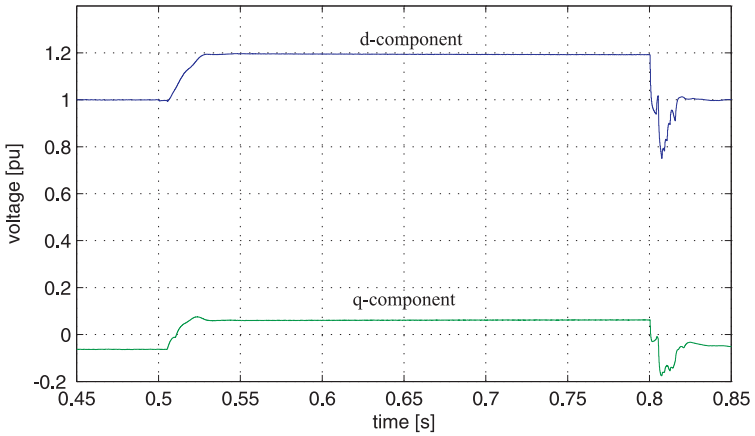

Figure 5.15: Simulated voltages over the capacitor in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references. Positive sequence in positive SRF.

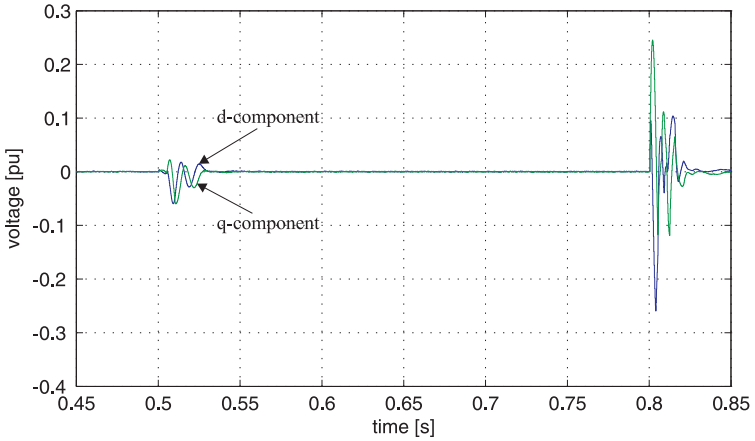

Figure 5.16: Simulated voltages over the capacitor in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references. Negative sequence in negative SRF.

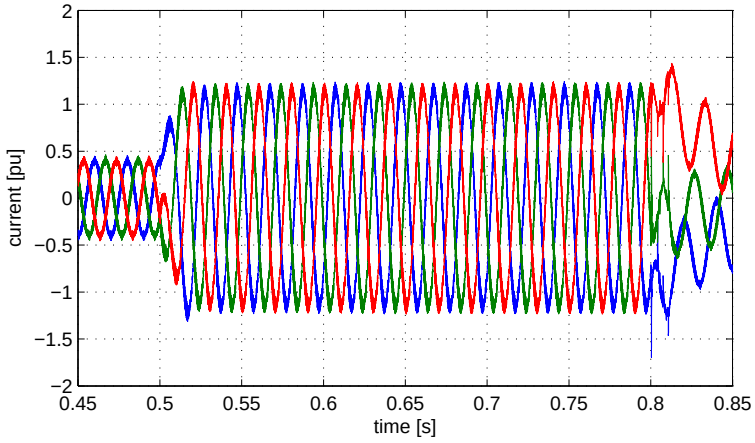

Figure 5.17: Simulated three-phase VSC output currents during voltage dip. Voltage dip mitigation is used with new voltage references.

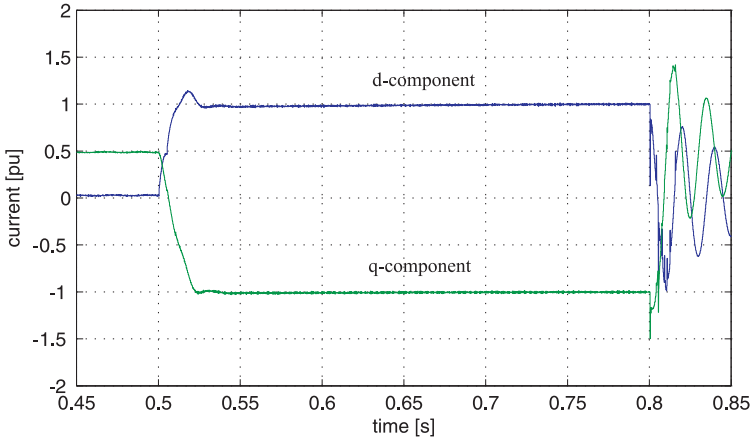

Figure 5.18: Simulated VSC output currents in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references. Positive sequence in positive SRF.

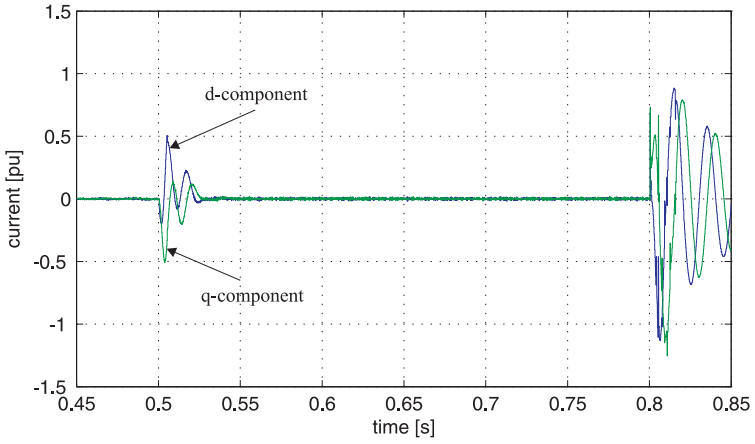

Figure 5.19: Simulated VSC output currents in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references. Negative sequence in negative SRF.

An alternative way to implement the derivative term is to use this transfer function

$$G_d(s) = \frac{s}{1 + sT} \tag{5.4}$$

In Figure 5.20 is shown the Bode diagram of the derivative term and the transfer function (5.4). It is possible to observe that the transfer function G_d has the same behavior of the derivative term at low frequencies (depending on the time constant T) but for the high frequencies the gain remains constant, decreasing the amplification of the noise.

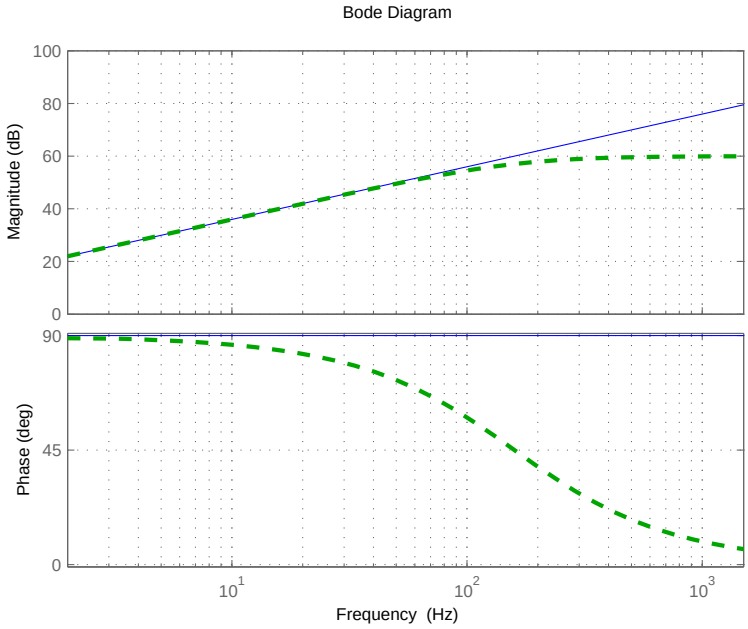

Figure 5.20: Bode diagram of the derivative term (solid) and the method used for its implementation (dash).

Figures 5.21 to 5.29 show the grid voltage, the capacitor voltage and the VSC output currents in a three-phase system and $dq-$coordinate system, respectively, when also the derivative term of the voltage drop over the transformer is included in the calculation of the reference capacitor voltage. From the comparison with the previous figures it is possible to observe that by using of transfer function $G_d(s)$ the performance of the control system increase. In particular the rise time decrease from 0.025 s to 0.01 s (0.5 cycle). Only a small transient, due to the DSC, can be observed in the grid voltages.

It is possible to observe that the VSC output currents increase much. In particular $d-$component of the positive sequence makes a step from 0.031 pu to 0.89 pu while $q-$component of the positive sequence makes a step from 0.55 pu to -0.87 pu. This results in that it needs a large amount of current, and considering the eqs.(A.18) and (A.19) in Appendix A, a large amount of active and reactive power to mitigate a 70% voltage dip with 10° phase-angle jump.

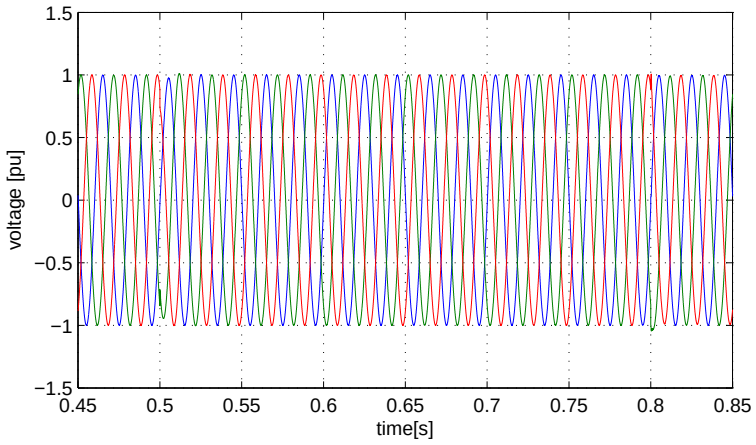

Figure 5.21: Simulated three-phase grid voltages during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms.

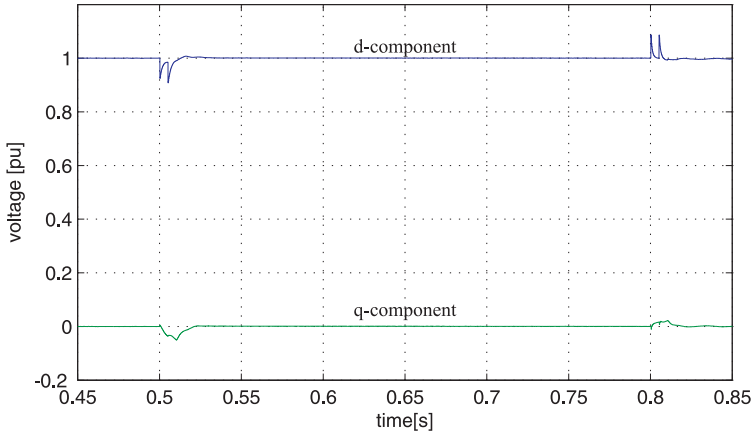

Figure 5.22: Simulated grid voltages in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms. Positive sequence in positive SRF.

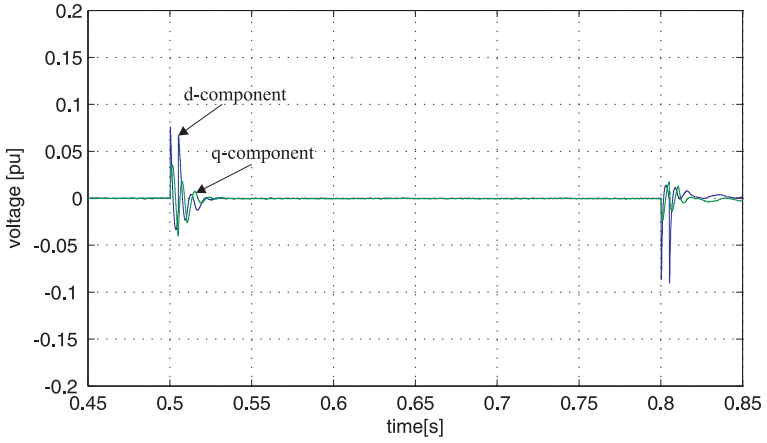

Figure 5.23: Simulated grid voltages in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms. Negative sequence in negative SRF.

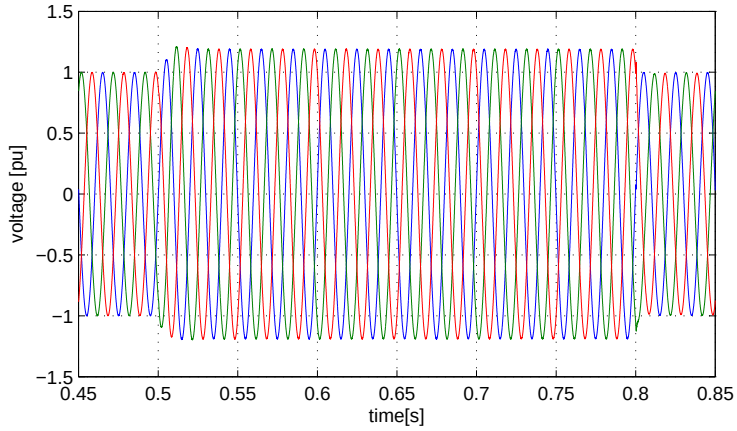

Figure 5.24: Simulated three-phase voltages over the capacitor during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms.

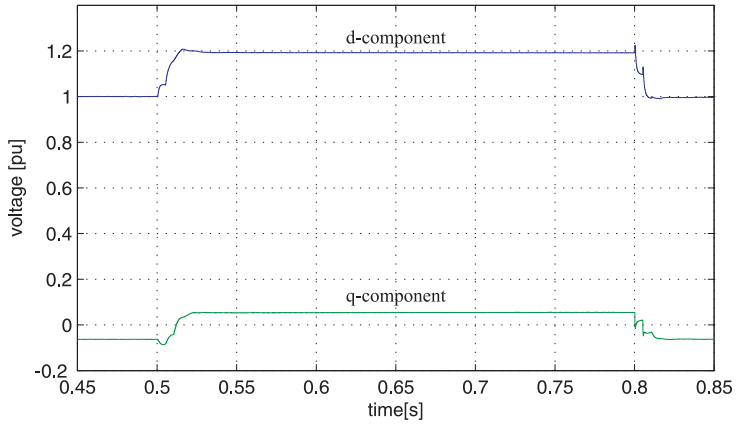

Figure 5.25: Simulated voltages over the capacitor in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms. Positive sequence in positive SRF.

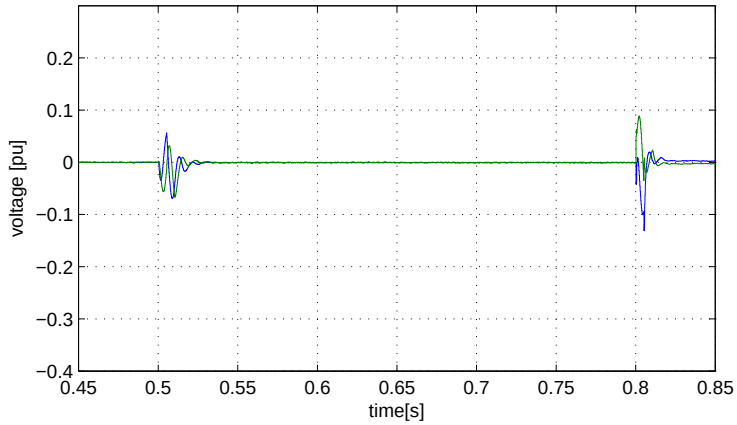

Figure 5.26: Simulated voltages over the capacitor in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms. Negative sequence in negative SRF.

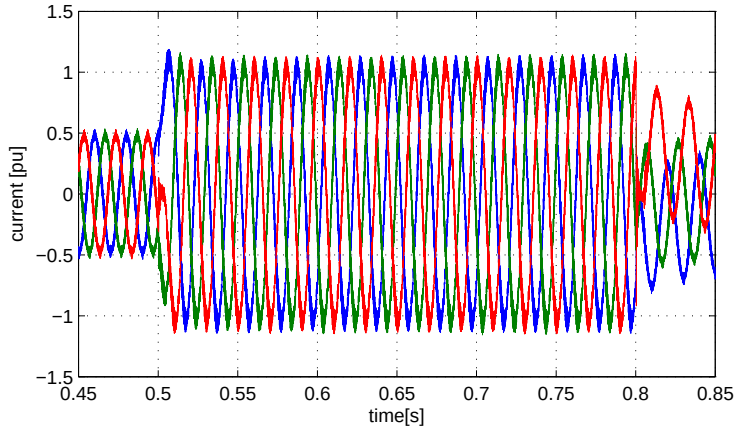

Figure 5.27: Simulated three-phase VSC output currents during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms.

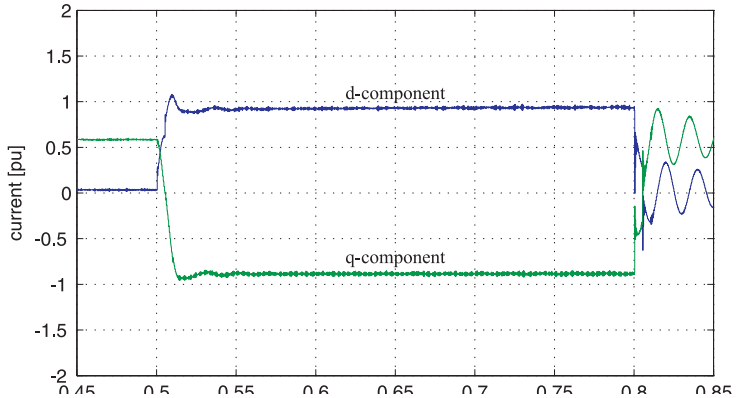

Figure 5.28: Simulated VSC output currents in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms. Positive sequence in positive SRF.

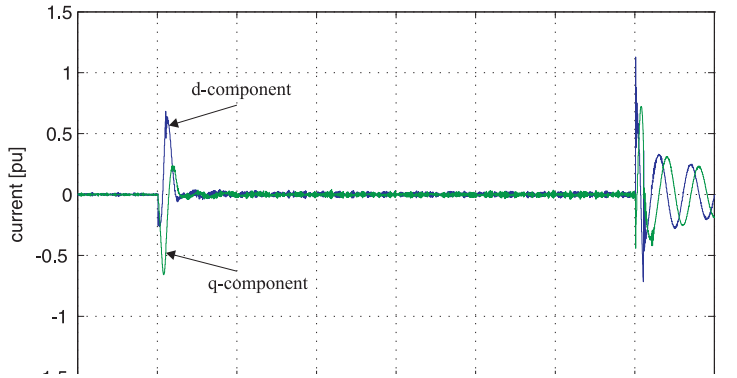

Figure 5.29: Simulated VSC output currents in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms. Negative sequence in negative SRF.

The grid voltages in $dq-$coordinate system for both sequences are affected by two identical transient spikes with 5 ms in between. It then takes 5 ms more to restore the voltage exactly to the pre-fault value. This behavior is due to the use of DSC for sequence separation. Figure 5.30 and 5.31 show the restored grid voltages without the use of DSC. It is possible to observe that the performance increases and that the damping decreases. This is due to the more severe voltage variation seen by the control algorithm when the DSC is not used (see Figure 5.31).

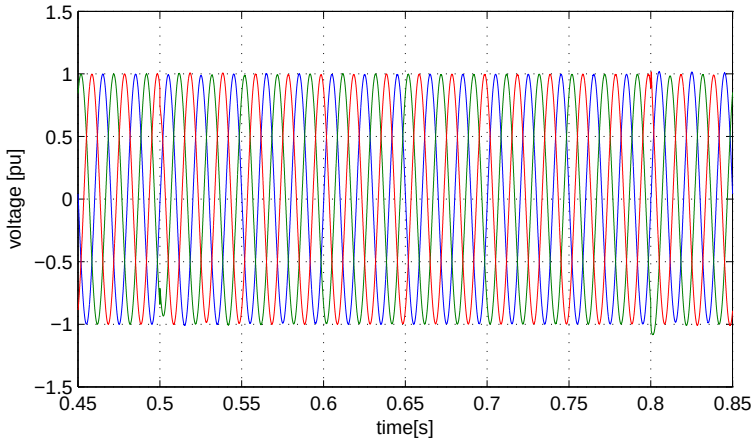

Figure 5.30: Simulated three-phase grid voltages during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms and without the DSC.

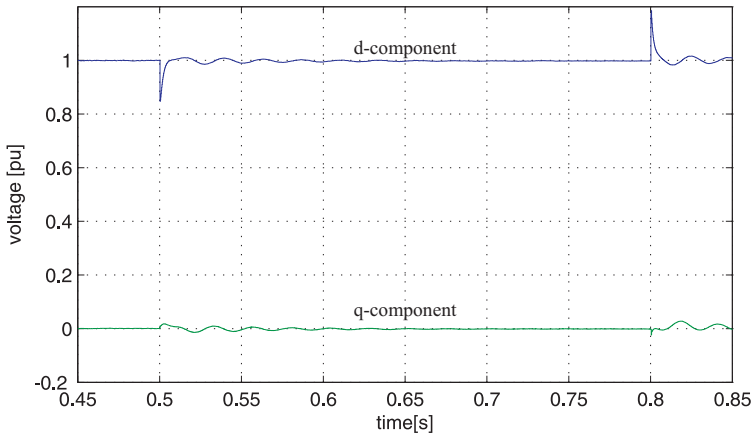

Figure 5.31: Simulated grid voltages in $dq-$coordinate system during voltage dip. Voltage dip mitigation is used with new voltage references considering the derivative terms and without the DSC.

5.4 Mitigation of unsymmetrical voltage dips

The system has also been tested under unsymmetrical voltage dips to protect a RL-load. The three-phase grid voltages at PCC are displayed in Figure 5.32. At $t = 0.5$ s, a single-phase fault occurs in the grid causing a 80% unbalanced voltage dip with unbalance of 11.55% that lasts for 300 ms. As a result, phase a drop from 1 pu to 0.7 pu while phases b and c remain constant and equal to 1 pu. The positive and negative sequence of the grid voltages in the $dq-$coordinate system in positive and negative SRFs are displayed in Figures 5.33 and 5.34, respectively. As shown, at $t = 0.5$ s the positive sequence d-component makes a step down from 1 pu to 0.8 pu, while the q-component goes from 0 pu to 0.01 pu and than goes to 0 due to PLL. The negative sequence components of the grid voltage are both equal to zero before and after the dip, negative $d-$component makes a step from 0 pu to -0.012 pu while negative $q-$component makes a step from 0 pu to 0.11 pu during the dip. By the comparison with the previous case studied (balanced voltage dip), it is possible to observe that the negative sequence component of the grid voltage is not equal to zero; this is due to the unbalanced voltage dip.

The grid voltages are completely restored to the pre-fault value, as shown in Figure 5.35. Figures 5.36 and 5.37 show the restored positive and negative sequences of the grid voltages in the corresponding SRFs respectively. After a small transient, all coordinates remain constant to pre-fault values.

It is possible to clearly notice that an unbalanced voltages is need over the capacitor to compensate the unbalanced voltage dip at the PCC (see Figure 5.38). Figures 5.39 and 5.40 show the positive and negative sequence voltage over the capacitor in $dq-$coordinate system in positive and negative SRFs respectively. Positive sequence of the voltages over the capacitor in $dq-$coordinate in positive SRF system increased during the dip. In particular the $d-$component makes a step from 1.0 pu to 1.13 pu, while the $q-$component makes a step from -0.05 pu to -0.01 pu. The $d-$component of negative sequence in negative SRF of the voltages over the capacitor increased during the dip, with a step from 0 pu to -0.016 pu, while the $q-$component of negative sequence in negative SRF makes a step from 0 pu to -0.067 pu.

Figures 5.41 to 5.43 shown the VSC output currents in three-phase system, positive sequence $dq-$coordinate system in positive SRF and negative sequence $dq-$coordinate system in negative SRF. Obviously in order to mitigate an unbalanced voltage dip, an unbalanced VSC output currents must be produced.

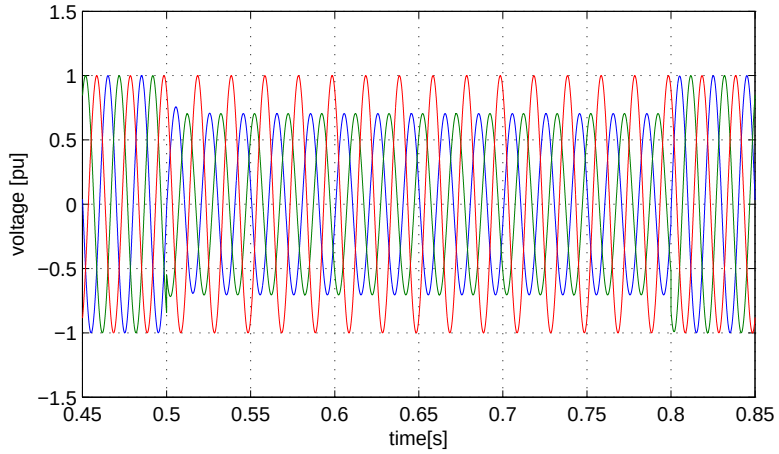

Figure 5.32: Simulated three-phase grid voltages during 80% with unbalance of 11.55%.

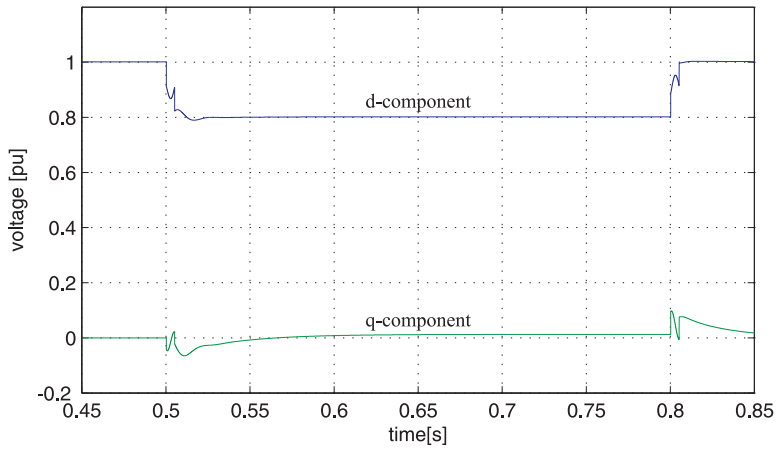

Figure 5.33: Simulated grid voltages in $dq-$coordinate system during 80% with unbalance of 11.55%. Positive sequence in positive SRF.

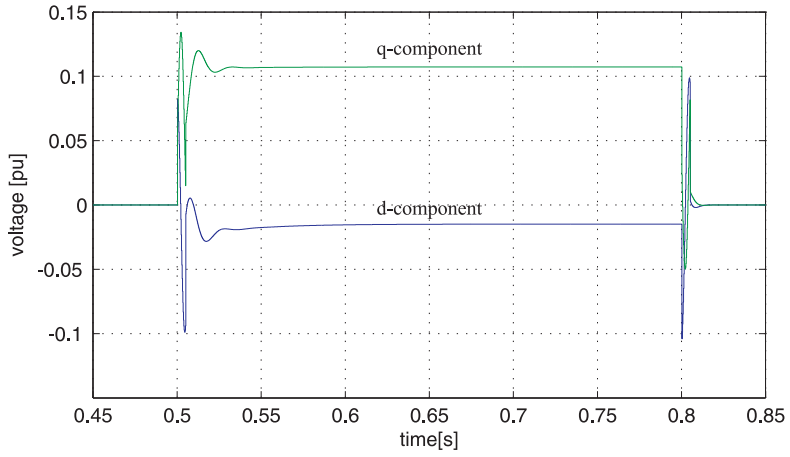

Figure 5.34: Simulated grid voltages in $dq-$coordinate system during 80% with unbalance of 11.55%. Negative sequence in negative SRF.

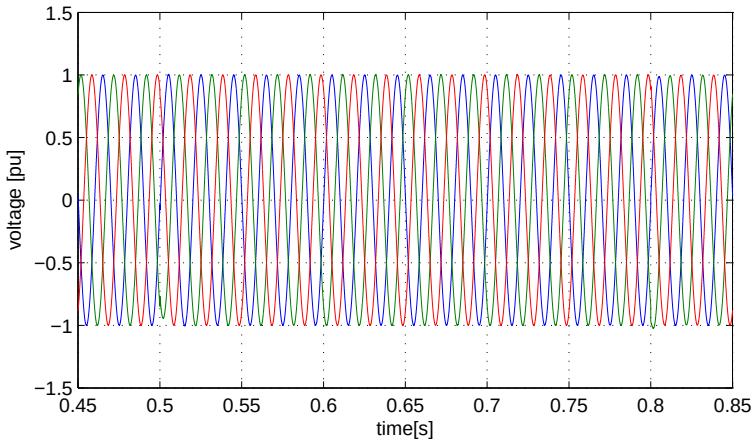

Figure 5.35: Simulated three-phase grid voltages during unbalanced voltage dip. Voltage dip mitigation is used.

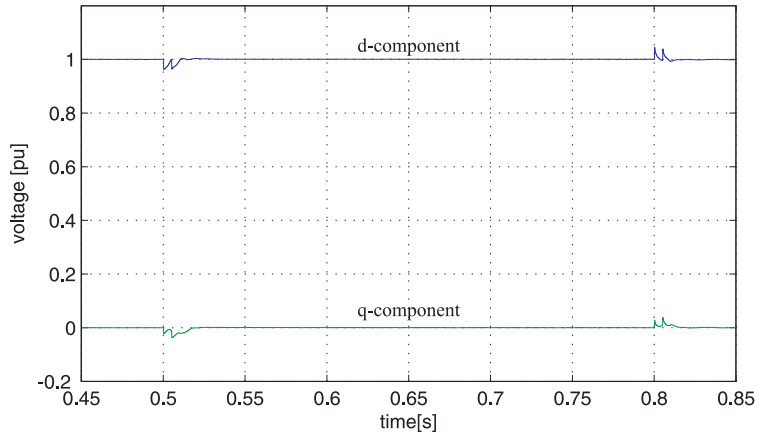

Figure 5.36: Simulated grid voltages in $dq-$coordinate system during unbalanced voltage dip. Voltage dip mitigation is used. Positive sequence in positive SRF.

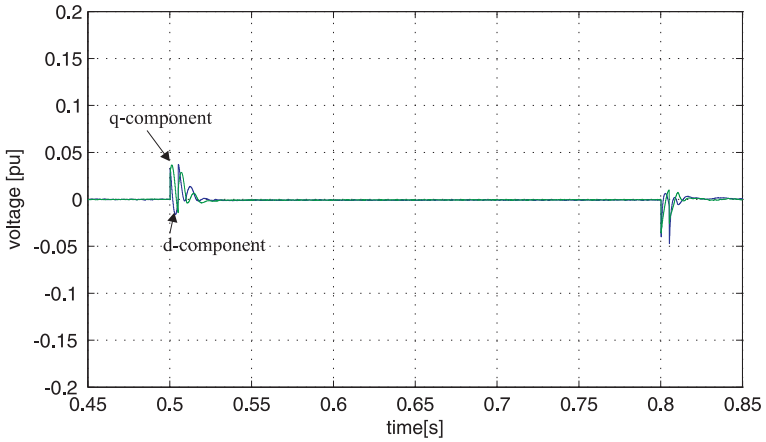

Figure 5.37: Simulated grid voltages in $dq-$coordinate system during unbalanced voltage dip. Voltage dip mitigation is used. Negative sequence in negative SRF.

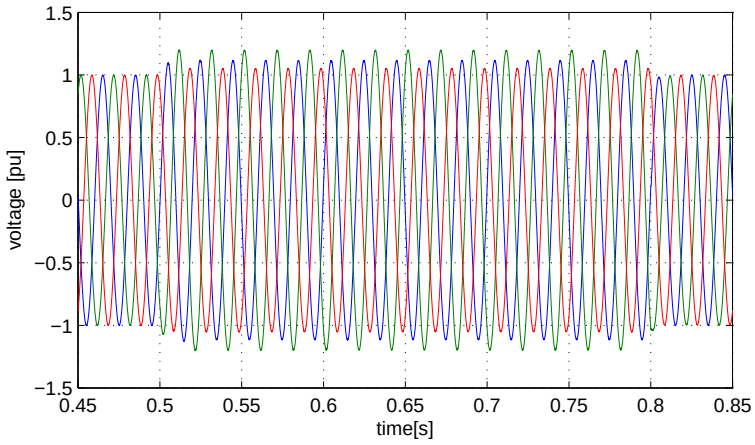

Figure 5.38: Simulated three-phase voltages over the capacitor during unbalanced voltage dip. Voltage dip mitigation is used.

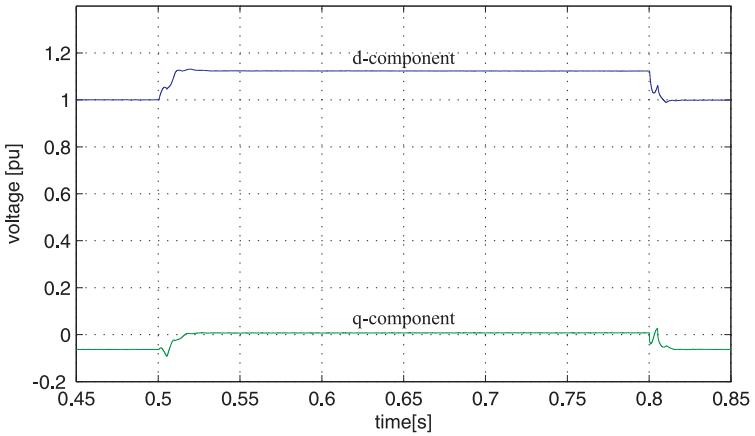

Figure 5.39: Simulated voltages over the capacitor in $dq-$coordinate system during unbalanced voltage dip. Voltage dip mitigation is used. Positive sequence in positive SRF.

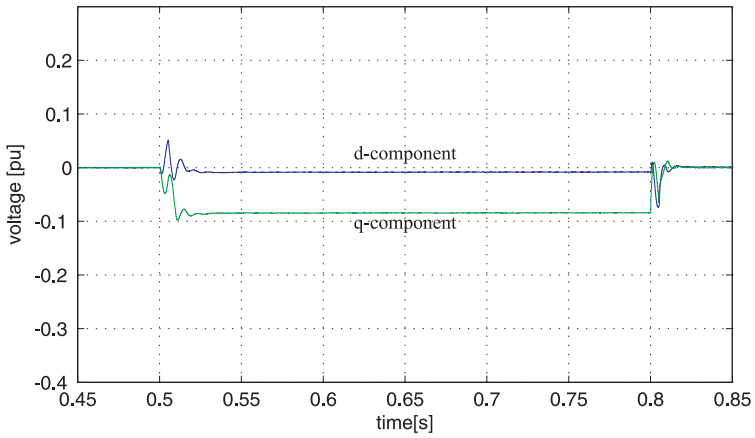

Figure 5.40: Simulated voltages over the capacitor in $dq-$coordinate system during unbalanced voltage dip. Voltage dip mitigation is used. Negative sequence in negative SRF.

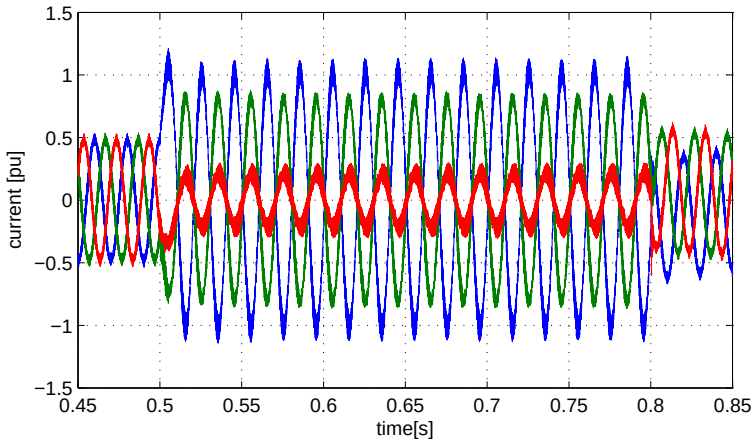

Figure 5.41: Simulated three-phase VSC output currents during unbalanced voltage dip. Voltage dip mitigation is used.

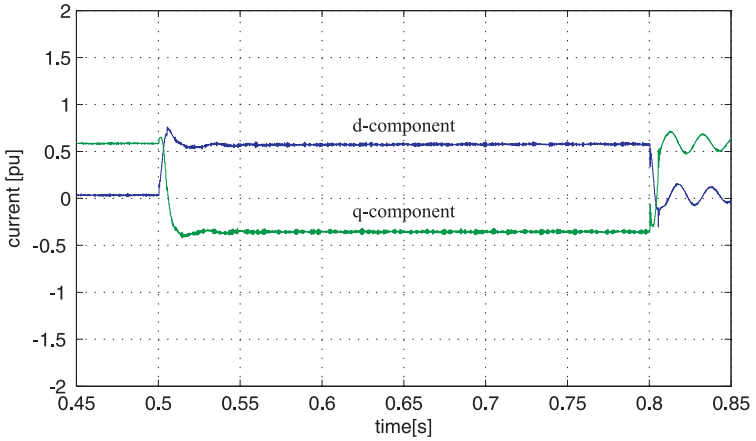

Figure 5.42: Simulated VSC output currents in $dq-$coordinate system during unbalanced voltage dip. Voltage dip mitigation is used. Positive sequence in positive SRF.

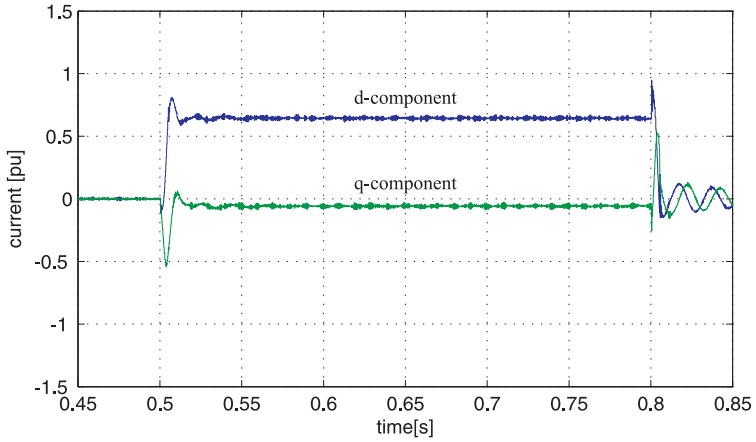

Figure 5.43: Simulated VSC output currents in $dq-$coordinate system during unbalanced voltage dip. Voltage dip mitigation is used. Negative sequence in negative SRF.

5.5 Induction machine load

The performance of the system has also been tested for protection of an induction machine. The induction machine is a sensitive load, a few cycle voltage dip can force it to stall. It is also important to study how the system operates with this type load because in this case is important to see the impact of the back emf. The electrical scheme of the grid with the E-STATCOM installed to protect the induction machine is shown in Figure 5.44. The same system and control parameters as for the previous cases have been used. Parameters of the simulated induction machine are displayed in Table 5.3. A constant torque, equal to 197 Nm has been applied to the rotor shaft, resulting in 0.68 pu load level.

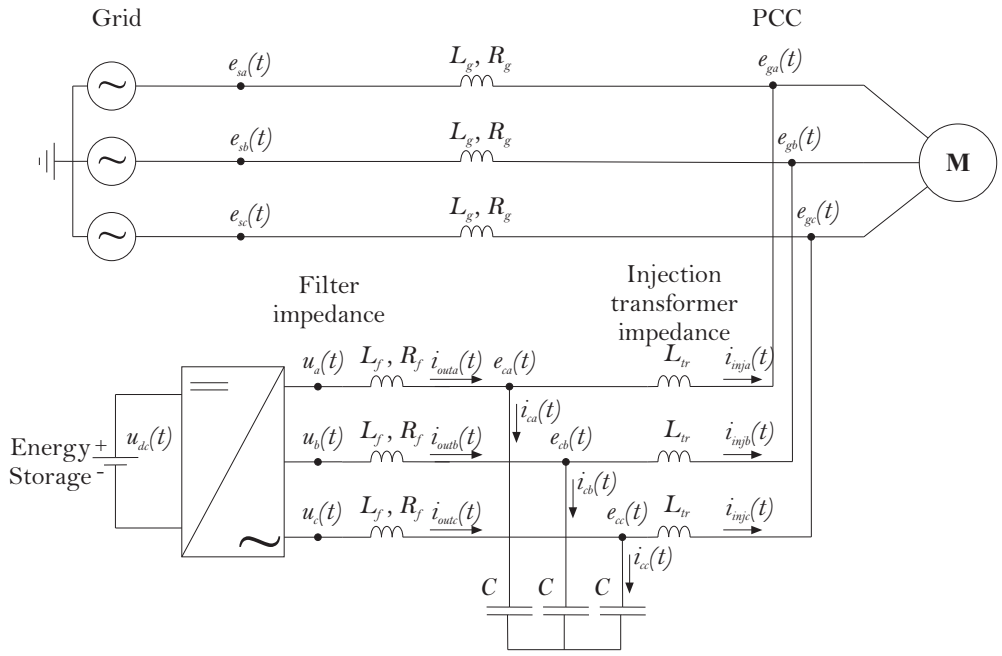

Figure 5.44: Scheme of shunt-connected VSC and machine load.

Table 5.3 induction machine parameters.

Rated power	60hp = 44.76 kW	Rated voltage	400 V
Rated frequency	50Hz	Number of poles	2
Rated speed	1470 rpm		

For this type of load, a three-phase voltage dip has been considered. The three-phase grid voltages at the PCC are displayed in Figure 5.45. At $t = 1.3$ s, a three-phase fault occurs causing a 70% balanced voltage dip with 10° phase-angle jump and lasts for 300 ms. The sequence components of the grid voltage in the dq-coordinate system are shown in Figures 5.46 and 5.47 (E-STATCOM is off-line).

As shown, during the dip the $dq-$components of the positive sequence don't remain constant; when the dip starts, due to the back-emf of the machine, the machine starts to demand reactive power from the grid resulting in a voltage decrease at PCC.

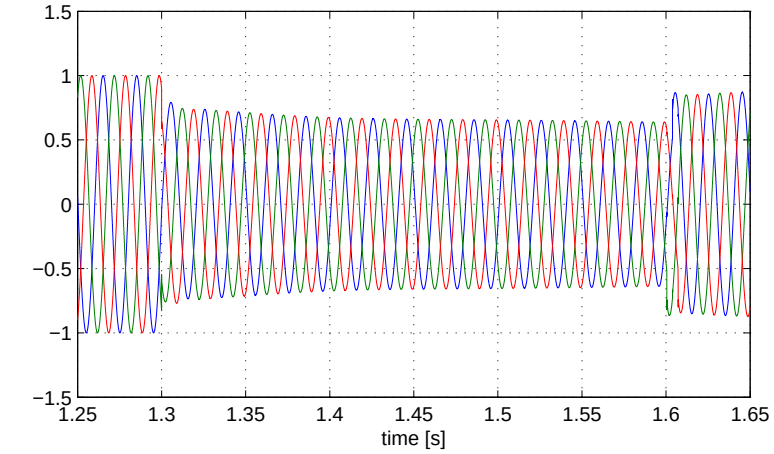

Figure 5.45: Simulated three-phase grid voltages during 70% balanced voltage dip with 10° phase-angle jump.

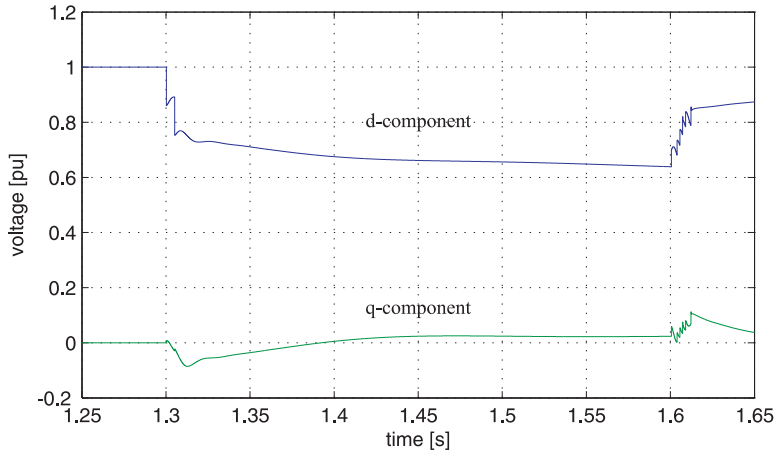

Figure 5.46: Simulated grid voltages in $dq-$coordinate system during 70% balanced voltage dip with 10° phase-angle jump. Positive sequence in positive SRF.

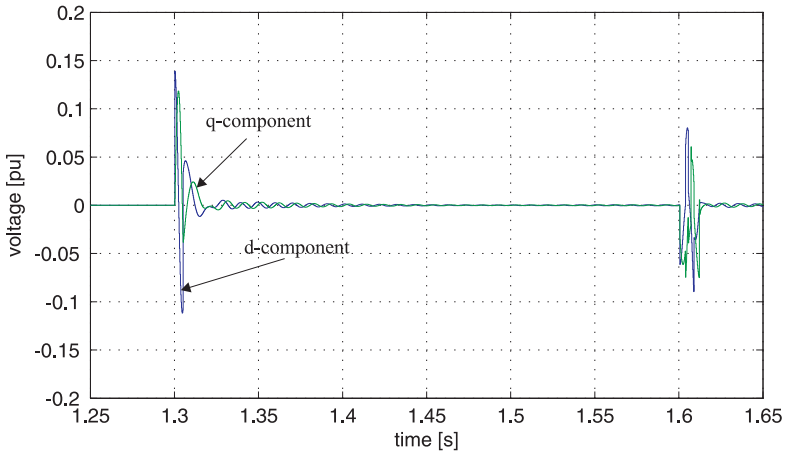

Figure 5.47: Simulated grid voltages in $dq-$coordinate system during 70% balanced voltage dip with 10° phase-angle jump. Negative sequence in negative SRF.

When the compensator is active, the grid voltages are completely restored as shown in Figure 5.48. Figures 5.49 and 5.50 show the complete restore of the positive and negative sequence of the grid voltages in $dq-$coordinate system in positive and negative SRFs respectively. Again, a small transient all the coordinates remain constant to pre-fault values.

Finally, it is possible to compare the torque and the speed of the machine when the E-STATCOM is on-line and when the compensator is disconnected from the mains. As shown in Figures 5.57 and 5.58, where the rotor speed and the electrical torque in pu are depicted, when the machine is exposed to a voltage dip and the compensator is off-line, the speed of the rotor decreases when reduced voltage is applied to its stator windings and then slowly goes back to the rated speed after that the fault has been cleared, while the electrical torque decreases and, after a transients, reaches a value not equal to reference (0.68 pu). If the E-STATCOM is on-line, the speed and the electrical torque of the machine are instead constant, after a transient.

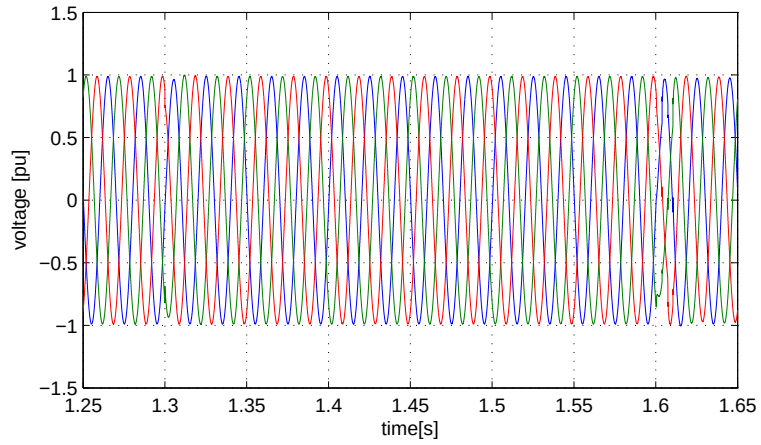

Figure 5.48: Simulated three-phase grid voltages during 70% balanced voltage dip with 10° phase-angle jump. Voltage dip mitigation is used.

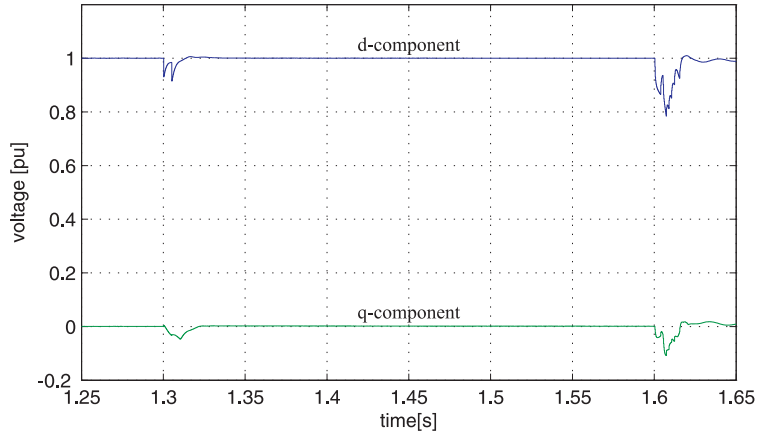

Figure 5.49: Simulated grid voltages in $dq-$coordinate system during 70% balanced voltage dip with 10° phase-angle jump. Voltage dip mitigation is used. Positive sequence in positive SRF.

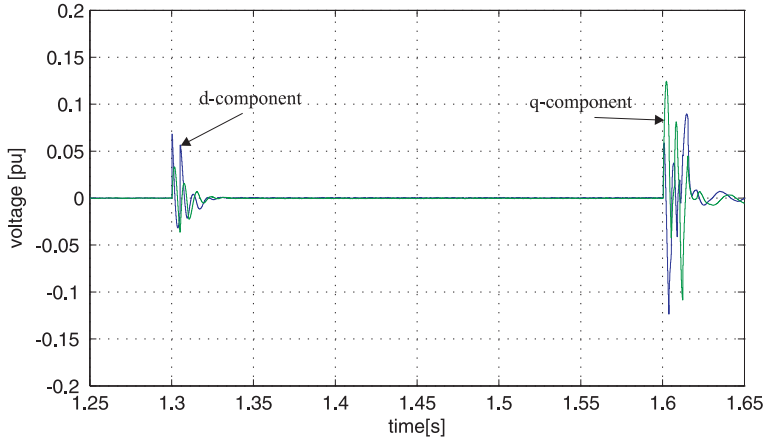

Figure 5.50: Simulated grid voltages in $dq-$coordinate system during 70% balanced voltage dip with 10° phase-angle jump. Voltage dip mitigation is used. Negative sequence in negative SRF.

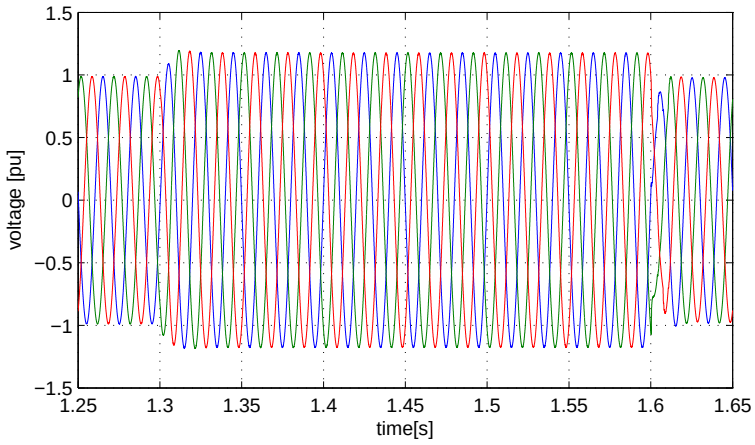

Figure 5.51: Simulated three-phase voltages over the capacitor during balanced voltage dip. Voltage dip mitigation is used.

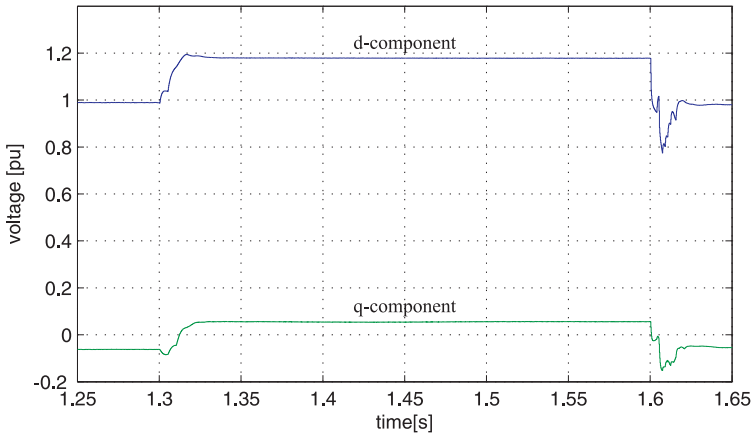

Figure 5.52: Simulated voltages over the capacitor in $dq-$coordinate system during balanced voltage dip. Voltage dip mitigation is used. Positive sequence in positive SRF.

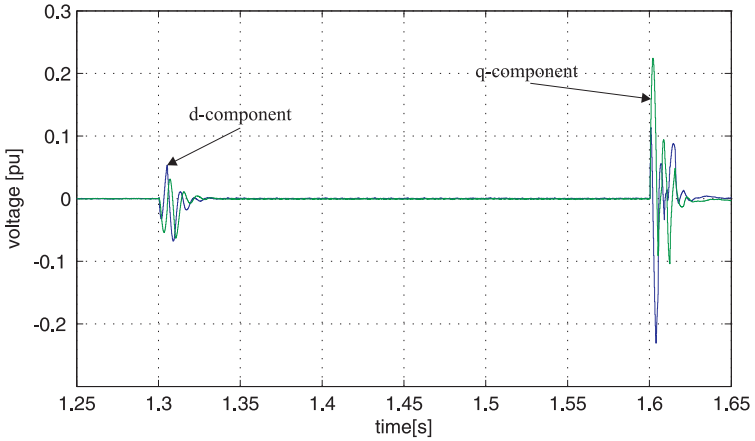

Figure 5.53: Simulated voltages over the capacitor in $dq-$coordinate system during balanced voltage dip. Voltage dip mitigation is used. Negative sequence in negative SRF.

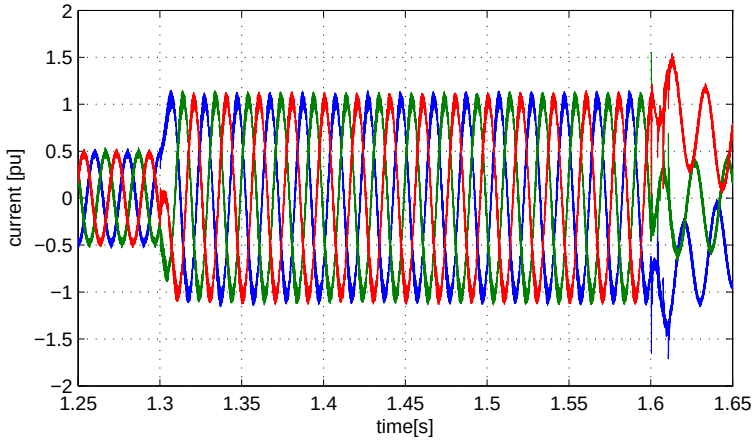

Figure 5.54: Simulated three-phase VSC output currents during balanced voltage dip. Voltage dip mitigation is used.

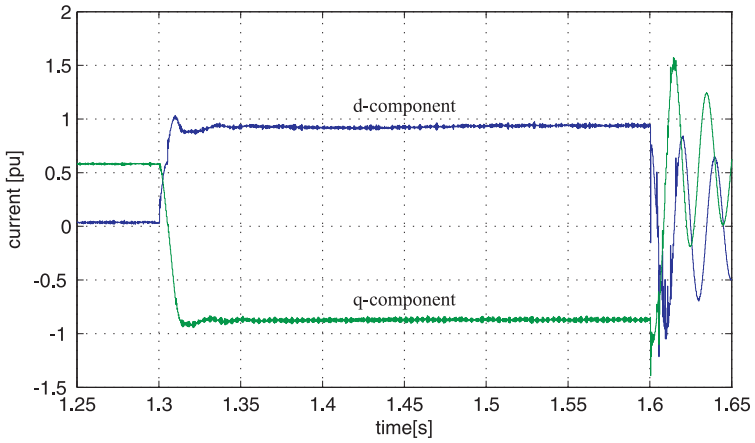

Figure 5.55: Simulated VSC output currents in $dq-$coordinate system during balanced voltage dip. Voltage dip mitigation is used. Positive sequence in positive SRF.

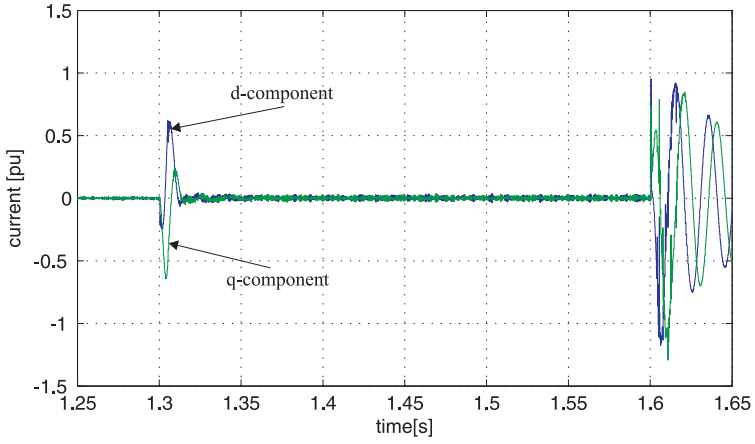

Figure 5.56: Simulated VSC output currents in $dq-$coordinate system during balanced voltage dip. Voltage dip mitigation is used. Negative sequence in negative SRF.

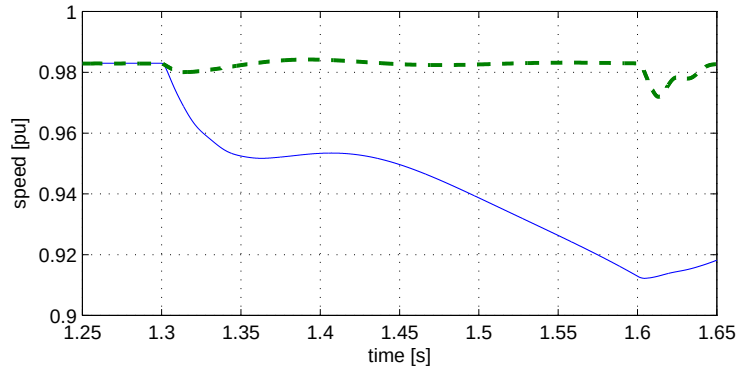

Figure 5.57: Simulated machine speed response during balanced voltage dip. E-STATCOM is off-line(solid) and E-STATCOM is on-line(dash).

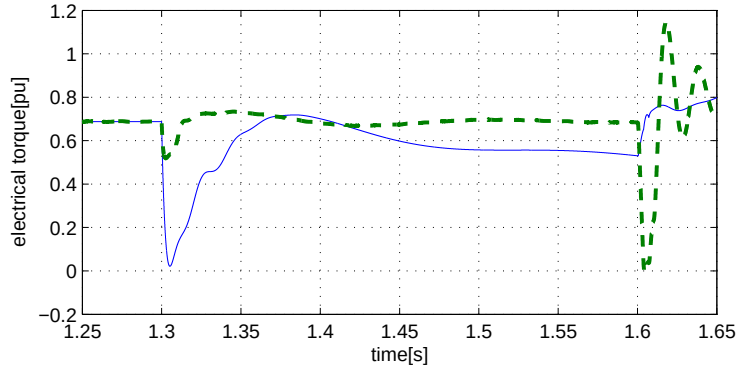

Figure 5.58: Simulated machine electrical torque response during balanced voltage dip. E-STATCOM is off-line(solid) and E-STATCOM is on-line(dash).

5.6 Conclusions

In this chapter, voltage dips mitigation with the E-STATCOM has been carried out. It has been noticed the influence of the transformer impedance on the control system. The system has been tested under balanced and unbalanced voltage dips, for two different kinds of load. The results have shown the impact of the DSC calculation above the performance of the control system. Moreover it has been demonstrated that successful restoration of the grid voltage at the PCC at the pre-fault value.

Chapter 6

Conclusions

Among power quality problems voltage dips are one of most important. Voltage dips are sudden drops in voltage with duration between half a cycle and some seconds, mainly caused by short circuits and starting of large motors. The interest in voltage dips is due to the problems they cause on several types of equipment.

There are three main mitigation categories for the voltage dip: power system improvement, increasing equipment immunity and mitigation devices. In this last category, the devices used are: motor-generator sets, transformer-based mitigation devices, static transfer switch, uninterruptible power supply, series connected VSC (also called SSC) and Shunt connected VSC (also called STATCOM).

This thesis focuses on the control of STATCOM equipped with energy storage with the grid for mitigation of voltage dips. One important issue is to have a fast-response, high-performance control system that is robust to voltage disturbances. The control system has been derived and a stability analysis has been carried out in order to investigate on the impact of the controller bandwidths and the model parameters. the controller system has been improved introducing the transformer compensation and using the DSC for the sequence separation.

The control system has been tested under symmetrical an unsymmetrical voltage dips when protecting a fixed RL-load and an induction motor. It has been shown that successful restoration of the amplitude of the voltage at PCC can be achieved with a very good performance. The current control algorithms presented in this thesis are very general and can be applied in different applications of VSC connected to the grid. It was pointed out that a drawback of using a E-STATCOM for voltage dip mitigation is that the current to be injected into the grid may be too high if the grid is strong.

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Appendix A

Transformation for three-phase systems

A.1 Transformation to fixed coordinates

It is possible to describe a three-phase positive system, constituted by three quantities usually denoted as $\underline{V}_a, \underline{V}_b$ and $\underline{V}_c$, as an equivalent two-phases system, with two perpendicular axes, denoted as $\alpha-$ and $\beta-$axes. It is convenient to consider these axes as the real and imaginary axes in a complex plane. The three-phase/two-phase transformation is given by

$$\underline{v}(t)^{(\alpha\beta)} = v_\alpha(t) + \jmath v_\beta(t) = K(v_a(t) + v_b(t)e^{\jmath\frac{2\pi}{3}} + v_c(t)e^{\jmath\frac{4\pi}{3}}) \tag{A.1}$$

The equation (A.1) can be expressed as a matrix equation as follows

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = K \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{A.2}$$

The inverse transformation is given by

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \frac{1}{K} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} \tag{A.3}$$

The scaling constant K can be chosen arbitrarily, depending on the application. There are three standard selection

Peak-value scaling: K=1

RMS-value scaling: K=$\frac{1}{\sqrt{2}}$

Power-invariant value: K=$\sqrt{\frac{3}{2}}$

In this work, power-invariant transformatios have been used. Therefore (A.2) and (A.3) with $K = \sqrt{\frac{3}{2}}$ can be written as

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{A.4}$$

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} \tag{A.5}$$

Figures A.1 and A.2 show a three-phase voltage system and its vector in a complex reference α β-frame. It is possible to observe that, having used $K = \sqrt{3/2}$, the ratio between the peak-value in α β-frame and in the three-phase system is equal to $\sqrt{3/2}$.

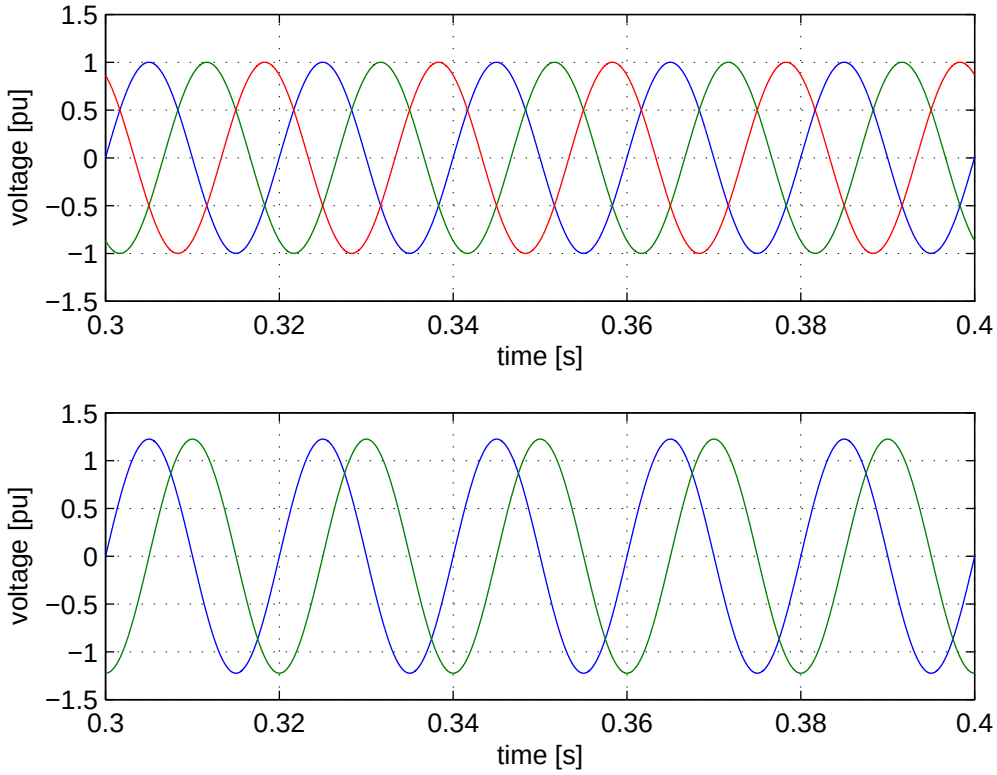

Figure A.1: Transformation to fixed coordinate: top three-phase system,bottom fixed transformation α β-frame.

If a balance drop occurs the radius of the circle, displayed in the following figure, decreases. If an unbalance drop occurs the circle becomes an ellipse.

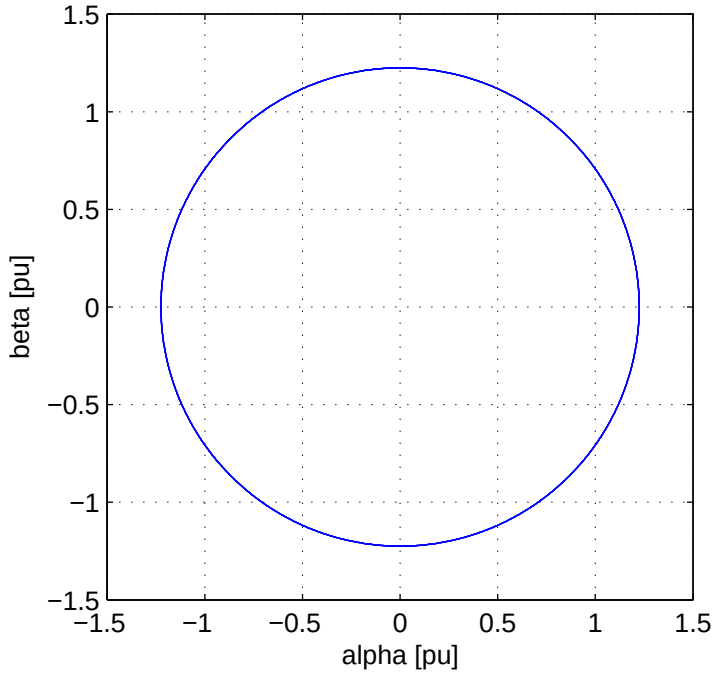

Figure A.2: $\alpha\beta$-Plot.

A.2 Transformation to synchronous coordinate

In the $\alpha\beta$ plane, the vector $\underline{v}(t)$ rotates with the angular frequency ω(t) in the positive direction (if three-phase system is positive). If we considerate a coordinate system that rotates, with the angular frequency ω(t) in the positive direction, the new voltage components will be constant. This coordinate system is called synchronous coordinates or dq coordinates.

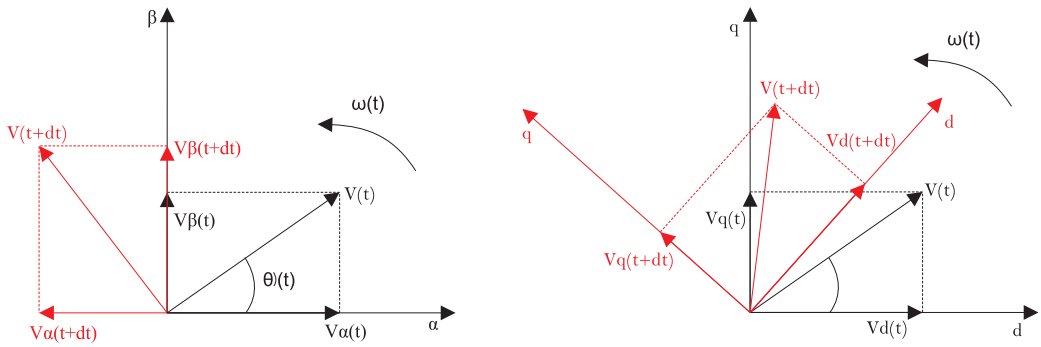

Figure A.3: Vector v(t) and v(t+dt): on left fixed coordinate; on right rotate coordinate

The transformation, for a positive sequence component, can be written in vector form as

$$\underline{v}^{(dqp)} = \underline{v}^{(\alpha_p\beta_p)}(t)e^{-\jmath\theta(t)} \tag{A.6}$$

with the angle θ(t) given by

$$\theta(t) = \theta_0 + \int_0^{\tau} \omega(\tau)d\tau \tag{A.7}$$

The inverse transformation is defined by

$$\underline{v}^{(\alpha\beta p)} = \underline{v}^{(dqp)}(t)e^{\jmath\theta(t)} \tag{A.8}$$

Equations (A.6) and (A.8) can be written in matrix form

$$\begin{bmatrix} v_{dp}(t) \\ v_{qp}(t) \end{bmatrix} = \begin{bmatrix} cos(-\theta(t)) & -sin(-\theta(t)) \\ sin(-\theta(t)) & cos(-\theta(t)) \end{bmatrix} \begin{bmatrix} v_{\alpha p}(t) \\ v_{\beta p}(t) \end{bmatrix} \tag{A.9}$$

$$\begin{bmatrix} v_{\alpha p}(t) \\ v_{\beta p}(t) \end{bmatrix} = \begin{bmatrix} cos(\theta(t)) & -sin(\theta(t)) \\ sin(\theta(t)) & cos(\theta(t)) \end{bmatrix} \begin{bmatrix} v_{dp}(t) \\ v_{qp}(t) \end{bmatrix} \tag{A.10}$$

The transformation, for a negative sequence component, can be written in vector form as

$$\underline{v}^{(dqn)} = \underline{v}^{(\alpha\beta n)}(t)e^{\jmath\theta(t)} \tag{A.11}$$

The inverse transformation is defined by

$$\underline{v}^{(\alpha\beta n)} = \underline{v}^{(dqn)}(t)e^{-\jmath\theta(t)} \tag{A.12}$$

From the latter, it is straightforward to understand that a positive-sequence component corresponds to a DC-component (zero frequency) in the positive SRF, while a negative-sequence component corresponds to a vector that rotates with 100 Hz clockwise in the positive SRF

$$\underline{v}_n^{(dqp)}(t) = e^{-\jmath\theta(t)}e^{-\jmath\theta(t)}\underline{v}^{(dqn)}(t) = e^{\jmath 2\theta(t)}\underline{v}^{(dqn)}(t) \tag{A.13}$$

Using the equations (A.11) and (A.12) it is possible to write the relations in matrix form

$$\begin{bmatrix} v_{dn}(t) \\ v_{qn}(t) \end{bmatrix} = \begin{bmatrix} cos(\theta(t)) & -sin(\theta(t)) \\ sin(\theta(t)) & cos(\theta(t)) \end{bmatrix} \begin{bmatrix} v_{\alpha n}(t) \\ v_{\beta n}(t) \end{bmatrix} \tag{A.14}$$

$$\begin{bmatrix} v_{\alpha n}(t) \\ v_{\beta n}(t) \end{bmatrix} = \begin{bmatrix} cos(-\theta(t)) & -sin(-\theta(t)) \\ sin(-\theta(t)) & cos(-\theta(t)) \end{bmatrix} \begin{bmatrix} v_{dn}(t) \\ v_{qn}(t) \end{bmatrix} \tag{A.15}$$

The instantaneous active and reactive power are given by

$$P = v_a i_a + v_b i_b + v_c i_c \tag{A.16}$$

$$Q = \frac{1}{\sqrt{3}}[v_a(i_c - i_b) + v_b(i_a - i_c) + v_c(i_b - i_a)] \tag{A.17}$$

Substituting the relations (A.4) and (A.9) in (A.16) and (A.17) and if $v_q = 0$, (A.16) and (A.17) can be rewritten as

$$P = v_d i_d \tag{A.18}$$

$$Q = -v_d i_q \tag{A.19}$$

while if $v_d = 0$, (A.16) and (A.17) can be rewritten as

$$P = v_q i_q \tag{A.20}$$

$$Q = v_q i_d \tag{A.21}$$

Appendix B

Normalized (Per-Unit) Values

It is common practice to use normalized or per-unit(pu) quantities in electric power engineering. Normalization is done with respect to a set of base values, which account for the nominal (rated) operation of the system. The base values for the voltage and the power are equal to

$$V_b = 400V \tag{B.1}$$

$$S_b = 59.3kVA \tag{B.2}$$

where E_{base} is the line-to-line rms value of the grid voltage and S_{base} is the the apparent power rating of the injection transformer. The base value for the current, considering that the scaling constant K selected is $\sqrt{3/2}$, is given by

$$I_b = \frac{2K^2}{3}\frac{S_b}{V_b} = \frac{S_b}{V_b} = 148.25A \tag{B.3}$$

The base value for the impedance is then obtained according to

$$Z_b = \frac{V_b}{I_b} = \frac{V_b^2}{Z_b} = 2.698\Omega \tag{B.4}$$

Z_b can be divided into bases for inductance and capacitance according to

$$L_b = \frac{Z_b}{w_b} = 8.59mH \tag{B.5}$$

$$C_b = \frac{1}{Z_b w_b} = 1.179mF \tag{B.6}$$