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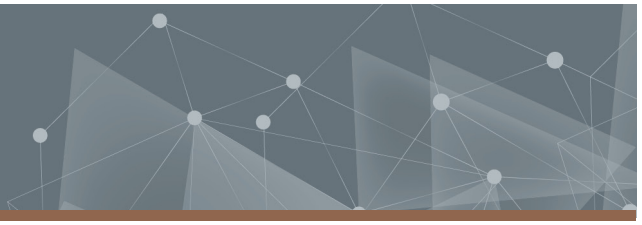

Design of a High Frequency Transformer for High Voltage Applications

Master's thesis in Electric Power Engineering

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Abstract

An Electrostatic Precipitator is an industrial device that filters exhaust gases from process plants to release clean air into the atmosphere. For its functioning, a suitable high voltage transformer is required which operates under electrical stresses induced by power electronic components. Existing transformers for this application are bulky in size, expensive due to material requirement, and require complex balancing circuitry to operate due to multiple cores. A "planar" transformer is therefore suggested as a suitable replacement. With the secondary consisting of multiple PCBs with deposited traces layered around a single core, it is expected that the size of the transformer can be reduced along with the system complexity and material requirements.

This thesis introduces FEM (finite element method)-based simulation model for designing the high-voltage high-frequency planar transformer. Implementation of the model in COMSOL Multiphysics software is presented focusing on application specific aspects such as AC effects at high frequencies, planar PCB design, insulation standards, and the implementation of integrated rectification. In addition, the effect of using dielectric barriers to mitigate high voltage stresses is evaluated based on simulations of the electric fields in the transformer.

Furthermore, based on the results of the simulations, a prototype of the transformer was assembled and its efficiency was evaluated. The measurements of core losses were performed to identify limiting operational conditions. It was found that operating the core close to the saturation magnetic flux density should be avoided since this resulted in rapid heating and high steady-state temperatures in the tests. The least losses were obtained by operating at nearly one-third of saturation flux density. The efficiency of the transformer was calculated considering the measured core loss, winding loss and rectification loss. The results of the performed simulations and measurements indicate that a planar transformer can be considered as a promising solution for replacement of traditional transformers used in electrostatic precipitators.

Keywords: Planar transformer, high frequency, high voltage, PCB design, ESP

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

ESP	Electrostatic Precipitator
FEM	Finite Element Method
HV	High Voltage
LV	Low Voltage
OSE	Original Steinmetz Equation
PA	Polyamide
PCB	Printed Circuit Board
PP	Polypropylene
PVC	Polyvinyl chloride
RF	Radio Frequency
SiC	Silicon Carbide
SRC	Series Resonant Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

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1
Introduction

This chapter presents the background, aim, problem description, scope, and outline of the thesis. The sustainable and ethical aspects of the work are also discussed.

1.1 Background

Air pollution is one of the major health risk factors across the globe, and industrial process plants contribute largely to this [1]. To reduce the impact of emissions from these processes, electrostatic precipitators (ESP) are frequently used. An ESP is a device that uses high electrostatic potential to remove dust and other fine particles from a moving air stream. ESPs have uses in both domestic and industrial applications for air purification. The operation of an ESP is as follows; The high electrostatic potential is applied to discharge electrodes, which are spike-shaped wires, causing ionization of particles due to the high electric field caused by the accumulation of charges at the sharp points. The electrostatic force will attract the charged dust particles to several grounded collector plates. The voltage is then turned off for a short period of time and the collector plates are rapped to remove the collected dust. This dust will then be collected in hoppers placed below the plates and clean gas is emitted [2]. The required high voltage is provided by a power supply consisting of a suitable step-up transformer and rectifier unit.

The existing power supply uses a high voltage transformer that consists of a primary winding wound across several toroidal cores to achieve the required operating voltage. The cores are made of nanocrystalline material, which is expensive. Each toroidal core contains a secondary winding, whose rectified outputs are series-connected to obtain the final voltage. Due to such discrete magnetic circuits, each core requires individual flux-balancing. The present transformer is a bulky device of high cost, sophisticated construction, and complex circuitry. Overall, the transformer is the most expensive part of the converter. By redesigning, it is possible to reduce the cost by carefully choosing the topology of the transformer; its core shape and material.

An alternative design approach is to use a single core design, by packing multiple ferrite cores into a singular magnetic circuit. This eliminates the need for flux-balancing. The core is assembled such that there is a suitable window for stacking multiple secondary windings, sharing the same primary flux. They are similarly rectified at each stage, and series connected to achieve the required voltage. The

secondary is in the form of traces, etched onto PCBs. This reduces complexity, size, material requirement and hence cost, making the construction and assembly simple.

Reducing the transformer's size, material and cost, by increasing the operating frequency has limitations when it comes to high-voltage transformers [3]. Hence, a proper insulation design for the transformer is necessary.

The switching converter that provides the adjustable high-frequency input voltage, is made of Silicon Carbide (SiC) MOSFET modules; a new technology that reduces switching losses and enables high switching frequencies. To efficiently utilize the SiC modules, the transformer needs to be designed to operate at a higher frequency.

1.2 Aim

The aim of the thesis is to design a high frequency, planar transformer for a specific high voltage application, the ESP, evaluate the feasibility of the design using FEM software simulations, and validate its design theoretically.

1.3 Problem Description

The transformer currently used for supplying power to the ESP uses expensive nanocrystalline cores, which are difficult to assemble due to their toroidal shape. A machine is required to keep the windings tightly wound. This is both time-consuming and cumbersome. There are 10 such toroidal cores, required to be wound separately, increasing the total amount of copper.To keep them in balance, additional compensation windings with a dedicated balancing circuitry are required for each secondary. Several hundred turns of copper wire are used in each core. The bulkiness, cost and complexity make it desirable to look for alternatives.
By changing the topology of the transformer to planar, the multiple cores can be reduced to a single core design that carries multiple planar secondary windings. Using a single core eliminates the need for flux balancing. It also reduces the overall size of the core. The planar design reduces copper material usage. The core material is chosen based on the redesigned frequency and insulation requirements.

The main challenge with the proposed design, because of reducing the size, is insulation design. Since the output voltage requirement is the same, the electrical insulation needs to be carefully considered while reducing overall size in the design. The use of a core bobbin having high dielectric strength, conformal PCB (Printed Circuit Board) coatings, suitable distances with a safe margin in regions experiencing high voltage stresses are considered. Due to the increase in frequency and power density, consideration of heating and core loss is necessary as well. The physical design is equally important since sharp boundaries and points can experience high voltage stresses.

The output is rectified and series connected from one PCB to the next PCB. This

is known as “integrated rectification”. As opposed to standard rectification where the total output is rectified, this method follows a stage-rectification process that has the advantage of lowering alternating voltage stress. It can also reduce the high winding capacitance. Another advantage is the possibility of using components with lower voltage ratings [4].

1.4 Scope

In this thesis work, the magnetic and electrical aspects, including the insulation system, are simulated and analyzed. The design is based on calculations and electromagnetic simulations in the FEM-based software, COMSOL Multiphysics. The thermal aspects of the transformer are not considered in COMSOL. Assembly of the prototype is not carried out as part of the thesis, however the core is physically tested for optimal temperature distribution.

1.5 Outline of the Thesis

This thesis is divided into 7 chapters with several subsections. Chapter [1] includes the background, problem description, aim and scope. This chapter also discusses the sustainable and ethical aspects of the thesis work. Chapter [2] presents the basic concepts of transformer design, procedure for selection of core and loss calculations. Chapter [3] describes the high voltage design aspects considered for the PCB design, an overview of diodes and their loss, and a comparison between the old and new designs. It also includes a discussion on the effect of stray capacitance and methods to minimize it. Chapter [4] is the methodology followed during the thesis work for the selection of the primary winding; the calculations and COMSOL simulations carried out to obtain an optimal design. Chapter [5] presents the steps followed for design of the secondary, COMSOL modeling procedure, insulation requirements and calculations. Chapter [6] presents the results obtained from the setups in chapters 4 and 5. These include B-field and E-field plots for different geometries with verification of materials, assembly, and insulation distances in regard to their effect on E-field stresses. In Chapter [7], the results are discussed, and conclusions are drawn to arrive at the most efficient design for the high frequency transformer. The future work is also discussed in this chapter.

1.6 Sustainability Aspects

The United Nations adopted 17 sustainable development goals in 2015 to ensure future needs are met without compromising present consumption [5]. The goals are expected to be met by the year 2030 and encompass a wide range of social and environmental issues.
With the energy sector being a major contributor to the climate change issues challenging the world, it is important to analyze the impact of new innovations on the environment. This thesis work, while improving the efficiency of the transformer

and reducing costs, also contributes to some of the sustainable goals as presented below.

- Affordable and Clean Energy (goal 7)
  The project aims at ensuring access to affordable, reliable, sustainable, and modern energy. There are encouraging signs that the world is progressing towards the goal of achieving affordable and clean energy as energy is becoming more sustainable and widely available.
  The new design of a planar transformer replaces the expensive cores of the old design and reduces copper requirement for its secondary. This brings down the cost of the transformer and makes it much more affordable. With the introduction of the planar design, there is lower core loss, elaborated in further chapters. The efficiency goes up, resulting in a reliable supply for the ESP.
- Sustainable Consumption and Production (goal 12)
  Electricity is hailed as one of the major ways in achieving sustainable development goals. The transformer design introduced in this thesis reduces the size and hence the material required. As described in the previous section, with a reduction in loss, the ESP supply becomes more efficient and hence more sustainable. With a future scope of mass production, this would cause the ESP industry to have improved and more sustainable operation.

1.7 Ethical Aspects

A list of 10 ethical aspects is described by the Institute of Electrical and Electronics Engineers (IEEE) [6], which forms a code of ethics that all members are expected to follow. Some of the ideas covered in this thesis work include:

- Objectivity (2)
  The goal is to compare and replace an existing transformer with a planar transformer. By doing so, actual outcomes are compared by monitoring energy loss and material savings.
- Carefulness (3)
  It is critical to deliver the desired outcome, since this study will determine if an entire line of transformers will require a change. It is necessary that measurements are done carefully, and reliable data is produced.
- Unlawful conduct (4)
  This project is only for Research and Development; no supplier is being promoted or advertised. This is purely a study for potential replacement of an existing product to a higher-efficiency one.
- Honesty (5)
  The outcome of this study will greatly influence the company's production for the ESP industry; hence it is important that honest results are presented, and not in the favor of the present transformer or the new one. If it reaches a conclusion that introducing a planar topology into the required high voltage system is not feasible, then it is presented with honest data describing why it is not a good choice.

2

Principles of Transformer Design

This chapter introduces the basic concepts involved in the design of a transformer; laws of electromagnetism, transformer equations, core and winding losses. It also contains a description of the transformer used in a series resonant converter network.

To begin the design of a transformer, it is necessary to understand the principles governing its working, namely; the laws of electromagnetism. Transformers are based on Ampere's Magnetic Circuit Law, and Faraday's Law of Electromagnetic Induction.

2.0.1 Ampere's Law

The derivation follows from Maxwell's equations for a linear, homogeneous, isotropic medium. Ampere's law relates current, and the magnetic field created by it, described by Equation (2.1) [7].

$$\oint_C \vec{B} \cdot d\vec{l} = \mu_0[I_{enc} + \epsilon_0 \cdot \frac{d}{dt} \int_S (\vec{E} \cdot \vec{n}) ds] \tag{2.1}$$

where, "B" [T] is the induced magnetic field vector, with the dot product of the closed integral indicating the B field along the path "C".
"μ_0" indicates the magnetic permeability [H/m] of free space, "I_{enc}" [A] indicates the enclosed conduction current, and "ϵ_0" indicates the electric permittivity [F/m] of free space. The displacement current is expressed as the rate of change of "E", electric flux [Wb] with respect to time "t". The electric field [V/m] is a vector, bounded by the closed surface "S".

2.0.2 Faraday's Law

Maxwell's equation for Faraday's law describes the relationship between the electric field intensity and the rate of change of magnetic flux within a closed surface. In the integral form, Faraday's law equates the integral of electric field intensity around a closed contour "C" to the rate of change of the magnetic flux that crosses the surface "S" enclosed by "C", described by Equation (2.2) [7].

$$\oint_C \vec{E} \cdot d\vec{l} = -\frac{d}{dt} \int_S \vec{B} \cdot \vec{n} da \tag{2.2}$$

where, "E" [V/m] is the induced electric field circulating around the closed path "C", caused by the changing magnetic field "B" [T] with respect to time. The negative sign is explained by Lenz's law [2.0.3].

2.0.3 Lenz's Law of Electromagnetic Induction

Lenz's law states that the direction of the magnetic field generated by the induced electric field is such that it opposes the original magnetic field causing it. It is explained using Equation (2.3) [7].

$$e = -\frac{d\phi_B}{dt} \tag{2.3}$$

where, the induced e.m.f. "e" [V], and the changing magnetic flux "ϕ_B" have opposite signs.

2.0.4 Transformer Efficiency

The efficiency of the transformer can be expressed as the ratio of the output power to the input power, as described in Equation (2.4).

$$\eta = \frac{P_{in} - loss}{P_{in}} \cdot 100 \tag{2.4}$$

2.0.5 Flux Density

When a magnetic field passes through a material, the measure of the material's resulting flux density to the applied magnetic field is given by its magnetic permeability μ, described by Equation (2.5) [7].

$$\vec{B} = \mu_0 \mu_R \vec{H} \tag{2.5}$$

where "μ_R" is the relative magnetic permeability of the material.
The magnetic flux density of a transformer under a changing flux density is obtained by relating Ampere's law and Faraday's law, as described in Equation (2.6).

$$e = N \cdot \frac{d\phi}{dt} = N \cdot A_e \cdot \frac{\vec{B}}{dt} \tag{2.6}$$

where "ϕ" is the alternating flux in the core, "A_e" [m^2] is the effective cross-sectional area of the core, and "e" is the counter e.m.f. as described in Equation (2.3) to the applied primary voltage "v", and in accordance to Kirchoff's voltage law [7], $v = e$.

In the case of an applied square wave voltage, v remains constant until the polarity changes, and the corresponding flux density is a triangular wave. When the voltage changes polarities, flux density "B" switches to its maximum values from positive to negative. Therefore, there are two peaks every half period, as illustrated in Figure 2.1 from [7].

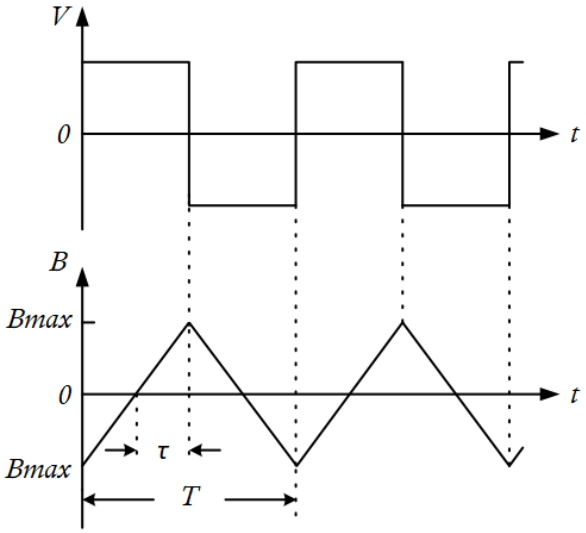


Figure 2.1: Applied square wave voltage and corresponding flux density

The average value of the applied voltage during an interval $t = \tau$, where the flux density varies from zero to its maximum value is $|v|$. The value of $|v|$ is found by integrating Equation (2.6), resulting in Equation (2.7).

$$|v| = \frac{1}{\tau}\int_0^{\tau} v(t)\,dt = \frac{1}{\tau}N\cdot A_e\int_0^{B_{max}} d\vec{B} = \frac{1}{\tau}N\cdot A_e\cdot B_{max} \tag{2.7}$$

The form factor "k" relates the obtained average value of $|v|$ to the rms value of the applied waveform as described in Equation (2.8).

$$k = \frac{V_{rms}}{|v|} \tag{2.8}$$

Combining Equation (2.7) and Equation (2.8) results in Equation (2.9),

$$V_{rms} = \frac{K}{\frac{\tau}{T}}\cdot f\cdot N\cdot B_{max}\cdot A_e \tag{2.9}$$

where "K" is the waveform factor defined in Equation 2.10

$$K = \frac{k}{\tau f} \tag{2.10}$$

The wave shape from the SRC (Series Resonant Converter) source is a square wave as described in Figure 2.1, hence the duty cycle D is 0.5. To establish the value of K for a square wave, the flux rises from zero to B_{max} in time $\tau = T/4$, therefore resulting in $\tau/T = 0.25$. The form factor k for a square wave is 1, since the average value over the time τ is V_{dc}, and the rms value is V_{dc}. K is hence $1/0.25 = 4$. Applying the obtained K value in Equation (2.9), Equation (2.11) is obtained.

$$V_{rms} = 4\cdot f\cdot N\cdot B_{max}\cdot A_e \tag{2.11}$$

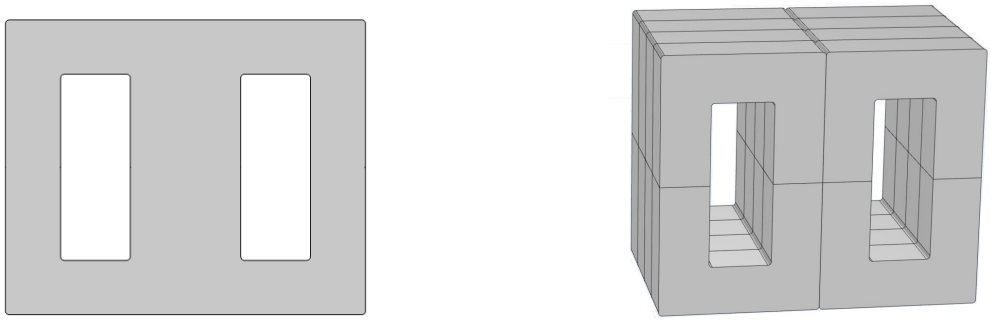
Rearranging Equation (2.11) to present in terms of B_{max}, Equation (2.12) is obtained.

$$B_{max} = \frac{v}{4 \cdot f \cdot N \cdot A_e} \tag{2.12}$$

Equation (2.12) will be used for all calculations henceforth for values of the peak flux density of the core to select the most optimal combination of B_{max} and number of cores to achieve the most efficient design [7].

2.0.6 Core Shape and Magnetizing Inductance

The core shape is an early design factor in the construction of the transformer. The conventional shell-type transformer and its realization using multiple cores is shown in Figure 2.2.



(a) Core shape cross-section **(b)** Realized with multiple cores

Figure 2.2: Shell-type transformer core shape

As the cross section area, core window distance, and other design factors are decided, the transformer is assembled using smaller ferrite cores to obtain the desired size. For effective transformer operation, a suitable B-field needs to be set up across the cross-section of the core, and this is done by the alternating flux established by the changing voltage across the primary, described in Equation (2.12).
The magnetizing current is a small portion of the primary current, which is always drawn to keep the core magnetized. This is observed even when there is no secondary load. The magnetizing inductance [H] can be calculated by Equation (2.13).

$$L_m = \frac{N^2}{R_c} \tag{2.13}$$

where, "N" is the number of primary turns and "R_c" is the reluctance of the core.

The core's reluctance R_c can be thought of as the magnetic equivalent of electrical impedance, as magnetic flux is to electric current. Reluctance is the measure of the impeding effect by a material to a magnetic field flowing through it. Reluctance is given in Ampere-turn per Weber [AT/Wb] or inverse Henry [1/H], and can be calculated using Equation (2.14).

$$R_c = \frac{l_c}{\mu_r \cdot \mu_0 \cdot A_e} \tag{2.14}$$

where, "l_c" is the length of the magnetic path in [m], "A_e" is the effective cross-section area of the core [m^2], and "μ_r" is the relative magnetic permeability of the core material.

The m.m.f generated in the core's magnetic path can be expressed in the form of Equation (2.15).

$$mmf = N \cdot I = \phi \cdot R_C \tag{2.15}$$

where "N" is the number of primary turns and "I" is the primary current [A]. It can also be equated to the product of "ϕ" which is the magnetic flux [Wb] generated, and "R_C", the core's reluctance [AT/Wb]. The reluctance of a transformer's core can be derived by expressing the transformer as a magnetic circuit. Figure 2.3 expresses the primary winding as an m.m.f. source.

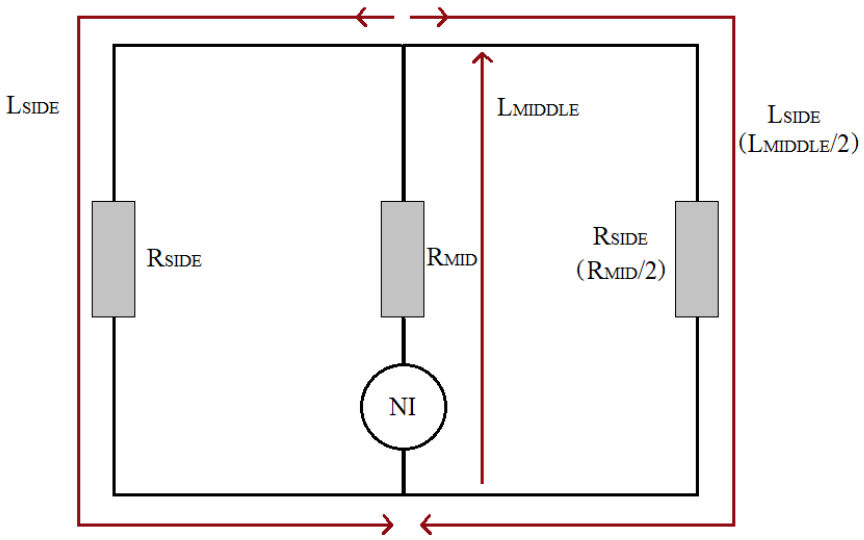


Figure 2.3: Magnetic circuit of a Shell-type transformer

The established flux travels through the middle leg and splits into half (into parallel magnetic paths) across each side leg, to add and return to the source. The path that the flux takes is known as the Magnetic Path Length or Mean Magnetic Path. It is the path of least reluctance that the flux takes, which is the mean circumference of the core's magnetic loop, normal to the current direction in the winding. Figure 2.4 illustrates the magnetic flux lines through the mean magnetic path of the core.

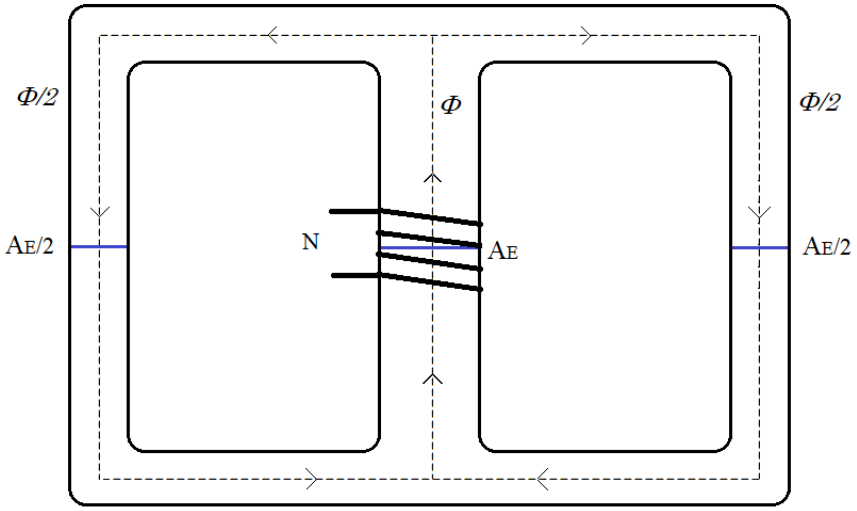


Figure 2.4: Flux path in a Shell-type transformer

2.1 Series Resonant Converter

The transformer's input power is fed using an SRC which is a DC-DC converter that allows "soft-switching" operation due to topology. In this operation, switching can occur when voltage and/or current values are zero (ZVS)/(ZCS) (Zero Voltage Switching/Zero Current Switching), thus significantly improving the converter's efficiency under optimal conditions [8].
In the case of the current design the power input is an industrial three-phase power network that is rectified in the DC-link. The specific application is an ESP, that can be described as a load in the form of a parallel RC network. The resonant network has the inductance split into two inductors. The transformer is also included in the resonant tank as a part of the circuit, as illustrated in Figure 2.5.

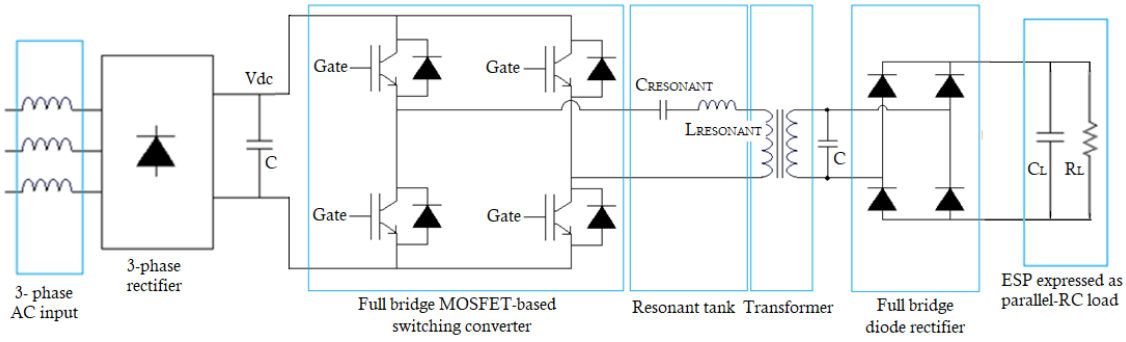


Figure 2.5: Circuit diagram of the series resonant converter

2.2 Choice of core

The design of the primary starts with the choice of the core. The core is essential to contain the magnetic field and provide a path for the flux. Mn-Zn ferrites are the most common core materials used for power electronic devices. This material has a high electrical resistivity which reduces Eddy Current losses in the core. The selection of the type of ferrite core for transformers depends on several factors.
In practice, a transformer needs to be designed around a particular input waveform, taking into consideration the amplitude, frequency and current. Additionally, there will be changes in properties such as permeability during operation due to rise in temperature. The transformer needs to be designed to operate over a range of values for its parameters.

2.2.1 Factors affecting the selection of core material

- Magnetic permeability (μ): The permeability varies with temperature and magnetic flux density. However, this relationship is not linear. It takes an optimum value across a range of temperature and flux density. Ideally, maximum permeability is desirable at the operating point of the transformer.

- Temperature (T): The resistive heating, eddy currents and hysteresis loss gradually raise the temperature of the core. Different cores have different optimal temperatures. At a certain temperature, some materials will lose their magnetic properties. Additionally, temperature will cause the core's permeability to change. Hence cooling might be needed to prevent such a situation.

- Frequency (f): Input frequency selection is important. Chosen correctly, it will allow low core losses, reduce temperature and increase flux.
  From Equation (2.12), an alternating voltage is required to establish a flux. Since the input voltage is fixed at $500V_{RMS}$, frequency, primary turns and cross-section area are the allowed variables;
  - Increasing the cross-section area results in increased material cost.
  - Increasing the number of primary turns results in increased secondary turns (multiplied by the transformation ratio), requiring more Litz cable length on the primary and increased number of copper volume by traces on the secondary, as well as the increased volume occupied within the core window.
  - Increasing the frequency reduces core material requirement and hence cost, while increasing loss in the converter and winding.

  Losses are proportional to the frequency, but also to the flux. The decrease due to the lower flux can have more influence than the increase due to high frequency, hence increasing the frequency in this case will be beneficial.

- Core loss: Core loss is divided into hysteresis loss and eddy current loss;
  - $P_{Hysteresis}$: proportional to "f" and "B"
  - P_{Eddy}: proportional to "f^2" and "B^2".

In the current design, the use of a ferrite core reduces eddy currents substantially due to its high electrical resistivity, unlike soft iron cores.

2.3 Core Loss

The core loss in a transformer core consists of two parts; Hysteresis and Eddy current loss. Hysteresis loss is due to the continuous reversal of the magnetic domains, and the heating it causes. Eddy current loss is caused by the alternating magnetic field inducing circular currents within the core material itself.

To determine the core loss, usually in [mW/cm^3] or [kW/m^3] as a function of the given peak flux density B$_{max}$ [T], the Original Steinmetz Equation (OSE), given by Equation (2.16), is used

$$P_v = K_c \cdot f^{\alpha} \cdot B_{max}^{\beta} \tag{2.16}$$

where "f" is the frequency in [kHz], and "K$_c$", "α", and "β" are constants that may be found from the manufacturer's datasheet, or found by curve fitting from existing data.

2.3.1 Measurement of Core Loss

In the design of magnetic components, it is necessary to understand the complete characteristics of the materials. However, there is an inadequacy in the availability of data and validation models for high frequency applications. This can be due to several factors such as the lack of reliable experimental methods, the complexity of providing excitation, along with the changes in properties of the material with varying parameters [9].

For the measurement of core loss, a suitable excitation source is provided. The primary and secondary turns are kept equal and are tightly wound. The primary winding is the exciting winding, whereas the secondary is more of a sensory winding. This is necessary to avoid any voltage drop across primary, due to resistance, from affecting the measurements [9].

To measure the core loss, electro-mechanical wattmeters were conventionally used. However, these measurements are not reliable at high frequencies. For an accurate core loss measurement, the setup with equal primary and secondary turns can be used, and the waveforms of secondary voltage and primary current are then multiplied to find the power of the core. The average power loss is then measured by finding the mean of the power in one cycle. To find the loss per unit volume, the measured core loss can be divided by the core volume provided by the manufacturer. This calculated loss is then plotted versus frequency, and the process is repeated for different frequencies, voltages and flux density levels, arriving at an overall core loss characterization [9].

2.4 Winding Loss

In the case of high frequency transformers, besides DC loss, the copper winding exhibits significant AC loss that needs consideration [7].

2.4.1 DC resistance

For a DC input, the conductor exhibits Ohmic I^2R loss, and the resistance "R" is given by the resistivity of the material "ρ" at the chosen temperature, its length "l" and cross sectional area "A".

$$R = \frac{\rho \cdot l}{A} \tag{2.17}$$

Copper's resistance is frequently calculated for 100^0C, as that would be typical steady state temperature for a transformer during operation.
Electrical resistivity as a function of temperature $R\rho[T]$ is given by Equation (2.18).

$$R\rho(T)l/A = \rho_{(T_0)}[1 + \alpha(T - T_0)l/A] \tag{2.18}$$

where "T_0" is the initial reference temperature, "α" is the temperature coefficient of conductivity of the material, "l" is the length of the conductor, and "A" is the cross section of the conductor. The resistivity described in Equation (2.18) is calculated from the standard resistivity for copper given at 20^0C with the parameters presented in Table 2.1.

Table 2.1: Properties of Copper

Symbol	Definition	Expression	Value	Unit
T	Conductor Temperature	-	100	^0C
T_0	Initial Temperature	-	20	^0C
ρ_{20}	Copper resistivity at 20^0C	-	1,68E-8	Ωm
α	Temperature coefficient of copper	-	0,00386	-
ρ_{100}	Copper resistivity at 100^0C	$\rho_{20}[1 + \alpha(T - T_0)]$	2,2E-8	Ωm
σ_{100}	Copper conductivity at 100^0C	$(1/\ \rho_{100})$	4,55E+7	S/m

Hereafter, every calculation concerning copper material will be carried out with the resistivity and conductivity as presented in Table 2.1.

2.4.2 AC resistance

While it is quite straightforward for DC, several effects are exhibited with AC, namely; skin effect and proximity effect. Especially at high frequencies (it is apparent at low frequencies as well, but their losses are significant as frequency increases), skin effect takes place within a conductor, and proximity effect takes place between two insulated, nearby conductors. The skin and proximity effects together result in higher loss in conductors since they cause non-uniform distribution of current, resulting in an increase of effective AC-resistance.

2.4.2.1 Skin effect

An isolated conductor carrying AC generates a concentric, alternating magnetic field, which induces Eddy currents. This cancels some of the currents at the center, while increasing surface current. This is called skin effect and the overall result is that current flows in a smaller annular area, as illustrated in Figure 2.6 [7].

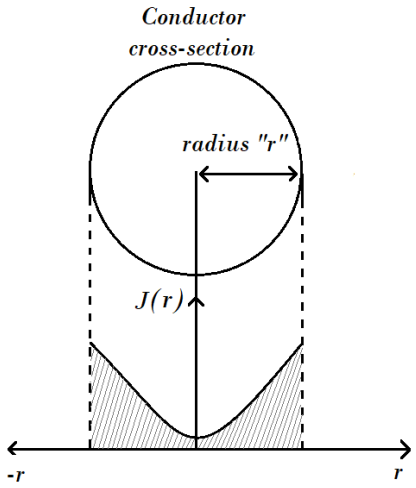


Figure 2.6: Skin effect in a circular conductor

where, "J(r)" is the surface current density taken along the radius "r" from the center of the conductor to the outer surface.
At higher frequencies, the current flows in an equivalent annular cylindrical portion, of radial thickness "δ", called skin depth. Deriving from Equation (2.1), Equation (2.2) and Bessel's equation, the skin depth is given by Equation (2.19).

$$\delta = \sqrt{\frac{1}{\pi \cdot f \cdot \mu_0 \cdot \mu_R \cdot \sigma}} \tag{2.19}$$

where "f" is input frequency in [Hz], "σ" is the conductor's conductivity in [S/m], and "μ" is the conductor's magnetic permeability in [H/m].
While the DC resistance is fixed with the conductor's design, the AC resistance depends on the operating frequency of the application. A factor "k_s" is defined as R_{AC}/R_{DC}, this gives the approximation as described in Equation (2.20).

$$k_s = 1 + \frac{\frac{r_0}{\delta_0}^4}{48 + 0,8 \cdot \frac{r_0}{\delta_0}^4} \tag{2.20}$$

From Equation (2.19), it is visible that "δ" reduces with increasing frequency, reducing effective conduction area. Skin depth describes the depth up to which 67% of

the maximum current density flows within that surface area.
To determine the diameter of the strands (d_0) with regard to skin depth, the following factors are considered,

- If $d_0 \gg \delta$, it is wasteful to use more conducting material since most of the current would only flow in the skin depth from the surface.
- If $d_0 \ll \delta$, the conductor would exhibit mostly DC properties but at the cost of small surface area, requiring more conductors to carry the same rated current.

The recommendation for diameter, from Litz wire manufacturers is to use "1/e" times the "δ" value, where "e" is Euler's constant [10].

2.4.2.2 Proximity effect

At high frequencies, conductors in close proximity induce Eddy currents in adjacent conductors. This disturbs the uniform distribution of currents by concentrating them towards the region that is furthest from the nearby conductors that induce the Eddy currents. This is called proximity effect, it reduces effective conduction area and hence increases the AC resistance.[7]. The COMSOL simulation shown in Figure 2.7 describes the uniform current density due to AC and the varying current density due to high frequency AC flowing in the same direction in adjacent conductors.

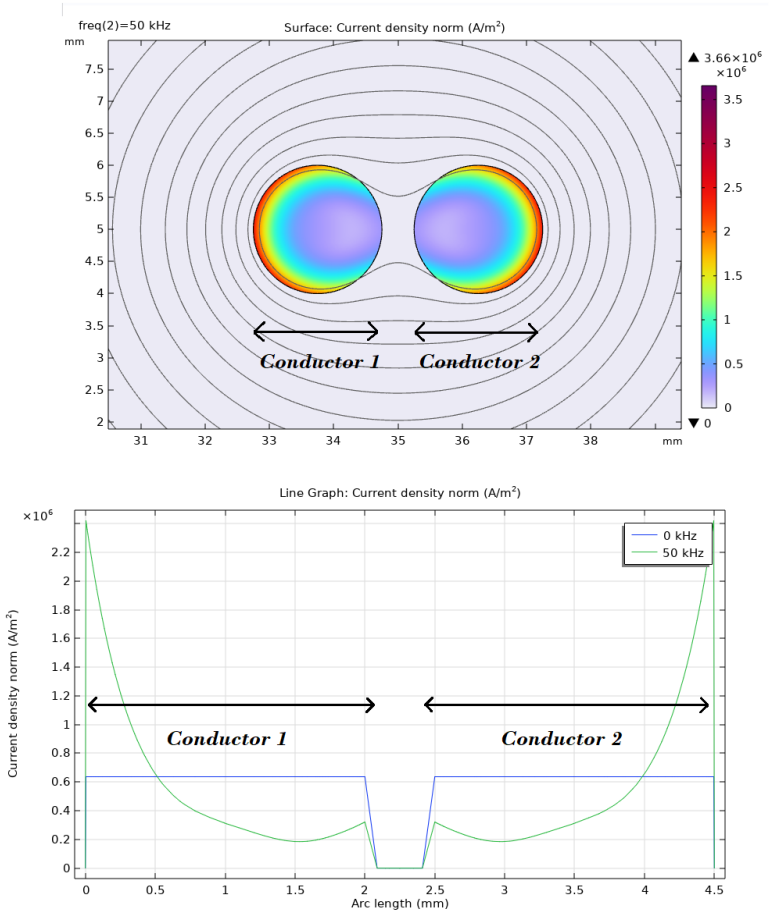


Figure 2.7: Proximity effect in a circular conductor

The variation in current density for high frequency AC increases the effective resistance, as presented in Table 2.2 [11].

Table 2.2: Ohmic resistance of DC and high frequency AC in adjacent conductors

Frequency (kHz)	Conductor 1 R(Ω)	R% increase	Conductor 2 R(Ω)	R% increase
0,0	0,0053	171.5%	0,0053	171.5%
50,0	0,01439	171.5%	0,01439	171.5%

2.5 Primary winding design

To minimize the effects of AC, Litz wire is used. Litz wire is composed of multiple, thin individual strands that are twisted together, with each strand insulated. If a solid conductor of the same cross section is considered, high frequency AC will cause the currents to gravitate to the surface of the conductor, hence not utilizing a major portion of the actual conductor. With several smaller, insulated conductors making up effectively the same cross section, the current in each cable is limited to each strand's surface, allowing a much greater effective conducting area. While this reduces the skin effect, the chances of proximity effect increases as the strands are bunched together. Hence, the method of transposing them at intervals evens the magnetic field across all conductors, maintaining the uniformity of current density [7].

With Litz wire proving beneficial to reduce loss, it is necessary to understand how to effectively design the strands. Manufacturers of Litz wires provide different recommendations for the diameters of strands based on frequency; however these may not always lead to optimal designs and can lead to high resistances and hence higher loss [14]. From [14], a simple design approach was implemented in this thesis work. This provides a method to calculate the number and diameter of strands needed for the present application. Once the numbers are derived, the arrangement of the strands in bundles can also be chosen.

2.5.1 Steps for Litz wire design [14]

- Skin depth calculation (δ)

  Using Equation 2.19, the skin depth in [mm] is calculated for the required frequency of operation. Based on this value, the diameter (d_c) can be deduced to be 1/e times δ, as mentioned in Section 2.4.2.1.

- Winding specifications

  To calculate number of strands, the parameters of the winding required are the available core window area (b_c) in [mm] and the number of turns per section (N). Since there is no interleaving, the number of turns here can be chosen as the number of primary turns of the design.

- Calculation of number of strands

  From these parameters, the number of strands can be calculated using Equa-

tion (2.21), as derived in [14].

$$n = k\frac{\delta^2 \cdot b_c}{N} \tag{2.21}$$

where, "n" is the effective number of strands, and "k" [mm^{-3}] is a constant derived in [14] based on the strand diameter and resistance factor for economical designs.
Based on availability and manufacturer limitations, the number of strands can be up to 25% greater or less than the calculated value of n.

- Choice of optimal number and diameter of strands

  While finalizing the number of strands acceptable for the design, the calculated cross-sectional area must be within 25 to 30% of the core window available. This value must take into account the cost and performance for the required application.

- AC loss factor

  The AC loss coefficient of a Litz wire, given a sinusoidal current of known frequency and amplitude can be found from Equation (2.22), derived in [15].

$$F_r = \frac{R_{AC}}{R_{DC}} = \left(1 + \frac{\pi^2\omega^2{\mu_0}^2N^2n^2d_c^6k}{768\rho_c b_c^2}\right) \tag{2.22}$$

  where, "F_r" is a factor relating DC resistance to the AC resistance.

- AC loss calculation

  The winding loss due to AC is described by Equation (2.23), derived in [15].

$$P_{loss} = F_r \cdot {I_{ac}}^2 \cdot R_{dc} \tag{2.23}$$

- Choice of arrangement

  The twisting arrangement in mainly advantageous to avoid a bundle-level proximity effect. To avoid a bundle-level skin effect, the placement of the strands must also be considered. The twisted strands must be arranged in multiple levels with respect to their centres. Each group can consist of 5 or less twisted sub-bundles to have a minimum skin effect, using strands with diameters much smaller than the skin depth [14].

3

Design of Planar Secondary

In this chapter, the high voltage design factors are discussed, along with the choice of planar coils for the secondary winding and their parameters. Characteristics of the diode used and the output rectification method are also described.

3.1 PCB for Secondary

Unlike conventional wound transformers, the distinct development here is to use a planar winding as the secondary. There are several types of transformer windings, such as foil, multi-layer, and pancake/disc type. Foil type transformers are for low voltages (not relevant to this study). The multi-layer type is most commonly found in the medium voltage range, and pancake/disc/sandwich winding offers the best design for high voltage and extra high voltage purposes [16].

- Multi-layer winding
  The turns are laid next to each other, and as layers on top of the other, as illustrated in Figure 3.1. Paper winding on the conductor, or an oil-proof enamel coating serves as inter-turn insulation.

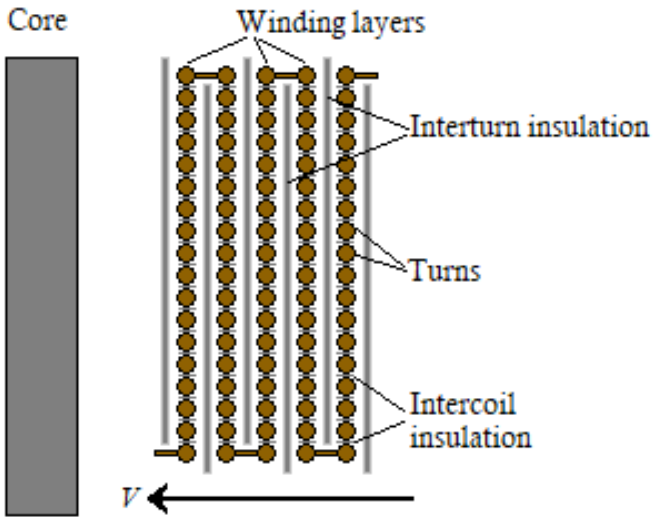


Figure 3.1: Multi-layer transformer winding [16]

The full voltage is found to occur at the narrow front side of the winding.

Hence, it is used in the medium voltage range. This geometry offers excellent packing hence most commonly found in domestic to medium voltage ranges. Shortening the winding layer length and increasing radius causes a potential grading in the axial direction.

- Disc/Pancake/Sandwich winding
  This is the basis of the planar design. At a first approximation, the DC extreme "V" is uniformly distributed over the winding layer length as illustrated in Figure 3.2, hence it can be implemented for HV. Across the narrow front side, there is a relatively low partial voltage.

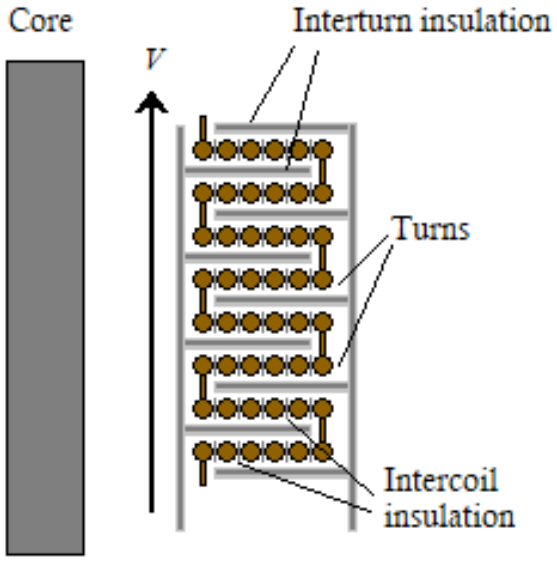


Figure 3.2: Disc/Pancake/Sandwich transformer winding [16]

By gross comparison, disc winding is better when considering higher voltages. There are however undesirable effects observed in disc winding, such as increased longitudinal capacitance. Other factors of interest include leakage inductance and heat removal. Leakage inductance is the result of insulation distances, gap widths between winding, layers and turns. It is mainly the distance between the primary and secondary winding that results in a large leakage inductance. Compact designs reduce $L_{leakage}$ but they compromise insulation distances. Insulation design is hence a crucial part of this study.
In conclusion, using a planar coil for this application would work best [16].

3.2 High Voltage Design Aspects

The design of the electrical insulation involves electric strength calculations, clearance and creepage distances, breakdown of oil, among other factors. This design must be based on semi-empirical relationships to consider all parameters that can have an impact on the system [16].
Due to the reduction in the size of the transformer, the constraints related to the

E-field stresses need to be addressed. In this planar transformer, there is a DC-field with a small super imposed AC-ripple. It is the conductivity of the dielectric materials that determines the distribution of the E-field and this in turn determines the design of the transformer secondary [16]. Hence an electric conduction model is considered for the simulations as well. In the case of DC stresses, the electrical conduction field is prevalent and in the case of AC stresses, it is the dielectric displacement field. Maxwell's Equations form the basis for the classification of these stationary fields [16]. These are further discussed in the next section.
Under the sub-categories of the Maxwell's equations, the material equations are relevant to this study. These describe the impact of material properties on the electric and magnetic fields. For insulation systems with a DC stress, the Maxwell equation described in Equation 3.1 is the starting point.

$$J = \sigma \cdot E \tag{3.1}$$

where, "J" is the current density [A/m^2] and "σ" is the material conductivity [S/m].

The transformer is being designed to generate $50kV_{DC}$ at the output terminals. The stresses in the secondary observed across its compact design make it necessary to ensure that there is no possibility of inception and dielectric breakdown, and to design for a suitable margin for distances.

3.2.1 Fields for AC and DC stresses

From Maxwell's equations, fields are classified based on their time rate of change into Static and Stationary, Quasi-Static and Non-stationary [16]. Since the field quantities here are time invariant, the non-stationary field is not discussed.
In the case of a static electric field, it must be assumed that the material has zero conductivity or is a perfect dielectric and this is not possible in reality. Hence, the conduction field must be considered instead of an electrostatic field.
The electrical conduction and dielectric displacement (capacitive) fields are as depicted in Figure 3.3. The properties of oil and the bobbin influence the E-field distribution across the modelled geometry and hence are indicated here. The material for bobbin is a polymer plastic called Polypropylene (PP), motivated in further chapters.

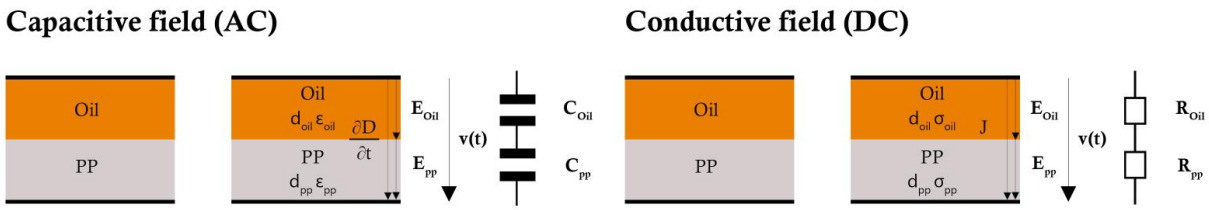


Figure 3.3: Capacitive and Conduction Fields

3.2.1.1 Conduction Fields

A stationary or steady-state field, the field quantities here, E and J, are constant or time-invariant. According to Equation (3.1), these fields are defined by a constant J and a proportional E. When there is a DC stress, the distribution of the E-field is influenced by a conduction current caused by the material conductivity that result in the movement of charges. The relative permittivity of the material does not have an impact on this field [16].
The E-field stress on oil can be calculated using the properties of the dielectric interface between oil and the bobbin (PP). For the conduction field, the conductivity is considered, as shown in Equation 3.2.

$$E_{oil} = \frac{U}{d_{oil} + d_{PP} \cdot \frac{\sigma_{oil}}{\sigma_{PP}}} \tag{3.2}$$

where, "U" is the output voltage [kV], "d_{oil}" and "d_{PP}" are the distances [mm] of oil and bobbin respectively, and "σ_{oil}" and "σ_{PP}" are the conductivities [S/m] of oil and bobbin respectively.

3.2.1.2 Capacitive Fields

A quasi-stationary displacement field, the field quantities here can be slightly time-varying. However, in insulating materials, the changes in the field are insignificant when compared with the source field and can hence be neglected. For HV insulating materials, the AC stress is of importance. If the conductivity is determined to be relatively low and negligible, the displacement currents would be larger than the conduction. For the capacitive field, the relative permittivities are considered to study the E-field stresses, as in Equation 3.3.

$$E_{oil} = \frac{U}{d_{oil} + d_{PP} \cdot \frac{\epsilon_{oil}}{\epsilon_{PP}}} \tag{3.3}$$

where, "ϵ_{oil}" and "ϵ_{PP}" are the relative permittivities of oil and bobbin respectively.

Depending on the condition described in Equation 3.4, the displacement or conduction currents would dominate the E-field distribution within the insulation system.

$$\frac{\partial D}{\partial t} = \epsilon_0 \epsilon_r \frac{\partial E}{\partial t} << J = \sigma \cdot E \tag{3.4}$$

Considering the materials used in the current design and the stress applied, the conductivity cannot be neglected and hence the model for E-field must be based on the electrical conduction field. Equation 3.4 would in this case be satisfied and the conduction currents would dominate the displacement. The material with the lowest conductivity would face the highest E-field, and as will be explained in further chapters, this reduces the stress on the insulating oil and renders the assembly safe from breakdowns [16].

3.3 Insulation

The stressed E-field regions define the voltages experienced across the materials. The materials in the transformer should be capable of withstanding these stresses. Here are some of the desired qualities of a good insulation [17].

- High Dielectric strength
- Low Dielectric constant

3.3.1 HV Insulation

The transformer is placed inside a tank containing the insulating oil to facilitate cooling and provide safety while generating a high voltage output. The strength of the insulating oil is largely affected by the gap width, along with the material properties of the electrode surfaces and coatings used [16].

The barriers created by adding coatings, plastic bobbin, and plastic sheets between PCBs, help in sub-dividing oil gaps. While the gap width reduces, introducing a dielectric material increases dielectric strength. This is due to the formation of fiber bridges preventing particle/charge carrier drift. These barriers also reduce stress on the oil [16].

The shape of the electrode plays a major role in determining streamer ignition. Since E-fields tend to concentrate at sharp geometries, it is usually recommended to keep rounded conductors to reduce the chances of streamers being formed. This includes the PCB traces' edges and soldered connections that need to be rounded.

Coatings are applied over conducting, as well as non-conducting surfaces, also to prevent streamer formation [18]. The quality of the oil and the coating of the electrode makes a significant difference to the inception field strength. Streamer formation is limited to the gap width, and the inception field strength for a discharge to occur increases as the gap width reduces, Section 3.4.1.4 in [16]. The empirical relation is described by Equation 3.5 and this can be used as a basic dimensioning guideline for AC voltage test loading of oil gaps.

$$E_{BD} = E_0.(d)^{-a} \tag{3.5}$$

where "d" [mm] is the gap distance, and "a" is a factor derived from the slope of the discharge inception field strength standard plot, indicating the quality of oil and insulation of electrodes, for mineral oil [16].

The oil gaps within the transformer tank in this study are designed according to the insulation of the electrode and the saturation levels of the oil. Stresses of 5-10 kV/mm for AC voltage are permitted within these oil gaps to avoid a breakdown [16]. This is dependent on the local field strengths within the transformer assembly. To ensure the safety of the transformer setup and avoid breakdowns even after several years of operation, the operating field strengths are much below the actual. In practice, stresses on the oil gaps are restricted to 70% of their value. In this study, the stress on the insulating oil is hence restricted to 7 kV/mm, considering an AC stress of 10 kV/mm on the oil gaps. The materials and their properties are chosen and dimensioned in such a way that the insulating oil is within the safety limit of 7 kV/mm [16].

To obtain optimal distances from standards for insulation, some of the extreme voltages and E-fields experienced in the transformer's geometry were studied and referenced with Equation 3.5 to ensure safe distances. These are presented in Table 3.1.

Table 3.1: Maximum Voltage experienced for 20-20 turn PCB

Between following points	V_{max} (kV)
Trace-to-trace	0,125
Inner trace to inner core leg	48,75
Outer trace to outer core leg	50

The use of barriers in oil gaps greatly increase the dielectric strength; the gap widths are reduced and the drifting of particles and charge carriers over larger gaps is prevented. Impregnated pressboard barriers causing subdivisions in the oil greatly increase the dielectric strength because of these insulating boundaries. Hence, smaller dimensions can be achieved for transformers, with reduced magnetic leakage flux, weight, dimension and cost [16].

3.4 Diode for Rectification

The required output of the transformer is DC. Diodes can be used to rectify the AC output of the secondary into DC. The diodes will be connected in the form of a bridge rectifier. Slight conduction loss is observed in every diode. For light to no loads, the output will be the peak of the sine wave, and for heavy loads, it will be

$$V_{DCout} = 0.9 \cdot V_{RMS} \tag{3.6}$$

For diode loss in the case of the current design, only conduction loss was considered, since switching loss was found to be negligible.

3.4.1 BYT78

BYT 78 is a fast switching diode having soft recovery characteristics and low reverse current, well-suited for high voltage high frequency rectification. The sintered glass case and spherical shape make it suitable for HV applications [19].
Due to its semiconducting properties, there will be a small voltage required by the diode to start conducting in forward bias. Hence there is a voltage difference observed across the diode terminals in forward bias called "forward voltage" $V_{FORWARD} > 0V$.
This voltage difference across the diode causes conduction loss and is described using Equation 3.7

$$P_{LOSS} = I_{DIODE} \cdot V_{FORWARD} \tag{3.7}$$

3.5 Output Rectification

The rectification can be done in single or multiple steps. The process can be explained by considering a simple step-up transformer (turns in diagram do not reflect actual number of turns) that uses only one core to get the required output. From insulation standards, this cannot be achieved.
Splitting the secondary turns into planar PCBs gives the setup in Figure 3.4. This is the case of standard rectification, which is the same as having a single multi-turn coil and having the ends connected to the full-bridge rectifier.

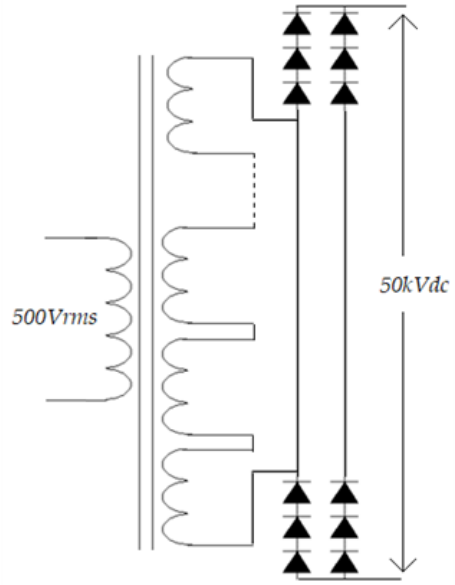


Figure 3.4: Standard output rectification

Standard rectification works well at lower voltages and frequencies, however there are limitations while considering the insulation requirements of high voltage transformers. This can be addressed by integrated rectification, which reduces AC field stresses across the coils and also prolongs the ageing of the insulation system [4].
The splitting and individual rectification of the secondary windings into separate,

winding sections of desired geometry and proportions, which are later connected in series is known as integrated rectification, as illustrated in Figure 3.5.

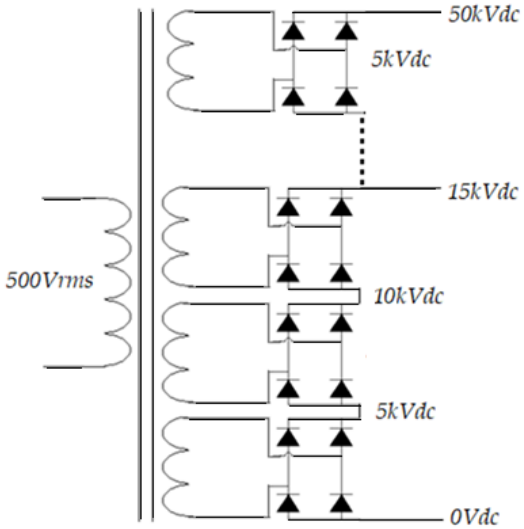


Figure 3.5: Integrated/ Stage output rectification

The diodes in integrated rectification can be of a lower rating (or lower in number) since the voltage across each coil is lower. The DC output is connected to a load through a low pass filter (capacitor C_F). Although the output voltage between the two setups is not affected, it will impact the E-field distribution in the transformer. The secondary with integrated rectification enables the separation of the E-field into AC and DC components. The introduction of a DC field implies an associated reduction of the AC field. This has proven to be beneficial since high magnitude high frequency E-fields can give rise to partial discharge problems in the insulation materials [4]. The separation is governed by the winding structure and the number of winding sections. To consolidate these points, the benefits of integrated rectification over standard rectification are:

- Reduced inter-layer field strengths
- Prolonged ageing of insulation system
- Reduction of AC stress in the windings (hence lower chances of partial discharge)
- Major portion of the winding capacitance is moved to the DC side of the rectifier

From these conclusions, the best choice in the case of a HV planar transformer is to use integrated rectification.

3.6 Stray Capacitance and Optimization

Stray capacitance is an unavoidable, parasitic capacitance, due to parallel arrangement of conductors. High frequency systems encounter this and with increasing frequency, the losses increase. At extremely high frequencies, capacitors can act as conductors. All circuit elements such as inductors and wire wound resistors have a

capacitance due to the geometric arrangement of the conductor. At high frequencies, it causes them to move further from their ideal characteristics [16].

Stray capacitance can also combine with stray inductance to give parasitic oscillations. There are two stray capacitances in this transformer design; the self-capacitance within the planar traces in a single PCB, and between the stacked PCBs.
While this is a major issue in Radio Frequency (RF) circuits, the transformer will operate at a maximum of 50kHz. Hence the losses are small but present. The proportionality of capacitance with regards to physical dimensions can be expressed using Equation 3.8.

$$C \propto \frac{A}{d} \tag{3.8}$$

where, "A" is the area of parallel plate exposure [mm^2] and "d" is the distance of separation [mm].

A few effective methods to reduce stray capacitance are based on the fundamental proportionality of capacitance [16].

1. Separation of wires (in case of traces, more plate spacing and less plate area)
2. Using guard rings
3. Using ground/power planes
4. Shielding between the input and output

The priority is to ensure electrical insulation and since the operating frequency is low, it results in low stray capacitance effects. The design is meant to ensure that there is no inception or chances of breakdown. Taking this into account, ways to reduce C_{stray} are considered optimization and not elaborated in this thesis work.

4

Transformer Primary Calculations and Setup

This chapter describes the methods followed for choice of core and primary winding, simulations on COMSOL for B-field, and loss calculations.

4.1 Transformer Input and Output Specifications

The transformer's input supply provided by the SCR system, and the output specifications are presented in Table 4.1.

Table 4.1: Transformer specifications

Parameter	Value
Primary voltage	$500V_{rms}$
Primary current	$50A_{rms}$
Secondary voltage	$50kV_{DC}$
Secondary current	$0.5A_{DC}$
Frequency	50kHz

4.2 Transformer Design Procedure

The design method followed for the high frequency, high voltage planar transformer is illustrated in Figure 4.1. Each step is further elaborated in following sections, with conditions and calculations.

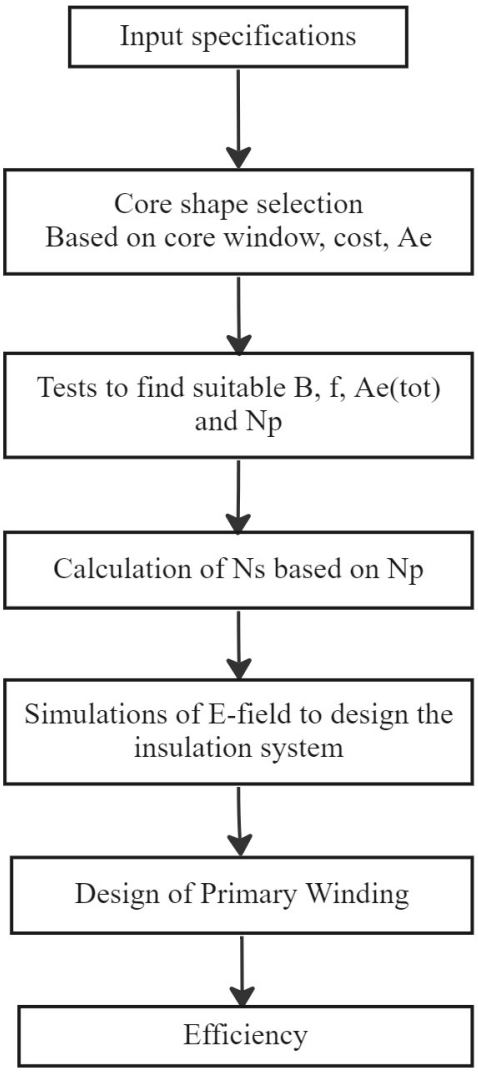


Figure 4.1: Design method for the high frequency planar transformer

From the input parameters and the output desired, primary and secondary turns are obtained. The permissible flux density is calculated with the limit of saturation, and the number of cores are chosen. Based on required insulation, the core dimensions are chosen, and the availability and ease of assembly leads to the choice of material and shape respectively. Core and winding losses are calculated, and this can lead to change in number of primary turns and B_{max} values. From tests, the number of primary turns were narrowed down to an optimal number. These are setup on COMSOL and the B-field is simulated.
For the secondary, number of turns are calculated using Equation (5.1). From this, the number of PCB stacks required can be calculated to obtain the required output voltage. The secondary current, that the PCB must handle, gives the optimal trace width. Insulation considerations here are the trace gap, clearance and creepage distances, use of bobbin and PCB coating. To find the setup with the least E-field stresses, the secondary is modelled for 40 turns.
To calculate the efficiency of the transformer, the core and winding losses of the

primary, the AC loss of the secondary, and the diode loss are considered.

4.3 Choice of Core

Considering the electrical requirements of the transformer's core, the suppliers and materials shown in Figure 4.2 are available.

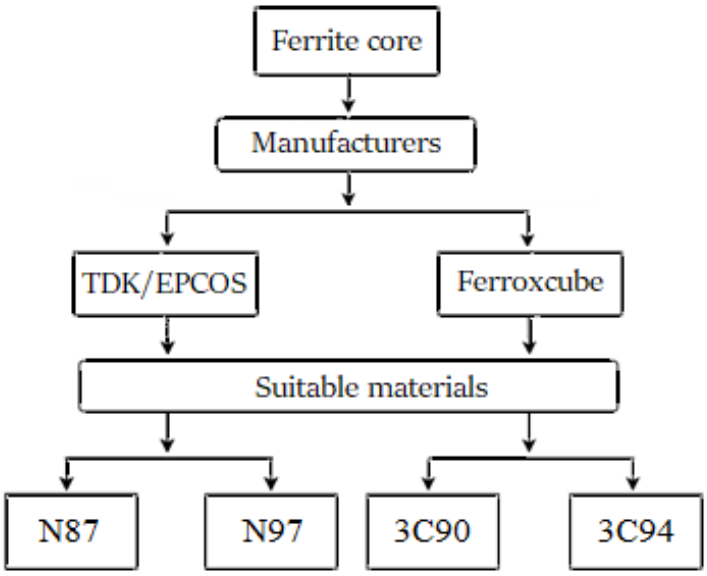


Figure 4.2: Core suppliers and materials

For the transformer, the U-shaped core appears to be most suitable based on supplier datasheets. The core material is made of ferrite. Based on a Manganese-Zinc composition, it has a high resistivity that reduces eddy currents to a negligible value. Since E-cores have a small window area, U-cores were assembled to form the shell-type design. Based on design limitations and material availability, the standard core shape U93/76/30 is chosen. This core has the largest cross-section area, hence requiring fewer parallel cores. Certain assumptions, such as taking 2,3, and 4 primary turns were considered as a starting point, after which the values were optimized to obtain the number of parallel cores that returned the least losses for the specifications. For the chosen shape, core dimensions, temperature range and frequency, the material N87, from the supplier TDK, has been found to be the most cost-effective solution [11].

After the core is chosen, the flux density must be deduced based on the frequency and core properties. Theoretically, it is advised to choose the operating B_{max} value at the "knee" of the curve which is the closest to saturation. However, on practical implementation, it was found that operating close to B_{sat} causes excessive heating due to the large volume and local hotspots, further accentuated due to several cores making up the main core instead of a single solid core. This works well for cores with smaller volume but otherwise the heating implications are severe and can lead

to thermal runaway. Hence it is preferred to keep the operating B_{max} at a lower value.

4.3.1 Core Calculations

The properties of the core U93/76/30 with the material N87 are presented in Table 4.2 from [11].

Table 4.2: Core properties of N87 Ferrite

Material Property of Core	Value
Relative permeability	3600
Effective area (m^2)	0,00084
Volume, per pair (cm^3)	297
Length of magnetic path (m)	0,354
Saturation flux density, $B_{sat}(T)$	0,39
Steinmetz coefficients	
α	1,8392
β	2,9104
K_c	10,67

The Steinmetz coefficients "α" and "β" may be found from the manufacturer's datasheet. "K_c" can be calculated from the value of power loss "P_v", given by the manufacturer, using Equation (2.16). For the core material N87, the coefficients, presented in Table 4.2, are defined for a frequency of 50kHz.

It is also noted that, given the properties of N87 Ferrite, $\beta > \alpha$. From Equation (2.16), variation of B_{max} largely affects core loss, hence it is desirable to minimize B_{max} by varying N and A_e. From factors described in Subsection [2.2.1], and the window area of the chosen core, $N = 4$ primary turns was found to be the best choice. Increasing the turns over $N = 4$ would mean that greater secondary turns, or increased number of stacks would be required to maintain the transformer's turn ratio, which would not fit within the core window according to insulation standards. Reducing the number of turns from $N = 4$ would require an increased cross-section area, leading to increased material cost.

The magnetizing inductance is calculated for each combination of cores and flux density. For this, it is necessary to calculate the reluctance of the core. The equation used to calculate the magnetizing inductance "L_m" and reluctance "R_c" are described by Equations (2.13) and (2.14) respectively. Based on the equations and data, the volume loss and magnetizing inductance are calculated as tabulated below. From the calculations presented in Table 4.3, the core's total reluctance "R_c", magnetizing inductance "L_m", and core loss (Hysteresis) were found for 4 primary turns carrying $500V_{rms}$, at 50kHz.

Table 4.3: Calculations for core at a frequency of 50 kHz

Parallel cores Units	B_{max} Tesla	% of B_{sat} %	Core loss mW/cm^3	Volume loss kW	R_c kH^{-1}	L_m mH
1	0,37	95,39	800,02	0,48	53,42	0,3
2	0,19	47,70	106,41	0,13	26,71	0,6
3	0,12	31,80	32,70	0,058	17,81	0,9
4	0,09	23,85	14,15	0,03	13,36	1,2
5	0,07	19,08	7,39	0,02	10,68	1,5

The calculations presented in Table 4.3 present the core loss for different number of parallel cores for $N = 4$. With regards to the core's temperature rise as presented in Table 6.1, material cost, and operating frequency, the option of 3 parallel cores was found to be most suitable.

4.3.2 Core Packing

The assembly of the cores also needs consideration. Since they are discrete units, any gaps in assembly will mean there is air introduced into the magnetic path, and the much weaker magnetic permeability of air will not let the transformer transfer power and will cause hotspots between cores. Gluing them together would require the material to have both high magnetic permeability as well as a long life, as the core will operate at 100^0C. Existing solutions within time and cost feasibility indicate that the glue will lose its properties after several thousand hours of operation, hence robust mechanical packing has been considered.

4.3.3 Measurement of Core Loss

As mentioned in Section [2.3.1], the core material can be characterised using the core loss data. The core loss is plotted for different frequencies, voltages and flux densities. Hence, to find the core loss, 12 pieces of the U93/76/30 core are assembled as two E-cores to form a shell-type construction. The primary and secondary windings are wound on the middle leg with four turns each. From the manufacturer's data and the core dimensions, the cross-sectional area is found to be 5040 [mm^2]. The equipment used for the measurements are presented in Table 4.4.

Table 4.4: Instruments used in core loss measurement

Instrument	Model
Oscilloscope	Tektronix MD04104C
Rogowski current probe	CWT mini 3B
Differential probes	Tektronix THDP0200
Heat camera	FLIR E60

Figure 4.3 illustrates the core loss measurement setup. A variable 3-phase voltage source is rectified and applied to a full bridge converter of variable frequency. The output of the full bridge is connected to the primary winding with a capacitor (1,25

μF) in series. The primary current is measured with a Rogowski probe and the secondary voltage is measured with a differential probe. Using a digital oscilloscope, the two signals are obtained and the average power is calculated by multiplying the signals and utilizing the built-in mean function.

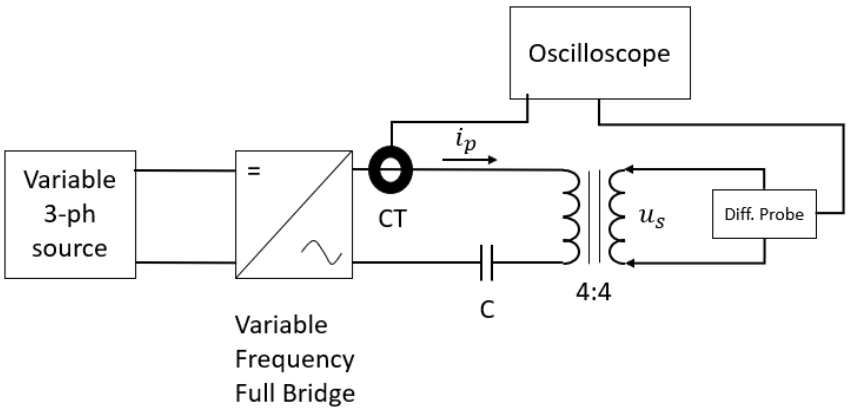


Figure 4.3: Core loss measurement setup

Using this setup, the average core loss was measured for variations in frequency, flux density and voltage, presented in Chapter 6.

4.3.4 COMSOL Simulations

The FEM-based software COMSOL Multiphysics 6.0 is used throughout this thesis work to verify and support calculations. Under the core, B-field distribution and magnetizing inductance are mainly simulated for the core's dimensions.

4.3.4.1 Geometry

The core was built using the 3D geometry facility, with dimensions from the data sheet [11]. The geometry is shown in Figure 4.4. The material properties of interest are mainly the magnetic permeability of the cores and electrical conductivity of the coils, presented in Table 4.5.

Table 4.5: N87 material properties used in COMSOL

Material property	Value	Unit
Electrical conductivity	1e-12	S/m
Relative permittivity	1	
Magnetic field norm	normH	A/m
Magnetic flux density norm	normB	T

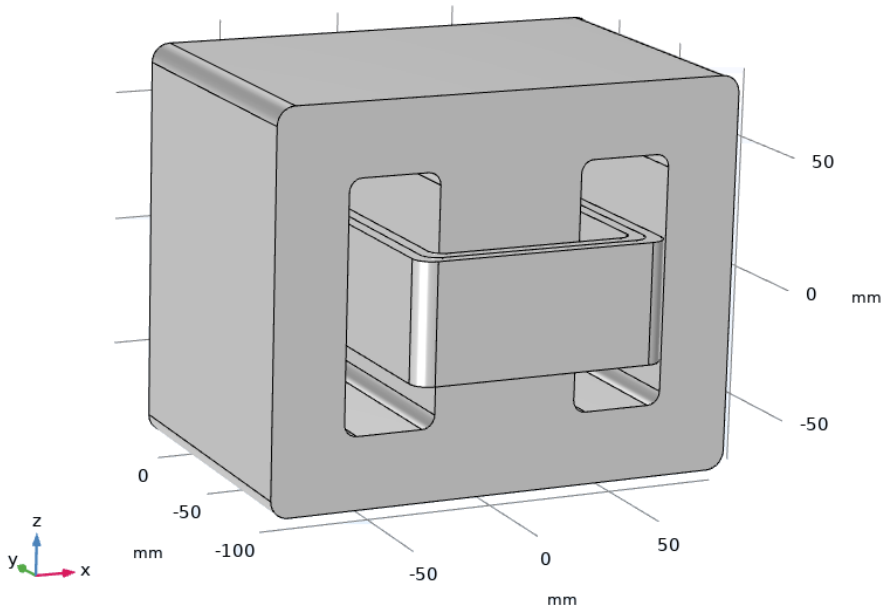


Figure 4.4: Core geometry setup in COMSOL

Since the ferrite core does not have a fixed magnetic permeability, it has been defined as a function of the varying magnetization with respect to the applied B-field. The values are graphed in the BH-curve by interpolation from the core material's data sheet [11], using COMSOL's "BH-curve checker" application, as shown in Figure 4.5.

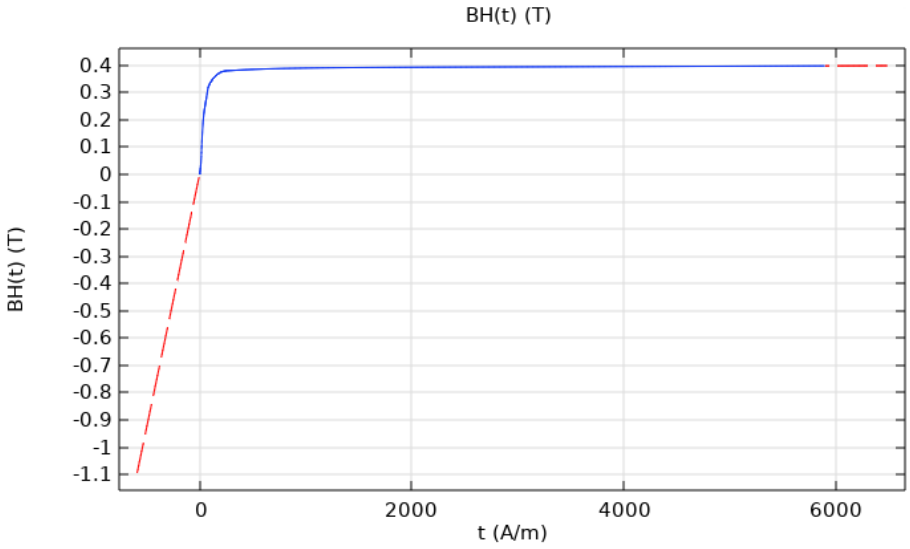


Figure 4.5: BH interpolation of N87 ferrite

4.3.4.2 Mesh

The "free tetrahedral" option allows us to choose the meshing degree for different domains, hence domains such as air, and the coils were given normal meshing sizes.

The core was given a finer mesh, considering the filleted and sharp edges that can cause changes in results, if not meshed properly. The meshed geometry is shown in Fig 4.6.

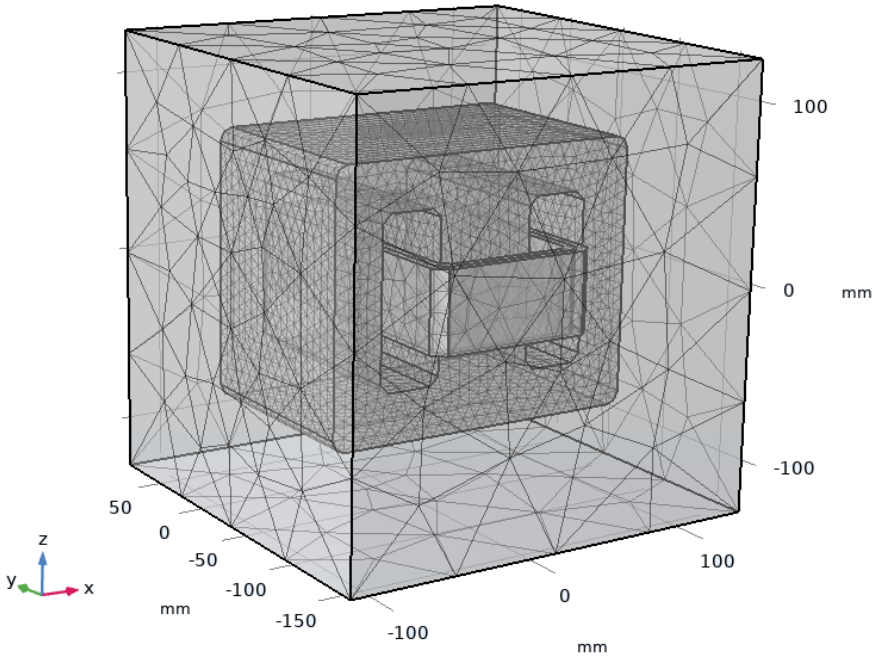


Figure 4.6: Free Tetrahedral (Selective) meshing

The mesh statistics of the core geometry are presented in Table 4.6.

Table 4.6: Mesh statistics

Domain	Mesh type	Mesh size limits
Air	Extra coarse	13,5 mm - 75 mm
Core	Normal	2,7 mm - 8 mm

4.3.4.3 Physics

To study the B-field, the "magnetic fields" physics was chosen for simulation. The "coil" option was used to identify the coil carrying the primary current. Only the primary coil was considered since the objective here is to obtain B-field which is independent of the load. "Effective BH curve" was the mode of coil induction to account for the non-linear BH curve of the core. The entire geometry had a magnetic insulation across its boundary to limit the simulation, with no initial value (initial magnetic field = 0 Wb/m in all axes).

4.3.4.4 Study

A frequency sweep was performed for 50kHz in a period of 20 steps from 0Hz. The magnetic flux in the core is in phase with the magnetizing current, which lags the supplied current by 90 degrees. Since the flux is also alternating as it is in the case

of any transformer action, a frequency sweep helps in gauging its values as it varies with time.

An additional study “Coil geometry analysis” was chosen for COMSOL to realise the coil’s structure before the frequency sweep is performed. This feature enables us to define a physical domain that is not necessarily "coil" shaped, and whose properties are defined as a coil having a certain number of turns.

4.3.4.5 Equations

The governing equations that COMSOL uses to compute this model in frequency domain study include Maxwell’s equation of Ampere’s law, Equation (2.1). This explains how the alternating current generates a magnetic field around the current’s axis. The current density is found using Equation (4.1).

$$J = \sigma E \tag{4.1}$$

where, "J" is the current density, expressed as the conductivity of the material "σ" times the applied E-field.

The curl of the magnetic field at any point in space is equal to the obtained current density at that point. This relates magnetic fields to moving charges described by Equation (4.2).

$$\vec{B} = \nabla \times \vec{A} \tag{4.2}$$

where "$\vec{A}$" is the tangential component of the magnetic potential. The Electric field under frequency domain is described by Equation (4.3).

$$\vec{E} = -\frac{\partial \vec{A}}{\partial t} \tag{4.3}$$

4.4 Boundary Conditions

Boundary conditions are constraints that act as limits to solving one or many differential equations. Unlike initial value problems that have conditions defined for one extreme, and are solved in time, the application of electromagnetism is limited by spatial dimensions of the defined domain. It helps to constrain the behaviour of fields at a boundary where two different media intersect. An improperly defined boundary condition may lead to the convergence or divergence of an incorrect solution [12].

The boundary conditions for the electric current density defines the limits for the electric current within the concerned domain, the surface region acting as an ideal insulator. Only a surface charge can be contained at the boundary of the two media, described by Equation (4.4).

$$\vec{n} \cdot \left(\vec{D}_1 - \vec{D}_2\right) = \rho_s \tag{4.4}$$

where, "$\vec{D}_1$" and "$\vec{D}_2$" are the perpendicular "$\vec{n}$" electric flux densities $[C/m^2]$ of both media, and "ρ_s" is the boundary surface charge "C".

The boundary conditions for $\vec{A}$ contain the magnetic field within the concerned domain, causing the magnetic field at the boundary to be tangential. It is described by Equation (4.5).

$$\vec{n} \cdot \left(\vec{B}_1 - \vec{B}_2\right) = 0 \tag{4.5}$$

where, "$\vec{B}_1$" and "$\vec{B}_2$" are the perpendicular "$\vec{n}$" electric flux densities $[C/m^2]$ of both media.

4.5 Primary Winding

For a DC input, the conductor exhibits I^2R loss, and the resistance is given by the resistivity of the material at that temperature, its length and cross section. The AC resistance is given by a coefficient for skin effect and proximity effect. The primary Litz winding is purchased from the manufacturer PACK [13].

4.5.1 Primary Winding Geometry

The primary winding was designed using litz wire, based on [14]. The benefit of using litz wire as described earlier is to reduce AC effects. By reducing the diameter calculated by several factors including operating frequency, the transmission almost acts as DC, and the compensation for using lesser cross section is done by increasing the number of such strands. Using the method described in Section [2.5], the litz wire parameters were designed.

- Using Equation (2.19), the skin depth at 20^0C for copper at 50kHz was calculated to be 0.3185mm.
- The winding parameters "b" and "Ns" are chosen based on the core window and number of primary turns respectively. The core window is 36mm, subtracting 3mm on either side for the bobbin, we have 30mm. The number of primary turns is 4 which is chosen as "N_s".
- The constant "k" is described as a value taken depending on the strand diameter. The diameter is chosen as δ/e. Within the skin depth, 67% of the current density exists.

  From the manufacturer's recommendation, for the skin depth of 0.3mm, the recommended diameter comes to 0.11mm. The corresponding "k" value is 1800, from [14].

  Recommended number of strands is given by Equation (2.21). For the chosen values, $n_e = 1215$, PACK offers a bundle of 1260 strands which is closest to the requirement. The distribution is $5 \cdot 5 \cdot 51$; 5 bundles of 5 smaller bundles, with each carrying 51 copper strands of 0,1mm diameter.

Table 4.7: PACK's RUPALIT V155 Litz cable [13]

Cable parameters	Value	Unit
Copper area	10,013	mm^2
DC Resistance	1,762	$m\Omega/m$
No. of strands	1260	-
Diameter of each strand	0,1	mm
Type of cable	P155 G1	Litz wire
Construction	$5 \cdot 5 \cdot 51$	-

4.5.2 Primary Winding AC Resistance

The AC resistance of the winding is found by multiplying the DC resistance provided by the manufacturer, as presented in Table 4.7, with the AC loss factor found from Equation (2.22). The cable AC resistance is the AC resistance at the transformer's operating temperature, multiplied by the cable's length, as presented in Table 4.8.

Table 4.8: Primary winding AC resistance

Cable parameter	Value	Unit
Manufacturer provided DC resistance	1,762	$m\Omega/m$
Sullivan loss coefficient for AC	2,32	-
Calculated AC resistance	4,087	$m\Omega/m$
AC resistance for 100^0C	5,362	$m\Omega/m$
Cable length	5	Meters
Cable AC resistance	0,027	Ω

5

Transformer Secondary Design, Calculations and Modeling Procedure

This chapter describes the design procedure followed for the secondary of the transformer, including PCB design calculations and arrangement, E-field setup on COMSOL and diode loss calculations.

5.1 Secondary Winding

As described in Equation (5.1), the turns ratio can be expressed as the ratio of respective voltages of the primary and secondary to the ratio of the respective number of turns. Therefore, the number of turns required for the secondary can be calculated, as presented in Table 5.1.

$$\frac{V_s}{V_p} = \frac{N_s}{N_p} \tag{5.1}$$

where, "V_s" is the voltage output at the secondary, "V_p" is the voltage at primary, "N_s" and "N_p" are the number of secondary and primary turns respectively.

Stacked PCBs are used in the secondary to provide the required output. Based on the requirement, number of stacks needed can also be calculated as presented in Table 5.1. These stacks are a total of 10, split into 5 on either side of the primary.

Table 5.1: Secondary turns and PCB stacks calculations

Secondary parameters	Value	Unit
V_p	500	V_{rms}
V_s	50	kVDC
Voltage per stack	5	kVDC
Number of stacks needed	10	-
Number of turns for:	Primary	Secondary
	3	30
	4	40

5.2 PCB for Secondary

This transformer design is meant to operate at 50kV. Since there is an idea on the number of secondary turns required, the geometry of the winding, required gaps and clearances need to be considered. The PCB design was first modelled in COMSOL Multiphysics for optimization and validation, and further designed using the Altium tool, for placing orders with suppliers, which is not elaborated here. The coils are arranged on a PCB for the following reasons.

- Mechanical support offered by the PCB to hold the coils.
- PCB's insulation qualities, which along with the coating would enclose the windings' E-field stresses.
- Easy to manufacture and assemble PCBs.

These together form the basis of the "planar" arrangement of the secondary windings.

5.2.1 PCB and traces

While modelling the secondary PCB, several designs were considered. The objective is to obtain 50 kV from a set of stacked PCBs. Each PCB would have a planar winding and it would fit in the core window, with a suitable number of turns and a full-bridge rectifier across the output. Several such PCBs would be stacked and their terminals would be connected in series to obtain the full output. This could be done by having increased turns to have fewer stacks, or vice-versa as long as the output voltage is reached.
The factors that would define the construction of the PCB are listed here.

- For the PCB, with each turn, there will be downsides such as stray capacitance, fringe capacitance and parasitic capacitance.
- The increasing outward spiral will also increase length, causing an increase in resistance (geometric series) with linear increase in turns.
- There will be a limit on the number of turns since the core-window is 36mm for the U93/76/30 core.
- The trace width would have to be chosen for the amount of current and skin depth needed, and inter-trace width would have to be calculated to prevent inter-trace breakdown.
- Since the cores are grounded, the separation between the innermost (say *d1*) and outermost trace (say *d2*) would have to be sufficient.
- Inter-trace voltage difference would be $V_{max} \cdot (1/\text{total turns})$, but trace-core voltage can reach V_{max} during the peak.

5.2.2 PCB design calculations

The material used for the PCB in this design is an FR4 standard material and its properties are as presented in Table 5.2 [20].

Table 5.2: Properties of PCB FR4 material

Properties	Maximum value	Unit
Glass Transition Temperature, T_g	160	^{0}C
Ambient temperature, T_a	60	^{0}C
Operating temperature, T_0	105-130	^{0}C
Dielectric strength	45	kV/mm
Dielectric constant	4,4	-
Surface resistivity	$4 \cdot 10^{18}$	Ω

where, the glass transition temperature "T_G" represents the temperature at which the solid material loses its rigidity and becomes flexible. "T_O" describes the operating temperature. The dielectric strength and electric permittivity are useful in calculating the stress experienced under an E-field. The surface resistivity addresses its resistance to prevent creepage currents.

5.2.2.1 Dimensions of the trace

The trace design must consider the current handling capacity, insulation distances between traces and from core to trace. The allowable AC and DC resistances, stray capacitance and inductance values must also be considered.

- The first step was to consider the dimensions of the trace itself. The current it would carry is 0,5A$_{rms}$, at a frequency of 50kHz. Hence the cross-section would have to be chosen such that it can handle 0,5A$_{rms}$, and the width and height would have to accommodate for skin depth.
  The formula for calculating allowable current through an external trace is taken from the IPC-2221 standards - section 6.2 [21]

$$I = 0,048 \cdot dT^{0,44} \cdot A^{0,725} \tag{5.2}$$

  where, "dT" is the temperature rise above ambient in [^{0}C], "A" is the cross-sectional area in [mils], "I" is the maximum current in [A]. Rearranging to get the area as a function of current, we get -

$$A = \left(\frac{I}{0,048 \cdot dT^{0,44}} \right)^{\frac{1}{0,725}} \tag{5.3}$$

  To find the trace width required, the minimum required area is considered with available trace thicknesses from the PCB manufacturer. The recommended trace widths for given thicknesses at the ambient temperature $T_a = 60^0$C under IPC-2221 standards are presented in Table 5.3, as derived from [22].

Table 5.3: Recommended trace widths for different trace thicknesses

Trace thickness	Trace width $T_r = 20^0$ C	Trace width $T_r = 40^0$ C
70 μm	0,038 mm	0,025 mm
35 μm	0,076 mm	0,05 mm

However, while this gives an idea of the minimum cross section to handle the ampacity, it is the length of the trace that determines the resistance, and I^2R loss heating that can cause drastic temperature rise. Once the length is ascertained, the cross section is given a suitable margin to account for heating.

- The second step after finalizing the trace cross section is to decide the clearance and creepage distances. These factors are important to ensure HV insulation. Clearance is the shortest distance between each turn, and the voltage difference will be V_{max} · (1/total turns). This is to prevent breakdown between traces. This distance can be chosen for the dielectric (the worst case is to use air to get the safest values). This distance will also have to be considered to reduce creepage. Creepage occurs across the PCB layer's surface.
  Under the same IPC2221B standards (specifically 9592B rule for power conversion devices), track clearance required for external layers is presented in Table 5.4, as derived from [23].

Table 5.4: Track clearance required as per IPC2221B standards

$V_{peak}(V)$	Uncoated (mm)	Rule 9592B (mm)	Coated (mm)
125	1,25	1,45	0,4

- The other distance to be considered is between the traces on each extreme to the core since the outermost trace will be V_{max} itself.
- After obtaining the least and safest distance between traces, and the minimum core-trace distance, the turns can be modelled.
- After this, the resistances and other quantities can be calculated, R_{ac}, R_{dc}, L, C etc.

The minimum trace width offered by the PCB manufacturer PACK [13], is 0,254mm, which is well-above the margin, and affordable for this application.

While it is desirable to keep the number of secondary turns low to reduce both loss and ensure generous distances for insulation, operating the core at 2 and 3 primary turns showed extreme heating for 50kHz. Since 4 primary turns indicated a steady state temperature of 90^0C in air itself, the secondary now requires 40 turns to obtain 5kV per PCB. Simulations and calculations were done for a PCB design that had 40 turns split into two sets of 20 turns in the double layer "shifted" format, elaborated in further sections.

5.2.3 PCB turns distribution

An effective method is to use double-layered windings on the PCB; having a trace on the upper and lower portion, connected by "via" to complete the winding, and the terminals could be traced to the extreme edges.
Using double layered windings greatly reduces number of turns that would have to be squeezed on one side, and allows for a greater inter-trace gap. This also reduces creepage and field strength across the PCB and air/oil, but also poses some challenges. The parasitic capacitance greatly increases, and a proper geometry is

needed to address this carefully. Considering the PCB's thickness, the upper and lower layers have to be arranged such that the stray capacitance is reduced [24].

5.2.4 PCB resistance measurement

The 4-wire method was used to measure the DC resistance of the PCB. The quantities are presented in Table 5.5.

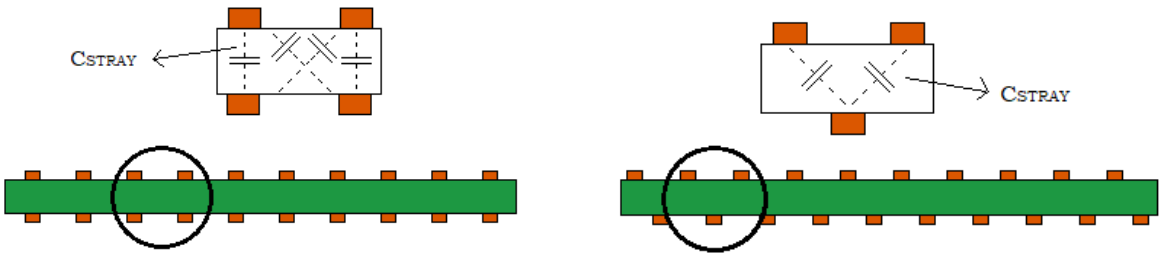
Table 5.5: 4 - wire testing for PCB trace DC resistance

Quantity	Value	Unit
Measured terminal voltage	7,4	V_{DC}
Applied current	0,49	A_{DC}
Ambient temperature	26	^{0}C
Calculated resistance	15,1	Ω
Estimated resistance at 100^{0}C	19,41	Ω

5.3 COMSOL Simulations

To assess the insulation distances required, the E-field distribution was verified for the secondary. This includes PCB geometry with different trace widths and gaps, presence of bobbin and PCB coating, placement of PCB with respect to the core, and arrangement of PCB stacks. The E-field stresses were then simulated, across transformer oil and PCB surface, to find the optimal insulation design for an output of 50kV.

Along with this, two distinct models were designed in COMSOL; one with layers in parallel and the other, with a planar offset in both x and y directions at lengths of the trace width. On superimposing in the latter case, both traces will fill in the gaps of the other. Comparing these two models, it was found that the shifted layers have a lower parallel plate capacitance compared to the parallel layers. The difference in geometries is illustrated in Figure 5.1.



(a) Parallel layers

(b) Shifted layers

Figure 5.1: Placement of secondary turns in different layers on a PCB

5.3.1 Geometry

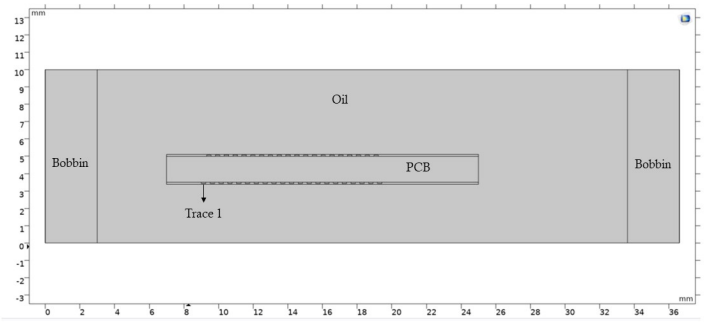
The E-field simulations were carried out using a 2D geometry for simplicity. The dimensions are not up to scale, however the distances are. The number of turns on the secondary are chosen relative to the primary turns; for 4 primary turns, there are 40 secondary, using Equation (5.1). The PCB and traces are placed at a distance from the core, validated in further sections, along with bobbin, PCB coating and transformer oil. The arrangement of the PCB stacks on either side of the primary winding is also validated with respect to distances and E-field stresses.
The permittivity and conductivity of the materials are considered for E-field simulations, and the corresponding properties used are presented in Table 5.6, [16], [18], [20], [25], [26].

Table 5.6: Relative permittivities and conductivities of different dielectrics in the geometry

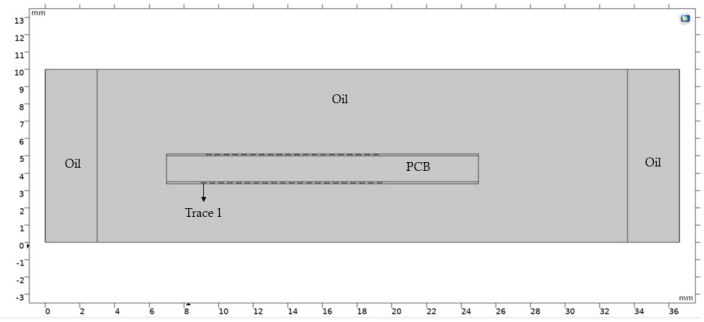
Material	Relative permittivity	Conductivity (S/m)
Bobbin	2,3	10^{-16}
Oil	2,2	10^{-13}
Copper traces	10^{12}	$5{,}96 \cdot 10^{7}$
PCB (FR4)	4,4	10^{-11}
PCB coating	4,4	10^{-11}
Mylar sheet	2,3	10^{-11}

5.3.1.1 Requirement of bobbin

In any conventional transformer, the core is surrounded by a plastic bobbin. The purpose of this is mechanical, to hold the primary windings in place. But, it also plays a role in electrical isolation between the core and the windings. With the present case, a plastic bobbin made of polypropylene, with a relative permittivity of 2,3 and conductivity of 10^{-16} [S/m], is used [16].
To plot the E-field and verify the need for bobbin in the present PCB design, the geometries shown in Figure 5.2, were modelled on COMSOL. The traces are given potentials with an offset of 125 V, starting from 48.7 kV at the first trace up to the final trace of 50 kV, which is the output required from the PCB as per the design.
To compare the effect of the presence and removal of bobbin, the geometry is kept intact, but the material properties are changed. In the first case, the geometry is modelled for the conductivity of the bobbin as presented in Table 5.6 as in Figure 5.2a and for the next case, the bobbin area has the conductivity of oil as in Figure 5.2b.
The E-field stresses are then observed across oil and compared for both cases to validate the requirement of the bobbin.



(a) Transformer with bobbin



(b) Transformer without bobbin

Figure 5.2: Geometry for secondary to compare E-field stresses with and without a bobbin

5.3.1.2 Comparison of Bobbin Materials

Thermoplastic polymers are used here since the bobbin must be capable of handling high temperatures and have high mechanical strength. To decide on the most suitable thermoplastic, a comparison study was conducted between Polypropylene (PP) and Polyamide (PA 12). The PA 12 material was used for the previous construction (transformer with nanocrystalline cores) and was therefore considered for the new planar transformer. Both materials have high thermal resistance and good mechanical properties. However, polyamides have high water absorption and conductivity, and exhibit higher losses. This makes the material less suitable for the high electrical stress of the application. While comparing other plastics such as PP, polyethylene, PVC and Polystyrene, PP has higher thermal resistance [16]. The motivation behind the choice of bobbin material is to keep the E-field across the insulating oil less than 7kV/mm, elaborated in Chapter 3. COMSOL simulations are carried out to understand the impact of both the materials on E-field distribution across the PCB geometry.

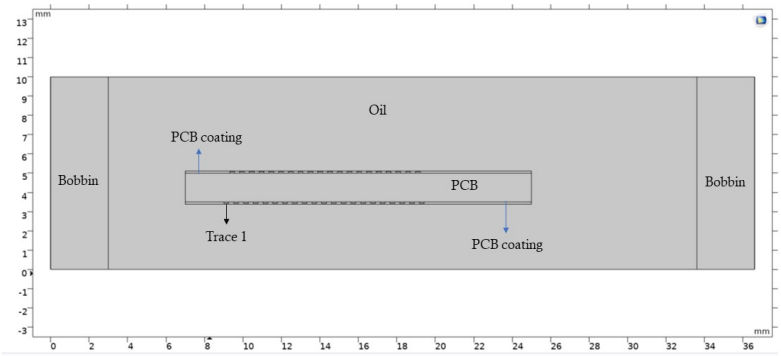
The dielectric properties and conductivity for PP and PA 12 are listed in Table 5.7 [25].

Table 5.7: Properties of bobbin materials

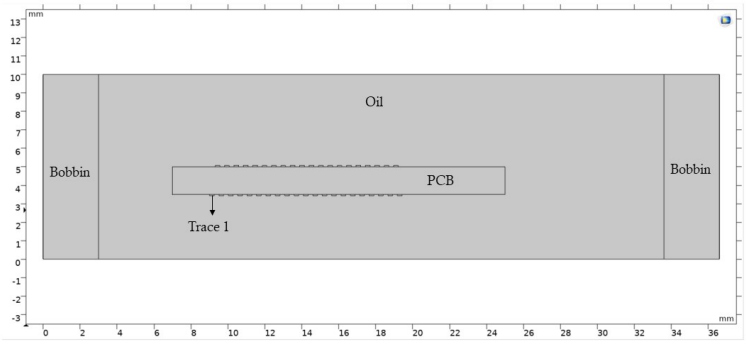
Material Units	Permittivity (Relative)	Dielectric Strength kV/mm	Conductivity S/m
Polypropylene	2,3	23-25	10^{-18}-10^{-16}
PA 12	4,5	26-30	10^{-11}

5.3.1.3 Requirement of PCB coating

To verify the need for the coating, COMSOL models were simulated with and without PCB coating as shown in Figure 5.3.



(a) With PCB coating



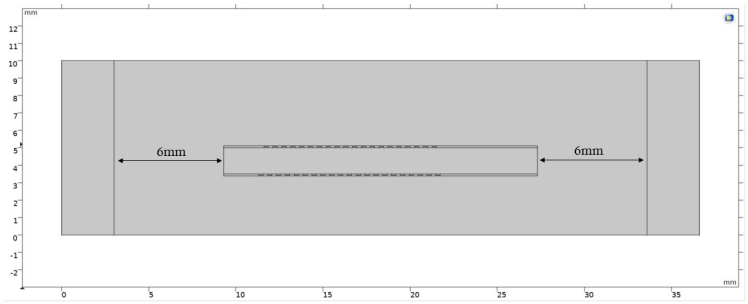
(b) Without PCB coating

Figure 5.3: Geometry for secondary to compare E-field stresses with and without the presence of PCB coating

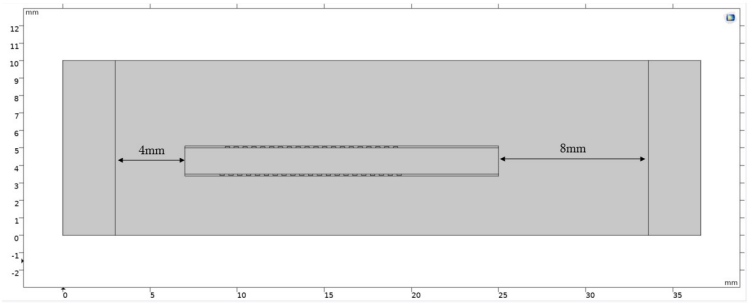
From the earlier section on insulation in Chapter 3, it is known that the stressed E-field regions can cause breakdown of materials in the transformer. It is necessary to have sufficient insulation and withstanding properties. With this consideration, the PCB is coated with an insulating material of higher breakdown strength. This helps reduce the stresses caused by high voltages on the PCB and the traces enclosed within the coating. The E-field models here have been simulated with a layer of a PCB coating called Pre-preg, the other possibilities include solder mask and conformal coatings [16]. The coating has been chosen as BEVI's "Ultimeg 2000/380 impregnating varnish". This has a dielectric strength of 166,6 kV/mm [18].

5.3.1.4 Position of traces and PCB

The position of the traces and the PCB with respect to the core has an influence on the E-field and the magnetic coupling. To study this behaviour, a geometry was modelled on COMSOL placing the PCB in the center of the core window shown by Figure 5.4a, and another geometry close to the middle-leg of the core, Figure 5.4b.



(a) PCB centered



(b) PCB close to core

Figure 5.4: Placement of PCB with respect to core to compare E-field stresses

5.3.2 Insulation distances between core and PCB

Taking the obtained values for trace width, height, and clearance, the PCB was modelled in COMSOL, as shown in Figure 5.5.

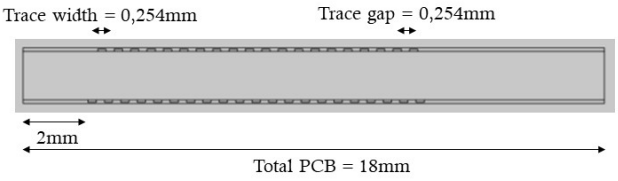


Figure 5.5: PCB design

Now that the dimensions within the PCB are defined, the placement of the PCB within the core window is shown in Figure 5.6.

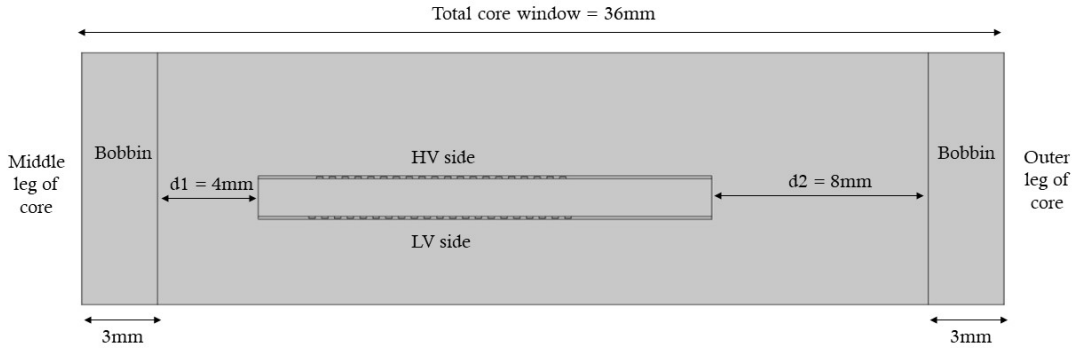


Figure 5.6: PCB placement in core window

Here, the distances "*d1*" and "*d2*" need to be chosen based on insulation, which can be described by the following points.

- The closer the PCB is to the middle leg of the core, better the magnetic coupling. Hence d1 is shorter than d2. This will also bring the HV side away from the outer core.
- d1 should not be too small such that E-field of oil between the core and the first trace is above the given average (7kV/mm).

From a parametric study of several distributions of d1 and d2, and from the conclusions of 5.3.1.4,
$d1 = 4$mm
$d2 = 8$mm
were found to be the best values to have fields within the average as well as low peak values at the extremes of the PCB.

5.3.2.1 Arrangement of the PCB stacks

The geometry of the planar transformer consists of 10 stacked PCBs, as illustrated in Figure 5.7. The PCBs are split into 2 halves, 5 PCBS above the primary and 5 PCBs below. Each PCB is designed as described in the previous sections and stacked with a Mylar sheet in between them. There are PP sheets for insulation at the top and the bottom of the core window, and at the center surrounding the primary. The E-field is simulated to check for stresses across oil, the bobbin, the traces and the PCB to validate this assembly. The distances indicated in the figure are obtained from COMSOL simulations to arrive at values causing the least stresses.

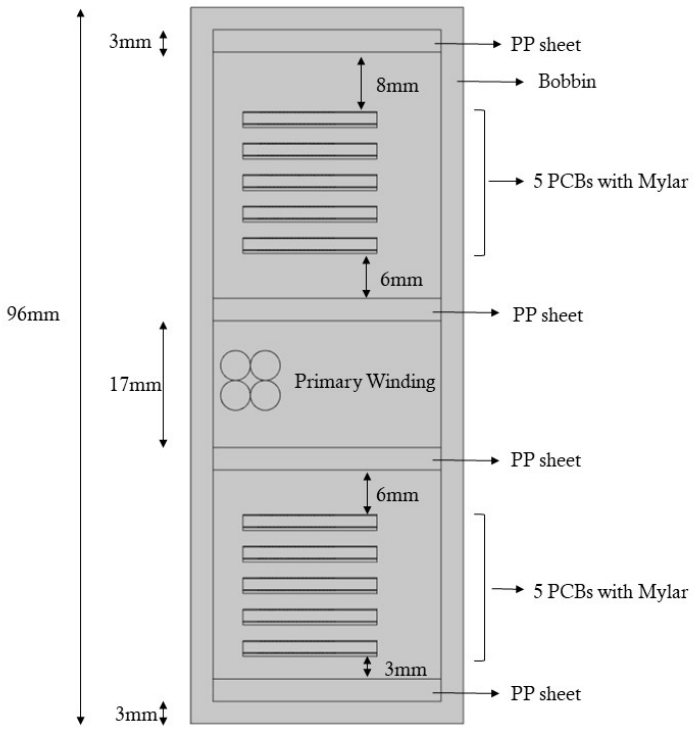


Figure 5.7: Stacked PCBs with primary winding

5.3.3 Mesh

The PCB geometry consists of several sizes and each domain of the geometry needs a mesh that takes into account the size of the domain and the boundary conditions, so it does not hinder the result. To achieve this, the "free triangular" option was chosen; the traces and PCB coating domains were given an extremely fine mesh, whereas the rest of the geometry was given an extra fine mesh.

5.3.4 Physics

To study the capacitive field with only the permittivities of the materials, "Electrostatics" is used for simulation. This interface uses the electric potential given as a dependent variable to compute the E-field distribution in the dielectrics, by solving for Gauss' law [27]. However, since the E-field distribution is decided by the conductivities of the bobbin and oil [16], the "Electric Currents" interface is used to simulate a conductive field. This interface uses electric potential as the dependent variable to solve the current conservation equation based on Ohm's Law [28].
The traces are given potentials with an offset of 125V to reach 50kV on the top layer, and the boundaries of the core are grounded.

5.3.5 Study

In COMSOL, the Stationary study sweep can be used to simulate steady-state conditions. In the case of an electrostatics physics interface to compute E-field distribution, this study is suitable since there are no dynamic dependencies and the electric potentials remain constant.
The Frequency Domain study can be used when the geometry is subjected to a harmonic excitation. In this study, the simulations are carried out for a frequency of 0 Hz.

5.3.6 Equations

The equations that govern the simulation of these interfaces in the stationary study specify the conditions for the electric field [29].
Faraday's law described in Equation (2.2), is derived here in its differential form defining the electric potential.

$$E = -\nabla \cdot V \tag{5.4}$$

The electric displacement field "D" for the Electrostatics interface is determined by Charge Conservation as in the equation

$$D = \epsilon E \tag{5.5}$$

where, "ϵ" is the permittivity of the material.

The conduction field "J" for the Electric Currents interface is determined by Current Conservation as in the equation

$$J = \sigma E \tag{5.6}$$

where, "σ" is the conductivity of the material.

5.4 Diode Loss Calculations

For practical purposes, the diode loss will have to be calculated considering its operating conditions. If a specific operating region is known, the V-I curve can be approximated to a straight line, which gives the slope, and can be used to calculate the dynamic resistance, "R_D". It is important to note that the graph will vary with different junction temperatures. The following formula is with respect to a fixed junction temperature, "T_J".

$$R_D(T_J) = \frac{V_F(I_{F2}) - V_F(I_{F1}, T_J)}{I_{F2} - I_{F1}} \tag{5.7}$$

The diode's datasheet provides graphs of its behaviour at two extreme temperatures, while the operating temperature of this design is in between these extremes [19]. So, a relation of how its forward voltage and dynamic resistance as functions of junction temperature was obtained from the extreme cases by use of a slope as illustrated in Figure 5.8, by,

$$V_{TO}(T_J) = \frac{V_F(I_{F1}, T_J) \cdot I_{F2} - V_F(I_{F2}, T_J) \cdot I_{F1}}{I_{F2} - I_{F1}} \tag{5.8}$$

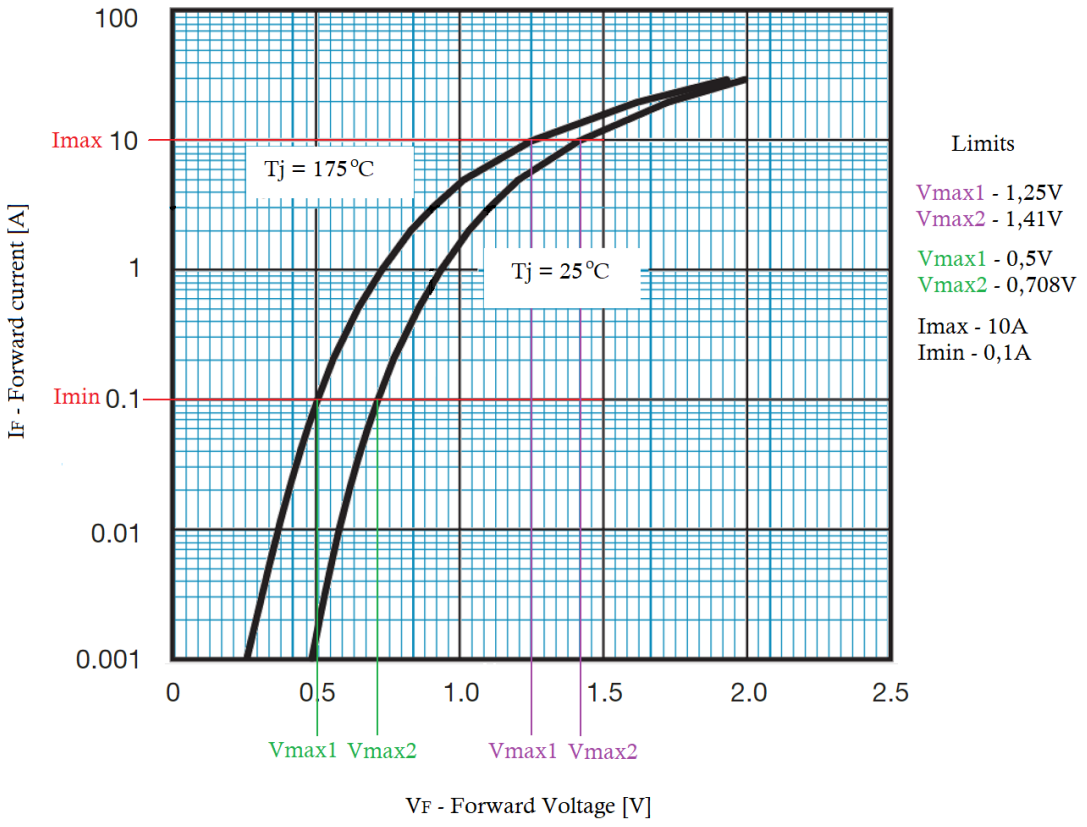


Figure 5.8: BYT78 diode - plotted characteristics [19]

5.4.1 Threshold and Forward voltages, and Dynamic resistance

The forward voltage, "V_F" is the voltage drop observed across the terminals of the diode while operating at a specific temperature and current, and "V_{T0}" is the threshold voltage to achieve conduction in the diode under those conditions. In an ideal case, $V_F = V_{TO} = 0V$, with the existence of a forward voltage required to conduct the diode $V_F = V_{TO} > 0V$. However, from the practical graph, the forward voltage is not along the y-axis over the threshold voltage and instead increases with current.
The voltage values were plotted after choosing two current values (0.1 and 10Amps, these are arbitrarily chosen but enclose the currents which the diode will face) and they were expressed as a function of junction temperature by comparison. For any junction temperature T_J, $V_{T0}(T_J)$, $R_D(T_J)$, and $V_F(T_J,I_F)$ can be calculated using Equations 5.9, 5.10, and 5.11 from [30].

$$V_{TO}(T_J) = V_{TO} \cdot (T_{JRef1}) + \alpha_{VTO} \cdot (T_J - T_{JRef1}) \tag{5.9}$$

$$R_D(T_J) = R_D \cdot (T_{JRef1}) + \alpha_{RD} \cdot (T_J - T_{JRef1}) \tag{5.10}$$

$$V_F(I_F, T_J) = V_F \cdot (I_F, T_{JRef1}) + (T_J - T_{Jref1}) \cdot (\alpha_{RV_{TO}} + \alpha_{R_D} \cdot I_F) \tag{5.11}$$

And the thermal coefficients are calculated using Equation 5.12 and Equation 5.13.

$$\alpha_{V_{TO}} = \frac{V_{TO}(T_{J_Ref2}) - V_{TO}(T_{J_Ref1})}{T_{J_Ref2} - T_{J_Ref1}} \tag{5.12}$$

$$\alpha_{R_D} = \frac{R_D(T_{J_Ref2}) - R_D(T_{J_Ref1})}{T_{J_Ref2} - T_{J_Ref1}} \tag{5.13}$$

There is a slight difference in the voltage expression when a sine wave and square wave are passed through the diode. For a sine wave, there will be a threshold voltage fixed by that junction temperature, and a current dependent loss which is defined as the dynamic resistance value (fixed here by junction temperature as well) multiplied by the square of the RMS value of the current to account for the AC current's loss (Not switching loss but conduction loss as a result of AC current).

For a square wave, the rectified waveform will have a constant voltage value causing a constant current and an off period, so it will simply be the forward voltage which is calculated at the junction temperature and the current, then multiplied by I_{avg} and duty cycle to get loss during square wave rectification.

5.4.2 Conduction loss calculation [30]

Each PCB has a full-bridge rectifier, with 10 series BYT78 diodes in each leg. At a given instant, two opposite legs will be conducting, with $I_{RMS} = 2A$ being the diode current. Across the entire transformer, considering all 10 PCB stacks, 200 diodes

will be active at an instant of operation. The schematic of one side of the PCB is illustrated in Figure 5.9.

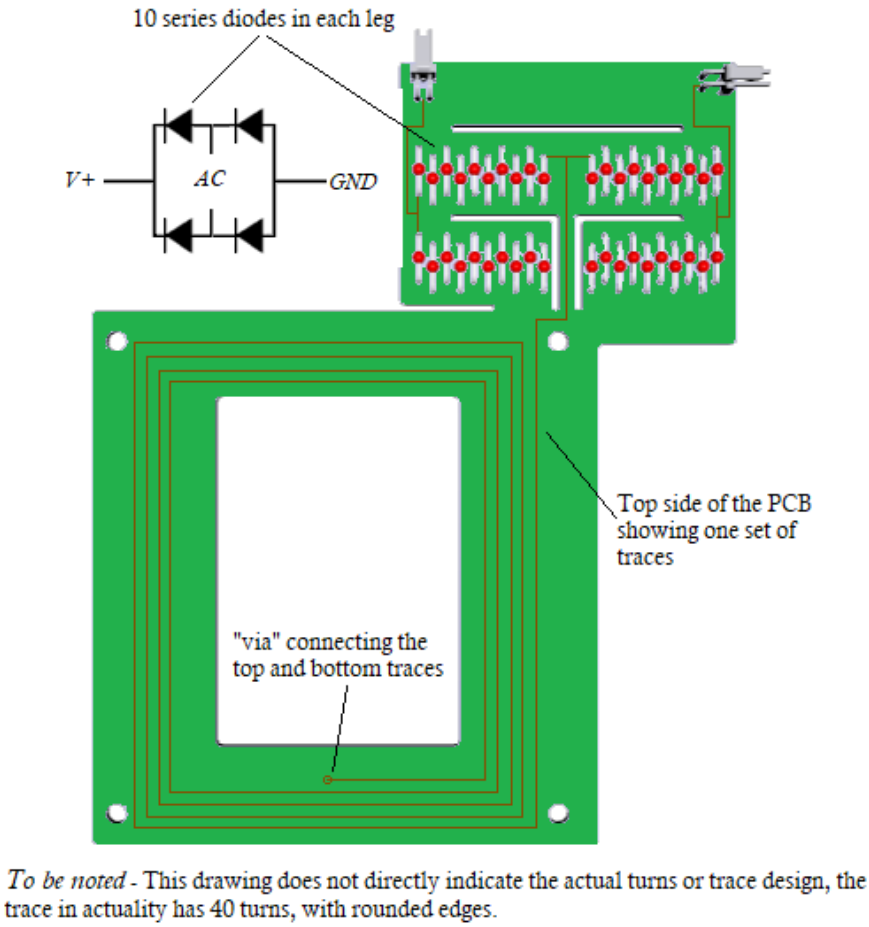


Figure 5.9: PCB trace with diode bridge

The method to calculate diode loss is described as follows [30].

1. Calculating conduction loss at a specific junction temperature.
   For a sine wave,

$$P_{COND}(T_J) = V_{TO}(T_J) \cdot I_{Favg} + R_D(T_J) \cdot (I_{FRMS})^2 \tag{5.14}$$

   $I_{RMS} = 0{,}5A$
   $I_{AVG} = 0{,}45A$

2. Obtaining V_{MAX} values at I_{MIN} and I_{MAX} for reference temperatures.
   From the datasheet, the reference temperatures are -
   $T_{J1} = 25^0C$
   $T_{J2} = 175^0C$
   The calculated V_{FMAX} values are presented in Table 5.8.

Table 5.8: V_{FMAX} for the extreme temperature values

I_F	$V_{FMAX}(I_F, 25^0C)$ (Volts)	$V_{FMAX}(I_F, 175^0C)$ (V)
$I_{MIN}(0,1A)$	0,708	0,5
$I_{MAX}(10A)$	1,41	1,25
$I_{RMS}(0,5A)$	0,854	0,645

3. Calculating V_{TO} and $R_D(T_J)$ in the application condition range.
From Equations (5.7), (5.8), (5.12), and (5.13), the values of V_{TO} and R_D for T_{JRef1} and T_{JRef2} are calculated, from which $\alpha(V_{T0})$ and $\alpha(R_D)$ are obtained, and presented in Table 5.9.

Table 5.9: V_{TO} and R_D at the reference T_J values

T_{JREF} (^{0}C)	V_{TO} (V)	R_D (mΩ)	$\alpha(V_{TO})(V/^0C)$	$\alpha(R_D)(\Omega/^0C)$
25	0,7	70,91	-1,39E-03	3,23E-05
175	0,492	75,76	-1,39E-03	3,23E-05

Using Equation 5.9,
$V_{TO}(T_J) = 0{,}735 - 1{,}387\text{E-}03 \cdot T_J$ [V]
Using Equation 5.10,
$R_D(T_J) = 0{,}0701 + 3{,}233\text{E-}05 \cdot T_J$ [Ω]

4. Finding conduction losses using Equation 5.14,
$P_{COND}(T_J) = 0{,}348 - (6{,}16\text{E-}04) \cdot (T_J)$ [W]

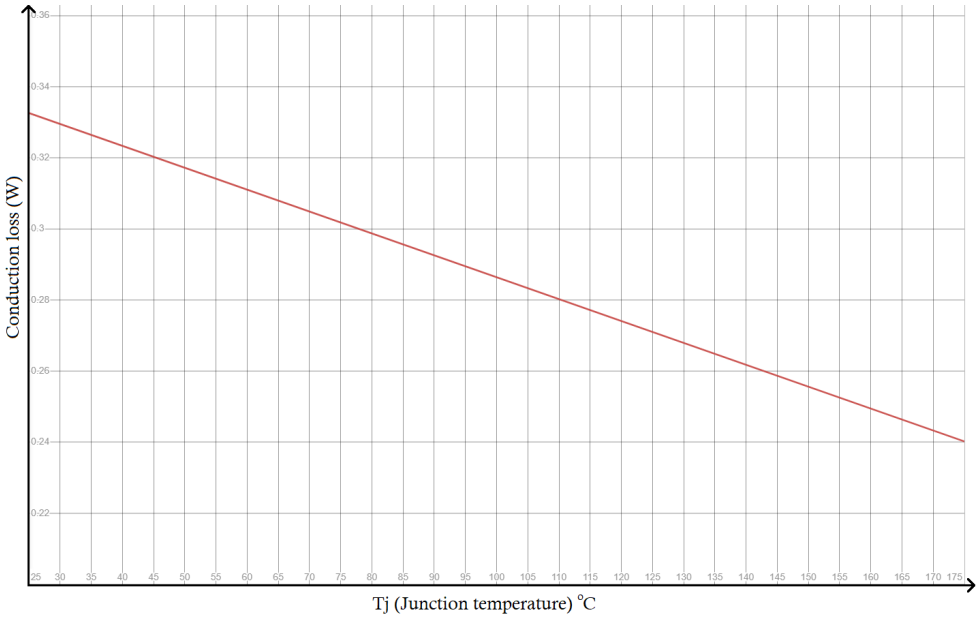


Figure 5.10: BYT78 conduction loss vs. T_J

From Equation 5.10 for $R_D(T_J)$, and P_{COND}, it is visible that the resistance increases and loss reduces with temperature, hence cooling the diode will reduce

resistance but can cause chances of thermal runaway. The low temperatures are hence chosen as the worst case.

5. For the required current to flow, the diode will reach a certain T_J, and its dissipation will depend on ambient temperature T_A. Using the value of 100^OC as the steady-state temperature of the diode, in Equation (5.14), the conduction loss per diode is obtained as
P_{COND} = 0,286 [W]

   The conduction loss for 200 diodes (across the entire transformer, during operation) is $200 \cdot 0,286 = 57,28W$.

6
Results and Discussions

This chapter presents the results for the primary and secondary COMSOL simulations. This includes the B-field and E-field plots for the core and PCB respectively.

6.1 Core and B-field

The maximum B-field is observed at half the time period with the critical regions as shown in Figure 6.1.

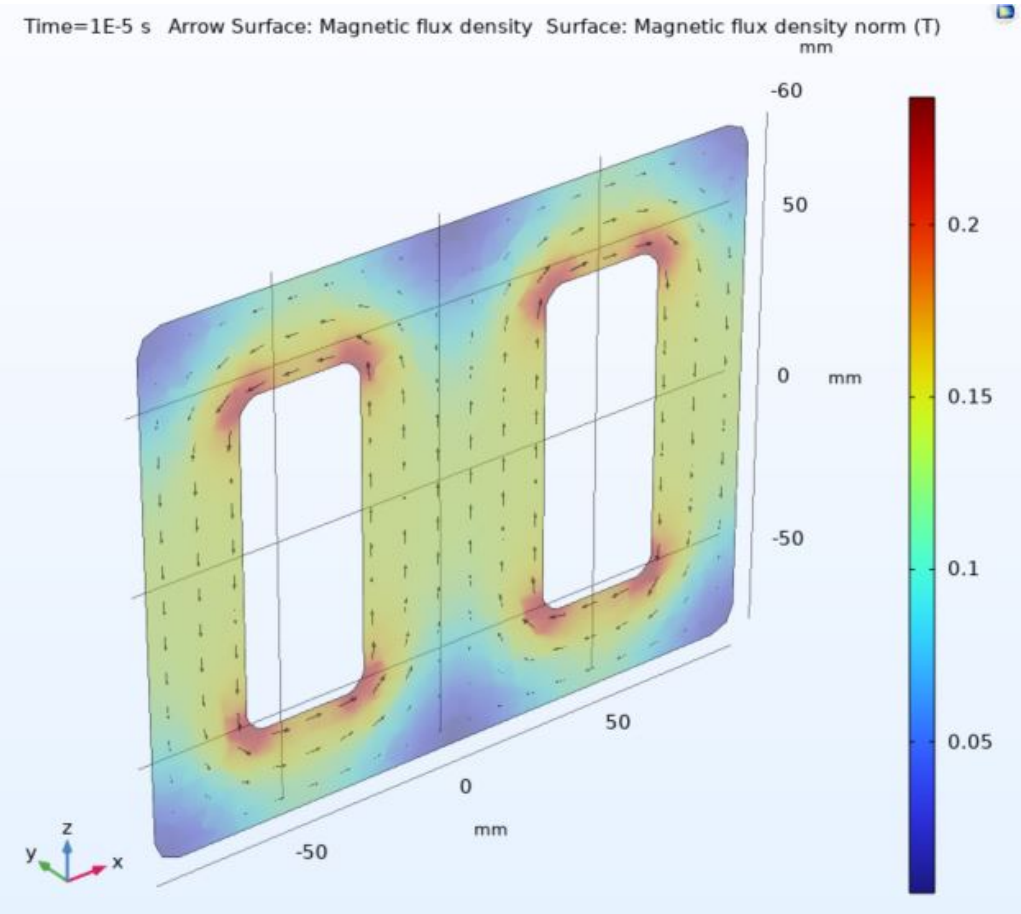


Figure 6.1: B-field 2D plot

The magnetizing inductance is simply the primary coil's inductance with no-load (open circuit) at the secondary. For the given frequency, core dimensions, and

BH curve of the material, L_m = 0.83 mH from Equation (2.13). From the B-field plot, the field distribution appears to be uniform along the magnetic path, with an exception at the edges. The field reaches a maximum of 0.14T at the center of the core's middle path. The edges exhibit a stronger field of 0.22T.

6.1.1 Temperature Rise Test on the Core

From the calculations presented in Table 4.3, the optimal values for number of cores, flux density and frequency are found. For this, the ferrite cores were tested in air, with different combinations of these parameters. From the tests, the temperature rise was observed for a period of one to four hours. The cores were given an input voltage of 500 V_{DC}.

Table 6.1: Temperature rise test of core

B [T]	Frequency [kHz]	Time [Hours]	Hot-spot temperature [^{0}C]
0,276	30	1	150
0,197	42	2	150
0,124	50	2	90
0,138	60	1	150

From the results in Table 6.1, it can be seen that with a flux density of 0,124 T, at a frequency of 50kHz, the temperature rise was found to be reasonable after stabilizing. In the other cases, the core rose to high temperatures rather quickly and the configuration was discarded.

6.1.2 Core Loss Measurement

From the core loss setup shown in Figure 4.3, core loss is measured for different frequencies, flux density and voltage levels. The results for the N87 material are presented in Table 6.2 and plotted in Figure 6.2.

Table 6.2: Core loss measurement results

f [kHz]	B [mT]	U_{dc} [V]	P_{avg} [W]
30	50	121	5,8
30	100	242	19,5
30	150	363	44
30	200	484	79
40	50	161	7
40	100	323	29,5
40	150	484	65
40	200	645	122
50	50	202	8.7
50	100	403	39,8
50	124	500	60
50	150	605	91,5

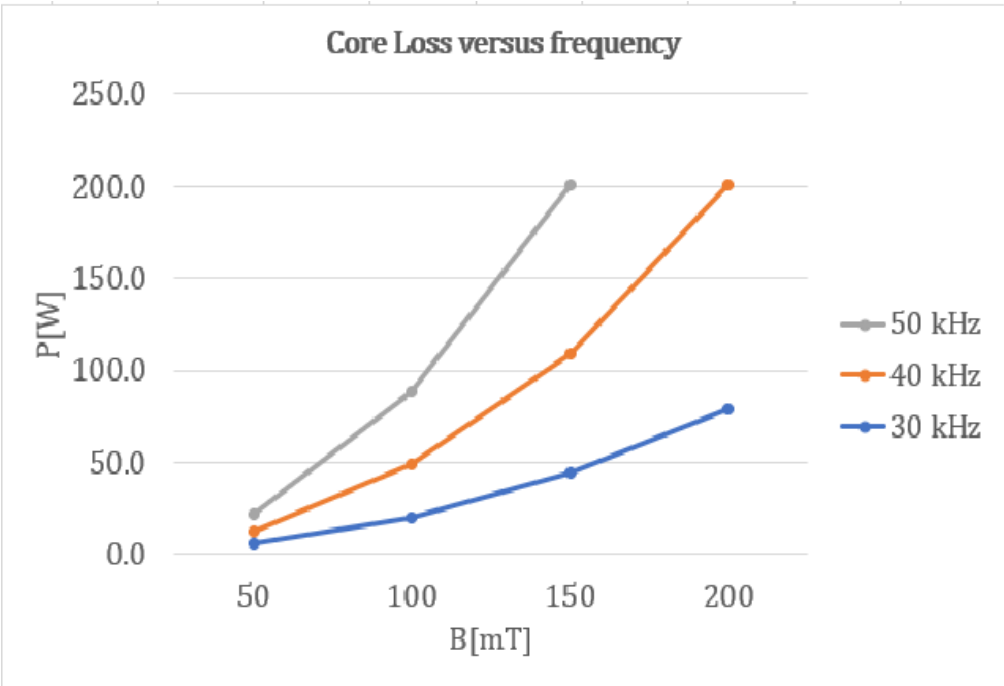


Figure 6.2: Core loss versus Frequency

Figure 6.2 shows how core loss is found to increase with frequency, for the same values of B[mT] described by Equation (2.16).
Comparing the calculations and measurements for 3 parallel cores at a frequency of 50kHz, flux density of 124 mT and 500 V_{dc}, the core loss values are approximately equal. Hence, the calculations are validated and the core loss measurement setup proves to be a reliable source of data for the core material.

6.1.3 Litz Wire dimensions

To calculate the value of k_s, the ratio of radius and skin depth must be less than 1,7 and it was found from Equation (2.19) to be 0,472 and hence the condition is satisfied. The value obtained for k_s is 1,001.

6.2 PCB geometry and E-field

As mentioned in Chapter 3, the conductivity of the materials influence the distribution and shape of the E-field within an electric conduction field and hence, the conductivities are considered here while simulating the secondary design. The geometries are simulated using the Electric Currents interface and Frequency Domain study.

6.2.1 Requirement of bobbin

For the geometry described in Figure 5.2a, the E-field is plotted across the bobbin-oil-PCB coating until the first trace on the LV side. This is the trace closest to the

middle leg of the core.
The line plot for the E-field is presented in Figure 6.3.

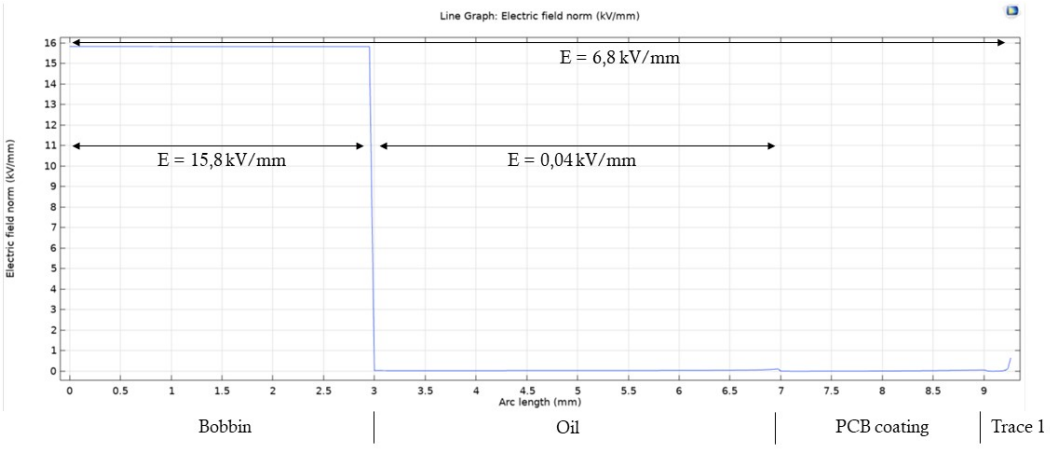


Figure 6.3: E-field with bobbin

From this plot, it can be seen that the bobbin takes away most of the stress from the oil, keeping it generously below the safety margin.

For the geometry in Figure 5.2b, the E-field is plotted across oil and PCB coating until the first trace on LV side, as in Figure 6.4. Here, the geometry of the bobbin is modified to have oil as the material for simulations.

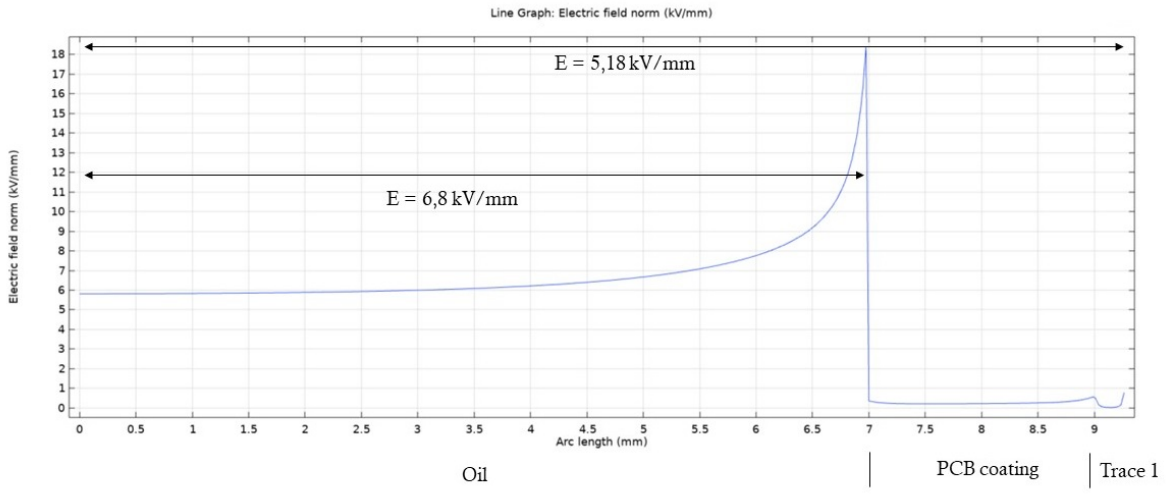


Figure 6.4: E-field without bobbin

From Figure 6.4, it is observed that without a bobbin the stress on the oil is almost at 7kV/mm which is the safety limit for the insulating oil. This is not desirable since it can lead to a breakdown. Hence, it can be concluded that the bobbin is necessary for insulation, mechanical support, and for reducing E-stresses across the oil.
Additionally, it can be observed that the average E-field across the geometry is higher when a bobbin is present. However, this is acceptable since the objective is to reduce the stress across the insulating oil.

6.2.2 Comparison of Bobbin Materials

From the previous section, it is established that a bobbin is necessary. The simulations compare the effect of the materials considered, on oil. The E-field is simulated across the bobbin, oil, PCB coating and the first trace, on the LV side of the PCB. Figures 6.5 and 6.6 present the effect of PP and PA 12 on the E-field, across bobbin and oil, respectively.
Comparing the results, the E-field stress is majorly on the bobbin and significantly less over the oil for the bobbin with PP material. For the PA 12 bobbin, the E-field over oil is much higher than the set limit. Hence, the PP bobbin is the clear choice.

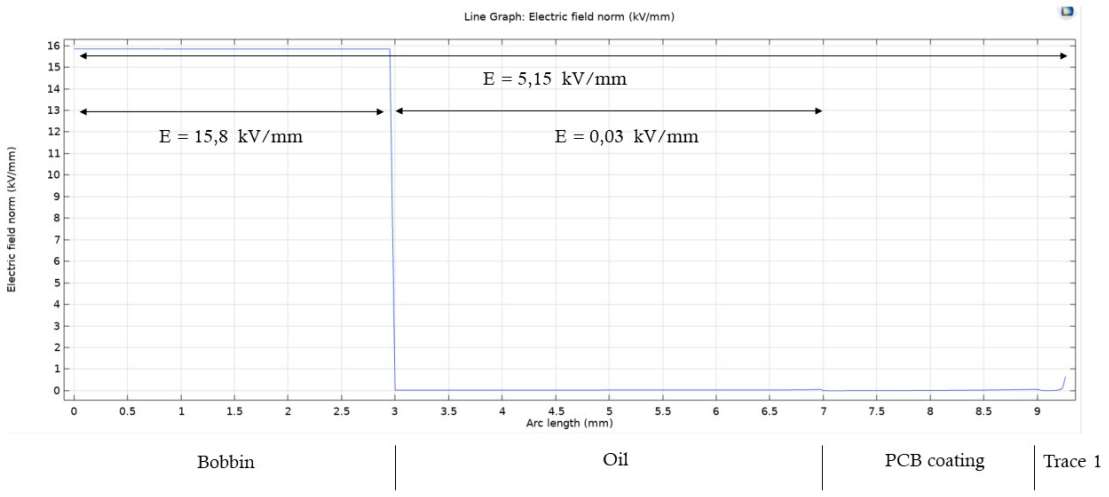


Figure 6.5: Bobbin material PP

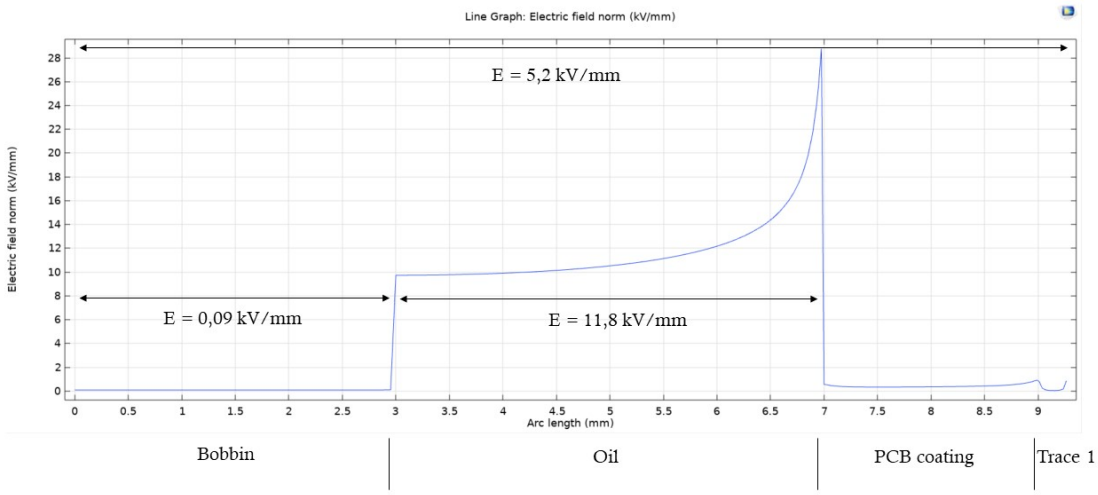


Figure 6.6: Bobbin material PA12

6.2.3 Requirement of PCB coating

The geometry described in Figures 5.3a and 5.3b, with and without PCB coating respectively, are simulated to verify the E-field stresses on the traces closest to the core on either side. This is because the E-field stresses are found to be highest at the edges of the trace. The triple junction formed by the different dielectrics and the edge effect cause such an effect [16].

For these geometries, the E-field is observed across the traces on the 50kV PCB. These are as shown in Figures 6.7 and 6.8.

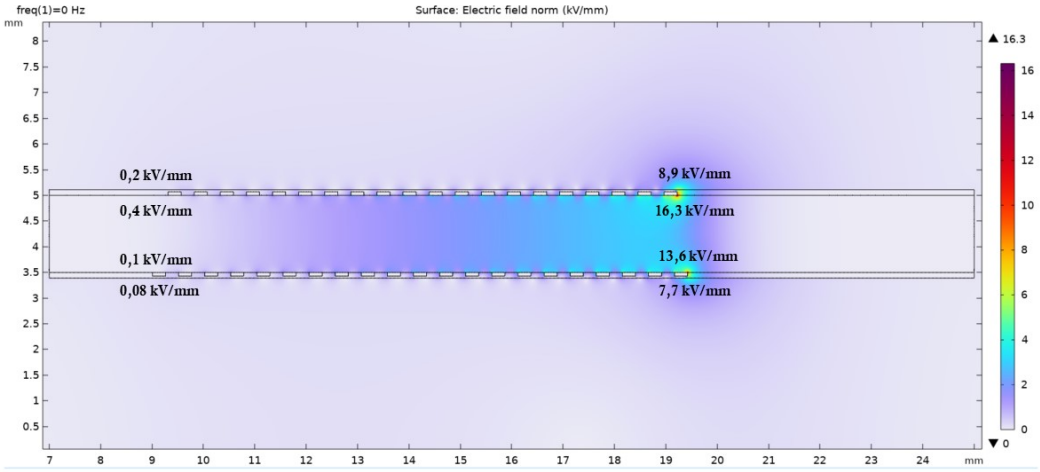


Figure 6.7: E-field surface plot with PCB coating

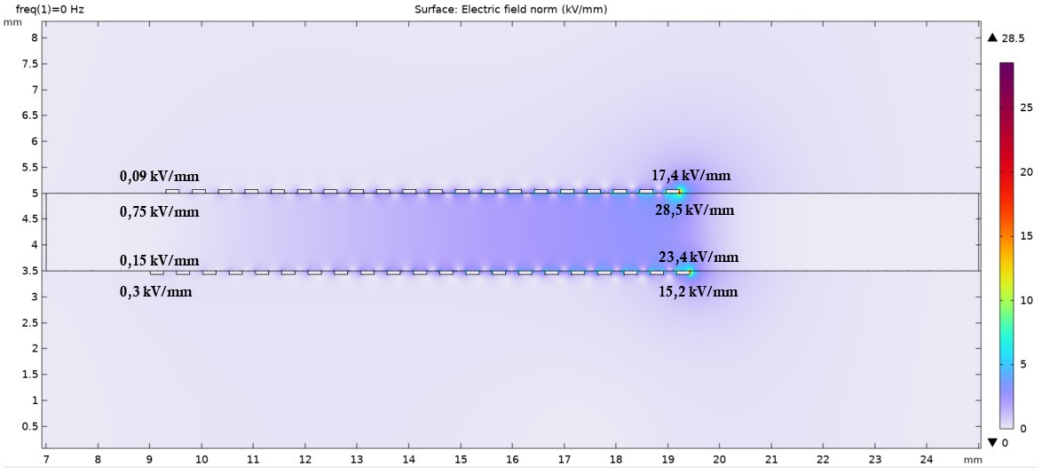


Figure 6.8: E-field surface plot without PCB coating

From the plots presented above, the inclusion of the coating is beneficial in reducing the E-stresses, especially on the HV (50 kV) trace. The coating reduces stresses on traces closest to the core and hence the average E-field stress across the geometry.

6.2.4 Insulation distances between core and PCB

As mentioned in Section 5.3.2, the distances between the PCB and the core on either side play an important role in minimising E-field stresses and in keeping the

distribution uniform.
The E-field distribution across the first PCB (the topmost in the stacks) as in Figure 5.7, including all traces on the HV side, is simulated. It is found to have an even distribution and an acceptable peak value on the HV trace, due to the inclusion of a PCB coating.

The E-field is plotted across the bobbin, oil, PCB, and traces, shown in Figure 6.9. Considering the average E-field distribution across oil and bobbin, the values support the insulation distances used in the geometry. These distances provide a good safety margin and hence the insulation design is acceptable.

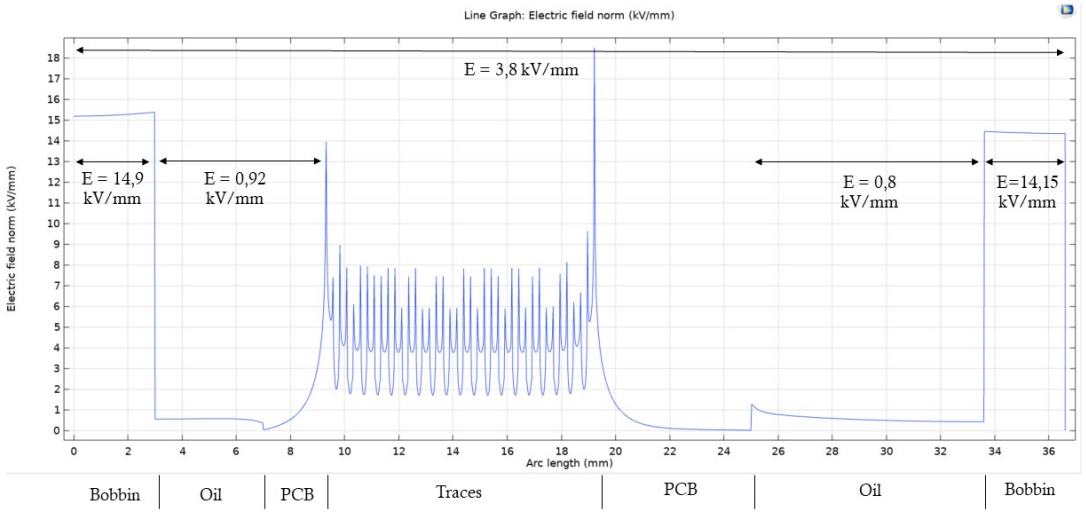


Figure 6.9: E-field with all traces on the top layer

From this plot, it is observed that the bobbin takes most of the E-field stresses, keeping the stress across the oil at a significantly safe level. This result also validates that the PCB should be placed closer to the middle leg of the core thereby increasing magnetic coupling and reducing stress on the HV side.

6.2.5 Arrangement of the PCB stacks

The complete geometry of the planar transformer, with 10 PCBs and primary winding, from Figure 5.7 is simulated with the Electric Currents interface and a Frequency Domain study.

The average E-field values are tabulated in Table 6.3, for PCBs 1, 5, 6 and 10 as per Figure 5.7.

Table 6.3: Average E-field in [kV/mm] across bobbin, oil, coating, and first trace

PCB	E-field (DC)
1	5,4
5	3,5
6	2,7
10	0,8

The E-field is plotted across the bobbin until the first trace on the LV side, through the oil and PCB coating. It is presented here in Figures 6.10 and 6.11 for the top and bottom PCBs.

The average E-field across each dielectric material is within a safe margin of its dielectric strength, 25-30kV/mm for the bobbin (PP) and 7kV/mm for oil. Taking conductivity of the materials into consideration, the E-stress is found to be focused on the bobbin instead of the oil. This is preferred from a safety perspective and to prevent breakdown across the oil. The E-field observed across each PCB successively reduces from the top PCB to the bottom PCB. This is as expected since the top PCB has the highest potential of 50 kV and it goes down to 0 kV at the bottom.

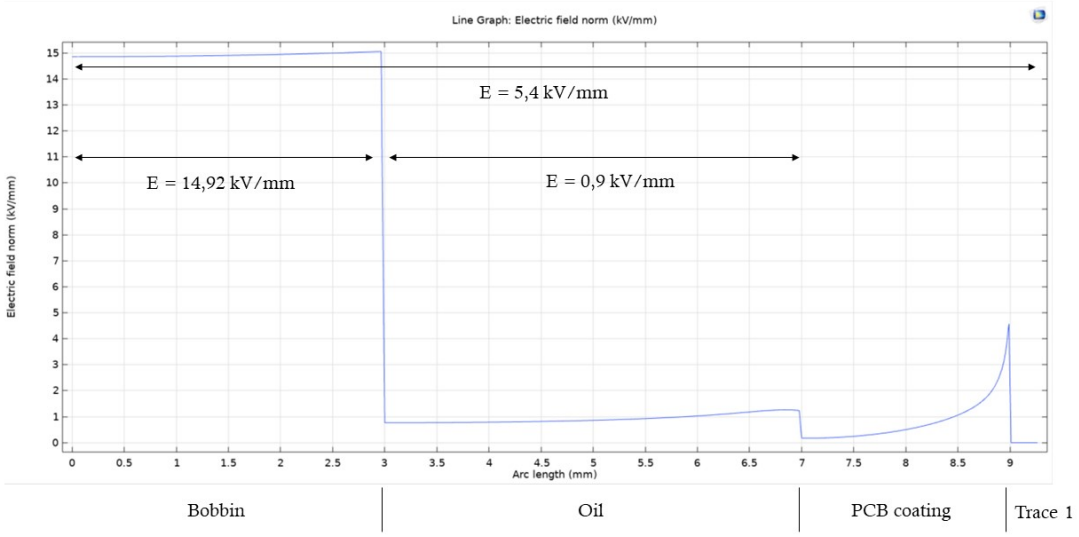


Figure 6.10: E-field line plot for the top PCB on LV side

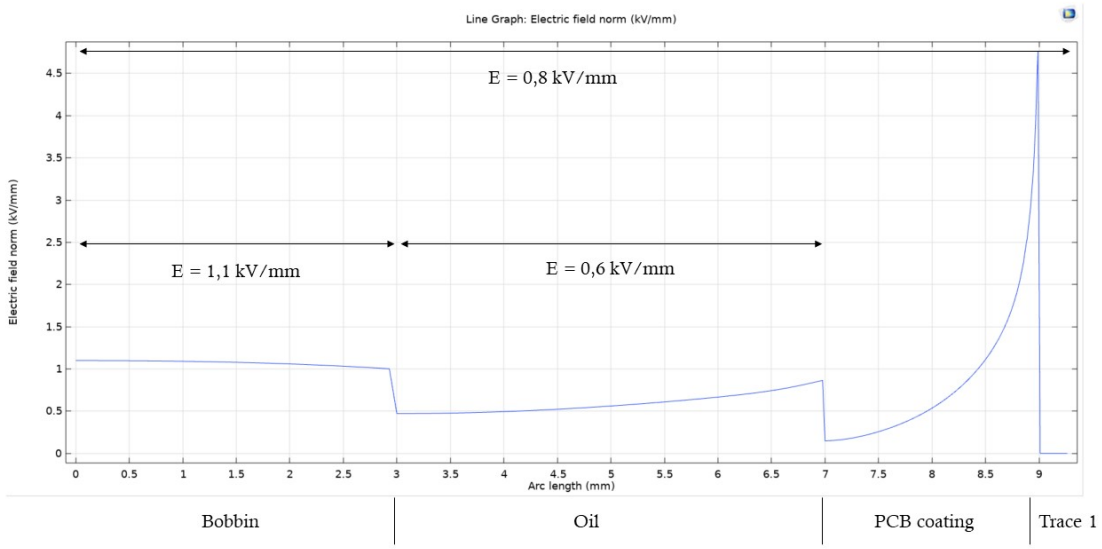


Figure 6.11: E-field line plot for the bottom PCB on LV side

The E-field distribution was observed for various sections of the geometry; across and along the bobbin, across the oil and across all the traces on a PCB - from middle to outer legs of the core, along PCBs and the Mylar sheets. These are tabulated below in Table 6.4 considering conductivity of the materials and the geometry in Figure 5.7. From these results, it can be seen that there are no unnecessary stresses on any material throughout the geometry and all the safety margins are maintained as per material properties. The placement of the PCB stacks within the core window, along with the dimensions chosen for every material, result in low stresses across the PCB with traces, oil, and Mylar while letting the bobbin take most of the stress. The distribution obtained from the COMSOL simulations also validate the insulation distances and materials chosen in the design.

Table 6.4: Results from the simulation of PCB stacks

Material	Section (of plot)	Position considered	E-field (kV/mm)
Bobbin	Across	Close to the primary	5
Bobbin	Along	Close to middle core	7,36
Bobbin	Along	Close to outer core	7,34
Oil	Across	Between PCB 1 and 2	0,93
Oil	Across	Between PCB 6 and 7	0,92
Traces	Across	PCB 1	3,8
Traces	Across	PCB 5	3,15
Traces	Across	PCB 6	2,45
Traces	Across	PCB 10	1,8
PCB	Along	PCB 1	3,2
PCB	Along	PCB 5	3,2
PCB	Along	PCB 6	3,2
PCB	Along	PCB 10	3,2
Mylar	Along	Below PCB 1	0,1
Mylar	Along	Below PCB 5	0,1
Mylar	Along	Below PCB 6	0,1
Mylar	Along	Below PCB 10	0,1

6.3 Total Loss and Efficiency

The various losses experienced across the transformer are -

- Core loss
- Primary winding loss
- Secondary winding loss
- Diode loss

The core loss has been measured directly from tests, while the remaining losses have been calculated from theory. They are presented in Table 6.5.

Table 6.5: Calculated transformer losses

Loss type	Value [W]
Core	60 [6.1.2]
Primary winding	67,5 [4.5.2]
Secondary winding	4,66 [5.2.4]
Diode	57,28 [5]
Total	189,44

The estimated efficiency, calculated using Equation (2.4), is 99,24%.

7
Conclusion

Several conclusions can be drawn from this thesis work;

- By replacing the secondary of a transformer with a planar design, the size is significantly reduced, along with the material used. The estimated efficiency is 99,24% and the cost is drastically reduced.
- At high frequencies, operating the transformer close to its magnetic saturation is not always effective, as it was found to cause rapid heating and high steady-state temperature, leading to high core loss.
- With results from the FEM-software COMSOL, it was found that using dielectric materials in High-Voltage systems, such as a plastic bobbin, coating over PCB, and dielectric grading across the insulating medium (oil), raised the dielectric strength and reduced E-field stresses.

7.1 Future work and Scope

- Testing individual PCBs in oil, by applying their maximum rated voltage and current at the rated frequency, to test for heating, and any discharges.
- Running the fully-assembled transformer in air, at a lower voltage rating.
- Testing the fully-assembled transformer in oil, at its maximum rated capacity.

There is also the possibility of expanding the transformer's design, to raise its generating capacity to 90kV, for larger ESP uses.

Bibliography

[1] Manisalidis I, Stavropoulou E, Stavropoulos A and Bezirtzoglou E, "Environmental and Health Impacts of Air Pollution: A Review," Front. Public Health 8:14, Feb 2020, doi: 10.3389/fpubh.2020.00014.

[2] K. R. Parker and Institution Of Electrical Engineers, "Electrical operation of electrostatic precipitators," London: Institution Of Electrical Engineers, 2003.

[3] Wang, Yan & Hu, Min & Xiao, Deng & Jiang, Yi. (2009). "Design of a cascade planar transformer for electrostatic precipitator use," WSEAS Transactions on Circuits and Systems. 8. 938-947.

[4] P. Ranstad and H. Nee, "On the Distribution of AC and DC Winding Capacitances in High-Frequency Power Transformers With Rectifier Loads," in IEEE Transactions on Industrial Electronics, vol. 58, no. 5, pp. 1789-1798, May 2011, doi: 10.1109/TIE.2010.2055773.

[5] United Nations, "The 17 sustainable development goals," United Nations, 2015. https://sdgs.un.org/goals

[6] IEEE, "IEEE Code of Ethics," ieee.org, 2020. https://www.ieee.org/about/corporate/governance/p7-8.html

[7] W. G. Hurley and Wolfle W. H., "Transformers and inductors for power electronics : theory, design and applications". Chichester: Wiley, November, 2014.

[8] T. Taufik, M. McCarthy, S. Watkins and M. Anwari, "Performance study of Series Loaded Resonant converter using super barrier rectifiers," TENCON 2009 - 2009 IEEE Region 10 Conference, 2009, pp. 1-5, doi: 10.1109/TENCON.2009.5395978.

[9] V. J. Thottuvelil, T. G. Wilson and H. A. Owen, "High-frequency measurement techniques for magnetic cores", in IEEE Transactions on Power Electronics, vol. 5, no. 1, pp. 41-53, Jan. 1990, doi: 10.1109/63.45998.

[10] "Litz Wire, HF-Litz, High Frequency Litz Wire, Litz Wire for High Efficiency | ELEKTRISOLA," www.elektrisola.com. https://www.elektrisola.com/en/Litz-Wire/Info [Accessed Jun. 17, 2022].

[11] "Ferrites and accessories - SIFERRIT material N87", https://www.tdk-electronics.tdk.com, 2018. [Online]. Available: https://www.tdk-electronics.tdk.com/download/528882/71e02c7b9384de1331b3f625ce4b2123/pdf-n87.pdf. [Accessed: March 10, 2022].

[12] COMSOL documentation, AC/DC module, boundary conditions of electromagnetism, https://doc.comsol.com/6.1/docserver/!/com.comsol.help.comsol/comsol refacdc.25.05.html!/com.comsol.help.acdc/acdc_ug_theory.05.02.html [Accessed Dec. 8, 2022].

[13] "PACK Litz wire, RUPALIT Profile Litz wires", https://www.packlitzwire.com. https://www.packlitzwire.com/products/litz-wires/rupalit-profile/ [Accessed Jun. 17, 2022].
[14] C. R. Sullivan and R. Y. Zhang, "Simplified design method for litz wire," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, 2014, pp. 2667-2674, doi: 10.1109/APEC.2014.6803681.
[15] Sullivan, C.R., "Optimal choice for number of strands in a litz-wire transformer winding", IEEE Transactions on Power Electronics, 1999, volume 14, number 2, pages 283-291 [Accessed Dec. 2, 2022].
[16] Kuchler A. "High voltage engineering fundamentals - technology - applications". Berlin Springer Vieweg, 2018.
[17] "Conformal Coatings Vs Encapsulation Resins - Which do I Choose?," Electrolube. https://electrolube.com/knowledgebase/conformal-coatings-versus-encapsulation-resins-making-an-informed-choice-for-electronic-protection/
[18] "Ultimeg 2000/380 impregnating varnish," BEVI. Available: https://www.bevi.com/@/File/Get/?id=1095download=0 [Accessed Jun. 17, 2022].
[19] "Fast Avalanche Sinterglass Diode", Vishay Semiconductors, 2018. [Online]. Available: https://www.vishay.com/docs/86034/byt77.pdf. [Accessed: May 19, 2022].
[20] R. Tarzwell and K. Bahl, "SIERRA Proto Express HIGH VOLTAGE PRINTED CIRCUIT DESIGN MANUFACTURING NOTEBOOK," 2004. Available: http://www.magazines007.com/pdf/High-Voltage-PCDesign.pdf [Accessed: Dec. 12, 2022].
[21] "Generic Standard on Printed Board Design", IPC-2221B, 2012
[22] "Printed Circuit Board Trace Width Tool | Advanced Circuits," www.4pcb.com. Available: https://www.4pcb.com/trace-width-calculator.html
[23] "PCB Trace Spacing Calculation for Voltage Levels", Smps.us. [Online]. Available: https://www.smps.us/pcbtracespacing.html. [Accessed: May 19, 2022].
[24] T. Johansson, "Passive Devices," in Radio Frequency Integrated Circuits (RFIC), 2018.
[25] "Dielectric Strength," Polymerdatabase.com, 2015. https://polymerdatabase.com/polymer%20physics/Dielectric%20Strength.html [Accessed: Dec. 2, 2022].
[26] "Mylar", BEVI. Available: https://www.bevi.com/@/File/Get/?id=934download=0 [Accessed: Dec. 12, 2022].
[27] "An Introduction to the Theory of Electrostatics" (2019), Multiphysics Cyclopedia, COMSOL. Available at: https://www.comsol.com/multiphysics/electrostatics-theory [Accessed: November 9, 2022].
[28] The Electric Currents Interface (no date), COMSOL. Available at: https://doc.comsol.com/5.5/doc/com.comsol.help.acdc/acdc_ug_electric_fields.07.043.html [Accessed: November 9, 2022].
[29] "An Introduction to Electroquasistatics Theory," www.comsol.com. https://www.comsol.com/multiphysics/electroquasistatics-theory [Accessed Nov. 11, 2022].

[30] "Calculation of conduction losses in a power rectifier", St.com, 2011. [Online]. Available: https://www.st.com/resource/en/application_note/cd00003894-calculation-of-conduction-losses-in-a-power-rectifier-stmicroelectronics.pdf. [Accessed: May 19, 2022].

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