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Electro-Thermal Modelling of an HVDC-Converter During Fault Conditions

Master of Science Thesis

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Abstract

This thesis investigates the electro-thermal stresses on the converter semiconductor components during surge currents events in a VSC HVDC-system using MMC topology. A typical HVDC-link is described and modelled in PSCAD simulation software and analytical calculations were performed alongside in order to confirm the simulated fault current peak values. Both the analytical calculations and simulations have shown that the most severe fault cases for the converter components are when faults occurs on DC-side of the converter, so called pole-to-pole and pole-to-ground faults. These fault currents are mainly conducted by the semiconductor diodes in the converter for which two different kinds of voltage drop models were derived - one extrapolated measurement based model and one physics based Lauritzen power diode model. The corresponding temperature response of the diode was simulated by a thermal model using Cauer electrical network representation. All models were created and combined in a Matlab/Simulink environment.

The Lauritzen model has proven to give satisfying results in the transient electro-thermal investigation for surge currents with lower peak values. However, during higher surge currents, the model starts to deviate from the measurement based model and estimate larger losses. The parameter extraction process for the Lauritzen model is time consuming for a new component and if the model parameters does not already exist, the benefits compared to the measurement based model are negligible. Similar to the Lauritzen model, the extrapolated model with the three different types of temperature coefficient starts also to deviate for higher surge currents. Better knowledge of the temperature dependent voltage drop combined with more detailed measurements in higher current and temperature range are needed in order to achieve more accurate simulations.

Keywords: HVDC, MMC, Fault Analysis, Surge Current, Electro-Thermal Modelling, Semiconductors

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Abbreviations

Abbreviations

A	Ampere
AC	Alternating Current
CSC	Current-Source Converter
CTL	Cascaded Two-Level
DC	Direct Current
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
KVL	Kirchhoff's Voltage Law
MMC	Multi-Modular Converter
PWM	Pulse Width Modulation
RMS	Root Mean Square
SSC	Short-Circuit Capacity
V	Voltage
VSC	Voltage-Source Converter

1 Introduction

The demand for electric power in urban areas around the world continues to increase, but the energy is often harvested far away from the consumption in order to use energy sources with less environmental impact. This has encouraged the development of power system solutions for large bulk power transmission. High Voltage Direct Current, HVDC, is a technology used for transmission of large amount of electric power over long distances with relatively low losses. From the beginning was the HVDC-technology based on line commutated converters, but the development of power semiconductors has enabled the use of self commutated converter technology which has encouraged the growth of renewable resources such as offshore wind farms [1].

The components inside an HVDC-station must have the capability of withstanding several kiloamperes, kA, and kilovolts, kV, during different operations and even higher during fault events in the system. To be able to design and build cost-efficient, reliable and compact solutions for the HVDC-stations, accurate simulation models are essential in order to design the station. However, often does these not include transient surge levels which can introduce uncertain margins during the design of the converter station which increases the cost of the projects.

1.1 Problem Description and Motivation of Work

The complexity of an HVDC-project is large and before the construction begin, several investigations must be performed to secure safe and beneficial operation reliability for all years the HVDC-system will be used. By analysing the power grids that are being connected with new transmission based on Direct Current, DC, can the most severe operation and fault cases be determined and used as design criteria for the converter station. These can be critical limits for electric, thermal and mechanical design of the converter components, transformer, cable or station facility.

When the most critical conditions are known, they are used to calculate the corresponding current levels and temperatures the components must be able to withstand. Most certainly these will be different for different locations, which makes it important to have proper tools during the design work. Therefore are different simulation tools used that represents the intended system and thereby reduce the testing before the final design is found. It is also a tool to predict the life-time and possible failure scenarios.

A commonly used tool for the design of power electronic converters are physical or behaviour base models of the semiconductor components. These can have various levels of detail, each suitable for different applications.

Some can be accurate during steady-state operations but can not cover more dynamic behaviours. On the other hand are these rather easy and less time consuming to implement in comparison with more detailed, dynamic models [2].

During a surge-current event in a half-bridge rectifier configuration, one of the anti-parallel diodes is exposed to high transient currents. During this time period before the fault is cleared, the exposed diode absorbs energy and could potentially reach dangerous temperatures which shortens the components life-time or in the worst case lead to a breakdown.

One commonly used physical model of semiconductor switching devices is the Lauritzen model which is normally used for design and simulation of switching circuits. However, this model does not include all physical phenomena and uncertainties will occur for higher injection levels [2].

1.2 Purpose

The purpose of this thesis is to investigate different fault scenarios occurring in a Cascaded Two-level voltage source converter based HVDC-system. The faults resulting in the highest current through the converter will be investigated further and how these affects the performance of the power semiconductors inside the converter.

The semiconductors will be modelled with a commonly used physics based Lauritzen device model and compared with extrapolated measurement model data in order to investigate the performance of these during surge current events. The thermal stress on these components will also be investigated to give an indication of any possible damage as a result of a surge.

1.3 Scope

This thesis will not cover the control system functions of an HVDC-station using simulations. During a fault scenario the control unit will instantly go into blocking mode, thus the surge currents will in most cases go through the diodes. However, to be able to run realistic operation simulations, an existing model of a full scale HVDC-control unit from the system department at ABB HVDC will be used. This control system is also used to provide system steady-state values before any fault is applied. The switching components are considered ideal during surge events in the converter. To simplify the analytical calculations, the case system will only transfer active power and no reactive power.

The implementation of the thermal model will only consider heat transfer through conduction, both convection and radiation are neglected to reduce the complexity.

The thesis is limited to theoretical work only and new measurements was

not possible due to practical reasons. Therefore, datasheet information was used.

1.4 Method

The thesis was conducted in several iteratively steps for each part of the investigations. In the beginning, the HVDC-technology and its components were studied to be able to perform a fault analysis on the case system. To determine which fault cases is the most severe for the converter in an HVDC-station, analytical calculations based on basic electrical circuit theory was performed. In order to verify the the calculated results, a computer simulation software from Manitoba HVDC Research Center named PSCAD was used.

In the PSCAD simulations, the standard library components were used, except the converter representation and the control system configuration, which were received from ABB HVDC in Ludvika. The control system model is used to generate the steady-state simulation of the system and will not be of any concern during fault simulations. In parallel with these system studies for different fault scenarios were analytical fault analysis calculations performed in order to compare and verify the simulation results. These results from the fault analysis investigation were later used as input to the semiconductor evaluation including both a device and a thermal model.

In order to analyse how the determined surge currents affect the semiconductor components, two models were created. The first model was a physic based Lauritzen model, which initially was extracted from parameters given in the datasheet. These model parameters together with the Lauritzen representation were implemented in a Simscape block integrated in Matlab/Simulink. The model response of and reverse recovery and forward characteristics were later used in order to understand how the model parameters affected the performance of the model and these were iteratively improved to fit to datasheet measurements. The other semiconductor device model is based on measurements, however, this was not fully complete for high current and temperature levels and therefore extended with the help of extrapolation. Due to uncertainties about the thermal behaviours of the forward characteristics, three different cases were investigated and evaluated to determine the worst characteristics of the case device.

To be able to simulate how the surge currents from different fault cases within the HVDC-system affect the converter components in terms of temperature, a thermal model of the device was created. This enables an investigation of how the temperature development from these surges affect the lifetime and reliability of the components as well as an evaluation of the semiconductor models created. The thermal model, based on thermal impedance response measurements in the datasheet, were created and im-

plemented in Matlab/Simulink. The model was iteratively improved, mainly in order to increase the convergence of the simulations.

To be able to simulate the whole chain, from surge current to resulting virtual junction temperature, both semiconductor models and the thermal model were combined in one iterative loop. This was also implemented in Matlab/Simulink software and the most severe surge current waveforms through the converter components determined in the fault analysis were used as input together with the virtual junction temperature before the fault occur, visualized in Figure 1. Both semiconductor models were implemented and tested in this simulation tool, including the 3 different temperature characteristics of the extrapolated model. In this way, the different semiconductor models can be evaluated, in order to determine which one that gives the most reasonable losses in comparison to the device specifications and what is the resulting stress on the components.

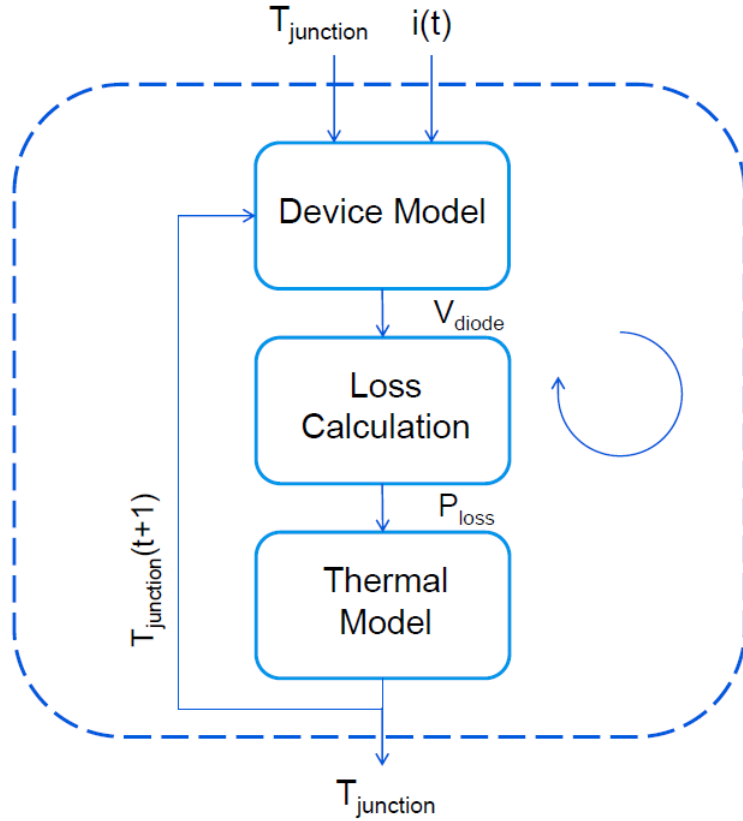


Figure 1: Schematic view over the simulations program with both semiconductor and thermal model implemented in an iterative loop in order to calculate the device temperature during the surge.

2 HVDC-system and Components

High Voltage Direct Current, HVDC, is a technique for transporting energy. Using semiconductor components, an Alternating Current, AC, is rectified and being transported as a Direct Current, DC, before being converted back to AC-power again. This transformation leads to benefits and are interesting for example in long-distance power transfer and the interconnection between two grid areas with different frequencies.

The HVDC-technique was pioneered by ABB in the early 1950s and has since then evolved and now consist of different types of converter topologies and switching components. The first HVDC-converter stations were based on Current-Source Converters, CSC, using line-commutated mercury-arc valves and was later replaced with silicon-based thyristors [1]. The other common technology for HVDC is based on Voltage-Source Converters, VSC, which utilize self-commutated devices, usually Insulated Gate Bipolar Transistors, IGBT, and can therefore, in comparison to the thyristor-based converters, be controlled at which point to be switched-off [3].

The HVDC-technology can be used in different roles. It can be used to transfer energy over an distance from place A to B or to connect regions either because of frequency differences or for stability reasons. When making decisions to use HVDC-technology or conventional AC-based technology, factors as economy, space usage and reliability has to be taken into consideration [3].

2.1 Advantages with HVDC

The specific requirements and specifications of each project has to be considered when determining the advantages of utilizing the HVDC-technology instead of AC-transmission technology. Investment and maintenance costs have to be compared with the calculated cost of the power losses in the whole system. Technical factors can sometimes make the HVDC-technology the only viable options due to technical restrictions of AC-transmission systems in terms of transmission distance.

When using DC-power for transmission of electrical energy trough cables or overhead lines the effective resistance is lower in comparison with an AC-system. This reduces losses and the required cable area for the same amount of transferable power. This is partly due to the absence of skin effect and a reactive power component that also has to be transmitted in the conductor [1].

The absence of an reactive power component enables the transmission distance to increase without using any intermediate reactive compensating apparatus to maintain the voltage of the system. Combined with the fact that

an HVDC-system only requires two conductors, and sometimes only one when a sea or ground return is used, makes it interesting and sometimes the only viable options for the connection of islands and offshore platforms [3].

Transmission tower design becomes simpler and space usage of overhead transmission lines is less than for an AC-system due to fewer required conductors. Magnetic and electrical fields being emitted from transmission cables and equipment are DC-fields and are less worrying compared to an AC-system. By placing both the conductor and the return cable close to each other, the emitted magnetic field is reduced due to field cancellation as both conductors are carrying the same current in opposite directions [1].

The HVDC-technique also acts as a stabilizer for the rest of the AC-power system and can be used to quickly control the amount of active and reactive power being transferred.

2.2 Converter Topologies

Two types of switching topologies are mainly used today: CSC and VSC. The CSC are utilizing self-commutated components like thyristors and are current-stiff in that sense that the current does not change direction in the converter when the power is reversed. In the other topology VSC, the DC-link voltage is kept stiff and is using forced-commutated components for example IGBT, to control the direction of the current [1].

The VSC based HVDC-station does not require any synchronous machines in their connected AC-network to contribute with reactive power during the commutation phase. Thus, the VSC HVDC-stations are able to perform a black-start where the rotating machines have lost their power and are at a standstill [1].

The first generation of VSC HVDC-stations were based on a two-level converter topology. The full DC-link voltage was switched between positive respectively negative half of the DC-link voltage in a Pulse Width Modulation, PWM, pattern to be able to produce a sinusoidal AC-waveform, as can be seen in Figure 2. By only using two voltage levels, the output AC-waveform contained harmonics which required large smoothing capacitors to produce an acceptable output [1].

In order for the HVDC-station based on the two-level converter to operate with high voltages, several IGBTs for each switching position had to be connected in series which required gate-control units with simultaneous firing capabilities. If the upper and lower position in the two-level converter fired simultaneously, the DC-link capacitors would be short-circuited and the stored power would be unloaded through the IGBTs with potential of destruction as a consequence. A typical three-phase, two-level converter is shown in Figure 3.

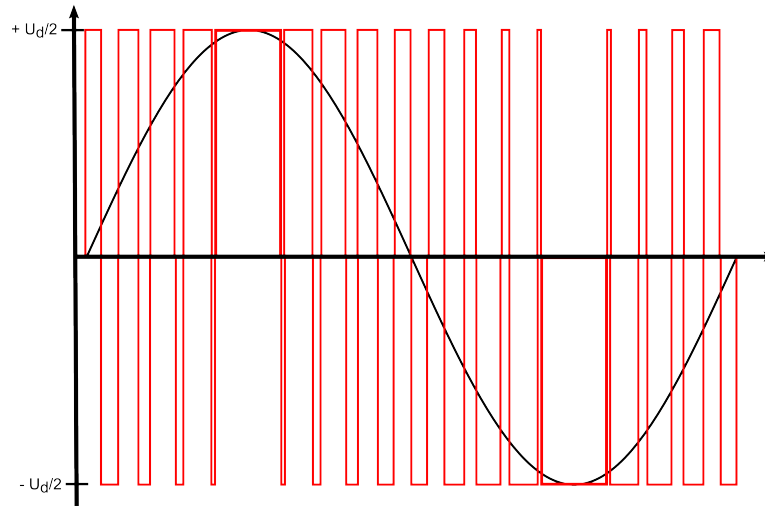


Figure 2: Simplified PWM-switching pattern for a two-level converter operating in inverter mode.

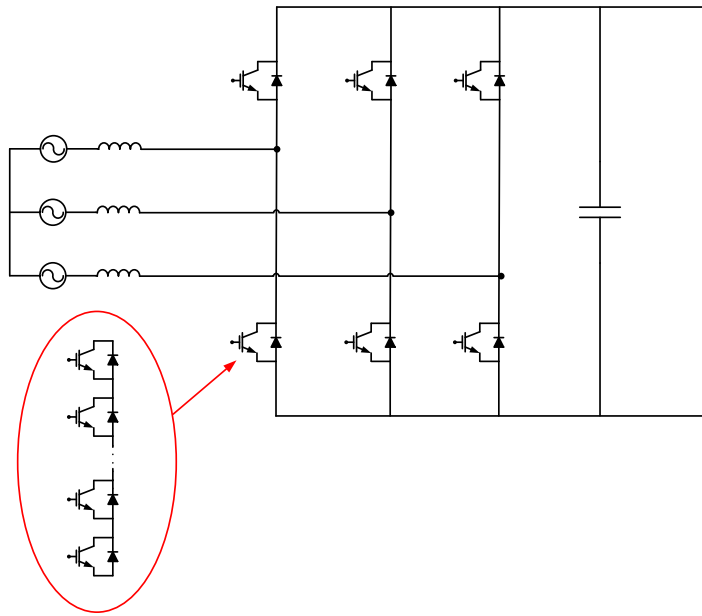


Figure 3: Simplified circuit layout of a three-phase, two-level converter with multiple IGBTs in series per switching position

Connecting several two-level converters in series results in a topology called Modular Multi-Level Converter, MMC. Each separate two-level converter contains an own DC-link capacitor and are called a cell. When several series connected IGBTs in each switching position in the cell is used, it is called

Cascaded Two-Level, CTL, converter. This topology is used by ABB in its latest generation of HVDC Light [1].

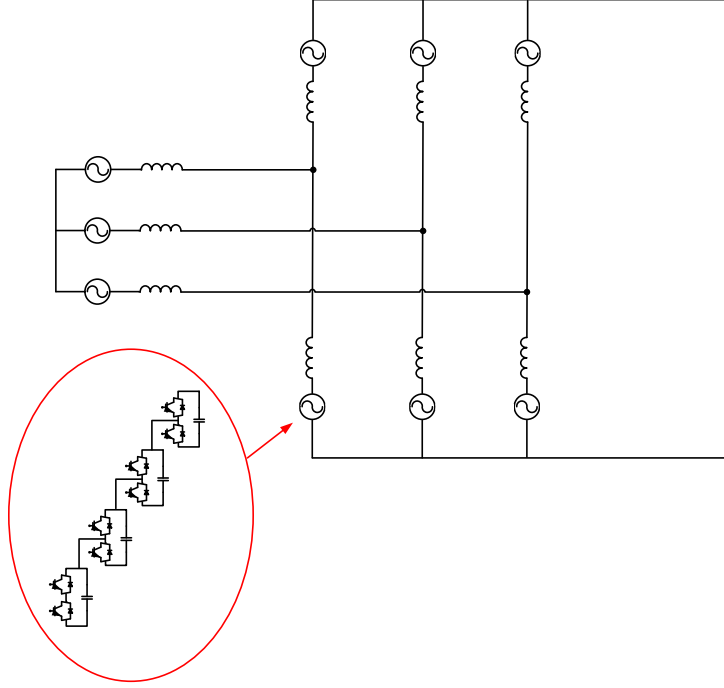


Figure 4: Simplified circuit layout of an three-phase, Cascaded Two-level converter. In this example, each phase contains $4 + 4 = 8$ cells and are therefore capable of switching with 8 different voltage levels.

Each cell can operate individual and by controlling the switches depending of the current flow, the DC-link capacitor in each cell can either be charged, discharged or to keep its voltage constant, be bypassed. Utilizing these individual cells in a CTL-topology, the voltage steps in the output waveform is corresponding to the cell capacitor voltage in each cell and is much smaller than for an ordinary two-level converter. This reduces the total harmonics in the output waveform, minimizing the need for filters as can be seen in Figure 5. Also, the cascade formation allows for each cell to be switched at a lower frequency compared to the fundamental switching frequency, which minimize the switching losses [1]. The effective switching frequency for the whole converter becomes higher and therefore allows a reduction in the size of the filters [4].

2.3 System Layout

A HVDC-station consist of many different components that can vary with the demands and specifications regarding for example output harmonics tol-

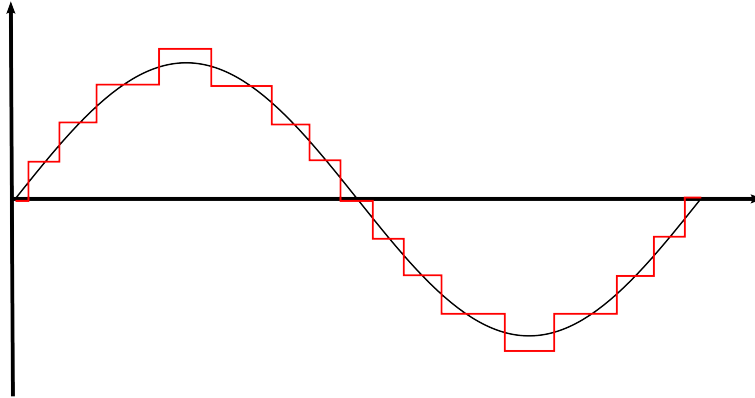


Figure 5: Simplified output voltage waveform of a Cascaded Two-level converter.

erance and operation redundancy. In this chapter a basic station layout for an HVDC Light station from ABB will be presented.

The HVDC-station can be divided into four different main sections: AC-yard, reactors, valves and DC-yard. A simplified circuit layout diagram of an typical HVDC-station is presented in Figure 6.

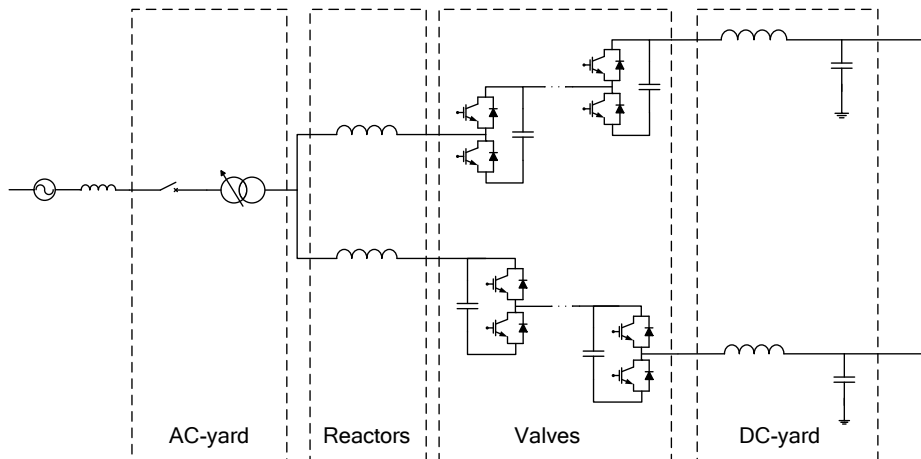


Figure 6: Simplified single line diagram of an typical HVDC-station with the four main areas marked.

The AC-yard contains the power transformer that either can consist of three single-phase transformers or a single three-phase transformer depending on the power rating of the station or logistical aspects. In order to be able to change the ratio of the transformed voltage, a tap changer is installed. On the high voltage side of the power transformer, AC-breakers is located to be

able to handle and clear fault conditions.

The reactor section consists of the converter reactors. These reactors can supply or consume active and reactive power depending on the operating condition and therefore acts as a regulator. The amount of active and reactive power are a function of the voltage difference over the reactor

$$P = \frac{U_c U_v \sin(\delta)}{\omega L} \quad (1)$$

$$Q = \frac{U_c(U_c - U_v) \cos(\delta)}{\omega L} \quad (2)$$

where δ is the phase angle difference over the reactor and L is the inductance value. By controlling the output converter valve voltage U_v and by using the tap changer of the power transformer to adjust the voltage U_c , the active and reactive power can be adjusted according to (1) and (2). The valid operation ratio between active and reactive effect for a typical HVDC-station is presented in Figure 7 [1].

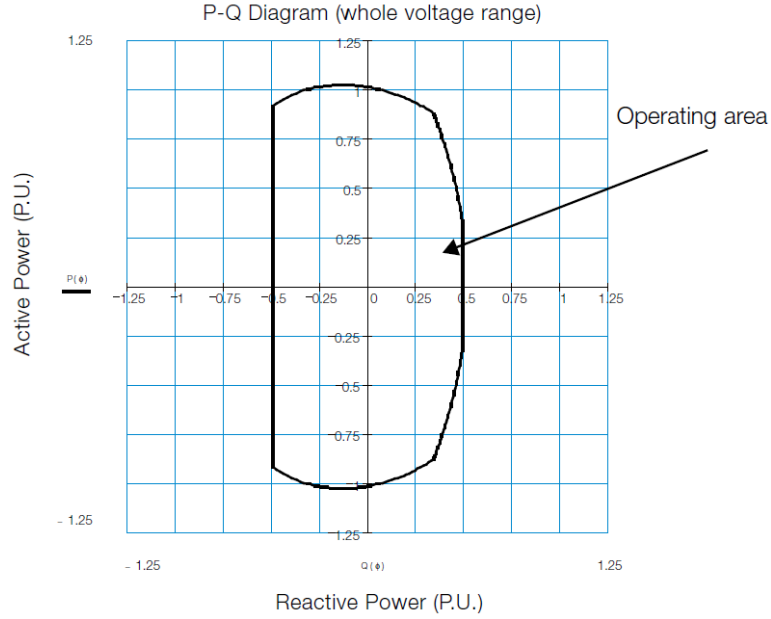


Figure 7: Simplified PQ-diagram over the possible operation area of a typical HVDC-station [1].

The valve section consists of three valve phase legs, one for each AC-phase. Each valve phase leg is made up of two valve arms, where one valve arm is connected between AC and the positive DC-node and the other valve arm is

connected in the same way but instead connected to the negative DC-node. Each valve arm consists of different numbers of cascaded two-level converter cells depending on the desired voltage rating and redundancy requirements. A simplified layout of the valve section can be seen in Figure 8. In order to prevent contamination and reduce the risk of failure, both the reactor and valve hall are usually built in a controlled environment [1].

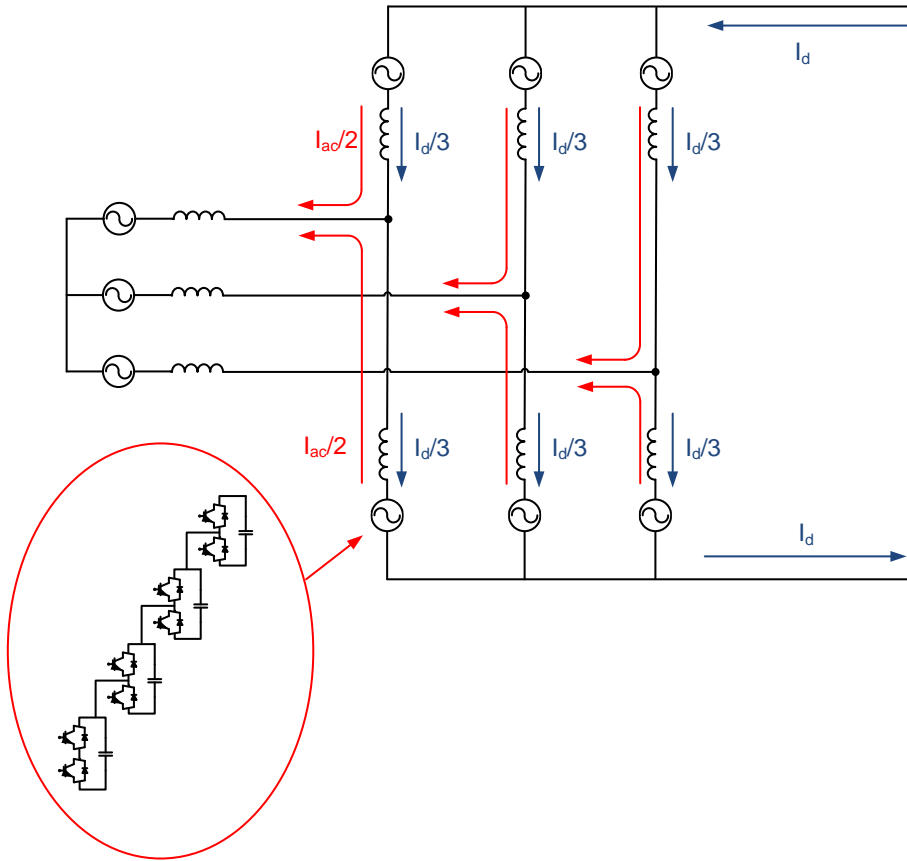


Figure 8: Simplified circuit diagram of the currents in a three-phase MMC-based converter

Using electrical node analysis techniques and neglecting the circulating second harmonic AC-current component, the current flowing in each valve arm can be described

$$I_{arm} = \frac{I_{DC}}{3} + \frac{I_{AC}}{2} \quad (3)$$

where the DC-current I_{DC} can be calculated from

$$I_{DC} = \frac{S_{transferred}}{U_{DC}} \quad (4)$$

where $S_{transferred}$ is the amount of transferred apparent power of the station at the given moment and U_{DC} is the potential difference of the two DC-nodes. The AC-current in one phase can also be expressed by using the total amount of transferred power for the station

$$I_{AC} = \frac{S_{transferred}/3}{U_{AC}/\sqrt{3}} \quad (5)$$

where U_{AC} is the line-to-line voltage.

The DC-yard mainly consists of filters in order to suppress harmonics from the converter. The amount of filters needed is dependent on the requirement from the grid owner. If the chosen transfer method is by cable instead of overhead lines, the inherent suppression in the DC-cable is enough and therefore no additional DC-filters are in general cases needed. High-frequency ripple from the converter switching can in some case be needed to be filtered [1].

Different configurations of how to interconnect HVDC-stations exists. Three main types exists and are called monopole, bipole and multi-terminal type of operating configuration. The monopole configuration consists of two converters, the bipole of four converters and a multi-terminal that consists of a different number of HVDC-converters. The monopole configuration consists of one converter at each transfer site, which means limited redundancy. If two fully insulated cables are used for the energy transfer, the configuration is called a symmetric monopole and are illustrated in Figure 9. To reduced cost, one of the cables can be replaced with either a metallic return DC-conductor without full insulation or using a ground return that utilizes the ground or water as a return conductor. These alternatives are called asymmetric monopoles and are normally not build for environmental aspects [1].

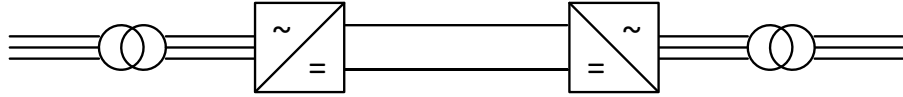


Figure 9: Simplified circuit diagram of a symmetric monopole configuration of a HVDC-transmission system. The two cables are fully insulated for the required operating voltage.

The bipole configuration consists of two HVDC-converters on each transfer site, thus achieving a redundancy for 50 percent of the total rating but are more costly than a monopole configuration. Bipolar configuration can in the same way as the monopolar, also utilize either a metallic return or a ground return alternative. The multi-terminal configuration is several HVDC-converters connected in a grid consisting of various configuration [1].

2.4 Fault Analysis Theory

Analytical determination of surge currents during a system fault case demands calculation models. These calculation models are a trade off between accuracy and simplicity, for example if the results will be used for further calculation accuracy is preferred, or if the results will be used for validation of simulations results, some degree of simplicity is acceptable. The HVDC-station is a dynamic system, where the control system responds differently to different fault cases. One of the features is if a fault occurs in one of the connected AC-systems, the HVDC-systems will try to prevent the fault to propagate into the other AC-system and try to keep it unaffected. This is mainly done by continue switching the converts in order to keep the AC-side currents in the non-faulty AC-system balanced during the fault [5].

2.4.1 AC-Faults

Depending on how the fault has occurred, the fault types in a three-phase system can be divide into different subgroups. When an asymmetrical fault has occurred, one or two of the phases have been affected. It can either be a single-phase-to-ground fault or a phase-to-phase fault. When calculating these types of fault, three different types of currents have to be analysed: positive sequence, negative sequence and zero sequence current [6].

The other type of faults is the symmetrical fault type, and is characterized by that all three phases are affected at the same time. One example is the three-phase-to-ground fault. When analysis these types of fault, only the positive sequence current has to be analysed. In general, when a fault occur far away from the generation, three-phase fault generates the largest fault currents [6].

To represent the characteristic or the strength of the electrical power grid, the term Short-Circuit Capacity, SCC, is used. This is the maximal power that a grid can provide during a fault case, and can be described as

$$SCC = \frac{S_B}{X_{th}} \quad (6)$$

where S_B is the three-phase base power of the source of the grid expressed in MVA and X_{th} is the short circuit reactance of the lines and equipment

between the source and the fault location. The unit of SCC in (6) is MVA. A strong grid has a high SCC , which indicates a smaller X_{th} which means that the voltage during a fault is theoretically kept close to the operating voltage, except for zero impedance faults [7].

When a short-circuit occurs in a network that is represented by the complex impedance

$$Z_{network} = R + jwL \quad (7)$$

and is connected to an AC-generator, the corresponding short circuit current is described as

$$i_{SC}(t) = I_m \sin(wt + \theta - \phi) - I_m \sin(\theta - \phi) \exp\left(\frac{-Rt}{L}\right) \quad (8)$$

where θ is the angle of the voltage wave when the fault is occurring, I_m is the maximum steady-state current and ϕ is the angle

$$\phi = \frac{\arctan(wL)}{R} \quad (9)$$

and can also be described as the ratio between reactance and resistance in the network, X/R . High-voltage network often has a high ratio of X/R , thus having a large angle ϕ , close to 90° . If a fault occurs in a high voltage network, when the voltage angle $\theta = 0$ and at the time instant $t = 0$, according to (8) the instantaneous value of the short circuit current $i_{SC}(0)$ then becomes equal to $2I_m$. This effect is called the doubling effect. With increasing time, the amplitude will decay with the exponential term in (8) [8][7].

2.4.2 Transmission Cable

A transmission cable can be represented by its impedance, capacitance and inductance. For transmission lines in the range of 80 to 240 km, the shunt capacitance is either modelled as a T-circuit or as a Pi-circuit. The T-circuit models the whole capacitance of the line as a single capacitor in the midpoint, and the Pi-circuit divides the capacitance equally between the sending and receiving end [8], as can be seen in Figure 10.

When a fault occurs somewhere along the transmission line or in its connected HVDC-stations, the stored energy in the modelled DC-cable is discharged in a oscillatory behaviour. The equivalent discharge circuit can be seen as a second-order series RLC-resonance circuit, see Figure 11 [9]. Using

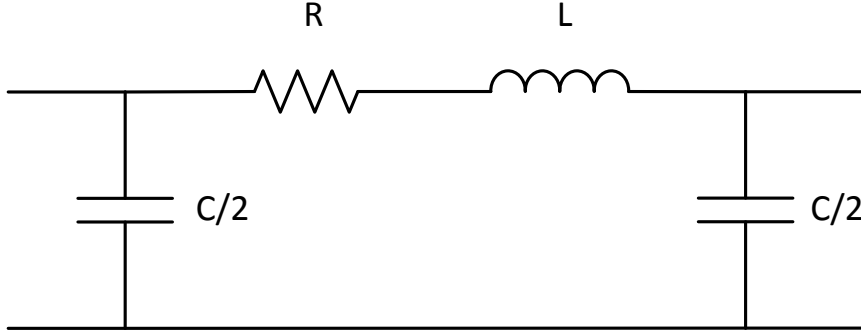


Figure 10: Simplified circuit diagram of a transmission cable modelled as a Pi-circuit.

Kirchhoff's Voltage Law, KVL, the circuit equation becomes after differentiation and division with L

$$\frac{1}{L} \frac{dv_s}{dt} = \frac{d^2 i}{dt^2} + \frac{R}{L} \frac{di}{dt} + \frac{1}{LC} i \quad (10)$$

which is a second-order differential equation. Assuming a natural response, in other words without a voltage source $V_s = 0$ and $i_s = 0$, (10) can be expressed as

$$0 = \frac{d^2 y(t)}{dt^2} + 2\zeta\omega_0 \frac{dy(t)}{dt} + \omega_0^2 y(t) \quad (11)$$

where ω_0 is the undamped natural frequency expressed in rad/s and ζ is the dimensionless damping ratio. The two parameters are defined as following

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (12)$$

$$\zeta = 0.5 R \sqrt{\frac{C}{L}}. \quad (13)$$

If $0 < \zeta < 1$, the resonance circuit has a underdamped response [9]. The general solution to the differential equation (11) becomes

$$y(t) = A \exp(-\alpha t) \cos(\omega_d t + \theta) \quad (14)$$

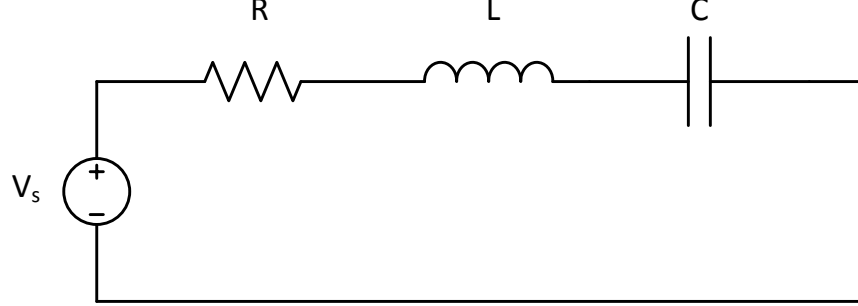


Figure 11: Discharge circuit modelled as a second-order series RLC-resonance circuit.

where A and θ is the initial condition-constants. The parameter α is defined as

$$\alpha = \zeta\omega_0 \quad (15)$$

and ω_d is called the damped frequency and is expressed

$$\omega_d = \omega_0\sqrt{1 - \zeta^2}. \quad (16)$$

The instant of the fault occurring in the system, the equivalent resonance circuit inductor current is $i_L(0^+) = 0$ and the DC-cable capacitance voltage is $v_C(0^+) = V_{DC}$. Using KVL and the inductance law, the initial condition in (14) should fulfil

$$i(0^+) = 0 \quad (17)$$

$$\frac{di(0^+)}{dt} = -\frac{V_{DC}}{L}. \quad (18)$$

Using the initial conditions stated in (17) and (18) to find the initial conditions-constants in (14), yields the following solution for the current [9],

$$i(t) = \frac{V_{DC}}{\omega_d L} \exp(-\alpha t) \sin(\omega_d t). \quad (19)$$

2.4.3 DC-Faults

In the event of an pole-to-pole fault, when the DC-side of the converter is short circuited, the converter acts like a six-pulse diode rectifier bridge due to the MMC-cell capacitors is considered to not contributing to the short circuit current during the fault event [10]. The corresponding short-circuit current can be calculated as

$$I_{SC,pole-pole} = \kappa \frac{3 \sqrt{2} U_{AC,ph}}{\pi Z_{AC}} \quad (20)$$

where $U_{AC,ph}$ is the Root Mean Square, RMS, phase voltage on the AC-side of the converter and Z_{AC} is the total impedance, with half the impedance value for the arm reactors, between the AC-source and the converter. The parameter κ is an approximation of the transient peak current, expressed as

$$\kappa = 1 + 1.04 \exp \left(-2.45 \frac{R_{AC}}{X_{AC}} \right) \quad (21)$$

where R_{AC} is the resistance and X_{AC} is the inductive reactance on the AC-side of the converter. To be noticed about these formulas is that they are not ideal for MMC-converter calculations and deviation may occur in comparison with simulations or measurements. However, it is a appropriate approximation. The deviation is due to the additional arm reactance, which result in a larger commutation angle and a corresponding reduction of the current peak [10].

3 Component and Modelling Theory

This chapter provides a theoretical background on semiconductor devices and different modelling approaches used for simulation of their characteristics. Both electrical and thermal aspects will be introduced and described in order to build up different simulation based representation.

3.1 Semiconductors

A semiconducting material is a material that has both insulating and conducting properties. Materials with high concentration of free charge carriers is called conductors. These carriers will start to move if an electric field is applied and a resulting electrical current is conducted. The number of charge carriers can be in the order of 10^{23} cm^{-3} for a conductor, in comparison with 10^3 cm^{-3} for an insulating material which has poor conducting properties. Semiconductors on the other hand, usually have a free-electron density in the range of $10^8 - 10^{19} \text{ cm}^{-3}$. The carrier concentration within a semiconductor is rather easy to manipulate by introducing impurities or apply an electric field on adapted structures. This is a unique property which makes it superior for electrical implementations [11].

Semiconductors can be doped with different materials that usually have one valance electron more or less compared with the semiconducting material. Silicon is a semiconductor material widely used in electronic application and the material has four valence electrons. If it is doped with a material with three valence electrons, the holes become the majority carrier. This is usually refereed to as *p*-type silicon with an impurity of acceptors. When silicon is doped with a material with five valences electrons, the electrons will become the majority carriers and holes minority carriers, and is then called *n*-type silicon [11].

When a silicon crystal has both a *p* and *n*-type region, a *pn*-junction is formed with a metallurgical junction in between them. This junction can be abrupt or graded in order to get different characteristics. The different concentration of majority carriers on each side will diffuse into the other side and become minority carriers. This creates ionized impurities which is not as mobile as the free carriers and therefore creates a space charge density. With a potential difference between the *p* and *n*-side, an electric field created over this region which is normally referred to as the depletion layer, see Figure 12 [11].

In order to conduct a current through the junction, a potential must be applied over the silicon crystal in order to overcome the potential difference between the *p* and *n*-side of the depletion layer [11].

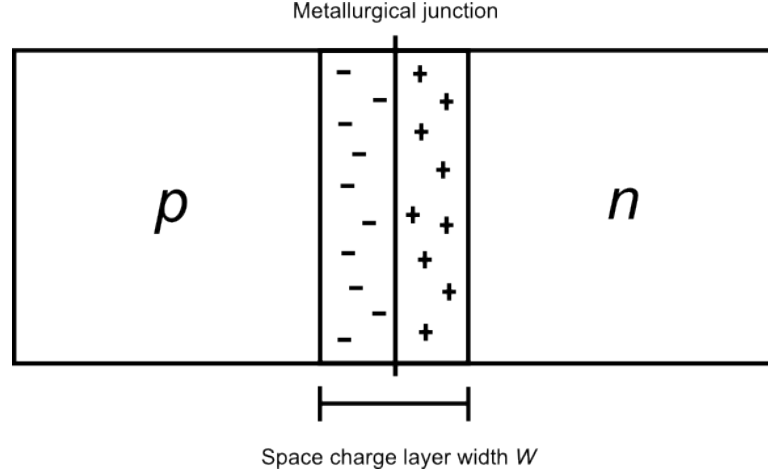
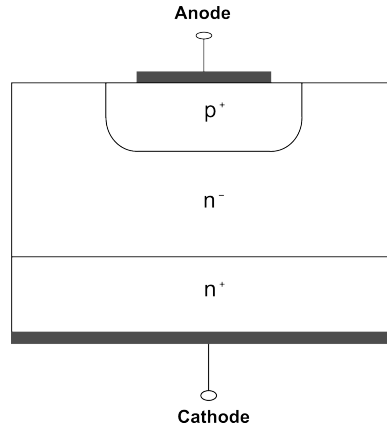


Figure 12: Positive and negative space charges within the pn -junction forms a depletion layer around the metallurgical junction [11].

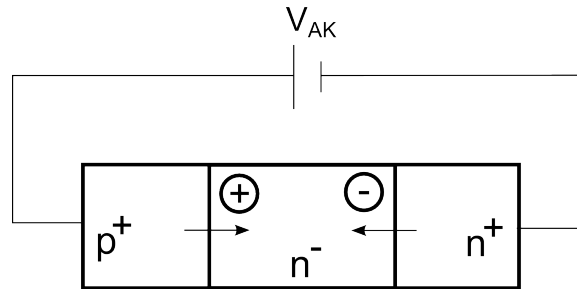
3.2 Power Diode

The power diode is a semiconductor device that is designed and manufactured to withstand conduction up to several kA during its on state and block up to several kV when reverse biased. To achieve this, the depletion layer must be wide enough in order to keep the electric field strength under the critical limit and prevent electrical breakdown. By having a low space charge density inside the depletion layer which enables a wide depletion layer for the maximum electrical field strength allowed. These design criteria can be fulfilled with a wide, lightly doped pn -diode. But the disadvantage would be high resistance during on-state which results in undesirable losses at nominal current. The resistivity can be reduced by increasing the doping level, but this will on the other hand reduce the breakdown strength. An other solution to this design problem is to divide the N-region of the pn -junction into to areas, one heavily n^+ -doped region and one lightly n^- -doped region placed between the usual p^+ - and n^+ -region. The n^- -doped region can also be referred to as the drift region and will absorb the depletion layer during reverse bias and increases the breakdown strength. This structure is called a PiN -structure and is displayed in Figure 13 [11].

When a positive voltage is applied over the power diode, the p^+ -region will inject p-type carriers into the n^- -region near the metallurgical p^+n^- junction of the PiN -structure. During low level of injection, all p -type carriers will recombine with the n -type carriers in the drift region. But when the injection is larger, during high level of injection, the excess p -type carries distribution reaches the n^-n^+ -junction and starts attracting electrons from the n^+ region and these are injected into the drift region, see Figure 14. Inside the drift region, these excess p - and n -type carriers

Figure 13: Principal structure of an *PiN* diode

will start to recombine. If the diffusion length of the carriers is longer than the drift region width, the spatial distribution of these will be relatively flat over the drift region, as presented in Figure 15. The average of the concentration distribution will be much greater than the doping density of the drift region, which results in increased conduction of the region, referred to as conductivity modulation [12].

Figure 14: Excess carriers are injected from both p^+ - and n^+ -region.

During high forward bias voltage, the current conducted through the power diode starts to deviate from an ideal exponential function because of the presence of an on-state resistance in the diode and the effect of high level injection. These effects are usually modelled with a parameter R_s , which represents the deviation from the exponential curve, and the voltage v across the p^+n^- -junction is given by

$$v = v_{AK} - R_s i \quad (22)$$

where v_{AK} is the applied voltage over the diode and i is the conducted current. Typical on-state characteristics with simplified temperature dependence for a power diode can be seen in Figure 16 [12].

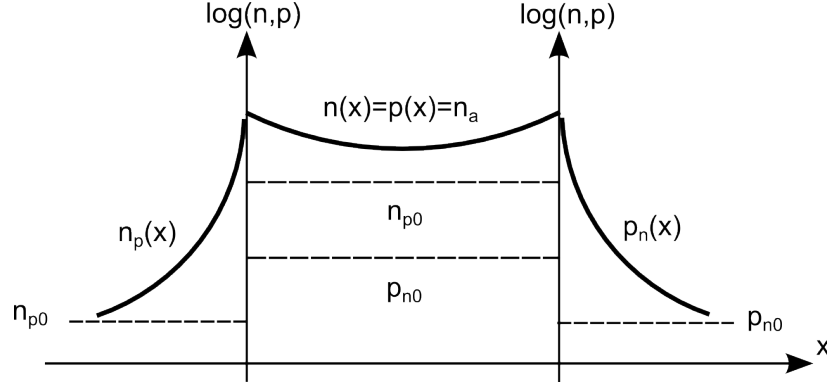


Figure 15: Charge distribution across the power diode during high injection forward-biased. The average concentration n_a is large in comparison with the majority carrier density n_{n0} in the drift region [11].

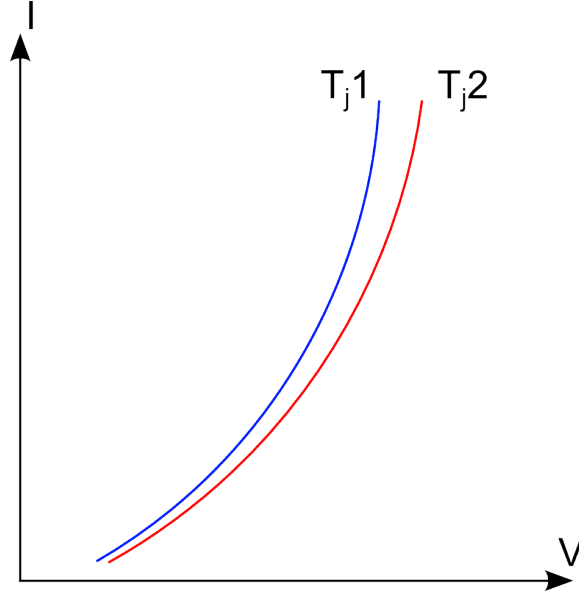


Figure 16: Typical forward characteristics for a power diode including simplified temperature dependence, where T_j is the junction temperature and $T_{j1} < T_{j2}$.

When the power diode is in reverse bias, only a small leakage current flows independently of the applied voltage until the critical point of breakdown voltage is reached. At this point, the current will increase very rapidly without any major increase of the reversed voltage. The high values of the applied voltage and current leads to an excessive power dissipation which quickly could destroy the diode, see Figure 17 for typical characteristics of a power diode in reverse bias including temperature dependence [11].

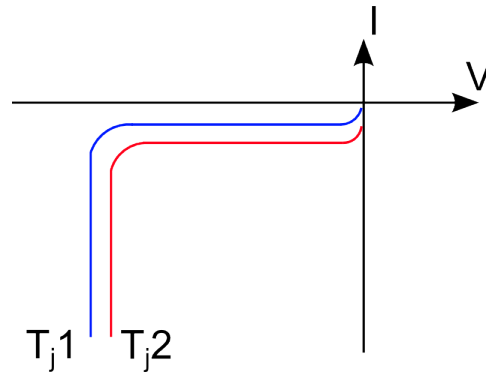


Figure 17: Typical reverse characteristics for a power diode including simplified temperature dependence, where T_j is the junction temperature and $T_{j1} < T_{j2}$.

During reverse bias, the applied voltage establish a depletion layer at the p^+n^- -junction. This space charge layer is mostly extended into the drift region due to the magnitude difference in doping levels between the two regions. The extension of the depletion layer can either be smaller or greater than the drift region width at breakdown voltage. If the boundary of the depletion layer dose not exceed the drift region, the diode is of non punch through-type. For the opposite case, the diode is a punch through-diode. Due to very high doping density in the n^+ -cathode the risk of penetration of the depletion layer into this region is negligible. The main difference between the two diode types are therefore how the electrical field strength varies inside the drift region. For a non punch through-diode, the electrical field strength is high at the anode and decreases towards zero at the other end of the drift region. The punch through-type will on the other hand have a relatively constant electrical field strength across the drift region, and decreases abruptly near the n^-n^+ -junction [11].

3.2.1 Switching Characteristics

During the transition from conduction state to blocking state or vice versa, the power diode goes trough a transition state which is not instant. From a circuit design perspective, it is important to take these transitions into account because they can result in severe over voltages/currents and increase the losses in the circuit. There are in general two types of characteristics for power diodes during switching, rectifying and fast switching. The rectifying diodes are design for conversion from AC to DC and therefore designed with low conduction losses and can not withstand large transient stresses. Fast diodes on the other hand are design for free-wheeling applications and can withstand larger transient stresses, normally used in parallel configuration

with switches. However, this comes with a trade off resulting in higher conduction losses [11].

When the voltage across a power diode in reverse bias is switched, it enters into the forward mode and starts to conduct current. This is referred to as forward recovery and during this transition the voltage drop over the diode can be several orders greater, especially if the current increases rapidly, in comparison with steady-state on-state operation. The number of diffusion minority carriers during this transient will be limited, which results in a current dependence of the voltage drop across the drift region. If the current derivative is large, some parts of the drift region will not be exposed to conductivity modulation and therefore have higher resistance, which results in a larger voltage drop over the diode, see Figure 18. After some time, the resistance will become constant over the drift region, resulting in the regular, steady-state voltage drop of the device [12].

When the power diode is switched off, the high concentration of free carriers in the drift region, which enables the low voltage drop during on-state, must be transported away so a new formation of a depletion layer can take place. This is called reverse recovery and results in an current transient, which is dependent on the circuit configuration. If the circuit consists of a resistive load, the current will immediately be reversed until the charge stored in the drift region is removed. But if an inductive load is connected to the circuit, the current will follow a certain ramp rate $a = -di/dt$ until the charge is transported away and the diode can support voltage again. When this takes place, the current has reached the reversed current peak I_{RM} and after will continue towards zero again. The voltage across the diode will be in forward mode until I_{RM} is reached, after this point the voltage is rapidly increased in the reversed direction, and reaches a peak short after that I_{RM} has occurred. After this, the voltage decrease to the reverse supply voltage, see Figure 18 for details [12].

3.2.2 Temperature Characteristics

How the forward voltage drop over a power diode changes depending on the current and the temperature of the device, is complex to fully understand and predict in simulations [13]. Depending on the level of current density and the manufacturing technique, different physical phenomena influences the voltage drop. This makes it hard to predict how the voltage drop will change for different levels of current density, and is individual for every power diode and manufacturer [13].

For a *PiN*-type of diode and low current densities, the forward voltage drop decreases with increasing temperature, mostly due to the increase of the intrinsic concentration in the diode [14]. This is referred to as a negative temperature coefficient for the device. For higher current densities, mainly

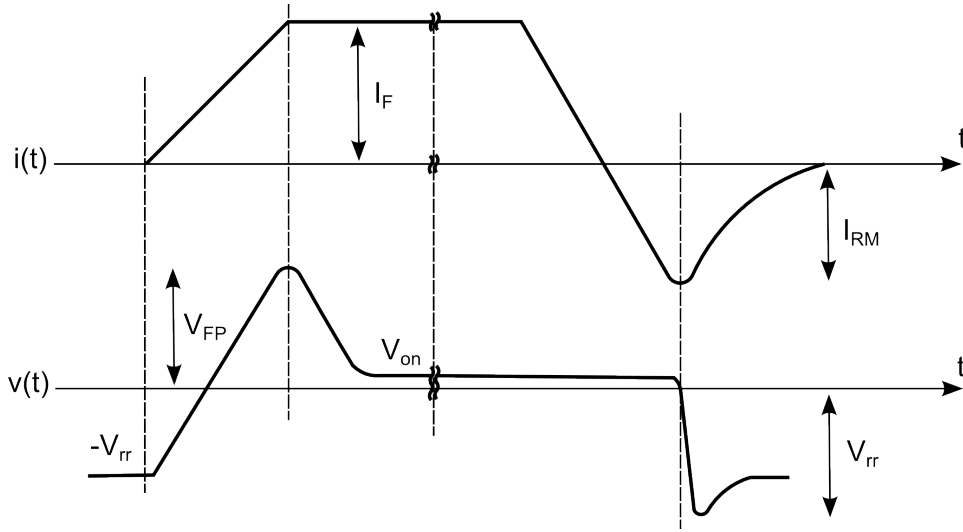


Figure 18: Current response for both switching stages of a power diode. To the left is a forward recovery conducted and to the left of the figure a reverse recovery.

two effects are considered: carrier mobility and carrier lifetime. With increased temperature, the carrier mobility decreases and carrier lifetime increases. How the resulting effect on the voltage drop becomes, is however hard to predict [14]. For some other levels of current densities and diode temperatures, the temperature coefficient can either be negative or positive depending of the device structure and manufacturing techniques [15].

3.2.3 Reliability

Reliability of a semiconductor device is the probability that the device can perform a desired task under a certain time interval without failing. Failure of performing the task can be a result of either instantaneous factors or related to long term degradation of performance. The definition of the two categories are not entirely clear and sometime the reason and classification of the failure can be a combination of the two. In general, a failure that occurs because of parameter change during a certain expected time interval and are measurable, can be classified as long term degradation. A much quicker change, often with a destructive outcome, is classified as instantaneous [15].

Long term degradation are not directly noticed, but affects the performance and the safe operation limits to avoid a instantaneous failure. Instantaneous failures occurs when the physical stress load on the device exceeds a certain limit. These loads can for example either be electrical, mechanical or thermal [15].

Temperature affects these two categories of failures, and therefore the reliability. The long term degradation of a device increase exponential with the increase of temperature, which means that a device operated under high temperatures has less lifetime then a device operating in a cooler condition. The manufacturers of semiconductors are using increased temperatures to be able to test the life time of their semiconductors in shorter time, also called to operate with a acceleration factor. An increase of temperature also affects the likelihood of an instantaneous failure. For example, semiconductor materials experiences mechanical stresses with increased temperature, especially if the increase rate is high, which could cause cracks and dislodgement of solder joints. At a certain temperature, these types of failure mechanisms can result in the loss of the device [15].

3.3 Lauritzen Diode Model

Many different types of diode models used for circuit simulations exists, they are either based on physics or the behaviour of the semiconductor device during operation. One of the physics based diode models, is the Lauritzen diode model which is based on lumped charge theory. The main difference from other models implemented in circuit simulators, is that the Lauritzen model includes the reverse recovery dynamics. However, there are more detailed models available which takes more physical phenomena into account. But these models demands a higher number of input parameters which normally are based on detailed data or measurements on the device, and are therefore complicated first to find and then to implement [16].

The Lauritzen model is developed for diodes with high injection rate, common for power diodes, and is based on equations for the charge transportation inside the semiconductor device. When the diode is rapidly turned off, a reversed recovery occurs. During this events, the charges inside the diode structure causes a current to run in the opposite direction when the diode becomes reversed bias, further explained in Section 3.2.1. The Lauritzen model of semiconductor devices is therefore often used for analysis of switching performance during power electronic design.

Analysing the charge distribution in the intrinsic part of the P-i-N structure before a reverse recovery, the charge distribution can be represented by four charge storage nodes presented in Figure 19 and a schematic plot over a reverse recovery is displayed in Figure 20 [16].

If electron and hole mobilities are assumed equal, the charge distribution becomes symmetric in the i-region which simplifies the representation further. The charge within each node can then be calculated as

$$q_1 = qA\delta p_1 \quad (23)$$

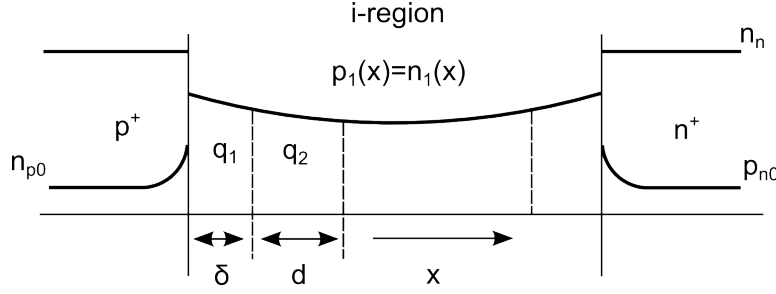


Figure 19: Charge distribution in the *i*-region before reverse recovery including the charge zones q_1 and q_2 .

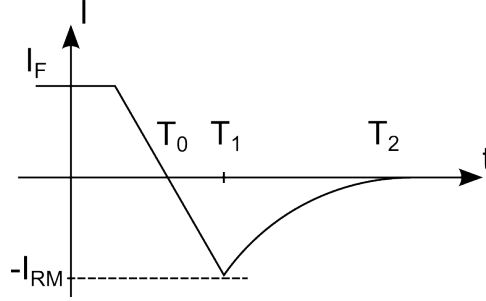


Figure 20: Turn-off current waveform for an inductive load, where T_1 is the time when the reverse current reaches the peak I_{RM} .

$$q_2 = qAdp_2 \quad (24)$$

where A is the area of the junction, q the electron charge, δ and d represent the width of the charge nodes and p_1 p_2 the average hole concentration in the different nodes [17]. The current flowing between the two nodes can then be represented by the ambipolar diffusion equation as

$$i(t) = -2qAD_a \frac{dp}{dx} = \frac{4qAD_a(p_1 - p_2)}{\delta + d} \quad (25)$$

where D_a is the ambipolar diffusion constant. This current is also known as the diffusion current. During a reverse recovery, the stored charge in q_1 will be drained before the charge in q_2 . This leads to an abrupt current change in the opposite direction at $t = T_1$ when the charge in q_1 becomes zero and the q_2 node provides the only charge by diffusion to q_1 [17]. If the charge in q_1 is minimized by letting $\delta \rightarrow 0$, (25) becomes

$$i(t) = \frac{q_0 - q_2}{T_{12}} \quad (26)$$

where the diffusion time through q_2 is $T_{12} = d^2/4D_a$ and $q_0 = qAd(p_1 - p_{i0})$. This does not represent any charge storage, it is the remaining part of the variables when $\delta \rightarrow 0$ [17]. By applying the continuity equation for the charge control in node q_2 the following is given

$$0 = \frac{dq_2}{dt} + \frac{q_2}{\tau} + \frac{q_0 - q_2}{2T_{12}}. \quad (27)$$

The continuity equation consists of three terms. The first term dq_2/dt is charge storage, followed by the recombination term with the lifetime τ and the last term is half of the diffusion charge flowing from the junction between the P - i -region of the diode into the q_2 -node. The relationship between the applied junction voltage and the variable q_0 can be found by applying the junction equation at the intersection between P - and i -region,

$$(p_1 - p_{i0}) = p_{n0} \left[\exp\left(\frac{V}{2V_T}\right) - 1 \right] \quad (28)$$

where $V/2$ is half of the applied junction voltage representing the voltage over the P - i junction [17]. If (28) is multiplied with qAD_a , q_0 is given by

$$(p_1 - p_{i0}) = q_0 = \frac{I_s \tau}{2} \left[\exp\left(\frac{V}{2V_T}\right) - 1 \right]. \quad (29)$$

In (29) the diode saturation current I_s , could also be expressed as $I_s = qA_2dp$. To simplify the derived expressions, the following substitutions can be done; $q_M = 2q_2$, $q_E = 2q_0$ and $T_M = 2T_{12}$ [17]. This gives three model equations

$$i(t) = \frac{q_E - q_M}{T_M} \quad (30)$$

$$0 = \frac{dq_M}{dt} + \frac{q_M}{\tau} + \frac{q_E - q_M}{T_M}. \quad (31)$$

$$q_E = I_s \tau \left[\exp\left(\frac{V}{nV_T}\right) - 1 \right] \quad (32)$$

where n is the emission coefficient and replaces the factor two in (32). This coefficient is normally two for power diodes and one for diodes with low level of injection. To complete the model for the diode, both series resistance and junction capacitance must be modelled as displayed in Figure 21 [18].

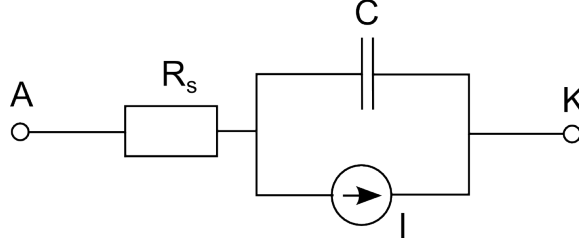


Figure 21: Circuit representation of power diode with both series resistance R_s , junction capacitance C and the junction is represented by a current source.

The junction capacitance can be represented by the following set of equations [18],

$$\begin{aligned} C &= T_M \frac{di}{dV} + Cj0 \left(1 - \frac{V}{V_j}\right)^{-m_j} \quad \text{for } V < F_c V_j \\ C &= T_M \frac{di}{dV} + \frac{Cj0}{F_2} \left(F_3 + \frac{m_j V}{V_j}\right) \quad \text{for } V < F_c V_j. \end{aligned} \quad (33)$$

In (33), $Cj0$ is the zero bias junction capacitance, m_j a capacitance grading coefficient and V_j the built-in junction voltage. The parameter F_c is a coefficient which represents the depletion of the capacitance in forward-bias and is used for calculation of F_2 and F_3 [18], as

$$\begin{aligned} F_2 &= (1 - F_c)^{1+m_j} \\ F_3 &= 1 - F_c(1 + m_j). \end{aligned} \quad (34)$$

This is the final equation needed in the Lauritzen diode model and several of these Lauritzen representation parameters are usually given by the manufacturer.

3.3.1 Parameter Extraction

The derivation of the Lauritzen diode model in Section 3.3 resulted in the following parameters which are needed for implementation of the model, see Table 1.

Both τ and T_M can be estimated from a diode turn off waveform, or reverse recovery for a given load displayed in Figure 20. When $t \leq T_1$ the current is dominated by the circuit and the stored charge $q_M(t)$ can be found by

Table 1: The parameters needed for the physics based Lauritzen model.

I_s	Saturation current
τ	Minority carrier lifetime
T_M	Diffusion transit time
V_j	Built-in junction potential
n	Emission coefficient
R_S	Series resistance
C_{j0}	Junction capacitance at zero bias
m_j	Junction capacitance grading coefficient
F_c	Junction capacitance depletion coefficient

eliminating $q_E(t)$ from (30) and (31) and evaluate $q_M(t)$ when $a = -di/dt$ and $i(t) = I_F$ [17],

$$q_M(t) = a\tau \left[T_0 + \tau - t - \tau \exp\left(-\frac{t}{\tau}\right) \right]. \quad (35)$$

When $t = T_1$ the charge $q_M(t) \rightarrow 0$ due to depletion and the transfer of charge from q_M is limited by diffusion which results in initiation of the diode recovery [17]. Then (30) becomes

$$i(T_1) = -I_{RM} = -\frac{q_M(t)}{T_M} \quad (36)$$

where I_{RM} is the peak of the reverse current and is normally given in component specification datasheet. The recovery of the diode when $t \geq T_1$ is independent of the reverse voltage and the following relationship can be derived from (31), (32) and (36) [17],

$$I_{RM} = a(\tau - \tau_{rr}) \left[1 - \exp\left(-\frac{T_1}{\tau_{rr}}\right) \right]. \quad (37)$$

The coefficient τ_{rr} is the reverse recovery time constant and can be represented by τ and T_M as [17],

$$\frac{1}{\tau_{rr}} = \frac{1}{\tau} + \frac{1}{T_M}. \quad (38)$$

The coefficient τ can be estimated by $\tau = Q_{rr}/I_F$, where Q_{rr} is the recovery charge and I_F the forward current before recovery and these quantities are

usually given in datasheets together with τ_{rr} . If these are known, (38) can be used to find T_M . Otherwise it can be extracted from (37) and (38), by inserting $T_1 = T_0 + I_{RM}/a$ which only requires a reverse recovery waveform [19].

The model parameter F_c is normally a factor between zero and one, and is set to $F_c = 0.5$ as default to represent the linear approximation of the exponential junction capacitance during forward bias. For a linear graded junction, the junction capacitance coefficient is set to $m_j = 0.33$ and $m_j = 0.5$ for abrupt junctions. Usually, the junction potential V_j is in the range of 0.2-1 V if nothing else is given in the component specification. The emission coefficient n can be set to $n = 1$ for low level injection devices and $n = 2$ for high level injection devices, which is common for power diodes. The zero-bias capacitance can be estimated to $C_{j0} = 1$ nF if measurements are not available [18].

Both R_s and I_s can be estimated from the forward characteristics in the datasheet by using a set of data points in the regular diode equation [18].

3.4 Thermal Modelling

Modelling the thermal properties of a semiconductor device, the virtual junction temperature can be decided. Since the temperature of the semiconductor chip is not evenly distributed in the package, a virtual junction temperature is defined. This temperature is the average chip temperature assuming homogeneous cooling of the device [20]. The temperature is critical for the performance and reliability of the device and alters its electrical properties [11].

Thermal representation is often considered to be a one-dimensional problem. The heat flows from a point with high temperature to a point with lower temperature. For a given constant heat flux between these two points, the absolute thermal resistance is described as the amount of heat energy that flows per unit time.

By using analogy to electrical circuits, the heat flow can be represented with a constant current source. With the same reasoning the absolute thermal resistance are modelled as a resistor. By using common electrical calculation methods, the temperature calculations are analogous to those of voltage. By using these passive components, the steady state temperatures in a semiconductor device can be determined. Using the electrical analogy, the temperature difference between two points, where one point has a constant power loss can be defined as

$$T_1 - T_2 = R_{th,1-2} P_{loss} \quad (39)$$

where $R_{th,1-2}$ is the thermal resistance between the two points.

By introducing a capacitor in the thermal-electrical analogy, the transient thermal behaviour of the device can be modelled. During a power surge, the generated heat is spread through the materials and the capacitor is used to represent the heat capacity of the material [11].

3.4.1 Foster Model

Foster thermal model consists of parallel resistors and capacitors, called a cell, connected in a series ladder configuration. The model is used to determine the thermal transient response between two points in the semiconductor. This means that each individual cell in the series ladder configuration is not directly represented by the thermal response of a geometrical layer in the semiconductor. Thus, each individual cell can change place with each other without altering the thermal response of the system. By using electrical calculations, the temperature at the virtual junction related to the ambient temperature can be described by the expression

$$T_{junction} = Z_{th,tot} P_{loss} + T_{ambient} \quad (40)$$

where $Z_{th,tot}$ is the total impedance between the two nodes $T_{junction}$ and $T_{ambient}$. P_{loss} is the total thermal loss at the virtual junction of the semiconductor.

The Foster model parameters can be calculated from curve fitting with measurement data. The curve can be expressed as a finite sum of exponential terms

$$Z_{th} = \sum_{i=1}^n R_i (1 - \exp(-\frac{t}{\tau_i})) \quad (41)$$

where i is the term index, t is the time, n is the number of chosen time constants, R_i is the thermal resistance and τ_i is the thermal time constant [21]. The thermal capacitance C_i can be expressed from the definition of the thermal time constant

$$\tau_i = R_i C_i \quad (42)$$

where R_i is the thermal resistance. The Foster model can be expressed with a different number of time constant with index number i , a large number of indexes improves accuracy but increases simulation time [20].

3.4.2 Cauer Model

A Cauer thermal model consists of resistors connected in series, with ground connected capacitors connected between every resistor. Each pair of resistor and capacitor can, opposite to the Foster model, be represented by a geometrical layer in the semiconductor structure. Thus, the values in model can be calculated from material parameters

$$R_{th} = \frac{1}{\lambda} \frac{d}{A} \quad (43)$$

$$C_{th} = c\rho dA \quad (44)$$

where λ is the specific thermal conductivity, d and A are the thickness respectively the cross section area of the geometrical layer, c is the specific heat capacity and ρ is the specific density [21].

The model parameters for the Cauer model can also be derived from the Foster model parameters. By setting the thermal responses as equal and comparing the two circuits, a relationship between the two models can be established [21]. When performing this procedure, the resulting Cauer parameters has no physical representation to the geometrical layers in the semiconductor structure [20].

Simulations using the Cauer model has in some specific cases easier to converge than the Foster model, but the parameters extraction from measurements are more complicated [21].

4 Case Set-up

Two separated electrical networks are planned to be connected with an HVDC-link between them in order to increase the flexibility and enable trading with electricity. At the prospective location of the interconnection, the two grids are separated by a 100 km wide ocean bay and therefore a submarine cable is a suitable solution.

The first grid, referred to as Network A, has a nominal voltage of 420 kV, 50 Hz on transmission level and has a short circuit power of 27560 MVA. The second grid, Network B, are built up with 360 kV, 50 Hz as nominal voltage on the transmission level and the system has a short circuit power of 8360 MVA. The HVDC-transmission connecting the two networks has the capacity rating $P_b = 700$ MW active power, and is of a symmetric monopole configuration. This means that two separated cables are used, one for each DC-pole, charged with positive or negative voltage at the same amplitude. The two converter stations are assumed to be placed close to shore, which means that no land cables will be necessary and only submarine cables will be used. The converter stations are based on the MMC-voltage source converter technology with a DC-voltage of ± 320 kV, see Figure 22 for a schematic overview [22].

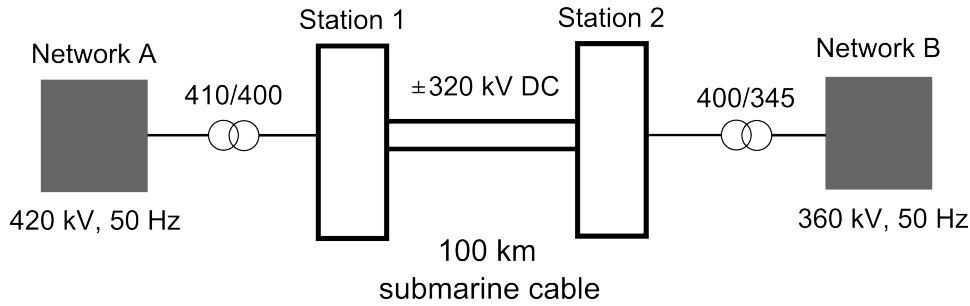


Figure 22: Layout of the case system connecting Network A with Network B through a ± 320 kV submarine cable based HVDC-link.

Both HVDC-stations are designed according to a standardized ABB M9-station with a converter AC-voltage of 400 kV, resulting in a transformer with 410/400-ratio in Station 1 and a 345/400-ratio of the transformer in Station 2. The submarine cables connecting the two stations are fabricated of a cross-linked polyethylene insulation material and the conductors are made of copper. As an outer layer, the cables are equipped with a heavy shield in order to withstand sub-sea applications. The capacity of the M9-system, ratings of the ingoing converter components and cable data are presented in Table 2 [1][22].

The M9 MMC-converter are built up of 6 valve arms, one positive and one

Table 2: Ratings of the standardized ABB M9-station together with corresponding values of ingoing system components [1][22].

Rated power, S_b	1281 MVA
Converter AC voltage, U_c	400 kV
Nominal DC voltage, U_d	320 kV
Converter reactor, L_r	57.6 mH
Smoothing reactor, L_{sm}	10 mH
Valve arm resistance, R_v	40 m Ω
Rated power of Transformers, S_{tb}	1150 MW
Transformer impedance, X_t	0.17 p.u
Cable conductor area, A_c	1800 mm ²
Cable diameter, d_c	137 mm
Cable resistance, R_c	9.8 m Ω /km
Cable inductance, L_c	126 μ H/km
Cable capacitance, C_c	212 nF/km
Spacing between cables, $d_{c,spacing}$	0.12 m
Cable distance to ground, $d_{c,ground}$	0.2 m

negative for each phase. These arms consists of 38 cells and each cell itself consists of two position with eight series connected 5SNA 2000K450300 StakPak IGBT-modules. This component is able to block 4.5 kV and conduct a continuous current of 2000 A [23].

When the HVDC-transmission is in operation, the highest temperature the StakPak modules can withstand during continues operation is 125 degrees. In the investigation, this will be considerer as the worst case scenario before any fault occurs in the system, which results in the most severe thermal stress on the semiconductor component. The StakPak casing temperature will be considered constant during surge events, which normally is a transient sequence [23].

5 Analysis

In the following chapter, the previous described case will be investigated in order to find the highest fault currents through the converter components during a set of possible fault scenarios. This will be done both analytically and by simulations of the case system in order to compare and verify the results. During a fault event, the control system is assumed to immediately block the IGBTs, hence the surge current flow through the diodes only. These worst case currents will then be used for performance evaluation of the Lauritzen diode model during transient surge conditions. This will also be compared with extrapolated measurements of the StakPak component. The comparison will contain an investigation on how the temperature changes inside the component during a surge event by implementing a thermal model of the component together with both representations of the diode characteristics.

5.1 System Fault Analysis

Fault analysis of the HVDC-system described in Section 4 is performed in this part of the analysis. For different fault cases, the fault current and the corresponding current through the converter components will be calculated analytically and later compared with simulation result from a system model build up in PSCAD.

The complexity of a HVDC-tansmission system is high with many fault scenarios that may occur, which makes fault analysis a comprehensive task. Therefore, the number of different fault cases investigated are limited to those with the highest probability of large fault currents. In general, according to the information in Section 2.4.1, symmetrical AC-faults are more severe in aspect of the fault current amplitude in comparison with asymmetrical faults. On the AC-side of the converter, a fault occurring in valve and reactor hall is unlikely due to its location in a building with controlled environment. On the other hand, the AC-yard is usually located outdoors and is more likely to be exposed to disturbances. On of the key components in the AC-yard is the power transformer, therefore two fault cases located at each side of the transformer are investigated and are labelled fault F1 and F2. On the DC-side of the converter, faults occurring close to the converter are most severe due to lower fault impedance. More or less does it only exist two fault cases on the DC-side, pole-to-pole and pole-to-ground fault. Therefore are these two cases selected to be investigated, located between the converter valve and the smoothing reactor in the DC-yard. Pole-to-ground fault is referred to as fault F3 and the pole-to-pole fault is labelled as fault F4. All the fault cases are presented in Figure 23. The fault impedance in all cases are assumed to be zero.

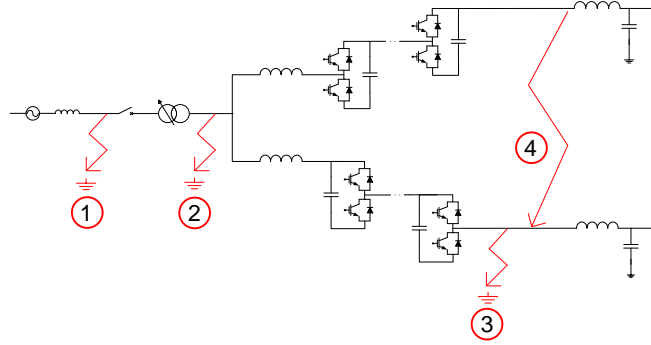


Figure 23: Four fault cases are considered in each station in order to find the most severe scenario and highest current through the components.

In the case set-up, the HVDC-link consists of two stations that can operate in both rectifying and inverter mode in order to enable power transmission in both directions. However, for simplification of the analytical fault analysis, these modes will be considered to give equal fault currents, but in the simulations on the other hand will both operating modes for each station be investigated in order to find the most severe fault cases.

5.1.1 Fault Current Calculations, Station 1

When Station 1 operates in rectifier mode, active power is transferred from Network A to Network B and in opposite direction when operating in inverter mode. The most severe fault current occurs when the system is operating at the maximum active power capacity P_b . Using (6), (7) and $S_B = 100$ MVA, the short circuit impedance of Network A is calculated to $Z_{netA} = 6.40 \Omega$. The peak current through the fault location F1, fed from the AC-network side, is determined by

$$I_{scAC,F1} = \frac{2\sqrt{2} V_{netA}}{\sqrt{3} Z_{netA}} = \frac{2\sqrt{2} 420}{\sqrt{3} 6.40} = 107.16 \text{ kA} \quad (45)$$

where V_{netA} is the nominal voltage of Network A and the current is scaled by the factor $2\sqrt{2}$ in order to get the surge current peak according to Section 2.4.1. However, the DC-side will be discharge during this fault and contribute to the total fault current $I_{sc,F1}$. Because the switching IGBTs are set to block instantly, will the cell capacitance not be discharged during a fault event and dose not contribute to the fault current. Due to the layout of each cell in the valve arms, one side of the converter will have the parallel diodes in block direction towards the DC-cables, which results in only one of the two DC-cables in the system will be discharged, see Figure 24.

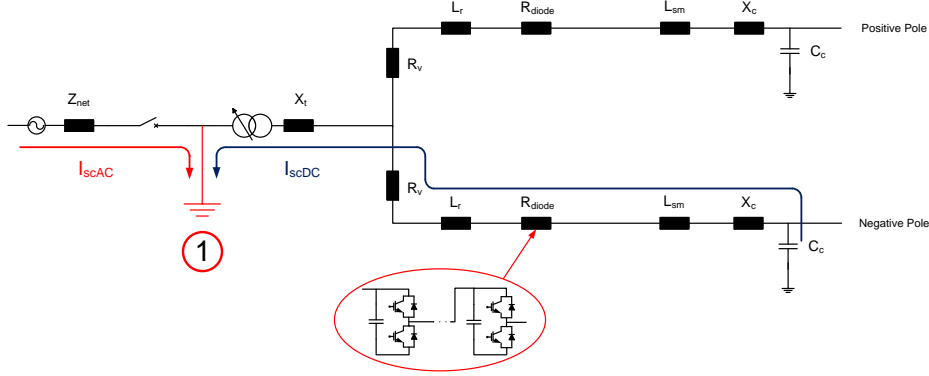


Figure 24: Schematic view of the surge current paths during fault F1.

This DC-cable discharge will on the other hand feed the fault through the non-blocking converter valve arms, reactors and transformer. This current is of high interest in order to find the most severe fault case with aspect of the semiconductor components. This current path, with a resistance several orders smaller than the LC-components, can be seen as a resonating series RLC-circuit and the current peak can be calculated using (19) derived in Section 2.4.2, inserting values of the case system components. The total resistance of the StakPak diodes in each valve arm is given in the datasheet as $R_{diode,arm} = 1.2 \cdot 10^{-3} \cdot 38 \cdot 8 = 0.12 \Omega$, where it is 8 devices conducting during the fault in each cell and the total number of cells are 38. The total resistance of the three conducting phase arms, which are connected in parallel, is given by $R_{diode} = R_{diode,arm}/3 = 0.04 \Omega$. All this results in a fault current contribution $I_{scDC,F1} = 3.65$ kA referred to the network side of the transformer. The current through each valve arm, will however be $I_{arm,F1} = I_{scDC,F1}/3 = 1.22 \cdot 410/400 = 1.25$ kA referred to the converter side of the transformer. The total fault current will be the sum of these two currents $I_{sc,F1} = I_{scAC,F1} + I_{scDC,F1} = 107.16 + 3.65 = 110.82$ kA.

To find the fault current and the corresponding current through the valve arms when fault F2 occurs, similar calculations are performed. The only difference will be that the transformer inductance is added to the network calculation and withdrawn from the converter calculation, see Figure 25. This results in a fault current $I_{scAC,F2} = 22.82$ kA from the Network A through fault F2. The corresponding fault current from the converter side is $I_{scDC,F2} = 5.30$ kA and each valve arm conducts $I_{arm,F2} = 1.73$ kA. The total fault current is once again the sum of $I_{scAC,F2}$ and $I_{scDC,F2}$, $I_{sc,F2} = 28.03$ kA.

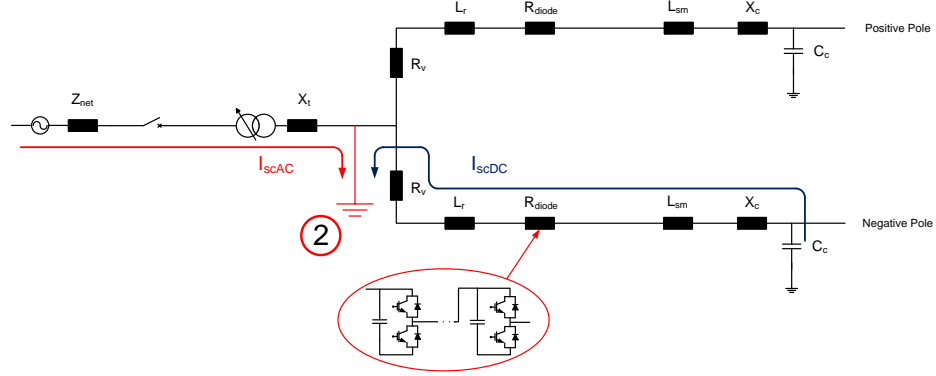


Figure 25: Schematic view of the surge current paths during fault F2.

When analysing fault case F3, similar calculations can be used once again. However, when the fault location is on the DC-side of the converter it can be represented as a three phase rectifying bridge because the IGBTs are blocked, see Section 2.4.3. The total fault current from the AC-side thereby flows mainly through one valve arm at a time. Summation of the impedances on the left side of fault F3 and used in calculation of fault current from AC-side results in $I_{scAC,F3} = I_{arm,F3} = 14.24$ kA. The DC-cable will also be discharge, but only with a resonating series RLC circuit consisting of the cable and the smoothing reactor. This results in $I_{scDC,F3} = 9.80$ kA and the total current of $I_{sc,F3} = 24.05$ kA, see Figure 26.

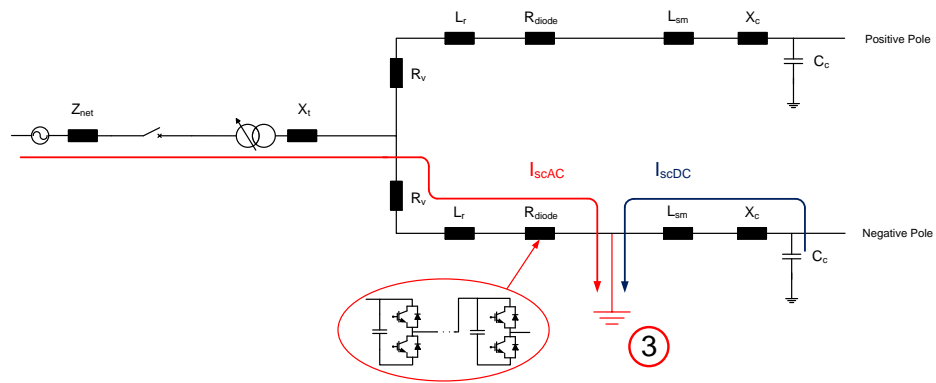


Figure 26: Schematic view of the surge current paths during fault F3.

When fault F4 occur in Station 1, the converter is short-circuited on the DC-

side of the valve arms. During this fault can the converter be represented by a short-circuited diode rectifier bridge according to Section 2.4.3. The current through the valve arm from the AC-side can then be calculated with (20) and (21) which gives $I_{scAC,F4} = I_{arm,F4} = 17.06$ kA when inserting the total reactance and resistance of the AC-side. The DC-cable will discharge in the similar way as in fault case F3, but the two cables are now connected together and the resonating series RLC-circuit will consist of both cables. The DC-voltage applied to the circuit will also be doubled and result in a $I_{scDC,F4} = 9.80$ kA which gives the total fault current $I_{sc,F4} = I_{scAC,F4} + I_{scDC,F4} = 26.86$ kA.

All fault currents calculated for each fault case and the corresponding current through the valve arm is given in Table 3 for Station 1. It is clear that the highest fault currents are generated from fault on the network side of the transformer but the most severe valve arm currents are generated from DC-side faults.

Table 3: Resulting fault currents for each fault case in Station 1 from analytical calculations.

	I_{sc} [kA]	I_{arm} [kA]
Fault F1	110.83	1.25
Fault F2	28.03	1.73
Fault F3	24.05	14.24
Fault F4	26.86	17.06

5.1.2 Fault Current Calculations, Station 2

Network B, connected to Station 2 has both lower short circuit power and lower nominal voltage in comparison with Network A which could result in a reduction of the fault stresses. However, fault analysis will still be conducted for Station 2, at least for verification of the simulation results in PSCAD. With (6), (7) and $S_b = 100$ MVA can the short circuit impedance $Z_{netB} = 15.55 \Omega$. Using (45) and inserting $V_{netB} = 360$ kV and Z_{netB} , the resulting current from the AC-side during fault F1 becomes $I_{scAC,F1} = 37.81$ kA. During this fault F1 will the DC-side discharge in the same way as in previous calculations for Station 1. Because the stations has de same components will the valve arm current be equal for Station 2, $I_{arm,F1} = 1.25$ kA. The corresponding current from the DC-side $I_{scDC,F1} = 4.33$ kA referred to the network side of the transformer and the total current is $I_{sc,F1} = I_{scAC,F1} + I_{scDC,F1} = 42.14$ kA.

The other three fault cases can be calculated in the same way as in Station 1 and the result is presented in Table 4, where it is clear that the fault currents are lower for each fault case in Stations 2 in comparison with Station 1. The result are also displaying similar result as the previous section, the highest valve arm current is generated by DC-side faults and the highest fault current corresponds to AC-faults.

Table 4: Resulting fault currents for each fault case in Station 2 from analytical calculations.

	I_{sc} [kA]	I_{arm} [kA]
Fault F1	42.14	1.25
Fault F2	21.03	1.73
Fault F3	20.06	10.26
Fault F4	24.43	14.63

5.1.3 PSCAD Simulations

A simulation model of the HVDC-transmission system presented in Section 4 was built up in PSCAD. The simulation platform was built around a model received from ABB System Department containing the valve and control system including the switching logic. In this package, the diodes in the valve had constant forward voltage drop which was according to component datasheet. The control system included both an active power control and a voltage control. However, only the active power control was used in this study. The AC-network, converter reactor, power transformer and DC-cable were represented with standard PSCAD-components. The AC-network was modelled as a three-phase voltage source with a corresponding impedance in series to receive the correct short-circuit power.

In order to verify the steady-state operation of the simulation model, no fault was applied and maximum active power according to case set-up was simulated and studied, the waveforms can be seen in Figure 27. In this steady-state plots, it shows that the active power control stabilize the power flow at the reference value $P = 700$ MW. The current through the converter has a waveform comparable with a standard rectified current shape, which shows acceptable performance of the simulation model in steady state.

When the operation of the HVDC-system simulation was verified, four different fault cases were applied to the system. To find the moment when the highest surge current through the diodes occur, the time of fault was swept in steps of 1 ms over a whole AC-voltage period of 20 ms. The same fault cases were applied on the HVDC-stations as in the analytical calculations,

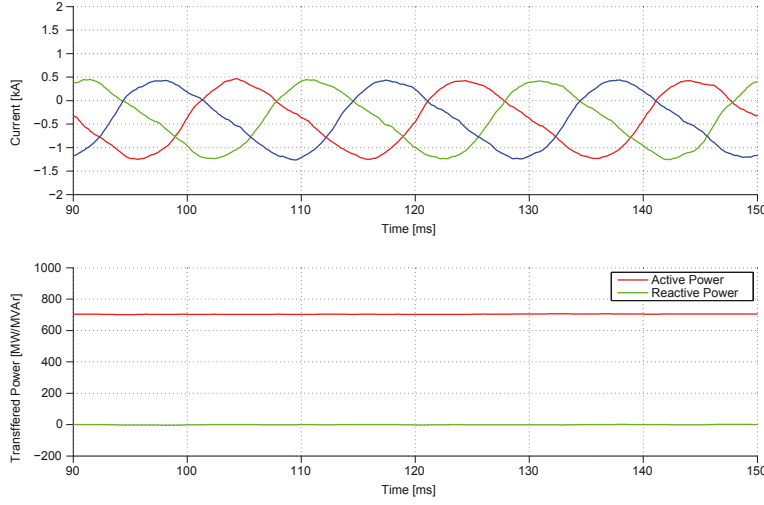


Figure 27: Station 1 operation in steady-state, transferring 700 MW of active power to station 2. The corresponding valve current in each valve arm is presented in a) and the active and reactive power is presented in b)

except now the four fault cases were applied for both rectifying and inverter mode in each station. The number of simulated fault cases therefore becomes 16 in total and all fault cases were applied with zero fault impedance.

The outcome of the simulations yielded that the largest surge current peaks occurs in station 1 when it operates in rectifying mode. This result corresponds to the analytical calculations. Both simulation and calculation shows similar results, the largest valve arm currents occurs during faults on the DC-side of the converter. On the other hand, when a fault occurs on the AC-side of the converter, the largest currents through the fault are generated. The results from each fault simulation are presented and compared with analytical results in Table 5, where each current value from simulations corresponds to the highest peak occurring for the different fault cases. First, all fault cases were applied in Station 1 for the two operating modes and then in the same way for Station 2.

In Table 5, the highest fault currents appear when the faults are applied in Station 1, mainly because of the stronger Network A connected to this station. However, for the surge current through the valve arms, both stations are exposed to similar currents, but Station 1 revives a slightly higher surges for DC-side faults. It can also be seen that the fault current through the valve arm appears to be slightly higher when the converter operates in rectifier mode in comparison with inverter mode for fault on the DC-side, which is according to the analytical results. But, it seems like the calculations over-

Table 5: Comparison between simulation and calculation results. The simulations are also conducted for the two different operating modes of each station.

		F1		F2		F3		F4	
	[kA]	I_{sc}	I_{arm}	I_{sc}	I_{arm}	I_{sc}	I_{arm}	I_{sc}	I_{arm}
Station 1									
Calculated		110.83	1.25	28.03	1.73	24.05	14.24	26.86	17.06
Sim. Rectifier		103.48	1.69	28.88	3.71	20.46	8.58	28.12	15.13
Sim. Inverter		105.19	3.24	28.93	3.78	20.72	7.44	28.66	15.08
Station 2									
Calculated		42.14	1.25	21.03	1.73	20.06	10.26	24.43	14.63
Sim. Rectifier		38.47	1.7	20.77	3.66	20.36	7.43	26.75	12.06
Sim. Inverter		40.23	3.16	21.67	3.68	20.76	6.25	27.59	12.05

estimates the peak value. Probably is the approximated equation in Section 2.4.3 giving the noticed overestimation of the peak for fault F4. In Figure 28, it can also be seen that the surge current actually flows through two diodes when the peak occurs which could explain the lower simulation peak value. Fault F3 on the other hand, Figure 28 shows that only one phase conducts the current according to the assumptions in the calculations for this fault but the results are still deviating. This could be an indication that another calculation method is needed for DC-fault, similar to F4. However, fault F3 shows lower peak values for both calculations and simulations in comparison to F4 and the calculation error can therefore be accepted and fault F4 is considered the most severe case for the converter valve components.

For these two fault cases, F3 and F4, the current though the fault has similar characteristics. In Figure 29, the simulation results for fault F3 is presented where the DC-cable discharge is visual in the fault current. In the plot, the active and reactive power starts to oscillate when the fault occurs and stabilizes after a short time when the converter IGBTs blocks.

For AC-faults, the both valve arm and fault currents are actually slightly higher for inverter operation in comparison with rectifier mode, which is the opposite to DC-faults. In general, these higher simulation results matches the calculated peak values rather well for the fault currents, but not very well for the valve arm currents. This could be that the approximation of the oscillating RLC-circuit it not accurate enough, with reservation that it matches better when the stations are operating in rectifier mode. One possible explanation of this mismatch is according to Figure 30 and Figure 31

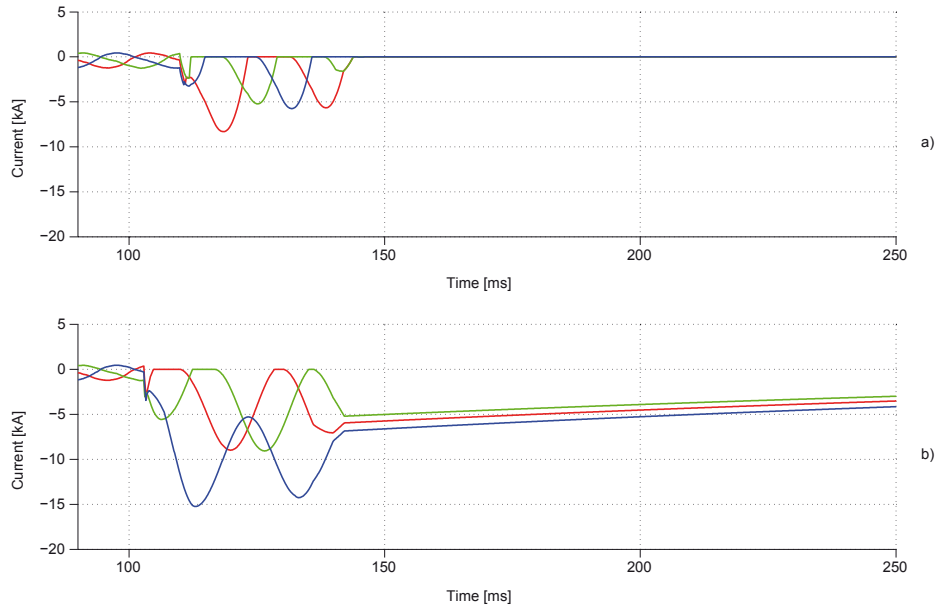


Figure 28: Surge currents through each valve arm for fault F3 presented in a) and fault F4 in b) when Station 1 operates in rectifier mode.

that the converter actually continues to switch during these AC-faults. As described in Section 2.4, this is performed to prevent the fault to propagate between the connected AC-network and maintaining the DC-link voltage. In Figure 30 and Figure 31, this is clearly noticed in the active and reactive power oscillations generated during fault F3 and F4. This dynamic behaviour was not take into account during the analytical calculations and is likely to correspond to the calculation error of the valve arm currents during fault on the AC-side.

5.2 Lauritzen Model Parameter Extraction

In order to build a complete Lauritzen model of the StakPak module characteristics, usually two models are designed. One representation for the IGBT and another for the diode parallel to the switching IGBT. However, in this thesis, the IGBTs are neglected because they are set directly in blocking mode when a fault occur in the HVDC-system. The only Lauritzen model needed is therefore the representation of the power diode inside the StakPak module. Data from a reverse recovery measurement at a junction temperature of 125 degrees presented in the StakPak datasheet enables an extraction of the model parameters according to the derivation in Section 3.3. This results in a diode model representing the characteristics under worst case continuous operation.

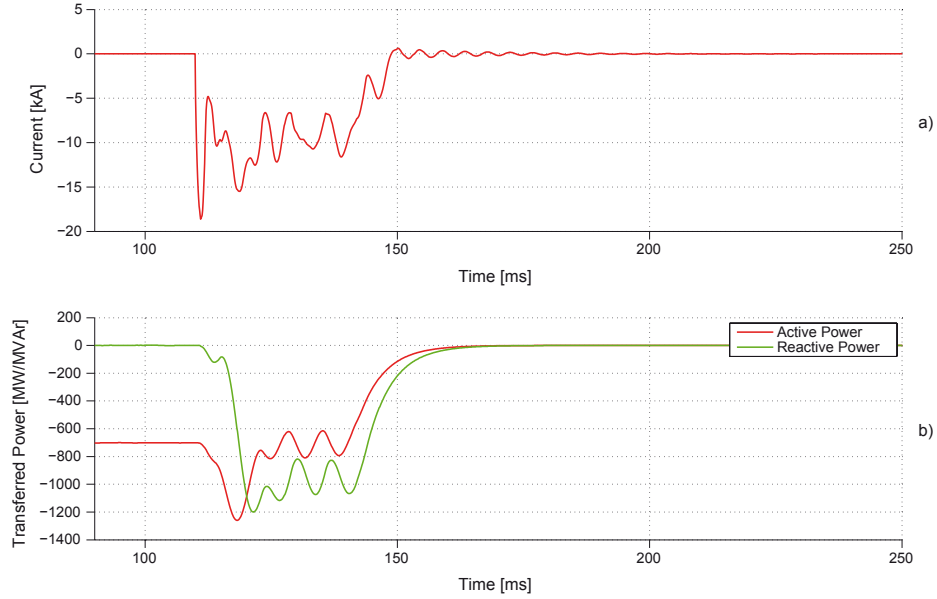


Figure 29: Plot a) presents the current through the fault in case F4 and b) the transmitted active and reactive power through Station 1 when it operates in rectifier mode.

There are a few parameters given in the datasheet that can be used for extraction of the initial model parameters in the Lauritzen model. However, updated measurements of a reverse recovery has been received from the manufacturer, which will be used for the extrapolation of the model parameters. When all parameters is calculated for the StakPak module, it still needs to be tuned against the reverse recovery and forward measurements, in order to receive adequate accuracy. For a forward current $I_F = 2000$ A, the resulting reverse current peak is $I_{RM} = 1940$ A when the component has a chip temperature of $T_j = 125$ degrees, stray inductance $L_\sigma = 200$ nH and inductive loading. The resulting slope of the decreasing current, which is circuit dependent, is $di/dt = -2.6$ kA/ μ s and the reverse recovery time is $\tau_{rr} = 4.08$ μ s. Both current and voltage from the recovery process are presented in Figure 32, although the voltage is not needed for the Lauritzen model [23][24].

Inserting the values of a , τ_{rr} and the time when the reverse current reaches its peak value $T_1 = 1.09$ μ s in (37) and (38) gives the model parameters τ and T_M , presented in Table 6. $Cj0$ were set to 1 nF, $F_c = 0.5$ and $m_j = 0.5$ as initial values according to the information given in Section 3.3.1. In this investigation, the StakPak diode will be mostly under high injection and therefore the emission coefficient is set to $n = 2$. The junction potential is

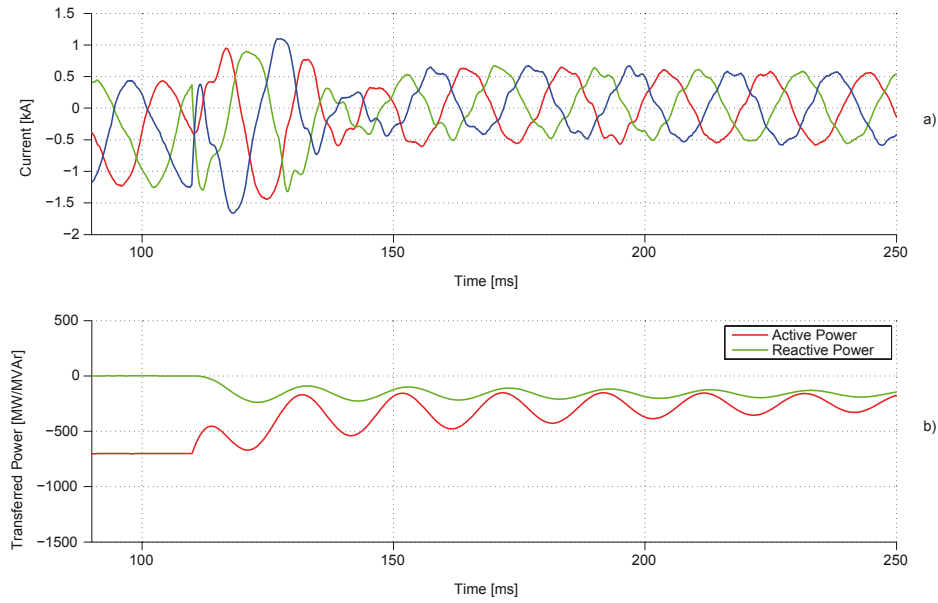


Figure 30: Valve arm current for fault F1 is presented in a) and active and reactive power in the converter during the fault is displayed in b).

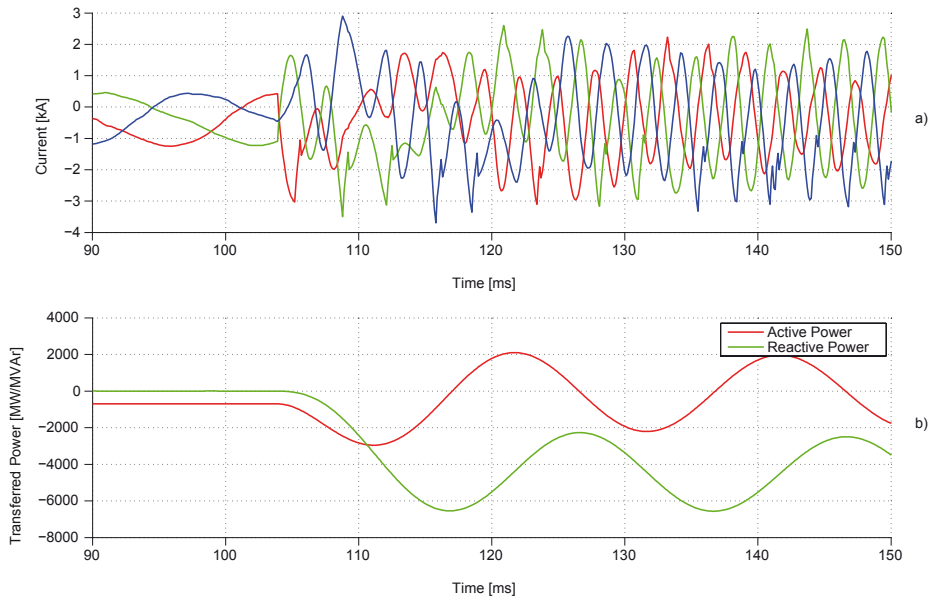


Figure 31: Valve arm current for fault F2 is presented in a) and active and reactive power in the converter during the fault is displayed in b).

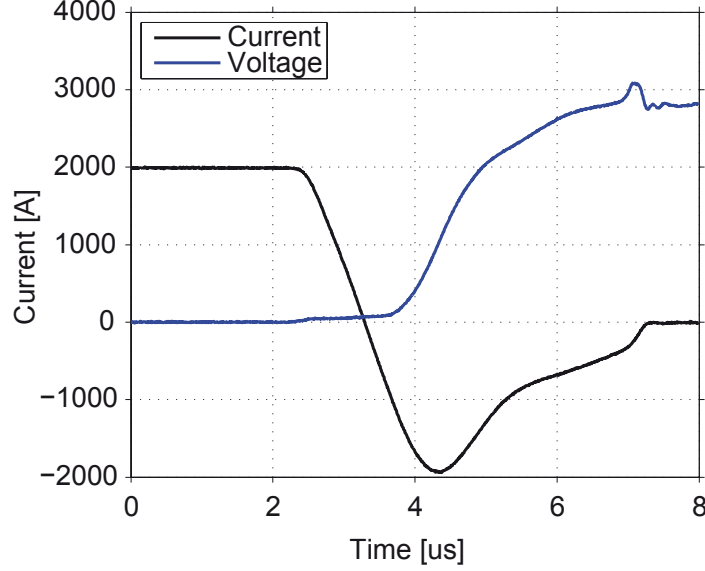


Figure 32: The resulting current and voltage waveform of a reverse recovery measurement on the StakPak diode [24].

not given in the datasheet of the component and is therefore set to $V_j = 1$ V, see Section 3.3.1. Both the series resistance R_s and the saturation current I_s are estimated from a comparison between the forward characteristics in the datasheet. R_s represents the slope of the forward voltage drop and I_s is calculated as

$$I_s = I \exp\left(\frac{-V}{nV_T}\right) \quad (46)$$

where V_T is the thermal voltage of the diode. All initial parameters are presented in Table 6.

Table 6: Initial Lauritzen model parameters from parameter extraction.

τ	T_M	V_j	n	R_s	I_s	$Cj0$	F_c	m_j
14.27 μ s	5.71 μ s	1 V	2	400 $\mu\Omega$	22.0 μ A	1 nF	0.5	0.5

5.2.1 Simulation build-up and model tuning

The Lauritzen model is usually implemented in Pspice or similar circuit simulation software, however in this case the model was implemented in Matlab/Simulink. The model equations were integrated into a Simulink

component block using Simscape language, which enables programmable blocks in Simulink.

In order to evaluate the performance of the implementation in Simulink and the parameter extraction, a reverse recovery simulation was compared with measurements received from the manufacturer. To understand the behaviour of each parameter on how they affect the shape of the reverse recovery waveform, a parameter sweep were performed. Increase of parameter T_M , changed the negative reverse recovery current peak I_{RM} accordingly. In the same way, the model parameter τ alters the reverse recovery time constant τ_{rr} . Change of τ also resulted in small variations in I_{RM} . If the junction capacitance $Cj0$ were decreased, the recovery from the negative current peak started to oscillate. For visualization of these relationships, see Figure 33. Parameter sweep of the remaining model parameters did not have any influence on the reverse recovery response of the simulation.

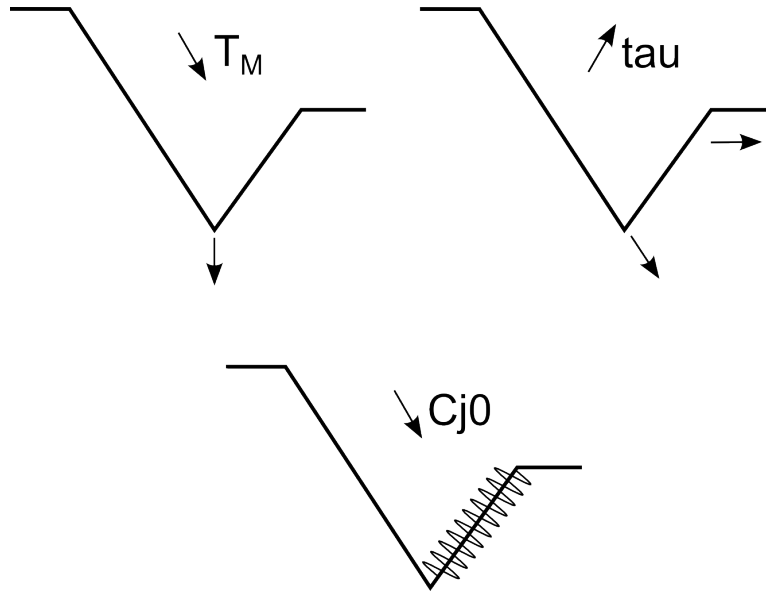


Figure 33: Simulation response when different parameter sweeps on T_M , τ and $Cj0$ were performed.

To reduce the simulation model error, the knowledge gained from the parameter sweep was used to refine the model. The error reduction turned out to be a trade off between accuracy of the reverse recovery current peak value, and the reverse recovery time constant, τ_{rr} . If τ was increased in order to fit the measurement waveform better in the region after the current peak, it was not enough to only change T_M to compensate for the unwillingly increase of the reverse current peak.

The final parameters are presented in Table 7 and a comparison between

simulation and measurement of a reverse recovery is displayed in Figure 34 and Figure 35. The accuracy of the simulation model is not perfect, a slightly deviation after the reverse current peak occur. However, as mention above, it was difficult to adjust both the peak and the recovery after the peak. The value of τ_{rr} in the simulation is $3.75 \mu s$ in comparison with $4.08 \mu s$ in the measurement. The reverse current peak, I_{RM} was simulated to 1910 A in comparison with 1940 A found in the measurement.

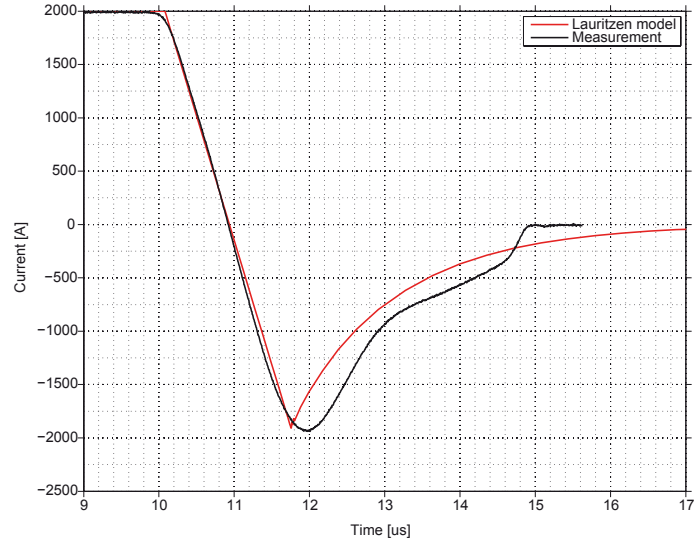


Figure 34: Simulation and measurement waveform of a reverse recovery case when the component is switched of from 2000 A.

For the forward characteristics of the Lauritzen model, mainly R_s , I_s and n affects the accuracy compared to measurements. The model is mainly developed for simulation of different switching applications, therefore are the parameters in this thesis tuned for normal operational current levels at 125 degrees and later compared with measurements on surge current level. During test of the forward characteristics, smaller changes in the parameters was necessary to reduce the deviation. Simulation response is presented in Figure 36. The model accuracy is not perfect, which indicates that the StakPak diode has more exponential behaviour that is hard to cover with this model. At higher current levels, the deviation increases which is expected for the Lauritzen model. This is displayed in Figure 37, where the simulation result is compared with measurement data. However, how much it affects simulations of device temperature will be investigated further in the following sections.

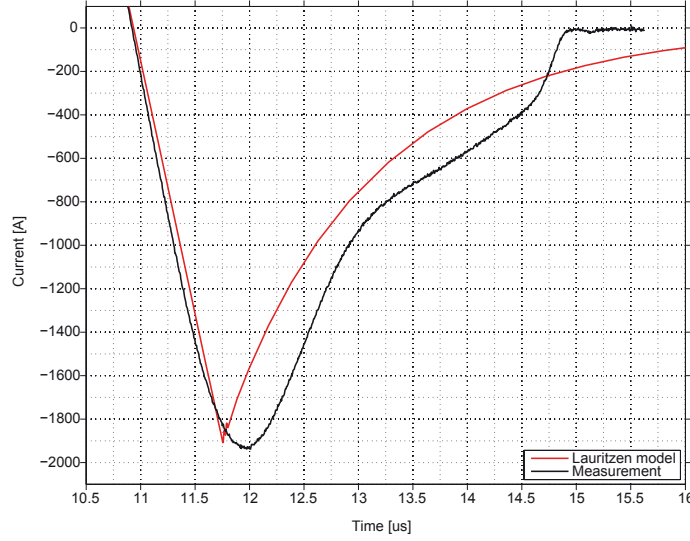


Figure 35: The simulated reverse recovery deviate from the measurements, however both the reverse peak and the reverse time constant are within reasonable values in comparison with the measurement.

Table 7: The final Lauritzen model parameters after tuning of the simulation performance for both reverse and forward characteristics.

τ	T_M	V_j	n	R_s	I_s	$Cj0$	F_c	m_j
$3.28 \mu s$	$2.0 \mu s$	$0.7 V$	2.54	$445 \mu \Omega$	$34.7 \mu A$	$1 nF$	0.5	0.5

5.3 Extrapolation of Measurement Data

During a fault in the HVDC station, according to Section 5.1 the surge current through the diodes can reach up to 15.4 kA. After contact with the manufacturer, a diagram of how the forward voltage drop depends on current up to 13 kA for two temperatures $25^\circ C$ and $125^\circ C$ was provided. To determine the voltage drop for greater currents up to the maximum surge current of 15.4 kA, extrapolation of measurement data was necessary. By using polynomial curve fitting technique, the two measurements from the datasheet were extrapolated with a polynomial of the sixth degree up to 16 kA.

To be able to simulate the diodes behaviour in temperatures besides the two measurement temperatures $25^\circ C$ and $125^\circ C$, approximations of the temperature dependency were made. The diode is assumed to increase its forwards voltage drop linearly between $25^\circ C$ and $125^\circ C$ and for all currents up to the maximum of the model of 16 kA, the linear increase can be seen

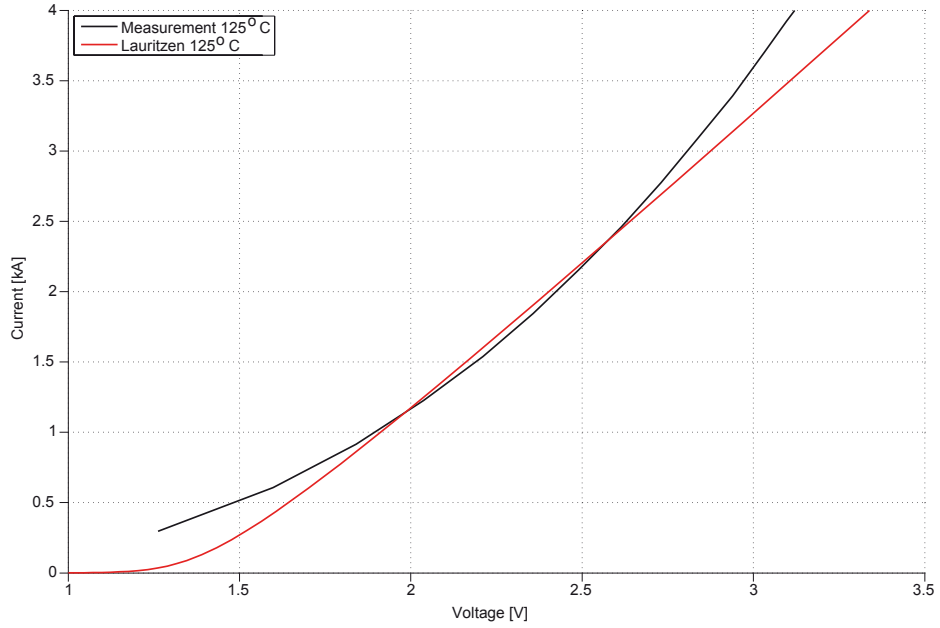


Figure 36: The simulation model is tuned in to fit the measurements within normal operation current levels, which is the normal procedure for the Lauritzen representation.

in Figure 38.

For temperatures above 125°C , three different possibilities exists that are visualised in Figure 39: the forward voltage drop continues to increase with the temperature (positive temperature coefficient), the forward voltage drop decreases (negative temperature coefficient) or the forward voltage drop stabilise for all above temperatures until the destruction of the diode. According to Section 3.2.2, the temperature coefficient is dependent on the current density of the surge current and the temperature of the diodes. Since no data about the diode manufacturing and parameters used in the case is provided from the manufacturer, no single possibility can be determined to be correct. Thus, all three possibilities will be investigated.

For the case when the voltage drop continues to increases with the temperature, the rate of increase is considered to be linear for the whole temperature range. The temperature coefficient is calculated from the two measurement curves for 25°C and 125°C , and the resulting voltage drop model can be seen in Figure 40.

Using the same assumptions as for the case when the voltage drop is considered to be increasing, the temperature coefficient for the case when the voltage is decreasing becomes the same but negative. In this case, the voltage

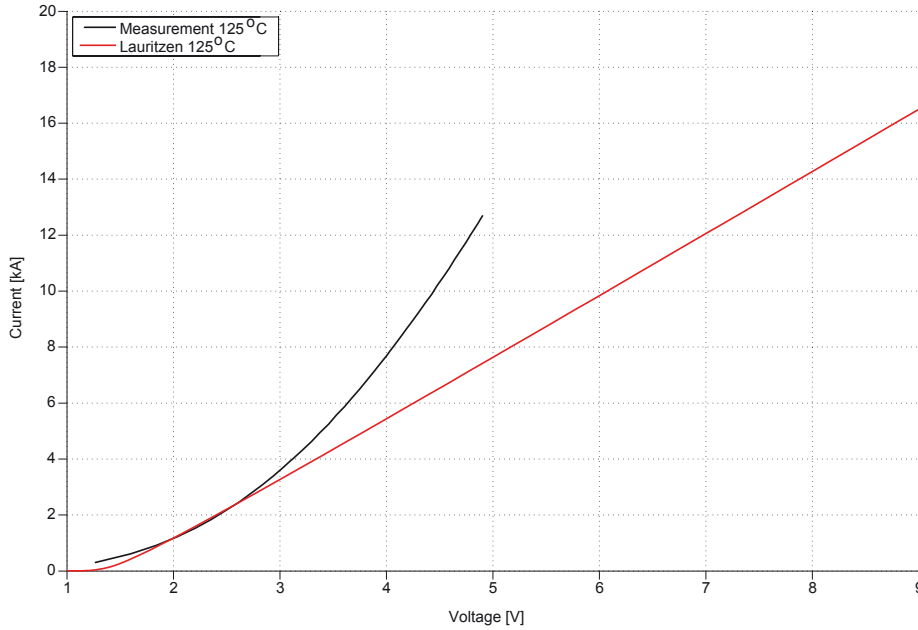


Figure 37: When the simulation result for a surge current levels is compared with the component measurement it is clear that the model does not cope with these high currents very well.

decreases linearly from 125° C until the maximum simulation temperature of 225° C. The corresponding voltage drop model can be seen in Figure 41.

The third case is when the voltage drop is assumed to stabilize at 125° C. All temperatures above is considered to have the same properties as the measurement curve for 125° C. The voltage drop increase between 25° C and 125° C, is as the two previous cases still assumed to be linear.

5.4 Thermal Model Parameters

Since no measurements were conducted for this thesis, the thermal impedance data from the manufacturer's datasheet was used. This data was defined between the virtual junction of the diode chip and the casing of the package. Based on (41), the data was implemented for a Foster thermal model of the fourth-order. Using (42), the corresponding absolute thermal capacitance value was calculated for implementation in the electrical circuit representation and are presented in Table 8 alongside the model parameters for the absolute thermal resistance values.

The Foster model can in some simulation situation have problems converging compared to a Cauer based thermal model. To improve the simulation stability, the Foster model parameters were converted to parameters for

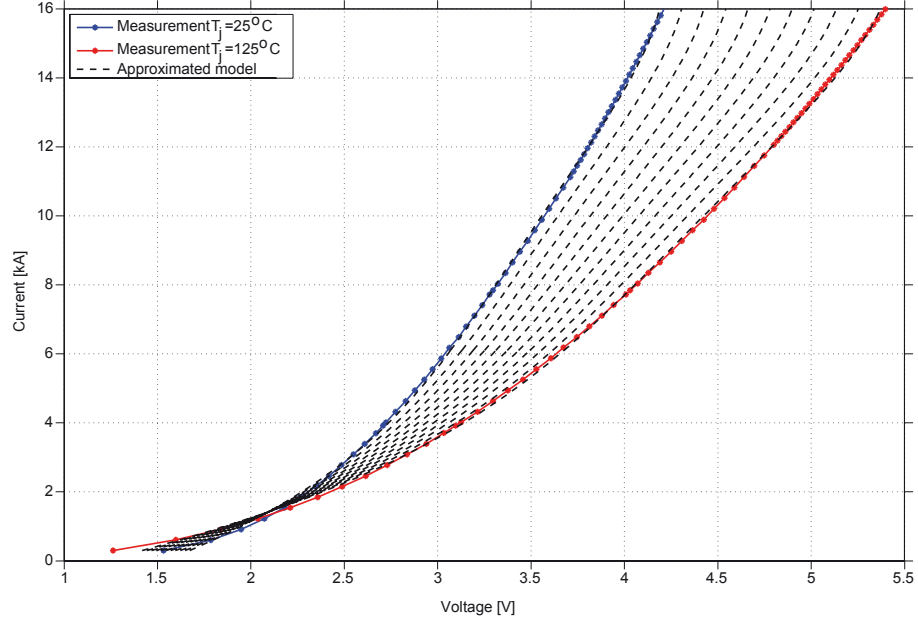


Figure 38: The approximated temperature dependency between 25°C and 125°C in steps of 10°C . The figure also shows the resulting extrapolation of the measurement data from 13 kA to 16 kA

Table 8: Foster model parameters

i	1	2	3	4
R_i [K/kW]	1.606	1.759	0.357	0.001
C_i [kJ/K]	0.3636	0.0335	0.0168	0.0031

a Cauer model described in Section 3.4.2. The result of the conversion are presented in Table 9, and the thermal impedance curve from the two models, Cauer and Foster, are presented in Figure 42.

Table 9: Cauer model parameters

i	1	2	3	4
R_i [K/kW]	0.5167	0.6997	1.5762	1.2524
C_i [kJ/K]	0.0024	0.0114	0.0250	0.4227

During the simulation, the case temperature is considered to be at constant

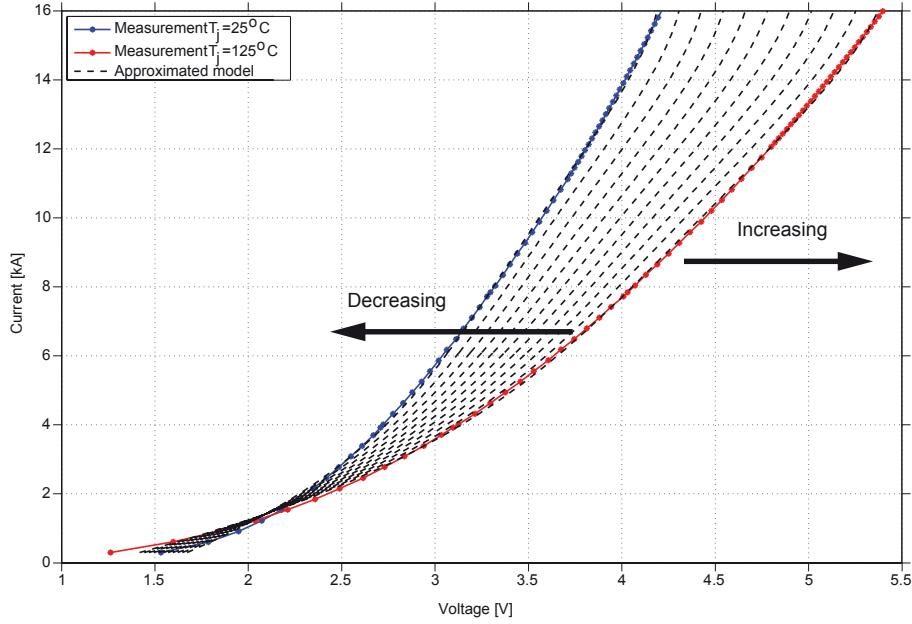


Figure 39: Three possible cases how the temperature coefficient changes for virtual junction temperatures above 125°C .

temperature. This is an approximation that the later simulated surge current will have short duration, for longer periods of surge currents would a thermal model including the cooler could be more appropriate. The initial value is based on the initial steady-state temperature of the virtual junction in the diodes. Using (3) and the rated power and voltages of the HVDC-link described the case set-up 4, the average current in steady-state operation through the diodes in one valve arm I_{diode} , can be determined to be 869.8 A. The corresponding power loss in the diodes can be expressed as

$$P = U_{diode} I_{diode} = R_{diode} I_{diode}^2 \quad (47)$$

and was determined to be 0.984 kW. R_{diode} was calculated from the typical diode characteristic values retrieved from the datasheet for a temperature of 125°C [23]. Using (39) and the worst case diode virtual junction temperature from the case set-up, the case temperature was determined to be 121°C .

5.5 Thermal Response of Fault Current through the Diode

The semiconductor diodes in the HVDC-valve experience thermal stresses when exposed to a surge current. According to Section 5.1, fault F3 and fault

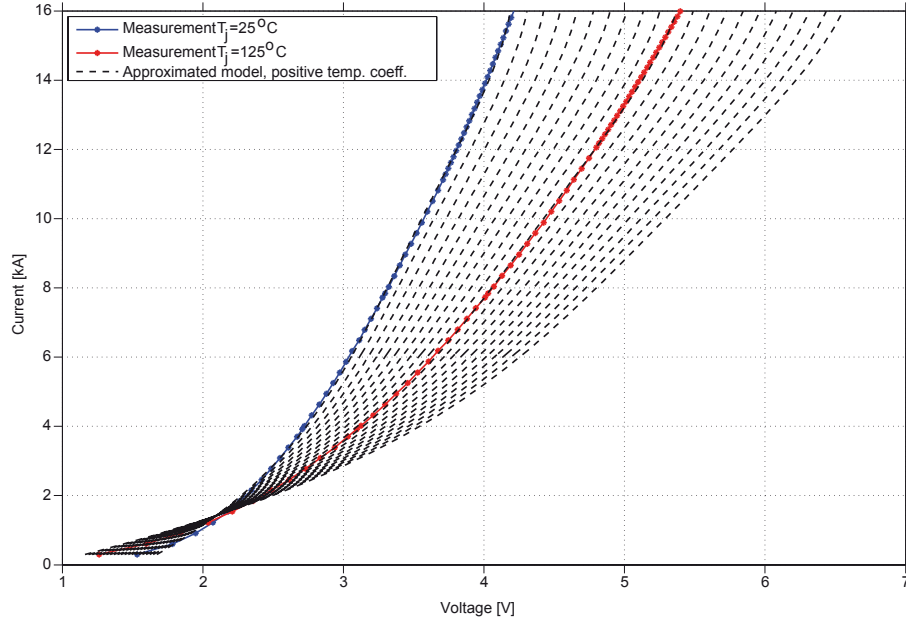


Figure 40: The approximated temperature dependency between 25°C and 225°C in steps of 10°C . In this case the temperature coefficient is assumed to be positive.

F4 in Station 1 during rectifier operation results in the largest surge currents through the valve arm components. To determine the thermal stresses on the diodes, the two corresponding surge current waveforms retrieved from system simulations described in Section 5.1.3 are used in the diode models that are described in Section 5.2 and Section 5.3. For the extrapolated diode model, all three possibilities regarding temperature coefficient are considered and the resulting virtual junction temperatures are presented in Figure 43 and Figure 44. The Lauritzen based model operates with a constant temperature and the resulting thermal waveform is also presented in Figure 43 and 44. Both diode models uses the thermal model and properties described in 5.4.

For the surge with the lower peak, fault F3, the simulation result shows three distinct levels of temperature response. The simulation model that has the lowest temperature response, is the extrapolated model with fix temperature dependency at 25°C , which reaches a temperature of 143.9°C . The three other versions of the extrapolated data are more or less coherent and reaches a peak of 148.1°C . The model that resulted in the highest temperature peak was the Lauritzen model that reached 153.3°C . To be noticed is that all the three peaks are within a range of 10°C . At the second peak, the simulated

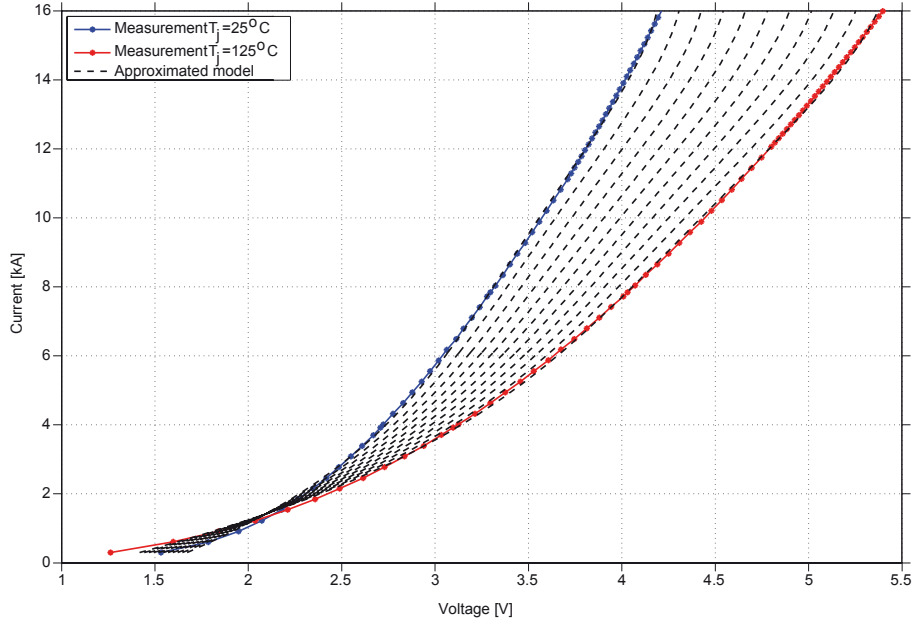


Figure 41: The approximated temperature dependency between 25°C and 225°C in steps of 10°C . In this case the temperature dependency is considered to be negative.

temperature range is even smaller.

Fault F4 corresponds to the largest valve current surge and the simulated temperature response is less coherent than for previous fault case. Once again, the Lauritzen model reached the highest temperature of 216.3°C and 242.6°C . In this fault case, the temperature of the diodes reaches their maximum at the second peak. This indicates that the loss energy in the diode does not dissipate fast enough before the second peak occurs. The difference between the extrapolated model versions are in this case noticeable, but they are still in the same order. The lowest model version has a peak of 172.5°C and 188.6°C , which is 54°C lower than the Lauritzen simulation result. The maximum temperature of 242.6°C is high above the rated temperature of 125°C , which affects the component in different ways. Due to different thermal coefficients in the diode, fast temperature transients results in tension and fatigue between the different materials. These tensions introduces reliability risks and the transients could in worse case lead to cracks in the material. Higher temperatures also results in degradation described in 3.2.3.

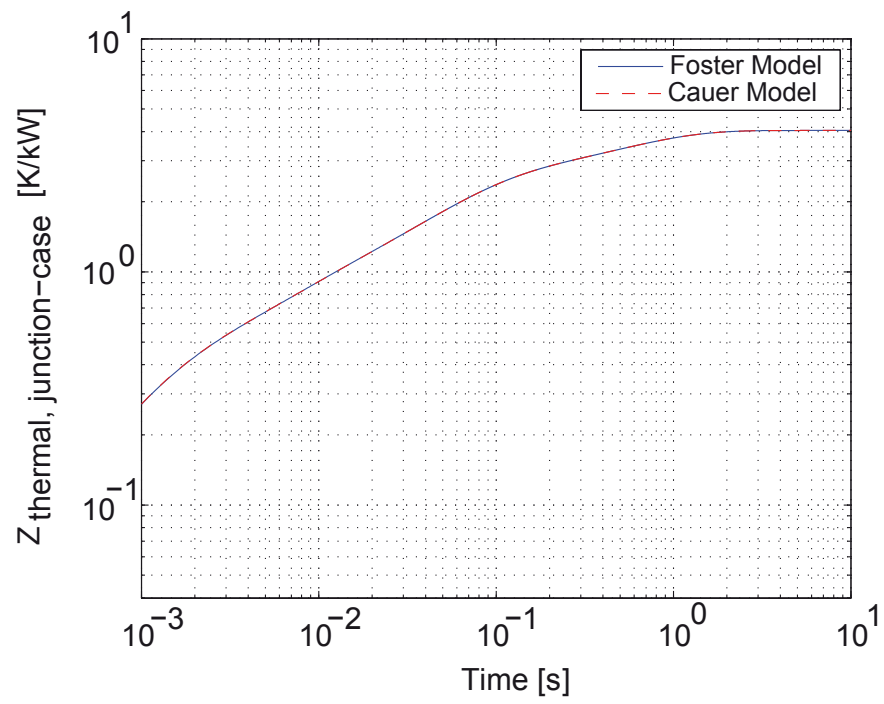


Figure 42: Thermal impedance curve based on datasheet values [23] for both the Foster and the Cauer model.

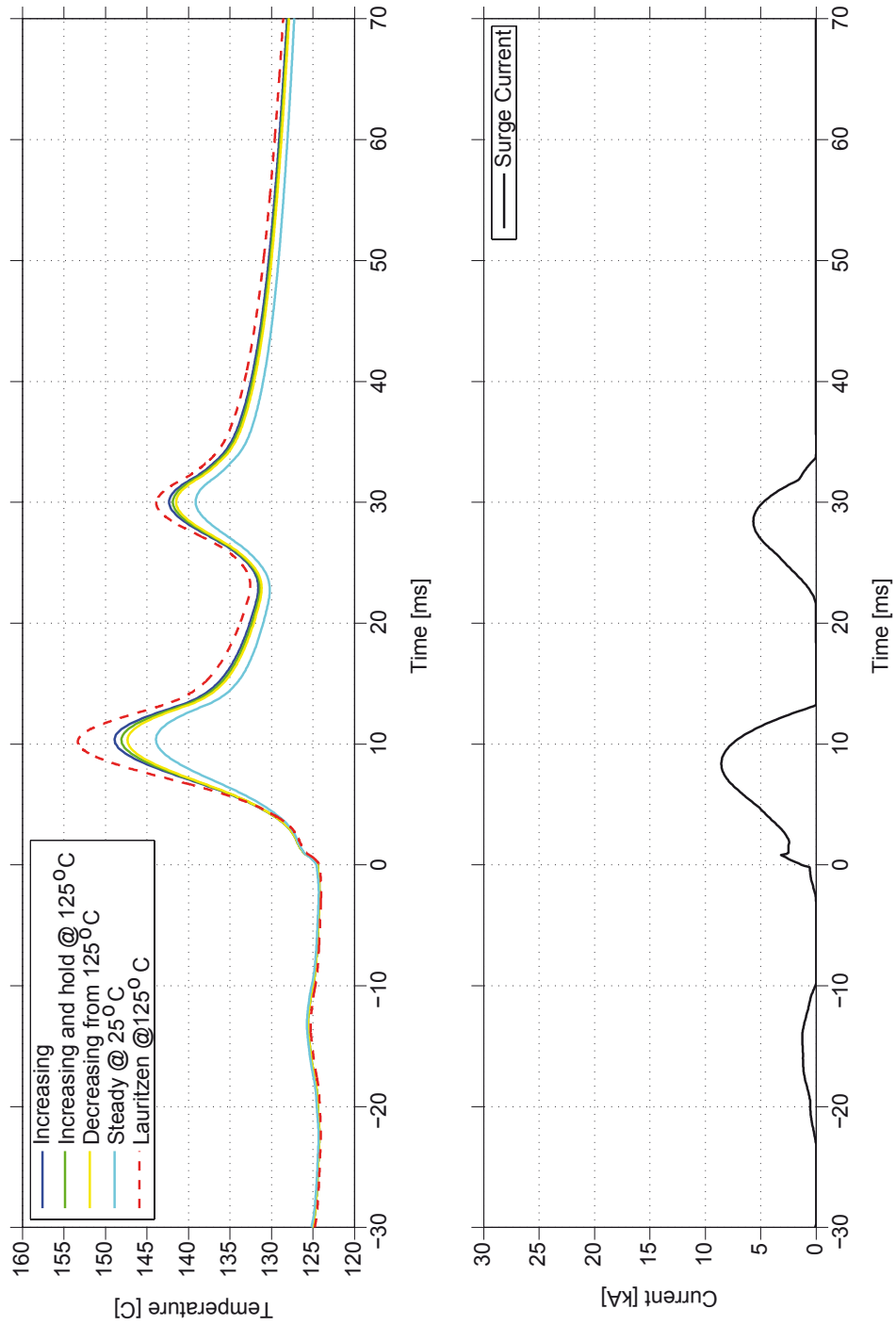


Figure 43: Junction temperature of the diode in the HVDC-valve during resulting surge current from fault F3.

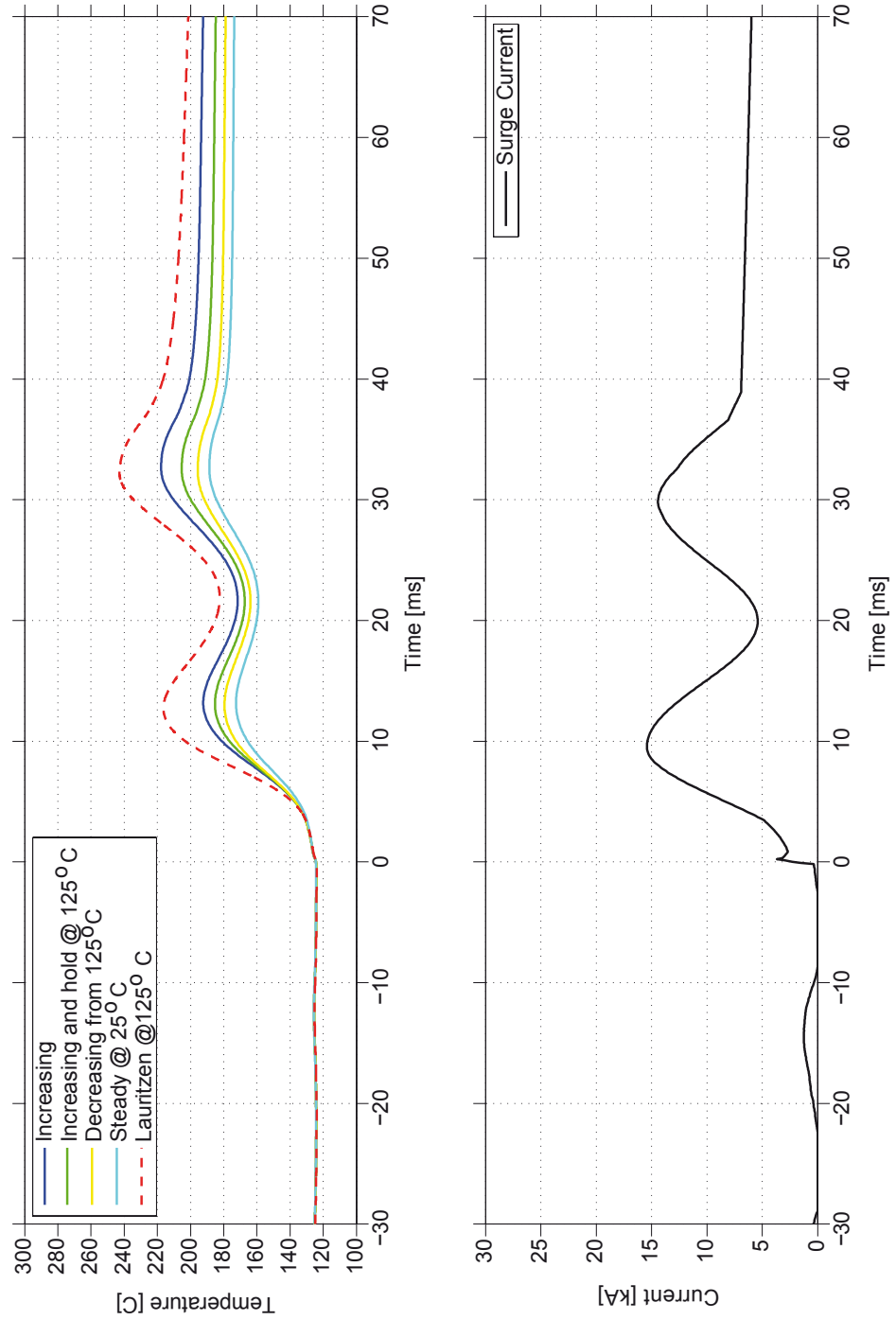


Figure 44: Junction temperature of the diode in the HVDC-valve during resulting surge current from fault F4.

6 Conclusions

This thesis has shown how a surge current fault event in a VSC HVDC-station based on MMC topology affects the temperature of the semiconductor diodes in the converter valve. In order to determine the worst case fault currents with aspect of the converter components, a typical HVDC-link is described and modelled in PSCAD simulation software. Analytical calculations were performed in order to confirm the simulated fault current peak values. To be able to evaluate the temperature change during the surge current event, two types of voltage drop models are presented alongside the parameter extraction process. In conjunction, a thermal model of the diode casing, based on the Cauer type of equivalent electrical network was implemented. In the end, the temperature response of two most severe fault currents from the fault analysis were simulated, combining the thermal model and the voltage drop models.

The performed fault analysis on the HVDC-system case have shown that analytical calculations of an MMC-based station during fault are not an easy task and further refinement of the approximated equations are needed. The simulated peak values deviates slightly from the analytical values, but are still in the same region. The investigation has shown that faults occurring on the DC-side of the converter are the most severe with aspect of the converter semiconductor components, especially pole-to-pole fault. The operation mode of the converter, rectifier or inverter, has shown to have small impact on the resulting surge current peak.

From the simulations, the resulting junction temperature of the StakPak component shows that the Lauritzen diode model is performing rather well compared to the extrapolated measurement model. Even though the Lauritzen model is developed for switching investigations during steady-state operation. On the other hand, for higher current levels, this model starts to deviate from the measurement model and is more likely to lead to an overestimation of the heat generated in the component during surges. This could result in unnecessary design margins, increased cost and size of the system. Similar conclusion is valid for the extrapolated model, all versions shows a coherent results for low surge current levels but for higher currents the result starts to deviate. This means that the temperature swing is not affecting the outcome of the thermal simulations in low surge currents, but when the current reaches higher current levels, the detailed temperature dependence starts to be important. The results have not clearly shown that one temperature swing approximation is more correct than the others, and must be verified with measurements in these high current, high temperature range. An other aspect that requires detailed knowledge of the temperature coefficient behaviour, is the risk of thermal runaway when several diodes

with negative coefficient are connected in parallel.

The thesis has shown that if the Lauritzen diode model already exist, the model is a good start for electro-thermal study of the component. However, the parameter extraction process and model tuning is a time consuming task, but still results in a rather simple forward voltage drop characteristic. Therefore, it is more time efficient to perform more measurements in order to build a reliable voltage drop model for simulations of thermal response during surge currents. This method is preferable if the surge current reaches several orders higher than normal steady-state operation.

6.1 Future Work

To further develop the study performed in this thesis, new measurements of the Stakpak component regarding temperature dependent forward characteristics are needed. These type of measurements are not easy to perform, when both high surge currents and temperatures are investigated. With more detailed measurements, the estimated temperature characteristics could be investigated further and improve the model accuracy.

The thesis has also shown that the Lauritzen diode model, developed for switching applications, can be used for estimation of the component stresses rather efficient. But, more detailed and advanced physic based model exists, for example Hefner or Kauer diode model. These models are designed for very high injection levels of power diodes, which occurs during surge currents. The drawback is that these type of models demands a high number of design parameters and component details in order to be created. On the other hand, it could be used to verify the estimated temperature characteristics in this thesis. This was mainly not performed in this thesis due to lack of components specifications and the time frame of the project.

The simulation results from the fault analysis differed slightly from the implemented analytical calculation tools. Therefore, further refinements of the analytical equations of an MMC-based HVDC-converter during fault are needed in order to get a better match with simulation results.

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