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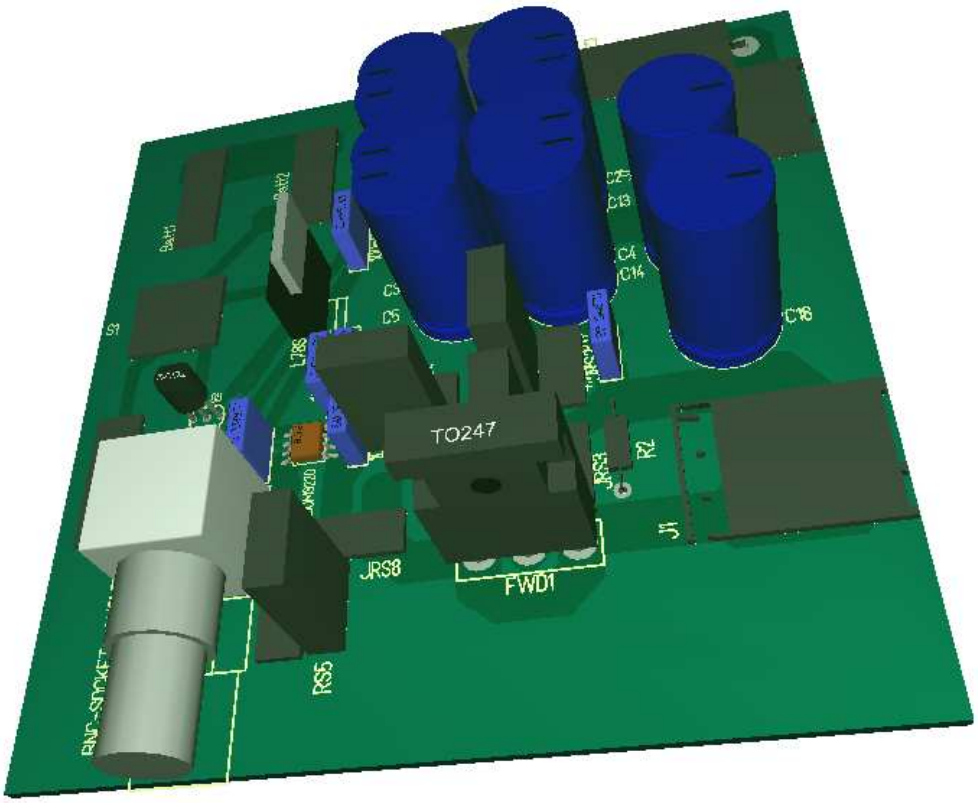

Experimental evaluation and modeling of the thermal behavior of a TO-247 Mosfet

Master of Science Thesis

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Department of Energy and Environment
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2013

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Cover:
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Abstract

In this thesis, analytical modeling of a MOSFET as well as investigation of its gate drive was performed. Firstly, the performance of the gate drive circuit during switching mode was tested. In order to do so, four simple case set-ups consisting of RC circuit were switched by the gate drive. For the first case a large resistor and small capacitor was selected ($C = 2.2nF$, $R = 4.7\Omega$). For the second case a small resistor and small capacitor were selected ($C = 2.2nF$, $R = 1\Omega$). For the third case a large resistor and large capacitor were selected ($C = 10nF$, $R = 4.7\Omega$). For the fourth case a small resistor and large capacitor were selected ($C = 10nF$, $R = 1\Omega$). The results in these four cases were in agreement with the results from the simulation test set-ups.

The next step was modelling a MOSFET thermally using PLECS/Simulink. The analogy between the electrical and thermal components was used to obtain thermal equivalent circuit diagrams. The sources of power dissipation which was generated by the device was expressed as $P = I * V_{TJ}$ which correspond to current sources, and RC elements were used to represent the thermal impedances Z_{th} of the MOSFET which could be obtained from the manufacture datasheet. The energy losses of all internal components in the module would be dissipated through the thermal impedance Z_{th}.

The power dissipated in the MOSFET in DC operation mode, which was generated by conduction losses (P_c), was calculated by multiplying the square of the root mean value of the drain current by the on-state resistor. In this experiment, the first power supply was used to control the drain current through the MOSFET while the second power supply was used to keep the MOSFET on by supplying a DC source at the gate pin. The power dissipation and the ambient temperature was measured for each value of the drain current.

The temperature was measured by using a resistor sensor. The tip of one thermocouple was attached to the MOSFET while the other thermocouple was positioned approximately 10 cm away from the device to measure the ambient temperature in the vicinity of the MOSFET device.

The temperature measurement circuit was designed and then the PCB was built and analyzed in the simulation software Target. After that the PCB was ordered. Three case set-ups were studied. For the first case the MOSFET without heat sink was tested. The case temperature was measured and compared with the simulation results. For the second and third tests the MOSFET was screwed onto a small and big heat sink respectively. In the third and fourth test a thermal isolation pad with thermal resistance of $3\frac{^\circ C}{W}$ was put between the MOSFET and heat sink. The case temperature, heat sink temperature, and ambient temperature were measured. The measurement results were in agreement with the results from the simulation test set-ups.

Index Terms: Gate drive circuit, MOSFET thermal modeling, junction temperature, losses calculation.

Acknowledgements

This work has been carried out at the Department of Energy and Environment at Chalmers University of Technology. First and foremost, I would like to express my sincere gratitude to my examiner Professor Torbjörn Thiringer for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of experiment and writing of this thesis while allowing me the room to work in my own way.

Besides my advisor, I would like to thank my supervisor Ali Rabiei for his encouragement, insightful comments, best suggestions.

My sincere thanks also goes to Christian Dubar for many fruitful discussions and his technical guidance.

I would like to thank Robert Karlsson and Magnus Ellsen for providing me the devices and equipments in the laboratory.

Last but not least I would like to thank my wife Basma Tuama, for her love, encouragement, and understanding.

Ibrahim Malik Al-janabi
Göteborg, Sweden, 2013

Contents

Chapter 1

Introduction

1.1 Problem background

The implementing of silicon carbide (SiC) offers high speed switching, high temperature and low size. Many researches began from the last decade to improve the viability of SiC technology. The losses and junction temperature of the device are very important issues in any converter design. This can be improved by using a high switching speed device such as a SiC. However, a main limitation is the stray inductances in the circuit and EMI restriction. The main limitation of the semiconductor devices capability is the increase of the power dissipation. In other words, the maximum current and power capability of semiconductor devices are limited by the maximum junction temperature of the device. The junction temperature increases beyond the specific limit due to the switching losses and conduction losses of the semiconductor devices. Both the electrical and thermal optimization are needed in order to know electrical and thermal properties of power electronics system. Often the simulation of the semiconductor device is made at a fixed and static temperature. However, this might not be a suitable approach since many features of the semiconductor device is strongly depending on the temperature. Therefore, the temperature is one of the vital parameters to predict the behaviour of the system [16]. The junction temperature and cycling temperature are important parameter to maintain the lifetime of the device. The junction temperature is affected by many component parameters. Thus, the device could be permanently damaged, if the junction temperature exceeds the maximum value. For most converters, the switch is required to turn ON/OFF at the entire load current which gives high switching losses due to large $\frac{di}{dt}$ and $\frac{dv}{dt}$. As a result, electromagnetic interface (EMI) is produced. So it is a trade-off between the EMI behaviour and the thermal optimization of the device.

The percentage of the total heat that flows out through the MOSFET device is important to know. This importance is due to that it affects the amount of the current that can be successfully switched through the MOSFET. Guaranteeing a low on-state resistance and better flow of heat away from the junction will ensure the reliability and performance of the MOSFET as a switch device.

1.2 Purpose of the work

The first aim of this thesis is to verify the experimental results with the simulation results of the thermal model of a MOSFET. The accurate calculation of the temperature is needed to make an integrated effort between the thermal and electrical design aimed at verifying loss calculation theory. Moreover, a target is to make thermal measurement on a MOSFET and compare the result with the simulation result of the thermal model. Moreover, using different sizes of heat sinks, these will be used to quantify the effect of cooling on the MOSFET. In addition, an objective is to calculate the power dissipation for different drain currents. It is also studied how the temperature act back on the junction temperature and drain-source resistance. Last but not least, an important aim of this work is to design as much accurate temperature measurement circuit as possible to measure the case, heat sink, and ambient temperature.

Chapter 2

Technical background

2.1 Metal-Oxide transistor(MOSFET)

2.1.1 Operating principle

The MOSFET transistor is a majority device which means that there are no excess minority carriers that must move in or out the device during ON/OFF switching. Therefore, the MOSFET device is faster than a bipolar device [26]. For the MOSFET transistor there is a stray capacitance and depletion layer capacitance which can be modelled as shown in Fig. 2.1. Therefore, a current is needed to charge and discharge the capacitor during turn-on and turn−off. The peak value of this current is limited by the gate resistance and last only during the charging or discharging of the gate capacitance.

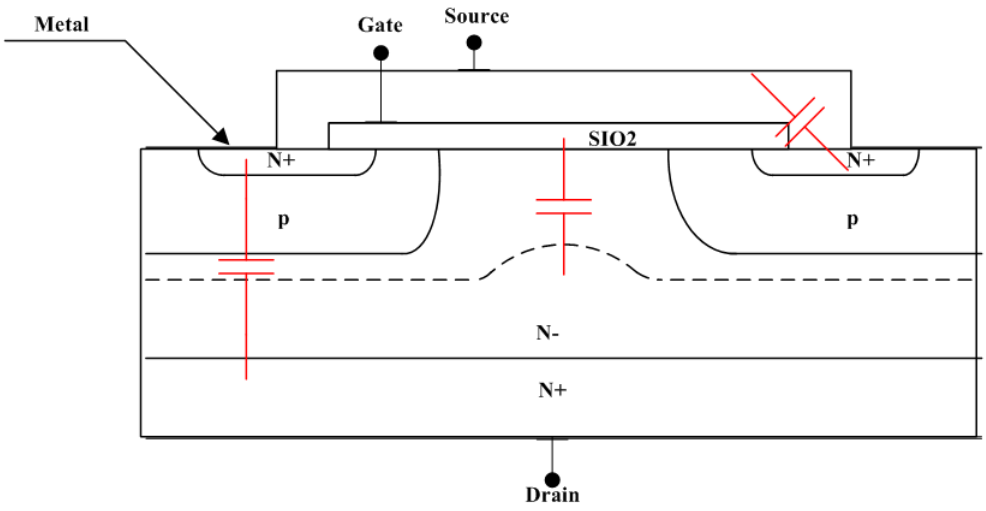
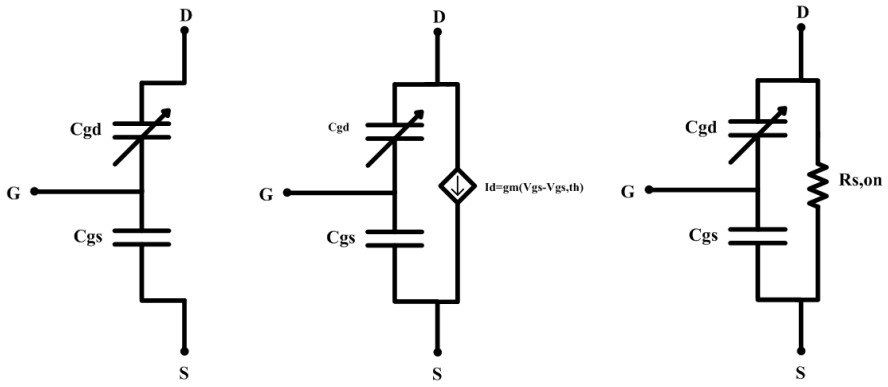


Fig. 2.1 Cross section view of n-channel MOSFET

Three important capacitances inherent in a MOSFET structure is shown in Fig. 2.2. The most prominent capacitor in a MOSFET structure is formed by the gate oxide layer between the gate metallization and the n+ type source region. It has the largest value (a few nano farads) and remains more or less constant for all values of v_{gs} and v_{ds}. The second largest capacitor (a few hundred pico forwards) is formed by the drain body depletion region directly below the gate metallization in the n- drain drift region. Being a depletion layer capacitance its value is a function of the drain-source voltage v_{ds}. For low values of v_{ds} ($v_{ds} < (v_{gs} - v_{gs,th})$ the value of c_{gd} (c_{gd2}) is considerably higher than its value for a large v_{ds} as shown in Fig. 2.7. Although the variation of c_{gd} between c_{gd1} and c_{gd2} is continuous, a step change in the value of c_{gd} at $v_{ds} = v_{gs} - v_{gs,th}$ is assumed for simplicity. The lowest value capacitance is formed between the drain and the source terminals due to the drain body depletion layer away from the gate metallization and below the source metallization. Although this capacitance is important for some design considerations (such as



(a) Cutt-off region (b) Active region (c) Ohmic region

Fig. 2.2 MOSFET equivalent circuit during various ON modes

snubber design, zero voltage switching etc) it does not appreciably affect the 'hard switching' performance of a MOSFET. Consequently, it will be neglected in our discussion. From the above discussion and the steady state characteristics of a MOSFET, the circuit models of a MOSFET in the three main modes of operation can be drawn as shown in Fig. 2.2 [26].

The most significant change in capacitance is the change in the gate-drain capacitance c_{gd} due to the change in the voltage v_{gd}. The capacitance c_{gd} is the capacitance of the oxide layer in series with the depletion layer. A varying voltage v_{gd} will change the length of the depletion layer and thereby also the capacitance c_{gd}.

2.1.2 MOSFET switching

There are many factors that affect the switching behaviour of a MOSFET transistor such as stray capacitances, switching frequency, etc. A step down converter is used to investigate the behaviour of the MOSFET transistor switching. Many assumptions are considered for simplicity. The free-wheeling diode D_f is assumed to be ideal which means that there is no reverse recovery current. Furthermore, the load current is assumed to be constant during the short switching interval. Finally, the gate drive circuit is assumed to be a step voltage source to give a voltage step between zero and V_{GG} in series with the gate resistor R_G in Fig. 2.3 [5].

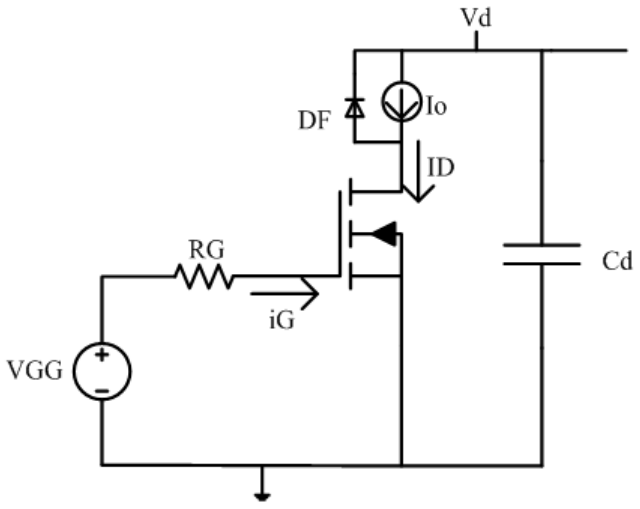


Fig. 2.3 Step-down converter

•Turn−on procedure

To turn the MOSFET transistor on, the gate drive voltage (v_{gs}) switches from 0 to +V_{GG}. The input capacitance c_{gs} is charged from 0 to $v_{gs,th}$. The equivalent circuit for the MOSFET transistor during this interval is illustrated in Fig. 2.4. When the gate drive voltage change from 0 to V_{GG}, there is an inrush gate current which can be expressed as [28]

$$i_g = \frac{V_{GG}}{R_G} \tag{2.1}$$

Where V_{GG} is the gate voltage (V), R_G is the gate resistor (Ω), and i_g is the gate current (A).

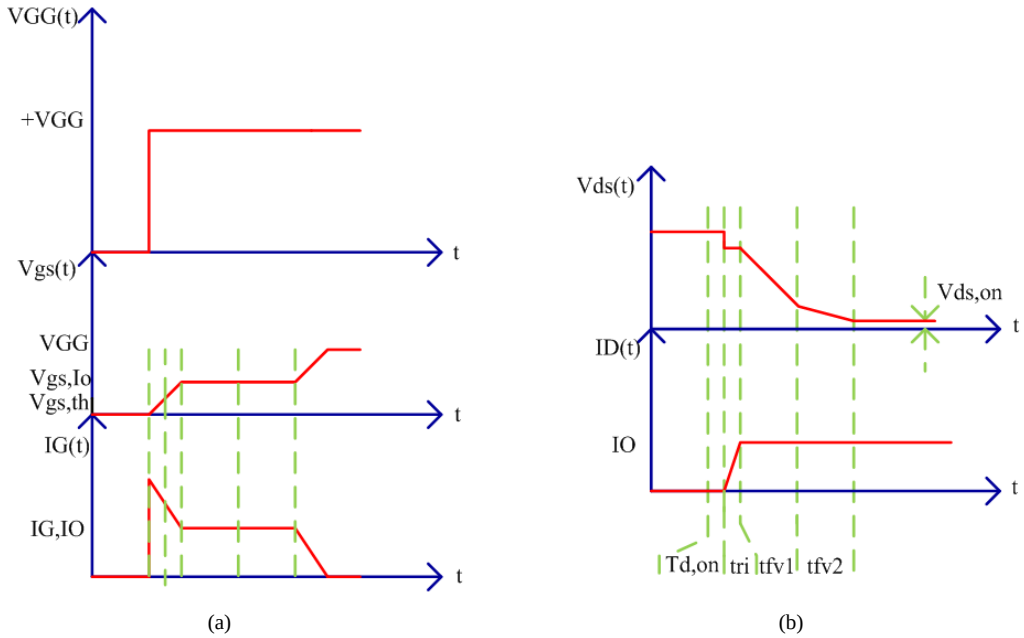


Fig. 2.4 Two MOSFET turn-on waveforms

Most of the gate current is flowing in the gate−source branch to charge the gate-source capacitance (C_{gs}). While, a small portion of this current is flowing through the gate- drain branch. As the voltage on C_{gs} increases, the voltage on C_{gd1} decreases slightly. The input equivalent circuit can be represented by a series combination of R_G, C_{gs} and C_{gd1} as shown in Fig. 2.5(a) [28].

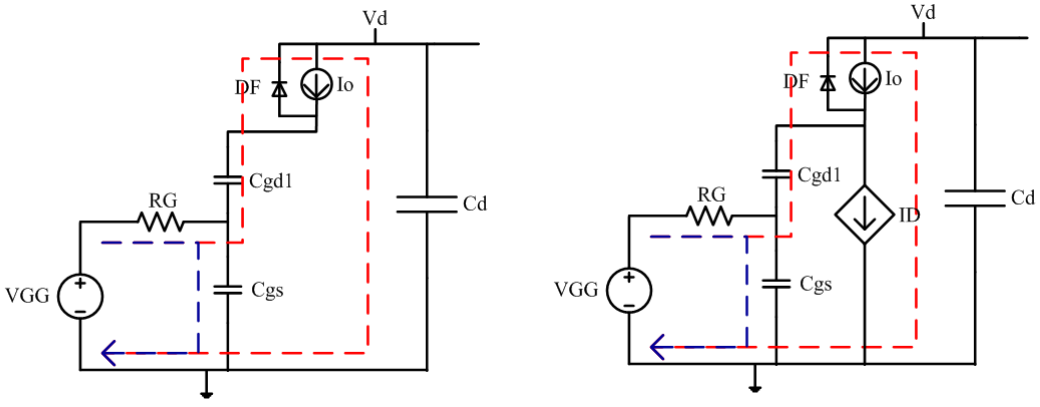
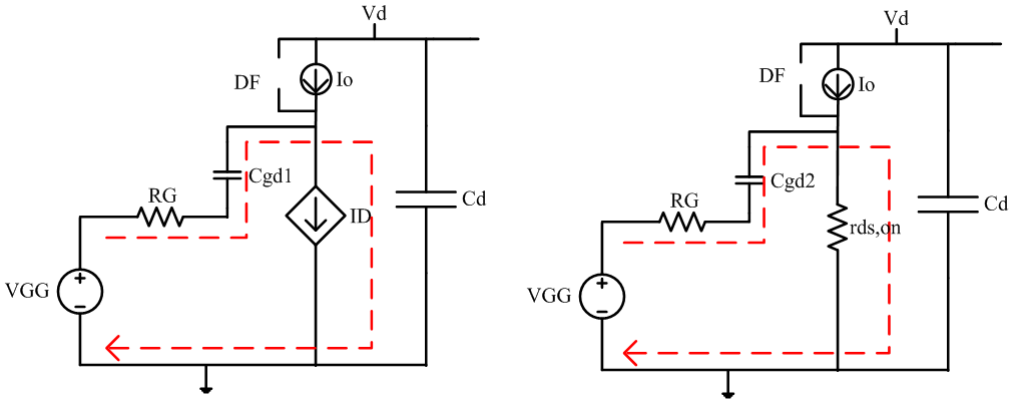


Fig. 2.5 MOSFET equivalent circuit



(a) Active region (b) Ohmic region

Fig. 2.6 MOSFET equivalent circuit

$$i_c = C_{in}\frac{dv_c}{dt} \tag{2.2}$$

where C_{in} is the equivalent of C_{gs} and C_{gd1}

$$C_{in} = C_{gs} + C_{gd1} \tag{2.3}$$

$$c_{in}\frac{dv_c}{dt} = \frac{V_{in} - v_c}{R_c} \tag{2.4}$$

As a result we can represent

$$\frac{C_{in}dv_{gs}}{dt} = \frac{V_{GG} - v_{gs}}{R_G} \tag{2.5}$$

This is a first order linear equation that can be solved by

$$v_{gs}(t) = V_{GG}(1 - \exp(-\frac{t}{\tau_1})) \tag{2.6}$$

where $\tau_1 = R_G(C_{gs} + C_{gd1})$. The voltage drop on the diode is zero because it is assumed that the diode is an ideal diode and the entire load current I_o is free-wheeling in the diode. While, both drain current and drain voltage are kept constant during this period. Therefore, this period is called a turn-on delay ($t_{d,on}$) [20].

$$t_{d,on} = -R_G(C_{gs} + C_{gd})\ln(\frac{V_{GG} - v_{gs,th}}{V_{GG}}) \tag{2.7}$$

At $v_{gs}(t) = v_{gs,th}$, i_d starts to increase and now the MOSFET enters the active region area where the equivalent circuit shown in Fig. 2.5(b) will apply. The gate voltage v_{gs} will continue to increase as before. Then , the drain current (i_d) starts to rise as a function of v_{gs} as it is given in below equation [26].

$$i_d = g_m(v_{gs} - v_{gs,th}) \tag{2.8}$$

At the end of this interval, the corresponding value of v_{gs} is $v_{gs,Io}$ and I_G is $I_{G,Io}$ as illustrated in Fig. 2.4. The total time it takes for i_d to reach I_o is,

$$tv_{gs,Io} = -R_G(C_{gs} + C_{gd})\ln(\frac{V_{GG} - v_{gs,Io}}{V_{GG}}) \tag{2.9}$$

Hence the rise time of the current is

$$t_{ri} = tv_{gs,Io} - t_{d,on} \tag{2.10}$$

At the end of the rising time of the current, all the current has been transferred from the free-wheeling diode D_F to the MOSFET transistor. The drain current (i_d) cannot increase beyond the load current (I_o). Therefore, v_{gs} will remain clamped at the $v_{gs,Io}$ level and the voltage on C_{gs} will be constant as shown in Fig. 2.4. The MOSFET transistor equivalent circuit can be illustrate as shown in Fig. 2.6(a). While, the drain−source voltage v_{ds} begins to fall from its previous value v_d because the gate current I_G starts discharge (C_{gd}) [5].

$$I_G = -C_{gd}\frac{dv_{gd}}{dt} = -\frac{V_{GG} - V_{gs,Io}}{R_G} \tag{2.11}$$

The drain−source voltage can be expressed as

$$v_{ds} = v_{dg} + v_{gs} \tag{2.12}$$

As mentioned above, the gate−source voltage v_{gs} is kept constant in active region. The drain−source voltage falls from its initial value v_d to the $v_{ds,on}$.

So

$$\frac{dv_{ds}}{dt} = \frac{dv_{gd}}{dt} = \frac{V_{GG} - V_{gs,Io}}{C_{gd}R_G} \tag{2.13}$$

Solving the above equation yields

$$v_{ds}(t) = v_d - \frac{V_{GG} - V_{gs,Io}}{C_{gd}R_G}t \tag{2.14}$$

At the end of the this interval, the MOSFET transistor enters the ohmic region where the $v_{ds,on}$ can be expressed as

$$v_{ds,on} = I_o R_{on} \tag{2.15}$$

The decrease of drain-source voltage $v_{ds,on}$ from v_d to $v_{ds,on}$ has two intervals. In the first interval, the MOSFET transistor operates in active region where

$$v_{ds} > (v_{gs} - v_{gs,th}) \tag{2.16}$$

This can be seen in Fig. 2.7 the value of the C_{gd1} is small. Therefore, the fall time is short in this interval as shown in the following equation [5].

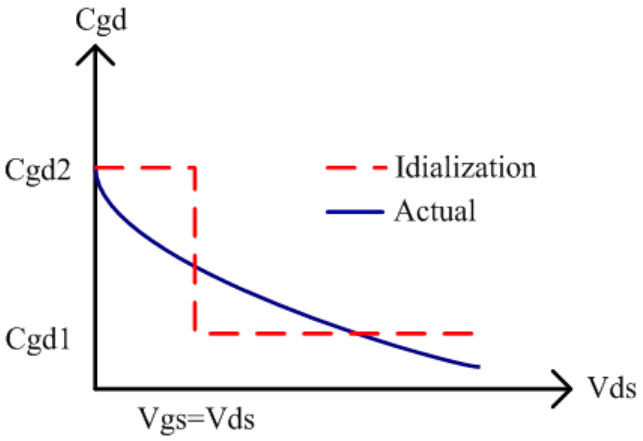


Fig. 2.7 Change of the gate-drain capacitor with the drain-source voltage

$$t_{fv1} = \frac{(V_d - v_{ds})C_{gd1}R_G}{V_{GG} - v_{gs,Io}} \tag{2.17}$$

While, when the MOSFET transistor enters the ohmic region, the falling of $v_{ds,on}$ is slower than before because $C_{gd2} \gg C_{gd1}$ as shown in Fig. 2.4 and the falling time is determined as

$$t_{fv2} = t_{on} - t_{d,on} - t_{ri} - t_{fv1} \tag{2.18}$$

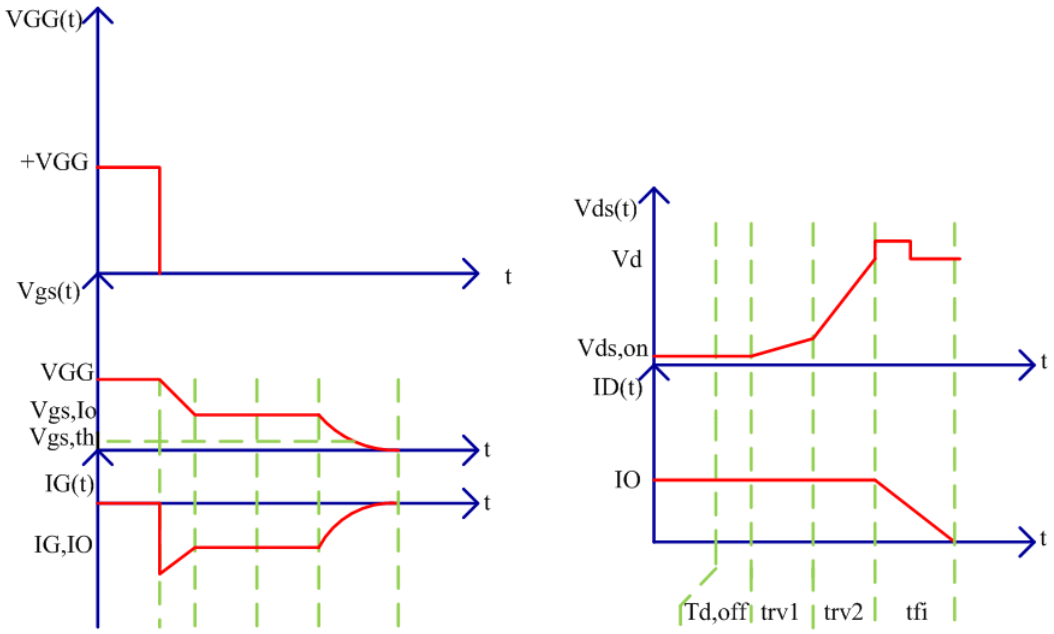
At the end of the falling time t_{fv2}, the gate−source voltage (v_{gs}) becomes un-clamped and begins to increase to V_{GG} with a time constant as in shown in the below equation and the equivalent circuit can be represented in Fig. 2.6(b) [5].

$$\tau_2 = R_G(C_{gs} + C_{gd2}) \tag{2.19}$$

•Turn−off procedure

The turn off procedure is the reverse process of the turn on steps. The first step is to reduce the gate voltage from +V_{GG} to 0. At this time the gate capacitor is charged to V_{GG} ($v_{gs}(t = t_0) = V_{GG}$) and due to this the gate current will be negative as shown in Fig. 2.8 and can be expressed as

$$i_G(t = 0) = -\frac{V_{GG}}{R_G} \tag{2.20}$$



(a) (b)

Fig. 2.8 Two MOSFET turn-off waveforms

The drain current is carrying the entire load current which means that there is no current flowing in the free-wheeling diode. Since the MOSFET transistor is operating in ohmic region, the drain-source voltage v_{ds} is calculated in (2.15). The negative gate current will discharge the capacitor and the gate voltage will decrease, see Fig. 2.8 [26].

$$i_g = -\frac{V_{GG}}{R_G} \tag{2.21}$$

$$v_{gs}(t) = V_{GG}\exp(-\frac{t}{\tau}) \tag{2.22}$$

The gate-source voltage decreases until it reaches a constant level where $v_{gs} = v_{gs,Io}$, while, the drain current is equal the load current. The gate−source voltage is

$$v_{gs} = v_{gs,th} + \frac{I_o}{g_m} \tag{2.23}$$

Solving the above equations for $t = t_{d,off}$ gives

$$t_{d,off} = R_G(C_{gs} + C_{gd})\ln(\frac{V_{GG}}{v_{gs,th} + \frac{I_o}{g_m}}) \tag{2.24}$$

When the gate voltage reaches the level when the drain-source current equals the load current, the gate voltage will be clamped to this level at the end of $t_{d,off}$. From this time, the gate drain capacitor will be charged by a negative current which leads to the increase of the drain-source voltage as is visualized in Fig. 2.8. During the time t_{rv1}, the gate drain capacitor is equal to C_{gd2} value which is a high value and during the time t_{rv2} the gate drain equal to C_{gd1} value which is low value [26].

As previous, $v_{gs} = v_{gs,Io}$

$$i_g = C_{gd}\frac{dv_{gd}}{dt} = C_{gd}\frac{d(v_{gs} - v_{ds})}{dt} \tag{2.25}$$

During this interval the source-gate voltage is constant. This yields

$$i_g = -C_{gd}\frac{dv_{ds}}{dt} \tag{2.26}$$

The drain current can also be found

$$i_g = \frac{V_{gs}(t1)}{R_G} = \frac{1}{R_G}(v_{gs,th} + \frac{I_o}{g_m}) \tag{2.27}$$

With $v_{ds}(0) = v_{ds,on}$, the solution is given by

$$V_{ds} = V_{ds,on} + \frac{1}{C_{gd}R_G}(v_{gs,th} + \frac{I_o}{g_m})(t - t_1) \tag{2.28}$$

At $t = t_{rv}$,$v_{ds} = V_d$ solving for t_{rv} yields

$$t_{rv1} = \frac{(V_d - V_{ds,on})R_G C_{gd1}}{v_{gs,th} + \frac{I_o}{g_m}} - t_{d,off} \tag{2.29}$$

$$t_{rv2} = \frac{(V_d - V_{ds,on})R_G C_{gd2}}{v_{gs,th} + \frac{I_o}{g_m}} - t_{rv1} \tag{2.30}$$

When the drain-source voltage reaches V_d, the diode starts to conduct and the gate-source capacitance is discharged leading to decreasing in both gate voltage and drain current as shown in Fig. 2.8 [26].

At $t = 0$, $v_{gs}(0) = v_{gs,Io}$ and then

$$v_{gs}(t) = (V_{gs,Io} + V_{GG})\exp(-\frac{t - t_2}{\tau}) \tag{2.31}$$

At $t = t_{fi}$, $v_{gs} = v_{gs,th}$. Solving for t_{fi} yields

$$t_{fi} = R_G(C_{gs} + C_{gd})\ln(\frac{V_{gs,Io}}{v_{gs,th}}) - t_{rv2} \tag{2.32}$$

When the gate voltage reaches the threshold voltage, the MOSFET transistor stops to conduct and the drain current is zero as shown in Fig. 2.8.

2.2 Phase leg converter

The configuration of the phase leg converter 'two quadrant converter ' is shown in Fig. 2.9. It consists of two switches Q_1 and Q_2 connecting in series and two diodes D_1 and D_2. The switch Q_1 and the diode D_2 form a buck converter. While, the switch Q_2 and the diode D_1 form a boost converter [25]. The voltage in the two quadrant converter is always positive. While, the current can flow in both direction as illustrated in Fig. 2.10. This feature is useful in many applications for instance in a battery storage system [17].

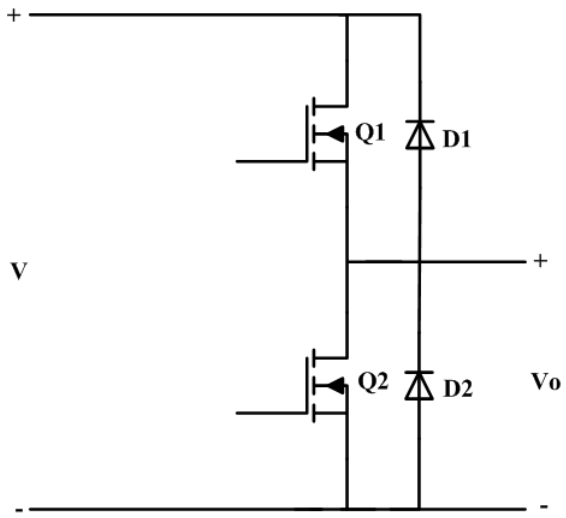


Fig. 2.9 Change of the gate-drain capacitor with the drain-source voltage

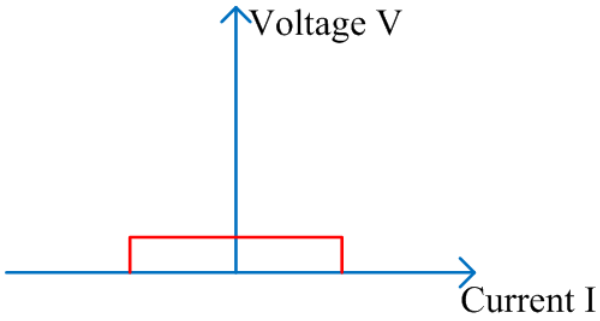


Fig. 2.10 voltage-current in two quadrant converter

The switching properties can be investigated by using this phase leg converter. When the power flow is positive it means that both voltage and current are positive as shown in Fig. 2.10. Thus, the converter is operating in the first quadrant where only the upper switch Q_1 and the lower diode D_2 are conducting. The phase leg converter operates as a step-down converter. However, when the output voltage is higher than the input voltage, the current will change its direction as the power flow does. In this operation mode, the phase leg converter is acting as a step$-$up converter where the lower switch Q_2 and the upper diode D_1 will conduct. The equivalent circuit for both operation modes is illustrated in Fig. 2.11(a) and Fig. 2.11(b) respectively.

(a) buck converter (b) boost converter

Fig. 2.11 Operating modes of half bridge converter

To implement the phase leg converter, there are many vital features that need to be taken into the account. An important aspect is the blanking time. Theoretically, the switch is assumed to be ideal. Therefore,

it is possible to consider that the switches in the converter can be changed simultaneously. However, in practice, the switches are not allowed to change simultaneously, in order to prevent a short circuit of the input voltage. So, a few micro seconds are implemented when none of the switches are conducting to prevent acting at the same time. This short time is called blanking time [17]. The blanking time introduces a reduction of the output voltage.

$$\Delta v_o = sign(i)\frac{T_b}{T_s}V \tag{2.33}$$

where T_b is the blanking time, T_s is the switching time, and V is the input voltage.

2.3 Drive circuit

The basic function of the drive circuit is to interface between the logic control circuit and the power semiconductor device. The drive circuit must be able to provide enough power to switch the device ON or OFF properly. In the MOSFET device, the drive circuit should achieve a constant gate voltage. Thus, the current shall charge and discharge the depletion region capacitance during turn-on and turn-off. Any drive circuit has to achieve several vital aspects such as, minimizing the switching time to reduce the power dissipation during the switching transient. Additionally, it has to keep the device ON during the switch-on period and prevent it from turning-off due to the stray inductance. Similarly, the drive circuit has to keep the device OFF during the off-state [26]. The drive circuit can also provide an electrical isolation between the control circuit and the power circuit to provide the control circuit against a high fault current.

For any drive circuit, there are three basic functions that should be considered [26]. First, whether the output signal of the drive is unipolar or bipolar is needed to know. The advantage of the unipolar drive circuit is to provide a simple circuit and few components. However, the advantage of the bipolar circuit is that it can turn-on and turn-off the power switch faster. Secondly, the control signal can be coupled directly to the power circuit, or the control circuit must be electrically isolated from the power circuit. The third consideration is if the drive circuit is connected in series or parallel with the device. The high requirements on the switching, the more complexity of the drive circuit is needed. In this section two types of drive circuits will be discussed.

The gate resistor is an important component to control the switching behavior of the MOSFET device. If the amount of the gate current varies, the charging and discharging time of the depletion capacitors will be changed. Thus, the gate resistor has to be designed properly [27].

As the voltage V_{GG} increases, the gate voltage rises according to

$$v_{gs} = V_{GG}(1 - \exp(-\frac{-t}{\tau})) \tag{2.34}$$

where $\tau = R_G(C_{gs} + C_{gd})$

At $t = t_{on}$, $v_{gs} = V_{gs,th}$

Thus,

$$v_{gs,th} = V_{GG}(1 - \exp(-\frac{-t_{on}}{\tau})) \tag{2.35}$$

Solving (2.35) for R_G yields

$$R_G = \frac{-t_{on}}{(C_{gs} + C_{gd}) \ln(1 - \frac{v_{gs,th}}{V_{GG}})} \tag{2.36}$$

By changing the gate resistor, the switching time (t_{on},t_{off}), switching losses (E_{on},E_{off}), turn ON/OFF peak current, $\frac{di}{dt}$, $\frac{dv}{dt}$, voltage spike, EMI noise will be affected [27]. If the gate resistor is reduced, the gate current will increase. As a result, the switching time (t_{on},t_{off}) will be faster. Moreover, the switching losses (E_{on},E_{off}) are decreased. However, this causes high $\frac{di}{dt}$ and $\frac{dv}{dt}$ which produces voltage spikes in the switch and high EMI noise. However, it is the opposite consequences if the value of the gate resistor is increased since the switching time is then increased [27].

2.3.1 Simple unipolar MOSFET drive circuit

The drive circuit controls the gate current to switch ON/OFF the power device as shown in Fig. 2.12. The drive circuit needs to increase the gate-source voltage (v_{gs}) above the threshold voltage ($v_{gs,th}$) to turn the device on. While, the drive circuit has to reduce the gate-source voltage below the threshold voltage ($v_{gs,th}$) to turn it off.

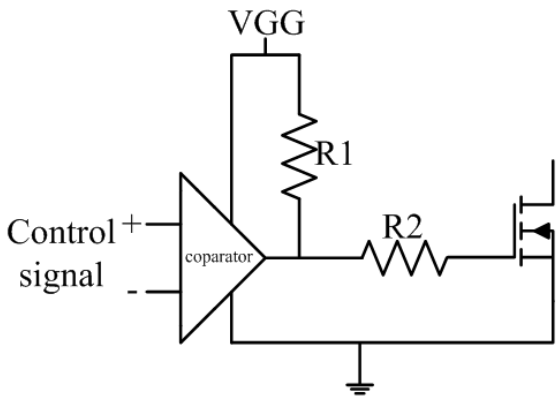


Fig. 2.12 Simple MOSFET drive circuit

The input of the comparator is the control signal. When the comparator is OFF, the gate current is limited by resistors R_1 and R_2 to achieve fast switching. While, when the comparator is ON, the depletion capacitance will discharge through the resistor R_2 to switch the device OFF. The resistor R_2 is an important component to control the speed of the device switching. The low value of R_2 could achieve a faster turn-on switching, while, a high value of the power dissipation is obtained during a slow turn-off of the device. So, it is a trade-off between the speed of switching and the power dissipation [26].

2.3.2 MOSFET driving circuit,quicker switching

To decrease the power dissipation during the ON/OFF switching, the switching time has to be as fast as possible. Therefore, a totem-pole arrangement is used to solve this problem as shown in Fig. 2.13. When the comparator is OFF, the npn transistor of the totem-pole arrangement is turned-on providing a positive voltage to the MOSFET device to turn it on. While, when the comparator is off, the pnp transistor of the totem-pole arrangement will turn-on. Thus, the gate will be shorted through the gate resistorR_G to the source. In this case there is no trade-off between the speed of the switching and the power dissipation. Therefore, the gate resistor has to have a high value [26].

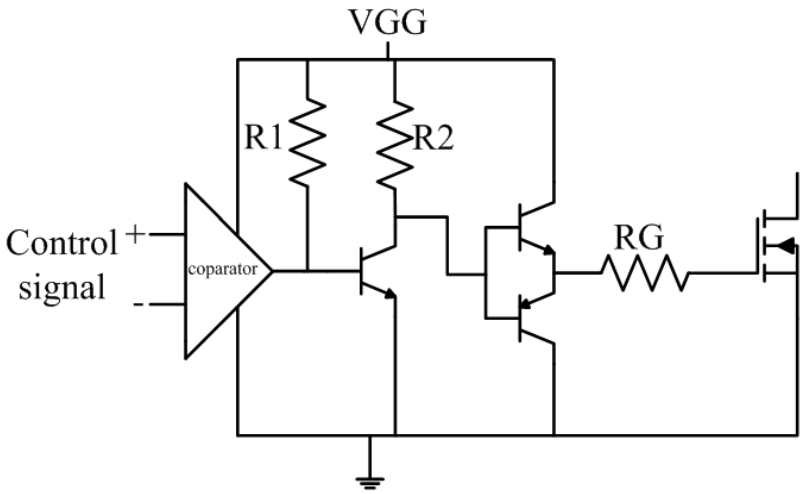


Fig. 2.13 Half bridge rectifier circuit

2.4 Electrically isolated drive circuit

There are many methods of isolating the control circuit from the MOSFET device. The simplest method is by using a passive element such as a pulse transformer. However, there are many limitations in using a transformer, such as the size of the transformer, transformer saturation, and magnetizing current. All these factors will reduce the efficiency [1]. Another method is to use a screen opto-coupler as shown in Fig. 2.14.

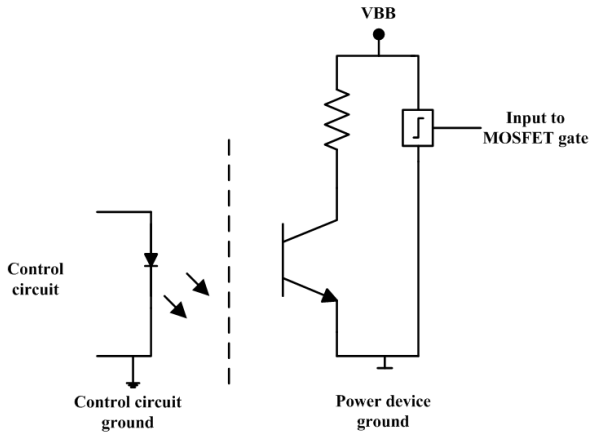


Fig. 2.14 screen opto-coupler

When a positive signal from the control circuit is applied on the photo diode terminals, there will be a current flow in the diode causing the LED to turn-on. Both a photo diode and photo transistor are integrated in the IC. Thus, the light is falling on the base region of the photo transistor. As a consequence, a significant number of electron-hole pair is generated. Then, the photo transistor is turned on [26].

There is a potential difference between the transistor emitter (ground of the power circuit) and the reference point of the control circuit. This is due to the turn ON/OFF of the photo transistor. So, there is a stray capacitor between the photo diode and the base of the photo transistor. Therefore, unwanted re-triggering of the transistor is possible. To avoid this problem, a metallic screen between the photo diode and transistor should be used as shown in Fig. 2.14 [26].

2.5 Losses in MOSFET

The semiconductor switch needs to perform as close as possible to an ideal switch. There are many features when the semiconductor device operates as an ideal switch as shown below:

- Zero rise time and fall time which means that there is no speed limitation of the device.
- When the device is in off-state, there is no leakage current. Therefore, the device has an infinite off-state resistance.
- Limitation on the amount of current and voltage that the device can carry when it is in the conduction state (on-state) and in the non-conduction state (off-state) respectively.
- Zero on state voltage and resistance when it is in the conduction state (on-state).

The power loss is zero during the switching and conduction periods as shown in Fig. 2.15. As a result, an ideal switch has 100% efficiency, unlimited power capacity, infinite operating frequency, and no switching delay is needed.

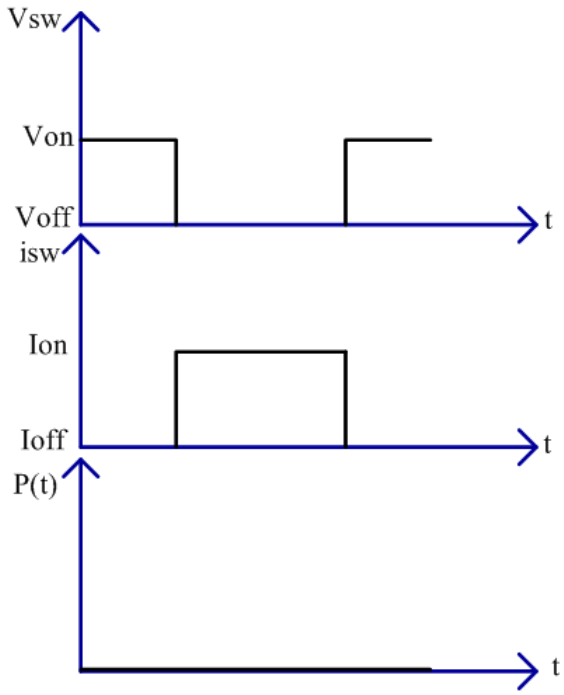


Fig. 2.15 More realistic MOSFET waveforms

While, the practical switch has specific characteristics as shown below:

- Finite rise time and fall time. On the other hand, the device has a limited switching speed.
- Finite on-state and off-state resistor.
- Limited amount of the current and voltage when the switch is in the on-state and off-state respectively. Therefore, the device has a specific power handling capacity.
- Finite forward voltage drop when the device in the on-state.

The losses of the MOSFET device can be divided into two types; conduction losses (P_c)and switching losses (P_{sw}). To evaluate the average switching and conduction power losses, a step down converter with inductive load is used as in Fig. 2.3. The switching current, and voltage waveforms of the circuit are visualised in Fig. 2.16. For simplicity, a linear approximation of rising and falling time for both current and voltage is considered. Moreover, the ripple in the load current is neglected as in Fig. 2.16.

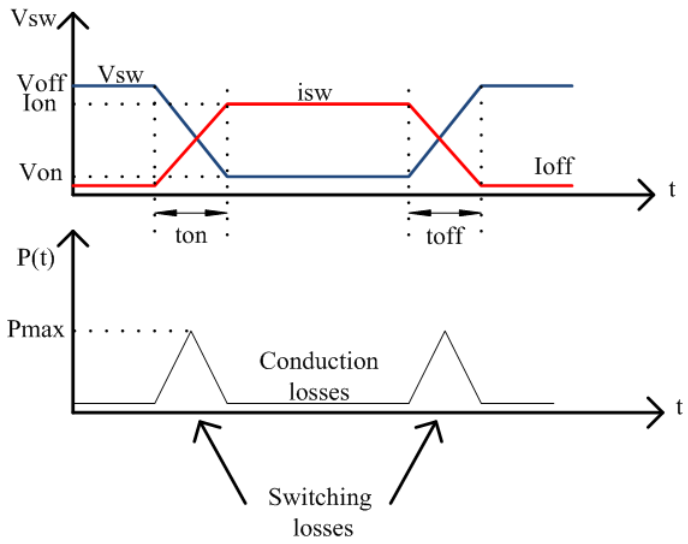


Fig. 2.16 Step-down converter

where

T_{on}: turn-on time.
T_{off}: turn-off time.
V_{on}: forward conduction voltage during the conduction state.
V_{off}: dc voltage across the switch during the non-conduction state.
I_{off}: leakage current during the non-conduction state.
I_{ON}: dc current through the switch when it is on.

The conduction losses can be obtained by multiplying the on-state voltage by the load current

$$P_d = V_{on} I_o \tag{2.37}$$

The switching losses are the losses dissipated during the transition from on-state to off-state and vice versa. Both the current and the voltage are not zero during the the transition periods as it is visualized in Fig. 2.16. The energy dissipated during one turn ON/OFF period is given by

$$E_{sw,off} = V I_o = \frac{t_{rv} + t_{fi}}{2} \tag{2.38}$$

$$E_{sw,on} = V I_o = \frac{t_{ri} + t_{fv}}{2} \tag{2.39}$$

The switching losses are given by switching frequency multiplication by energy dissipated in the one switching cycle.

$$P_{sw} = (E_{sw,off} + E_{sw,on}) f_{sw} \tag{2.40}$$

2.6 MOSFET junction temperature

Fig. 2.16 shows theoretical turn ON/OFF switching waveforms. The overlapping periods between the voltage and the current represents the losses in the switch. This is due to the stray inductance in the conductors. This stray inductance comes from the placement of the components, so they are not physical inductors. The design of the circuit should be done to minimize the effect of these inductors.

To calculate the junction temperature in the MOSFET, the total losses must be known. The total losses are the sum of the conduction losses and switching losses. Then the junction temperature can be calculated

as

$$P_{totallosses} = P_{sw} + P_{cond} \tag{2.41}$$

$$T_j = T_a + P_{totallosses} \times R_{\theta ja} \tag{2.42}$$

where T_j is the junction temperature, T_a is the ambient temperature, $R_{\theta ja}$ is the junction to ambient thermal resistor.

Chapter 3

Case study and simulation analysis of drive circuit

3.1 case set-up

In this chapter the drive circuit is tested. First, different values of R and C are used in drive circuit instead of the MOSFET. Then, the MOSFET is used to analyze the switching characteristics of the device during ON and OFF transients.

3.1.1 Power circuit

Fig. 3.2 illustrates the electrical circuit that is used in this project to study the drive circuit for one MOSFET transistor. The DC voltage is applied by DC voltage source through the junction $J2$. The range of DC voltage source is $(0$ to $10)V$ when the MOSFET is tested. A $9V$ battery is connecting through the junction $C1x2$. A $30A$, $250V$ fuse is put in series with the DC voltage source to protect the MOSFET against a probable short circuit that might occur. Two low-ohms high power resistors (0.1Ω) are put in the current path in order to enable us to calculate the current by the aid of Ohm's law. Four parallel capacitors are connected in the input path to stabilize the DC link voltage that is applied to the MOSFET device. Each capacitor is selected to $100\mu F$. Thus, the total capacity of the capacitor bank is $0.4mF$ as it is visualized in Fig. 3.1. Series connection of resistors and ceramic capacitors are connected at the input voltage to filter out the ripple in the DC link voltage. Both ceramic capacitors are used since they operate at high frequency and works for both polarities; positive and negative.

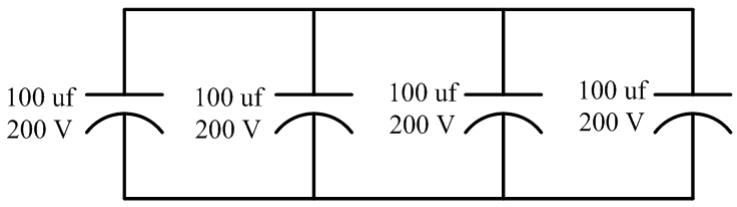


Fig. 3.1 DC link Capacitor bank

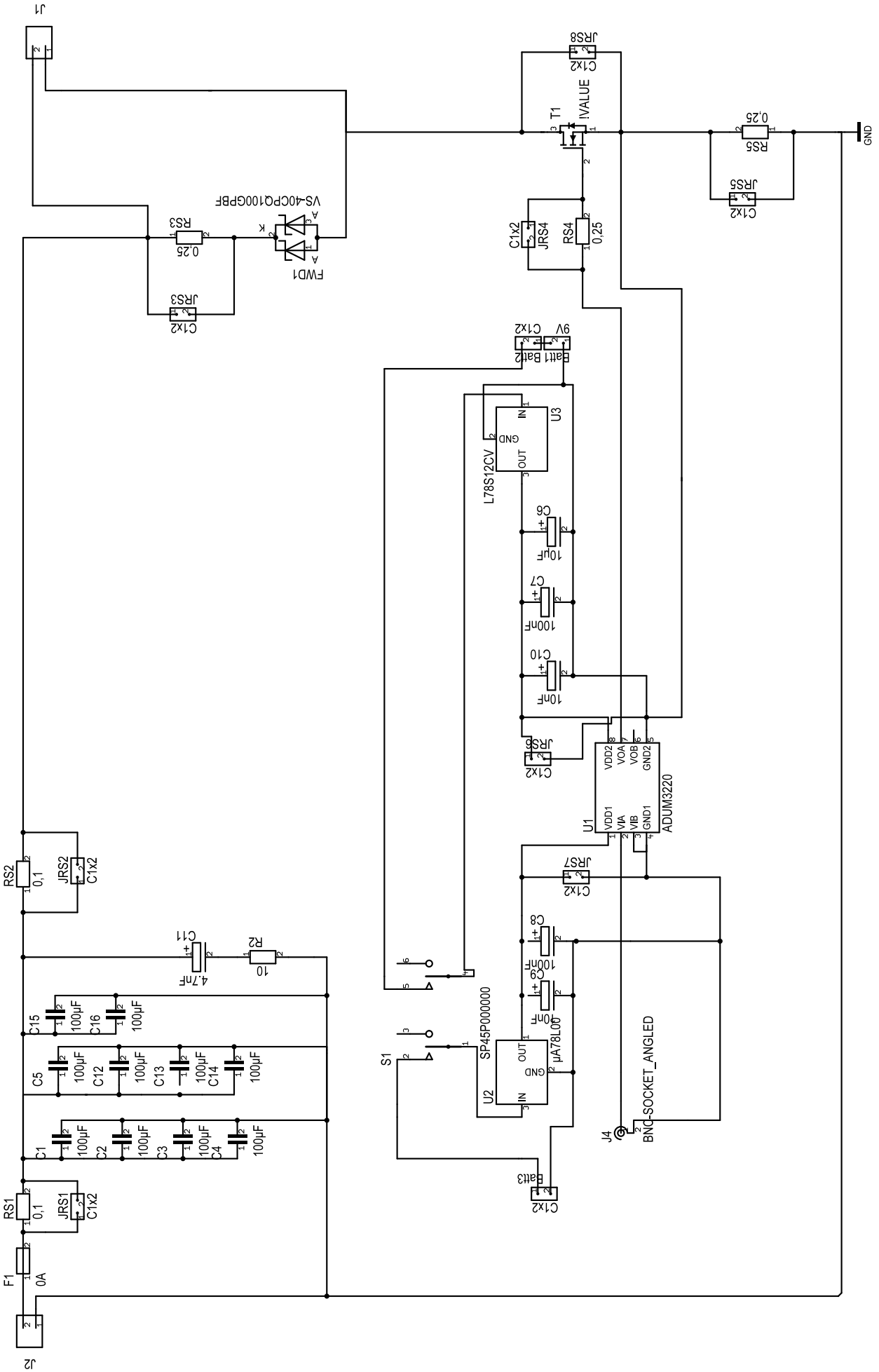


Fig. 3.2 Power and drive circuit

An N-channel FAIRCHILD HUF75639G3 is used as a switch device. This power MOSFET has very low on-state resistance, capable to withstand high power dissipation, low reverse time recovery, low stored charge, and high efficiency [23]. Table 3.1 shows some of the important specifications of this device.

Table 3.1: MOSFET specification

Part number	Package	$I_{D_{max}}(A)$	$R_{ds_{on}}(\Omega)$	$Q_g(TOT)(ns)$
HUF75639G3	TO-247	56	0.021	130

A VS-40CPQ100PBF Schottky diode is used as a free-wheeling diode as shown in Fig. 3.2. This diode has a low forward voltage drop, high frequency operation, and withstand high junction temperature [30]. Table 3.2 shows some of the important specifications of this diode.

Table 3.2: Schottky diode specification

Part number	$I_{F_{AV}}(A)$	$V_R(V)$	$V_F(V)$	T_j
$40CPQ080PbF$	40	80-100	0.61	-55 to 175

A current stiff load is used to study the turn-on and turn-off transient characteristics. This can be achieved by connecting $10mH$ in series with 10Ω through the junction $J1$. A small power resistor (0.25Ω) is connected between the MOSFET source pin and the ground to measure the drain current.

3.1.2 Drive circuit

The main part of the drive circuit is the isolated, 4 A Dual-Channel Gate Driver ADUM3220. This device has many features such as

1. It provides a digital isolation between the input and the output. The digital isolation is provided by a combination of a high speed CMOS and monolithic transformer technology [18]. Therefore, no external protection is required.
2. ADUM3220 has two output channels. But, it provides a shoot-through protection to prevent both channels being on simultaneously.
3. High junction temperature range (-40 to 125)°C

Fig. 3.3 illustrates the pin configuration of ADUM3220

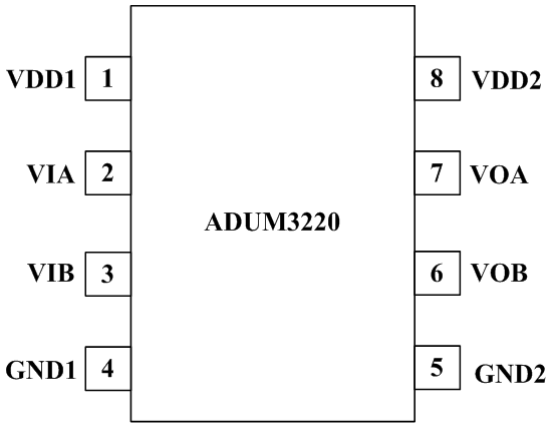


Fig. 3.3 4 A Dual-Channel Gate Driver ADUM3220 pin configuration

Two power supplies are required to operate this device. The first power supply $VDD1$ for isolated side A and the second supply $VDD2$ for the isolated side B. Bypass capacitors are required at both supply pins to the ground pins as shown in Fig. 3.4. On the first power supply $VDD1$, a small ceramic capacitor ($10nF$) is selected to bypass the high frequencies [18]. However, two $10nF$ capacitors are put at the second power supply $VDD2$ to provide the required charge for the MOSFET gate capacitor. The distance between these capacitors and the supply pins ought not to exceed 20 mm to reduce the stray inductance in the switching path [18].

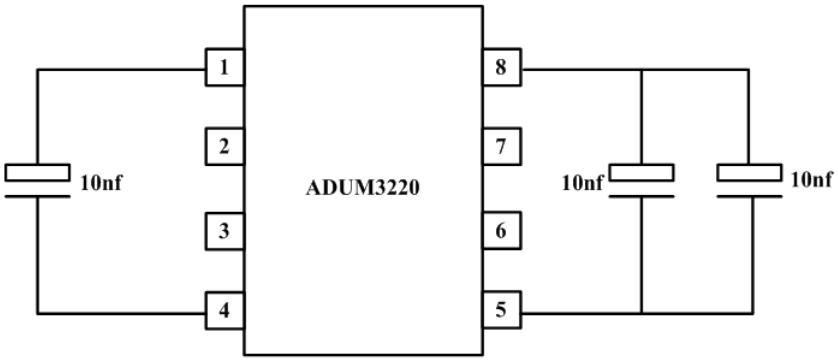


Fig. 3.4 By passing capacitors of 4 A Dual-Channel Gate Driver ADUM3220

A three terminal regulator μA78L05C is used to regulate the first power supply $VDD1$ that supply the $5V$ as is visualized in Fig. 3.5. A $100nF$ capacitor is connected on the output terminal to stabilize the output voltage at $5V$ [29]. In addition to that , two $9V$ batteries are connected in series through the junction $C1x2$ as shown in Fig. 3.2. A three terminals regulator L78S12CV is shown in Fig. 3.6 is used to regulate the second power supply $VDD2$ at $12V$. A $100nF$ capacitor is connected at the L78S12CV output pin to stabilize the $VDD2$ at $12V$. A TTL signal is applied through the junction $C1x4$ to the ADUM3220 at the VIA pin. The output voltage at the pin VOA is the V_{GG} . A gate resistor is connected between the MOSFET gate pin and the ADUM3220 output pin VOA.

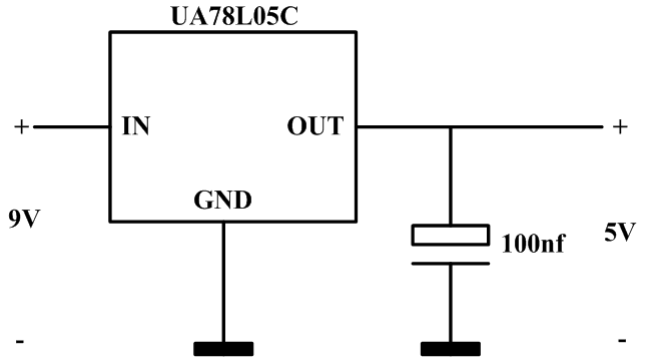


Fig. 3.5 μA78L05C electrical connection

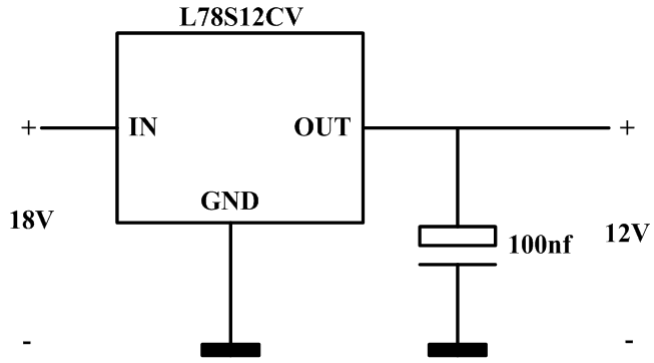


Fig. 3.6 L78S12CV electrical connection

3.2 Experimental set-up

The measurement is divided in two scenarios. In the first scenario, the performance of the drive circuit is tested four times by using different values of RC_s circuit. However, the drive circuit is used to study the switching characteristics of the MOSFET in the second scenario. The gate voltage V_{GG}, gate-source voltage V_{GS}, and gate current are investigated in this section. The gate current is recorded by two different methods. The first method is by using a differential probe on the gate resistor. However, the gate current is observed by using a rogowski coil in the second method. Both methods have a delay time which comes from the measurement instrument but rogowski coil has more delay time than the differential probe.

3.2.1 RC setup circuit

Fig. 3.7 shows the gate drive circuit that is used to study the performance of the drive circuit by connecting a simple RC circuit.

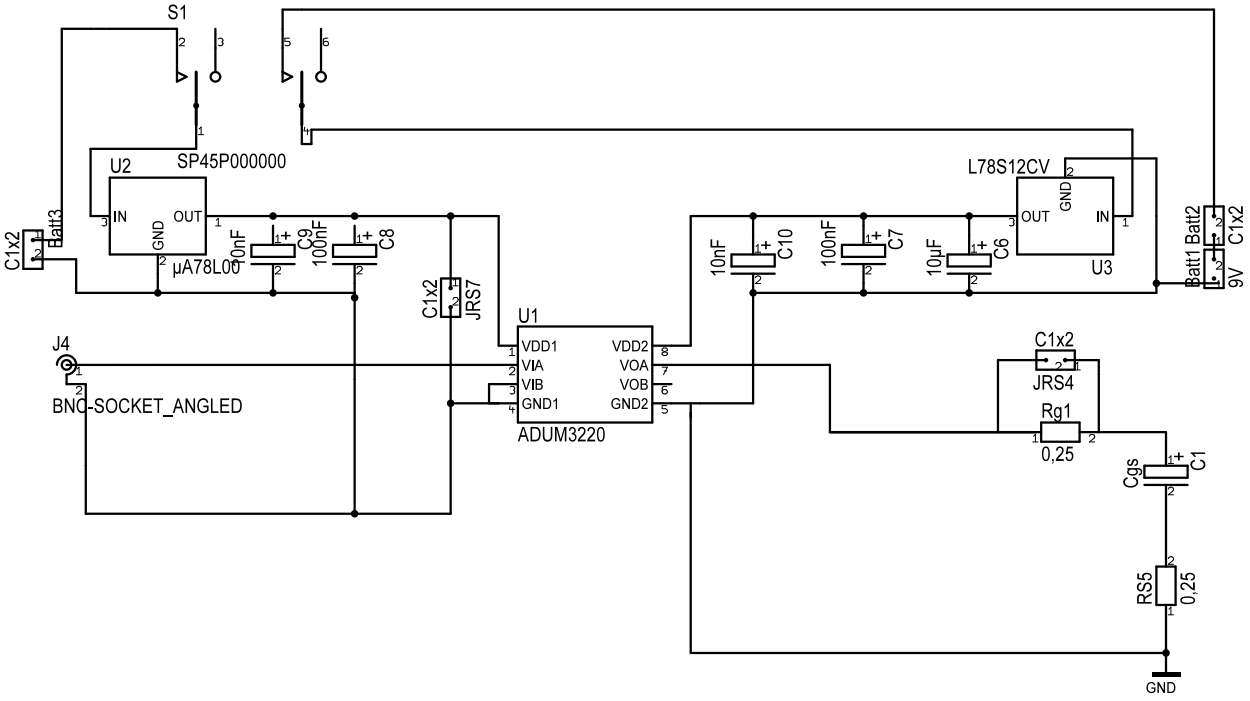


Fig. 3.7 L78S12CV electrical connection

The path from the output of ADUM3220 (V_{GG}) to the gate-source voltage (V_{gs}) is affected by the values of the gate resistor (R_G) and the gate-source capacitor (C_{gs}). However, the stray inductance of the drive circuit is assumed to be small, and as a result it can be neglected [27]. The output response of the network can be determined according to

$$V(t) = V_0(1 - exp(-\frac{t}{\tau})) \tag{3.1}$$

In the first test, a low value of the time constant ($R_G = 4.7\Omega$, $C_{gs} = 2.2nf$) circuit are selected. The rise time is obtained according to

$$V(t) = V_0(1 - exp(-\frac{t}{\tau})) \iff \frac{V(t)}{V_0} = (1 - exp(-\frac{t}{\tau})) \tag{3.2}$$

The rise time is the time required for a signal to increase from $10\%$to 90% of its final value

$$0.1 = (1 - exp(-\frac{t_1}{\tau})) \qquad\qquad 0.9 = (1 - exp(-\frac{t_2}{\tau})) \tag{3.3}$$

Solving for t_1 and t_2 gives

$$t_1 = \tau(\ln(10) - \ln(9)) \qquad\qquad t_1 = \tau \ln(10) \tag{3.4}$$

Then

$$t_r = t_2 - t_1 = \tau \ln(9) \tag{3.5}$$

where $\tau = RC$. substituting it in (3.5)

$$t_r = \ln(9)\tau \tag{3.6}$$

The rise time of the gate voltage (V_{GG}) and the gate-source voltage is $15.35ns$ and $28.25ns$ respectively. As the gate voltage increases, the gate-source voltage increases after a delay and therefore the gate current flows in positive direction. When the gate-source voltage is equal to the gate voltage (at steady state), there is no current flowing in the circuit which is shown in Fig. 3.9. However, in the negative edge of the gate

voltage, the gate-source voltage decreases slower than V_{GG} and therefore a negative gate current flows in the circuit.

In the second test, a small value of the gate resistor ($R_G = 1\Omega$) and the same gate-source capacitor is used. During the turn-on, the gate-source voltage increases as the gate voltage increases. There is a small difference between V_{GG} and V_{gs} because of the small voltage drop over the gate resistor. As shown in Fig. 3.9, there is an oscillation in the gate-source voltage until it reaches the steady state. As a result, the gate current also oscillates. There is also an oscillation in the gate current during the turn-off transient as shown in Fig. 3.9.

In the third test, a high value of the gate-source capacitor ($10nF$) and the gate resistor ($R_G = 1\Omega$) are selected. There is no oscillation in the gate current in both the turn-on and turn-off period that is due to the big capacitor that is selected as shown in Fig. 3.10. The rise time of the gate voltage and the gate-source voltage is $39.93ns$ and $51.55ns$ respectively.

Finally in the fourth test, a high value of the gate resistor ($R_G = 4.7\Omega$) is selected. However, the gate-source capacitor remains the same. The voltage drop on the gate resistor is high and therefore a big difference between the gate voltage and the gate-source in both turning-on and turning-off period occurs as is visualized in Fig. 3.10. The rise time of the gate voltage and the gate-source voltage is $34.51ns$ and $133.6ns$ respectively.

In all the tests above it is observed that there is a delay time in the gate current measurement if the rogowski coil is used. This is due to the delay in the electronic components of the rogowski coil.

3.3 Drive circuit simulation analysis

In this part the drive circuit is modelled by using a SIMPLORER from (ANSOFT Corp.). By implementing this model make it is possible to simulate the gate voltage, gate-source voltage, and gate current. It is also possible to observe the change in the switching transient of the voltage and the current by changing the gate resistor and/or the gate-source capacitance.

Fig. 3.8 visualizes the drive circuit model which is implemented in SIMPLORER. The gate voltage (V_{gg})is modelled by using a $\pm$6 V pulse generator. To simulate the correct rise time of the gate voltage a basic RC circuit is used. The path from the output of the ADUM3220 to the gate of the MOSFET creates a stray inductance. Since this distance is less than $10mm$, $5nF$ is put in series with the gate resistor. $20nH$ is the internal inductance of the gate according to the data sheet. Therefore, it is essential to add this value to the model to get better simulation results.

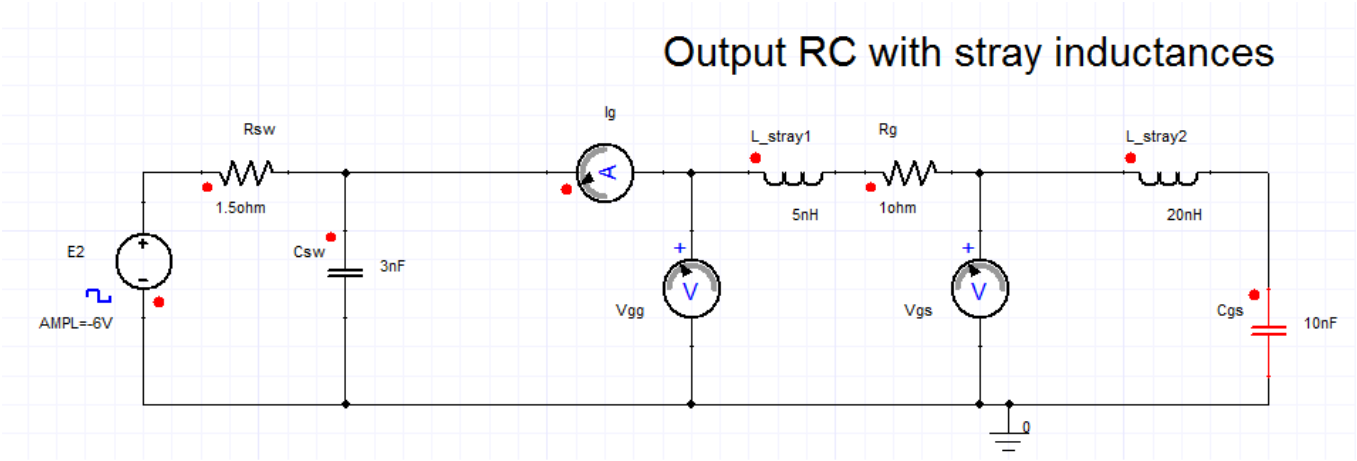


Fig. 3.8 Drive circuit simulation circuit

Fig. 3.11 and Fig. 3.12 show both the simulation results and the measurement results. One can say that the simulation curves and the measurement curves match each other at steady state($12V$). However, during the transients there are mismatch between them and that is probably due to error in measurement or error in modelling of the stray inductance of the drive circuit.

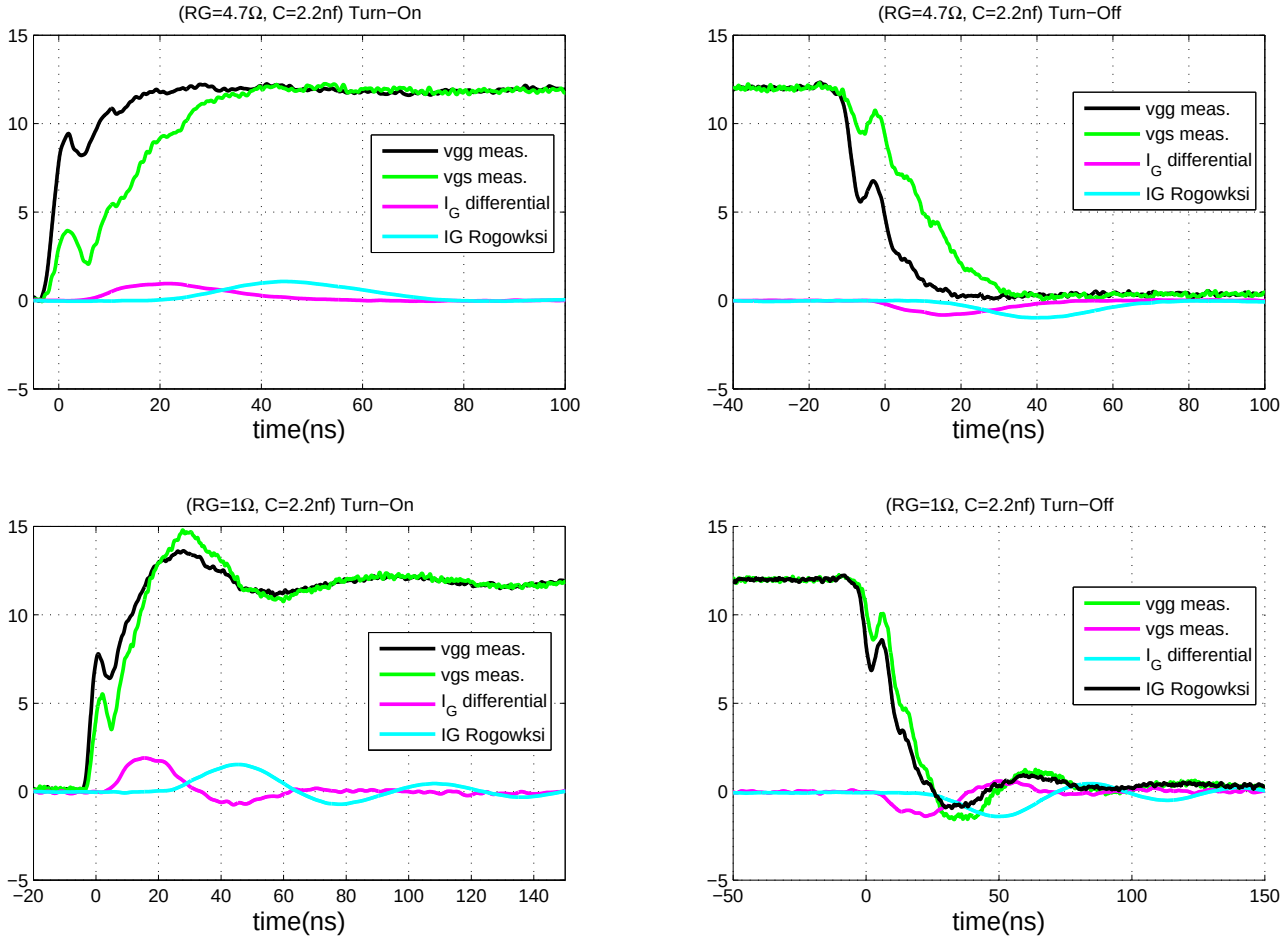


Fig. 3.9 Simulation and measurement curves with $C = 2.2nf$

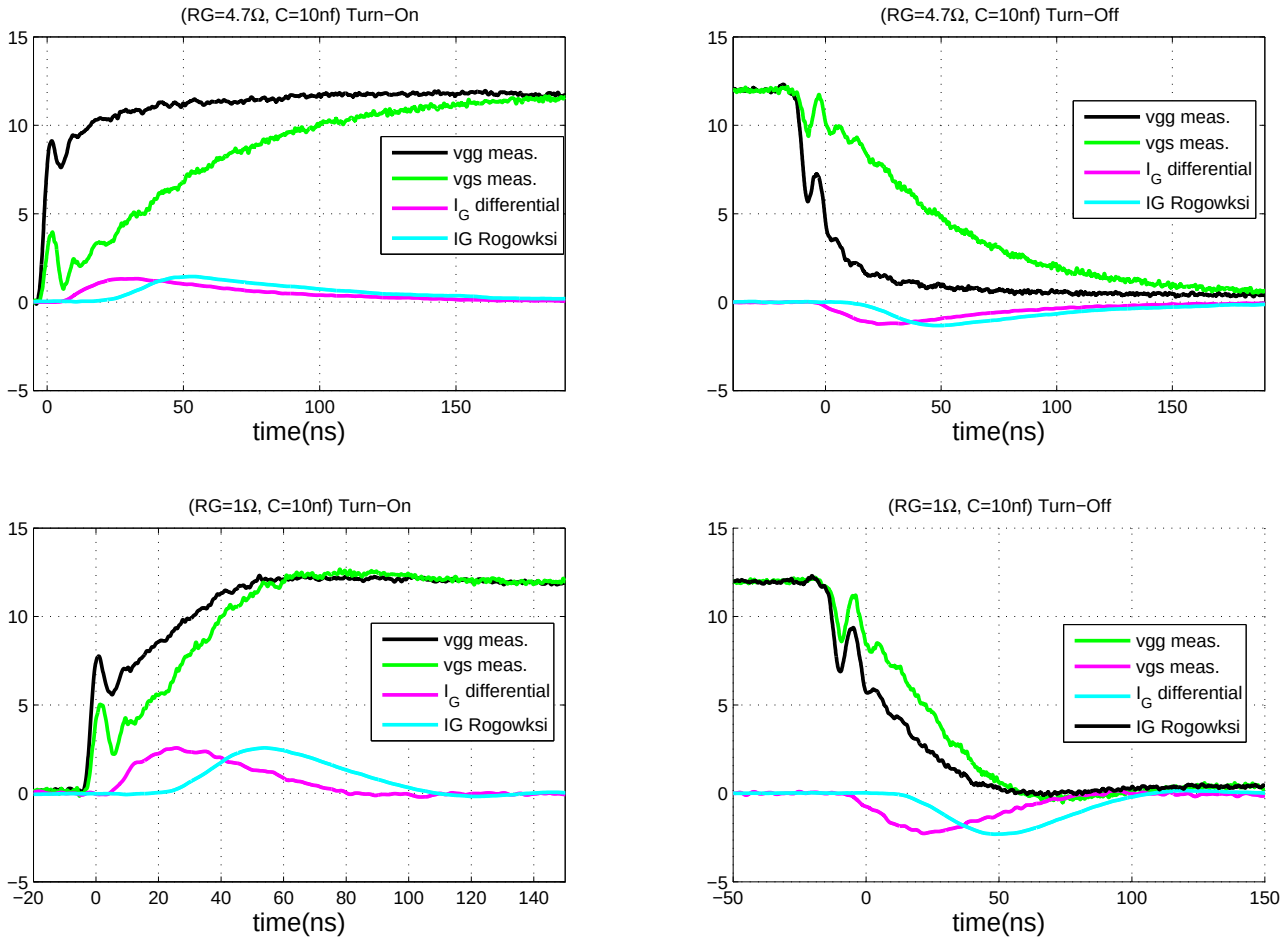


Fig. 3.10 Simulation and measurement curves with $C = 10nf$

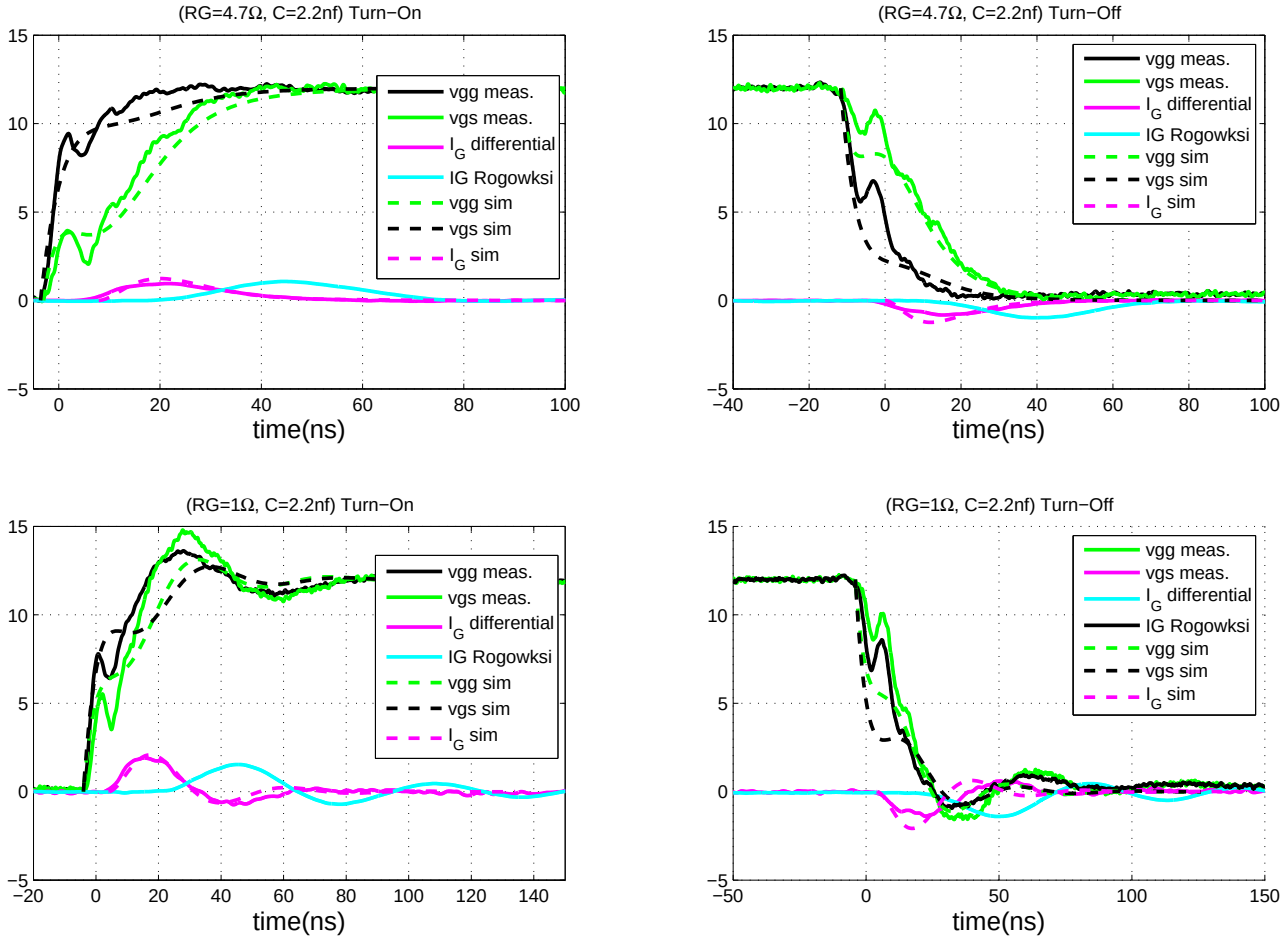


Fig. 3.11 Simulation and measurement curves with $C = 2.2nf$

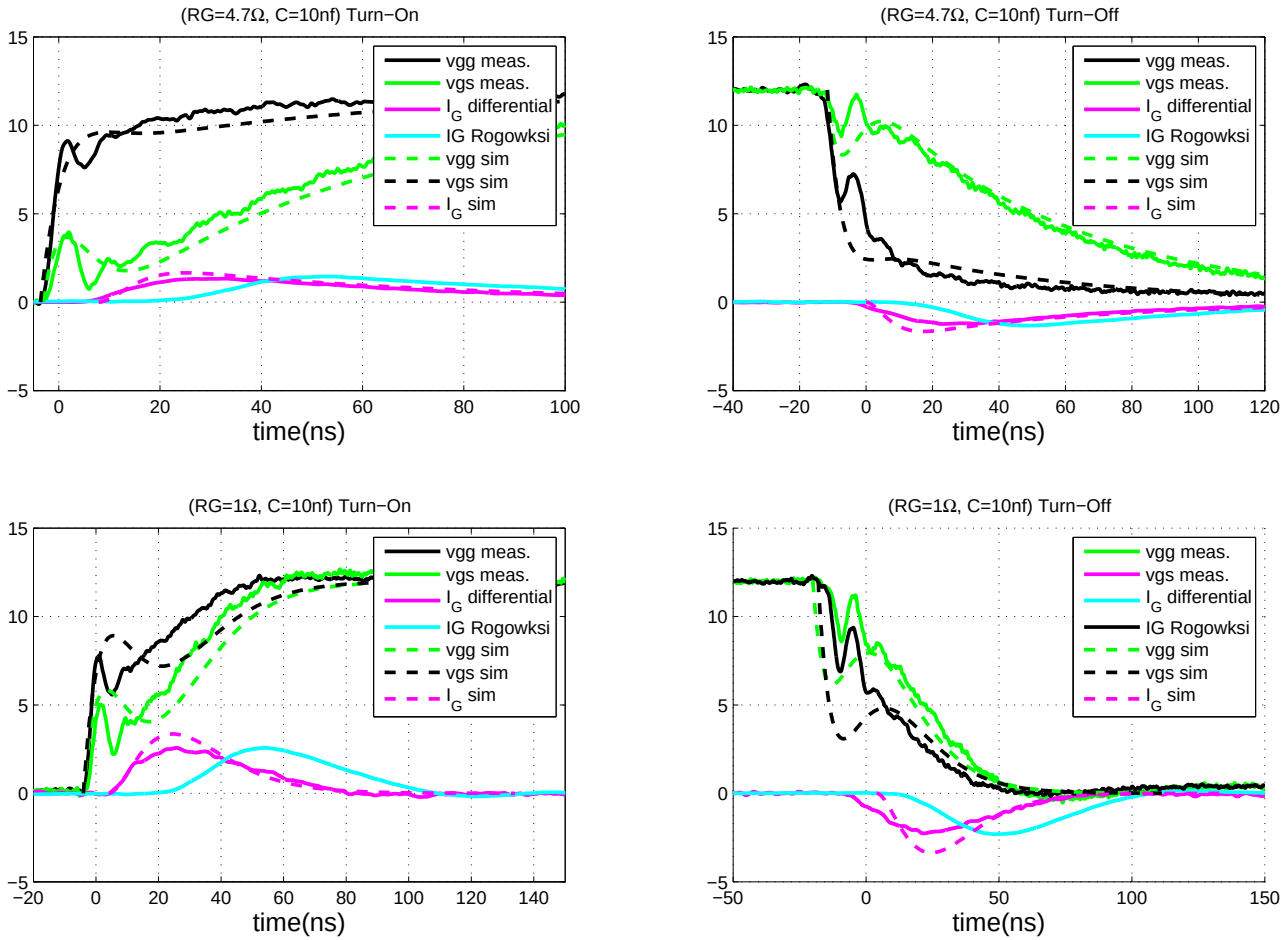


Fig. 3.12 Simulation and measurement curves with $C = 10nf$

Chapter 4

Thermal model

Any power electronic components consume electric power and convert it into heat which is another form of energy [19]. Heat is produced when the total power dissipation under a specific load condition comprises the conduction and switching loss. The junction temperature and cycling temperature are important parameters to maintain the lifetime of the device. The junction temperature is affected by many component parameters. Thus, the device will be permanently damaged, if the junction temperature exceeds the maximum value. For hard switching converters, the switch requires to turn ON/OFF at the entire load current which gives high switching losses due to large $\frac{di}{dt}$ and $\frac{dv}{dt}$. As a result, electromagnetic interference (EMI) is produced. So it is a trade-off between the EMI behaviour and the optimal thermal behavior of the device. The percentage of the total heat that flows out through the MOSFET device is important to know. This importance is due to that it affects the amount of the current that can be successfully switched through the MOSFET. Keeping a low on-state resistance and better flow of heat away from the junction will ensure the reliability and performance of the MOSFET as a switch device.

A power semiconductor thermal design is important for a reliable operation. If the temperature rating is violated, the device safe operating area is reduced. As a result, the device might suddenly fail. The junction temperature can be calculated by knowing the thermal impedance and the power dissipation of the device. In a power MOSFET, there are six physical layers that describe the device heat transfer as is visualized in Fig. 4.1.

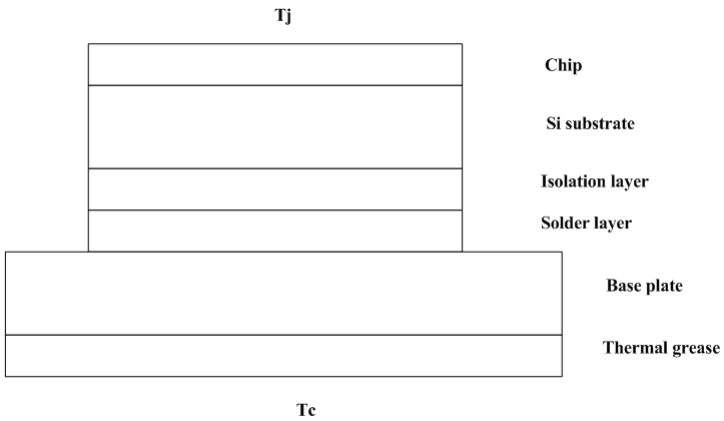


Fig. 4.1 MOSFET layers

The chip temperature which is caused by power dissipation, and a safe operation area that is limited by the virtual junction temperature. The term virtual junction temperature is used due to non-homogeneous of the chip temperature. However, the junction to case thermal impedance ($Zthjc$) of the device is calculated by the virtual junction temperature by assuming a homogeneous cooling of the device [2]. In practice, the operating junction temperature has to be between the maximum and minimum allowed value of the junction temperature even in overload situation. The case temperature is the temperature of the plastic housing material of the semiconductor device. Usually the case temperature is less than the junction temperature.

Moreover, the heat sink surface temperature can be described by the heat sink temperature. The temperature of the heat sink rises due to the absorption of the power dissipation by the heat sink. To understand the propagation of heat within the MOSFET device, the heat transfer mechanism needs to be recognized. In fact, heat is transferred in three different ways: conduction, convection, and radiation. Conduction is 'the transfer of energy through matter from particle to particle ' [3]. In a MOSFET, the heat conduction will take place from the chip junction through solid materials. However, the other two heat transfer mechanism, convection and radiation, are more complicated than conduction. Convection is 'the transfer of heat by the actual movement of the warmed matter. For example, heat leaves the coffee cup as the currents of steam and air rise ' [3]. In another words, convection takes place when there is a temperature difference between a solid surface and the surrounding gas which is a contact with the surface of the solid. Convection depends on the heat transfer area and the temperature difference

$$P_{convection} = 1.34A\frac{(\Delta T)^{1.25}}{(d_{vertical})^{0.25}} \tag{4.1}$$

where

$P_{convection}$: heat transfer per second (W).
A: Vertical area of the body (m^2).
ΔT: temperature difference between the solid surface and air ($^{\circ}$C).
$d_{vertical}$:Vertical height of the body (m) .

The heat sink carries out this propagation of heat from the MOSFET device to ambient air. Radiation is 'electromagnetic waves that directly transport energy through space. Sun light is a form of radiation that is radiated through space without the aid of fluids or solids ' [3]. Radiation occurs at high temperature when the surface receives and emits the radiative heat from the surrounding

$$P_{radiation} = \epsilon\sigma(T_h^4 - T_c^4) \tag{4.2}$$

where

$P_{radiation}$: heat transfer per second (W).
ϵ: emissivity of the object.
σ: Boltzmann constant 5.6703$\times$ 10^{-8} ($\frac{W}{m^2K^4}$).
T_h: absolute temperature of the hot body (K).
T_c: absolute temperature of the surrounding (K).

Radiation mechanism is strongly depending on the $4th$ order of the heat. For a large object, the radiation has to be included in thermal analysis. For simplicity reasons, a one dimensional heat flow (heat conduction) is assumed in this project [8].

$$\frac{\partial^2 T}{\partial x^2} = \frac{c\rho}{\lambda_{th}}\frac{\partial T}{\partial t} \tag{4.3}$$

where

λ_{th}: thermal conductivity ($wm^{-1}c^{-1}$).
c: thermal capacitance ($\frac{J}{kgK}$).
ρ: density of the material (kg/m^3).
T: temperature (K).
λ_{th}: coordinate in the direction of heat propagation.

Fig. 4.2 shows the electrical analogy model of a transmission line which is the closest model that can represent the heat conduction [22].

$$\frac{\partial^2 u}{\partial x^2} = C'L'\frac{\partial^2 u}{\partial t^2} + (C'R' + G'L') + \frac{\partial u}{\partial t} + +G'R'u \tag{4.4}$$

where

C': capacitance per unit length ($\frac{F}{m}$).
R': resistance per unit length ($\frac{\Omega}{m}$).

G': transverse conductance per unit length ($\Omega^{-1}m^{-1}$).
L': capacitance per unit length ($\frac{H}{m}$).

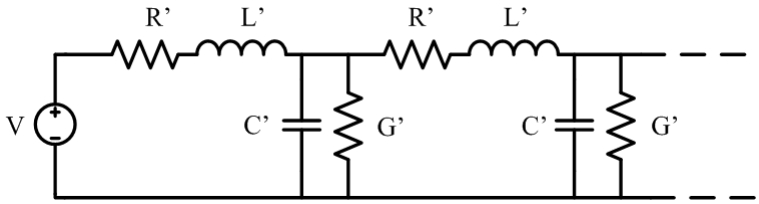


Fig. 4.2 Transmission line

Putting the linear capacitor and resistor to zero we obtain

$$\frac{\partial^2 u}{\partial x^2} = G'L'\frac{\partial u}{\partial t} \tag{4.5}$$

The transmission line wave (4.3), depicts all the wave properties such as propagation, reflection, etc, while, the heat conduction (4.5) depicts the heat diffusion process [9]. An electrical model of the transmission line is illustrated in Fig. 4.3

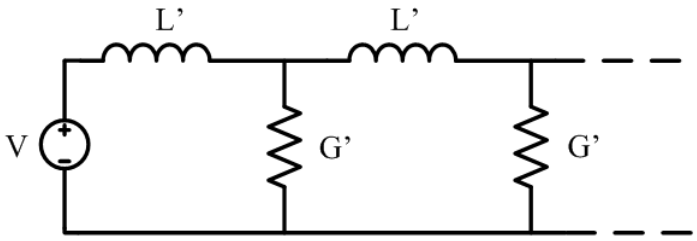


Fig. 4.3 Simplified electrical model of the transmission line

By the principle of circuit duality, the above model can be transformed as shown in Fig. 4.4

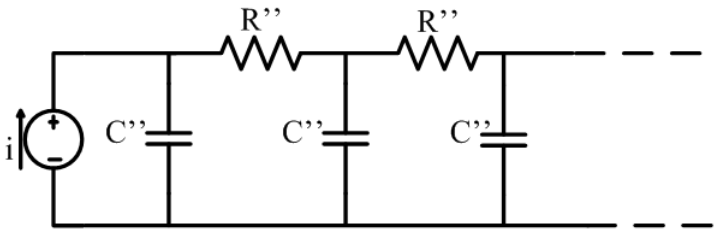


Fig. 4.4 Transformation by the principle of duality

The equation above becomes

$$\frac{\partial^2 i}{\partial x^2} = R''C''\frac{\partial i}{\partial t} \tag{4.6}$$

Thus, the structure of the relationship (4.6) is similar to that of the heat transfer equation (4.3) [9]. Therefore, both the electrical domain and the thermal domain are similar and have the same principles. As a result, all the principles of electrical circuit analysis are applied to the thermal circuit analysis, especially when it is related to thermal conduction. The through variable in an electrical circuit is the current that flows from one point to another as in Fig. 4.5 [7]. However, the across variable in the electrical domain is the voltage difference between two points which forces the current flowing between A and B. The across variable in the thermal circuit is the power which forces the through variable, heat, to flow from one point

to another point as in Fig. 4.5. The resistance in both systems has the same principle. So, it is not surprising that fundamental equation such as 'ohm's law ' of electrical domain also can be applied in thermal domain. Moreover, the symbols of the electrical circuit can be used in thermal circuit.

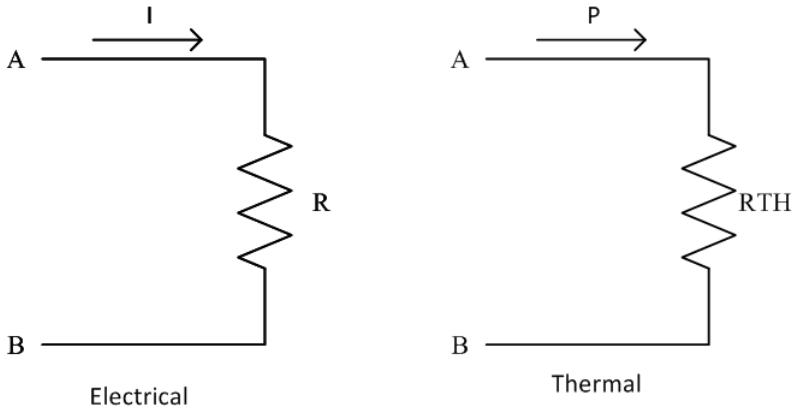
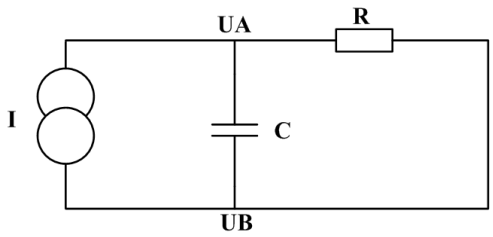


Fig. 4.5 Basic principle of electrical and thermal domain

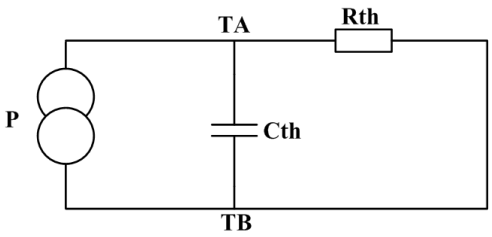
The equivalence between thermal and electrical quantities can be defined in Table 4.1.

Table 4.1: Definition of physical magnitudes

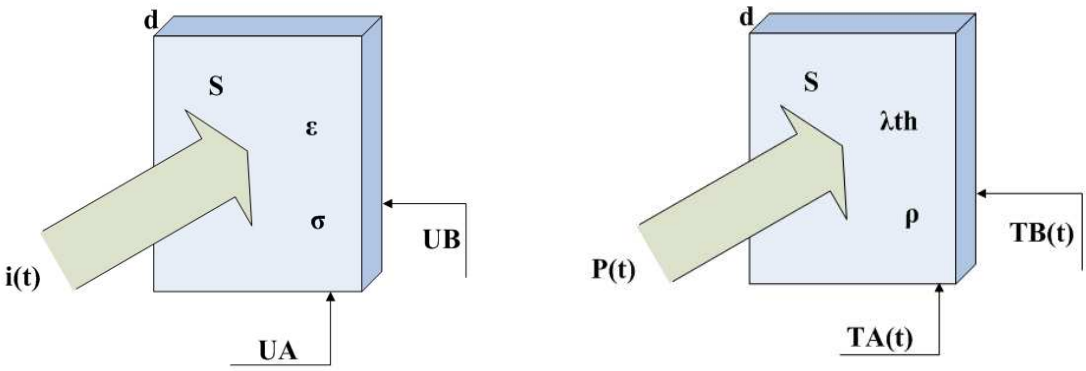
Electrical		Thermal	
Description	Units	Description	Units
Electrical potential difference	V (volt)	Temperature difference	T (celsus eller kelvin)
Stored charge	C ($Q(t) = \int_0^t i(t)\,dt$)	Stored heat	J ($Q(t) = \int_0^t p(t)\,dt$)
Electrical current	A ($i = \frac{C}{S}$)	Heat flow	W ($W = \frac{J}{S}$)
Electrical resistance	Ω ($R = \frac{d}{\sigma \times S}$)	Thermal resistance	$\frac{K}{W} or \frac{^\circ C}{W}$ ($R_{TH} = \frac{T}{W}$)
Conductivity	$\frac{1}{\Omega m}$ ($\sigma = \frac{A}{V \times m}$)	Thermal Conductivity	$\frac{W}{Km}$ ($\lambda = \frac{W}{T \times m}$)
Electrical capacitance	F ($\frac{A \times V}{S}$)	Thermal capacitance	$\frac{W \times S}{K}$ ($C_{TH} = \frac{P \times S}{T}$)
ohm's law	$\Delta V = I \times R$	ohm's law	$\Delta V = P \times R_{TH}$



(a)



(b)



(c) (d)

The thermal capacitance and thermal resistance in the analogy with the electrical transmission line equivalent circuit are considered as a variables related to the unit length as shown in Fig. 4.6. Moreover, in the thermal equivalent circuit, the electrical power source p(t) is stand for as a heat source.

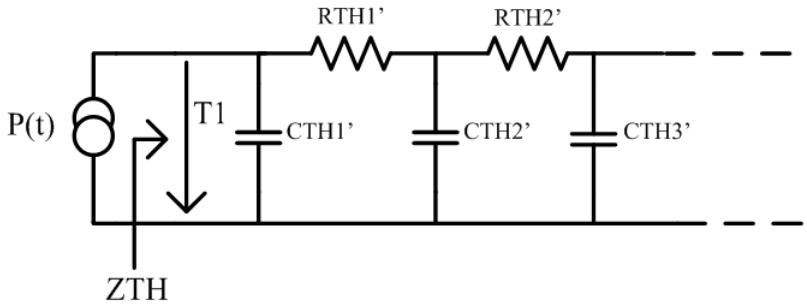


Fig. 4.6 thermal model

However, it is possible to simplify the model by considering each thermal capacitance and thermal resistance as a resistance and capacitance that is describing a homogeneous volume. Thus, a particular case can be represented by the segment structure as shown in Fig. 4.7.

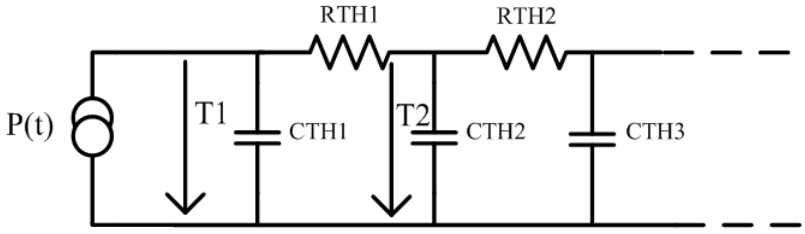


Fig. 4.7 Thermal segmented model of a real case

It is essential to know the differences between the electrical and thermal domains to avoid some misunderstandings. The first difference between these two domains is that the lumped circuit elements such as capacitors, resistors, inductors, etc. are allowed to be used in the electrical circuit analysis. That is due to the fact that the current path is defined by the current. Whereas, the heat flow is diffusing by one of the three heat transport mechanism from the heat source. However, the thermal lumped components such as thermal resistance and capacitance are used for thermal analysis. But, we should remember that many assumptions are made for simplification purposes.The second difference is that the isolating devices in electrical models are not required. However, it is important to include it in the thermal model to obtain a proper thermal model. The third difference is that the measuring tools of the thermal circuit and electrical circuit are shown

in Table 4.2 [7].

Table 4.2: Test and evaluation tools in electrical mode and thermal mode

Electrical domain	Thermal domain
Wattmeter	Heat flux meter
Oscilloscope	Infrared camera
Voltage probe	Thermocouple

4.1 Effective thermal impedance

4.1.1 Manufacturer's data

Understanding the transient behavior of the thermal response will help the designer to select the adequate heatsink [7]. Most electronics manufacturers provide the thermal parameters needed. For instance, the thermal resistance of the HUF75639G3 that is used in this project is shown in Table 4.3.

Table 4.3: Thermal resistances

Parameter	Symbol	Test conditions	MIN	TYP	MAX	Units
Thermal resistance junction to case	$R_{TH_{jc}}$	TO-247	-	-	0.74	$\frac{^\circ C}{w}$
Thermal resistance junction to ambient	$R_{TH_{ja}}$	TO-247	-	-	30	$\frac{^\circ C}{w}$

The thermal impedance consists of a combination of thermal resistance and thermal capacitance from junction to case of the semiconductor device. For a pulse train, as it is customary in practice, the manufacturer provides a graph showing the thermal impedance $Z_{th}(t)$ relative to the actual frequency and the duty cycle of the pulse train rectangular power dissipation in the component as is visualized in Fig. 4.8. On this curve we can see that for pulses t_p higher than $100ms$, the value of the thermal impedance tends to be equal to the value of the thermal resistance.

$$Z_{TH_{JC}}\Big|_{t_p \geq 100ms} \longrightarrow R_{TH_{JC}}$$

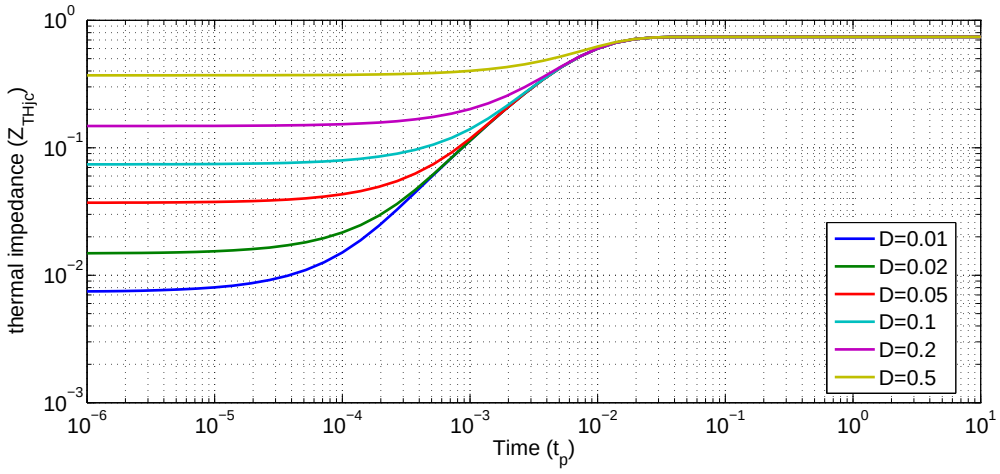


Fig. 4.8 Effective thermal impedance using only one thermal time constant

Fig. 4.9 shows the simplified thermal model used by MOSFET manufacturers

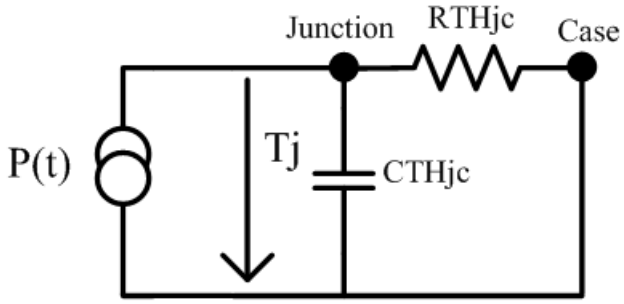


Fig. 4.9 Equivalent electrical model of the thermal system of a power component

4.1.2 Mathematical relationship

It should be noted that the temperature (T) is defined as an increase in temperature from a reference temperature T_{ref}.The equivalent thermal impedance value depends on the time when the heat source (P) is active and on the pulse train duty cycle.

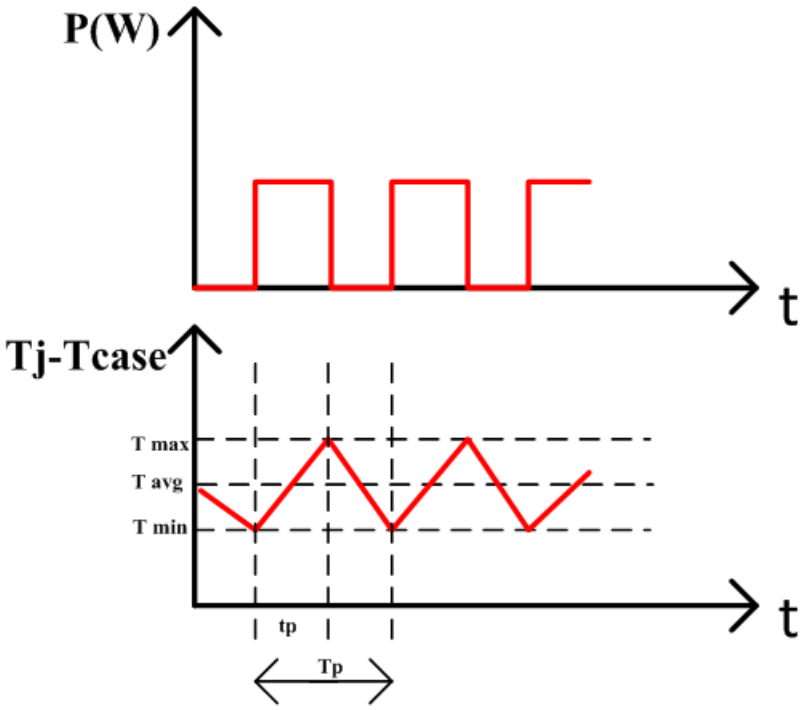


Fig. 4.10 Thermal response to a pulse train of heat

During the time t_p, the occurrence of power pulses, temperature, heat source side believes according to the relationship

$$T(t) = PR_{TH_{JC}} \left(1 - EXP(-\frac{t}{R_{TH_{JC}}C_{TH_{JC}}})\right) + T_{min}EXP(-\frac{t}{R_{TH_{JC}}C_{TH_{JC}}}) \tag{4.7}$$

During the absence of a heat source, the temperature decreases according to the relationship

$$T(t) = T_{max}EXP(-\frac{t}{R_{TH_{JC}}C_{TH_{JC}}}) \tag{4.8}$$

The maximum and minimum temperature can be found

$$T_{max} = T(t_o+t_p) = PR_{TH_{JC}} \left(1 - EXP(-\frac{t_p}{R_{TH_{JC}}C_{TH_{JC}}})\right) + T_{min}EXP(-\frac{t_p}{R_{TH_{JC}}C_{TH_{JC}}}) \quad (4.9)$$

$$T_{min} = T(t_o + T_p) = T_{max}EXP(-\frac{T_p - t_P}{R_{TH_{JC}}C_{TH_{JC}}}) \quad (4.10)$$

$$T_{min} = T_{max}EXP(-\frac{t_p(1-D)}{DR_{TH_{JC}}C_{TH_{JC}}}) \quad (4.11)$$

where $D = \frac{t_p}{T_p}$

Solving

$$T_{max} = PR_{TH_{JC}} \frac{1 - EXP(-\frac{t_p}{R_{TH_{JC}}C_{TH_{JC}}})}{1 - EXP(-\frac{t_p}{DR_{TH_{JC}}C_{TH_{JC}}})} \quad (4.12)$$

$$T_{min} = PR_{TH_{JC}} \frac{1 - EXP(-\frac{t_p}{R_{TH_{JC}}C_{TH_{JC}}})}{1 - EXP(-\frac{t_p}{DR_{TH_{JC}}C_{TH_{JC}}})} EXP(-\frac{t_p(1-D)}{DR_{TH_{JC}}C_{TH_{JC}}}) \quad (4.13)$$

If a duty cycle $D = 1$, the heat source (p) is constant

$$T_{max} = T_{max} = PR_{TH_{JC}} \quad (4.14)$$

The average temperature of the heat source is defined as

$$T_{max} = \frac{1}{T_p} \int_0^{T_p} T(t)\, dt \quad (4.15)$$

After some calculations

$$T = DPR_{TH_{JC}} \quad (4.16)$$

The definition of the thermal impedance is given by the following relationship

$$T_{max} = PZ_{TH_{JC}} \quad (4.17)$$

then

$$Z_{TH_{JC}} = R_{TH_{JC}} \frac{1 - EXP(-\frac{t_p}{R_{TH_{JC}}C_{TH_{JC}}})}{1 - EXP(-\frac{t_p}{DR_{TH_{JC}}C_{TH_{JC}}})} \quad (4.18)$$

The effective thermal impedance junction to case depends on the duration of conduction (t_p) and the duty cycle. This relationship can be illustrated by the graph in Fig. 4.8.

4.2 Thermal model development

4.2.1 General

Thermal modelling of a component is a complex operation involving finite element analysis. Such an approach is not realistic in most cases. Manufacturers can circumvent this problem by proposing values of thermal resistances and thermal capacitances by segmenting the volume of the component into several significant parts.

4.2.2 Segment structure of thermal model

Assumption and constraints

The practice shows that the segmentation of the semiconductor structure into partial volumes is not vital when the following features are considered:

1. The thickness and the succession of layers should be chosen so that the thermal time constant ($\tau = RC$) goes in ascending in the direction of heat propagation. A better result is obtained for a growth time constant by factor 2-8 between two layers [9].

2. If the silicon surface where heat is generated is smaller than the cross section of the conducting material, the effect of lateral diffusion occurs. Practice shows that heat propagation in homogeneous layer can be described by an angle of expansion ($\alpha = 40°$). There is one restriction if a layer has a low thermal conductivity (cumulative effect) [9].

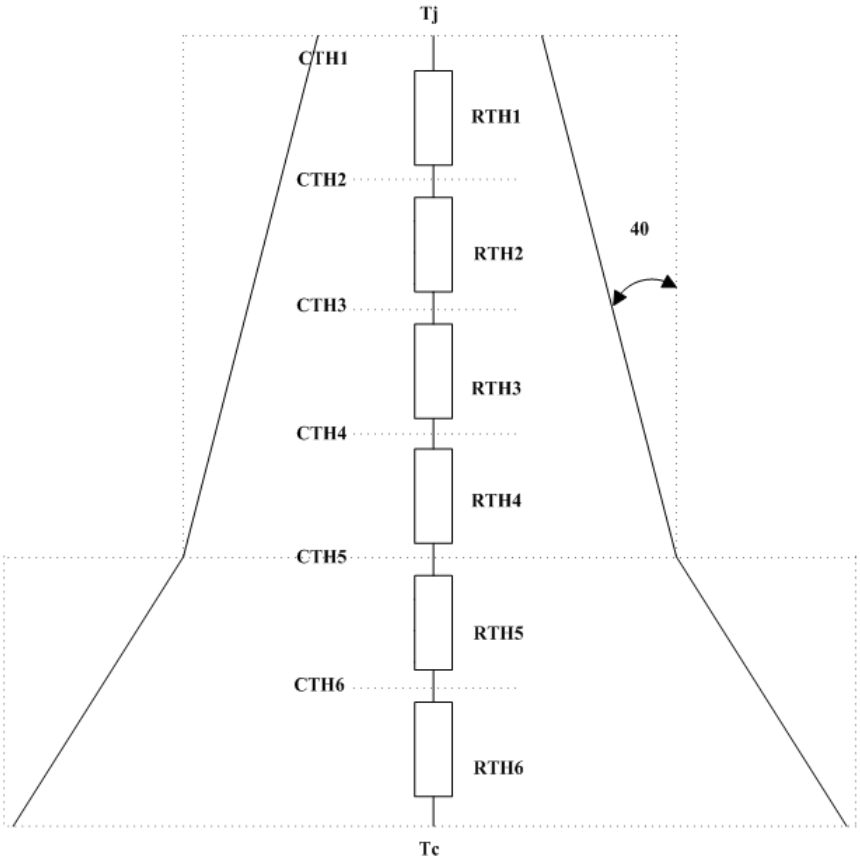


Fig. 4.11 Thermal model of a power MOSFET structure

3. Dimensions and thermal characteristics of each volume element traversed by the heat flux must be determined precisely. This is since if a short duration power dissipation pulses occur, the heat capacity of these layers has a major influence on the thermal impedance of the system. The equivalent circuit shows that the thermal capacitance of this volume always appears in parallel to the flow of heat [9].

   In power MOSFETs, the epitaxial layer and the array of the layers are corresponding to the heat source. For complex geometries, the thermal model is only being roughly estimated. In this case, it may be necessary to use a finite element analysis in order to improve the accuracy. It is also possible for a component, which is provided at least in the form of a prototype, to change the values of the equivalent circuit based on a measurement and comparison of the profile of junction temperature. The practical procedure is to heat the component with a specific power dissipation (P_D) until it reaches a stationary junction temperature (T_{j1}). In principle, knowledge of the temperature is given by an indirect measurement. Indeed, the temperature dependence of several parameters of the component is known. Usually the measuring voltage drop (V_F) of an integrated diode into the structure. By

removing the power dissipation (heat source), it is possible to plot the cooling curve $T_J(t)$. The transient thermal impedance is

$$Z_{TH}(t) = \frac{T_{j1} - T_j(t)}{P_i} \tag{4.19}$$

The transient thermal impedance contains the full description of the system thermal behavior. As a fist approximation, the system can be considered as linear as long as the temperature dependence of the specific materials is ignored. Once the transient thermal impedance known, it is possible to determine the junction temperature (T_J) for any power dissipation profile.

$$T_j(t) = T_o + \int_0^t p(\tau) dZ_{TH}(t-\tau)\, d\tau \tag{4.20}$$

where T_o is the initial temperature, $dZ_{TH}(t)$ is the derivative with respect to time of (4.19).'Differential of the step response of the thermal impedance (impulse response is not directly measurable' .

To be able to use the results of a measuring thermal simulation, it is necessary to find an equivalent electrical network whose step response describes the transient thermal impedance $Z_{TH}(t)$. If only the profile of the junction temperature (T_j) is of interest, there is an unlimited number of electrical equivalent networks to describe the cooling curve with an acceptable accuracy. There are two prevailing topologies:

(a) Fractional equivalent circuit

The first connection is called Fractional equivalent circuit or foster thermal equivalent circuit. Each layer in the MOSFET is represented by RC pairs. The thermal capacitance is connected in parallel to the thermal resistance as shown in Fig. 4.12 . By applying the two port analysis, the transfer function for this simple RC circuit is

$$H(S) = \frac{V}{I} = Z(S) = \frac{1}{G + CS} \tag{4.21}$$

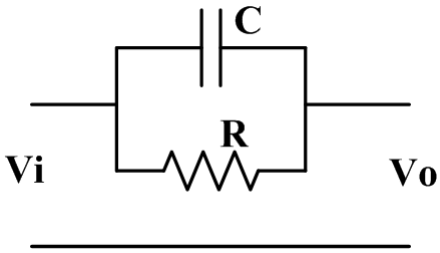


Fig. 4.12 Basic RC circuit

The cascade network is illustrated in Fig. 4.13. The originality of this system has a simple mathematical form where the step response thermal impedance is given by

$$Z_{TH}(S) = \frac{1}{G_{TH_1} + SC_{TH_1}} + \frac{1}{G_{TH_2} + SC_{TH_2}} + ... + \frac{1}{G_{TH_n} + SC_{TH_n}} \tag{4.22}$$

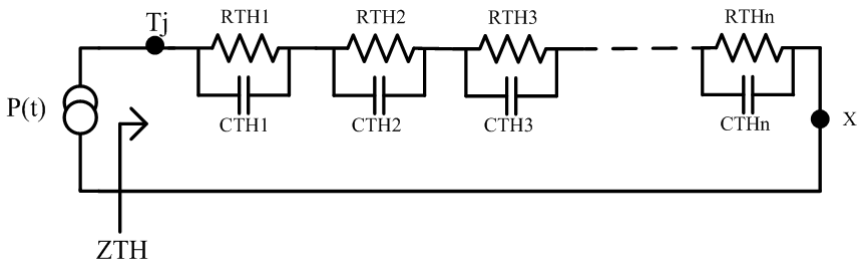


Fig. 4.13 Foster thermal equivalent circuit

This property simplifies the determination of the values of the equivalent circuit diagram and calculates its step response. This explains the popularity of this equivalent network. Therefore, this technique is supplied by most of data sheets [4].
This network must be considered as a 'black box ' . So, it is possible to correctly describe the curve of the junction temperature at the input terminal of the black box. However, the internal nodal voltage of the equivalent circuit cannot describe the real temperature distribution. Moreover, the internal network structure has no physical meaning. Therefore, it is impossible to access the network at point X to extend (such as with the thermal equivalent circuit of heat sink). In this case, the entire system has to be measured. Then, all the values of thermal resistances and capacitances need to be recalculated [9].

This assertion can be removed as follows. Open node X to replace the equivalent circuit of a heat sink as a couple of R_{TH}, C_{TH} and assume a temperature step (T_j) at the input node. Immediately at the output of this network, this temperature step would appear in differentiated form. This is due to the capacitor of the network (capacitive divider) which is physically impossible. However, in reality, the storage energy in the thermal capacitor depends on the volume element absolute temperature. In this network, the stored energy is proportional to the difference between two nodes. As a result, if the thermal description extension is needed, this network equivalent circuit is unsuitable to use it in the simulation model [9].

(b) Natural equivalent circuit

The circuit of heat conduction is called natural equivalent circuit or Cauer thermal equivalent circuit which is derived from the theory of the transmission lines. The thermal capacitance is connected in the node between two thermal resistances and the reference point as shown in Fig. 4.15. The reference temperature in the thermal circuit is selected to be zero. Moreover, the ambient temperature is modeled as a temperature source. This network describes only the temperature distribution between equivalent elements and the physical elements (Chip, si substrate , Isolation layer, Solder layer, Base plate, Thermal grease, etc) correctly [4]. The transfer function for the basic element of the Cauer network (see Fig. 4.14) is

$$H(S) = \frac{V}{I} = Z(S) = \frac{1}{G + CS} \tag{4.23}$$

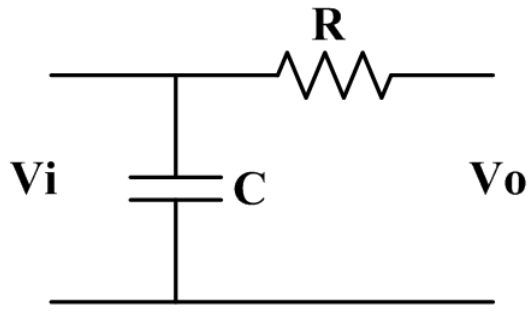


Fig. 4.14 Basic thermal RC circuit

For a cascade Cauer network as illustrated in Fig. 4.15, the impedance is

$$Z_{TH}(S) = \frac{1}{SC_{TH_1} + \frac{1}{\frac{1}{G_{TH_1}} + \frac{1}{SC_{TH_2} + \frac{1}{\frac{1}{G_{TH_2}} + \frac{1}{SC_{TH_3} + \ldots + \frac{1}{\frac{1}{G_{TH_n}}}}}}}} \tag{4.24}$$

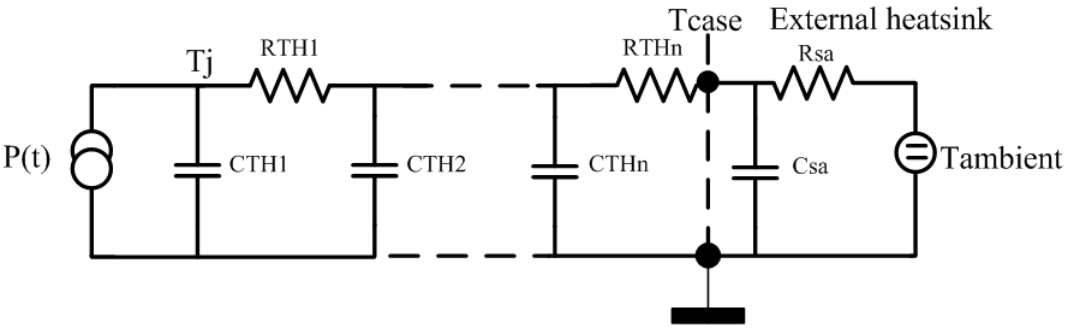


Fig. 4.15 MOSFET Cauer network

Chapter 5

Temperature measurement

5.1 Temperature measurement

A resistance-temperature detector (RTD) 'is a temperature sensing device whose resistance increases with temperature ' [12]. In industrial application, there are three types of RTD sensors constructions can be used; coil , thin film , and wire$-$wound.

Different metals can be used for the construction of RTD sensors such as Platinum, Copper, or Nickel. However, Platinum is the most popular RTD sensor. This is due to that the Platinum has relatively linear resistance-temperature curve over a wide temperature range. While, Copper and Nickel RTD have a limited temperature range. To define the resistance-temperature relationship, the Callendar-Van Dusen equation is commonly used [21].

$$R_t = R_o[1 + At + Bt^2 + C(1 - 100)t^3] \tag{5.1}$$

where

R_t: RTD resistance at temperature (T).
R_o: RTD resistance at 0 °C.
A, B, C: Callendar-Van dusen coefficients.
t: temperature (°C).

The constant C is zero above 0 °C. Solving (5.1) for t we get

$$t = \frac{-R_o \times A + \sqrt{((R_o \times A)^2 - 4 \times B \times (R_o - R))}}{2 \times R_o \times B} \tag{5.2}$$

Another important parameter is the resistance-temperature coefficient which is described as [6].

$$\alpha = \frac{R_{100} - R_o}{100 R_o} \tag{5.3}$$

Based on the international practical scales, the Platinum RTD can be represented by one of three standardized curves as shown in Table 5.1 [21]- [10].

Table 5.1: Callendar-Van Dusen constants

Standard	Temperature coefficient	A (C^{-1})	B (C^{-2})	C (C^{-3})
DIN 43760	0.003850	3.908×10^{-3}	-5.8019×10^{-7}	-4.2735×10^{-12}
American	0.003911	3.9692×10^{-3}	-5.8495×10^{-7}	-4.2325×10^{-12}
ITS	0.003926	3.9848×10^{-3}	-5.870×10^{-7}	-4.0000×10^{-12}

A typical resistance-temperature curve for a PT1000 element is shown in Fig. 5.1, where $\alpha = 0.003850$ and the PT1000 resistance at 0 °C is 1000 Ω.

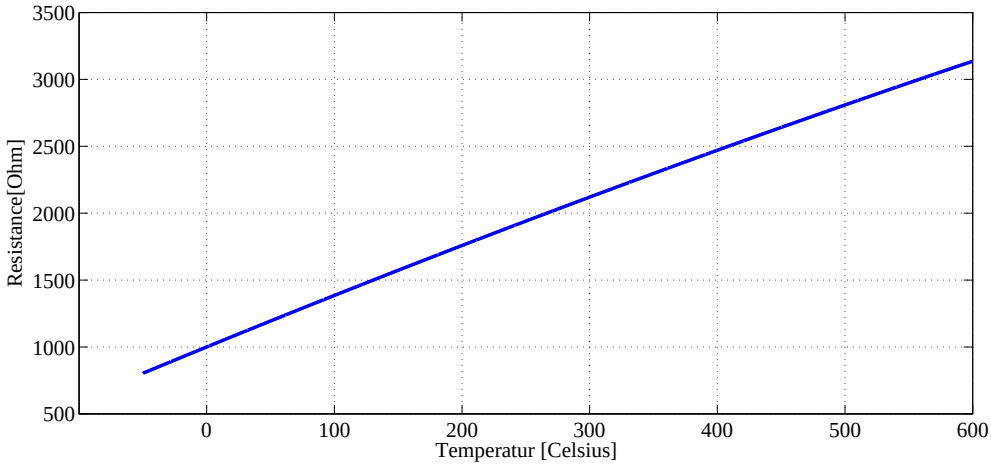


Fig. 5.1 Typical characteristics of a PT1000 element

5.2 RTD measurement circuit

To measure the resistance of the PT1000 element, a known current is passing through it. Then the voltage across the device is measured. Thus, the resistance of the PT1000 element can be computed by knowing both the current and voltage. Then, this resistance is used for temperature calculation.

A Wheatstone bridge is another method to calculate the resistance of a RTD. The Wheatstone bridge consists of four resistors as shown in Fig. 5.2. Three of them are fixed resistors. However, the fourth is a variable resistor. A constant voltage V_{in} is applied to Wheatstone bridge [13].

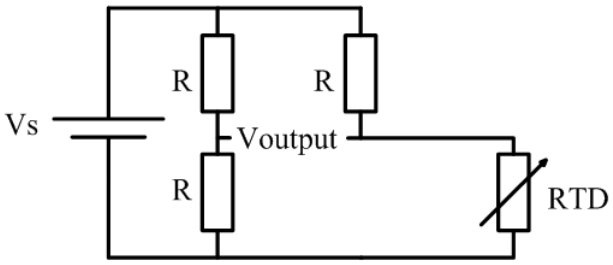


Fig. 5.2 Wheatstone bridge circuit

$$V_{output} = V_b - V_a = V_{in}\frac{RTD}{R+RTD} - V_{in}\frac{R}{2R} \tag{5.4}$$

$$= \frac{V_{in}}{2}[\frac{RTD}{R+RTD} - \frac{R}{R+RTD}] \tag{5.5}$$

Therefore, any variation in the PT1000 resistance results a variation in the V_{output} of the Wheatstone bridge as shown in Fig. 5.3.

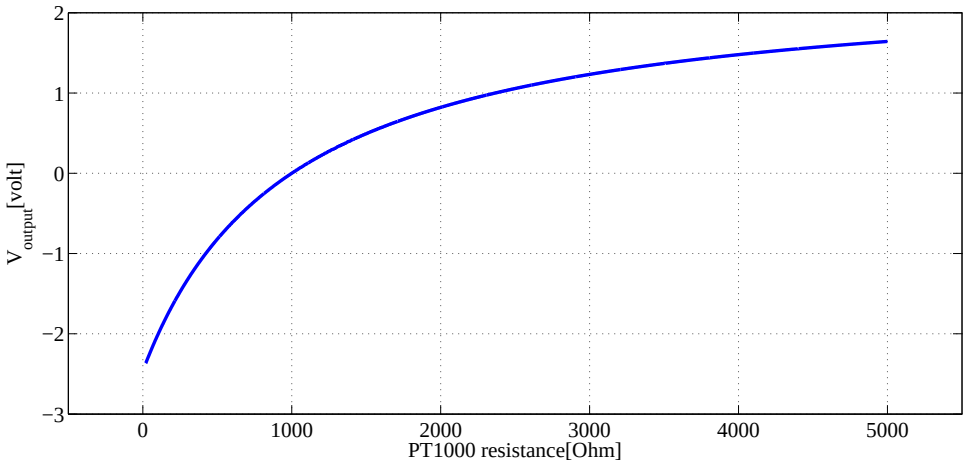


Fig. 5.3 Voltage versus temperature

A simple temperature measurement circuit is designed in this project. The overall temperature measurement system is presented in Fig. 5.4.

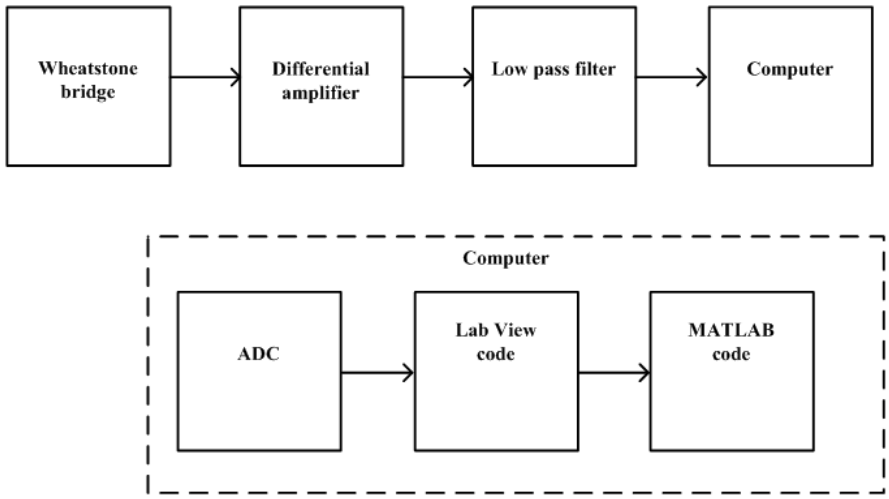


Fig. 5.4 Voltage versus temperature

The input to the system is a PT1000 device. At 0 °C, the output voltage of Wheatstone bridge is designed to be zero. The PT1000 converts the change of the temperature to a resistance change. Therefore, the Wheatstone bridge becomes unbalance due to this resistance change. As a result the output voltage of the Wheatstone bridge will deviate from zero. Generally, this change in the output voltage is small. So, a differential amplifier with a specific gain is used to increase the output voltage level. A simple RC low pass filter to eliminate the possible interference on the amplifier output whose frequencies above the cut-off frequency of the low pass filter as shown in Fig. 5.5 will be used.

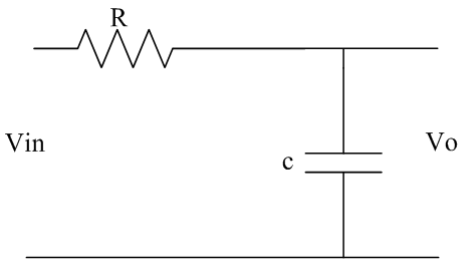


Fig. 5.5 Passive low pass filter

The transfer function of the low pass filter is described by

$$H(S) = \frac{V_o(S)}{V_i(S)} \tag{5.6}$$

The Laplace domain description for the RC filer transfer function is

$$H(S) = \frac{\frac{1}{RC}}{S + \frac{1}{RC}} \tag{5.7}$$

where, S is a complex number.
For sinusoidal signals, S can be approximately equal to (jw).

$$S \sim jw \tag{5.8}$$

By substituting (5.8) in (5.7) we get

$$H(S) = \frac{\frac{1}{RC}}{jw + \frac{1}{RC}} \tag{5.9}$$

where j is complex coefficient, and w is radian frequency (rad/sec). Then the numerator is just a real part. While, the denominator is a complex number. Finding the magnitude, the numerator is just a real number. However, to find the magnitude of the denominator, the standard process is followed by taking the square root of the summation of squaring both real and t imaginary part .

$$|H(jw)| = \frac{\frac{1}{RC}}{\sqrt{w^2 + (\frac{1}{RC})^2}} \tag{5.10}$$

This equation is described the low pass filter because

- If $w = 0$ which is basically a DC input, The amplitude is equal to 1.
- If $w = \infty$ which means a high frequency signal, The magnitude will become zero.
- If $w = \frac{1}{RC}$ which is called the cut-off frequency, the magnitude decreases by -3db or goes to 0.707 point.

In another word, this transfer function passes low frequencies and rejects high frequencies. The corresponding phase shift angle of the low pass filter can be obtained according to

$$\angle H(jw) = -tan^{-1}(\frac{w}{RC}) \tag{5.11}$$

A Lab view program is used to enable the user to plot the values of the temperature over the time on a waveform chart. Moreover, it shows the final values of the temperature and the output voltage from the measurement board . The Lab view code is designed to store the previous values. Therefore, the user can see the change of the temperature over the time.

5.3 Temperature measurement case set-up

A platinum-chip temperature sensor (PCA style PT1000) is selected to measure the temperature of the MOSFET device since it has fast response and linear characteristics. Table 5.2 illustrates some specifications of the PT1000 device.

Table 5.2: PT1000 specification

Type	Inaccuracy	Temperature coefficient	Measuring range	Resistance range	Dimension L*W*H
PT1000	Klass A	$3.850 \times 10^{-3}(^{\circ}C^{-1})$	(-70 to 600)(°C)	20-5000 (Ω)	$5 \times 1.5 \times 1$ (mm)

The deviation limit of class A PT1000 is defined according to

$$\Delta T = \pm(0.15 + 0.002 \times T) \tag{5.12}$$

For instance, the measurement tolerance at 0°C temperature is ± 0.15°C . However, the tolerance at 100°C is ± 0.75°C.

The Wheatstone bridge which is visualized in Fig. 5.2 is balanced only if the values of the resistors are equal according to (5.5). As mentioned above, the Wheatstone bridge is designed to be balanced at 0°C. Thus, the values of the resistors (R) is selected to be (1000Ω). Since the value of the PT1000 element is 1000Ω at 0°C. The input voltage of the Wheatstone bridge is $5V$. From the PT1000 specifications, the resistance range of the PT1000 element is $(20 - 5000)\Omega$. Therefore, the output voltage of the Wheatstone bridge is negative if the PT1000 resistance value $(20 \leqslant RTD < 0)\Omega$. However, the output voltage is positive if the resistance of the PT1000 is in the range $(0 < RTD \leqslant 5000)\Omega$. In another word, the negative voltage implies a negative temperature is measured but the positive output voltage means a positive temperature is measured.

An accurate and low noise instrumentation amplifier INA122 has been chosen for the purpose is shown in Fig. 5.6.

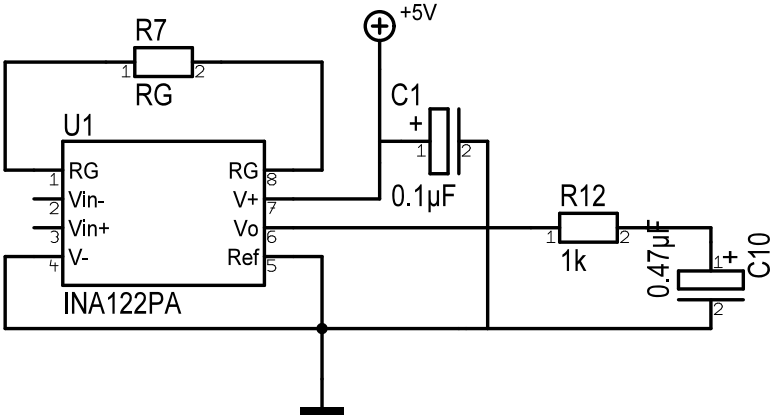


Fig. 5.6 $INA122$ pin configuration and connection

The device is operated with a $5V$ dc power supply. To keep the power supply voltage stabilized, a 0.1μF is connecting to ground. The output voltage V_o is the difference between the two inputs V_{in+} and V_{in-} with a specific gain [15].

$$V_o = (V_{in+} - V_{in-})G \tag{5.13}$$

where V_{in+} is the input voltage at pin 3, V_{in-} is the input voltage at pin 2, G is the gain of instrumentation amplifier. The voltage level from the Wheatstone bridge is amplified by an instrumentation amplifier when the voltage from the bridge is in the mV range, and this requires a high resolution for accurate A / D

conversion. This amplifier has a gain level (G) which is determined by the value of the external resistor R_G according to the following equation

$$G = 5 + \frac{200K}{R_G} \tag{5.14}$$

where, the $200k\Omega$ is the internal resistor of INA122. The gain that can be obtained is varied from 5 to 20 as shown in Table 5.4 . In the practical measurement circuit, the INA122 with gain 5 is selected. Therefore, the external resistor R_G is not connected.

Table 5.3: The gain of instrumentation amplifier for different R_G values

Desired Gain	$R_G(\Omega)$
5	NC
10	40 K
20	13.33 K
50	4444
1000	201
10000	20

The value of R and C of low pass filter is selected (1000Ω, $0.47mF$). Thus, the cut-off frequency f_c Hz is obtained according to (5.16).

$$w_c = \frac{1}{RC} = 2127.66rad/sec \tag{5.15}$$

$$f_c = \frac{1}{2\pi RC} = 338.63Hz \tag{5.16}$$

Fig. 5.7 and Fig. 5.8 shows the Matlab Simulation for low pass filter.

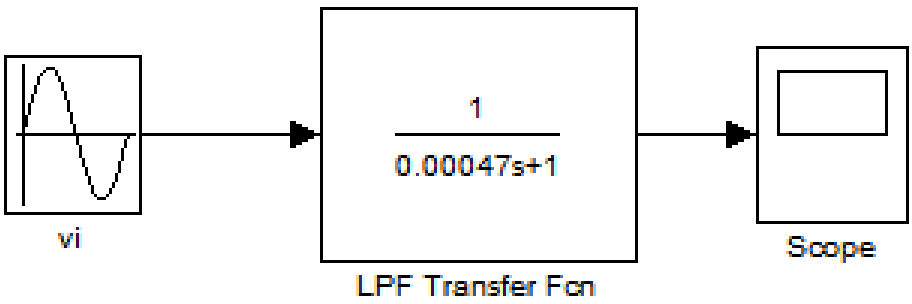


Fig. 5.7 Step-down converter

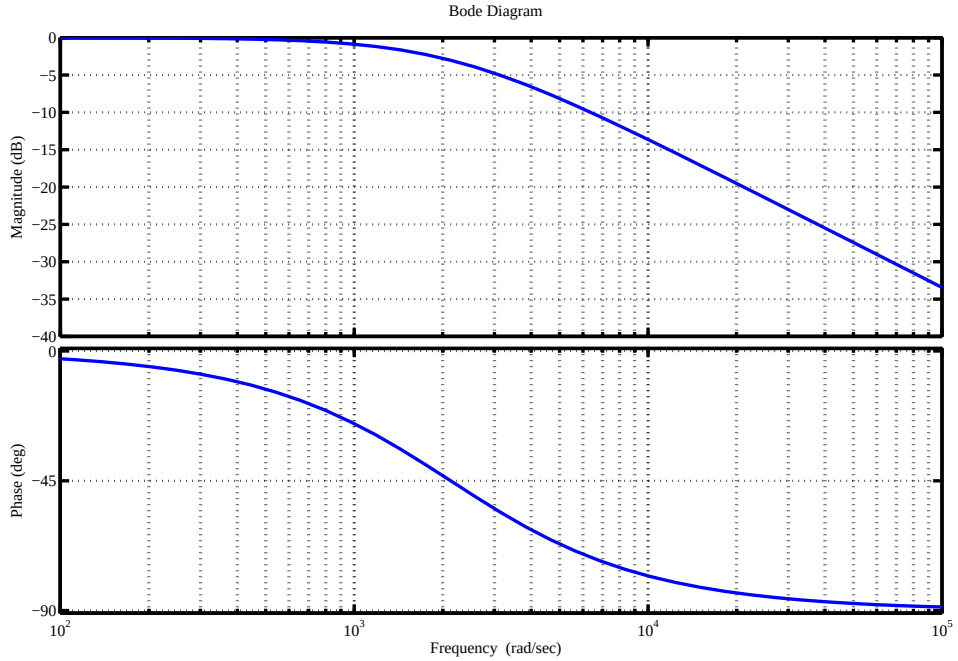


Fig. 5.8 Step-down converter

Table 5.4 visualizes the temperature and the voltages for different values of the PT1000 resistance.

Table 5.4: Practical measurement

$RTD(\Omega)$	V_{output}(bridge)	V_{output}(instrumentation amplifier)	V_{output}(L.P.F)	Temperature (°C)
1079	0.096	0.49	0.49	20.3
1118	0.141	0.704	0.704	30.4
1308	0.332	1.68	1.68	79.7

5.4 Printed circuit Board

The PCB is used to connect the electrical components electrically by using copper traces on an isolated layer. The PCB is usually glued on the substrate to protect the copper from the oxidizing. To arrange a PCB design requires a lot of knowledge about layout design. In this project a two layer PCB is designed for temperature measurement. The top layer is selected for the positive supply voltage and the bottom layer is selected for the ground. Many copper traces across the PCB from the top layer to the bottom layer is made by drill holes which may create a stray inductance.

Target 3001 is a CAD software which is used to convert a schematic circuit to a PCB layout. This software is provided in Germany by the IBF company. The software provides schematic blocks and the actual size of many component in the library. However, if the component is not available in the library, the user has to create the schematic block and figure out the actual size of this component. In the schematic layer, all the components are put in their desired positions and are connected by the copper traces. The color of the connecting copper line is green if the connection is correct otherwise the color of the connection line is cyan if the line is unconnected.

When the design is completed, the user goes from the schematic to the PCB viewer. In the PCB view, the components are put on the correct positions, the width of the copper traces are fixed according to the currents that are passing through these copper traces, and the diameter and the thickness of the drill holes

are specified. The size of the PCB is $(95.25 \times 137.43)mm$.The 3D PCB designed is visualized in Fig. 5.10.

Fig. 5.9 shows the circuit configuration of five channels which is used to measure the temperature. The input voltage to the PCB is applied through a $9v$ battery. A three terminal regulator (μA78L00) is used to regulate the voltage to $4.932V$. Three capacitors ($0.33nF$, $10\mu F$,$100\mu F$) are placed on the regulator output to smooth the dc link voltage.

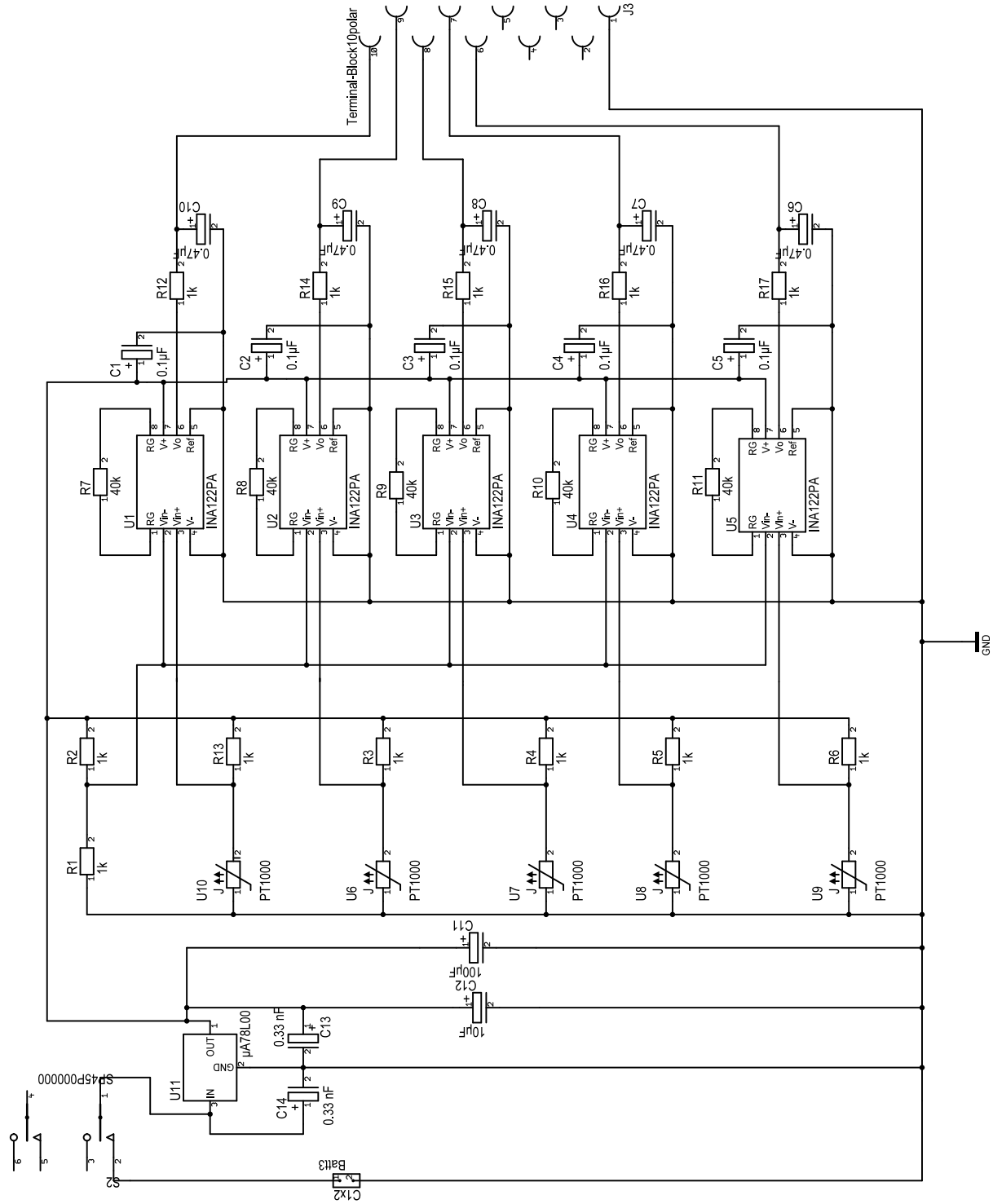


Fig. 5.9 Temperature measurement schematic circuit

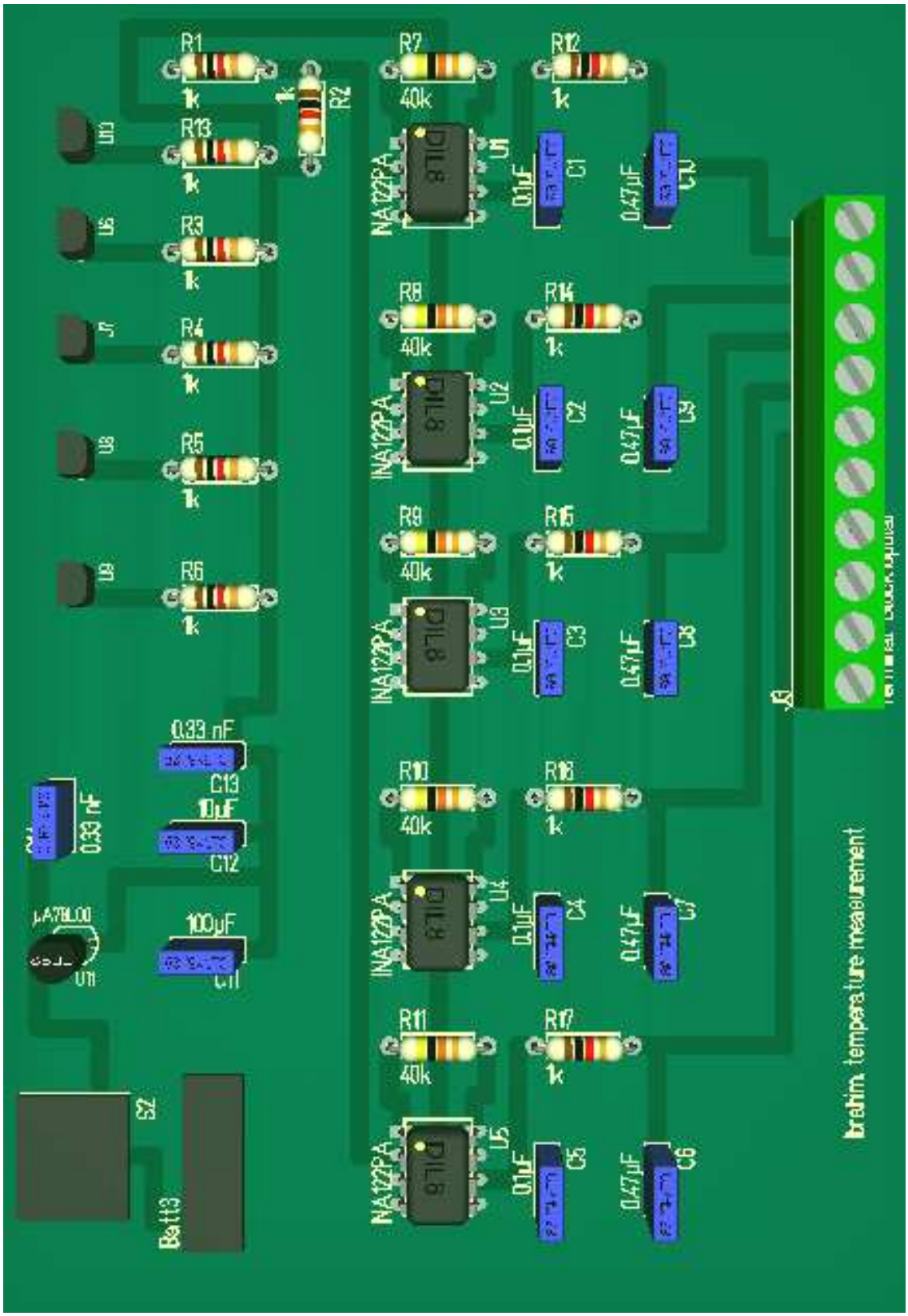


Fig. 5.10 Temperature measurement PCB layout

5.5 Lab view

In this work, two measurement circuits are used. The voltage signal from each channel in the measuring circuit is connected to a control panel via a coaxial cable which in turn is connected to an ADC of a computer. To save the continuous change of the voltage of each channel over the time, a Lab view software is used as it is visualized in Fig. 5.13 . The LAB VIEW program is designed as a while-loop that for each iteration obtains 1,000 samples from each channel. A mean function in the program is used to average these samples and then write them to a text file with 8 columns, one column for each channel as shown in Fig. 5.11.

Fig. 5.12 shows the control panel of the Lab view program in which the last mean voltage value of each channel is given. The sampling frequency is selected to 1000 Hz, which means that each iteration in the while loop is one second. When the desired time is reached, the stop button in the control panel is pressed to interrupt the while-loop and stop the program.

CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0.576165	0.565332	0.559326	0.580979	0.573459	0.566484	0.564116	0.559536
0.576138	0.565303	0.559309	0.580957	0.573425	0.566428	0.563904	0.559507
0.576152	0.565388	0.559397	0.581003	0.573430	0.566406	0.563850	0.559585
0.576104	0.565435	0.559438	0.580845	0.573384	0.566426	0.564004	0.559590
0.576108	0.565383	0.559536	0.581033	0.573374	0.566533	0.563958	0.559595
0.576035	0.565398	0.559673	0.580959	0.573376	0.566567	0.563979	0.559646
0.576116	0.565461	0.559673	0.580950	0.573523	0.566445	0.563965	0.559792
0.576123	0.565161	0.559678	0.580928	0.573457	0.566543	0.563984	0.559812
0.576123	0.565085	0.559600	0.581069	0.573489	0.566531	0.563950	0.559653
0.576106	0.565105	0.559685	0.580999	0.573579	0.566475	0.563962	0.559824
0.576147	0.565229	0.559795	0.581013	0.573352	0.566514	0.563933	0.559797
0.576140	0.565337	0.559680	0.581016	0.573477	0.566475	0.563936	0.559912
0.576116	0.565361	0.559780	0.581084	0.573547	0.566631	0.563999	0.559932
0.576150	0.565457	0.559863	0.580972	0.573542	0.566582	0.564087	0.560210
0.576165	0.565625	0.559902	0.580942	0.573508	0.566587	0.564033	0.559917
0.576169	0.565898	0.560115	0.581018	0.573511	0.566729	0.564182	0.560186
0.576140	0.565969	0.560022	0.581033	0.573518	0.566636	0.564063	0.560168
0.576152	0.566013	0.560122	0.581045	0.573606	0.566758	0.564080	0.560122
0.576167	0.566096	0.560034	0.581001	0.573643	0.566589	0.564041	0.560159
0.576157	0.566033	0.560012	0.580996	0.573608	0.566689	0.564060	0.560095
0.576189	0.565986	0.560015	0.580959	0.573621	0.566655	0.564050	0.560266
0.576050	0.566106	0.560186	0.580986	0.573643	0.566748	0.564070	0.560208

Fig. 5.11 Example of 22 samples of 8 channels

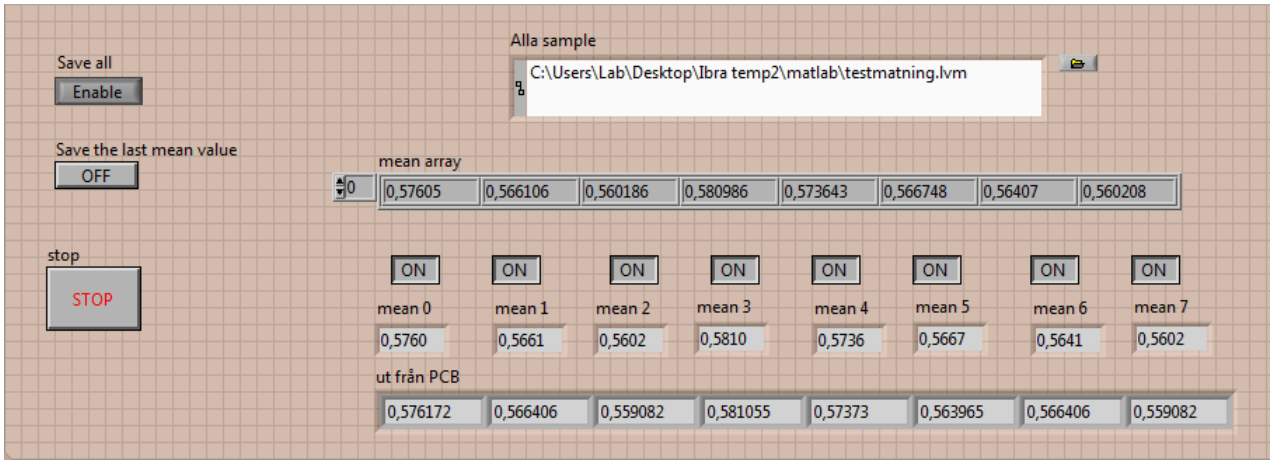


Fig. 5.12 Control panel of Lab view

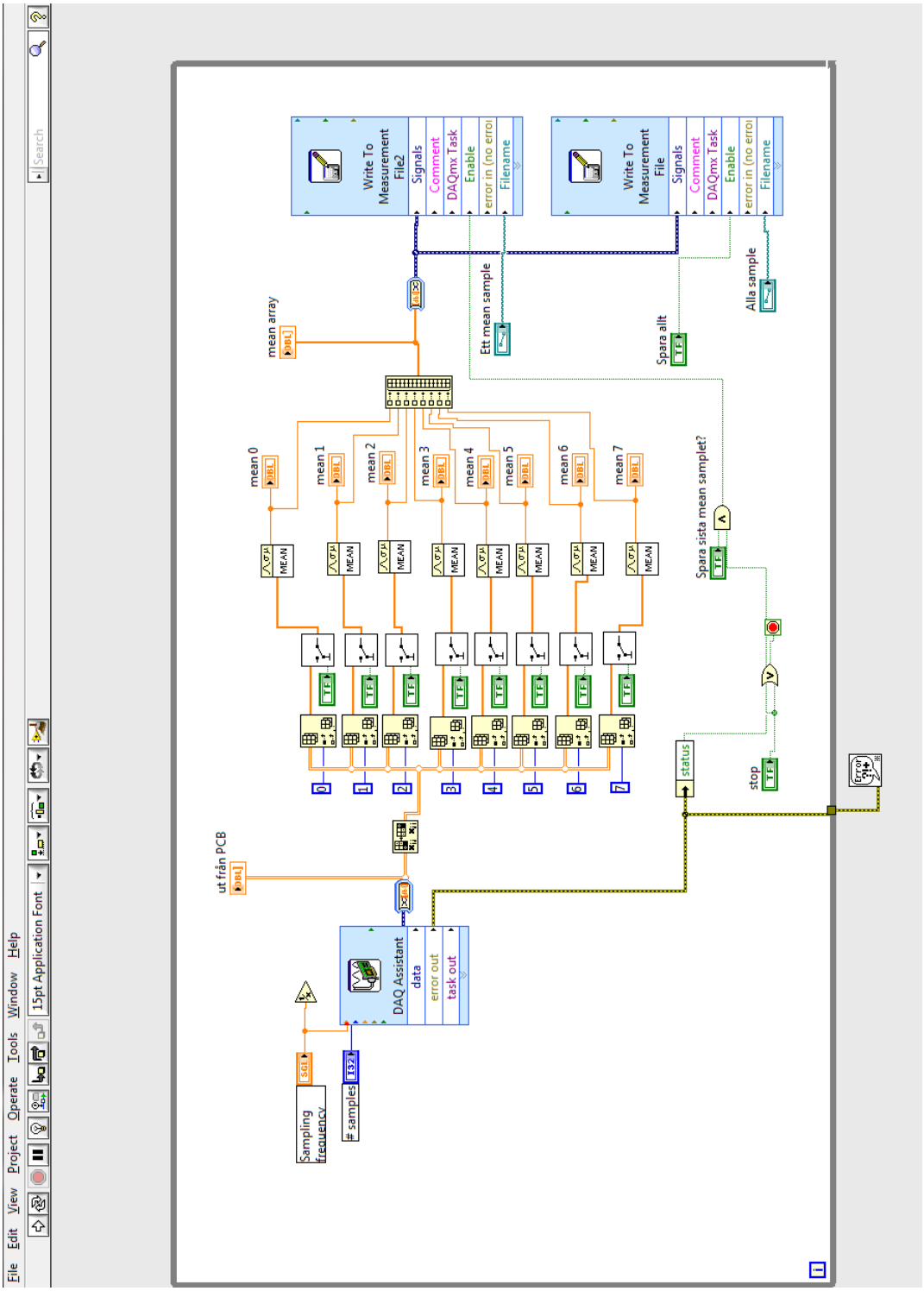


Fig. 5.13 Block diagram in Lab view

All collected data from Lab view must now be treated mathematically to derive a temperature. Ideally, two steps are used to determine the temperature:

$Step1$ The resistance of the PT1000 element is calculating according to the following equation.

$$R_{PT100} = \frac{\frac{V_{channel}}{4.933*5} + 0.5}{0.5 - \frac{V_{channel}}{4.933*5}} \tag{5.17}$$

The collected data of each channel has to be divided by 5 which is the gain of the instrumentation amplifier.

$Step2$ After knowing the resistance of the thermometer, the temperature can be calculated according to

$$T_{PT100} = \frac{-a + \sqrt{a^2 - (4 \times b \times (1 - \frac{R_{PT1000}}{1000}))}}{2 \times b} \tag{5.18}$$

a and b are selected according to Table 5.1

a= 3.908×10^{-3} .

b= -5.8019×10^{-7} .

The equations in $Step1$ and $Step2$ are easily be implemented in MATLAB to obtain the ideal temperature over time curve. Fig. 5.1 illustrates that the PT1000 resistance increases linearly with the temperature. This means, for instance that, all wires have zero internal resistance, all the resistors which are used in the measurement circuit board are 100% identical, and all the components are ideal. But this is not the case since the results from the measurement circuit is far from linear due to non-negligible differences between the channels. In order to obtain reliable results, the PT1000 element must be calibrated against a reference temperature. This process is described in Sec. 5.6.

5.6 Calibration

The calibration is a comparison between the theoretical results of the device and the results from the device under the test. When all the PT1000 resistance are placed in a uniform known temperature, different voltage levels are recorded in each channel for the various different temperature. This indicates that the circuit has characteristics that are far from the ideal case which is described in the previous section. Therefore, this theory can not be used to measure the voltage. As a result, the system must be calibrated to obtain the most exact measurement. The voltage from each channel must be registered for different temperatures. Then, a mathematical temperature function ($T = f(v)$) curve in Matlab is adapted to these points. An external thermometer with an uncertainty of measurement ($-0.5°C$). To ensure that the reference temperature and the sensors are in the same ambient temperature, an environment with absolutely homogeneous temperature should be created. This is achieved by putting all the PT1000 sensors and the external temperature sensor together in a Thermos filled with water. Boiled water is poured into the Thermos. After 5 minutes, when the temperature has stabilized, the voltage levels of all channels and the external thermometer temperature are registered. By pouring in a small amount of cold water, stirring in the Thermos, an extended temperature range can be obtained. As the temperature stabilizes again, new voltage levels and the current temperature of the external thermometer is recorded again. This process is repeated for the range of $15 - 95°C$. The temperature references are chosen arbitrarily over the measurement interval.

Fig. 5.14 shows the difference between the theoretical temperature against the voltage which is obtained by implementing (5.17) and (5.18) in MATLAB and the other is the curve fitting of the data points for one channel of the measurement circuit. The curve fitting is drawn in Matlab by forming two vectors, one for the temperature of the thermometer and the other for the voltage levels of each channel. Then, a quadratic function is used to create the temperature against the voltage curve since it matches the calibration points properly. Therefore, each channel in the measuring circuit has an associated temperature function which is only valid for that channel.

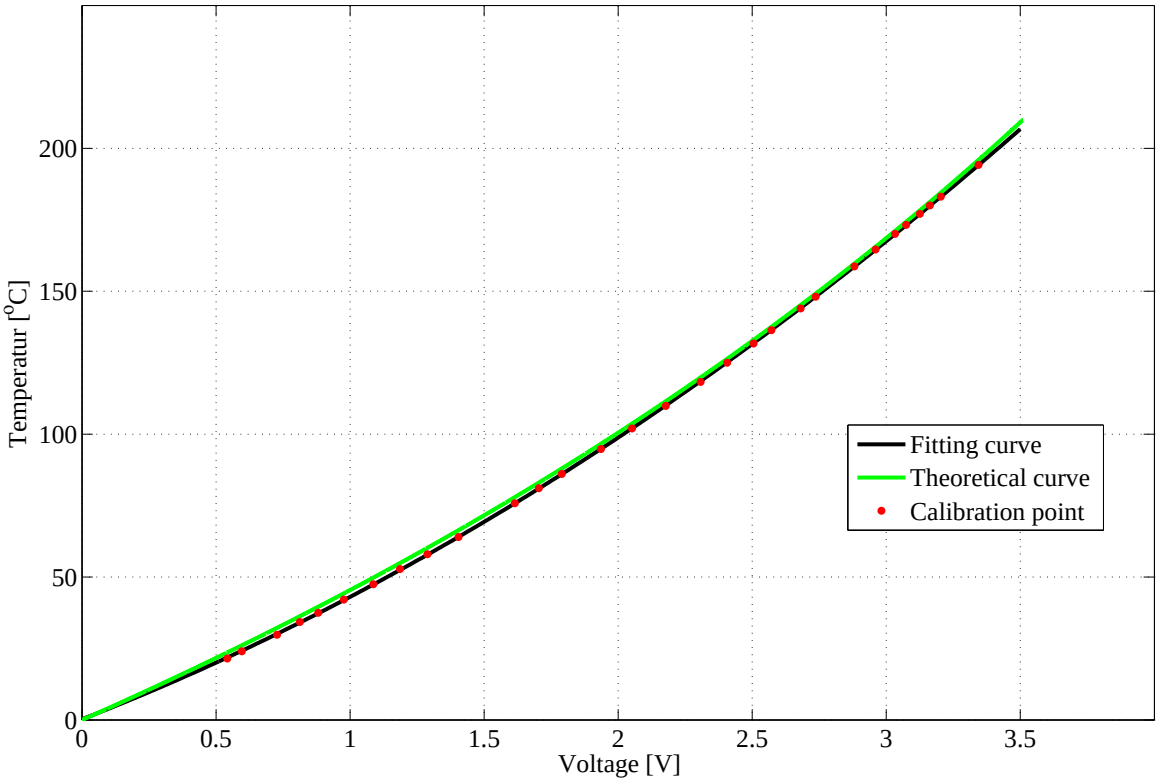


Fig. 5.14 Temperature VS. voltage comparison of ideal and fitting curve

Chapter 6

Experimental set-up and simulation analysis

6.1 Experimental set-up

In this section, three different tests are performed to measure the case temperature, heat sink temperature, ambient temperature. Then the junction temperature is calculated, estimated, and plotted versus the drain current.

In this work, the power dissipation is dominated by pure conduction losses which are caused by the drain current and the on-state resistance of the MOSFET. The change of the on-state resistance and the amount of heat that flows out of the MOSFET device affect the amount of current which can be switched successfully by the device. There is no switching loss included in this experiment because it is difficult to read the on-state value accurately during the switching transient. The test circuit that is used in the experiment is shown in Fig. 6.1.

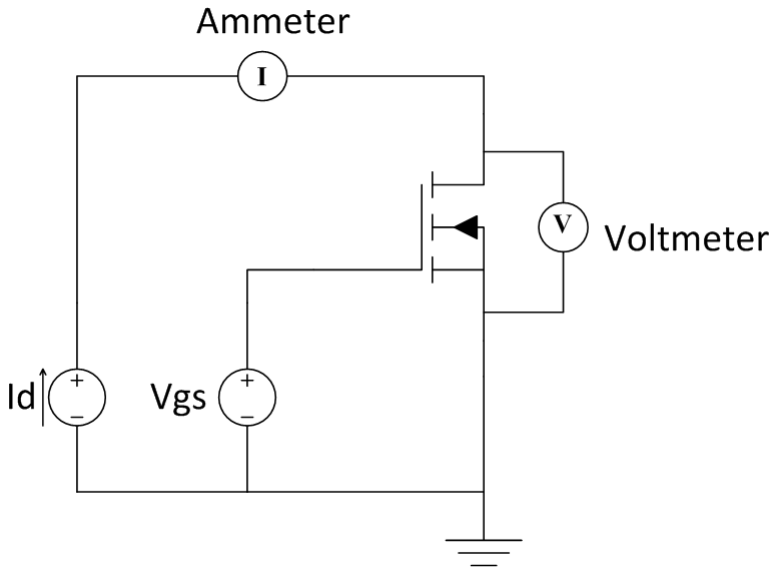


Fig. 6.1 Circuit arrangement for temperature measurement

The circuit consists of two voltage sources. The first voltage is connected between the gate and source of the device and it is selected to be higher than the threshold voltage ($V_{gs_{th}}$) to keep the MOSFET on. The second voltage source acts as a current source. This is used to set the drain current that flows in MOSFET in order to heat up the device. Heat sink and case temperature have to be stabilized. Therefore, the drain current is driven continuously for (60 minutes).

The drain-source voltage and the drain current are measured by using an accurate voltmeter with sub-mill volt and ammeter with sub-milliamp respectively as shown in Fig. 6.1. The power dissipation is calculated by multiplying the drain-source voltage by the drain current.

$$P_d = I_d V_{ds_{on}}(T_j) \tag{6.1}$$

The drain -source voltage depends on the junction temperature. As it is mentioned above only the DC operation mode is tested, therefore, the drain-source voltage is recorded at the steady state (after 60 minutes). The internal temperature of MOSFET rises due to the power dissipation that flows out of the device. This heat is affected both the performance and reliability of the MOSFET [19]. The junction temperature is calculated by using the following equation

$$Tj = P_d(R_{TH_{jc}} + R_{TH_{cs}} + R_{TH_{sa}}) + T_{ambient} \tag{6.2}$$

where ($R_{TH_{jc}}$ is the junction to case thermal resistance, $R_{TH_{cs}}$ is the case to heat sink thermal resistance, ($R_{TH_{sa}}$ is the heat sink to ambient thermal resistance, and $T_{ambient}$ is the ambient temperature.

6.2 Simulation analysis using PLECS

Comparing the simulation results with the measurement results obtained from the experiment is the best way to validate our thermal model. A one dimensional thermal equivalent circuit is modeled. However, the heat transfer by radiation is not included in the simulation for simplicity. The radiation power dissipation is such a small object is low that can be neglected safely. Table 6.1 shows the radiation power dissipation for both heat sinks which are used in this project.

Table 6.1: Radiation power dissipation

Small heat sink (test 1)			Big heat sink (test 2)		
$Theatsink$	$Tambient$	$P_{radiation}$	$T_{heatsink}$	$T_{ambient}$	$P_{radiation}$
35.31	28.23	0.000171068	30.55	28.95	0.00607308
41.82	29.06	0.000436424	33.28	29.64	0.00163811
50.14	29.77	0.001029842	35.76	29.65	0.003105783
65.75	32.14	0.003278806	41.09	30.24	0.007254456
82.4	31.19	0.008401671	45.23	31.06	0.011719988

PLECS(symbole) is the Simulink program that is used for modeling our thermal network. PLECS (Piecewise Linear Electrical Circuit Simulation) is a Simulink toolbox for system-level simulations of electrical circuits developed by Plexim [14] . This program is designed for power electronics systems. The advantage of PLECS is the high-speed simulation of the power electronics networks. Both electrical and thermal circuit is modeled as it is visualized in Fig. 6.2. The gate-source voltage is set to $10V$. However, the DC current source is connected to the drain. The power dissipation is calculated by using a multiplication math tool box for both the drain current and drain-source voltage. The error between the simulated drain-source voltage and the measurement is too small is about 0.3% so does the power dissipation which indicates that the electrical circuit is simulated correctly. The interface between the electrical circuit and the thermal model is done by the heat sink as shown in Fig. 6.2.

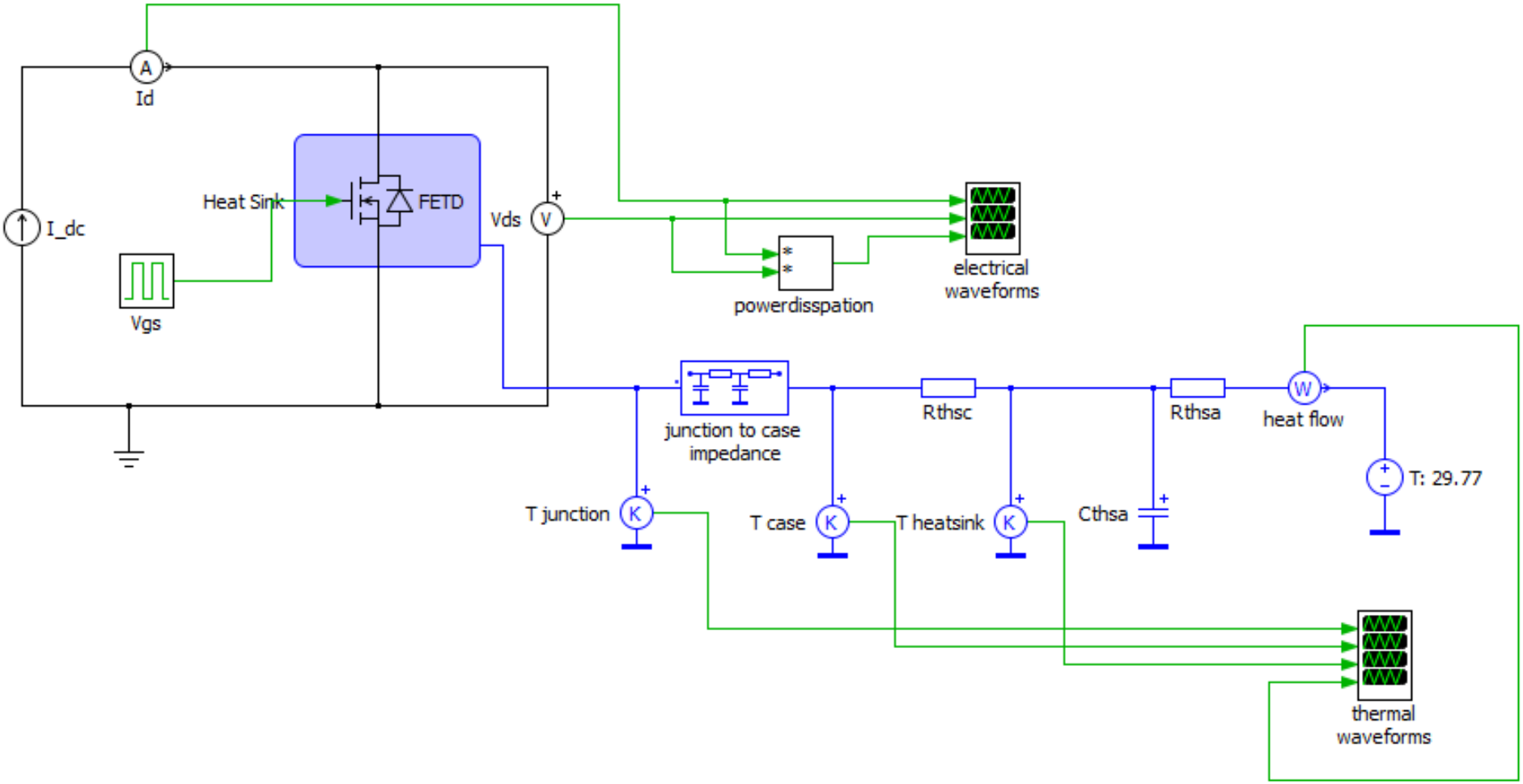


Fig. 6.2 Electrical and thermal simulation model

To model the thermal network, the MOSFET thermal description has to be separated from the electrical data sheet. The thermal editor dialog is used to create and edit the thermal data sheet as shown in Fig. 6.3. The turn-on and turn-off switching losses are not included in the simulation. Therefore, all these values are set to zero. However, the conduction loss has to be created.

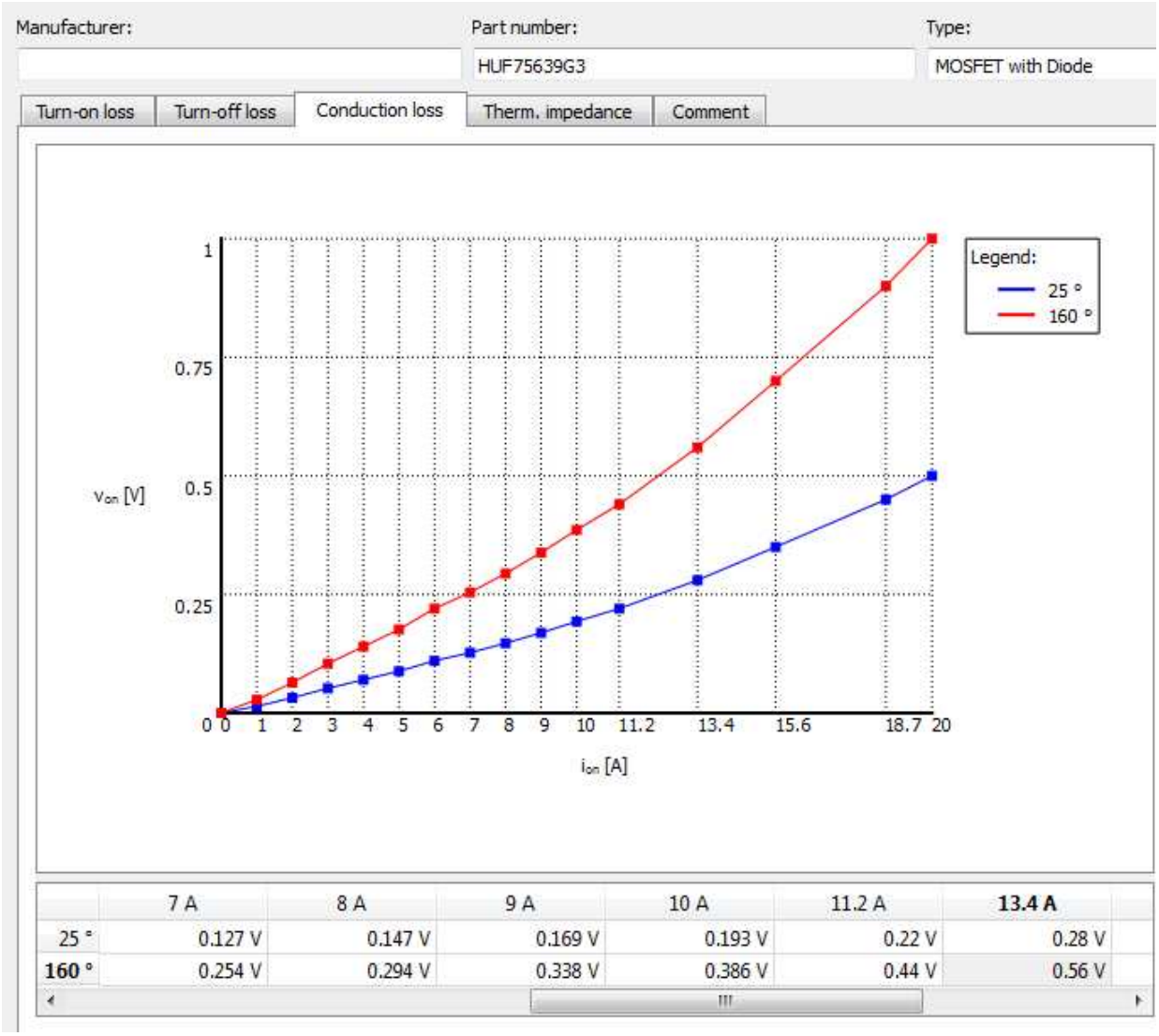


Fig. 6.3 MOSFET thermal description in PLECS

The conduction loss is defined by using a 2D lookup-table. The drain-source voltage is a function of the drain current and the device temperature (Vds_{on}=f(I_d,T_j)). The on-state voltage is obtained for two different temperatures, 25°C and 160°C. The voltage at 25°C is extracted from the drain current versus drain-source voltage curve which is given by the data sheet (see Fig. A.4). However, the drain-source voltage at the maximum junction temperature (160 °C) is obtained by normalize the drain-source voltage at 25°C and the result is shown in Table 6.2 and Fig. 6.4.

Table 6.2: Drain-source voltage normalization

I_d(A)	$V_{ds_{on}}$ at(25°C)	$V_{ds_{on}}$ at(175°C)
0	0	0
1	0.014	0.028
2	0.032	0.064
3	0.052	0.104
4	0.07	0.14
5	0.088	0.176
6	0.11	0.22
7	0.127	0.254
8	0.147	0.294
9	0.169	0.338
10	0.193	0.386
11.2	0.22	0.44
13.4	0.3	0.6
15.6	0.35	0.7
18.7	0.45	0.9
20	0.5	0.1

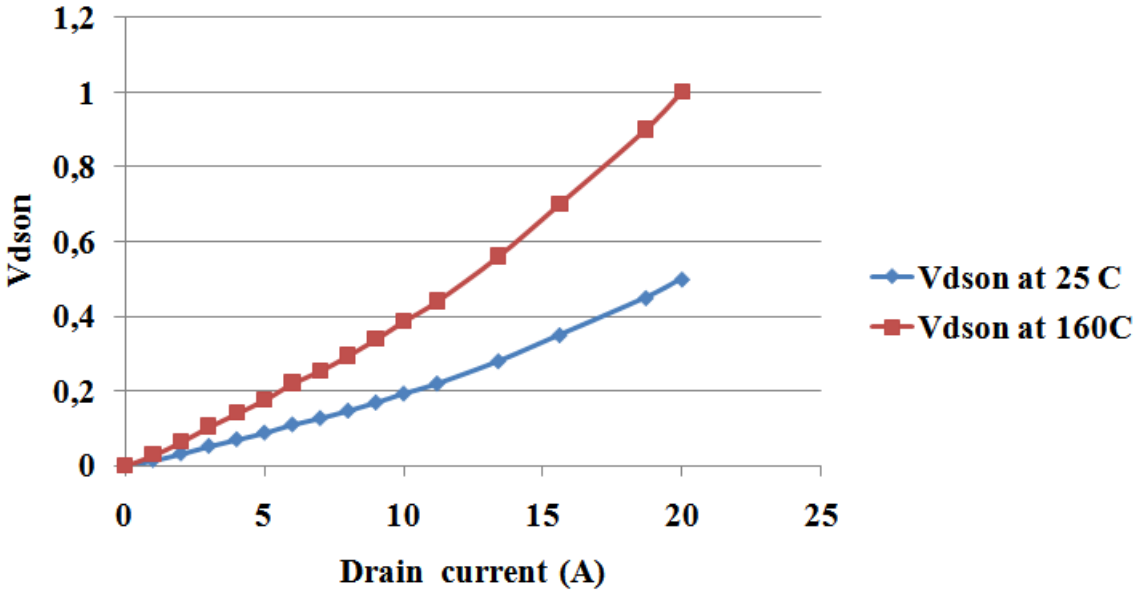


Fig. 6.4 current versus drain-source voltage at two different temperature(25°C and 175°C)

PLECS always uses a Cauer thermal equivalent network to model the thermal impedance of the device from junction to case. In the data sheet, the Foster thermal equivalent circuit is supported (see Fig. A.9). Therefore, the transformation from Foster to Cauer network is implemented using the following procedure

1. The impedance of the Foster network (4.22) can be written as

$$Z(S) = \frac{a_{n-1}S^{n-1} + a_{n-2}S^{n-2} + ... + a_1S + a_0}{b_nS^n + b_{n-1}S^{n-1} + ... + b_1S + b_0} \tag{6.3}$$

2. The first value of Cauer capacitance is found by inverting (6.3)and subtracting the value of the first capacitance [11].

$$Y_1(S) = \frac{b_nS^n + b_{n-1}S^{n-1} + ... + b_1S + b_0}{a_{n-1}S^{n-1} + a_{n-2}S^{n-2} + ... + a_1S + a_0} - C_1S \tag{6.4}$$

$$Y_1(S) = \frac{(b_n - C_1a_{n-1})S^n + (b_{n-1} - C_1a_{n-2})S^{n-1} + ... + (b_1 - C_1a_0)S + b_0}{a_{n-1}S^{n-1} + a_{n-2}S^{n-2} + ... + a_1S + a_0} \tag{6.5}$$

Then

$$C_1 = \frac{b_n}{a_{n-1}} \tag{6.6}$$

3. The first value of the Cauer resistance can be found according to the following

$$Z_1(S) = \frac{a_{n-1}S^{n-1} + a_{n-2}S^{n-2} + ... + a_1S + a_0}{(b_n - C_1a_{n-1})S^n + (b_{n-1} - C_1a_{n-2})S^{n-1} + ... + (b_1 - C_1a_0)S + b_0} - R_1 \tag{6.7}$$

$$Z_1(S) = \frac{(a_{n-1} - R_1(b_n - C_1a_{n-1}))S^{n-1} + ... + (a_1 - R_1(b_1 - C_1a_0))S + (a_0 - R_1b_0)}{(b_n - C_1a_{n-1})S^n + (b_{n-1} - C_1a_{n-2})S^{n-1} + ... + (b_1 - C_1a_0)S + b_0} \tag{6.8}$$

$$R_1 = \frac{a_{n-1}}{b_n - C_1a_{n-1}} \tag{6.9}$$

4. To calculate the next value of the resistance and the capacitance, the procedure from (1 to 3) must be repeated.

Table 6.3 and Table 6.4 show the transformation results from Foster to Cauer thermal resistance and thermal capacitance respectively.

Table 6.3: Foster to Cauer thermal resistance conversion

Thermal resistance(°C/W)		
Thermal resistance	Foster	Cauer
R_{TH_1}	0.0005	0.00311
R_{TH_2}	0.0015	0.01074
R_{TH_3}	0.02	0.0698
R_{TH_4}	0.09	0.1959
R_{TH_5}	0.19	0.1959
R_{TH_6}	0.29	0.1165

Table 6.4: Foster to Cauer thermal capacitance conversion

Thermal capacitance(J/°C)		
Thermal capacitance	Foster	Cauer
C_{TH_1}	0.0028	0.001056
C_{TH_2}	0.0046	0.0009371
C_{TH_3}	0.0055	0.0009228
C_{TH_4}	0.0092	0.003488
C_{TH_5}	0.017	0.01427
C_{TH_6}	0.043	0.07497

Three simulation tests results are compared with the measurement results:

6.2.1 Test1

Measurement results

In this test, the MOSFET is not mounted to any heat sink. The MOSFET is isolated from the PCB by using thermal isolation paper to measure the correct temperature. To stop the air flow and get a balance and non-fluctuating temperature, the circuit is put inside a plastic chamber. Two thermocouples (PT1000) are used in this test; the first PT1000 element is glued on the case of the MOSFET to measure the case temperature while the second PT1000 element is used to measure the ambient temperature inside the chamber box. The case, and the ambient temperature are measured by passing different drain currents ($6A, 8A, 10A$) through the MOSFET as shown in Fig. 6.6 to Fig. 6.8. A drain current of $12A$ resulted in a substantial increase in the junction temperature. Fig. 6.5 shows the temperature increases incredibly by passing $12A$ through the MOSFET.

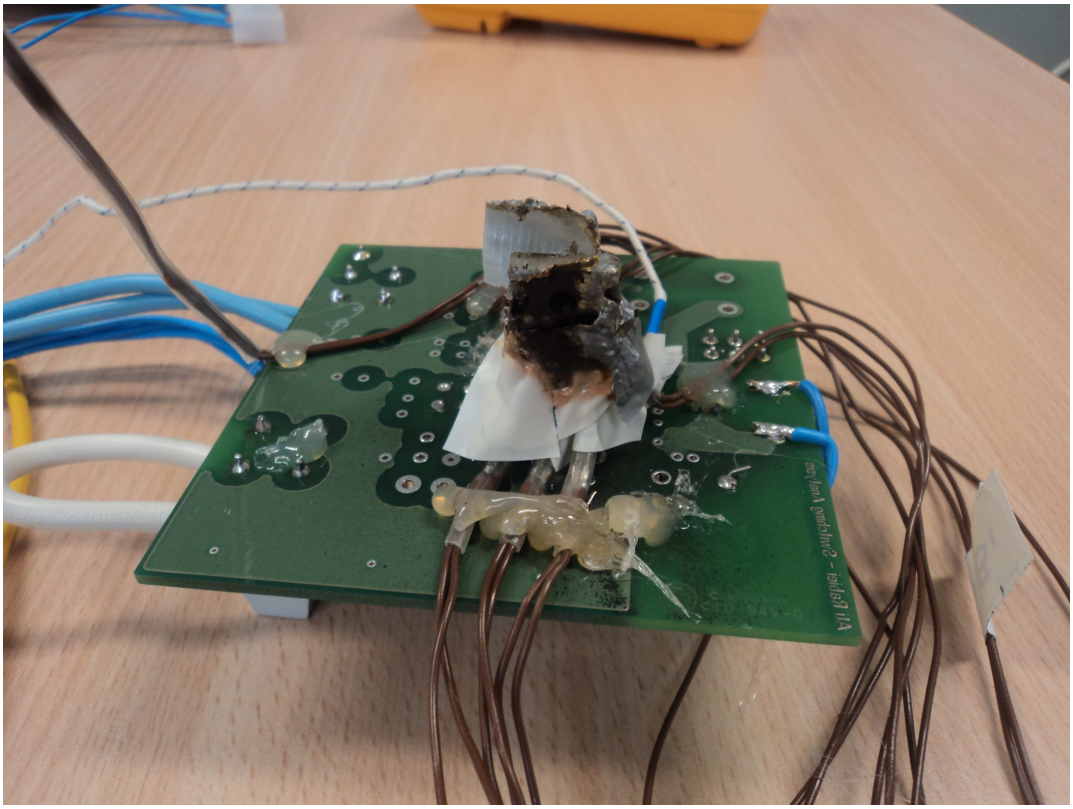


Fig. 6.5 Experimental test of MOSFET with I_d=12 A

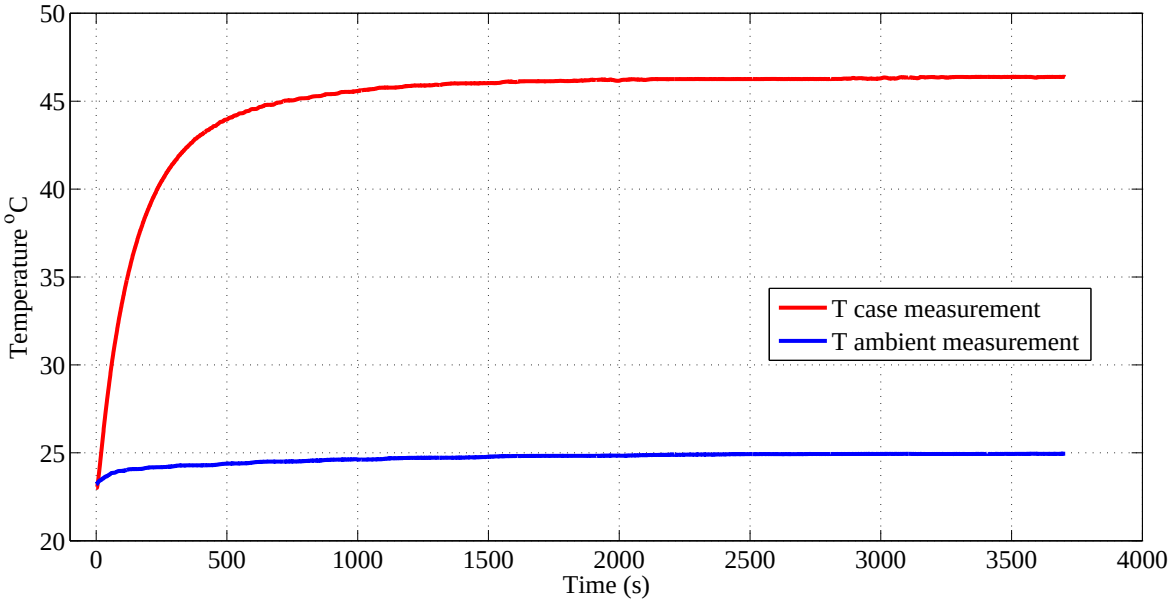


Fig. 6.6 Experimental measurement with I_d=5.993 A

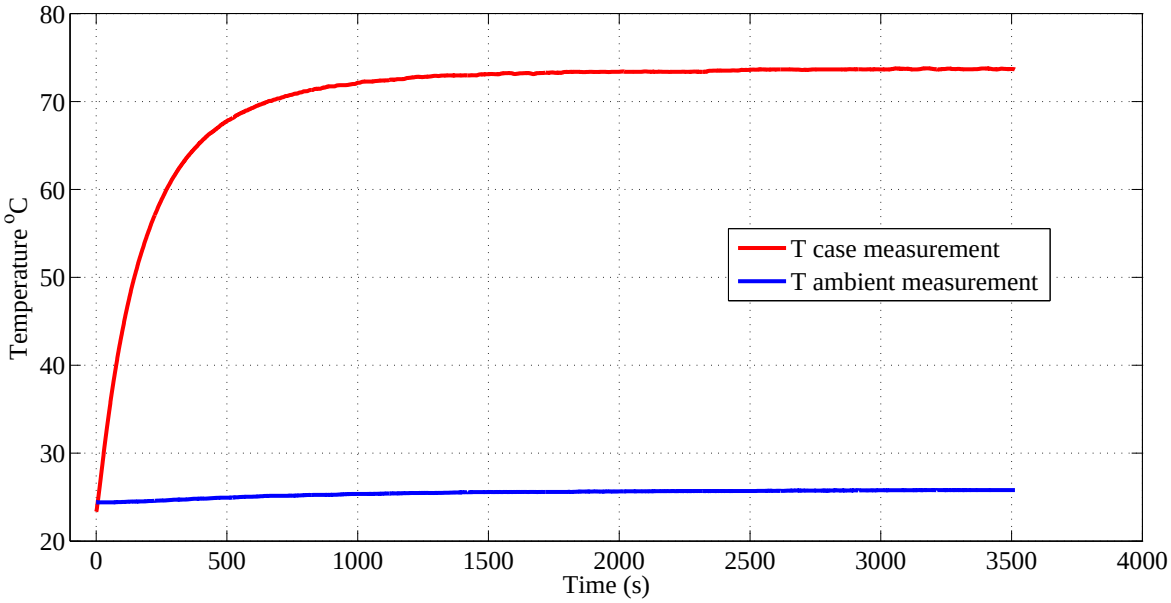


Fig. 6.7 Experimental measurement with I_d=7.99 A

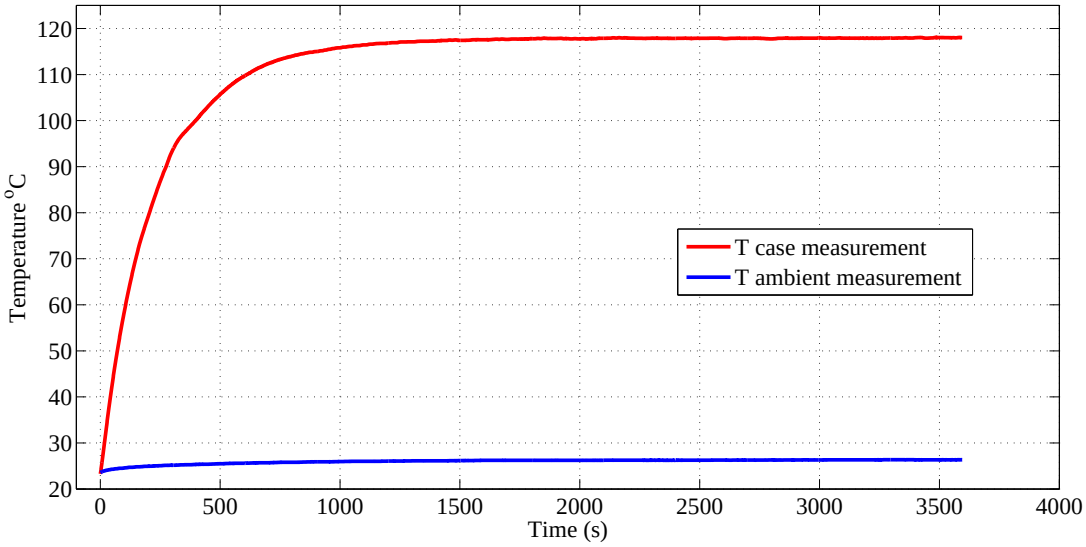


Fig. 6.8 Experimental measurement with I_d=9.89 A

Table 6.5 shows the power dissipation for various drain current, steady state case temperature measurement and steady state ambient temperature.

Table 6.5: MOSFET thermal measurement at different drain current

I_d (A)	$V_{ds_{on}}$ (V)	P_d (W)	T_{case} (°C)	T_{amb} (°C)
5.993	0.138	0.8270	46.38	24.95
7.99	0.229	1.8297	73.7	25.8
9.89	0.402	3.9758	118	26.3

The junction temperature is calculated according to (6.2) as shown in Table 6.6. The junction to ambient thermal resistance ($R_{TH_{ja}}$) is the only thermal resistance that exists if the MOSFET is not mounted onto heat sink. The value of $R_{TH_{ja}}$ is $30\frac{^\circ C}{W}$ which is founded in the data sheet [23]. Moreover, the junction temperature is estimated by normalizing the calculated on-state resistance ($\frac{V_{ds_{on}}}{I_d}$) using the normalized drain to source on resistance versus the junction temperature as shown in Fig. A.5.

Table 6.6: MOSFET junction temperature calculation for different drain current

P_d(W)	$R_{TH_{ja}}$(°C/W)	T_{amb} (°C)	$T_{j_{calc.}}$(°C)	$T_{j_{estim.}}$(°C)	Error(%)
0.8270	30	24.95	49.76	47.7	4.32
1.8297	30	25.8	80.69	76.6	5.34
3.9758	30	26.3	145.57	138.8	4.88

Both power dissipation and junction temperature increase for various drain current as shown in Fig. 6.9 and Fig. 6.10 respectively.

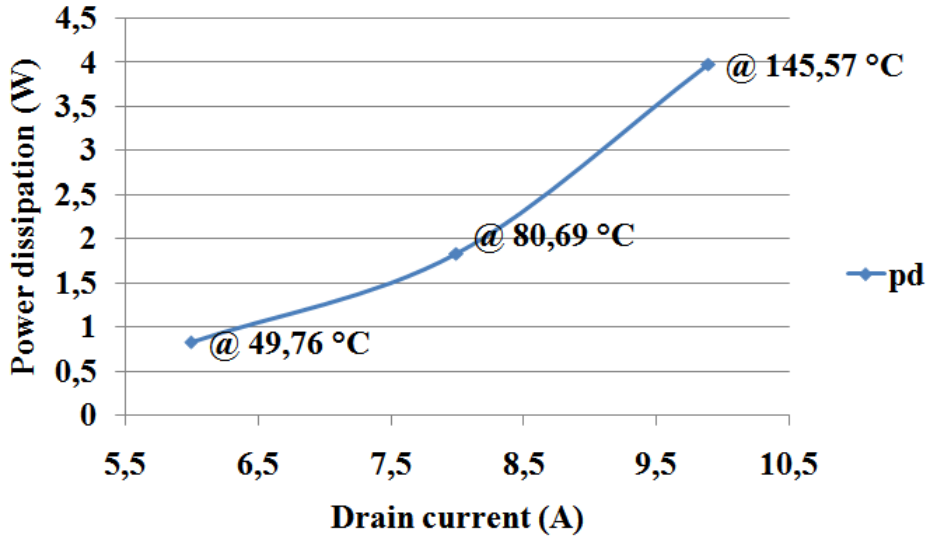


Fig. 6.9 Power dissipation versus drain current

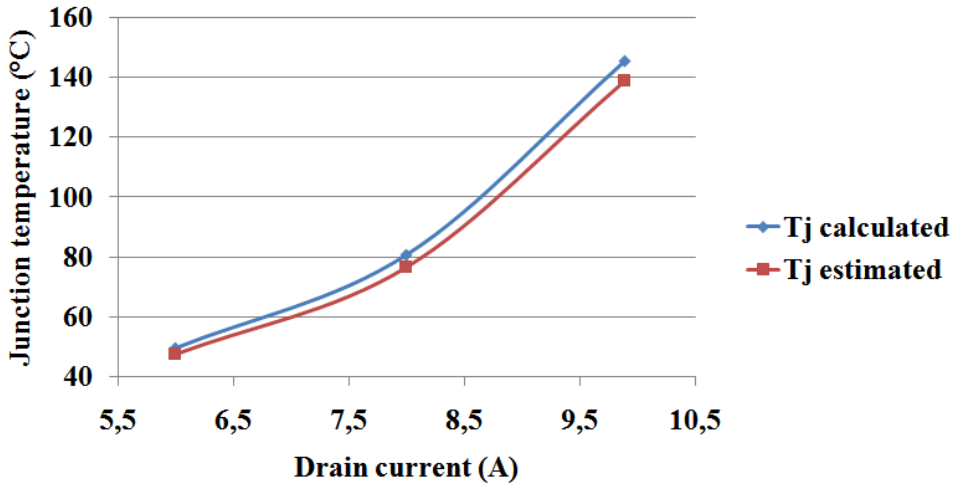


Fig. 6.10 Junction temperature versus drain current

The on-state resistance is a function of drain current, gate voltage, and MOSFET temperature. All MOSFET data sheet provides the relationship between the on-state resistance and the temperature. As the junction temperature increases, the on-state resistance has to be modified according to the following relationship [24].

$$R_{ds_{on}}(T_J) = R_{ds_{on}}(25°C)(\frac{T_J}{300})^{2.3} \tag{6.10}$$

where the value of $R_{ds_{on}}(25°C)$ is 0.021Ω which is obtained from the data sheet [23] and T_J is the junction temperature in Kelvin (K).

The on-state drain-source resistance is calculated using two methods. The first method by dividing the drain-source voltage by the drain current. However, the second method is calculated by using (6.10). The results and error of calculating the on-state resistance by using these two methods are visualized in Table 6.7. Fig. 6.11 shows how the on-state drain-source resistance for various drain currents by using these two methods.

Table 6.7: Error in the drain-source resistance by using two methods

I_d(A)	$V_{ds_{on}}$(V)	$R_{ds_{on}}$ $method1$ (Ω)	$R_{ds_{on}}$ $method2$ (Ω)	Error(%)
5.993	0.138	0.0230268	0.023563	2.27
7.99	0.229	0.0286608	0.029083	1.45
9.89	0.402	0.040647	0.042843	5.12

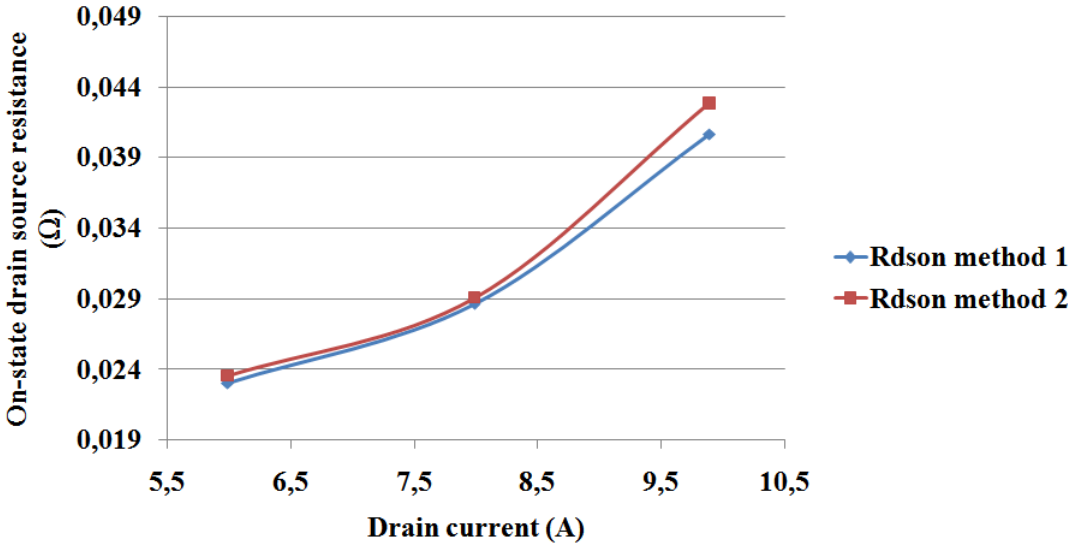


Fig. 6.11 Drain source resistance versus drain current

Now, the percentage of the heat that flows out through gate, source,and drain pin of the MOSFET device is calculated. Fig. 6.12 shows the cross section of the MOSFET pin. The energy flow per unit time that flows from the high temperature end to the the lower temperature end is

$$P_d = \frac{\lambda h W \Delta T}{I} \tag{6.11}$$

where λ is the material thermal conductivity ($\frac{w}{m^\circ C}$), ΔT is the change of the temperature in each Pin ($^\circ C$), and h, b, d is the MOSFET pin dimensions (m).

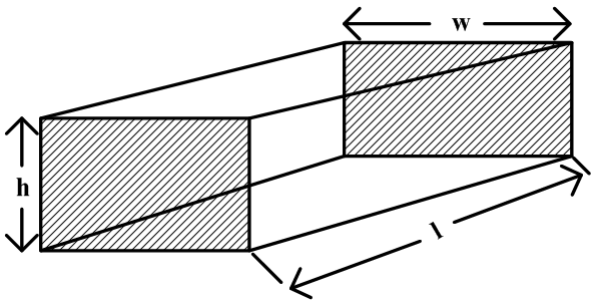


Fig. 6.12 MOSFET pin configuration

To measure the change of the temperature in each pin of the device, six thermocouples (PT1000) are used as illustrated in Fig. 6.13. On each pin, one PT1000 element is put on the top and the other is put in the bottom. Another two PT1000 elements are used to measure the case temperature and the ambient temperature. A drain current of ($9.89A$) is tested. The drain-source voltage ($V_{ds_{on}}$)of the MOSFET without heat sink for this drain current is $0.402V$. Table 6.8 shows the percentage of the power dissipation in each pin of the device.

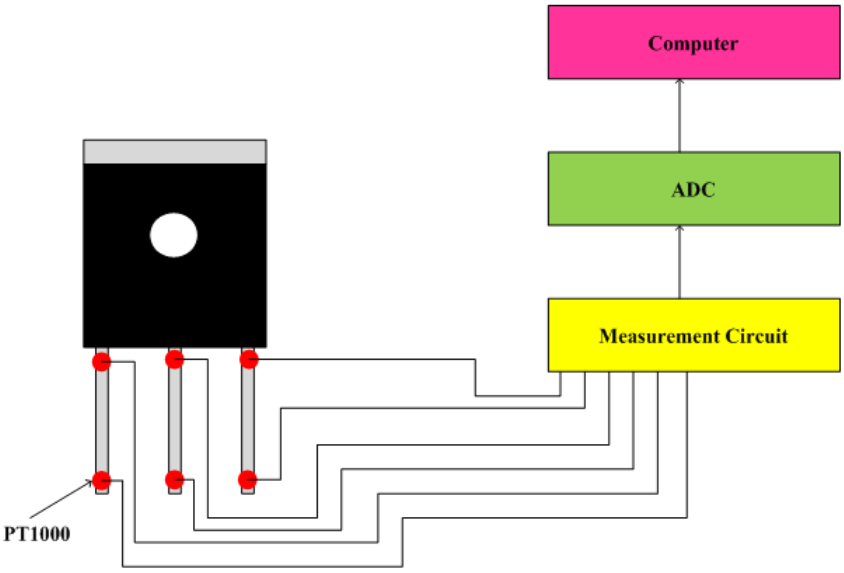


Fig. 6.13 PT1000 positions on the MOSFET

Table 6.8: MOSFET thermal measurement at different drain current

$Type$	T_{top}(°C)	T_{bottom}(°C)	$P_d(W)$
Drain	114.1	91.49	0.2238
Source	83.07	61.74	0.2112
Gate	65.87	61.12	0.047

The total power dissipation is $(3.976W)$. However, the total power dissipation of drain, source, and gate pin is $(0.482W)$ which means that 12% of the energy flows through the MOSFET pins and 88% of the energy flows through the case.

The thermal resistance for each pin is calculated by using (6.11). Table 6.9 shows the dimensions and the thermal resistance for each pin.

Table 6.9: MOSFET thermal measurement at different drain current

$Type$	$h(mm)$	$I(mm)$	$W(mm)$	$R_{TH}(\frac{^\circ C}{W})$
Drain	0.6	16	1.2	101.02
Source	0.6	16	1.2004	100.99
Gate	0.6	16	1.199	101.06

The maximum chip temperature for the MOSTFET is $175°C$. To be on the safe side, the temperature on the semiconductor is often designed so that the temperature is kept under $100°C$ with help of additional cooling. This has mainly to do with the fact that the life length of the chip is temperature dependent, high temperature reduces the life length drastically. To lower the temperature, two different heat sinks are tried out as they illustrate in test 2 and test 3.

Simulation analysis

The MOSFET in this test is not mounted onto a heat sink. Therefore, only junction to ambient thermal resistance ($R_{TH_{ja}}$) is modeled in thermal simulation model as illustrated in Fig. 6.14. The value of $R_{TH_{ja}} = 30\frac{^\circ C}{W}$ is founded in the MOSFET data sheet as it is illustrated in Table 4.3. In PLECS, this resistance is divided into two resistance; junction to case thermal resistance ($R_{TH_{jc}} = 0.74\frac{^\circ C}{W}$) and case to ambient thermal resistance ($R_{TH_{ca}} = 29.26\frac{^\circ C}{W}$). To simulate the thermal rise time of the case temperature a thermal capacitance is connected from the case point to the reference point which is calculated according to

$$t_r = 2.2 R_{Th} C_{TH} \tag{6.12}$$

Table 6.10 shows the thermal capacitance for different drain current. The ambient temperature is set as a constant temperature source as it is visualized in Fig. 6.14. The junction temperature and case temperature are measured and compared with the measurement results. The maximum error between the simulation and measurement is about $\pm$ 5.9 %.

Table 6.10: Thermal capacitance which is used in PLECS

P_d (W)	$R_{TH_{jc}}$ (Ω)	$R_{TH_{ca}}$ (Ω)	τ_{TH} (sec)	C_{TH} ($\frac{J}{^\circ C}$)
0.8270	0.74	29.26	485	7.53
1.8297	0.74	29.26	530	8.23
3.9758	0.74	29.26	541	8.40

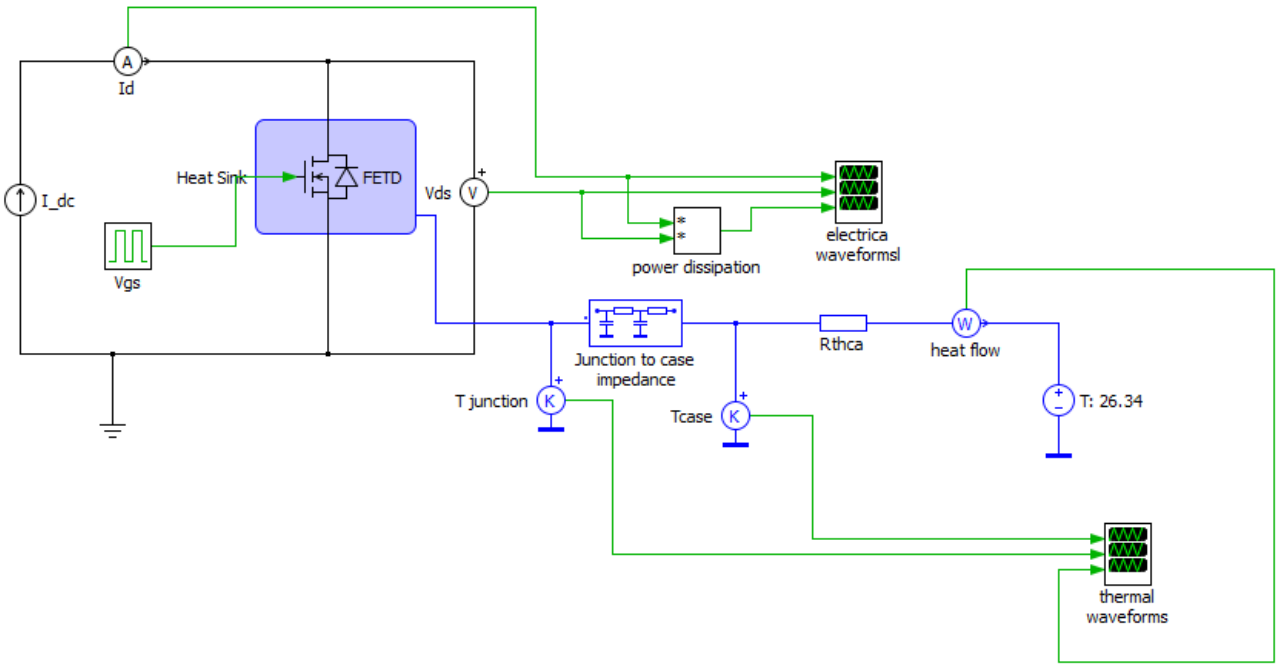


Fig. 6.14 Thermal and electrical simulation model for the MOSFET without heat sink

Fig. 6.15 to Fig. 6.17 show the simulation result for each power dissipation step.

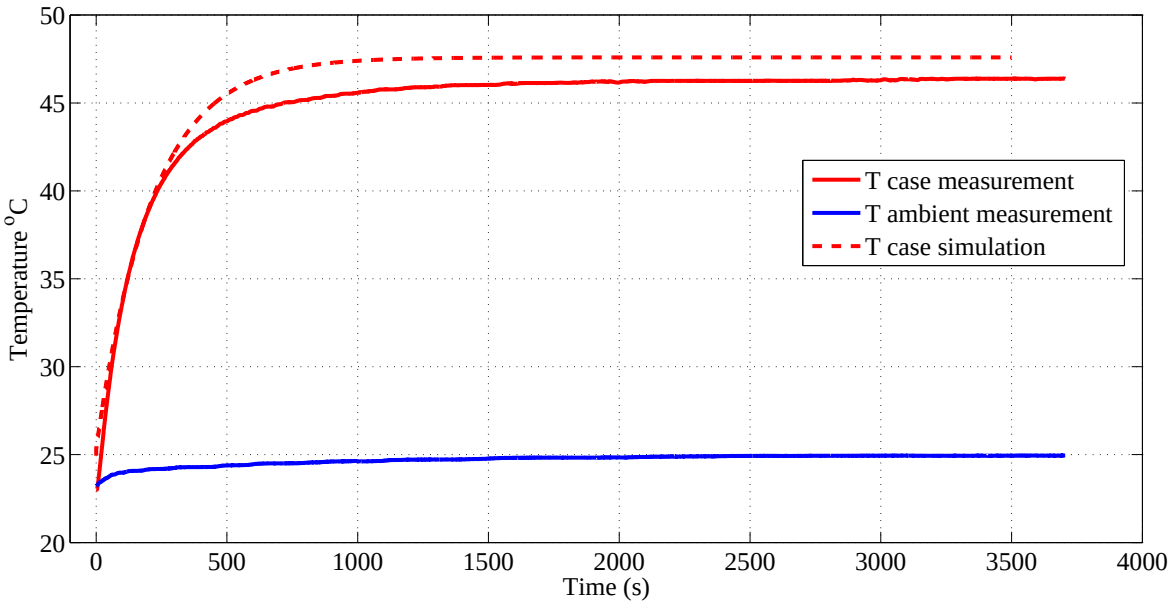


Fig. 6.15 Measurement and experimental results with I_d=5.984 A

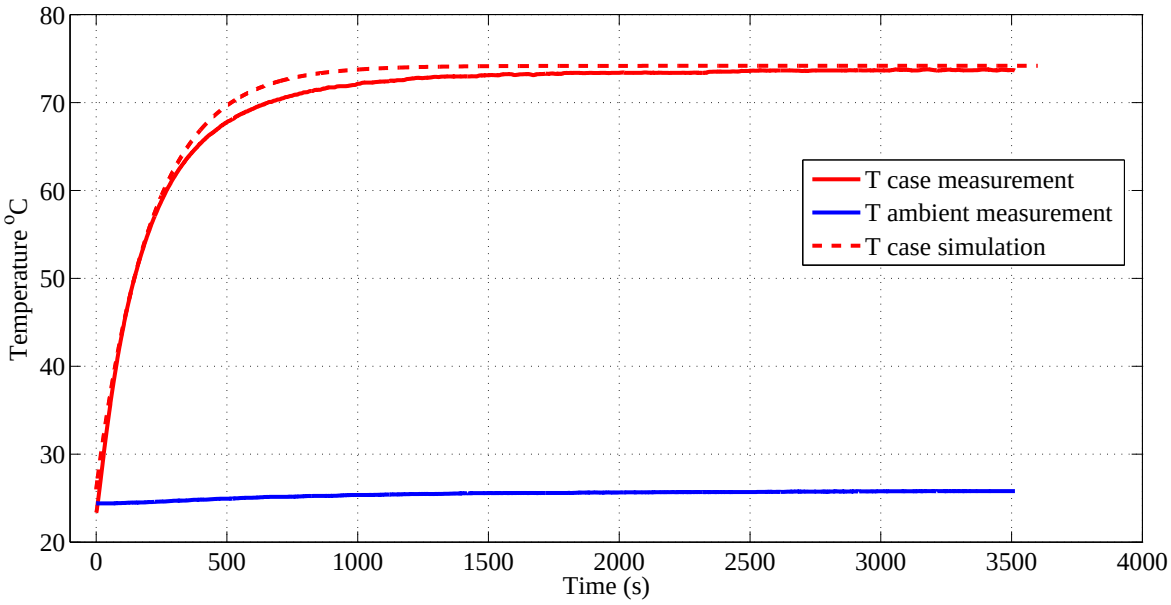


Fig. 6.16 Measurement and experimental results with I_d=7.99 A

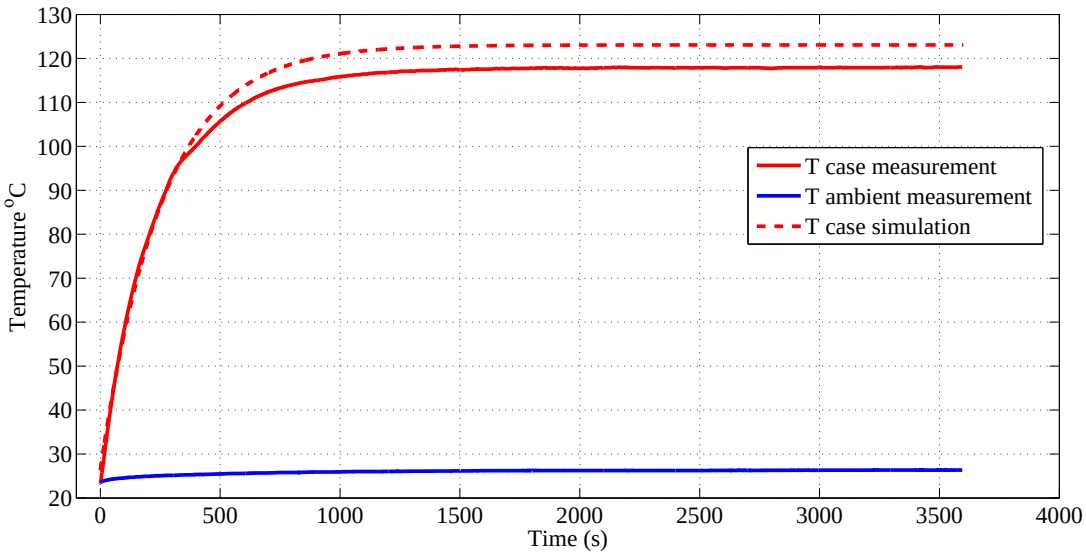


Fig. 6.17 Measurement and experimental results with I_d=9.93 A

Table 6.11 shows the percentage error between the simulation and experimental results

Table 6.11: Measurement and simulation thermal calculation error

P_d	$T_{casemeasur.}$	$T_{casesim.}$	Error %
0.8270	46.38	47.59	-2.543
1.8297	73.7	74.18	-0.647
3.9758	118	123.1	-4.143

6.2.2 Test2

Measurement results

The MOSFET is screw-mounted onto a 50mm*50*12mm (KS 50) heat sink. A thermal isolation pad is put between the MOSFET device and the heat sink to ensure a good thermal contact. The thermal resistance of the isolation pad ($R_{TH_{cs}}$) is $3.7\frac{^\circ C}{W}$ which is extracted from the data sheet (see Fig. A.15). Moreover, the thermal resistance of the heat sink (R_{THsa}) can be extracted from the data sheet for different power dissipations (see Fig. A.15) . Three thermocouples (PT100) are used in this experiment set-up. The first one is attached on the MOSFET case to measure the case temperature. The second thermocouple is mounted in the heat sink to measure the temperature of the heat sink. The last thermocouple is used for measuring the ambient temperature as shown in Fig. 6.18. Two tests are done in this part:

1. The circuit is put inside a plastic chamber to stop the air flow as shown in Fig. 6.18 and in Fig. 6.19. Fig. 6.20 to Fig. 6.24 visualize the measurement for different power dissipation by passing different drain currents through the device.

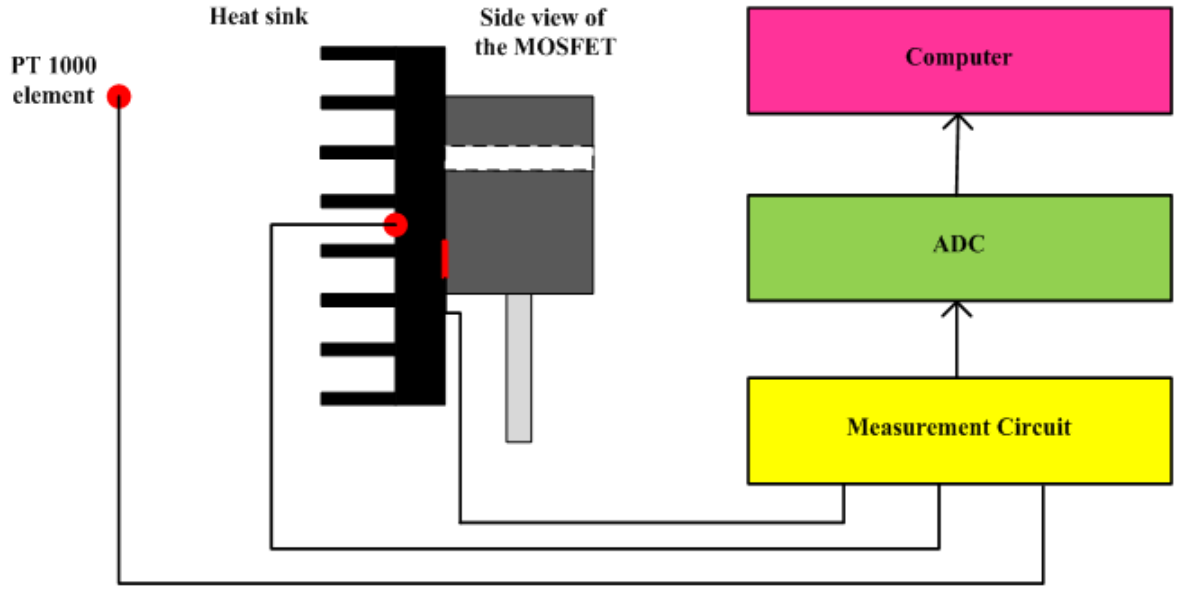


Fig. 6.18 Schematic experimental case-up

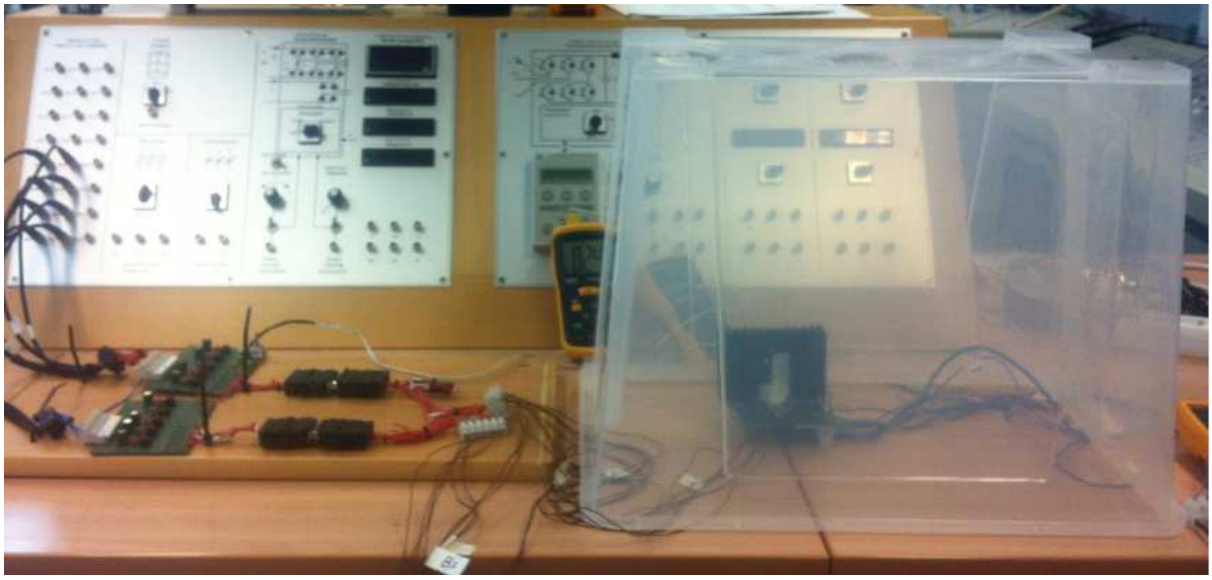


Fig. 6.19 Experimental case-up

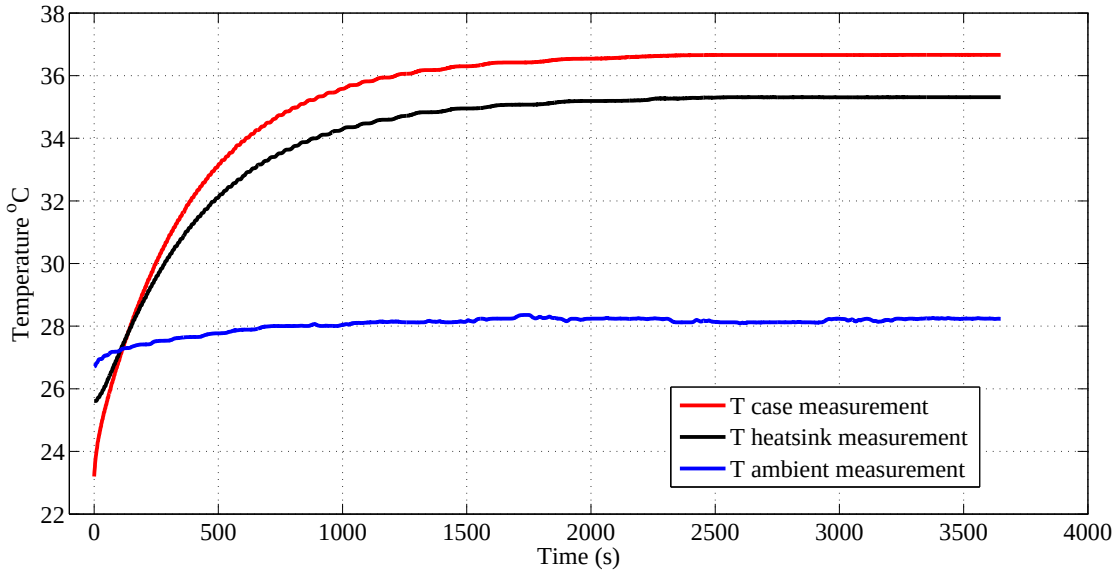


Fig. 6.20 Experimental measurement with $I_d = 5.993A$

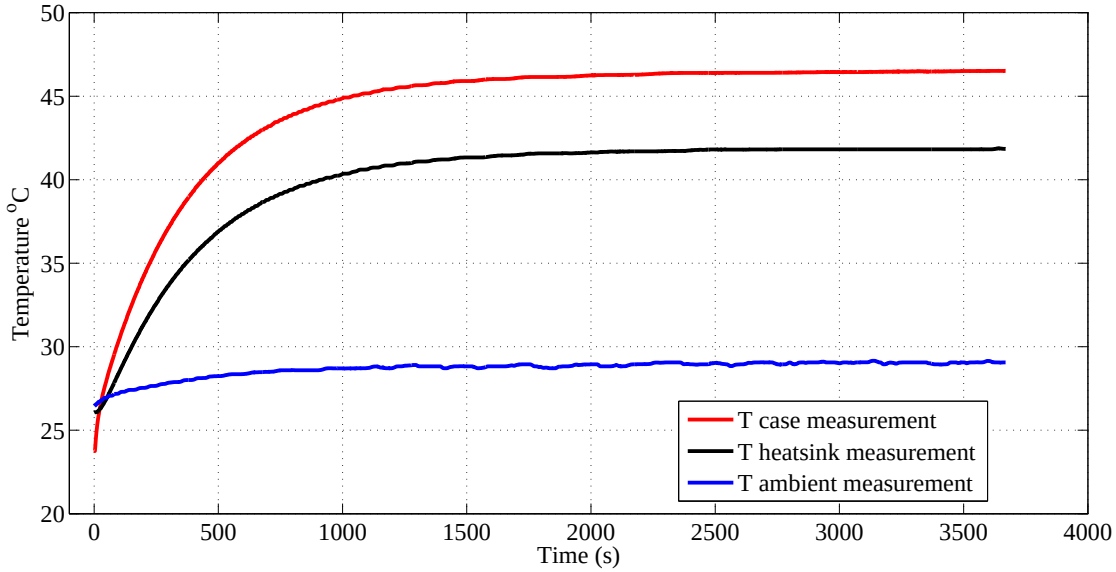


Fig. 6.21 Experimental measurement with $I_d = 7.99A$

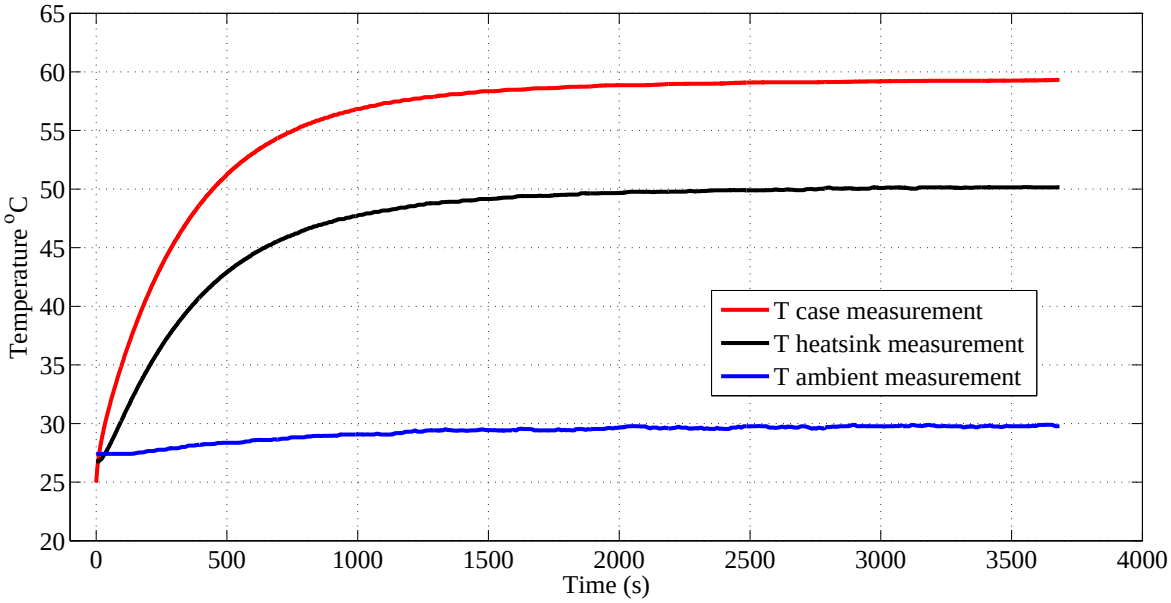


Fig. 6.22 Experimental measurement with $I_d = 9.89A$

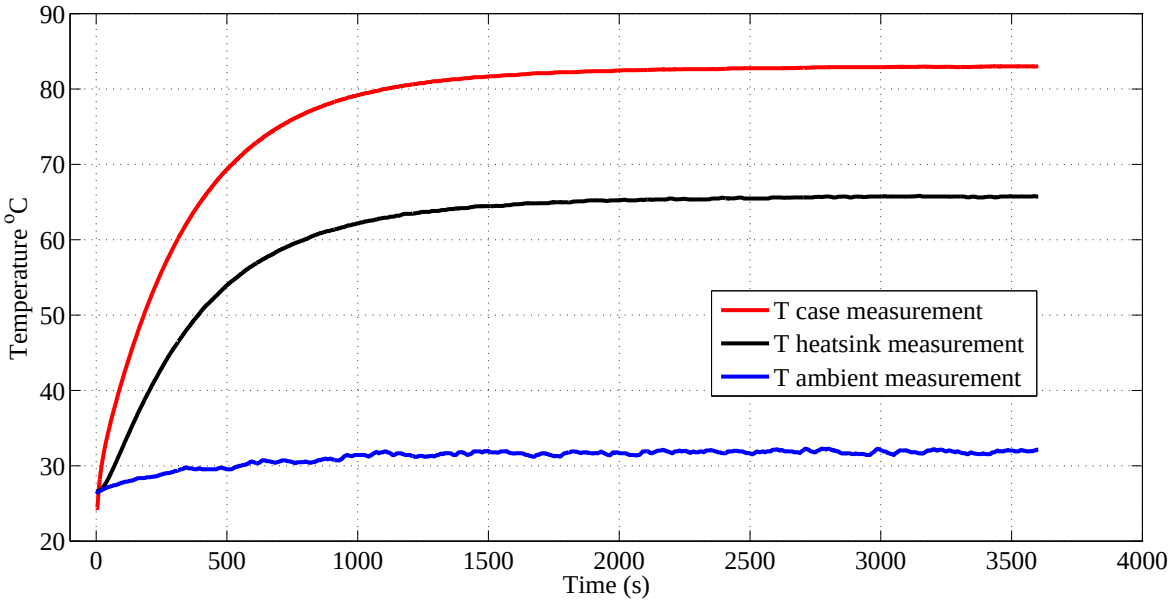


Fig. 6.23 Experimental measurement with $I_d = 12.31A$

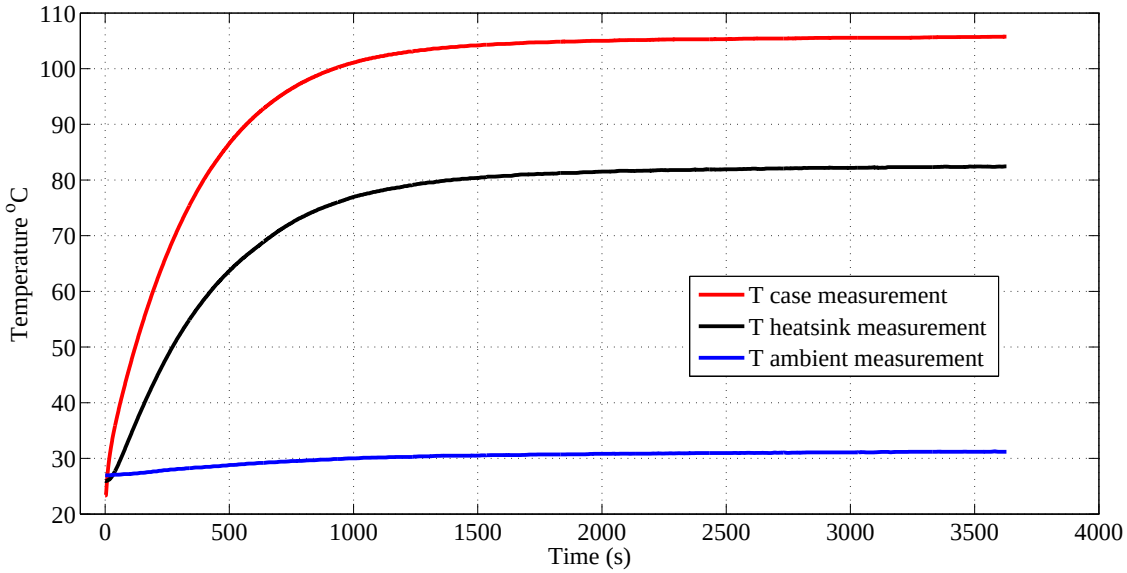


Fig. 6.24 Experimental measurement with $I_d = 13.99A$

To sum up, the power dissipation for various drain current and the steady state case, heat sink, ambient temperatures are shown in Table 6.12.

Table 6.12: MOSFET thermal measurement at different drain current

I_d	$V_{ds_{on}}$	P_d	T_{case}	$T_{heatsink}$	T_{amb}
5.993	0.126	0.7552	36.66	35.31	28.23
7.99	0.182	1.4542	46.51	41.82	29.06
9.89	0.251	2.4824	59.25	50.14	29.77
12.31	0.381	4.6901	83.01	65.75	32.14
13.99	0.511	7.1489	105.7	82.40	31.19

The junction temperature is calculated according to (6.2) as shown in Table 6.13. The values of the junction to case thermal resistance ($R_{TH_{jc}}$) and the case to source thermal resistance ($R_{TH_{cs}}$) are extracted from the data sheet of the MOSFET and the thermal isolation pad respectively. The source to ambient thermal resistance ($R_{TH_{sa}}$) is extracted from the temperature to power dissipation curve for various power dissipation which is supported by the data sheet. Moreover, the junction temperature is estimated by using the normalized drain to source on resistance versus junction temperature as shown in Fig. A.1.

Table 6.13: MOSFET junction temperature calculation for different drain current

P_d (W)	$R_{TH_{jc}}$ (°C/W)	$R_{TH_{cs}}$ (°C/W)	$R_{TH_{sa}}$ (°C/W)	T_{amb} (°C)	$T_{j_{calc.}}$ (°C)	$T_{j_{estim.}}$ (°C)	Error (%)
0.7552	0.74	3	9.7	28.23	38.175984	40.1	4.79
1.4542	0.74	3	9	29.06	47.193874	48.46	2.61
2.4824	0.74	3	8.4	29.77	59.236088	60.56	2.18
4.6901	0.74	3	7.2	32.14	82.183367	84.3	2.51
7.1489	0.74	3	7	31.19	106.038983	109.7	3.34

The power dissipation is increased as the drain current is increased. As a result the junction temperature is also increased as the drain current increases as shown in Fig. 6.25 and Fig. 6.26 respectively.

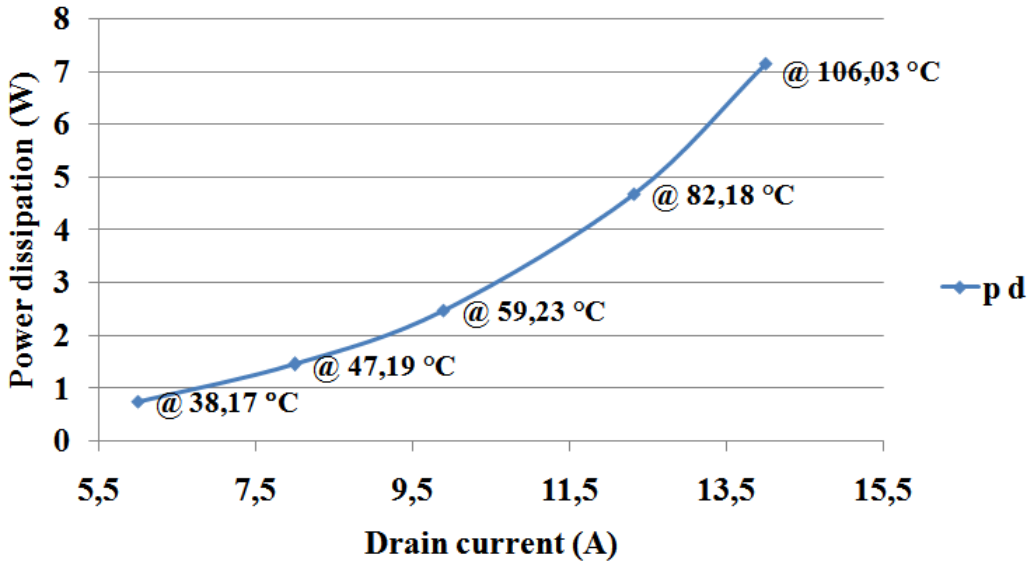


Fig. 6.25 Power dissipation versus drain current

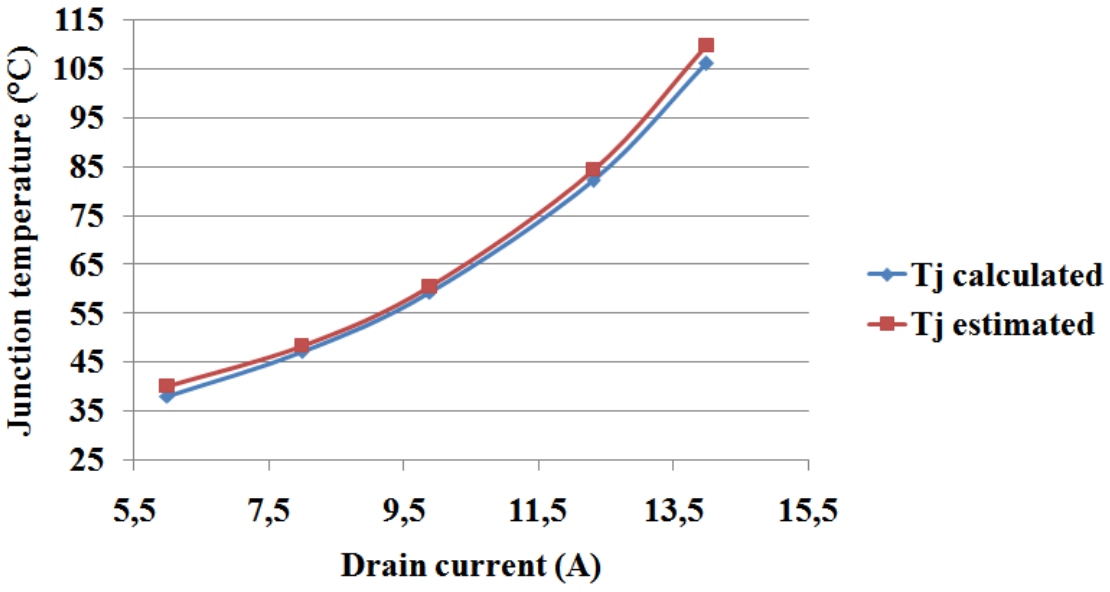


Fig. 6.26 Junction temperature versus drain current

The data sheet on-state drain-source resistance is determined by using (6.10). Dividing the drain-source voltage by the drain current gives the calculated on-state drain-source resistance. The results and error of calculating the on-state resistance are visualized in Table 6.14. Fig. 6.27 shows how the on-state drain-source resistance for various drain currents by using these two methods.

Table 6.14: Error in the drain-source resistance by using two methods

I_d(A)	$V_{ds_{on}}$(V)	$R_{ds_{on}}$ $method1$ (Ω)	$R_{ds_{on}}$ $method1$ (Ω)	Error(%)
5.993	0.126	0.0210245	0.02064217	1.82
7.99	0.182	0.022778	0.02234205	1.91
9.89	0.251	0.02538	0.024908645	1.86
12.31	0.381	0.03095	0.029569162	4.46
13.99	0.511	0.03653	0.034898263	4.47

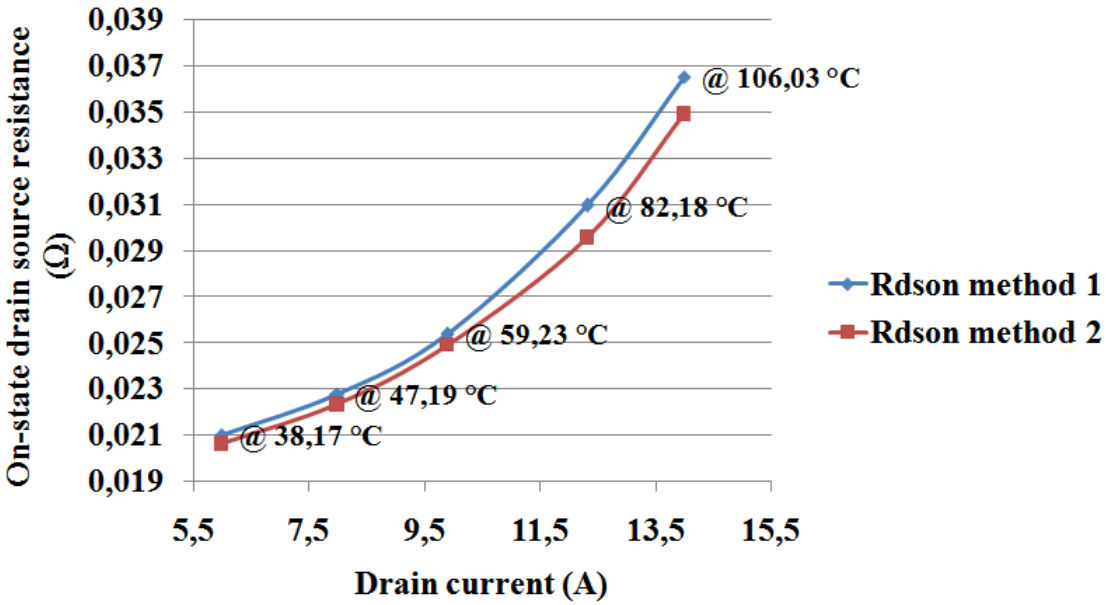


Fig. 6.27 Drain source resistance versus drain current

2. In this part, a fan is put in front of the MOSFET to cool it as shown in Fig. 6.28 . The case, heat sink, and ambient temperatures are measured and the steady-state results are shown in Table 6.15. This table shows the on-state resistance ($R_{ds_{on}}$) which is calculated by dividing the drain-source measured voltage by the measured drain current. This resistance is used to estimate the junction temperature depending on the normalized drain to source on resistance versus junction temperature curve.

Table 6.15: MOSFET thermal measurement at different drain current

I_d (A)	$V_{ds_{on}}$ (V)	P_d (W)	$R_{ds_{on}}$ (Ω)	T_{case} (°C)	$T_{heatsink}$ (°C)	T_{amb} (°C)	$T_{j_{estimated}}$ (°C)
5.993	0.122	0.7311	0.020357	29.01	26.85	26.54	31.35
7.99	0.171	1.366	0.0214017	33.8	27.23	26.91	34.7
9.89	0.222	2.1956	0.0224469	39.05	27.34	27.01	39.5
12.31	0.285	3.5084	0.0231827	45.8	27.89	27.32	46.05
13.99	0.356	4.9810	0.0254496	53.17	28.69	27.44	53.5

Fig. 6.28 Forced air cooling experimental set-up

Using air forced cooling, the source to ambient thermal resistance (R_{Sa}) reduces depending on the speed of air. The maximum reduction of this thermal resistance is approximately a factor of 4. The minimum and maximum reduction of the power dissipation by using air forced cooling are 3.19% and 30.23% respectively as shown in Fig. 6.29.

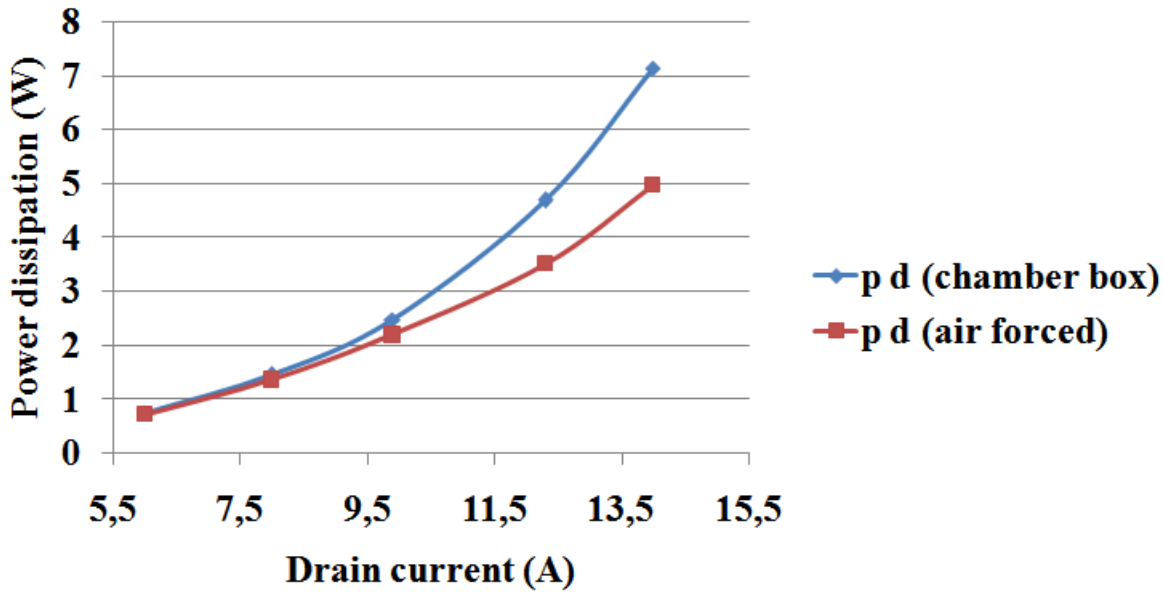


Fig. 6.29 Reduction in power dissipation by using air forced cooling

In this case, the power dissipation from the case to the ambient is higher than the power dissipation with chamber box. As a result, both the drain-source resistance and the junction temperature reduces as shown in Fig. 6.30 and Fig. 6.31. The maximum and minimum reduction on the drain-source resistance is 3.17% and 30.33% respectively. Whereas, The maximum and minimum reduction on the junction temperature is 17.88% and 49.55% respectively.

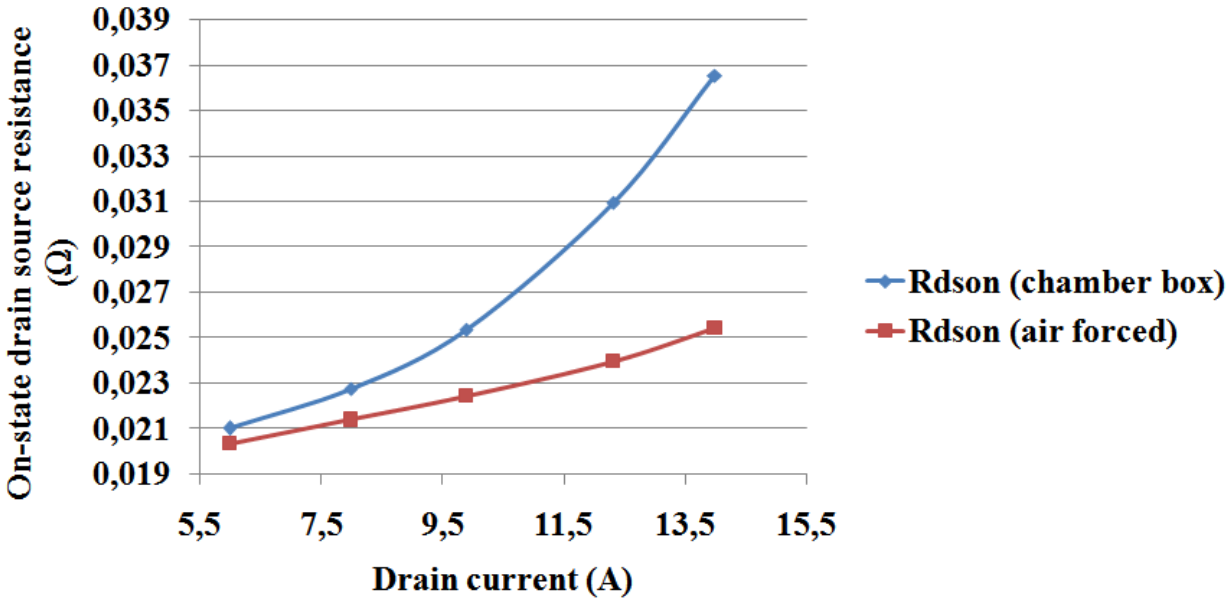


Fig. 6.30 Reduction in drain source resistance by using air forced cooling

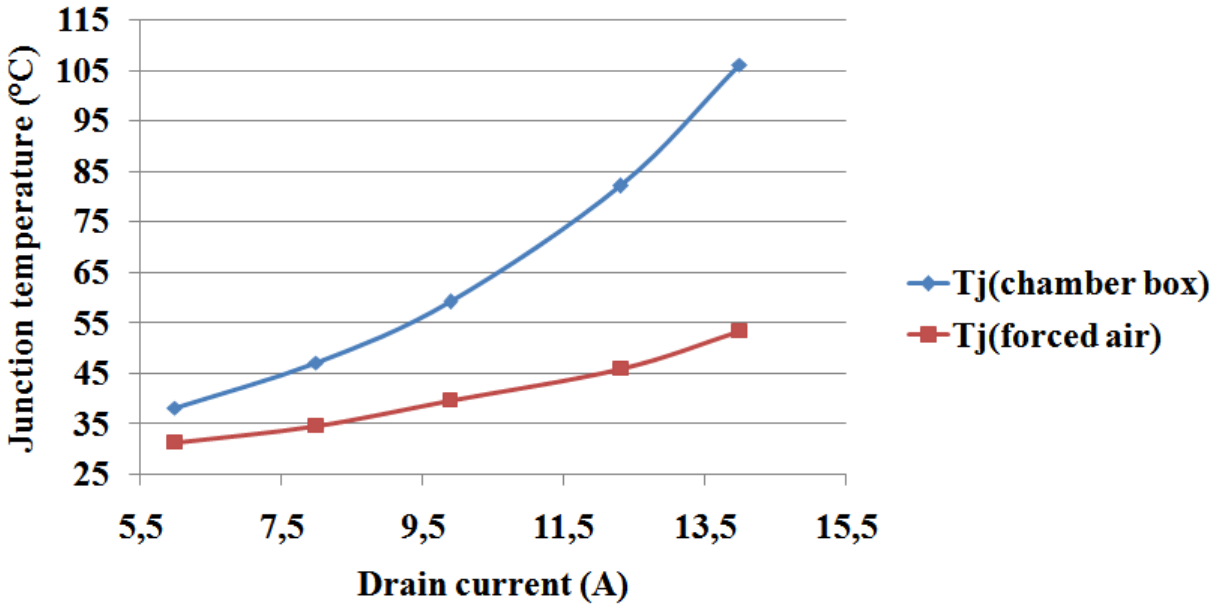


Fig. 6.31 Reduction in the junction temperature by using air forced cooling

The thermal resistance by using air forced cooling reduces approximately a factor of 2 which is calculated using (6.2). Table 6.16 shows the junction to ambient thermal resistance ($R_{TH_{jc}}$ + $R_{TH_{cs}}$ + $R_{TH_{sa}}$) by using chamber box and forced air cooling.

Table 6.16: Total thermal resistance reduction by using forced air cooling

I_d (A)	$R_{TH_{ja}}$ (Chamber box) ($\frac{^\circ C}{W}$)	$R_{TH_{ja}}$ (Forced air cooling) ($\frac{^\circ C}{W}$)
5.993	13.44	6.579
7.99	12.74	5.703
9.89	12.14	5.688
12.31	10.94	5.338
13.99	10.74	5.232

Table 6.20 shows the heat sink thermal resistance which is calculated by using the following equation. The junction to case thermal resistance is $0.74\frac{^\circ C}{W}$ and the case to source thermal resistance is $3\frac{^\circ C}{W}$.

$$R_{TH_{sa}} = R_{TH_{ja}} - R_{TH_{jc}} - R_{TH_{cs}} \tag{6.13}$$

Table 6.17: Heat sink thermal resistance reduction by using forced air cooling

I_d (A)	$R_{TH_{sa}}$ (Chamber box) ($\frac{^\circ C}{W}$)	$R_{TH_{sa}}$ (Forced air cooling) ($\frac{^\circ C}{W}$)	Reduction factor
5.993	9.7	2.839	3.4
7.99	9	1.963	4.6
9.89	8.4	1.948	4.3
12.31	7.2	1.598	4.5
13.99	7	1.492	4.6

Simulation analysis

Fig. 6.2 is the simulation model which is used in this test. The case temperature and heat sink temperature are compared with the measurement results. The maximum error between the simulation and measurement is about is about ± 5 %. The 3D heat transfer from the junction to the ambient is modelled as a 1D heat transfer path and this is the first source of the error between the simulation and measurement results. Only the thermal resistance of the isolation pad is modelled in the thermal network and its value is obtained from the data sheet. However, its thermal capacitance is not included in the simulation network since it is not supported by the data sheet and that is the second source of the error. Moreover, for better results the thermal resistance and capacitance of the chamber box should be included in the simulation. The thermal model of the heat sink is modelled by a thermal capacitance and a thermal resistance. The value of the thermal resistance is obtained from the data sheet. However, the thermal capacitance is calculated by calculating the rise time of the heat sink temperature by using (6.12). In each power dissipation step, the heat sink thermal resistance value is set to a fixed value in the simulation and it is extracted from the data sheet temperature to power dissipation curve. However, in reality this value change slightly with the temperature of the heat sink and that is another source of the error. Table 6.18 shows the junction to case thermal resistance, case to source thermal resistance, source to ambient thermal resistance, and heat sink thermal capacitance.

Table 6.18: Thermal capacitance which is used in PLECS

I_d (A)	$R_{TH_{jc}}$ ($\frac{^\circ C}{W}$)	$R_{TH_{cs}}$ ($\frac{^\circ C}{W}$)	$R_{TH_{sa}}$ ($\frac{^\circ C}{W}$)	τ_{TH} (sec)	C_{TH} ($\frac{J}{^\circ C}$)
5.993	0.74	3	9.7	879	41.19
7.99	0.74	3	9	843	42.57
9.89	0.74	3	8.4	822	44.48
12.31	0.74	3	7.2	780	49.24
13.99	0.74	3	7	769	49.94

Fig. 6.32 to Fig. 6.36 show the simulation result for each power dissipation step.

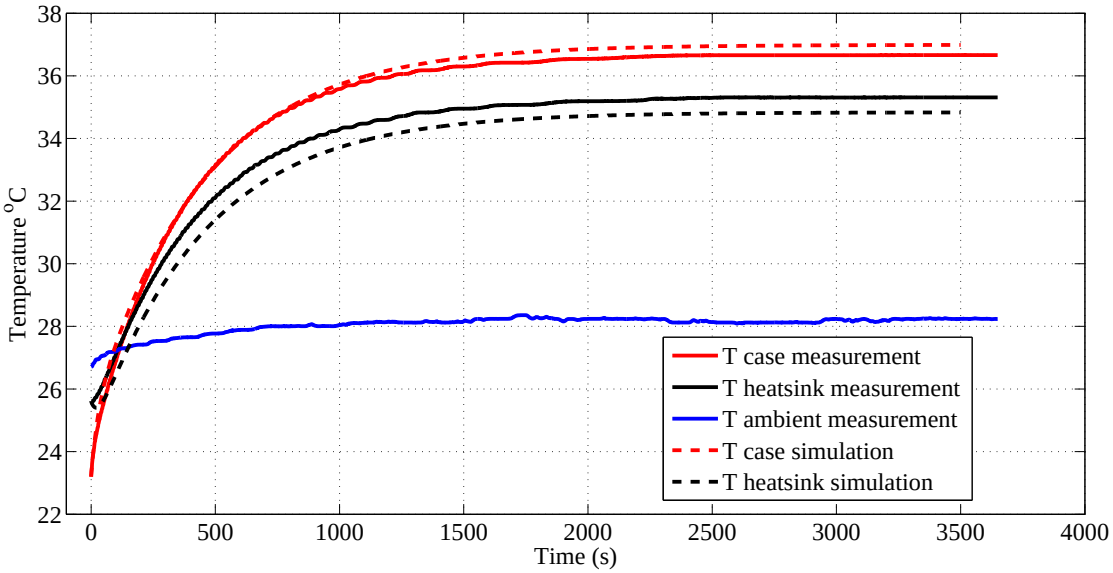


Fig. 6.32 Measurement and experimental results with $I_d = 5.984A$

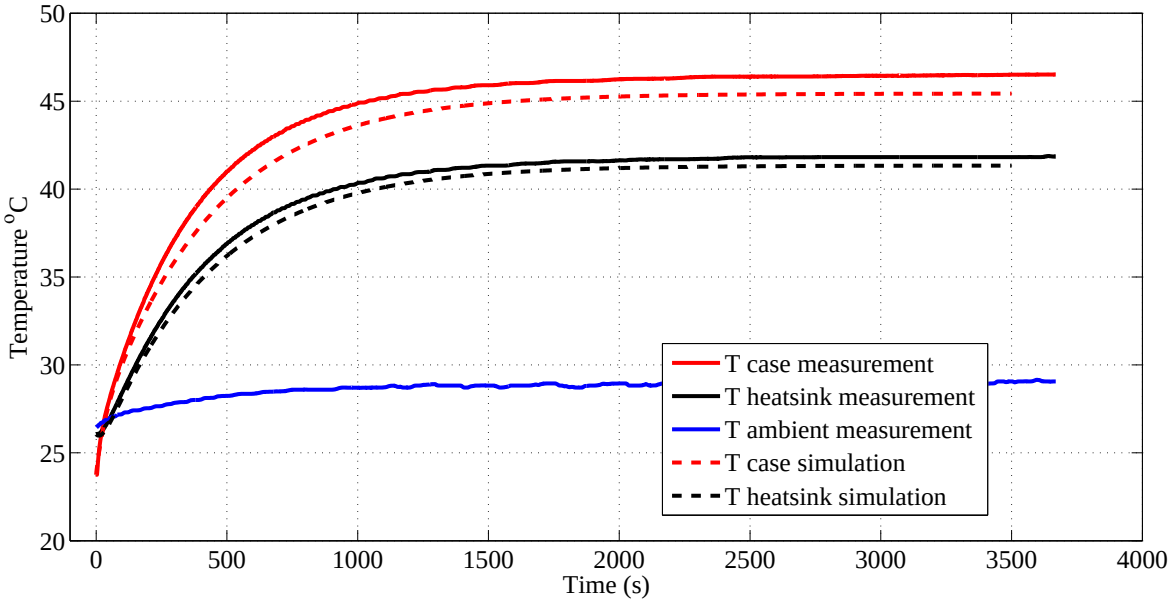


Fig. 6.33 Measurement and experimental results with $I_d = 7.99A$

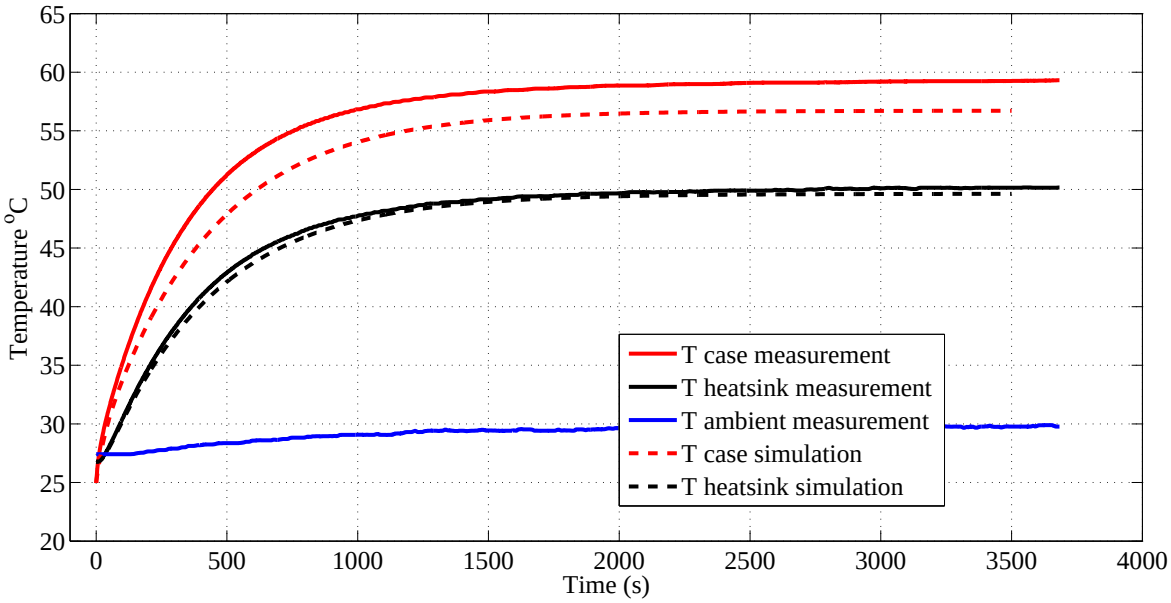


Fig. 6.34 Measurement and experimental results with $I_d = 9.89A$

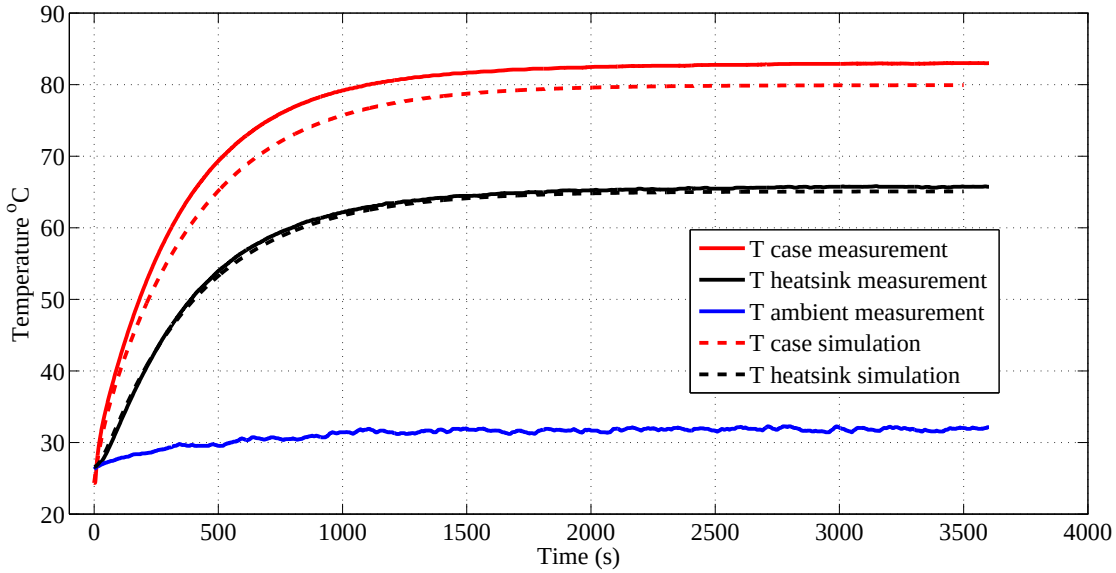


Fig. 6.35 Measurement and experimental results with$I_d = 12.31A$

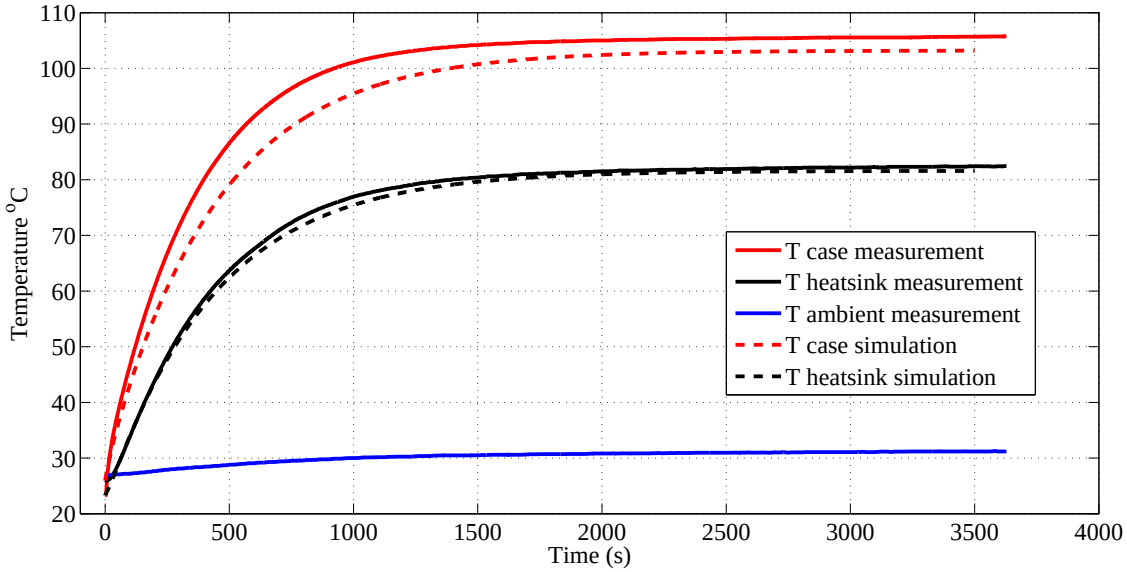


Fig. 6.36 Measurement and experimental results with$I_d = 13.99A$

Table 6.19 shows the percentage error between the simulation and experimental results

Table 6.19: Measurement and simulation thermal calculation error

P_d	$T_{casemeasur.}$	$T_{casesim.}$	Error %	$T_{hsmeasur.}$	$T_{hssim.}$	Error %
0.748	36.66	36.99	-0.892	35.31	34.83	1.359
1.4542	46.51	45.43	2.322	41.82	41.34	1.148
2.4824	59.25	56.71	4.287	50.14	49.62	1.037
4.6901	83.01	79.92	3.722	65.75	65.07	1.034
7.1489	105.7	103.2	2.365	82.4	81.58	0.995

Table 6.20 shows the heat sink thermal resistance which is calculated by using the . The junction to case thermal resistance is $0.74\frac{^\circ C}{W}$ and the case to source thermal resistance is $3\frac{^\circ C}{W}$.

$$R_{TH_{sa}} = R_{TH_{ja}} - R_{TH_{jc}} - R_{TH_{cs}} \tag{6.14}$$

Table 6.20: Heat sink thermal resistance reduction by using forced air cooling

I_d (A)	$R_{TH_{sa}}$ (Chamber box) ($\frac{^\circ C}{W}$)	$R_{TH_{sa}}$ (Forced air cooling) ($\frac{^\circ C}{W}$)	Reduction factor
5.993	9.7	2.839	3.4
7.99	9	1.963	4.6
9.89	8.4	1.948	4.3
12.31	7.2	1.598	4.5
13.99	7	1.492	4.6

6.2.3 Test3

Measurement results

In this test, the MOSFET is screw-mounted onto a 50mm*50*12mm (KS 108) heat sink. The thermal resistance of the heat sink can be obtained from the data sheet for different power dissipations (see Fig. A.17). A thermal isolation pad with thermal resistance of ($3.7\frac{^\circ C}{W}$) is put between the MOSFET and the heat sink. Three PT1000 sensors are used to measure the case, heat sink and ambient temperature. There are also two parts in this test :

1. The MOSFET and the test circuit are put inside a chamber box as shown in Fig. 6.19. Fig. 6.37 to Fig. 6.41 visualize the measurement for the case, the heat sink,and the ambient temperature by passing different drain current through the device.

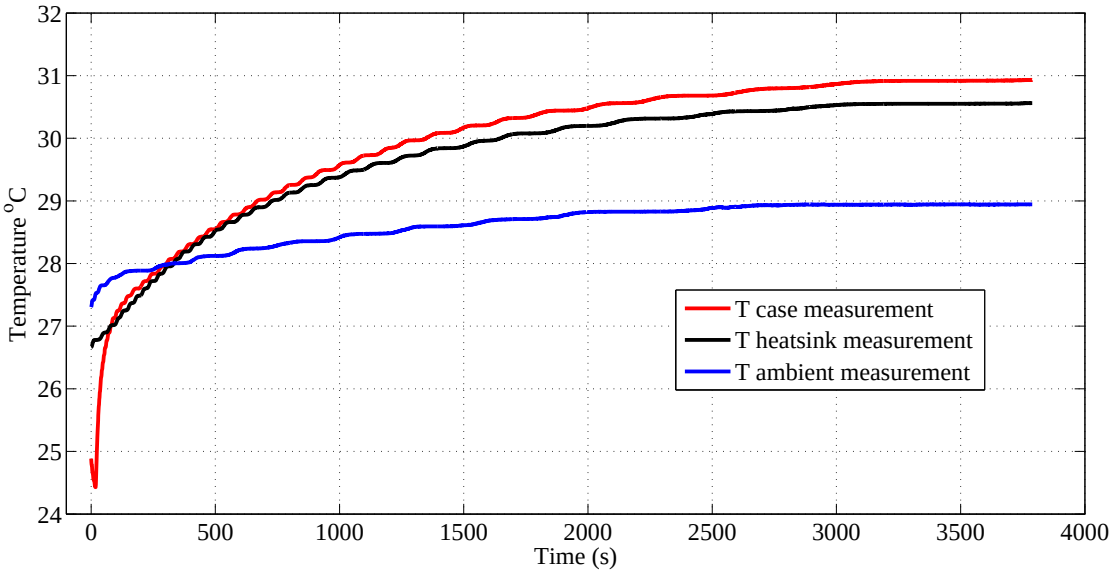


Fig. 6.37 Experimental measurement with $I_d = 5.993A$

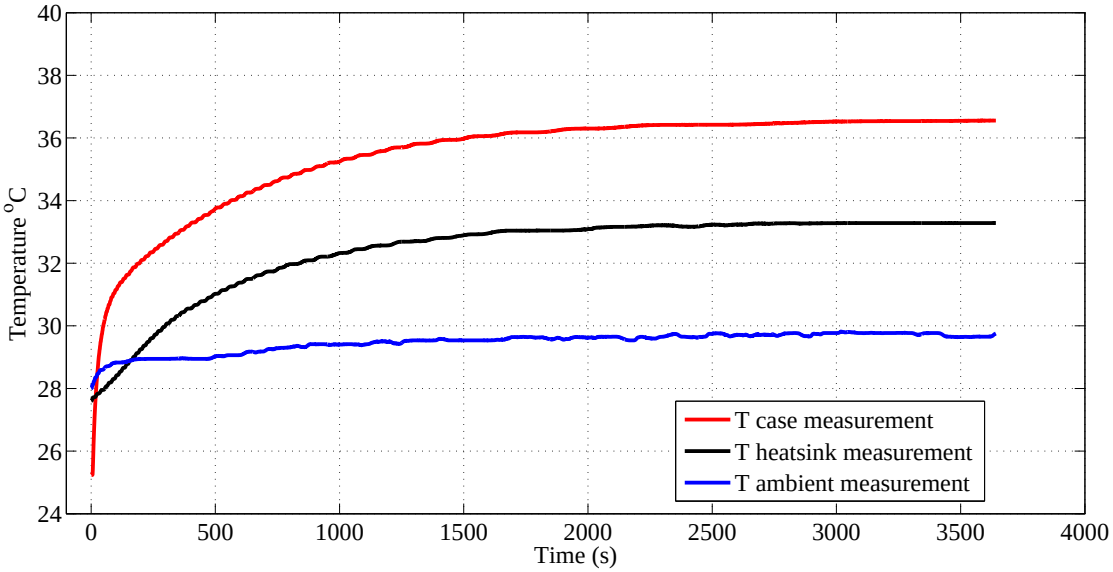


Fig. 6.38 Experimental measurement with $I_d = 7.99A$

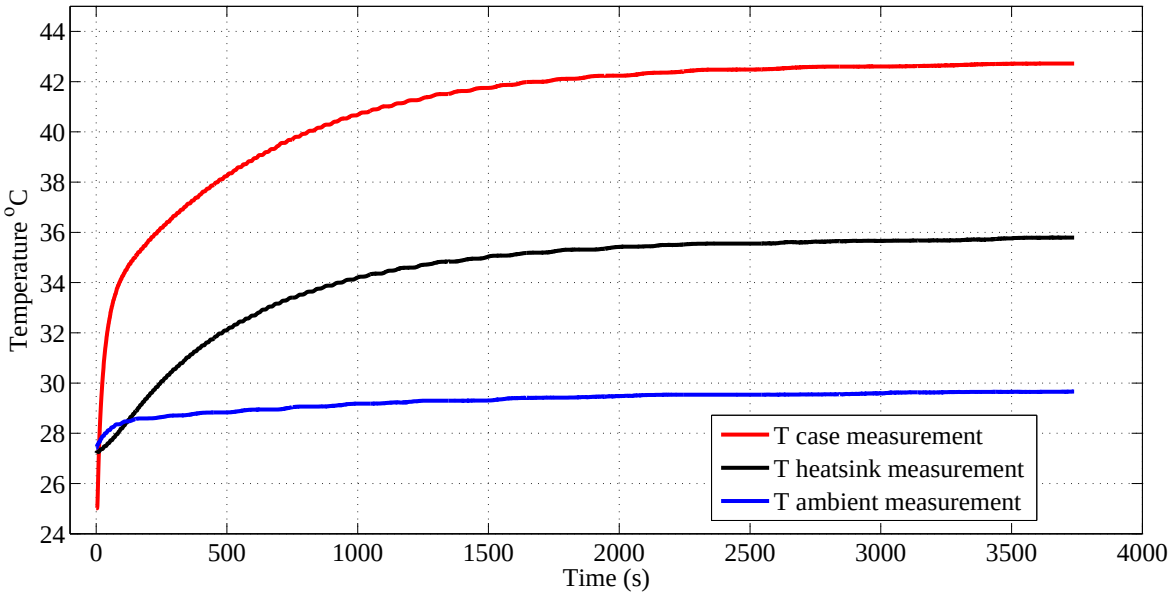


Fig. 6.39 Experimental measurement with $I_d = 9.89A$

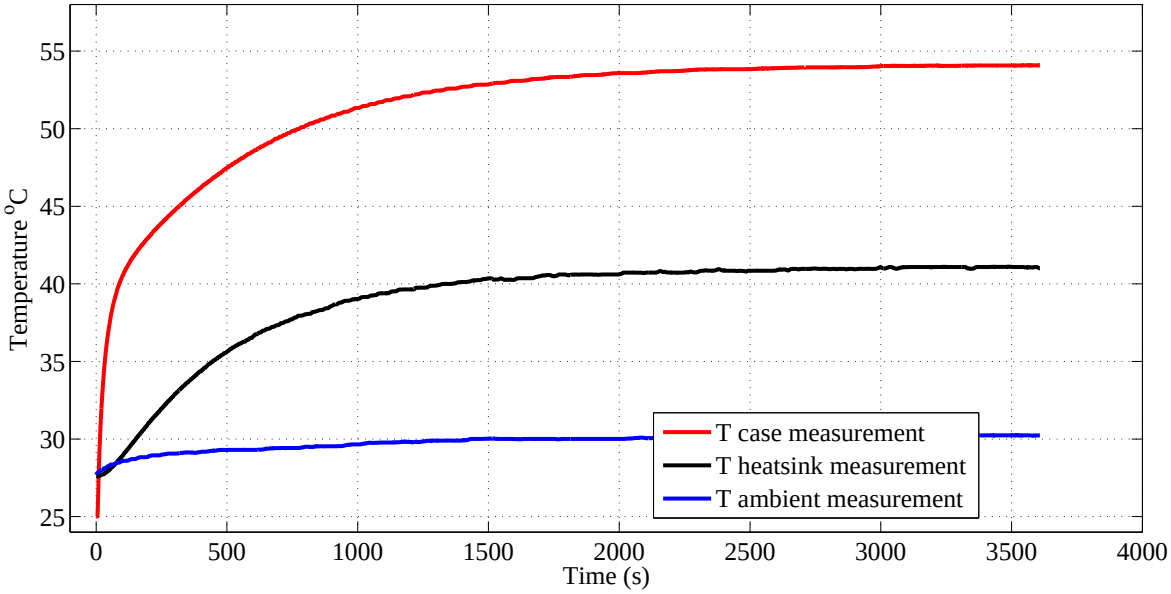


Fig. 6.40 Experimental measurement with $I_d = 12.31A$, $V_{ds_on} = 0.323V$

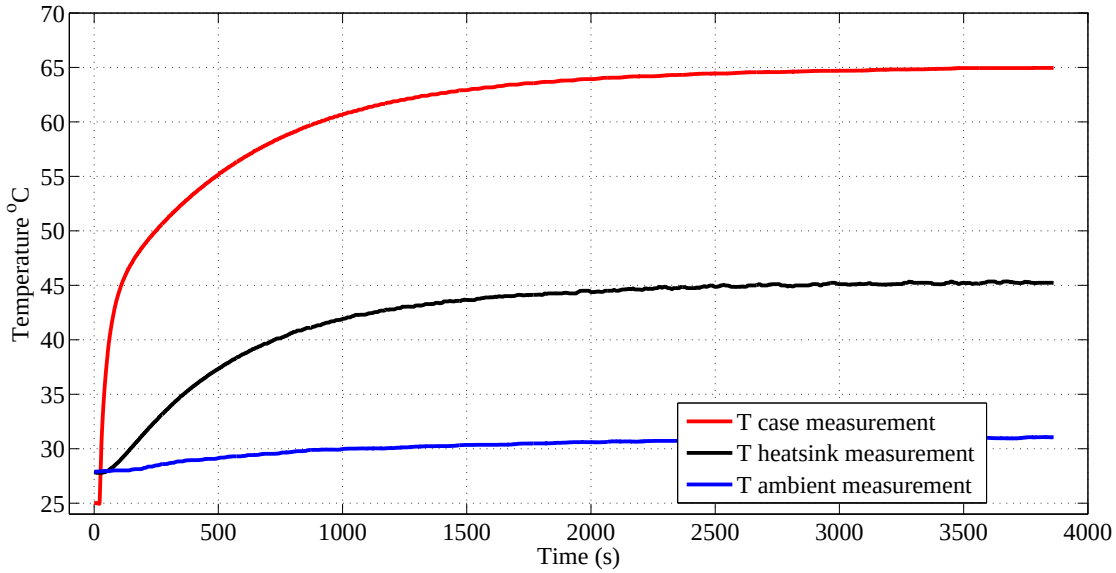


Fig. 6.41 Experimental measurement with $I_d = 13.99A$

To sum up, the steady state results are shown in Table 6.21.

Table 6.21: MOSFET thermal measurement at different drain current

I_d	$V_{ds_{on}}$	P_d	T_{case}	$T_{heatsink}$	T_{amb}
5.993	0.121	0.7252	30.92	30.55	28.95
7.99	0.172	1.3743	36.55	33.28	29.64
9.89	0.227	2.2450	42.71	35.76	29.65
12.31	0.323	3.9761	54.08	41.09	30.24
13.99	0.416	5.8198	64.94	45.23	31.06

The calculated junction temperature is calculated according to (6.2) as shown in Table 6.22. The value of the junction to case thermal resistance ($R_{TH_{jc}}$) is $0.74\frac{^\circ C}{W}$ which is founded in the MOSFET data sheet [23]. The case to source thermal resistance ($R_{TH_{cs}}$) are extracted from the data sheet (see Fig. A.15). The source to ambient thermal resistance ($R_{TH_{sa}}$) is extracted from the data sheet temperature versus power dissipation curve for various drain current (see Fig. A.17). Moreover, the junction temperature is estimated by using the normalized drain to source on resistance versus junction temperature as shown in Fig. A.1.

Table 6.22: MOSFET junction temperature calculation for different drain current

P_d (W)	$R_{TH_{jc}}$ (°C/W)	$R_{TH_{cs}}$ (°C/W)	$R_{TH_{sa}}$ (°C/W)	T_{amb} (°C)	$T_{j_{calc.}}$ (°C)	$T_{j_{estim.}}$ (°C)	Error (%)
0.7252	0.74	3	2.2	28.95	33.23198	34.4	3.11
1.3743	0.74	3	2.71	29.65	38.63696	40.05	3.53
2.2450	0.74	3	2.7	29.64	44.95641	46.88	4.10
3.9761	0.74	3	2.65	30.24	58.94341	61.98	4.89
5.8198	0.74	3	2.2	31.06	71.59426	74.21	3.52

The power dissipation and the junction temperature are also increased as the drain current is increased as shown in Fig. 6.42 and Fig. 6.43 respectively.

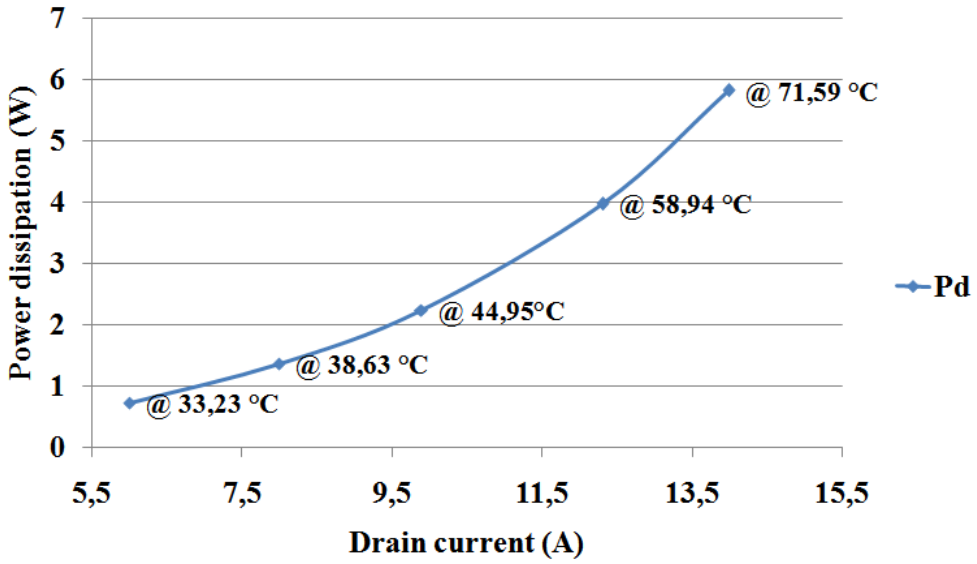


Fig. 6.42 Power dissipation versus drain current

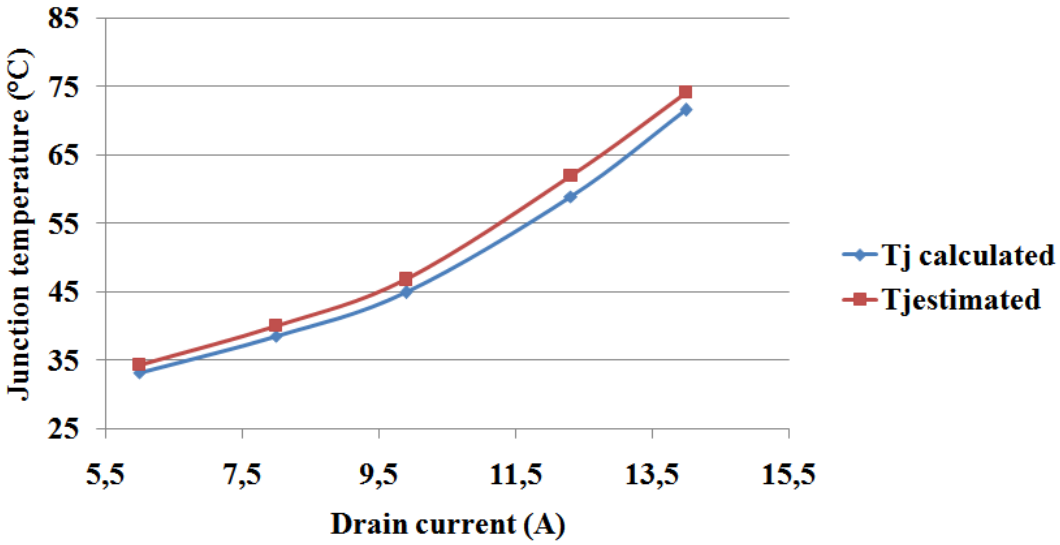


Fig. 6.43 Junction temperature versus drain current

The on-state resistance for various drain current is calculated by using the same two methods which are illustrated in TEST1 and the results are shown in Table 6.23 and Fig. 6.44

Table 6.23: Error in the drain-source resistance by using two methods

$I_d(A)$	$V_{ds_{on}}(V)$	$R_{ds_{on}}\ method1\ (\Omega)$	$R_{ds_{on}}\ method1\ (\Omega)$	Error(%)
5.993	0.121	0.02109	0,02000	5.17
7.99	0.172	0.021527	0,02102	2.36
9.89	0.227	0.022952	0,022013	4.09
12.31	0.323	0.026239	0,024304	7.37
13.99	0.416	0.029736	0,026487	10.92

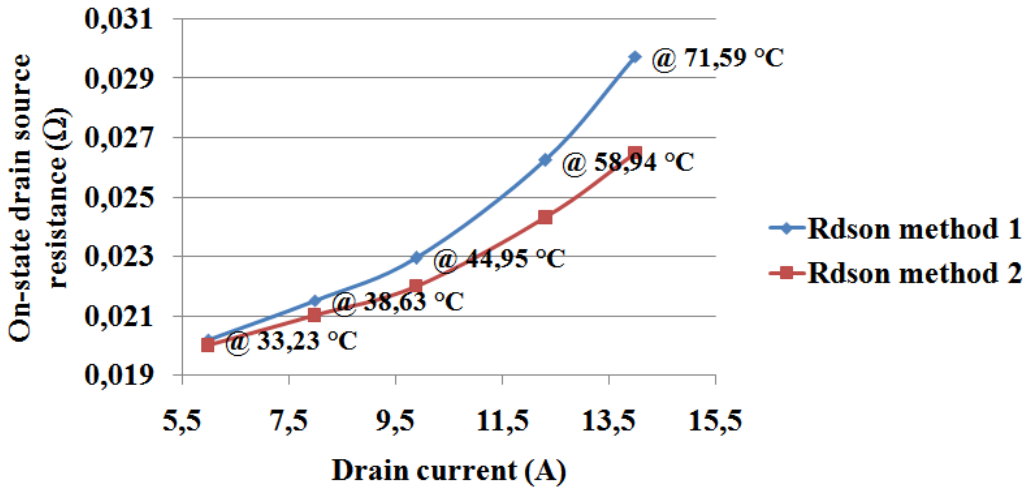


Fig. 6.44 Drain source resistance versus drain current

For the variation of the drain current from $5.993A$ to $13.99A$, the on-state resistance ($R_{ds_{on}}$) increases only about 43.35% from 49.76°C to 145.57°C for the MOSFET without heat sink (test 1). Whereas it increases about 39.75% from 38.1759°C to 106.039°C when the MOSFET is mounted onto a small heat sink (test 2). When the MOSFET is mounted onto the big heat sink, the on-state resistance ($R_{ds_{on}}$) increases about 29.07% from 33.232°C to 71.59°C. These can be illustrated in Fig. 6.45.

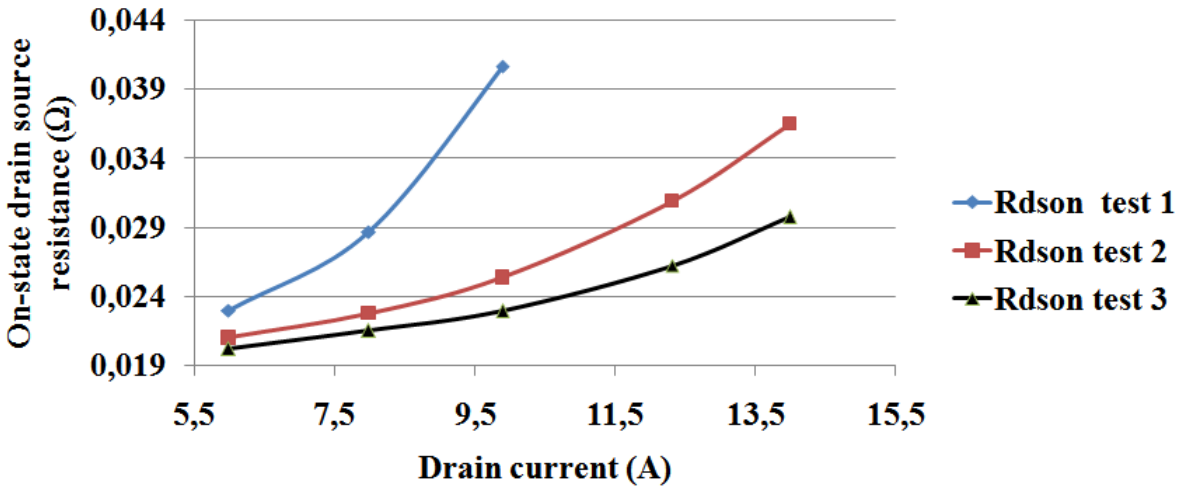


Fig. 6.45 Comparison of drain source resistance versus drain current for three different tests

2. In this part, a fan is put in front of the MOSFET to cool it as shown in Fig. 6.28. Table 6.24 shows the the case, the heat sink, and the ambient temperatures steady-state results measurement. This table also shows the on-state resistance (Rdson) which is calculated by dividing the drain-source measured voltage by the measured drain current. This resistance is used to estimate the junction temperature de-

pending on the normalized drain to source on resistance versus junction temperature curve as shown in Fig. A.1.

Table 6.24: MOSFET thermal measurement at different drain current

I_d (A)	$V_{ds_{on}}$ (V)	P_d (W)	$R_{ds_{on}}$ (Ω)	T_{case} (°C)	$T_{heatsink}$ (°C)	T_{amb} (°C)	$T_{j_{estimated}}$ (°C)
5.993	0.1189	0.7126	0.019839	27.91	26.71	26.4	28.02
7.99	0.1647	1.3159	0.0206137	32.89	27.35	26.66	31.15
9.89	0.21	2.0769	0.0212336	33.02	27.33	27	33.4
12.31	0.2733	3.3643	0.0221978	35.8	27.55	27.2	36.12
13.99	0.3222	4.5076	0.023031	38.1	27.89	27.3	38.67

In the above table, it is obvious that there are reduction in the power dissipation, the junction temperature, and the drain-source resistance as compared to the values by using chamber box:

- The minimum and maximum reduction in the power dissipation by using air forced cooling are 1.7% and 21.2% respectively as shown in Fig. 6.46.

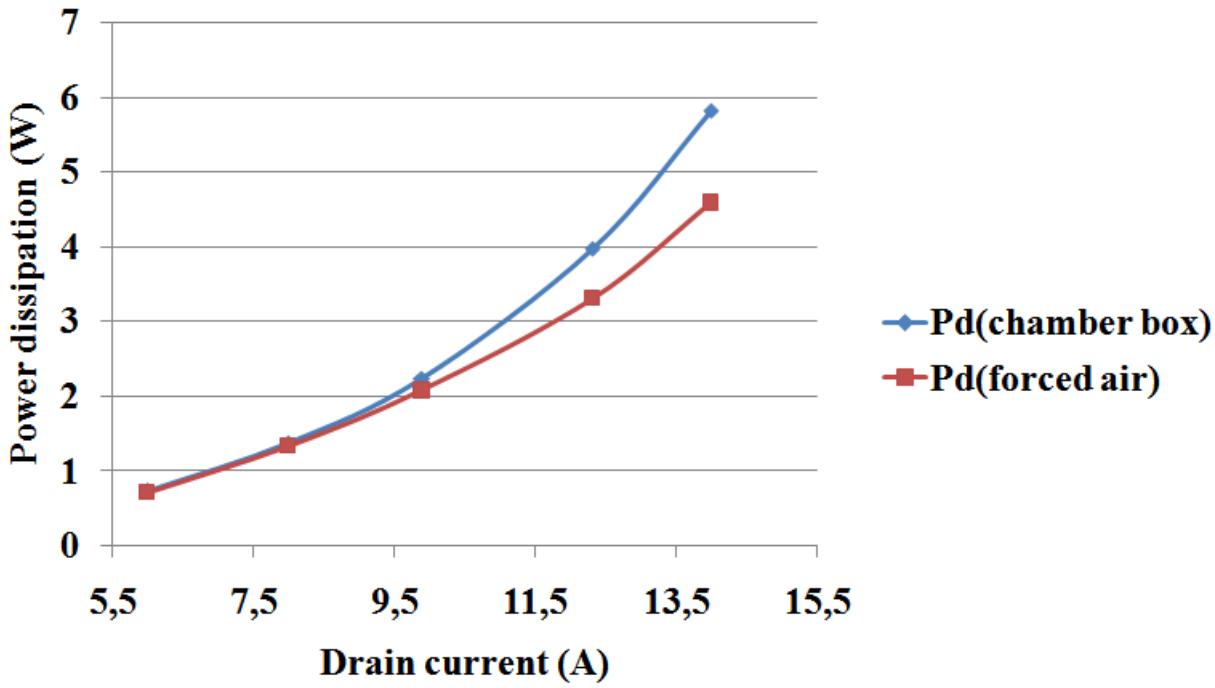


Fig. 6.46 Reduction in power dissipation by using forced air cooling

- The minimum and maximum reduction in the drain-source resistance are 1.74% and 22.5% respectively as shown in Fig. 6.47.

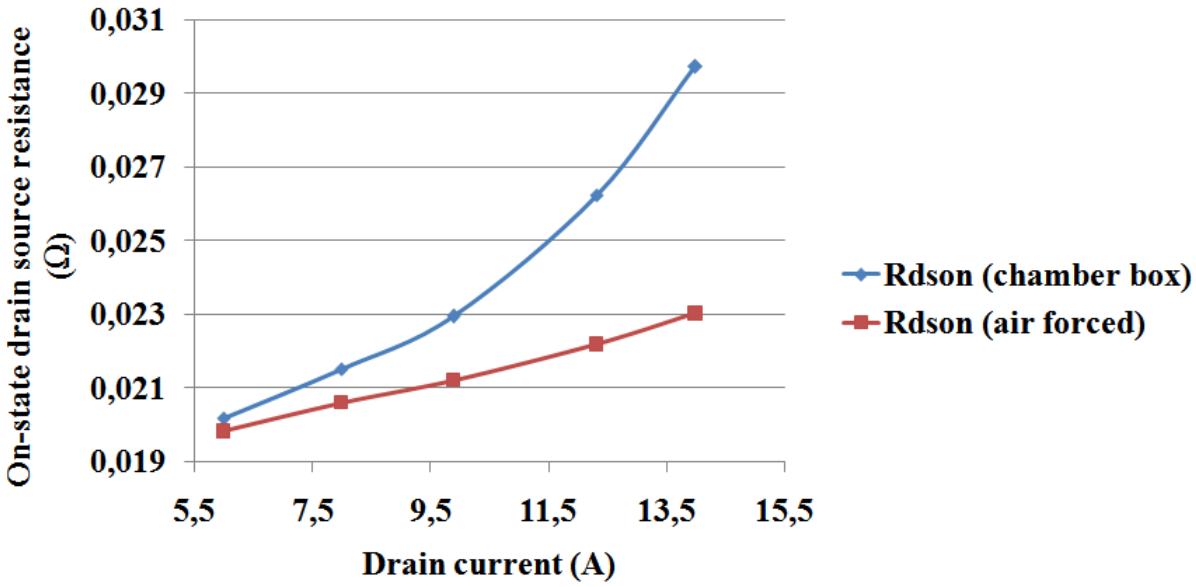


Fig. 6.47 Reduction in power dissipation by using forced air cooling

- The minimum and maximum reduction in the junction temperature are 15.67% and 45.68% respectively as shown in Fig. 6.48.

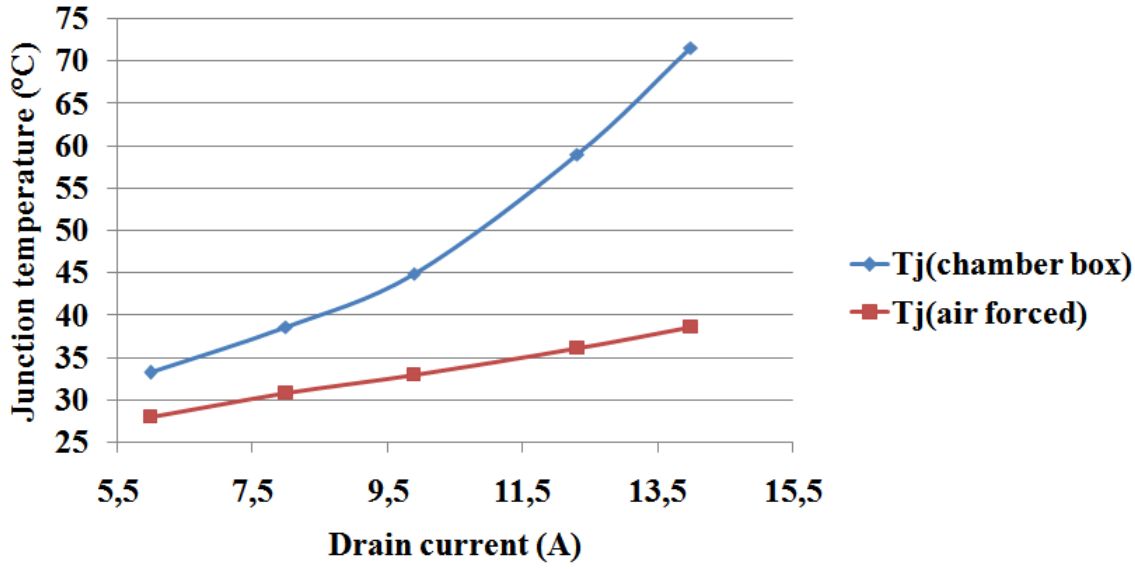


Fig. 6.48 Reduction in power dissipation by using forced air cooling

Using air forced cooling, the thermal resistance reduces approximately a factor of 2 which is calculated using (6.2). Table 6.25 shows the junction to ambient thermal resistance ($R_{TH_{jc}}$ + $R_{TH_{cs}}$ + $R_{TH_{sa}}$) by using chamber box and forced air cooling.

Table 6.25: Thermal resistance reduction by using forced air cooling

I_d (A)	$R_{TH_{ja}}$ (Chamber box) ($\frac{^\circ C}{W}$)	$R_{TH_{ja}}$ (Forced air cooling) ($\frac{^\circ C}{W}$)
5.993	5.94	2.27
7.99	6.45	3.41
9.89	6.44	3.08
12.31	6.39	2.65
13.99	5.94	2.52

Table 6.26 shows the heat sink thermal resistance which is calculated by using (6.14). The junction to case thermal resistance is $0.74\frac{^\circ C}{W}$ and the case to source thermal resistance is $3\frac{^\circ C}{W}$.

Table 6.26: Heat sink thermal resistance reduction by using forced air cooling

I_d (A)	$R_{TH_{sa}}$ (Chamber box) ($\frac{^\circ C}{W}$)	$R_{TH_{sa}}$ (Forced air cooling) ($\frac{^\circ C}{W}$)	Reduction factor
5.993	2.2	1.47	1.5
7.99	2.71	0.66	4.1
9.89	2.7	0.33	8
12.31	2.65	1.09	2.4
13.99	2.2	1.22	1.8

Simulation analysis

Fig. 6.2 is the simulation model witch is used in this test. The values of the thermal isolation pad remains the same. However, the heat sink thermal resistance for each power dissipation is extracted from the temperature versus power dissipation curve which is given in data sheet. However, the thermal capacitance is calculated by calculating the rise time of the heat sink temperature by using (6.12). change slightly with the temperature of the heat sink and that is another source of the error. Table 6.27 shows the junction to case thermal resistance, case to source thermal resistance, source to ambient thermal resistance, and heat sink thermal capacitance.

Table 6.27: Thermal capacitance which is used in PLECS

I_d (A)	$R_{TH_{jc}}$ ($\frac{^\circ C}{W}$)	$R_{TH_{cs}}$ ($\frac{^\circ C}{W}$)	$R_{TH_{sa}}$ ($\frac{^\circ C}{W}$)	τ_{TH} (sec)	C_{TH} ($\frac{J}{^\circ C}$)
5.993	0.74	3	2.2	1613	333.2
7.99	0.74	3	2.71	1057	177.3
9.89	0.74	3	2.7	1047	176.3
12.31	0.74	3	2.65	960	164.7
13.99	0.74	3	2.2	1013	209.3

The case temperatures and heat sink temperatures are compared with the measurement results. The maximum error between the simulation and measurement is about is about $\pm$ 5.9 $\%$. Fig. 6.49 to Fig. 6.53 show the simulation result for each power dissipation step.

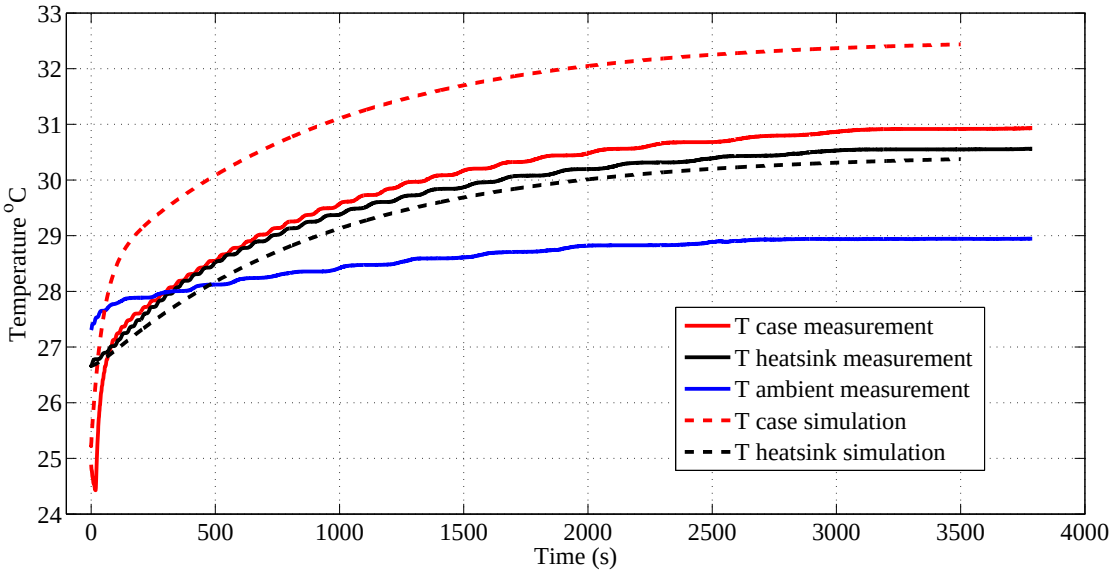


Fig. 6.49 Measurement and experimental results with $I_d = 5.984A$

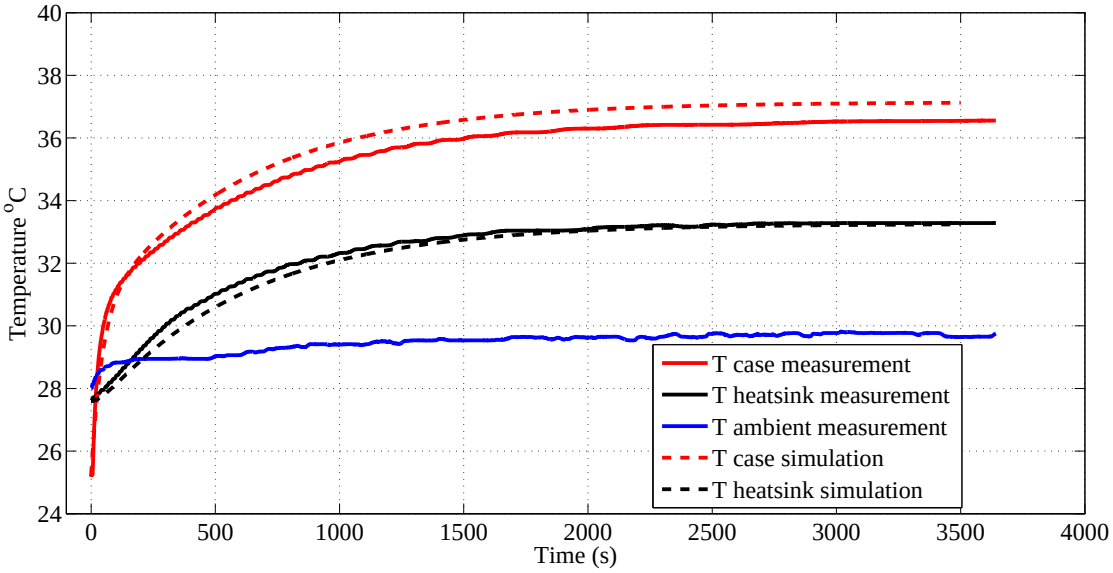


Fig. 6.50 Measurement and experimental results with $I_d = 7.99A$

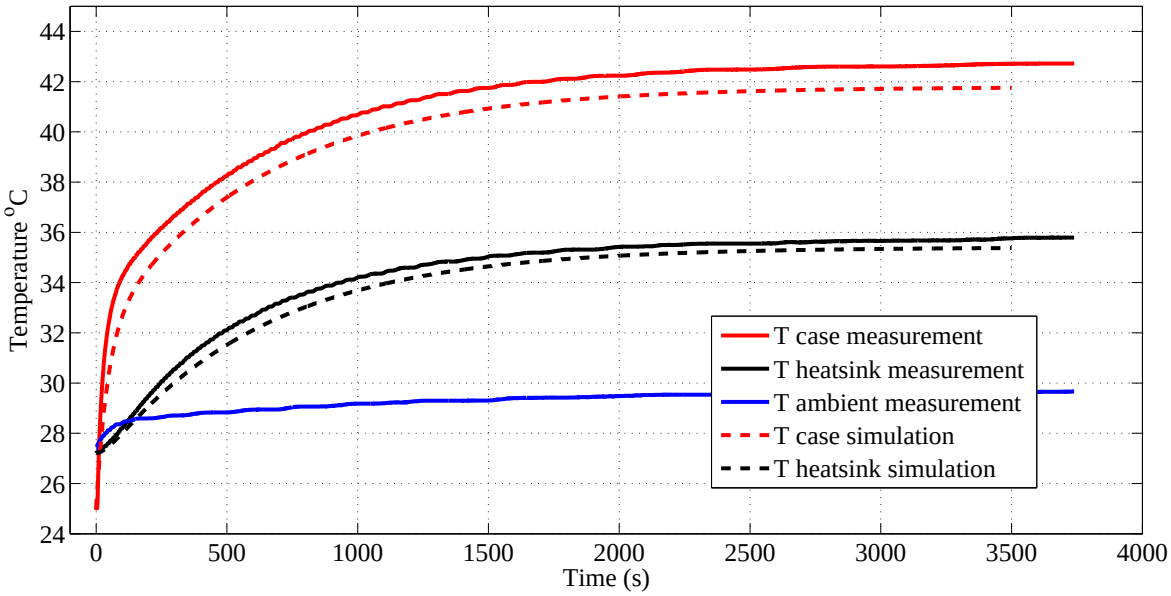


Fig. 6.51 Measurement and experimental results with $I_d = 9.89A$

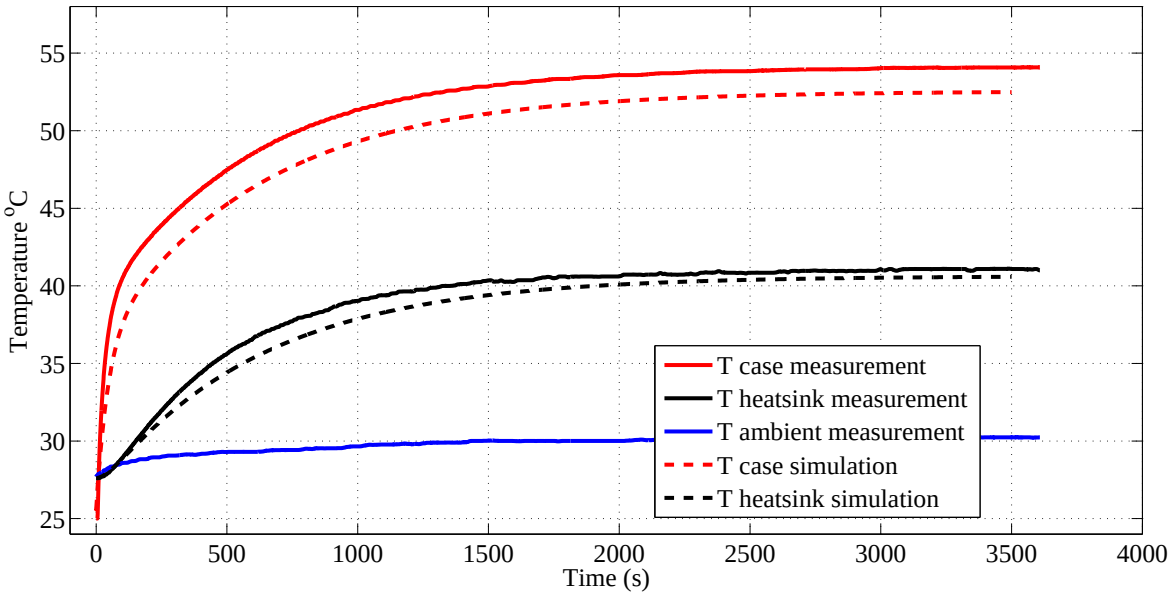


Fig. 6.52 Measurement and experimental results with$I_d = 12.31A$

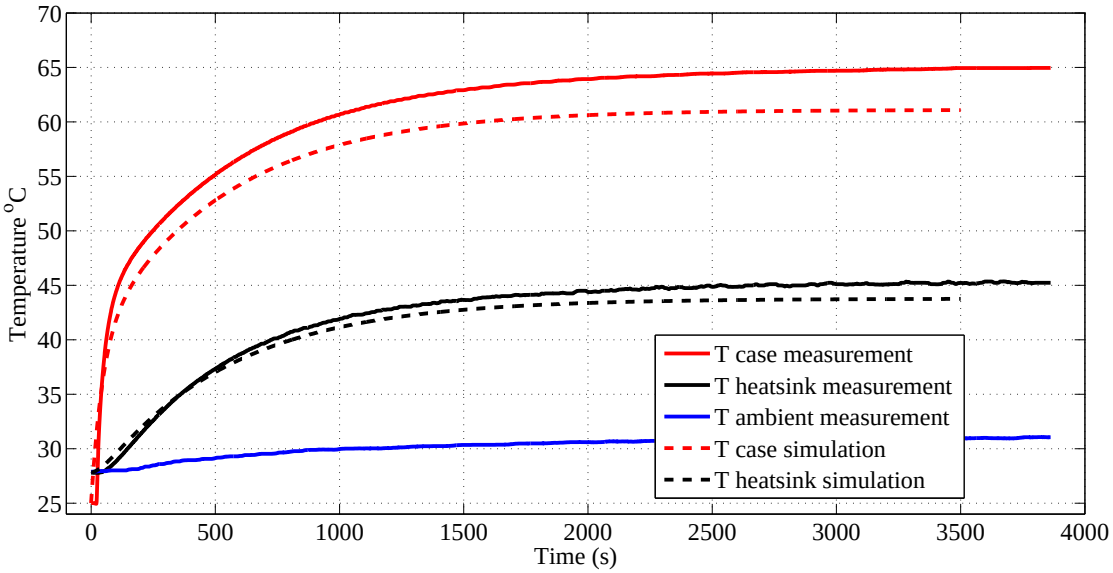


Fig. 6.53 Measurement and experimental results with $I_d = 13.99A$

Table 6.28 shows the percentage error between the simulation and experimental results

Table 6.28: Measurement and simulation thermal calculation error

P_d	$T_{casemeasur.}$	$T_{casesim.}$	Error %	$T_{hsmeasur.}$	$T_{hssim.}$	Error %
0.7252	30.92	32.44	-4.916	30.55	30.38	0.556
1.3743	36.55	37.12	-1.560	33.28	33.24	0.120
2.2450	42.71	41.75	2.248	35.76	35.38	1.063
3.9761	54.71	52.49	2.940	41.09	40.59	1.217
5.8198	64.94	61.09	5.929	45.23	43.75	3.272

Chapter 7

Conclusions

7.1 Results from present work

The main goal of this thesis was to model a MOSFET in PLECS/Simulink thermally. Results from the experiments and simulation were compared. Moreover, the temperature measurement circuit was designed to measure the case, heat sink, ambient temperature.

In order to study the thermal behavior of the MOSFET, three case set-up were considered. In the first one the MOSFET was not attached to a heat sink. The results for this test showed that the drain current could not be increased higher than $10A$ because of increasing the junction temperature too much after some minutes. In the second one, the MOSFET was screwed onto a small heat sink to cool down the device and in this case set-up two tests were studied. firstly, the MOSFET was put inside a chamber box to prevent air flowing. Secondly, a fan was used to cool down the MOSFET. The results from these tests showed that the power dissipation, on-state resistance, and junction temperature reduce by using the chamber box and forced air cooling as compared to the results from the first test as shown in Fig. 7.1. In the third one the MOSFET was screwed onto a big heat sink. Also, in this case set-up the chamber box and the forced cooling fan were studied. The results showed that the big heat sink and forced air cooling have substantial effect on the power dissipation and junction temperature of the MOSFET. Fig. 7.1 reveals how the power dissipation increases for different drain current.

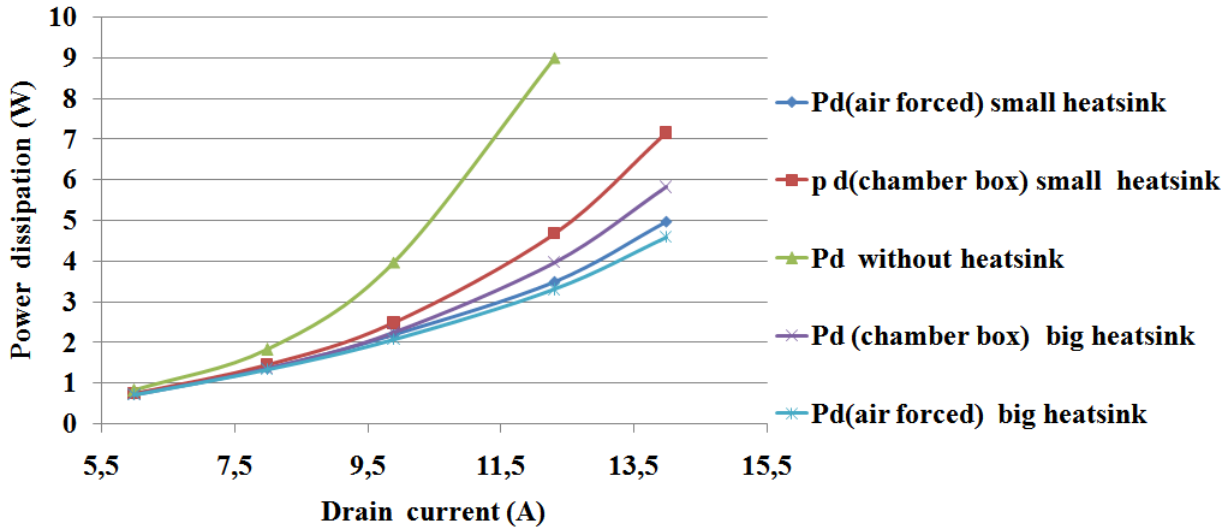


Fig. 7.1 Power dissipation versus drain current

Fig. 7.2 highlights how the junction temperature rise for different drain current.

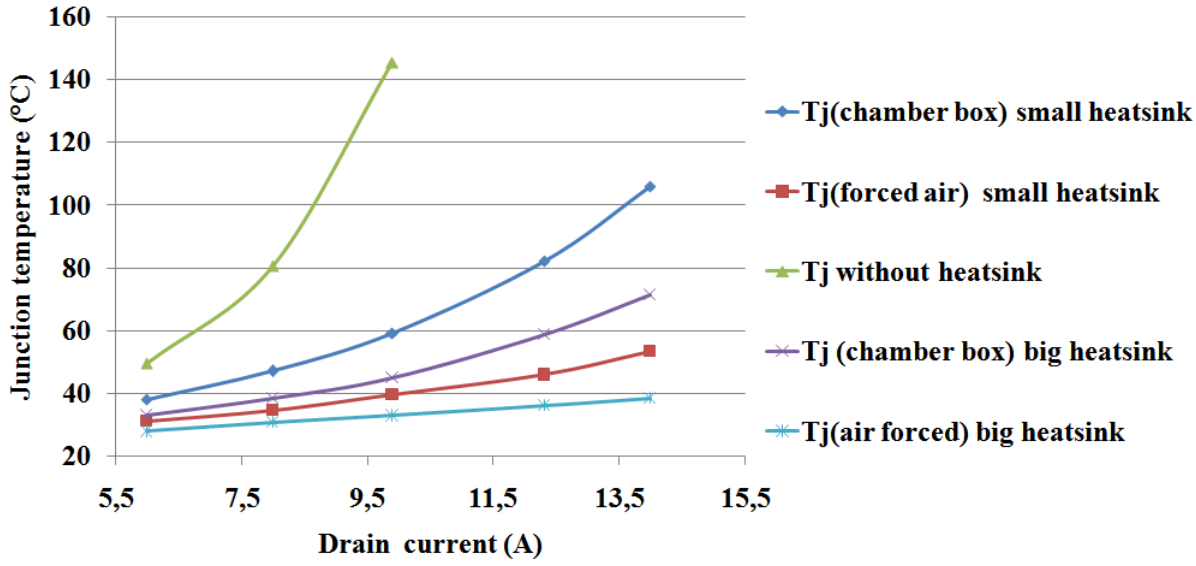


Fig. 7.2 Junction temperature versus drain current

For these three tests, satisfactory results were achieved. Comparison between the simulation and experimental results proved the accuracy of the MOSFET thermal model with maximum error about $\pm 5\%$.

In this thesis a reliable temperature measurement circuit was designed with an accuracy of $\pm 1\%$. Ensuring better cooling to reduce the power dissipation and the junction temperature which indicate that the MOSFT can still handle higher drain current.

7.2 Future work

It is recommended to further validate the developed model by:

1. Taking measurements of SIC devices to verify that they all perform similarly in terms of their thermal behavior under the same experimental power levels.

2. Using more thermocouples located at many different locations to validate the thermal model with more precision. The use of a thermal camera may also aid to verify these readings.

3. Changing the heat sink and isolation pad to check if the the whole module of the device under low and high power levels is being adequately modeled.

4. Increase the speed of the flowing air to make sure that the thermal resistance decreases by factor 4 and validate the results with the thermal model results.

5. Include the switching losses to calculate the total power dissipation. This is due to that during the transition from off-state to on-state and vice versa both the current through and the voltage across the device are larger than zero and this leads to large instantaneously power dissipation. The simulation of switching losses is usually challenging because it requires a quite detailed and accurate thermal model.

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Appendix A

Components data sheet

FAIRCHILD SEMICONDUCTOR®

HUF75639G3, HUF75639P3, HUF75639S3S, HUF75639S3

Data Sheet **December 2001**

56A, 100V, 0.025 Ohm, N-Channel UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75639.

Ordering Information

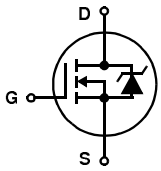
PART NUMBER	PACKAGE	BRAND
HUF75639G3	TO-247	75639G
HUF75639P3	TO-220AB	75639P
HUF75639S3S	TO-263AB	75639S
HUF75639S3	TO-262AA	75639S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75639S3ST.

Features

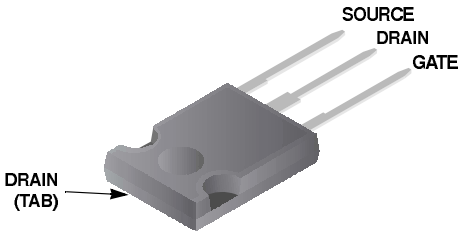
- 56A, 100V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and Saber Thermal Impedance Models
  - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC STYLE TO-247



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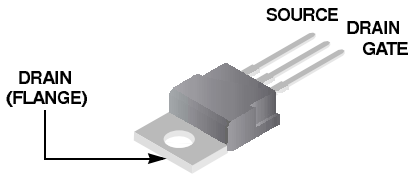

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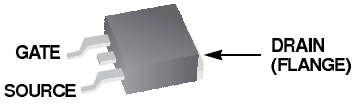
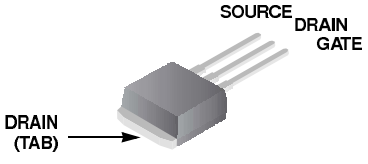


TO-262AA



Product reliability information can be found at http://www.fairchildsemi.com/products/discrete/reliability/index.html
For severe environments, see our Automotive HUFA series.
All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

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Figure A.1: MOSFET data sheet

HUF75639G3, HUF75639P3, HUF75639S3S, HUF75639S3

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Figure 2)	I_D	56	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15	
Power Dissipation	P_D	200	W
Derate Above 25^oC		1.35	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 95V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 90V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 10)		2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 56A, V_{GS} = 10V (Figure 9)		-	0.021	0.025	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	0.74	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247		-	-	30	$^oC/W$
		TO-220, TO-263		-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 50V, $I_D \cong$ 56A, R_L = 0.89Ω, V_{GS} = 10V, R_{GS} = 5.1Ω		-	-	110	ns
Turn-On Delay Time	$t_{d(ON)}$			-	15	-	ns
Rise Time	t_r			-	60	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	20	-	ns
Fall Time	t_f			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	70	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 50V, $I_D \cong$ 56A, R_L = 0.89Ω, $I_{g(REF)}$ = 1.0mA (Figure 13)	-	110	130	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	57	75	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	3.7	4.5	nC
Gate to Source Gate Charge	Q_{gs}			-	9.8	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	24	-	nC

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Figure A.2: MOSFET data sheet

HUF75639G3, HUF75639P3, HUF75639S3S, HUF75639S3

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)	-	2000	-	pF
Output Capacitance	C_{OSS}		-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	65	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 56A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 56A, dI_{SD}/dt = 100A/μs	-	-	110	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 56A, dI_{SD}/dt = 100A/μs	-	-	320	nC

Typical Performance Curves

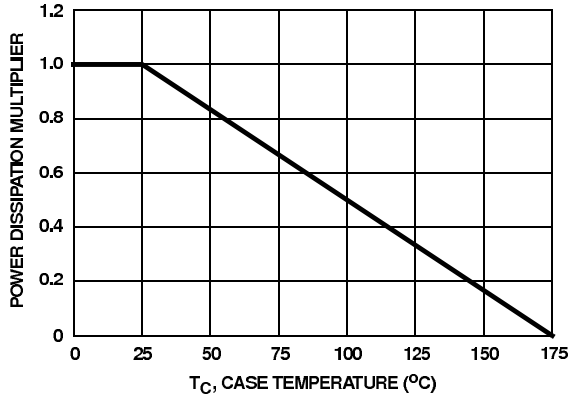

FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

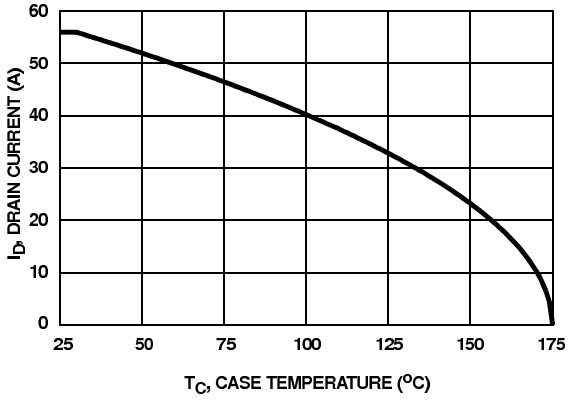

FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

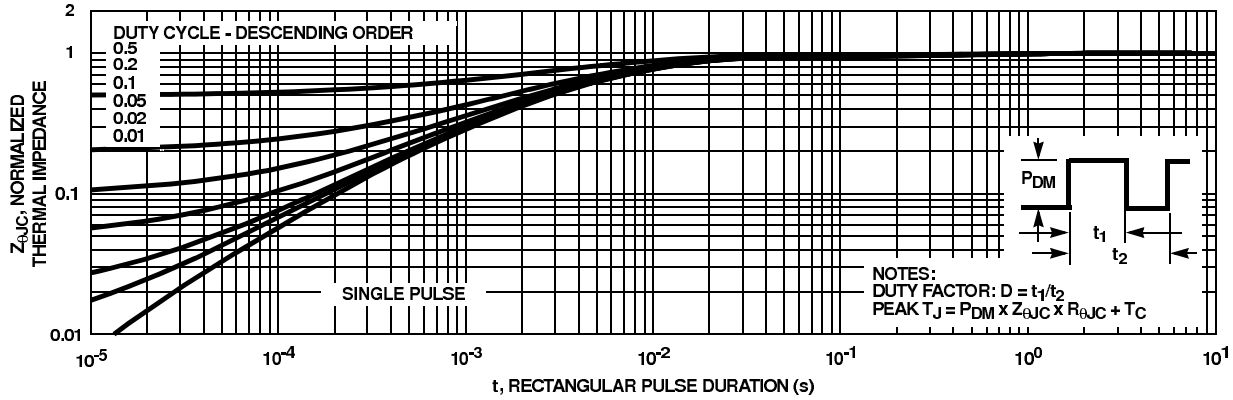

FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

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Figure A.3: MOSFET data sheet

Typical Performance Curves (Continued)

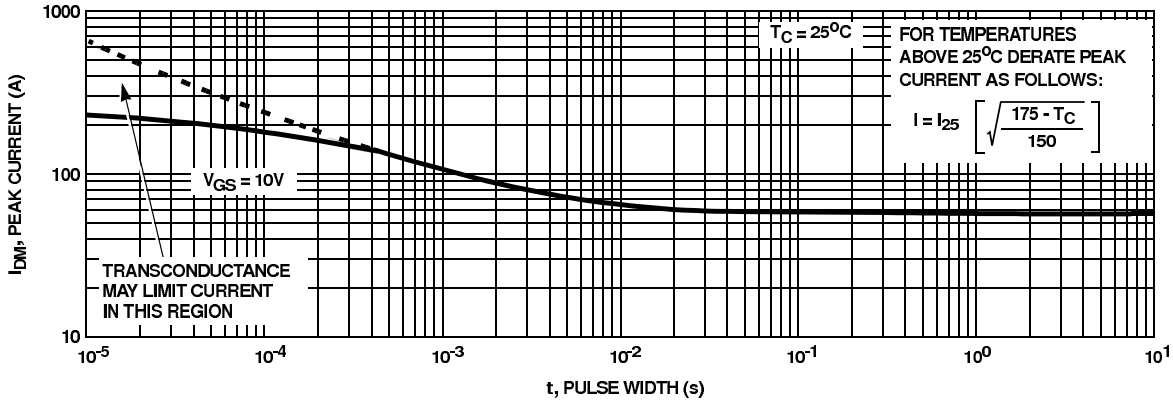


FIGURE 4. PEAK CURRENT CAPABILITY

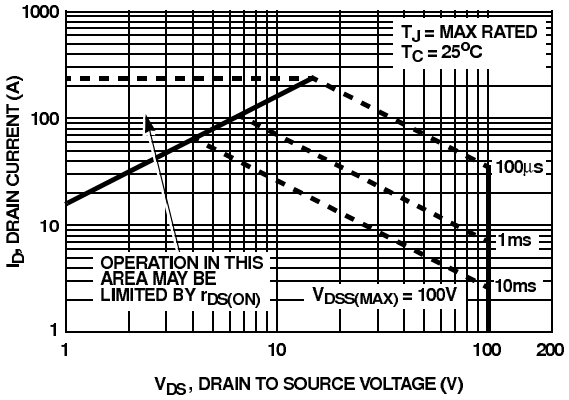
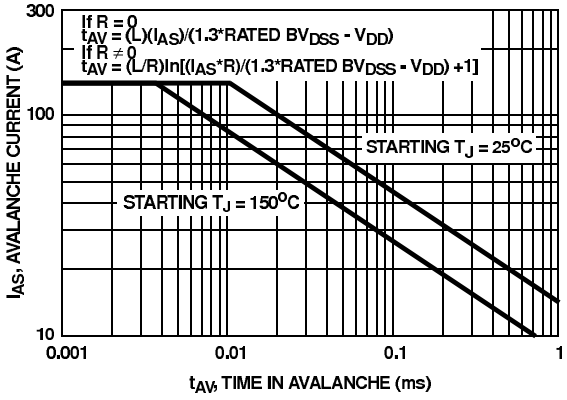


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

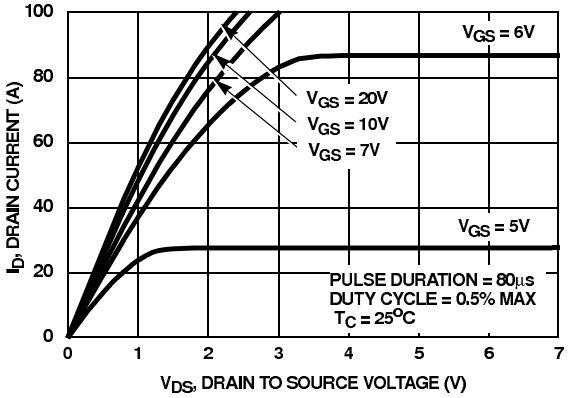


FIGURE 7. SATURATION CHARACTERISTICS

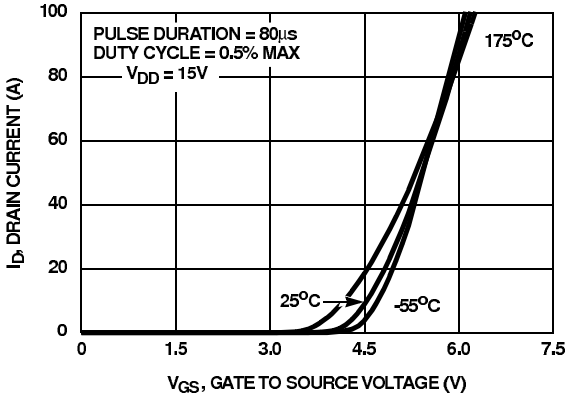


FIGURE 8. TRANSFER CHARACTERISTICS

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Figure A.4: mos4

Typical Performance Curves (Continued)

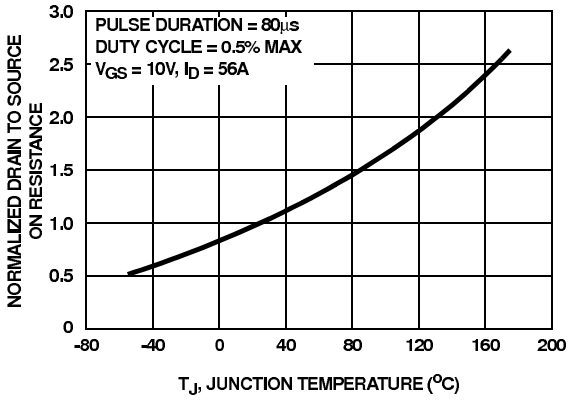


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

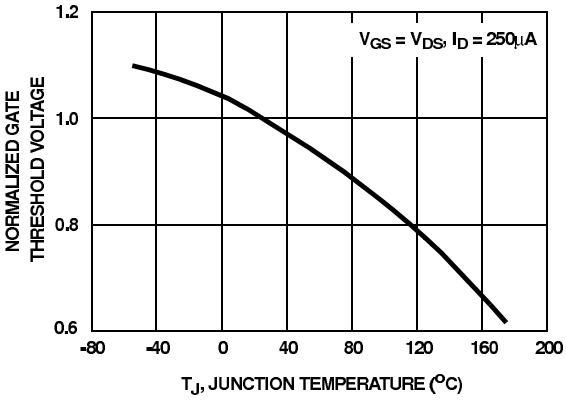


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

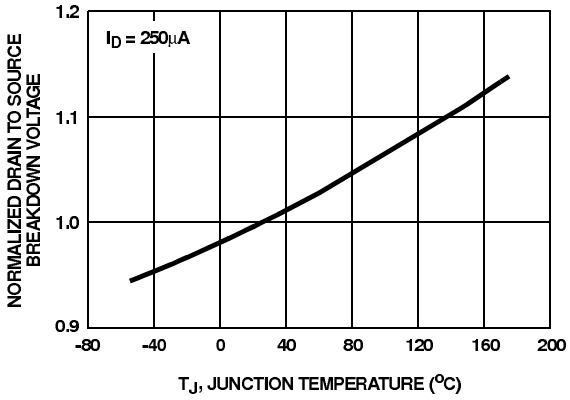


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

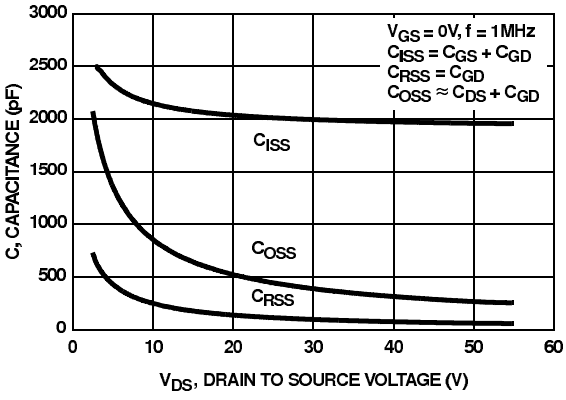
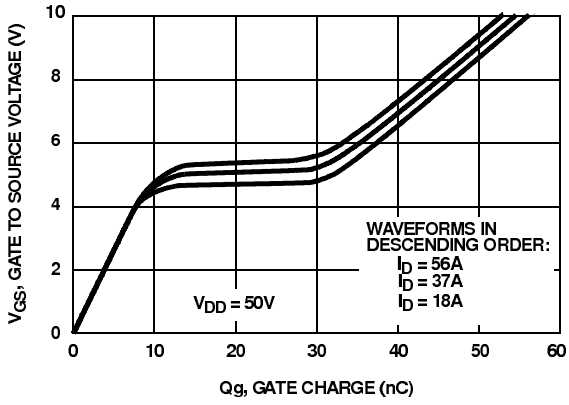


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

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Figure A.5: MOSFET data sheet

Test Circuits and Waveforms

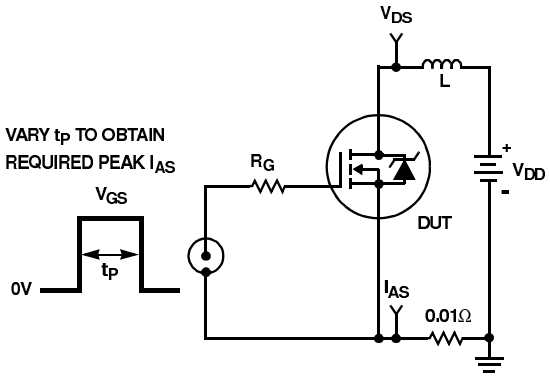

FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

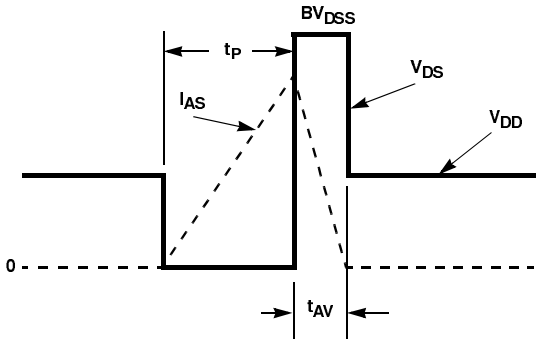

FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

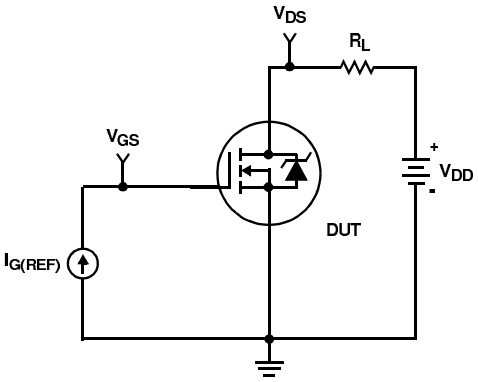

FIGURE 16. GATE CHARGE TEST CIRCUIT

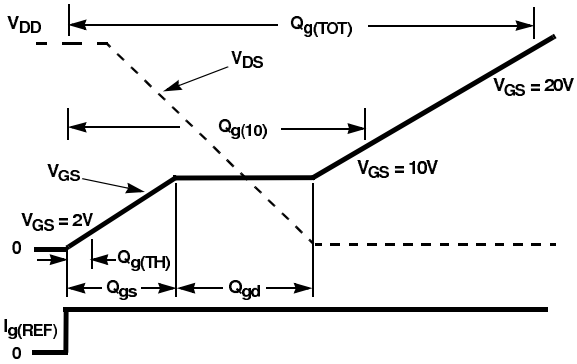

FIGURE 17. GATE CHARGE WAVEFORM

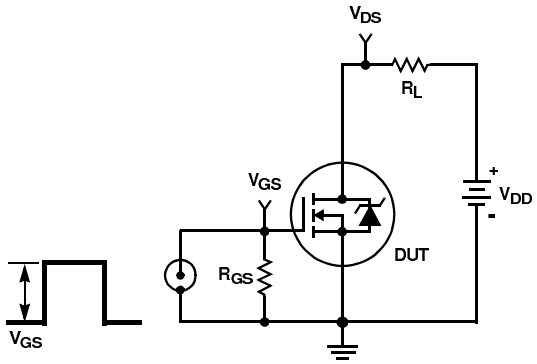

FIGURE 18. SWITCHING TIME TEST CIRCUIT

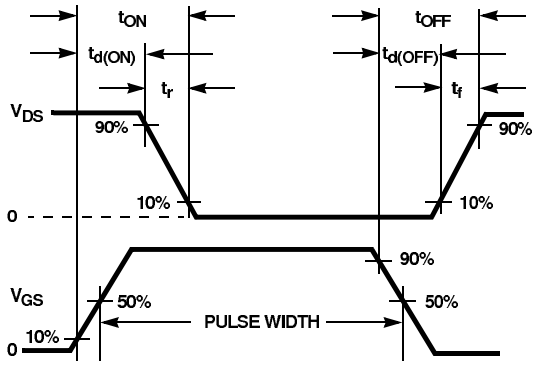

FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

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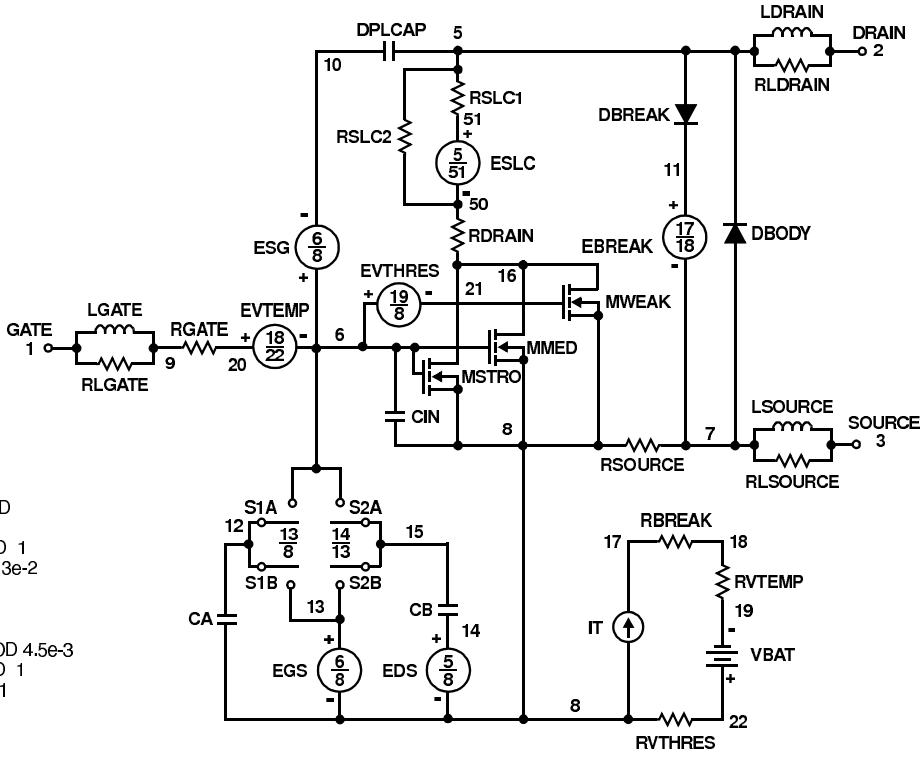
Figure A.6: MOSFET data sheet

PSPICE Electrical Model

```
SUBCKT HUF75639 2 1 3 ;       rev Oct. 98
CA  12  8 2.8e-9
CB  15  14 2.65e-9
CIN  6  8 1.9e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 110
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 2e-9
LGATE 1  9 1e-9
LSOURCE  3  7 0.47e-9

RLGATE 1 9 10
RLDRAIN 2 5 20
RLSOURCE 3 7 4.69

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 1.3e-2
RGATE  9  20 0.7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 4.5e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*115),4))}

.MODEL DBODYMOD D (IS = 1.4e-12  RS = 3.3e-3 XTI = 4.7  TRS1 = 2e-3  TRS2 = 0.1e-5  CJO = 3.3e-9  TT = 6.1e-8 M = 0.7)
.MODEL DBREAKMOD D (RS = 3.5e-  1TRS1 = 1e-  3TRS2 = 1e-6)
.MODEL DPLCAPMOD D (CJO = 2.2e-  9IS = 1e-3  0N = 10 M = 0.95 vj = 1.0)
.MODEL MMEDMOD NMOS (VTO = 3.5 KP = 4.8 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u Rg = 0.7)
.MODEL MSTROMOD NMOS (VTO = 3.97 KP = 56.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO =3.11 KP = 0.085 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 7 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 0.8e-  3TC2 = 1e-6)
.MODEL RDRAINMOD RES (TC1 = 1e-2  TC2 = 1.75e-5)
.MODEL RSLCMOD RES (TC1 = 2.8e-3 TC2 = 14e-6)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = -2.0e-3 TC2 = -1.75e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.75e-  3TC2 = 0.05e-9)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -6.0  VOFF = -3.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.5  VOFF = -6.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.5  VOFF = 4.95)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 4.95  VOFF = -2.5)

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

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Figure A.7: MOSFET data sheet

SABER Electrical Model

nom temp=25 deg c 100v Ultrafet

REV Oct. 98

```
template huf75639 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod =  (is=1.4e-12, xti=4.7, cjo=33e-10,tt=6.1e-8, m=0.7)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo=22e-10,is=1e-30,n=10,m=0.95, vj=1.0)
m..model mmedmod = (type=_n,vto=3.5,kp=4.8,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=3.97,kp=56.5,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=3.11,kp=0.085,is=1e-30, tox=1)
sw_vcsp..model s1amod =  (ron=1e-5,roff=0.1,von=-6.0,voff=-3.5)
sw_vcsp..model s1bmod =  (ron=1e-5,roff=0.1,von=-3.5,voff=-6.0)
sw_vcsp..model s2amod =  (ron=1e-5,roff=0.1,von=-2.5,voff=4.95)
sw_vcsp..model s2bmod =  (ron=1e-5,roff=0.1,von=4.95,voff=-2.5)

c.ca n12 n8 = 28.5e-10
c.cb n15 n14 = 26.5e-10
c.cin n6 n8 = 19e-10

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 2.0e-9
l.lgate n1 n9 = 1e-9
l.lsource n3 n7 = 4.69e-10

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1=0.8e-3,tc2=-1e-6
res.rdbody n71 n5 = 3.3e-3, tc1=2.0e-3, tc2=0.1e-5
res.rdbreak n72 n5 = 3.5e-1, tc1=1e-3, tc2=1e-6
res.rdrain n50 n16  = 13e-3, tc1=1e-2,tc2=1.75e-5
res.rgate n9 n20 = 0.7
res.rldrain n2 n5 = 20
res.rlgate n1 n9 = 10
res.rlsource n3 n7 = 4.69
res.rslc1 n5 n51  = 1e-6, tc1=2.8e-3,tc2=14e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 4.5e-3, tc1=0,tc2=0
res.rvtemp n18 n19  = 1, tc1=-2.75e-3,tc2=0.05e-9
res.rvthres n22 n8  = 1, tc1=-2e-3,tc2=-1.75e-5

spe.ebreak n11 n7 n17 n18 = 110
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/115))** 4))
}
}
```

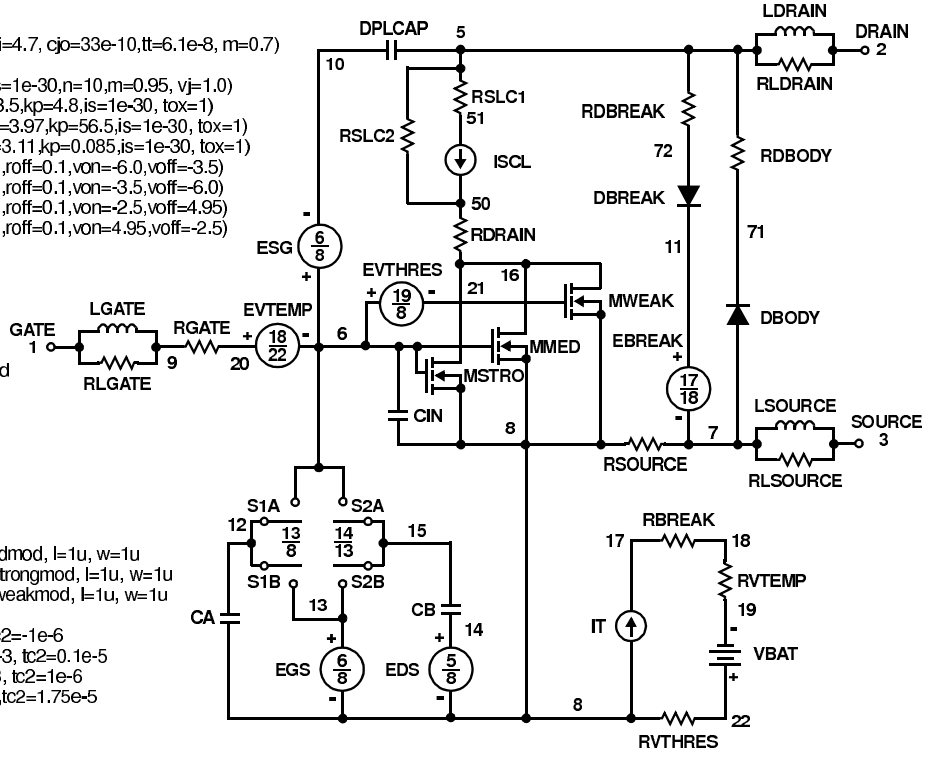

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Figure A.8: MOSFET data sheet

Spice Thermal Model

REV APRIL 1998

HUF75639

CTHERM1 TH 6 2.8e-3
CTHERM2 6 5 4.6e-3
CTHERM3 5 4 5.5e-3
CTHERM4 4 3 9.2e-3
CTHERM5 3 2 1.7e-2
CTHERM6 2 TL 4.3e-2

RTHERM1 TH 6 5.0e-4
RTHERM2 6 5 1.5e-3
RTHERM3 5 4 2.0e-2
RTHERM4 4 3 9.0e-2
RTHERM5 3 2 1.9e-1
RTHERM6 2 TL 2.9e-1

Saber Thermal Model

Saber thermal model HUF75639

template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 2.8e-3
ctherm.ctherm2 6 5 = 4.6e-3
ctherm.ctherm3 5 4 = 5.5e-3
ctherm.ctherm4 4 3 = 9.2e-3
ctherm.ctherm5 3 2 = 1.7e-2
ctherm.ctherm6 2 tl = 4.3e-2

rtherm.rtherm1 th 6 = 5.0e-4
rtherm.rtherm2 6 5 = 1.5e-3
rtherm.rtherm3 5 4 = 2.0e-2
rtherm.rtherm4 4 3 = 9.0e-2
rtherm.rtherm5 3 2 = 1.9e-1
rtherm.rtherm6 2 tl = 2.9e-1
}

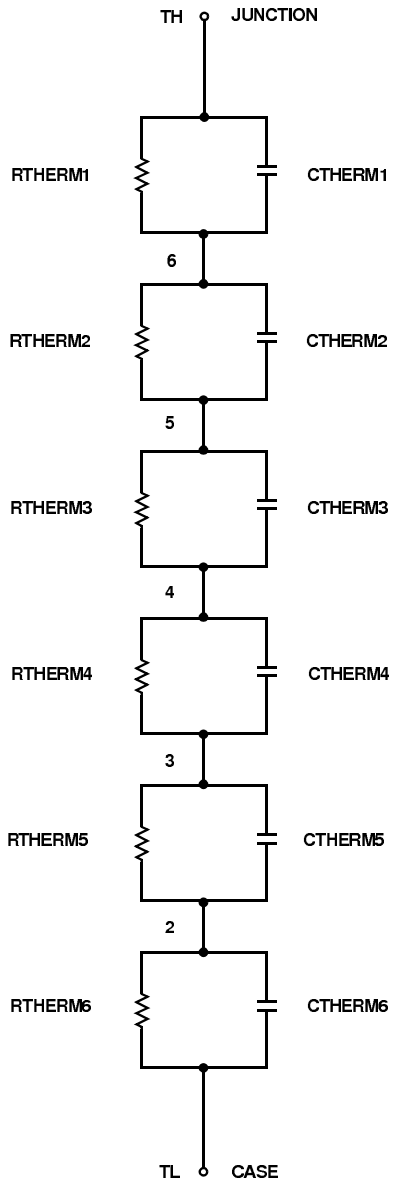

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Figure A.9: MOSFET data sheet

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DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E²CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H4

Figure A.10: MOSFET data sheet

Bulletin PD-20675 rev. B 08/04

International
IOR Rectifier

40CPQ080PbF
40CPQ100PbF

SCHOTTKY RECTIFIER

40 Amp

$I_{F(AV)}$ = 40Amp
V_R = 80 -100V

Major Ratings and Characteristics

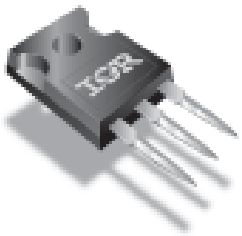
Characteristics	Values	Units
$I_{F(AV)}$ Rectangular waveform	40	A
V_{RRM}	80/100	V
I_{FSM} @tp=5µs sine	2950	A
V_F @20 Apk, T_J=125°C (per leg)	0.61	V
T_J	-55 to 175	°C

Description/ Features

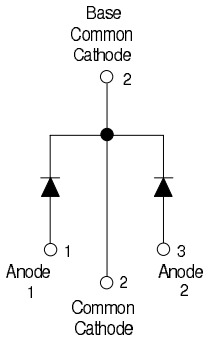
The 40CPQ...PbF center tap Schottky rectifier has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175° C junction temperature. Typical applications are in switching power supplies, converters, free-wheeling diodes, and reverse battery protection.

- 175° C T_J operation
- Center tap TO-247 package
- High purity, high temperature epoxy encapsulation for enhanced mechanical strength and moisture resistance
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Lead-Free ("PbF" suffix)

Case Styles



TO-247AC

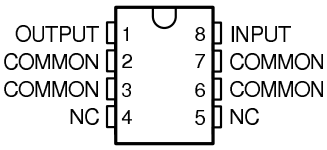


μA78L00 SERIES
POSITIVE-VOLTAGE REGULATORS

SLVS010P – JANUARY 1976 – REVISED JUNE 2002

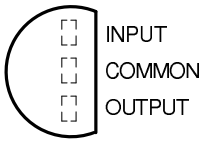
- **3-Terminal Regulators**
- **Output Current up to 100 mA**
- **No External Components**
- **Internal Thermal-Overload Protection**
- **Internal Short-Circuit Current Limiting**
- **Direct Replacements for Fairchild μA78L00 Series**

D PACKAGE
(TOP VIEW)



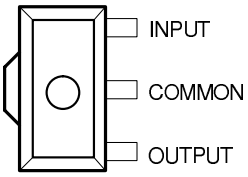
NC – No internal connection

LP PACKAGE
(TOP VIEW)



TO–226AA

PK PACKAGE
(TOP VIEW)



The center lead is in electrical contact with the tab.

description

This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. One of these regulators can deliver up to 100 mA of output current. The internal limiting and thermal-shutdown features of these regulators essentially make them immune to overload. When used as a replacement for a zener diode-resistor combination, an effective improvement in output impedance can be obtained, together with lower bias current.

The μA78L00C and μA78L00AC series are characterized for operation over the virtual junction temperature range of 0°C to 125°C. The μA78L05AI is characterized for operation over the virtual junction temperature range of –40°C to 125°C.

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TEXAS INSTRUMENTS
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Figure A.11: Small heat sink

JUMO GmbH & Co. KG

Delivery address: Mackenrodtstraße 14,
36039 Fulda, Germany
Postal address: 36035 Fulda, Germany
Phone: +49 661 6003-0
Fax: +49 661 6003-607
e-mail: mail@jumo.net
Internet: www.jumo.net

JUMO Instrument Co. Ltd.

JUMO House
Temple Bank, Riverway
Harlow, Essex CM 20 2TT, UK
Phone: +44 1279 635533
Fax: +44 1279 635262
e-mail: sales@jumo.co.uk
Internet: www.jumo.co.uk

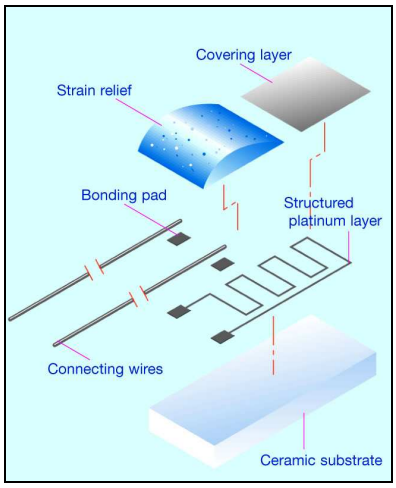
JUMO PROCESS CONTROL INC.

885 Fox Chase, Suite 103
Coatesville PA 19320, USA
Phone: 610-380-8002
1-800-554-JUMO
Fax: 610-380-8009
e-mail: info@JumoUSA.com
Internet: www.JumoUSA.com

Platinum-chip temperature sensors with connecting wires to EN 60 751

- **for temperatures from -70 to +600 °C**
- **standardized nominal values and tolerances**
- **resistance values from 20 to 5000 Ω**
- **linear characteristic**
- **fast response**
- **highly resistant to shock and vibration**
- **low price level**

PCA style



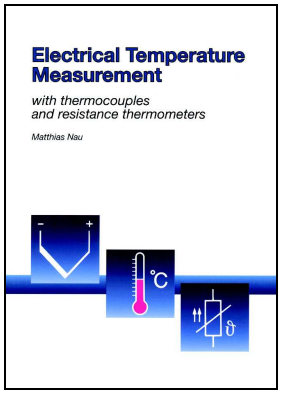
Introduction

Platinum-chip temperature sensors belong to the category of temperature sensors that incorporate thin-film techniques. They are produced at JUMO under clean-room conditions using state-of-the-art technology. A platinum layer, which constitutes the active layer, is sputtered onto a ceramic substrate and subsequently formed into a serpentine structure by a photolithographic procedure. Afterwards, a laser trimming process is used for fine calibration. After calibration, a special glass covering layer is fused onto the platinum serpentine, as a protection against external effects and for insulation. The electrical connection is made through contact areas to which the connecting wires are bonded. Depending on the version, the connecting wires may consist of different materials and may, within certain limits, also have varying lengths and diameters. A further glass layer that is applied to the contact area fixes the connecting wires and additionally provides strain relief.

A large variety of PCA style platinum-chip temperature sensors can be supplied ex-stock as Pt100, Pt500 or Pt1000 temperature sensors. Special nominal values can be produced on request. High-resistance platinum-chip temperature sensors in small sizes are also available. And, thanks to their low mass, very fast response times are achieved. Furthermore, they are outstandingly resistant to shock and vibration when installed and fixed. The operating temperature depends on the particular version, but generally covers -70 to +600 °C. However, these platinum-chip temperature sensors can also be used with temperatures far below -70 °C, provided that shifts in the nominal value and hysteresis effects, which may occur within certain limits, can be tolerated.

Most temperature applications in the market make use of platinum-chip temperature sensors as the active component for acquiring temperature. Typical application areas can be found in HVAC, medical and laboratory technology, white goods, automobiles and utility vehicles as well as in machinery construction and industrial engineering.

Technical publication



This revised edition takes account of altered standards and recent developments. The new chapter "Measurement uncertainty" incorporates the basic concept of the internationally recognized ISO guideline "Guide to the expression of uncertainty in measurement" (abbreviated: GUM).
In addition, the chapter on explosion protection for thermometers has been updated in view of the European Directive 94/9/EC, which has been in force since 1st July 2003.

February 2003, 164 pages
Publication FAS 146
Sales No. 90/00085081
ISBN 3-935742-07-X

JUMO platinum temperature sensors

Construction and application of platinum temperature sensors	Data Sheet 90.6000
Platinum-glass temperature sensors	Data Sheet 90.6021
Platinum-ceramic temperature sensors	Data Sheet 90.6022
Platinum-foil temperature sensors	Data Sheet 90.6023
Platinum-glass temperature sensors with glass extension	Data Sheet 90.6024
Platinum-chip temperature sensors with connecting wires	Data Sheet 90.6121
Platinum-chip temperature sensors on epoxy card	Data Sheet 90.6122
Platinum-chip temperature sensors with terminal clamps	Data Sheet 90.6123
Platinum-chip temperature sensors in cylindrical style	Data Sheet 90.6124
Platinum-chip temperature sensors in SMD style	Data Sheet 90.6125

01.05/00311575

Figure A.12: pt1000 data sheet

Heraeus

Platinum Resistance Temperature Detector M 422

M series PRTDs are especially robust and are designed for large volume applications where long term stability, interchangeability and accuracy over a large temperature range are vital. Typical applications are Automotive, White Goods, HVAC, Energy Management, Medical and Industrial Equipment.

Nominal Resistance R_0	Tolerance	Order No. Plastic bag	Order No. Blister reel
100 Ohm at 0°C	DIN EN 60751, class B DIN EN 60751, class A DIN EN 60751, class 1/3 DIN	32 208 392 32 208 498 32 208 500	32 208 520 32 208 521 32 208 522
500 Ohm at 0°C	DIN EN 60751, class B DIN EN 60751, class A DIN EN 60751, class 1/3 DIN	32 208 414 32 208 501 32 208 502	32 208 523 32 208 524 32 208 525
1000 Ohm at 0°C	DIN EN 60751, class B DIN EN 60751, class A DIN EN 60751, class 1/3 DIN	32 208 499 32 208 503 32 208 537	32 208 526 32 208 527

The measuring point for the nominal resistance is defined at 8 mm from the end of the sensor body.

Specification DIN EN 60751 (according to IEC 751)

Temperature range -70°C to +500°C (continuous operation)
(temporary use to 550 °C possible)
Tolerance class B: - 70 °C to + 500 °C
Tolerance class A: - 50 °C to + 300 °C
Tolerance class 1/3 DIN: 0 °C to + 150 °C

Temperature coefficient TC = 3850 ppm/K ; 3750 ppm/K available on request

Leads Pt clad Ni wire
Recommend connection technology:
Welding, Crimping and Brazing

Lead lengths (L) 10 mm +- 1 mm

Longterm stability max. R_0-drift 0.04% after 1000 h at 500 °C

Vibration resistance at least 40 g acceleration at 10 to 2000 Hz, depends on installation

Shock resistance at least 100 g acceleration with 8ms half sine wave, depends on installation

Environmental conditions unhoused for dry environments only

Insulation resistance > 100 MΩ at 20 °C; > 2 MΩ at 500 °C

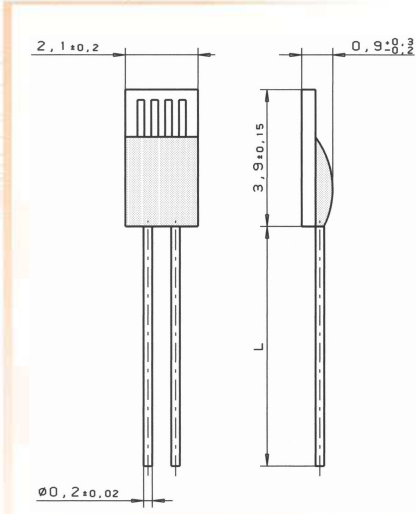
Self heating 0.3 K/mW at 0 °C

Response time

water current (v = 0.4 m/s):	$t_{0.5}$ = 0.07 s
	$t_{0.9}$ = 0.20 s
air stream (v = 2 m/s):	$t_{0.5}$ = 3.2 s
	$t_{0.9}$ = 11 s

Measuring current
100 Ω: 0.3 to 1.0 mA
500 Ω: 0.1 to 0.7 mA
1000 Ω: 0.1 to 0.3 mA
(self heating has to be considered)

Note Other tolerances, values of resistance and wire lengths are available on request.



We reserve the right to make alterations and technical data printed. All technical data serves as a guideline and does not guarantee particular properties to any products.

Heraeus Sensor Technology GmbH, Reinhard- Heraeus- Ring 23, 63801 Kleinostheim, Germany
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name of document: 30910021 Index A
Status: 09/2008

Figure A.13: pt1000 data sheet

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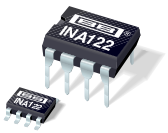


INA122

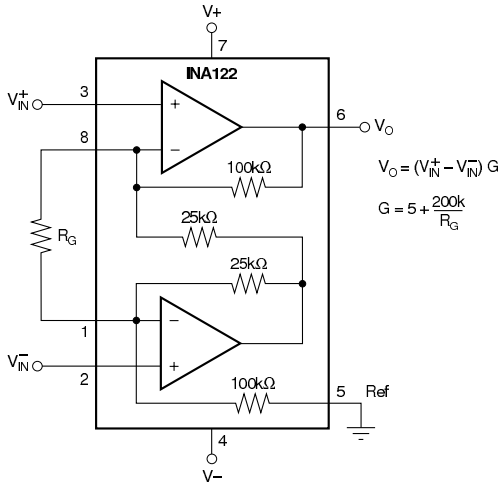
Single Supply, *Micro*Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 60μA
- WIDE POWER SUPPLY RANGE
  Single Supply: 2.2V to 36V
  Dual Supply: –0.9/+1.3V to ±18V
- COMMON-MODE RANGE TO (V–)–0.1V
- RAIL-TO-RAIL OUTPUT SWING
- LOW OFFSET VOLTAGE: 250μV max
- LOW OFFSET DRIFT: 3μV/°C max
- LOW NOISE: 60nV/√Hz
- LOW INPUT BIAS CURRENT: 25nA max
- 8-PIN DIP AND SO-8 SURFACE-MOUNT

APPLICATIONS

- PORTABLE, BATTERY OPERATED SYSTEMS
- INDUSTRIAL SENSOR AMPLIFIER:
  Bridge, RTD, Thermocouple
- PHYSIOLOGICAL AMPLIFIER:
  ECG, EEG, EMG
- MULTI-CHANNEL DATA ACQUISITION



DESCRIPTION

The INA122 is a precision instrumentation amplifier for accurate, low noise differential signal acquisition. Its two-op-amp design provides excellent performance with very low quiescent current, and is ideal for portable instrumentation and data acquisition systems.

The INA122 can be operated with single power supplies from 2.2V to 36V and quiescent current is a mere 60μA. It can also be operated from dual supplies. By utilizing an input level-shift network, input common-mode range extends to 0.1V below negative rail (single supply ground).

A single external resistor sets gain from 5V/V to 10000V/V. Laser trimming provides very low offset voltage (250μV max), offset voltage drift (3μV/°C max) and excellent common-mode rejection.

Package options include 8-pin plastic DIP and SO-8 surface-mount packages. Both are specified for the –40°C to +85°C extended industrial temperature range.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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PDS-1388B

Printed in U.S.A. October, 1997

SBOS069

Figure A.14: 4 A Dual-Channel Gate Driver ADUM3220 pin configuration

Sil-Pad® K-10

The High Performance Kapton®-Based Insulator

Features and Benefits

- Thermal impedance: 0.41 °C-in²/W (@50 psi)
- Tough dielectric barrier against cut-through
- High performance film
- Designed to replace ceramic insulators

Sil-Pad K-10 is a high performance insulator. It combines special film with a filled silicone rubber. The result is a product with good cut-through properties and excellent thermal performance.

Sil-Pad K-10 is designed to replace ceramic insulators such as Beryllium Oxide, Boron Nitride and Alumina. Ceramic insulators are expensive and they break easily. Sil-Pad K-10 eliminates breakage and costs much less than ceramics.

TYPICAL PROPERTIES OF SIL-PAD K-10

PROPERTY	IMPERIAL VALUE	METRIC VALUE	TEST METHOD
Color	Beige	Beige	Visual
Reinforcement Carrier	Kapton	Kapton	—
Thickness (inch) / (mm)	0.006	0.152	ASTM D374
Hardness (Shore A)	90	90	ASTM D2240
Breaking Strength (lbs/inch) / (kN/m)	30	5	ASTM D1458
Elongation (%)	40	40	ASTM D412
Tensile Strength (psi) / (MPa)	5000	34	ASTM D412
Continuous Use Temp (°F) / (°C)	-76 to 356	-60 to 180	—
ELECTRICAL			
Dielectric Breakdown Voltage (Vac)	6000	6000	ASTM D149
Dielectric Constant (1000 Hz)	3.7	3.7	ASTM D150
Volume Resistivity (Ohm-meter)	10^{12}	10^{12}	ASTM D257
Flame Rating	VTM-O	VTM-O	U.L.94
THERMAL			
Thermal Conductivity (W/m-K)	1.3	1.3	ASTM D5470

THERMAL PERFORMANCE vs PRESSURE					
Pressure (psi)	10	25	50	100	200
TO-220 Thermal Performance (°C/W)	2.35	2.19	2.01	1.87	1.76
Thermal Impedance (°C-in²/W) (1)	0.86	0.56	0.41	0.38	0.33

1) The ASTM D5470 test fixture was used. The recorded value includes interfacial thermal resistance. These values are provided for reference only. Actual application performance is directly related to the surface roughness, flatness and pressure applied.

Typical Applications Include:

- Power supplies
- Motor controls
- Power semiconductors

Configurations Available:

- Sheet form, die-cut parts and roll form
- With or without pressure sensitive adhesive

Building a Part Number

SPK10 – 0.006 – AC – 1212 – NA

- Section A: SPK10 = Sil-Pad K10 Material
- Section B: Standard thicknesses available: 0.006"
- Section C: AC = Adhesive, one side; 00 = No adhesive
- Section D: ____ = Standard configuration dash number, 1212 = 12" x 12" sheets, 12250 = 12" x 250' rolls, or 00 = custom configuration
- Section E: NA = Selected standard option. If not selecting a standard option, insert company name, drawing number, and revision level.

Standard Options

example

Note: To build a part number, visit our website at www.bergquistcompany.com.

Sil-Pad®: U.S. Patents 4,574,879; 4,602,125; 4,602,678; 4,685,987; 4,842,911 and others.

Kapton® is a registered trademark of DuPont.

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PDS_SP_K10_12.08

Figure A.15: Thermal isolation pad

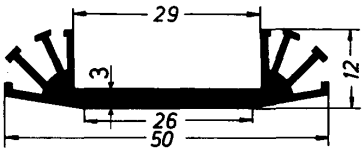
austerlitz electronic

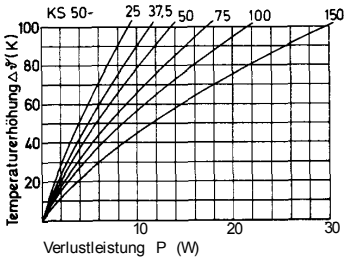
Kühlschienen

Extruded profiles / Profiles extrudes de refroidissement

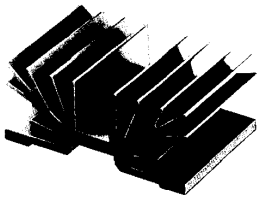
KS 50

Länge (mm): 25/37,5/50/75/100/150/
1000
Gewicht (g/cm): 5,4



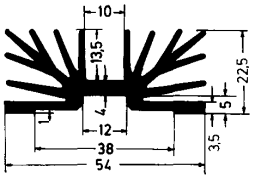


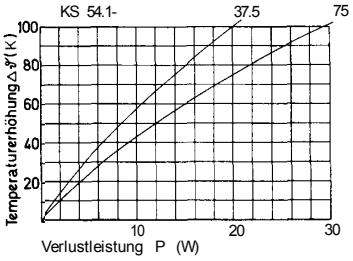
KS 54.1



R_{th} K/W: ca. 3,5 bzw. 1,9
Material: AlMgSi 0,5
Oberfläche: schwarz eloxiert
Gewicht (g): 50 bzw. 100
Gehäuse: TO 220

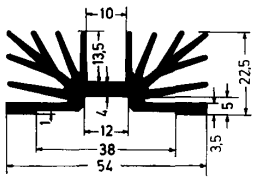
Bestell-Nr. KS 54.1-37,5 E 3 x M3
KS 54.1– 75 E 6 x M3





KS 54.1

Länge (mm): 25/37,5/50/75/100/150/
1000
Gewicht (g/cm): 13



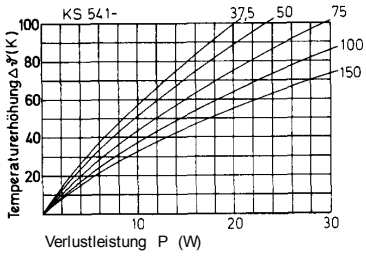


Figure A.16: Small heat sink

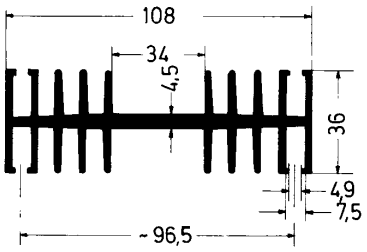
austerlitz electronic

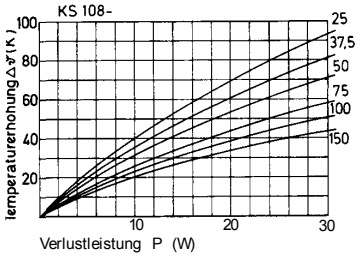
Kühlschienen

Extruded profiles / Profiles extrudes de refroidissement

KS 108

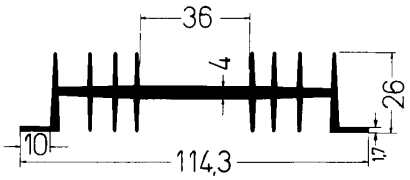
Länge (mm): 50/75/100/150/1000
Gewicht (g/cm): 25,6

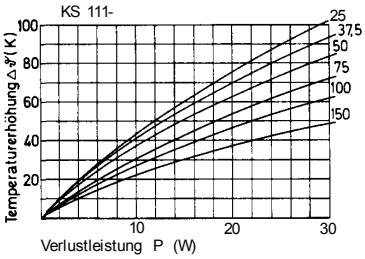




KS 111

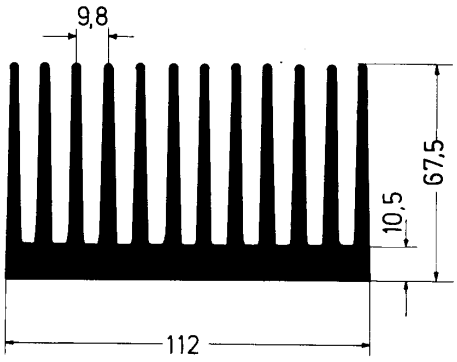
Länge (mm): 50/75/100/150/1000
Gewicht (g/cm): 17,5

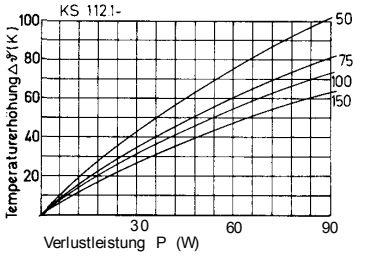




KS 112.1

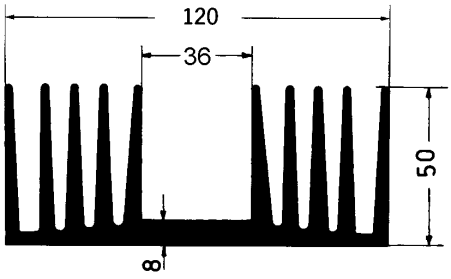
Länge (mm): 50/75/100/150/1000
Gewicht (g/cm): 87





KS 120.9

Länge (mm): 37,5/50/75/100/150/1000
Gewicht (g/cm): 59,2



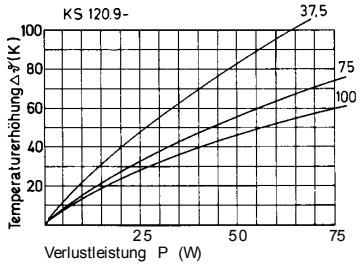


Figure A.17: Big heat sink

Appendix B

Matlab code

```
/*================================================
 * FileName: counter.c
 * Author  : Ibrahim Malik <abraheem1982b@gmail.com>
 * Date    : 2013-06-24
  *================================================*/
#################################################################
                Draw drive circuit waveforms
#################################################################

 clear
 close all
 clc
 name=[''];
 kommando1=['load C1C00004',name,'.dat'];
 kommando2=['load C2C00004',name,'.dat'];
 kommando3=['load C3C00004',name,'.dat'];
 kommando4=['load C4C00004',name,'.dat'];
 kommando5=['load C1C00005',name,'.dat'];
 kommando6=['load C2C00005',name,'.dat'];
 kommando7=['load C3C00005',name,'.dat'];
 kommando8=['load C4C00005',name,'.dat'];
 kommando9=['load C1C00006',name,'.dat'];
 kommando10=['load C2C00006',name,'.dat'];
 kommando11=['load C3C00006',name,'.dat'];
 kommando12=['load C4C00006',name,'.dat'];
 kommando13=['load C1C00007',name,'.dat'];
 kommando14=['load C2C00007',name,'.dat'];
 kommando15=['load C3C00007',name,'.dat'];
 kommando16=['load C4C00007',name,'.dat'];
 kommando17=['load vgs4',name,'.dat'];
 kommando18=['load vgg4',name,'.dat'];
 kommando19=['load ig4',name,'.dat'];
 kommando20=['load vgg5',name,'.dat'];
 kommando21=['load vgs5',name,'.dat'];
 kommando22=['load ig5',name,'.dat'];
 kommando23=['load vgg6',name,'.dat'];
 kommando24=['load vgs6',name,'.dat'];
 kommando25=['load ig6',name,'.dat'];
 kommando26=['load vgg7',name,'.dat'];
 kommando27=['load vgs7',name,'.dat'];
 kommando28=['load ig7',name,'.dat'];


 eval(kommando1)
 eval(kommando2)
 eval(kommando3)
 eval(kommando4)
 eval(kommando5)
 eval(kommando6)
 eval(kommando7)
```

```
eval(kommando8)
eval(kommando9)
eval(kommando10)
eval(kommando11)
eval(kommando12)
eval(kommando13)
eval(kommando14)
eval(kommando15)
eval(kommando16)
eval(kommando17)
eval(kommando18)
eval(kommando19)
eval(kommando20)
eval(kommando21)
eval(kommando22)
eval(kommando23)
eval(kommando24)
eval(kommando25)
eval(kommando26)
eval(kommando27)
eval(kommando28)


subplot (2,2,1)
a1=C1C00004(:,1);
b1=C1C00004(:,2);
plot(a1.*1e9,b1+6,'k','Linewidth',2)
grid
hold on
a2=C2C00004(:,1);
b2=C2C00004(:,2);
plot(a2.*1e9,b2+6,'g','Linewidth',2)
a3=C3C00004(:,1);
b3=C3C00004(:,2);
plot(a3.*1e9,(b3*10/4.7),'m','Linewidth',2)
a4=C4C00004(:,1);
b4=C4C00004(:,2);
plot(a4.*1e9,b4/0.02,'c','Linewidth',2)
a5=vgs4(:,1);
b5=vgs4(:,2);
plot(a5-3,b5,'--g','Linewidth',2)
a6=vgg4(:,1);
b6=vgg4(:,2);
plot(a6-3.6012,b6,'--k','Linewidth',2)
a7=ig4(:,1);
b7=ig4(:,2);
plot(a7+7.9,b7,'--m','Linewidth',2)
xlabel('time(ns)','fontsize',14)
axis([-5  190 -5 15]);
legend('vgg meas.','vgs meas.','I_G differential','IG Rogowksi',...
```

```
...'vgg sim','vgs sim','I_G sim')
legend('vgg meas.','vgs meas.','I_G differential','IG Rogowksi')
title('(RG=4.7\Omega, C=10nf) Turn-On')


subplot (2,2,2)
a1=C1C00005(:,1);
b1=C1C00005(:,2);
plot(a1.*1e9,b1+6,'k','Linewidth',2)
grid
hold on
a2=C2C00005(:,1);
b2=C2C00005(:,2);
plot(a2.*1e9,b2+6,'g','Linewidth',2)
hold on
a3=C3C00005(:,1);
b3=C3C00005(:,2);
plot(a3.*1e9,(b3/4.7)*10,'m','Linewidth',2)
hold on
a4=C4C00005(:,1);
b4=C4C00005(:,2);
plot(a4.*1e9,b4/0.02,'c','Linewidth',2)
a5=vgs5(:,1);
b5=vgs5(:,2);
plot(a5-11.65,b5+12,'--g','Linewidth',2)
a6=vgg5(:,1);
b6=vgg5(:,2);
plot(a6-11.65,b6+12,'--k','Linewidth',2)
a7=ig5(:,1);
b7=ig5(:,2);
plot(a7,b7,'--m','Linewidth',2)
legend('vgg','vgs','I_G differential','IG Rogowksi')
 legend('vgg meas.','vgs meas.','I_G differential','IG Rogowksi',...
...'vgg sim','vgs sim','I_G sim')
legend('vgg meas.','vgs meas.','I_G differential','IG Rogowksi')
xlabel('time(ns)','fontsize',14)
axis([-40 190 -5 15]);
title('(RG=4.7\Omega, C=10nf) Turn-Off')


subplot (2,2,3)
a1=C1C00006(:,1);
b1=C1C00006(:,2);
plot(a1.*1e9,b1+6,'k','Linewidth',2)
hold on
a2=C2C00006(:,1);
b2=C2C00006(:,2);
plot(a2.*1e9,b2+6,'g','Linewidth',2)
a3=C3C00006(:,1);
b3=C3C00006(:,2);
```

```
plot(a3.*1e9,(b3*10/1),'m','Linewidth',2)
a4=C4C00006(:,1);
b4=C4C00006(:,2);
plot(a4.*1e9,b4/0.02,'c','Linewidth',2)
a5=vgs6(:,1);
b5=vgs6(:,2);
plot(a5-4,b5,'--g','Linewidth',2)
a6=vgg6(:,1);
b6=vgg6(:,2);
plot(a6-4,b6,'--k','Linewidth',2)
a7=ig6(:,1);
b7=ig6(:,2);
plot(a7+4,b7,'--m','Linewidth',2)
axis([-20  150 -5 15]);
legend('vgg meas.','vgs meas.','I_G differential','IG Rogowksi',...
...'vgg sim','vgs sim','I_G sim')
legend('vgg meas.','vgs meas.','I_G differential','IG Rogowksi')
xlabel('time(ns)','fontsize',14)
title('(RG=1\Omega, C=10nf) Turn-On')
grid


subplot (2,2,4)
a1=C1C00007(:,1);
b1=C1C00007(:,2);
hold on
a2=C2C00007(:,1);
b2=C2C00007(:,2);
plot(a2.*1e9,b2+6,'g','Linewidth',2)
a3=C3C00007(:,1);
b3=C3C00007(:,2);
plot(a3.*1e9,(b3*10/1),'m','Linewidth',2)
a4=C4C00007(:,1);
b4=C4C00007(:,2);
plot(a4.*1e9,b4/0.02,'c','Linewidth',2)
plot(a1.*1e9,b1+6,'k','Linewidth',2)
a5=vgs7(:,1);
b5=vgs7(:,2);
plot(a5-20,b5+12,'--g','Linewidth',2)
a6=vgg7(:,1);
b6=vgg7(:,2);
plot(a6-18,b6+12,'--k','Linewidth',2)
a7=ig7(:,1);
b7=ig7(:,2);
plot(a7+4,b7,'--m','Linewidth',2)
legend('vgg meas.','vgs meas.','I_G differential','IG Rogowksi',...
...'vgg sim','vgs sim','I_G sim')
legend('vgg meas.','vgs meas.','I_G differential','IG Rogowksi')
xlabel('time(ns)','fontsize',14)
title('(RG=1\Omega, C=10nf) Turn-Off')
```

```
 axis([-50 150 -5 15]);
 grid



#################################################################
             PT100 resistance  versus temperature
#################################################################

 a=3.9080e-3;b=-5.8019e-7;
 alpha=0.003850;
 t=-50:0.1:600;
  r=1000*(1+a.*t+b.*t.^2);
 plot(t,r,'LineWidth',2.5)
 grid
  axis([0  200 900 2000]);
  xlabel('temperature(\circC)','fontsize',14);
  ylabel('Resistance(\Omega)','fontsize',14);
  set(gca,'fontsize',14)

#################################################################
              PT100 resistance  versus bridge voltage
#################################################################

 R=20:5000;
 v1=4.927*((R./(R+1000))-((998/(998+998))));
 plot(R,v1,'LineWidth',2.5)
 grid
 axis([-500 5500  -3 2 ]);
  xlabel('PT1000 resistance(\Omega)','fontsize',14);
 ylabel('V_{output}(volt)','fontsize',14)
 set(gca,'fontsize',14)

#################################################################
                 temperature versus voltage
#################################################################

 a=3.9080e-3;b=-5.8019e-7;
 alpha=0.003850;
 t=-50:0.1:600;
 r=1000*(1+a.*t+b.*t.^2);
 v1=4.927*((r./(r+1005))-((998/(998+998))));
 plot(t,v1)
 grid
 axis([-100 650  -0.5 1.5 ]);
  xlabel('Temperature(C)');
 ylabel('V_{output}(volt)')
```

```
251
252
253 ##############################################################
254             Calibration of PT1000
255 ##############################################################
256
257  TA=[     194.2;    183.1;    180;     177.1;     173.2;    170.1;
    164.6;    158.7;    148.1;     144.0;   136.4;    131.7;      125;
    118.3;   109.9;     102;      94.8;     86.1;   81.1;       75.8;
    64;      58;      52.8;    47.5;       42.1;    37.5;      34.3;
    29.8;      24.0;     21.5;  ];
258  CH0=[3.344194; 3.203159; 3.162729; 3.125034; 3.073923; 3.032883; 2.959971; 2.881062;
259       2.736821; 2.680742; 2.571765; 2.504851; 2.406592; 2.307346; 2.177363; 2.051934;
260       1.936038; 1.789497; 1.704031; 1.614587; 1.404600; 1.288809; 1.185977; 1.086462;
261       0.976636; 0.881125; 0.812607; 0.727368; 0.596313; 0.541821;];
262
263  CH1=[3.342336; 3.200129; 3.159392; 3.123198; 3.071731; 3.031072; 2.959045; 2.880742;
264       2.735735; 2.679451; 2.570498; 2.504280; 2.405698; 2.306960; 2.175264; 2.050818;
265       1.934121; 1.789111; 1.703948; 1.613850; 1.406125; 1.289175; 1.183723; 1.083975;
266       0.973652; 0.878699; 0.812766; 0.712183; 0.583398; 0.517627;];
267
268  CH2=[3.337473; 3.196716; 3.155037; 3.118198; 3.066323; 3.025950; 2.954072; 2.874822;
269       2.729402; 2.675239; 2.565720; 2.498970; 2.400320; 2.302905; 2.171270; 2.048293;
270       1.932781; 1.784390; 1.698967; 1.608894; 1.399150; 1.284060; 1.181694; 1.082830;
271       0.971804; 0.876465; 0.807974; 0.712036; 0.582788; 0.536670;];
272
273  CH3=[3.346555; 3.200815; 3.159304; 3.122710; 3.074609; 3.030188; 2.958860; 2.879626;
274       2.734314; 2.678594; 2.570066; 2.503669; 2.405334; 2.306946; 2.175234; 2.050735;
275       1.935686; 1.789380; 1.704019; 1.614282; 1.405859; 1.289985; 1.190271; 1.086213;
276       0.976431; 0.879285; 0.810449; 0.722510; 0.591895; 0.538354;];
277
278  CH4=[3.344895; 3.199175; 3.158762; 3.121733; 3.069810; 3.029114; 2.956909; 2.878374;
279       2.734038; 2.676077; 2.568308; 2.500881; 2.402302; 2.304663; 2.173171; 2.047578;
280       1.931335; 1.787339; 1.701602; 1.612085; 1.402300; 1.285830; 1.178989; 1.086013;
281        0.976035; 0.881091; 0.814436; 0.723291; 0.593091; 0.548682;];
282
283  CH5=[3.341516; 3.202056; 3.161638; 3.125063; 3.073855; 3.032356; 2.959954; 2.881086;
284       2.736387; 2.680737; 2.571494; 2.505100; 2.406941; 2.307722; 2.177095; 2.052119;
285       1.935742; 1.791228; 1.705183; 1.616064; 1.406296; 1.289172; 1.185969; 1.086025;
286       0.976401; 0.881274; 0.813015; 0.712085; 0.579370; 0.537085;];
287
288  CH6=[3.330281; 3.193079; 3.150171; 3.113428; 3.061567; 3.020715; 2.949360; 2.871060;
289       2.725437; 2.668870; 2.559148; 2.492827; 2.395005; 2.295012; 2.165254; 2.040840;
290        1.923828; 1.779568; 1.693396; 1.603926; 1.396138; 1.279297; 1.172224; 1.077075;
291         0.967004; 0.871724; 0.805334; 0.726562; 0.595776; 0.547412;];
292
293  CH7=[3.336067; 3.193638; 3.154177; 3.117192; 3.066372; 3.025012; 2.953489; 2.873726;
294       2.729553; 2.673293; 2.563777; 2.497175; 2.399114; 2.300947; 2.170850; 2.045710;
295        1.930425; 1.787212; 1.699377; 1.611172; 1.399927; 1.285125; 1.178923; 1.085403;
296        0.974976; 0.880830; 0.812964; 0.729321; 0.599634; 0.546753;];
```

```
297
298 ##################################################################
299                         fitting curve
300 ##################################################################
301  FitCH0=fit(CH0,TA,'poly2');
302  FitCH1=fit(CH1,TA,'poly2');
303  FitCH2=fit(CH2,TA,'poly2');
304  FitCH3=fit(CH3,TA,'poly2');
305  FitCH4=fit(CH4,TA,'poly2');
306  FitCH5=fit(CH5,TA,'poly2');
307  FitCH6=fit(CH6,TA,'poly2');
308  FitCH7=fit(CH7,TA,'poly2');
309 ##################################################################
310              voltage versus temperature
311 ##################################################################
312
313  x=0:0.01:5;
314  y0A=FitCH0(x);
315  y1A=FitCH1(x);
316  y2A=FitCH2(x);
317  y3A=FitCH3(x);
318  y4A=FitCH4(x);
319  y5A=FitCH5(x);
320  y6A=FitCH6(x);
321  y7A=FitCH7(x);
322
323  plot(x,y0A,x,y1A,x,y2A,x,y3A,x,y4A),grid
324  ylabel('temperature␣C')
325  xlabel('raw␣voltages')
326  legend('CH0A','CH1A','CH2A','CH3A','CH4A','CH5A','CH6A','CH7A')
327
328 ##################################################################
329                temperature versus time
330 ##################################################################
331
332  load('testmatning34.lvm')
333
334  kanal0=testmatning34(:,1);
335  kanal1=testmatning34(:,2);
336  kanal2=testmatning34(:,3);
337  kanal3=testmatning34(:,4);
338  kanal4=testmatning34(:,5);
339  kanal5=testmatning34(:,6);
340  kanal6=testmatning34(:,7);
341  kanal7=testmatning34(:,8);
342
343  x1=0:length(kanal0)-1;
344
345  y0A=FitCH0(kanal0);
346  y1A=FitCH1(kanal1);
```

```
y2A=FitCH2(kanal2);
y3A=FitCH3(kanal3);
y4A=FitCH4(kanal4);
y5A=FitCH5(kanal5);
y6A=FitCH6(kanal6);
y7A=FitCH7(kanal7);

yjunc=(0.43932+Riso+Rhs)*Pd+y3A;

load('data1555.csv');
o=data1555(:,1);
 p=data1555(:,2);
q=data1777(:,3);
l=data1777(:,4);


a=3.908e-3;b=-5.8019e-7;
R0=1005*((kanal0./(4.933*5))+0.5)./(0.5-(kanal0./(4.933*5)));
T0=(-a+sqrt(a^2-(4*b*(1-(R0./1000)))))/(2*b);

R1=1005*((kanal1./(4.933*5))+0.5)./(0.5-(kanal1./(4.933*5)));
T1=(-a+sqrt(a^2-(4*b*(1-(R1./1000)))))/(2*b);

R2=1005*((kanal2./(4.933*5))+0.5)./(0.5-(kanal2./(4.933*5)));
T2=(-a+sqrt(a^2-(4*b*(1-(R2./1000)))))/(2*b);

R3=1005*((kanal3./(4.933*5))+0.5)./(0.5-(kanal3./(4.933*5)));
T3=(-a+sqrt(a^2-(4*b*(1-(R3./1000)))))/(2*b);

R4=1005*((kanal4./(4.933*5))+0.5)./(0.5-(kanal4./(4.933*5)));
T4=(-a+sqrt(a^2-(4*b*(1-(R4./1000)))))/(2*b);

plot(x1,y0A,'y',x1,y1A,'m',x1,y2A,'c',x1,y3A,'r',x1,y4A,'g',x1,y5A,'b',...
...x1,y6A,'--r',x1,y7A,'k','LineWidth',2.5)
legend('T_amb','T_case','T_gate_{bottom}','T_source_{top}','T_drain_{top}',...
...'T_gate_{top}','T_source_{bottom}','T_drain_{bottom}')
xlabel('time_(s)','fontsize',14)
ylabel('temperature_^\oC','fontsize',14)
axis([-100  2000 20 400]);
grid on
```