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# Study of Modulation Schemes for the Dual-Active-Bridge Converter in a Grid-Connected Photovoltaic Park

Master's Thesis in M. Sc. Sustainable Electrical Power Supply at the University of Stuttgart

VERENA STEUB

Department of Electrical Engineering
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY, Gothenburg, Sweden 2018

Master's thesis 2018

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VERENA STEUB
(Enrolment Number: 2573849)

Institut für Leistungselektronik und Elektrische Antriebe ILEA

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Electrical Drives (ILEA)
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VERENA STEUB



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Supervisors:
Dr. Amin Bahmani, Department of Electrical Engineering
M. Sc. Johannes Ruthardt, Institute of Power Electronics and Electrical Drives

Examiners:
Prof. Torbjörn Thiringer, Department of Electrical Engineering
Prof. Dr.-Ing. Jörg Roth-Stielow, Institute of Power Electronics and Electrical Drives

Master's Thesis 2018

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg, Sweden
Telephone +46 31 772 1000

Institute of Power Electronics and Electrical Drives (ILEA)
University of Stuttgart
DE-70569 Stuttgart, Germany
Telephone +49 711 685 67401

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# Erklärung

Ich versichere, dass ich die vorliegende Arbeit, abgesehen von den Anregungen, die mir von Seiten meiner Betreuer, Herrn Dr. Amin Bahmani und Herrn M. Sc. Johannes Ruthardt sowie von meinen Prüfern, Herrn Prof. Torbjörn Thiringer und Herrn Prof. Dr.-Ing. Jörg Roth-Stielow gegeben worden sind, selbstständig durchgeführt und verfasst habe. Es wurden keine anderen als die angegebenen Quellen und Hilfsmittel benutzt. Alle Ausführungen, die wörtlich oder sinngemäß aus anderen Werken übernommen wurden, sind als solche gekennzeichnet.

Göteborg, den 28. Juli 2018

Verena Steub

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# Abstract

This works aims at comparing two modulation schemes for the Dual-Active-Bridge DC-DC converter topology. On the basis of a specific case of application, the most suitable method shall be identified.

The model of a Dual-Active-Bridge converter is built and simulated in PLECS®. It is embedded in the configuration of a photovoltaic park with an output power of $P = 0.97$ MW, an input voltage level of $V_i = 1.3$ kV and an output voltage level of $V_o = 16$ kV $\pm 5\,\%$. The considered load levels are assumed to be full load, 80 %, 50 %, 30 % and 10 % of the full load, respectively. The feed-in of solar power into the transmission grid is facilitated by the Dual-Active-Bridge. The power flow through the converter is controlled either by the so called single-phase-shift modulation or the trapezoidal modulation scheme. Both techniques are examined and compared concerning the root mean square value of their inductor current, possible load range, switching losses and resulting efficiency.

The root mean square value of the inductor current is found to be lower with single-phase-shift modulation than with trapezoidal modulation for all voltage and load levels. Additionally, the single-phase-shift modulation can cover a wider load range than the trapezoidal modulation scheme. However, the trapezoidal modulation scheme features better soft-switching capabilities and therefore generally lower switching losses than the single-phase-shift modulation. Altogether, it is observed that depending on the used switch and load level, a different modulation scheme is favorable. Using a SiC MOSFET switch, the single-phase-shift modulation shows a better efficiency than the trapezoidal modulation for loads down to 50 % of the full load. For lower loads, the trapezoidal modulation provides slightly better results. In the case of an IGBT switch, the trapezoidal modulation outplays the single-phase-modulation over the entire load range.


Keywords: Dual-Active-Bridge, Modulation Schemes, Photovoltaic Park, Single-Phase-Shift Modulation, Trapezoidal Modulation.

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# Kurzfassung

In der vorliegenden Arbeit werden zwei Modulationsarten für den Dual-Active-Bridge-Gleichspannungswandler verglichen. Anhand eines spezifischen Anwendungsfalls soll das für diese Topologie am besten geeignete Verfahren bestimmt werden.

Ein Modell eines Dual-Active-Bridge-Wandlers wird in PLECS® aufgebaut und simuliert. Dieses wird am Beispiel eines Photovoltaik-Parks mit einer Ausgangsleistung von $P = 0{,}97$ MW, einer Eingangsspannung von $V_i = 1{,}3$ kV und einer Ausgangsspannung von $V_o = 16$ kV $\pm 5\,\%$ untersucht. Es werden Lastfälle von Volllast über 80 %, 50 %, 30 % und 10 % der maximalen Last betrachtet. Die Einspeisung in das Übertragungsnetz wird durch die Dual-Active-Bridge ermöglicht. Der Leistungsfluss durch den Gleichspannungswandler wird entweder durch die sogenannte Single-Phase-Shift-Modulation oder die trapezoide Modulation geregelt. Beide Techniken werden bezüglich des Effektivwerts ihres Spulenstroms, des möglichen abgedeckten Lastbereichs, der Schaltverluste und des resultierenden Wirkungsgrades untersucht und verglichen.

Der Effektivwert des Spulenstroms stellt sich bei der Single-Phase-Shift-Modulation für alle Spannungs- und Lastebenen als niedriger heraus als bei der trapezoiden Modulation. Darüber hinaus kann mit der Single-Phase-Shift-Modulation ein breiterer Lastbereich abgedeckt werden als mit der trapezoiden Modulation. Letztere verfügt jedoch über bessere Eigenschaften bezüglich weicher Einschaltvorgänge und weist daher allgemein geringere Schaltverluste auf. Insgesamt zeigt sich, dass je nach verwendeter Schalterart und Lastebene eine jeweils andere Modulationsart vorzuziehen ist. Unter Verwendung eines SiC MOSFET-Schalters bietet die Single-Phase-Shift-Modulation bessere Wirkungsgrade für Lasten von Volllast bis hinunter zu 50 % der Last. Für Lasten kleiner als 50 % liefert die trapezoide Modulation bessere Ergebnisse. Im Falle des IGBT-Schalters übertrifft die trapezoide Modulation die Single-Phase-Shift-Modulation über den gesamten Lastbereich.

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Verena Steub
Gothenburg, Sweden, July 2018

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# List of Abbreviations and Symbols

## Abbreviations

| | |
|---|---|
| **AC** | Alternating Current |
| **DAB** | Dual-Active-Bridge |
| **DC** | Direct Current |
| **HV** | High Voltage |
| **IGBT** | Insulated-Gate Bipolar Transistor |
| **LV** | Low Voltage |
| **MF** | Medium Frequency |
| **MOSFET** | Metal-Oxide-Semiconductor Field-Effect Transistor |
| **MPP** | Maximum Power Point |
| **MPPT** | Maximum Power Point Tracking |
| **MV** | Medium Voltage |
| **PV** | Photovoltaic |
| **RMS** | Root Mean Square |
| **SiC** | Silicon Carbide |
| **SPS** | Single-Phase-Shift |
| **STC** | Standard Test Conditions |

## Symbols

| | |
|---|---|
| $\boldsymbol{\epsilon}$ | Auxiliary Parameter for Phase-Shifting in Trapezoidal Modulation |
| $\boldsymbol{\Omega_1}$ | Zero-Voltage Length of Primary Side Transformer Voltage |
| $\boldsymbol{\Omega_2}$ | Zero-Voltage Length of Secondary Side Transformer Voltage |
| $\boldsymbol{\varphi}$ | Phase-Shift Angle |
| $\boldsymbol{D_1}$ | Duty Cycle of Primary Side Transformer Voltage in Trapezoidal and Triangular Modulation |
| $\boldsymbol{D_2}$ | Duty Cycle of Secondary Side Transformer Voltage in Trapezoidal and Triangular Modulation |
| $\boldsymbol{D}$ | Duty Cycle of Primary and Secondary Side Transformer Voltage in Single-Phase-Shift Modulation |

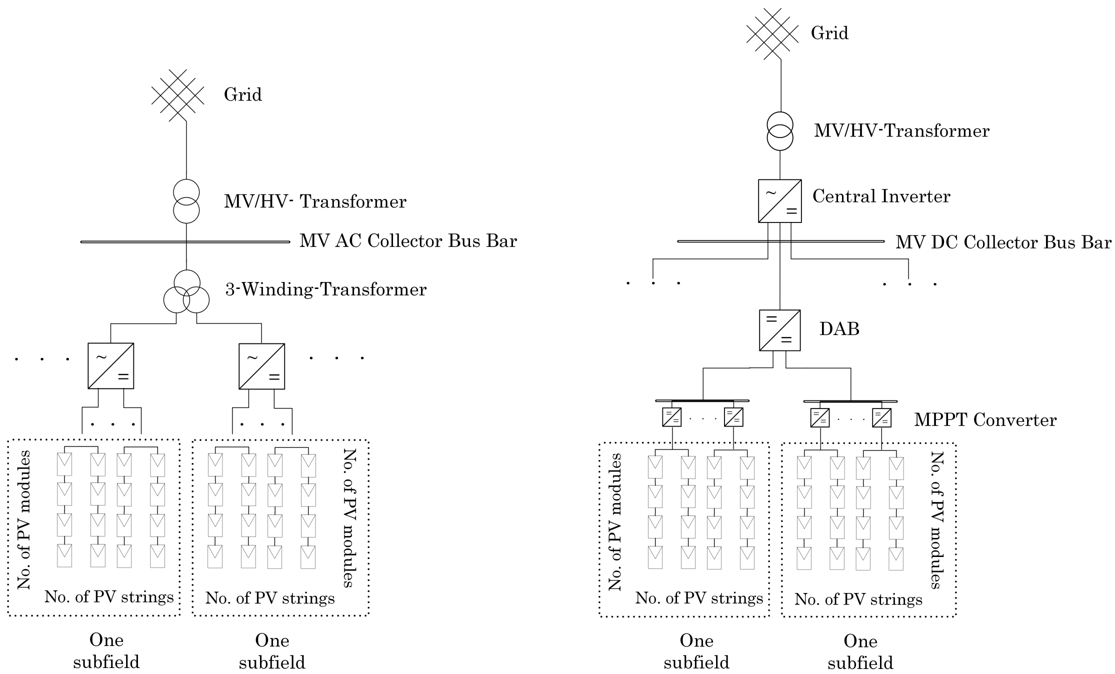
| | |
|---|---|
| $\boldsymbol{d}$ | DC Transformation Ratio |
| $\boldsymbol{f_s}$ | Switching Frequency |
| $\boldsymbol{L}$ | Leakage Inductance |
| $\boldsymbol{n}$ | Transformer Turns Ratio |
| $\boldsymbol{T_s}$ | Switching Period |
| $\boldsymbol{T_{hs}}$ | Half a Switching Period |
| $\boldsymbol{V_i}$ | Input Voltage |
| $\boldsymbol{V_o}$ | Output Voltage |
| $\boldsymbol{v_{T1}}$ | Primary Side Transformer Voltage |
| $\boldsymbol{v_{T2}}$ | Secondary Side Transformer Voltage |

# 1

# Introduction

## 1.1 Problem Background and Previous Work

Today's energy system is shifting more and more towards renewable energies. In this transformation process, it is necessary to overthink common and established ways of feeding power into the grid in order to find the best possible solutions for high efficiency and low cost. For the grid connection of large photovoltaic parks different options have been examined in [37]. Two of them are presented in Figure 1.1.




**(a)** MV AC Collector Bus Bar **(b)** MV DC Collector Bus Bar

**Figure 1.1:** Two options for the PV park configuration according to [37]

In Figure 1.1(a), the generated solar current is converted from DC to AC right at the output of the solar field by means of an inverter. This inverter simultaneously acts as MMP tracker for the PV subfield [37]. After this stage, a transformer transmits the voltage from the low voltage level to the medium voltage level. The entire power generated by the PV park will be collected at the following AC bus bar and can either be used at medium voltage level or, after another transformation stage, be fed into the main grid at high voltage level.

In Figure 1.1(b), the generated solar voltage is boosted up by means of a DC-DC converter ensuring a constant output voltage of all solar subfields. At the same time, this DC-DC converter functions as MPP tracker. The resulting voltage is handed over to another DC-DC converter boosting up the voltage from low voltage level to medium voltage level. Only after this second transmission stage, the voltage will be converted from DC to AC by the help of a central inverter. This means that the power generated by the PV park will be collected at a DC bus bar and be inverted collectively. After the inversion stage and a transformation stage, it is fed into the main grid at high voltage level.

According to [37], the use of the second configuration will lead to an increased energy yield per year as well as an improved efficiency and economic performance. Comparing both configurations, it is apparent that the DC configuration is equipped with an additional DC-DC converter to execute the voltage boosting between low voltage and medium voltage level. Thereby, this converter is replacing the respective transformer in the AC configuration and functioning as a key component in the alternative DC configuration. In order to realize this concept, first a topology for the DC-DC conversion stage has to be chosen. A comparison of three topologies for this purpose has been done in [5]. It resulted in the choice of the two-level Dual-Active-Bridge (DAB) converter which will consequently be employed in this work. In order to control the flow of power through this converter, various modulation techniques are available and can be applied. In the following, two of these shall be examined and compared with respect to overall efficiency, switching losses, possible load range and root mean square (RMS) value of the inductor current.

## 1.2 Dual-Active-Bridge Topology, its Modulation and Application

The two-level Dual-Active-Bridge presented in [15] consists of two full bridges that are connected via a high- or medium-frequency transformer as can be seen in Figure 1.2. The transformer provides galvanic isolation and its leakage inductance serves as power transfer element [15, 27].

By giving respective gate signals to the switches, a square voltage is generated on the primary and secondary side of the transformer, named as $v_{T1}$ and $v_{T2}$ in Figure 1.2.

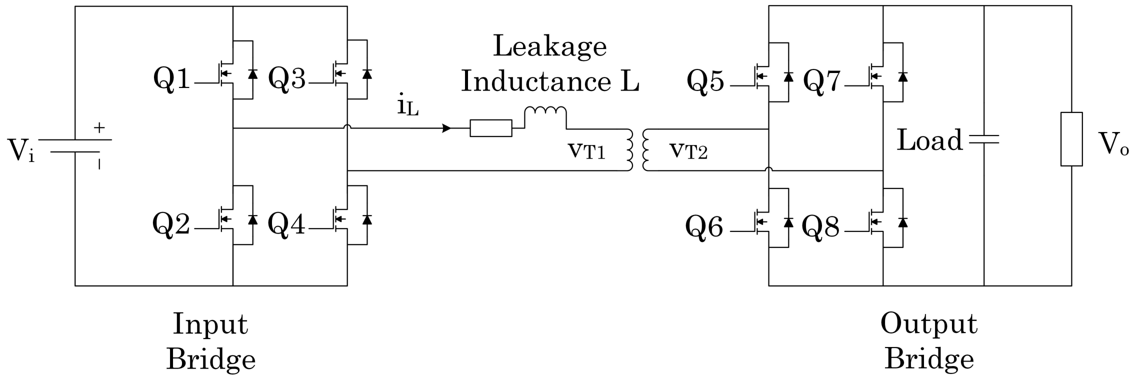



**Figure 1.2:** Dual-Active-Bridge topology

Adequate switching actions control the power flow between input and output. As mentioned before and also according to [27], the DAB converter topology shows advantageous features which make its use preferable over other DC-DC converter topologies. Among these features are the value of the possible efficiency of the converter that can be achieved as well as its power density. Additionally, it is stated in [15] that all switches of the DAB exhibit zero- or low-switching loss capabilities. This improves efficiency in comparison with hard-switched topologies. Moreover, it allows for higher switching frequencies which would have led to unreasonably high switching losses if soft-switching was not available. High switching frequencies in turn lead to a smaller area footprint of the transformer, reducing weight and making transport easier. Aside from that, it is notable that the DAB is a bidirectional topology and is therefore often utilized in applications of energy storage, e. g. for linking batteries in automotive applications. However, this advantage will not be made use of in this work. [15]

In literature, numerous different modulations schemes for the DAB are presented. Among these are for example the single-phase-shift (SPS) control, dual-phase-shift control [26, 43], extended-phase-shift control and triple-phase-shift control [44] as well as trapezoidal [35, 27], triangular [35, 27] and optimized modulation [27] method. Other modulation schemes making use of a change in switching frequency in order to control the power flow are not considered in this work. After extensive research, the single-phase-shift modulation and the trapezoidal modulation scheme are selected to be applied to the DAB and to be modelled, simulated and tested in PLECS®.

Due to the available resources in the scope of this work, the theory of the triangular modulation scheme which complements the trapezoidal modulation scheme (refer Section 3.4) will be presented shortly, but not implemented in the simulation. In [27] and related works like [29] and [30], the single-phase-shift, trapezoidal, triangular and optimized modulation are employed for low voltage automotive applications. In the present work, the single-phase-shift and trapezoidal modulation will be applied to a high voltage photovoltaic application, following the use case of [37].

## 1.3 Methodology

At first, the boundary conditions for the specified application of a grid-connected photovoltaic park are defined and presented in Chapter 2. In Chapter 3, the theoretical details of the chosen modulation schemes are compiled and differences between them are worked out. A model of a Dual-Active-Bridge is built in PLECS® and the chosen modulation schemes are applied to the model and simulated. Details of simulation parameters and modeling are given in Chapter 4. A set of parameters is determined and presented in Chapter 5, that shall be used in order to compare and evaluate the suitability of the respective modulation scheme in the determined application. Conclusions with respect to which modulation scheme is most suitable for the decided case are drawn and presented in Chapter 6.

## 1.4 Ethical and Sustainability Aspects

On one hand, semiconductor appliances generally belong to a conflicting area of technology, as the used materials feature several difficulties concerning availability and acquirement. On the other hand, the development and improvement of converters using semiconductor switches facilitate the grid integration of renewable energies and can therefore promote their advancement. Furthermore, the use of modern power electronic devices can improve the efficiency of electrical plants. The advantages and disadvantages of these technologies therefore have to be weighed up and decided upon in every specific situation. For this project, only software simulations will be applied. Hence, questions of material choice and usage are not yet urgently relevant at this stage and will not be discussed in the scope of this work. When it comes to the experimental set up and practical application of the considered technology, a detailed assessment should be carried out.

# 2

# Case Set Up

## 2.1 Case of Application

In order to test the behaviour of the chosen modulation schemes, the model of the Dual-Active-Bridge along with the respective modulations is embedded in a test scenario where different load conditions apply. As mentioned earlier, a photovoltaic park is chosen as case of application, building up on the accomplished work in [5]. The location of the considered photovoltaic park is Tarifa, Cádiz in Spain, at a latitude of 36.092390° and a longitude of -5.770569°. This is chosen in line with [37]. The selected test date is March 20, 2016. The insolation data for this site and date is available from [2]. Figure 2.1 shows the course of the global irradiance in $\left[\frac{W}{m^2}\right]$.

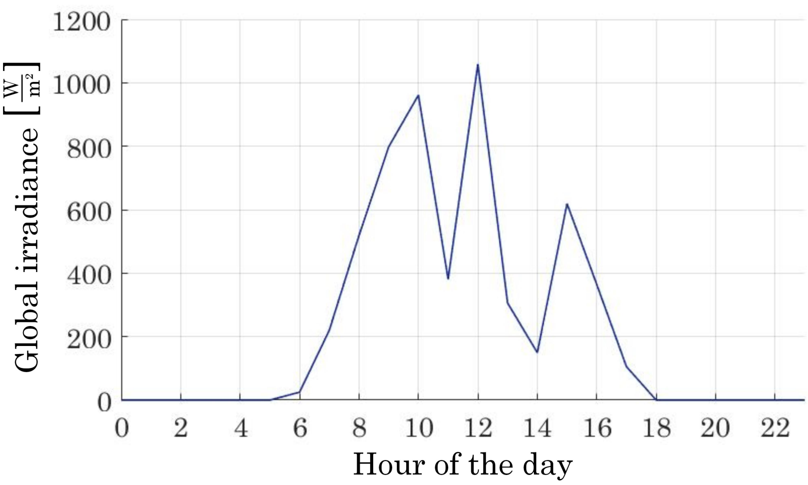



**Figure 2.1:** Global irradiance in Tarifa on March 20, 2016

The layout of the park follows the one presented in [37] and is shown in Figure 2.2. The park is divided into six subfields, each built up of 150 strings and 24 photovoltaic panels in each string. With a nominal power of 260 W per panel, the resulting nominal power of the park is 5.6 MW. As can be seen in Figure 2.2, the MPPT is realized by boost converters, bringing up the voltage to 1.3 kV. The boost converters will not be further contemplated within the scope of this work and their output voltage of 1.3 kV is assumed to be constant. The input of one subfield is then fed into the DC-DC conversion stage on medium voltage level, the Dual-Active-Bridge, stepping up the voltage from 1.3 kV to 16 kV. The output voltage is assumed to incorporate a voltage fluctuation of ± 5 % so that it can take the values of 15.2 kV, 16 kV and 16.8 kV.

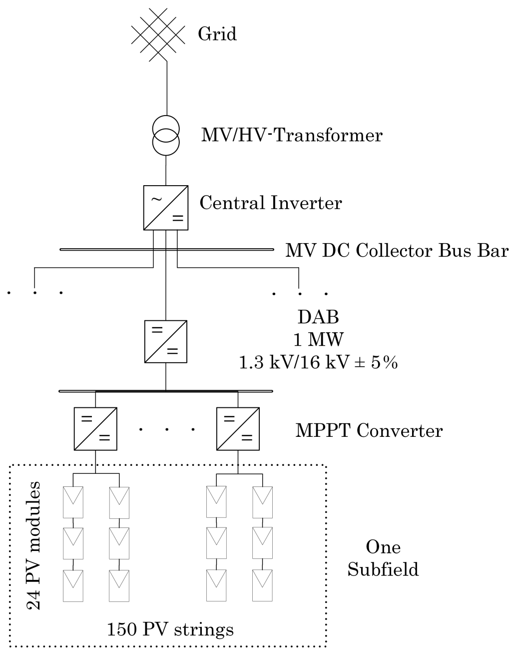



**Figure 2.2:** Adapted configuration of the PV park based on [37]

The power fed into the medium voltage DC-DC conversion stage is calculated as follows:

$$P_{DAB} = (B_i + D_i)\ N_{panel}\ A_{PV}\ \eta_{PV}\ \eta_{MPPT}\ \eta_{system} \tag{2.1}$$

where $B_i$ is the in-plane beam irradiance in $\left[\frac{W}{m^2}\right]$, $D_i$ is the in-plane diffuse irradiance in $\left[\frac{W}{m^2}\right]$, $N_{panel}$ is the number of panels, $A_{PV}$ is the surface area of one PV panel in $[m^2]$, $\eta_{PV}$ is the efficiency of the chosen panels, $\eta_{MPPT}$ is the efficiency of the MPP tracker and $\eta_{system}$ is the efficiency of the whole system, representing e. g. losses in cables. This is a simplified approach as the efficiency of the PV panels is given for standard test conditions which in reality will not always be satisfied. However, it is sufficient for the designated application which is merely to feed an exemplary varying load into the medium voltage level DC-DC stage.

The panels that are assumed to be used for this photovoltaic park are of type Q.PRO BFR-G4.1 260-270 from Q-Cells (refer datasheet in Appendix E). The 260 W module is chosen which has an efficiency of 15.6 %. The dimensions of the module are 1670 mm x 1000 mm. With the given insolation and total number of panels, this leads to a maximum input power per Dual-Active-Bridge of 0.97 MW, corresponding to the output power of one PV subfield at 12 PM (refer Figure F.1 in Appendix F).

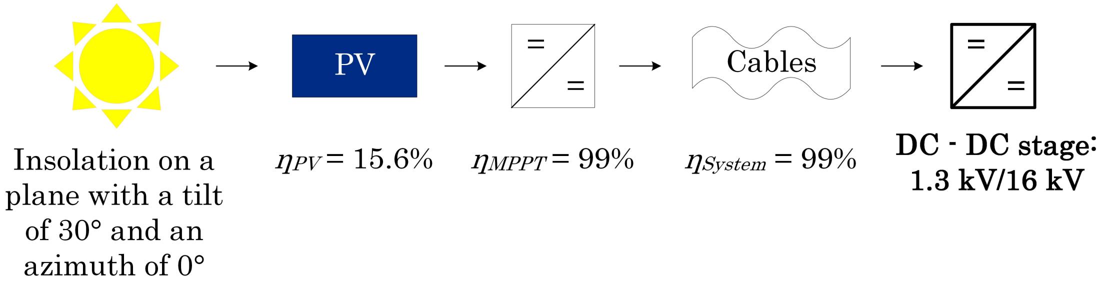



**Figure 2.3:** Assumed losses in the system

The resulting power that will be fed into one of the six DABs in the course of the chosen exemplary day is depicted in Figure 2.4.

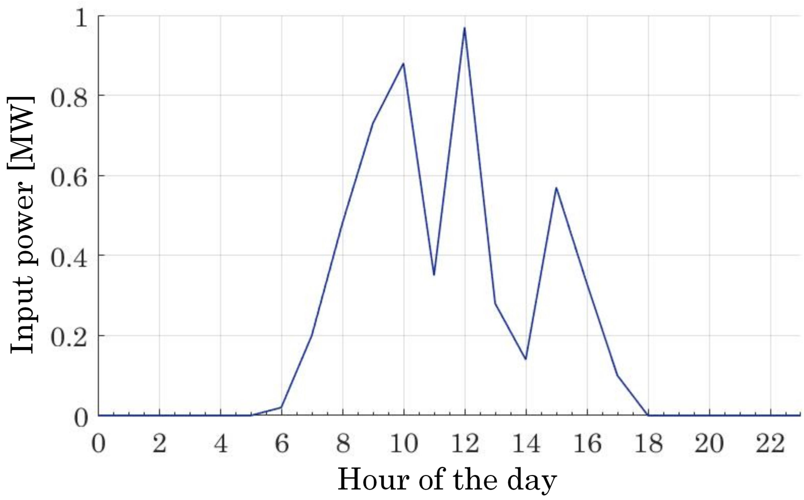



**Figure 2.4:** Power fed into one DAB in the course of March 20, 2016

## 2.2 Choice of Switches

Due to the usage of a medium to high switching frequency in the converter, it is beneficial to opt for a switch type featuring low switching losses. Comparing IGBTs and MOSFETs with respect to switching performance, MOSFETs clearly show better qualities [33]. The switches that are used for the Dual-Active-Bridge are therefore

SiC MOSFETs of type C2M0045170D by Cree. These MOSFETs feature a blocking voltage $V_{DSmax}$ of 1700 V, an on-resistance $R_{DS(on)}$ of 45 mΩ and a continuos drain current $I_D$ of 72 A at 25 °C. Moreover, the intrinsic body diode of a MOSFET can be utilized as anti-parallel diode so that an external diode is not necessary.

Every switching block Q1 to Q8 has to be able to withstand the full input voltage of 1.3 kV on the input side and 16 kV on the output side and the current resulting from transmission of maximum power (refer Figure 1.2). This leads to a necessary parallel and series connection of a certain number of MOSFETs in each switching block. It is assumed that an allowed current of 70 % of the maximum current and a safety margin of 55 % of the maximum blocking voltage for the allowed voltage are safe choices. This results in a connection of two MOSFETs in series and 15 MOSFETs in parallel in each switching block Q1 to Q4 on the low voltage side and 15 MOSFETs in series and two MOSFETs in parallel in each switching block Q5 to Q8 on the high voltage side. The respective calculations are presented in Figure F.2 in Appendix F.

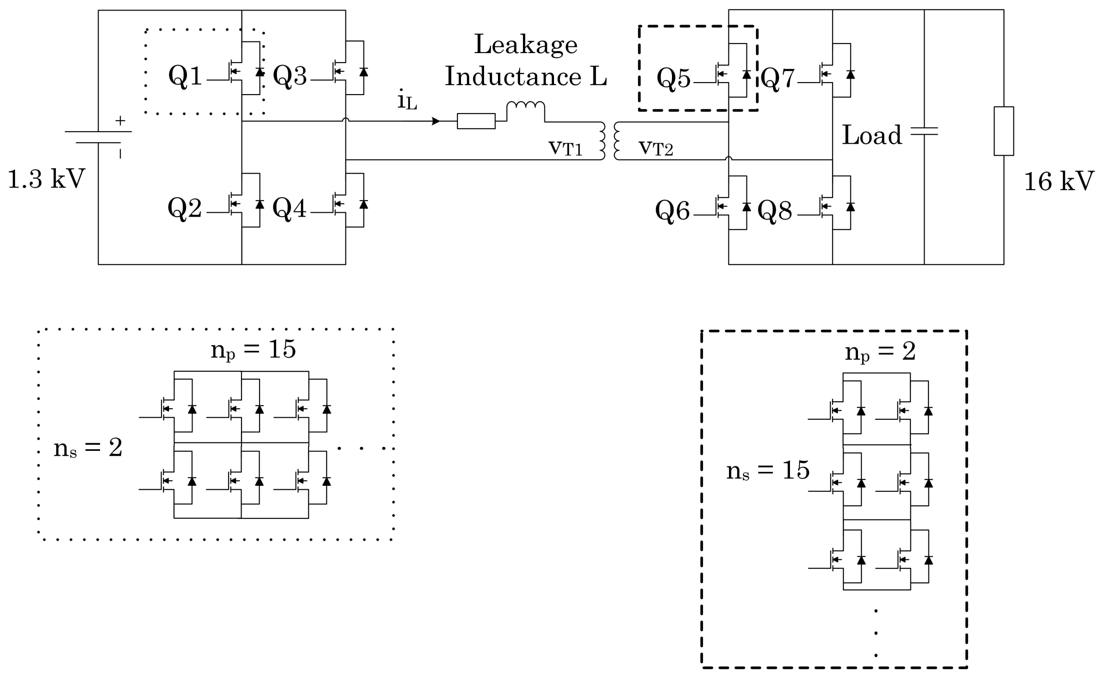
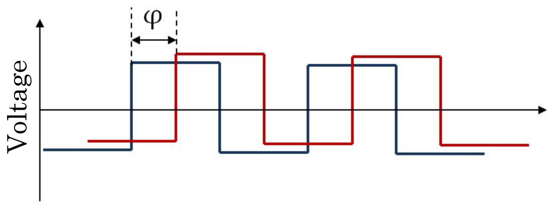



**Figure 2.5:** Series and parallel connection of MOSFETs and anti-parallel diodes in one switching block

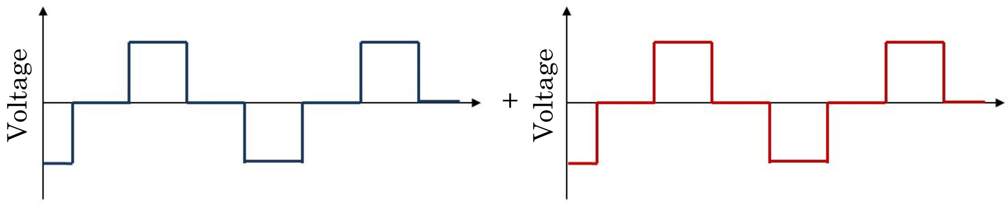
# 3

# Modulation Schemes

Generally, three parameters can be controlled in order to affect the power flow between the primary and secondary side of a Dual-Active-Bridge converter: The phase-shift between the primary and secondary square voltages, the respective duty cycle of the square voltages and the switching frequency. The modulation schemes that are considered in this work take advantage of a change in phase-shift as shown in Figure 3.1(a) and/or duty cycle to control the power flow as shown in Figure 3.1(b). Also, frequency switching methods are not considered.




**(a)** Change of the phase-shift between the two transformer voltages




**(b)** Change of the duty ratio of the two transformer voltages

**Figure 3.1:** Considered variables for modulation

Two modulation schemes will be contemplated: The single-phase-shift modulation scheme, in literature also called as rectangular modulation [35], and the trapezoidal modulation scheme. The latter has its name due to the trapezoidal shape the inductor current takes when applying it.

The single-phase-shift modulation solely uses a phase-shift between the two transformer voltages to control the power flow while the trapezoidal modulation uses a phase-shift and additionally changes the duty ratio of the transformer voltages introducing a zero-voltage period. The zero-voltage period is attained by introducing a phase-shift between the two legs of each full bridge. Both modulation schemes have been presented in [27] and [35]. These are therefore the main sources from which the following theory and equations originate and on which grounds the modulation schemes have been implemented in PLECS®.

## 3.1 Single-Phase-Shift Modulation

The SPS control is the standard modulation scheme for the Dual-Active-Bridge. The square voltages in a circuit that is modulated with this scheme will always have duty cycles of 50 % of the switching period while the frequency stays constant. Two square voltages $v_{T1}$ and $v_{T2}$ are generated on the primary and secondary side of the transformer by giving respective switching signals to the switches Q1 to Q8. A phase-shift $\varphi$ is introduced between the switching signals for the primary side and the switching signals for the secondary side, leading to the same phase-shift $\varphi$ between the two voltages $v_{T1}$ and $v_{T2}$. This is shown in Figures 3.2 and 3.3, with $v_{T2}$ referred to the primary side. A voltage difference is induced and a current flows from the primary to the secondary side.

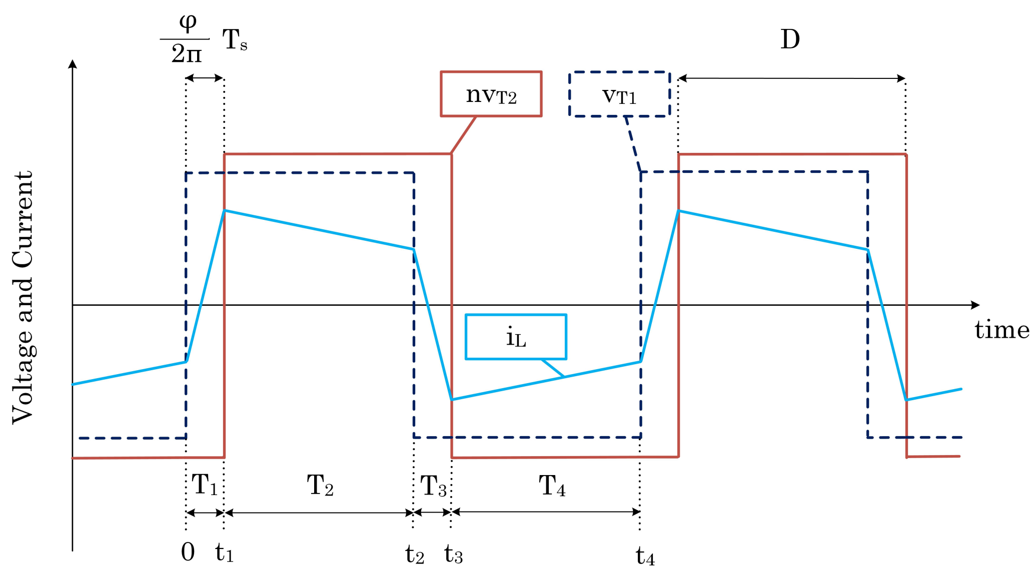



**Figure 3.2:** Primary and referred secondary transformer voltage and inductor current for the single-phase-shift modulation

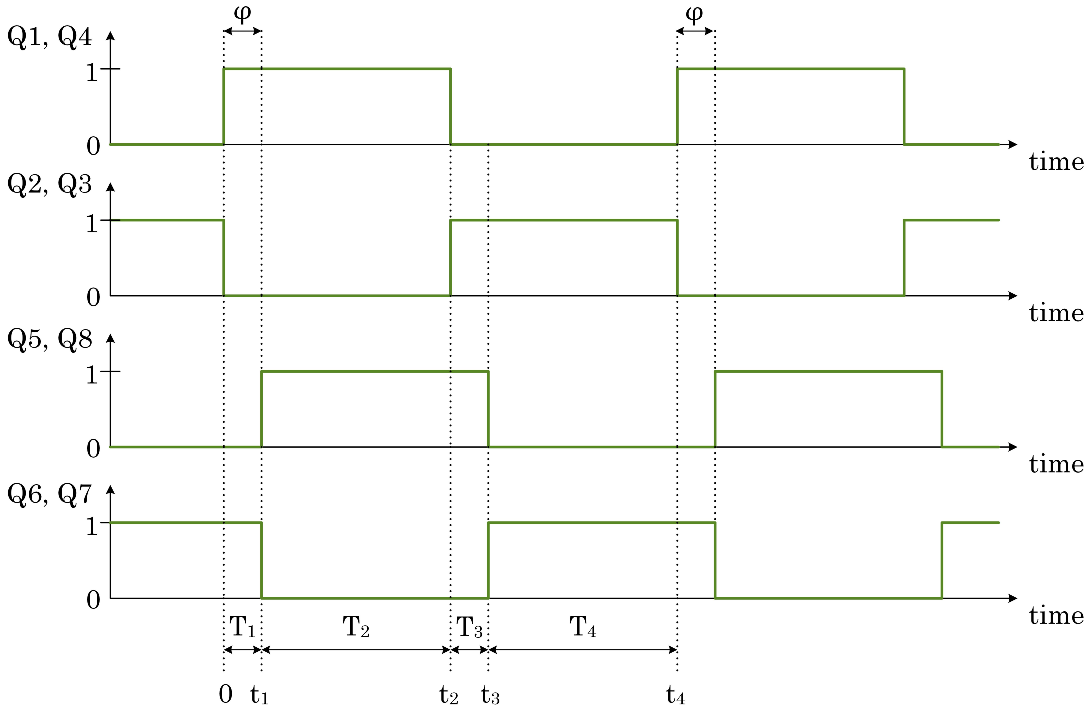



**Figure 3.3:** Switching signals for the gates Q1 to Q8

### 3.1.1 Transmission Power and Phase-Shift Angle $\varphi$

Originating from [16] and [27], the transmitted power in the SPS control is expressed as

$$P = \frac{nV_oV_i}{2\pi f_s L}\,\varphi\,(1 - \frac{\varphi}{\pi}) \tag{3.1}$$

The required angle for the transmission of a desired amount of power then reads as

$$\varphi_{1,2} = \frac{\pi \pm \sqrt{\pi^2 - \frac{8\pi^2 f_s L P}{nV_oV_i}}}{2} \tag{3.2}$$

Considering only the results for $\varphi_2$, this results in possible values of $\varphi = [0, \frac{\pi}{2}]$. The term under the square root must not become smaller than zero as imaginary values for $\varphi_{1,2}$ are not valid:

$$L \overset{!}{\leq} \frac{nV_oV_i}{8 f_s P} \tag{3.3}$$

With this maximum value for the leakage inductance, the maximum power would be transferred at an angle of $\varphi = \frac{\pi}{2}$. However, this is the maximum possible angle and it is not favorable for the minimization of reactive power in the system. A smaller phase-shift angle will therefore be chosen later in this work (refer Section 4.1.1).

### 3.1.2 Voltages and Currents

During the different periods of one switching cycle, different voltages and currents apply. These are explained in the following. The labels of the time intervals are referring to Figures 3.2 and 3.3.

1. Time interval $\mathrm{T_1}$ ($0 < \mathrm{t} < \mathrm{t_1}$)

   - Q1 and Q4 are switched ON
   - Q2 and Q3 are switched OFF
   - Q5 and Q8 are OFF
   - Q6 and Q7 are ON

   In the first time interval $\mathrm{T_1}$, the voltage across the inductor is equal to $(V_i + nV_o)$ and therefore positive. This causes the inductor current $i_L$ to rise. While $\mathrm{i_L} < 0$, the anti-parallel diodes conduct the current on the primary side and allow for soft turn-on. At the zero-crossing point, the current is handed over to the switches Q1 and Q4. The flow of the inductor current in this time interval is given by

   $$i_L(t) \;=\; i_L(0) + \frac{1}{L}\,(V_i + nV_o)\,\Delta t \tag{3.4}$$

2. Time interval $\mathrm{T_2}$ ($\mathrm{t_1} < \mathrm{t} < \mathrm{t_2}$)

   - Q1 and Q4 are ON
   - Q2 and Q3 are OFF
   - Q5 and Q8 are switched ON
   - Q6 and Q7 are switched OFF

   In the second time interval $\mathrm{T_2}$, the voltage across the inductor is equal to $(V_i - nV_o)$ and is negative if $V_i < nV_o$. This relation holds in the case of nominal output voltage $V_o$ = 16 kV and $V_o$ = 16 kV + 5 % and causes the inductor current to fall. In the case of $V_o$ = 16 kV - 5 %, $V_i$ will be larger than

$nV_o$ and the current slope during this time interval is reversed (refer simulation results in Section 5.2). The current flow in this time interval is given by

$$i_L(t) \;=\; i_L(t_1) + \frac{1}{L}\,(V_i - nV_o)\,\Delta t \tag{3.5}$$

3. Time interval $T_3$ ($t_2 < t < t_3$)

   - Q1 and Q4 are switched OFF
   - Q2 and Q3 are switched ON
   - Q5 and Q8 are ON
   - Q6 and Q7 are OFF

   The voltage across the inductor is given by $(-V_i - nV_o)$. It is therefore always negative and causes the inductor current to decrease further and at a steeper slope than during the previous time interval. The current flow in this time interval is given by

$$i_L(t) \;=\; i_L(t_2) + \frac{1}{L}\,(-V_i - nV_o)\,\Delta t \tag{3.6}$$

4. Time interval $T_4$ ($t_3 < t < t_4$)

   - Q1 and Q4 are OFF
   - Q2 and Q3 are ON
   - Q5 and Q8 are switched OFF
   - Q6 and Q7 are switched ON

   During the last time interval $T_4$, the voltage across the inductor is equal to $(-V_i+nV_o)$. Similar to time interval $T_2$, the sign of this voltage depends on the relation between $V_i$ and $V_o$. In the case of nominal output voltage $V_o = 16$ kV and $V_o = 16$ kV + 5 %, a positive voltage is applied across the inductor causing the inductor current to rise again. In the case of $V_o = 16$ kV - 5 %, the slope will consequently be negative (refer simulation results in Section 5.2). The currrent flow in this time interval can be described as

$$i_L(t) \;=\; i_L(t_3) + \frac{1}{L}\,(-V_i + nV_o)\,\Delta t \tag{3.7}$$

In general, it is notable that the current shows a reversed symmetrical behaviour.

### 3.1.3 Switching Behaviour

Power electronic circuits can be divided into soft-switched and hard-switched topologies. A switching action is named as soft if either the current through the switch or the voltage across the switch is zero in the moment of switching. Otherwise, it is called as hard-switched. By ensuring soft switching actions, switching loss are avoided.

Figure 3.4 shows the example of a switch on the primary side of the Dual-Active-Bridge. It can be seen that the current through the MOSFET is negative prior to turn-on. That means that in the turn-on moment, the current will also flow through the diode and facilitates soft-switching for the MOSFET, i e., no switching losses occur. Furthermore, it is visible from the graph that the MOSFET current is positive in the moment of turn-off. Hence, it will solely flow through the switch and switching losses occur in the turn-off moment. In the single-phase-shift modulation, all eight switches of the DAB show the same behaviour as the exemplary switch in Figure 3.4. This could be observed during the simulations and means that in the turn-on moment eight switches are soft-switched and in the turn-off moment zero switches are soft-switched.

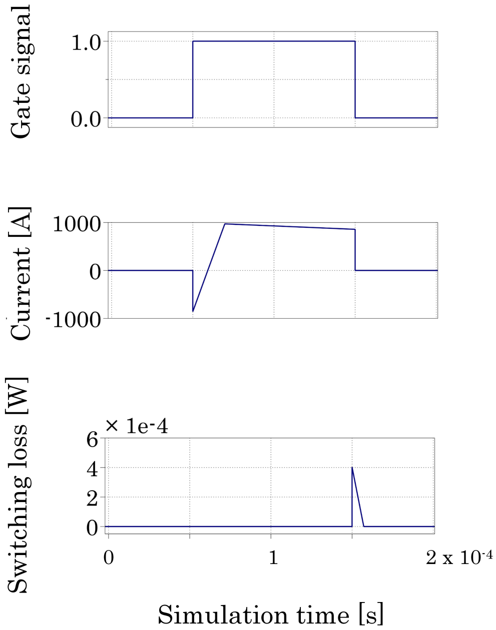



**Figure 3.4:** Gate signal to the switch, current through the switch and switching losses for the example of a MOSFET switch on the primary side of the DAB

## 3.2 Trapezoidal Modulation

Equal to the single-phase-shift modulation, the two transformer voltages $v_{T1}$ and $v_{T2}$ will be phase-shifted in the trapezoidal modulation scheme. In addition to that, two inner phase-shifts are introduced between the two legs of each full bridge. This causes the duty cycle of $v_{T1}$ and $v_{T2}$ to change and introduces a period of time during which $v_{T1}$ and $v_{T2}$ will be zero. These intervals are named $\Omega_1$ and $\Omega_2$ [35] and can be seen in Figure 3.5. An auxiliary parameter $\epsilon$ is introduced which is needed for the simulation and is further explained in Section 4.2.2. It is notable that the on and off times of the switches continue to equal 50 % of one switching period and it is only the duty cycles of the transformer voltages that change.

### 3.2.1 Transmission Power, Phase-Shift Angle $\varphi$ and Duty Cycles

The equations for the transmission power, phase-shift angle and other following expressions are given in [35]. However, they have been supplemented with the transformer turns ratio $n$ since $n$ is not equal to 1 in this work and therefore has to be considered. Furthermore, the corresponding equations have been simplified concerning the factors $sgn(\varphi)$ and $sgn(I_{ch2})$ which in this work will always be equal

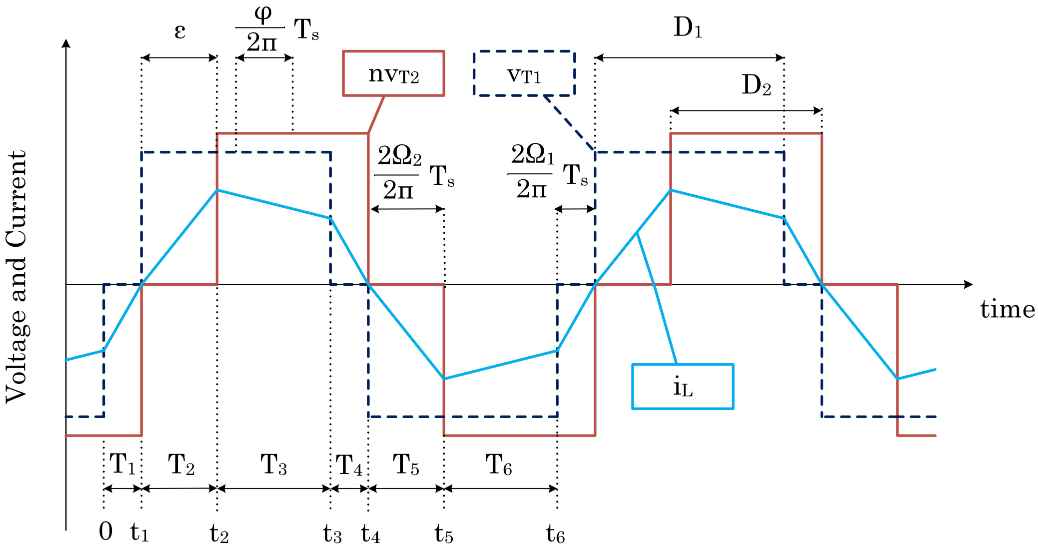



**Figure 3.5:** Primary and referred secondary transformer voltage and inductor current for the trapezoidal modulation

to 1 as only unidirectional and positive power flow occurs. Lastly, the blanking time $\tau_{blank}$ that has been considered in [35] is neglected because in the scope of this work it is not considered in the single-phase-shift modulation either.

According to [27] and [35], the ratio of input and output power is decisive for calculating the necessary parameters to implement the trapezoidal modulation scheme. Two cases can be distinguished which lead to different values for $d$, the so called DC transformation ratio. This ratio is defined as

$$d = \frac{nV_o}{V_i} \tag{3.8}$$

**Case 1: Input voltage $V_i$ is lower than referred output voltage $nV_o$**

In the case of

$$V_i \leq nV_o \tag{3.9}$$

it follows that

$$d \geq 1 \tag{3.10}$$

In order to implement the trapezoidal modulation, values for the parameters $\Omega_1$, $\Omega_2$ and the phase-shift $\varphi$ between the two bridges have to be calculated. $\Omega_1$ and $\Omega_2$ are defined as zero-voltage widths [35] of the primary and secondary side transformer voltages $v_{T1}$ and $v_{T2}$, given by the following equations

$$\Omega_1 = \frac{\pi\ (V_i - nV_o) + 2nV_o\varphi}{2(V_i + nV_o)} \tag{3.11}$$

$$\Omega_2 = \varphi - \Omega_1 \tag{3.12}$$

**Case 2: Input voltage $V_i$ is higher than referred output voltage $nV_o$**

In the case of

$$V_i > nV_o \tag{3.13}$$

it follows that

$$d < 1 \tag{3.14}$$

In this case, the equations for $\Omega_1$ and $\Omega_2$ change and are given by

$$\Omega_1 = \varphi - \Omega_2 \tag{3.15}$$

$$\Omega_2 = \frac{\pi\ (nV_o - V_i) + 2V_i\varphi}{2(V_i + nV_o)} \tag{3.16}$$

By means of $\Omega_1$ and $\Omega_2$, the equations of the duty cycles of $v_{T1}$ and $v_{T2}$ can be derived, leading to

$$D_1 \;=\; \left(1 - \frac{2\Omega_1}{\pi}\right)\ T_{hs} \tag{3.17}$$

$$D_2 \;=\; \left(1 - \frac{2\Omega_2}{\pi}\right)\ T_{hs} \tag{3.18}$$

where $T_{hs}$ is half a switching period.

$D_1$ and $D_2$ are not only representing the duty cycles, but also corresponding to the inner phase-shifts, i. e., the phase-shifts between the two legs of the input and output bridge. This can be seen in Figures 3.6 and 3.7.

It is notable that the inner phase-shifts attain different values in the input and output bridge. Again with the respective values for $\Omega_1$ and $\Omega_2$, the transmitted

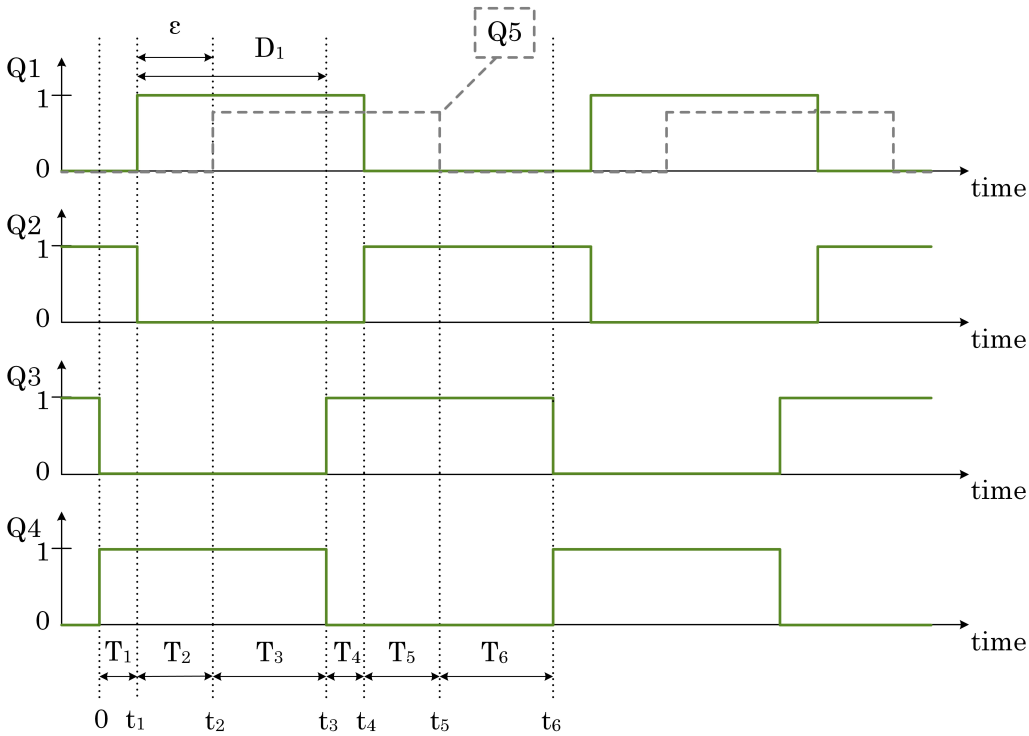



**Figure 3.6:** Switching signals for the gates Q1 to Q4

power and corresponding angle are calculated equally in both cases [35]:

$$\begin{aligned} P &= \frac{nV_o\,(\pi-\varphi-\Omega_1-\Omega_2)\,[nV_o\,(\varphi-\Omega_2+\Omega_1)+V_i\,(\varphi-\Omega_1+\Omega_2)]}{4\pi^2 L f_s} \\ &+ \frac{(nV_o)^2\,(\varphi-\Omega_2+\Omega_1)^2}{4\pi^2 L f_s} \end{aligned} \tag{3.19}$$

and

$$\varphi = \pi\left(\frac{e_1}{2e_2} - \frac{(V_i+nV_o)\,\sqrt{e_3-4f_s I_{ch2} L e_2}}{2\sqrt{V_i}e_2}\right) \tag{3.20}$$

where

$$e_1 = V_i^2 + (nV_o)^2 \tag{3.21}$$

$$e_2 = V_i^2 + nV_oV_i + (nV_o)^2 \tag{3.22}$$

$$e_3 = nV_oV_i^2 \tag{3.23}$$

and $I_{ch2}$ is set as $I_{ch2} = \frac{P}{nV_o}$.

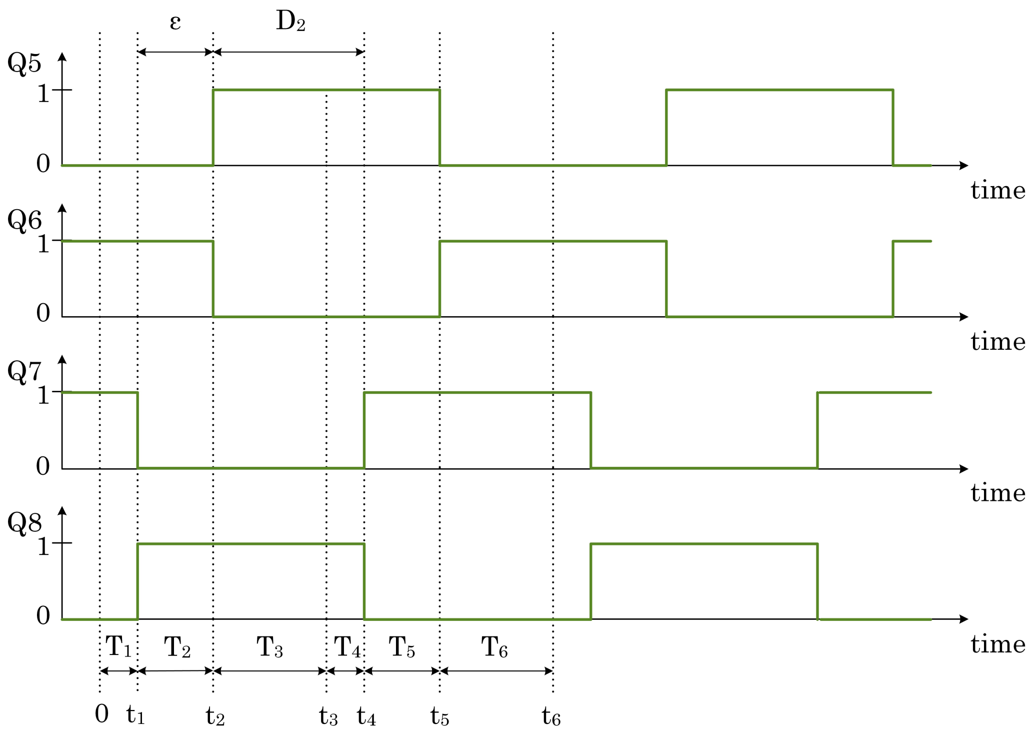



**Figure 3.7:** Switching signals for the gates Q5 to Q8

Corresponding to the case in single-phase-shift modulation, the maximally transmitted power can be deduced by derivation of this equation by the phase-shift angle $\varphi$ and setting this expression to zero. This gives the value of $\varphi$ at which maximum power transfer occurs ($\varphi = \frac{\pi}{3}$) and subsequently the corresponding leakage inductance. The expression is taken from [35] and reads as:

$$L = \frac{(nV_o)^2 \, V_i^2}{4 f_s P_{max} \, [V_i^2 + nV_o V_i + (nV_o)^2]} \tag{3.24}$$

With $P_{max} = 0.97$ MW and nominal voltages, the leakage inductance corresponds to $L = 29.8$ $\mu$H (refer Section 4.1.1 for final determination of L).

### 3.2.2 Voltages and Currents

Similarly to single-phase-shift modulation, different voltages and currents apply during the different periods of one switching cycle. These are explained in the following. The labels of the time intervals are referring to Figures 3.5, 3.6 and 3.7.

1. Time interval $T_1$ ($0 < t < t_1$)

   - Q2, Q6 and Q7 are ON
   - Q4 is switched ON
   - Q1, Q5 and Q8 are OFF
   - Q3 is switched OFF

   In the first time interval the voltage across the inductor is given by $nV_o$. This voltage is always positive and causes a rising current $i_L$ equal to

$$i_L(t) \;=\; i_L(0) + \frac{1}{L}\, nV_o\, \Delta t \tag{3.25}$$

2. Time interval $T_2$ ($t_1 < t < t_2$)

   - Q4 and Q6 are ON
   - Q1 and Q8 are switched ON
   - Q3 and Q5 are OFF
   - Q2 and Q7 are switched OFF

   The voltage across the inductor is now given by $V_i$. This voltage is again positive so that $i_L$ will increase further. However, the slope will be different than in the first time interval. Depending on the relation between $V_i$ and $nV_o$, the slope will be less steep for $V_o = 16$ kV and $V_o = 16.8$ kV and steeper for $V_o = 15.2$ kV.

$$i_L(t) \;=\; i_L(t_1) + \frac{1}{L}\, V_i\, \Delta t \tag{3.26}$$

3. Time interval $T_3$ ($t_2 < t < t_3$)

   - Q1, Q4 and Q8 are ON
   - Q5 is switched ON
   - Q2, Q3 and Q7 are OFF
   - Q6 is switched OFF

In the third time interval, a voltage of $(V_i - nV_o)$ is applied across the inductor. This corresponds to the second time interval $\mathrm{T}_2$ in 3.1.2. Therefore, the same relations apply and in case of nominal output voltage $V_o = 16$ kV and $V_o = 16.8$ kV, the inductor current will fall. For $V_o = 15.2$ kV the current in this time interval will rise.

$$i_L(t) \;=\; i_L(t_2) + \frac{1}{L}\,(V_i - nV_o)\,\Delta t \tag{3.27}$$

4. Time interval $\mathrm{T}_4$ ($\mathrm{t}_3 < \mathrm{t} < \mathrm{t}_4$)

- Q1, Q5 and Q8 are ON
- Q3 is switched ON
- Q2, Q6 and Q7 are OFF
- Q4 is switched OFF

During the fourth time interval, the voltage across the inductor is given by $(-nV_o)$. This expression is always negative and causes the inductor current to fall.

$$i_L(t) \;=\; i_L(t_3) + \frac{1}{L}\,(-nV_o)\,\Delta t \tag{3.28}$$

5. Time interval $\mathrm{T}_5$ ($\mathrm{t}_4 < \mathrm{t} < \mathrm{t}_5$)

- Q3 and Q5 are ON
- Q2 and Q7 are switched ON
- Q4 and Q6 are OFF
- Q1 and Q8 are switched OFF

The voltage across the inductor is now expressed by $(-V_i)$. This expression is again always negative and causes the inductor current to decrease further. Similar to time interval $\mathrm{T}_2$, it depends on the level of the output voltage $V_o$ if the slope is steeper or less steep than during the previous time interval.

$$i_L(t) \;=\; i_L(t_4) + \frac{1}{L}\,(-V_i)\,\Delta t \tag{3.29}$$

6. Time interval $T_6$ ($t_5 < t < t_6$)

- Q2, Q3 and Q7 are ON
- Q6 is switched ON
- Q1, Q4 and Q8 are OFF
- Q5 is switched OFF

In the last time interval, the applied voltage across the inductor equals $(-V_i + nV_o)$. This corresponds to the voltage in the time interval $T_4$ in Section 3.1.2. For $V_o = 16$ kV and $V_o = 16.8$ kV, the inductor current rises due to the positive voltage. For $V_o = 15.2$ kV the applied voltage is negative and gives a negative slope to the inductor current (refer simulation results in Section 5.5).

$$i_L(t) \;=\; i_L(t_5) + \frac{1}{L}\,(-V_i + nV_o)\,\Delta t \tag{3.30}$$

### 3.2.3 Switching Behaviour

Just like in SPS modulation, the MOSFET current in all switches is negative prior to the turn-on moment (refer Figure 3.4). Thus, also the diode will conduct the current and ensure soft-switching. However, in contrast to SPS modulation and according to [35], four switches are expected to feature soft-switching also in the turn-off moment. By switching according to the trapezoidal modulation scheme, two points in time are generated where both $v_{T1}$ and $v_{T2}$ are zero. These moments are labeled as $t_1$ and $t_4$ in Figure 3.5. Choosing the duty ratios $D_1$ and $D_2$ according to equations (3.17) and (3.18), it is then ensured that the switching happens in the very moment when the inductor current crosses zero. From Figures 3.6 and 3.7, it can be observed that it is the switches Q1, Q2, Q7 and Q8 that will profit from this modulation and be soft-switched in the turn-off moment. That means that in total eight switches are soft-switched in turn-on and four switches are soft-switched in turn-off. It can be noted that two of these switches are on the LV-side and two on the HV-side.

## 3.3 Triangular Modulation

The triangular modulation owes its name to the triangular shape that the current takes when it is applied. The variables for controlling the power flow are the phase-shift angle between primary and secondary transformer voltage as well as a change in duty ratio of these voltages. In distinction from the trapezoidal modulation scheme, the triangular modulation features two time periods during which both square voltages $v_{T1}$ and $v_{T2}$ are zero. This results in two time intervals with zero inductor current $i_L$ as can be seen in Figure 3.8.

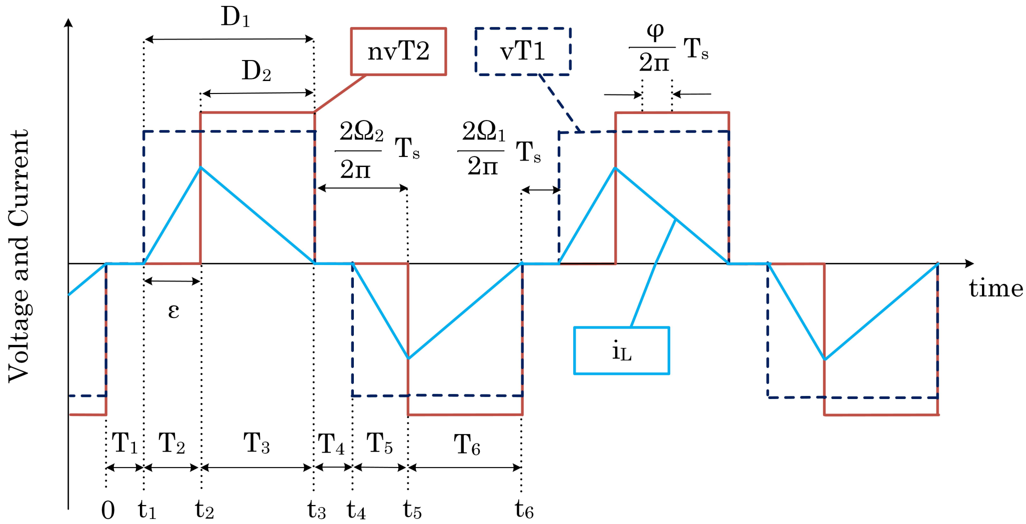



**Figure 3.8:** Primary and referred secondary transformer voltage and inductor current for the triangular modulation

### 3.3.1 Transmission Power, Phase-Shift Angle $\varphi$ and Duty Cycles

Again the parameters to implement this modulation scheme have to be calculated and two cases are distinguished. The following relations are based on [35].

**Case 1: Input voltage $V_i$ is lower than referred output voltage $nV_o$**

In the case of

$$V_i \leq nV_o \tag{3.31}$$

it follows that

$$d \geq 1 \tag{3.32}$$

The zero-voltage widths $\Omega_1$ and $\Omega_2$ are defined as

$$\Omega_1 = \frac{\pi}{2} - \frac{nV_o\varphi}{nV_o - V_i} \tag{3.33}$$

$$\Omega_2 = \varphi + \Omega_1 \tag{3.34}$$

In contrast to the trapezoidal modulation, the transmission power is given by two different expressions according to the value of $d$. In the first case it reads as

$$P = \frac{nV_oV_i\varphi\left(\pi - 2\Omega_2\right)}{2\pi^2 Lf_s} \tag{3.35}$$

while the corresponding angle is given by

$$\varphi = \frac{\pi\sqrt{I_{ch2}Lf_s\left(nV_o - V_i\right)}}{V_i} \tag{3.36}$$

**Case 2: Input voltage $V_i$ is higher than referred output voltage $nV_o$**

In the case of

$$V_i > nV_o \tag{3.37}$$

it follows that

$$d < 1 \tag{3.38}$$

The zero-voltage widths $\Omega_1$ and $\Omega_2$ differ from case 1 and read as

$$\Omega_1 = \varphi + \Omega_2 \tag{3.39}$$

$$\Omega_2 = \frac{\pi}{2} + \frac{\varphi V_i}{nV_o - V_i} \tag{3.40}$$

The power and angle are defined as

$$P = \frac{nV_oV_i\varphi\left(\pi - 2\Omega_1\right)}{2\pi^2 Lf_s} \tag{3.41}$$

and

$$\varphi = \frac{\pi\sqrt{I_{ch2}Lf_s\left(V_i - nV_o\right)}}{\sqrt{nV_oV_i}} \tag{3.42}$$

The duty cycles can be calculated with the same relations that are given in (3.17) and (3.18). Like in the other two modulation methods, various voltages and resulting currents will apply during the six different time intervals. Since the triangular modulation is not simulated in the scope of this work, the quantitative course of these values is not further regarded.

### 3.3.2 Switching Behaviour

According to [35], the triangular modulation scheme features soft-switching in the turn-on moment for all switches. Additionally, it is mentioned that six switches will be soft-switched also in the moment of turn-off. When examining the course of the inductor current and transformer voltages in Figure 3.8, it can be seen that both will be zero at the moments 0, $t_1$, $t_3$ and $t_4$. Comparing with the switching signals in Figures 3.9 and 3.10, it is concluded that it is therefore the switches Q1, Q2, Q3, Q4, Q7 and Q8 that will be soft-switched at turn-off. However, the triangular modulation is not simulated in the scope of this work. This assumption has therefore yet to be proven.

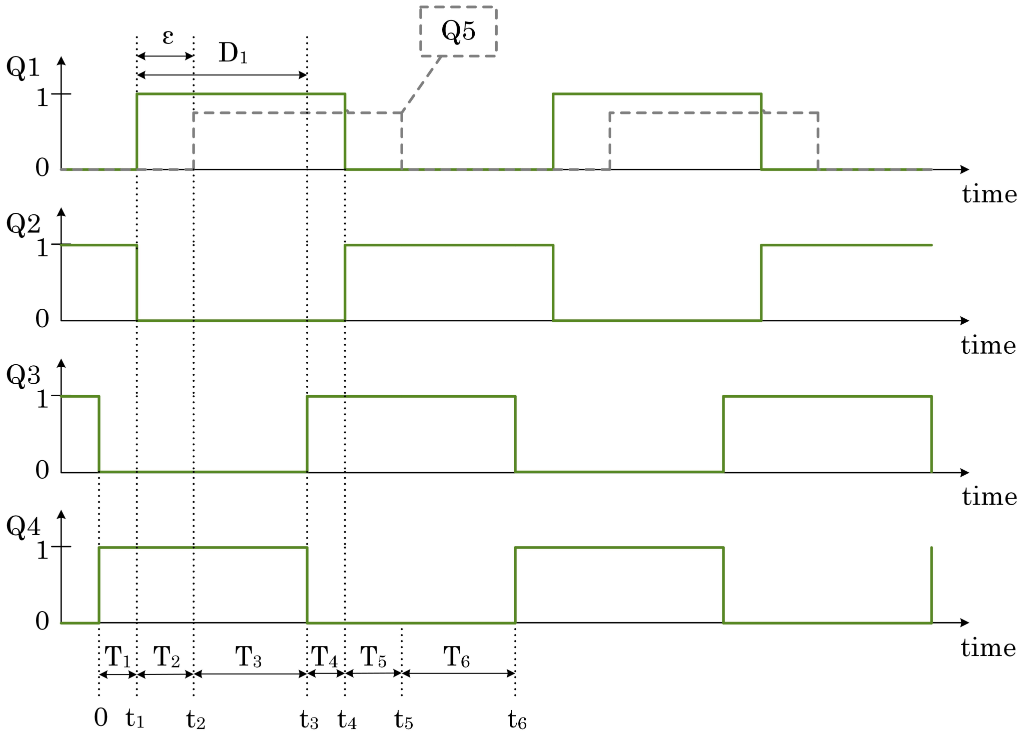



**Figure 3.9:** Switching signals for the gates Q1 to Q4

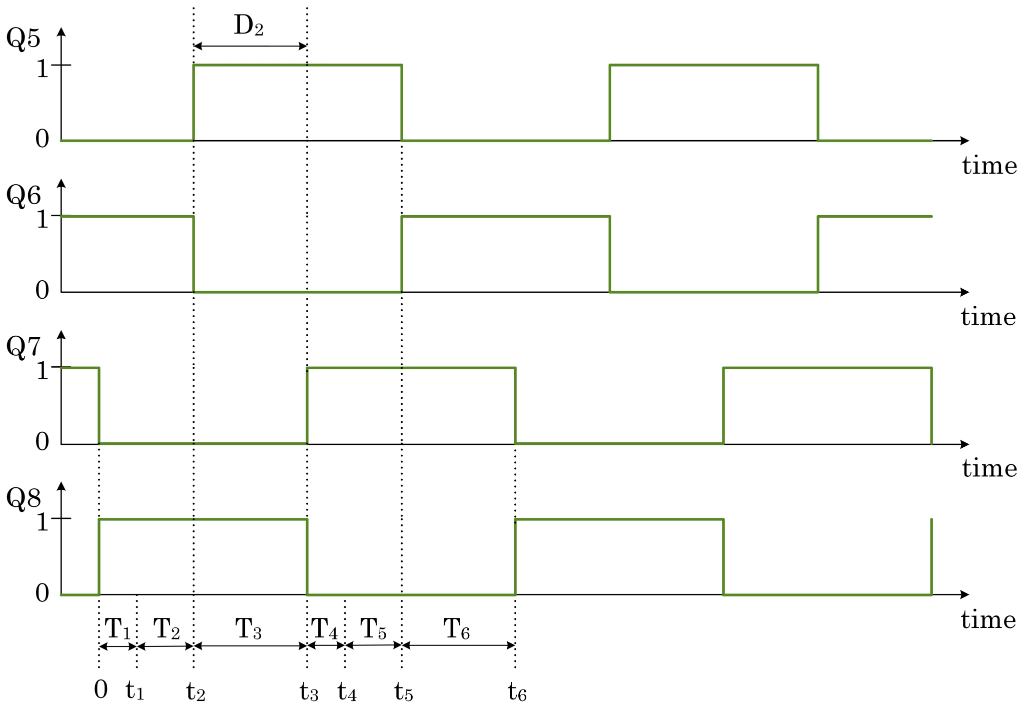



**Figure 3.10:** Switching signals for the gates Q5 to Q8

## 3.4 Combined Modulations

It is described in [27] and [35] that different modulations are varyingly well suited for different power levels. When combining the three presented modulations, the following distribution is suggested in [35]:

**Case 1: Input voltage $V_i$ is lower than referred output voltage $nV_o$**

- Triangular modulation for

$$0 = \varphi \leq \frac{\pi}{2}\left(1 - \frac{V_i}{nV_o}\right) \tag{3.43}$$

- Trapezoidal modulation for

$$\frac{\pi}{2}\left(1 - \frac{V_i}{nV_o}\right) \leq \varphi \leq \frac{\pi}{2}\left(\frac{V_i^2 + (nV_o)^2}{V_i^2 + nV_oV_i + (nV_o)^2}\right) \tag{3.44}$$

- Single-phase-shift modulation for

$$\frac{\pi}{2}\left(\frac{V_i^2+(nV_o)^2}{V_i^2+nV_oV_i+(nV_o)^2}\right) \;\leq\; \varphi \leq \frac{\pi}{2} \tag{3.45}$$

**Case 2: Input voltage $V_i$ is higher than referred output voltage $nV_o$**

- Triangular modulation for

$$0 \;=\; \varphi \;\leq\; \frac{\pi}{2}\left(1-\frac{nV_o}{V_i}\right) \tag{3.46}$$

- Trapezoidal modulation for

$$\frac{\pi}{2}\left(1-\frac{nV_o}{V_i}\right) \;\leq\; \varphi \;\leq\; \frac{\pi}{2}\left(\frac{V_i^2+(nV_o)^2}{V_i^2+nV_oV_i+(nV_o)^2}\right) \tag{3.47}$$

- Single-phase-shift modulation for

$$\frac{\pi}{2}\left(\frac{V_i^2+(nV_o)^2}{V_i^2+nV_oV_i+(nV_o)^2}\right) \;\leq\; \varphi \;\leq\; \frac{\pi}{2} \tag{3.48}$$

With the chosen voltage levels, this leads to the distribution shown in Figure 3.11.

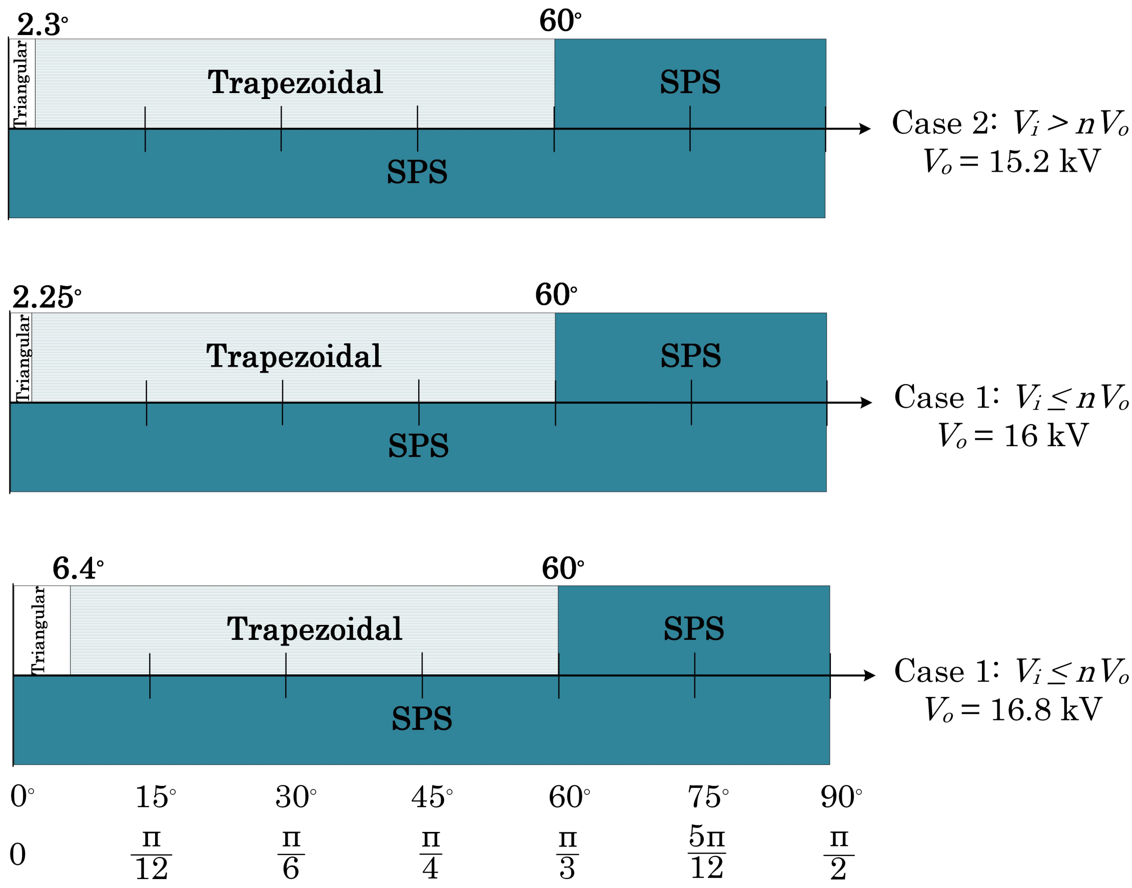



**Figure 3.11:** Distribution of modulation schemes over the whole angle range with the chosen output voltages $V_o = 15.2$ kV, $V_o = 16$ kV and $V_o = 16.8$ kV

It is notable that the upper limit value for trapezoidal modulation slightly changes due to the changing output voltages. The exact values are 60.0068° (for $V_o = 15.2$ kV), 60.0064° (for $V_o = 16$ kV) and 60.055° (for $V_o = 16.8$ kV), but it will be set to 60° for reasons of simplicity.

Also, this work does not focus on the exact switching moment from one modulation scheme to the other and this is therefore not regarded.

# 4

# Model in PLECS®

## 4.1 Components and Parameters

With the framework conditions given in Chapter 2, the model of the Dual-Active-Bridge can be built in PLECS®. Parameters that are defined in the Simulation Parameter Initialization dialogue in PLECS® are given in Table 4.1. The definition of certain parameters will be explained in the following sections. A schematic of the PLECS® model is presented in Figure 4.1 and the complete PLECS® simulation initialization dialogues for both modulation schemes and all voltage levels are provided in Appendix A.

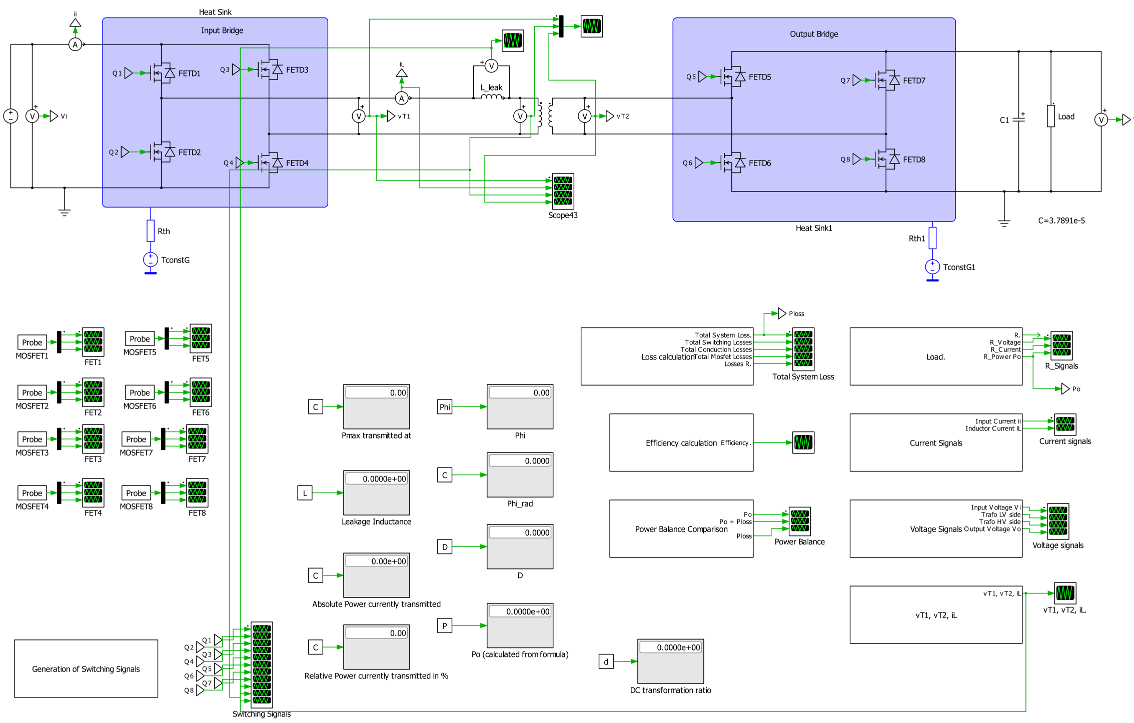



**Figure 4.1:** Schematic of the DAB model in PLECS® for the example of single-phase-shift modulation

**Table 4.1:** Simulation Parameter Initialization

| | Parameter | Value |
|---|---|---|
| Input Voltage | $V_i$ | 1.3 kV |
| Output Voltages | $V_o$ | 15.2 kV, 16 kV, 16.8 kV |
| Maximum Input Power | $P$ | 0.97 MW |
| Switching Frequency | $f_s$ | 5 kHz |
| Primary Number of Turns | $N_1$ | 1 |
| Secondary Number of Turns | $N_2$ | 12 |
| Turns Ratio | $n$ | 0.0833 |
| On-Resistance $R_{DS(on)}$ | Ron | 45 mΩ |
| $n_s/n_p$ on the Low Voltage Side | $ns\_LV/np\_LV$ | 2 / 15 |
| $n_s/n_p$ on the High Voltage Side | $ns\_HV/np\_HV$ | 15 / 2 |
| Leakage Inductance | $L$ | 28.3 $\mu$H |
| Output Capacitance | $C$ | 37.9 $\mu$F |

### 4.1.1 Transformer and Leakage Inductance

In this work, the transformer does not feature any core or winding losses, but is assumed to show ideal behaviour. Thus, it is modeled as a combination of two windings with a turns ratio of 1:12 and an attached leakage inductance. The leakage inductance is one of the most important elements of the Dual-Active-Bridge and makes it possible to transmit power. An appropriate sizing is fundamental for the behaviour of the model, because a large leakage inductance leads to an undesirable flow of reactive power and circulating current in the system. Is it too small, the soft-switching capability of the topology might be obstructed. The inductance value is chosen such that it is suitable for all three modulation schemes. Thus, the comparison is carried out under equal initial conditions.

The value of the leakage inductance is a function of the power and the angle at which this power is transferred (refer Equations (3.1) and (3.19)). To determine its value, these two variables have to be set. In case of trapezoidal modulation, it was shown in Figure 3.11 that with the chosen input and output voltages, the maximum possible angle lays at 60° in both case 1 and case 2. Consequently, this angle is chosen as maximum power transmission angle. For the SPS modulation, the maximum power transmission angle is also set to 60°, hereby allowing for a fair comparison. The procedure for determining the final value of the leakage inductance is shown in Figure 4.2.

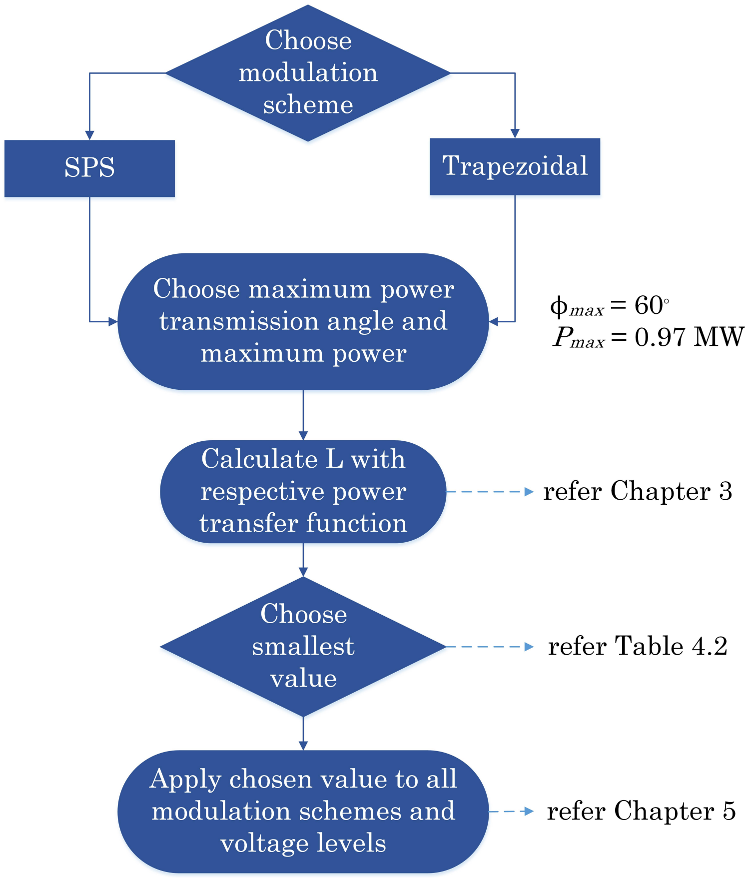



**Figure 4.2:** Process of choosing the value of leakage inductance for all the three modulation schemes

From Table 4.2 the leakage inductance is consequently set to $L = 28.3\ \mu$H for all modulation schemes and all output voltage levels.

**Table 4.2:** Value for the leakage inductances with full power transmission at $\varphi = 60°$

| | 15.2 kV | 16 kV | 16.8 kV |
|---|---|---|---|
| SPS | 37.7 $\mu$H | 39.7 $\mu$H | 41.7 $\mu$H |
| Trapezoidal | 28.3 $\mu$H | 29.8 $\mu$H | 31.2 $\mu$H |

It is notable that with this choice of leakage inductance only in the case of trapezoidal modulation at $V_o = 15.2$ kV, full load will be transmitted at 60° and in the other cases it has been naturally shifted to smaller angles (refer Figure 4.3 where the division of power over the modulation schemes is shown). Further, it has to be noted that the triangular modulation is not involved in this process. This is because it is not yet known at which power the modulation scheme will change from trapezoidal to triangular. Therefore, no power values can be assigned to the respective angles presented in Figure 3.11.

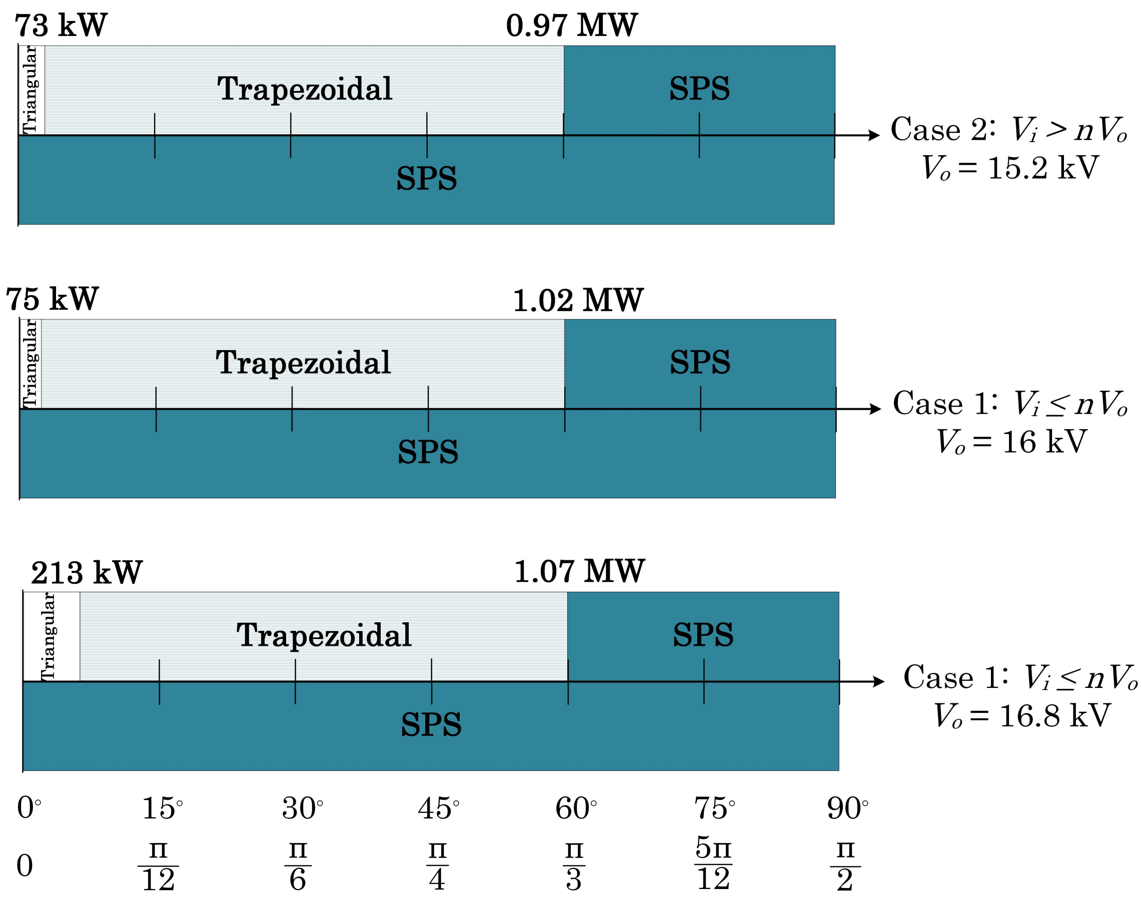



**Figure 4.3:** Distribution of modulation schemes over the power range with the chosen leakage inductance and the output voltages $V_o = 15.2$ kV, $V_o = 16$ kV and $V_o = 16.8$ kV

### 4.1.2 MOSFET Switches

In order to simulate conduction and switching losses in PLECS®, a thermal description has to be assigned to each switch. The thermal description is based on the graphs available from the data sheet: The $V_{DS} - I_{DS}$−diagram at 25 °C, the $I_{DS} - E_{on}$−diagram and $I_{DS} - E_{off}$−diagram, respectively. However, it was described in Section 2.2 that it is necessary to connect multiple MOSFETs in series and parallel in each switching block Q1 to Q8. In order to avoid the physical modeling of these series and parallel connections, a thermal description of a MOSFET equivalent is created. It features the same characteristics as $n_s$ in series and $n_p$ in parallel connected switches. This allows to model only this MOSFET equivalent in PLECS® and will avoid unnecessary slowing down of the simulation. Moreover, the adaptation of the model in case of desired changes in voltage or maximum transmitted power is facilitated.

To model the MOSFET equivalent, the following approach is tested and validated in an exemplary circuit before its implementation in the DAB model. First, the value of the on-resistance $R_{DS(on)}$ is multiplied by $\frac{n_s}{n_p}$. In addition, the mentioned diagrams are scaled by multiplying the voltage values with the number of serial connected switches $n_s$ and the current values with the number of parallel connected switches $n_p$, as shown in Figure 4.4. The scaled diagrams are fed into PLECS® and directly give the correct conduction losses of the MOSFET equivalent. To obtain the correct switching losses, the switching energy $E_{switch}$ that results from the simulation has to be multiplied with $n_s$ and $n_p$, subsequently. It is worth mentioning that two different MOSFET equivalents are created since $n_s$ and $n_p$ are different at the low voltage side from the high voltage side.

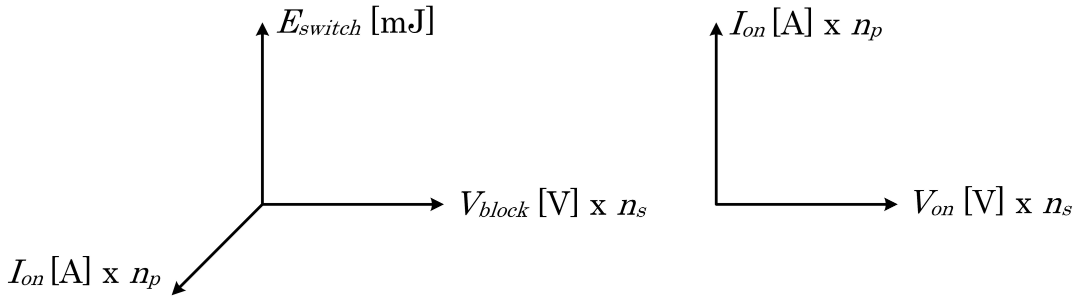



**Figure 4.4:** Scaling of switching and conduction losses

### 4.1.3 Anti-Parallel Diodes

The intrinsic body diode of the MOSFET is used as anti-parallel diode in the circuit. This is a simple approach in the case of SiC MOSFETs and decreases the cost as well as the required space compared to the use of an external anti-parallel diode [11, 12]. The characteristics of the body diode are given in the MOSFET datasheet in Appendix C. For the modeling of the diodes in PLECS®, the procedure is the same as in the case of the MOSFETs. The thermal description is based on the $V_{DS} - I_{DS}-$diagram at 25 °C and is scaled with the number of series and parallel connected switches. The diode switching losses are neglected.

### 4.1.4 Gate Signal Generation

In order to control the two full-bridges, a subsystem is created in which the necessary gate signals for the MOSFETs are generated. The signals are created by the comparison of a triangular wave with a constant reference signal $m$. The triangular wave is chosen to oscillate between 0 and 1 while the constant reference signal is equal to 0.5.

### 4.1.5 Output Capacitance

In the scope of this work no voltage control for the output capacitor is implemented. This leads to the assumption that a big capacitor would be suitable in order to keep the output voltage $V_o$ at a constant level. However, this approach causes a long time span until the system reaches steady-state conditions. In [35], the output capacitance is proposed to be chosen as

$$C \;=\; 50\,\frac{I_{Load}}{V_o f_s} \tag{4.1}$$

with

$$I_{Load} \;=\; \frac{P}{V_o} \quad . \tag{4.2}$$

Setting the maximum output power $P$ at 0.97 MW leads to a value of $C = 37.9\ \mu$F. With this choice, the circuit reaches steady-state within 0.04 s while the voltage ripple lies within an acceptable range (refer also Figure 4.5).

### 4.1.6 Output Voltage $V_o$

It was mentioned earlier that the output voltage $V_o$ is allowed to vary between the three values $V_o = 16$ kV, $V_o = 15.2$ kV and $V_o = 16.8$ kV which correspond to the nominal voltage and to $V_o \pm 5\,\%$. Prior to every simulation, the value of $V_o$ is preset and fixed.

## 4.2 Specialities in the Simulation of the Trapezoidal Modulation Scheme

### 4.2.1 Soft-Switching Qualities

Table 4.3 presents the expected switching losses of the system with trapezoidal modulation as explained in Section 3.2.3. In comparison, the observations in the simulation are presented and it can be seen that the values do not correspond to each other in the switches Q1, Q2, Q7 and Q8. It is apparent from Figures 3.5 to 3.7 that these switches should achieve soft-switching in turn-on and turn-off

**Table 4.3:** Expected and observed switching losses of the trapezoidal modulation scheme (0: no switching losses, 1: switching losses are observed)

| | Turn-On | | Turn-Off | | |
|---|---|---|---|---|---|
| | expected | observed | expected | observed | |
| Q1 | 0 | 1 | 0 | 1 | set all to zero |
| Q2 | 0 | 1 | 0 | 1 | |
| Q3 | 0 | 0 | 1 | 1 | correct |
| Q4 | 0 | 0 | 1 | 1 | |
| Q5 | 0 | 0 | 1 | 1 | |
| Q6 | 0 | 0 | 1 | 1 | |
| Q7 | 0 | 1 | 0 | 1 | set all to zero |
| Q8 | 0 | 1 | 0 | 1 | |

due to the fact that their switching happens in the moment when the inductor current $i_L$ crosses zero. From the simulation results, it is however obvious that this moment is missed by several microseconds depending on voltage level and load. This causes unexpected turn-on and turn-off losses. A possible explanation could be that all parameters that form the trapezoidal modulation, $\Omega_1$, $\Omega_2$, $D_1$, $D_2$ and $D$, are calculated based on the theoretical equations presented in Chapter 3. These equations have been implemented in PLECS® with values like the output voltage $V_o$ assumed to be constant and at nominal value. In the simulation it is however observed that due to ohmic losses in the switches, the output voltage $V_o$ will not reach this nominal value, but settle at a slightly lower value (refer Figure 4.5). To solve this discrepancy between the theoretical equations and the simulation results, two suggestions are put forward. One one hand, a control circuit could be implemented to keep the voltage across the output capacitor at the constant and nominal value of 16 kV. On the other hand, the momentary value $V_o$ could be dynamically fed back to the equations that are used to calculate the necessary parameters. Hence, ensure the correct determination and dynamic adaptation of these values. Due to the available resources in the scope of this work, these possible solutions are not tested in the simulation. Nevertheless, it is the goal to fairly treat the trapezoidal modulation in comparison with the SPS and not lose its main achievement of partial zero turn-off losses that are mentioned in literature [19, 35]. After considering different feasible options, it is decided that the switching losses of the respective switches will be manually set to zero in the simulation. This is shown in Table 4.3.

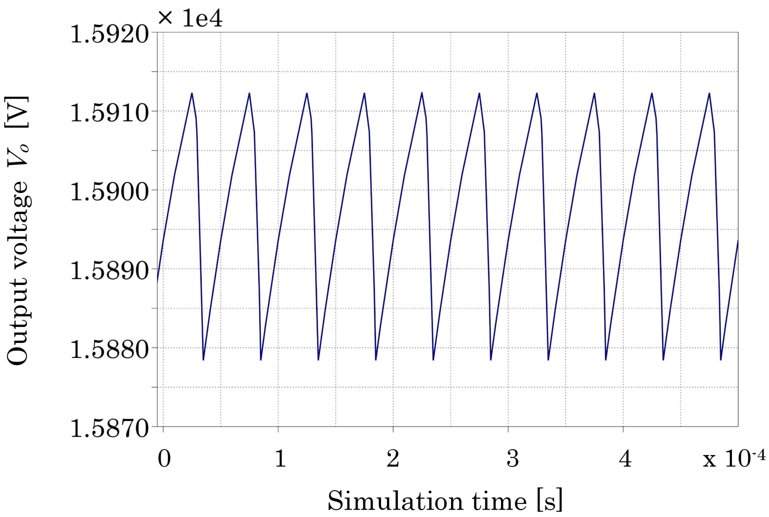



**Figure 4.5:** Course of the simulated output voltage $V_o$ with $V_o = 16$ kV

### 4.2.2 Auxiliary Parameter $\epsilon$

For the implementation of the trapezoidal modulation in PLECS®, an auxiliary parameter $\epsilon$ is set additionally to (3.17) and (3.18) which is used to phase-shift the switching signals in order to reach the correct voltage and current forms. As can be seen in Figure 3.5, this value is not equal to the phase-shift angle $\varphi$. This is due to the fact that the phase-shift is measured between half the on-time of $v_{T1}$ and half the on-time of $v_{T2}$. In the single-phase-shift modulation, $\epsilon$ equals $\varphi$ because of the constant duty cycle of 0.5 $T_s$ for both square voltages where $T_s$ is one switching period. However, in trapezoidal modulation, the duty cycle of the square voltages can differ from 0.5 $T_s$ and the resulting difference between $\epsilon$ and $\varphi$ has to be considered. The complete initialization parameters are provided in Appendix A.2.2.

# 5

# Analysis of Simulation Results

After modeling the Dual-Active-Bridge as well as the two considered modulation schemes in PLECS®, the presented case set up from Chapter 2 is simulated. According to this set up, the modulation schemes are subject to a variation in load and to a fluctuation in output voltage. The considered load cases are full load, 80 %, 50 %, 30 % and 10 % of full load, respectively. The output voltage $V_o$ will vary between the nominal voltage of $V_o = 16$ kV, a voltage drop down to $V_o = 15.2$ kV and a voltage rise up to $V_o = 16.8$ kV. This corresponds to a fluctuation of $\pm 5\,\%$. Both modulation schemes are simulated individually over the whole load range and the results of each case are compared and evaluated with regards to the following criteria:

- RMS Inductor Current
- Total Losses of the Semiconductor Switches
- Overall Efficiency
- Switching Losses
- Soft-Switching Range

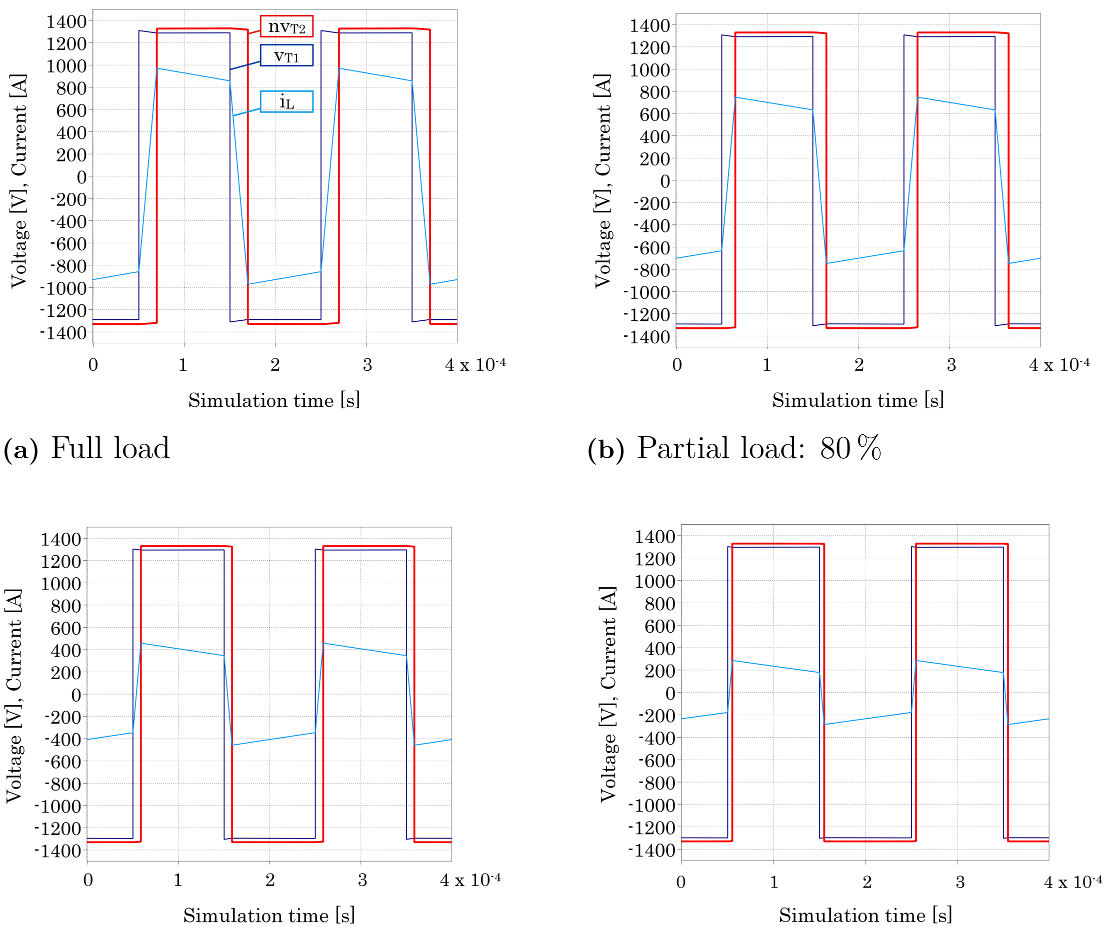
The parameters for comparison were chosen inspired by [13] and [19].

## 5.1 Transformer Voltages and Inductor Current

The basic functionality of the model and the two modulation schemes is tested by looking at the transformer voltages $v_{T1}$ and $v_{T2}$ and the resulting current $i_L$ through the leakage inductance. In the following Figures 5.1 to 5.6, the course of these parameters is presented for the three possible output voltage levels and different load conditions. It must be noted that the secondary transformer voltage is referred to the primary side and is consequently displayed as $nv_{T2}$.

### 5.1.1 Single-Phase-Shift Modulation

In Figure 5.1, the Dual-Active-Bridge is subject to an output voltage of $V_o = 16$ kV. All wave forms show the theoretically expected behaviour presented in Figure 3.2. It is visible that the current value decreases when the load is decreasing while at the same time the phase-shift angle between $v_{T1}$ and $nv_{T2}$ becomes smaller.




(a) Full load

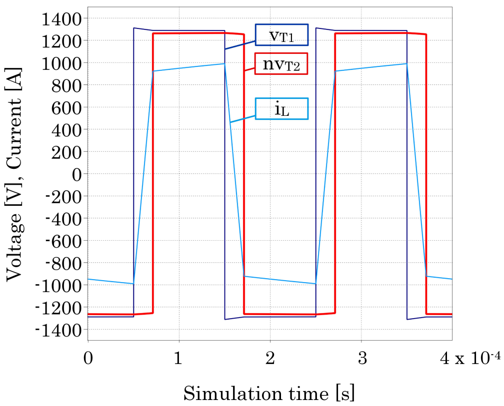
(b) Partial load: 80 %

(c) Partial load: 50 %

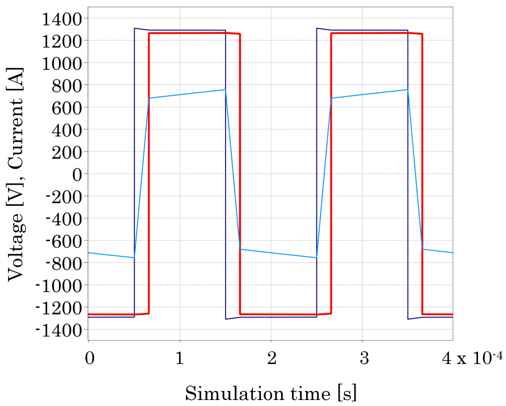
(d) Partial load: 30 %

**Figure 5.1:** Primary and referred secondary transformer voltage $v_{T1}$ and $nv_{T2}$ and respective inductor current $i_L$ at $V_o = 16$ kV with single-phase-shift modulation

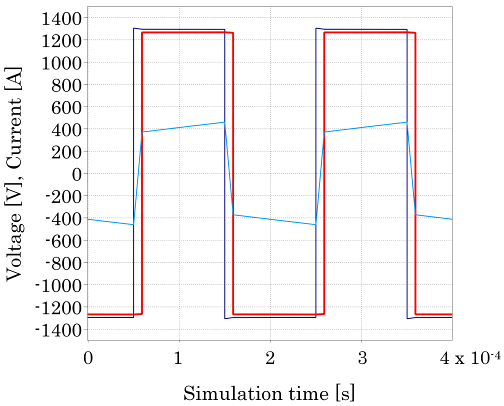
Figure 5.2 depicts the course of $v_{T1}$ and $nv_{T2}$ at a 5 % deviated value of the nominal voltage level of $V_o = 15.2$ kV. It can be observed in this case that the referred output voltage is lower than the input voltage. Therefore, the slope of the inductor current has changed its sign to a positive value while the inductor voltage is $(V_i - nV_o)$. This was explained in Section 3.1.2.



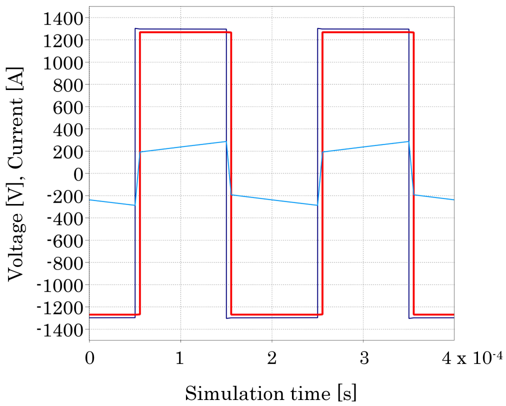

**(a)** Full load




**(b)** Partial load: 80 %



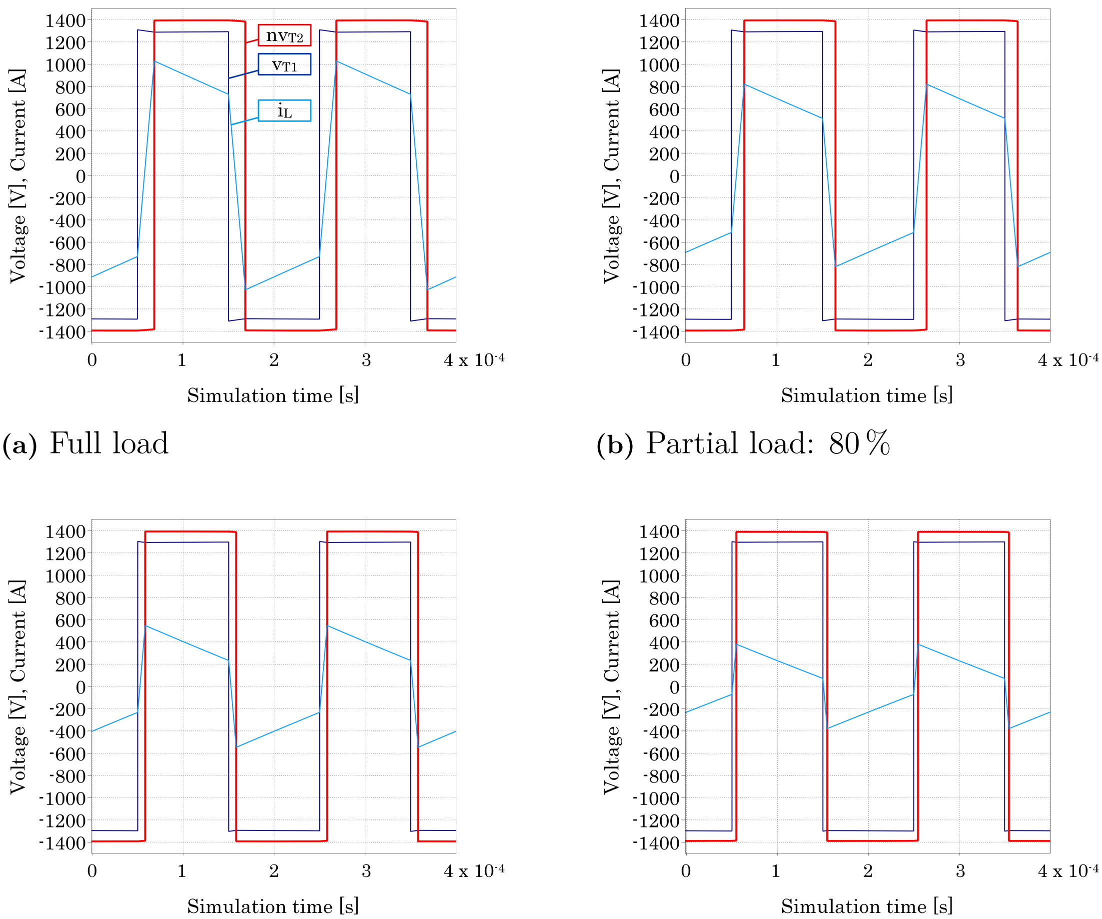

**(c)** Partial load: 50 %




**(d)** Partial load: 30 %

**Figure 5.2:** Primary and referred secondary transformer voltage $v_{T1}$ and $nv_{T2}$ and respective inductor current $i_L$ at $V_o = 15.2$ kV with single-phase-shift modulation

In Figure 5.3 the output voltage shows a rise of voltage of 5 %. Thus, the referred output voltage is higher than the input voltage. The sign of the slope of the inductor current in the second time interval is negative, corresponding to the case of nominal voltage.




**(a)** Full load

**(b)** Partial load: 80 %

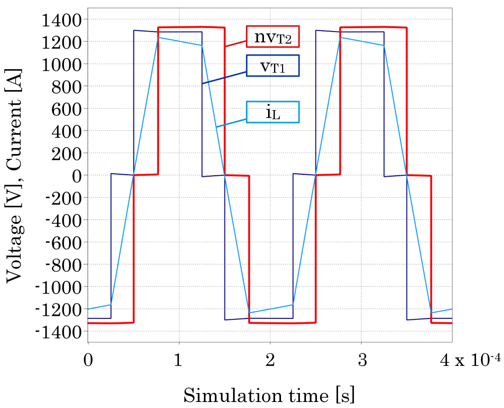
**(c)** Partial load: 50 %

**(d)** Partial load: 30 %

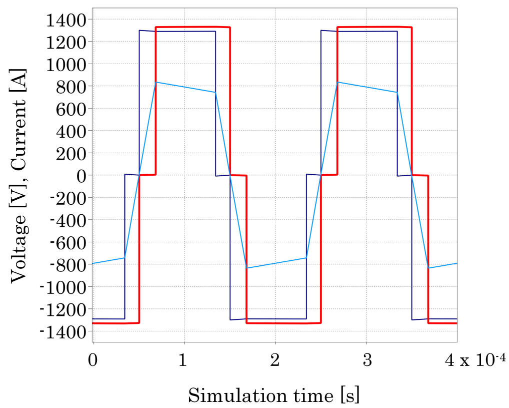
**Figure 5.3:** Primary and referred secondary transformer voltage $v_{T1}$ and $nv_{T2}$ and respective inductor current $i_L$ at $V_o$ = 16.8 kV with single-phase-shift modulation

### 5.1.2 Trapezoidal Modulation

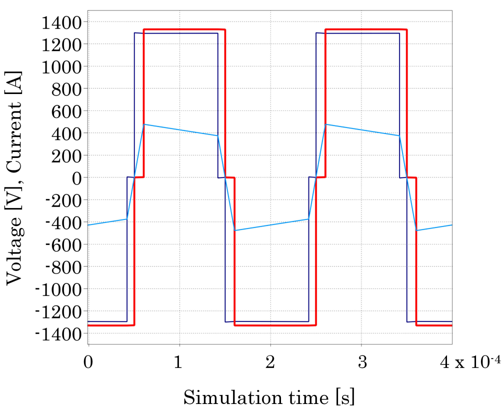
The wave forms from the simulation of the trapezoidal modulation exhibit the expected behaviour from Figure 3.5. Equally to single-phase-shift modulation, the value of the current as well as the phase-shift angle decrease with decreasing load. According to the equations in Section 3.2.1, the zero-voltage widths $\Omega_1$ and $\Omega_2$ decrease with decreasing phase-shift angle. The duty cycles are in return increasing. Furthermore, the slope of the current alternates in the third time interval while $(V_i - nV_o)$ is applied, depending on the relation of $V_i$ and $V_o$. This was presented in Section 3.2.2.



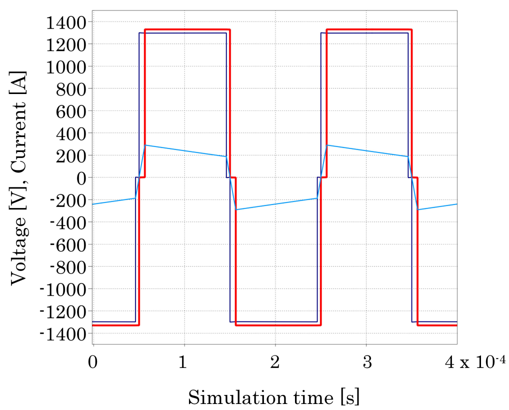

**(a)** Full load




**(b)** Partial load: 80 %

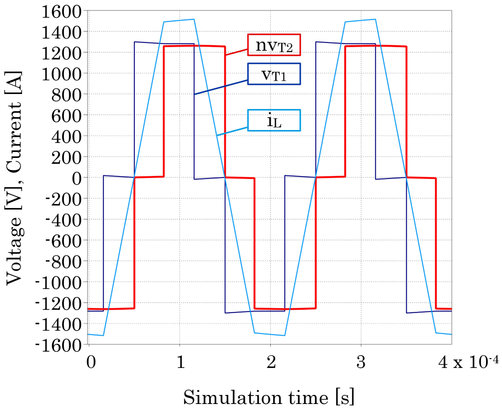



**(c)** Partial load: 50 %

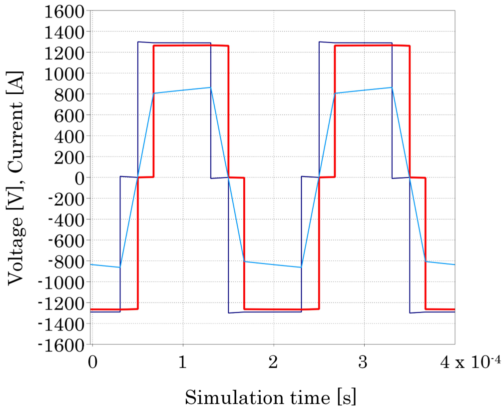



**(d)** Partial load: 30 %

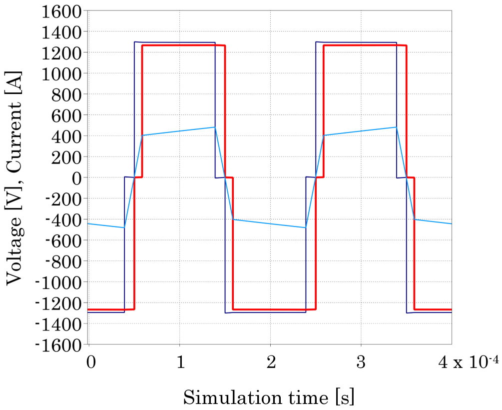
**Figure 5.4:** Primary and referred secondary transformer voltage $v_{T1}$ and $nv_{T2}$ and respective inductor current $i_L$ at $V_o = 16$ kV with trapezoidal modulation



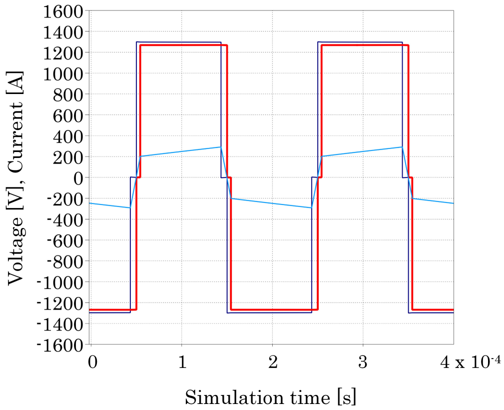

**(a)** Full load




**(b)** Partial load: 80 %

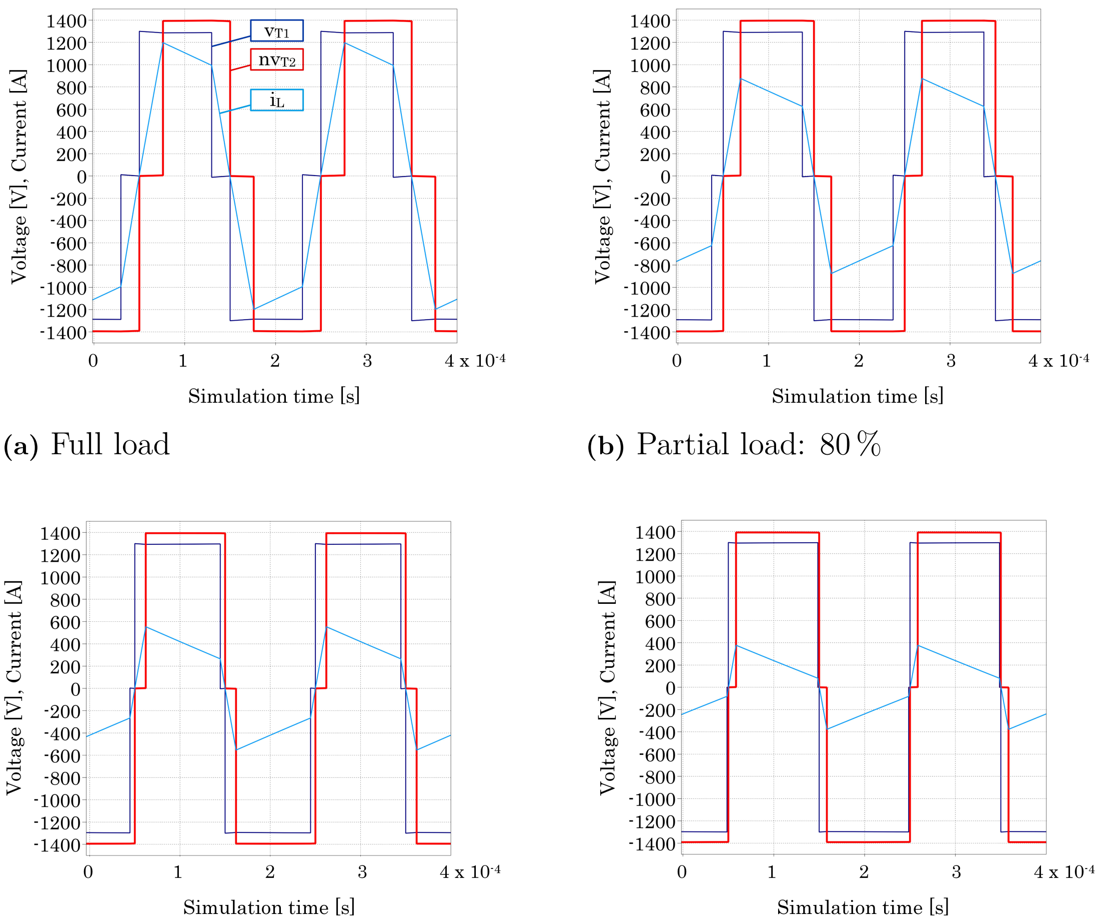



**(c)** Partial load: 50 %




**(d)** Partial load: 30 %

**Figure 5.5:** Primary and referred secondary transformer voltage $v_{T1}$ and $nv_{T2}$ and respective inductor current $i_L$ at $V_o = 15.2$ kV with trapezoidal modulation




**(a)** Full load

**(b)** Partial load: 80 %

**(c)** Partial load: 50 %

**(d)** Partial load: 30 %

**Figure 5.6:** Primary and referred secondary transformer voltage $v_{T1}$ and $nv_{T2}$ and respective inductor current $i_L$ at $V_o = 16.8$ kV with trapezoidal modulation

## 5.2 Comparison of Single-Phase-Shift and Trapezoidal Modulation

### 5.2.1 RMS Inductor Current

In the following Figures 5.7 to 5.9, the course of the RMS inductor current is depicted for the three different output voltage levels and different load conditions, respectively. Firstly, it can be noted that due to the constant output voltage in every case, the current value decreases with decreasing load. Secondly, it is visible that for an output voltage lower than nominal at $V_o = 15.2$ kV, the current takes a larger value in order to deliver the requested power while for a higher output voltage at $V_o = 16.8$ kV, the current reduces. Beyond that, it is apparent that for all voltage and load levels, the single-phase-shift modulation presents lower RMS current values than the trapezoidal modulation. Depending on the voltage level, a difference between 9 % and up to 20 % in current stress can be observed for the full load condition. This observation coincides with simulation results that are shown in [13]. Finally, it is noted that the minimum load that can be transmitted via trapezoidal modulation at $V_o = 16.8$ kV is 213 kW, corresponding to 22 % of the full load (refer Figure 4.3). Therefore, no current value is available in the case of a 10 % load for trapezoidal modulation in Figure 5.9, but the power transmission must be handled by means of the triangular modulation.

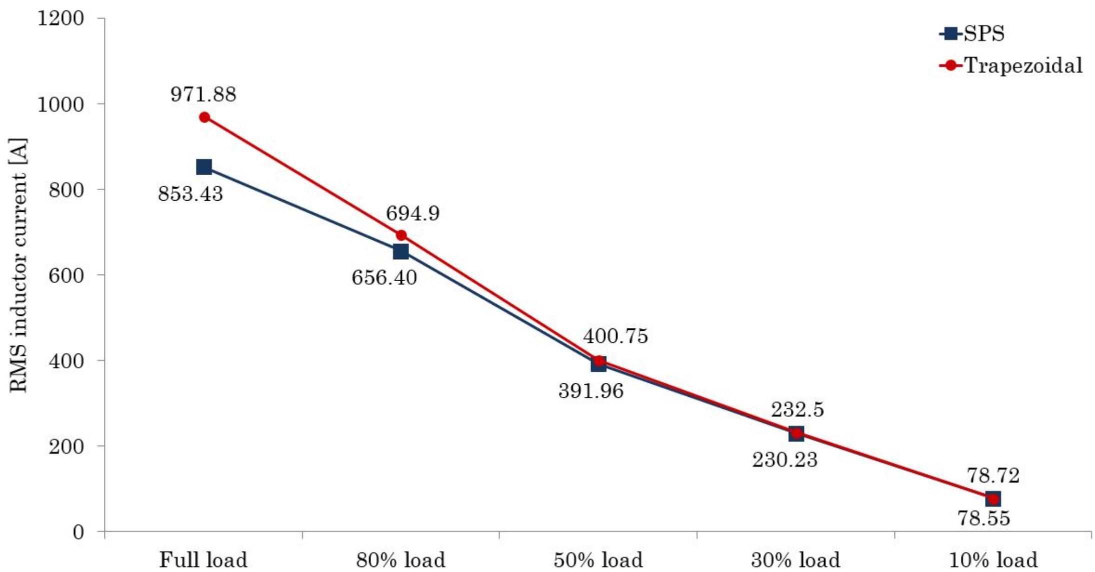



**Figure 5.7:** RMS inductor current at different transmission power levels with $V_o = 16$ kV and MOSFET switches

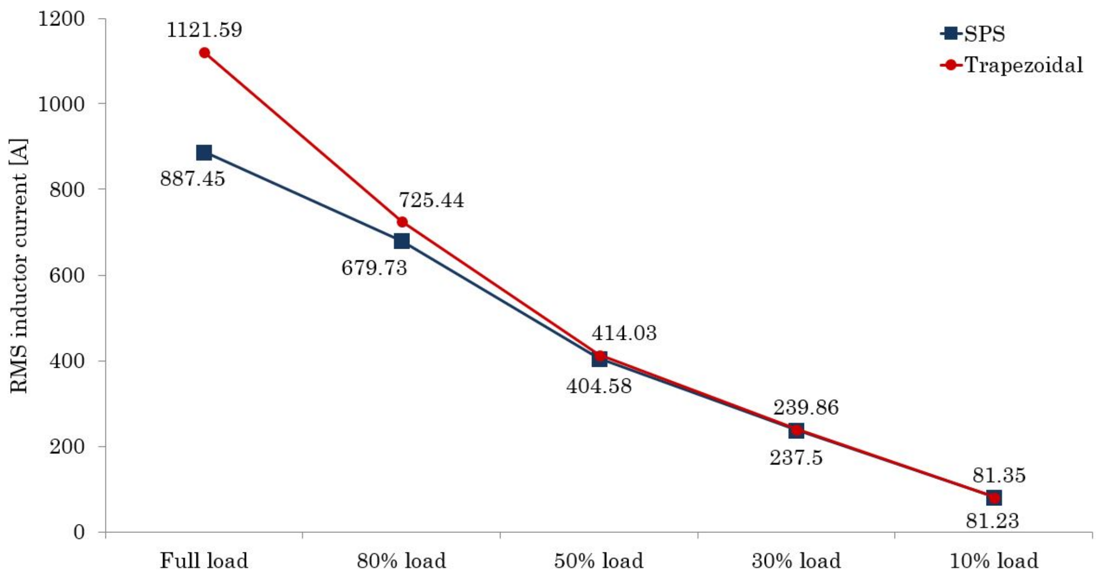



**Figure 5.8:** RMS inductor current at different transmission power levels with $V_o = 15.2$ kV and MOSFET switches

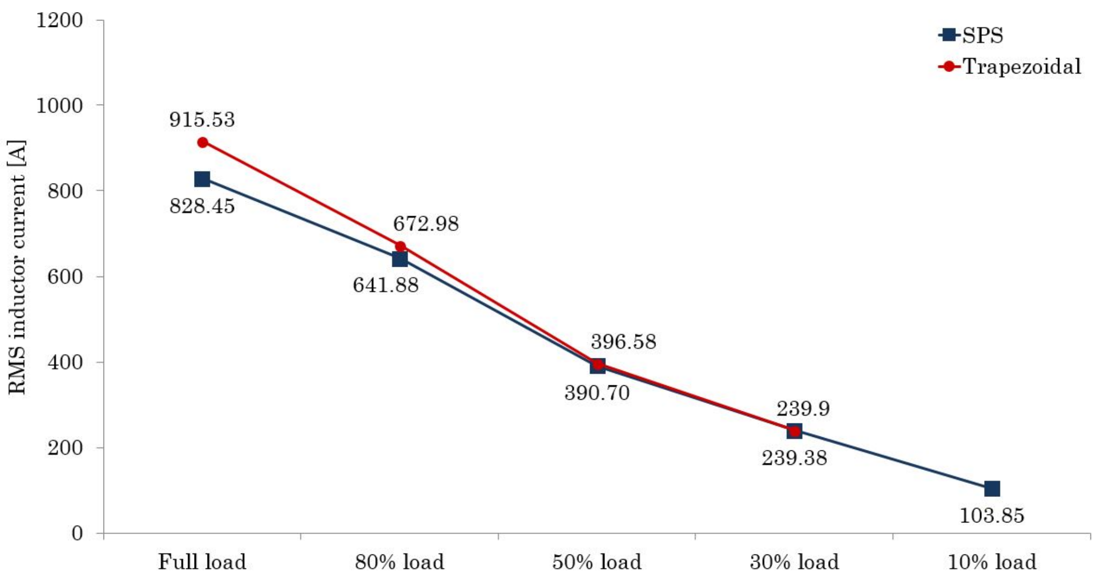



**Figure 5.9:** RMS inductor current at different transmission power levels with $V_o = 16.8$ kV and MOSFET switches

### 5.2.2 Total Losses and Efficiency

The Figures 5.10 to 5.12 show the total losses and the Figures 5.13 to 5.15 show the corresponding efficiencies of the built up model. The losses consist of switching losses and conduction losses of the semiconductor switches and conduction losses of the anti-parallel diodes. The respective diagrams of turn-on and turn-off switching energy and characteristics of the body diode are presented in the MOSFET datasheet in Appendix C.

It is apparent that the total losses decrease with decreasing load and accordingly decreasing current. Corresponding to the behaviour of the RMS current, the total losses will be higher for a lower output voltage and lower for a higher output voltage.

According to what is expected from the course of the RMS current, the total losses in trapezoidal modulation can at first be observed to be larger than in single-phase-shift modulation. However, starting at a load of 30 % and downwards, the relation is inverted and the total loss values of the trapezoidal modulation scheme become slightly smaller than the ones of the SPS modulation. Consequently, it is visible in the Figures 5.13 to 5.15 that for load conditions down to 50 % of the load, the SPS modulation will provide a better efficiency than the trapezoidal modulation. For smaller values of transmitted power, the figures show that the trapezoidal modulation presents slightly better results. This is in line with the suggestions in literature to apply SPS modulation for large loads and trapezoidal modulation for light loads. The results can be explained when looking at the distribution of switching and conduction losses at the different load levels. It is presented in the following Section 5.2.3.

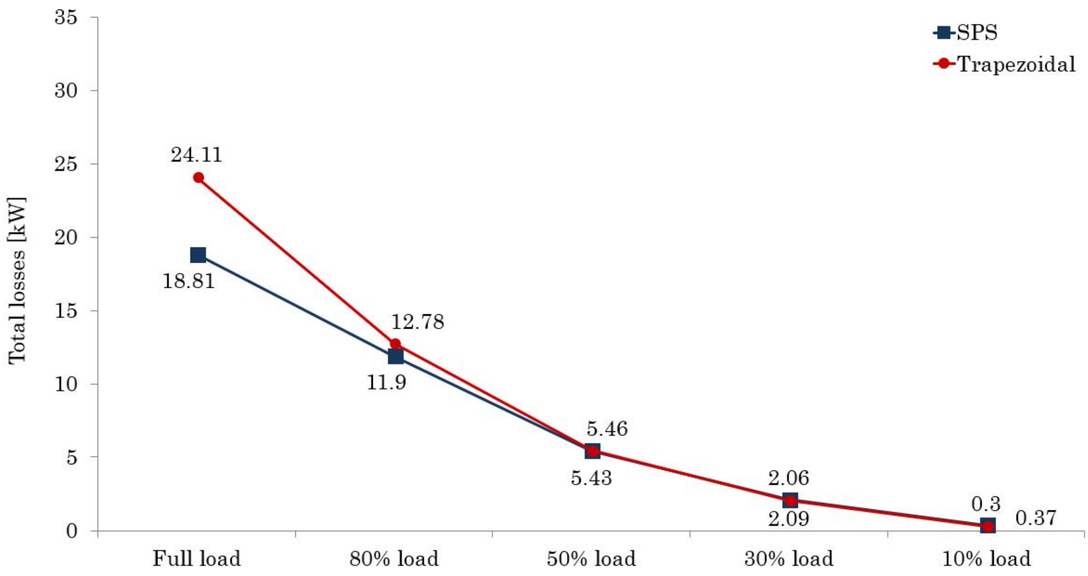



**Figure 5.10:** Total losses at different transmission power levels with $V_o$ = 16 kV and MOSFET switches

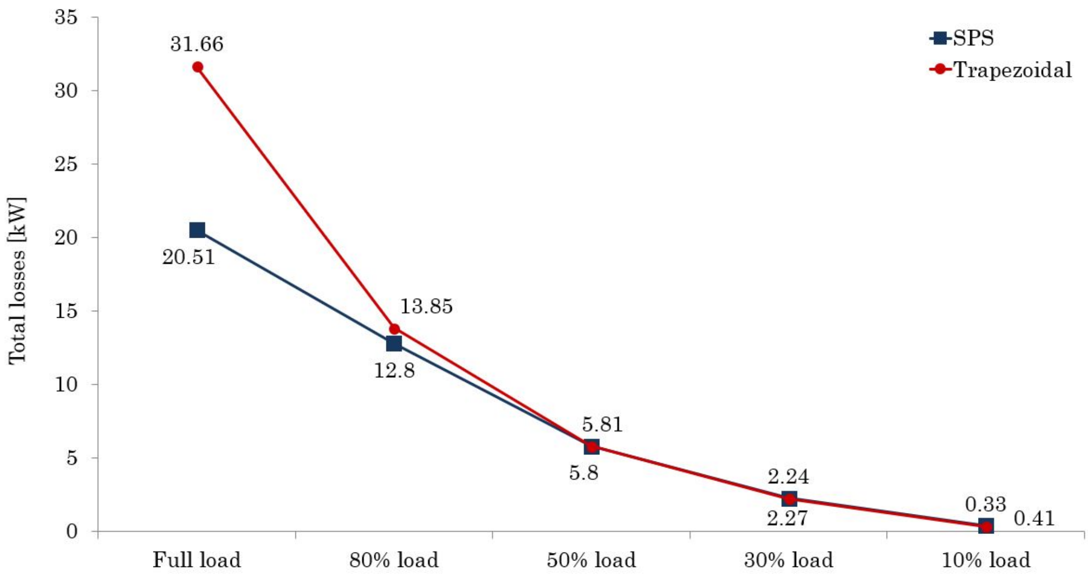



**Figure 5.11:** Total losses at different transmission power levels with $V_o$ = 15.2 kV and MOSFET switches

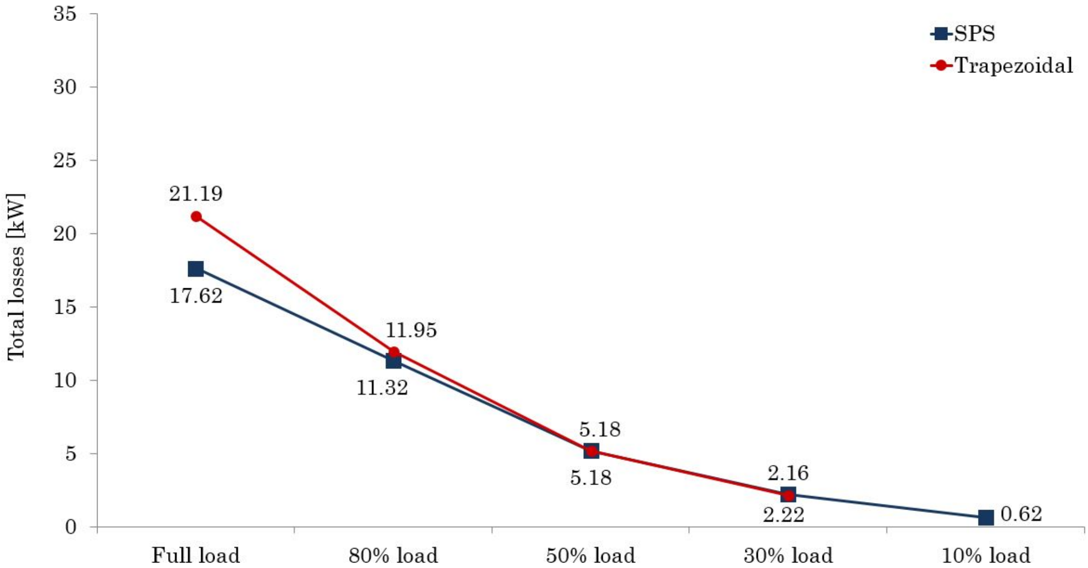



**Figure 5.12:** Total losses at different transmission power levels with $V_o = 16.8$ kV and MOSFET switches

In general, the efficiency of the built up DAB controlled via SPS modulation varies between 97.91 % and 99.62 %, depending on the load and voltage condition. If the control is done by means of the trapezoidal modulation scheme, the efficiency settles between 96.78 % and 99.69 %.

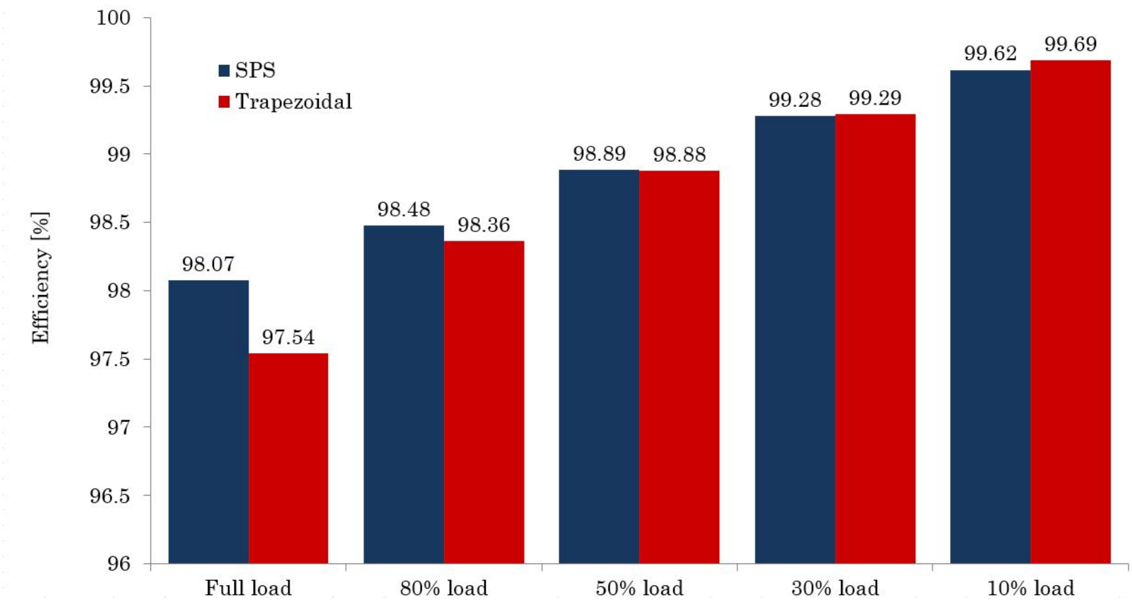



**Figure 5.13:** Efficiency at different transmission power levels with $V_o = 16$ kV and MOSFET switches

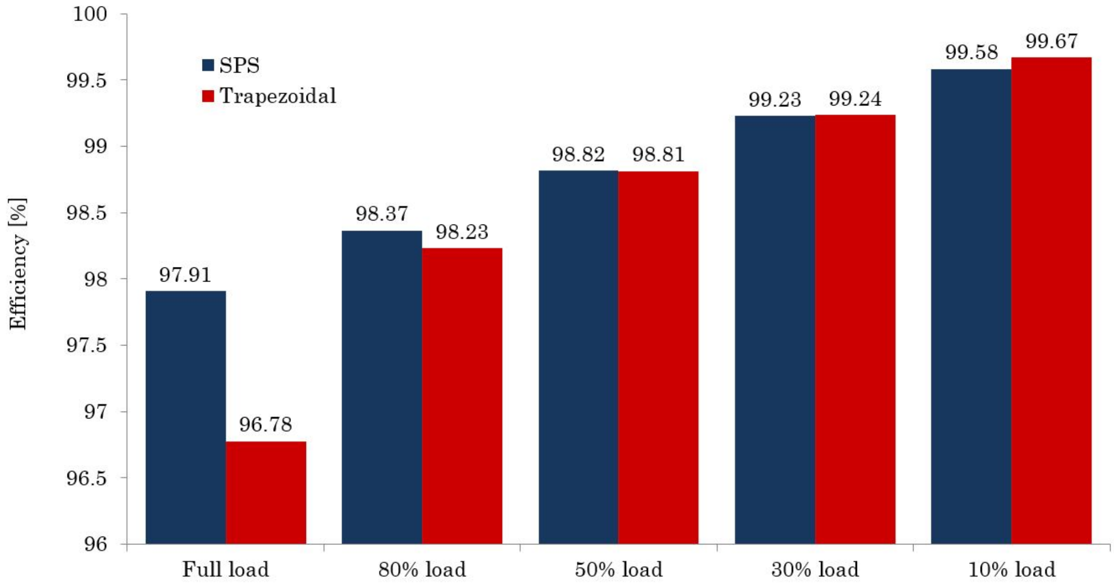



**Figure 5.14:** Efficiency at different transmission power levels with $V_o$ = 15.2 kV and MOSFET switches

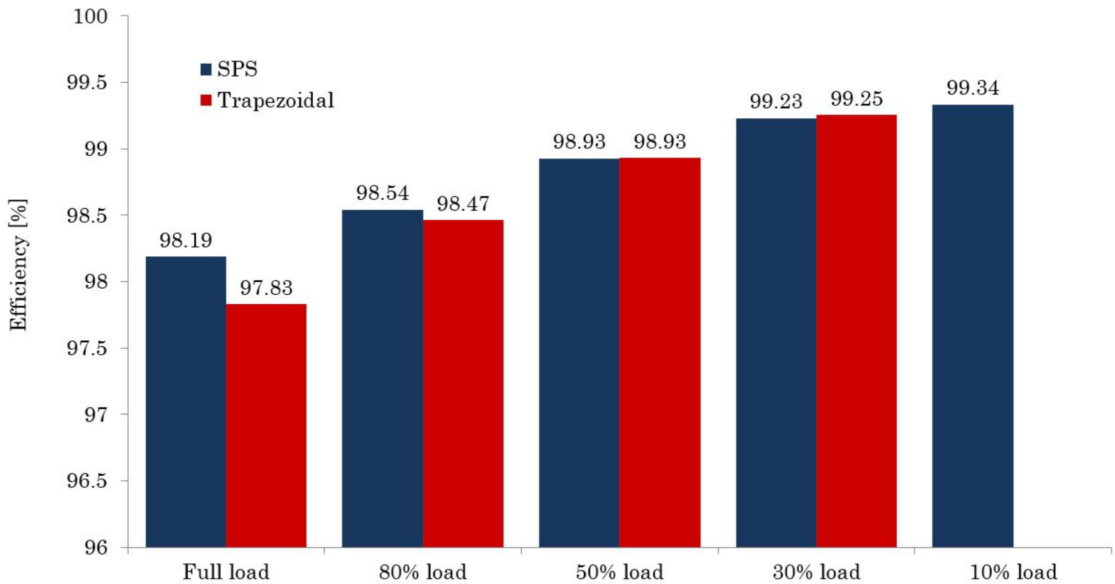



**Figure 5.15:** Efficiency at different transmission power levels with $V_o$ = 16.8 kV and MOSFET switches

### 5.2.3 Share of Switching Losses

Generally, it is visible that the percentile share of switching losses with respect to total losses increases with decreasing load. That is because the current and thereby, the absolute value of conduction losses decreases. Moreover, the SPS modulation and the trapezoidal modulation show different characteristics concerning soft-switching. This was presented in the Sections 3.1.3 and 3.2.3. From these findings, the trapezoidal modulation is expected to exhibit a lower share of switching losses than the SPS modulation. The Figures 5.16 to 5.18 support this assumption. At 50 % of the load, the switching losses with trapezoidal modulation account for only around half of the switching losses in SPS modulation. At 10 % of the load, the trapezoidal switching losses represent around 60 % of the SPS switching losses.

However, this behaviour is reflected in the overall efficiency only at very low loads. At full load and nominal voltage, the absolute value of switching losses is observed to be even higher in trapezoidal than in SPS modulation (compare Figure B.1 and Figure B.2 in Appendix B).

Starting at 80 % towards lighter loads, the absolute value of switching losses is in fact smaller in trapezoidal than in SPS modulation. Yet, it was shown that the RMS inductor current in trapezoidal modulation is always larger than in SPS modulation. This causes the absolute value of the conduction losses to be larger in trapezoidal than in SPS. Hence, the sum of switching and conduction losses results to be larger as well. The effect of lesser switching losses in trapezoidal modulation becomes only visible at very light loads of 30 % or 10 %. Here, the inverted proportions are apparent in the overall efficiency and total losses. These results can be explained by the good switching performance featuring low switching energies exhibited by the chosen SiC MOSFETs.

It should additionally be noted that in the case of single-phase-shift modulation, the Dual-Active-Bridge loses soft-switching capabilities in the case of 10 % of the load when the output voltage is deviating from the nominal value:

- $V_o = 15.2$ kV: HV-side switches loose soft-switching in turn-on
- $V_o = 16.8$ kV: LV-side switches loose soft-switching in turn-on

Moreover, it is noticed that for trapezoidal modulation, only the switch Q6 looses soft-switching in turn-on for $V_o = 15.2$ kV at 10 % of the load. These observations support the choice of the trapezoidal modulation for low loads.

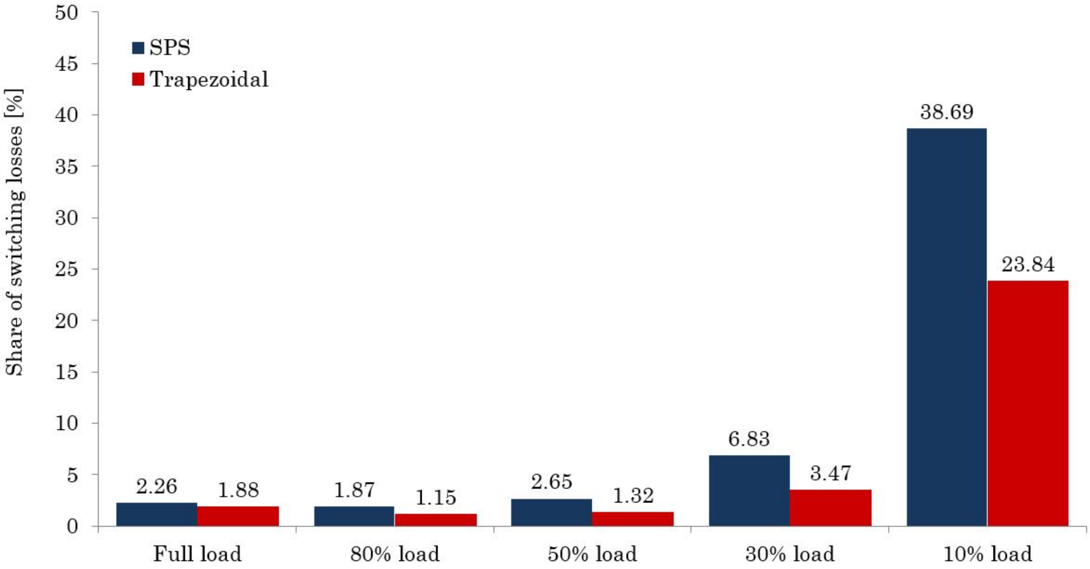



**Figure 5.16:** Percentage share of switching losses at different transmission power levels with $V_o = 16$ kV and MOSFET switches

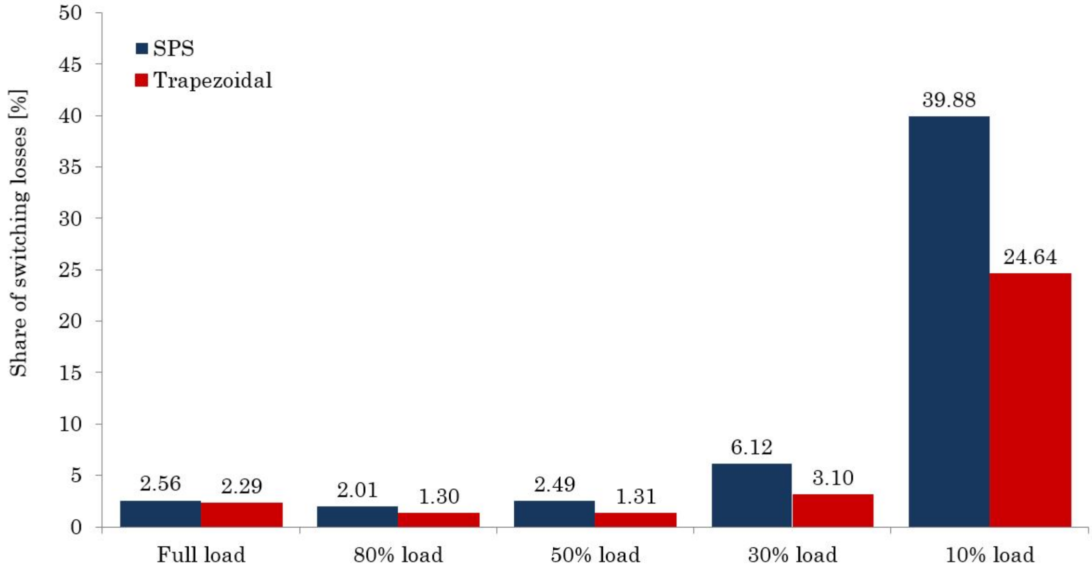



**Figure 5.17:** Percentage share of switching losses at different transmission power levels with $V_o = 15.2$ kV and MOSFET switches

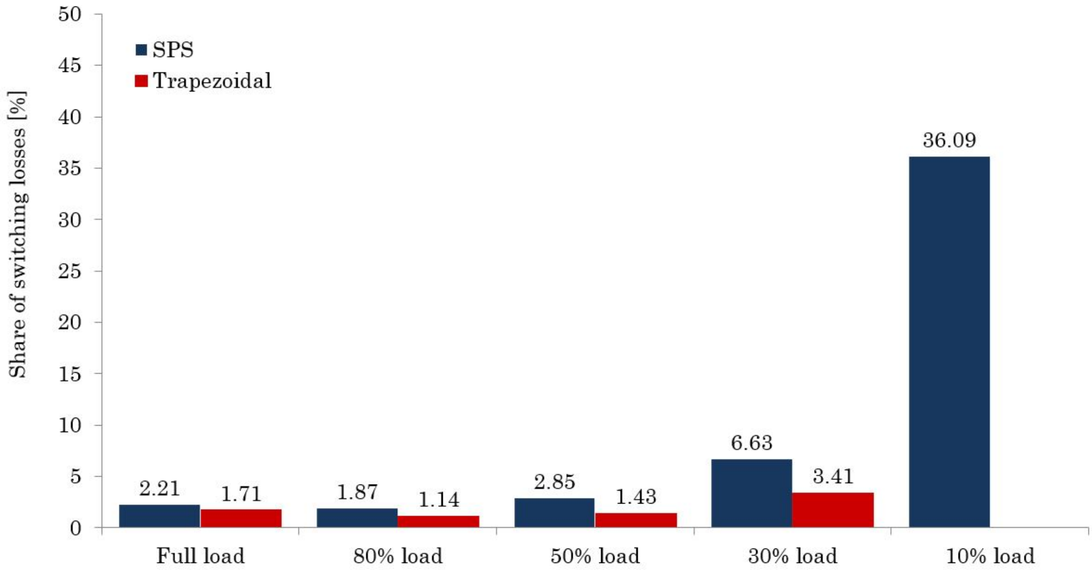



**Figure 5.18:** Percentage share of switching losses at different transmission power levels with $V_o = 16.8$ kV and MOSFET switches

## 5.3 Application of an IGBT Switch

Considering the findings in Section 5.2.3, the model of the Dual-Active-Bridge is re-designed applying a dummy IGBT model based on the IGBT switch IKQ75N120CT2 by Infineon. The IGBT has considerably lower conduction losses, but higher switching energies than the considered MOSFET. It is expected that the effect of lower switching losses in trapezoidal mode will thereby be made more visible in the results. Similarly to the procedure when creating the MOSFET model, a thermal model is built in PLECS®, based on the switching energies that are given in the datasheet in Appendix D. The on-resistance is identified to equal $R_{on} = 27.8$ mH. The anti-parallel diode continues to have the charasteristics of the MOSFET body diode. It has to be noted that this is a simplified approach as the blocking voltage of the used IGBT is lower than the blocking voltage of the employed MOSFET. For a real implementation, the number of switches that are connected in series and parallel might therefore have to be adapted in order to comply with required safety margins for IGBTs.

The course of the primary and secondary transformer voltage and the leakage inductor current is identical to the graphs presented in Section 5.1.

### 5.3.1 RMS Inductor Current

In the following Figures 5.19 to 5.21, the course of the RMS inductor current is presented when the IGBT switch is used. The current shows the same behaviour as with MOSFETs. Solely the values of the current are slightly higher due to the lower ohmic resistance of the IGBTs.

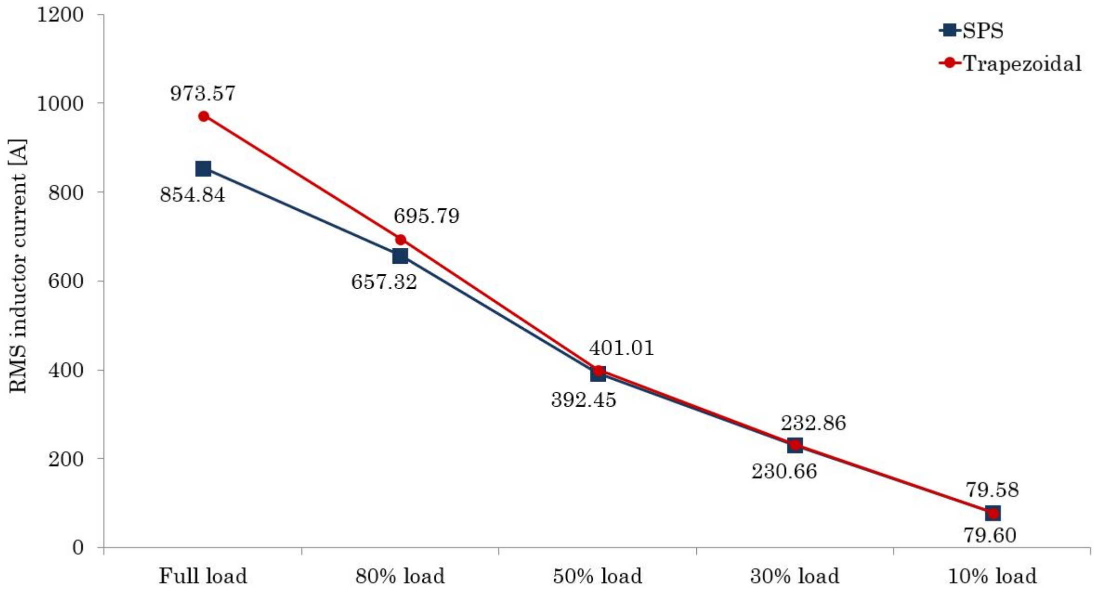



**Figure 5.19:** RMS inductor current at different transmission power levels with $V_o = 16$ kV and IGBT switches

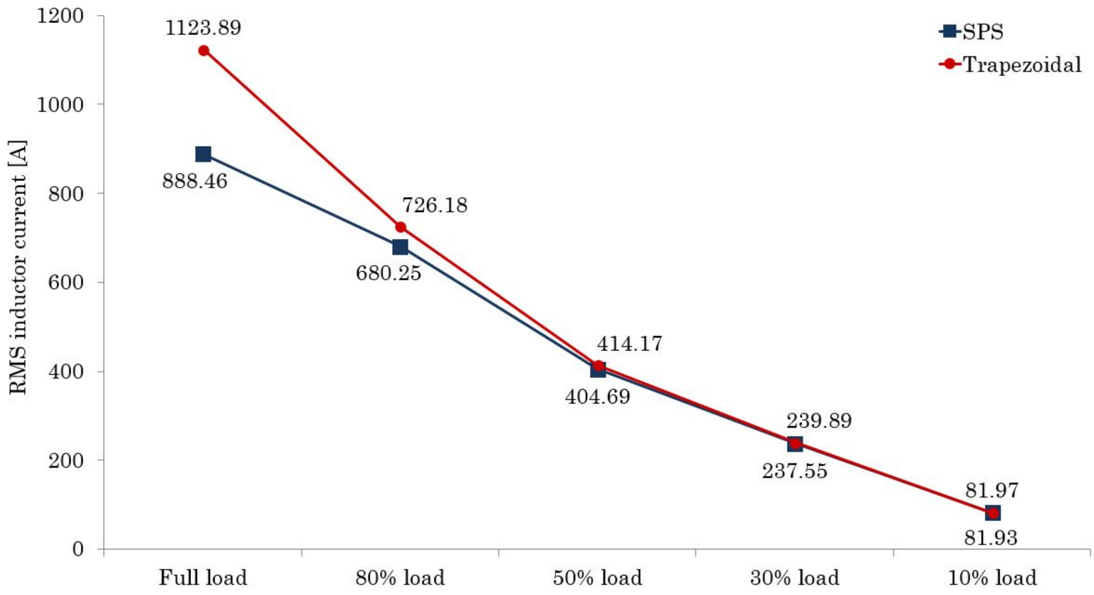



**Figure 5.20:** RMS inductor current at different transmission power levels with $V_o = 15.2$ kV and IGBT switches

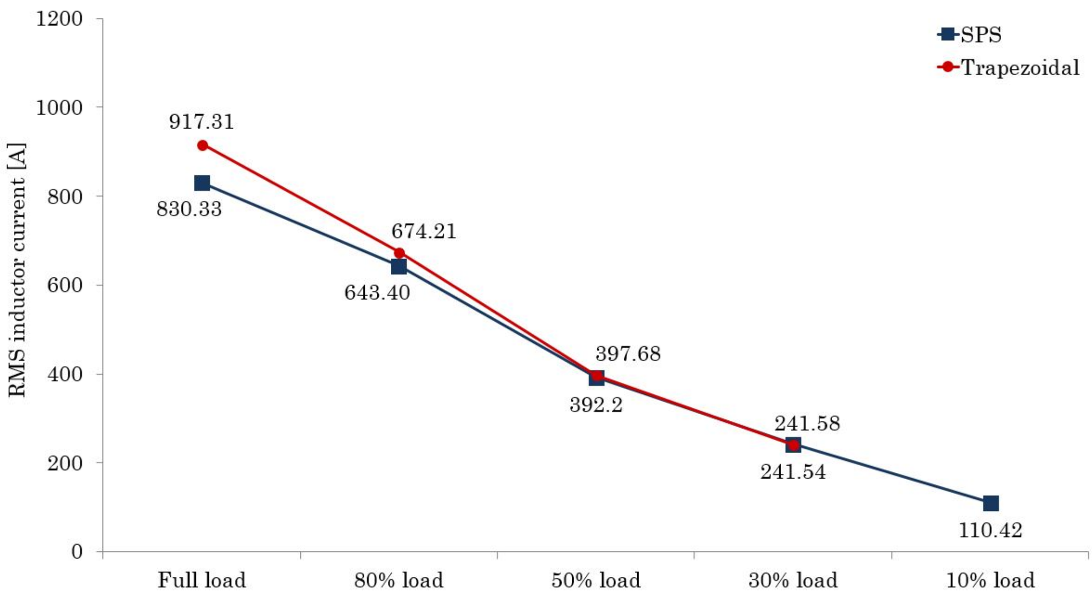



**Figure 5.21:** RMS inductor current at different transmission power levels with $V_o = 16.8$ kV and IGBT switches

### 5.3.2 Total Losses and Efficiency

In the Figures 5.22 to 5.27, the total losses and resulting efficiencies of the Dual-Active-Bridge that is equipped with IGBT switches are presented. It is visible that in comparison with the results of Section 5.2.2, the total losses in trapezoidal modulation are lower than the SPS losses over the whole load range. These results are reasonable considering the better switching performance of the trapezoidal modulation scheme combined with the inverted share of switching and conduction losses with IGBTs. For both modulation schemes, the total losses at low loads are considerably higher when using IGBTs instead of MOSFETs: While the conduction losses are very low due to both the low current and the good conducting behaviour of the IGBTs, the switching losses stay at a comparatively high level (compare Figure B.3 and Figure B.4 in Appendix B).

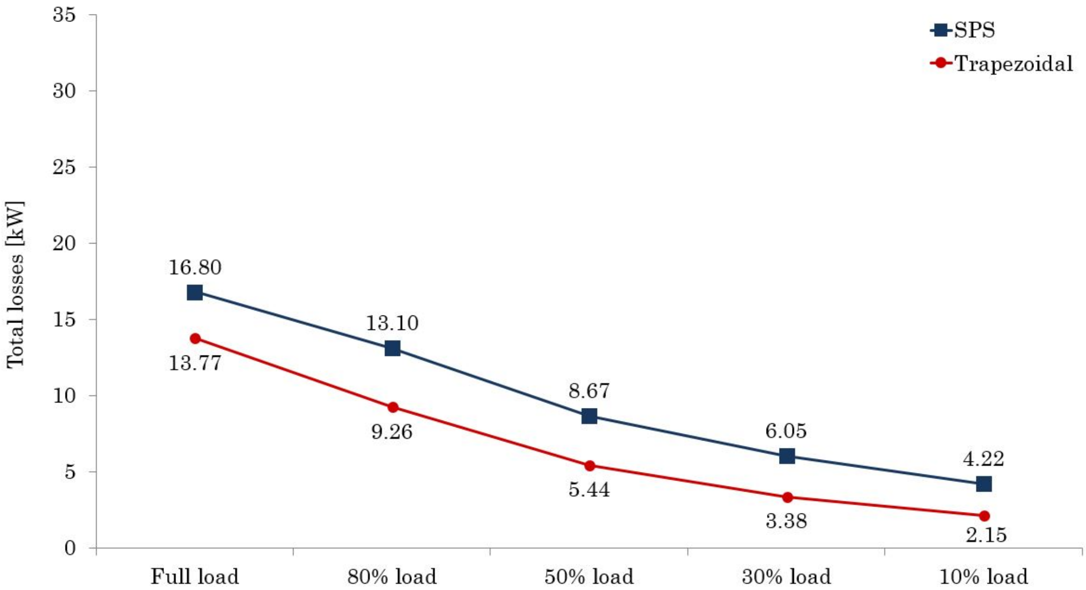



**Figure 5.22:** Total losses at different transmission power levels with $V_o$ = 16 kV and IGBT switches

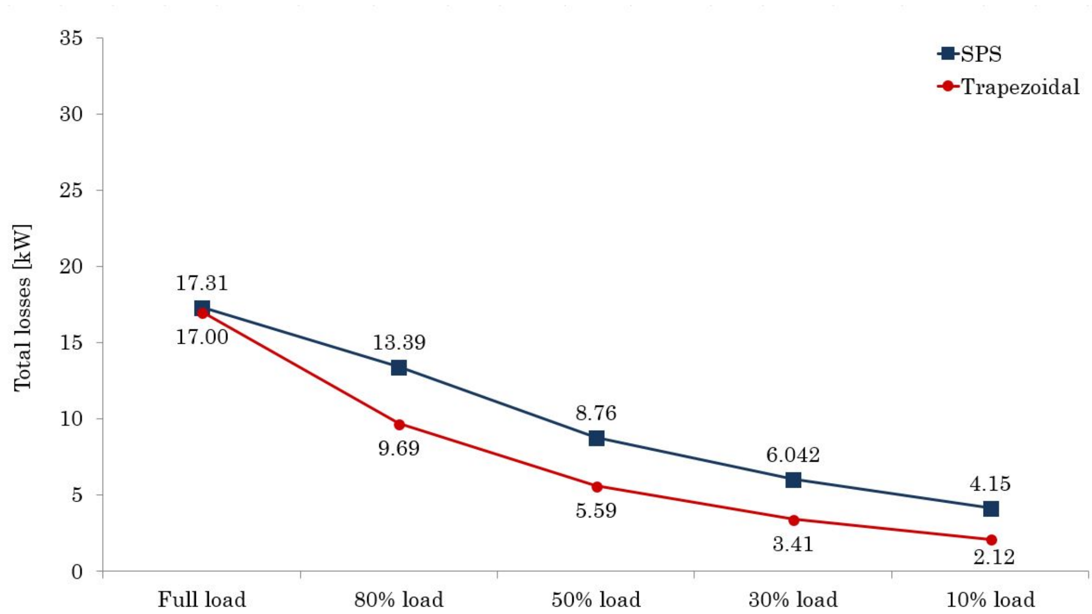



**Figure 5.23:** Total losses at different transmission power levels with $V_o = 15.2$ kV and IGBT switches

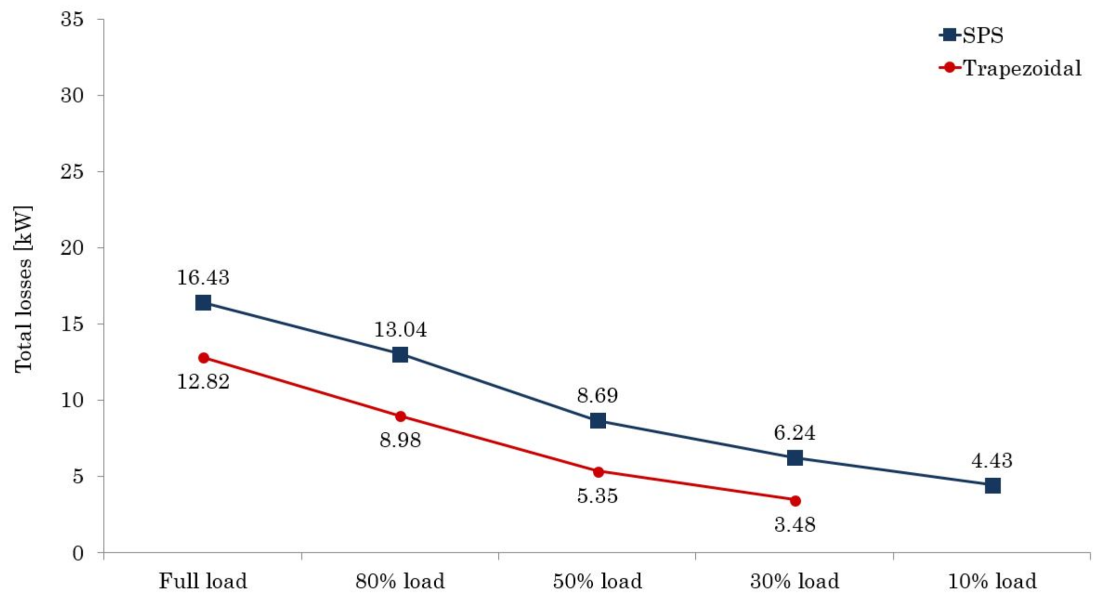



**Figure 5.24:** Total losses at different transmission power levels with $V_o = 16.8$ kV and IGBT switches

In general, the efficiency of the DAB with IGBT switches varies between 95.52 % and 98.33 % with SPS modulation and between 97.81 % and 98.9 % with trapezoidal modulation. The trapezoidal modulation shows better efficiencies than the SPS modulation at all voltage and load levels. An explanation is given in the following Section 5.3.3. It is worth noting that the efficiency does not increase with decreasing load like in the case of MOSFETs.

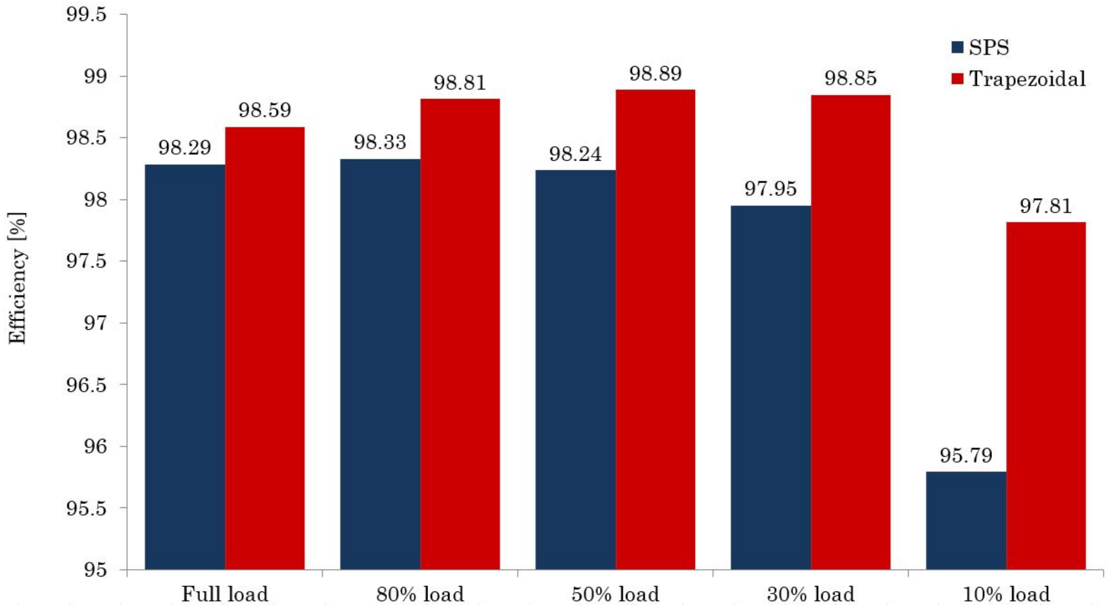



**Figure 5.25:** Efficiency at different transmission power levels with $V_o = 16$ kV and IGBT switches

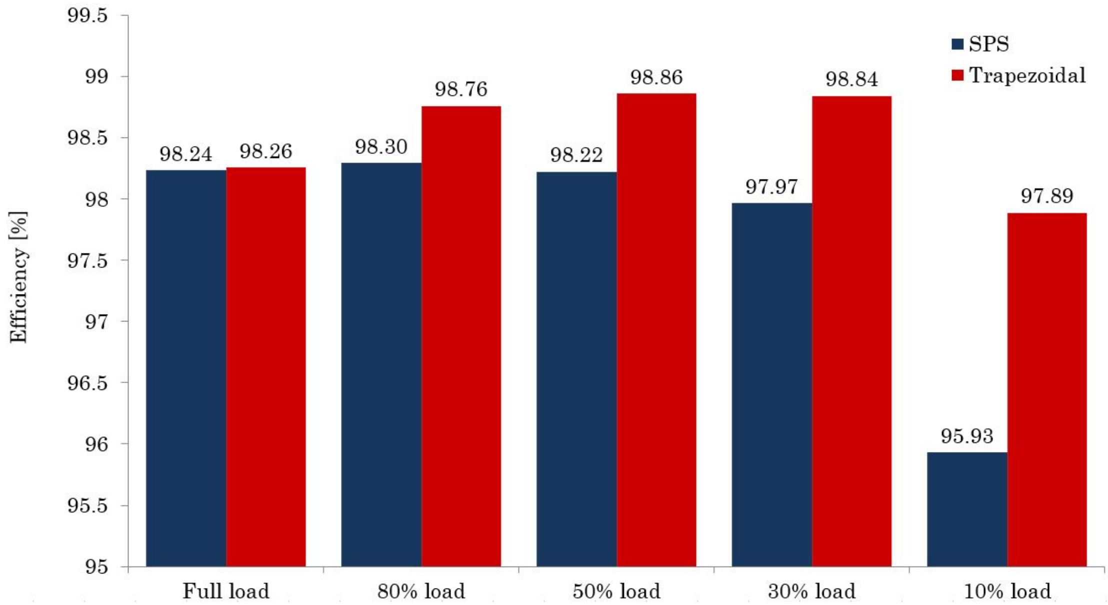



**Figure 5.26:** Efficiency at different transmission power levels with $V_o$ = 15.2 kV and IGBT switches

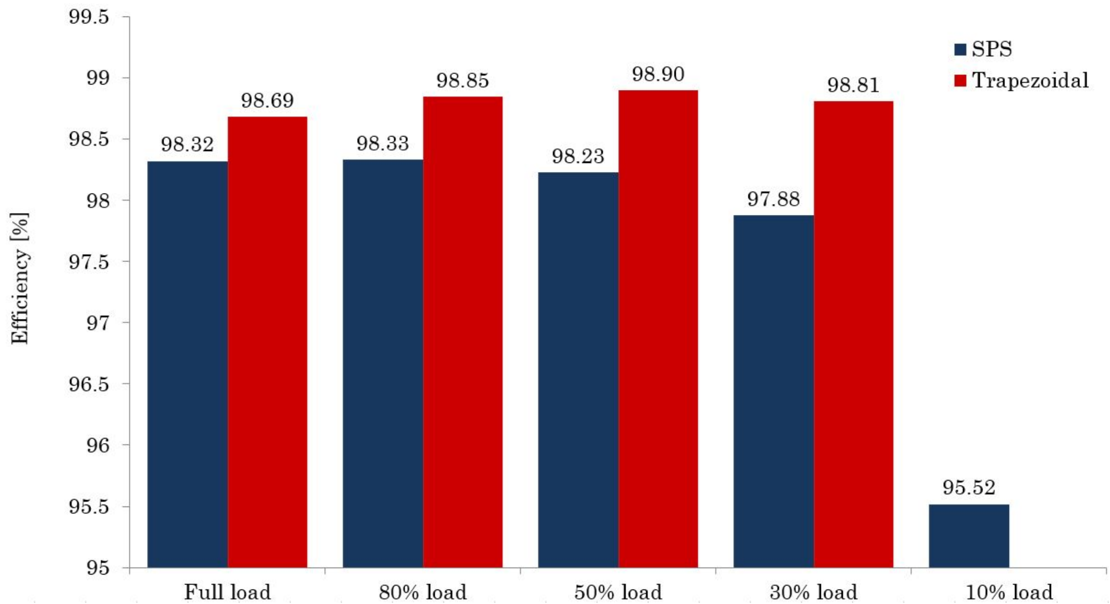



**Figure 5.27:** Efficiency at different transmission power levels with $V_o$ = 16.8 kV and IGBT switches

### 5.3.3 Share of Switching Losses

In general, the following Figures 5.28 to 5.30 show the lower share of switching losses in trapezoidal modulation than in SPS modulation as expected. This is also valid for the absolute switching loss values (compare Figure B.3 and Figure B.4 in Appendix B). Although the absolute value of conduction losses with trapezoidal modulation is still higher than with SPS modulation due to the higher current value, the role of the switching losses is now different. The proportion of switching and conduction losses is inverted when using IGBT switches. Thus, comparing with Figures 5.16 to 5.18, it is obvious that the share of switching losses is clearly larger than in the MOSFET case for both modulation schemes. The effect of the better switching performance of the trapezoidal modulation scheme therefore becomes explicitly visible in the efficiency. Besides, it is notable that soft-switching occurs at all examined voltage and load levels.

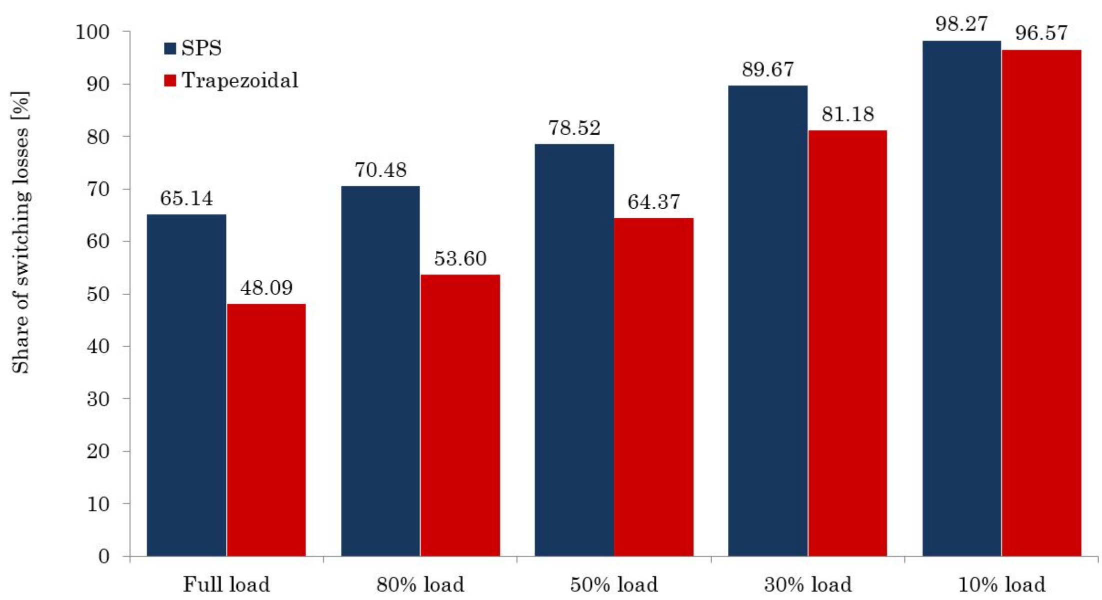



**Figure 5.28:** Percentage share of switching losses at different transmission power levels with $V_o$ = 16 kV and IGBT switches

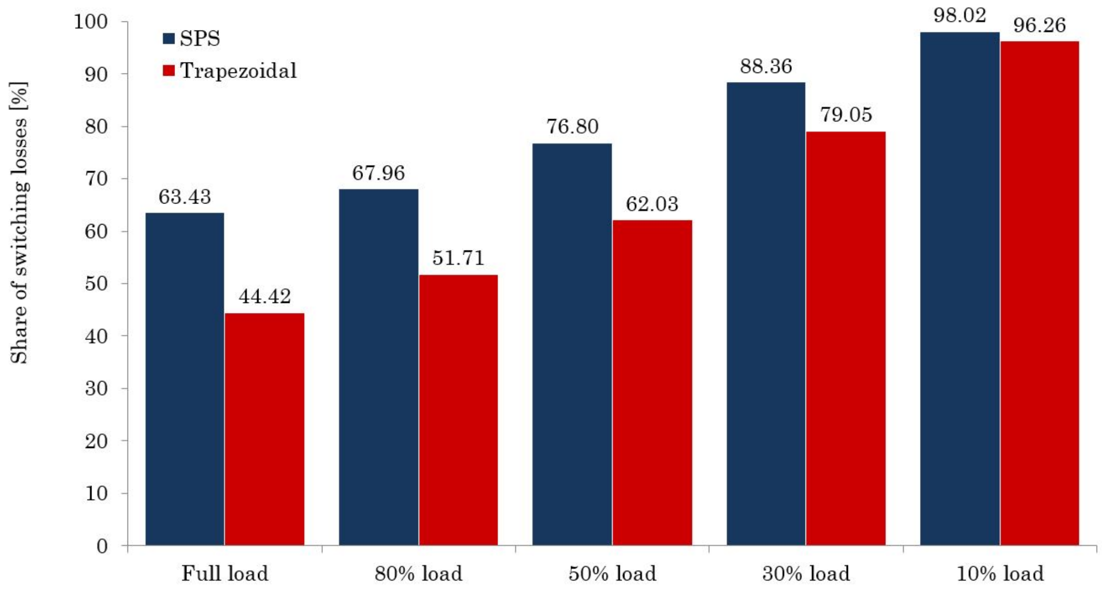



**Figure 5.29:** Percentage share of switching losses at different transmission power levels with $V_o$ = 15.2 kV and IGBT switches

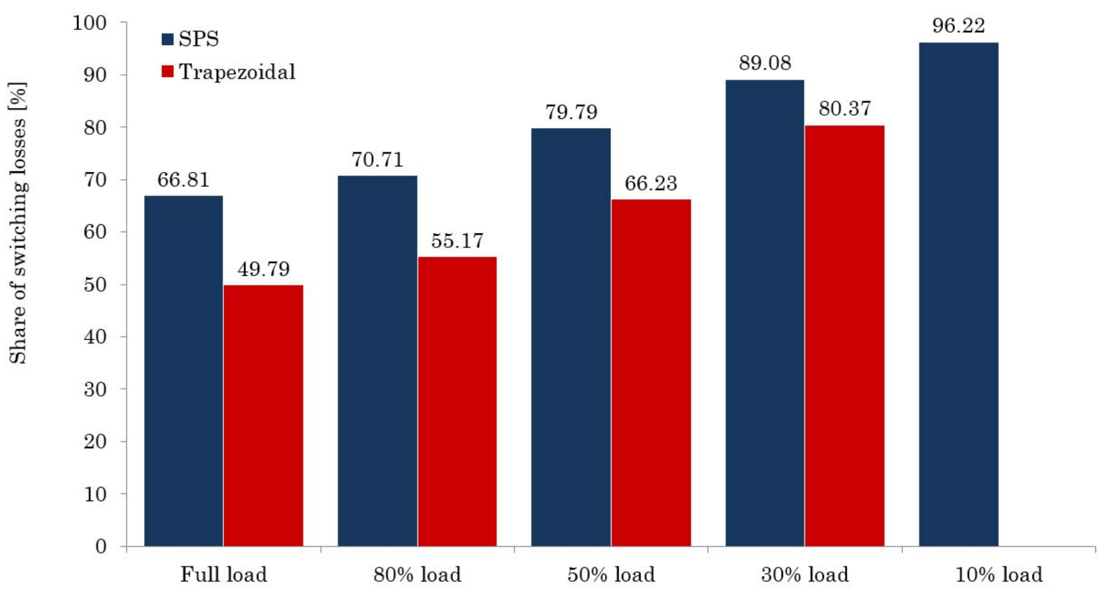



**Figure 5.30:** Percentage share of switching losses at different transmission power levels with $V_o$ = 16.8 kV and IGBT switches

# 6 Conclusion

## 6.1 Round-Up of the Presented Work

In this work, a Dual-Active-Bridge is employed to transfer the generated power from a photovoltaic park to the medium voltage level. Two suitable modulation schemes for this purpose are evaluated. The parameters of the transformer and semiconductor switches were chosen to fit the solar output power of 0.97 MW. The input voltage level $V_i$ is equal to $V_i = 1.3$ kV. The output voltage level $V_o$ varies between the nominal value of $V_o = 16$ kV, $V_o = 15.2$ kV and $V_o = 16.8$ kV which corresponds to a deviation of $\pm 5\,\%$. Other simulation parameters are given in Table 4.1.

The power flow through the Dual-Active-Bridge is chosen to be controlled by either the single-phase-shift modulation scheme or the trapezoidal modulation scheme. From the presented equations in Chapter 3, it is evident that the single-phase-shift modulation features a simpler implementation than the trapezoidal modulation scheme. The single-phase-shift modulation is realized with only one variable, namely the phase-shift angle $\varphi$, and functions identically for all voltage levels. For the trapezoidal modulation scheme, two more variables have to be calculated, namely the zero-voltage widths $\Omega_1$ and $\Omega_2$. Furthermore, two cases have to be differentiated according to the voltage levels.

Due to their good switching performance favorable for a medium switching frequency, SiC MOSFETs were chosen for this simulation. Additionally, a dummy IGBT was created to confirm the obtained results.

Concerning the covered load range, the single-phase-shift modulation is advantageous over the trapezoidal modulation scheme. It can cover the whole load range whereas the trapezoidal modulation has to be combined with the triangular modulation scheme for low loads. Additionally, the single-phase-shift modulation generates lower RMS inductor currents than the trapezoidal modulation at all voltage and load levels.

However, the trapezoidal modulation scheme shows advantages over the single-phase-shift modulation with respect to soft-switching behaviour. While the single-phase-shift modulation exhibits eight softly turned on switches and eight hard turned off switches, the trapezoidal modulation scheme allows for eight softly turned on switches, but has only four hard turned off switches.

When it comes to efficiency, the favoured modulation scheme depends on the chosen switch and load level. In case of a SiC MOSFET switch with low switching losses, the single-phase-shift modulation is favorable over the trapezoidal modulation for loads down to 50 % of full load. At lower loads, the trapezoidal modulation slightly outplays the single-phase-shift modulation due to the lower share of switching losses. In case of the IGBT dummy switch featuring better conduction performance, the trapezoidal modulation is more suitable over the entire load range.

Depending on various parameters like the chosen switches, the load range that has to be covered, the voltage levels and power range in the individual use case, it can be concluded that the single-phase-shift modulation is expected to be more suitable for higher loads and the trapezoidal modulation scheme for medium to low loads. Nevertheless, a “cost-benefit-analysis” between the necessary calculation effort and the improvement of the efficiency should be conducted for every individual use case in order to opt for the optimal modulation scheme.

## 6.2 Future Work

Several measures can be taken for further investigation and improvement of the presented analysis. To fully benefit from the respective advantages, first of all, the triangular modulation should be modeled and added to the simulation. This allows for coverage over the whole load range. After that, an adequate voltage control strategy should be added to the model as was explained in Section 4.2.1. In addition, the transformer is treated as an ideal component in the scope of this work. In order to include transformer losses in the study and to examine possible effects of the different modulation schemes on the transformer parameters, a detailed model of the transformer should be included.

Moreover, some results in [19] and [29] give rise to the assumption that the outcomes concerning the suitability of the modulation techniques might depend on the respective ratios of voltage levels, power levels and resulting currents. Hence, the presented application could be modified to different boundary conditions.

Finally, many more modulation techniques for the Dual-Active-Bridge converter are available in literature. Among these are the dual-phase-shift modulation, the extended-phase-shift modulation, the triple-phase-shift modulation and the optimized modulation method. All these methods vary the phase-shift between the input and output bridge as well as between the two legs of one full-bridge according to different criteria that can be found in the respective literature.

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# A

# PLECS® Modeling

## A.1 Single-Phase-Shift Modulation

### A.1.1 Initialization Parameters for all Voltage Levels

```
% Input Voltage
Vi=1.3e3

% Output Voltage: 16e3 +/- 5% deviation
Vo=16e3

% Switching Frequency
fs=5e3

% Switching Period
Ts=1/fs
Ths=0.5*1/fs

% Triangular Wave
dutycycle=0.5

% Modulation Index
m=0.5

% Transformer
N1=1              % Number of turns on primary side
N2=12             % Number of turns on secondary side
n=N1/N2           % Turns ratio

% MOSFET Series and Parallel Connection
% Ron Value from Data Sheet
Ron_datasheet=45e-3

% LV-side
ns_LV=2
np_LV=15
```

```
% HV-side
ns_HV=15
np_HV=2

% DC Conversion Ratio
d=Vo*n/Vi

% Single-Phase-Shift
Pmax=0.97e6

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% set angle in degrees at which maximum power
% should be transmitted

Phi_SPS_max=60
Phi_SPS_rad_max=Phi_SPS_max/180*pi

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% calculate respective leakage inductance
L_SPS=(Vi*Vo*n)/(2*pi*pi*fs*Pmax)*Phi_SPS_rad_max*
(pi-Phi_SPS_rad_max)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% set power that should be transmitted
% L=L_SPS
L=2.82868e-5
Ptransmit=1*0.97e6
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Calculate respective Phi
% Power transfer function for SPS
a=1
b=-pi
c=(Ptransmit*2*pi*pi*fs*L)/(Vi*Vo*n)

% not applicable
Phi1=1/(2*a)*(-b+sqrt(b*b-4*a*c))

% Varying Values for Phase-Shift depending on given P
Phi2=1/(2*a)*(-b-sqrt(b*b-4*a*c))
Phi_SPS=Phi2/(pi)*180;

% Enter Phase-Shift in Degrees
Phi=Phi_SPS
Phi_rad=(Phi/180)*pi
```

```
D=Phi/180

ph_input=0
ph_output=D*Ths

% Transmission Power and Load
P=Vi*Vo*n/(2*pi*pi*fs*L)*Phi_rad*[pi-(Phi_rad)]
R=(Vo)^2/P
```

## A.2 Trapezoidal Modulation

### A.2.1 Initialization Parameters for $V_i \leq nV_o$

```
% Input Voltage
Vi=1.3e3

% Output Voltage: 16e3 and 16e3 + 5% deviation
Vo=16e3

% Switching Frequency
fs=5e3

% Switching Period
Ts=1/fs
Ths=0.5*1/fs

% Triangular Wave
dutycycle=0.5

% Modulation Index
m=0.5

% Transformer
N1=1              % Number of turns on primary side
N2=12             % Number of turns on secondary side
n=N1/N2           % Turns ratio

% MOSFET Series and Parallel Connection
% Ron Value from Data Sheet
Ron_datasheet=45e-3

% LV-side
ns_LV=2
np_LV=15
```

```
% HV-side
ns_HV=15
np_HV=2

% DC Conversion Ratio
d=Vo*n/Vi

Pmax=0.97e6


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% set angle at which maximum power should be transmitted
Phi_tr_max=60
Phi_tr_rad_max=Phi_tr_max/180*pi
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% calculate respective leakage inductance
Omega1_max=(pi*(Vi-n*Vo)+2*n*Vo*Phi_tr_rad_max)/(2*(Vi+n*Vo))

Omega2_max=Phi_tr_rad_max-Omega1_max

L_Trapez=(n*Vo*(pi-Phi_tr_rad_max-Omega1_max-Omega2_max)*
(n*Vo*(Phi_tr_rad_max-Omega2_max+Omega1_max)+Vi*
(Phi_tr_rad_max-Omega1_max+Omega2_max))+((n*Vo)^2)*
((Phi_tr_rad_max-Omega2_max+Omega1_max)^2))/(4*Pmax*pi*pi*fs)


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% enter power that should be transmitted
Ptransmit=0.3*0.97e6

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Calculate respective Phi, Omega1 and Omega2
% L=L_Trapez
L=2.82868e-5

% Phi calculation according to Schibli
e1=Vi^2+(n*Vo)^2
e2=Vi^2+Vi*n*Vo+(n*Vo)^2
e3=Vi^2*(n*Vo)
```

```
Phi_trapez_rad=pi*(e1/(2*e2)-((Vi+n*Vo)*
(sqrt(e3-4*fs*(Ptransmit/(n*Vo))*L*e2))/(2*(sqrt(Vi))*e2)))

Phi_trapez=Phi_trapez_rad/pi*180

Omega1=(pi*(Vi-n*Vo)+2*n*Vo*Phi_trapez_rad)/(2*(Vi+n*Vo))
Omega2=Phi_trapez_rad-Omega1

Phi=Phi_trapez
Phi_rad=(Phi_trapez/180)*pi

% inner phase-shift of input bridge (duty ratio of vT1)
D1=(1-(2*Omega1/pi))*Ths

% inner phase-shift of output bridge (duty ratio of vT2)
D2=(1-(2*Omega2/pi))*Ths

% Phase-Shift between vT1 and vT2 (outer phase-shift)
D=(2*Omega2/pi)*Ths

% Gate Signals
ph_Q12=0
ph_Q34=ph_Q12+D1

ph_Q56=ph_Q12+D
ph_Q78=ph_Q12+D+D2

% Transmission Power and Load
P=(n*Vo*(pi-Phi_rad-Omega1-Omega2)*
(n*Vo*(Phi_rad-Omega2+Omega1)+Vi*
(Phi_rad-Omega1+Omega2)))/(4*L*pi*pi*fs)+(((n*Vo)^2)*
((Phi_rad-Omega2+Omega1)^2)/(4*L*pi*pi*fs))

R=Vo^2/P
```

### A.2.2 Initialization Parameters for $V_i > nV_o$

```
% Input Voltage
Vi=1.3e3

% Output Voltage: 16e3 - 5% deviation
Vo=15.2e3

% Switching Frequency
fs=5e3

% Switching Period
Ts=1/fs
Ths=0.5*1/fs

% Triangular Wave
dutycycle=0.5

% Modulation Index
m=0.5

% Transformer
N1=1            % Number of turns on primary side
N2=12           % Number of turns on secondary side
n=N1/N2         % Turns ratio

% MOSFET Series and Parallel Connection
% Ron Value from Data Sheet
Ron_datasheet=45e-3

% LV-side
ns_LV=2
np_LV=15

% HV-side
ns_HV=15
np_HV=2

% DC Conversion Ratio
d=Vo*n/Vi

Pmax=0.97e6
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% set angle at which maximum power should be transmitted
Phi_tr_max=60
Phi_tr_rad_max=Phi_tr_max/180*pi
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% calculate respective leakage inductance
Omega2_max=(pi*(n*Vo-Vi)+2*Vi*Phi_tr_rad_max)/(2*(Vi+n*Vo))
Omega1_max=Phi_tr_rad_max-Omega2_max
L_Trapez=(n*Vo*(pi-Phi_tr_rad_max-Omega1_max-Omega2_max)*
(n*Vo*(Phi_tr_rad_max-Omega2_max+Omega1_max)+Vi*
(Phi_tr_rad_max-Omega1_max+Omega2_max))+((n*Vo)^2)*
((Phi_tr_rad_max-Omega2_max+Omega1_max)^2))/(4*Pmax*pi*pi*fs)


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% enter power that should be transmitted
Ptransmit=0.3*0.97e6

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Calculate respective Phi, Omega1 and Omega2
%L=L_Trapez
L=2.82868e-5

% Phi calculation according to Schibli
e1=Vi^2+(n*Vo)^2
e2=Vi^2+Vi*n*Vo+(n*Vo)^2
e3=Vi^2*(n*Vo)

Phi_trapez_rad=pi*(e1/(2*e2)-((Vi+n*Vo)*
(sqrt(e3-4*fs*(Ptransmit/(n*Vo))*L*e2))/(2*(sqrt(Vi))*e2)))
Phi_trapez=Phi_trapez_rad/pi*180

Omega2=(pi*(n*Vo-Vi)+2*Vi*Phi_trapez_rad)/(2*(Vi+n*Vo))
Omega1=Phi_trapez_rad-Omega2

Phi=Phi_trapez
Phi_rad=(Phi_trapez/180)*pi

% inner phase-shift of input bridge (duty ratio of vT1)
D1=(1-(2*Omega1/pi))*Ths
```

```
% inner phase-shift of output bridge (duty ratio of vT2)
D2=(1-(2*Omega2/pi))*Ths

% Phase-Shift between vT1 and vT2 (outer phase-shift)
D=(2*Omega2/pi)*Ths

% Gate Signals
ph_Q12=0
ph_Q34=ph_Q12+D1

ph_Q56=ph_Q12+D
ph_Q78=ph_Q12+D+D2

% Transmission Power and Load
P=(n*Vo*(pi-Phi_rad-Omega1-Omega2)*
(n*Vo*(Phi_rad-Omega2+Omega1)+Vi*
(Phi_rad-Omega1+Omega2)))/(4*L*pi*pi*fs)+(((n*Vo)^2)*
((Phi_rad-Omega2+Omega1)^2)/(4*L*pi*pi*fs))

R=Vo^2/P
```

# B
# Simulation Results

| SPS Modulation | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **16 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 425.713 | 2.262685695 | 222.075 | 1.866756891 | 143.613 | 2.646673436 | 142.896 | 6.827100861 | 142.617 | 38.69027595 |
| Conduction losses [W] | 18388.8 | 97.7373834 | 11674.2 | 98.13303296 | 5282.56 | 97.35338185 | 1950.17 | 93.17270803 | 225.995 | 61.30972405 |
| Total losses [W] | 18814.5 | 100 | 11896.3 | 100 | 5426.17 | 100 | 2093.07 | 100 | 368.612 | 100 |
| Total losses [kW] | 18.8145 | | 11.8963 | | 5.42617 | | 2.09307 | 0.1 | 0.368612 | |
| RMS inductor current [A] | 853.426 | | 656.402 | | 391.96 | | 230.225 | | 78.553 | |
| Peak inductor current [A] | 971.397 | | 747.732 | | 458.742 | | 286.091 | | 120.605 | |
| Efficiency [%] | 98.0732 | | 98.4749 | | 98.8851 | | 99.2804 | | 99.6166 | |
| **15.2 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 525.668 | 2.56315887 | 255.967 | 2.000476738 | 144.638 | 2.49466186 | 138.863 | 6.120170652 | 163.686 | 39.87828409 |
| Conduction losses [W] | 19982.9 | 97.4366851 | 12539.3 | 97.99926536 | 5653.27 | 97.50547612 | 2130.08 | 93.87996157 | 246.778 | 60.12171591 |
| Total losses [W] | 20508.6 | 100 | 12795.3 | 100 | 5797.9 | 100 | 2268.94 | 100 | 410.464 | 100 |
| Total losses [kW] | 20.5086 | | 12.7953 | | 5.7979 | | 2.26894 | | 0.410464 | |
| RMS inductor current [A] | 887.451 | | 679.733 | | 404.58 | | 237.498 | | 81.226 | |
| Peak inductor current [A] | 990.143 | | 756.095 | | 460.684 | | 286.966 | | 121.033 | |
| Efficiency [%] | 97.9077 | | 98.3666 | | 98.8186 | | 99.2276 | | 99.5831 | |
| **16.8 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 389.829 | 2.212473609 | 211.187 | 1.865428271 | 147.687 | 2.851116898 | 146.852 | 6.62707474 | 225.508 | 36.09433171 |
| Conduction losses [W] | 17229.7 | 97.78712343 | 11110 | 98.13534021 | 5032.28 | 97.14882519 | 2069.08 | 93.37256424 | 399.267 | 63.90582835 |
| Total losses [W] | 17619.6 | 100 | 11321.1 | 100 | 5179.97 | 100 | 2215.94 | 100 | 624.774 | 100 |
| Total losses [kW] | 17.6196 | | 11.3211 | | 5.17997 | 0.1 | 2.21594 | | 0.624774 | |
| RMS inductor current [A] | 828.449 | | 641.881 | | 390.703 | | 239.381 | | 103.853 | |
| Peak inductor current [A] | 1028.24 | | 820.699 | | 547.168 | | 379.215 | | 201.9 | |
| Efficiency [%] | 98.1889 | | 98.5424 | | 98.9286 | | 99.2308 | | 99.3351 | |

| | |
|---|---|
| HV side looses soft switching in turn-on | LV side looses soft switching in turn-on |

**Figure B.1:** Simulation results of SPS modulation when the chosen MOSFET switch is used

| Trapezoidal Modulation | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **16 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 453.539 | 1.881522014 | 147.394 | 1.153642654 | 72.0305 | 1.320378935 | 71.4677 | 3.470299746 | 71.323 | 23.83790107 |
| Conduction losses [W] | 23651.4 | 98.11863978 | 12628.9 | 98.84552769 | 5383.26 | 98.67963023 | 1987.98 | 96.53153088 | 227.875 | 76.16143048 |
| Total losses [W] | 24104.9 | 100 | 12776.4 | 100 | 5455.29 | 100 | 2059.41 | 100 | 299.2 | 100 |
| Total losses [kW] | 24.1049 | | 12.7764 | | 5.45529 | | 2.05941 | | 0.2992 | |
| RMS inductor current [A] | 971.878 | | 694.9 | | 400.751 | | 232.495 | | 78.7217 | |
| Peak inductor current [A] | 1236.22 | | 835.206 | | 477.753 | | 290.771 | | 120.995 | |
| Efficiency [%] | 97.5387 | | 98.364 | | 98.88 | | 99.2925 | | 99.6888 | |
| **15.2 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 725.179 | 2.290347542 | 180.673 | 1.304875054 | 76.0188 | 1.309501703 | 69.4182 | 3.10193485 | 81.4319 | 24.6403435 |
| Conduction losses [W] | 30937.2 | 97.70958613 | 13665.3 | 98.69492994 | 5729.17 | 98.69082215 | 2168.48 | 96.89798472 | 249.05 | 75.35962624 |
| Total losses [W] | 31662.4 | 100 | 13846 | 100 | 5805.17 | 100 | 2237.9 | 100 | 330.482 | 100 |
| Total losses [kW] | 31.6624 | | 13.846 | | 5.80517 | | 2.2379 | | 0.330482 | |
| RMS inductor current [A] | 1121.59 | | 725.443 | | 414.025 | | 239.856 | | 81.3457 | |
| Peak inductor current [A] | 1516.27 | | 862.505 | | 482.076 | | 291.823 | | 121.276 | |
| Efficiency [%] | 96.778 | | 98.2317 | | 98.8139 | | 99.2377 | | 99.6693 | |
| **16.8 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 361.687 | 1.707101457 | 136.071 | 1.138507493 | 73.9313 | 1.427584156 | 73.484 | 3.409740525 | n.p. | n.p. |
| Conduction losses [W] | 20825.9 | 98.29472512 | 11815.6 | 98.86124986 | 5104.85 | 98.57263404 | 2081.64 | 96.59044508 | n.p. | n.p. |
| Total losses [W] | 21187.2 | 100 | 11951.7 | 100 | 5178.77 | 100 | 2155.12 | 100 | n.p. | n.p. |
| Total losses [kW] | 21.1872 | | 11.9517 | | 5.17877 | | 2.15512 | | n.p. | n.p. |
| RMS inductor current [A] | 915.533 | | 672.982 | | 396.578 | | 239.898 | | n.p. | n.p. |
| Peak inductor current [A] | 1197.27 | | 876.003 | | 553.768 | | 377.713 | | n.p. | n.p. |
| Efficiency [%] | 97.8307 | | 98.4652 | | 98.9313 | | 99.2535 | | n.p. | n.p. |

Q6 looses soft switching in turn-on

**Figure B.2:** Simulation results of trapezoidal modulation when the chosen MOSFET switch is used

| SPS Modulation | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **16 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 10945.2 | 65.13798049 | 9234.48 | 70.47876359 | 6806.4 | 78.51949952 | 5429.11 | 89.66517861 | 4150.76 | 98.26656376 |
| Conduction losses [W] | 5857.99 | 34.86255512 | 3968.06 | 30.28475482 | 1862.02 | 21.48050048 | 625.759 | 10.33480488 | 73.2178 | 1.733384154 |
| Total losses [W] | 16803.1 | 100 | 13102.5 | 100 | 8668.42 | 100 | 6054.87 | 100 | 4223.98 | 100 |
| Total losses [kW] | 16.8031 | | 13.1025 | | 8.66842 | | 6.05487 | | 4.22398 | |
| RMS inductor current [A] | 854.836 | | 657.323 | | 392.452 | | 230.657 | | 79.6028 | |
| Peak inductor current [A] | 969.85 | | 746.476 | | 458.572 | | 287.237 | | 124.772 | |
| Efficiency [%] | 98.2851 | | 98.3302 | | 98.2364 | | 97.9525 | | 95.7937 | |
| **15.2 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 10979.6 | 63.43216324 | 9101.63 | 67.96064962 | 6727.45 | 76.79939085 | 5338.72 | 88.36043813 | 4063.77 | 98.02444478 |
| Conduction losses [W] | 6329.6 | 36.56783676 | 4290.85 | 32.03920105 | 2032.34 | 23.20083746 | 703.261 | 11.63957842 | 81.9011 | 1.975581752 |
| Total losses [W] | 17309.2 | 100 | 13392.5 | 100 | 8759.77 | 100 | 6041.98 | 100 | 4145.67 | 100 |
| Total losses [kW] | 17.3092 | | 13.3925 | | 8.75977 | | 6.04198 | | 4.14567 | |
| RMS inductor current [A] | 888.462 | | 680.253 | | 404.69 | | 237.55 | | 81.9326 | |
| Peak inductor current [A] | 995.47 | | 760.321 | | 463.746 | | 289.772 | | 125.441 | |
| Efficiency [%] | 98.2368 | | 98.2973 | | 98.2244 | | 97.9687 | | 95.9303 | |
| **16.8 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 10976.1 | 66.80889397 | 9220.94 | 70.70513902 | 6930.47 | 79.78658249 | 5560.48 | 89.08141916 | 4265.59 | 96.22072892 |
| Conduction losses [W] | 5453 | 33.19110603 | 3820.47 | 29.29493766 | 1755.79 | 20.21341751 | 681.542 | 10.91861288 | 167.544 | 3.779361309 |
| Total losses [W] | 16429.1 | 100 | 13041.4 | 100 | 8686.26 | 100 | 6242.02 | 100 | 4433.13 | 100 |
| Total losses [kW] | 16.4291 | | 13.0414 | | 8.68626 | | 6.24202 | | 4.43313 | |
| RMS inductor current [A] | 830.33 | | 643.404 | | 392.198 | | 241.536 | | 110.422 | |
| Peak inductor current [A] | 1028.55 | | 821.644 | | 550.096 | | 385.053 | | 216.158 | |
| Efficiency [%] | 98.32 | | 98.3341 | | 98.2259 | | 97.8771 | | 95.5185 | |

**Figure B.3:** Simulation results of SPS modulation when the chosen IGBT switch is used

| Trapezoidal Modulation | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **16 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 6622.35 | 48.09154485 | 4965.25 | 53.59766319 | 3499.1 | 64.36594276 | 2741.6 | 81.18231969 | 2077.25 | 96.57136216 |
| Conduction losses [W] | 7147.9 | 51.90809205 | 4298.7 | 46.4025527 | 1937.17 | 35.63424119 | 635.416 | 18.81548907 | 73.7516 | 3.428712227 |
| Total losses [W] | 13770.3 | 100 | 9263.93 | 100 | 5436.26 | 100 | 3377.09 | 100 | 2151 | 100 |
| Total losses [kW] | 13.7703 | | 9.26393 | | 5.43626 | | 3.37709 | | 2.151 | |
| RMS inductor current [A] | 973.565 | | 695.792 | | 401.007 | | 232.859 | | 79.5802 | |
| Peak inductor current [A] | 1235.79 | | 834.007 | | 477.274 | | 291.549 | | 123.968 | |
| Efficiency [%] | 98.5883 | | 98.8138 | | 98.8874 | | 98.8483 | | 97.8139 | |
| **15.2 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 7551.98 | 44.4194924 | 5009.41 | 51.71334836 | 3467.29 | 62.03109346 | 2697.64 | 79.0477837 | 2036.02 | 96.25525357 |
| Conduction losses [W] | 9449.53 | 55.58056642 | 4677.51 | 48.28706457 | 2122.31 | 37.96890654 | 715.023 | 20.95201118 | 79.2058 | 3.744547874 |
| Total losses [W] | 17001.5 | 100 | 9686.88 | 100 | 5589.6 | 100 | 3412.67 | 100 | 2115.23 | 100 |
| Total losses [kW] | 17.0015 | | 9.68688 | | 5.5896 | | 3.41267 | | 2.11523 | |
| RMS inductor current [A] | 1123.89 | | 726.179 | | 414.17 | | 239.893 | | 81.9648 | |
| Peak inductor current [A] | 1521.93 | | 866.303 | | 484.71 | | 294.232 | | 125.351 | |
| Efficiency [%] | 98.2581 | | 98.7614 | | 98.8593 | | 98.8422 | | 97.8891 | |
| **16.8 kV** | Full load | | 80% load | | 50% load | | 30% load | | 10% load | |
| | Absolut | % | Absolut | % | Absolut | % | Absolut | % | Absolut | % |
| Switching losses [W] | 6382.37 | 49.79379915 | 4956.12 | 55.16539757 | 3545.77 | 66.22730176 | 2797.09 | 80.37407079 | n.p. | n.p. |
| Conduction losses [W] | 6435.21 | 50.20604481 | 4028.01 | 44.83482504 | 1808.17 | 33.77269824 | 683.006 | 19.62610162 | n.p. | n.p. |
| Total losses [W] | 12817.6 | 100 | 8984.11 | 100 | 5353.94 | 100 | 3480.09 | 100 | n.p. | n.p. |
| Total losses [kW] | 12.8176 | | 8.98411 | | 5.35394 | | 3.48009 | | n.p. | n.p. |
| RMS inductor current [A] | 917.309 | | 674.205 | | 397.677 | | 241.575 | | n.p. | n.p. |
| Peak inductor current [A] | 1197.79 | | 876.015 | | 555.5 | | 382.236 | | n.p. | n.p. |
| Efficiency [%] | 98.6848 | | 98.8479 | | 98.9008 | | 98.8071 | | n.p. | n.p. |

**Figure B.4:** Simulation results of trapezoidal modulation when the chosen IGBT switch is used

# C
# MOSFET Datasheet

CREE

# C2M0045170D

## Silicon Carbide Power MOSFET
## C2M[TM] MOSFET Technology

N-Channel Enhancement Mode

| | |
|---|---|
| $V_{DS}$ | 1700 V |
| $I_D$ @ 25˚C | 72 A |
| $R_{DS(on)}$ | 45 mΩ |

### Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

### Benefits

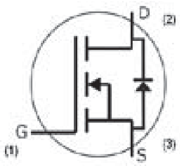
- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

### Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Motor Drive
- Pulsed Power Applications

### Package


TO-247-3




| Part Number | Package | Marking |
|---|---|---|
| C2M0045170D | TO-247-3 | C2M0045170 |

### Maximum Ratings ($T_C$ = 25 ˚C unless otherwise specified)

| Symbol | Parameter | Value | Unit | Test Conditions | Note |
|---|---|---|---|---|---|
| $V_{DSmax}$ | Drain - Source Voltage | 1700 | V | $V_{GS}$ = 0 V, $I_D$ = 100 μA | |
| $V_{GSmax}$ | Gate - Source Voltage | -10/+25 | V | Absolute maximum values, AC (f >1 Hz) | |
| $V_{GSop}$ | Gate - Source Voltage | -5/+20 | V | Recommended operational values | |
| $I_D$ | Continuous Drain Current | 72 | A | $V_{GS}$ =20 V, $T_C$ = 25˚C | Fig. 19 |
| | | 48 | | $V_{GS}$ =20 V, $T_C$ = 100˚C | |
| $I_{D(pulse)}$ | Pulsed Drain Current | 160 | A | Pulse width $t_P$ limited by $T_{jmax}$ | Fig. 22 |
| $P_D$ | Power Dissipation | 520 | W | $T_C$=25˚C, $T_J$ = 150 ˚C | Fig. 20 |
| $T_J$ , $T_{stg}$ | Operating Junction and Storage Temperature | -40 to +150 | ˚C | | |
| $T_L$ | Solder Temperature | 260 | ˚C | 1.6mm (0.063") from case for 10s | |
| $M_d$ | Mounting Torque | 1<br>8.8 | Nm<br>lbf-in | M3 or 6-32 screw | |



CREE

### Electrical Characteristics ($T_C$ = 25˚C unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | 1700 | | | V | $V_{GS}$ = 0 V, $I_D$ = 100 μA | |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | 2.6 | 4 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 18mA | Fig. 11 |
| | | | 1.8 | | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 18mA, $T_J$ = 150 °C | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | | 2 | 100 | μA | $V_{DS}$ = 1700 V, $V_{GS}$ = 0 V | |
| $I_{GSS}$ | Gate-Source Leakage Current | | | 600 | nA | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | |
| $R_{DS(on)}$ | Drain-Source On-State Resistance | | 45 | 70 | mΩ | $V_{GS}$ = 20 V, $I_D$ = 50 A | Fig. 4,5,6 |
| | | | 90 | | | $V_{GS}$ = 20 V, $I_D$ = 50 A, $T_J$ = 150 °C | |
| $g_{fs}$ | Transconductance | | 21.7 | | S | $V_{DS}$= 20 V, $I_{DS}$= 50 A | Fig. 7 |
| | | | 24.4 | | | $V_{DS}$= 20 V, $I_{DS}$= 50 A, $T_J$ = 150 °C | |
| $C_{iss}$ | Input Capacitance | | 3672 | | pF | $V_{GS}$ = 0 V<br>$V_{DS}$ = 1000 V<br>f = 1 MHz<br>$V_{AC}$ = 25 mV | Fig. 17,18 |
| $C_{oss}$ | Output Capacitance | | 171 | | | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | 6.7 | | | | |
| $E_{oss}$ | $C_{oss}$ Stored Energy | | 105 | | μJ | | Fig 16 |
| $E_{ON}$ | Turn-On Switching Energy (SiC Diode FWD) | | 2.1 | | mJ | $V_{DS}$ = 1200 V, $V_{GS}$ = -5/20 V, $I_D$ = 50A, $R_{G(ext)}$ = 2.5Ω, L= 105 μH, $T_J$ = 150 °C, using SiC Diode as FWD | Fig. 26, 29b Note 2 |
| $E_{OFF}$ | Turn Off Switching Energy (SiC Diode FWD) | | 0.86 | | | | |
| $E_{ON}$ | Turn-On Switching Energy (Body Diode FWD) | | 4.7 | | mJ | $V_{DS}$ = 1200 V, $V_{GS}$ = -5/20 V, $I_D$ = 50A, $R_{G(ext)}$ = 2.5Ω, L= 105 μH, $T_J$ = 150 °C, using MOSFET as FWD | Fig. 26, 29a Note 2 |
| $E_{OFF}$ | Turn Off Switching Energy (Body Diode FWD) | | 0.93 | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | | 65 | | ns | $V_{DD}$ = 1200 V, $V_{GS}$ = -5/20 V<br>$I_D$ = 50 A,<br>$R_{G(ext)}$ = 2.5 Ω, Timing relative to $V_{DS}$<br>Inductive load | Fig. 27, 29 Note 2 |
| $t_r$ | Rise Time | | 20 | | | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | 48 | | | | |
| $t_f$ | Fall Time | | 18 | | | | |
| $R_{G(int)}$ | Internal Gate Resistance | | 1.3 | | Ω | f = 1 MHz, $V_{AC}$ = 25 mV | |
| $Q_{gs}$ | Gate to Source Charge | | 44 | | nC | $V_{DS}$ = 1200 V, $V_{GS}$ = -5/20 V<br>$I_D$ = 50 A<br>Per IEC60747-8-4 pg 21 | Fig. 12 |
| $Q_{gd}$ | Gate to Drain Charge | | 57 | | | | |
| $Q_g$ | Total Gate Charge | | 188 | | | | |

### Reverse Diode Characteristics

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Diode Forward Voltage | 4.1 | | V | $V_{GS}$ = - 5 V, $I_{SD}$ = 25 A | Fig. 8, 9, 10 Note 1 |
| | | 3.6 | | V | $V_{GS}$ = - 5 V, $I_{SD}$ = 25 A, $T_J$ = 150 °C | |
| $I_S$ | Continuous Diode Forward Current | | 72 | A | $T_C$= 25 °C, $V_{GS}$ = - 5 V | Note 1 |
| $t_{rr}$ | Reverse Recovery Time | 70 | | ns | $V_{GS}$ = - 5 V, $I_{SD}$ = 50 A , $V_R$ = 1200 V<br>dif/dt = 1400 A/μs | Note 1 |
| $Q_{rr}$ | Reverse Recovery Charge | 530 | | nC | | |
| $I_{rrm}$ | Peak Reverse Recovery Current | 14 | | A | | |

Note (1): When using SiC Body Diode the maximum recommended $V_{GS}$ = -5V

### Thermal Characteristics

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| $R_{θJC}$ | Thermal Resistance from Junction to Case | 0.22 | 0.24 | °C/W | | Fig. 21 |
| $R_{θJC}$ | Thermal Resistance from Junction to Ambient | | 40 | | | |

CREE

## Typical Performance

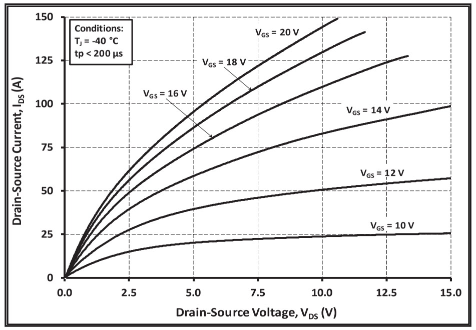



Figure 1. Output Characteristics $T_J$ = -40 °C

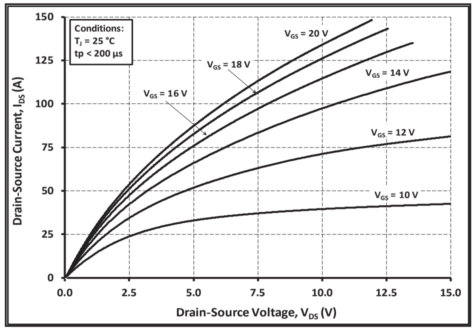



Figure 2. Output Characteristics $T_J$ = 25 °C

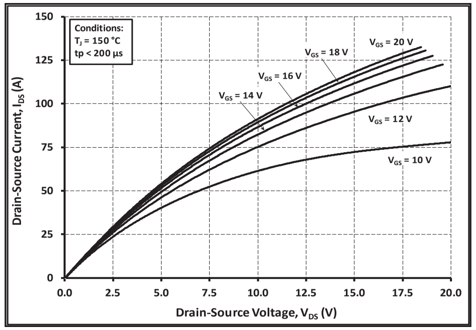



Figure 3. Output Characteristics $T_J$ = 150 °C

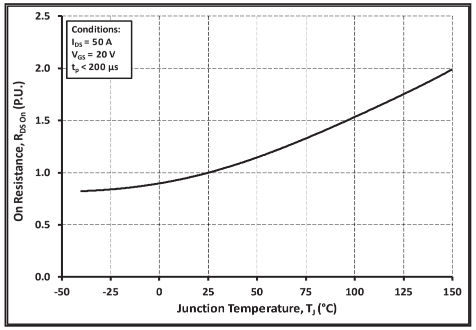



Figure 4. Normalized On-Resistance vs. Temperature

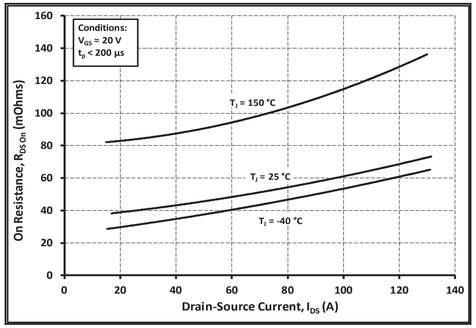



Figure 5. On-Resistance vs. Drain Current For Various Temperatures

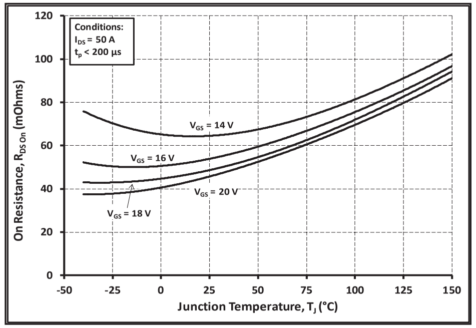



Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



CREE

## Typical Performance

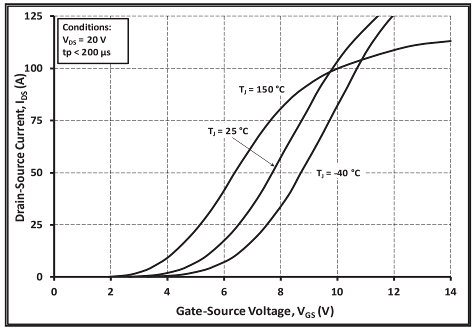



Figure 7. Transfer Characteristic For Various Junction Temperatures

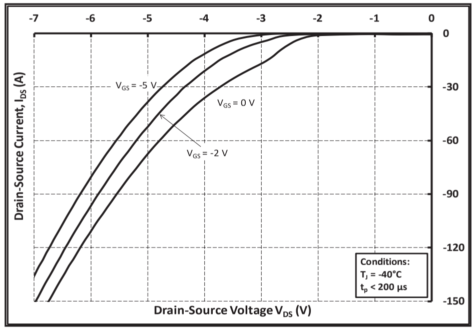



Figure 8. Body Diode Characteristic at -40 °C

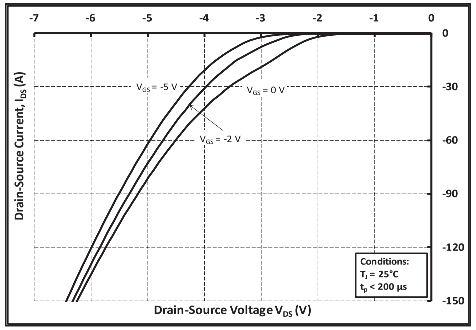



Figure 9. Body Diode Characteristic at 25 °C

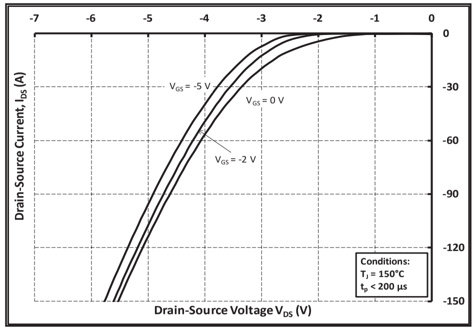



Figure 10. Body Diode Characteristic at 150 °C

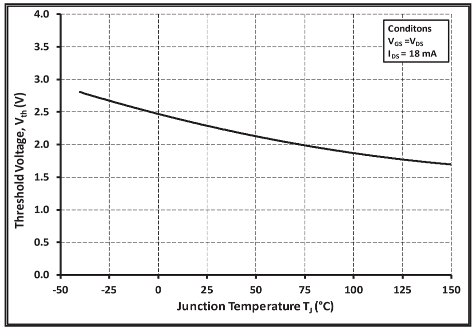



Figure 11. Threshold Voltage vs. Temperature

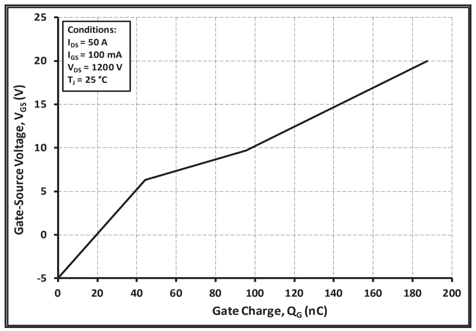



Figure 12. Gate Charge Characteristic

Typical Performance

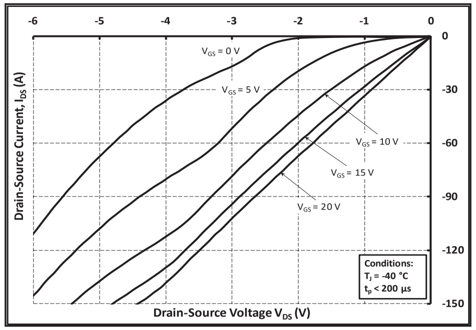



Figure 13. 3rd Quadrant Characteristic at -40 °C

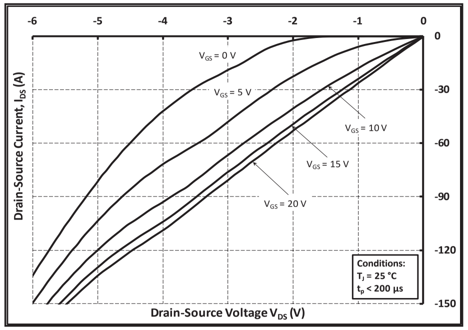



Figure 14. 3rd Quadrant Characteristic at 25 °C

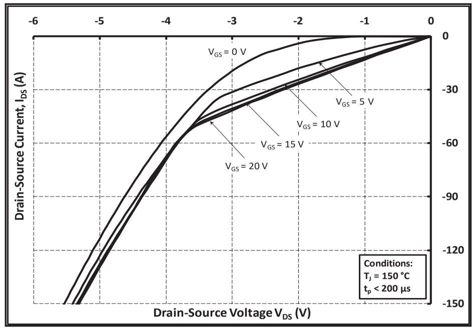



Figure 15. 3rd Quadrant Characteristic at 150 °C

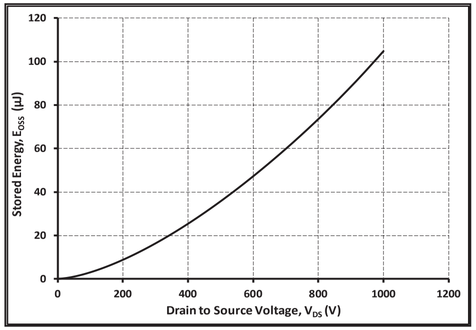



Figure 16. Output Capacitor Stored Energy

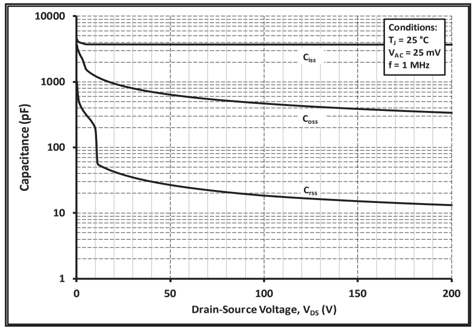



Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

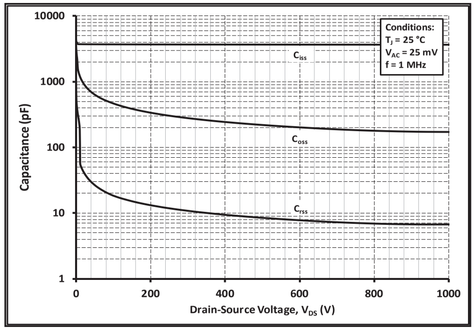



Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)



Typical Performance

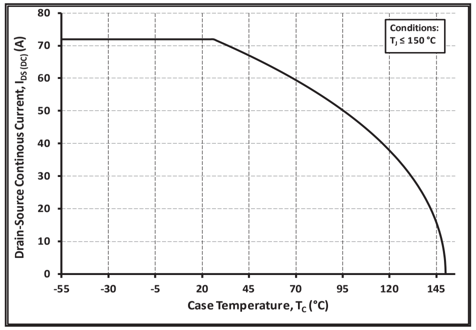



Figure 19. Continuous Drain Current Derating vs. Case Temperature

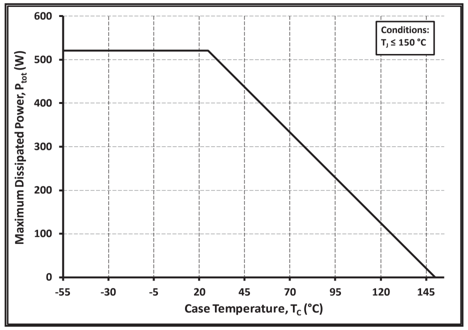



Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

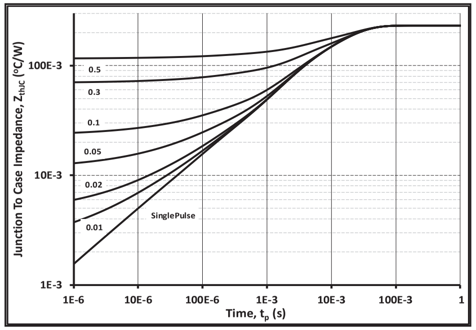



Figure 21. Transient Thermal Impedance (Junction - Case)

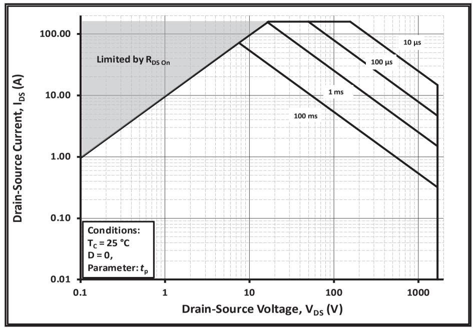



Figure 22. Safe Operating Area

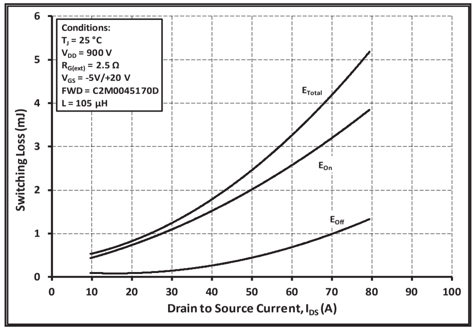



Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD}$ = 900V)

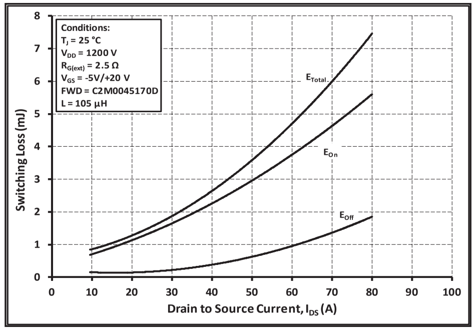



Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD}$ = 1200V)

## Typical Performance

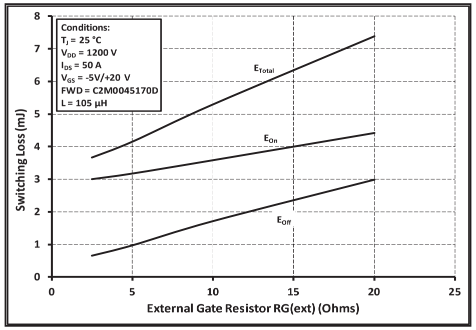



Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

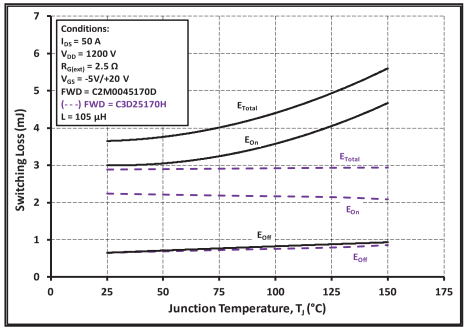



Figure 26. Clamped Inductive Switching Energy vs. Temperature

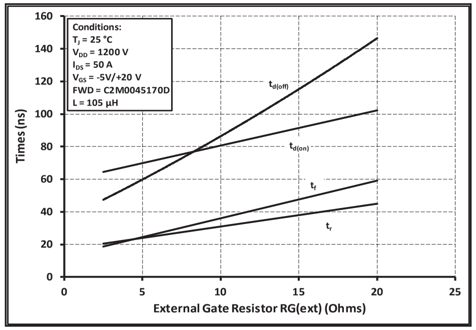



Figure 27. Switching Times vs. $R_{G(ext)}$

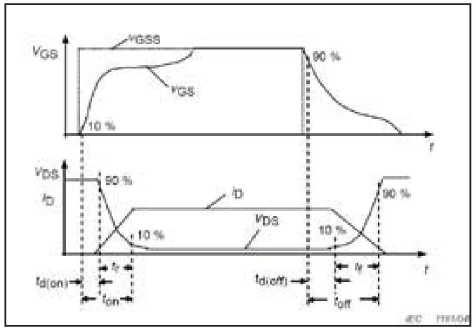



Figure 28. Switching Times Definition

## Test Circuit Schematic

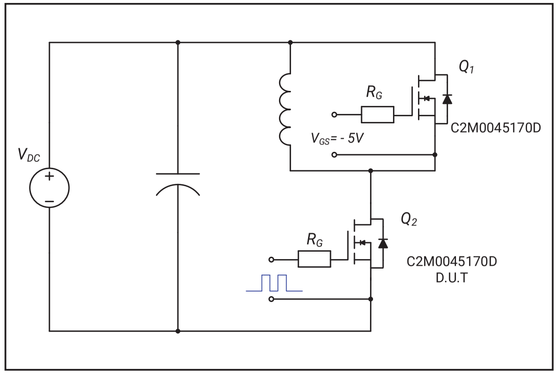



Figure 29a. Clamped Inductive Switching Test Circuit using MOSFET intristic body diode

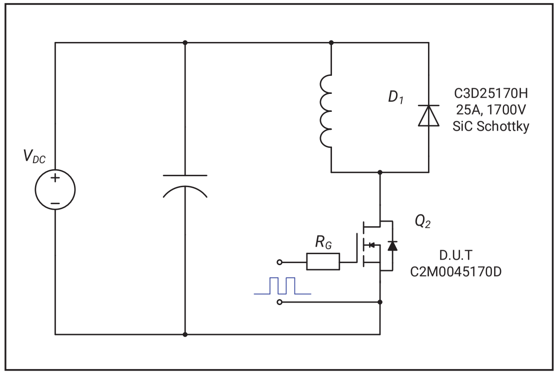


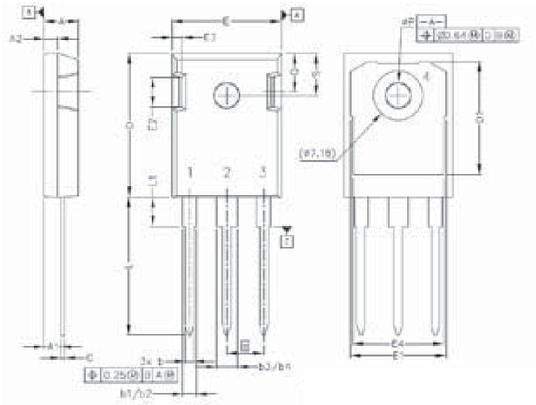

Figure 29b. Clamped Inductive Switching Test Circuit using SiC Schottky diode

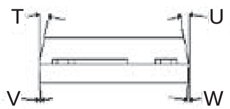
## ESD Ratings

| ESD Test | Total Devices Sampled | Resulting Classification |
|---|---|---|
| ESD-HBM | All Devices Passed 4000V | 3A (>4000V) |
| ESD-CDM | All Devices Passed 1000V | IV (>1000V) |

## Package Dimensions

Package TO-247-3



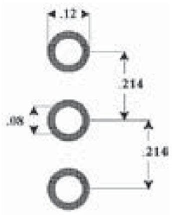



Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

| POS | Inches | | Millimeters | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | .190 | .205 | 4.83 | 5.21 |
| A1 | .090 | .100 | 2.29 | 2.54 |
| A2 | .075 | .085 | 1.91 | 2.16 |
| b | .042 | .052 | 1.07 | 1.33 |
| b1 | .075 | .095 | 1.91 | 2.41 |
| b2 | .075 | .085 | 1.91 | 2.16 |
| b3 | .113 | .133 | 2.87 | 3.38 |
| b4 | .113 | .123 | 2.87 | 3.13 |
| c | .022 | .027 | 0.55 | 0.68 |
| D | .819 | .831 | 20.80 | 21.10 |
| D1 | .640 | .695 | 16.25 | 17.65 |
| D2 | .037 | .049 | 0.95 | 1.25 |
| E | .620 | .635 | 15.75 | 16.13 |
| E1 | .516 | .557 | 13.10 | 14.15 |
| E2 | .145 | .201 | 3.68 | 5.10 |
| E3 | .039 | .075 | 1.00 | 1.90 |
| E4 | .487 | .529 | 12.38 | 13.43 |
| e | .214 BSC | | 5.44 BSC | |
| N | 3 | | 3 | |
| L | .780 | .800 | 19.81 | 20.32 |
| L1 | .161 | .173 | 4.10 | 4.40 |
| ØP | .138 | .144 | 3.51 | 3.65 |
| Q | .216 | .236 | 5.49 | 6.00 |
| S | .238 | .248 | 6.04 | 6.30 |
| T | 9° | 11° | 9° | 11° |
| U | 9° | 11° | 9° | 11° |
| V | 2° | 8° | 2° | 8° |
| W | 2° | 8° | 2° | 8° |

## Recommended Solder Pad Layout




TO-247-3



## Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

## Related Links

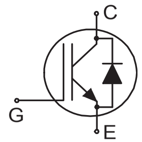
- **C2M PSPICE Models: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Isolated Gate Driver reference design: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support**

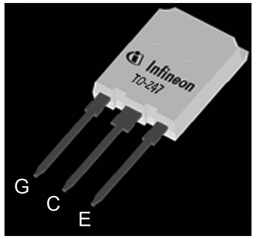


Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5451
www.cree.com/power

# D
# IGBT Datasheet

## Low $V_{ce(sat)}$ IGBT in TRENCHSTOP™ 2 technology copacked with soft, fast recovery full current rated anti-parallel Emitter Controlled Diode




**Features:**

TRENCHSTOP™ 2 technology offers:
- Very low $V_{CE(sat)}$, 1.75V at nominal current
- 10µsec short circuit withstand time at $T_{vj}$=175°C
- Easy paralleling capability due to positive temperature coefficient in $V_{CE(sat)}$
- Low EMI
- Very soft, fast recovery full current anti-parallel diode
- Maximum junction temperature 175°C
- Pb-free lead plating; RoHS compliant
- Complete product spectrum and PSpice Models: http://www.infineon.com/igbt

**Applications:**

- GPD (General Purpose Drives)
- Servo Drives
- Commercial Vehicles
- Agricultural Vehicles
- Three-level Solar String Inverter
- Welding

**Product Validation:**

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

**Key Performance and Package Parameters**

| Type | $V_{CE}$ | $I_C$ | $V_{CEsat}$, $T_{vj}$=25°C | $T_{vjmax}$ | Marking | Package |
|---|---|---|---|---|---|---|
| IKQ75N120CT2 | 1200V | 75A | 1.75V | 175°C | K75MCT2 | PG-TO247-3-46 |





**Table of Contents**

### Maximum Ratings

For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Collector-emitter voltage, $T_{vj} \geq 25°C$ | $V_{CE}$ | 1200 | V |
| DC collector current, limited by $T_{vjmax}$<br>$T_C$ = 25°C value limited by bondwire<br>$T_C$ = 137°C | $I_C$ | 150.0<br>75.0 | A |
| Pulsed collector current, $t_p$ limited by $T_{vjmax}$ | $I_{Cpuls}$ | 300.0 | A |
| Turn off safe operating area<br>$V_{CE} \leq 1200V$, $T_{vj} \leq 175°C$, $t_p = 1µs$ | - | 300.0 | A |
| Diode forward current, limited by $T_{vjmax}$<br>$T_C$ = 25°C value limited by bondwire<br>$T_C$ = 100°C | $I_F$ | 150.0<br>75.0 | A |
| Diode pulsed current, $t_p$ limited by $T_{vjmax}$ | $I_{Fpuls}$ | 300.0 | A |
| Gate-emitter voltage | $V_{GE}$ | ±20 | V |
| Short circuit withstand time<br>$V_{GE}$ = 15.0V, $V_{CC} \leq 600V$<br>Allowed number of short circuits < 1000<br>Time between short circuits: ≥ 1.0s<br>$T_{vj}$ = 175°C | $t_{SC}$ | 10 | µs |
| Power dissipation $T_C$ = 25°C<br>Power dissipation $T_C$ = 137°C | $P_{tot}$ | 938.0<br>237.0 | W |
| Operating junction temperature | $T_{vj}$ | -40...+175 | °C |
| Storage temperature | $T_{stg}$ | -55...+150 | °C |
| Soldering temperature,<br>wave soldering 1.6mm (0.063in.) from case for 10s | | 260 | °C |

### Thermal Resistance

| Parameter | Symbol | Conditions | Value min. | Value typ. | Value max. | Unit |
|---|---|---|---|---|---|---|
| **$R_{th}$ Characteristics** | | | | | | |
| IGBT thermal resistance,[1]<br>junction - case | $R_{th(j-C)}$ | | - | - | 0.16 | K/W |
| Diode thermal resistance,[1]<br>junction - case | $R_{th(j-C)}$ | | - | - | 0.28 | K/W |
| Thermal resistance<br>junction - ambient | $R_{th(j-a)}$ | | - | - | 40 | K/W |

[1] Thermal resistance of thermal grease $R_{th(c-s)}$ (case to heat sink) of more than 0.1K/W not included.





### Electrical Characteristic, at $T_{vj}$ = 25°C, unless otherwise specified

| Parameter | Symbol | Conditions | Value min. | Value typ. | Value max. | Unit |
|---|---|---|---|---|---|---|
| **Static Characteristic** | | | | | | |
| Collector-emitter breakdown voltage | $V_{(BR)CES}$ | $V_{GE}$ = 0V, $I_C$ = 0.50mA | 1200 | - | - | V |
| Collector-emitter saturation voltage | $V_{CEsat}$ | $V_{GE}$ = 15.0V, $I_C$ = 75.0A<br>$T_{vj}$ = 25°C<br>$T_{vj}$ = 175°C | -<br>- | 1.75<br>2.30 | 2.15<br>- | V |
| Diode forward voltage | $V_F$ | $V_{GE}$ = 0V, $I_F$ = 75.0A<br>$T_{vj}$ = 25°C<br>$T_{vj}$ = 175°C | -<br>- | 1.90<br>1.85 | 2.30<br>- | V |
| Gate-emitter threshold voltage | $V_{GE(th)}$ | $I_C$ = 1.88mA, $V_{CE}$ = $V_{GE}$ | 5.1 | 5.8 | 6.5 | V |
| Zero gate voltage collector current | $I_{CES}$ | $V_{CE}$ = 1200V, $V_{GE}$ = 0V<br>$T_{vj}$ = 25°C<br>$T_{vj}$ = 150°C<br>$T_{vj}$ = 175°C | -<br>- | -<br>-<br>5000 | 450<br>-<br>- | µA |
| Gate-emitter leakage current | $I_{GES}$ | $V_{CE}$ = 0V, $V_{GE}$ = 20V | - | - | 100 | nA |
| Transconductance | $g_{fs}$ | $V_{CE}$ = 20V, $I_C$ = 75.0A | - | 27.0 | - | S |

### Electrical Characteristic, at $T_{vj}$ = 25°C, unless otherwise specified

| Parameter | Symbol | Conditions | Value min. | Value typ. | Value max. | Unit |
|---|---|---|---|---|---|---|
| **Dynamic Characteristic** | | | | | | |
| Input capacitance | $C_{ies}$ | $V_{CE}$ = 25V, $V_{GE}$ = 0V, f = 1MHz | - | 4856 | - | pF |
| Output capacitance | $C_{oes}$ | | - | 505 | - | |
| Reverse transfer capacitance | $C_{res}$ | | - | 290 | - | |
| Gate charge | $Q_G$ | $V_{CC}$ = 960V, $I_C$ = 75.0A,<br>$V_{GE}$ = 15V | - | 370.0 | - | nC |
| Internal emitter inductance measured 5mm (0.197 in.) from case | $L_E$ | | - | 13.0 | - | nH |

### Switching Characteristic, Inductive Load

| Parameter | Symbol | Conditions | Value min. | Value typ. | Value max. | Unit |
|---|---|---|---|---|---|---|
| **IGBT Characteristic, at $T_{vj}$ = 25°C** | | | | | | |
| Turn-on delay time | $t_{d(on)}$ | $T_{vj}$ = 25°C,<br>$V_{CC}$ = 600V, $I_C$ = 75.0A,<br>$V_{GE}$ = 0.0/15.0V,<br>$R_{G(on)}$ = 6.0Ω, $R_{G(off)}$ = 6.0Ω,<br>$L\sigma$ = 90nH, $C\sigma$ = 67pF<br>$L\sigma$, $C\sigma$ from Fig. E<br>Energy losses include "tail" and diode reverse recovery. | - | 37 | - | ns |
| Rise time | $t_r$ | | - | 49 | - | ns |
| Turn-off delay time | $t_{d(off)}$ | | - | 326 | - | ns |
| Fall time | $t_f$ | | - | 46 | - | ns |
| Turn-on energy | $E_{on}$ | | - | 6.70 | - | mJ |
| Turn-off energy | $E_{off}$ | | - | 4.10 | - | mJ |
| Total switching energy | $E_{ts}$ | | - | 10.80 | - | mJ |

**Diode Characteristic, at $T_{vj}$ = 25°C**

| | | | | | | |
|---|---|---|---|---|---|---|
| Diode reverse recovery time | $t_{rr}$ | $T_{vj}$ = 25°C, $V_R$ = 600V, $I_F$ = 75.0A, $di_F/dt$ = 800A/µs | - | 320 | - | ns |
| Diode reverse recovery charge | $Q_{rr}$ | | - | 5.10 | - | µC |
| Diode peak reverse recovery current | $I_{rrm}$ | | - | 29.0 | - | A |
| Diode peak rate of fall of reverse recovery current during $t_b$ | $di_{rr}/dt$ | | - | -300 | - | A/µs |

**Switching Characteristic, Inductive Load**

| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **IGBT Characteristic, at $T_{vj}$ = 175°C** | | | | | | |
| Turn-on delay time | $t_{d(on)}$ | $T_{vj}$ = 175°C, $V_{CC}$ = 600V, $I_C$ = 75.0A, $V_{GE}$ = 0.0/15.0V, $R_{G(on)}$ = 6.0Ω, $R_{G(off)}$ = 6.0Ω, $L\sigma$ = 90nH, $C\sigma$ = 67pF $L\sigma$, $C\sigma$ from Fig. E Energy losses include “tail” and diode reverse recovery. | - | 35 | - | ns |
| Rise time | $t_r$ | | - | 50 | - | ns |
| Turn-off delay time | $t_{d(off)}$ | | - | 460 | - | ns |
| Fall time | $t_f$ | | - | 103 | - | ns |
| Turn-on energy | $E_{on}$ | | - | 10.30 | - | mJ |
| Turn-off energy | $E_{off}$ | | - | 9.10 | - | mJ |
| Total switching energy | $E_{ts}$ | | - | 19.40 | - | mJ |

**Diode Characteristic, at $T_{vj}$ = 175°C**

| | | | | | | |
|---|---|---|---|---|---|---|
| Diode reverse recovery time | $t_{rr}$ | $T_{vj}$ = 175°C, $V_R$ = 600V, $I_F$ = 75.0A, $di_F/dt$ = 800A/µs | - | 600 | - | ns |
| Diode reverse recovery charge | $Q_{rr}$ | | - | 13.30 | - | µC |
| Diode peak reverse recovery current | $I_{rrm}$ | | - | 42.0 | - | A |
| Diode peak rate of fall of reverse recovery current during $t_b$ | $di_{rr}/dt$ | | - | -125 | - | A/µs |





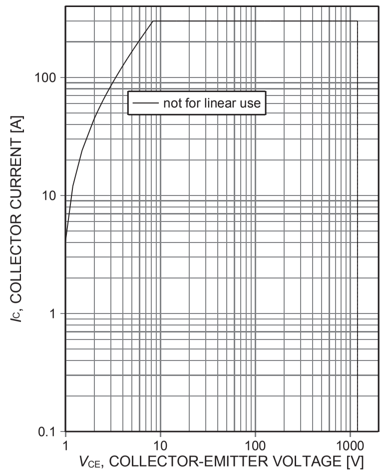



Figure 1. **Forward bias safe operating area**
($D$=0, $T_C$=25°C, $T_{vj}$≤175°C; $V_{GE}$=15V)

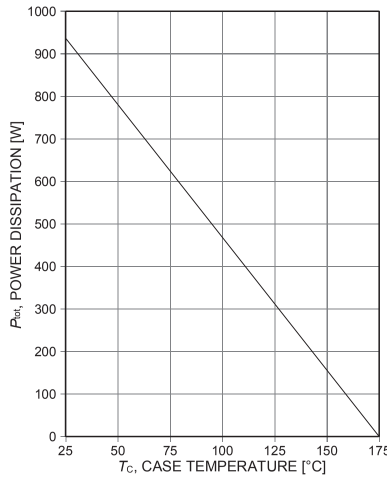



Figure 2. **Power dissipation as a function of case temperature**
($T_{vj}$≤175°C)

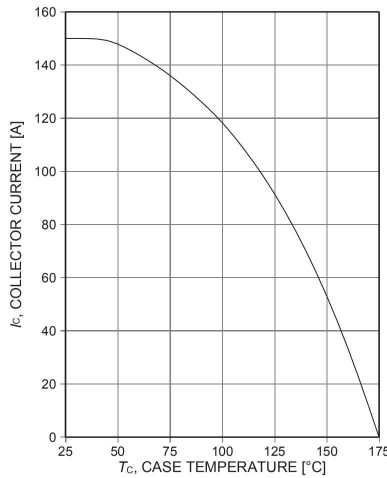



Figure 3. **Collector current as a function of case temperature**
($V_{GE}$≥15V, $T_{vj}$≤175°C)

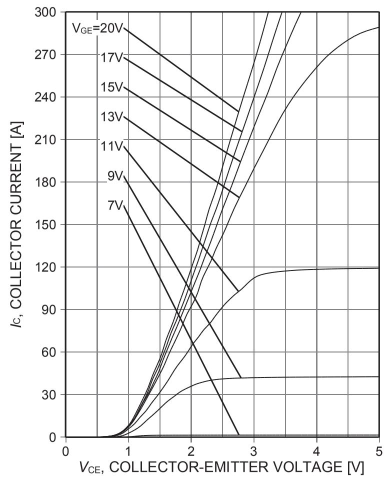



Figure 4. **Typical output characteristic**
($T_{vj}$=25°C)

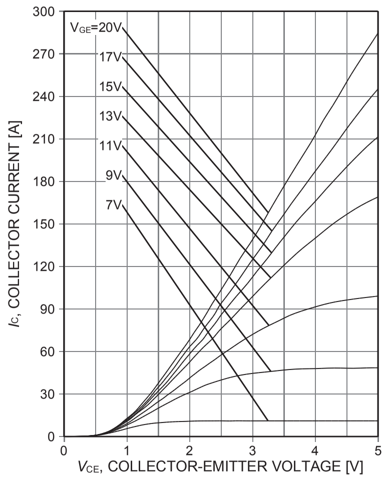



Figure 5. **Typical output characteristic**
($T_{vj}$=175°C)

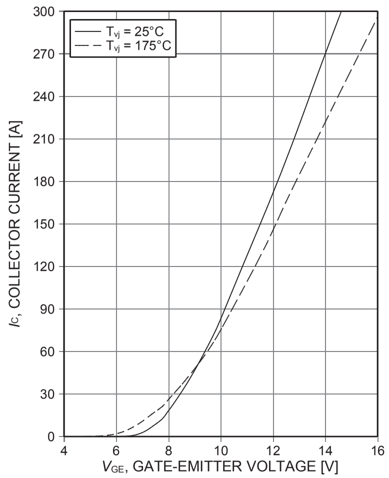



Figure 6. **Typical transfer characteristic**
($V_{CE}$=20V)

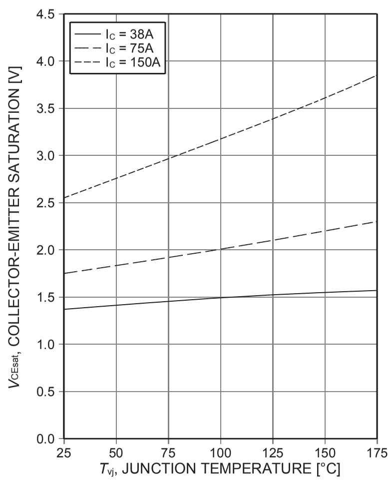



Figure 7. **Typical collector-emitter saturation voltage as a function of junction temperature**
($V_{GE}$=15V)

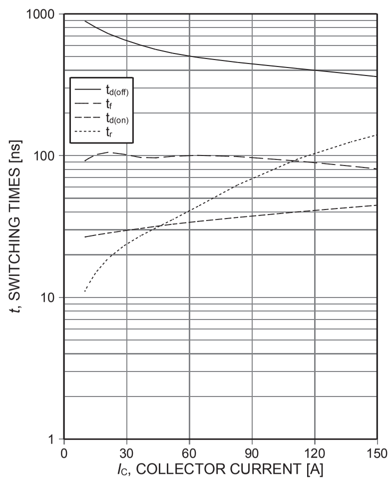



Figure 8. **Typical switching times as a function of collector current**
(inductive load, $T_{vj}$=175°C, $V_{CE}$=600V, $V_{GE}$=0/15V, $r_G$=6Ω, Dynamic test circuit in Figure E)





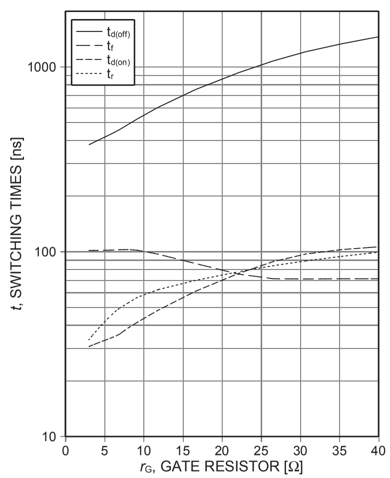



Figure 9. **Typical switching times as a function of gate resistor**
(inductive load, $T_{vj}$=175°C, $V_{CE}$=600V, $V_{GE}$=0/15V, $I_C$=75A, Dynamic test circuit in Figure E)

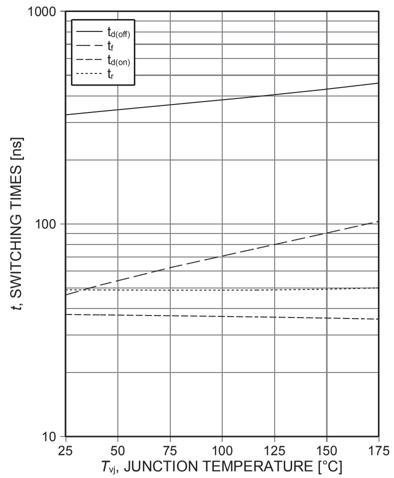



Figure 10. **Typical switching times as a function of junction temperature**
(inductive load, $V_{CE}$=600V, $V_{GE}$=0/15V, $I_C$=75A, $r_G$=6Ω, Dynamic test circuit in Figure E)

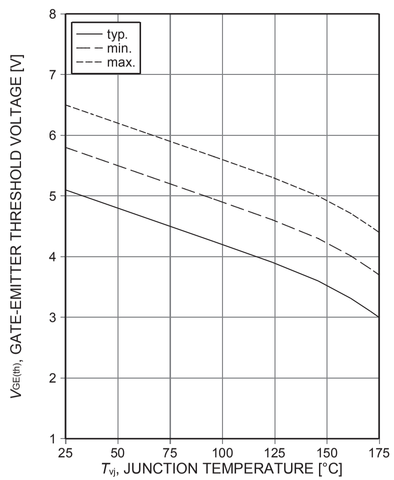



Figure 11. **Gate-emitter threshold voltage as a function of junction temperature**
($I_C$=1,875mA)

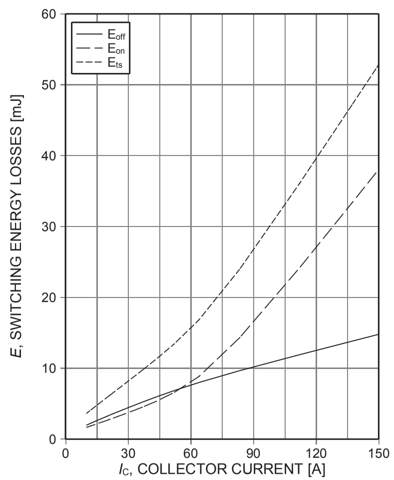



Figure 12. **Typical switching energy losses as a function of collector current**
(inductive load, $T_{vj}$=175°C, $V_{CE}$=600V, $V_{GE}$=0/15V, $r_G$=6Ω, Dynamic test circuit in Figure E)

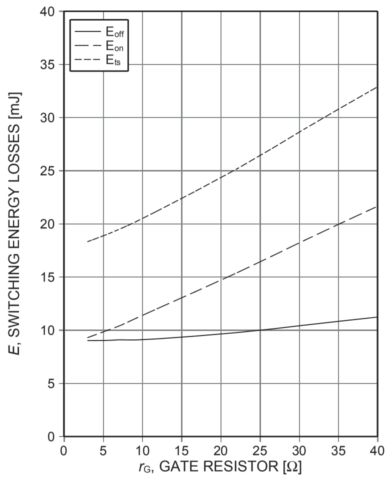



Figure 13. **Typical switching energy losses as a function of gate resistor**
(inductive load, $T_{vj}$=175°C, $V_{CE}$=600V, $V_{GE}$=0/15V, $I_C$=75A, Dynamic test circuit in Figure E)

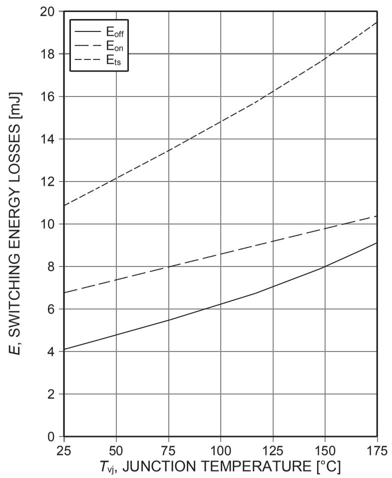



Figure 14. **Typical switching energy losses as a function of junction temperature**
(inductive load, $V_{CE}$=600V, $V_{GE}$=0/15V, $I_C$=75A, $r_G$=6Ω, Dynamic test circuit in Figure E)

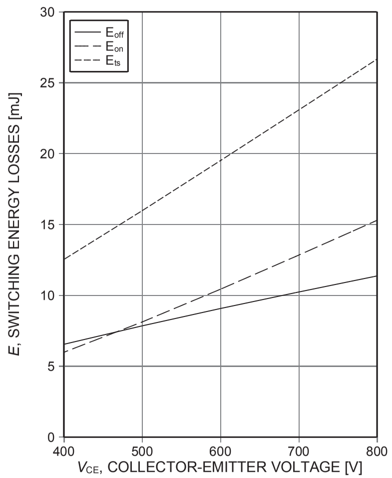



Figure 15. **Typical switching energy losses as a function of collector emitter voltage**
(inductive load, $T_{vj}$=175°C, $V_{GE}$=0/15V, $I_C$=75A, $r_G$=6Ω, Dynamic test circuit in Figure E)

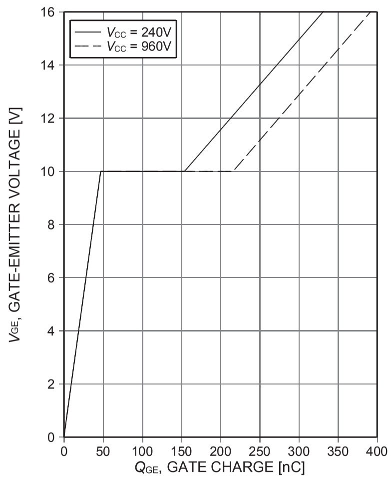



Figure 16. **Typical gate charge**
($I_C$=75A)





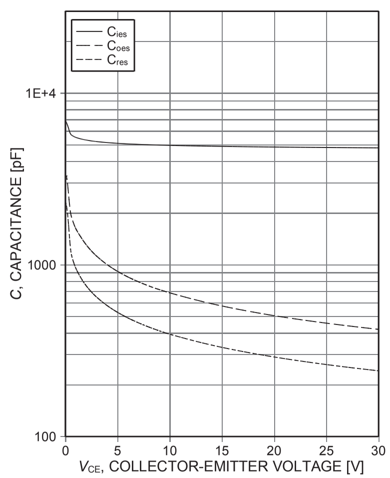



Figure 17. **Typical capacitance as a function of collector-emitter voltage**
($V_{GE}$=0V, f=1MHz)

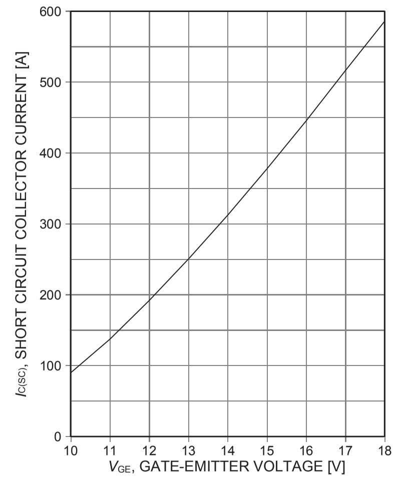



Figure 18. **Typical short circuit collector current as a function of gate-emitter voltage**
($V_{CE}$≤600V, $T_{vj}$≤175°C)

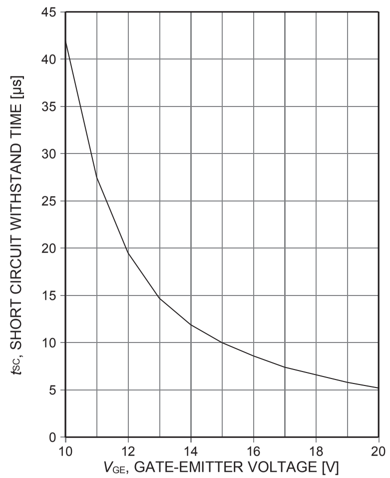



Figure 19. **Short circuit withstand time as a function of gate-emitter voltage**
($V_{CE}$≤600V, start at $T_{vj}$≤175°C)

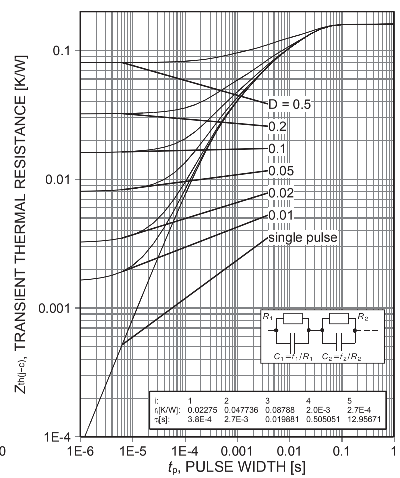
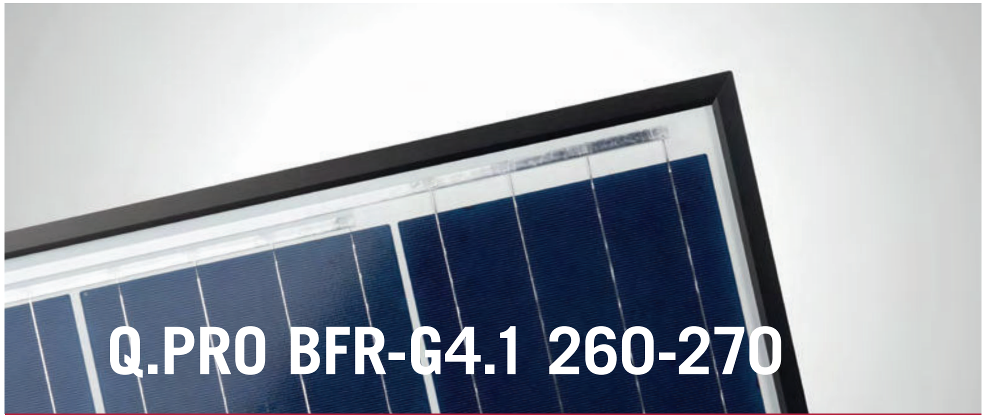



Figure 20. **IGBT transient thermal resistance**
($D$=$t_p$/T)

# E
# Photovoltaic Panel Datasheet



# Q.PRO BFR-G4.1 260-270

## POLYKRISTALLINES SOLARMODUL

**Das neue Q.PRO BFR-G4.1 ist das Ergebnis der konsequenten Weiterentwicklung unserer Q.PRO-Familie. Dank verbesserter Leistungsausbeute, ausgezeichneter Zuverlässigkeit und höherer Betriebssicherheit erzeugt das neue Q.PRO BFR-G4.1 Strom zu niedrigen Stromgestehungskosten und eignet sich für ein breites Anwendungsspektrum.**

**NIEDRIGE STROMGESTEHUNGSKOSTEN**
Höherer Ertrag pro Fläche und niedrigere BOS-Kosten dank hoher Leistungsklassen und einer Effizienz von bis zu 16,5 %.

**INNOVATIVE ALLWETTER-TECHNOLOGIE**
Optimale Erträge bei allen Wetterlagen dank herausragendem Schwachlicht- und Temperaturverhalten.

**ANHALTENDE LEISTUNGSSTÄRKE**
Langfristige Ertragssicherheit dank Anti PID Technology[1], Hot-Spot Protect und Traceable Quality Tra.Q™.

**LEICHTGEWICHTIGER QUALITÄTSRAHMEN**
Rahmen aus High-Tech-Aluminiumlegierung, zertifiziert für hohe Schnee- (5400 Pa) und Windlasten (4000 Pa).

**MAXIMALE KOSTENREDUZIERUNG**
Bis zu 10 % verringerte Logistikkosten dank höherer Modulkapazität pro Transportbox.

**SICHERE ELEKTRONIK**
Schutz vor Kurzschlüssen und Leistungsverlust durch Hitze dank atmungsaktiver Anschlussdose und geschweißten Kabeln.

**INVESTITIONSSICHERHEIT**
12 Jahre Produktgarantie sowie 25-jährige lineare Leistungsgarantie[2].

EUPD RESEARCH TOP BRAND PV MODULES EUROPE 2016

Q CELLS ERTRAGSSICHERUNG: ANTI PID TECHNOLOGY (APT), HOT-SPOT PROTECT (HSP), TRACEABLE QUALITY (TRA.Q™)

VDE Quality Tested – hohe Zuverlässigkeit, geringe Degradation, regelmäßige Produktüberwachung – ID. 40042038

Photon – Q CELLS Bestes polykristallines Solarmodul 2014 Q.PRO-G2 235 – Getestet wurden 174 Module

[1] Testbedingungen: Zellen auf -1500 V gegenüber der geerdeten, mit Metallfolie bedeckten Moduloberfläche, 25 °C, 168 h

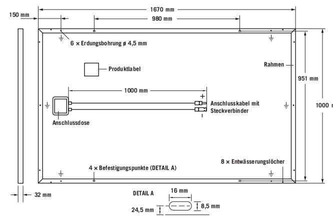
[2] Für weitere Informationen siehe Rückseite dieses Datenblatts.

**DIE IDEALE LÖSUNG FÜR:**

- Private Aufdachanlagen
- Kommerzielle und industrielle Aufdachanlagen
- Solarkraftwerke auf Freiflächen

Engineered in **Germany**

| | |
|---|---|
| Format | 1670 mm × 1000 mm × 32 mm (inklusive Rahmen) |
| Gewicht | 18,8 kg |
| Frontabdeckung | 3,2 mm thermisch vorgespanntes Glas mit Antireflexions-Technologie |
| Rückabdeckung | Verbundfolie |
| Rahmen | Schwarz eloxiertes Aluminium |
| Zelle | 6 × 10 polykristalline Solarzellen |
| Anschlussdose | 77 mm × 90 mm × 15,8 mm<br>Schutzart IP67, mit Bypassdioden |
| Kabel | 4 mm² Solarkabel; (+) ≥ 1000 mm, (-) ≥ 1000 mm |
| Steckverbinder | MC4, IP68 |

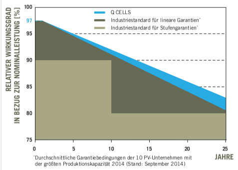



## ELEKTRISCHE KENNGRÖSSEN

| LEISTUNGSKLASSEN | | | | 260 | 265 | 270 |
|---|---|---|---|---|---|---|
| **MINIMALLEISTUNG BEI STANDARD TESTBEDINGUNGEN, STC[1] (LEISTUNGSTOLERANZ +5 W / -0 W)** | | | | | | |
| Minimum | Leistung bei MPP[2] | $P_{MPP}$ | [W] | 260 | 265 | 270 |
| | Kurzschlussstrom* | $I_{SC}$ | [A] | 9,07 | 9,15 | 9,23 |
| | Leerlaufspannung* | $U_{OC}$ | [V] | 37,70 | 37,93 | 38,16 |
| | Strom bei MPP* | $I_{MPP}$ | [A] | 8,46 | 8,54 | 8,62 |
| | Spannung bei MPP* | $U_{MPP}$ | [V] | 30,74 | 31,03 | 31,31 |
| | Effizienz[2] | η | [%] | ≥ 15,6 | ≥ 15,9 | ≥ 16,2 |
| **MINIMALLEISTUNG BEI NORMALEN BETRIEBSBEDINGUNGEN, NOC[3]** | | | | | | |
| Minimum | Leistung bei MPP[2] | $P_{MPP}$ | [W] | 191,3 | 194,9 | 198,6 |
| | Kurzschlussstrom* | $I_{SC}$ | [A] | 7,31 | 7,38 | 7,44 |
| | Leerlaufspannung* | $U_{OC}$ | [V] | 35,09 | 35,31 | 35,52 |
| | Strom bei MPP* | $I_{MPP}$ | [A] | 6,62 | 6,68 | 6,75 |
| | Spannung bei MPP* | $U_{MPP}$ | [V] | 28,90 | 29,16 | 29,42 |

[1] 1000 W/m², 25 °C, Spektrum AM 1.5G [2] Messtoleranzen STC ± 3 %; NOC ± 5 % [3] 800 W/m², NOCT, Spektrum AM 1.5G * Typische Werte, tatsächliche Werte können abweichen

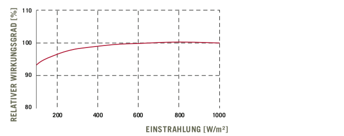
### Q CELLS LEISTUNGSGARANTIE




Mindestens 97 % der Nennleistung innerhalb des ersten Jahres. Danach max. 0,6 % Degradation pro Jahr. Mindestens 92 % der Nennleistung nach 10 Jahren. Mindestens 83 % der Nennleistung nach 25 Jahren.

Alle Daten innerhalb der Messtoleranzen. Volle Produkt- und Leistungsgarantien entsprechend der jeweils gültigen Garantien der Q CELLS Vertriebsgesellschaft Ihres Landes.

### SCHWACHLICHTVERHALTEN




Typische Modulleistung unter niedrigen Einstrahlungsbedingungen im Vergleich zu STC-Bedingungen (25 °C, 1000 W/m²).

### TEMPERATURKOEFFIZIENTEN

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Temperaturkoeffizient $I_{SC}$ | α | [%/K] | +0,04 | Temperaturkoeffizient $U_{OC}$ | β | [%/K] | −0,30 |
| Temperaturkoeffizient $P_{MPP}$ | γ | [%/K] | −0,41 | Nennbetriebs-Zellentemperatur | NOCT | [°C] | 45 |

## KENNGRÖSSEN ZUR SYSTEMEINBINDUNG

| | | | | | |
|---|---|---|---|---|---|
| Maximale Systemspannung | $U_{SYS}$ | [V] | 1000 | Schutzklasse | II |
| Rückstrombelastbarkeit | $I_R$ | [A] | 20 | Brandklasse | C |
| Wind-/Schneelast (Test-Last nach IEC 61215) | | [Pa] | 4000/5400 | Zulässige Modultemperatur im Dauerbetrieb | −40 °C – +85 °C |

## QUALIFIKATIONEN UND ZERTIFIKATE

VDE Quality Tested; IEC 61215 (Ed. 2); IEC 61730 (Ed. 1), Anwendungsklasse A
Dieses Datenblatt entspricht der DIN EN 50380.

## PARTNER

**HINWEIS:** Den Anweisungen in der Installationsanleitung ist unbedingt Folge zu leisten. Weitere Informationen zur freigegebenen Nutzung der Produkte sind der Installations- und Betriebsanleitung zu entnehmen oder können beim Technischen Service erfragt werden.

**Hanwha Q CELLS GmbH**
Sonnenallee 17-21, 06766 Bitterfeld-Wolfen, Germany | TEL +49 (0)3494 66 99-23444 | FAX +49 (0)3494 66 99-23000 | EMAIL sales@q-cells.com | WEB www.q-cells.com



Engineered in **Germany**

# F

# Series and Parallel Connection of Switches

| | | | |
|---|---|---|---|
| Latitude (decimal degrees):36.092 | Efficiency PV panels | 0.156 | |
| Longitude (decimal degrees):-5.771 | Efficiency MPP Tracker | 0.99 | |
| Elevation (m):26 | System losses, cables etc | 0.99 | |
| Radiation database:PVGIS-CMSAF | Area of 1 panel [m2] | 1.67 | |
| | Number of panels in the park | 21600 | with STC-irradiance of 1000 W/m2 |
| Tarifa, Cadiz, Spain | Number of subfields | 6 | 5.627232 |
| Slope: 30 | Subfields per DAB | 1 | |
| Azimuth: 0 | | | |

Bi: In-plane beam irradiance (W/m2)
Di: In-plane diffuse irradiance (W/m2)
Ri: In-plane reflected irradiance (W/m2)
As: Sun elevation (deg.)
Tamb: Ambient temperature (deg. C)
W10: 10m Wind speed (m/s)
Int.: 1 means solar radiation values are reco

| Hour | Bi [W/m2] | Di [W/m2] | Ri [W/m2] | Global irradiance [W/m2] | Energy of total PV park area [MW] | Power reduced by system losses [MW] = Output Power of Park | **Output Power per subfield [MW] = Input to ONE DAB** |
|---|---|---|---|---|---|---|---|
| 00:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 01:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 02:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 03:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 04:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 05:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 06:54 | 0 | 24.88 | 0.37 | 24.88 | 0.14 | 0.14 | **0.02** |
| 07:54 | 89.51 | 130.13 | 2.7 | 219.64 | 1.24 | 1.21 | **0.20** |
| 08:54 | 349.41 | 168.98 | 5.84 | 518.39 | 2.92 | 2.86 | **0.48** |
| 09:54 | 665.54 | 132.64 | 8.76 | 798.18 | 4.49 | 4.40 | **0.73** |
| 10:54 | 817.63 | 143.56 | 10.5 | 961.19 | 5.41 | 5.30 | **0.88** |
| 11:54 | 30.2 | 350.28 | 5.31 | 380.48 | 2.14 | 2.10 | **0.35** |
| 12:54 | 909.65 | 149.27 | 11.59 | 1058.92 | 5.96 | 5.84 | **0.97** |
| 13:54 | 10.72 | 295.24 | 4.34 | 305.96 | 1.72 | 1.69 | **0.28** |
| 14:54 | 0 | 149.54 | 2.15 | 149.54 | 0.84 | 0.82 | **0.14** |
| 15:54 | 501.47 | 117.7 | 6.81 | 619.17 | 3.48 | 3.41 | **0.57** |
| 16:54 | 275.22 | 89.07 | 4.05 | 364.29 | 2.05 | 2.01 | **0.33** |
| 17:54 | 64.23 | 40.98 | 1.21 | 105.21 | 0.59 | 0.58 | **0.10** |
| 18:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 19:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 20:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 21:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 22:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |
| 23:54 | 0 | 0 | 0 | 0 | 0.00 | 0.00 | **0.00** |

**Figure F.1:** Calculation of PV output power in Tarifa on March 20, 2016

| | | | |
|---|---|---|---|
| Input voltage [kV] | 1.3 | 2015 | 1.19 |
| Output voltage [kV] | 16 | 24800 | |
| | | | |
| Safety margin current | 70% of rating | | |
| Safety margin voltage | 55% | | |
| I_D [A] | 72 | 50.40 | |
| V_DS [V] | 1700 | 1096.77 | |
| | | | |
| **Low voltage side** | | **High voltage side** | |
| Input DC - current [A] | Number of Mosfets in parallel (dependent on current) | Output DC - current [A] | Number of Mosfets in parallel (dependent on current) |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 17.59 | 0.35 | 1.43 | 0.03 |
| 155.30 | 3.08 | 12.62 | 0.25 |
| 366.54 | 7.27 | 29.78 | 0.59 |
| 564.38 | 11.20 | 45.86 | 0.91 |
| 679.64 | 13.48 | 55.22 | 1.10 |
| 269.03 | 5.34 | 21.86 | 0.43 |
| 748.74 | **14.86** | 60.84 | **1.21** |
| 216.34 | 4.29 | 17.58 | 0.35 |
| 105.74 | 2.10 | 8.59 | 0.17 |
| 437.80 | 8.69 | 35.57 | 0.71 |
| 257.58 | 5.11 | 20.93 | 0.42 |
| 74.39 | 1.48 | 6.04 | 0.12 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| 0.00 | 0.00 | 0.00 | 0.00 |
| | | | |
| Configuration of one "switching element" in the full bridge | | | |
| **Low voltage side** | | **High voltage side** | |
| Number of Mosfets in series ns | 1.19 | 14.59 | 14.59 |
| Number of Mosfet-strings in parallel np | 14.86 | 1.21 | |
| | | | |
| **ns** | **2** | **15** | |
| **np** | **15** | **2** | |

**Figure F.2:** Calculation of necessary number of in series and in parallel connected switches for the given power

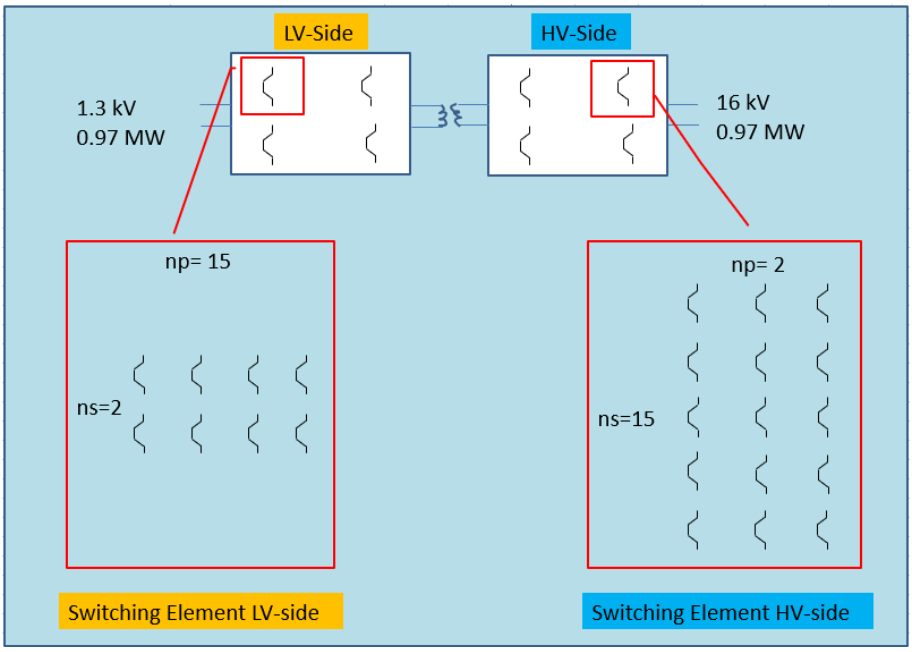



**Figure F.3:** Composition of the switching elements on the LV- and HV-side