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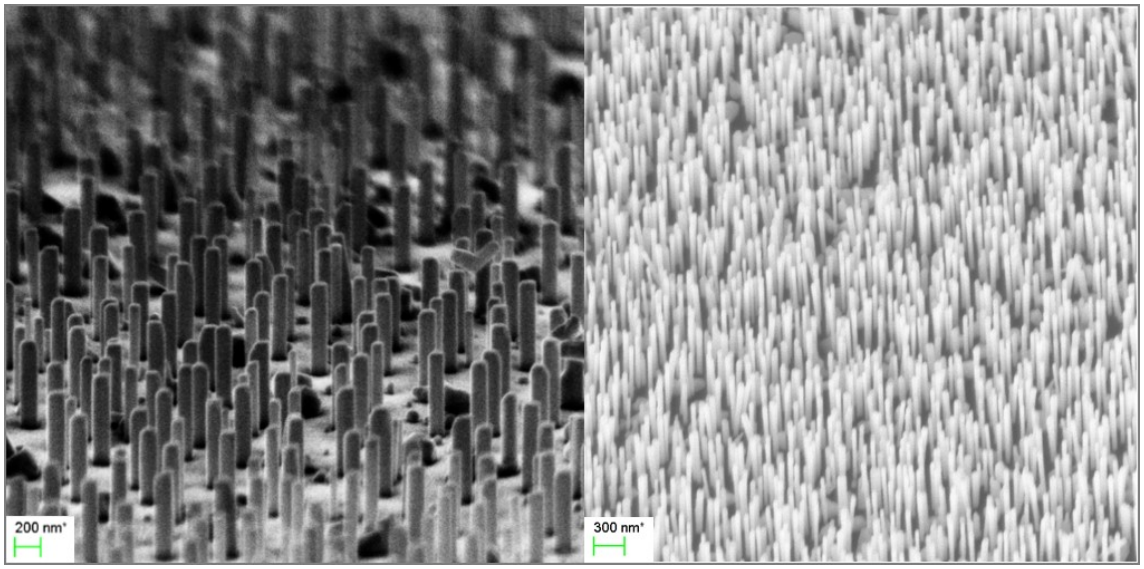

Molecular Beam Epitaxy of Catalyst-Free InAs Nanowires on Si (111)

Thesis for Erasmus Mundus Master of Science in Nanoscience and Nanotechnology

Specialization in Nanoelectronics

Elham Fadaly

Department of Microtechnology & Nanoscience
Terahertz and Millimitre Wave Laboratory
Chalmers University of Technology
Gothenburg, Sweden 2015

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Elham Fadaly

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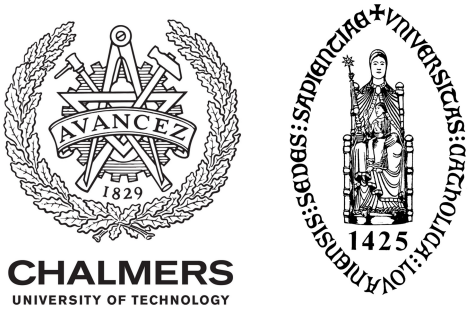

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Molecular Beam Epitaxy of Catalyst-Free InAs Nanowires on Si (111)
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Cover: 30 deg. tilt SEM images of catalyst-free InAs nanowires by molecular beam epitaxy using the two strategies discussed in this report in Chapters 5 and 6.

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To

my father (Mohamed Fadaly), my grandfather (Ehab Kassab)- may their souls rest in peace- and my beloved mother (Amal Kassab)

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Abstract

Semiconductor nanowires (NWs) represent a unique system for exploring phenomena at the nanoscale and are also expected to play a critical role in future electronic and optoelectronic devices. For some functional NW-based devices, it is essential to have control over position, size and directionality of NWs for homogeneous and predictive performance. Moreover, the growth of device-quality NWs with high purity should abstain from conventional nucleation schemes that employ foreign catalyst such as gold. Recent progress in selective-area epitaxy (SAE) technique has allowed position controlled catalyst-free growth of NWs, where semiconductor substrates are masked by dielectrics with nano-aperture patterns. This is a kind of template method, which involves a combination of bottom up (epitaxial growth) and top down (lithography) approaches. However, the current approaches for the nano-patterning are mainly based on electron beam lithography (e-beam), which is expensive and not suitable for large scale productions. In this master's thesis, we demonstrate the molecular beam epitaxy (MBE) of catalyst free InAs NWs on Si (111) by different techniques. The first technique adapts a fully bottom-up approach for selective-area molecular beam epitaxy (SA-MBE) growth of catalyst-free InAs NWs. Specific to this work, the inexpensive, versatile and simple colloidal lithography technique is applied for opening nano-apertures in a SiO_2 layer deposited on Si substrates, and methods to have control over the size and density of patterns were studied. In the second approach, epitaxy of non-ordered catalyst-free InAs NWs was demonstrated on substrates without lithography patterning. This is realized by generating pinholes in the SiO_2 layer using wet etching.

Keywords: MBE, nanowires, indium arsenide (InAs), selective-area epitaxy, catalyst-free, III-V, colloidal lithography.

Acknowledgements

In 2006, my physics teacher in school wrote on my notebook Prof. Elham Zewail, naming me after Prof. Ahmed Zewail, the Egyptian-American Nobel laureate in 1999 for his work on femto- chemistry and physics. My teacher wanted to see me one day like Prof. Zewail due to my excellence in physics, curiosity and thirst to knowledge like researches and scientists. Since then, I have been passionate about science and research with having Prof. Zewail as my role model. I kept this piece of paper with my name after Prof. Zewail reminding me of my passion to science and technology. In 2011, I found the starting point in my journey when Prof. Sherif Sedky, the director or Youssef Jameel for Science and technology research center in the American University in Cairo in Egypt back at that time, offered me the opportunity to join a summer research internship in the clean room in the center to learn and practice the fundamentals of nanotechnology and nanofabrication. It was like a dream to wear the clean room safety clothes and hold wafers and start working on there. Having this great opportunity to work in a high tech environment with experts inspired me to make a positive change in this world and add to human knowledge with the help of science and technology.

Two years later was a turning point in my life when I was admitted as a master's student in the Erasmus Mundus Master program for nanoscience and nanotechnology (EMM-NANO) in Katholieke Universiteit Leuven in Belgium and Chalmers University of Technology in Sweden. Since then, I realized that scientific research is my perfect match. I am truly indebted to Prof. Sedky who opened the door for me to enter this field and spared no effort and time to enrich my knowledge and capabilities. I am also grateful to Prof. Guido Groeseneken, Prof. Marc Heyns and the whole EMM-NANO family who made their best to establish such multidisciplinary program. I do think that I would have never acquired these skills or rich knowledge anywhere else.

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I shall finalize my words with deep gratitude to 25 January revolution in 2011 in Egypt and its martyrs who inspired me back then in 2011 and made me take the decision and follow my passion to make a difference on earth. May be my contribution here to science and humanity is like a droplet in a sea. However, I believe in Vincent Van Gogh saying, "Great things are not done by impulse but by a series of small things brought together".

Elham Fadaly, Gothenburg, August 2015

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Abbreviations

FETs	Field Effect Transistors
InAs	Indium Arsenide
GaAs	Gallium Arsenide
MBE	Molecular Beam Epitaxy
NWs	Nanowires
SAE	Selective Area Epitaxy
SA-MBE	Selective Area Molecular Beam Epitaxy
UHV	Ultra-High Vacuum
BOE	Buffer Oxide Etchant
CL	Colloidal Lithography
HCL	Hole-Mask Colloidal Lithography
CVD	Chemical Vapor Deposition
PECVD	Plasma Enhanced Chemical Vapor Deposition
RMS	root mean square
VLS	Vapor-liquid-solid
EBL	Electron Beam Lithography
FIB	Focused Ion Beam
NIL	Nanoimpint Lithography
LPE	Liquid Phase Epitaxy
VPE	Vapor Phase Epitaxy
MOVPE	Metal Organic Phase Epitaxy
RHEED	Reflection High-Energy Electron Diffraction
QMS	Quadruple Mass Spectrometer
AFM	Atomic Force Microscopy
SEM	Scanning Electron Microscopy
STM	Scanning Tunneling Microscopy

Abbreviations

SPM	scanning probe microscopy
WD	Working Distance
PS	Polystyrene
SC	Surface Coverage
IPS	Inter-Particle Spacing
NND	Nearest Neighbor Distance
PDDA	polydiallyldimethylm-monium
PSS	Poly sodium4Styrenesulfonate
ACH	Aluminium Chloride Hydroxide
DI	De-ionized Water
EDL	Electric Double Layer

1

Introduction

1.1 III-V/Si Integration

The rapid scaling of Silicon (Si) technology, as predicted by the Moore's law, has enabled the dramatic success of integrated circuits during the past few decades. Millions of transistors are fully integrated onto a single chip and the node size has reached 14 nm which has been deployed in the 5^{th} generation of core processors by Intel in early 2015. However, miniaturizing the size feature of transistors poses a real limitation on the top down fabrication technique, as precise control of chip manufacturing becomes increasingly difficult and expensive to maintain in the nanometer regime. Moreover, the continuing size down-scaling also reaches the physical limits imposed by the material properties of Si. The hot carrier effect due to a low saturation velocity leads to a dramatic increase in the leakage current and thus deteriorating the performance of the electronic devices. Many technological advancements and innovations as summarized in figure 1.1 have been proposed to sustain the scaling such as utilizing uniaxial strained Si channels, metal-gate/high-k dielectric stack, 3D-multi-gate configurations and many others. Moreover, alternative channel materials such as the compound III-V semiconductors have been proposed to combine the merits of III-V materials and Si. III-V materials possess much higher electron mobilities compared to Si, and direct band gaps which are more efficient for light emitting. Yet, III-V materials needs to be monolithically integrated with Si to be compatible with the well-developed Si processing platform.

Various approaches have been proposed to achieve this combination, from die-to-

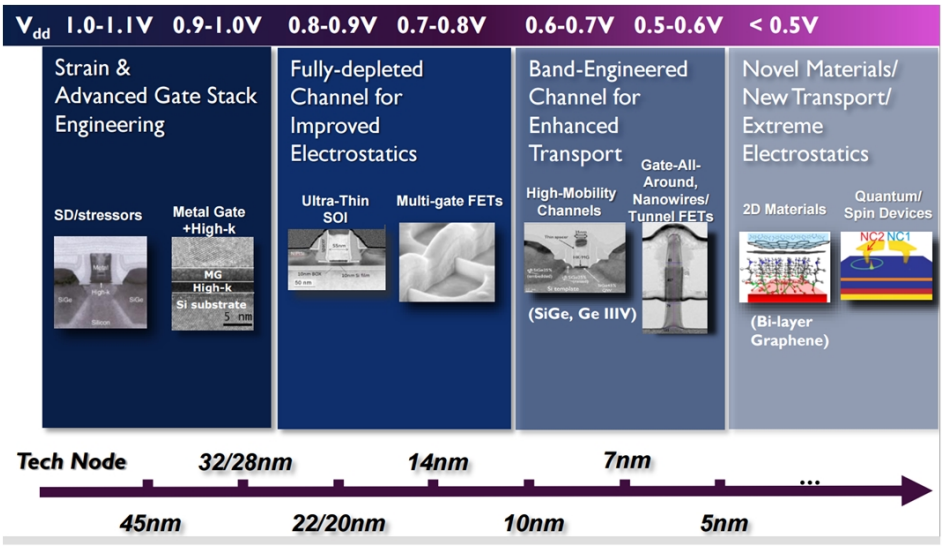

Figure 1.1: Technological innovations and advancements to mitigate the challenges of scaling of transistors size with technology node to sustain Moore's Law (adopted from B-KUL-H062NA-1415 course lecture notes by Prof. Wilfried Vandervorst).

wafer bonding to full wafer bonding to direct growth of III–V devices on Si [7–9]. Despite the flexibility provided by the bonding approaches, such solutions have found difficulties in industrial implementation due to a few reasons such as increased costs, lower yields, higher thermal budget and etc. In contrast to bonding approaches a truly monolithic integration solution achieved via epitaxial methods is the most sustainable one. However, there are great challenges for III-V/Si integration by direct epitaxial growth, due to the physical limitations imposed by lattice, thermal and valence-mismatches [10–12]. See figure 1.2, InAs displays an 11.6 % mismatch in lattice constants with respect to Si. This large lattice mismatch leads to a high density of defects and dislocations. Moreover, the thermal expansion coefficients mismatch between III-Vs and Si causes the formation of cracks when they are cooled down after growth. Furthermore, the difference in polarity (valence mismatch) leads to the formation of antiphase domains yielding defective materials. Therefore, integration of III-V materials with Si via a conventional planar interface is problematic concerning obtaining pure single crystalline materials and limits the performance and life-time of the electronic devices.

To overcome these limitations, 1D nanostructures namely, nanowires (NWs) have

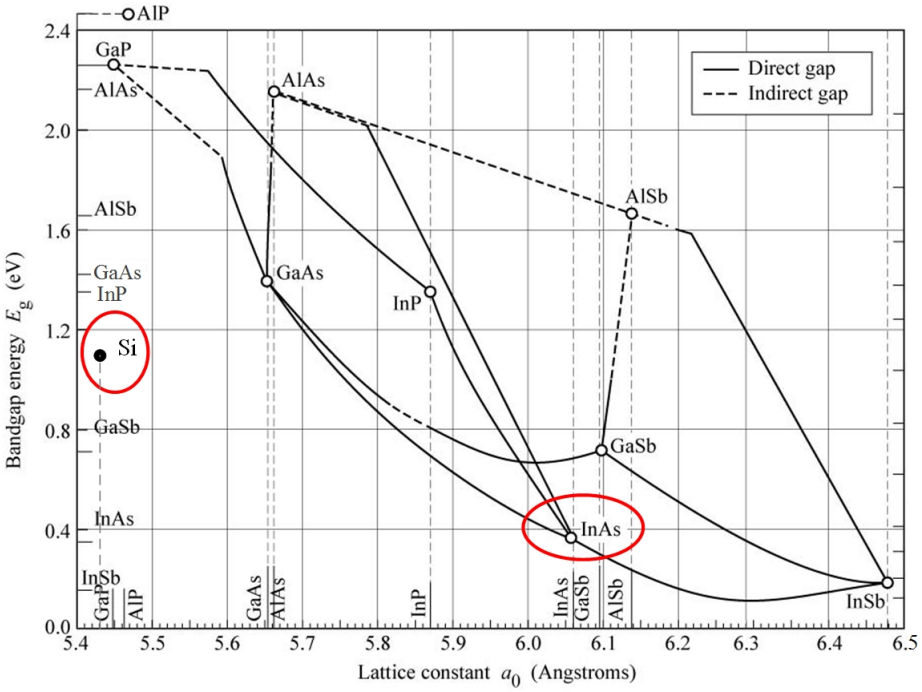

Figure 1.2: Lattice constants and energy bandgaps for the different III-V materials with respect to Si (adopted from [1]).

been extensively investigated in the past decade [13–15] to build NW based field effect transistors (FETs). These intensive researches were motivated by the fact that NWs can accommodate a greater elastic strain with respect to the host substrate than what is commonly seen in the planar interfaces. This is due to the lateral strain relaxation at the side wall borders [16], and the nanoscale nature no longer requires lithography thus greatly reduces the fabrication cost.

1.2 InAs NWs

NWs are one dimensional structures with diameters as small as tens of nanometers and as long as several micrometers. In semiconductor NWs the electronic conduction takes place both by bulk conduction and through tunneling mechanism. And due to their high density of electronic state, diameter-dependent band gap, enhanced surface scattering of electrons and phonons, increased excitation binding energy, high surface to volume ratio and large aspect ratio, NWs exhibit unique properties thus holding lots of promises for applications in electronics, optics, magnetic

media, thermoelectric, energy storage, sensor devices etc [17]. Moreover, the alleviated mismatch of lattice parameters and thermal expansions coefficients enabled the integration of III-V NWs with Si substrate. In addition, NWs can be grown in heterostructures form (axially in the form of quantum barriers and radially in the form of core-shell configuration) with atomically sharp interfaces [18–20].

In this work, we are focusing on epitaxy of III-V materials especially indium arsenide (InAs) NWs. InAs is remarkably attractive material due to its high electron mobility (30000 cm2/V s) at room temperature (300 K) [21], small effective electron mass (0.023mo), narrow direct bandgap (0.35 ev), strong orbit-spin coupling [22] and ability to form low-resistance ohmic contacts [23]. These unique material properties makes InAs NWs very promising for diverse applications such as high frequency electronics, spintronic and sensor devices.

1.3 III-V NWs Synthesis Techniques

Different growth techniques have been developed to fabricate III-V NWs, such as chemical vapor deposition (CVD), molecular beam epitaxy (MBE), laser ablation, thermal evaporation, and a few other options [24]. Most reported NW growths were governed by the famous vapor-liquid-solid (VLS) mechanism, either through self-induced [25,26] or foreign metallic catalyst (e.g Au, Ag, Ni ...etc) [27,28]. The metal catalysts are either lithographically patterned or self-assembled. Such processes in which the catalyst is self-assembled produce NWs that are randomly positioned and also exhibit a significant variation of diameters. A further problem with catalytic growth for certain material combinations, mainly in the case of using foreign catalysts, is that the foreign catalysts can be inevitably incorporated into the NWs, which may be prohibitive for many applications [29]. In the case of self-catalyzed growth, self-assembled catalysts produce randomly positioned NWs with a significant variation in diameter. This auto-catalytic growth may lead to unintentional kinking in the grown NWs. All the aforementioned challenges of NWs catalyst-assisted growth led to massive efforts to investigate the viability of synthesizing catalyst free III-V NWs.

Most reported catalyst-free growth of III-V NWs utilized substrates masked with patterned dielectric layer with nano-aperture patterns. Apart from avoiding catalysts, this technique enables control over size and position of NWs allowing homogenous arrays. To date, nano-patterning of the host substrates is mainly based on top-down approaches like electron beam lithograhy (EBL) [30, 31] and nanoimprint lithography (NIL) [32, 33]. However, like most of the top-down lithography techniques, EBL suffer from the low throughput due to long writing times over millimeter (mm^2) areas in addition to the high cost and the need for complex machinery. NIL provide an alternative with a relatively lower cost and much higher throughput through a replication process. But the technique still needs EBL for stamp fabrication and innovative solutions are still needed to solve process and stamp lifetime issues for different applications [34]. These drawbacks of EBL and NIL greatly limit mass production of semiconductor NWs and thus their industrialization. Therefore, alternative lithography techniques are required to overcome the obstacles of the aforementioned top-down lithography techniques.

In the meantime bottom-up lithography techniques such as colloidal lithography (CL) have shown more attractive properties than conventional lithography techniques for nano-patterning, due to its versatility, simplicity, low-cost and viability of patterning various nano-sized features on large areas (several cm^2). For nanopatterning, the self-assembled colloids are capable of producing 2D-3D templates, which can act as a mask for direct etching [35] or a mask for lift-off [36] to produce structures ranging from tens of micrometers down to tens of nanometers [37]. The abovementioned properties made CL more attractive than conventional lithography techniques, such as immersion lithography, EBL, scanning probe, and focused ion beam (FIB) lithography [38]. Recent researches performed on NWs synthesis utilizing CL techniques used nanoparticles either as a lift-off mask to pattern foreign metal catalyst [39] or an etching mask for the underlying layer to fabricate NWs. To the best of our knowledge, no work has been done on catalyst free growth of III-V NWs utilizing CL.

1.4 Outline of the Thesis

The objective of this work is to explore catalyst-free InAs NWs growth on Si by MBE. Two approaches are adapted here. In the first approach, the templates used for the growth, are prepared by the inexpensive CL. CL enables fabricating short-range ordered nano-aperture patterns on macroscopic templates, which opens a new perspective for mass production of uniform semiconductor NWs. The second approach demonstrates the epitaxy of non-ordered catalyst-free InAs NWs selectively on Si using the natural pinholes opened in SiO_2/Si. The thesis is structured as follows. Chapter 2 starts with introduction to the MBE followed by chapter 3 which describes various characterization techniques used in this work. Chapter 4 discusses about CL techniques. In Chapter 5, MBE growth of InAs NWs on CL patterned substrate is presented. Chapter 6 describes the growth of non-ordered InAs NWs on Si via pinholes. Finally, conclusion and outlook is given.

2

Molecular Beam Epitaxy

This chapter start with introducing the Molecular Beam Epitaxy (MBE) technique for the growth of semiconductor materials, followed by a description of the MBE system layout used in this work Finally, a short introduction of in-situ growth monitoring techniques is presented.

2.1 MBE

Epitaxy refers to the ordered growth of single crystalline film on a crystalline substrate such that the epitaxial layer follows the crystal structure of the underlying substrate. The term 'epitaxy' comes from the Greek words *epi*, and *taxis*, meaning meaning "over" and "in an ordered matter", respectively. Epitaxy is a cornerstone in the semiconductor technology to produce high quality crystalline films. In the last few decades, it has been proved that epitaxial technologies outperformed other film deposition techniques despite being expensive and having complicated instrumentation. Since 1960s, many epitaxial techniques were developed for the growth of semiconductor materials, including liquid phase epitaxy (LPE), vapour-phase epitaxy (VPE), metal-organic VPE (MOVPE), MBE and others [40–43] . Throughout the past years, MOVPE and MBE techniques were the most frequently used techniques for the growth of III/V semiconductor materials. In this thesis, MBE was used for the epitaxy of InAs nanowires.

The fundamental concept of MBE utilizing evaporation of materials in an ultra-high vacuum environment (UHV) was there long time ago. However, it was not

realized until the work of Cho and Arthur [44, 45] in the early 1970s in Bell Laboratories. Since that time, MBE was rapidly developed and evolved to be a main technique for the growth of III/V compound semiconductors and a variety of other materials. MBE features a UHV environment which helps minimizing the incorporation of unwanted impurities and accordingly obtain materials of high purity [42]. Moreover, it offers a very precise control over the growth rate (sub-monolayer/sec) realized by using ultrafast shutters which allows fast switching between material sources. Accordingly, abrupt interfaces at an atomic scale can be achieved in heterostructures and leads to the absence of boundary layers unlike MOVPE which is significant for the quality of the nanostructures. Furthermore, a low temperature growth is used in MBE compared to the other aforementioned deposition techniques which is compatible with the back end complementary metal oxide semiconductors (CMOS) processes. Table 2.1 which is adapted from [46] shows a comparison between the growth parameters of LPE, VPE and MBE epitaxial growth techniques for Gallium Arsenide (GaAs) confirming the promising potential of MBE compared to other techniques.

Table 2.1: Comparison between the epitaxial growth techniques for the growth of GaAs

Growth Parameters	**LPE**	**MOVPE**	**MBE**
Growth Rate (μ/h)	≈ 60	≈ 6	≈ 0.6
Growth Temperature (^oC)	850	750	580-600
Thickness Control (Å)	500	25	5
Interface Width (Å)	≥ 50	<10	<5
Dopant Range (cm^{-3})	$10^{13} - 10^{19}$	$10^{14} - 10^{19}$	$10^{14} - 10^{19}$
Mobility at 77 K for GaAs (n-type) (cm^2/V)	150,000-200,000	140,000	160,000

2.2 MBE System Layout

MBE occurs via the interaction of adsorbed species from one or multiple molecular/atomic beams on the surface of a heated crystalline substrate under UHV. These molecular/atomic beams are evaporated or sublimated in the growth chamber from solid sources contained in crucibles inside the cells. The mean free path of the traversing atoms and molecules is comparable or larger than the growth chamber critical lengths (e.g, the distance between the effusion cells and the substrate), therefore atoms and molecules do not suffer any collisions while traversing constituting a 'molecular flow'. The growth of InAs NWs presented in this work was conducted in a Riber Compact C21 MBE system equipped with three chambers separated by valves and operating independently under UHV to avoid cross contamination, namely loading chamber, outgassing chamber and growth chamber. Figure 2.1 shows an image for the system with its key components named on it.

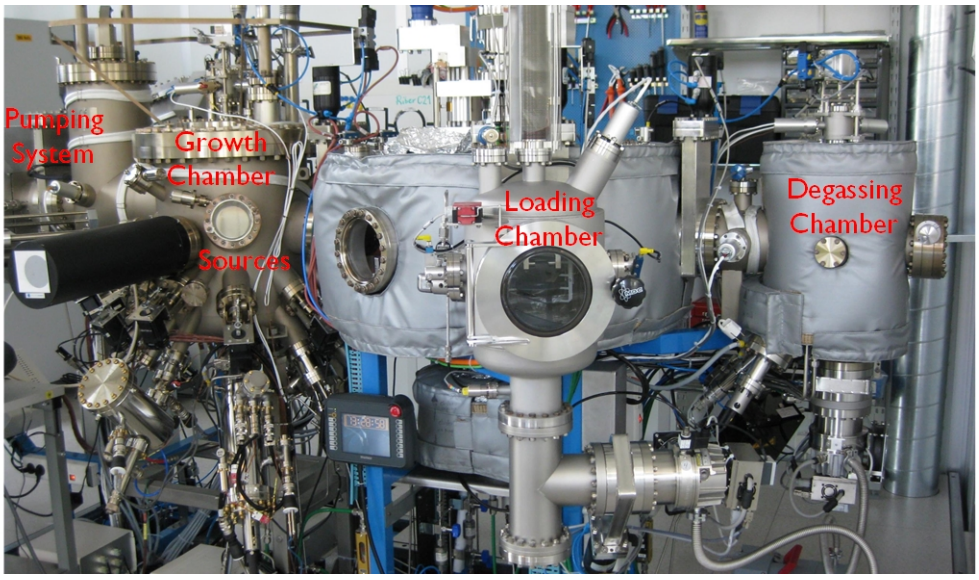

Figure 2.1: Riber MBE Compact C21 System used for the growth of InAs in this work.

The substrates are loaded to the system from the loading chamber, then transferred to the degassing chamber, outgassed at a high temperature for a few hours before being loaded to the main growth chamber. Coming to the main part of the system, the growth chamber is a stainless steel vessel that is comprised of materials sources,

mechanical shutters, and a heatable substrate holder. A schematic drawing for the growth chamber is illustrated in figure 2.2 with a magnified image for the substrate handeling system. The substrate is placed on the substrate handling system in the growth chamber facing down to the sources cells.The substrate holder is heated to the desired growth temperature to activate the diffusion of adsorbed species on the substrate surface promoting epitaxial growth. To improve the growth uniformity across the wafer, the substrate holder is rotated. The sources are contained in high purity crucibles that are thermally heated by Joule effect via Tantalum (Ta) ribbons or wires to provide molecular and atomic beams for the growth. The temperature of the sources is monitored by tungsten/rhenium (W/Re) thermocouples connected to the bottom of the cell or its sidewalls. Several types of sources can be used in the Riber MBE Compact C21 including effusion cells, valved crackers and RF plasma sources. Valved cracker cells are used for the arsenic (As) and antimony (Sb) sources and effusion cells for the III-group sources, see figure 2.3. High vacuum is maintained inside the growth chamber providing the desired base pressure via liquid N_2 cryo-panels surrounding the whole chamber in addition to a diffusion pump attached to the chamber.

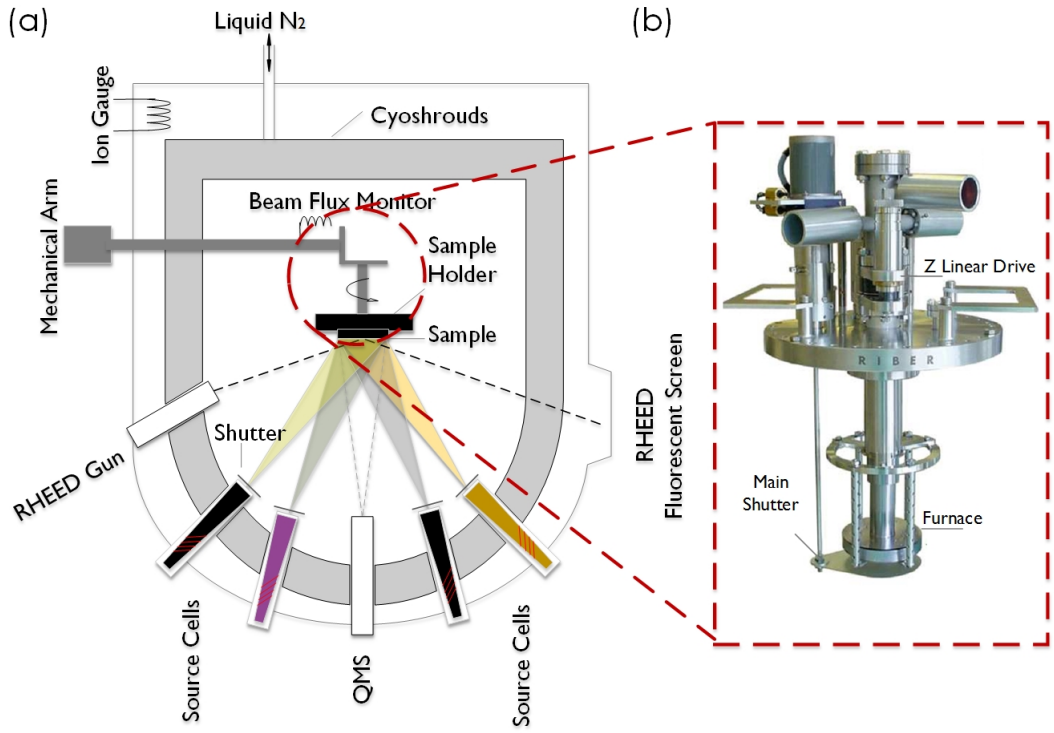

Figure 2.2: (a) Schematic drawing illustrating the MBE growth chamber with (b) a magnified image of the substrate handling system.

Figure 2.3: Images of sources cells used in the MBE system (a) effusion cell used for In and (b) valved-cracker cell used for As [2].

2.3 In-situ Growth Monitoring Techniques

MBE system is usually equipped with two effective in-situ analysis techniques in order to monitor the growth in real-time,namely, reflection high-energy electron diffraction (RHEED) and quadruple mass spectrometer (QMS). RHEED is used to study the surface morphology of the epitaxial layers as well as calibrating the growth

rates. This is achieved by emitting a high energy electron beam (10 keV) with a shallow angle. The electron beam interacts with the crystal structures nearby the surface and the diffracted electron beams constitute a diffraction pattern on a photoluminescent screen which is related to the atomic structures nearby the surface, see figure 2.4 (a). As for the QMS, it is typically used for contamination monitoring and leak detection by analyzing the residual gases, such as hydrogen, oxygen, hydrocarbons ...etc [47]. Moreover, it can be utilized to monitor the desorbing species by measuring the reflected beam fluxes from the substrate [48] as illustrated in figure 2.4 (b).

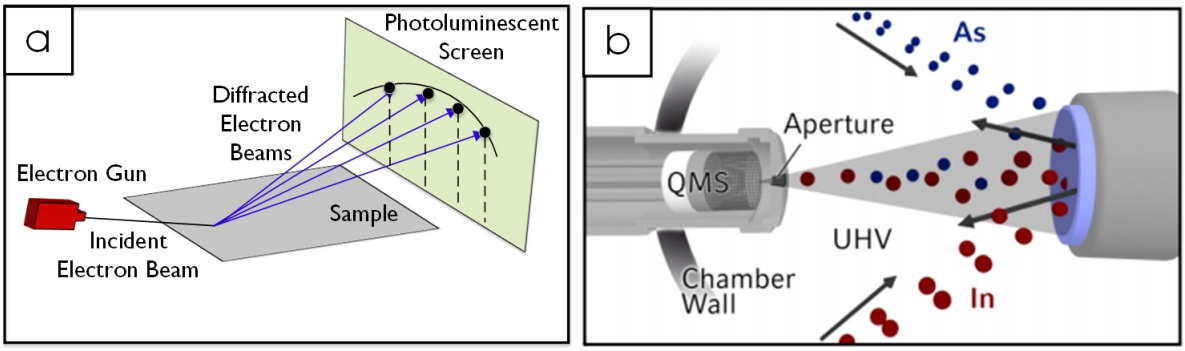

Figure 2.4: Schematic drawings illustrating the in-situ analysis techniques in the MBE system (a) RHEED and (b) QMS (image from [3]).

3

Characterization

In this chapter, the characterization techniques used in this work is discussed in details including atomic force microscopy (AFM), scanning electron microscopy (SEM) and spectroscopic ellipsometry. The working principle of each technique is explained supported by examples studied in this work.

3.1 Atomic Force Microscopy

AFM is a type of scanning probe microscopy (SPM) that enables high resolution imaging of all types of surfaces either soft, or hard and irrespective of their nature and conductivity. In 1986, AFM was first demonstrated by Gerd Binning, Calvin Quate and Christoph Gerber [49] attempting to image non-conducting samples with atomic resolution. Since then, it has emerged to be a promising characterization tool to study materials surface. AFM has been greatly improved over the years to be used in a wide range of applications including biochemistry, material science, physics, biophysics, and nanotechnology. It is commonly used for surface morphology characterizations, fabrication quality control, atoms manipulation and identification, and nanolithography.

AFM measurements are commonly carried out in air, yet liquid and vacuum environments can also be applied when needed. Figure 3.1 shows a schematic drawing for the working principle of AFM. AFM utilizes a cantilever with a mounted sharp tip (probe) commonly micro-fabricated of Si or silicon nitride (Si_3N_4). While being brought in proximity of the specimen surface, it interacts with the sample surface

and acts as a force sensor, sensing the mutual local atomic forces between the tip and the sample. Each point in 2D scanned area, a measurement of the height is recorded as a function of sensed force.

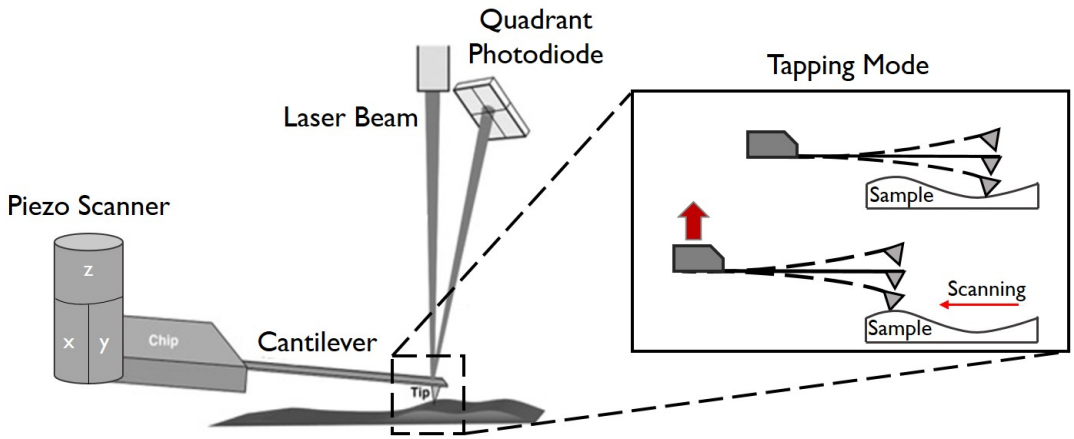

Figure 3.1: Schematic drawing illustrating the working principle of the AFM.

AFM measures the vertical and lateral deflections of the flexible cantilever that supports the tip while scanning the surface. The cantilever deflection is monitored and calibrated by various techniques in order to reproduce the surface topography. These techniques include using an interferometer [50], measuring change in capacitance [51], calibrating the tunneling current from the cantilever to a scanning tunneling microscope (STM) [49], utilizing self-sensing cantilevers [52, 53] or the most commonly used optical lever method [54, 55]. In the optical lever method, a laser beam is focused on the rear side of the cantilever and the reflected laser beam off the top surface of the cantilever is detected by a position-sensitive photodetectors array which are usually composed of quadrant photodiodes. The probe motion across the sample surface is controlled via a piezo-scanner that move in a 3D pattern with respect to the sample surface. The piezo-scanner are made of piezoelectric material that expands and contracts as a response to an applied voltage. The piezo-scanner configuration is based on three independent piezo-segments corresponding to the movement in x, y and z directions, respectively.

AFM can be utilized in various modes depending on the nature of the sample and

the required resolution. It can be operated in a 'contact' mode where the the distance between the tip and the sample is controlled by a feedback loop to maintain a constant cantilever deflection. In this regime, topographic images are recorded by sliding the probing tip which senses different repulsive forces across the sample surface. Although this mode can be used for fast scan, the probe can be damaged if the sample surface is very rough, and the surface can also be damaged if the material is soft. AFM can also be operated in a 'non-contact' mode, in which the tip does not contact the sample surface but stays close to it (1 - 10 nm) sensing attractive forces while scanning the sample surface. In this mode, the cantilever is excited by a piezo-actuator to oscillate at its resonance frequency . During the scan, the oscillation frequency is changed with the tip-sample interactions in order to maintain a constant oscillation amplitude. Degradation of sample surface can be avoided while measured in this mode,yet at a cost of lower image resolution. Somewhere between the contact and the non-contact modes, operation of AFM measurements in a tapping mode enables a fast scan while keeping a high image resolution. In the tapping mode, the cantilever is oscillated at its resonance frequency with a swing (20 - 100 nm) and the probing tip gently touches the sample surface while scanning.

In this work, AFM scans were performed in a Bruker Dimension 3100 SPM system. Either NSG10 or NSC15 tip made of n-type silicon were used for the measurements in the tapping mode. The two types of tips are coated with gold (Au) and Titanium/Platinum (Ti/Pt), respectively providing a high reflectivity for the beam deflection instrumentation, and their radius of curvature is less than 10 nm and 35 nm, respectively. In the framework of this project, AFM was used for characterizing the topography of the nanostructures (nano-apertures and nanospheres), and the quality of the deposited thin films and depicting materials etching rates. Figures 3.2 (a) and b show samples for polystyrene nanospheres and nano-apertures, respectively on Si/SiO_2 substrates. Figures 3.2 (c and d) show the quality of SiO_2 thin films deposited on Si substrates via dry thermal oxidation and evaporation techniques, respectively and the root mean square roughness information was extracted from these images as labeled in the figures. Figures 3.2 (e and f) which

displays etching of thermal oxide inside nano-apertures masked with chromium (Cr) in an buffer oxide etchant (BOE) for 15 and 120 s, respectively and accordingly the etching rate can be readily calculated.

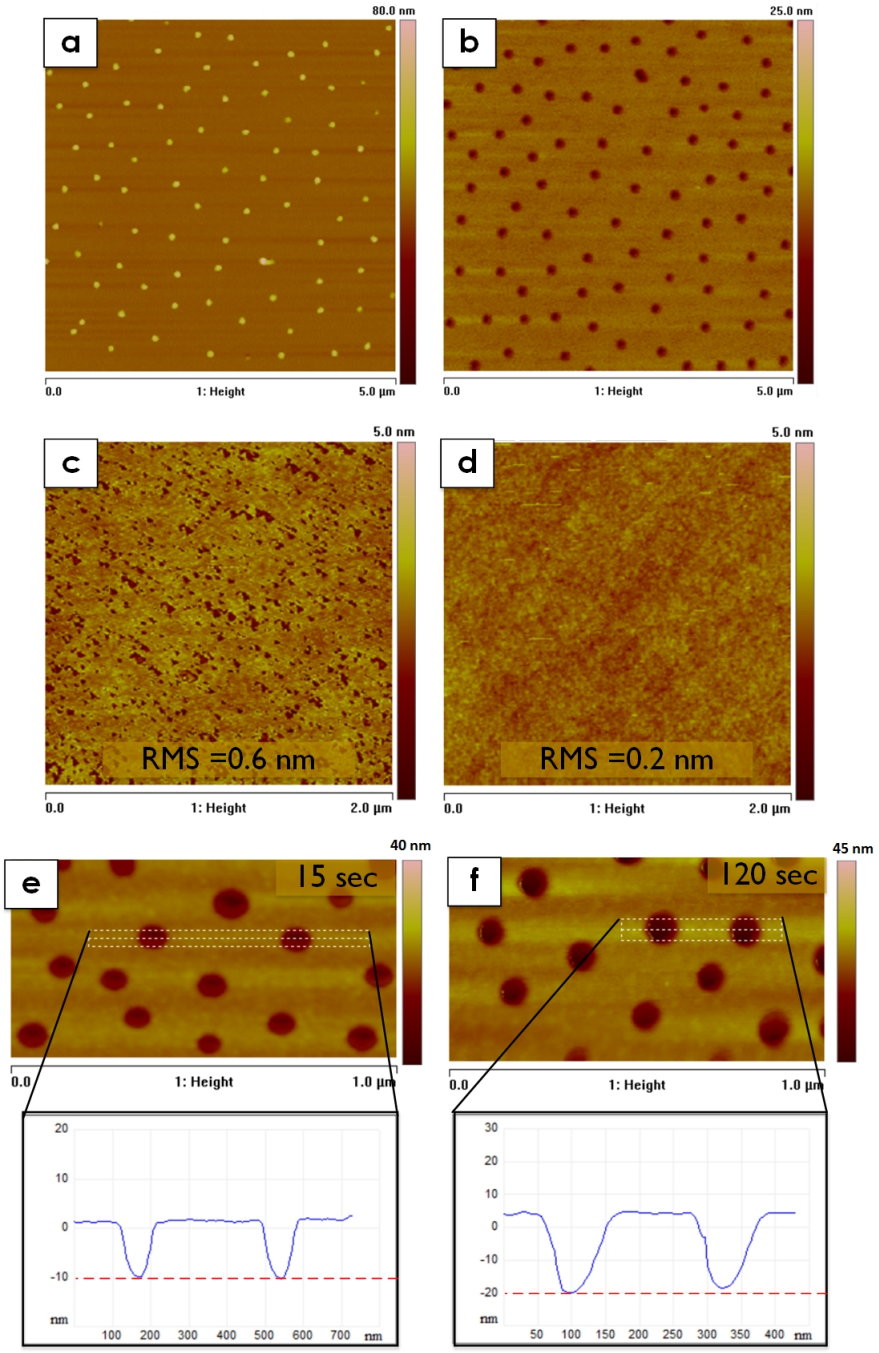

Figure 3.2: AFM images showing height data for different types of samples characterized in this work:(a) PS nanospheres adsorbed on Si/SiO_2 substrates, (b) nano-apertures in an oxide layer on a Si substrate, (c) 15 nm evaporated SiO_2 thin film on Si, (d) 15 nm dry-thermal oxide film on Si, and (e), (f) 80 nm large nano-apertures in SiO_2/Si etched for 15 and 120 s, respectively.

3.2 Scanning Electron Microscopy

The earliest renowned work explaining the SEM concept was in 1935 by M. Knoll [56] and then SEM witnessed a lot of critical improvements. SEM is considered a versatile non-destructive technique for the examination of a variety of materials. SEM utilizes electrons to image specimens allowing the very closely spaced fine features to be magnified at a high resolution down to few nanometers with a large depth of field. The wavelength of an electron can be up to 100,000 times shorter than the visible light photons, achieving much higher resolution and larger magnification whereas most optical microscope are limited by diffractions. SEM micrographs are monochromatic grey-scale images that display maps of intensity information from the detected electrons from the specimen surface. The darkest (black color) pixels represents the weakest intensity of electrons and the brightest (white color) represents the highest intensity. SEM depends on an electron beam that is ejected from an electron gun at the upper part of the microscope following a vertical path where there are magnetic lenses and electromagnetic lenses that focus the beam under UHV on the mounted sample. An applied acceleration voltage allows the electron beam to hit the sample and penetrate it. Accordingly, photons (x-ray photons, photons of visible light) and electrons (secondary electrons (SE), back scattered electrons (BSE), and Auger electrons) are ejected from the sample, detected and converted to an image displayed on a computer screen. Figure 3.3 shows a schematic diagram of the SEM system and its main components as well as a diagram for the sample when an electron beam is focused on the sample and particles are ejected from it.

In the framework of this thesis, a Zeiss Supra 60 VP SEM was used to image a variety of samples of nanospheres and NWs at a high resolution down to a few nanometers with magnifications up to 3 Mx. Top-view and tilted images were taken at an 'in lens' mode to fully characterize the samples as shown in figure 3.4. The in lens mode enables characterization of samples based on detection of secondary electrons. The efficiency of this mode depends on the working distance from the specimen surface which is determined based on the used acceleration voltage and

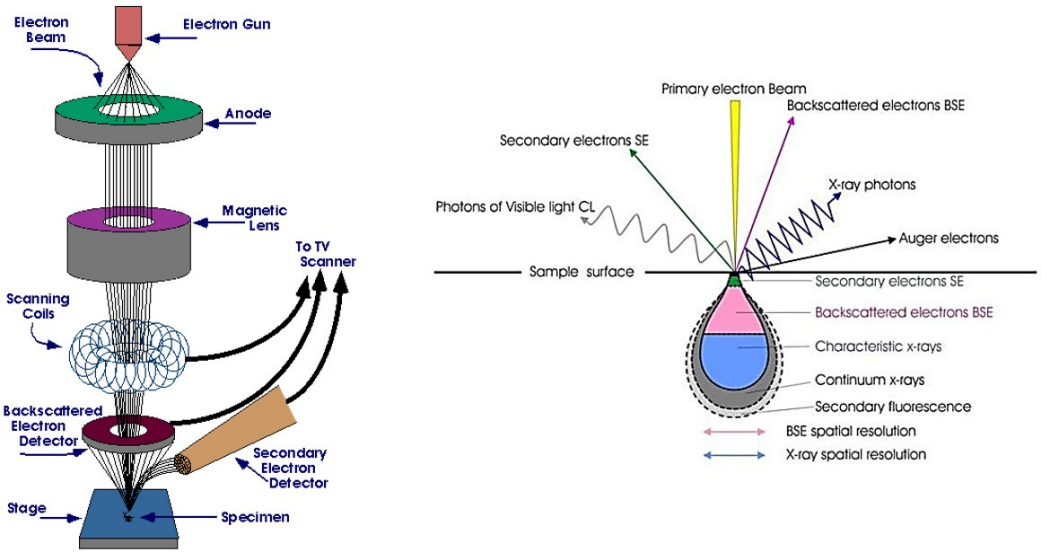

Figure 3.3: A schematic diagram developed by Iowa state university [4] explaining the SEM setup is shown on the left side with an anatomical description of the specimen surface when it is hit by an electron beam and electrons and photons are ejected on the right side.

the geometry of the specimen. To characterize NWs in this work, very small working distances (WDs) were used in combination with acceleration voltages ranging from 3 to 15 Kv. Higher acceleration voltages results in higher resolution images in case of metal specimen and conductive surfaces. However, lower acceleration voltages are more suitable for non-conductive samples due to the surface charging. Therefore, there is a trade-off between the WD in combination with the acceleration voltage a specified specimen. Conductive samples don't require any special preparation prior to imaging, whereas for non-conductive samples it is better to coat the surface with a very thin metal layer for a better image quality. In this work, substrates with adsorbed PS nanospheres or nanoholes pattern were sputter-coated with a 5 nm thick aluminum (Al) layer however InAs NWs were imaged as grown without any metal layer being sputter-coated. As for the tileted SEM images of the NWs, they show the projection (H_{proj}) of the grown NWs.

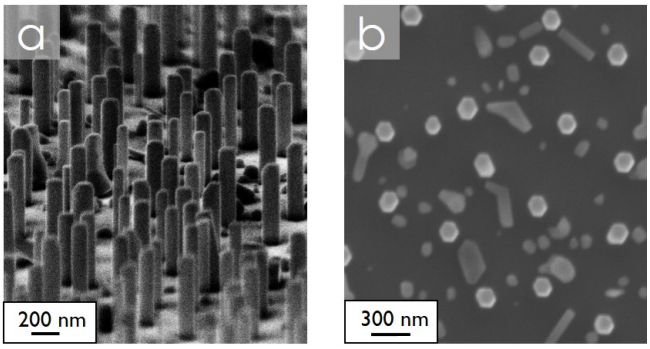

Figure 3.4: SEM images of an InAs NWs sample measure in 'in lens' mode (a) with a 75 deg. tilt and (b) top view.

3.3 Ellipsometry

In 1988, Paul Drude was the first to use the change in polarization of a light beam reflected off the examined sample to characterize thin film properties such as measuring film thickness [57]. Later, in 1945, Alexandre Rothen featured the word 'ellipsometer' for the first time in his published paper entitled "The ellipsometer: an apparatus to measure thickness of thin surface films" [58]. Since then, spectroscopic ellipsometry was greatly developed to provide a high sensitivity to measure nanometer-scale films. Nowadays, ellipsometry has become a powerful optical technique for characterizing thin film materials and surfaces. It can be used to investigate optical constants, film thickness (single or multilayers), doping concentration, roughness, crystallinity and other physical quantities with sub-monolayer resolution by analyzing the reflected light off the sample.

Ellipsometry measurements are based on a setup comprised mainly of a light source, a polarizer, an analyzer and a detector as shown in the simplified schematic in figure 3.5 (a). The light source generates unpolarized light that is linearly polarized when passes through the polarizer. Afterwards, the linearly polarized light interacts with the sample, causing change of the polarization state of the reflected light off the sample. Then the reflected light passes through a continuously rotating polarizer, namely the analyzer, to modulate the intensity of the passing light which will

be detected afterwards with the detector. The detector converts the detected light to an electronic signal such that fourier analysis of the detected light phase and amplitude yields the ellipsometric angles Δ and ψ.

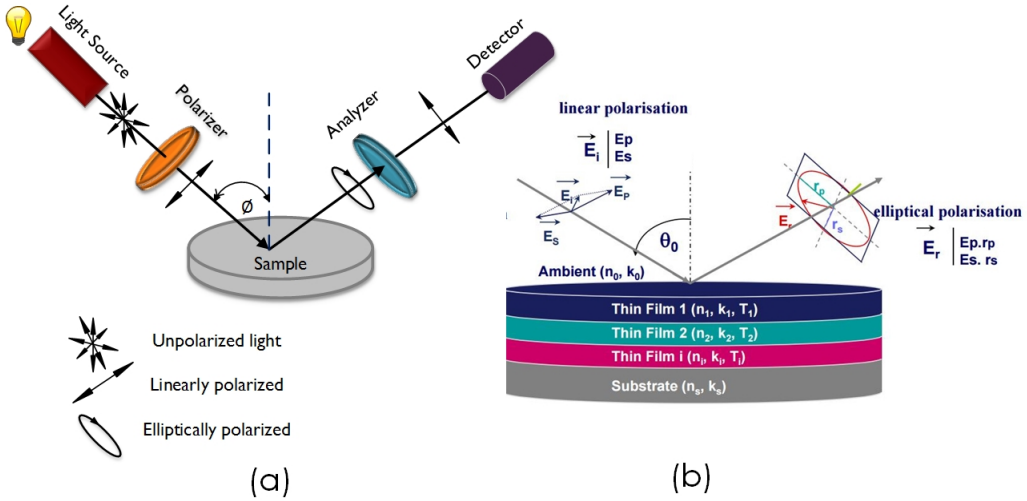

Figure 3.5: Simplified schematics illustrating (a) the ellipsometry measurement setup and (b) the anatomy of the characterized sample (schematic in (b) is a courtesy of EPFL University).

Ellipsometry is based on measuring the change in the polarization state of light, reflected off or transmitted through the sample. Figure. 3.5 (b) is a schematic diagram showing the measurement principle. The incident light beam is linear in its components (s and p) and the reflected beam is polarized and has undergone changes. The physical quantities of interest are expressed in terms of the ellipsometric angles ψ and Δ. Conceptually, ellipsometry measurement proceeds as follows, optical response of the thin film is spectroscopically scanned with a range of angles and Δ and ψ are collected versus wavelength and spectroscopic angles. Then one have to propose a layered structure model for the examined sample with an estimation of the thickness of each layer. Afterwards, the calculated response from the model is fitted iteratively till they match the experimental data as shown in figure 3.6. The difference between the fitted response from the model and the experimental data is quantified by the mean squared error (MSE) such that the smaller the MSE the better the fit. Therefore, we can conclude that ellipsometry is an indirect characterization technique such that the physical parameters are not directly provided after

measurements.

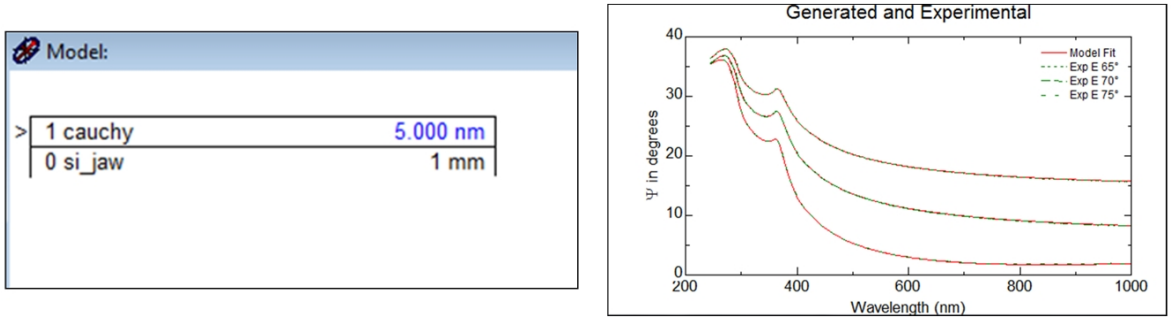

Figure 3.6: The image on the left side explains the proposed model for the layered structure of a SiO_2 thin film on a Si substrate characterized in this work by ellipsometry and on the right side an image showing the generated and experimental data on the same plot.

Figure 3.7 illustrates the process flow of ellipsometry measurements and data analysis which is divided basically to four main steps: measuring, constructing the model comprised of the layered structure to be investigated (i.e. substrate, film1, film2...etc). In this work, Variable Angle Spectroscopic Ellipsometer (VASE) from

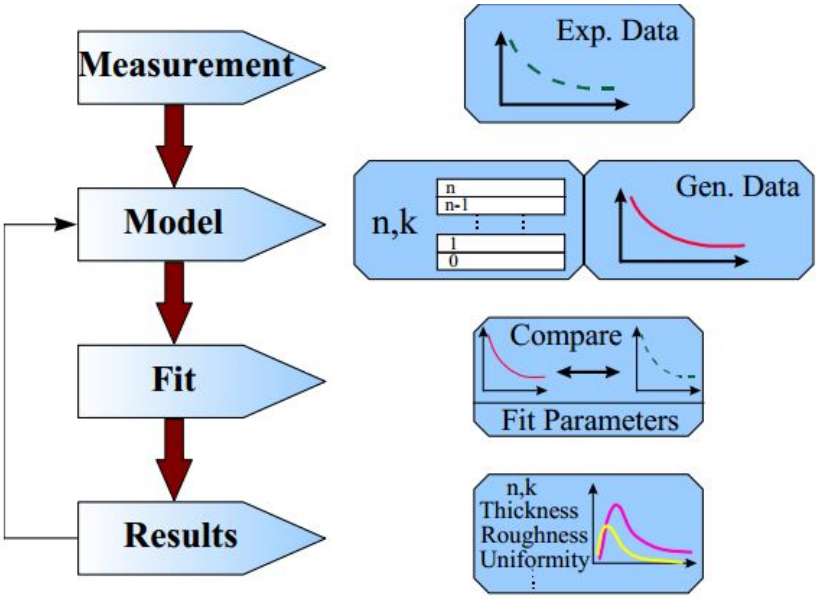

Figure 3.7: A flow chart from [5] that illustrates the basic procedures followed for ellipsometric measurements to extract material properties.

J. A. Woollam was used allowing the variation of angle of incidence utilizing the

computer system. For this work, ellipsometry was used to measure SiO_2 thin films thickness deposited on Si substrates. An incidence angle of 70^o was used and spectroscopic scan angle range of 65^o to 75^o with offset of 5^o at a scan rate of 50 rev/meas. The model used to fit the optical constants for SiO_2 is the Cauchy model, see Eq. 3.1. The three constants (A,B,C) are fitted to match the refraction index (n) as a function of the wavelength (λ) :

$$n(\lambda) = A_n + B_n/\lambda^2 + C_n/\lambda^4 \tag{3.1}$$

4

Colloidal Lithography for Nanoholes Pattern on Si

In the framework of this thesis, MBE growth of catalyst free InAs NWs was achieved on patterned Si (111) substrates utilizing Colloidal Lithography (CL) and Hole-Mask Colloidal Lithography (HCL) techniques. In this chapter, patterning the Si substrates via CL and HCL techniques and the influence of the patterning process on the quality of the NWs growth are presented. Moreover, the challenges of these techniques along with suggestions on how to improve the patterning process will be discussed. The results discussed in this chapter are based on the results published in the paper and the poster appended at the end of this thesis.

4.1 Colloidal Lithography

CL is a novel bottom-up lithography technique which uses self-assembly of surface-charged nanoparticles onto a substrate pre-coated with a thin polymer film providing a net charge opposite to that of the particles. Therefore, there is a repulsive electrostatic interaction between the particles and an attractive substrate-particle interaction as illustrated schematically in figure 4.1. The result of the coexistence of these two interactions is a non-periodic pattern with a short range order. A nanoholes pattern can be obtained by evaporating a thin mask layer over the adsorbed particles and removing them through a lift-off process. This technique allows the fabrication of several kinds of nanostructures such as arrays of nanoholes, nanodiscs, nanocones, and dimers which could be used for a wide range of applications [37]. In this work

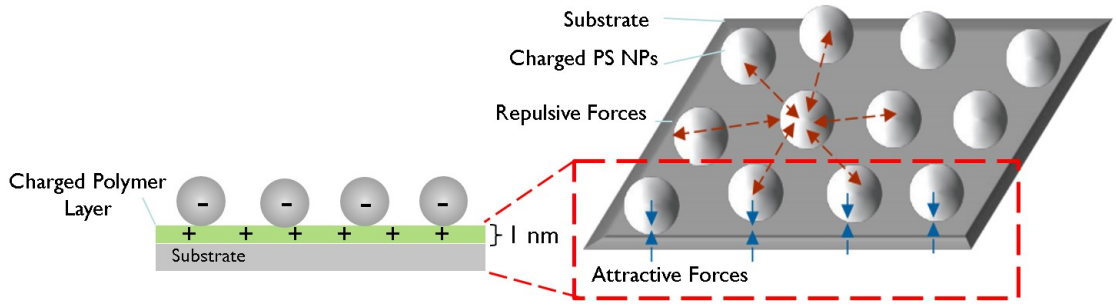

Figure 4.1: Schematic drawing showing the coulomb forces balancing the adsorption of the short-range ordered nanoparticles on the Si substrates.

the obtained nanoholes pattern is defined by the size of the particles and the subtle balance of repulsive particle-particle, and attractive substrate-particle interactions. Accordingly, the size of the final aperture patterns is determined by the size of the particles.

The nanopaticles and nanoholes patterns SEM images in this work were analyzed with ImageJ software [59] to extract the nanoparticles size, surface coverage (SC) and inter-particle spacing (IPS). To analyze the particles, the nanoparticles (black) are selected from the background (white) on a black and white scale via 'color thresholding' function, see figure 4.2. The nanoparticles diameter accordingly was calculated from the extracted particles area. Also, IPS is evaluated using the nearest neighbor distance 'NND' function in the ImageJ software measuring the nearest neighbor distance between the centroids of the particles. Additionally, SC was extracted by calculating the nanoparticles surface coverage and dividing it by the total sample area.

4.1.0.1 Colloidal Lithography for Nanoholes Pattern

2-inch Si wafers with crystallographic orientation (111) cleaved in quarter samples were used for all the experiments. The substrates were first cleaned using the standard cleaning RCA recipe (SC1/SC2) that is, removal of organic contamination, removal of thin oxide layer, and an ionic clean (for details, refer to appendix A.1). Afterwards, the substrates were treated in light oxygen plasma (50 W - 250 mTorr

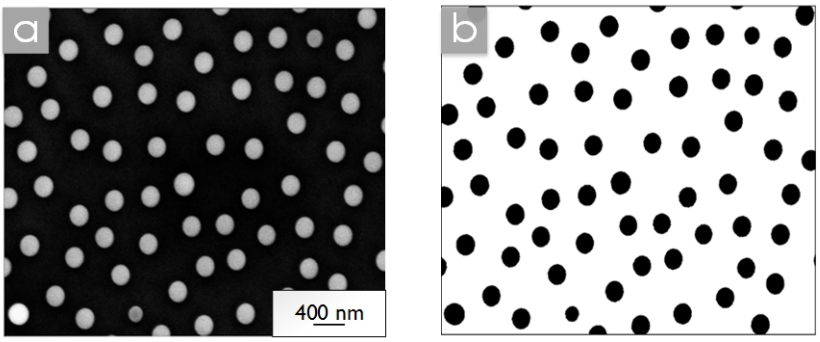

Figure 4.2: Extracting the nanoparticles properties in ImageJ by color thresholding the SEM image of the analyzed particles (a), and selecting the nanoparticles of specified circularity (b).

- 30 s) in a Therm BatchTop RIE (O_2) system to enhance the polymer film hydrophilicity. These steps were directly performed before processing.The SEM images were taken in a SEM Zeiss Supra 60 VP system. In order to reduce the charging effect due to the non-conductivity SiO_2, a 5 nm thick Al layer was sputtered for the SEM measurement.

The CL technique used in all experiments in this project relies on a process adapted from [60]. The detailed pocedures are explained in appendix B.1.1. A colloidal dispersion consisting of a negatively charged polystyrene (PS) particles dispersed in de-ionized water (DI) was used to produce a 2D short-range ordered arrangement of particles. A schematic diagram in figure 4.3 illustrates the whole patterning process with SEM images for the key steps in the patterning process. First, triple layers of charged polymers comprised of polydiallyldimethylmmonium(PDDA, Sigma Aldrich, 0.2 wt % in Milli-Q water, Millipore), poly sodium $4-Styrenesulfonate$ (PSS, Sigma Aldrich, 5 wt % in Milli-Q water, Millipore), and aluminium chloride hydroxide (ACH 2 wt % in Milli-Q water, Millipore) were drop-casted on a clean Si (111) substrate to make the surface positively charged. Each polymer layer was adsorbed on the substrate, then rinsed carefully with DI water to remove polymers in excess and finally blow dried with N_2 gun. The thickness of the charged polymer layer is reported to be approximately 1 nm [60]. Then, a colloidal suspension of PS nanoparticles (sulfate latex, life technologies, 0.2 wt % in Milli-Q water, Milli-

pore) was drop-casted and adsorbed on the charged polymers on the Si substrate until surface saturation with nanoparticles was reached, then rinsed in DI water to remove the excess PS particles. Consequently, hot ethylene glycol at $150\breve{}200^oC$ (above glass transition of PS) was directly applied on the wet sample. The sample was then rinsed again with DI water and blow dried with N_2 gun from the center. This hot step leads to a partial melting of the beads onto the substrate, thereby preventing the short-range order pattern to be distorted during rinsing and drying of the sample. It is also worth mentioning that the drying step with nitrogen gun is a critical step in the process that has to be done fast and from the center to avoid disturbing the amorphous pattern with capillary forces while drying [61].

The size of the PS particles, which determines the size of the holes pattern later on, can be controlled by an O_2 plasma shrinking process, see figure 4.3 (c). The details will be discussed in section 4.1.2. After shrinking the PS particles to a desired size, a 15 nm thick layer of SiO_2 was evaporated in an AVAC HVC600 electron beam evaporator system. Then the PS particles were lifted-off by tape stripping. Afterwards, O_2 plasma treatment was used to remove the triple polymer layers. Eventually, InAs NWs were grown on the patterned Si substrates using MBE, see figure 4.3 (d-g).

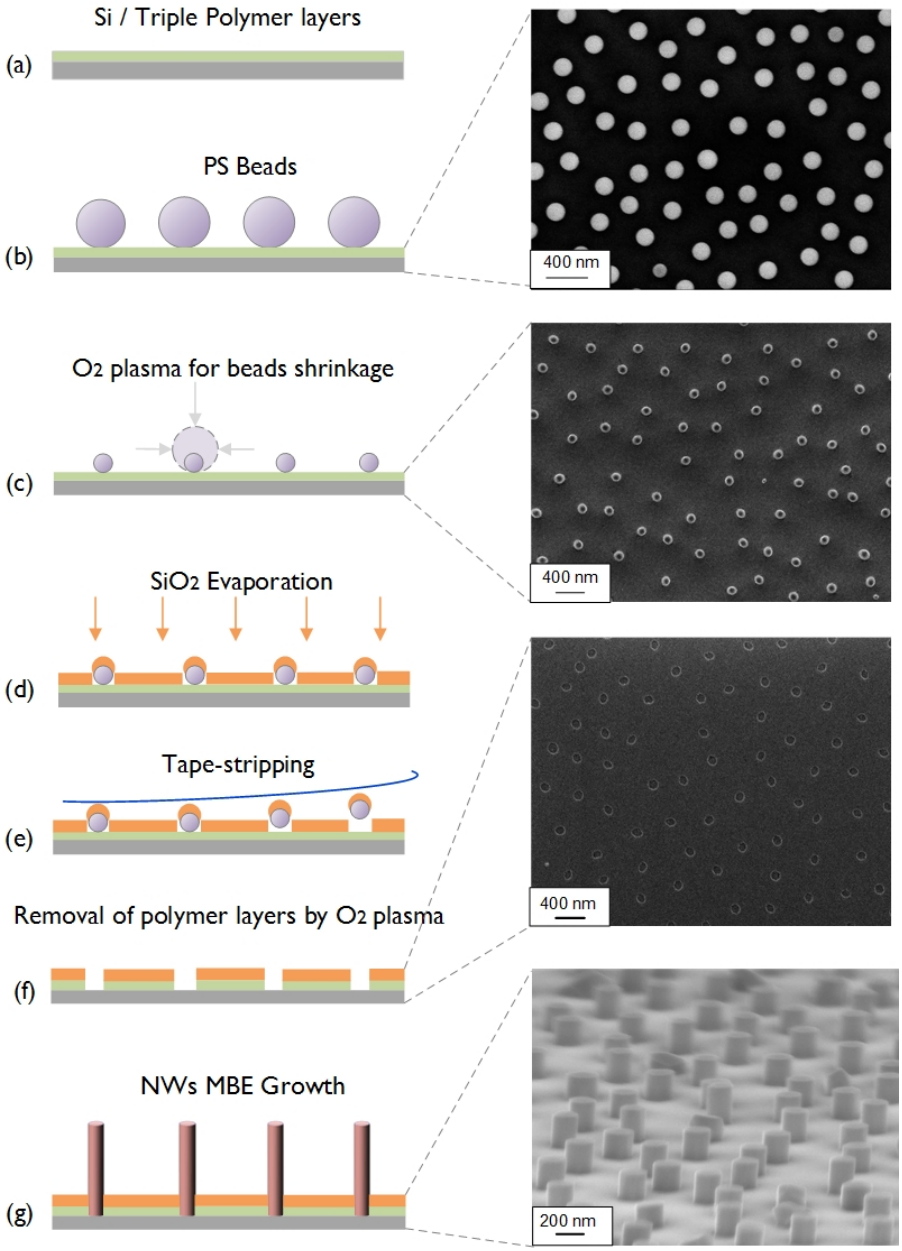

Figure 4.3: A schematic process flow demonstrating the process steps for the SAE of NWs: (a) adsorption of triple layers of charged polymers on the Si substrate, (b) adsorption of PS particles on the charged polymer layer, reducing the PS particles size by O_2 plasma treatment, (d) evaporation of SiO_2, (e) removal of the particles via tape-stripping, (f) exposing Si after PS particles lift-off by oxygen plasma treatment and (g) SAE growth of the NWs. The corresponding SEM pictures on the right column shows the morphology of the surface after each key step.

4.1.1 Density Control of the Nanoholes Pattern

The density of the nano-hole patterns, determined by the inter-particle spacing, can be controlled generally by two approaches; steric stabilization and electrostatic stabilization [62]. Electrostatic stabilization can be realized by tuning the magnitude of the electrostatic inter-particle repulsion, see figure 4.4 (a). On the other hand, nanoparticles sterically stabilized can be achieved by the adsorption of bulky moieties on the surface of the nanoparticles, effecting the inter-particle distance, see figure 4.4 (b). In this work, the former approach was used and IPS was tuned by electrostatically shielding the charges on the PS particles, which can be realized by adding salt to increase the ionic strength of the solution.

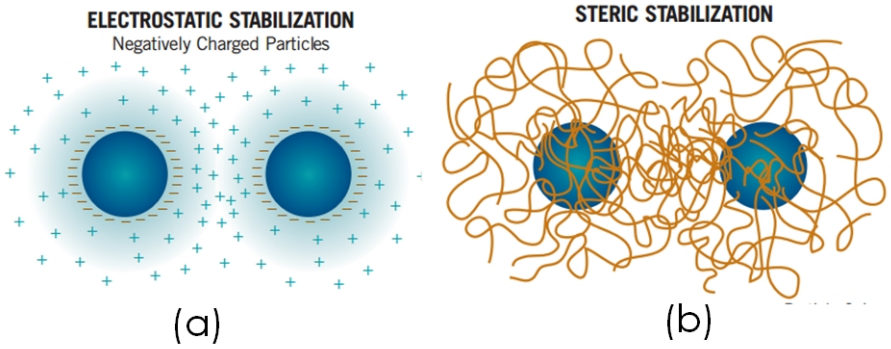

Figure 4.4: Stabilization mechanisms of nanoparticles: (a) electrostatic stabilization and (b) steric stabilization [6].

The net electrostatic effect in the colloidal solution can be described by a length scale with which we can deduce the strength of the electrostatic forces. The distance over which the charged surface of the particles is shielded from the bulk of the solution is represented by the debye length (κ^{-1}). This debye length represents the thickness of the electric double layer (EDL) which denotes the distance between the particles surface charge (-ve) and the diffuse cloud of counter-charge (+ve) in the colloidal solution as elucidated in figure 4.5. Adsorbed ions from the salt determine the surface potential which is referred to as the zeta potential (ζ) as shown in figure 4.5 (a). It is worth noting that EDL is calculated by dividing the zeta potential by the natural logarithm (ζ/e). Accordingly, electric potential that arises from the distribution of the charges in the colloidal solution is a function of the surface potential of the

particles and the debye length as expressed in the following equation:

$$Potential = \zeta \, exp\,(-\kappa x) \tag{4.1}$$

Adding salt to the solution increases the ionic strength of the solution, decreasing the double layer thickness. Thus increasing the salt concentration reduces the inter-particle spacing and decreasing the nanoparticles concentration in the colloidal dispersion will force particles to adsorb further from each other to maintain the surface saturation and keep their short-range order.

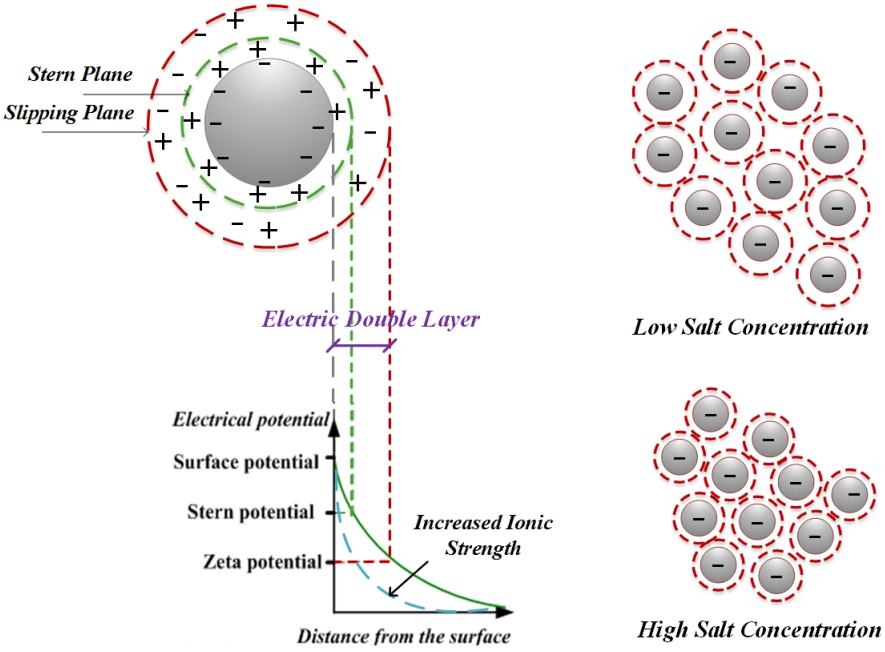

Figure 4.5: Schematics illustrating (a) the surface potential as a function of the distance from the charged surface of the particle, and (b) the salt influence on the double layer thickness and the inter-particles spacing.

To produce dense patterns, 270 nm (0.2 wt %) PS nanoparticles suspension with salt concentrations of 0, 0.25, 0.5, 1 and 1.1 mM were investigated. Figure 4.6 (a-c) shows SEM images of the nanoparticles adsorbed on Si substrates with salt concentrations 0, 0.25 and 1.1 mM. SEM images of other concentrations are not shown here. A correlation between the salt concentration and the resulting IPS and the SC is established in figure 4.6 (d). The resultant IPS and SC values are summarized in

table 4.1. Addition of 1.1 mM of Nacl to the colloidal solution achieved a total 28 % decrease in IPS and a 14 % increase in SC. An obvious decrease of IPS (22 %) is observed when adding 0.25 mM salt compared to the no added salt case. Further increase of the salt concentration (1.1 mM) leads to a smaller decrease in IPS (6 %) but also an appearance of nanoparticles aggregation.

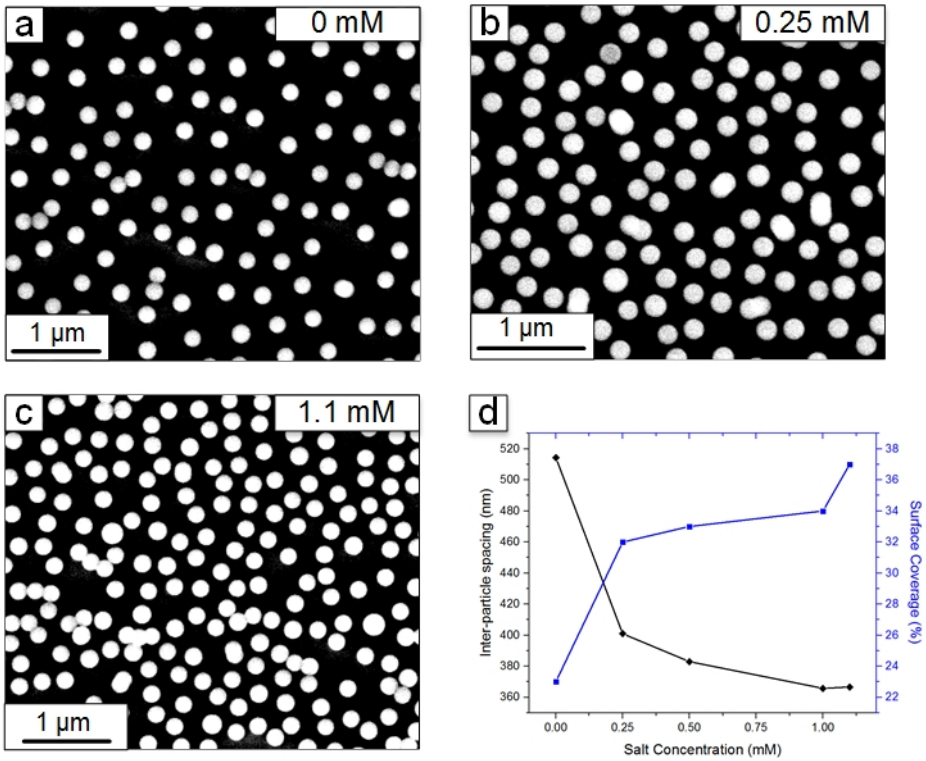

Figure 4.6: SEM images of the short-range ordered PS pattern for different salt (NaCl) concentrations: (a) 0, (b) 0.25, (c) 1.1 mM and (d) a curve illustrating IPS (black) and SC (blue) as a function of the salt concentration.

Table 4.1: Summary of inter-particle spacing and surface coverage of the PS nanoparticles as a function of salt concentration.

Concentration (mM)	IPS (nm)	SC(%)
0	514	23
0.25	401	32
0.5	383	33
1	366	34
1.1	367	37

4.1.2 Size Control of the Nanoholes Pattern

Another concern of fabricating the nanoholes pattern is the control of the aperture size, which is mainly determined by the PS particle size. Nano-sized apertures can be obtained either by using commercially available PS particles from the supplier or using plasma to shrink larger PS particles to desired sizes [63, 64]. Here, the uniformity of the pattern is the main concern while selecting the approaches in this work. First, PS particles purchased with a wide range of diameters from 20 nm up to 230 nm were investigated. Variation coefficients in diameters of 2.5 %, 8.2 %, 15 % and 14.4 % are declared by the manufacturer for the 230, 80, 40, 20 nm large PS particles, respectively. It has been found that the bigger PS particles show better uniformity in size and inter-particle spacing, complying with the declared variation coefficients as shown in figure 4.7. Nevertheless, the measured mean sizes of the PS particles are 251, 89, 51 nm for the 230, 80, 40 nm large PS particles, respectively. The size distribution of the 20 nm large PS particles is not displayed because of difficulties to analyze the SEM images due to the huge variations in size and unclear boundaries of the PS particles in the SEM images.

On the other hand, tuning nanoparticles size by plasma treatment was also investigated. Low power O_2 plasma (50 W, 250 mtorr) was used to treat 230 nm large PS particles. Figure 4.8 shows SEM images of the PS particle size as a function of

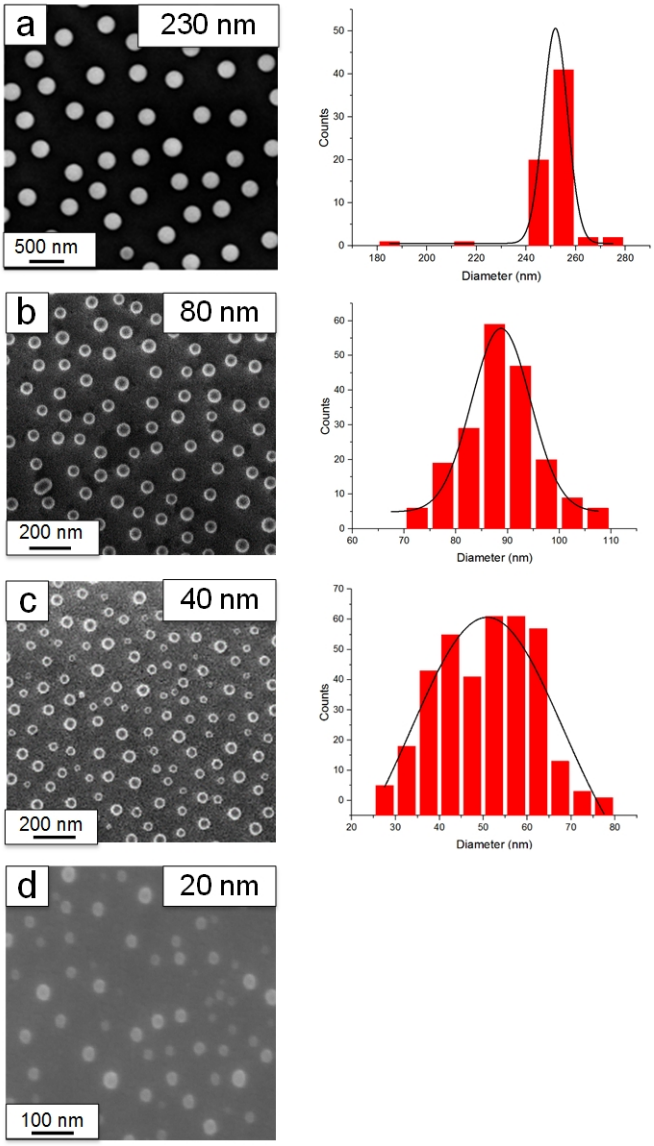

Figure 4.7: SEM images of different sizes of commercially available PS particles: (a) 230 nm, (b) 80 nm, (c) 40 nm, (d) 20 nm large particles confirming the increased polydispersity of the particles as the particles size scales down.

the O_2 plasma treatment duration, 0, 30, 60 and 135 s, resulting in mean particle sizes of 251 ± 4, 201 ± 7, 133 ± 12 and 50 ± 8 nm, respectively. As illustrated in figure 4.8, the O_2 plasma treatment allows high control over both the PS particles size and the inter-particle spacing. In particular, for 135 s of O_2 plasma treatment, we demonstrate a particle distribution with a coefficient of variation of diameter of 12.5 %, to be compared to 15 % for commercially available particle solutions with comparable mean particle size (41 ± 6 nm) [65].Therefore, instead of using com-

mercially available small PS particles, this approach was selected for the nanoholes pattern fabrication.

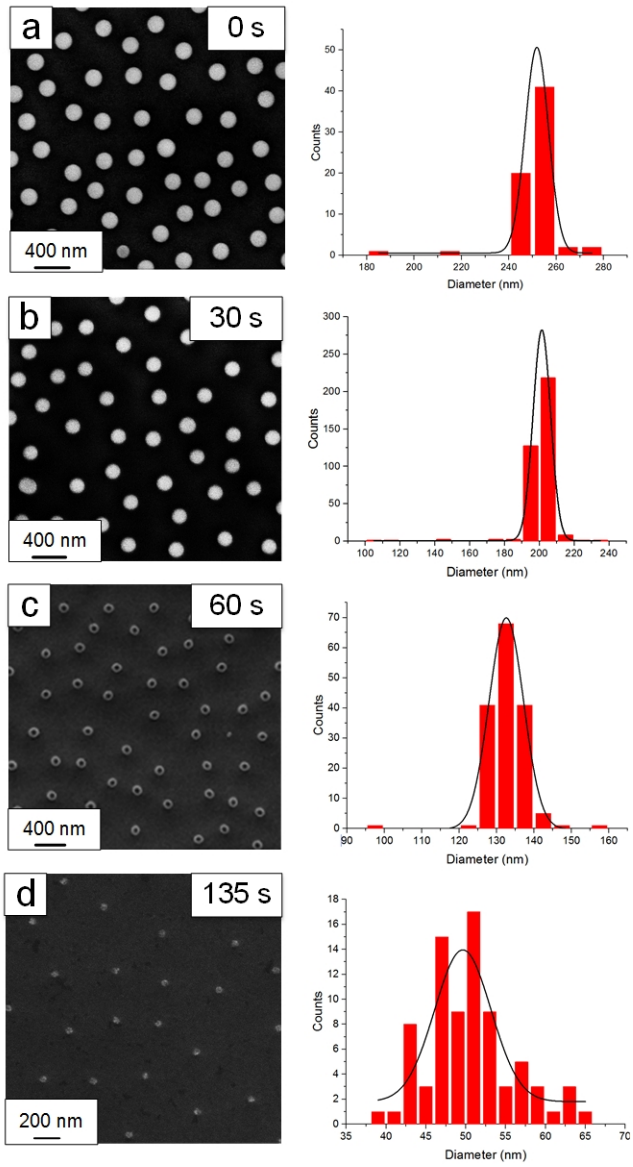

Figure 4.8: SEM images of PS particles after the O_2 plasma treatment for (a) 0 s, (b) 30 s, (c) 60 s and (d) 135 s, respectively. The correspondent size distribution of the adsorbed PS particles is shown on the right side.

4.1.3 Challenges of Colloidal Lithography in Patterning Si Substrates

CL proved to be an inexpensive novel bottom-up technique that enables patterning large areas of substrates in a time efficient manner. However, the technique used in this work has some limitations and challenges that need to be thoroughly investigated. These challenges are summarized as follows:

- **Quality of the Evaporated Thin Film Mask**

  In order to transfer the short-range ordered nanoparticles pattern to a nanoholes pattern on the Si substrates, a thin film layer is deposited on top of the nanoparticles layer and then the nanoparticles are removed via tape-stripping. For the particles lift-off process, evaporation enabling a directional thin film deposition is the most suitable technique than other techniques (e.g. thermal oxide, sputtering, chemical vapor deposition, ... etc) yielding a better off cut profile as illustrated in figure 4.9. However, the quality of the evaporated SiO_2 layer in an AVAC HVC600 system is very poor.

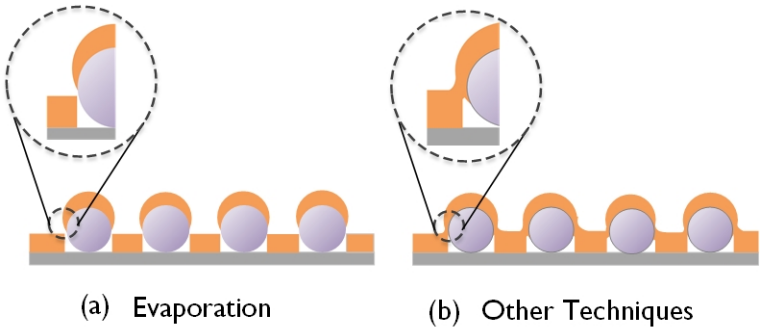

Figure 4.9: A schematic drawing shows step coverage around PS nanoparticles by SiO_2 fabricated by (a)evaporation and (b)other thin film deposition techniques.

AFM images in figure 4.10 confirm the low quality of the evaporated SiO_2 mask layer in comparison to a very high quality oxide obtained by dry thermal oxidation. The root mean square (RMS) roughness for a 15 nm thick

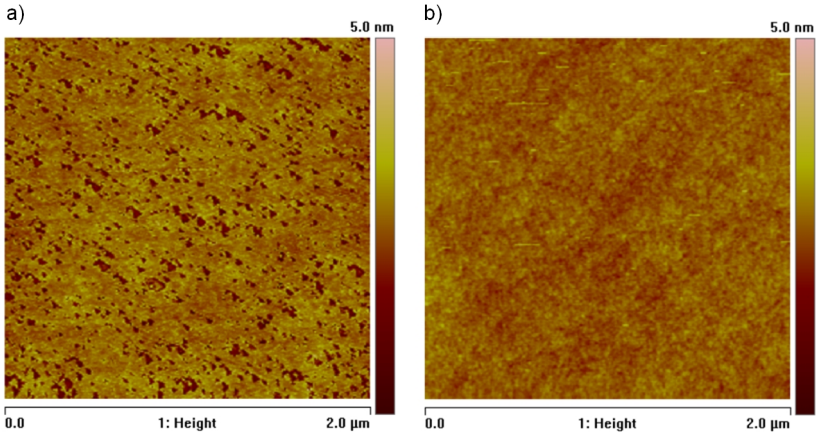

Figure 4.10: AFM images for (a) 15 nm thick evaporated SiO_2 thin film and (b) 15 nm thick dry-thermal oxidized SiO_2 film, featuring RMS roughness of 0.57 and 0.21 nm, respectively, over a 4 μm^2 scan.

SiO_2 obtained by evaporation -as in this study- is 0.6 nm, and for the thermal oxidized SiO_2 is 0.2 nm over a 4 μm^2 scan. As evidenced through the AFM measurements, native pinholes in the evaporated SiO_2 layer and pits on the rough surface can provide extra nucleation sites for the NW growth outside the patterned apertures, this effect on the growth will be presented in chapter 5. The quality of the SiO_2 layer needs to be improved by using other deposition techniques which may ruin the lift-off process. Therefore, a modified CL process was developed to overcome the bad quality of the evaporated SiO_2 which will be presented in section 4.2.

- **Shape Deformation of the Shrinked PS Particles**

Though the shrinkage process of the PS particles using O_2 plasma has shown to be an effective way to tune the particle size while maintaining the uniformities in the particle size and inter-spacing, it also deforms the particles. And the deformation becomes more serious with longer O_2 plasma treatment. This deformation limits the proper lift-off process of the nanoparticles especially for the particles treated with a longer time. Figure 4.11 shows SEM images of 230 nm PS particles after a 60 s O_2 plasma treatment and the correspondent nanoholes pattern.

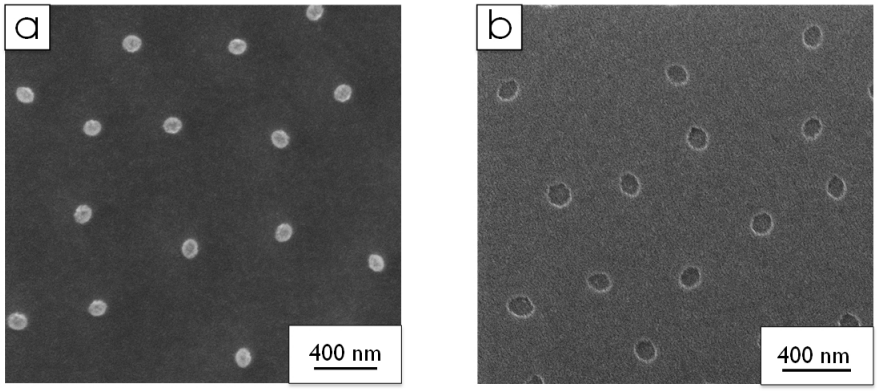

Figure 4.11: SEM images for (a) 230 nm PS particles after a 60 sec O_2 plasma treatment and (b) corresponding nanoholes pattern.

Figure 4.12 illustrates the nanoholes patterns corresponding to particles shrinked with different durations of plasma treatment. With 60 and 70 s plasma treatment, successful lift-off process without any PS residue was obtained, see figure 4.12 (a and b). With a longer treatment time (>80 s), remaining PS residues were observed in the nano-apertures patterns , see figures 4.12 (c-f). To solve the problem, in addition to tape-stripping physical removal with a sponge bud or a clean room paper was applied. As shown in figure 4.13, clean nanoholes pattern was obtained by using physical removal even for the 135 s plasma treated particles. Physical removal is not harmful to the SiO_2 layer since SiO_2 is hard enough and is not affected by gentle rubbing.

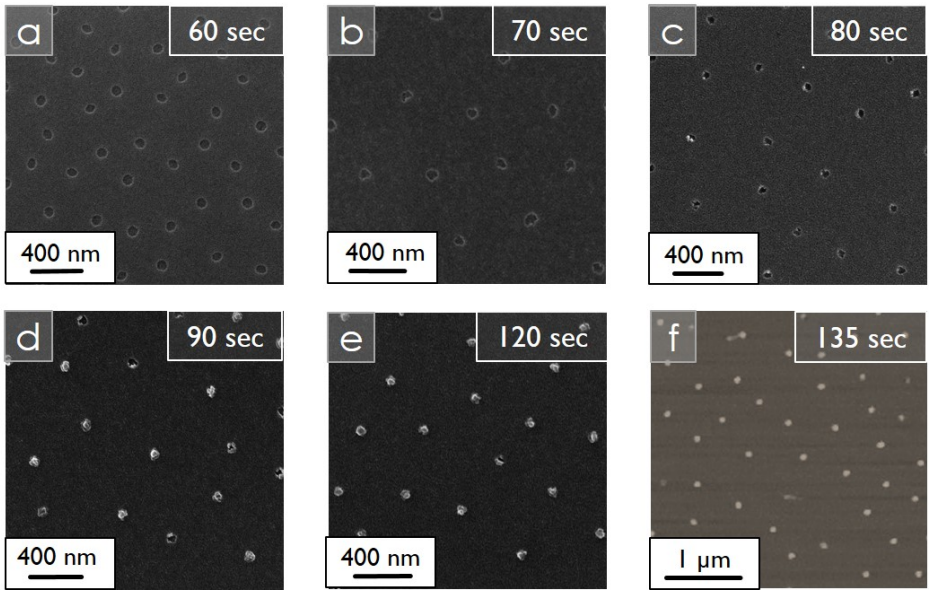

Figure 4.12: SEM images of the nanoholes patterns corresponding to particles shrinked with different durations of plasma treatment (a) 60, (b) 70, (c) 80, (d) 90, (e) 120, (f) 135 s.

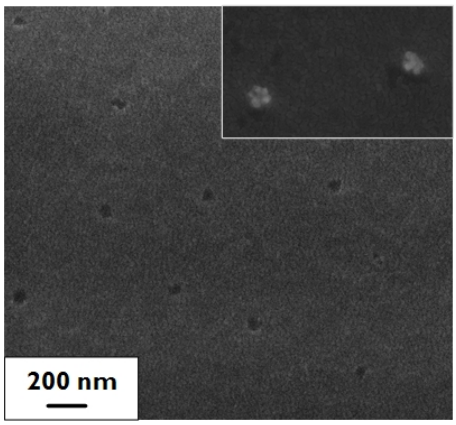

Figure 4.13: SEM image for a nanoholes pattern corresponding to a 230 nm PS particles exposed to O_2 for 135 sec and the PS remnant residues were removed physically by a clean room sponge bud. Inset shows an SEM image for the corresponding deformed nanoparticles pattern that hindered lift-off by tape-stripping.

4.2 Hole-Mask Colloidal Lithography

In spite of the several advantages realized by CL and the variety of nano-sized structures produced by this technique, it suffers from the very low quality

of the evaporated SiO_2 layer which may be challenging for obtaining NWs with high growth selectivity, which will be discussed in chapter 5. Therefore, an adapted process of hole-Mask colloidal lithography (HCL) technique, developed by Fredriksson et. al [37] is used to mitigate the aforementioned challenge posed by CL. In the HCL approach, the nanoparticles pattern is formed on top of a high quality SiO_2 layer, which can be fabricated by either oxidation or thermal oxidation. Then this nanoparticles pattern is transferred to a nanoholes pattern in a thin metal layer, which later is used as an dry etching mask to form a nanoholes pattern in the beneath SiO_2 layer. Finally, the metal mask layer is removed using selective etching, leaving a nanoholes pattern in the SiO_2 layer. Figure. 4.14 shows the key steps of the HCL process.

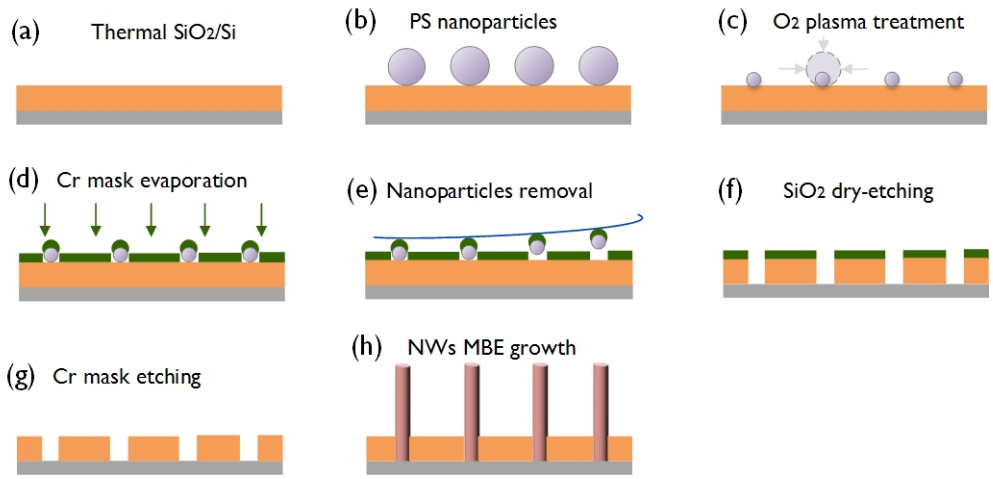

Figure 4.14: Schematic diagram for the key steps of HCL technique: (a) deposition of 20 nm thermal oxide on Si, (b)formation of PS nanoparticles monolayer, (c) O_2 plasma treatment, (d) Cr evaporation, (e) nanoparticles removal, (f) SiO_2 dry-etching, (g) Cr mask removal, and (h) NWs MBE growth.

The experimental procedures are explained in details in appendix B.1.2 . First, Si substrates are cleaned. Then, they were dry thermal-oxidized in a furnace for 20 min at 950 ^oC to obtain a 20 nm thick SiO_2 layer on Si (111) substrate. Positively charged triple layers of polymers (PDDA, PSS, ACH) with the same specifications as in the CL technique discussed in section. 4.2 were drop-casted

on the Si/SiO_2 substrates, rinsed under DI water and blow dried with N_2 gun. Subsequently, the negatively charged PS nanoparticles solution was drop-casted on the charged polymer layer resulting in an amorphous 2D arrangement of the PS nanoparticles. The adsorbed PS nanoaprticles were treated with O_2 to shrink it to the size of interest. Afterwards, a 10 nm of chromium (Cr) acting as a hard mask was evaporated on the adsorbed PS nanoaprticles monolayer. To transfer the nanoparticles pattern into a nanoholes pattern in the underlying deposited SiO_2 layer, a series of steps were followed. Firstly, the nanoparticles were lifted-off via tape-stripping. Then the substrate was loaded in an Oxford Plasmalab 100 inductively coupled plasma/reactive ion etcher (ICP / RIE) system to dry-etch the SiO_2 layer leaving a few nanometers of SiO_2 so as not to damage the underlying Si substrate. The remaining thin SiO_2 layer was eventually wet-etched with BOE. Figure. 4.15 shows the resulting nanoholes pattern produced by HCL.

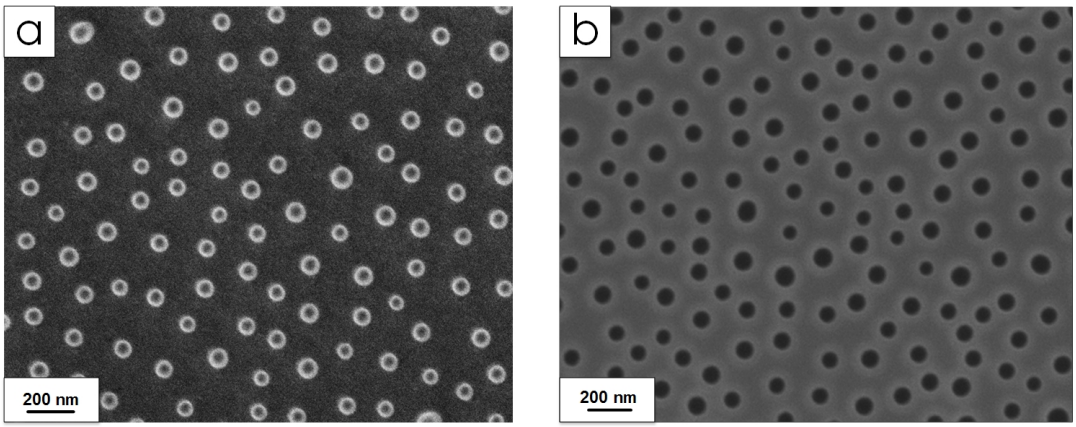

Figure 4.15: SEM images of (a) plasma treated 80 nm large nanoparticles on SiO_2/Si and (b)the corresponding nanoholes pattern transferred to SiO_2/Si by HCL with a Cr mask on top of it.

As illustrated in figure. 4.15, the nanoholes pattern was successfully transferred to the underlying SiO_2/Si substrate. Yet, the Cr mask was not successfully wet etched. We have investigated the possible reasons. However, we couldn't reach a solid conclusion within the time-frame of the project. Therefore, future

work should focus on tackling the problem of the hard mask lift-off. Despite the challenge of removing the Cr, We have proved in this study that oxide layer quality can be improved by replacing the evaporated SiO_2 with the thermal SiO_2 as evidenced by the AFM images in figure. 4.10.

5

Epitaxy of InAs NWs on Patterned Si Substrates Utilizing Colloidal Lithography

In this chapter, growth of short-range ordered catalyst-free InAs NWs on CL patterned Si (111) substrates is presented. The effect growth temperature on the growth is discussed here.

5.1 Experimental Procedures

The NWs growth experiments were performed in a Riber Compact C21 system. Two-inch Si (111) wafers cleaved in quarters were used for all growth runs. To ensure the removal of the native oxide layer inside the nano-apertures, the processed nanoholes template were etched with a 1:10 solution of BOE : DI for a few seconds prior to being loaded in the MBE system. The final thickness of the SiO_2 layer was around 12 nm. Then the substrates were loaded to the MBE system in the loading chamber under UHV and then transferred to the growth temperature with a robot arm. Before starting the growth, the substrate was degassed at $740\,^oC$ for 10 mins to ensure the cleanliness of the surface and removal of any remnant residues. The As flux was opened during the degassing step to protect the surface. Then the substrate was cooled down to the desired growth temperature. The growth was initiated by opening the

In shutter while the As shutter is open. The substrate is rotated throughout the whole growth at a rate of 6 rev/s for a better growth uniformity across the wafer. Finally, the growth was terminated by closing the In flux. The substrate temperature was cooled down to $200\,^oC$ under As flux. Then, the substrate was transferred again from the growth chamber to the loading chamber to be taken out of the system. All growth experiments discussed in this section were performed at different temperatures ranging from $460\,^oC$ to $510\,^oC$ at a fixed growth duration of 90 mins, an In-flux rate of 0.2 Å/s, and an As beam equivalent pressure (BEP) of 4.5×10^{-6} mbar. Figure 5.1 summarizes the growth temperature scheme for all experiments discussed in this chapter.

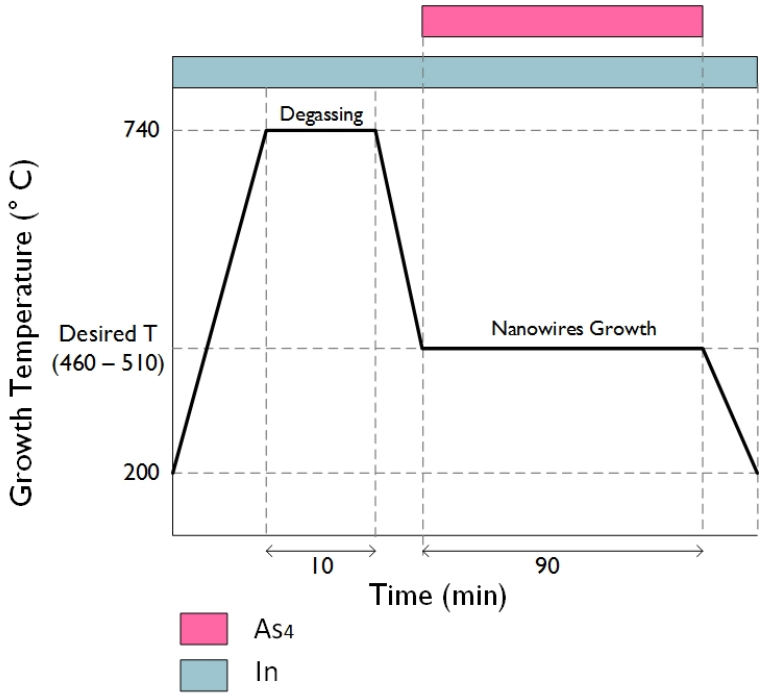

Figure 5.1: Growth temperature scheme of the NWs growth based on CL patterned Si substrates.

5.2 Selective Area Epitaxy of InAs NWs

Selective area epitaxy (SAE) on patterned substrates is essential to have control over position, size and directionality of NWs for homogenous and predic-

tive performance. In the SAE approach, substrates are usually masked with patterned dielectric layer commonly SiO_2 [66] or Si_3N_4 [67] layer with aperture sizes below 100 nm. Growth conditions are appropriately chosen to restrict the growth inside the patterned nano-apertures, which makes use of the higher sticking coefficient of the growth species approaching the semiconductor surface than those approaching the dielectric layer. In this work, selective area molecular beam epitaxy (SA-MBE) of InAs NWs utilizes Si substrates with nano-holes patterns produced by CL.

The drawing in figure 5.2 illustrates the process of selective area growth of NWs. NWs growth start when the impinging species (As/In) form critical nuclei of certain size on the semiconductor substrate, then it start spreading laterally followed by axial growth. Critical nuclei are formed when the impinging In adatoms diffuse on the surface until being restricted in the nano-apertures. In the mean while, the impinging As_4 is cracked into As_2 which gets incorporated by In in the open apertures. In spite of having two factors contributing to the growth of NWs, which are the diffusion rate of adatoms and the direct incorporation of the impinging species on the growing NWs, growth is much more dependent on the incorporated diffusing atom. Diffusivity is enhanced whereas the sticking coefficient is reduced by increasing the growth temperature. To achieve optimal selectivity, growth parameters especially growth temperature should be optimized.The following section will discuss the effect of growth temperature on the NWs geometry and growth selectivity.

5.3 Effect of the Substrate Temperature on the NWs Growth

NWs geometry, selectivity and yield are among the figures of merits upon which one can judge the growth quality. In this work, temperature is the main parameter that was optimized to obtain high aspect ratio NWs with

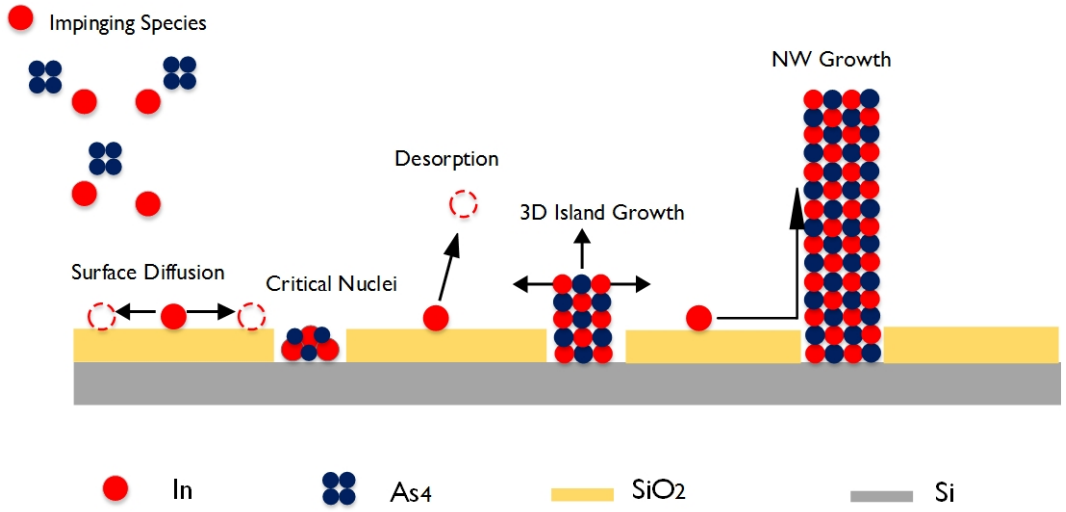

Figure 5.2: Schematic drawing illustrates the selective area growth of NWs.

good selectivity. A narrow window of growth temperature ($460 - 510\,^oC$) was investigated using templates of 149 and 50 nm large nano-apertures patterns.

Using 149 nm large nano-aperture patterns at $467\,^oC$, short NWs with a height of 300 ± 12 nm and a diameter of 127 ± 24 nm were obtained with parasitic clusters on the SiO_2 layer as in figure. 5.3 (a). Increasing the temperature up to 475^oC, selectivity was almost perfectly achieved with very few clusters among the NWs (see figure. 5.3 (c)) and resulted in shorter and fatter NWs with a diameter of 177 ± 30 nm and a height of 184 ± 21 nm. The growth at $490\,^oC$ still achieved perfect selectivity however resulted in discs instead of NWs, see figure. 5.3 (d). Further increase in the temperature yielded big clusters and few nuclei in some of the nano-apertures, see figure. 5.3 (e). Despite the fact that the influence of the nano-apertures size on the growth quality is not studied thoroughly in the framework of this thesis, one smaller-sized nano-apertures based SiO_2 / Si template were tried. Figure 5.4 shows high aspect ratio NWs at a lower temperature ($460\,^oC$) than what is used in the case of bigger nano-apertures featuring improved selectivity with a mean diameter of 109 ± 16 nm and a height of 594 ± 21 nm based on a 50 nm wide nano-apertures template.

Based on the observations drawn from the aforementioned growth runs, growth

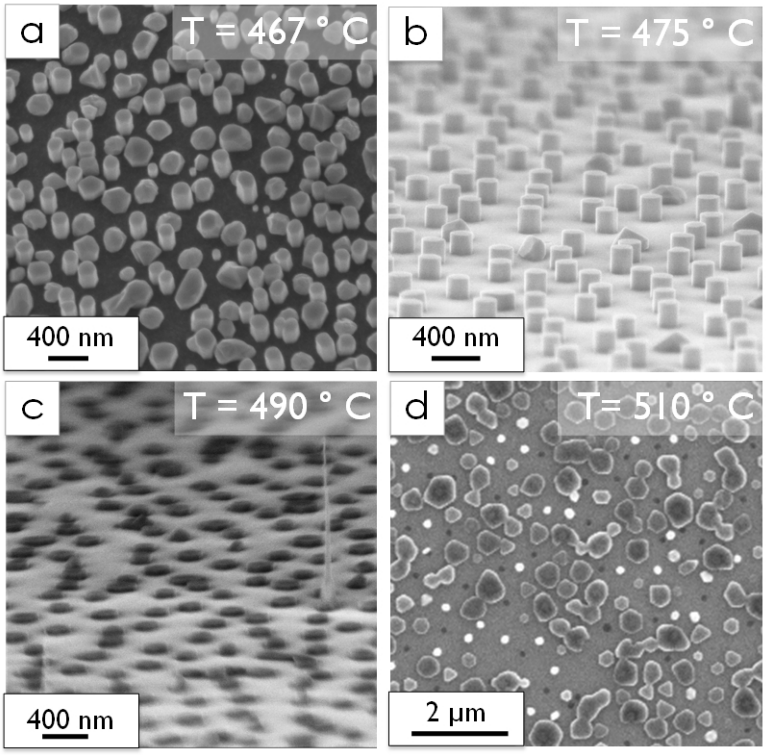

Figure 5.3: Tilted SEM images of InAs NWs grown at different temperatures (a)467 ^oC (30 deg. tilt), (b) 475 ^{o} (75 deg. tilt), (c)490 ^oC (75 deg. tilt), (d)510 ^oC (top-viw).

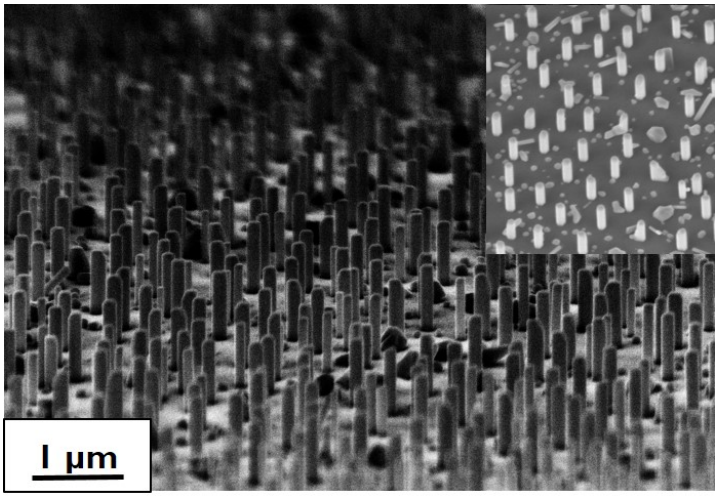

Figure 5.4: 75 deg. tilt SEM image of InAs NWs grown on small sized nano-apertures pattern at 460 ^oC. Inset- zoomed-in NWs arrays (30 deg. tilt SEM view) confirming the improved growth selectivity.

selectivity was enhanced at higher temperatures. This is because higher growth temperature (eg. $475\,^oC$) increases the diffusion coefficient of In such that it diffuses fast to the nanoholes instead of nucleating on the SiO_2 layer, and decreases the sticking coefficient leading to its desorption before nucleating on the SiO_2 layer as illustrated schematically in figure 5.5. Furthermore, the poor growth selectivity at low temperatures is due to the poor quality of the evaporated SiO_2 mask layer as previously discussed in figure 4.10. Pinholes in the $SiO2$ layer and steps/pits on such rough surface can provide extra nucleation sites during the NWs growth besides the patterned apertures, resulting in parasitic clusters. Additionally, NWs could be grown in these pinholes and not corresponding to the predefined nanoholes. In addition, With the increase of growth temperature, NWs were observed to be fatter and shorter until reaching the cases of obtaining discs (e.g at $490\,^oC$) or no growth at all (e.g. at $510\,^oC$). One can reason this by the decrease in the axial growth rate with increased growth temperature due to the higher desorption coefficient at higher temperatures from the surface of the substrate as well as the growing NWs. Moreover, the increase in the lateral growth rate results from the increased diffusion rates causing impinging species to be incorporated laterally faster and not having the time to diffuse on the sidewalls of the NWs to be incorporated axially.

As for the templates based on smaller nano-apertures, the NWs obtained at a lower temperature ($460\,^oC$) with poor selectivity confirmed the above-mentioned explanations about the reason behind the poor selectivity at low temperatures. In addition to that, the preliminary conclusion that can be drawn here, is that using small nano-apertures in combination with reduced growth temperature enables obtaining NWs with much higher aspect ratio. The lower density of parasitic clusters observed in this case couldn't be reasoned in the time frame of this work. Therefore, further experiments on templates with small size nano-apertures is still needed to reach a solid reasoning behind the influence of the nano-apertures size on the growth kinetics, quality

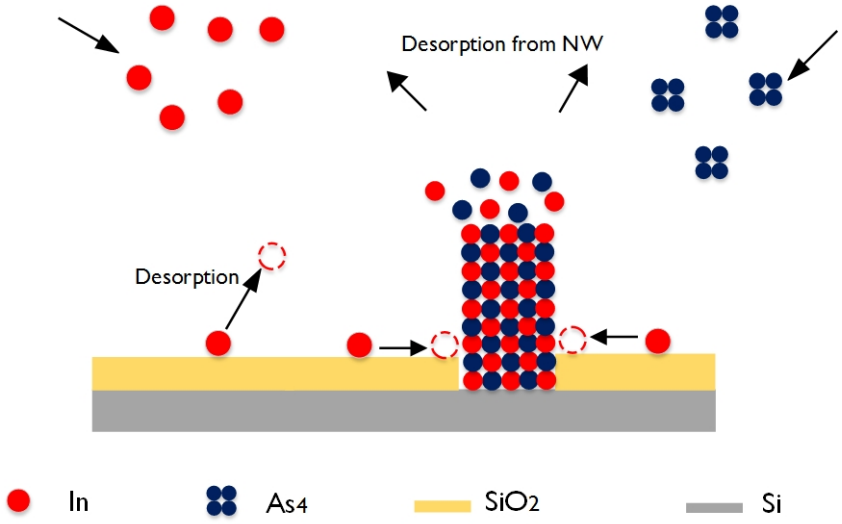

Figure 5.5: Schematic overview for the high temperature influence on the NWs growth.

and the NWs geometry.

The results reached here comply with the conclusions drawn by Simon Hertenberger in [3] concerning the SA-MBE of InAs NWs on patterned Si (111) substrates using EBL and NIL. However, the results reached in [3] seems much better than the preliminary results reached here mainly due to the poor quality of the oxide layer and the optimized growth parameters that are not tackled in this study. Therefore, growth of high aspect ratio NWs with better growth selectivity and higher aspect ratio is expected to be obtained at a lower growth temperature and a high quality SiO_2 mask layer utilizing the proposed HCL technique in section 4.14. Such bottom-up short-range ordered NWs platforms can find a direct use in energy harvesting devices based on as-grown vertical NWs with well controlled uniformity and density [68, 69]. Furthermore, the growth selectivity is not crucial in the case of NW-based transistors or biosensors usually produced on planar NW configurations, where the NWs are transferred onto another substrate [70]. The fully bottom-up approach presented here can also be deployed in applications requiring ordered arrangement of NWs by CL patterning of the long-range ordered nano-aperture arrays [71,72].

6

Growth of Non-ordered InAs NWs on Si

In this chapter, the growth of catalyst free InAs nanowires on Si (111) in a non-ordered manner is investigated. The growth is carried out on a thin grainy layer of SiO_2 on Si (111) utilizing the openings of pinholes in the SiO_2 layer to serve as nucleation sites for the NW growth. Different thicknesses of SiO_2 layers were deposited on Si substrates, and the SiO_2 layers were wet-etched down to different thicknesses, to investigate how the initial oxide layer thickness and the etching process influence the formation of pinholes and thereafter the NW growth. Other researchers used the same technique to perform optical measurements on the InAs NWs and to optimize the growth temperature. Yet, to the best of our knowledge, no work was performed to investigate the effect of the oxide thickness on the growth process.

6.1 Substrate Preparation and Growth Details

Substrates specifications and their cleaning steps are identical to what is discussed in section 4.1.0.1 and the rest of the process steps are discussed in details in appendix B.2. After the cleaning step, the Si substrates were sputtered with 10 - 30 nm SiO_2 in a radio frequency (RF) FHR MS150 system. Then, the SiO_2 layer was etched down to few nanometers (1 - 3 nm) using a buffer oxide etchant solution (BOE 10%). AFM was used to check the sur-

face morphology. Sputter deposition was selected in purpose of obtaining a granular surface which facilitate the opening of pinholes in the SiO_2 layer with wet etching. Other deposition techniques like thermal oxidation, CVD and PECVD provide smooth layers even when etched down to few nanometers. For a better illustration for the process, schematic drawings are shown in figure 6.1. The detailed steps and key parameters of processing to prepare the substrates for the non-ordered epitaxial growth of the NWs is indicated in appendix **??**. Table 6.1 summarizes the nine samples used in this study, and the RMS roughness, measured by AFM, before and after wet etching as shown in figure 6.2. The substrates were loaded directly after processing (within one hour) to the MBE under UHV environment system to prevent re-oxidation of the exposed Si in the pinholes. Here, the NWs growth temperature scheme and the growth details resembles the growth process followed in chapter 5 except that the growth here was performed at $420\,^oC$ for 60 min.

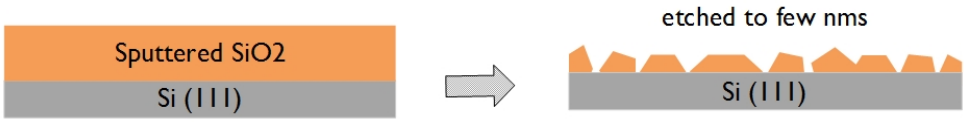

Figure 6.1: Schematic drawing of the substrate preparation process for the growth of non-ordered NWs, the pinholes are generated in the granular oxide layer when etched down to few nanometers.

6.2 Results and Discussion

Intentional production of pinholes in the oxide layer requires etching a grainy surface down to few nanometers. Wet etching is a very critical step that needs to be handled carefully since we are dealing with a very narrow window of oxide thickness (1 - 3 nm). The AFM images of the SiO_2/Si substrates before and after wet etching are shown in figure 6.2. From the AFM images, it is observed that the pinholes are of different sizes indicated by the width of the dark brown areas. For example, samples (A1 and A2) show very tiny openings

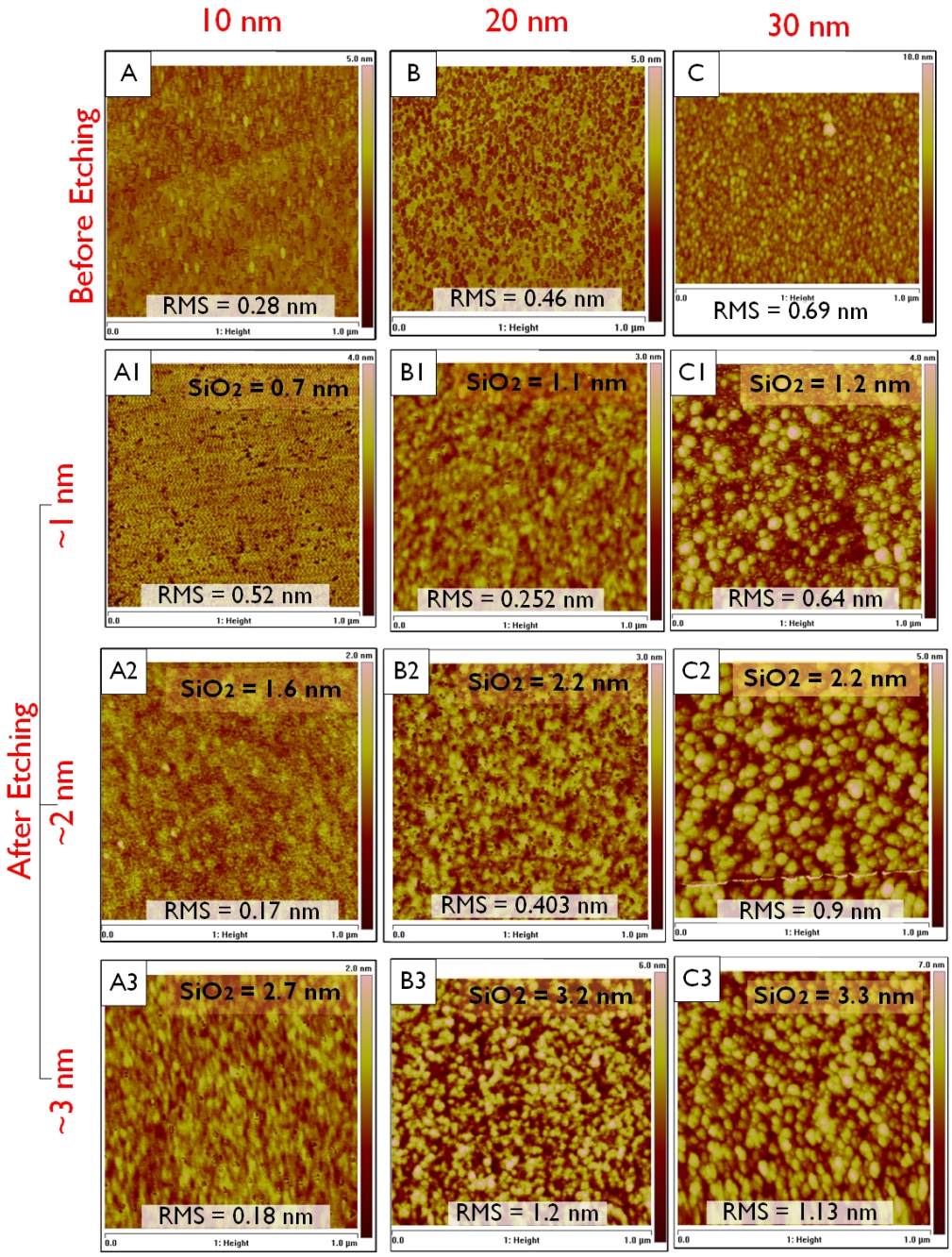

Figure 6.2: AFM images of (a-c) 10 nm, (d-f) 20 nm, and (g-i) 30 nm thick sputtered SiO_2 on Si substrates which are eventually etched down to 1, 2, and 3 nm.

in the oxide layer unlike samples (C1-C3) which have much wider openings. A general trend is that a thicker initial SiO_2 layer results in more rough surface if etched down to similar final thickness (t_f), and more rough surface

Table 6.1: Summary of the nine samples used in this study, with the initial deposited thickness of SiO_2 (t_i), final thickness (t_f) and their roughness, measured by AFM over 1 $\mu^2 scan, before$(R_{RMS})$_i$ and after $(R_{RMS})_f$ wet etching.

Sample	t$_i$(nm)	$(R_{RMS})_i$ (nm)	t$_f$(nm)	$(R_{RMS})_f$ (nm)
A1			0.7	0.52
A2	10	0.28	1.6	0.17
A3			2.7	0.18
B1			1.1	0.25
B2	20	0.46	2.2	0.40
B3			3.2	1.2
C1			1.2	0.64
C2	30	0.69	2.2	0.9
C3			3.3	1.1

is observed with thicker final thickness if the initial thickness is the same. Based on these results, the morphology of wet-etched oxide films were found to be greatly affected by the initial sputtered thickness (t_i) and the etching depth. This effect is attributed to the wet-etching mechanism of thin films. Wet-etching is known to be an isotropic etching technique, where material is etched both vertically and horizontally. Therefore, oxide etching down to very small thicknesses ($\approx$ 1 nm) especially starting from thicker films leads to the opening of large holes in the oxide layer such as in sample C1.

Top–view and side view SEM images of the grown NWs were thoroughly investigated along with their corresponding AFM images to further understand the factors affecting the growth process, see figures 6.3 and 6.4 respectively. In the top view images, NWs are distinguished by the brightest color compared to the dark-color parasitic clusters and the darkest substrate. Different morphologies are observed and can be classified to three cases: NWs with parasitic clusters, NWs with a few clusters in between and a few NWs (nanodots) only. For SiO_2 with an initial thickness of 10 nm, the NW density increases with

decreased SiO_2 final thickness. Sample A3, which feature the smallest etching depth in these batch of samples, reveal almost no growth on the surface. This is because such a shallow etching is not adequate enough and the etching depth should be above a critical thickness to generate pinholes. Considering the isotropic characteristic of the wet etching, the critical thickness is related to both the thickness and the roughness of the initial SiO_2 layer. It is easier to generate pinholes from a rough surface. Since surface roughness increases as the increase of the sputter layer, see from the AFM results, the critical thickness is increases with increased initial SiO_2 thickness. That is why in contrast to A3, NW growth was observed in B3 and C3. For SiO_2 thickness of 20 and 30 nm, the NW density first increases and then decreases with decreased SiO_2 final thickness. However, the parasitic clusters show an opposite trend. So the change in NW density is a result of competition between the NW growth and the cluster growth. If more adatoms contribute to cluster growth, the NW density will be decreased and vice versa. There are two mechanisms in this case that actuate the cluster growth: One is that the pinholes are too big and connected with each other turning out to be large opening area of bare substrate, which corresponds to Sample A1, B1 and C1 with very thin SiO_2 left on the Si substrate; another reason is the surface roughness of the residue SiO_2 layer. As discussed before in chapter 5, SiO_2 layer with rough surface provide extra nucleation sites for cluster growth. The high density of clusters observed in sample B3 and C3 are related to rough surface which is proved by the AFM results.

For a deep investigation of the NWs growth kinetics, morphology and dimensions, tilted view SEM images of the as-grown NWs in figures. 6.4 are studied. Moreover, the NWs dimensions (height and diameter) as summarized in table 6.2 are analyzed based on a statistical analysis for 40 NWs/sample. As displayed in the SEM images, there are two types of NWs that nucleate either on the clusters or the pinholes as will be discussed later. In this study, NWs nucleating on the pinholes only are considered for the statistical analysis. Concurrent with the above-mentioned discussion about the influence of the oxide

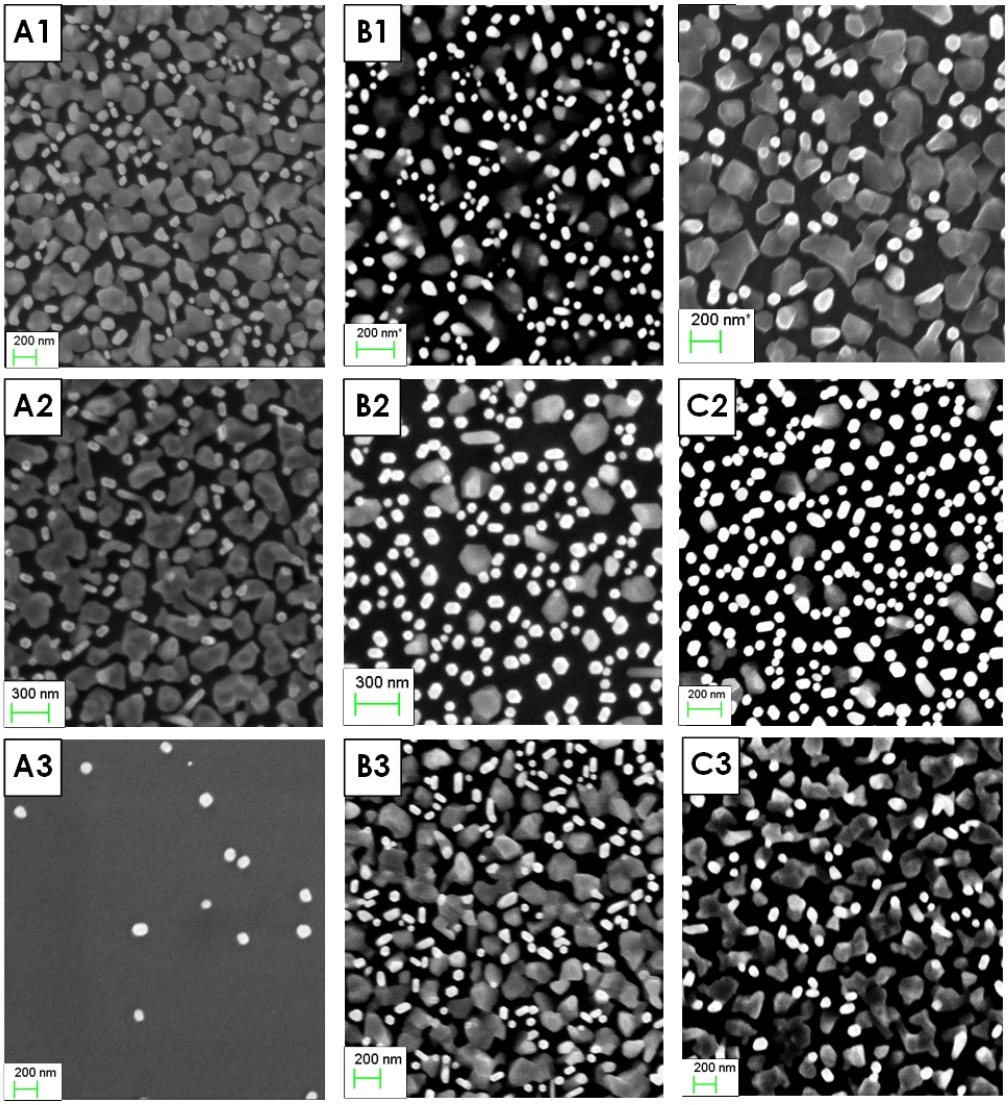

Figure 6.3: Top-view SEM images for the grown NWs on the SiO_2/Si.

layer on the growth quality, it is evidenced that the absence of the parasitic clusters promotes a high density of the NWs. The highest NWs densities (25 and 40 NWs/μm) are obtained in B2 an C2, respectively.

Growth kinetics of NWs is dependent on the inter-wire distance, which in our study depends on the density of the pinholes in the oxide layer. From the height measurements in figure 6.5, it is observed that samples B2 and C2 are of shorter NWs corresponding to other samples. Recent work conducted to examine the pitch influence on the radial and axial growth rates revealed similar results. This is ascribed to having two growth regimes, materials competition regime

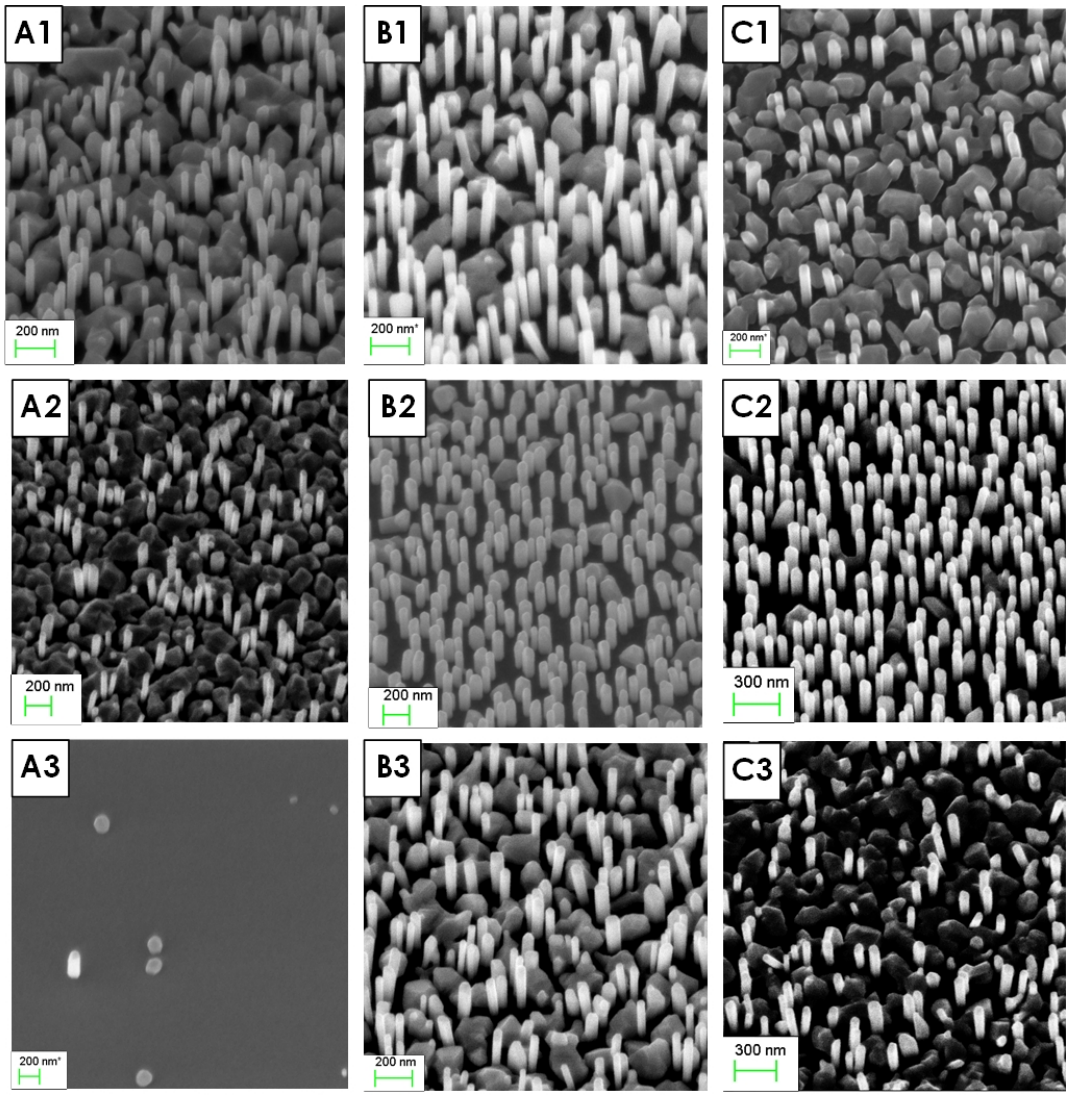

Figure 6.4: 30 deg. tilt SEM images for the grown NWs on SiO_2/Si templates of (A) 10, (B) 20, and (C) 30 nm thick oxide etched down to 1-3 nm.

and diffusion limited regime. If NWs are close to each other such that the diffusion length of adatoms is in the same order or higher than the capture area defined by half of the pitch, material is distributed among the nearby NWs leading to a decrease in the axial growth rate. On the other hand, increased pitch enhances the growth rates since each NW is no longer competing with its surroundings. Samples B2 and C2 are two exemplary cases since they are almost free of parasitic clusters. However, this explanation cannot be accurately used to explain other samples due to the existence of randomly distributed clusters which ruin the concept of inter-wire distance. This random

distribution of clusters can also explain the reason behind the great variability in the heights of the NWs more than diameters which are summarized in Table 6.2. Despite the fact that there is radial overgrowth, diameters of NWs are dependent on the size of the nuclei formed in the generated pinholes in the oxide-layer at the beginning of the growth process unlike the heights which is greatly influenced by the previously-mentioned materials competition concept which is dependent on the inter-wire distance and the clusters formation. It is worth noting that, the density measurements for the grown NWs does not reflect the same density one can see from the SEM images except for samples B2 and C2 in figures 6.3 and 6.4. This is due to the non-uniformity of the NWs positioning and distribution across the sample. Moreover, the densities reported in table 6.2 are of the NWs grown on the substrate only and it does not include the NWs nucleated on the parasitic clusters. However, samples B2 and C2 has uniform density across the whole sample and no nucleated NWs on the clusters, so they reflect the real densities.

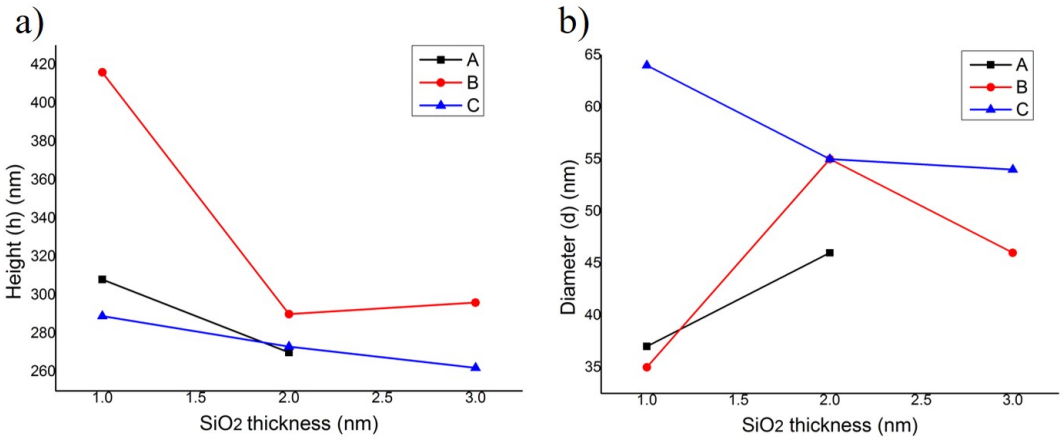

Figure 6.5: Analysis of the NWs (a) height and (b) diameter corresponding to the different oxide layer thicknesses.

Continuing on evaluating the growth quality, epitaxial growth of InAs NWs utilizing the native pinholes in the oxide layer enabled us achieve large forests of high aspect ratio free-standing NWs free of catalysts with heights up to 700 nm and diameters down to 25 nm, see figure 6.6. Although, this technique produces a high yield of free-standing NWs, there is still a possibility to get

Table 6.2: Summary of the NWs dimensions (height (h), diameter (d))and their density.

Sample	h (nm)	d (nm)	$\rho(NWs/sample)$
A1	308 ±34	37 ±19	24
A2	270 ±20	46 ±20	8
A3	-	-	-
B1	416 ±62	35 ±3	24
B2	290 ±34	55 ±18	25
B3	296 ±61	46 ±11	12
C1	289 ±109	64 ±21	10
C2	273 ±91	55 ±8	40
C3	263 ±91	54 ±16	7

unintentionally tilted NWs which are mostly nucleated on the oxide layer or on the parasitic InAs clusters. Nucleation away from the Si substrate gives rise to non-vertical NWs which are not in an epitaxial relation with the underlying substrate. Figure 6.7 depicts the non-vertical growth of the InAs NWs; the yellow color shows a NW nucleated on a parasitic cluster and the green color displays NWs nucleated on the oxide layer.

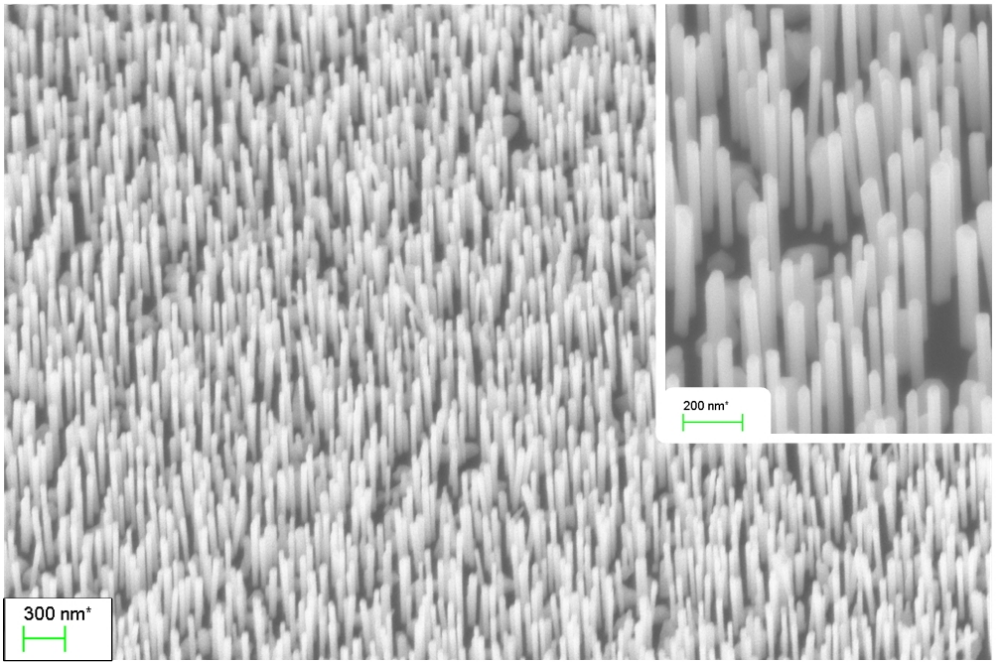

Figure 6.6: 30 deg. tilt SEM image for a forest of high aspect ratio InAs NWs. Inset shows a magnified view of the NWs.

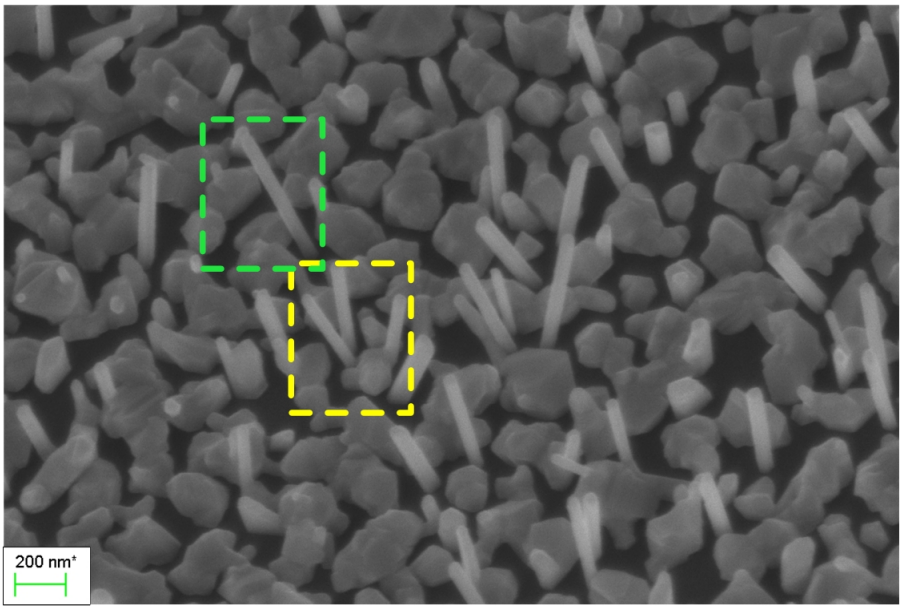

Figure 6.7: 30 deg. tilt SEM image for non-vertical NWs.

7

Conclusion and Outlook

In this work, we presented catalyst-freegrowth of InAs NWs On Si (111). First, the MBE growth technique and the MBE system were discussed. Then various characterization techniques including AFM, SEM and ellipsometry, used for this work, were presented . Afterwards, the two NWs synthesis approaches were discussed in details along with evaluating each technique with its strengths and weaknesses and showing how to improve each technique in the future.

In the first synthesis approach, we presented a fully bottom-up strategy that employs colloidal lithography to fabricate large-scale (up to 6 cm^2 obtained so far) templates with diameter down to 50 nm for SAE catalyst-free growth of InAs NWs. Efficient control of the pattern, size and spacing of the nano-apertures in the bottom-up growth template was obtained. A uniform size distribution of free-standing InAs NWs was achieved at $460\,^oC$. In general, this full bottom-up strategy paves the way towards the realization of NWs-based devices with a low-cost, time-efficient, high-throughput and highly parallel large-scale nanofabrication. Specifically, such bottom-up short-range ordered NWs platforms can find a direct use in energy harvesting devices based on as-grown vertical NWs with well controlled uniformity and density [68, 69]. Furthermore, the growth selectivity is not of a priority in the case of NW-based devices usually produced on planar configurations in which NWs are transferred onto another substrate. For further development of this strategy

and to overcome its pitfalls, we have modified the CL technique to HCL technique which proved the viability of improving the quality of the SiO_2 and accordingly will improve the growth selectivity in the future work. The fully bottom-up approach presented here can also be extended in the future to applications requiring ordered arrangement of NWs by enabling patterns of periodic aperture arrays.

In addition, we have demonstrated the growth of non-ordered catalyst-free InAs NWs in the pinholes generated on SiO_2-masked Si(111) when etched down to few nanometers. This approach is considered the simplest routine to achieve epitaxial growth of InAs NWs since it does not require special patterning step for the substrates prior to growth. Utilizing this simple approach, we have been able to obtain large areas of highly dense high aspect ration NWs with diameters down to 30 - 40 nm and heights up to 1 μm. In this approach, we focused on investigating the effect of the SiO_2 layer thickness and the etching depth on the morphology of the grown NWs. We have shown the NWs growth dependency on the density of the pinholes as well as the density of the parasitic clusters.

In this thesis we presented the viability of avoiding the usage of catalysts to guide the epitaxial growth of NWs and achieved promising results using simple, versatile, low-cost, time-efficient and high throughput techniques. However, further studies on the optimization of growth parameters (In and As fluxes, growth rate, growth duration, size of nano-apertures, inter-wire distance and SiO_2 thickness) is highly needed to achieve high aspect ratio NWs with high yield and excellent growth quality. Moreover, X-ray diffraction (XRD) and transmission electron microscopy (TEM) measurements need to be performed to study the structure and the quality of the grown NWs. Moreover, to confirm the potential of InAs NWs, NW-based test devices should be fabricated to examine the electrical and optical properties of these NWs.

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A

Substrates Preparation

A.1 Substrates cleaning

RCA cleaning recipe is a standard recipe commonly used for cleaning Si wafers. RCA involves three chemical processes that are performed in sequentially: SC-1 for organic cleaning, HF treatment for native oxide removal and SC-2 for ionic cleaning. If the substrates were visibly contaminated, a preliminary 'degrease' procedure is performed before the RCA cleaning process. After the cleaning process, the substrates were processed within 24 hours after being cleaned otherwise the substrates were considered contaminated and need to be cleaned again. The cleaning procedure is summarized in the following steps:

Preliminary degrease procedure:

- Soak the substrates in acetone for 5 minutes.
- Remove substrates from acetone and soak them in IPA for 5 minutes.
- Remove the substrates from IPA and soak them in DI water for 5 minutes.
- Rinse the substrates sufficiently with DI water and blow dry them with N_2 gun.

RCA cleaning procedure:

- **SC-1** : Soak the substrates in a 1:1:5 solution of $NH_4OH : H_2O_2 : H_2O$ at $80\,^oC$ for 10 minutes.
- Rinse the substrates sufficiently under DI water.

- Soak the substrates in 2% HF for 30 seconds.
- Rinse the substrates sufficiently under DI water.
- **SC-2** Soak the substrates in a 1:1:5 solution of $HCl : H_2O_2 : H_2O$ at $70\,^oC$ for 10 minutes.
- Rinse the substrates sufficiently under DI water and blow dry them with N_2 gun.

A.2 Substrates preparation for SEM characterization

Sputter-deposition of 6 nm of aluminium (Al) on the investigated non-conductive substrates at a deposition rate of 1.95 nm/sec.

- Sputtering duration = 3 sec.
- Power = 1 kW.
- Reflected power = 0.
- Pressure = 8E-03 mbar.
- $d_(targer - susbtrate)$ = 72 mm.
- Q_{Ar}) = 40 sccm.
- Valve = 35 %.

B

Preparation of the Si Substrates for the SA-MBE of Nanowires

B.1 Substrates patterning for the short-range ordered growth of NWs

B.1.1 Substrates patterning via CL

Formation of PS nanosphere monolayer:

- Treat the substrates with light power O_2 plasma (50 W - 250 mtorr - 15 sccm) for 1 min to enhance the surface hydrophilicity.
- Drop-cast a triple layer of charged polymers of PDDA (0.2%), PSS (2 %) and ACH (5 %) on the Si substrate to make it positively charged and let each polymer layer to adsorb for 30 s.
- Rinse the substrate after the adsorption of each polymer layer under DI water for 30 s and blow dry it with N_2 gun.
- Drop-cast the negatively charged PS particles solution on the positively charged substrate with the polymer layer and let it to adsorb for 2-3 mins until the surface saturation with the nanoparticles is reached.
- Rinse the substrate under DI water for 15 s to get rid of the naoparticles in excess.

- Apply hot ethylene glycol at a temperature $(150 - 200^oC)$ above the melting temperature of PS particles for few seconds on the wet substrate to allow the slight melting and immobilization of of PS particles to the substrate.
- Rinse the substrate under DI water for 1 min and blow dry it with N_2 gun.
- Expose the formed PS nanosphere monolayer on the Si substrate to O_2 plasma (50 W - 250 mtorr - 15 sccm) for a certain duration to shrink it to the desired size.

Transfer of the colloidal pattern to a nanoholes pattern:

- Load the substrate in an AVAC system and evaporate a 15 nm thick SiO_2 layer at a deposition rate of 0.1 Å/s.
- Remove the PS nanoparticles via tape-stripping for 3 times to make sure that all particles are removed.
- Expose the Si substrate to light power O_2 plasma (50 W- 250 mtorr - 15 sccm) for 1 min to remove the remnant residues and the polymer layer in the Si nanoholes.

B.1.2 Substrates patterning via HCL

Formation of PS nanosphere monolayer:

- Load the Si substrate in the furnace-centrotherm system for dry thermal oxidation to deposit 20 nm of SiO_2 at T= 950^oC for 20 min.
- Follow the same procedures mentioned in subsection B.1.1 for the formation of PS nanosphere monolayer except the first step.

Transfer of the colloidal pattern to a nanoholes pattern:

- Load the substrate in the Lesker evaporator system and evaporate a 10 nm thick Cr layer.

- Remove the PS nanoparticles via tape-stripping for 3 times to make sure that all particles are removed.
- Load the substrate in an Oxford Plasmalab System- RIE/CVD for dry etching the SiO_2 layer and obtain a nanoholes pattern.The etching process is divided into two steps,
  - Step 1: Breakthrough etching for the removal of the polymer layer inside the nano-apertures pattern. The recipe off cleaning is as follows:
    - Q_{Ar} = 10 sccm.
    - Q_{O2} = 10 sccm.
    - t = 30 s.
  - Step 2: Etching of the SiO_2 layer inside the nano-apertures. The etching recipe is as follows:
    - Q_{Ar} = 10 sccm.
    - Q_{N2} = 10 sccm.
    - $Q_N F_3$ = 30 sccm.
    - Forward Power = 50 W.
    - Reflected power = 2.
    - DC bias = 80 V.
- Fill a beaker with a 1 : 1 solution of Cr etchant : DI water.
- Fill another beaker with DI water.
- Submerge the substrate to be etched in the Cr etchant until the change of the surface color indicating Cr removal is observed. Then rinse it with DI water in the other beaker.

B.1.3 Substrates final preparations before being loaded in the MBE system:

After patterning the Si substrates, they were loaded in the MBE system for the SAE of NWs. To make the substrates ready for the growth, they were

dipped in an oxide etchant to remove the remnant oxide layer and make sure that Si is exposed.

- Submerge the substrates in 10:1 solution of H_2O : BOE for 2-3 s calibrated based on the etching rate of the evaporated SiO_2 usin AVAC system in a 10% BOE solution.
- Rinse the substrates sufficiently with DI water and blow dry them with N_2 gun.
- Load the substrates directly in the MBE system under UHV environment within 30 mins to avoid the formation of native oxide layer in the Si nanoholes.

B.2 Substrates preparation for the non-ordered growth of NWs

Sputter Deposition of silicon dioxide on Si substrates:

The substrates are loaded in an FHR MS150 puttering system and sputtered with a thin film of SiO_2 at a deposition rate of 0.233 nm /s.

- Sputtering duration: varies according to the desired film thickness. In this thesis 3 film thicknesses were prepared as follows:
  - 10 nm thick film = 42 s.
  - 20 nm thick film = 83 s.
  - 30 nm thick film = 125 s.
- Output Power = 1 kW.
- Reflected power = 0.
- DC bias = 126 V.
- Pressure = $1.3E-02$.
- $d_(target - substrate)$ = 72 mm.

- $Q_{Ar} = 40$ sccm.
- $Q_{O2} = 15$ sccm.
- Valve = 30 %.

Etching the sputter deposited silicon dioxide to open pinholes:

- Fill a beaker with a 1 : 10 solution of BOE : DI water.
- Fill another beaker with DI water.
- Submerge the substrate to be etched in the BOE for certain time calibrated based on the etching rate of the sputter-depositd SiO_2 on Si and then submerge directly in the DI water.
- Each group of substrates of 10, 20 and 30 nm thickness, etched down to 1, 2 and 3 nm.
- Blow dry the substrate with N_2 gun and check thickness with ellipsometer.
- Load the substrate in the MBE system under UHV and proceed to growth.

Poster

MBE growth of InAs nanowires on large scale colloidal lithography patterned Si substrates

Elham Fadaly, Fitria Rahayu, Huan Zhao

MyFab/NorFab User Meeting

Lund, Sweden, 21st -22nd April 2015

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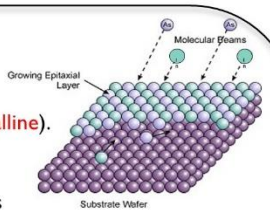
MBE growth of InAs nanowires on large scale colloidal lithography patterned Si substrates

Elham Fadaly, Fitria Rahayu, Huan Zhao

Introduction



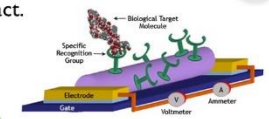
Why MBE ?

- Ultra-high vacuum (Pure crystalline).
- Precise growth rate control (sub-monolayer/sec).
- Fast switch of sources shutters (Atomic Precise control of heterostructure interface).

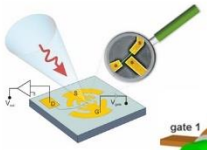
Why InAs ?

Material	Si	Ge	GaAs	InP	InAs	GaSb	InSb
Electron mobility (cm^2/Vs)	1450	3900	8000	4000	30000	3750	70000
Hole mobility (cm^2/Vs)	370	1900	320	150	350	680	850

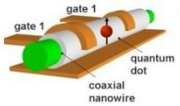
- Low ohmic contact.
- **Applications:**



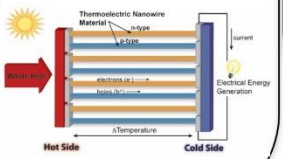
Bio-sensors



THz Detectors

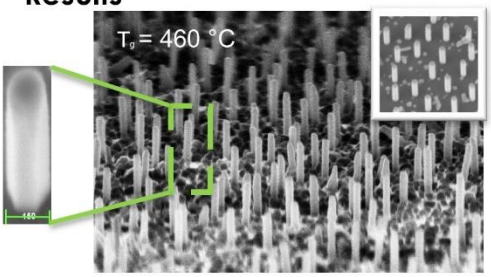


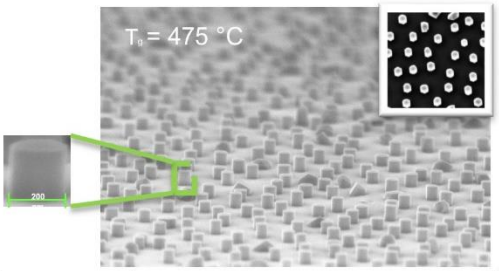
Spintronics



Thermoelectrics

Results

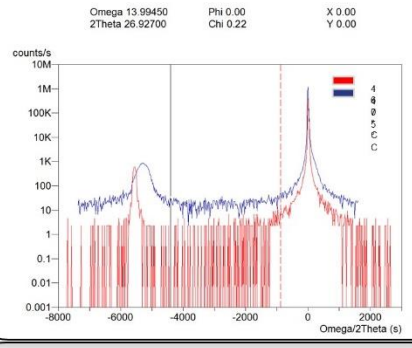




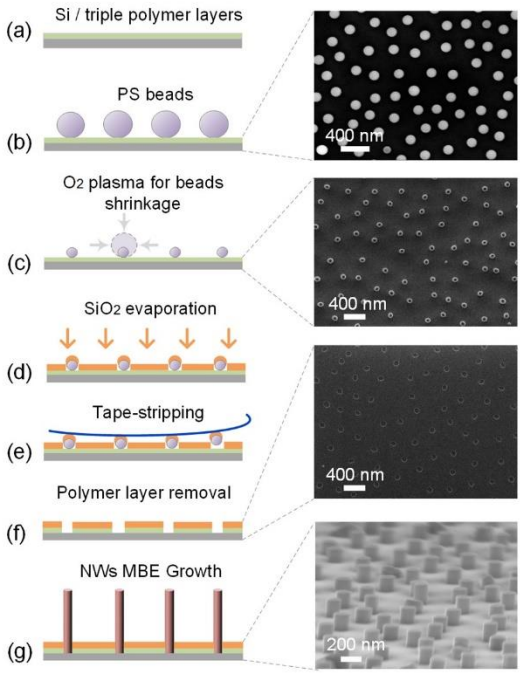
In flux = 0.2 Å/s, As (BEP) = 4.5 ×10^{-6} Torr, t_g = 90 min

XRD Measurement

Out of plane symmetric ω - 2Θ scan

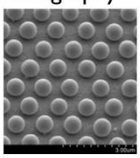


Fabrication Technique



Future Work

- Characterize the as grown NWs with TEM.
- Perform mobility measurements..
- Tune the growth parameters to get NWs diameter comparable to particle/hole size.
- Control the pattern density and alignment to be comparable to top-down lithography techniques.
- Fabricate test devices.



Paper

Production of nano-holes pattern on Si (111) by colloidal lithography for growth of InAs nanowires

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Production of nano-holes pattern on Si (111) by colloidal lithography for growth of InAs nanowires

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***Abstract*—Colloidal lithography is a simple, versatile and low-cost technique that can be used to pattern diverse nanostructures on a wafer scale. In this work, colloidal lithography utilizing polystyrene nanoparticles as a lift-off mask was used to produce nanoholes pattern on Si (111) substrates. The holes size, which is determined by the size of the polystyrene particles, can be well controlled by oxygen plasma shrinking. Using this technique, we were able to obtain nanoholes pattern with feature size down to 50 nm, which is close to the limit that conventional lithographic techniques can reach, in a time-efficient and cost-effective manner. This template is intended for the growth of InAs nanowires using molecular beam epitaxy.**

Keywords—Nanomaterials; semiconductors; colloidal lithography; InAs nanowires; MBE; selective area epitaxy

I. INTRODUCTION

Colloidal lithography (CL) has attracted much attention over the past decade, due to its versatility, simplicity, low-cost and viability of patterning various nano-sized features on large areas (several cm^2). The self-assembled nanoparticles are capable of producing two- and three-dimensional templates, acting as a mask for direct etching or deposition to produce structures ranging from tens of micrometers down to tens of nanometers [1]. The aforementioned properties made CL more attractive than conventional lithography techniques, such as immersion lithography, e-beam lithography (EBL), scanning probe, and focused ion beam (FIB) lithography which feature high cost, complex machinery, low throughput and limitation of patterning areas (several mm^2) [2].

Semiconductor nanowire (NW) based devices are considered as ideal building blocks for the next generation of electronics, photonics, sensors and energy harvesting applications [3]. Most reported NW growths are governed by the vapor-liquid-solid (VLS) mechanism, either through foreign [4, 5] or self-induced metallic catalysts [6-8]. However, such processes in which the catalyst is self-assembled, produce NWs that are randomly positioned and also exhibit a significant range of diameters. A further problem with catalytic growth is that the metal catalyst will be inevitably incorporated into the NWs, which may be prohibitive for many semiconductor applications. On the other hand, selective area epitaxy (SAE) on patterned substrate is essential to have control over position, size and directionality of nanowires for homogenous and predictive performance. In the SAE approach, substrate is usually masked with dielectrics patterned with aperture sizes below 100 nm, and growth conditions are appropriately chosen to restrict the epitaxial growth inside the apertures. However, current approaches for the nano-patterning are mainly based on EBL. The aforementioned drawbacks of EBL greatly limit mass production of semiconductor NWs and thus their commercialization. Nano-imprinting has been applied for nano-patterning to grow NWs, with a relatively lower cost and much higher throughput through a replication process. But the technique still needs EBL for stamp fabrication and innovative solutions are still required to solve process and stamp lifetime issues for different applications [9].

Herein, a modified CL process is taken to pattern Si (111) substrates for SAE growth of InAs nanowires. A colloidal solution consisting of charged polystyrene (PS) nanoparticles was used to produce a short-range ordered 2D particle array. Oxygen (O_2) plasma treatment was utilized to shrink the particles size. The inter-particles spacing is defined by the mutual electrostatic repulsions among the nanoparticles that keep them far apart. Using the PS particles as a lift-off mask, the nanoparticles pattern was successfully transferred to a nano-holes pattern in a SiO_2 layer on Si (111) substrates.

II. EXPERIMENT AND RESULTS

2-inch boron doped silicon wafers with crystallographic orientation (111) cut in quarters were used for all the experiments. A colloidal suspension of negatively charged PS nanoparticles dispersed in deionized water (DI) purchased from interfacial dynamics corporation (IDC) was used for CL. A 5 nm thick Aluminum layer was sputtered on samples with coated PS particles or nano-holes pattern to reduce the charging effect in the scanning electron microscope (SEM) measurements.

A process adapted from the standard CL technique reported in [10] was used to define the template. First, the wafers were cleaned by the standard cleaning recipe RCA (SC1/SC2). Then the samples were oxidized with oxygen plasma to enhance the hydrophilicity of the surface. Afterwards, triple layers of charged polymers, poly diallyldimethyl ammonium Chloride (PDDA), poly Sodium 4-Styrenesulfonate (PSS), and aluminum chloride hydroxide (ACH), were adsorbed on the surface to make the surface positively charged. Then the

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solution with negatively charged PS nanoparticles was drop-casted on the triple polymer layers and let to adsorb on the surface until surface coverage saturation with nanoparticles was achieved. To remove excess PS particles, the sample was rinsed under DI water after self-assembly and then blow-dried with nitrogen (N_2) gun. Next, hot ethylene glycol at a temperature around 150-200 ^oC (above glass transition of PS particles) was directly applied on the wet sample to avoid the formation of PS particles aggregates. This step allows the slight melting and proper immobilization of the PS particles to avoid the disturbance of the amorphous pattern by the capillary forces while rinsing and drying. Finally, the sample was rinsed again under DI water and blow-dried with N_2 gun. After this step, a monolayer of spherical PS particles was formed on the Si (111) surface.

In this work, the size of the PS particles, which determines the size of the holes pattern, was controlled by an O_2 plasma treatment process. After shrinking the PS particles to the desired size, a thin layer of SiO_2 was evaporated on the PS monolayer. Then the PS particles were lifted-off by tape stripping. Afterwards, O_2 plasma was used again to remove the remnant triple polymer layers in the nanoholes pattern. The patterned substrate was then etched in a buffer oxide etchant for 2-3 s prior to loading in the MBE system.

III. Discussion and Summary

For functional NW devices, it is essential to have control over position, size and directionality of NWs for homogenous and predictive performance. Moreover, the growth of device-quality NWs with high purity should abstain from conventional nucleation schemes that employ foreign catalyst such as gold. The SAE technique allows positioning controlled catalyst-free growth of NWs, where templates with nano-holes pattern are required to restrict the places for nucleation and thus defined the area for vertical growth. However, current approaches for the nano-patterning are mainly based on EBL, which is expensive and not suitable for large scale productions. In this work, we demonstrated a fully bottom up approach for producing the templates for the SAE growth of catalyst-free NWs. The templates are fabricated by the inexpensive colloidal lithography technique, which features properties of simplicity, low cost and viability of patterning different nano-sized features on large scales. Future work will focus on developing colloidal lithography methods for a better control of size and ordering of the patterns, which enables fabricating well-ordered 2D nano-aperture arrays. The developed technique in this work opens a new perspective for production of uniform ordered semiconductor NWs on macroscopic templates, which can be used for the fabrication of a variety of devices for a wide range of applications.

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