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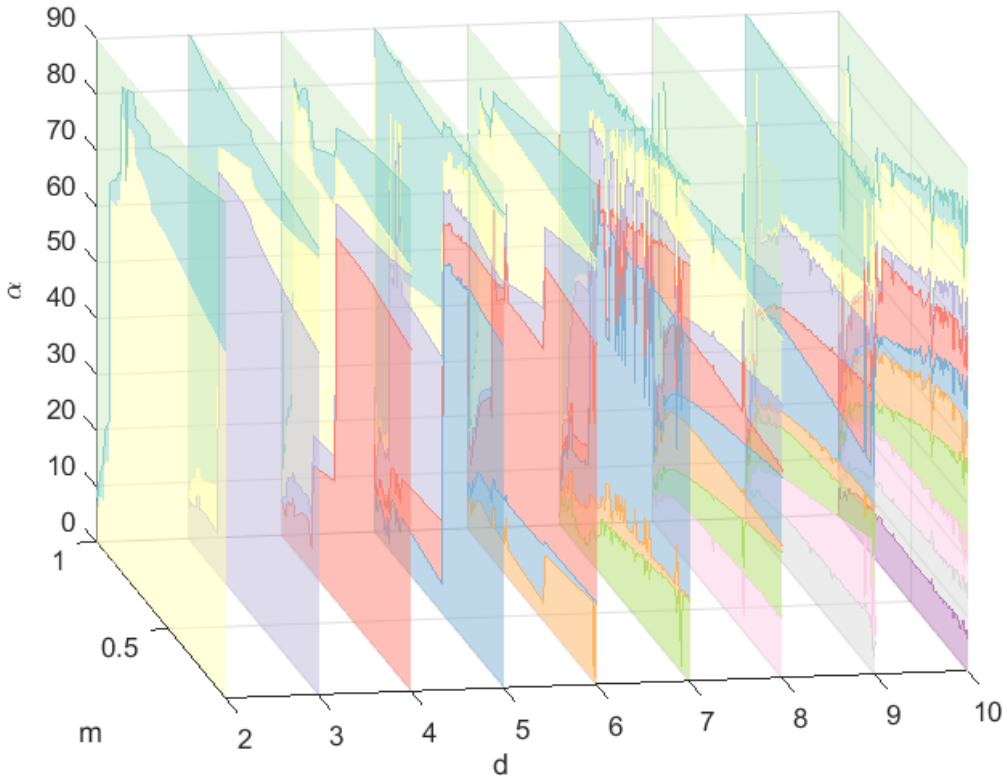

Optimized Pulse Pattern Control Strategy Investigation on Signal Level Hardware in the Loop

Master's Thesis in Sustainable Electric Power Engineering and Electromobility

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Gothenburg, Sweden 2023
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Master's thesis 2023

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Cover: Generated optimized pulse pattern, where d represents number of adjustable switching angles per quarter period, m represents modulation index and $\boldsymbol{\alpha}$ represents switching angles.

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Abstract

Electric vehicles (EVs) are gaining popularity worldwide due to their low cost of use and sustainability. Key components of the EV drivetrain include an inverter and a permanent magnet synchronous machine (PMSM). To better improve their efficiency, optimized pulse pattern (OPP) can be used. However, simulating OPP together with the inverter and motor takes a lot of time because of high computational complexity. This thesis project utilizes a hardware in the loop (HiL) platform to accelerate the simulation. The PMSM and inverter models are running on a field-programmable gate array (FPGA) separately from the controller model to ensure a high sampling rate while the whole system is still running in real time. Then OPP is evaluated with this platform in comparison with the conventional space vector pulse width modulation (SVPWM). The result shows a significant advantage of OPP in reducing inverter switching losses. Finally, the limitation and operating range of the OPP is also discussed in this thesis report.

Keywords: Permanent Magnet Synchronous Machine, Hardware in the Loop, Field-Programmable Gate Array, Space Vector Pulse Width Modulation, Optimized Pulse Pattern.

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Chenye Zou, Gothenburg, August 2023

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

API	Application Programming Interface
DAQ	Data Acquisition
ECU	Electronic Control Unit
EDU	Electric Drive Unit
EV	Electric Vehicle
FEM	Finite Element Method
FOC	Field-oriented Control
FPCU	Field-programmable Control Unit
FPGA	Field-programmable Gate Array
HiL	Hardware in the Loop
HWS	Half-wave Symmetry
LUT	Look-up Table
MPC	Model Predictive Control
NVH	Noise, Vibration and Harshness
OPP	Optimized Pulse Pattern
PMSM	Permanent Magnet Synchronous Machine
QWS	Quarter-wave Symmetry
RCP	Rapid Control Prototyping
SOPWM	Synchronous Optimal Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter

Nomenclature

Below is the nomenclature of indices, sets, parameters, and variables that have been used throughout this thesis.

Indices

n	Indices for the harmonic order
i	Indices for switching angles
j	Indices for elements in the main FEM
k	Indices for layers in the post 1-D FEM

Sets

$\boldsymbol{\alpha}$	Set of switching angles

Parameters

R_s	Stator resistance
L_d	D-axis inductance
L_q	Q-axis inductance
Ψ_m	Flux linkage induced by the permanent magnets
n_p	Number of pole pairs
a_n,b_n	Fourier coefficients
V_{CE}	IGBT collector-emitter saturation voltage
R_{CE}	IGBT internal gate resistance
V_{D0}	Diode forward voltage
R_{D0}	Diode internal resistance
f_{sw}	Switching frequency

E_{sw}	Turn on and turn off energy loss per switching pulse
E_{rec}	Diode reverse recovery energy
U_{DC}	DC supply voltage
I_{ref},V_{ref}	Current and voltage references for switching loss calculation
K_i,K_v	Current and voltage correction factors for switching loss calculation
n_e	Number of elements in the main FEM
n_{sym}	Symmetry multiplier
S_j	Area of the jth element
l	Active length
T	Signal sampling period
h	Laminate thickness
κ	Excess loss coefficient
ρ	Steel resistivity
n_l	Number of layers in the post 1-D FEM
z_k	Layer thickness
K_h	Hysteresis loss coefficient
L_σ	Load inductance
d	Number of adjustable switching angles per quarter period
T_s	ECU sampling period
f_s	ECU sampling frequency
$\Delta\alpha_{min}$	Minimum angle resolution

Variables

i_d	D-axis current
i_q	Q-axis current
u_d	D-axis voltage
u_q	Q-axis voltage
ω_r	Electrical speed
T_e	Electromagnetic torque
m	Modulation index
$\cos\phi$	Power factor
$\hat{I}_1$	Fundamental current amplitude
$\hat{I}_n$	nth order current harmonics amplitude

$\boldsymbol{A}_j$	Magnetic vector potential
f_1	Fundamental frequency
B_{ij}	Flux density
P_{cond_IGBT}	IGBT conduction loss
P_{cond_D}	Diode conduction loss
P_{sw_IGBT}	IGBT switching loss
P_{sw_D}	Diode switching loss
P_{inv}	Inverter loss
P_{h_r},P_{h_s}	Rotor and stator hysteresis loss
P_{e_r},P_{e_s}	Rotor and stator eddy-current loss
P_{Fe}	Iron loss
P_{Cu}	Copper loss
I_{THD}	Inverter current THD
$\hat{u}_n$	Phase voltage amplitude
ω_1	Fundamental electrical speed
α_i	ith switching angle
Ω	Mechanical speed

Contents

1
Introduction

With the rapid development of lithium-ion batteries, power electronics and electric machines, electric vehicles (EVs) are becoming increasingly popular among the world as an alternative to traditional internal combustion engine cars. EVs are an attractive option for consumers and policymakers due to their low cost of use and zero emissions. This makes them a more sustainable choice for transportation, reducing air pollution and carbon emissions. However, there is still room for improvement in terms of efficiency, particularly in the electric drive unit (EDU). One of the keys to an intelligent EDU is its control strategies, with which it can maximize its potential without an upgrade of the hardware. Developing new control strategies that optimize the performance of both the inverter and electric machine across a wide range of operating conditions is crucial for further improving the sustainability of EVs.

Space vector pulse width modulation (SVPWM) is a common control strategy that uses a fixed switching frequency and variable duty cycles. By increasing the switching frequency, it can reduce low order harmonics in the electric machine, but it also increases inverter switching losses. Therefore, an optimal switching frequency is necessary to balance the performance and efficiency of the inverter. On the other hand, optimized pulse pattern (OPP) is a more flexible modulation technique that uses electric angle position-based pulse patterns. These patterns can be optimized for various targets such as minimum total harmonic distortion (THD), total losses, or noise, vibration, and harshness (NVH), etc. Unlike SVPWM, OPP does not have a fixed switching frequency and can reduce switching losses without sacrificing waveform quality at high speeds. However, it cannot achieve a high equivalent switching frequency at low speeds due to the limited number of switching pulses per period. As a result, SVPWM and OPP can be used together to complement each other's strengths and weaknesses.

In order to validate SVPWM and OPP control strategies, an FPGA hardware in the loop (HiL) bench is used. A HiL platform makes it easier to test and calibrate various software functions and control strategies, and it is much safer without a real electric machine, especially when doing short circuit tests[1, 2]. An FPGA HiL is mainly composed of FPGA-based plant models, interfaces between plant models and the controller, host PC, etc. FPGA-based models are discrete and linearized, ensuring fast running speed without compromising accuracy. They can capture the dynamics of power electronics and electric machines by running at MHz, compared to models in a real-time PC that only runs at kHz.

The purpose of this thesis is to test and compare the performance between SVPWM and OPP with the dSPACE HiL Rig platform, which helps further improving the sustainability of EVs. The complete workflow with the HiL Rig platform will

be verified, which includes FPGA plant model design, process model design, test automation, post-processing, etc. According to the test results, the total losses of SVPWM and OPP will be compared at different operating points. The limitation of OPP will also be investigated based on the current setup.

The thesis report is organized as follows. In Chapter 2, basic theories about PMSM, SVPWM and OPP will be introduced. Fourier theory will be discussed in this part as well. In Chapter 3, the overall setup and implementation of the HiL Rig platform including the process model and FPGA-based plant models will be explained in detail. HiL test automation will also be introduced in this part. Basic principles and implementation of OPP will be discussed in Chapter 4. In Chapter 5, the performance between SVPWM and OPP under different operating points will be compared. Also, the limitation and operating range of OPP will be discussed in this chapter. Finally, conclusions will be drawn in Chapter 6.

2

Theory

2.1 Permanent Magnetic Synchronous Machine

Permanent magnet synchronous machines (PMSMs) are used in many applications such as electric vehicles and wind turbines because of their high efficiency, high power density, high torque density and low maintenance requirements. It is a type of synchronous electric motor that uses permanent magnets attached to the rotor. The stator windings are energized with AC current which produces a rotating magnetic field. The rotor is attracted to the rotating magnetic field and rotates with it.

In order to simplify the analysis and controller design of three-phase inverters and PMSMs, the direct-quadrature (dq) transformation is used. It is the product of Clarke and Park transformation, which first transform the abc frame into the $\alpha\beta$ frame, and then rotate the reference frame to transform the $\alpha\beta$ frame into the dq frame. So finally three-phase AC signals become two-phase DC signals. The equivalent circuit of a PMSM in dq frame can be written as

$$u_d = R_s i_d + L_d \frac{\mathrm{d}i_d}{\mathrm{d}t} - \omega_r L_q i_q \tag{2.1a}$$

$$u_q = R_s i_q + L_q \frac{\mathrm{d}i_q}{\mathrm{d}t} + \omega_r L_d i_d + \omega_r \Psi_m \tag{2.1b}$$

where u_d and u_q represent d-axis and q-axis voltage respectively, R_s represents the phase stator resistance, L_d and L_q represent d-axis and q-axis inductance respectively, i_d and i_q represent d-axis and q-axis current respectively, ω_r represents electrical speed of the rotor, Ψ_m represents the flux linkage induced by the permanent magnets.

The electromagnetic torque T_e of a PMSM can be calculated by

$$T_e = \frac{3n_p}{2}(\Psi_m i_q + (L_d - L_q) i_d i_q) \tag{2.2}$$

where n_p represents number of pole pairs.

Here, L_d, L_q and Ψ_m can either be constant parameters or nonlinear parameters with look-up tables (LUTs) depending on the required model accuracy and computational complexity. In this thesis project, 2-D LUTs-based PMSM model will be used to build FPGA-based plant models according to (2.1) and (2.2) in the following chapters.

2.2 Fourier Theory

Fourier theory is a mathematical technique which can be used to analyze and transform signals. With the Fourier transformation, a periodical signal can be transferred from the time domain to the frequency domain. This allows us to analyze the harmonic components of a signal which is important for the controller design and loss calculation in this thesis project. According to Fourier theory, a periodical signal $f(t)$ can be expressed as a superposition of sinusoidal waves, as

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}[a_n \cos(nt) + b_n \sin(nt)] \tag{2.3}$$

where a_0, a_n and b_n represent Fourier coefficients. These coefficients can be calculated by

$$a_0 = \frac{1}{\pi}\int_{-\pi}^{\pi} f(t)dt \tag{2.4a}$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(t)\cos(nt)\,dt,\ \ n = 1, 2, 3, \ldots \tag{2.4b}$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(t)\sin(nt)\,dt,\ \ n = 1, 2, 3, \ldots \tag{2.4c}$$

Considering quarter-wave symmetry (QWS), (2.4) can be simplified as (2.5), which will be used in Chapter 4.

$$a_n = 0,\ \ n = 0, 1, 2, \ldots \tag{2.5a}$$

$$b_n = \begin{cases} \frac{4}{\pi}\int_0^{\pi/2} f(t)\sin(nt)\,dt, & n = 1, 3, 5, \ldots \\ 0, & n = 2, 4, 6, \ldots \end{cases} \tag{2.5b}$$

2.3 Space Vector Pulse Width Modulation

Voltage source inverters (VSIs) are used in many medium and high power applications. There are a lot of different control strategies for VSIs, among which SVPWM is one of the most commonly used techniques. Compared with sinusoidal PMW (SPWM), SVPWM has a lot of advantages such as higher DC bus utilization, fewer harmonics at a high modulation index, easier implementation for over modulation, etc[3, 4, 5].

There are two different ways to implement SVPWM. One is the space vector approach, and the other is the triangular comparison approach. SVPWM with the space vector approach enables higher flexibility in the use of different switching sequences. However, it has a higher memory requirement and execution time compared with the triangular comparison approach[6]. This needs to be considered while running on an electronic control unit (ECU).

Figure 2.1 shows the voltage and current waveforms of SVPWM implemented by the triangular comparison approach. It has a fixed switching frequency and variable duty cycles. With a higher switching frequency, it ensures a lower inverter output current ripple. Although it brings a higher switching loss at the same time.

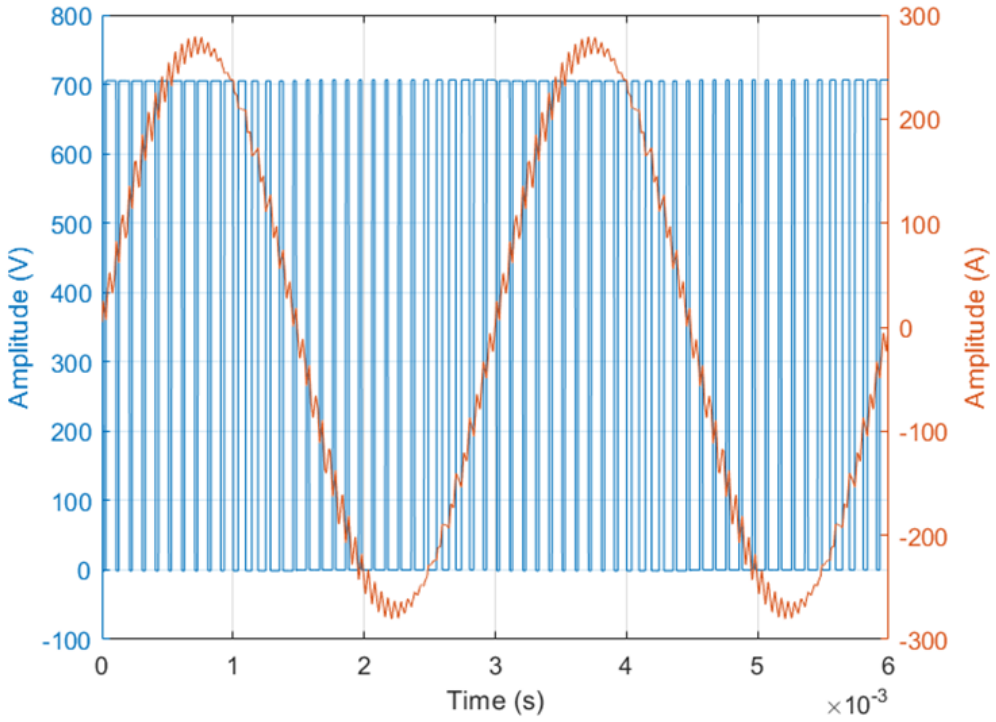

Figure 2.1: Voltage and Current Waveform for SVPWM

2.4 Optimized Pulse Pattern

OPP, also called synchronous optimal pulse width modulation (SOPWM), was first put into use in the 1970s[7]. At that time, power semiconductors could not achieve a high enough switching frequency. So OPP was proposed to reduce current harmonics. Nowadays, with the development of IGBT and MOSFET, power semiconductors are able to run at a very high switching frequency which brings high switching losses. OPP is used to reduce switching losses without sacrificing the current harmonics. As a result, OPP has now been used in many areas for different purposes. Annika et al.[8] used OPP to minimize the harmonic distortion in three-level inverters. Jorg et al.[9] modulate the Active Neutral-Point-Clamped 5-Level converter with OPP for high speed and high power applications. Steffen et al.[10] used OPP in three-phase to three-phase IGBT matrix converters to minimize the input current harmonics.

Researchers developed a lot of techniques to improve the process for generating and implementing OPP. Nina et al.[11] proposed an optimization target function which considering a salient machine type instead of a purely inductive load. A. Reardon et al.[12] used simulated annealing method together with the downhill simplex to avoid getting stuck in local minima while optimizing the target function. Kun

et al.[13] proposed the OPP with a continuous switching-to-fundamental frequency ratio to break through the limit of the discrete pulse numbers.

OPP has two different symmetry properties, which are half-wave symmetry (HWS) and quarter-wave symmetry. For the OPP with HWS, the switching angles range from 0 to π. The HWS waveform can fully utilize the potential of OPP since it has two times more variable switching angles than the OPP with QWS. However, it also means that it will cost more time to optimize and generate a pulse pattern. Another problem for the HWS waveform is that there is a phase shift for the fundamental voltage waveform, which needs to be considered during the OPP implementation[7, 14]. Due to the above reasons, the OPP with QWS is chosen for this thesis project. The switching angles range from 0 to $\frac{\pi}{2}$ for the OPP with QWS.

Figure 2.2 shows the voltage and current waveforms of the OPP with QWS. Compared with SVPWM in Figure 2.1, OPP does not have a fixed switching frequency. The gate switches according to the generated pulse pattern.

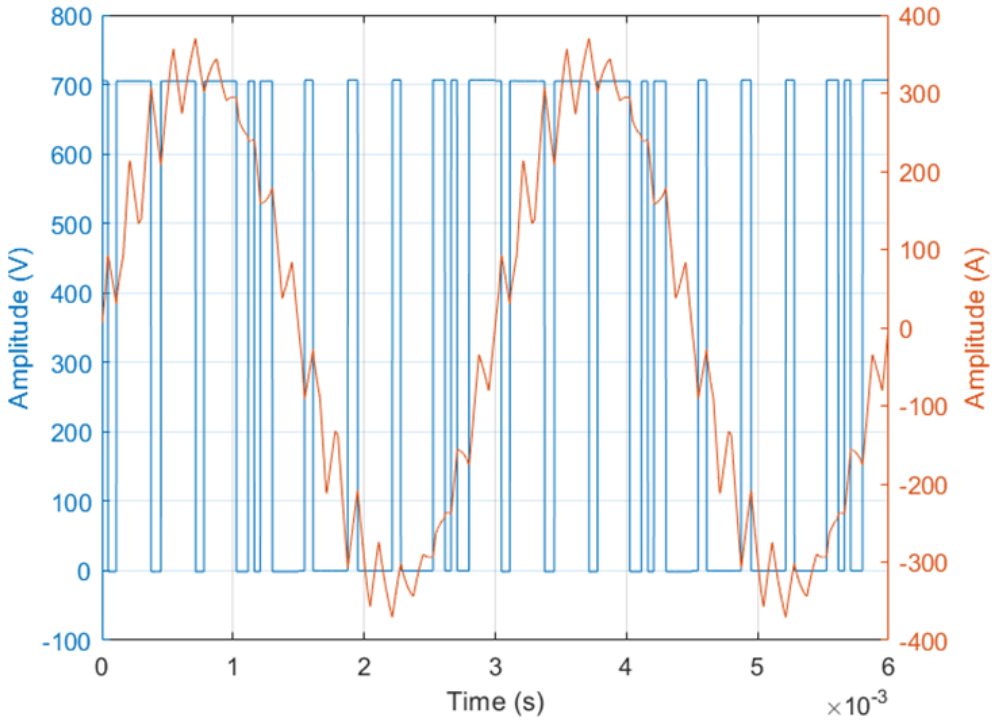

Figure 2.2: Voltage and Current Waveform for OPP

A problem for OPP is that it is usually used for low dynamic applications[7]. And it is hard to run OPP in a closed-loop control with the conventional PI controller. To solve this problem, model predictive control (MPC) can be used for a higher response speed[15].

3
Hardware in the Loop

3.1 HiL Rig Platform Setup

The HiL Rig platform we use is dSPACE SCALEXIO[16]. It provides a modular system with high flexibility which can be used for HiL and rapid control prototyping (RCP) applications. SCALEXIO contains a HiL host PC, a real-time PC, an FPGA module and several I/O modules. Table 3.1 shows the relevant software and hardware of SCALEXIO.

Table 3.1: Relevant Software and Hardware of SCALEXIO

	Product	Description
Software	RTI FPGA Programming Blockset	Tools for building FPGA-based plant models
	ConfigurationDesk	Configuration tool for signal chains and hardware resources
	ControlDesk	User interface for controlling and data acquisition
	XSG Electric Components Library	Electric motors and power electronics blocks for FPGA application
	XSG Utils Library	Basic function blocks for FPGA application
Hardware	SCALEXIO Processing Unit	Real-time PC
	DS2655 FPGA Base Board	Xilinx Kintex-7 160T
	DS2655M1 Multi-I/O Module	I/O Module
	DS2655M2 Digital I/O Module	I/O Module

Models running on the HiL rig platform can be divided into plant models and process models. FPGA-based plant models are usually designed in Simulink with the XSG Electric Components Library and the XSG Utils Library. The XSG Electric Components Library provides blocks of sensors, electric machines and power electronics. It also contains some predefined controllers that can be used while designing process models later. The XSG Utils Library provides some basic function blocks such as scopes, LUTs, and I/O access. After designing models, the RTI FPGA Programming Blockset will compile, synthesize and implement the whole FPGA application. In order to run on the FPGA, models should be discrete and linear. As a result, common Simulink blocks cannot be used while designing FPGA-based plant

models. Otherwise, the RTI FPGA Programming Blockset will fail to generate the FPGA application.

Process models are also designed in Simulink with the help of XSG libraries. The difference is that common Simulink blocks can also be used since models run on a real time PC. Registers and buffers need to be added because the FPGA is much faster than the real-time PC.

After designing plant and process models, the ConfigurationDesk will assign signal chains and hardware resources. Then it will evoke Matlab to build the whole project and download it to the target machines respectively. The parameters in process models can be controlled via the ControlDesk. It can also measure and visualize any parameter or variable. Figure 3.1 shows the system structure diagram of dSPACE SCALEXIO.

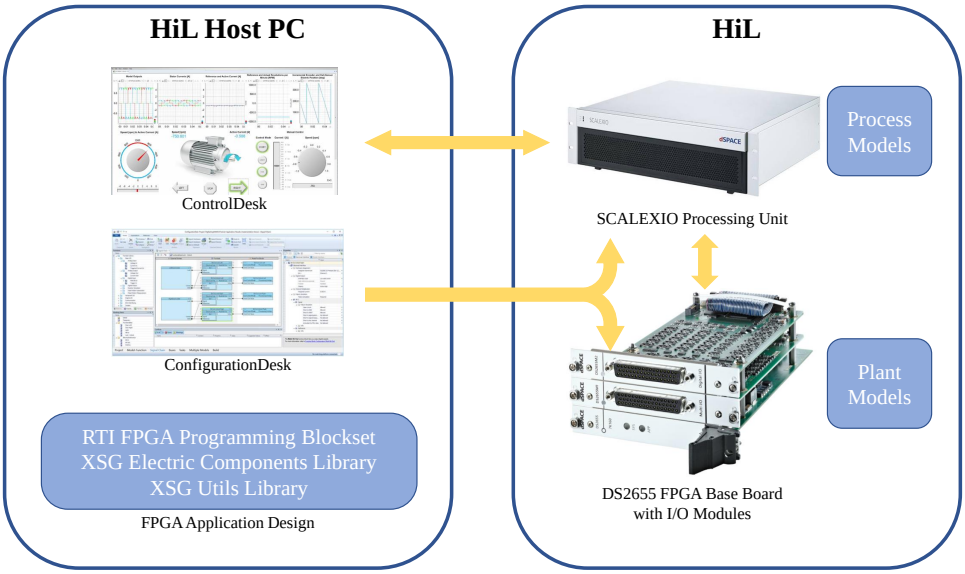

Figure 3.1: SCALEXIO System Structure Diagram

3.2 FPGA-based Plant Model with 2-D LUTs

Figure 3.2 shows the structure of the FPGA-based HiL model. The yellow part represents the structure of the FPGA-based plant model. Here, different colors mean different sampling times and they can be changed according to the required speed or model accuracy. In order to capture the dynamics caused by power electronics, the sampling time must be very high for the FPGA plant model. The blue and red parts represent the structure of the process model and it runs at a lower speed due to the hardware limitation.

The FPGA-based plant model is mainly composed of a PWM generator, an inverter, a DC link simulation, a PMSM and an FPGA scope. The most important part is the PMSM model with 2-D LUTs. It has 8 poles and 48 slots. The d-axis inductance, q-axis inductance and permanent magnetic flux linkage are 2-D LUTs

in related to d-axis current and q-axis current. The PMSM model is built according to (2.1).

The PWM generator has three different align modes. When the controller is running with SVPWM, the PWM generator uses the central-aligned mode. While for OPP, it automatically switching between left-aligned and right-aligned mode to better restore the OPP waveform and avoid extra switching losses.

In order to communicate between the slow and fast parts of the model, some buffers are needed to compensate for the sampling period difference. In Figure 3.2, the green part represents IOs and buffers. There are two main types of communication method. One is the real-time communication and the other one is the non-real-time communication which are represented by solid lines and dashed lines respectively in Figure 3.2.

For the real-time communication, all signals are sent to buffers first. Then, there is a down sampling for the data acquisition (DAQ) part of the process model. The down sampling rate is determined by the ratio of sampling frequency between the yellow part and blue part. This ensures the simulation of the whole model running at real-time at the expense of signal accuracy. But this sampling rate is not high enough to analyze the performance difference between SVPWM and OPP and it wastes the advantage of FPGA.

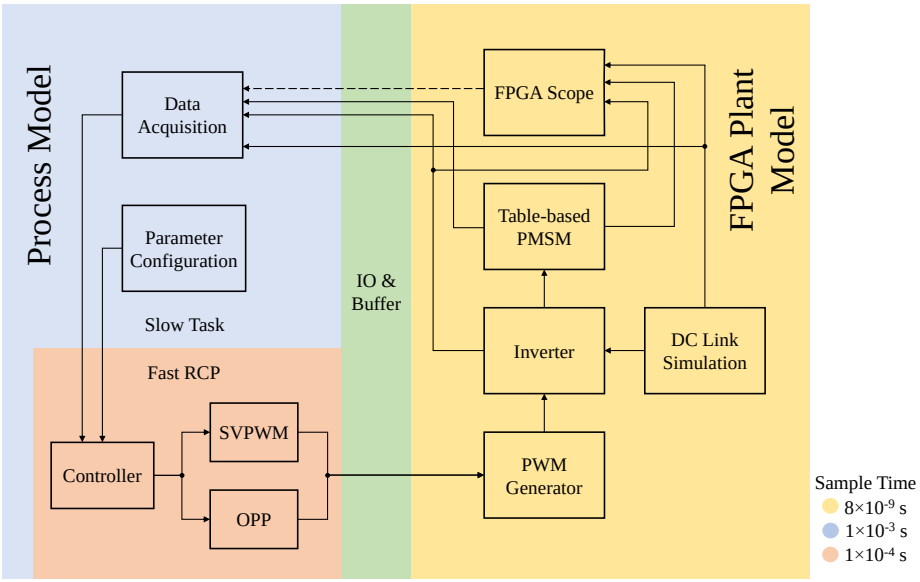

Figure 3.2: The Structure of FPGA-based HiL Model

The non-real-time communication is exactly the opposite way compared with real-time one. It cannot run in real-time. But it can capture the high frequency dynamics inside the FPGA model. For the non-real-time communication, all signals needed in the FPGA are sent to the FPGA scope first. There is a buffer inside the FPGA scope with an adjustable size. When the buffer is full, it will stop recording and send all the data to the process model with the same sampling rate as the DAQ part. And it will keep repeating the above process while running. There is also a down sampling rate in the FPGA scope. However, differing from the down sampling rate in real-time communication, it is not a fixed one and can be modified according

to how fast the required sampling rate of FPGA signals is. For example, supposing the FPGA scope has a buffer size of 5000 and a down sampling rate of 1, it only takes 40 ms to fill up the entire buffer. And then it needs another 5 s to send the data in the buffer to the process model. During this period, it cannot record FPGA signals. As a result, it should be carefully designed when to start recording. In the following tests, the FPGA scope will be triggered by the rising edge of phase A current with a trigger level of 0. The sampling rate will be selected according to the rotating speed so that the FPGA scope can record exactly one electrical period of those signals.

After building the plant model, it is compiled, synthesized and implemented by Vivado and is downloaded to Xilinx Kintex-7 160T. Xilinx Kintex-7 160T has 25350 configurable logic block slices which are the main logic resources for implementing sequential as well as combinatorial circuits. Each slice contains of four 6-input-1-output LUTs which means there are 101400 LUTs in total. One 6-input LUT can also be configured as two 5-input LUTs with separate outputs that can optionally be registered in a flip-flop. So one slice has eight flip-flops and there are 202800 flip-flops in total[17].

Table 3.2 shows the FPGA resource utilization rate. For the plant model with 2-D PMSM parameters introduced above, it utilizes over 80 percent of all configurable logic block slices after synthesis. It means that the FPGA is close to its resource limitation. More complex plant models can hardly be deployed on this FPGA baseboard.

Table 3.2: FPGA Resource Utilization Rate

Type	Used	Available	Utilization
Configurable Logic Block Slices	20640	25350	81.42 %
Configurable Logic Block Slices LUTs	48669	101400	48.00 %
Configurable Logic Block Slices Flip-Flops	53023	202800	26.15 %
Block Ram Blocks 36 Kb	99	325	30.46 %
Block Ram Blocks 18 Kb	31	650	4.77 %
DSP Slices	251	600	41.83 %

3.3 The Process Model with SVPWM

The blue and red parts in Figure 3.2 illustrate the structure of the process model. It is divided into the slow task with a sample time of 1 ms and the fast RCP with a sample time of 0.1 ms. These sample times can be adjusted according to the required speed. By this way, the computational complexity can be reduced. The DAQ part receives signals from both the real-time and non-real-time communication and it can send down-sampled signals to the controller. It is also connected to the ControlDesk and is responsible for data visualization.

The controller in the fast RCP uses conventional PI controllers with an anti-windup function. It can either be configured as the open-loop mode or the closed-loop mode according to different requirements. Then, the three-phase controlled

voltage values will be sent to the SVPWM block which has a third-harmonics injection. The parameters in the controller are set in the ControlDesk. They will be sent to the process model via the parameter configuration block. This enables users to tune the parameters while running.

3.4 Loss Models

3.4.1 Inverter Loss Model

Inverter losses can be divided into two parts: conduction losses and switching losses. According to equivalent circuits of IGBT and diode, they can both be treated as a series connection of a voltage source and a resistor. Depending on the power factor, the conducting time in one switching period can vary for the IGBT and diode. So conduction losses can be calculated by

$$P_{cond\_IGBT} = \left(\frac{1}{2\pi} + \frac{m\cos\phi}{8}\right) V_{CE}\hat{I}_1 + \left(\frac{1}{8} + \frac{m\cos\phi}{3\pi}\right) R_{CE}\hat{I}_1^2 \tag{3.1}$$

$$P_{cond\_D} = \left(\frac{1}{2\pi} - \frac{m\cos\phi}{8}\right) V_{D0}\hat{I}_1 + \left(\frac{1}{8} - \frac{m\cos\phi}{3\pi}\right) R_{D0}\hat{I}_1^2 \tag{3.2}$$

where m represents modulation index, $\cos\phi$ represents power factor, $\hat{I}_1$ represents fundamental current amplitude, V_{CE} represents IGBT collector-emitter saturation voltage, R_{CE} represents IGBT internal gate resistance, V_{D0} represents diode forward voltage, R_{D0} represents diode internal resistance.

Switching losses are proportional to the switching frequency. Turn on and turn off energy loss per switching pulse under the reference condition can be directly obtained from the datasheet. However, they need to be corrected according to the operating point. So switching losses are determined as

$$P_{sw} = f_{sw}E_{sw}\left(\frac{\hat{I}_1}{\pi I_{ref}}\right)^{K_i}\left(\frac{U_{DC}}{\pi V_{ref}}\right)^{K_v} \tag{3.3}$$

where f_{sw} represents switching frequency, E_{sw} represents turn on and turn off energy loss per switching pulse, U_{DC} represents DC supply voltage, I_{ref} and V_{ref} represent reference current and voltage obtained from the datasheet respectively, K_i and K_v are correction factors. Here K_i is 1. K_v is 1.6 for an IGBT and 0.6 for a diode. For a diode, E_{sw} is replaced with E_{rec}, which represents the diode reverse recovery energy. The parameters used for inverter loss calculation are listed in Table 3.3.

The total inverter losses are the summation of IGBT and diode conduction and switching losses for all six switches according to

$$P_{inv} = 6(P_{cond\_IGBT} + P_{cond\_D} + P_{sw\_IGBT} + P_{sw\_D}) \tag{3.4}$$

Table 3.3: Parameters for the Inverter Loss Calculation

Parameter	Value	Unit
V_{CE}	0.8276	V
R_{CE}	0.596	mΩ
V_{D0}	1.1152	V
R_{D0}	0.553	mΩ
E_{sw}	40.04	mJ
E_{rec}	8.92	mJ
I_{ref}	450	A
V_{ref}	400	V

3.4.2 Iron Loss Model

The iron loss calculation is usually based on the Steinmetz or Bertotti method. These methods are commonly used in low-frequency sinusoidal applications. However, when it comes to high-frequency sinusoidal and non-sinusoidal applications, they are not accurate enough due to the skin effect for the hysteresis and eddy current loss calculation[18].

The iron loss calculation requires the magnetic field distribution in the stator and rotor, which can be obtained from the finite element method (FEM) analysis. A 3-D LUT in related to rotor position, peak current amplitude and current angle can be generated from the FEM analysis. Figure 3.3 and 3.4 show one of the FEM results about the magnetic vector potential distribution. In this case, the rotor position is 0°, the peak current is 565.7 A and the current angle is 150°. The magnetic flux density is the curl of the magnetic vector potential so that it can be calculated.

The iron loss can already be calculated according to the magnetic field distribution which is shown in Figure 3.3 and 3.4. But the above FEM analysis is only a 2-D FEM which ignores the rotor and stator lamination. To better evaluate the skin effect for the iron loss calculation, Katsumi Yamazaki and Noriaki Fukushima[19] proposed the post 1-D analysis after the main FEM.

For each element in the main FEM, an individual 1-D FEM analysis is carried out. Figure 3.5 shows the schematic for both the main FEM and post 1-D FEM. Considering the laminate thickness, each element is now a triangular prism. Since the cross-sectional area of each element is small enough, the assumption can be made that the magnetic field is evenly distributed in each cross-section and only varies depending on the depth. So the 1-D FEM is enough for simulation. Furthermore, to reduce computational complexity, only half of the laminate is meshed and analyzed due to the symmetry. In this way, the post 1-D FEM analysis is proposed to evaluate the flux density difference along the longitudinal direction of the laminate.

The post 1-D analysis for all elements greatly increases the computational complexity. However, it is still far more efficient than a conventional 3-D FEM for the entire laminate[19].

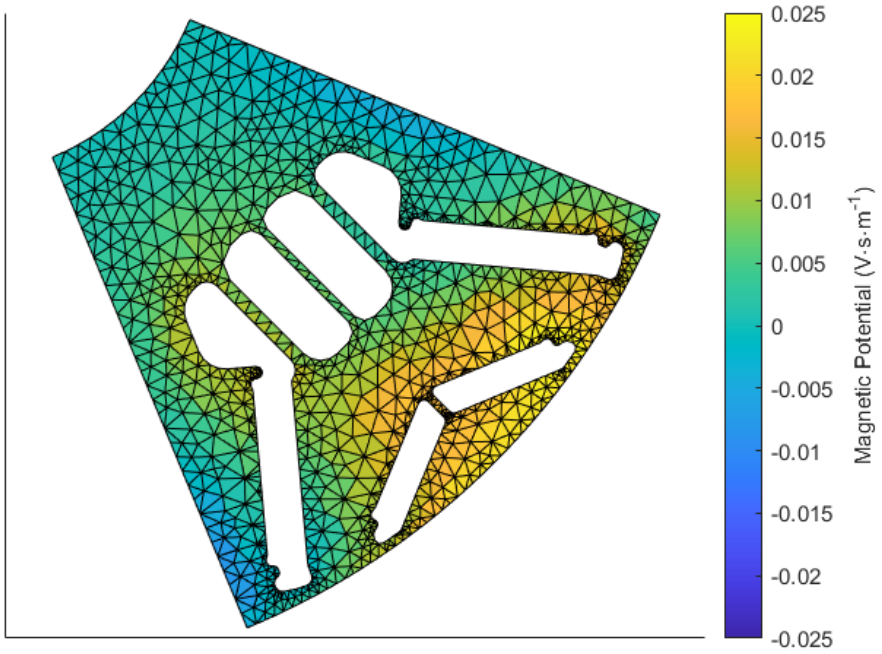

Figure 3.3: Rotor Magnetic Potential

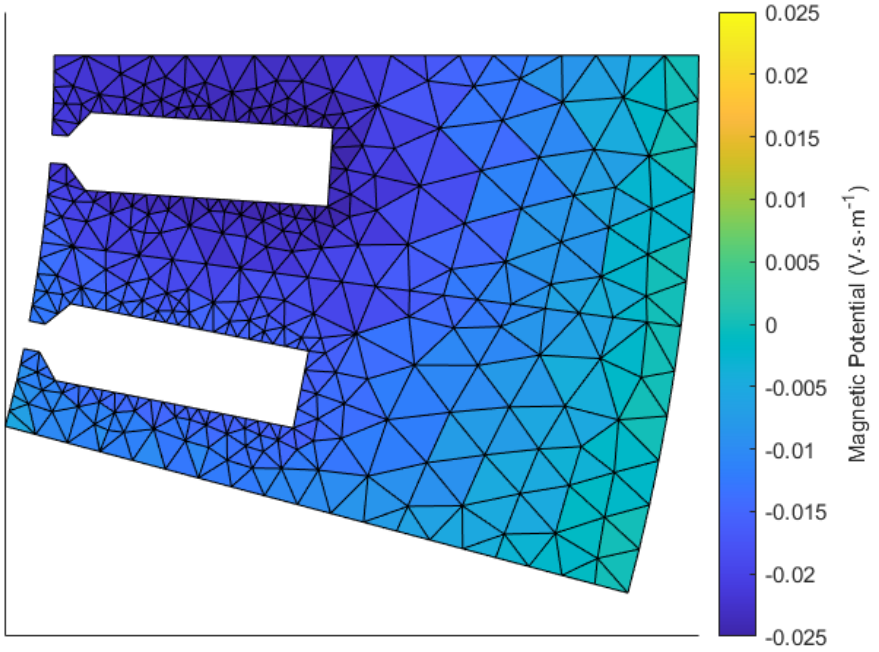

Figure 3.4: Stator Magnetic Potential

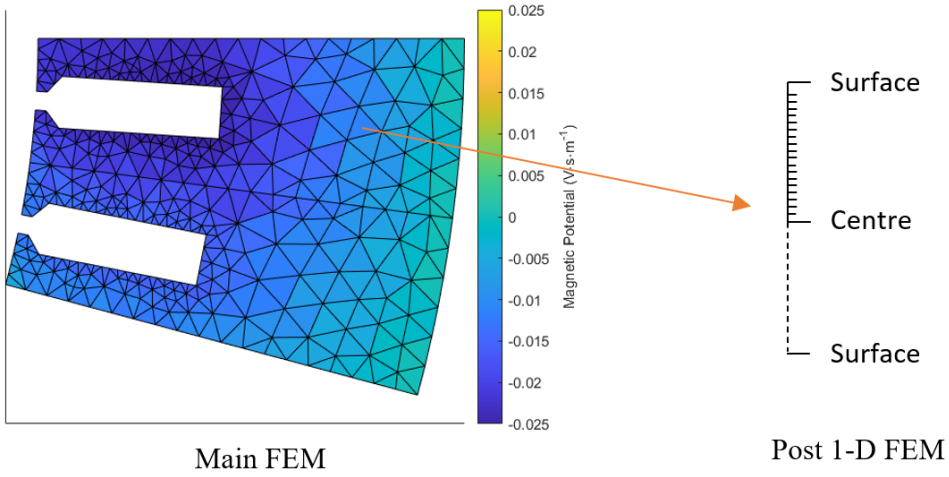

Figure 3.5: The Schematic for the Main FEM and Post 1-D FEM

The eddy-current loss can be calculated from the magnetic vector potential obtained by the post 1-D FEM as

$$P_e = \sum_{j=1}^{n_e} \frac{2n_{sym}S_j l}{Th} \int_0^T \int_0^{\frac{h}{2}} \frac{\kappa}{\rho} \left| \frac{\partial \boldsymbol{A}_j}{\partial t} \right|^2 dz\, dt \tag{3.5}$$

where n_e represents the number of elements in the main FEM, n_{sym} represents the symmetrical multiplier, S_j represents the area of the jth element, l represents the active length, T represents the sampling period, h represents the laminate thickness, κ represents the excess loss coefficient, ρ represents the steel resistivity, $\boldsymbol{A}_j$ represents the magnetic vector potential obtained by the post 1-D FEM. As is shown in Figure 3.3 and 3.4, the rotor and stator FEM geometry is 180° and 60° in electrical angle respectively. So here, n_{sym} is 8 for the rotor and 24 for the stator.

The hysteresis loss can also be calculated from the results of the post 1-D FEM as

$$P_h = \sum_{j=1}^{n_e} \sum_{k=1}^{n_l} \frac{2n_{sym}S_j z_k l f_1}{Th} \int_0^T K_h B_{ij}^2\, dt \tag{3.6}$$

where n_l represents the number of layers in the post 1-D FEM, z_k represents the layer thickness, f_1 represents the fundamental frequency, K_h represents the hysteresis loss coefficient, B_{ij} represents the magnitude of the flux density.

So the total iron losses are

$$P_{Fe} = P_{h\_r} + P_{e\_r} + P_{h\_s} + P_{e\_s} \tag{3.7}$$

where P_{h_r} and P_{h_s} represent the rotor and stator hysteresis loss respectively, P_{e_r} and P_{e_s} represent the rotor and stator eddy-current loss respectively. The parameters used for iron loss calculation are listed in Table 3.4.

Table 3.4: Parameters for the Iron Loss Calculation

Parameter	Value	Unit
l	107	mm
h	0.26	mm
K_h	220	
κ	2	
ρ	52	$\mu\Omega \cdot \mathrm{cm}$

3.4.3 Copper Loss Model

To simplify, we ignore the temperature effect for the phase resistance. So the copper loss can be found as

$$P_{Cu} = \frac{3}{2} R_s \hat{I}_1^2 \tag{3.8}$$

3.5 HiL Test Automation Setup

dSPACE SCALEXIO provides application programming interfaces (APIs) which can be called by Python. Both the ConfigurationDesk and ControlDesk can be controlled in this way. In this thesis project, we will only focus on the ControlDesk automation. Test automation is especially useful for repetitive work such as comparing different operating points, doing parameter sweeps and generating loss maps.

There are two different ways to implement HiL test automation. One is the direct approach and another one is the indirect approach. In the direct approach, all scripts are implemented in the internal interpreter of the ControlDesk. Instruments in the ControlDesk can be customized in this way if the original ones are not capable of meeting some unique requirements. The ControlDesk also has an interactive interpreter in which almost all the operations of the ControlDesk can be automated.

However, there is a limitation to the direct approach. When testing and measuring different operating points, usually we want to wait for a while until the system reaches a steady state. But if the "sleep" command in Python is executed, it will pause the whole HiL Rig platform. So in this thesis project, an indirect approach is chosen to overcome this problem. In the indirect approach, a third-party interpreter can be used to control almost everything from configuring tasks to testing and measuring data. It has similar functions to the interactive interpreter in the direct approach. But when it executes the "sleep" command, it will only pause itself instead of affecting the whole HiL Rig platform.

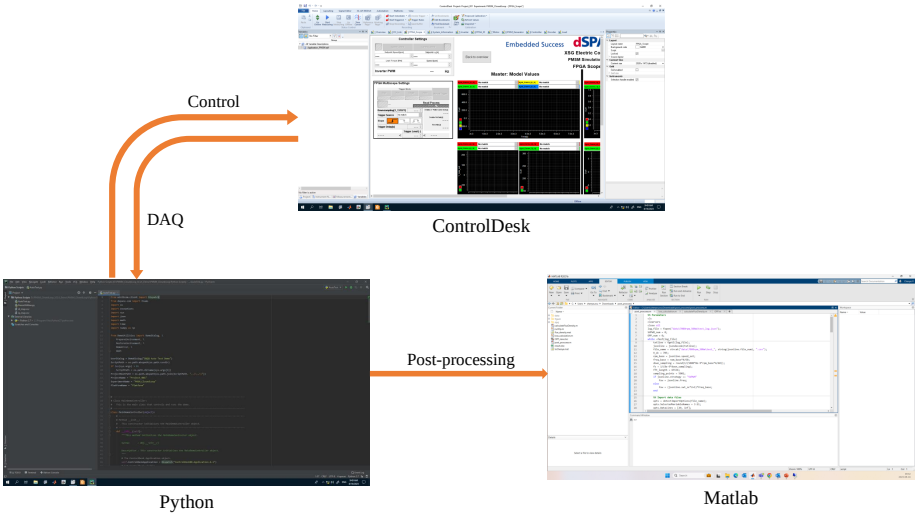

Figure 3.6: HiL Test Automation Workflow

Figure 3.6 shows the HiL test automation workflow using the indirect approach. All the operating points that need to be tested are set in a Python script. The script runs with an external Python interpreter for control and DAQ. It will first start the ControlDesk and load the experiment. For each operating point, all the parameters and settings such as required d-axis and q-axis current, modulation method, switching frequency will be sent to ControlDesk according to the field-oriented control (FOC) map. Then it will trigger the FPGA scope and start the measurement. Each test case will create a separate data file. After testing all operating points, these measurement data will be sent to Matlab for post-processing. Matlab will calculate losses for each case according to loss models introduced in Section 3.4.

4

Optimized Pulse Pattern

4.1 Basic Principles of OPP

In this section, basic principles of OPP will be discussed according to[8]. We will take a quarter-wave symmetry OPP which aims to minimize harmonic distortions in inverter currents as an example.

The THD of inverter currents I_{THD} can be calculated by

$$I_{\mathrm{THD}} = \frac{\sqrt{\sum_{n\neq 1} \hat{I}_n^2}}{\hat{I}_1} \times 100\% \tag{4.1}$$

where n represents the harmonic order, $\hat{I}_1$ represents the amplitude of the fundamental current, $\hat{I}_n$ represents the nth order harmonics.

To simplify the derivation of the target function, assuming the inverter is connected to a purely inductive load with inductance L_σ despite a practical PMSM also has resistance and back EMF, and those parameters are not constant. Then the amplitude of the nth order harmonics is

$$\hat{I}_n = \frac{\hat{u}_n}{n\omega_1 L_\sigma} \tag{4.2}$$

where $\hat{u}_n$ represents the amplitude of the phase voltage, ω_1 represents the angular fundamental frequency.

By substituting (4.2) into (4.1), the following expression is found,

$$I_{\mathrm{THD}} = \frac{1}{\hat{I}_1\omega_1 L_\sigma}\sqrt{\sum_{n\neq 1}\frac{\hat{u}_n^2}{n^2}} = \frac{1}{\hat{I}_1\omega_1 L_\sigma}\sqrt{\sum_{n\neq 1}\frac{a_n^2+b_n^2}{n^2}} \tag{4.3}$$

where a_n and b_n are the Fourier coefficients of u_n.

The next step is to get the expression for the phase voltage amplitude $\hat{u}_n$. Considering quarter-wave symmetric OPP and bipolar switch positions, we define switching angles as α_i $(i = 1, 2, ..., d)$. Here, d represents the number of adjustable switching angles within one quarter period. So the single phase voltage $u(\theta)$ in the first quarter cycle is

$$\begin{aligned} u(\theta) &= \begin{cases} U_{DC}, & \alpha_i < \theta < \alpha_{i+1},\ i = 0, 2, \dots \\ 0, & \alpha_i < \theta < \alpha_{i+1},\ i = 1, 3, \dots \end{cases} \\ &= (-1)^i \frac{U_{DC}}{2} + \frac{U_{DC}}{2},\ \alpha_i < \theta < \alpha_{i+1},\ i = 0, 1, \dots, d \end{aligned} \tag{4.4}$$

where θ represents the electric angle. To simplify, we assume $\alpha_0 = 0$, $\alpha_{d+1} = \frac{\pi}{2}$.

According to (2.5), b_n can be calculated by

$$\begin{aligned}
b_n &= \frac{4}{\pi}\int_0^{\pi/2} u(\theta)\sin(n\theta)\,d\theta,\ n = 1,3,5,\dots \\
&= \frac{2U_{DC}}{\pi}\sum_{i=0}^{d}\int_{\alpha_i}^{\alpha_{i+1}} (-1)^i \sin(n\theta)\,d\theta,\ n = 1,3,5,\dots \\
&= \frac{2U_{DC}}{n\pi}\sum_{i=0}^{d}(-1)^{i+1}(\cos(n\alpha_{i+1}) - \cos(n\alpha_i)),\ n = 1,3,5,\dots \\
&= \frac{2U_{DC}}{n\pi}\left((-1)^0\cos\alpha_0 + 2\sum_{i=1}^{d}(-1)^i\cos(n\alpha_i) + (-1)^{d+1}\cos\alpha_{d+1}\right),\ n = 1,3,5,\dots \\
&= \frac{2U_{DC}}{n\pi}\left(1 + 2\sum_{i=1}^{d}(-1)^i\cos(n\alpha_i)\right),\ n = 1,3,5,\dots
\end{aligned} \tag{4.5}$$

So considering quarter-wave symmetry and bipolar switch positions, a_n and b_n can be represented by

$$a_n = 0,\ n = 0,1,2,\dots \tag{4.6a}$$

$$b_n = \begin{cases} \dfrac{2U_{DC}}{n\pi}\left(1 + 2\displaystyle\sum_{i=1}^{d}(-1)^i\cos(n\alpha_i)\right), & n = 1,3,5,\dots \\ 0, & n = 2,4,6,\dots \end{cases} \tag{4.6b}$$

Define the modulation index of six step modulation as 1. Then the modulation index m can be determined as

$$m = \frac{\sqrt{a_1^2 + b_1^2}}{\frac{2}{\pi}U_{DC}} = 1 + 2\sum_{i=1}^{d}(-1)^i\cos\alpha_i \tag{4.7}$$

Since the semiconductors will also switch at $\alpha = 0$ and π, the total number of switching events per period is $4d + 2$, which means $2d + 1$ switching pulses. The equivalent switching frequency f_{sw} is

$$f_{sw} = (2d+1)f_1 = (2d+1)\frac{n_p\Omega}{60} \tag{4.8}$$

where f_1 represents the fundamental frequency, n_p represents the number of pole pairs, Ω represents the mechanical speed of the electrical machine.

In order to minimize the inverter current THD, (4.3) can be used as the target function. However, we do not care about the value of I_{THD}. What is important is the set of $\boldsymbol{\alpha}$ ($\boldsymbol{\alpha} = \{\alpha_1, \alpha_1, \dots \alpha_d\}$) which can be used to implement OPP. So we can ignore the constant factor and the square root function. In this way, we can reduce the computational complexity. Finally, the target function and constraints can be written as

$$\min_{\boldsymbol{\alpha}} \quad J(\boldsymbol{\alpha}) = \sum_{n=5,7,11,\dots}\frac{a_n^2 + b_n^2}{n^2} \tag{4.9a}$$

$$\text{subject to} \quad b_1 = m \tag{4.9b}$$

$$\alpha_{i+1} - \alpha_i > 0,\ i = 0,1,\dots,d \tag{4.9c}$$

This will be solved with "fmincon" in Matlab. A problem for "fmincon" is that it needs a starting point to begin the search. So it will fall into a local optimum solution. In order to get a global optimum solution, the easiest way is to exhaustive combinations of switching angles with a certain step size. Of course, this brings a huge amount of calculation. But since it is an offline calculation, it will not affect the efficiency of OPP.

4.2 The Process Model with OPP

According to (4.9), optimized pulse patterns can be generated. The result is a 2-D LUT in related to modulation index m and the number of switching angles per quarter period d which is shown in Figure 4.1. Here, m ranges from 0.1 to 1 and the step size is 0.01. d ranges from 2 to 10 and the step size is 1.

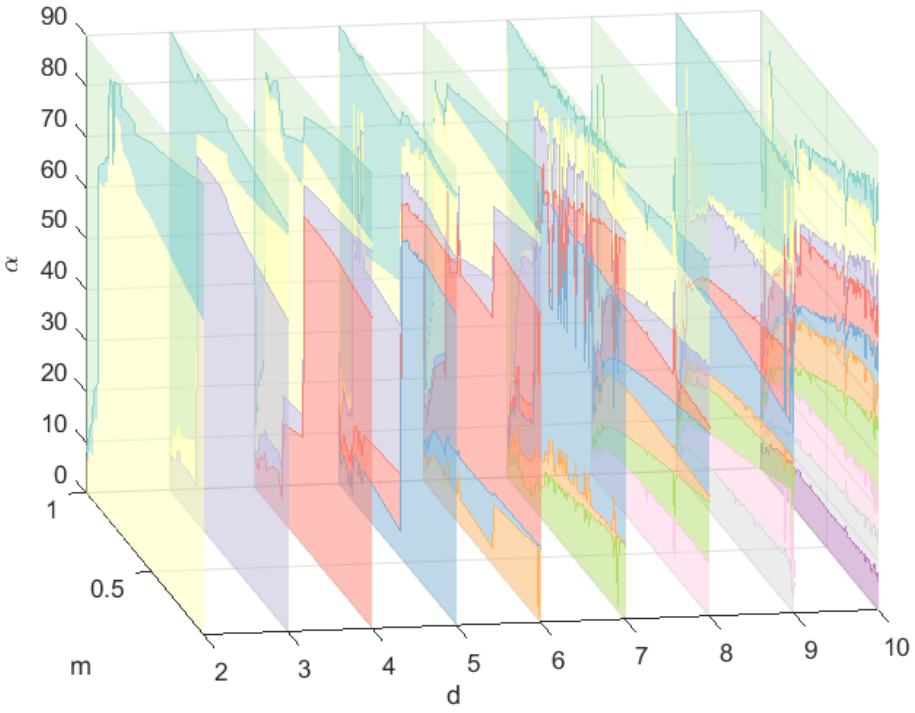

Figure 4.1: Generated Optimized Pulse Pattern

This 2-D LUT is used in the process model with OPP implementation. Figure 4.2 shows the pulse pattern when $d = 4$. Different colors represent different angles.

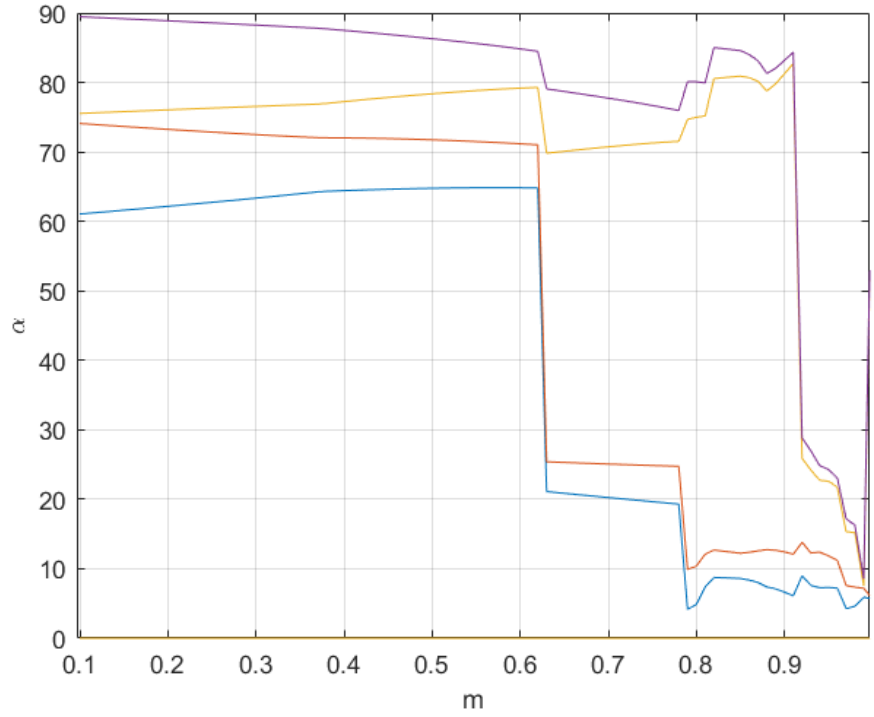

Figure 4.2: The Relationship between $\boldsymbol{\alpha}$ and m ($d = 4$)

After the optimization process, the three-phase voltage waveforms can be generated according to the 2-D OPP LUT. Figure 4.3 shows the schematic for restoring the correct waveform from the LUT.

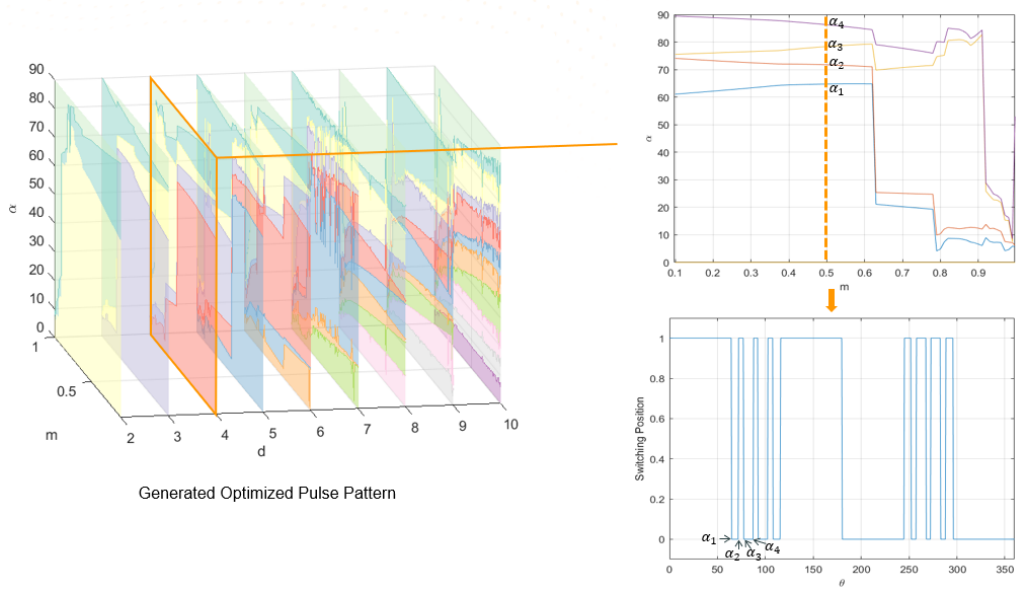

Figure 4.3: Schematic for Generating the Waveform from the LUT

According to the required number of switching angles d, a 1-D LUT can be selected from the set, which is the orange dashed line shown in Figure 4.3. Then,

the selected LUT is interpolated depending on the required modulation index m. In Figure 4.3, it shows the case when $d = 2$ and $m = 0.5$. The set of switching angles $\boldsymbol{\alpha} = \{\alpha_1, \alpha_2, \alpha_3, \alpha_4\}$ is obtained from the LUT. At the beginning of each period, the gate signal is at a high state. Then, the processor will compare the current rotor position with the pulse pattern. When it reaches a certain switching angle, the gate driver will toggle the signal. Thus, the phase voltage waveform can be restored from the pulse pattern.

The above process is an ideal case in which we assume that the processor is very fast and has no upper limitation on the sampling frequency. In other words, we assume that the processor can know the rotor position at any time. However, for a practical ECU, the maximum sampling frequency is limited. If there are two or more switching angles exist in the same sampling period, The ECU can only recognize the first one, which will cause problems. This will be further discussed in Chapter 5.

5

Results and Analysis

5.1 Evaluation of OPP Implementation

The OPP implementation inside the process model will be evaluated with open-loop control. Figure 5.1 and 5.2 show the inverter output voltage and current waveforms. The mechanical speed Ω is set as 5000 rpm, torque is set as 200 Nm and the number of adjustable switching angles within one quarter period d is set as 4. These give an equivalent switching frequency f_{sw} of 3000 Hz and a fundamental frequency of 333.33 Hz.

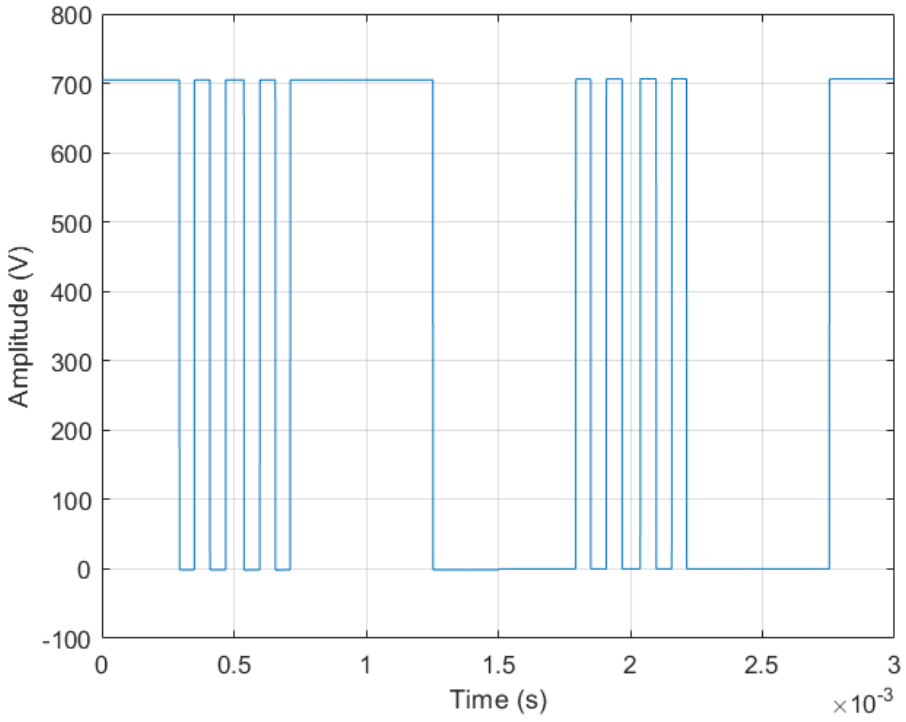

Figure 5.1: Inverter Output Voltage of Phase A with OPP

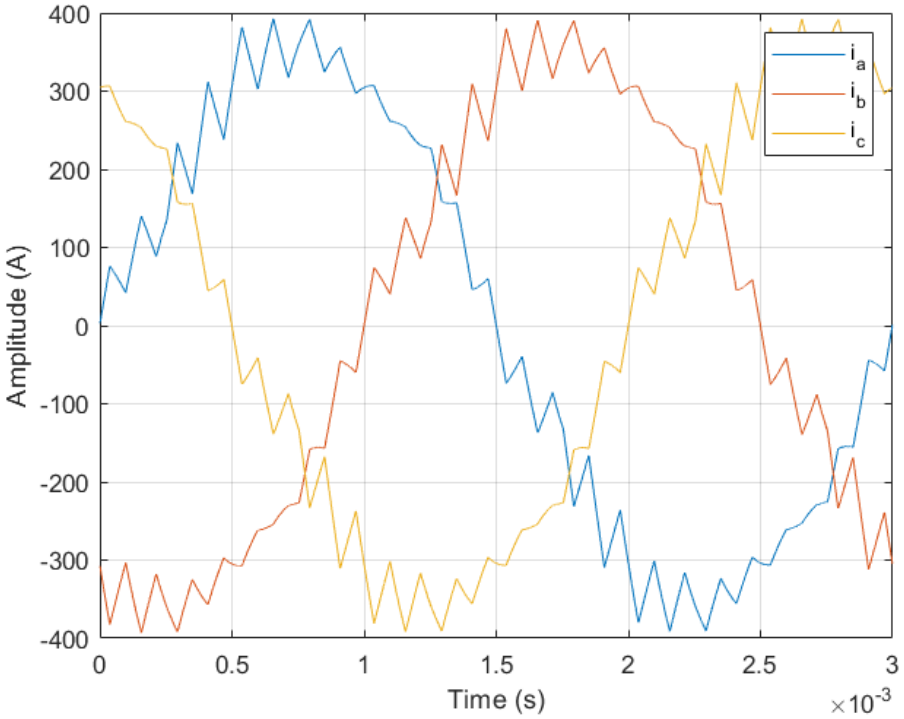

Figure 5.2: Inverter Output Current with OPP

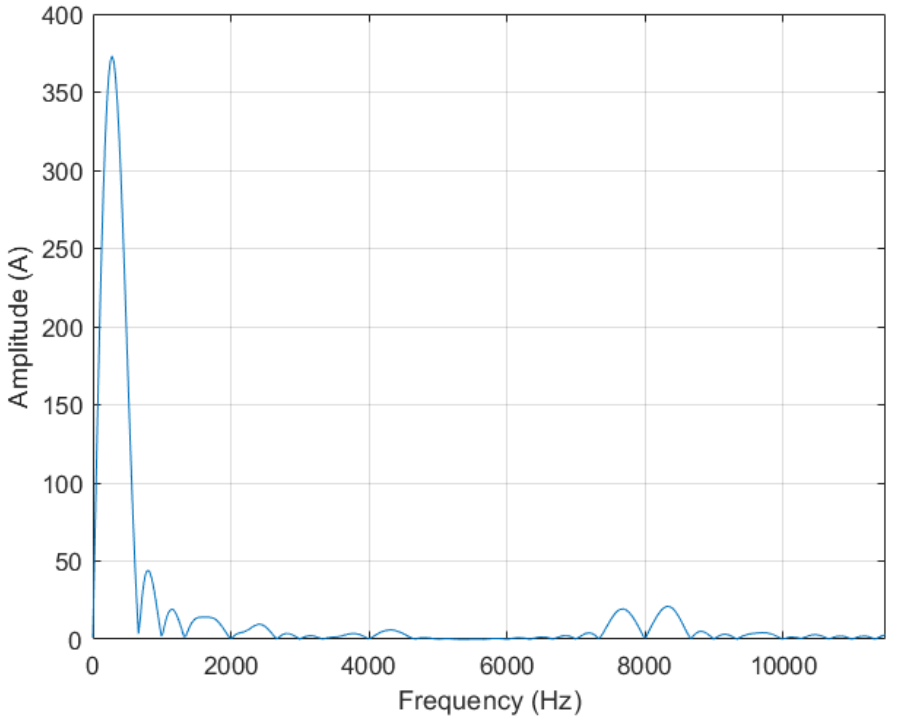

Figure 5.3: Frequency Spectrum of Inverter Output Current with OPP

The frequency spectrum can be obtained by applying Fourier transformation to

the inverter output current, as is shown in Figure 5.3. 7th, 11th, 13th, 17th and 19th-order harmonics can be seen in this case but their amplitude is not very high since OPP is designed to minimize these harmonic components. However, we can see some subharmonics from the spectrum. Compared with SVPWM, OPP lacks a fixed time interval for sampling and comparing between carrier wave and reference voltage[15], which brings more harmonics.

Table 5.1 shows the comparison of the inverter output current THD with SVPWM and OPP respectively at 5000 rpm and 200 Nm. Both SVPWM and OPP have the same equivalent switching frequency f_{sw} of 3000 Hz. It shows that OPP has a lower I_{THD} than SVPWM under the same equivalent switching frequency.

Table 5.1: Comparison of Inverter Output Current THD

Method	d	f_{sw}	I_{THD}
SVPWM		3000	8.93 %
OPP	4	3000	7.59 %

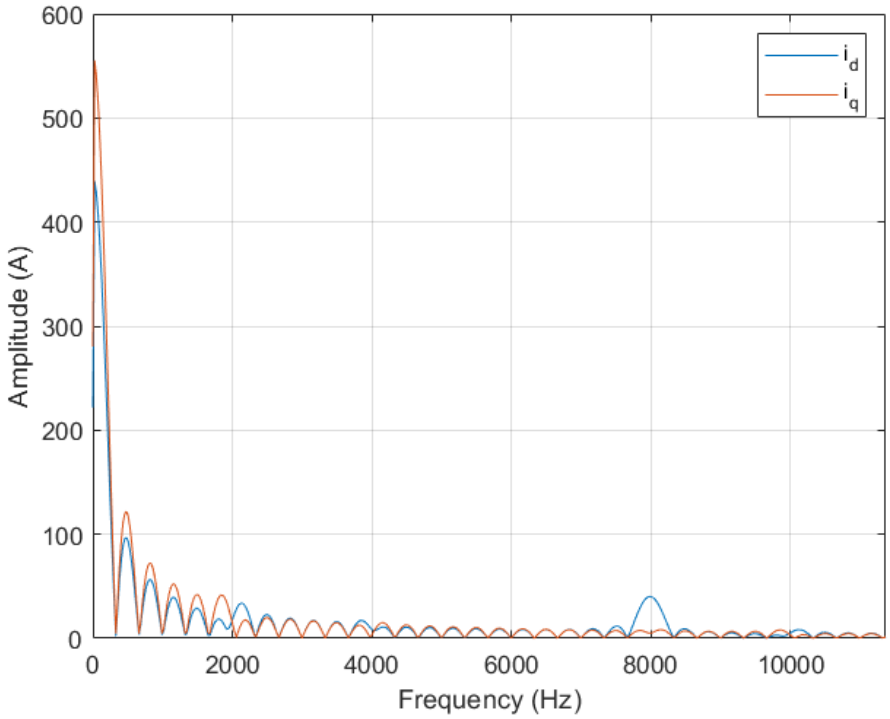

Figure 5.4: Frequency Spectrum of DQ-axis Current with OPP

By applying Park and Clarke transformation to the three-phase current, i_d and i_q can be obtained. For SVPWM, they can be used for the closed-loop control of the PMSM. However, it is not the case for OPP. Figure 5.4 shows the frequency spectrum of i_d, i_q. There are large harmonic components for both i_d and i_q at low frequency which makes it hard to design a digital low pass filter and filter them out. For the controller, only dc components are needed. The rest harmonics will make

the controller unstable. In order to achieve good dynamic responses for OPP with closed-loop control, MPC can be used[15]. But it will not be discussed in this thesis report.

As a result, for the following tests in the following sections, SVPWM will be tested with closed-loop control for a specific operating point first. Then at steady state, the controller will switch to open-loop control to test OPP for the same operating point.

5.2 The Comparison between OPP and SVPWM

In this section, two operating points which are 3000 rpm 200 Nm and 5000 rpm 200 Nm will be tested. The number of switching events per quarter period of OPP will be swept and the optimal parameter will be chosen for the performance comparison with SVPWM.

5.2.1 The Operating Point at 3000rpm 200Nm

Figure 5.5 shows the comparison of the switching loss and iron loss between SVPWM and OPP at 3000 rpm 200 Nm. SVPWM is running at 10 kHz. It shows in the dark grey label that at $d = 4$, OPP achieves the lowest loss. For SVPWM, the summation of the switching loss and iron loss is 687.32 W. While for OPP, it is 523.64 W. Here, the copper loss and conduction loss are not plotted in the figure because they are assumed to be the same since the operating point is the same. As d increases, the switching loss of OPP increases as well, which is as expected. The switching loss of OPP is much lower than that of SVPWM, because the equivalent switching frequency is lower. But for the iron loss, it has a tendency to drop first, and then it increases. Theoretically, with more switching events in a period, the inverter output current THD will decrease, which brings a lower iron loss. However, since OPP is running in the open loop, it is not stable enough. D-axis and q-axis current cannot perfectly follow the reference, which makes the iron loss vary. This problem will be further discussed in Section 5.3.

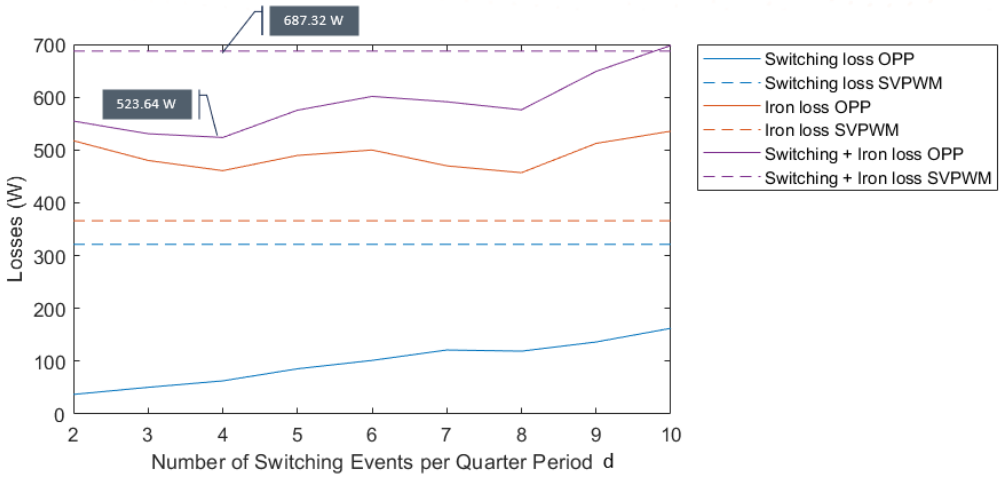

Figure 5.5: The Comparison between SVPWM and OPP at 3000 rpm 200 Nm

Table 5.2 shows the comparison of total losses, which includes the switching loss, conduction loss, iron loss and copper loss, between SVPWM and OPP at 3000 rpm 200 Nm. It shows a 4.60 % loss reduction for OPP at $d = 4$.

Table 5.2: Comparison of Total Losses at 3000 rpm 200 Nm

d	P_{SVPWM}	P_{OPP}	ΔP %
4	3498 W	3335 W	4.60 %

5.2.2 The Operating Point at 5000rpm 200Nm

Figure 5.6 shows the comparison of the switching loss and iron loss between SVPWM and OPP at 5000 rpm 200 Nm. SVPWM is running at 10 kHz. It shows in the dark grey label that at $d = 2$, OPP achieves the lowest loss. For SVPWM, the summation of the switching loss and iron loss is 875.59 W. While for OPP, it is 1092.90 W. As d increases, the switching loss of OPP increases as well, which is the same as that at 3000 rpm 200 Nm. For the iron loss, it almost remains the same and is close to the iron loss of SVPWM. At 5000 rpm, the fundamental wave dominates the iron loss. As a result, the iron loss does not show much difference even though the current THD is lower with a higher d.

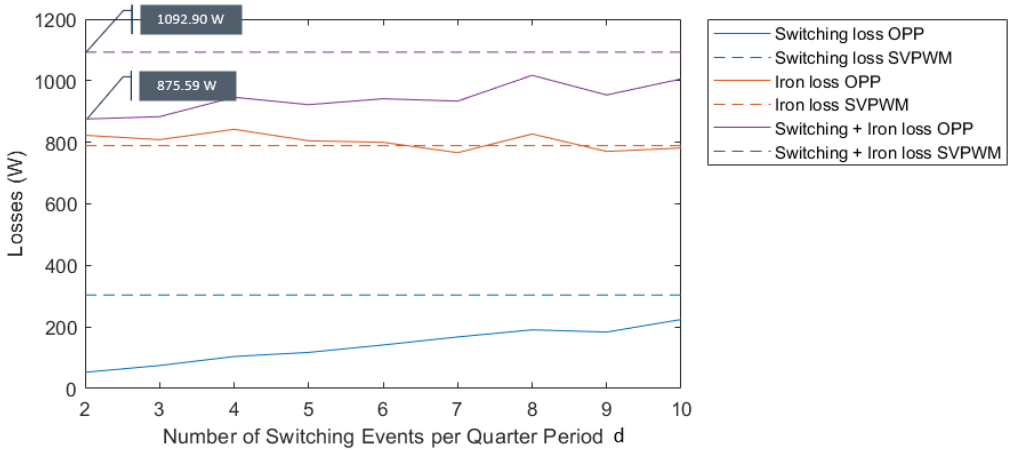

Figure 5.6: The Comparison between SVPWM and OPP at 5000 rpm 200 Nm

Table 5.3 shows the comparison of total losses which includes the switching loss, conduction loss, iron loss and copper loss, between SVPWM and OPP at 5000 rpm 200 Nm. It shows a 5.57 % loss reduction for OPP at $d = 2$.

Table 5.3: Comparison of Total Losses at 5000 rpm 200 Nm

d	P_{SVPWM}	P_{OPP}	ΔP %
2	3901 W	3683 W	5.57 %

5.2.3 Harmonics Differences

Figure 5.7 shows the frequency spectrum of the inverter output current with SVPWM. Compared with Figure 5.3, the output current does not have many low order harmonics. The main harmonic component for SVPWM is the switching harmonic.

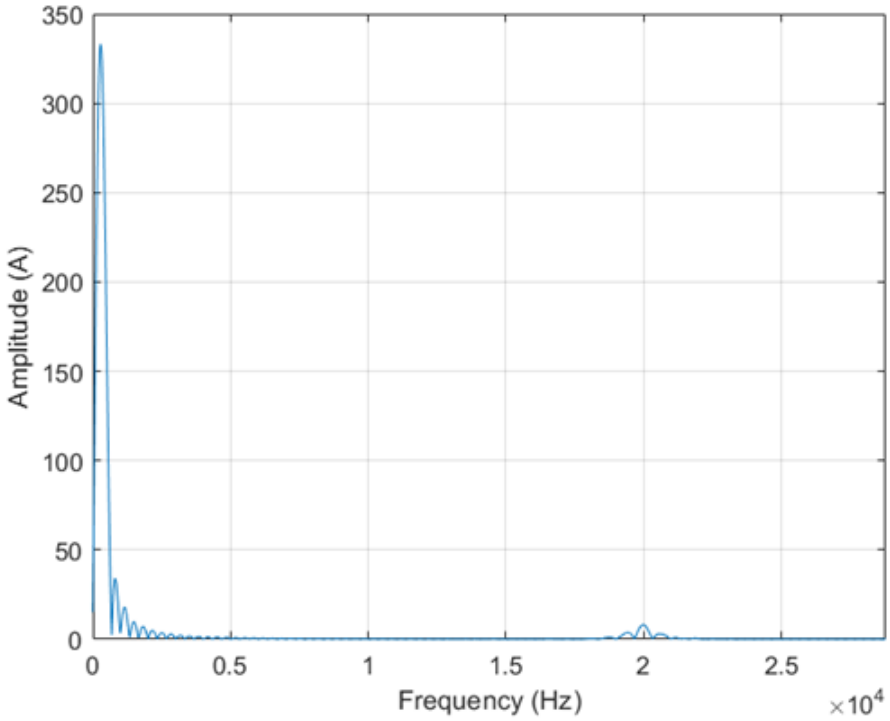

Figure 5.7: Frequency Spectrum of Inverter Output Current with SVPWM

Figure 5.8 and 5.9 show the radial flux density distribution along the stator laminate with SVPWM and OPP respectively. And they are selected from the same location as the stator. For SVPWM, the switching frequency f_{sw} is 10 kHz. For OPP, the number of switching angles per quarter period d is 2. Both of these two figures are tested at the same operating point of 5000 rpm 200 Nm. The dark green curve shows the distribution at the surface of the laminate, and the light green shows the flux density distribution in the center.

As we can see from Figure 5.8 and 5.9, the high frequency harmonics are mainly concentrated at the surface of the laminate due to the skin effect. In the center of the laminate, it is mainly the fundamental wave component for both SVPWM and OPP. For SVPWM, the laminate surface harmonics are mainly switching harmonics. While for OPP, they are low order harmonics but have a larger ripple than that of SVPWM. These are in line with the current spectrums which are shown in Figure 5.3 and 5.7.

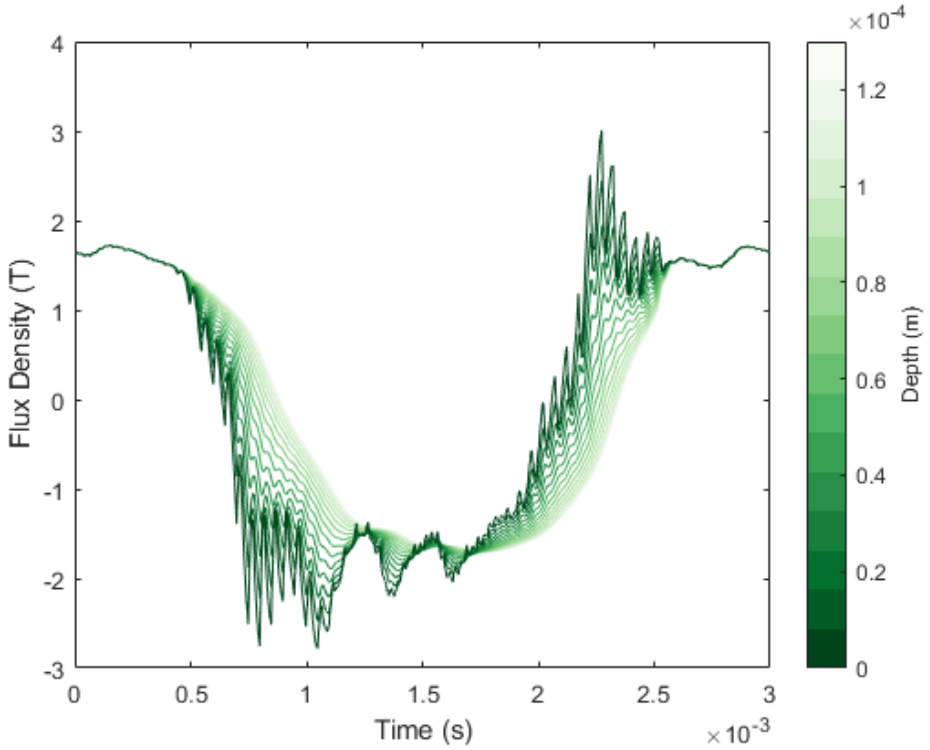

Figure 5.8: Flux Density Distribution Along the Stator Laminate with SVPWM

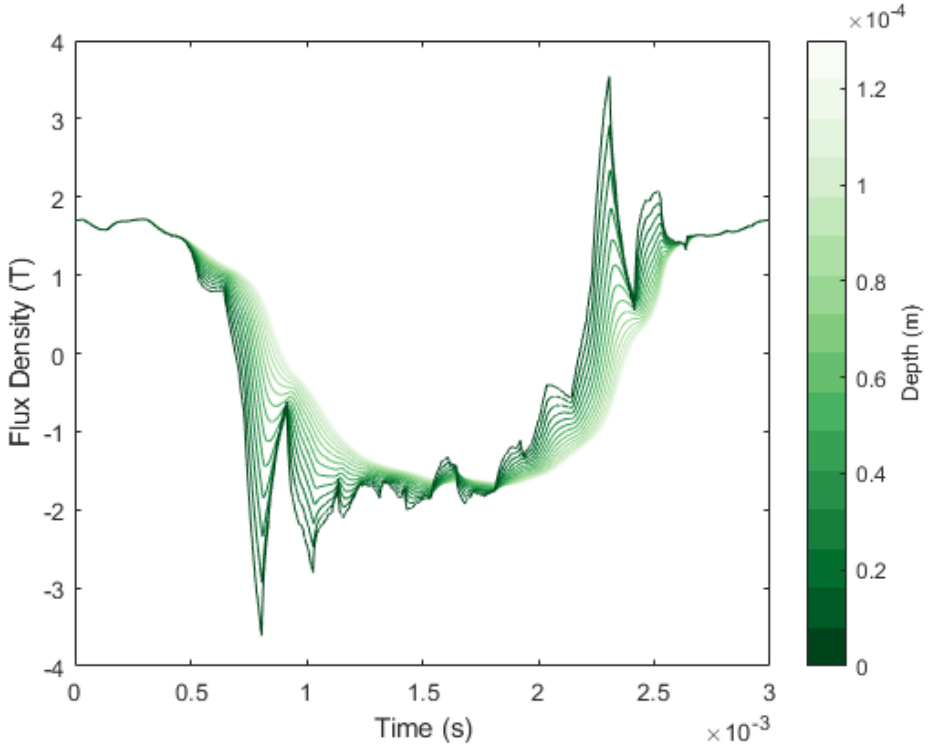

Figure 5.9: Flux Density Distribution Along the Stator Laminate with OPP

5.3 Existing Problems of OPP Implementation

5.3.1 Sampling Period Error

For the above OPP implementation, the biggest limitation is the maximum sampling rate of the ECU. During each sampling period, the ECU can only deal with one switching event. Otherwise, if two or more switching events occur, the ECU will fail to restore the waveform and will only respond to the first one that occurs. At a high speed or high modulation index, usually the time interval between two adjacent angles will be quite small. And that will limit the operating range of OPP.

But if the angle constraint in (4.9) is modified to

$$\min_{\boldsymbol{\alpha}} \quad J(\boldsymbol{\alpha}) = \sum_{n=5,7,11,\ldots} \frac{a_n^2 + b_n^2}{n^2} \tag{5.1a}$$

$$\text{subject to} \quad b_1 = m \tag{5.1b}$$

$$\alpha_{i+1} - \alpha_i > \Delta\alpha_{min},\ i = 0, 1, \ldots, d \tag{5.1c}$$

where $\Delta\alpha_{min}$ represents the minimum angle resolution.

Then the adjacent angles of OPP will not be too close for the ECU to process. Although the performance of OPP might be slightly affected, it avoids the sampling period error. However, $\Delta\alpha_{min}$ cannot be too big. Otherwise, it will be hard for Matlab to get an optimal solution. The minimum angle resolution $\Delta\alpha_{min}$ of OPP can be calculated by

$$\Delta\alpha_{min} = \omega_r T_s = \frac{\pi\Omega n_p}{30 f_s} \tag{5.2}$$

where ω_r represents the electrical speed, T_s represents the ECU sampling period, f_s represents the ECU sampling frequency.

According to (5.2), the minimum angle resolution map can be generated as is shown in Figure 5.10 assuming $n_p = 4$.

The way to solve this problem is to increase the sampling frequency of the ECU. For the HiL Rig platform, in order to maintain real-time simulation, the maximum sampling frequency is 40 kHz. The situation will be even worse for a normal ECU which may only have the capability of running at 10 kHz. According to (5.2) and Figure 5.10, for an ECU with a maximum sampling frequency of 10 kHz, the minimum angle resolution at 5000 rpm is 12°, which is too high. Some researchers[20] used a Field-programmable Control Unit (FPCU) which contains a CPU and a programmable hardware-accelerated area to solve this problem. The CPU will mainly focus on those slow tasks. Meanwhile, the hardware-accelerated area will handle the OPP implementation which can run at 200 kHz, which gives a minimum angle resolution of only 2.16°.

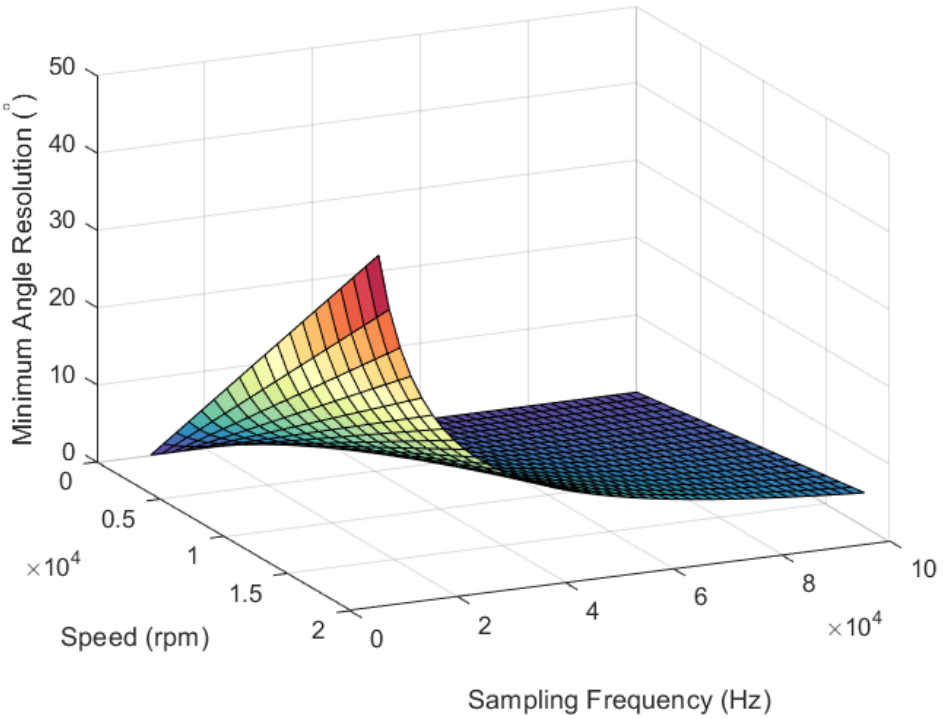

Figure 5.10: Minimum Angle Resolution Map

5.3.2 Interpolation Error

Another source of error is interpolation. According to (4.7), the relationship between the modulation index and switching angles is nonlinear so there are always some errors during interpolation. When α_i does not change much, (4.7) can be linearized by taking the derivative at that point. So this interpolation error is very small. But when α_i changes a lot, which means the slope of switching angles is very steep on the OPP LUT, this error cannot be ignored.

Figure 5.11 shows the comparison between switching angles and interpolation error when $d = 4$. Here, for the y-axis, m_{actual} represents the actual modulation index calculated by (4.7) with the interpolated switching angles and m represents the required modulation index. Most of the time, the error is almost zero but there are some peaks when the slope of switching angles is very steep.

Figure 5.12 shows the interpolation error versus d and m. The maximum error occurs at $d = 5$, $m = 0.526$ and is around 0.06. Another local maximum point is at $d = 3$, $m = 0.795$ and the absolute error is around 0.05. For an 800 V platform, this will bring a voltage swell of around 20 V in maximum.

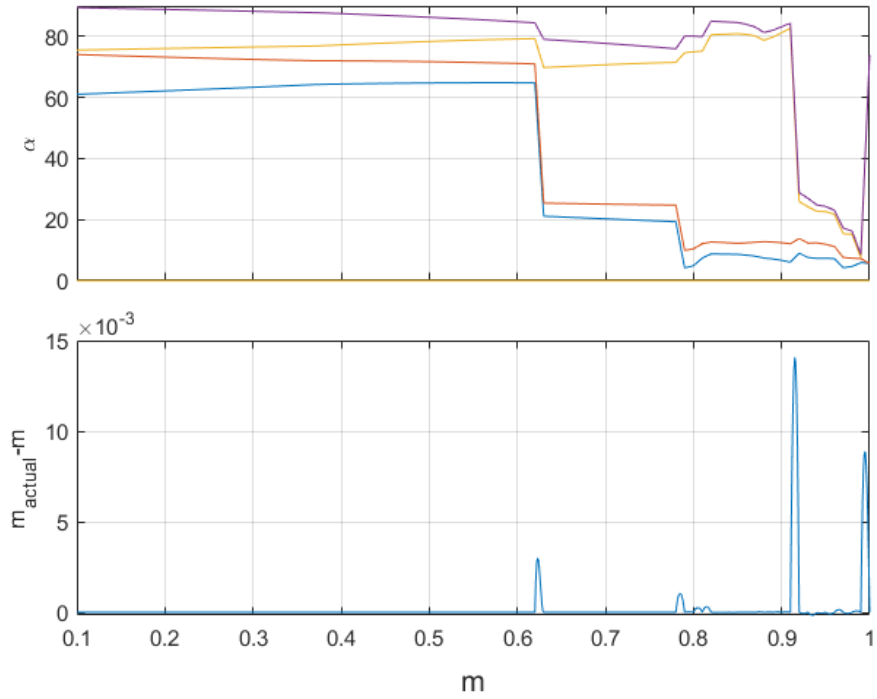

Figure 5.11: Comparison between Switching Angles and Interpolation Error ($d = 4$)

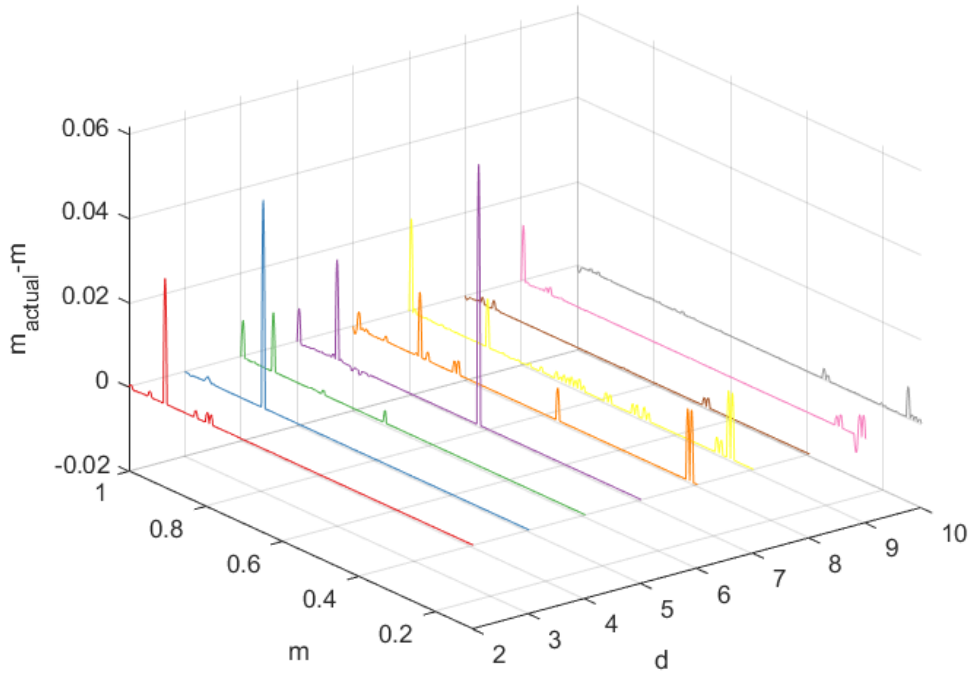

Figure 5.12: Interpolation Error Versus d and m

Most of the time, the interpolation error is very small and can be ignored. However, it may still affect the control loop. The easiest way to reduce this interpolation error is using a finer resolution to generate OPP at where the interpolation error is big. Another way is adding new constraints or some penalty coefficients to the target function which can limit the slope of switching angles while generating OPP. This will smooth the generated pattern at the cost of reducing the performance of OPP a little bit.

5.4 Operating Range of OPP

Due to existing problems of the OPP implementation, the operating range of OPP is limited. Figure 5.13 shows the d-axis and q-axis current versus the number of adjustable switching angles per quarter period d for OPP running at 7000 rpm and 50 Nm. The blue solid line stands for d-axis current and the orange solid line stands for q-axis current. When d increases, although the equivalent switching frequency increases, which can reduce the harmonics, the difference between two adjacent angles tends to be very small. This will cause a sample time error which is illustrated above. Thus there will be a gap between the reference and the actual current value.

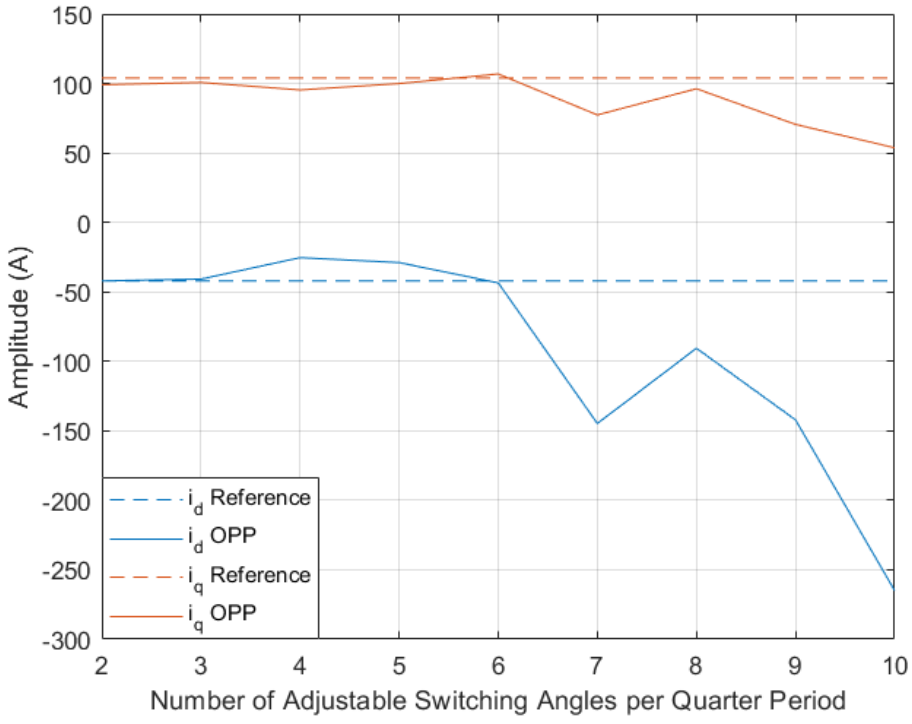

Figure 5.13: D-axis and Q-axis Current Versus d Diagram

Figure 5.14 shows the d-axis and q-axis current versus rotating speed for SVPWM and OPP. The motor runs at 100 Nm using FOC. Blue lines represent the d-axis current and orange lines represent the q-axis current. Meanwhile, dashed lines stand for SVPWM and solid lines stand for OPP. Some oscillations can be observed for

OPP. This is caused by the open-loop control of OPP which will always bring some errors. Since SVPWM is tested in a closed loop, they are quite stable and can be treated as a reference.

Below 2000 rpm, it is hard to use OPP because the equivalent switching frequency is too low which brings a lot of harmonics. When it is above 7000 rpm, a gap between SVPWM and OPP for the q-axis current can be observed. Compared with the reference value, the q-axis current of OPP is much lower which means it can not reach the target torque. At a high speed, the modulation index will be high with FOC. So the difference between two adjacent angles will be very small. Also, higher speed means a smaller time interval even for the same angle difference. Both factors work together to create an even greater challenge for the ECU. As we can see from Figure 5.14, the highest possible operating speed for OPP at 100 Nm is around 7000 rpm. This speed limit will be even lower for a heavier load since the modulation index will be higher.

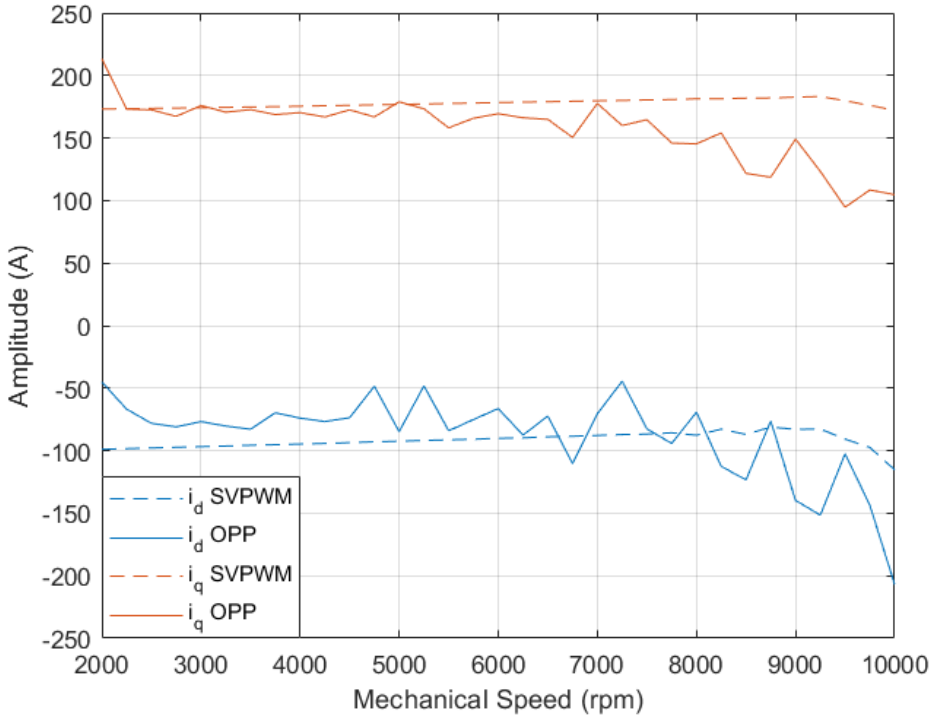

Figure 5.14: D-axis and Q-axis Current Versus Mechanical Speed Diagram

However, the above analyses are only valid for the current OPP implementation. With a better software or hardware, it is possible that these limitations will be overcome.

6
Conclusion

6.1 Results from Present Work

In this thesis project, a complete workflow with the HiL Rig platform is shown, including FPGA plant model design, process model design, testing, data measurement and post-processing. The HiL test automation with Python is also implemented for easier testing. It is a powerful tool for power electronics simulation with both fast speed and high accuracy.

According to the test results, OPP has a lower inverter output current THD than SVPWM under the same equivalent switching frequency. OPP shows lower losses compared with SVPWM for certain operating points. As the number of switching pulses per quarter period increases, OPP has a higher equivalent switching frequency. Thus the switching losses increase but the iron losses decrease. So there is always an optimal parameter choice for OPP. Of course, OPP does not always win against SVPWM. It struggles at a low speed, suffering from the low equivalent switching frequency. Due to hardware limitation, the drawback of OPP at a high speed or high modulation index is also shown.

6.2 Future work

In the future work, a hardware upgrade is possible for a better performance. With a larger FPGA, a PMSM plant model with 3-D LUTs (d-axis current, q-axis current and rotor position) can be deployed for a higher accuracy. Also, with the current HiL Rig platform, it is hard to evaluate the performance at a high speed since the controller is unstable. A possible way is to use another FPGA which is responsible for fast tasks in the controller. It can also reduce the error caused by the sampling period for OPP.

There is still a lot of work that needs to be done with regard to OPP. First, a closed-loop control algorithm should be realized. Otherwise, it is hard to apply it in practical electric vehicles. Also, some global optimization algorithms can be tried to replace the exhaustive method while generating switching patterns.

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