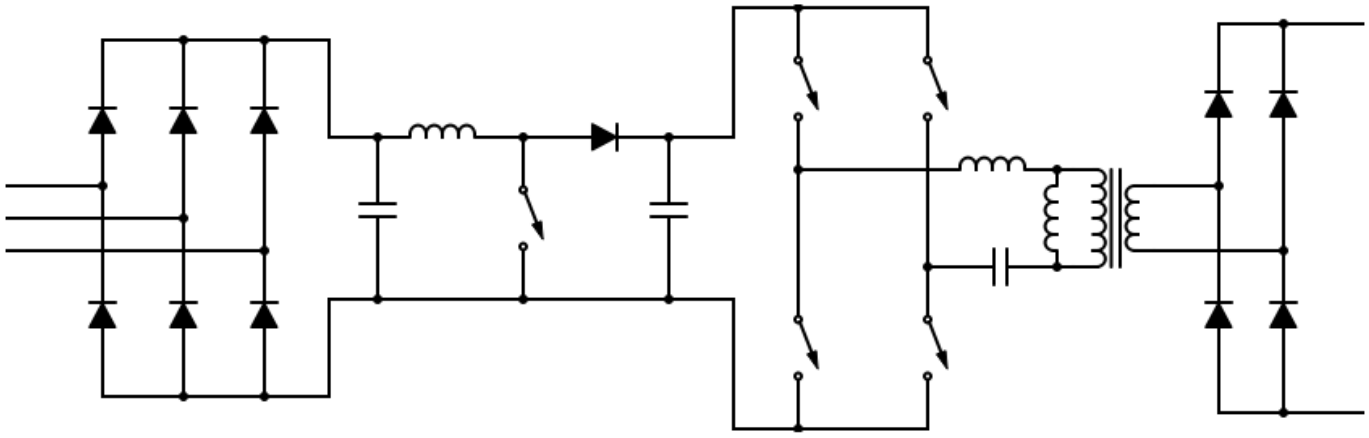
CHALMERS



Design of a grid connected battery charger for a 600 V Formula Student battery using SiC components

Master of Science thesis in Electric Power Engineering

Axel Andalen
Oskar Isaksson

Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg Sweden 2018

Master's thesis 2018

Design of a grid connected battery charger for a 600 V Formula Student battery using SiC components

Axel Andalen & Oskar Isaksson

CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
Göteborg, Sweden 2018

Design of a grid connected battery charger
for a 600 V Formula Student battery
using SiC components
Axel Andalen & Oskar Isaksson

Supervisor: Mikael Alatalo, Aros Electronics
Examiner: Stefan Lundberg, Department of Electrical Engineering

Master's Thesis 2018
Department of Electrical Engineering
Electric Power Engineering
Chalmers University of Technology
SE-412 96 Göteborg
Telephone +46 31 772 1000

Cover: Simplified schematic drawing of the designed two-stage converter

Typeset in LaTeX
Göteborg, Sweden 2018

Abstract

In this thesis, a grid connected battery charger design using SiC components with an output voltage range of 400 V to 600 V is proposed. The charger is supplied by an IEC 60309 standard 3-phase 16 A outlet and has been designed for a power output of 9 kW with a maximum output current of 20 A. Different topologies that fulfil these requirements were modelled and simulated with LTspice, using simulation models of SiC components provided by manufacturers, and the results were compared to find the most feasible solution.

The chosen topology consists of a boost converter with a switching frequency of 50 kHz used for voltage control coupled with an LLC resonant converter operating at unity voltage gain with a resonant frequency of 75 kHz. A buck converter and a SEPIC were also evaluated as alternative topologies. In simulations, the losses in all active components are found to be 303.1 W in the buck based converter and 195.7 W for the boost based converter at an operating point of 450 V and 20 A output. The results are similar for other operating points, motivating the use of a boost based converter for the final design. The use of a boost converter for voltage regulation allows for high power output while keeping currents low in the intermediate DC link and the resonant circuit. With this solution the maximum voltage on the DC link approaches 826 V and for this reason, SiC MOSFETs and Schottky diodes rated for 1200 V are used.

The complete charger, including several auxiliary circuits such as DC-link pre-charge, voltage measurements etc, has been drawn in a schematic that can be used to create a PCB layout for manufacturing. A prototype power transformer has been manufactured and partially tested and can be used in a future prototype of the charger.

Keywords: Battery charger, SiC MOSFET, SiC diode, Boost converter, Buck converter, LLC converter.

Acknowledgements

We wish to express our sincerest gratitude to Mikael Alatalo and Oskar Theliander, Aros Electronics, for their support and guidance as supervisors throughout this project. Additional thanks also go out to Adam Maaninka, Anders Bonde, Marie Wide, Björn Kvarnefalk, Per Lundberg, Per Forsberg and the rest of the development team at Aros Electronics for giving support and showing interest in our project. We also want thank our examiner Stefan Lundberg for valuable feedback and administrative guidance throughout this project.

Axel Andalen and Oskar Isaksson, Gothenburg, June 2018

Contents

List of Figures

List of Tables

1
Introduction

1.1 Background

Formula Student (FS) is an international student engineering competition in which teams from different universities design, build and race small-scale formula style racing cars. Chalmers University of Technology (CTH) has been participating in the Electric Vehicle (EV) class of the FS competitions since 2015 with the team name Chalmers Formula Student (CFS). The rules governing the design of the electric propulsion systems in these cars allow a maximum battery voltage up to 600 V [1]. For the 2017 season, CFS constructed a lithium-ion battery with a maximum voltage of 580 V, which is considerably higher than some of the most sold electric cars (in 2016) [2], such as the Nissan Leaf, Tesla Model S and Chevrolet Bolt, which all have a maximum battery voltage of roughly 350 V to 400 V [3]–[5]. To charge the CFS battery, a charger capable of delivering the maximum battery voltage is required and therefore the commercially available ones appropriate for the above mentioned vehicles will not suffice.

Sales of EVs has increased notably over the past six years [6], surpassing two million units in global vehicle stock in 2016. The variation in their batteries are plentiful, there are different voltages, capacities, temperature ratings etc, and each associated charger has to adhere to the same ratings as the corresponding battery. Subsequently, the number of chargers installed worldwide has increased in a similar fashion, also surpassing two million units in 2016 [6]. Furthermore, the number of chargers available is also proclaimed as a key requirement for the continued growth of the global EV stock [6]. As the global EV stock is projected to grow to over 200 million units in 2030 [6], the number of chargers will also have to grow in a similar manner.

Silicon Carbide (SiC), first put to use as an abrasive in the 1890s, has in recent years become an interesting material for semiconductor applications [7]. Devices such as MOSFETs and Schottky diodes made with SiC show multiple advantages compared to traditional silicon semiconductors. SiC devices can withstand higher voltages and temperatures while also showing a lower resistance when conducting current [8]. These properties make them highly suitable for modern EV applications, where low mass, small size and high efficiency is important.

1.2 Aim

The aim of the project is to design a battery charger capable of charging a lithium-ion battery with a fully charged voltage of up to 600 V. The power output of the charger shall be in the range of 6 kW to 10 kW and the power electronics used in the charger shall be realised using SiC technology for active components.

1.3 Limitations

It will be assumed that the rectification of the supply voltage can be done using an already available diode bridge rectifier providing a fixed DC voltage to the charger. Such a rectifier will draw a non-sinusoidal current from the grid [9]. If this solution is used, it may cause the charger to violate certain regulations regarding harmonic currents, such as the Swedish standard SS-EN 61000-3-2 [10]. In this case the charger cannot be used in regular operation unless the rectifier is improved or replaced with one that fulfils the requirements.

The charger will be designed to operate with a 400 V 16 A three phase connection to the grid as this type of supply is commonly available at the sites used by CFS for testing the car, as well as being provided at competition sites [11]. Designing the charger for such a power supply would also allow the charger to be used for charging passenger vehicles in Swedish households, which are typically fused for 16 A or more [12], [13]. The theoretical maximum power output of this type of power supply assuming no losses and perfect power factor is just above 11 kW. This puts a physical limit of the charger output power, which will have to be lower than this value. The maximum charging power of the battery in question is at nominal battery voltage higher than 15 kW. The battery is therefore not a limiting factor when using a 400 V 16 A source.

1.4 Problem Specification

To charge a battery in a safe and effective way, the charger needs to be programmed to follow a certain program, known as a charging cycle. Charging cycles may be more or less complex depending on the type of battery that is to be charged. For common lithium-ion battery chemistries, such as the Lithium Cobalt Oxide (LiCoO2) chemistry used by CFS, the Constant Current-Constant Voltage (CC-CV) cycle can be used [14]. In the constant current stage, the charger regulates its output voltage to maintain a constant current flow into the battery. This current should not exceed the maximum input current that the battery can safely handle. Once the output voltage of the charger reaches a pre-programmed value, which should be no higher than the maximum allowed voltage for the battery, the charger will stop increasing the voltage and enter the constant voltage stage. In this stage the current naturally decays until it reaches a low value where the charging is considered complete and the charger shuts off.

The output voltage range of the charger will decide which batteries can be charged. The minimum voltage for a given battery can be calculated from the minimum voltage of an individual battery cell, multiplied by the number of cells connected in series. The aforementioned CFS battery with a maximum voltage of 580 V also has a minimum voltage of 414 V. The charger must be able to provide this lower voltage output in order to achieve proper current control. If the charger should be able to charge other batteries, the voltage range has to be adjusted accordingly.

When in operation, software control of the charger should allow the user to set the maximum output voltage and current to any value within these limits to accommodate different batteries. Furthermore, a control system needs to be active during charging, monitoring the voltage and current and making sure that the charging procedure is following the expected profile. If voltage and current limits are for some reason exceeded or if the battery is suddenly disconnected, the charger has to turn off and no residual voltage should remain on the charger output terminals. For safety reasons it is important that sufficient galvanic insulation is present between the battery and the grid side of the charger [15]. How to achieve this will have to be considered when selecting the converter topology.

Finally, in order to turn the charger into a usable product, some thought has to be put into the packaging and housing of the charger hardware. Suitable input and output connectors need to be added in order to connect to the grid and the battery. A cooling system that can provide sufficient cooling for all components also needs to be included in the finished product. The charger's size and weight also have to be considered, as the charging procedure during FS competitions is determined by the rules and does put some requirements on practicality [1]. For charging during competitions, all batteries have to be removed from the vehicle and taken to a specified charging station on a hand cart. This hand cart needs to be of such size as to allow a person to push it, and may not be motorised. Therefore it is common practice by teams to fit their charger to this battery hand cart or have it on a separate hand

cart of a similar size. The charger should accordingly be designed to fit on a cart and be able to be propelled by hand.

The problem specification can be summarised with Figure 1.1. The charger needs the functions mentioned above, featured from the left in the figure: the 400 V grid, a rectifying stage to supply a DC-voltage to one or several high frequency converter/s. A transformer for galvanic isolation between the battery and the grid, followed by another block of converter/s to supply the battery with the DC voltage it requires. The charger is packaged in a housing which needs to house all the aforementioned parts and facilitate cooling possibilities for those. A controller block housing the software control supervising the converter blocks during the charging cycle is also needed, using the *ctrl-signals*. It will also need measuring points, such as the rectified input voltage $U_{DC-IN} + -U_{DC-IN}-$, the battery voltage $U_{Bat} + -U_{Bat}-$ and the charging current I_{Bat}. The controller block also needs to be able to communicate with the outside world, such as an external computer, to be able to accommodate reprogramming for different charging cycles.

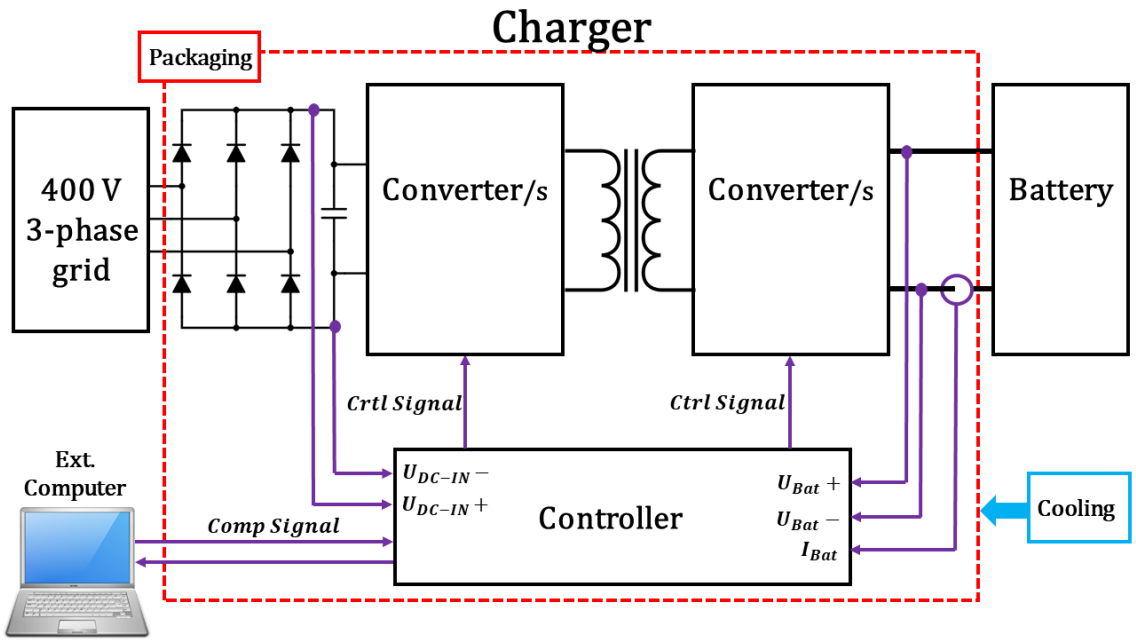


Figure 1.1: Block schematic of generalised charger with its assumed needed parts.

2

Methodology and Design Specifications

This chapter covers the methodology with the necessary steps needed to complete the project. It also includes a specification of what the finished charger needs to be capable of in terms of performance and functionality.

2.1 Overview

In order to design a battery charger according to Section 1.2 fulfilling the performance criteria in Section 1.4, several steps need to be taken before the actual design of the converter can commence. The minimum requirements from Section 1.4 will be used to decide on the final design specifications, which may be better than the minimum requirements in some cases.

A literature study will be performed on different topologies to be used for the main power electronic circuit, in order to find out which ones that are the most suitable for this application. Advantages and drawbacks of different designs as described in the literature will be taken into consideration, such as flexibility of voltage and current ranges and overall complexity of the circuit. Hand calculations of the switching operations will be performed to determine certain key properties such as peak and RMS voltages and currents to see if the topology can be realised using real components. Based on the results of this initial study, a few of these topologies will be selected as the most promising. Topologies that are excessively complex or cannot fulfil the requirements for output voltage and current will be removed from the selection.

Simulation models of the required circuitry will be built based on selected topologies to verify that the circuits work as intended. Here the literature study and results from hand calculations are important in order to gather all required data for realistic simulations. Models of real components will be added to the simulation where possible, to see how they affect circuit behaviour and to estimate the efficiency by taking component losses into account. This selection of components will be preliminary and can be optimised after the topology is decided on. For the final selection, the topology with the highest efficiency will be preferred.

After locking down the topology, all passive and active components will be selected. As one of the stated goals of the project is to evaluate the performance of SiC devices, such devices should be selected whenever possible. The maximum voltage and current ratings should be well above the expected voltages and currents in the circuit, and switching performance and on-state resistance should be selected such as to achieve the goal of maximum efficiency.
Driver circuits should be selected to match the switches. Passive components should also be selected to be sufficiently robust against overvoltage and overcurrent. Some magnetic components might have to be designed and manufactured rather than purchased, such as the isolating transformer and inductors used for filtering. In this case, core material, wire type and winding configuration has to be considered in order to achieve all desired properties.

2.2 Design specifications

2.2.1 Output voltage range

To provide some control margin and to round off the numbers, the output voltage range from Section 1.4 is extended to a range from 400 V to 600 V. Higher voltages will not be considered useful as it would not be allowed in an FS setting. Lower voltages will be considered a bonus feature to be implemented if it does not increase the cost and complexity of the charger.

2.2.2 Output current and power

Another important property to consider for a charger is the maximum current output. As previously mentioned, it is of no use to design a charger with a current output higher than the maximum allowed charging current for the corresponding batteries. The CFS battery is constructed with two cells in parallel, and a maximum continuous charging current of 15 A per cell for a total charging current of 30 A. Sizing the charger for such a current output would result in a maximum power of

$$600\,\mathrm{V} * 30\,\mathrm{A} = 18\,\mathrm{kW} \tag{2.1}$$

However for high-power applications, the power output from the grid is often a limiting factor. The required 16 A connection can only provide up to

$$\sqrt{3} * 400\,\mathrm{V} * 16\,\mathrm{A} = 11\,\mathrm{kW} \tag{2.2}$$

and considering the less than ideal power factor and efficiency present in real applications, the actual output power will be lower than this number. In a Formula Student testing and competition setting, it might also be desirable to connect side loads such as laptop computers and low voltage battery chargers to the same grid connection. In this case the output power has to be further reduced to avoid overloading the outlet.

A good starting point might be to set the charging power to half the maximum value calculated in (2.1), or 9 kW. This would allow for a charging current of 15 A at maximum output voltage. However, if the charger is dimensioned for a higher output current than this, the full charging power can be maintained over a range of voltages. For example, with a 20 A output, maximum power output is achieved at a voltage of

$$\frac{9\,\mathrm{kW}}{20\,\mathrm{A}} = 450\,\mathrm{V} \tag{2.3}$$

and above, which would improve charging speed at the cost of higher component current ratings. Rating the charger for 9 kW results in a maximum grid current consumption of

$$\frac{9\,\mathrm{kW}}{\sqrt{3} * 400\,\mathrm{V}} = 13\,\mathrm{A} \tag{2.4}$$

for an ideal charger, leaving 3 A per phase to be used for side loads, converter losses and possible reactive power consumption of the rectifier. For these reasons, the charger will be designed for a maximum output power of 9 kW and a maximum current of 20 A.

3
Power Converters Theory

This chapter gives a theoretical introduction to the different power circuits that are evaluated in the project, including equations supporting the design of the converters.

3.1 Basic battery charger layout

Dependent on the rated limits of the charger and battery, the DC/DC output voltage will be a few volts higher than the present battery voltage and the energy will therefore flow from the grid into the battery. As the charge accumulates in the battery, its voltage will rise and to keep up with the same rate of charge, the output voltage of the charger will have to rise accordingly. The charging will stop when the battery voltage equals the maximum rated battery voltage or maximum output voltage of the charger. A well designed charger will control these aspects of the charging cycle and have systems to detect failures, such as overcurrent or overvoltage, and interrupt the charging cycle in a safe manner. To make an efficient charger, the power converter(s) used must be able to operate at high efficiency at a range of output voltages and currents.

3.2 Hard switching DC/DC converter types

In this section, the background theory of the relevant hard switching DC/DC converters is described with ideal components. The converters are assumed to be operating in Continuous-Conduction Mode (CCM), i.e. that there is always a positive current flowing through the primary inductor of the circuit, i.e $i_L(t) > 0$. This mode is chosen as it generally yields a higher efficiency and lower component stress [16], [17] on the switch in comparison to the Discontinuous-Conduction Mode (DCM). DCM does in turn have advantages in a higher loop bandwidth [17], which is preferable when trying out more advanced control strategies. This is however not one of the primary research topics of this report. It is also assumed that the output voltage of the converters can be approximated to be constant. This can be achieved by using a sufficiently large output capacitor. This simplification is favourable as it enables simple comparisons between input and output voltages as they will be DC. In this report, values presented with lowercase letters (e.g v_{out}, i_L) are instantaneous values while uppercase letters (e.g V_{out}, I_L) are average values. Furthermore, as ideal components are assumed, the input power P_{in} is assumed to be equal to the output power P_{out}, which gives $V_{IN} * I_{IN} = V_{OUT} * I_{OUT}$.

Where applicable, the circuits are controlled by Pulse Width Modulation (PWM) which means that the part of the switching period where the main switch is closed is varied. This is shown in Figure 3.1 where two switching periods are shown. The part of the switching period, T, when the switch is on is DT and D is the duty cycle. As will be shown later, the ratio between input and output voltage will be controlled by the duty cycle.

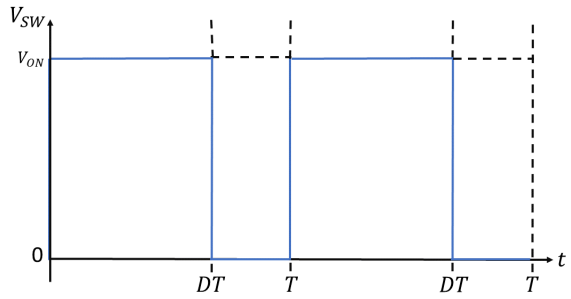


Figure 3.1: Plot of PWM switch signal for hard switched converters.

To facilitate background information for component selection and performance assessment of each converter topology, these main attributes are focused on in each converter:

• **Input/Output voltage relation:** A key relation for any DC/DC converter, the relation between the input voltage and the output voltage and how it is controlled.

• **Main waveforms for inductor, diode and switch** To see how the peaks and valleys are formed during a switching period is of high interest for understanding the function of the converters.

• **Inductance for CCM operation:** As the primary inductors directly effect which mode the converters will operate in, their dynamics are needed to ensure CCM operation.

•$\mathbf{I_{avg}}$ **and** $\mathbf{i_{RMS}}$ **for inductor, switch diode and capacitor:** The average and RMS currents are both used for matching component ratings and loss calculations.

•$\mathbf{i_{peak}}$ **for inductor, switch, diode and capacitor:** To match component ratings against the highest currents that will occur in each converter.

•$\mathbf{v_{max}}$ **for inductor, switch, diode and capacitor:** To match component ratings against the highest voltages that will occur in each converter.

3.2.1 Buck Converter (Step-down)

A buck converter is a non-inverting topology which outputs a lower voltage than its input. A simple version of the circuit can be seen in Figure 3.2. The output current will be continuous, as it is not directly connected to any switch. However, it will draw a discontinuous current from its source [18].

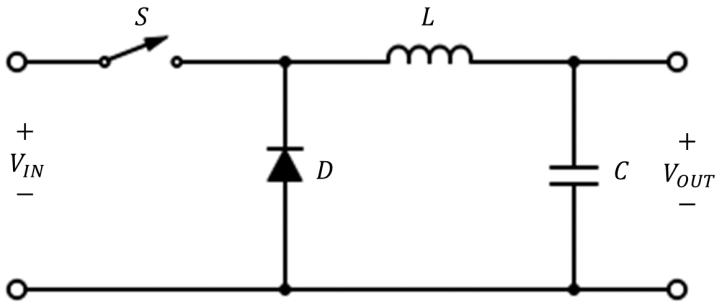


Figure 3.2: Basic circuit of a buck converter.

At steady-state CCM operation, during the on period of the switch $(0 - DT)$, the voltage over the inductor is $v_L = V_{IN} - V_{OUT}$, see Figure 3.6 for plot of inductor voltage. As this voltage is always positive, it reverse-biases the diode into blocking, see Figure 3.7 for plot of diode voltage, and all of the current flows towards the output providing output current, charging the primary inductor and charging the output capacitor, see Figure 3.3 for circuit, Figure 3.5 for plot of inductor current and Figure 3.8 for plot of capacitor current. When the switch opens, i.e the off period $(DT - T)$, the voltage across the inductor is reversed to $v_L = -V_{out}$ which then forward biases the diode which creates a way for the inductor current to continue to flow to the output, see Figure 3.4 for circuit. The output capacitor also provide current to balance the decaying inductor current. With CCM operation, the input/output ratio can be found with the average inductor voltage V_L, which should add up to zero over one period [18],

$$\begin{aligned} V_L = \frac{1}{T}\int_0^T v_L dt = \frac{1}{T}\int_0^{DT} v_L dt + \frac{1}{T}\int_{DT}^T v_L dt = 0 \Rightarrow \\ \frac{1}{T}(V_{IN} - V_{OUT})DT + \frac{1}{T}(-V_{OUT}(1-D)T) = 0 \Rightarrow \\ \frac{V_{OUT}}{V_{IN}} = D. \end{aligned} \tag{3.1}$$

As D can be varied between 0 and 1, V_{out} can be varied as

$$V_{OUT} = [0 \ \rightarrow \ V_{IN}]. \tag{3.2}$$

To simplify explanations, Δi_L is introduced, which is the peak-to-peak value of the inductor current. It is expressed using the constitutive equation of an inductor, applying the conditions during the charging part of the switching period and (3.1). Note that f_{sw} is the switching frequency of the switch.

$$v_L = L\frac{di_L}{dt} \Rightarrow di_L = \frac{v_L dt}{L} \Rightarrow \begin{bmatrix} dt = DT \\ v_L = V_{IN} - V_{OUT} \\ di_L = \Delta i_L \end{bmatrix} \Rightarrow \Delta i_L = \frac{(V_{IN} - V_{OUT})DT}{L} \Rightarrow$$
$$\Delta i_L = \frac{(V_{IN} - V_{OUT})D}{Lf_{sw}} \Rightarrow \Delta i_L = \frac{V_{OUT}(1 - \frac{V_{OUT}}{V_{IN}})}{Lf_{sw}}. \tag{3.3}$$

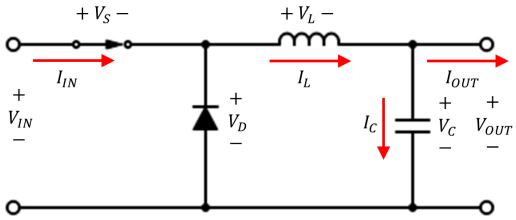


Figure 3.3: Buck converter circuit with currents while switch is closed during CCM operation.

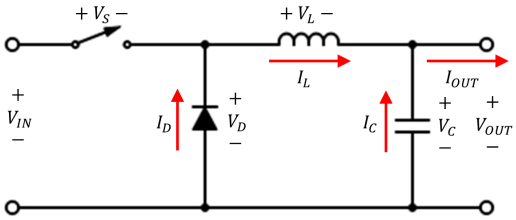


Figure 3.4: Buck converter circuit with currents while switch is open during CCM operation.

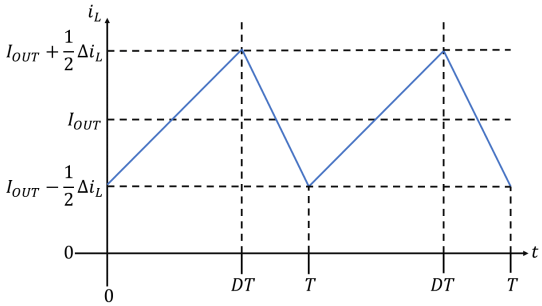


Figure 3.5: Plot of inductor current i_L during CCM operation for a buck converter.

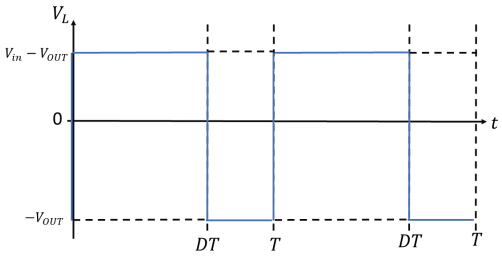


Figure 3.6: Plot of inductor voltage v_L during CCM operation for a buck converter.

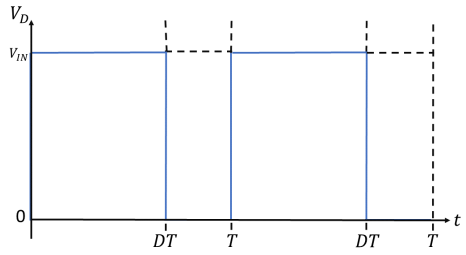


Figure 3.7: Plot of diode votlage v_D during CCM operation for a buck converter.

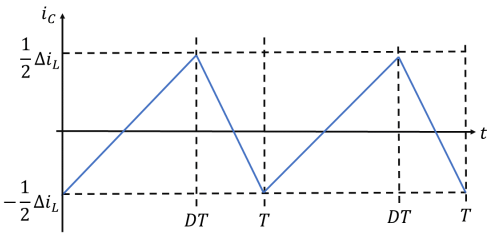


Figure 3.8: Plot of output capacitor current i_C during CCM operation for a buck converter.

As mentioned above, to operate in CCM, a current larger than zero must always flow through the inductor. Therefore one can define the CCM boundary with the inductor peak-to-peak current from (3.3). As long as the average inductor current is larger than half of the peak-to-peak current, the converter will operate in CCM. As the inductor is directly connected to the output in the buck converter, they must have the same average value: $I_L = I_{OUT}$. With this relation, the peak-to-peak expression (3.3) can be reworked to give the smallest inductance value needed to ensure CCM:

$$\begin{gathered}\Delta i_L = \frac{V_{OUT}(1-\frac{V_{OUT}}{V_{IN}})}{Lf_{sw}} \Rightarrow L = \frac{V_{OUT}(1-\frac{V_{OUT}}{V_{IN}})}{\Delta i_L f_{sw}} \Rightarrow \\ \begin{bmatrix} I_L \geq \frac{1}{2}\Delta i_L \\ I_L = I_{OUT} \end{bmatrix} \Rightarrow L \geq \frac{V_{OUT}(1-\frac{V_{OUT}}{V_{IN}})}{2I_{OUT}f_{SW}}.\end{gathered} \tag{3.4}$$

To find values for dimensioning components for a buck converter, follow Table 3.1 and use (3.1), (3.3) and (3.4), to calculate the needed ratings for each converter component. The expressions are either given by definition, such as I_C and I_L, by the waveforms from the buck operation, such as i_{Lmax}, i_{Smax}, i_{Dmax} and i_{Cmax}, converting the triangular waveforms to find the appropriate average- and RMS-values, such as i_{Lrms}, i_{Srms}, i_{Drms}, I_S and I_D or finding an appropriate expression from sources, such as i_{Crms} from [19]. For the voltage limits, the maximum voltage is the highest one available in the circuit, i.e V_{IN}.

Table 3.1: Usable values for the Buck converter

Comp \ Value	$\mathbf{i_{max}}$	$\mathbf{i_{rms}}$	$\mathbf{I_{avg}}$	$\mathbf{v_{max}}$
Inductor	$I_{OUT} + \frac{1}{2}\Delta i_L$	$I_{OUT}\sqrt{1 + \frac{1}{12}(\frac{\Delta i_L}{I_{OUT}})^2}$	I_{OUT}	V_{IN}
Switch	$I_{OUT} + \frac{1}{2}\Delta i_L$	$\sqrt{\frac{V_{OUT}}{V_{IN}}(I_{OUT}^2 + \frac{1}{12}\Delta i_L^2)}$	I_{IN}	V_{IN}
Diode	$I_{OUT} + \frac{1}{2}\Delta i_L$	$\sqrt{(1 - \frac{V_{OUT}}{V_{IN}})(I_{OUT}^2 + \frac{1}{12}\Delta i_L^2)}$	$I_{OUT} - I_{IN}$	V_{IN}
Capacitor	$\frac{1}{2}\Delta i_L$	$\frac{1}{\sqrt{12}}\Delta i_L$	0	V_{IN}

3.2.2 Boost Converter (Step-up)

A boost converter is a non-inverting topology which outputs a higher voltage than its input. A simple circuit can be seen in Figure 3.9. The input current drawn from the source is continuous but the output current will be pulsating [18].

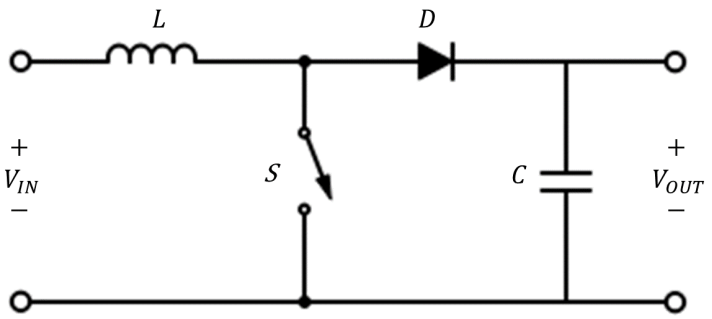


Figure 3.9: Basic circuit of a boost converter.

At steady-state CCM operation, during the on period of the switch $(0 - DT)$, the voltage across the inductor is $v_L = V_{in}$ and it is subsequently charged, see Figure 3.10 for circuit, Figure 3.13 for plot of inductor voltage and Figure 3.12 for plot of inductor current. As the the diode is reversed-biased (as $V_{IN} < V_{OUT}$), it blocks any current from flowing from the input to the output, see Figure 3.14 for plot of diode voltage and all of the output current is supplied by the output capacitor C, see Figure 3.15 for plot of capacitor current. During the off period $(DT - T)$, the input, aided by the discharging inductor, supplies the output current and charges the

output capacitor, see Figure 3.11 for circuit. With CCM operation, the input/output ratio can be found with the average inductor voltage which should add up to zero over one period [18],

$$\begin{aligned} V_L = \frac{1}{T}\int_0^T v_L dt = \frac{1}{T}\int_0^{DT} v_L dt + \frac{1}{T}\int_{DT}^T v_L dt = 0 \Rightarrow \\ \frac{1}{T}V_{IN}DT + \frac{1}{T}(V_{IN} - V_{OUT})(1-D)T = 0 \Rightarrow \\ \frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D} \Longleftrightarrow D = 1 - \frac{V_{IN}}{V_{OUT}}. \end{aligned} \tag{3.5}$$

Worth noting is that theoretically, the boost converter would be able to output an infinite output voltage as the duty cycle increases towards 1, $D \to 1 \Rightarrow V_{out} \to \infty$. However, due to losses in components, the actual voltage gain will taper off, stop and then drop off back towards 0 if D continues to increases beyond a certain point [18]. A simplified model from Texas Instruments [20] gives this equation for approximating this point D_{max}, the duty cycle which will give the highest boost, as

$$D_{max} \cong \frac{V_{IN} - I_{OUT}(R_S + R_D + 2R_L)}{V_{IN} + I_{OUT}(R_S - R_D)}. \tag{3.6}$$

This relation is dependent on the parasitic elements of the components modelled as resistors, the switch (R_S), diode (R_D) and inductor (R_L). With D being varied between 0 and D_{max}, V_{out} can varied as

$$V_{out} = [V_{IN} \ \to \ \frac{V_{IN}}{1 - D_{max}}]. \tag{3.7}$$

As for the buck converter, Δi_L is introduced to simplify expressions. Δi_L is the peak-to-peak value of the current through the inductor. It is expressed using the constitutive equation of an inductor and applying the charging part of the period $(0 - DT)$. Note that f_{sw} is the switching frequency of the switch,

$$\begin{aligned} v_L = L\frac{di_L}{dt} \Rightarrow di_L = \frac{v_L dt}{L} \Rightarrow \begin{bmatrix} dt = DT \\ v_L = V_{IN} \\ di_L = \Delta i_L \end{bmatrix} \Rightarrow \Delta i_L = \frac{V_{IN}DT}{L} \Rightarrow \Delta i_L = \frac{V_{IN}D}{Lf_{sw}} \Rightarrow \\ \Delta i_L = \frac{V_{IN}(1 - \frac{V_{IN}}{V_{OUT}})}{Lf_{sw}}. \end{aligned} \tag{3.8}$$

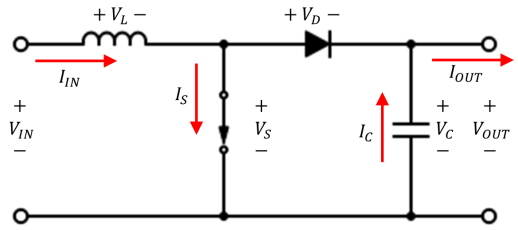


Figure 3.10: Boost converter circuit with currents while switch is closed during CCM operation.

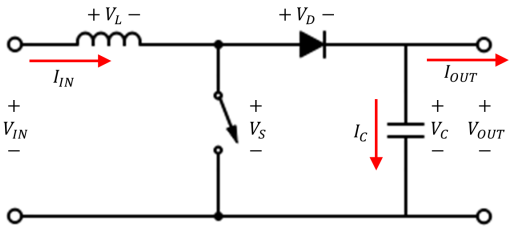


Figure 3.11: Boost converter circuit with currents while switch is open during CCM operation.

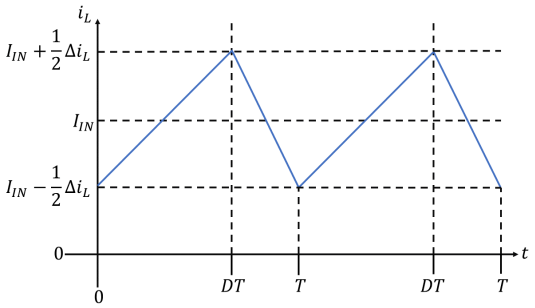


Figure 3.12: Plot of inductor current i_L during CCM operation for a boost converter.

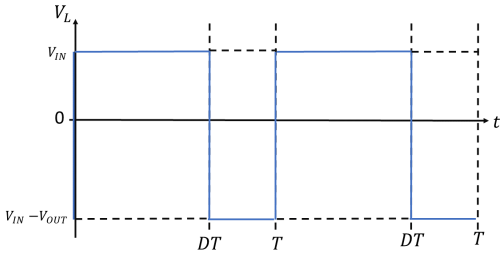


Figure 3.13: Plot of inductor voltage v_L during CCM operation for a boost converter.

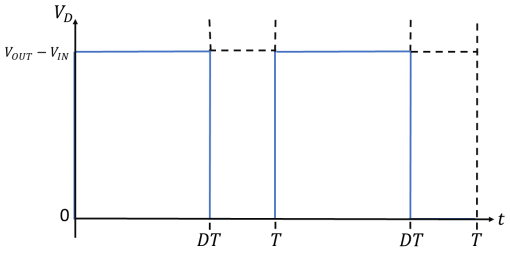


Figure 3.14: Plot of diode voltage v_D during CCM operation for a boost converter.

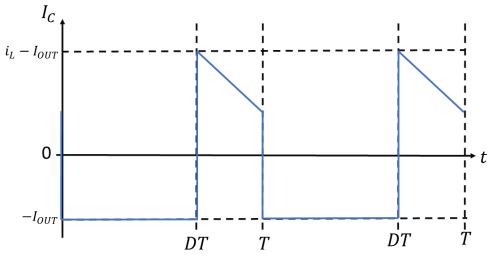


Figure 3.15: Plot of output capacitor current i_C during CCM operation for a boost converter.

As for the buck converter, to operate in CCM, a current larger than zero must always flow through the inductor. Therefore one can define the CCM boundary with the inductor peak-to-peak current from (3.8). As long as the average inductor current is larger than half of the peak-to-peak current, the converter will operate in CCM. As the inductor is directly connected to the input in the boost converter, they must have the same average value: $I_L = I_{IN}$. With this relation, the peak-to-peak expression (3.8) can be reworked to give the smallest inductance value needed to ensure CCM:

$$\Delta i_L = \frac{V_{IN}(1-\frac{V_{IN}}{V_{OUT}})}{Lf_{sw}} \Rightarrow L = \frac{V_{IN}(1-\frac{V_{IN}}{V_{OUT}})}{\Delta i_L f_{sw}} \Rightarrow \begin{bmatrix} I_L \geq \frac{1}{2}\Delta i_L \\ I_L = I_{IN} \end{bmatrix} \Rightarrow L \geq \frac{V_{IN}(1-\frac{V_{IN}}{V_{OUT}})}{2I_{IN}f_{SW}}. \tag{3.9}$$

To find values for dimensioning components for a boost converter, follow Table 3.2 and use (3.5), (3.8) and (3.9) to calculate the needed ratings for each converter component. The expressions are either given by definition, such as I_C and I_L, by the waveforms from the boost operation, such as i_{Lmax}, i_{Smax}, i_{Dmax} and i_{Cmax}, converting the triangular waveforms to find the appropriate average- and RMS-values, such as i_{Lrms}, i_{Srms}, i_{Drms}, I_S and I_D, or finding an appropriate expression from sources, such as i_{Crms} from [19]. For the voltage limits, the maximum voltage is the highest one available in the circuit, i.e V_{OUT}.

Table 3.2: Usable values for the Boost converter

Comp \ Value	$\mathbf{i_{max}}$	$\mathbf{i_{rms}}$	$\mathbf{I_{avg}}$	$\mathbf{v_{max}}$
Inductor	$I_{IN}+\frac{1}{2}\Delta i_L$	$I_{IN}\sqrt{1+\frac{1}{12}(\frac{\Delta i_L}{I_{IN}})^2}$	I_{IN}	V_{OUT}
Switch	$I_{IN}+\frac{1}{2}\Delta i_L$	$\sqrt{(1-\frac{V_{IN}}{V_{OUT}})(I_{IN}^2+\frac{1}{12}\Delta i_L^2)}$	$I_{IN}-I_{OUT}$	V_{OUT}
Diode	$I_{IN}+\frac{1}{2}\Delta i_L$	$\sqrt{\frac{V_{IN}}{V_{OUT}}(I_{IN}^2+\frac{1}{12}\Delta i_L^2)}$	I_{OUT}	V_{OUT}
Capacitor	$\frac{1}{2}\Delta i_L+I_{IN}-I_{OUT}$	$\sqrt{(I_{OUT}(1-\frac{V_{IN}}{V_{OUT}})\sqrt{\frac{V_{OUT}}{V_{IN}}})^2+(I_{OUT}\sqrt{\frac{V_{IN}}{V_{OUT}}})^2}$	0	V_{OUT}

3.2.3 SEPIC

SEPIC stands for Single Ended Primary Inductor Converter. It is a non-inverting topology that can output a voltage that is both above and below its input voltage, as it is essentially a boost converter followed by a buck-boost converter. A simple circuit can be seen in Figure 3.16. The input current is continuous but the output current will be pulsating [21].

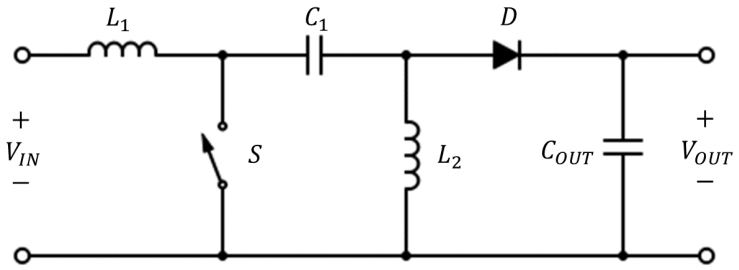


Figure 3.16: Basic circuit of a SEPIC.

At steady-state CCM operation, during the on time of the switch $(0 - DT)$, inductor L_1 is charged by the input, as the switch short circuits it to ground, making $v_{L1} = V_{IN}$. The coupling capacitor C_1 has been charged in the previous off cycle and holds its voltage over the inductor L_2, making $v_{L2} = -v_{c1}$, see Figure 3.17 for circuit, Figures 3.23 and 3.22 for plots of voltages over the inductors, Figures 3.19, 3.20 and 3.24 for plots of currents through the inductors and switch. During this time, all of the output current is supplied by the output capacitor C_{OUT}, see Figure 3.26 for plot of capacitor current. When the switch opens $(DT - T)$, inductor L_1 is connected to the rest of the circuit and the voltage over it becomes $v_{L1} = V_{IN} - V_{C1} - V_{OUT}$. The voltage over L_2 rises to V_{OUT} and the diode starts conducting. At that point both inductors will discharge together with the input to provide output current and charging current for the coupling capacitor C_1 and the output capacitor C_{OUT}, see Figures 3.25 and 3.27 for plots of currents through the coupling capacitor and diode. As the SEPIC has two inductors, CCM operating condition must hold for both inductors. As for the other converters, the average voltage over the inductors must add up to 0 over one period at steady state,

•V_{L1}

$$\begin{aligned} V_{L1} = \frac{1}{T}\int_0^T v_{L1}dt = \frac{1}{T}\int_0^{DT} v_{L1}dt + \frac{1}{T}\int_{DT}^T v_{L1}dt = 0 \Rightarrow \\ \frac{1}{T}V_{IN}DT + \frac{1}{T}((V_{IN} - V_{C1} - V_{OUT})(1-D)T) = 0 \Rightarrow \\ V_{OUT} = \frac{V_{C1}(1-D) - V_{IN}}{D-1} \iff \\ V_{IN} = (1-D)(V_{OUT} + V_{C1}) \iff \\ V_{C1} = \frac{V_{OUT}(1-D) - V_{IN}}{D-1}, \end{aligned} \tag{3.10}$$

•V_{L2}

$$\begin{aligned} V_{L2} = \frac{1}{T}\int_0^T v_{L2}dt = \frac{1}{T}\int_0^{DT} v_{L2}dt + \frac{1}{T}\int_{DT}^T v_{L2}dt = 0 \Rightarrow \\ \frac{1}{T}(-V_{C1}DT) + \frac{1}{T}(V_{OUT}(1-D)T) = 0 \Rightarrow \\ V_{OUT} = \frac{V_{C1}D}{1-D} \Longleftrightarrow V_{C1} = \frac{V_{OUT}(1-D)}{D}. \end{aligned} \tag{3.11}$$

As both expression are dependent on the voltage over the coupling capacitor V_{C1}, one of the expressions is substituted into the other to solve for the the voltage input/output relation,

$$\begin{aligned} \frac{V_{OUT}(1-D) - V_{IN}}{D-1} = \frac{V_{OUT}(1-D)}{D} \Rightarrow \\ V_{OUT}D - V_{OUT} = -V_{IN}D \Rightarrow \frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D} \Longleftrightarrow D = \frac{V_{OUT}}{V_{IN}+V_{OUT}}. \end{aligned} \tag{3.12}$$

Similar to the boost converter, the SEPIC can theoretically output an infinite voltage as D increases towards 1, $D \to 1 \Rightarrow V_{out} \to \infty$. But as for the boost, it will also hit a maximum voltage gain depending on the losses of the used components. With D being varied between 0 and D_{max}, V_{out} can varied as

$$V_{OUT} = [0 \ \rightarrow \ \frac{D_{max}V_{IN}}{1-D_{max}}]. \tag{3.13}$$

As for the buck and boost converter, Δi_L is introduced to simplify expressions. Δi_L is the peak-to-peak value of the current through each inductor. It is expressed using the constitutive equation of an inductor and applying the charging part of the period. Note that f_{sw} is the switching frequency of the switch:

•Δi_{L1}

$$\begin{aligned} v_{L1} = L_1\frac{di_{L1}}{dt} \Rightarrow di_{L1} = \frac{v_{L1}dt}{L_1} \Rightarrow \begin{bmatrix} dt = DT \\ v_{L1} = V_{IN} \\ di_{L1} = \Delta i_{L1} \end{bmatrix} \Rightarrow \Delta i_{L1} = \frac{V_{IN}DT}{L_1} \Rightarrow \\ \Delta i_{L1} = \frac{V_{IN}D}{L_1 f_{sw}} \Rightarrow \Delta i_{L1} = \frac{V_{IN}V_{OUT}}{f_{sw}L_1(V_{OUT}+V_{IN})}, \end{aligned} \tag{3.14}$$

•Δi_{L2}

$$\begin{aligned} v_{L2} = L_2\frac{di_{L2}}{dt} \Rightarrow di_{L2} = \frac{v_{L2}dt}{L_2} \Rightarrow \begin{bmatrix} dt = DT \\ v_{L2} = |-V_{C1}| \\ di_{L2} = \Delta i_{L2} \end{bmatrix} \Rightarrow \Delta i_{L2} = \frac{V_{C1}DT}{L_2} \Rightarrow \\ \Delta i_{L2} = \frac{V_{C1}D}{L_2 f_{sw}} = \frac{V_{OUT}(1-D)}{L_2 f_{sw}} \Rightarrow \Delta i_{L2} = \frac{V_{IN}V_{OUT}}{f_{sw}L_2(V_{OUT}+V_{IN})}. \end{aligned} \tag{3.15}$$

As the SEPIC has one more capacitor than the other converter topologies mentioned, the coupling capacitor C_1, the steady state operating conditions of it can be used to find other identities in the circuit. The steady state operation condition for the capacitor is that the average current through it adds up to 0 over one period [18], i.e $I_{C1} = 0$. As mentioned above, during the on-time of the switch $(0 - DT)$, the current through C_1 is flowing from L_2 down to ground via S. During the off time $(DT - T)$, the current flows from L_1, through C_1 and towards the output. With this information, the average current of flowing through L_2, I_{L2}, can be expressed as

$$\begin{gathered} I_{C1} = \frac{1}{T}\int_0^T i_{C1}dt = \frac{1}{T}\int_0^{DT} i_{C1}dt + \frac{1}{T}\int_{DT}^T i_{C1}dt = 0 \Rightarrow \\ \frac{1}{T}(-I_{L2})DT + \frac{1}{T}(I_{L1})(1-D)T = 0 \Rightarrow I_{L2}D = I_{L1}(1-D). \Rightarrow \\ I_{L2} = \frac{1-D}{D}I_{L1} \end{gathered} \tag{3.16}$$

As L_1 is directly connected to the input in the SEPIC, they must have the same average value: $I_{L1} = I_{IN}$. Using this, the inverse of (3.12) and $P_{IN} = P_{OUT}$, the expression for I_{L2} can be expressed as

$$\begin{gathered} I_{L2} = \frac{1-D}{D}I_{L1} \Rightarrow \begin{bmatrix} I_{L1} = I_{IN} \\ I_{IN} = \frac{V_{OUT}I_{OUT}}{V_{IN}} \\ \frac{V_{IN}}{V_{OUT}} = \frac{1-D}{D} \end{bmatrix} \Rightarrow \\ I_{L2} = \frac{V_{IN}}{V_{OUT}} * \frac{V_{OUT}I_{OUT}}{V_{IN}} = I_{OUT}. \end{gathered} \tag{3.17}$$

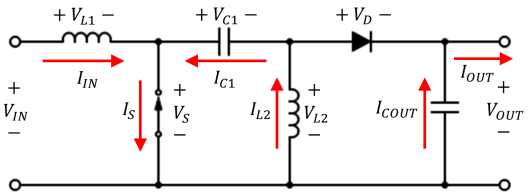


Figure 3.17: SEPIC circuit with currents while switch is closed during CCM operation.

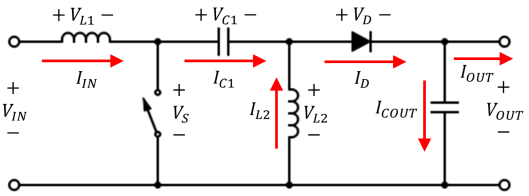


Figure 3.18: SEPIC circuit with currents while switch is open during CCM operation

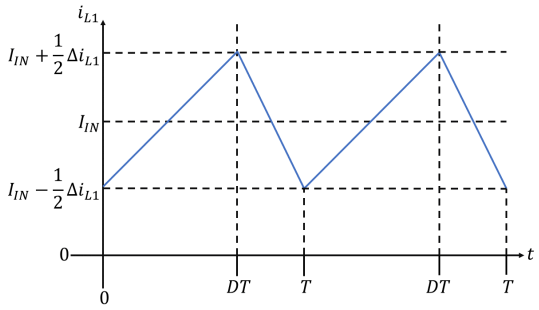


Figure 3.19: Plot of inductor current I_{L1} during CCM operation for a SEPIC.

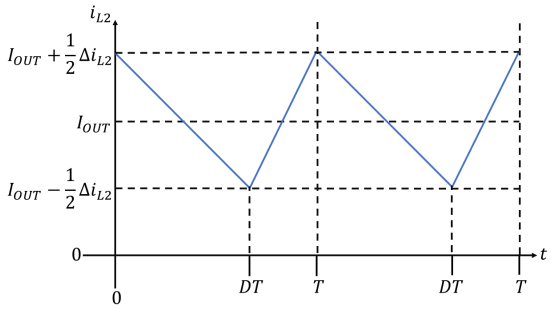


Figure 3.20: Plot of inductor current I_{L2} during CCM operation for a SEPIC.

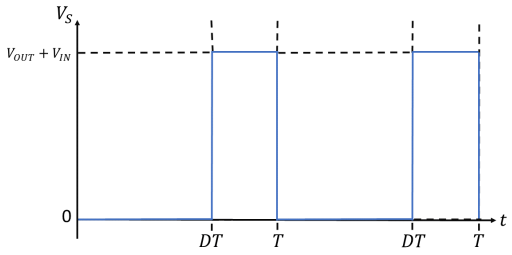


Figure 3.21: Plot of diode voltage v_D during CCM operation for a SEPIC.

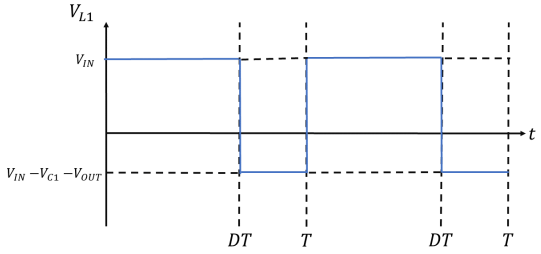


Figure 3.22: Plot of inductor voltage v_{L1} during CCM operation for a SEPIC.

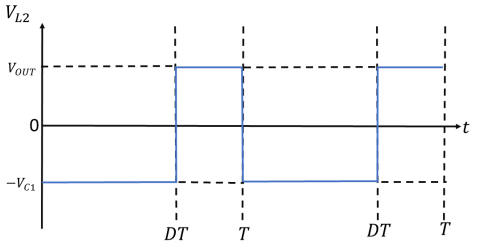


Figure 3.23: Plot of inductor voltage v_{L2} during CCM operation for a SEPIC.

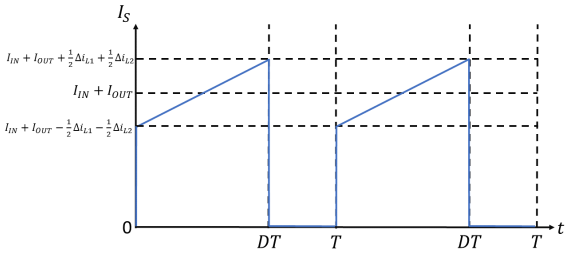


Figure 3.24: Plot of switch current i_S during CCM operation for a SEPIC.

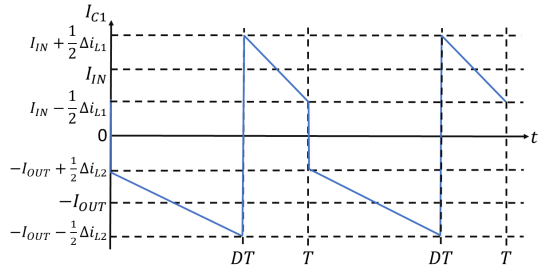


Figure 3.25: Plot of coupling capacitor current i_{C1} during CCM operation for a SEPIC.

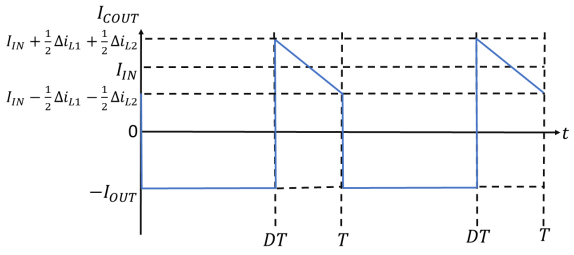


Figure 3.26: Plot of output capacitor current i_{COUT} during CCM operation for a SEPIC.

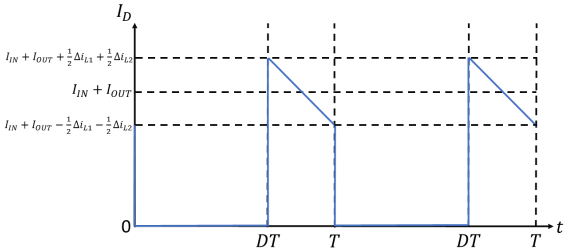


Figure 3.27: Plot of diode current i_D during CCM operation for a SEPIC.

As for the buck and boost converter, to operate in CCM, a current larger than zero must always flow through the inductors. Therefore one can define the CCM boundary with the inductors peak-to-peak current from (3.14) and (3.15). As long as the average inductor current is larger than half of the peak-to-peak current, the converter will operate in CCM. As mentioned above, $I_{L1} = I_{IN}$. With this relation, the peak-to-peak expression can be reworked to give the smallest inductance value needed to ensure CCM for L_1:

$$\begin{aligned} \Delta i_{L1} = \frac{V_{IN}V_{OUT}}{f_{sw}L_1(V_{OUT}+V_{IN})} \Rightarrow L_1 = \frac{V_{IN}V_{OUT}}{f_{sw}\Delta i_{L1}(V_{OUT}+V_{IN})} \Rightarrow \\ \begin{bmatrix} I_{L1} \geq \frac{1}{2}\Delta i_{L1} \\ I_{L1} = I_{IN} \end{bmatrix} \Rightarrow L_1 \geq \frac{V_{IN}V_{OUT}}{2f_{SW}(I_{IN}V_{OUT}+P_{IN})}. \end{aligned} \tag{3.18}$$

As mentioned in (3.17), $I_{L2} = I_{OUT}$. With this relation, the peak-to-peak expression can be reworked to give the smallest inductance value needed to ensure CCM for L_2:

$$\begin{aligned} \Delta i_{L2} = \frac{V_{IN}V_{OUT}}{f_{sw}L_2(V_{OUT}+V_{IN})} \Rightarrow L_2 = \frac{V_{IN}V_{OUT}}{f_{sw}\Delta i_{L2}(V_{OUT}+V_{IN})} \Rightarrow \\ \begin{bmatrix} I_{L2} \geq \frac{1}{2}\Delta i_{L2} \\ I_{L2} = I_{OUT} \end{bmatrix} \Rightarrow L_2 \geq \frac{V_{IN}V_{OUT}}{2f_{SW}(I_{OUT}V_{IN}+P_{OUT})}. \end{aligned} \tag{3.19}$$

To find values for dimensioning components for a SEPIC, follow Table 3.3 and use (3.10), (3.11), (3.14), (3.15), (3.18) and (3.19) to calculate the needed ratings for each converter component. The expressions are either given by definition, such as I_{L1}, I_{L2}, I_{C1}, I_{COUT}, v_{COUT}, by the waveforms from the SEPIC operation, such as i_{L1max}, i_{L2max}, i_{Smax}, i_{Dmax}, i_{C1max}, $i_{COUTmax}$, v_{L1max}, v_{L2max}, converting the triangular waveforms to find the appropriate average- and RMS-values, such as i_{L1rms}, i_{L2rms}, or finding an appropriate expression from sources [21] and [22], such as i_{Srms}, i_{Drms}, i_{C1rms}, $i_{COUTrms}$, I_S, I_D, v_{Smax}, v_{Dmax}, v_{C1max}.

Table 3.3: Usable values for the SEPIC

Comp \ Value	$\mathbf{i_{max}}$	$\mathbf{i_{rms}}$	$\mathbf{I_{avg}}$	$\mathbf{v_{max}}$
Inductor $\mathbf{L_1}$	$I_{IN} + \frac{1}{2}\Delta i_{L1}$	$I_{IN}\sqrt{1 + \frac{1}{12}(\frac{\Delta i_{L1}}{I_{IN}})^2}$	I_{IN}	Whichever is larger of $\begin{cases} V_{IN} \\ \lvert V_{IN} - V_{C1} - V_{OUT}\rvert \end{cases}$
Inductor $\mathbf{L_2}$	$I_{OUT} + \frac{1}{2}\Delta i_{L2}$	$I_{OUT}\sqrt{1 + \frac{1}{12}(\frac{\Delta i_{L2}}{I_{OUT}})^2}$	I_{OUT}	$V_{OUT} \geq V_{C1} \Rightarrow V_{OUT}$ $V_{OUT} \leq V_{C1} \Rightarrow V_{C1}$
Switch	$I_{IN} + I_{OUT} + \frac{1}{2}(\Delta i_{L1} + \Delta i_{L2})$	$I_{IN}\sqrt{\frac{V_{OUT}+V_{IN}}{V_{OUT}}}$	I_{IN}	$V_{IN} + V_{OUT}$
Diode	$I_{IN} + I_{OUT} + \frac{1}{2}(\Delta i_{L1} + \Delta i_{L2})$	$I_{OUT}\sqrt{\frac{V_{OUT}+V_{IN}}{V_{IN}}}$	I_{OUT}	$V_{IN} + V_{OUT}$
Capacitor $\mathbf{C_1}$	Whichever is larger of $\begin{cases} I_{IN} + \frac{1}{2}\Delta i_{L1} \\ I_{OUT} + \frac{1}{2}\Delta i_{L2} \end{cases}$	$I_{IN}\sqrt{\frac{V_{IN}}{V_{OUT}}}$	0	V_{IN}
Capacitor $\mathbf{C_{OUT}}$	Whichever is larger of $\begin{cases} I_{IN} + \frac{1}{2}\Delta i_{L1} + \frac{1}{2}\Delta i_{L2} \\ I_{OUT} \end{cases}$	$I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}}$	0	V_{OUT}

3.3 Resonant Converters

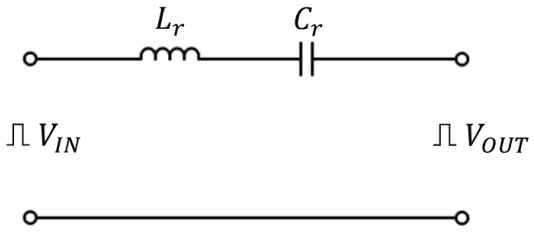


Figure 3.28: Series resonant circuit.

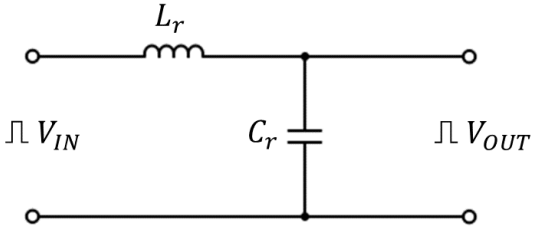


Figure 3.29: Parallel resonant circuit.

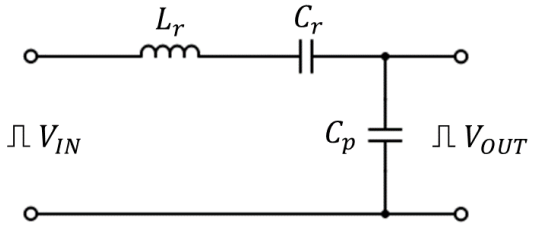


Figure 3.30: LCC circuit.

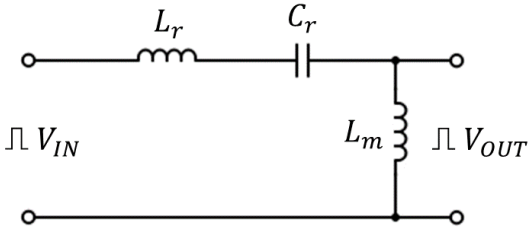


Figure 3.31: LLC circuit.

A resonant converter uses a network of inductors and capacitors known as a resonant tank to generate sinusoidal currents with very low harmonics [9], [23]. In the simplest form, only one inductor and one capacitor make up the resonant tank. This is known as a series or parallel tank network, depending on the connection of the resonant capacitor relative to the load. Figure 3.28 shows the series resonant tank, and the parallel resonant tank is shown in Figure 3.29. Adding a third element to the tank network results in two new network topologies. Adding a capacitor in parallel to the load in a series resonant converter results in a so called LCC topology, while the related LLC topology uses an inductor as the parallel element. Figures 3.30 and 3.31 show the LCC and LLC resonant tank networks, respectively.

Different from regular PWM converters, the output voltage of a resonant converter can be controlled by varying the switching frequency relative to the resonant frequency, thereby altering the impedance of the resonant tank. If the converter switching frequency is set to be equal or very close to the resonant frequency, very low switching losses can be achieved [16]. In a bridge converter, the transformer can be used to provide the required inductance in the resonant tank, avoiding the addition of some physical components. This is especially true for the LLC converter, as it uses two additional inductances, both of which can be incorporated into the transformer windings [16]. A major disadvantage of resonant converters is that high efficiency is typically only achieved close to the optimal switching frequency, suffering from large losses especially at light loads [9], [16].

Among the four types of resonant converters listed here, the LLC converter stands out for its ability to handle wide variations in load or output voltage, as well as the possibility to reduce the number of physical resonant elements [23]. For these reasons it has become a popular choice of converter for high voltage battery charger applications [16], and Section 3.3.1 will therefore focus on the design equations of an LLC converter.

3.3.1 The LLC DC/DC converter topology

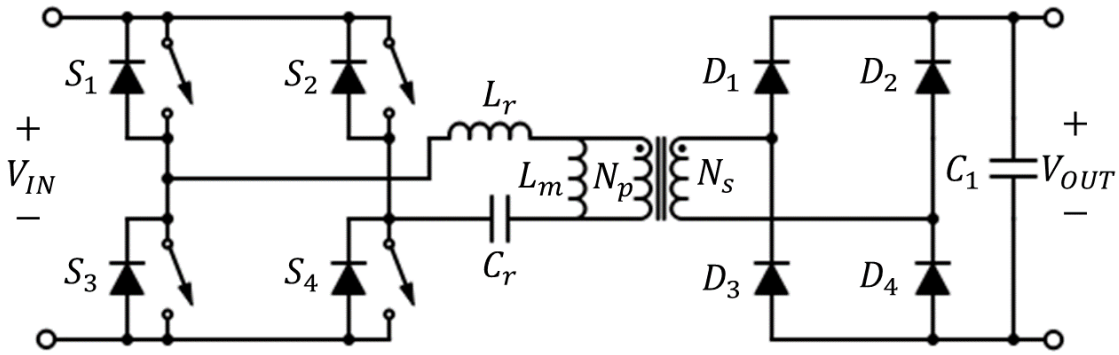


Figure 3.32: A full-bridge LLC converter.

Figure 3.32 shows one possible configuration of an LLC converter, here consisting of a full-bridge converter with an LLC resonant tank installed between the switches and the primary side of the transformer. Here it can be seen that the inductances L_r and L_m correspond to the leakage and magnetising inductances of the transformer. This means that the transformer can be designed to provide part or all of these inductances, reducing or eliminating the need for additional components. This is one major advantage of the LLC converter over the LCC converter, which always requires an additional physical capacitor. Compared to converters based on the simpler series and parallel resonant circuits, the LLC converter also comes with important benefits. Compared to the series resonant circuit the LLC is easier to control at light loads without too large changes in switching frequency, and it exhibits less circulating current losses than the parallel resonant converter [23].

As mentioned above, the voltage gain of an LLC converter is controlled by varying the switching frequency. The duty cycle is always 50 %, save for some dead time in order to prevent shoot-through in the converter bridge. When switches S_1 and S_4 are closed, S_2 and S_3 are open and vice versa. The voltage gain transfer function of an LLC resonant tank can be written as [23]

$$G = \left|\frac{V_{oe}}{V_{ge}}\right| = \left|\frac{j\omega L_m \parallel R_{ac}}{j\omega L_m \parallel R_{ac} + j\omega L_r + 1/j\omega C_r}\right| \tag{3.20}$$

where $\omega = 2\pi f_s$ is the switching frequency in rad/s and R_{ac} is the equivalent load resistance seen from the output of the resonant tank. R_{ac} is defined as

$$R_{ac} = \frac{8}{\pi}\frac{N_p^2}{N_s^2}R_0 \tag{3.21}$$

where N_p, N_s are the number of turns on the primary respectively secondary side of the transformer and R_0 is the resistance of a load connected to the output of the converter in parallel to the output capacitance C_1. The turns ratio of the transformer is defined as

$$n = \frac{N_p}{N_s} \tag{3.22}$$

where N_p is the primary winding and N_s is the secondary winding.The voltages V_{oe} and V_{ge} are the RMS values of the fundamental voltages of the square wave voltages on both sides of the resonant tank. In the case of the output voltage V_{oe}, this in an approximation which is often used in resonant converter design where the converter is assumed to operate close to resonant frequency [23]. The resonant tank input voltage V_{ge} relates to the DC input voltage V_{IN} as [23]

$$V_{ge} = \frac{2\sqrt{2}}{\pi}V_{IN} \tag{3.23}$$

and similarly V_{oe} relates approximately to V_{OUT} as

$$V_{oe} = \frac{2\sqrt{2}}{\pi}V_{OUT} \tag{3.24}$$

As can be seen from (3.20), the voltage gain of the LLC converter is dependent on the converter load, switching frequency and resonant component values. Due to the three resonant elements present in the LLC resonant tank, the tank will exhibit two different resonant frequencies [23]. The higher frequency

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.25}$$

is also found in the simpler series resonant tank, and provides unity gain at the resonant frequency. Replacing the series inductance term L_r with the total inductance $L_r + L_m$ yields another, lower, resonant frequency

$$f_r = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{3.26}$$

For the purpose of design and analysis of the converter, some new variables can be defined. First of all, the voltage gain is dependent on the switching frequency f_s of the converter relative to the higher resonant frequency, f_0. Knowing this, the switching frequency can be normalised to [24]

$$f_n = \frac{f_s}{f_0} \tag{3.27}$$

Similarly, the inductances L_r and L_m can be expressed as a ratio of total inductance to series inductance

$$m = \frac{L_r + L_m}{L_r} \tag{3.28}$$

Finally, the relationship between the series resonant elements L_r and C_r and the equivalent load resistance R_{ac} gives the quality factor

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}} \tag{3.29}$$

of the series resonant circuit. Using f_n, m and Q, the voltage gain transfer function G from (3.20) can now be written as

$$G = \frac{f_n^2(m-1)}{\sqrt{(mf_n^2-1)^2 + f_n^2(mf_n^2-1)^2(m-1)^2Q^2}} \tag{3.30}$$

The output voltage of the complete LLC converter is then expressed as

$$V_{OUT} = V_{IN} * G * n \tag{3.31}$$

that is, the product of resonant tank gain G and transformer turns ratio n.

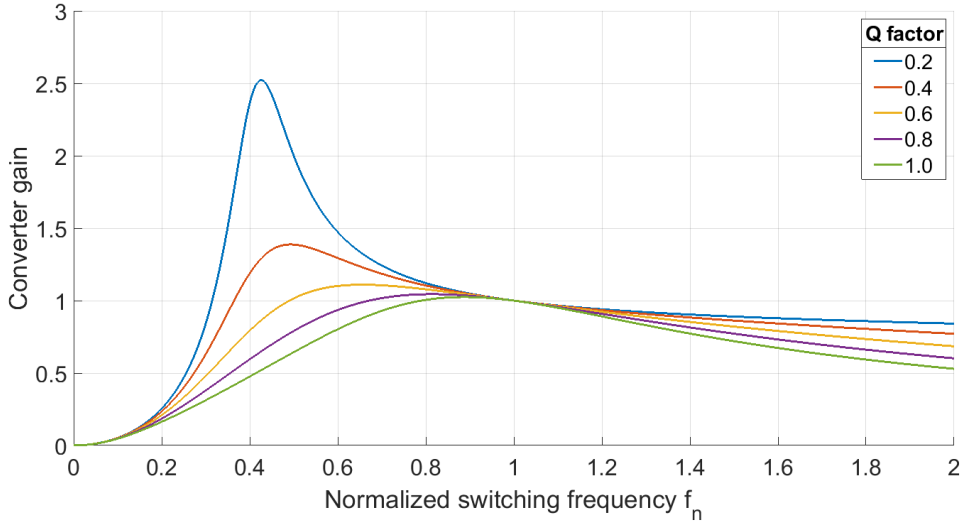


Figure 3.33: The LLC converter voltage gain V_{out}/V_{in} as a function of normalised switching frequency for different values of the Q factor and a fixed inductance ratio m = 6.

Figure 3.33 shows the converter gain of an LLC converter with an inductance ratio $m = 6$ plotted over the normalised switching frequency f_n for different values of Q. Since Q is load dependent, the curves can be thought of as showing the influence of the load as long as the series resonant elements are kept the same. It can be seen from the graph that operation above f_0 always results in a gain lower than one, while higher gains can be achieved in the region between f_r and f_0. Furthermore, all curves converge to unity gain at the resonant frequency, meaning that operation at this point is load independent. On the other hand, operation between f_r and f_0 is load dependent in both the amplitude of peak gain and the frequency at which peak gain occurs.

For frequency-modulated resonant converters such as the LLC converter, Pulse-Frequency Modulation (PFM) is often used instead of PWM. Using PFM, the duty cycle of the signal sent to the switches is fixed to a value close to 50%, and the output voltage is instead adjusted by varying the switching frequency dynamically.

3.3.2 Component stress in the LLC converter

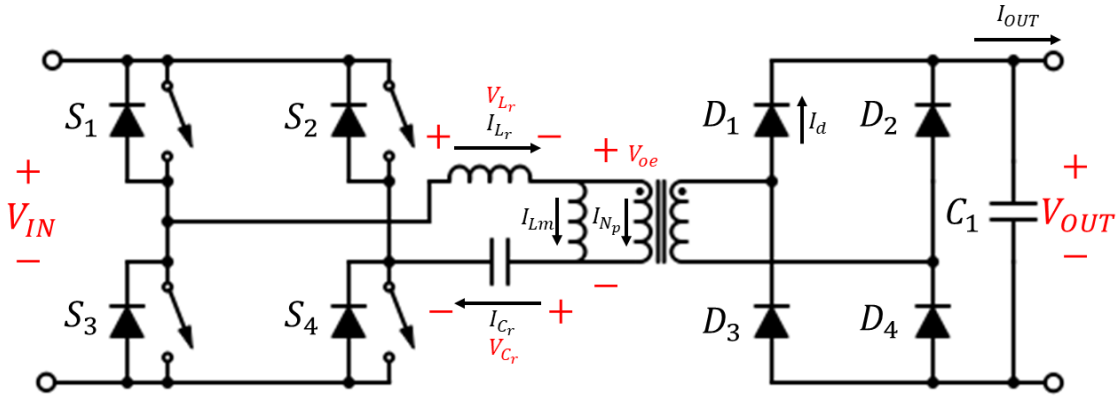


Figure 3.34: The full-bridge LLC converter with relevant voltages and currents.

The full-bridge LLC converter consists primarily of the switches in the H-bridge, the resonant elements, a transformer (itself part of the resonant circuit) and rectifying diodes. The voltages and currents which are relevant for component stress are illustrated in Figure 3.34 and the equations used to calculate them are listed below. The typical shape of some waveforms in the LLC converter can be seen in Figure 3.35. Note that these waveforms are valid for the case where the LLC converter is operating at resonant frequency. It can be seen that the shape of the current that

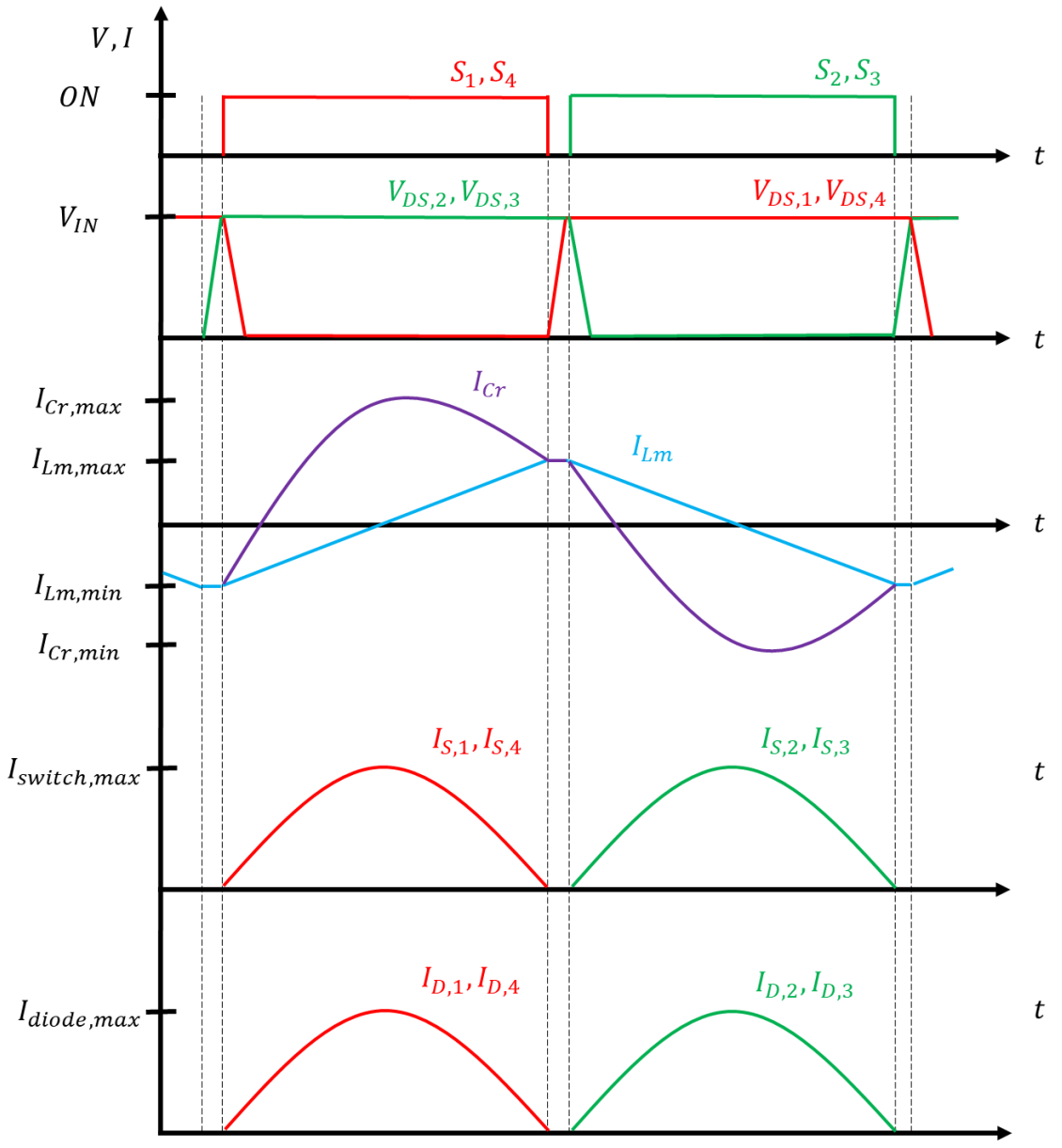


Figure 3.35: Typical waveforms of V_{DS}, I_{C_r}, I_{L_m}, I_{switch}, and I_{diode} in the LLC converter operating at resonant frequency.

flows through the resonant components C_r, L_r and the transformer is approximately sinusoidal. This approximation is useful in order to set up the equations needed to calculate current and voltage stress in the components that carry this current. It can also be seen that the dead time, when no switch is conducting, distorts the sinusoidal shape of the current. While a certain amount of dead time is necessary for safe operation of any bridge type converter, the dead time depicted in Figure 3.35 has been exaggerated for the purpose of illustration.

The magnetising inductance L_m is exposed to the voltage across the transformer primary winding, V_{oe} at the switching frequency f_s. The RMS value of this voltage can be expressed as [23]

$$V_{oe} = \frac{2\sqrt{2}}{\pi} n V_{OUT} \tag{3.32}$$

Using this expression for V_{oe} the current I_{L_m} can be calculated as

$$I_{L_m} = \frac{V_{oe}}{2\pi f_s L_m} = \frac{\sqrt{2} n V_{OUT}}{\pi^2 f_s L_m} \tag{3.33}$$

To calculate the voltage stress on the resonant capacitor, the capacitor current and capacitance needs to be known. As can be seen in Figure 3.34, the current in the resonant tank flows to the resonant capacitor from the parallel connection of the magnetising inductance and the transformer. The RMS current through the capacitor is therefore the sum of the currents I_{L_m} and I_{N_p} With these two currents known, the current I_{C_r} can be described as [23]

$$I_{C_r} = \sqrt{I_{N_p}^2 + I_{L_m}^2} \tag{3.34}$$

where I_{N_p} can be expressed as

$$I_{N_p} = \frac{\pi}{2\sqrt{2}} \frac{I_{OUT}}{n} \tag{3.35}$$

where n is the transformer turns ratio N_p/N_s and I_{OUT} is the DC output current. The RMS voltage across the capacitor, V_{C_r} is a function of current, capacitance and frequency according to

$$V_{C_r} = \frac{I_{C_r}}{2\pi f_s C_r} \tag{3.36}$$

In the resonant circuit from the input bridge to the transformer, the resonant inductor and resonant capacitor form a series connection. Therefore the current through the resonant inductor is the same as for the resonant capacitor, i.e $I_{C_r} = I_{L_r}$. The RMS voltage across the inductor, V_{L_r} is equal to

$$V_{L_r} = 2\pi f_s L_r I_{L_r} \tag{3.37}$$

For the switches S_1 to S_4, the maximum voltage that needs to be blocked is equal to the input voltage V_{IN}. Each pair of switches carry the resonant current approximately half of the time and the RMS current that one switch in the bridge needs to carry is related to the current in the resonant tank like

$$I_{switch} = \frac{I_{L_r}}{\sqrt{2}} = \frac{I_{C_r}}{\sqrt{2}} \tag{3.38}$$

The peak value of the switch current is equal to the peak value of the resonant circuit current:

$$I_{switch_{peak}} = \sqrt{2} I_{L_r} = \sqrt{2} I_{C_r} \tag{3.39}$$

which is the highest current that the switches must be rated for.

The maximum voltage stress on the rectifying diodes (D_1 to D_4 in Figure 3.34) is equal to the output DC voltage, V_{OUT}, and the peak current is equal to the peak current in the transformer secondary winding, which is related to the output DC current I_{OUT}. The RMS value of the transformer secondary current as a function of the DC output current can be expressed as [23]

$$I_{N_s} = \frac{\pi}{2\sqrt{2}} I_{OUT} \tag{3.40}$$

and its peak value, here expressed as the peak diode current, is therefore

$$I_{d_{peak}} = \sqrt{2} I_{N_s} = \frac{\pi}{2} I_{OUT} \tag{3.41}$$

For a transformer core, the minimum number of turns needed on the primary winding can be calculated by [25]

$$N_{p_{min}} = \frac{V_{IN}}{2 f_s \Delta B A_e} \tag{3.42}$$

where ΔB is the maximum flux density swing that the core should handle, and A_e is the core cross-sectional area.

For transformers operating at high frequencies, litz wire is often used in the windings to mitigate the skin and proximity effects [9]. Litz wire works best when the skin depth at a given operating frequency is larger than the wire strand radius. The skin depth δ can be calculated as [9]

$$\delta = \sqrt{\frac{\rho}{\pi \mu f_s}} \tag{3.43}$$

where ρ is the resistivity and μ the permeability of the wire material.

3.3.3 Zero voltage switching for the LLC converter

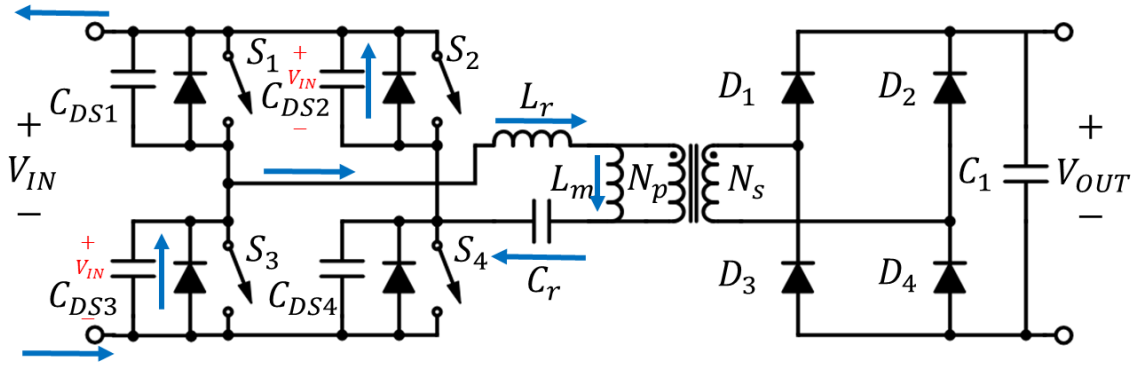


Figure 3.36: The full-bridge LLC converter with drain-source capacitance C_{DS} and all switches open during dead time.

The main reason why the LLC converter can achieve better efficiency than a non-resonant converter is the possibility to achieve Zero Voltage Switching (ZVS) [23]. With ZVS, turn-on losses become negligible, which is often a significant efficiency improvement especially in converters operating at high voltage or high frequency. The prerequisite of ZVS is that there should be no voltage across the switch when it turns on. In a MOSFET based converter, ZVS occurs when the MOSFET is turned on when its drain-source capacitance, C_{ds} is completely discharged. In an LLC converter, this capacitance is discharged during the so called dead time, in which all switches in the bridge are open in order to prevent shoot-through.

Figure 3.36 shows an instant of time in which switches S_1 and S_4 have just opened. Up until this point, these switches have been closed and carrying the resonant current, while switches S_2 and S_3 have been open, so that their C_{DS} are charged to V_{IN}. Due to the inductance of L_m, the current continues to flow during the dead time, but with S_1 and S_4 open, it finds a different path through the C_{DS} of switches S_2 and S_3, thereby discharging them.

Ideally, the dead time and the current through L_m should be matched so that the dead time is just enough to discharge C_{DS}. A too short dead time results in insufficient discharge of C_{DS} and failure to achieve ZVS. If the dead time is unnecessarily long, ZVS will be achieved but excessive current will flow through the antiparallel diodes of the switches, causing unnecessary losses. If L_m and C_{DS} are both known, the minimum dead time necessary can be written as [26]

$$t_d = 16 L_m C_{ds} f_s \tag{3.44}$$

If instead the dead time is pre-selected, the equation can be rearranged to calculate a maximum allowable inductance L_m according to

$$L_m = \frac{t_d}{16 C_{ds} f_s} \tag{3.45}$$

3.4 3-phase diode bridge rectification

From a common 3-phase outlet in Europe, each phase is supplied with 230 V (RMS), 50 Hz sinusoidal voltage with each phase 120° phase shifted in relation to each other. A common way to get DC voltage from the 3-phase AC source is to rectify it by using a 3-phase diode rectification bridge, see Figure 3.37 for circuit. Each phase in Figure 3.37, U_{L1}, U_{L2} and U_{L3} has the voltage source arrangement mentioned above, which can be expressed as

$$\begin{aligned} U_{L1} &= 230\cos(\theta)\text{V}, \\ U_{L2} &= 230\cos(\theta + 120°)\text{V}, \\ U_{L3} &= 230\cos(\theta - 120°)\text{V}, \end{aligned} \tag{3.46}$$

with θ being the phase angle.

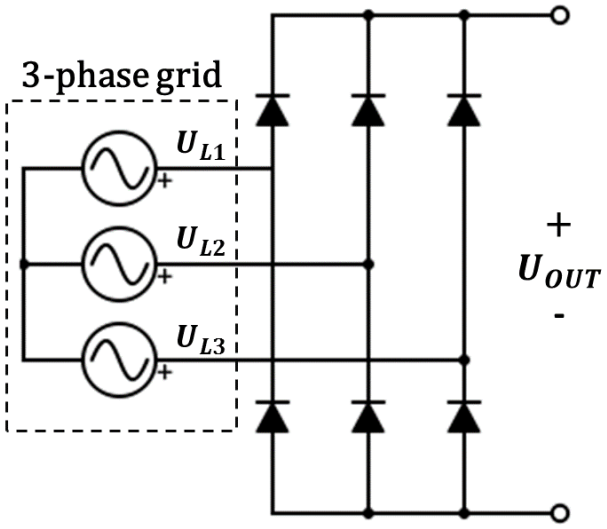


Figure 3.37: 3-phase grid supplying a diode rectification bridge.

During operation, each phase takes turns conducting through its corresponding top diode, when it is the most positive in relation to the other phases. While the top one is conducting, the other phases take turn in conducting through their bottom diode when they are the most negative in relation to each other. This pattern repeats itself over each period and creates a voltage at the output, U_{OUT}, that consists of positive co-sinusoidal bumps, each 60° wide with a peak value of the line-to-line peak value, which can be expressed as

$$\hat{U_{LL}} = U_{L1} \cdot \sqrt{3} \cdot \sqrt{2} = 563.383 \approx 563\,\mathrm{V}. \tag{3.47}$$

$\sqrt{3}$ comes from the 3-phase transformation from 1-phase to line-to-line identities and the $\sqrt{2}$ is there to obtain the peak value. To get an equivalent DC source to work with, the average of one bump is calculated, as mentioned above, each bump is $\theta_B = 60° = \frac{\pi}{3}$ with the peak in the middle, $\theta_P = \frac{\theta_B}{2} = 30° = \frac{\pi}{6}$. Note that the voltage drop over the diodes are neglected,

$$\begin{aligned} U_{OUT-AVG} &= \frac{1}{\theta_B}\int_0^{\theta_B} \hat{\mathrm{U_{LL}}}\cos(\theta - \theta_\mathrm{P})\,\mathrm{d}\theta = \frac{3}{\pi}\int_0^{\frac{\pi}{3}} \hat{\mathrm{U_{LL}}}\cos(\theta - \frac{\pi}{6})\,\mathrm{d}\theta = \\ &\frac{3}{\pi}\int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \hat{\mathrm{U_{LL}}}\cos(\theta)\,\mathrm{d}\theta \Rightarrow \frac{3\hat{\mathrm{U_{LL}}}}{\pi}\sin(\theta)\Big|_{-\frac{\pi}{6}}^{\frac{\pi}{6}} = \frac{3\hat{\mathrm{U_{LL}}}}{\pi} = 537.991 \approx 538\,\mathrm{V}. \end{aligned} \tag{3.48}$$

This voltage can be used as a simplified DC-source equivalent for simple simulations, calculations etc. For more precise uses, effects such as voltage ripple, voltage drop over diodes etc. needs to be taken into account.

3.5 Loss equations

This section contains equations required for the calculation of switching, core and conduction losses for the different components.

3.5.1 Switching losses

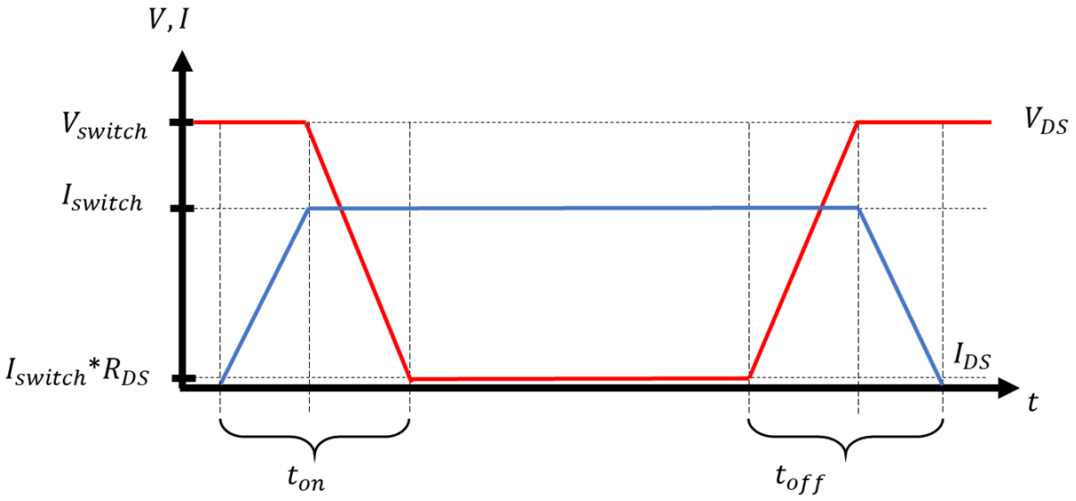


Figure 3.38: Simplified switching waveforms for a MOSFET.

Figure 3.38 shows the simplified switching waveforms of a MOSFET exposed to a drain-source voltage V_{switch} and carrying a current I_{switch}. Switching losses occur in the time periods t_{on} and t_{off}. For the buck converter, the switching loss can be calculated as [27]

$$P_{sw,buck} = \frac{1}{2} V_{in} I_{out} f_{s,buck} (t_{on} + t_{off}) \tag{3.49}$$

since $V_{switch} = V_{in}$ and $I_{switch} = I_{out}$. For the boost converter the equation looks like

$$P_{sw,boost} = \frac{1}{2} V_{out} I_{in} f_{s,boost} (t_{on} + t_{off}) \tag{3.50}$$

where $V_{switch} = V_{out}$ and $I_{switch} = I_{in}$. t_{on} and t_{off} are the rise and fall times of the MOSFET.

It is important to notice that these equations use the average current without considering the current ripple. The current at turn-on will be lower than the average current ripple by half the ripple magnitude, and the current at turn-off will be higher than the average by the same amount. Because of the linear relationship between switching current and losses, the end result when using the average current will be the same as if the ripple was considered.

For the LLC converter operating at resonant frequency, turn-on switching losses can be assumed to be zero. Turn-off losses will still be present, but thanks to resonance the turn-off current will be significantly lower than the average current passing through the switch. The turn-off current in the bridge can be calculated as [26]

$$I_{off} = \frac{nV_{OUT}T}{4L_m} \tag{3.51}$$

where $T = 1/f_s$, and from here the switching loss for all four MOSFETs is given as [26]

$$P_{off} = \frac{nI_{off}V_{OUT}t_{fall}}{T} = \frac{n^2V_{OUT}^2t_{fall}}{4L_m} \tag{3.52}$$

3.5.2 Ferrite core losses

The core loss density of a ferrite core can be calculated as

$$P_{fe} = kf_p^x B_{peak}^y \tag{3.53}$$

where coefficients k, x, y are all dependent on the specific ferrite and the shape of the core. The core loss is then calculated using the volume of the core as

$$P_{core} = P_{fe}V_{core} \tag{3.54}$$

3.5.3 Conduction losses

If the forward voltage drop across the component can be modelled as $V_0 + Ri(t)$, the average conduction losses over a switching period can be calculated as

$$P_{cond} = V_0I_{avg} + RI_{rms}^2 \tag{3.55}$$

where V_0 is the constant voltage drop across the component, I_{avg} is the average current through the component, and I_{RMS} is the RMS value of the current. For a diode this can be simplified to

$$P_{diode} = V_0I_{diode} \tag{3.56}$$

as long as the operating conditions of the diode does not exceed the test conditions used by the manufacturer when determining V_0.
If the element is a transformer or inductor winding, the resistance is calculated as

$$R_{winding} = \frac{\rho N * MLT}{A_w} \tag{3.57}$$

where N is the number of turns, MLT is the mean length per turn of wire and A_w is the copper area of the winding [26].

4
Initial Topology Selection

In this chapter, the initial topology selection is motivated using the available literature on the subject. Different stages of converters are suggested dependent of chosen topology and an initial choice is made regarding the SiC components in order to aid the design.

4.1 Two-stage converters

As mentioned in Section 1.4, galvanic insulation between the grid and the battery is an important requirement for this type of charger. Simple converter topologies such as the buck, boost and buck-boost converter therefore cannot be used alone in this case due to the galvanic connection between input and output. Bridge-type converters featuring a transformer on the output fulfil the galvanic insulation requirement, and using a resonant bridge converter can greatly improve converter efficiency by reducing switching losses. In [28] a highly efficient SiC-based LLC converter for high voltage applications is demonstrated. A bidirectional resonant converter intended for high power low voltage applications is described in [29], also using SiC MOSFETs.

In [30], a so called two stage converter is proposed for use as an electric vehicle charger. In this setup, a boost-type PFC converter is connected to the grid on the input side, and an LLC converter on its output. The boost PFC outputs a fixed DC voltage which is used as input by the LLC, and the output voltage of the charger is controlled by the LLC, in the same way as the single stage LLC converters. Such converters are however more difficult to control, and achieving the wide output voltage range necessary for charging batteries comes at the cost of lower efficiency when operating at frequencies away from the resonant frequency [16].

One solution that has been tested with good results in the literature ([16], [26], [31]) is to use a two-stage converter with a different voltage control strategy. Instead of regulating the output voltage via frequency control of the resonant converter, the non-isolated DC/DC power stage feeds an isolated resonant converter which always operates at unity voltage gain. Voltage control is then achieved by PWM control of the non-isolated stage. This type of setup combines the simplistic voltage control and design of a non-isolated converter and the high efficiency and galvanic isolation of the resonant bridge converter. See Figure 4.1 for a block schematic, in which $L_1 - L_3$ is the 3-phase grid input and $U_{DC}-$,$U_{DC}+$ is the DC voltage output .

In [16] the proposed converter, a SEPIC+LLC two-stage converter, is tested with both operation strategies in order to provide a direct comparison of efficiency. It is shown that while the two strategies provide similar efficiency at full load, the LLC converter operated at unity gain maintains close to maximum efficiency at all loads between 20% and 100%. At 20% load, the efficiency of the LLC at unity gain is close to 97%, while the efficiency of the frequency-controlled LLC converter drops to under 90%. In [26], a simulation model of another two-stage converter with boost PFC and LLC stages is tested in the same way, showing that the efficiency of the fixed-frequency control strategy is 2.5% more efficient at high load, and 8.9% more efficient at low load. Also in [31], simulation results of a similar converter show very high efficiency for this operation strategy.

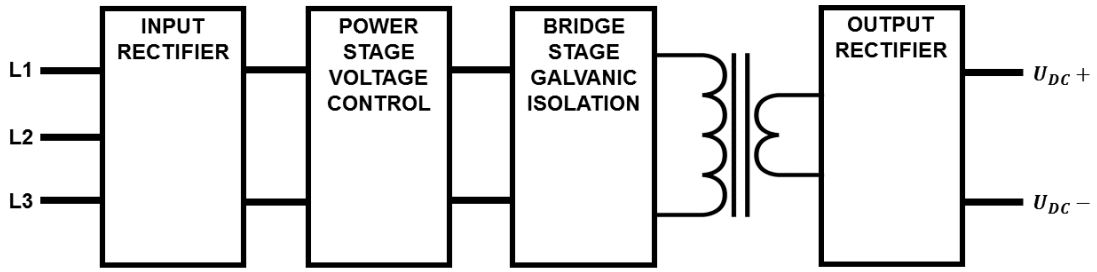


Figure 4.1: Block schematic of two-stage topology.

With this setup, there are different alternatives to consider for managing the desired output voltage range. Both the power stage and the turns ratio in the transformer can be used to steer it in either direction when compared to the input voltage. As the rectified input voltage is within the desired output voltage range, three main alternatives are available:

1. DC/DC power stage that can output a voltage both over and under its input voltage (Buck-Boost/SEPIC) with 1:1 transformer turns ratio.
2. Buck type DC/DC power stage and step up transformer turns ratio.
3. Boost type DC/DC power stage and step down transformer turns ratio.

As the full bridge LLC converter has proven itself to be a suitable and highly efficient bridge stage converter in the literature [16], [26], [28], [30], [31] and its advantages have been laid out in Section 3.3, this topology will be used in all converters studied within the scope of this project. Based on the available sources it is unlikely that other resonant or hard-switching bridge converters would outperform the LLC

converter in this application, and the project will therefore focus on the comparison of the different voltage regulating stages, with only small modifications to the LLC converter in order to adapt it to different voltage and current requirements.

4.2 SEPIC power stage

Out of the basic converters that can output both a higher and lower voltage compared to its input, the SEPIC was chosen as the most suitable as it does not invert the polarity of the output voltage. From Sections 3.2.3, 2.2.1 using (3.47), (3.48) one can combine the ratings of the charger and apply them to the ratings from Table 3.3, to find the maximum voltage stress, the average and the RMS-current stress on the switch and diode, as no other component rating is needed,

$$v_{Smax} = v_{Dmax} = V_{IN,max} + V_{OUT,max} = 563\,\mathrm{V} + 600\,\mathrm{V} = 1163\,\mathrm{V}, \tag{4.1}$$

$$i_{Srms} = I_{IN,avg}\sqrt{\frac{V_{OUT,min} + V_{IN,avg}}{V_{OUT,min}}} = \frac{9000\,\mathrm{W}}{538\,\mathrm{V}}\sqrt{\frac{400\,\mathrm{V} + 538\,\mathrm{V}}{400\,\mathrm{V}}} = 25.62\,\mathrm{A}, \tag{4.2}$$

$$i_{Drms} = I_{OUT,avg}\sqrt{\frac{V_{OUT,min} + V_{IN,avg}}{V_{IN,avg}}} = \frac{9000\,\mathrm{W}}{400\,\mathrm{V}}\sqrt{\frac{400\,\mathrm{V} + 538\,\mathrm{V}}{538\,\mathrm{V}}} = 33.01\,\mathrm{A}. \tag{4.3}$$

The current limits are taken from the lowest output voltage operating point to give the highest operating RMS-current. The voltage limits can be considered to be at the low end as it does not take any losses of the converter or harmonics from switching etc. into account. Furthermore, a good design principle is to keep a safety margin to ratings such as the ones calculated above, especially maximums. Therefore should the ratings of a prospective component be even higher than the above calculated values with a margin. SiC components available on the market that meet the requirements stated above are few, as the components rated to the standard 1200 V is deemed to be to close the maximum voltage rating. The standard step up from 1200 V is 1700 V, which is deemed more appropriate for this application. However, there are few manufacturers who offer SiC components rated to this higher rating - the only alternatives found can be seen in Table 4.1.

Table 4.1: Suitable SiC components rated to 1700 V

Switch	Diode
Cree/Wolfspeed C2M0045170D [32]	Cree/Wolfspeed C3D25170H [33]
Cree/Wolfspeed C2M0045170P [34]	GeneSic Semiconductor GB25MPS17-247 [35]
Cree/Wolfspeed C2M0080170P [36]	GeneSic Semiconductor GB50MPS17-247 [37]

Furthermore, none of the above mentioned components were available for purchase at any of these four major distributors:

- DigiKey (`https://www.digikey.se`)
- Mouser (`https://www.mouser.se`)
- Farnell (`https://se.farnell.com`)
- RS Components (`https://se.rs-online.com/`),

during the time of the project. Either they were not available at all or the stock was empty with a factory lead time of above 20 weeks. If one takes a step down and looks at suitable switches and diodes rated for 1200 V, more manufacturers joined with alternatives and the aforementioned manufacturers had a wider range of components to choose from, see Table 4.2 for a selection of suitable components rated to 1200 V.

Table 4.2: Suitable SiC components rated to 1200 V

Switch	Diode
Cree/Wolfspeed C2M0025120D [38]	Cree/Wolfspeed C4D40120D [39]
GeneSic Semiconductor GR25MT12K [40]	GeneSic Semiconductor GC50MPS12 [41]
ROHM SCT3030KL [42]	ROHM SCS240KE2 [43]
Littelfuse LSIC1MO120E0080 [44]	Littelfuse LSIC2SD120E30CC [45]
ST Microelectronics SCT30N120 [46]	ST Microelectronics STPSC20H12 [47]

Several of these components were available in stock at the above mentioned suppliers and other alternatives not named above were also available. Due to the timing constraint of this project, the SEPIC setup as a voltage control stage was discarded as it is dependent on components that would not be available for usage in a prototype build. Other topologies that can use 1200 V rated components should be considered instead.

4.3 Buck power stage

An alternative setup would be to have a step-up transformer coupled together with a buck converter. The step-up transformer moves the middle stage voltage range completely beneath the input voltage, i.e. a suitable environment for a buck converter. As the buck converter doesn't have a minimum output voltage and the maximum output voltage is the same as the input, the main concern for the *step up transformer ratio* η_{SU}, is to give some margin in buck output voltage and use a sensible number of turns. Due to maximum voltage output, the lower limit for the ratio becomes

$$\eta_{SU} \geq \frac{V_{Ch-OUT,max}}{V_{IN,avg}} = \frac{600}{538} \approx 1.115. \tag{4.4}$$

As the maximum voltage stress on the switch and diode from table 3.1 is only the maximum input voltage, i.e. = 563 V, the 1200 V rated SiC components mentioned in Section 4.2 are available depending on the current stress. Therefore the upper limit of the ratio is more connected to the output current - as a higher ratio will decrease the needed output voltage and subsequently increase the needed output current. As switching-, conduction- and diode-losses for a buck converter are connected to the

output current, keeping it low in preferable. Subsequently, keeping the transformer ratio low is preferable to reduce losses. Therefore $\eta_{SU} = 11/9 \approx 1.222...$ was chosen, setting the buck converter output limits to:
•600 V charger output

$$\begin{aligned} V_{OUT,600V} &= \frac{V_{Ch-OUT}}{\eta_{SU}} = \frac{600\,\mathrm{V}}{(11/9)} = 490.909\,\mathrm{V} \approx 491\,\mathrm{V}, \\ I_{OUT,600V} &= \frac{P_{OUT,max}}{V_{OUT,max}} = \frac{9\,\mathrm{kW}}{491\,\mathrm{V}} = 18.33\,\mathrm{A}, \end{aligned} \tag{4.5}$$

•400 V charger output

$$\begin{aligned} V_{OUT,400V} &= \frac{V_{Ch-OUT}}{\eta_{SU}} = \frac{400\,\mathrm{V}}{11/9} = 327.272\,\mathrm{V} \approx 327\,\mathrm{V}, \\ I_{OUT,400V} &= I_{Ch-OUT,max} \cdot \eta_{SU} = 20\,\mathrm{A} \cdot (11/9) = 24.44\,\mathrm{A}. \end{aligned} \tag{4.6}$$

4.4 Boost power stage

The last alternative setup would be to have a step-down transformer coupled together with a boost converter. The step-down transformer moves the middle stage voltage range completely above the input voltage, i.e. a suitable environment for a boost converter. As the average input voltage is the lowest voltage a boost converter can output, the *step down transformer ratio* η_{SD}, needs to divide it down to at least the lowest desired output voltage of the charger. Therefore the transfer ratio must be lower than or equal to

$$\eta_{SD} \leq= \frac{V_{OUT,min}}{V_{IN,avg}} = \frac{400\,\mathrm{V}}{538\,\mathrm{V}} \approx 0.7435. \tag{4.7}$$

For the lower limit, one can look at the maximum voltage stress on the switch and diode from Table 3.2, as a low ratio will push the required boost output voltage high and subsequently expose the switch and diode to the same voltage. A too small transformer ratio would move the required output voltage above the rated voltage of the available SiC components mentioned in Section 4.2 and therefore move the boost converter out of contention for the same reason as the SEPIC, lack of suitable components. Furthermore, as the middle stage voltage will be connected to more components with yet unknown voltage limits, a low middle stage voltage is somewhat preferable. The design of the mentioned components will be done later in the report. Therefore the transformer ratio is set to $\eta_{SD} = 11/15 \approx 0.733$, setting the boost converter output limits to:
•600 V charger output

$$\begin{aligned} V_{OUT,600V} &= \frac{V_{Ch-OUT}}{\eta_{SD}} = \frac{600\,\mathrm{V}}{11/15} = 818.182\,\mathrm{V} \approx 819\,\mathrm{V}, \\ I_{OUT,600V} &= \frac{P_{OUT,max}}{V_{OUT,max}} = \frac{9\,\mathrm{kW}}{819\,\mathrm{V}} = 10.99\,\mathrm{A}, \end{aligned} \tag{4.8}$$

•400 V charger output

$$V_{OUT,400V} = \frac{V_{Ch-OUT}}{\eta_{SD}} = \frac{400}{11/15} = 545.454 \approx 545\,\text{V}, \\ I_{OUT,400V} = I_{Ch-OUT,max} \cdot \eta_{SD} = 20\,\text{A} \cdot (11/15) = 14.67\,\text{A}. \tag{4.9}$$

4.5 SiC component selection

Since the use of SiC components is central to the aim of the project, an initial selection of MOSFETs and rectifying diodes will be done so that the properties of these components can be used for the design and that virtual models of the components may be used for simulation. Several of the components mentioned in Table 4.2 are feasible alternatives, as they surpass the output voltage of the suggested boost converter with some margin. The current rating is more of a wild card, as the peak-, rms- and average value is dependent on more components in the converter, however it does need to be large enough to meet the goal of 20 A charger output current, preferably with some margin.

The MOSFET eventually chosen for evaluation is the C2M0040120D SiC power MOSFET from Cree Inc. Some properties of this MOSFET are listed in Table 4.3.

Table 4.3: Some properties of the C2M0040120D SiC power MOSFET.

Property	Value
Drain-Source voltage, V_{DS}	1200 V
Continuous drain current, I_D	60 A
Drain-Source On-State resistance, R_{DS}	84 mΩ
Output capacitance energy, E_{OSS}	84 µJ
Rise time, t_{rise}	52 ns
Fall time, t_{fall}	34 ns

The selected SiC power diode used for rectifying current in the step-down, step-up and LLC converter stages is the C4D40120D SiC Schottky diode also from Cree, Inc. This diode has properties according to Table 4.4.

Table 4.4: Some properties of the C4D40120D SiC Schottky diode.

Property	Value
Repetitive peak reverse voltage, V_{RRM}	1200 V
Continuous forward current, I_F	54 A
Forward voltage, V_F	2.2 V

Both SiC components are delivered in TO-247-3 packages, and to simplify the design the same type of switch and diode will be used for both converter stages.

4.6 LLC converter design

In order to simplify the comparison of different converters, only two LLC converter designs will be developed. One will be intended for use together with a buck converter and therefore has an output voltage higher than its input. The opposite is true for the other LLC converter designed to work with a boost converter. If a SEPIC converter is chosen as the primary stage, it can use either LLC converter or a new LLC converter can be developed with unity transformer ratio. As the only important function of the LLC converter stage in this particular application is to drive the transformer and provide galvanic isolation, it will be designed to operate at unity gain only. The switching frequency, typically a tradeoff between magnetic component size and switching losses, was decided on after some discussion together with Aros Electronics. A low switching frequency, below 50 kHz, would be impractical due to the need for a high power transformer and other large magnetic components. At such low frequencies, transformer and inductor cores would become very large and possibly difficult to purchase from regular electronics and magnetics suppliers. On the other hand, a high switching frequency of above 150 kHz, would hurt efficiency and possibly make the selection of controller and gate driver components more difficult. For this reason a switching frequency of 75 kHz is eventually chosen for the LLC converter.

By optimising for one operating point, efficiency can be maximised [16], and in [26], the author proposes a design method for LLC converters that optimises efficiency at unity gain. The idea is to maximise the size of the magnetising inductor L_m while still achieving ZVS. A large magnetising inductance has the advantage of lower circulating current (see (3.33)) in the resonant tank and therefore lower conduction losses. However, a too large inductance does not allow the parasitic capacitance of the switches to discharge fully, forcing the converter out of ZVS and thereby lowering the efficiency.

The dead time is chosen to be 120 ns, as this value is close to the typical minimum dead time of some resonant controller circuits [48]–[50]. During testing, the dead time may then be increased if needed. With this value, the inductance of L_m is calculated using (3.45) to be 610 µH. The value of the MOSFET capacitance C_{OSS} was calculated from a datasheet value for E_{OSS} as

$$C_{OSS} = \frac{2E_{OSS}}{V^2} = \frac{2 * 82\,\mu\text{J}}{(1000\,\text{V})^2} = 164\,\text{nF} \tag{4.10}$$

taking the value of E_{OSS} from one of the suitable MOSFETs [38] described in (4.2). With L_m selected, the other component values can be chosen. Having also decided on the transformer turns ratios in Sections 4.3 and 4.4, the equivalent load resistances for the two alternatives can be calculated using (3.21). The load resistance used for this calculation is the lowest possible, i.e when the converter is operating at minimum voltage and maximum current, and the load resistances thus become $R_{ac_{buck}} = 10.85\,\Omega$ and $R_{ac_{boost}} = 30.14\,\Omega$, respectively.

The Q factor is chosen as a tradeoff between resonant component size, maximum voltage gain capability, and sensitivity to frequency control. A large value, such as 1, for a given load resistance requires an increase in the ratio L_r/C_r, see (3.33). A larger L_r or smaller C_r both lead to higher component voltage stress, see (3.37) and (3.36). It also makes the converter output voltage sensitive to small variations in normalised frequency, which could be caused by inductance or capacitance drift in the resonant components. A too low value such as 0.1 makes the converter insensitive to frequency variations to the point where PFM control can no longer be used to control the gain in a meaningful way. In Figure 3.33 it can be seen that while a low Q factor does enable a high gain at lower frequencies, the curve is very flat for frequencies above resonance. In other words, operation at a gain lower than unity is harder to achieve unless the switching frequency is significantly increased. This is detrimental in a situation where voltage control using the LLC converter might be desired, such as when operating in the soft-start mode described later in Section 6.3.5. With this in mind, the Q factor is set to 0.7 for both LLC converters. This value enables some voltage control around resonant frequency while also keeping the voltage stress of the components, especially that of the resonant capacitor C_r, within levels that can reasonably be handled by available off-the-shelf components.

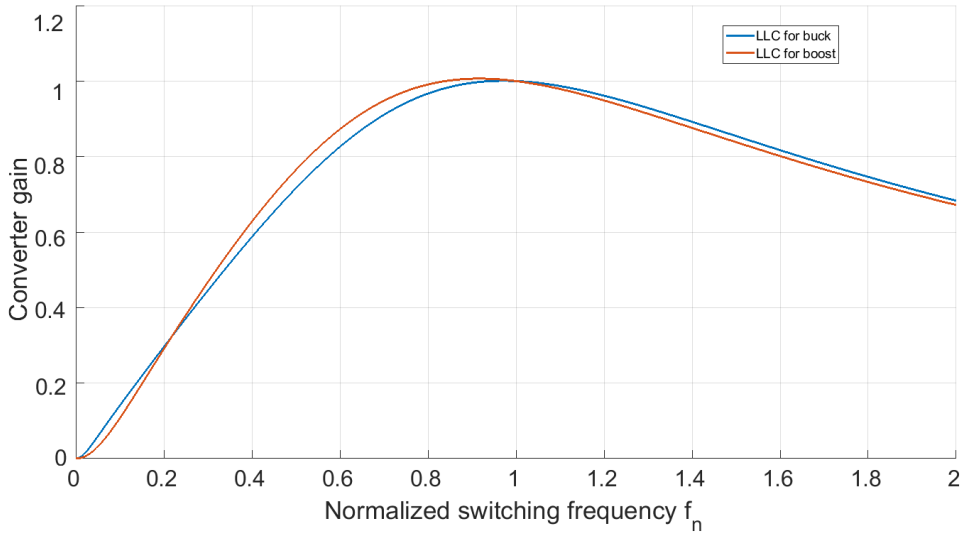


Figure 4.2: Converter gains of the two designed LLC converters

Knowing the Q value and L_m, the other resonant elements C_r and L_r can now be selected by rearranging (3.25) and (3.29). The final values of both LLC converters can be seen in Table 4.5. Figure 4.2 shows the gain plots for the two converters for the Q- and m-values listed at the bottom of Table 4.5. As can be seen from the plots, the peak gain barely goes above unity at any point, indicating that neither converter is designed to be able to output a voltage above the input voltage. This is a result of the relatively high Q-factor of 0.7 and is chosen so because there is no need for the converter to be able to operate with a voltage gain of more than unity in this application. Both converters are however able to reduce the output voltage

if the switching frequency is increased. As mentioned before, this reduced voltage operation is useful in the start-up procedure.

Table 4.5: Resonant element values for the two LLC converters.

Resonant element	LLC for buck	LLC for boost
L_m	610 µH	610 µH
L_r	45 µH	16 µH
C_r	100 nF	279 nF
Q factor	0.7	0.7
Inductance ratio m	14.6	38.8

4.6.1 Voltage and current stress

The theoretical values of voltage and current stress of the components in the two alternative LLC converters are calculated here. A summary of all calculated values is presented later in Tables 5.16–5.21 together with simulated values.

4.6.1.1 Magnetising inductor

The RMS current through the magnetising inductor is calculated using (3.33) for the operating point with the highest output voltage, as this maximises the current. This current is calculated to 1.54 A for the buck converter and 2.56 A for the boost converter. The peak voltage stress is simply the maximum input voltage, that is 491 V with the buck converter and 818 V with the boost converter.

4.6.1.2 Resonant capacitor

For the resonant capacitor, as well as for the resonant inductor, the highest current and voltage stress occurs at the operating points where the output current is the highest. Using (3.34) and (3.35), the RMS current through C_r is calculated as 27.19 A for the buck converter and 16.49 A for the boost converter. Using the values for capacitance listed in Table 4.5, the RMS voltages can be calculated with (3.36) to 206.8 V with the buck converter and 349.9 V with the boost converter.

4.6.1.3 Resonant inductor

As mentioned before, the same current flows through C_r and L_r, so it is enough to calculate the voltage across the inductor in the two cases using (3.37). This gives 205.0 V if using the buck converter and 349.7 V with the boost converter.

4.6.1.4 Transformer

The transformer primary side is exposed to the voltage V_{oe}. Using a fixed gain of 1, the magnitude of the square wave voltage is approximately equal to V_{IN}, in the worst case 818 V if a boost converter is used. The area of the switching voltage during normal operation would be equal to $V_{oe}/(2f_s) = 0.0055\,\mathrm{V\,s}$ in the same case. The output voltage is the same for both converters, 600 V. The output current from the transformer is equal to I_{N_p}/n, which is 22.21 A for both converters. The input current I_{N_p} to the transformer is 27.15 A with the buck and 16.29 A with the boost.

4.6.1.5 Switches

The switches need to block the input voltage of the two converters, which is as mentioned before equal to 491 V using the buck converter and 818 V using the boost converter. The peak current is equal to the peak of I_{C_r} and I_{L_r}, that is 38.46 A with the buck converter and 23.32 A with the boost converter. The RMS current load on the switches is lower than for the resonant elements, due to the fact that only two switches need to conduct at the same time. The RMS current through one switch in the LLC converter bridge is calculated using (3.38) to be 19.22 A with the buck converter and 11.66 A with the boost converter.

4.6.1.6 Diodes

The diodes need to block the maximum output voltage of 600 V for both converters. Using (3.41) the peak current that the diodes will have to carry can be calculated to 31.41 A. Similar to the MOSFETs, the bridge diodes share the load so that the RMS current through one diode becomes 15.71 A.

5

Simulations & Final Topology Selection

In this chapter, simulation models based on the two alternative converters designed in Chapter 4 are developed . The simulation models are made in LTspice with emphasis on the SiC components, and the simulations are then ran at different operating points, with the purpose of gaining values for loss calculations and component design. The results of the simulations are then used as basis for the final choice of the converter topology and its design parameters.

5.1 Buck simulations

For the power stage converter simulations, there are four main components and one attribute that needs to be dimensioned to build accurate simulation models:

- Switch
- Diode
- Main inductor
- Output capacitor
- Switching frequency

For the switch and diode, the components chosen in Section 4.5 had well functioning spice models and those were subsequently used (i.e switch: Cree Wolfspeed C2M0040120D, diode: Cree Wolfspeed C4D40120D). The MOSFET model had temperature ports for temperature estimations for both case and junction - but as temperature data is not of interest (as of yet) in this simulation set, those ports were connected to constant DC voltages of fitting values according to the manufacturer specification [51]. The switching frequency was set to 50 kHz after discussions with Aros Electronics, as it was seen as an achievable goal by using a similar driver circuitry as the bridge stage. Note that this switching frequency is different from the one chosen for the LLC converter, which is 75 kHz. As mentioned in Section 3.2.1, the size of the inductor has a big influence on the mode of operation for the converter. Applying the specifications in Sections 2.2.1 and 4.5 to (3.4), the minimum inductance value needed to keep CCM dependent on output voltage for the buck converter was calculated and then plotted in Figure 5.1. In the plot, maximum power output with the 20 A charger output current limit is assumed over the whole voltage range.

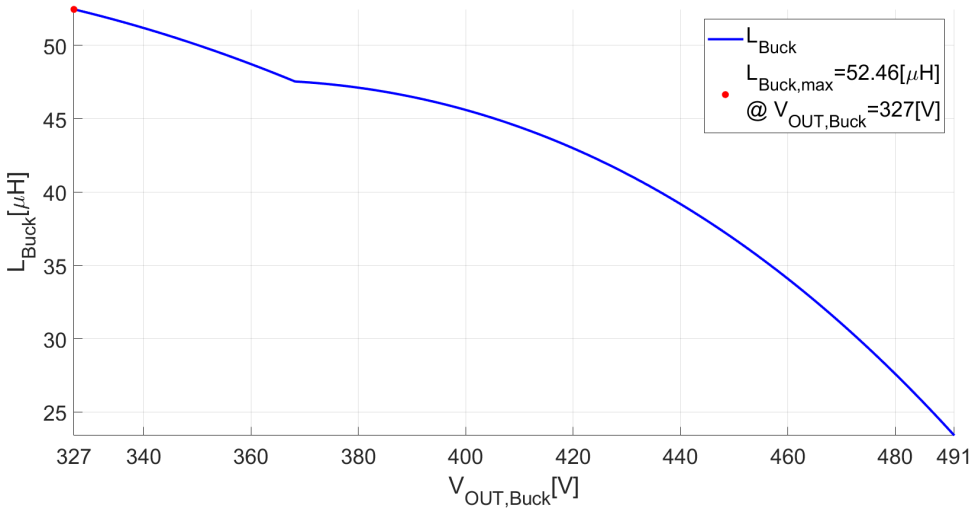


Figure 5.1: Plot of minimum inductance needed for CCM operation dependent on output voltage with maximum power output and charger current limitation.

The minimum value needed to achieve CCM operation over the whole voltage range at max power and current output became $L_{Buck} = 52.46\,\mu H$. However, as (3.4) is dependent on the output current, another scenario which could be of interest for the inductor design is if the charge current is reduced. With the output voltage locked to either minimum output voltage (blue line) or maximum output voltage (red line) in (3.4) and sweeping the output current from the maximum down to 0, the minimum inductance was calculated and plotted in Figure 5.2.

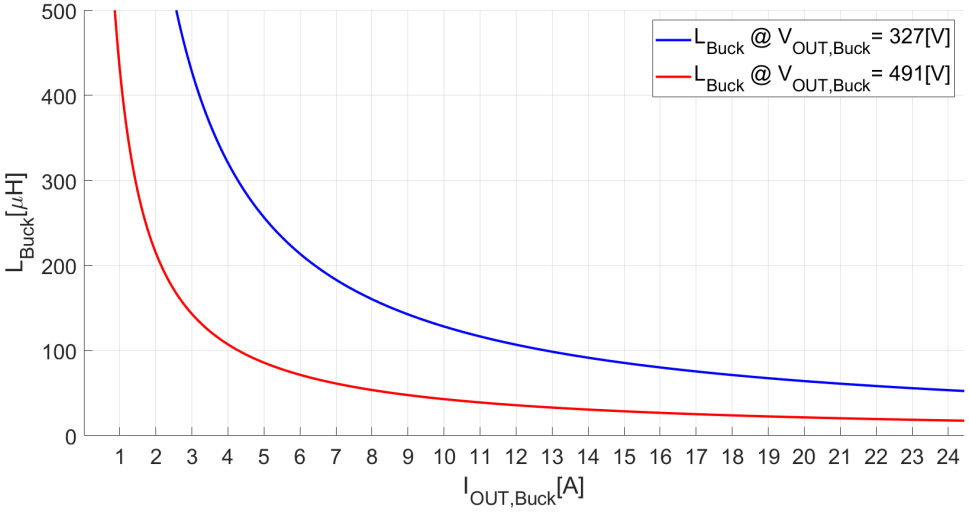


Figure 5.2: Plot of minimum inductance needed for CCM operation dependent on output current with the maximum (red) and minimum (blue) output voltage locked.

All other output voltage cases will become lines that will fall between these two lines seen in the plot. Worth noting is that as $I_{OUT,Buck}$ is part of the denominator in (3.4), as it approaches 0 A the inductor $L_{Buck} \to \infty$. Therefore it will be impossible to keep

the operation mode to CCM for low output currents, regardless of inductor size. If the output current is reduced below any of the change-over points, the converter will switch mode of operation to DCM and subsequently change operational dynamics. In all cases, a large inductor is preferable for keeping CCM operation for as low output currents as possible.

To simulate component stresses and get data for loss calculations on switch and diode, the high power operating points are chosen to be simulated. Three operating cases were chosen, see Table 5.1 for case summation. These correspond to the minimum output voltage (Case 1), charger current limitation change over point (Case 2) and maximum output voltage (Case 3). To make sure to get CCM operation in all of the cases, an inductor of 55 µH is chosen, to have some margin to the minimum value mentioned in the previous paragraph.

Table 5.1: Buck converter operating points for component stress simulation cases

Case	Output voltage	Output current	Output power
1	327 V	24.44 A	7.992 kW
2	368 V	24.44 A	9 kW
3	491 V	18.33 A	9 kW

To make the simulations run smoother and faster, a parallel resistance of 100 MΩ was added to the inductor model, as ideal components has a tendency to slow down simulations in LTspice. This small imperfection will result in a leakage current in the range of 0 µA to 6 µA, which is small enough to be neglected for the result but does still help to reduce the simulation time. With the given parameters above, the size of the output capacitor is calculated with an aimed maximum output voltage ripple of 5%, which is general accepted voltage ripple [16], [30]. For the buck converter, the high power, low output voltage operating point leads to the scenario with the largest output voltage ripple, and it is subsequently used to dimension the capacitor. Using the voltage-charge relation of a capacitor together with the aimed ripple voltage, the capacitor current waveform seen in Figure 3.15 and the peak-to-peak inductor current (i.e applying the inductor size and operating point to (3.3)), see Table 5.2 for summation of values, the smallest capacitance value can be calculated as

$$\begin{aligned} \Delta v_{OUT} = \frac{Q_c}{C_{OUT}} \Rightarrow \begin{bmatrix} Q_c = \Delta i_L T/8 \\ \Delta v_{OUT} \leq 0.05 \cdot V_{OUT} \end{bmatrix} \Rightarrow 0.05 \cdot V_{OUT} \geq \frac{\Delta i_L T}{8 C_{OUT}} \Rightarrow \\ 0.05 \cdot V_{OUT} \geq \frac{\Delta i_L}{8 C_{OUT} f_{sw}} \Rightarrow C_{OUT} \geq \frac{\Delta i_L}{8 \cdot 0.05 \cdot V_{OUT} f_{sw}}. \end{aligned} \tag{5.1}$$

Table 5.2: Summation of values for calculation of output capacitor size for Buck converter simulation model.

Property	Value
V_{OUT}	327 V
V_{IN}	538 V
f_{sw}	50 kHz
L_{Buck}	55 µH
Δv_{OUT}	16.35 V
Δi_L	42.749 A

With these values, a minimum capacitance of $C_{OUT,min} = 6.537\,\mu F$ is obtained, which is rounded of and increased to $C_{OUT} = 10\,\mu F$ to give some more margin. Note that a larger capacitor will only result in a smaller voltage ripple. The rest of the converter is modelled as an ideal current sources in order to simulate a constant load. With all major components dimensioned, a circuit model according to Figure 3.2 is setup in LTspice, see Figure 5.3 for schematic and Table 5.3 for circuit symbol explanation.

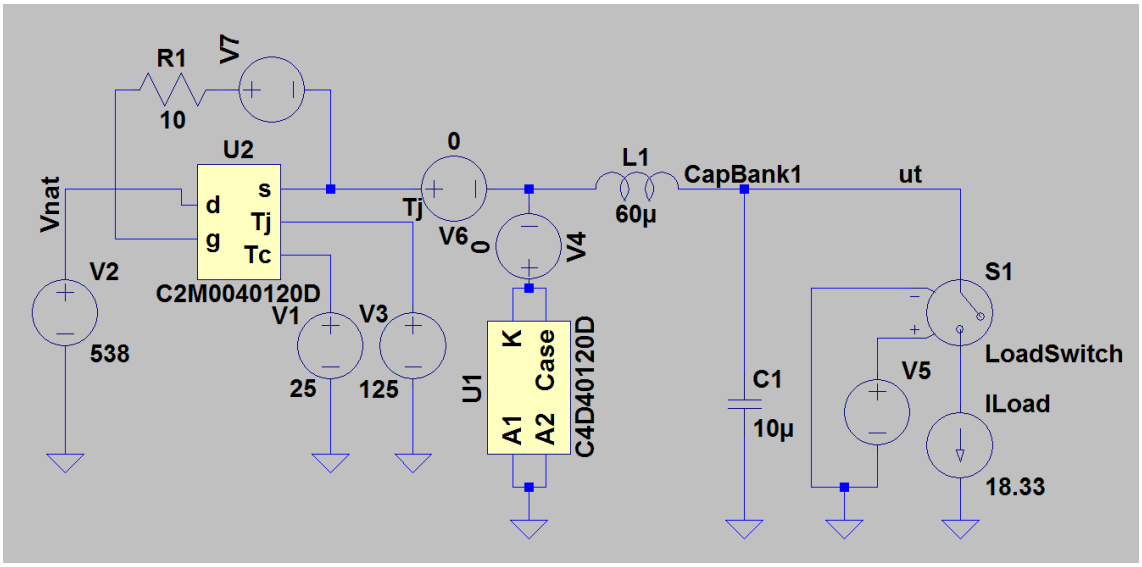


Figure 5.3: LTspice schematic of buck converter.

Table 5.3: Buck converter LTspice schematic symbol description.

Symbol name	Description	Value
V2	Equivalent rectified DC voltage source	538 V
V7	Pulse voltage source for PWM	−5 V to 20 V
V1, V3	DC voltage sources for temperature control of MOSFET	25 V, 125 V
V4, V6	0 V voltage sources for current tracing	0 V
V5	Step voltage source for control of load switch	N/A
S1	Load switch for connecting the load	N/A
ILoad	Simualted load as a current source	18.33 A, 24.44 A
U1	Diode model	N/A
U2	MOSFET model	N/A
L1	Inductor L_{Buck} with parallel resistance in model	55 µH
C1	Output capacitor C_{OUT}	10 µF

Each simulation was run for 50 ms to make sure that a steady state was reached, at 10 ms the load was connected. Between each simulation the duty cycle, load current and output capacitor voltage was adjusted to fit the corresponding case.

5.1.1 Simulation results

5.1.1.1 Case 1: 327 V

A plot of the output voltage can be seen in Figure 5.4, and a zoom of the curve at the 40 ms mark can be seen in Figure 5.5. A zoom of the inductor, diode and switch currents at the same 40 ms mark can be seen in Figures 5.6 and 5.7 respectively. A summation of average and RMS values from the simulation and calculated values can be found in Table 5.4. The calculated values are calculated using the case operating values (L_{Buck}, f_{sw}, V_{IN}, V_{OUT}, I_{OUT}, P_{OUT}) applied to the corresponding equations in Table 3.1.

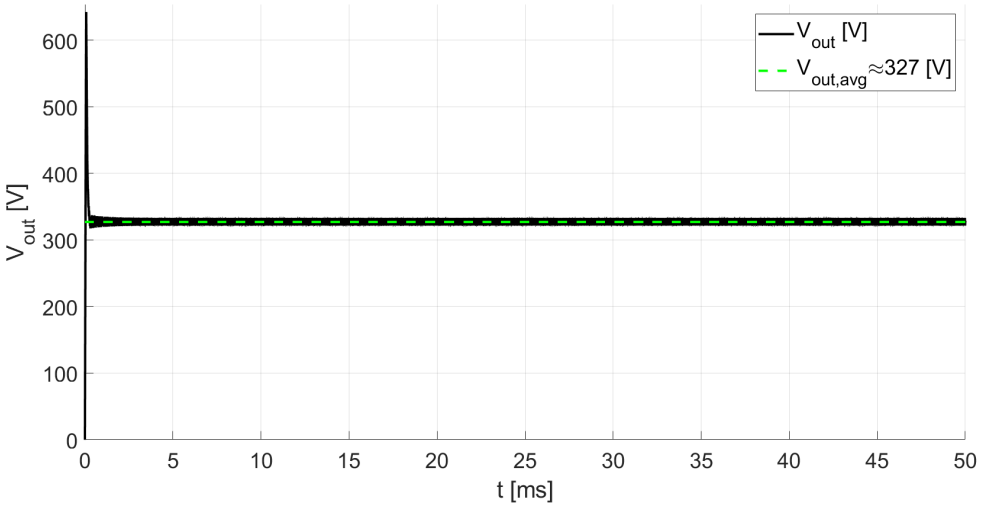


Figure 5.4: Simulated output voltage V_{OUT} from the buck converter power stage operating at 327 V with corresponding average value $V_{OUT,avg}$.

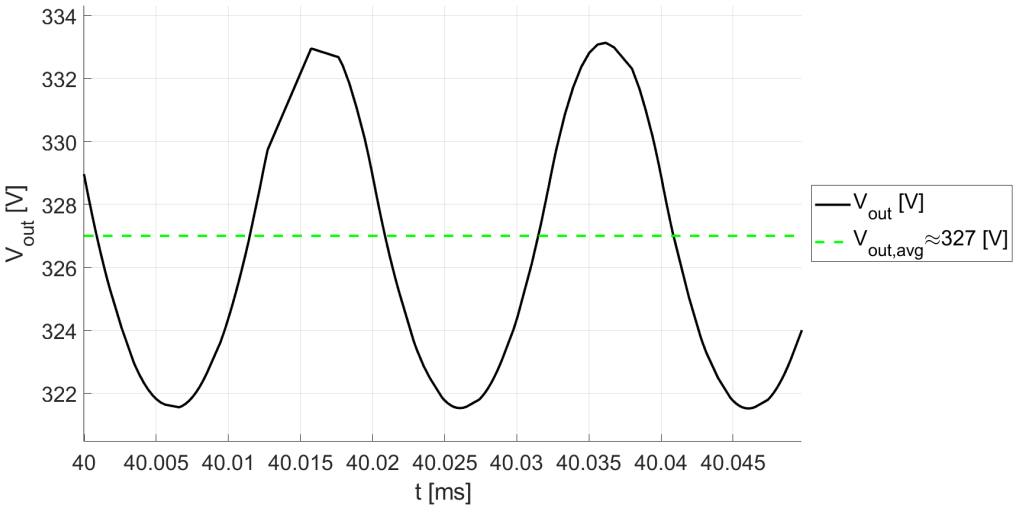


Figure 5.5: Zoom at 40 ms of simulated output voltage V_{OUT} from the buck converter power stage operating at 327 V with corresponding average value $V_{OUT,avg}$.

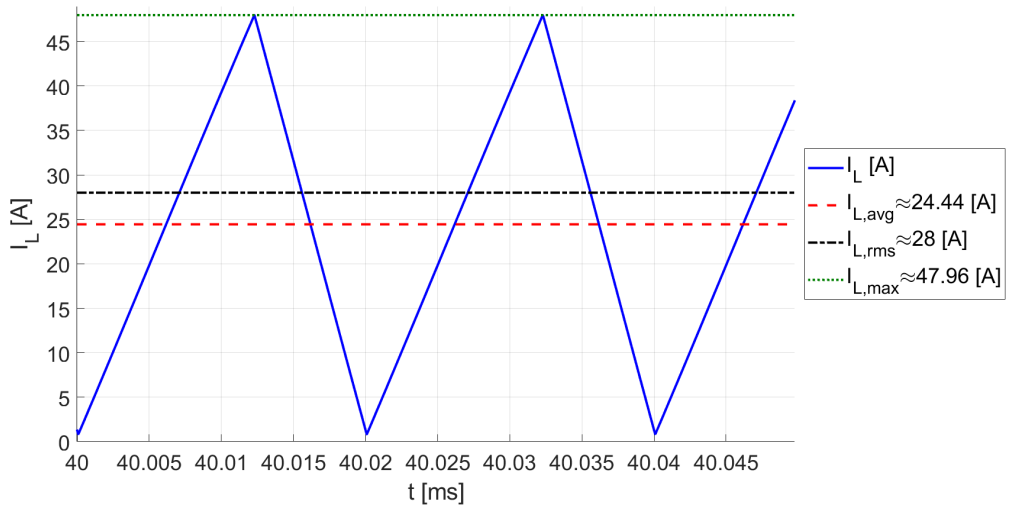


Figure 5.6: Zoom at 40 ms of simulated inductor current i_L from the buck converter power stage operating at 327 V with corresponding average and rms values $i_{L,avg}$ and $i_{L,rms}$.

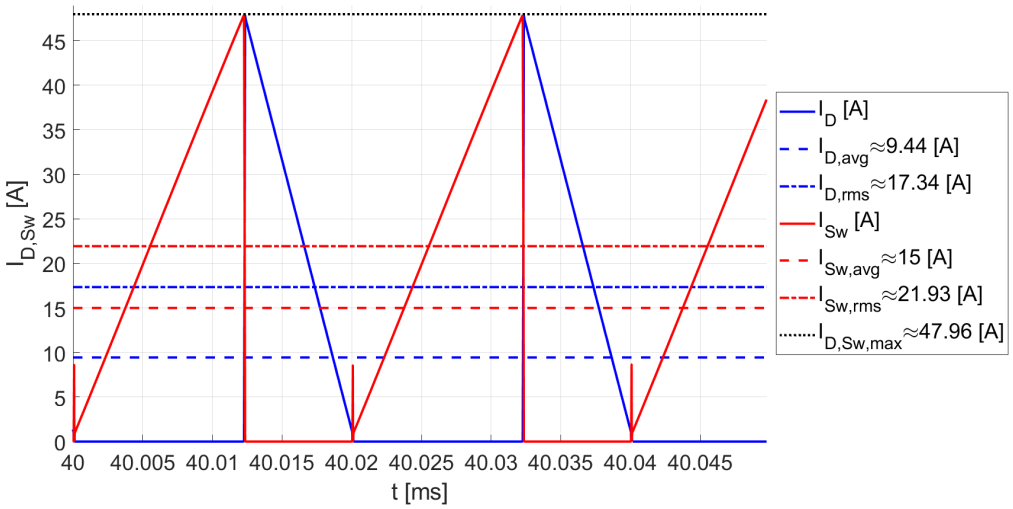


Figure 5.7: Zoom at 40 ms of simulated diode and switch current i_D and i_{Sw}, from the buck converter power stage operating at 327 V with corresponding average and rms values $i_{D,avg}$, $i_{D,rms}$, $i_{Sw,avg}$ and $i_{Sw,rms}$.

Table 5.4: Summation on values from simulation case 1

Property	Sim. Value	Calc. Value
$i_{L,avg}$	24.44 A	24.44 A
$i_{L,rms}$	28.00 A	27.97 A
$i_{D,avg}$	9.44 A	9.58 A
$i_{D,rms}$	17.34 A	17.52 A
$i_{Sw,avg}$	15.00 A	14.85 A
$i_{Sw,rms}$	21.93 A	21.81 A
$i_{L,D,Sw,max}$	47.96 A	47.76 A

5.1.1.2 Case 2: 368 V

A plot of the output voltage can be seen in Figure 5.8, and a zoom of the curve at the 40 ms mark can be seen in Figure 5.9. A zoom of the inductor, diode and switch currents at the same 40 ms mark can be seen in Figures 5.10 and 5.11 respectively. A summation of average and RMS values from the simulation and calculated values can be found in Table 5.5. The calculated values are calculated using the case operating values (L_{Buck}, f_{sw}, V_{IN}, V_{OUT}, I_{OUT}, P_{OUT}) applied to the corresponding equations in Table 3.1.

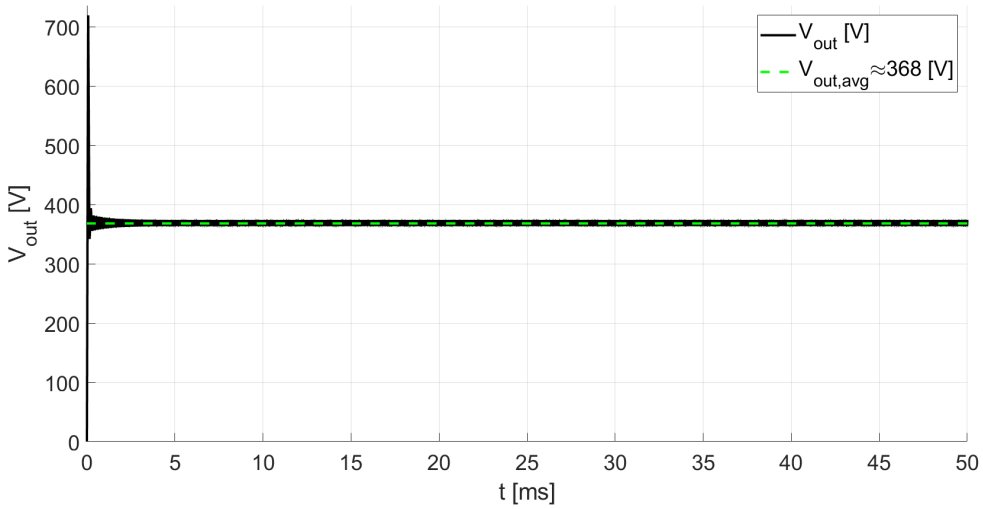


Figure 5.8: Simulated output voltage V_{OUT} from the buck converter power stage operating at 368 V with corresponding average value $V_{OUT,avg}$.

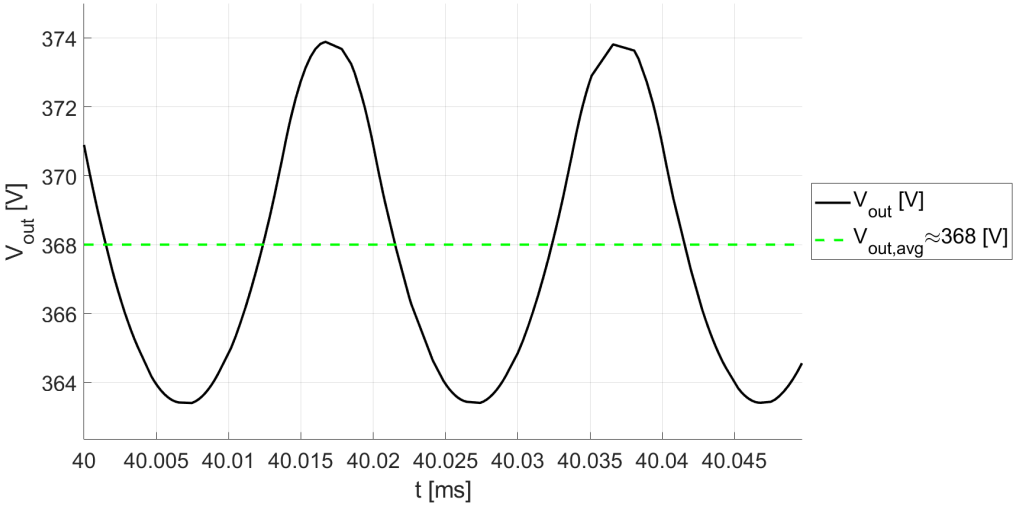


Figure 5.9: Zoom at 40 ms of simulated output voltage V_{OUT} from the buck converter power stage operating at 368 V with corresponding average value $V_{OUT,avg}$.

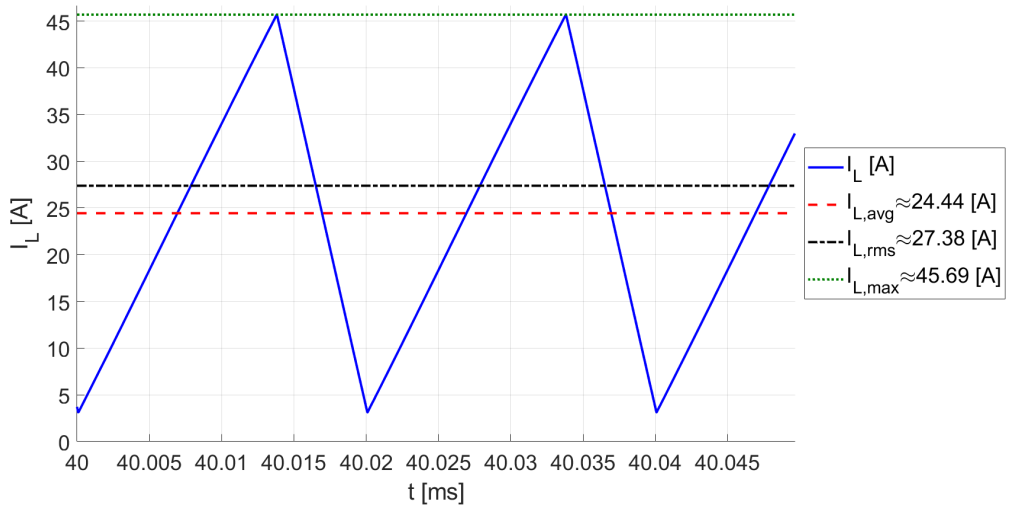


Figure 5.10: Zoom at 40 ms of simulated inductor current i_L from the buck converter power stage operating at 368 V with corresponding average and rms values $i_{L,avg}$ and $i_{L,rms}$.

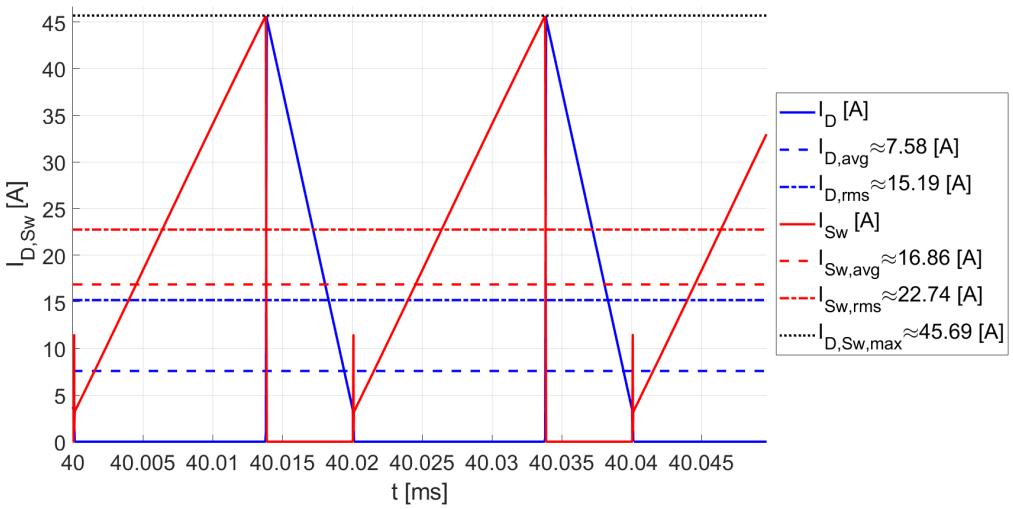


Figure 5.11: Zoom at 40 ms of simulated diode and switch current i_D and i_{Sw}, from the buck converter power stage operating at 368 V with corresponding average and rms values $i_{D,avg}$, $i_{D,rms}$, $i_{Sw,avg}$ and $i_{Sw,rms}$.

Table 5.5: Summation on values from simulation case 2

Property	Sim. Value	Calc. Value
$i_{L,avg}$	24.44 A	24.44 A
$i_{L,rms}$	27.38 A	27.35 A
$i_{D,avg}$	7.58 A	7.72 A
$i_{D,rms}$	15.19 A	15.38 A
$i_{Sw,avg}$	16.86 A	16.72 A
$i_{Sw,rms}$	22.74 A	22.62 A
$i_{L,D,Sw,max}$	45.69 A	45.58 A

5.1.1.3 Case 3: 491 V

A plot of the output voltage can be seen in Figure 5.12, and a zoom of the curve at the 40 ms mark can be seen in Figure 5.13. A zoom of the inductor, diode and switch currents at the same 40 ms mark can be seen in Figures 5.14 and 5.15 respectively. A summation of average and RMS values from the simulation and calculated values can be found in Table 5.6. The calculated values are calculated using the case operating values (L_{Buck}, f_{sw}, V_{IN}, V_{OUT}, I_{OUT}, P_{OUT}) applied to the corresponding equations in Table 3.1.

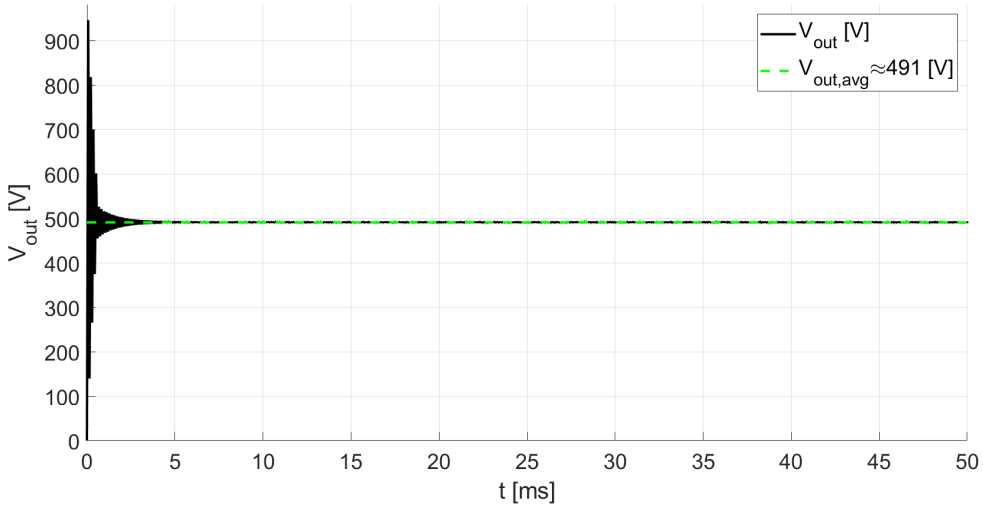


Figure 5.12: Simulated output voltage V_{OUT} from the buck converter power stage operating at 491 V with corresponding average value $V_{OUT,avg}$.

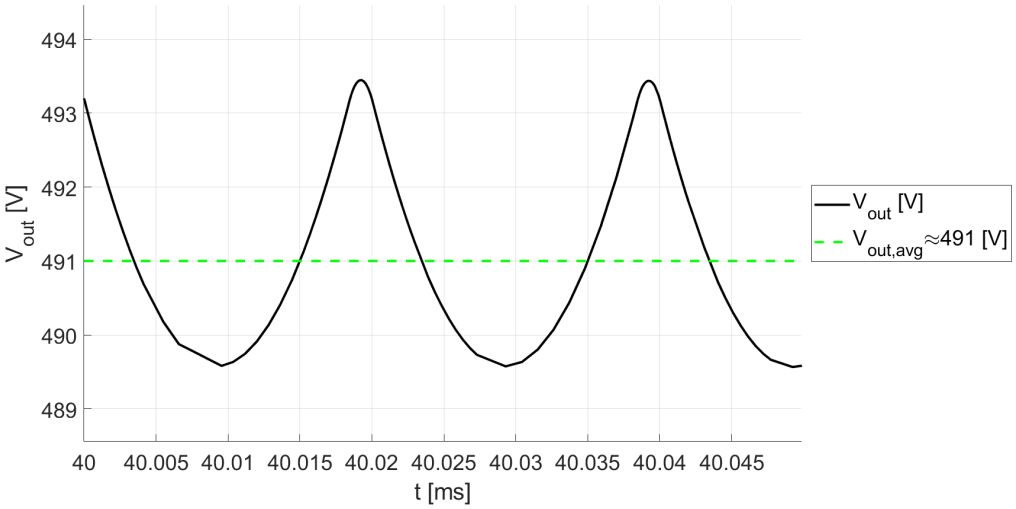


Figure 5.13: Zoom at 40 ms of simulated output voltage V_{OUT} from the buck converter power stage operating at 368 V with corresponding average value $V_{OUT,avg}$.

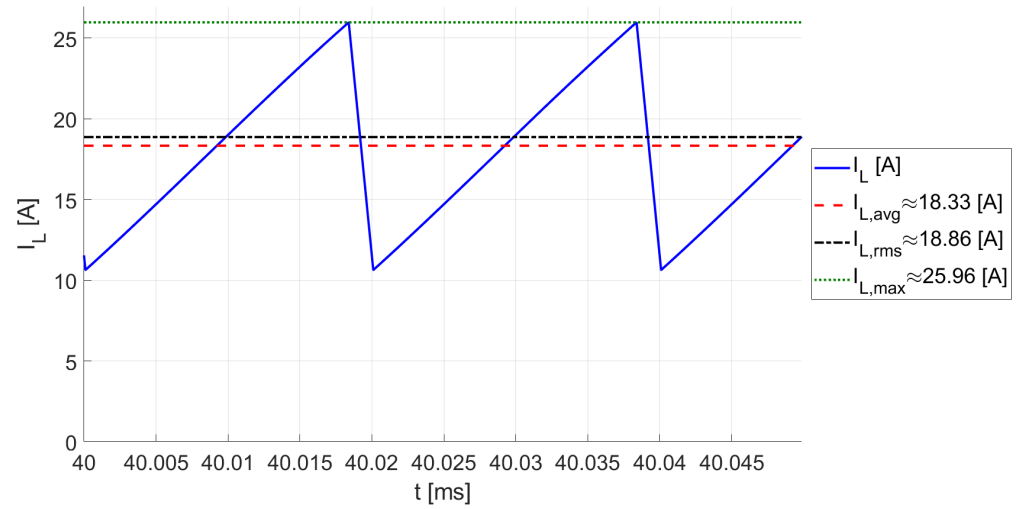


Figure 5.14: Zoom at 40 ms of simulated inductor current i_L from the buck converter power stage operating at 491 V with corresponding average and rms values $i_{L,avg}$ and $i_{L,rms}$.

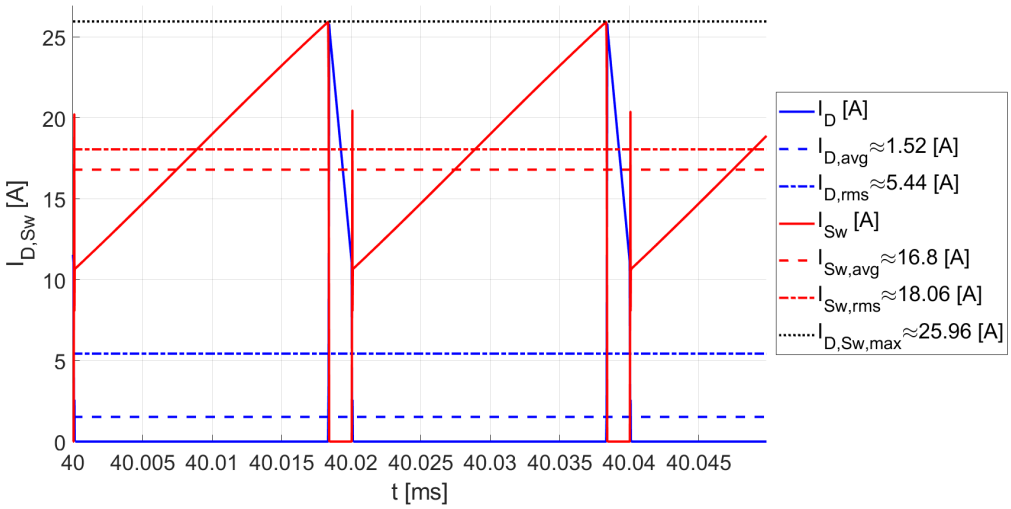


Figure 5.15: Zoom at 40 ms of simulated diode and switch current i_D and i_{Sw}, from the buck converter power stage operating at 491 V with corresponding average and rms values $i_{D,avg}$, $i_{D,rms}$, $i_{Sw,avg}$ and $i_{Sw,rms}$.

Table 5.6: Summation on values from simulation case 3

Property	Sim. Value	Calc. Value
$i_{L,avg}$	18.33 A	18.33 A
$i_{L,rms}$	18.86 A	18.85 A
$i_{D,avg}$	1.52 A	1.60 A
$i_{D,rms}$	5.44 A	5.57 A
$i_{Sw,avg}$	16.80 A	16.73 A
$i_{Sw,rms}$	18.06 A	18.01 A
$i_{L,D,Sw,max}$	25.96 A	26.13 A

5.1.2 Active component losses in buck converter

The relevant voltages and currents needed to calculate losses in the buck converter can be found in Tables 5.1, 5.4, 5.5 and 5.6. The switching losses for the buck converter is calculated using these values for voltage and current and (3.49). The conduction losses in the buck MOSFET are calculated using simulated values for the RMS current through the switch and (3.55), and the conduction losses in the buck diode are calculated using (3.56). The results of the loss calculations for the buck converter are listed in Table 5.7.

Table 5.7: Component losses for the buck converter at all operating points

Loss type	Op. point 1	Op. point 2	Op. point 3
Buck MOSFET, conduction	40.40 W	43.44 W	27.40 W
Buck MOSFET, switching	28.27 W	28.27 W	21.20 W
Buck diode, conduction	20.77 W	16.68 W	3.34 W

5.2 Boost simulations

For the boost simulation model, most of the components from the buck circuit were reused. Semiconductor components, switching frequency and the parallel resistor for the inductor were all the same. That leaves the inductor and output capacitor in need to be re-dimensioned to fit the boost converter power stage. The inductor size re-calculation was done in a similar manner to the buck. Applying Section 2.2.1 and above, into (3.9), the minimum inductance value needed to keep CCM for this boost setup was calculated and plotted in Figure 5.16. In the plot, maximum power output with the 20 A charger output current limit is assumed over the whole voltage range.

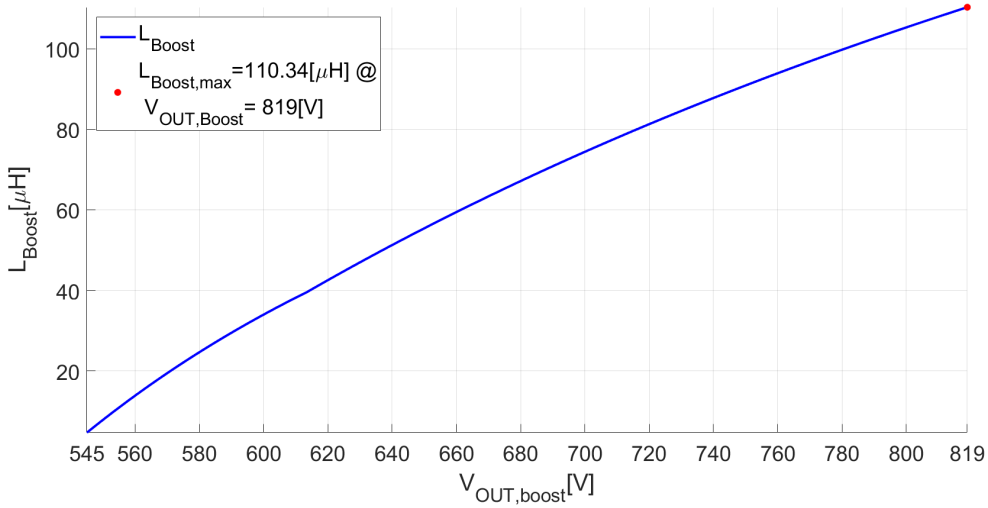


Figure 5.16: Plot of minimum inductance needed for CCM operation dependent on output voltage with maximum power output and charger current limitation.

The minimum value needed to achieve CCM operation over the whole voltage range at max power and current output become $L_{Boost} = 110.34\,\mu H$. Similarly to the buck, the scenario where the charging current is reduced is also of interest for the boost setup. With the output voltage locked to the minimum value (blue line in Figure 5.17) and maximum value (red line in Figure 5.17) and sweeping the output current from the maximum charge current down to 0 in (3.9), the minimum inductance was calculated and plotted in Figure 5.17.

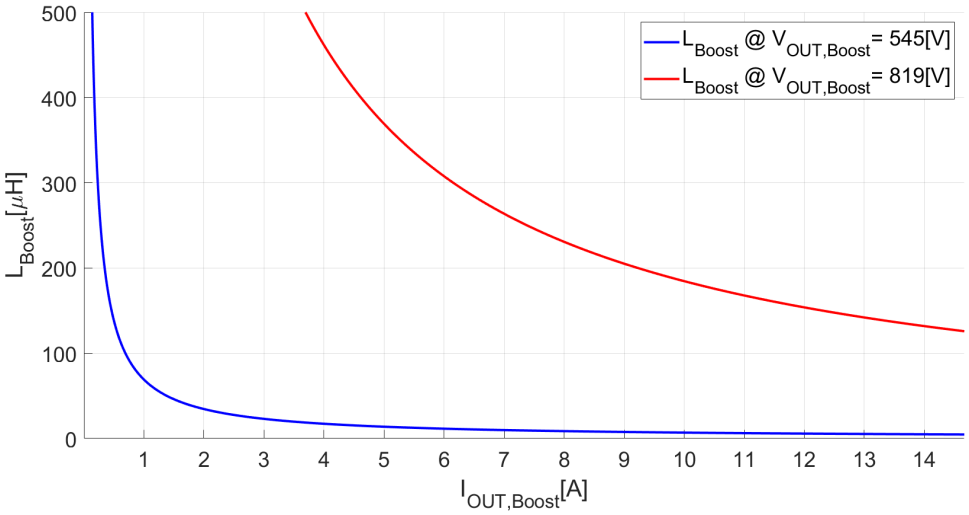


Figure 5.17: Plot of minimum inductance needed for CCM operation dependent on output current with the maximum (red) and minimum (blue) output voltage locked.

All other output voltages cases will become lines between the two lines in the plot. The same event as for the buck happens, as $I_{OUT,Boost}$ is linearly related to the denominator in (3.9), as it tends towards 0, the inductance $L_{Boost} \rightarrow \infty$. Therefore, as for the buck, it will be impossible to keep the operation mode to CCM for low output currents, regardless of inductor size. If the output current is reduced below any of the change-over points, the converter will switch mode of operation to DCM and subsequently change operational dynamics. In all cases, a large inductor is preferable for keeping CCM operation for as low output currents as possible.

To simulate component stresses and get data for loss calculations on switch and diode, the high power operating points are chosen to be simulated. Three operating cases were chosen, see Table 5.8 for case summation. These correspond to the minimum output voltage (Case 1), charger current limitation change over point (Case 2) and maximum output voltage (Case 3). To make sure to get CCM operation in all of the cases, an inductor of 120 µH is chosen, to have some margin to the minimum value mentioned in the previous paragraph.

Table 5.8: Boost converter operating points for component stress simulation cases

Case	Output voltage	Output current	Output power
1	545 V	14.67 A	7.993 kW
2	614 V	14.67 A	9 kW
3	819 V	10.99 A	9 kW

The minimum output capacitor value can be calculated in a similar manner to the buck converter. The same voltage ripple goal is set to 5% of the output voltage, but the rest needs to be adjusted. The worst output voltage ripple case is the highest output voltage operating point. Using the voltage-current relation for a capacitor

together with the defined voltage ripple, the capacitor current waveform seen in Figure 3.15 and the peak-to-peak inductor current (i.e applying the inductor size and operating point to (3.8)), see Table 5.9 for summation of values, the smallest capacitance value can be calculated as

$$\begin{aligned} \Delta v_{OUT} = \frac{Q_c}{C} \Rightarrow \begin{bmatrix} Q_c = I_{out}DT \\ \Delta v_{OUT} \leq 0.05 \cdot V_{OUT} \end{bmatrix} \Rightarrow 0.05 \cdot V_{OUT} \geq \frac{I_{out}DT}{C} \Rightarrow \\ 0.05 \cdot V_{OUT} \geq \frac{I_{OUT}(1 - \frac{V_{IN}}{V_{OUT}})}{Cf_{sw}} \Rightarrow C \geq \frac{I_{OUT}(1 - \frac{V_{IN}}{V_{OUT}})}{0.05 \cdot V_{OUT} f_{sw}}. \end{aligned} \tag{5.2}$$

Table 5.9: Summation of values for calculation of output capacitor size for Boost converter simulation.

Property	Value
V_{OUT}	819 V
V_{IN}	538 V
Δv_{OUT}	40.95 V
I_{OUT}	10.99 A
f_{sw}	50 kHz

With these values, a minimum capacitance of $C_{OUT,min} = 1.842\,\mu F$ is obtained, which is rounded up and increased to $C_{OUT} = 2\,\mu F$ to give some more margin. Note that a larger capacitor will only result in a smaller voltage ripple. The rest of the converter is modelled as an ideal current sources in order to simulate a constant load. With all major components dimensioned, a circuit model according to Figure 3.9 is setup in LTspice, see Figure 5.18 for schematic and Table 5.10 for circuit symbol explanation.

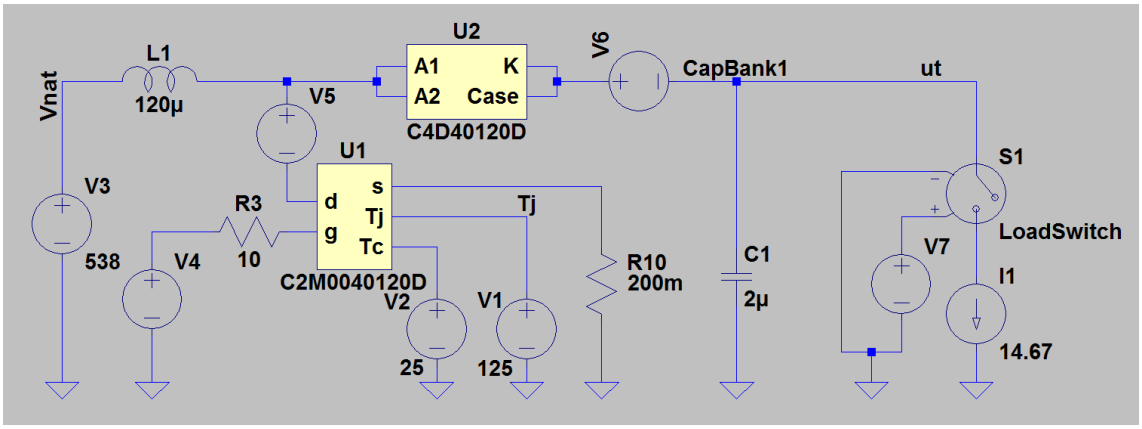


Figure 5.18: LTspice schematic of boost converter.

Table 5.10: Boost converter LTspice schematic symbol description.

Symbol	Description	Value
V3	Equivalent rectified DC voltage source	538 V
V4	Pulse voltage source for PWM	−5 V to 20 V
V1, V2	DC voltage sources for temperature control of MOSFET	25 V, 125 V
V5, V6	0 V voltage voltage sources for current tracing	0 V
V7	Step voltage source for control of load switch	N/A
S1	Load switch for connecting the load	N/A
I1	Simulated load as a current source	10.99 A, 14.67 A
U1	Diode model	N/A
U2	MOSFET model	N/A
L1	Inductor with parallel resistance in model	120 µH
C1	Output capacitor	2 µF

Each simulation was run for 50 ms to make sure that a steady state was reached, at 10 ms the load was connected. Between each simulation the duty cycle, load current and output capacitor voltage was adjusted to fit the corresponding case.

5.2.1 Simulations

5.2.1.1 Case 1: 545 V

A plot of the output voltage can be seen in Figure 5.19, and a zoom of the curve at the 40 ms mark can be seen in Figure 5.20. A zoom of the inductor, diode and switch currents at the same 40 ms mark can be seen in Figures 5.21 and 5.22 respectively. A summation of average and RMS values from the simulation and calculated values can be found in Table 5.11. The calculated values are calculated using the case operating values (L_{Boost}, f_{sw}, V_{IN}, V_{OUT}, I_{IN}, P_{OUT}) applied to the corresponding equations in Table 3.2.

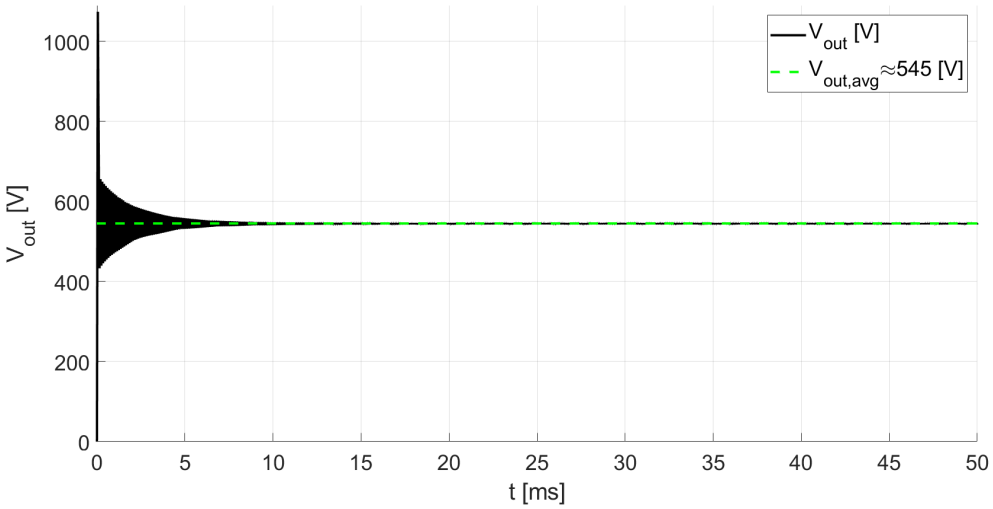


Figure 5.19: Simulated output voltage V_{OUT} from the boost converter power stage operating at 545 V with corresponding average value $V_{OUT,avg}$.

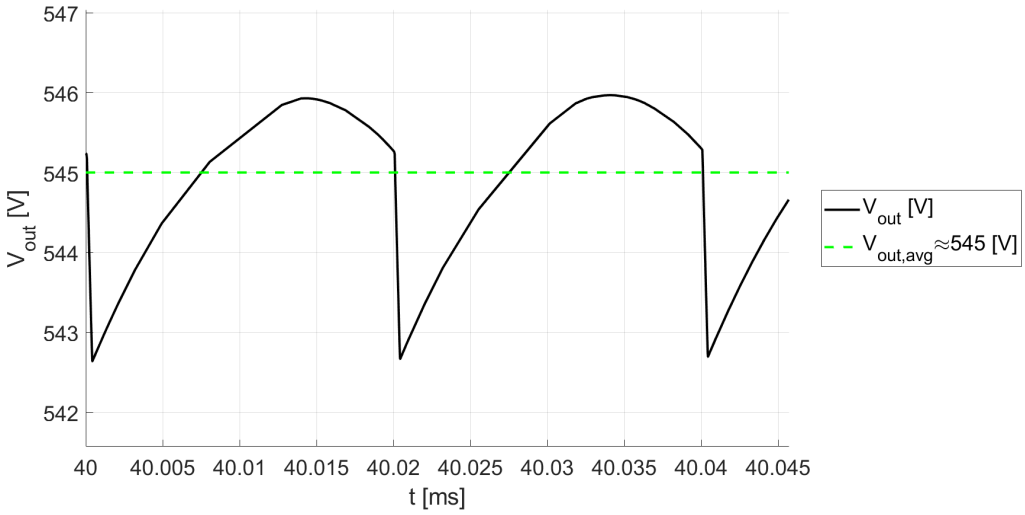


Figure 5.20: Zoom at 40 ms of simulated output voltage V_{OUT} from the boost converter power stage operating at 545 V with corresponding average value $V_{OUT,avg}$.

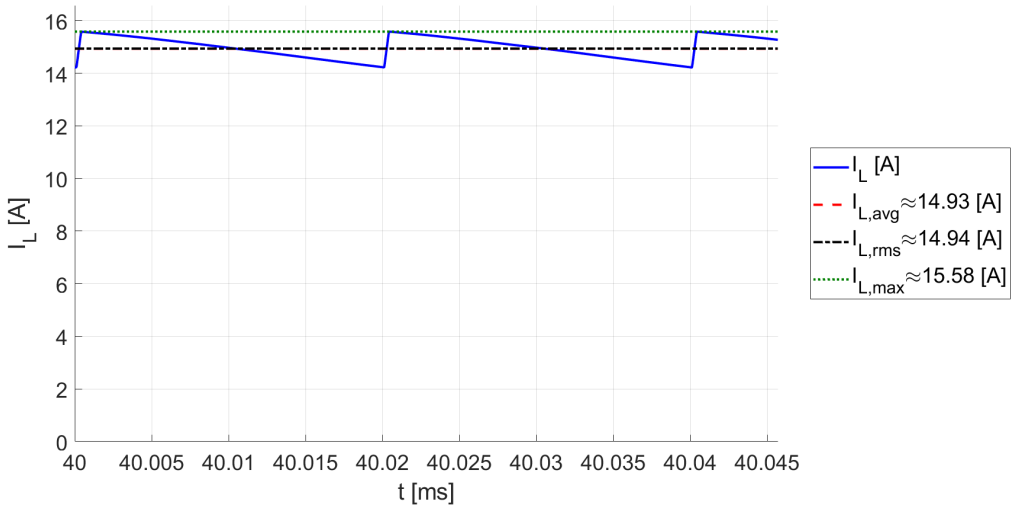


Figure 5.21: Zoom at 40 ms of simulated inductor current i_L from the boost converter power stage operating at 545 V with corresponding average and rms values $i_{L,avg}$ and $i_{L,rms}$.

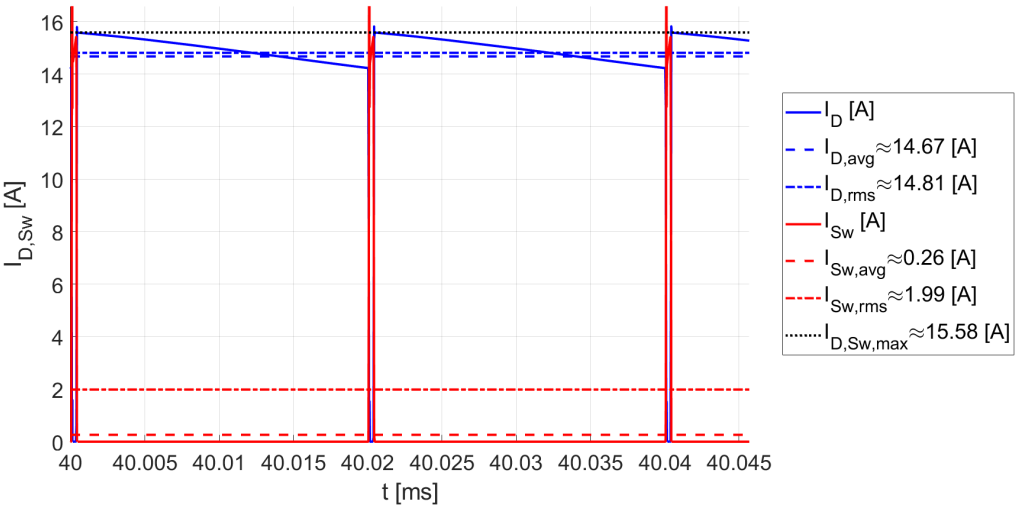


Figure 5.22: Zoom at 40 ms of simulated diode and switch current i_D and i_{Sw}, from the boost converter power stage operating at 545 V with corresponding average and rms values $i_{D,avg}$, $i_{D,rms}$, $i_{Sw,avg}$ and $i_{Sw,rms}$.

Table 5.11: Summation on values from simulation case 1

Property	Sim. Value	Calc. Value
$i_{L,avg}$	14.93 A	14.86 A
$i_{L,rms}$	14.94 A	14.94 A
$i_{D,avg}$	14.67 A	14.67 A
$i_{D,rms}$	14.81 A	14.84 A
$i_{Sw,avg}$	0.26 A	0.19 A
$i_{Sw,rms}$	1.99 A	1.69 A
$i_{L,D,Sw,max}$	15.59 A	15.43 A

5.2.1.2 Case 2: 614 V

A plot of the output voltage can be seen in Figure 5.23, and a zoom of the curve at the 40 ms mark can be seen in Figure 5.24. A zoom of the inductor, diode and switch currents at the same 40 ms mark can be seen in Figures 5.25 and 5.26 respectively. A summation of average and RMS values from the simulation and calculated values can be found in Table 5.12. The calculated values are calculated using the case operating values (L_{Boost}, f_{sw}, V_{IN}, V_{OUT}, I_{IN}, P_{OUT}) applied to the corresponding equations in Table 3.2.

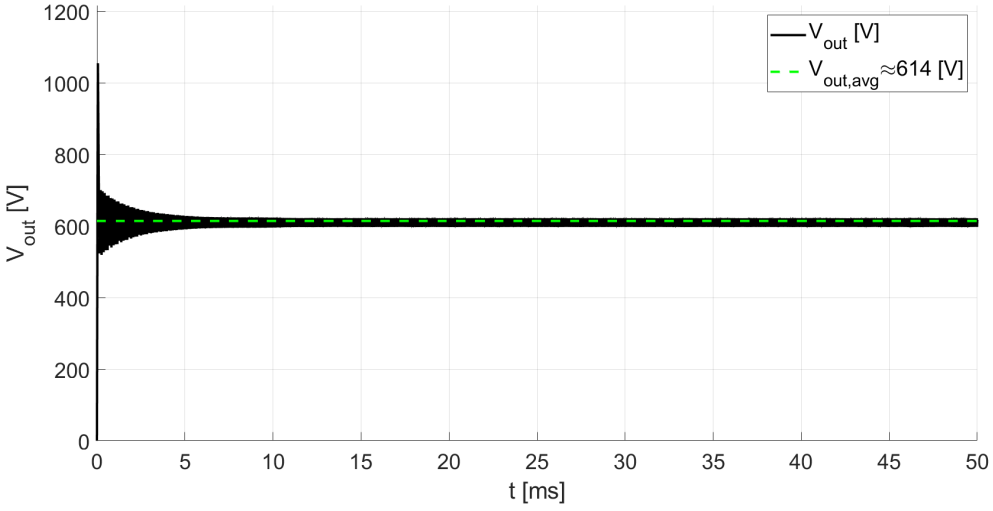


Figure 5.23: Simulated output voltage V_{OUT} from the boost converter power stage operating at 614 V with corresponding average value $V_{OUT,avg}$.

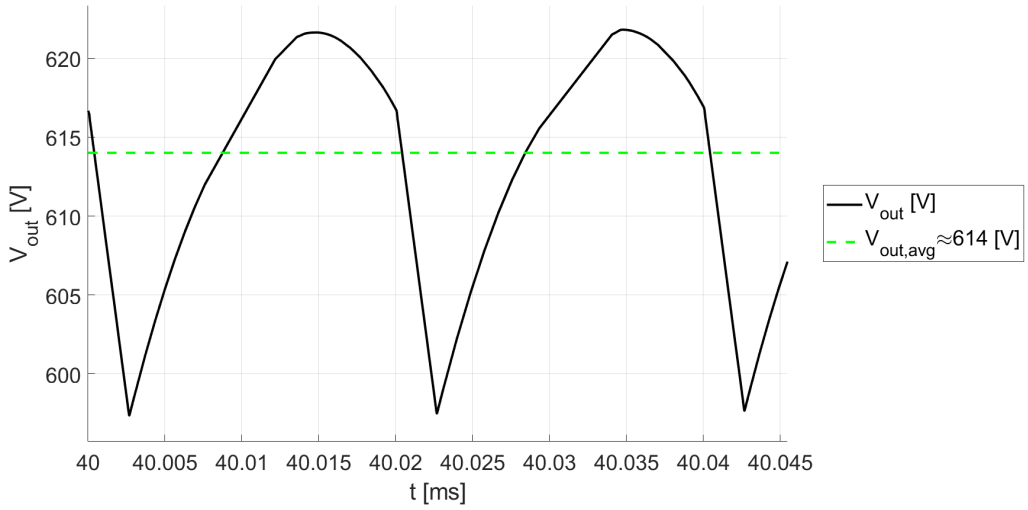


Figure 5.24: Zoom at 40 ms of simulated output voltage V_{OUT} from the boost converter power stage operating at 614 V with corresponding average value $V_{OUT,avg}$.

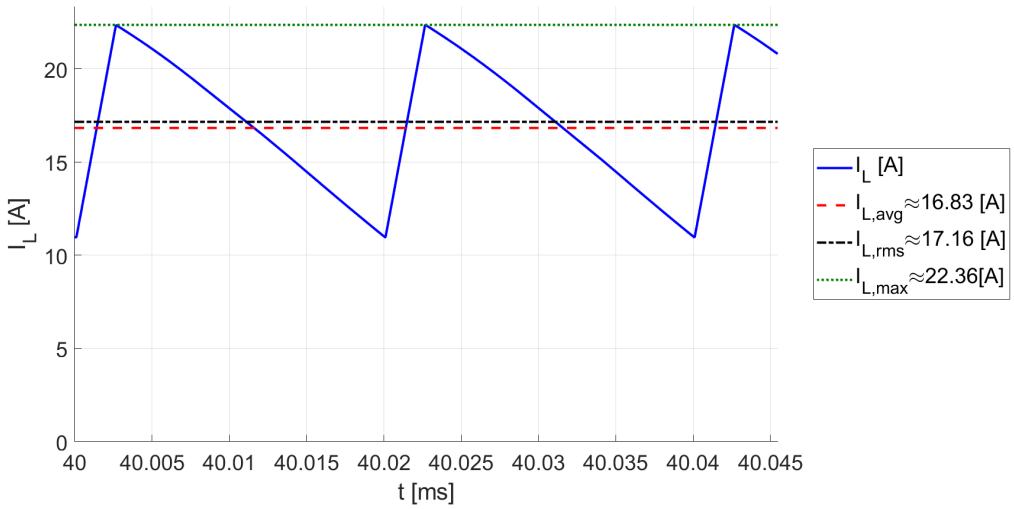


Figure 5.25: Zoom at 40 ms of simulated inductor current i_L from the boost converter power stage operating at 614 V with corresponding average and rms values $i_{L,avg}$ and $i_{L,rms}$.

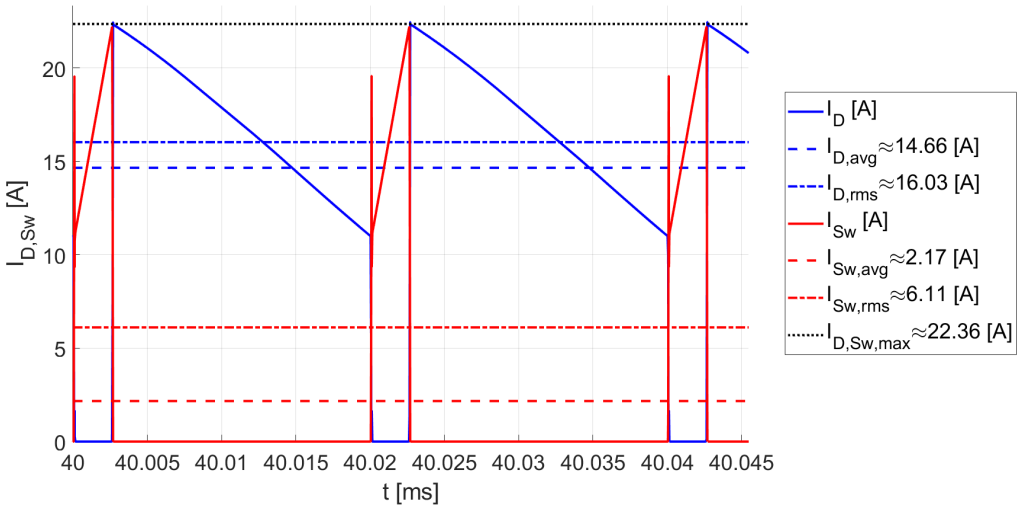


Figure 5.26: Zoom at 40 ms of simulated diode and switch current i_D and i_{Sw}, from the boost converter power stage operating at 614 V with corresponding average and rms values $i_{D,avg}$, $i_{D,rms}$, $i_{Sw,avg}$ and $i_{Sw,rms}$.

Table 5.12: Summation on values from simulation case 2

Property	Sim. Value	Calc. Value
$i_{L,avg}$	16.83 A	16.73 A
$i_{L,rms}$	17.16 A	17.05 A
$i_{D,avg}$	14.66 A	14.66 A
$i_{D,rms}$	16.03 A	15.96 A
$i_{Sw,avg}$	2.17 A	2.07 A
$i_{Sw,rms}$	6.11 A	6.00 A
$i_{L,D,Sw,max}$	22.43 A	22.28 A

5.2.1.3 Case 3: 819 V

A plot of the output voltage can be seen in Figure 5.27, and a zoom of the curve at the 40 ms mark can be seen in Figure 5.28. A zoom of the inductor, diode and switch currents at the same 40 ms mark can be seen in Figures 5.29 and 5.30 respectively. A summation of average and RMS values from the simulation and calculated values can be found in Table 5.13. The calculated values are calculated using the case operating values (L_{Boost}, f_{sw}, V_{IN}, V_{OUT}, I_{IN}, P_{OUT}) applied to the corresponding equations in Table 3.2.

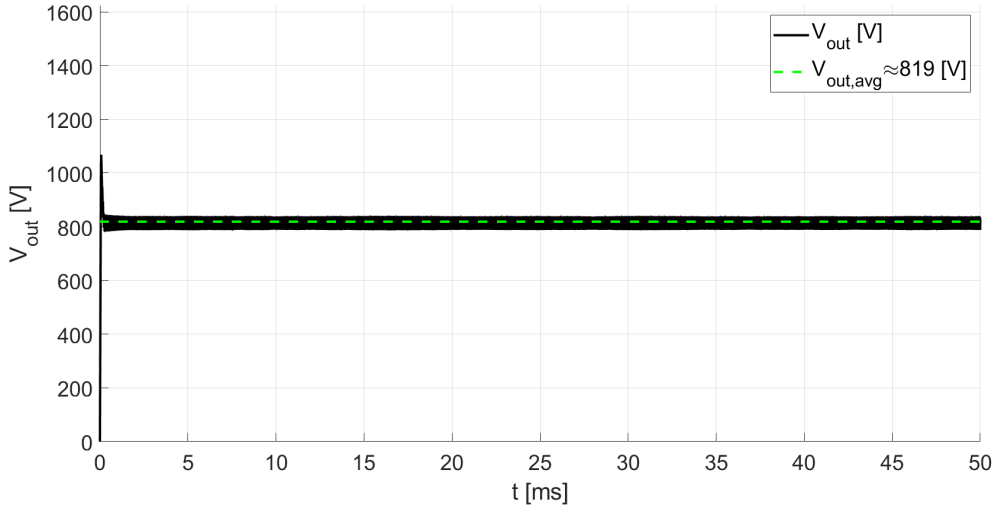


Figure 5.27: Simulated output voltage V_{OUT} from the boost converter power stage operating at 819 V with corresponding average value $V_{OUT,avg}$.

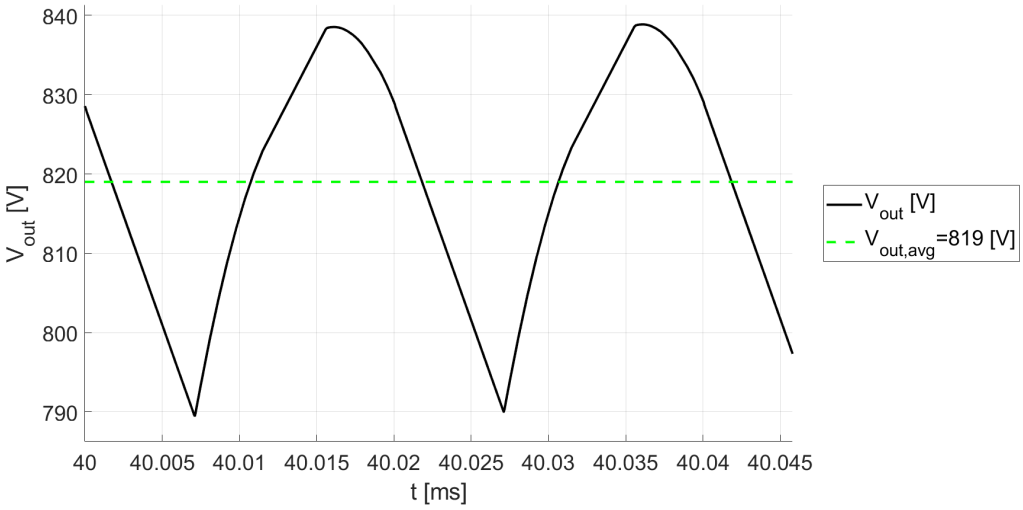


Figure 5.28: Zoom at 40 ms of simulated output voltage V_{OUT} from the boost converter power stage operating at 819 V with corresponding average value $V_{OUT,avg}$.

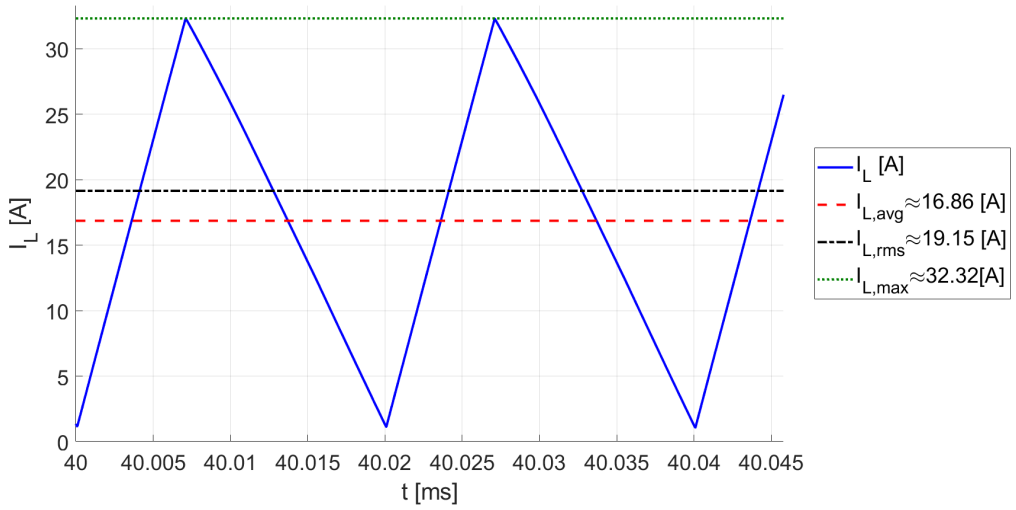


Figure 5.29: Zoom at 40 ms of simulated inductor current i_L from the boost converter power stage operating at 819 V with corresponding average and rms values $i_{L,avg}$ and $i_{L,rms}$.

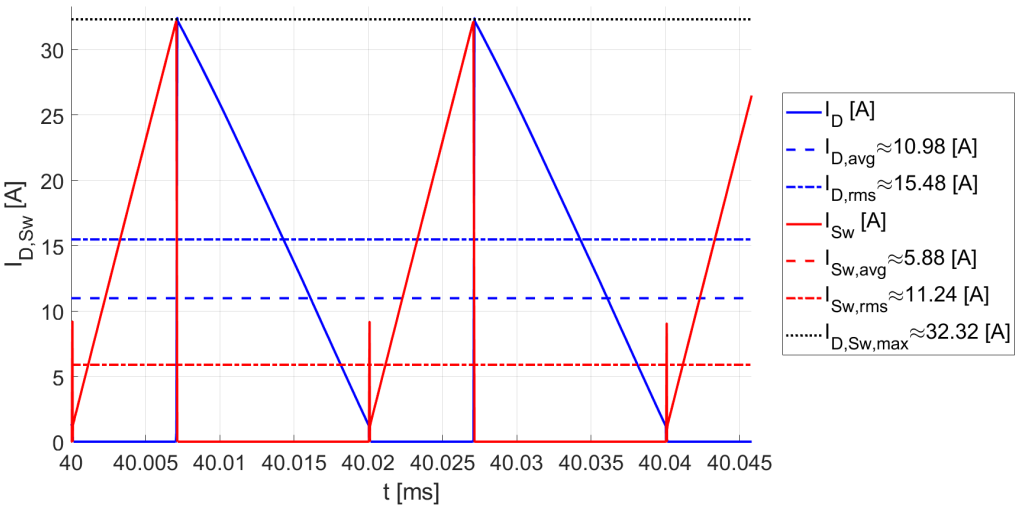


Figure 5.30: Zoom at 40 ms of simulated diode and switch current i_D and i_{Sw}, from the boost converter power stage operating at 819 V with corresponding average and rms values $i_{D,avg}$, $i_{D,rms}$, $i_{Sw,avg}$ and $i_{Sw,rms}$.

As seen from Tables 5.4, 5.5, 5.6, 5.11, 5.12 and 5.13, the calculated values are similar to the simulated values and it is therefore assumed that the simulation models are working accurately. The difference that is present is likely due to the active component losses modelled in the component models, which are assumed to be zero in the calculated values.

Table 5.13: Summation on values from simulation case 3

Property	Sim. Value	Calc. Value
$i_{L,avg}$	16.86 A	16.73 A
$i_{L,rms}$	19.15 A	19.01 A
$i_{D,avg}$	10.98 A	10.99 A
$i_{D,rms}$	15.48 A	15.41 A
$i_{Sw,avg}$	5.88 A	5.74 A
$i_{Sw,rms}$	11.24 A	11.13 A
$i_{L,D,Sw,max}$	32.32 A	32.11 A

5.2.2 Buck and Boost inductor

A difference between the buck converter power stage and the boost converter power stage which is worth noting for later design considerations is the peak current being pushed through the inductor. As the calculated values worked well in the previous sections, it was used as a base to calculate how the peak current is affected by inductor size.
With the worst case operating points for peak inductor current locked for each power stage and sweeping the inductance of the main inductor from the minimum value calculated in previous sections to 500 µH, the peak current is calculated and plotted in Figure 5.31. A summary of peak values at inductance intervals can be found in Table 5.14.

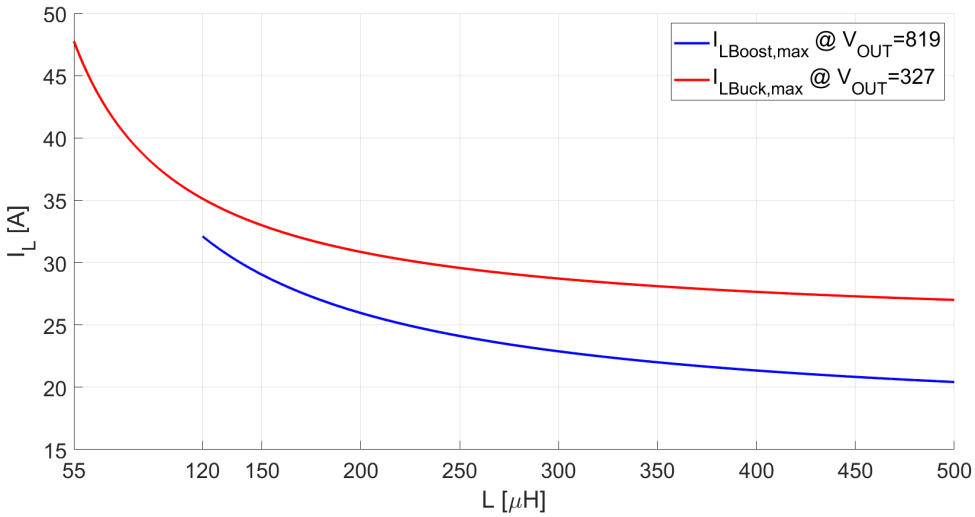


Figure 5.31: Plot of maximum inductor current dependent on inductor size given worst $i_{L,peak}$ case for buck and boost. Note the axis offsets and odd x-axis intervals.

The peak current is clearly lower across the board for the boost converter inductor. The lower peak will make the design of other current peak dependent components easier. Worth noting is that the RMS-value also follows the peaks trajectory, but is at a substantially lower level.

Table 5.14: Peak inductor current given inductor value per power stage converter

Inductance	**Buck** $i_{L,peak}$	**Boost** $i_{L,peak}$
55 µH	47.76 A	N/A
100 µH	37.27 A	N/A
120 µH	35.13 A	32.11 A
150 µH	32.99 A	29.03 A
200 µH	30.86 A	25.96 A
250 µH	29.57 A	24.11 A
300 µH	28.72 A	22.88 A
350 µH	28.11 A	22.00 A
400 µH	27.65 A	21.34 A
450 µH	27.29 A	20.83 A
500 µH	27.01 A	20.42 A

5.2.3 Active component losses in boost converter

The relevant voltages and currents needed to calculate losses in the boost converter can be found in Tables 5.8, 5.11, 5.12 and 5.13. The switching losses for the boost converter is calculated using these values for voltage and current and (3.50). The conduction losses in the boost MOSFET are calculated using simulated values for the RMS current through the switch and (3.55), and the conduction losses in the boost diode are calculated using (3.56). The results of the loss calculations for the boost converter are listed in Table 5.15.

Table 5.15: Component losses for the boost converter at all operating points

Loss type	Op. point 1	Op. point 2	Op. point 3
Boost MOSFET, conduction	0.33 W	3.14 W	10.61 W
Boost MOSFET, switching	17.49 W	22.21 W	29.69 W
Boost diode, conduction	32.27 W	32.25 W	24.16 W

5.3 LLC simulations

The simulation models of the two alternative LLC converters are built with Spice models of the components selected in Section 4.5 and values for the resonant elements and the transformer from Section 4.6. The LLC converter designed to work with a buck converter can be seen in Figure 5.32, and the one made for a boost converter in Figure 5.33.

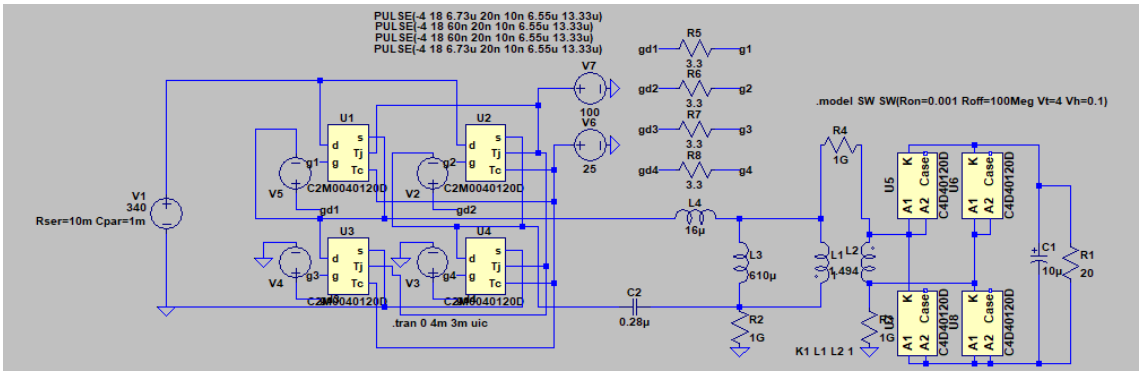


Figure 5.32: LTspice schematic of LLC converter designed for use with a buck converter

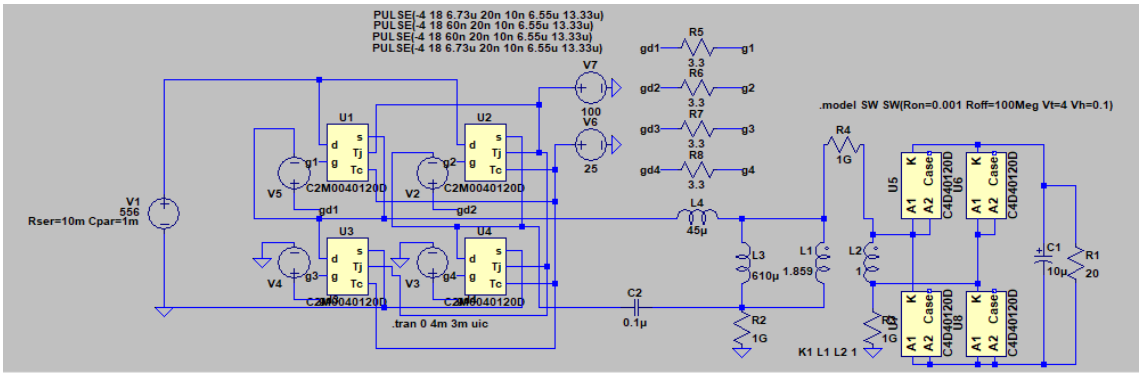


Figure 5.33: LTspice schematic of LLC converter designed for use with a boost converter.

To simplify and speed up the simulations, the input to the LLC converter is fed from an ideal DC voltage source instead of the actual primary stage converter. The gates of the simulated MOSFETs are also driven by such voltage sources (V2-V5) switching on and off with the chosen switching frequency of 75 kHz, and with small offsets added to their duty cycles to emulate the dead time of a real controller. Resistors R5-R8 are connected between the gate driving voltage sources and the gates (ports gd1-gd4 connect to the voltage sources, ports g1-g4 connect to the gates). The 1 GΩ resistors R2, R4 and R9 provide a high resistance path to ground for the floating stages and connect the two coils of the transformer. They are added for simulation flow reasons only and have a minimal impact on the simulated currents. Instead of a battery model, the load on the output is modelled as a simple resistor, as this makes it easy to adjust the output power. Three operating points are selected with respect to the output voltage and current:

- Operating point 1: 400 V, 20 A output
- Operating point 2: 450 V, 20 A output
- Operating point 3: 600 V, 15 A output

The aim of the LLC simulation is to compare calculated and simulated values for voltages and currents, especially with regards to the resonant circuit elements.

Due to the complexity of the model, each simulation was run for only 4 ms. Using the idealised input and resistive load this is more than enough to achieve steady state conditions. For each simulation, the input voltage was initially set to the buck and boost converter output voltage calculated in Sections 4.3 and 4.4 and then adjusted until the desired output voltage was reached.

5.4 LLC converter simulation results

The voltages and currents calculated in Section 4.6 are compared to simulated values in order to verify the simulations for all operating points.

Table 5.16: Comparison of calculated and simulated voltages and currents for the LLC converter designed for use with a buck converter for operating point 1.

Parameter	Sim. value	Calc. value
V_{IN}	340 VDC	327 VDC
I_{L_m}	1.04 A	1.03 A
I_{C_r}, I_{L_r}	27.2 A	27.17 A
V_{C_r}	205.9 V	206.6 V
V_{L_r}	206.7 V	204.9 V
$I_{switch,peak}$	38.54 A	38.42 A
$I_{switch,RMS}$	19.24 A	19.21 A
$I_{diode,peak}$	31.54 A	31.42 A
$I_{diode,RMS}$	15.73 A	15.71 A
I_{N_p}	27.23 A	27.15 A

Table 5.17: Comparison of calculated and simulated voltages and currents for the LLC converter designed for use with a buck converter for operating point 2.

Parameter	Sim. value	Calc. value
V_{IN}	381 VDC	368 VDC
I_{L_m}	1.17 A	1.15 A
I_{C_r}, I_{L_r}	27.21 A	27.17 A
V_{C_r}	206.0 V	206.7 V
V_{L_r}	207.5 V	204.9 V
$I_{switch,peak}$	38.57 A	38.43 A
$I_{switch,RMS}$	19.24 A	19.22 A
$I_{diode,peak}$	31.54 A	31.42 A
$I_{diode,RMS}$	15.73 A	15.71 A
I_{N_p}	27.24 A	27.15 A

Table 5.18: Comparison of calculated and simulated voltages and currents for the LLC converter designed for use with a buck converter for operating point 3.

Parameter	Sim. value	Calc. value
V_{IN}	501 VDC	491 VDC
I_{L_m}	1.56 A	1.54 A
I_{C_r}, I_{L_r}	20.44 A	20.42 A
V_{C_r}	154.7 V	155.3 V
V_{L_r}	158.8 V	154.0 V
$I_{switch,peak}$	29.0 A	28.88 A
$I_{switch,RMS}$	14.45 A	14.44 A
$I_{diode,peak}$	23.80 A	23.56 A
$I_{diode,RMS}$	11.83 A	11.78 A
I_{N_p}	20.40 A	20.36 A

Table 5.19: Comparison of calculated and simulated voltages and currents for the LLC converter designed for use with a boost converter for operating point 1.

Parameter	Sim. value	Calc. value
V_{IN}	556 VDC	545 VDC
I_{L_m}	1.73 A	1.71 A
I_{C_r}, I_{L_r}	16.38 A	16.38 A
V_{C_r}	347.2 V	347.6 V
V_{L_r}	347.7 V	347.3 V
$I_{switch,peak}$	23.19 A	23.16 A
$I_{switch,RMS}$	11.58 A	11.58 A
$I_{diode,peak}$	31.54 A	31.42 A
$I_{diode,RMS}$	15.73 A	15.71 A
I_{N_p}	16.33 A	16.29 A

Table 5.20: Comparison of calculated and simulated voltages and currents for the LLC converter designed for use with a boost converter for operating point 2.

Parameter	Sim. value	Calc. value
V_{IN}	624 VDC	614 VDC
I_{L_m}	1.95 A	1.92 A
I_{C_r}, I_{L_r}	16.39 A	16.40 A
V_{C_r}	347.5 V	348.1 V
V_{L_r}	348.1 V	347.8 V
$I_{switch,peak}$	23.21 A	23.20 A
$I_{switch,RMS}$	11.59 A	11.60 A
$I_{diode,peak}$	31.54 A	31.42 A
$I_{diode,RMS}$	15.73 A	15.71 A
I_{N_p}	16.33 A	16.29 A

Table 5.21: Comparison of calculated and simulated voltages and currents for the LLC converter designed for use with a boost converter for operating point 3.

Parameter	Sim. value	Calc. value
V_{IN}	826 VDC	819 VDC
I_{L_m}	2.59 A	2.56 A
I_{C_r}, I_{L_r}	12.45 A	12.48 A
V_{C_r}	264.0 V	264.9 V
V_{L_r}	267.8 V	264.7 V
$I_{switch,peak}$	17.66 A	17.65 A
$I_{switch,RMS}$	8.80 A	8.83 A
$I_{diode,peak}$	23.80 A	23.56 A
$I_{diode,RMS}$	11.83 A	11.78 A
I_{N_p}	12.26 A	12.22 A

It can be seen from Tables 5.16–5.21 that the simulated values do not differ much from the calculated values, and the simulation models are therefore assumed to work correctly. The small differences that do exist between the calculated and simulated values can be explained by the fact that some components are simulated as non-ideal, i.e the MOSFETs and diodes, as well as the slight reduction in actual duty cycle brought on by the need for dead-time between switching actions. Due to these imperfections in the simulation model, the input voltage needs to be increased slightly in order to achieve the desired output voltage. This higher input voltage results in additional deviations in voltages and currents when compared to the ideal case.

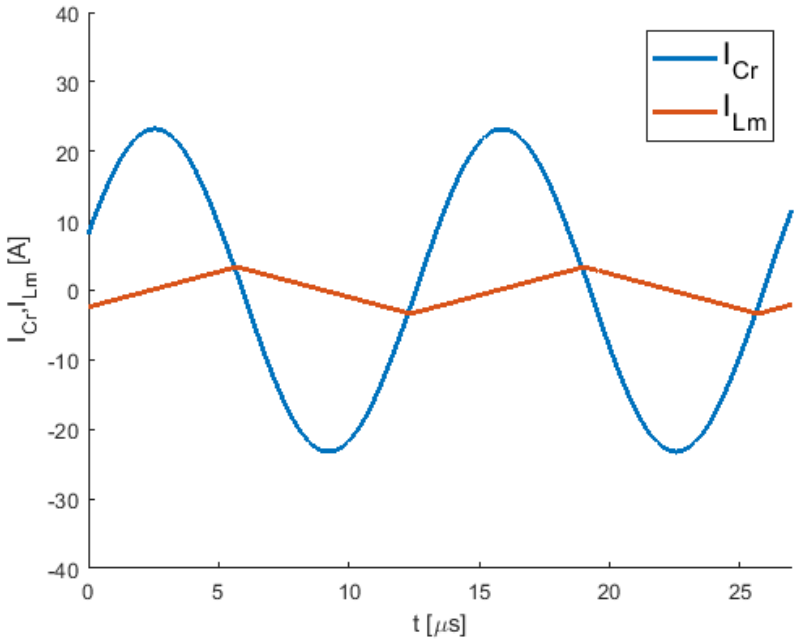


Figure 5.34: Simulated waveforms of I_{C_r} and I_{L_m} for the boost converter LLC at 450 V, 20 A output.

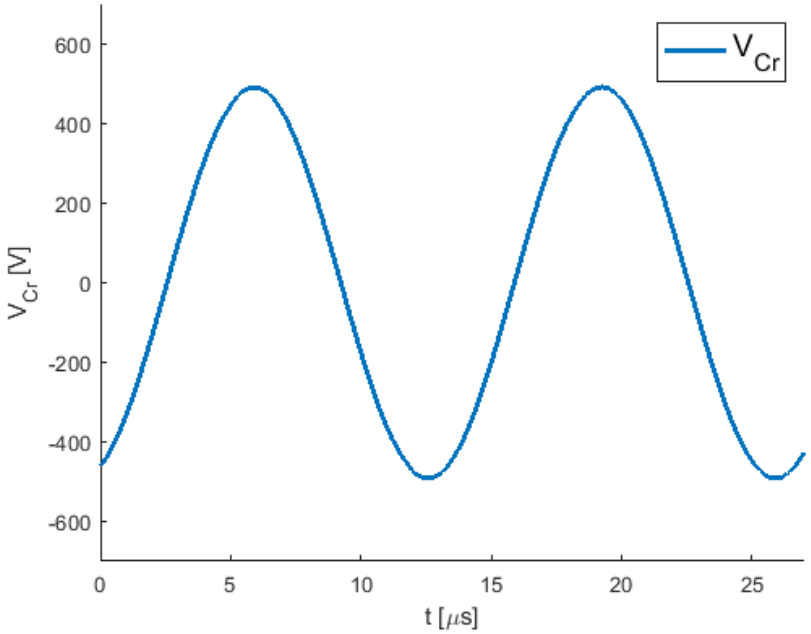


Figure 5.35: Simulated waveforms of V_{C_r} for the boost converter LLC at 450 V, 20 A output.

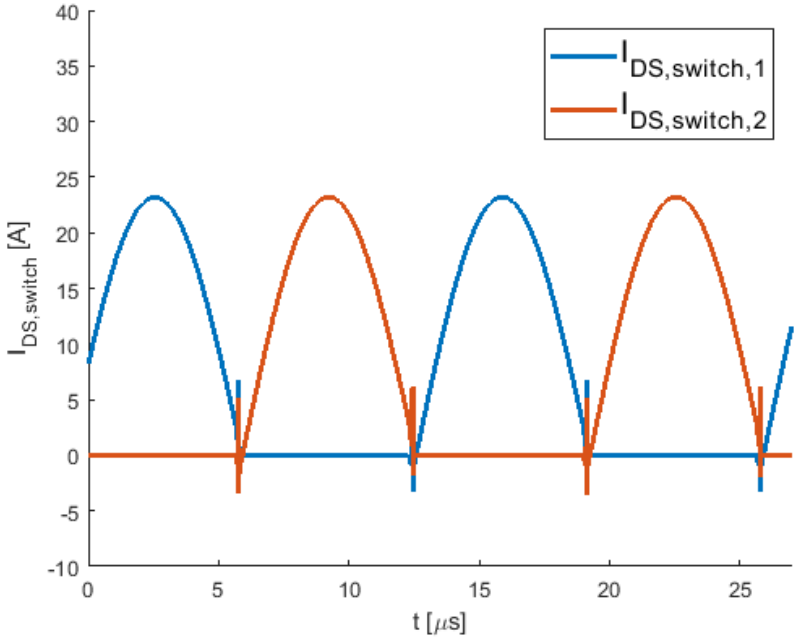


Figure 5.36: Simulated waveforms of $I_{switch,1}$ and $I_{switch,2}$ for the boost converter LLC at 450 V, 20 A output.

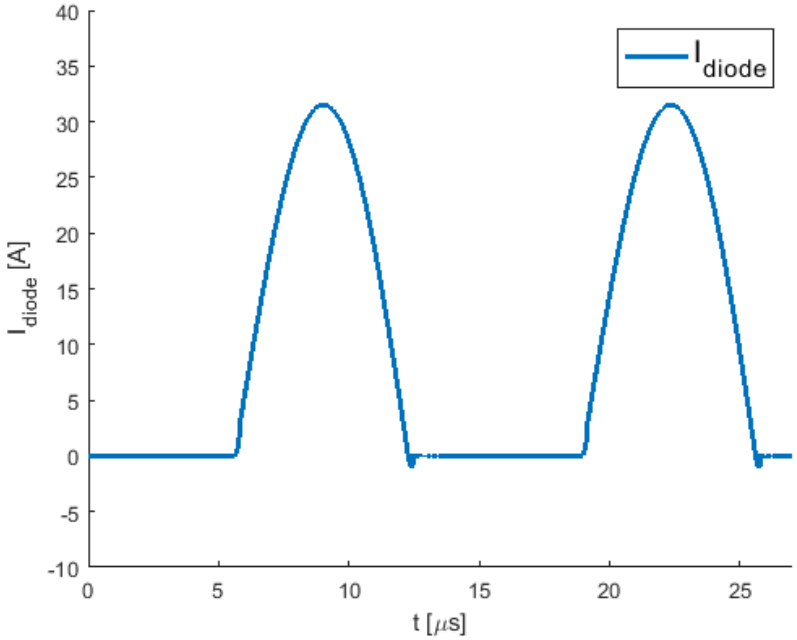


Figure 5.37: Simulated waveforms of I_{diode} for the boost converter LLC at 450 V, 20 A output.

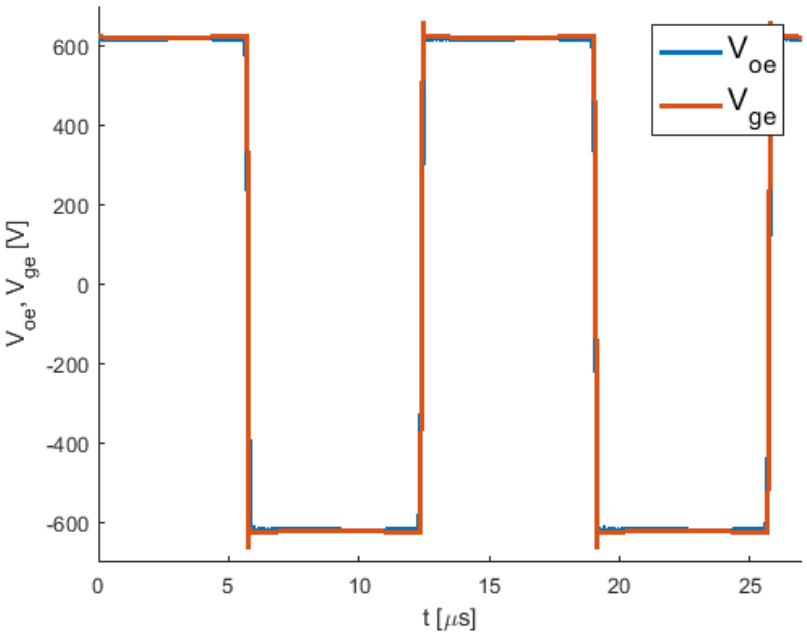


Figure 5.38: Simulated waveforms of V_{oe} and V_{ge} for the boost converter LLC at 450 V, 20 A output.

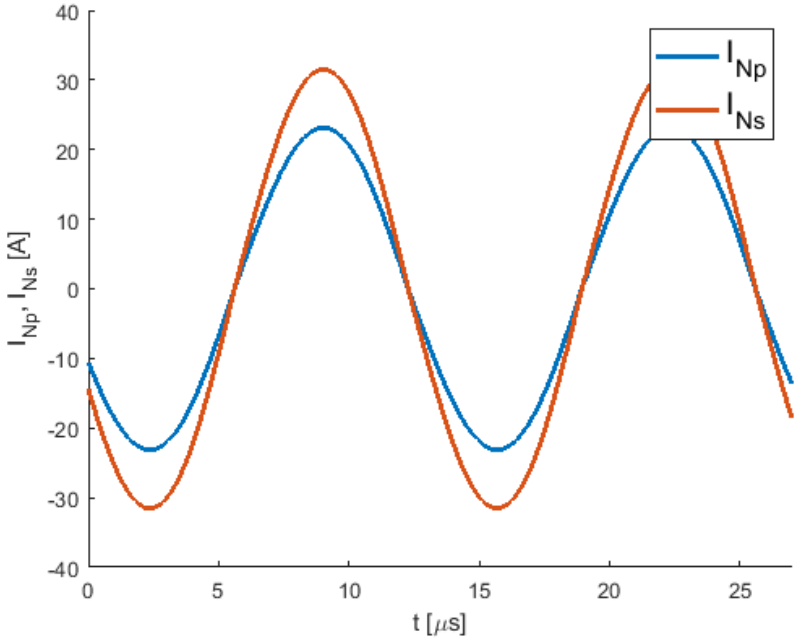


Figure 5.39: Simulated waveforms of I_{Np} and I_{Ns} for the boost converter LLC at 450 V, 20 A output.

The simulations were performed for both converter options and all operating points for a total of six simulation cases. For simplicity, Figures 5.34–5.39 show simulated waveforms for one converter and one operating point only. The LLC converter designed for use with a boost converter is chosen for the example, operating with an output voltage of 450 V and 20 A (operating point 2).

By studying the simulated waveforms it can be determined whether or not the converter is operating as intended and at the right operating point. As mentioned before, this converter is designed to operate at resonant frequency. Figure 5.34 shows the current through the resonant capacitor C_r and the magnetising current I_{Lm}. It can be seen from the figure that the current I_{C_r} is sinusoidal and crosses through the peak of the triangular I_{L_m}. This indicates that both converters are in fact operating at their resonant frequency, resulting in unity gain and the highest possible efficiency [24]. If operating below or above resonant frequency, the current I_{C_r} would have a distorted shape. Above resonant frequency, I_{C_r} will be higher than I_{L_m} at the point of switching, and the switches will have to break this excess current, increasing switching losses. Conversely, at a switching frequency below resonance, the current I_{C_r} will "finish" its cycle before the switching event, and the converter will enter a free-wheeling state for the remainder of the switching period. As no power is delivered in this state, any circulating current will only cause additional losses.

Another way to determine if the converter is operating at resonant frequency is to study the gain of the resonant tank, which should be equal to 1. Figure 5.38 shows the voltages V_{ge} and V_{oe}, which are measured before and after the resonant tank. It can be seen from the figure that these voltages are equal in magnitude, and we know

from (3.20) and Figure 4.2 that this is possible only at resonant frequency. Current stresses in the active components can also be determined from the simulation, such as the MOSFET currents seen in Figure 5.36 or the diode current in Figure 5.37. Figure 5.39 shows the currents in the transformer, and by comparing I_{N_p} and I_{N_s} the transformer turns ratio can be verified. In the same way the voltages present in the converter are also given by the simulation, such as the sinusoidal voltage across the resonant capacitor seen in Figure 5.35 or the previously mentioned V_{oe} in Figure 5.38.

As already said, all curves shown here are for one operating point only. How the simulated values change for the two versions of the LLC converter and their three operating points can be seen in Tables 5.16–5.21. In general, the shape of the curves do not change between converters or operating points, since both converters are tuned to operate at resonant frequency at all times. By studying the tables it can be seen that most currents such as I_{C_r}, I_{switch}, I_{diode} and I_{N_p} are more affected by the output current than the voltage. The exception is I_{L_m}, since this current is directly induced by V_{oe}, which in turn is proportional to the input voltage for a given converter gain. On the other hand, most voltage stresses are proportional to the input voltage, with the exception of the voltages across the resonant elements C_r and L_r, as these voltages are caused by the current flowing through the resonant tank.

5.4.1 Active component losses in LLC converter

The conduction losses of the MOSFETs can be easily calculated using (3.55), the simulated RMS currents in Tables 5.16–5.21 and the on-state resistance listed in Table 4.3. The switching losses are calculated using (3.52) using the fall time from Table 4.3. The diode losses will be the same for both LLC converters. This is due to the fact that the diodes are located in the output rectifier after the transformer, where voltages and currents are identical for both converters. The calculated losses for all operating points can be seen in Tables 5.22 and 5.23. The values for LLC MOSFETs and diodes are for all four MOSFETs/diodes together.

Table 5.22: Component losses for the LLC converter designed for use with a buck converter for all operating points.

Loss type	Op. point 1	Op. point 2	Op. point 3
Buck LLC MOSFETs, conduction	124.38 W	124.38 W	70.16 W
Buck LLC MOSFETs, switching	1.49 W	1.89 W	3.36 W
Buck LLC diodes, conduction	87.74 W	87.74 W	65.91 W

Table 5.23: Component losses for the LLC converter designed for use with a boost converter for all operating points.

Loss type	Op. point 1	Op. point 2	Op. point 3
Boost LLC MOSFETs, conduction	45.07 W	45.13 W	26.02 W
Boost LLC MOSFETs, switching	4.15 W	5.25 W	9.33 W
Boost LLC diodes, conduction	87.74 W	87.74 W	65.91 W

It is seen from the calculations that the buck LLC performs better for switching losses, and the boost LLC has lower conduction losses. Due to the magnitude of the respective losses, the total MOSFET loss is significantly lower for the boost LLC. The large difference in conduction loss in the MOSFET bridge can be explained by the fact that the bridge needs to carry the current of the resonant tank. This current is significantly larger in the buck based converter, resulting in much higher resistive losses in the MOSFETs.

5.5 Final power stage selection

The final choice of topology is done here after summing up the expected losses in all active components.

5.5.1 Active component loss summary

The two alternatives can now be compared with regards to the losses in their MOSFETs and diodes for all operating points. The results can be seen in Tables 5.24, 5.25 and 5.26.

Table 5.24: Summary of active component losses for the two alternative topologies at 400 V, 20 A output

Loss type	Buck and LLC	Boost and LLC
Buck or boost MOSFET, conduction	40.40 W	0.33 W
Buck or boost MOSFET, switching	28.27 W	17.49 W
Buck or boost diode, conduction	20.77 W	32.27 W
LLC MOSFETs, conduction	124.38 W	45.07 W
LLC MOSFETs, switching	1.49 W	4.15 W
LLC diodes, conduction	87.74 W	87.74 W
Total losses	303.1 W	187.1 W

Table 5.25: Summary of active component losses for the two alternative topologies at 450 V, 20 A output

Loss type	Buck and LLC	Boost and LLC
Buck or boost MOSFET, conduction	43.44 W	3.14 W
Buck or boost MOSFET, switching	28.27 W	22.21 W
Buck or boost diode, conduction	16.68 W	32.25 W
LLC MOSFETs, conduction	124.38 W	45.13 W
LLC MOSFETs, switching	1.89 W	5.25 W
LLC diodes, conduction	87.74 W	87.74 W
Total losses	302.4 W	195.7 W

Table 5.26: Summary of active component losses for the two alternative topologies at 600 V, 15 A output

Loss type	Buck and LLC	Boost and LLC
Buck or boost MOSFET, conduction	27.40 W	10.61 W
Buck or boost MOSFET, switching	21.20 W	29.69 W
Buck or boost diode, conduction	3.34 W	24.16 W
LLC MOSFETs, conduction	70.16 W	26.02 W
LLC MOSFETs, switching	3.36 W	9.33 W
LLC diodes, conduction	65.91 W	65.91 W
Total losses	191.4 W	165.7 W

It can be seen that the boost converter continues to be more efficient as the operating point shifts towards maximum voltage, even though the difference is smaller than in the lower voltage operating points. One reason for this is the drop in LLC MOSFET conduction losses. As these losses are more significant in the buck based converter, the lower losses caused by reduced output current will cause a larger reduction of loss power in this converter than in the boost based version. The higher voltage level also affects the buck and boost MOSFETs differently. The buck MOSFET will have lower conduction losses due to the lower output current, while the boost MOSFET sees higher conduction losses due to its increased duty cycle. In general, high currents affect the buck based converter the most, while high voltages cause more component stress in the boost based converter.

5.5.2 Selection

To summarise the result from the simulations, both setups work as concepts but the boost setup has several benefits:

- Lower active component losses in power stage
- Lower active component losses in LLC stage
- Lower peak current in boost inductor

Due to these reasons, the boost power stage with corresponding LLC converter is chosen as the charger topology.

As already mentioned in Section 4.2, the idea of using a SEPIC converter was discarded earlier in the project due to the lack of suitable MOSFETs. For this reason the SEPIC was not analyzed in detail and no simulations were made. By comparing the voltage and current stresses of the SEPIC (Table 3.3) to those of the buck (Table 3.1) and boost (Table 3.2), a rough estimate can be made. It can be seen that while the current stress can be similar, the voltage stress is always higher in the SEPIC for both the MOSFET and the diode, increasing switching losses in the MOSFET and forcing the use of higher rated components which may have higher internal resistance. Furthermore, the SEPIC features two additional passive components L_2 and C_1, which also add to the total losses and require additional space. Considering this, it is deemed unlikely that a SEPIC based converter would have been a more efficient choice than the selected boost based converter topology.

6
Converter Design

In this chapter, the final topology is turned into a complete converter schematic with real components, control hardware and auxiliary circuitry, see Figure 6.1 for block schematic. The proposed power transformer is manufactured and partially tested.

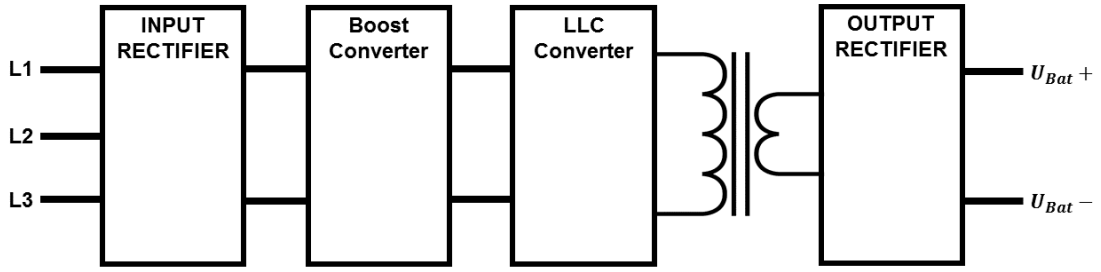


Figure 6.1: Block schematic of the chosen converter topology.

6.1 Input rectifier

A simple diode rectifier is selected to provide DC power for the boost converter. The chosen rectifier is International Rectifier 36MT, which is rated for a maximum repetitive peak reverse voltage of 1000 V and a DC output current of 35 A. It was mainly chosen as it fulfilled the ratings needed and was in stock at the production facility. As mentioned in Section 1.3, this solution is not ideal, but used here for simplicity in order to focus on other parts of the design.

6.2 Boost converter design

This section covers the component selection and design process of the boost converter stage used in the final design.

6.2.1 Boost inductor

As with most components in this project, it was hard (or impossible) to find a supplier that could source a suitable part with the given parameters. Therefore the boost inductor was designed to be a prototype, handwoven inductor with a ferrite core. To simplify and speed up the design process, the inductor design tool from FerroxCube [52] was used. FerroxCube is a ferrite core manufacturer which has made a design suite for matching different cores to different application specifications. It has several applications, one of them being an inductor design tool, see Figure 6.2 for picture. The inductor design tool needs to be fed several specifications to find a suitable core. The needed input is:

- Core size
- Core material
- Inductance
- Maximum current
- Ambient temperature
- Copper fill factor

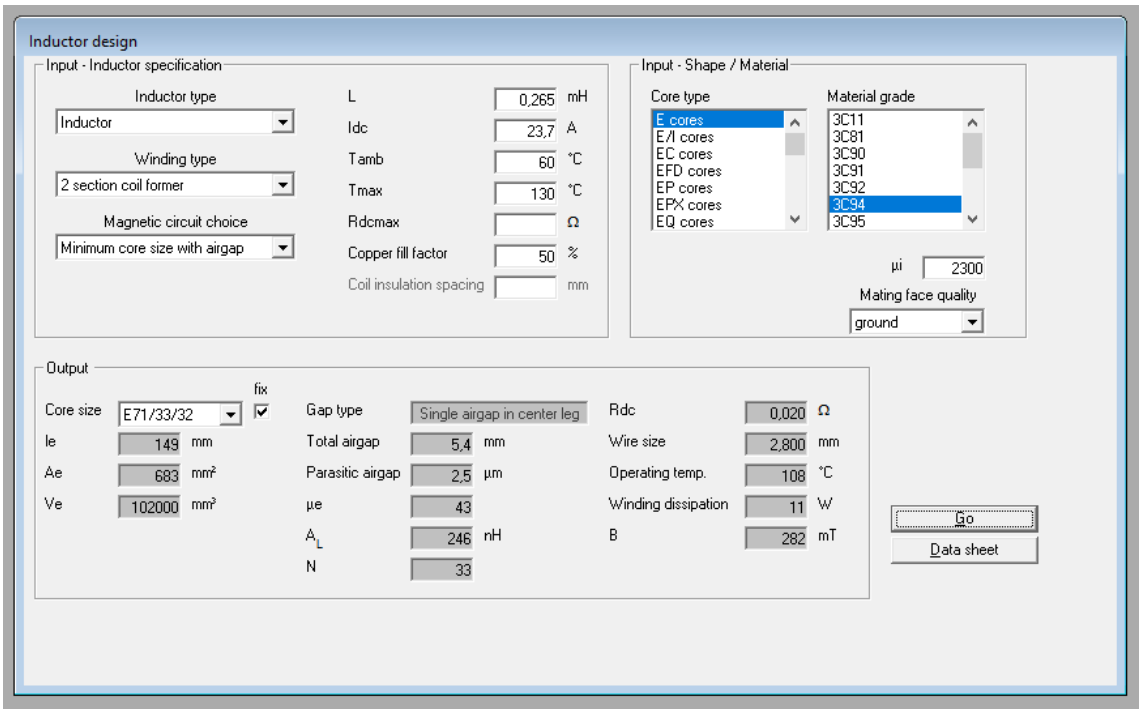


Figure 6.2: Picture of the inductor design tool in FerroxCube Design Suite.

The core size and material type go together to a single combination per core, but are linked to different properties of the application. The size is mainly linked to the power that needs to be put through the inductive element. As 9 kW is rather large, the cores suggested are on larger end of the spectrum of the standard sizes for each shape. The shapes suggested are the U- and E-shapes. However, as for the SiC components, the most suitable cores were not available at the time of purchase. The preferred cores were E100/60/28, E71/33/32, U126/91/20 and U93/76/16, of which only the E71/33/32 core was available. The most suitable material available for the E71/33/32 size was 3C94 ferrite [53]. 3C94 is appropriate for low frequency (less than 300 kHz), high power applications as it has a high saturation rating [54], see Table 6.1 below for a selection of ratings for the E71/33/32 3C94 core. This also makes it suitable for the transformer in the LLC converter stage. Being able to share components between the converters are preferable from a practical point of view, for example being able to share spares during testing, etc.

Table 6.1: E71 3C94 Core properties [53]

Property	**Value**
Saturation flux density, B_{sat}	320 mT
Effective core volume, V_e	102 000 mm^3
Effective core area, A_e	683 mm^2
Effective core length, A_e	149 mm

Inductance and maximum current have been covered in Section 5.2.2, one needs to pick matching set of values from Table 5.14. For the copper fill factor, a bobbin (also known as a coil former) is needed to give a fitting estimate. As for the cores themselves, matching bobbins were hard to come by at a reasonable cost. Therefore the coil former mentioned in Section 6.3.3 was used as a base for a 3D-printed bobbin made in-house. As the aforementioned bobbin is made for a double stacked core of the same size, the new one was simply shortened to fit a single core, whereby inheriting the same winding area A_n. With this, the copper fill factor is set at a moderate 0.5. The ambient temperature is hard to predict, and is therefore set at achievable 60 °C. This value can be altered at later stages by adding more cooling, for example a fan or similar.

With the values locked down, several inductance-maximum current value combinations were fed into the design tool. With the E71/33/32 3C94 core locked in, the inductance span 120 µH to 265 µH could be solved for. Larger values of inductance caused issues in the suggested size of the air-gap in the centre leg, which subsequently caused problems with the operating temperature. See Table 6.2 below for a summary of suggested designs in the above mentioned inductance range with their corresponding operating values calculated by the design tool.

Table 6.2: Suggested designs for 120 µH to 265 µH boost inductor

Prop. \ L	120 µH	150 µH	200 µH	250 µH	265 µH
Flux density max, B_{max}	284 mT	315 mT	306 mT	287 mT	282 mT
Air-gap length	3.3 mm	3.4 mm	3.8 mm	4.9 mm	5.4 mm
Number of turns, N	20	21	25	31	33
Wire size, diameter	3.55 mm	3.55 mm	3.15 mm	2.8 mm	2.8 mm
Operating temp	91 °C	87 °C	93 °C	106 °C	108 °C
Winding resistance	6.5 mΩ	7.3 mΩ	11 mΩ	18 mΩ	20 mΩ

The next design step is to find components that could fit the suggested designs and/or make adjustments to the designs to fit the available parts. If designs couldn't be realised with the available components, they will be discarded. Due to time constraints further design and manufacturing of a prototype was stopped. However, as the rest of the boost converter design needs an inductance value, the 120 µH case is chosen to be used for further design development. This is due to that most of its case specific data is already known and as it is the lowest suitable inductor value, it will cause the highest max- and RMS-current values, which leads to worst case scenarios for other components, whereby making the rest of the converter compatible with larger inductance values.

6.2.2 Power MOSFET

As mentioned in Section 4.5 the C2M0040120D SiC power MOSFET from Cree, Inc. was the preferred choice of component for purchase. As it was one of the few that was available, it was chosen.

6.2.3 Gate driver

The ACNU-3430 gate driver from Broadcom is used to drive the gates of the selected SiC MOSFETS. This gate driver is chosen for its high common mode noise immunity of 100 000 kV/µs and current carrying capacity of 5 A. A 4.7 Ω gate resistor is added between the driver and the gate of each MOSFET in order to limit the gate current below 5 A.

The loss calculations for the MOSFET which were performed in (5.5.1) used rise and fall times from the manufacturer datasheet [38], assuming gate driving voltages of −5 V to 20 V and a gate resistor of 2.5 Ω. The low voltage power supply used in this converter provides voltages of −4 V to 18 V. According to the datasheet, a conservative estimate is that this increases the rise time from 52 ns to 60 ns and the fall time from 34 ns to 42 ns. As a result of this, the switching losses in the boost converter MOSFET increase by 18.6% and the switching losses in the LLC MOSFETs increase by 23.5%.

6.2.4 Power diode

The C4D40120D SiC Schottky diode from Cree, Inc. that was used for simulations was also intended to be used for the converter design. Unfortunately this component went out of stock before it could be purchased, and an alternative component was found. The FFSH40120ADN_F155 [55] SiC Schottky diode from ON Semiconductor was chosen as a replacement diode. It features the same voltage rating of 1200 V as the originally selected component and a continuous forward current of 40 A. This is slightly lower than the C4D40120D, but still sufficient for this application. Other properties of the two diodes are also found to be similar enough to use the FFSH40120ADN_F155 as a replacement without further modification of the converter. When comparing forward voltage drop at rated current, it is lower for the new diode (2 V compared to the 2.2 V for the C4D40120D that was used for loss calculations). Therefore the new diode turns out to be a better choice.

6.2.5 Control circuit

To minimise the amount of programming needed to operate the charger, as the project is focused on hardware design and potentially save additional time spent programming, an extra IC called LM5020-2 [56] from Texas Instruments is added as a controller for the boost converter. The LM5020-2 IC is made for control of switch mode power supplies, and the pin layout with most of its associated circuitry can be found in Figure 6.3. The complete circuit is available in Appendix A. It can output a PWM signal with a maximum duty-cycle of 0.5 and change it dependent on its control input. With some added analogue electronics, the XMC micro-controller can use one of its analogue output pins to control to the LM circuit. Furthermore, it has functions such as soft-start, current limitation, input voltage too low, etc.

To control the boost converter via the LM5020-2 the COMP-pin in Figure 6.3 is used. The manufacturer recommends using it to bias the transistor side of an opto-isolator, in this case the Lite-On LTV-217-B [57] is used. The COMP-pin is internally fed by 1.4 V, which then is fed forward into the duty-cycle logic. As the voltage on the COMP-pin is changed by external circuitry, the duty-cycle is adjusted along with it. 0 V would cause the duty-cyle to drop to 0. The LED side of the opto-isolator is controlled by the boost converter output and the XMC processor. From the boost converter output voltage $V_{Boost,out}$, a voltage divider (R_{Div1}, R_{Div2}) is used to reduce the voltage to a manageable control voltage and feed the anode of the opto-isolator. A analogue output of the XMC (XMC_{VC}) is connected to the cathode through another voltage divider (R_{Div3}, R_{Div4}) and it can be used to bias the diode depending on the desired output voltage. When the opto-isolator conducts, the COMP-pin is virtually short circuited to ground. With this dynamic, the PWM_{Boost} duty-cycle can be adjusted by the present output voltage and the desired output voltage. The soft-start function, which is controlled by the SS-pin, is internally connected to the COMP-pin as well, however with a designed 0.35 V to 0.75 V offset. By connecting a capacitor, C_{SS}, to the SS-pin, an internal current source of 10 µA will charge the capacitor. As the voltage on the SS-pin will ramp up as the capacitor is charged, the voltage on the COMP-pin will follow. As the duty-cycle will be limited until

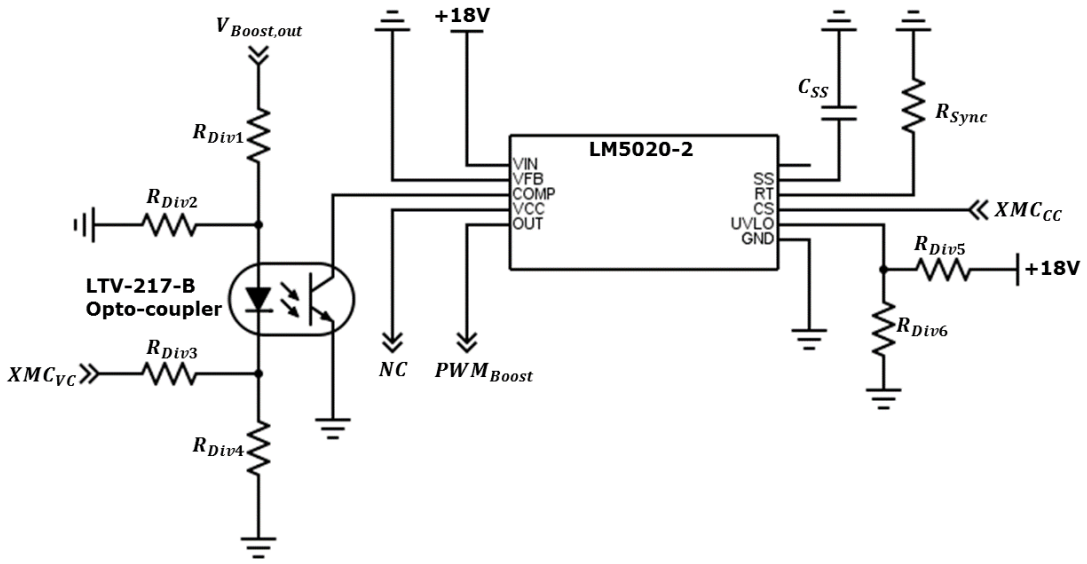


Figure 6.3: Pin layout of LM5020 IC with its associated circuitry.

charging has negated the voltage offset, a soft start function is achieved. As the size of the capacitor will decide the length of the soft start time, an appropriate capacitor value will have to be tested before future charger use.

The **VIN**-pin is the voltage supply pin for the IC and it is therefore connected to the on-board low-voltage supply, using the 18 V level. The **VCC**-pin is a 7.7 V reference output from the internal logic of the IC that isn't used and therefore is left unconnected (NC). Another function is the under voltage line detection (UVLO), which is controlled by the **UVLO**-pin. The pin needs to be fed 1.25 V for the IC to start operation. Therefore it is connected with a voltage divider (Rdiv5, Rdiv6) from the low-voltage supply. If the low-voltage supply would fail, the voltage on the **UVLO-pin** would drop and the LM5020-2 will clamp the PWM_{Boost} duty cycle to 0. The **RT/SYNC** pin sets the switching frequency of the PWM_{Boost} signal using an external resistor, R_{sync}. The switching frequency of the converter, f_{sw}, was set to 50 kHz in previous sections and to achieve that, the resistance value needed was calculated using (6.1) from the data-sheet [56],

$$R_{sync} = \frac{1}{f_{sw} \cdot 316 \cdot 10^{-12}}, \tag{6.1}$$

which yields $R_{sync} = 63.3\,\text{k}\Omega$.

The **CS**-pin is the over current/current control input for the IC. If the pin is not fed ≥ 0.5 V, the PWM-output will be clamped to 0 until it has been pushed over its limit again. Both over current protection and current control signals are available in the XMC processor and therefore the pin is connected to another XMC analogue output pin, such that it can control the boost converter dependent. The **VFB**-pin is an input for a internal error amplifier which can be used in conjunction with the

COMP-pin. As the need for additional error amplification has not been investigated, the pin has been connected to ground, as to affect the IC as little as possible. The **OUT**-pin is the PWM output from the internal duty-cycle logic. It is directly connected to the driver circuitry for the boost switch.

In total, the full boost converter schematic, with all the components and signals mentioned on the section above, can be seen in Figure 6.4. Additional circuits needed for the boost converter operation, the DC-link see Section 6.4, Pre-charge see Section 6.4.3 and XMC microcontroller see Section 6.6.

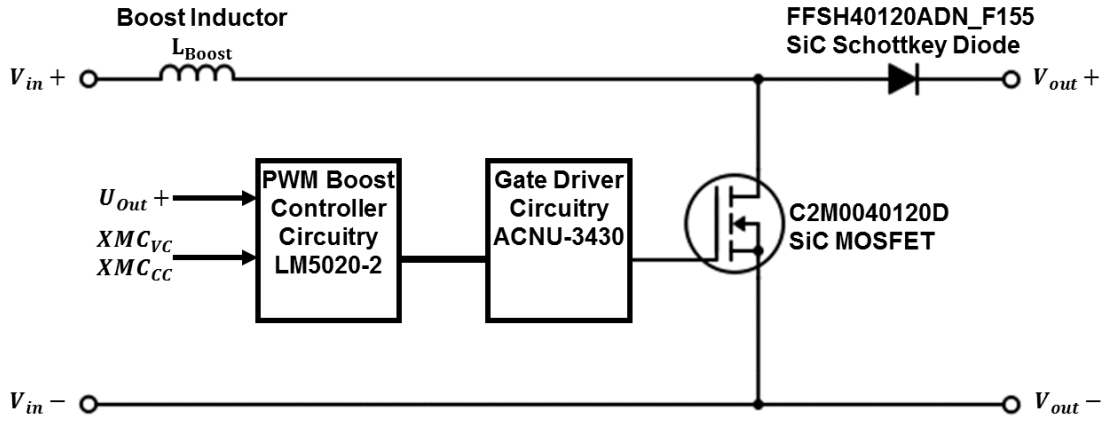


Figure 6.4: Schematic of the full boost converter

6.3 LLC converter design

This section covers the component selection and design process of the LLC converter stage used to provide galvanic insulation between the boost converter and the output of the battery.

6.3.1 Resonant capacitor

In high-powered resonant converters the series resonant capacitor can be a limiting factor due to the high voltages and current passing through the capacitor at high frequencies. This drastically limits the options when selecting a suitable component. A polypropylene film capacitor from EPCOS/TDK, model number B32653A8103J [58], is chosen for this task as it was the only polypropylene capacitor found which had a sufficient voltage rating at the selected operating frequency. This capacitor is rated for 2000 V at DC, and approximately 550 V RMS if operated at a frequency of 75 kHz and with an ambient temperature of less than 90 °C. The selected capacitor

has a capacitance of only 10 nF, so in order to realise the desired resonant circuit, ten capacitors are connected in parallel.

6.3.2 Resonant inductors

The voltage and current stresses on resonant inductors L_r and L_m have been calculated in Section 4.6.1 assuming an ideal transformer. Due to the unknown values of the real transformer's leakage and magnetising inductance, the exact inductance values of additional inductors L_r and L_m cannot be determined until after the transformer is built and tested. For L_r, desired inductance is equal to

$$L_r = L_{r,tot} - L_{leak} \tag{6.2}$$

and for L_m

$$L_m = \frac{1}{\frac{1}{L_{m,tot}} - \frac{1}{L_{mag}}} \tag{6.3}$$

The design process can then be carried out similar to the boost inductor, although no DC component of the current will be present in the resonant inductors.

6.3.3 Transformer

The Ferroxcube design tool, used earlier for the design of the boost inductor, can also be used for transformer core selection. For a throughput power of 9 kW, the design tool suggests using large E-cores such as the E100/60/28, alternatively U-cores or toroids of similar dimensions. These core were unfortunately, at the time of designing, difficult to order from suppliers. Instead it was decided to build a transformer using two smaller cores of the type E71/33/32, as both the cores themselves and corresponding double bobbins were readily available. The chosen ferrite type is 3C94, a material suitable for power transformers operating at frequencies below 300 kHz. Some properties of the chosen core and bobbin configuration are listed in Table 6.3

Table 6.3: Core and bobbin properties

Property	Value	Source
Recommended peak flux density, B_{max}	270 mT	Design tool
Effective core area, A_e	683 mm^2	Core datasheet
Effective core volume, V_e	102 000 mm^3	Core datasheet
Winding area, A_n	389 mm^2	Bobbin datasheet

The number of turns required on the primary side of the transformer can be calculated according to (3.42). The maximum flux density swing ΔB is twice the peak flux density listed in Table 6.3. However, in order to provide plenty of safety margin, only half the maximum value of ΔB is used for the calculation. This results in $14.79 \approx 15$ turns for the primary winding, and $10.84 \approx 11$ turns for the secondary winding.

For the designed operating frequency of 75 kHz, the skin depth can be calculated according to (3.43) using properties for copper [9], i.e. $\rho = 1.724 * 10^{-8} \Omega\,\mathrm{m}$, $\mu = \mu_0 = 4\pi * 10^{-7} \mathrm{H/m}$ resulting in a skin depth of $\delta = 241\,\mu\mathrm{m}$, meaning that the skin effect can be eliminated by using wire with a diameter less than $d = 2\delta = 582\,\mu\mathrm{m}$.

A type of litz wire is available which has a strand diameter of 100 µm, which is more than enough to mitigate the skin effect at this frequency. Each litz wire of this type can carry a rated current of 3.36 A, so several wires need to be connected in parallel. The primary winding needs 5 parallel litz wires and the secondary winding 6 parallel wires. The total available winding window for the selected core is $384\,\mathrm{mm}^2$ and the copper area of one litz wire is $0.94\,\mathrm{mm}^2$. Assuming a fill factor of 0.4 for this wire, the total area required for the desired winding configuration becomes

$$A_w = \frac{(15 * 5 + 11 * 6) * 0.94\,\mathrm{mm}^2}{0.4} = 331\,\mathrm{mm}^2 \tag{6.4}$$

filling up 85% of the available winding window.

The winding losses can be calculated using (3.55) and (3.57). The primary winding has 15 turns, a total copper area of $0.94 * 5 = 4.7\,\mathrm{mm}^2$, and the MLT of the bobbin is 230.5 mm. The secondary winding needs 11 turns, and has a total area of $0.94 * 6 = 5.64\,\mathrm{mm}^2$ The calculated winding resistance is

$$R_p = \frac{1.724 * 10^{-8} \Omega\,\mathrm{m} * 15 * 230.5\,\mathrm{mm}}{4.7\,\mathrm{mm}^2} = 12.7\,\mathrm{m}\Omega \tag{6.5}$$

for the primary winding and

$$R_s = \frac{1.724 * 10^{-8} \Omega\,\mathrm{m} * 11 * 230.5\,\mathrm{mm}}{5.64\,\mathrm{mm}^2} = 7.8\,\mathrm{m}\Omega \tag{6.6}$$

for the secondary. Corresponding power losses are 2.7 W in the primary and 3.1 W in the secondary, for a total winding loss of 5.8 W. Note that the use of the same MLT for both windings is a simplification that may cause some error in the calculation of the resistance.

The expected magnetising inductance can be calculated using

$$L = \mu_0 \mu_r * \frac{N_p^2 A_e}{l_e} \tag{6.7}$$

using the transformer core datasheet values for relative permeability μ_r and effective flux path length l_e. Using the values for initial permeability and taking into account the manufacturer tolerances, the inductance value is calculated to be between 4.8 mH and 7.4 mH.

6.3.4 Transformer testing

The transformer designed in Section 6.3.3 was manufactured and some basic tests were performed.

The transformer windings were connected one at a time to a DC power supply providing a current of 10 A and the voltage drop was measured for each winding. The results are listed in Table 6.4.

Table 6.4: DC resistance of transformer windings

Winding	Measured voltage	Resistance
Primary	141.7 mV	14.17 mΩ
Secondary	103.0 mV	10.30 mΩ

This is slightly higher than the values calculated in (6.5) and (6.6), and the greatest uncertainty in the calculations is likely the value of MLT. It can be seen that the error is larger in the secondary winding, which is wound on the outside of the primary and therefore requires more wire per turn. With the measured resistance, the total power loss is instead 7.2 W for both windings.

The inductance of the primary transformer winding was measured using an LCR meter at different frequencies, once with the secondary winding open and once with the secondary winding short circuited. The results from the open circuit testing are listed in Table 6.5 and from the short circuit test in Table 6.6. It can be seen that the inductance of the core increases with the applied frequency in the open circuit test. This is possibly due to a change in permeability of the ferrite material [53]. The LCR meter failed to give an inductance value for the short circuited transformer at 100 Hz. Measuring small inductances at low frequency is generally difficult due to the fact that the total impedance at low frequencies is significantly influenced by resistive loss in the coil. In any case, the relevant measurements are within the range 10 kHz to 100 kHz for this application.

Table 6.5: Primary side inductance, open secondary

Applied frequency	Measured inductance
100 Hz	4.73 mH
1 kHz	4.74 mH
10 kHz	4.71 mH
100 kHz	8.00 mH

In these measurements the open circuit inductance corresponds to the magnetising inductance, and the leakage inductance is neglected as it is much smaller. Conversely, in the short circuit test the magnetising inductance is neglected due to its size. In conclusion, the transformer inductances do not pose a problem for the design of the LLC converter. The leakage inductance is much smaller, and the magnetising inductance much larger than the design values of the resonant tank. This means that (6.2) and (6.3) can be used to finish the design of the resonant tank, either

Table 6.6: Primary side inductance, closed secondary

Applied frequency	Measured inductance
100 Hz	-
1 kHz	5.51 µH
10 kHz	5.68 µH
100 kHz	5.65 µH

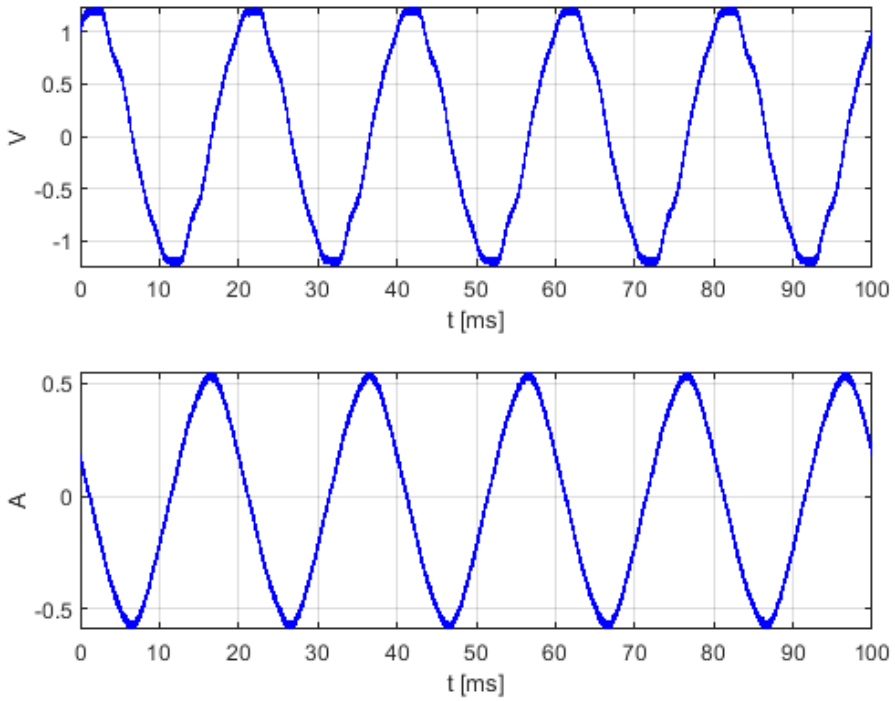


Figure 6.5: Transformer voltage and current at 50 Hz, no saturation.

by adding L_r and L_m physical inductors or by incorporating the inductances into the transformer. The magnetising inductance of the transformer can be adjusted by incorporating an airgap into the transformer core.
In this test, the primary winding was supplied with a sinusoidal 50 Hz voltage from a low voltage autotransformer connected to the grid, while the secondary winding was left open. The voltage was increased gradually until the transformer showed signs of saturation. In Figure 6.5, an applied voltage with a peak of approximately 1.2 V results in a current of around 0.55 A. The current shape is sinusoidal and the core shows no sign of saturation. In Figure 6.6, the applied voltage is above 2 V and the induced current is starting to peak, indicating that the transformer core is saturating. It can also be seen from the voltage plots that the voltage that was available for the test is slightly distorted. To compare the 50 Hz results to the actual operating point at 75 kHz, one can compare the area under the voltage plot for one half cycle in both cases. For the 50 Hz case this area is extracted from the figure and found to be 0.0077 V s. By comparison, the area of the switching voltage during normal operation would be equal to $V_{oe}/(2f_s) = 0.0055$ V s in the worst case where

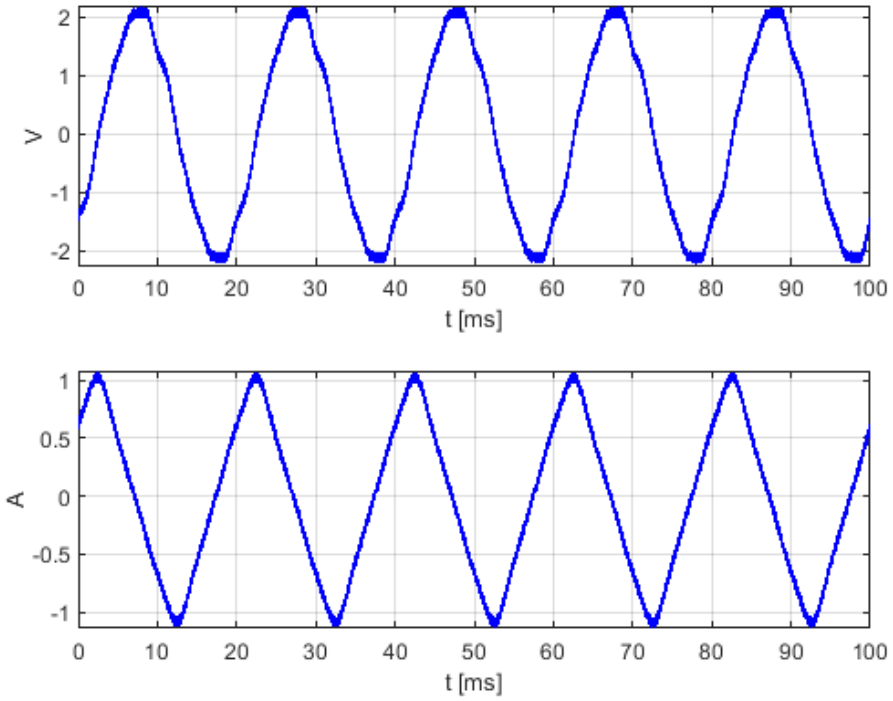


Figure 6.6: Transformer voltage and current at 50 Hz, beginning to saturate.

the output voltage is the highest. In conclusion, the test shows that the transformer is able to handle higher voltages than will be present at normal operation without saturating.

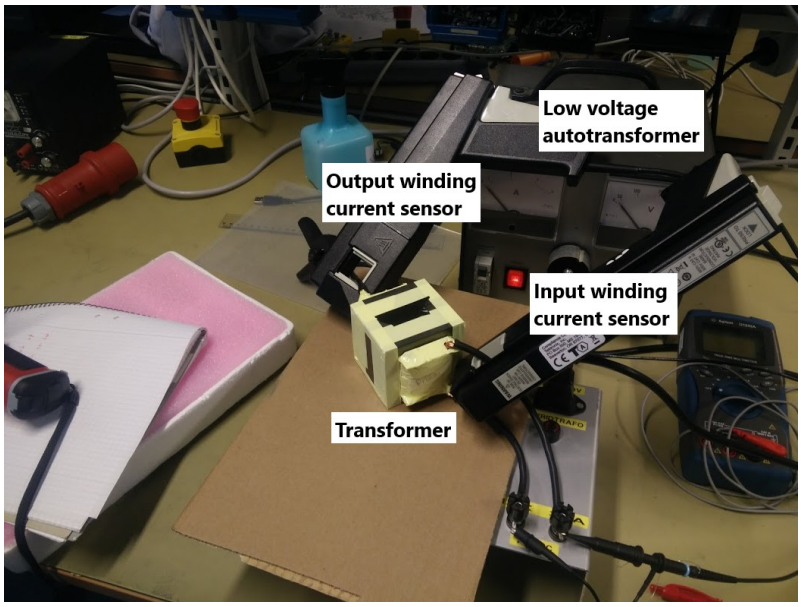


Figure 6.7: The transformer during testing with current sensors on both windings.

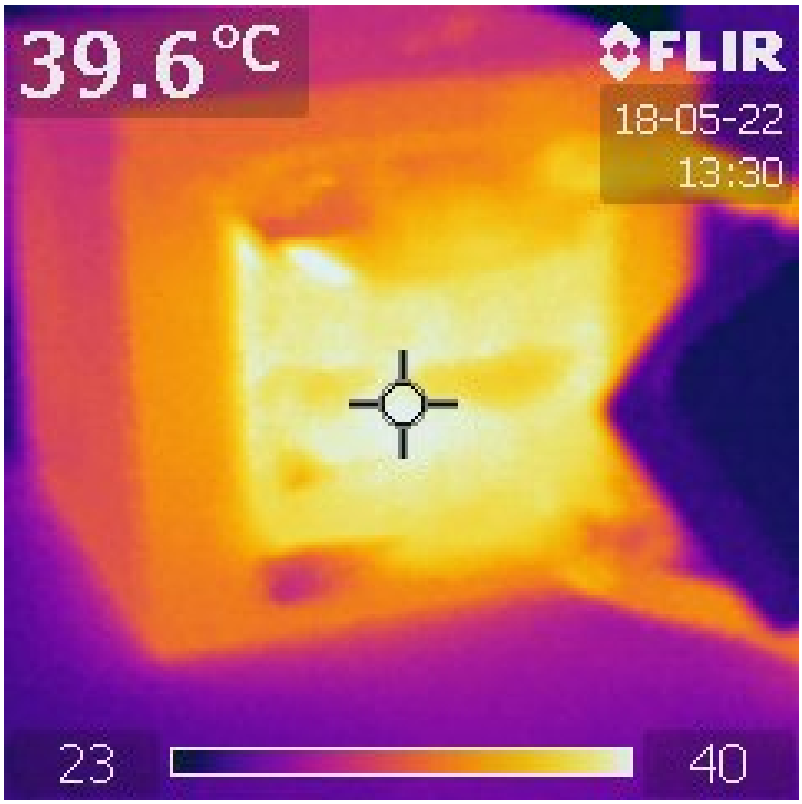


Figure 6.8: Thermal image of the transformer at the end of the winding load test.

With the primary winding still connected to the autotransformer, the secondary winding was short circuited and the output voltage adjusted so that the current flow in the windings corresponded to 20 A in the secondary winding. Figure 6.7 shows the transformer connected to the autotransformer. The transformer was left

running this way for one hour, during which the temperature of the windings was measured using a thermal imaging camera. This was done in order to get a first indication of the heating of the transformer during operation. Figure 6.8 shows one image taken by the camera at the end of the test. At an ambient temperature of 23 °C, the maximum temperature measured was 39.6 °C. This is well within the limits of operation for the transformer, but does not include core losses as these are negligible at the applied voltage and frequency. In order to verify the actual thermal performance of the transformer, a test at full power has to be done.

6.3.5 Controller

Analog controller ICs that are optimised for PFM control of half-bridge and full-bridge resonant converters are available from several manufacturers in different versions. They all provide similar functionality but differ in terms of switching frequency interval and availability of additional features.

The UCC25600 Resonant Mode Controller from Texas Instruments [48] has the advantage of being one of the least complex designs available with only eight pins to connect, while providing all necessary functions for this particular application. The available functions that will be used are:

- Adjustable dead time of the gate signals, which will be set to a higher value in case the minimum dead time cannot be used.
- Overcurrent protection, which can prevent damage to the switches by quickly turning off the converter if an overcurrent is detected.
- Adjustable switching frequency, so that the switching frequency can be tuned to the actual resonant frequency of the resonant circuit.
- A soft start function, which will prevent inrush currents during the startup sequence of the converter.

The switching frequency and dead time adjustments allow the controller to be used with different resonant circuits, gate drivers and switches. The overcurrent and soft start functions will, in combination with other safety functions and the design of the power circuit itself, protect the components from damage during normal and emergency operation. A schematic showing the UCC25600 can be seen in Figure 6.3.5.

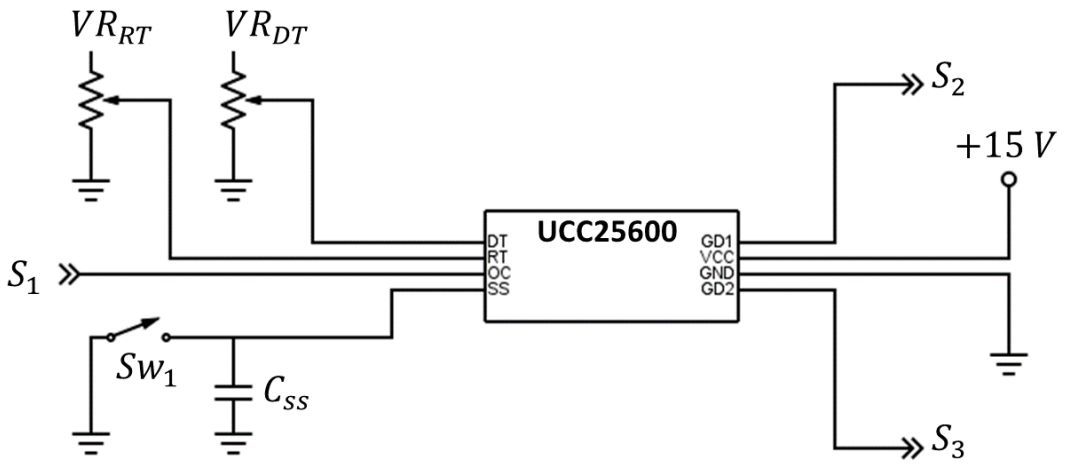


Figure 6.9: Pin layout of the UCC25600 controller.

The RT pin is used to control the switching frequency, and subsequently the converter gain, by varying the resistance between the pin and ground. For the purpose of simplifying the design of this converter, intended to operate at unity gain only, a simple analog potentiometer with a maximum resistance of 10 kΩ is used to set the switching frequency. The potentiometer allows modifying the switching frequency in order to compensate for non-ideal resonant elements or for testing the converter at different frequencies. To tune the controller to the desired operating frequency of 75 kHz, the required resistance is 2.7 kΩ.

The DT pin works in a similar fashion, but does instead control the dead time of the gate pulses. Utilising the dead time to achieve ZVS is an important part of resonant controller design, and for this reason controller ICs offer the option to adjust this property. For the purpose of testing the converter prototype, the DT pin is connected in the same way as the RT pin using a 10 kΩ potentiometer. The initial setting for the dead time is set to the minimum value of the controller, 120 ns.

The overcurrent pin (OC) shuts down the converter if the voltage on the pin goes above 1 V. A current sensor, further described in Section 6.5.2 , connected to a peak detector circuit is used to generate the voltage signal S_1 based on the sensed current in the resonant tank. Once the current drops to a value corresponding to a pin voltage of less than 0.6 V, the converter is started up again.

Similar to the PWM controller used for the boost converter stage, the UCC25600 also features a soft start pin SS to ramp up the output in a controlled fashion during startup. A 30 nF capacitor is used as soft start capacitor C_{ss} resulting in a soft start time of 16.8 ms. During this time, the converter operates with higher than nominal switching frequency. This increases the impedance of the resonant tank in order to

reduce the initial current. The switching frequency drops linearly during the soft start time and reaches the nominal frequency at the end. The switch Sw_1 is a regular mechanical switch used to short circuit the SS pin to ground, preventing the LLC converter from starting up. This can be useful in a situation where operation of the LLC converter is not desired, such as when testing the boost converter stage separately.

The outputs GD1 and GD2 are gate driver outputs generating alternating gate pulses for the converter bridge. The signals S_2 and S_3 are sent to gate drivers described in Section 6.2.3. How the gate drivers connect to the lower and upper leg MOSFETs can be seen on page 11 in the final schematic in Appendix A.

6.4 DC-link design

The dc-link is a bank of capacitors situated between the output of the input rectifier and the output of the boost converter. Its main purpose is to smoothen the input voltage to the LLC stage and keep it as stable as possible, as it will have accumulated ripple from both the input rectification and the switching in the boost converter. To design and operate this capacitive bank in a effective and safe manner, there are several precautions that needs to be taken into consideration.

6.4.1 Size and placement

Deciding the size of the dc-link is often a balancing act between physical space on the PCB, allowed voltage ripple and the current that needs to be put through. A generally allowed voltage ripple is 5% [16], [30] of the output voltage, and 5% is therefore set as a goal also in this application. The switching component that will most likely create the ripple is the propagated third multiple of the line frequency from the input mains [16], [30], rather than the switching ripple from the actual boost converter. For this application, the DC-link capacitance can be approximated as

$$C_{DC} = \frac{P_{max}}{2\pi V_{DC} V_{ripple} f_{prop}}, \tag{6.8}$$

with values from the chosen topology. The worst case for ripple is when the output voltage from the boost is at its lowest, see Table 6.7 for values;

Table 6.7: Operating point values for worst voltage ripple case.

Property	Value
V_{DC}	545 V
P_{max}	7.99 kW
V_{ripple}	27.25 V
f_{line}	$3{\cdot}50 = 150$ Hz

These values lead to $C_{DC} \geq 5.71076 * 10^{-}4 \approx 571\,\mu F$. Note that a larger capacitance value will result in even smaller ripple.

The bulk capacitor that was chosen is the 470 µF EPCOS-TDK B43642A5477M000 [59] as it has good ratings and was available in stock at the facility. The capacitor is rated to 450 V, therefore it needs a series connection to ensure 820 V usability. Due to this series connection, discrete 235 µF steps become the main building blocks of the DC-link. Each capacitor also has an AC peak rating of 5.48 A. Due to this limiting factor, more parallel branches should be added to decrease the current carried by each branch if the peak is too high. As the EPCOS capacitors are of the aluminium electrolytic type, they have comparatively high series resistance and series inductance. For this reason their proficiency at dealing with high frequency ripple is low, and therefore a smaller, 10 µF polypropylene capacitor is added to deal with the high frequency switching transients. The capacitor chosen is the Vishay MKP1848C61090JK2 [60], as it has a voltage rating of 900 V and was in stock at the facility.

A LTspice model based on the previous boost converter simulations with an added rectifying bridge was set up to simulate optimal DC-link placement and size, see Figure 6.10 for example circuit and Table 6.9 for symbol explanation. Four main cases were selected, each sub-case having the same total capacitance but different placements, see Table 6.8 for case presentation.

Table 6.8: Simulation cases for voltage ripple simulation.

Case #	Capacitance at rectifier output	Capacitance at boost output	Total capacitance	Total # of used capacitors
1.1 1.2	10 µF $3 * 235\,\mu F + 10\,\mu F$	$10\,\mu F + 3 * 235\,\mu F$ 10 µF	725 µF	8
2.1 2.2	10 µF $4 * 235\,\mu F + 10\,\mu F$	$10\,\mu F + 4 * 235\,\mu F$ 10 µF	960 µF	10
3.1 3.2	10 µF $5 * 235\,\mu F + 10\,\mu F$	$5 * 235\,\mu F + 10\,\mu F$ 10 µF	1.295 mF	12
4.1 4.2	10 µF $6 * 235\,\mu F + 10\,\mu F$	$6 * 235\,\mu F + 10\,\mu F$ 10 µF	1.43 mF	14

Case 1 represents the lowest number of 235 µF branches needed to surpass the calculated capacitance in (6.8), while cases 2 to 4 are each one branch larger to see what benefits that can be gained from an increase in size.

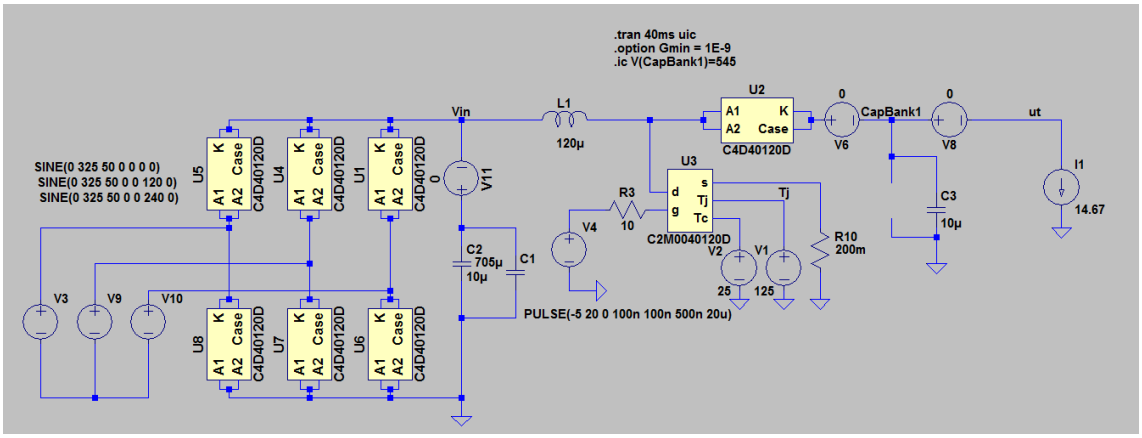


Figure 6.10: LTspice simulation circuit for voltage ripple simulation

Table 6.9: Boost converter output ripple LTspice schematic symbol description.

Symbol	Description	Value
V3, V9, V10	Phase voltage sources	325 V, 50 Hz
V4	Pulse voltage source for PWM	−5 V to 20 V
V1, V2	DC voltage sources for temperature control of MOSFET	25 V, 125 V
V6, V11	0 V voltage voltage sources for current tracing	0 V
I1	Simulated load as a current source	14.67 A
U1	Boost Diode model	N/A
U2	Boost MOSFET model	N/A
U1, U4-U8	Rectifier Diode model	N/A
L1	Inductor with parallel resistance in model	120 µH
C2	Electrolytic input/output capacitors	0.705 mF to 1.41 mF
C2, C3	Polypropylene input/output capacitors	10 µF

Worth noting in the circuit is that C2 moves from the input to the output depending on case. Each case was simulated for 50 ms to reach steady state operation. See Figures 6.11 and 6.12 for zoom plot of the voltage ripple of 10 ms steady state operation with all cases and their associated average value. Numerical values for ripple voltage and peak current per branch are presented in Table 6.10. The current through each parallel branch is the value corresponding to the rated peak current value mentioned above for the bulk electrolytic capacitor, as it, due to its size, will do most of the heavy lifting.

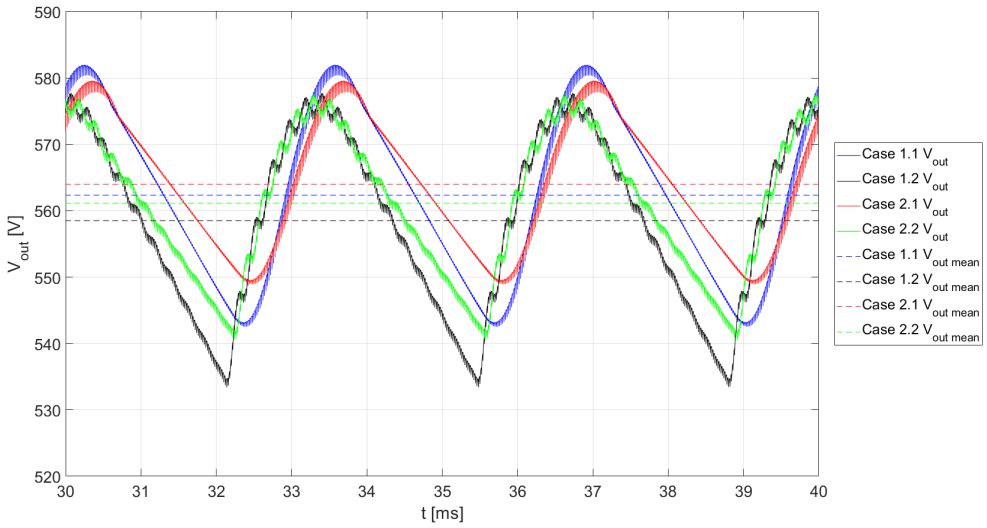


Figure 6.11: Case 1 and 2 simulated voltage ripple.

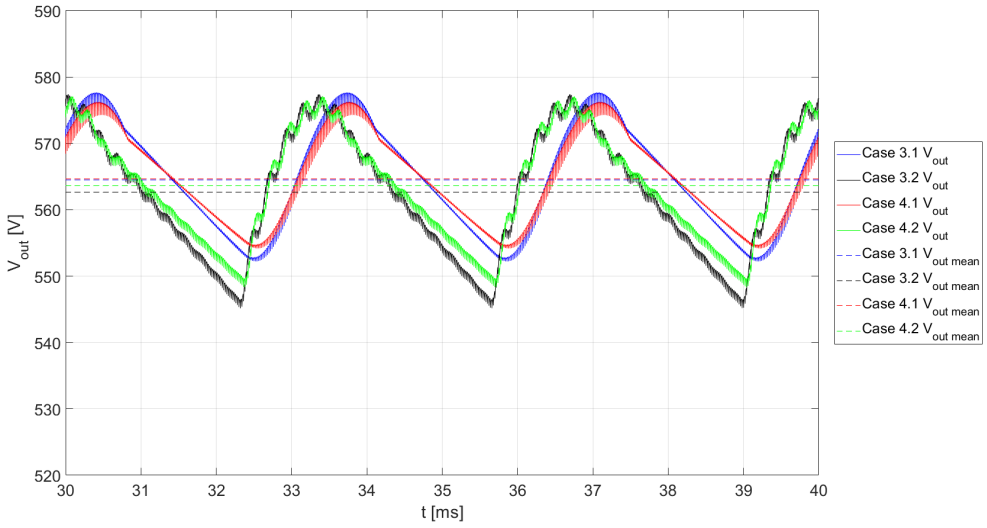


Figure 6.12: Case 3 and 4 simulated voltage ripple.

Table 6.10: Voltage ripple and peak current though each parallel branch per case.

Case #	Voltage ripple	I_{peak} per branch
1.1	7.017% (±3.509%)	11.574 A
1.2	7.946% (±3.973%)	10.748 A
2.1	5.438% (±2.719%)	8.386 A
2.2	6.584% (±3.292%)	8.779 A
3.1	4.508% (±2.254%)	6.547 A
3.2	5.732% (±2.866%)	7.348 A
4.1	3.907% (±1.953%)	5.361 A
4.2	5.107% (±5.553%)	6.287 A

As seen from the values, both case 3.1 and 4.1 meet the ripple requirement but only 4.1 has a lower peak current than the rated value of the bulk capacitor. Therefore case 4.1 is chosen as the suitable setup, i.e one 10 µF polypropylene capacitor at the output of the rectifier, one 10 µF polypropylene capacitor connected in parallel with a bank of six series connected branches of 470 µF aluminium electrolytic capacitors at the output of the boost converter, in total 1.43 mF.

6.4.2 Balancing and discharge

With several large capacitors connected in series and parallel, issues can occur with uneven voltage distribution over the capacitors as their manufacturing tolerances can be rather large. To mitigate this uneven charging, the manufacturers recommend [61] using a balancing resistor over each parallel branch through which the capacitors can discharge slowly. The resistor is designed to draw a current $i_{dis} > i_{leak}$, where i_{leak} is the leakage current through the capacitors which cause the unbalanced charge. As the built in discharge current is then defined by the resistor and not the tolerance difference in the capacitor, it can be designed such that the leakage current can be neglected. EPCOS, the electrolytic capacitor manufacturer, recommends choosing a balancing resistor according to

$$R_{balance} = 100\,\mathrm{M\Omega} * \frac{1}{\sqrt{N_p C_R}}, \tag{6.9}$$

where N_p is the number of capacitors in parallel (= 6) and C_R is the capacitance of a single capacitor in μF. For one capacitive branch the resistance becomes $R_{balance} = 8.68613384 * 10^4 \approx 86.7\,\mathrm{k\Omega}$. Worth noting is that smaller resistance would lead to a higher current and therefore a more balanced network, and a parallel branch can share the same balancing device. This balancing resistor can also double as a discharge resistor to discharge the DC-link when the charger is turned off. During discharge, the DC-link can be simplified to a RC-circuit, see Figure 6.13.

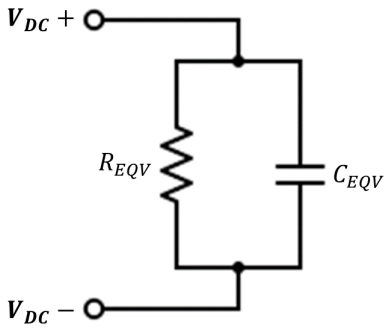


Figure 6.13: Equivalent circuit of DC-link when discharging.

With the values from the DC-link applied, RC circuit obtains $C_{EQV} = C_{DC-link} = 1.43\,\text{mF}$, and as there are two series connected parallel branches, $R_{EQV} = 2 * R_{balance} = 173.4\,\text{k}\Omega$. The discharge of a RC circuit can be can be expressed through

$$V_{discharge}(t) = V_0(1 - e^{-\frac{t}{R_{EQV}C_{EQV}}}). \tag{6.10}$$

When adding in the values from above and the highest operating voltage, $V_0 = 818.2\,\text{V}$, the time until the DC-link voltage drops below 60 V, the limit of high voltage as defined by Formula Student rules, after a shut off is 647.8 sec, or a little more than ten minutes. As this voltage is contained inside the converter, i.e not in direct contact with any output, there is no direct danger in operation with this rather slow discharge. However, as a precaution, a voltage measuring circuit which drives a couple of LEDs has been added to give a visual indication if the DC-link is charged above 30 V or not. The sensing circuit uses a high voltage MOSFET (IXYS IXTA3N150HV [62]) which acts as a switch for turning on and of two LEDs. The MOSFETs gate is controlled by a zener diode (ON MM5Z15VT1G [63]) based voltage reference which is compared to the voltage on the positive pole of the DC-link. If the DC-link voltage exceeds 30 V, the MOSFET turns on and lights up the diodes. Current limiting resistors are also in place to avoid overloading any components. The 30 V threshold was chosen as the LED circuit is based on similar circuit designed by Aros Electronics and the threshold was carried straight over. This indication will help during development and operation, as it will give a hint to the operator if the charger still has energy stored inside it and is therefore potentially dangerous.

The chosen balancing/discharge setup is small network of two series connected TE Connectivity 352227KFT [64] surface mounted 27 kΩ resistors per parallel capacitor branch, i.e four resistors in total, see Figure 6.14 for full circuit of the DC-link and Table 6.11 for symbol description.

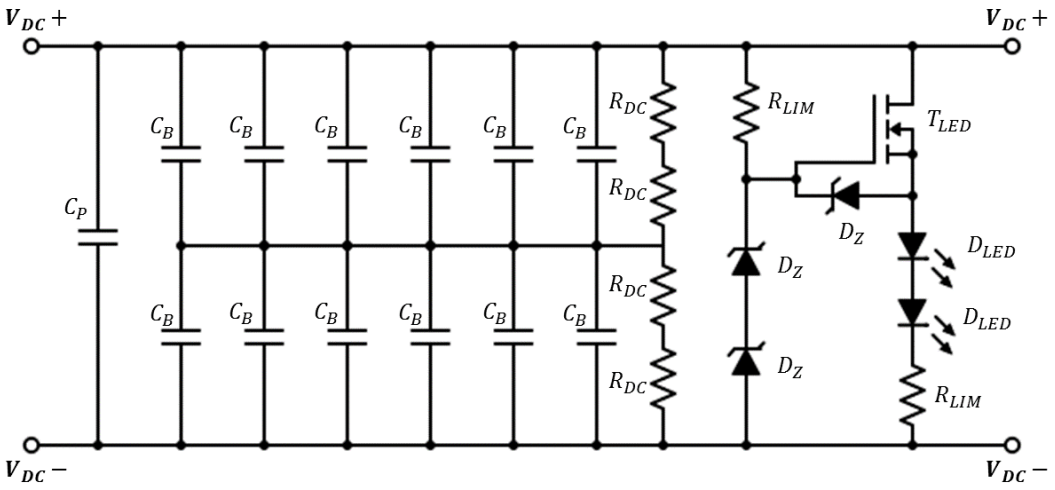


Figure 6.14: Full schematic of DC-link with balancing and LED indicator.

Table 6.11: DC-link circuit symbol description.

Symbol	Description	Value
C_P	Polypropylene capacitor	10 µH
C_B	Al electrolytic capacitor	470 µH
R_{DC}	Discharge resistor	27 kΩ
D_Z	Zener diode	N/A
R_{LIM}	Current limiting resistors	5.6 kΩ to 470 kΩ
T_{LED}	On/Off MOSFET	N/A
D_{LED}	LEDs in 1206 package	N/A

The setup sums up to $4*27\,\text{k}\Omega = 108\,\text{k}\Omega$, which is less that the that above calculated value, which as mentioned will result in a more balanced cap bank. This change in resistance also leads to cutting a little more than four minutes from the above mentioned discharge time, see Figure 6.15 for comparison of the voltage during a discharge cycle.

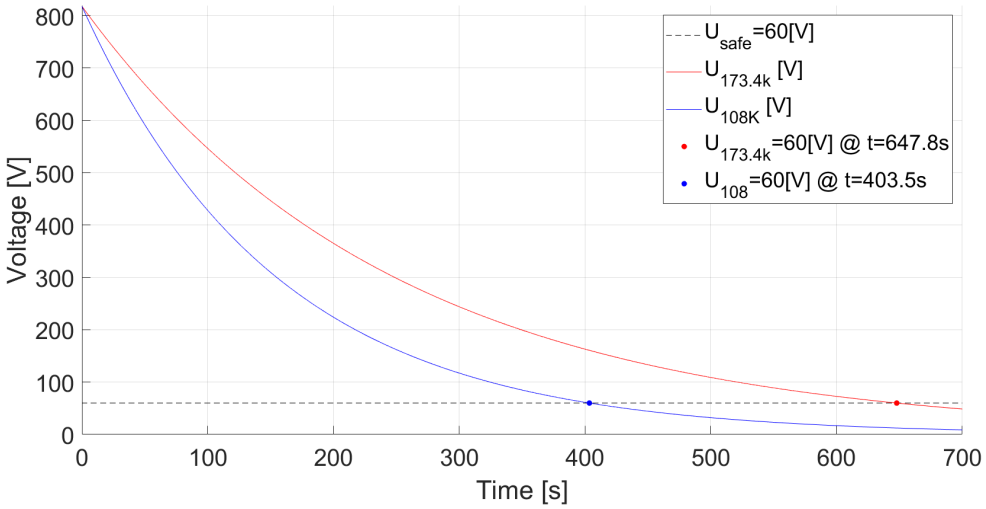


Figure 6.15: Comparison of discharge voltages over time for different discharge resistor values, red: 173.4 kΩ, blue: 108 kΩ.

The final discharge time to 60 V becomes 403.5 s (6 min and 43.5 s), which leads to a peak power dissipation per resistor of 1.55 W, which is well below the TE 352147KFT rating of 3 W.

6.4.3 Pre-charge

The purpose of the pre-charge circuit is to charge the dc-link to the voltage which is required at the start of a charging cycle. As the dc-link consists of a bank of capacitors and no current limiting elements, there will be a huge inrush current if it is directly connected to a high voltage input, such as the rectified three phase voltage supply. This current will most likely cause harm to the components in the current path, as it could be in the realms of several hundred ampere.

As a boost converter's lowest output voltage is the input voltage to the converter, it is not possible to pre-charge with just the boost stage in this design. Furthermore one of the capacitors is placed before the boost converter. A simple design for a separate charging circuit to cover the window from zero to the input voltage consists of a current limiting resistor in the current path from the input and a bypass parallel to it controlled by a relay. The boost diode is used to stop any current from flowing from the output side to the input rectifier side, see Figure 6.16 for circuit.

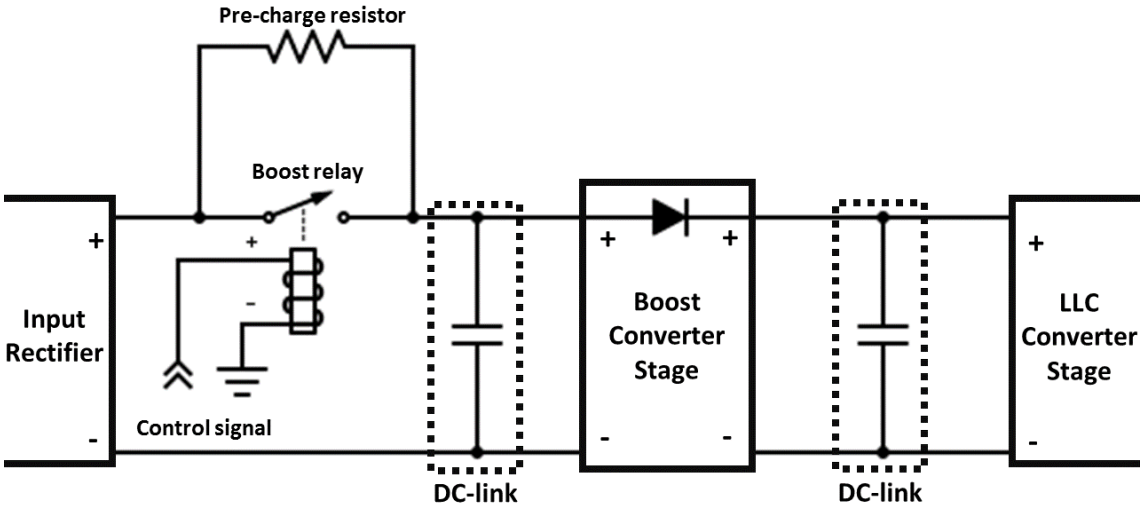


Figure 6.16: Schematic of pre-charge circuit placement in charger block schematic.

When the dc-link voltage has reached the maximum voltage that the pre-charge stage can output, the boost stage will take over and charge the dc-link up to a voltage which is sufficient for normal operation. As the resistive pre-charge will never be able to charge to the same level as the input due to voltage drops over the resistors and diode, there will be a small transitional period where there will be a current spike as the boost stage is turned on. To limit this spike, a large boost inductor value is preferred together with the soft start functions of the LM IC. There are many components on the market that would fit this application. Components chosen are:

Resistor: Ohmite TUM15J5K6E [65]. The chosen resistor is a 5.6 kΩ resistor rated for 15 W of power continuously. The resistor can be overloaded with five times the rated power for five seconds, i.e. 75 W. To reduce the time needed for pre-charge, and also the voltage drop, five of these resistors are connected in parallel. This connection gives $R_{EQV} = 1120\,\Omega$.

Relay: TE Connectivity's T9AS1D12-5 SPST [66]. This relay was chosen as it has sufficient ratings, can be PCB mounted and was available in stock.

To summarise, a pre-charge with this setup would result in a rise of the DC-link voltage seen in Figure 6.17 with a charging current running through the resistor seen in Figure 6.18. The DC-link would then be charged to 536 V, 99.63% of the input voltage in $\sim$ 11.2 s. The charging current peaks at 0.480 A at the starting point and decays as the charging takes place. The peak power put through each resistor becomes

$$P_{peak} = \left(\frac{i_{charge,max}}{N}\right)^2 * R_{res} = \left(\frac{0.48\,\text{A}}{5}\right)^2 * 5.6\,\text{k}\Omega = 51.609 \approx 52\,\text{W}. \qquad (6.11)$$

As the current decays, so will the power put through each resistor. At 5 s, the current is close to 0 A (≈ 0.0212 A) and power will be below the pre-charge resistors continuous power rating. When the DC-link is charged to the input voltage, the boost converter takes over the pre-charging, if further pre-charging is required.

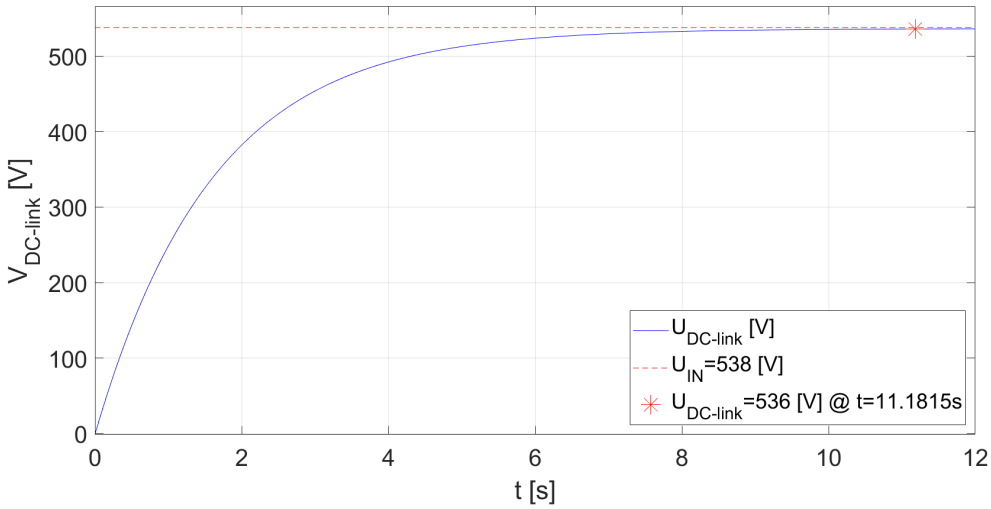


Figure 6.17: Pre-charge voltage over one pre-charging cycle with suggested setup.

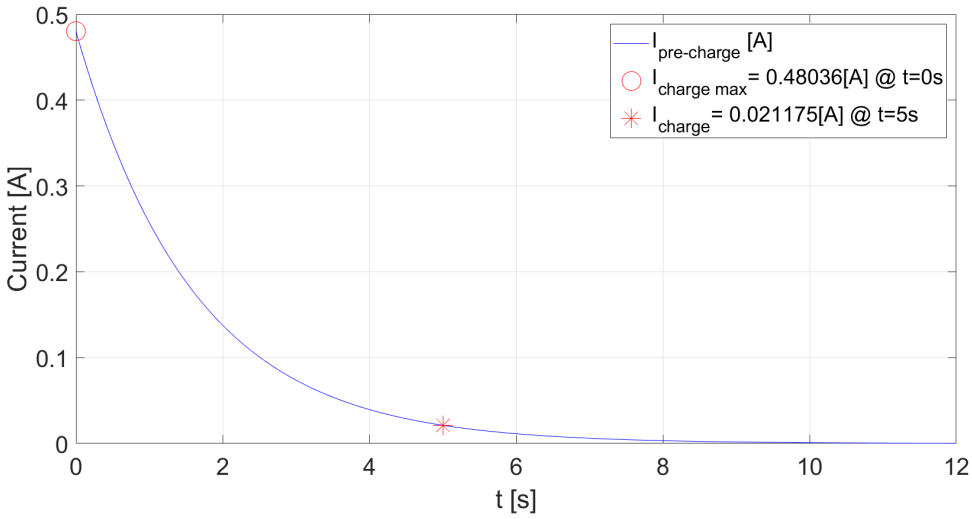


Figure 6.18: Pre-charge current during one pre-charge cycle with suggested setup.

6.5 Auxiliary circuit design

Apart from the power stages, their gate drivers, and the intermediate DC-link that bridges them, additional circuitry is required in order to build an operational battery charger. To verify the function of the charger during testing as well as monitor the state of the battery and the DC-link, voltage and current sensing should be

implemented at points where the voltages and currents are of interest. As an extra safety measure, a standalone overvoltage protection circuit is also integrated into the charger circuitry.

6.5.1 Voltage sensing

The voltages deemed most interesting during normal operation of the charger are the input voltage from the diode rectifier, the DC-link voltage and the output voltage. Out of these three voltages the first two can be measured using simple voltage dividers scaling the measured voltage down to a level that can be measured directly using the XMC processor. The output voltage does not share a ground with the XMC and therefore needs to be measured through an isolated interface. A Texas Instruments AMC1301-Q1 isolated operational amplifier is added for this purpose. A separate transformer winding on the isolated low voltage power supply (see pages 3-4 in Appendix A) is used to provide power to the operational amplifier on the output side.

6.5.2 Current sensing

Three LEM LTS 25-NP current sensors are installed in order to monitor currents in the power circuitry. One sensor is connected between the input rectifier and the boost converter, measuring the input DC current to the converter. Another sensor is connected between the output rectifier and the output connector, measuring the current flowing out of the charger and into the battery during charging. The last current sensor is inserted into the resonant tank, measuring the resonant current in order to monitor the function of the LLC converter and detect overcurrents if necessary.

6.5.3 Overvoltage protection

To lower the risk of an overvoltage happening inside the converter, the DC-link capacitor bank is equipped with an overvoltage protection circuit developed by Aros Electronics. The circuit is intended to pull down any voltage exceeding 875 V, and can be seen on page 8 in Appendix A.

6.6 Microcontroller

To turn the converter into an intelligent, programmable battery charger, the power stages should be controlled by some kind of microcontroller. The XMC4700-F144F2048 AA from Infineon Technologies is one such microcontroller, which has been used for other projects at Aros Electronics. It is therefore selected as a part of this project as well. The microcontroller is used to control the output voltage from the boost converter stage and to trigger the precharge relay. It is also used for reading all voltage and current measurements from the sensors in order to ensure safe and correct operation. An isolated CAN bus interface is connected to the XMC controller for programming and data transfer. Some pins are reserved for digital PWM/PFM

control of the boost and LLC converter stages, although discrete analog controller ICs will be used initially. The complete pin layout of the XMC microcontroller can be found on page 15 of the schematic in Appendix A.

6.7 Design phase results

The result of the converter design phase is a complete circuit schematic and one manufactured and partially tested power transformer. The transformer has been verified in terms of inductance, saturation limits and winding losses. The schematic is drawn in OrCAD Capture and can be used to create a PCB layout using other software in the same suite. All components chosen are at the time of writing available at Aros Electronics so that manufacturing of a physical converter can be completed after layouting. All parts of the complete schematics that were developed as part of this project can be found in Appendix A, Circuit Schematic.

7
Discussion

7.1 Results

Due to limited time and resources, the planned construction and verification of the converter could not take place. From the component loss comparison done in Chapter 5 it can still be concluded that the two stage converter using a boost converter feeding an LLC converter would be a feasible design for a battery charger at this power and voltage level, as all losses in the individual components are within component limits. In Chapter 6, passive components, such as the resonant capacitor, boost inductor and transformer, are also found that can handle the voltage and current stresses in the proposed converter. It is seen that utilising the high voltage rating of modern SiC MOSFETs is helpful in reducing conduction losses, since the high DC-link voltage allows a reduction of the DC-link current while maintaining output power. With regular silicon components, maximum voltage is usually limited to 600 V or less, meaning that the reduction in losses shown in the simulations would not be possible to realise with real components. It is also worth noting that the main source of losses is not in the switches but in the output rectifier bridge, as seen in Section 5.5.1. Optimising the selection of diodes for this bridge would likely be one of the easier ways to further improve efficiency. Another issue due to the time and resource constraint is that none of the converters cooling requirements has been assessed. It is subsequently unclear what type of cooling solution that would be needed. However, as the active components all come in a standard TO-247 package, there are several of the shelf heat sinks that would fit and therefore could be used as a starting point. Regarding the size of the converter, it seems likely from the size and weight of individual components that it could fulfil the requirement of being small enough to be mounted on a hand cart. The magnetic components, in particular the transformer and the boost inductor, add considerably to the total size and weight, and reducing the size of these component would provide another major benefit to the design.

7.2 Future Work

The first step in a future continuation of the project will be to make a PCB layout from the schematic and manufacture said PCB. This PCB will have to be thoroughly checked at each assembly stage as more and more components are added on. If a design fault is detected, an iterative process should be used to update the hardware to a functioning state.

A system for monitoring and control of the charger needs to be developed before the charger can be used. Such a system must take into account both the pre-programmed values for charging voltage and current as well as real time data about the state of the charger, such as output voltage and current.
This system also needs to react to fault conditions, such as over- or undervoltage, or an open circuit. The system with sensors and control hardware therefore needs to be fast enough to react to such conditions before a situation becomes dangerous to the operator, or causes damage to the battery or the charger itself. The user interface should allow the user to set all programmable parameters before charging and to monitor the charging sequence. An interface between the charger and the Battery Management System (BMS) can also be developed. This would provide additional information to the charger, such as the voltage of individual battery cells, which could help optimise charging. This is however not necessary for safe operation of the charger, as the BMS is always able to interrupt charging by disconnecting the battery output.

Before it is used on a real battery, the complete charger will need be thoroughly tested in different situations. As one of the stated applications of the charger is to be used in Formula Student projects, it must be safe to operate by members of teams participating in such projects. Among other regulations, the safety requirements given by the competitions demand that there is sufficient electrical insulation between high voltage and low voltage systems, and that it is physically impossible to touch high voltage terminals or other components on potential when the system is assembled and in use. Testing of the charger must therefore be done with emphasis on these, and other, safety criteria to ensure safe operation. If the charger is to be taken into operation within Formula Student, it is the moral responsibility of the designers to ensure safe operation of the device to their best extent, both in the design and construction of the device itself and in the development of relevant documents such as instruction manuals.

Furthermore, the testing must also incorporate software development to ensure a safe charging cycle, as the charger is connected to a fire hazard which is both hard to extinguish and could possibly explode [67]. The charger should not jeopardise the state of health of the battery that is charging and not push it towards any unsafe working conditions. The cooling requirements should also be assessed during testing, to ensure stable operation of the charger itself.

7.3 Future improvements to design

As for now, the switching frequency of the boost converter is rather low, set to 50 kHz. With the current design, it should be able to switch faster, however this was not investigated. The increase of said frequency could reduce the size of the inductor in the power stage and decrease the current ripple into the DC-link. The same is true for the LLC converter and its inductors and transformer.

As the development of SiC components advance even further, the design presented in the report can be improved by the use of higher operating voltages. As mentioned in the design part, the 1700 V components that are on the market were not available in stock. If one would use those components, one would be able to push the boost converter further such that it can output a higher voltage. This can then be used in different ways in the transformer, increasing the output voltage range in either direction. More form factors of the components will also be available. The TO-247 package that all of the SiC components came with in this design takes some space and does need to be placed with care on a PCB to achieve proper cooling. When SiC devices become available in module packages, such as the SOT-227-4, one would be able to make the PCB smaller and possibly easier to cool. As the charger application for vehicles probably lays with on-board chargers in the future, the size and weight of said charger will start to make a difference and the availability of the different form factors will be one of the key parts in transition towards this solution.

Another step the charger needs to take before it is launched in any commercial way, is to develop active power factor correction (APFC) control of the boost stage. With the rectifying bridge on the input and without any PFC control, the power factor will be relatively low and will draw unnecessary reactive power from the grid. With a PFC control, this can be raised to 0.99 [68]. This could possibly be done by using the XMC processor as the control IC for the boost converter rather than the LM IC that is used now.

8

Conclusion

The purpose of this project was to evaluate the feasibility of developing a high voltage battery charger using high powered SiC components as switches and rectifying diodes. During the project, different topologies have been compared in order to find the most efficient one. It is found that the two stage converter utilising a boost converter as its primary, voltage regulating stage and an LLC resonant converter operating at unity voltage gain is a suitable topology for the charger. Compared to a buck converter based solution it should be able to operate with lower losses and overall less component stress.

Running with the full output current of 20 A for voltages between 400 V and 450 V, the losses in the active components are found to be between 302.4 W and 303.1 W in the buck based converter and between 187.1 W and 195.7 W for the boost based converter. At the maximum voltage operating point of 600 V and 15 A, the losses are 191.4 W for the buck based converter and 165.7 W for the boost based converter. It can be seen that while the voltage stress on the components are higher in the boost based converter, the currents flowing through the switches are significantly higher in the buck based converter. At full output current in the buck based converter, the RMS current through the buck MOSFET is 22.74 A and the current through each LLC bridge MOSFET is 19.24 A. For comparison the currents through the boost MOSFET and corresponding LLC switches are 6.11 A and 11.59 A, respectively.

The chosen topology has then been further developed into a complete circuit schematic with real components and supporting circuitry such as controller ICs, sensors and more. Some of the components such as the SiC active components and the controllers have been purchased in anticipation of manufacturing a prototype of the charger.

A prototype power transformer has been manufactured and tested. This transformer is found likely to be suitable for use in the designed LLC converter, although testing at full power is yet to be done. The conduction losses are found to be 7.2 W, causing the operating temperature to stabilize at 39.6 °C in a low voltage test. The saturation limit is found to be 0.0077 V s.

References

[1] Formula Student Germany Executive Committee. (2018). "Formula Student Germany rules 2018", [Online]. Available: https://www.formulastudent.de/fileadmin/user_upload/all/2018/rules/FS-Rules_2018_V1.1.pdf (visited on 01/22/2018).

[2] EVObsession EV sales report. (2017). "US, Europe & China electric car sales in 2016", [Online]. Available: https://evobsession.com/us-europe-china-electric-car-sales-2016/ (visited on 02/08/2018).

[3] Nissan North America. (2017). "2017 LEAF First Responder's Guide", [Online]. Available: https://owners.nissanusa.com/content/techpub/ManualsAndGuides/LEAF/2017/2017_LEAF-first-responders-guide.pdf (visited on 01/22/2018).

[4] Tesla Motors. (2016). "2016 Model S Emergency Response Guide", [Online]. Available: https://www.tesla.com/sites/default/files/pdfs/first_responders/2016_Models_S_Emergency_Responders_Guide_en.pdf (visited on 01/22/2018).

[5] A. Kork. (2016). "Deep dive: The 2017 Chevrolet Bolt's electric powertrain", [Online]. Available: https://www.cnet.com/roadshow/news/deep-dive-2017-chevrolet-bolt-electric-powertrain/ (visited on 01/23/2018).

[6] IEA Publishing © OECD/IEA, Licence: www.iea.org/t&c. (2017). "Global EV Outlook 2017, Two million and counting", [Online]. Available: https://www.iea.org/publications/freepublications/publication/%5C%5CGlobalEVOutlook2017.pdf (visited on 01/22/2018).

[7] Digi-Key Electronics. (2016). "Silicon Carbide (SiC): History and Applications", [Online]. Available: https://www.digikey.com/en/articles/techzone/2016/dec/silicon-carbide-history-and-applications (visited on 02/12/2018).

[8] ROHM Co. Ltd. (2014). "SiC Power Devices and Modules", [Online]. Available: http://rohmfs.rohm.com/en/products/databook/applinote/discrete/sic/common/sic_appli-e.pdf (visited on 02/12/2018).

[9] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer, 2001, ISBN: 0792372700.

[10] *Electromagnetic compatibility (EMC) - Part 3-2: Limits for harmonic current emissions (equipment input current up to and including 16 A per phase)*, Svenska Elektriska Kommissionen, 2001.

[11] EVObsession EV sales report. (2018). "Formula Student Germany Competition Handbook 2018", [Online]. Available: https://www.formulastudent.de/fileadmin/user_upload/all/2018/rules/FSG2018_Competition_Handbook_V1.0.pdf (visited on 02/09/2018).

[12] E.ON Energidistribution. (2017). "Välj rätt huvudsäkring", [Online]. Available: https://www.eon.se/huvudsakring# (visited on 02/12/2018).

[13] Vattenfall. (2018). "Välj rätt huvudsäkring", [Online]. Available: https://www.vattenfalleldistribution.se/el-hem-till-dig/valj-ratt-huvudsakring/ (visited on 02/12/2018).

[14] Isidor Buchmann. (2017). "BU-409: Charging Lithium-ion", [Online]. Available: http://batteryuniversity.com/learn/article/charging_lithium_ion_batteries (visited on 02/12/2018).

[15] C. Mi, M. A. Masrur, and D. W. Gao, *Hybrid Electric Vehicles: Principles and Applications with Practical Perspectives*. Wiley, 2011, ISBN: 0470747730.

[16] C. Shi, H. Wang, S. Dusmez, and A. Khaligh, "A sic-based high-efficiency isolated onboard pev charger with ultrawide dc-link voltage range", *IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS*, vol. 53, no. 1, 2017.

[17] B. T. Lynch. (2008). Under the Hood of a DC/DC Boost Converter, Texas Instruments, [Online]. Available: http://www.ti.com/download/trng/docs/seminar/Topic_3_Lynch.pdf (visited on 03/02/2018).

[18] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. Wiley, 2002, ISBN: 0471226939.

[19] A. Martin, M. Davis-Marsh, G. Pinto, and I. Jorio. (2012). CAPACITOR SELECTION FOR DC/DC CONVERTERS: WHAT YOU NEED TO KNOW TO PREVENT EARLY FAILURES, AND REDUCE SWITCHING NOISE, SIMPLE SWITCHER Applications, [Online]. Available: http://www.kemet.com/Lists/TechnicalArticles/Attachments/5/Avnet2012PowerForum_CapacitorsSelection.pdf (visited on 05/23/2018).

[20] *Working with boost converters*, Texas Instruments, Jun. 2015. [Online]. Available: http://www.ti.com/lit/an/snva731/snva731.pdf (visited on 05/25/2018).

[21] J. Falin, *Designing DC/DC converters based on SEPIC topology*, Texas Instruments, 2008.

[22] D. Zhang, *Designing a SEPIC Converter*, AN-1484, Texas Instruments, May 2006.

[23] H. Huang, "Designing an llc resonant half-bridge power converter", *Texas Instruments Power Supply Design Seminar*, 2010.

[24] S. Abdel-Rahman, *Resonant LLC Converter: Operation and Design*, AN 2012-09, V 1.0, Infineon Technologies North America, Sep. 2012.

[25] H. Choi, *Design Considerations for an LLC Resonant Converter*, Fairchild Semiconductor, 2007.

[26] H. Wang, "Highly efficient sic based onboard chargers for plug-in electric vehicles", PhD thesis, University of Maryland, College Park, 2014.

[27] ROHM Semiconductor. (2016). "Calculation of Power Loss (Synchronous)", [Online]. Available: http://rohmfs.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/power_loss_appli-e.pdf (visited on 02/20/2019).

[28] J. Liu, J. Mookken, and K. L. Wong, "Highly efficient, and compact zvs resonant full bridge converter using 1200v sic mosfets", *PCIM Europe 2014*, May 2014.

[29] A. Greifelt, G. Heiland, and D. Gerling, "Modular 11kw bidirectional onboard charger with sic-mosfet technology for mobile applications", Nov. 2017, pp. 1–6. DOI: 10.1109/COBEP.2017.8257237.

[30] H. Wang, S. Dusmez, and A. Khaligh, "Design and analysis of a full-bridge llc-based pev charger optimized for wide battery voltage range", *IEEE TRANSACTIONS ON VEHICULAR TECHNOLOGY*, vol. 63, no. 4, May 2014.

[31] J.-H. Park and K.-B. Lee, "A two-stage bidirectional dc/dc converter with sic-mosfet for vehicle-to-grid (v2g) application", Oct. 2017, pp. 288–293. DOI: 10.1109/CENCON.2017.8262500.

[32] Cree Wolfspeed. (2018). "C2M0045170D Silicon Carbide Power MOSFET", [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/960/product/207/c2m0045170d.pdf (visited on 10/02/2018).

[33] ——, (2015). "C3D25170H–Silicon Carbide Schottky Diode", [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/103/product/75/c3d25170h.pdf (visited on 10/02/2018).

[34] ——, (2018). "C2M0045170P Silicon Carbide Power MOSFET", [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/1237/product/285/c2m0045170p.pdf (visited on 10/02/2018).

[35] GeneSic Semiconductor. (2018). "GB25MPS17-247 1700 V Silicon Carbide Schottky Diode", [Online]. Available: http://www.genesicsemi.com/sic_rectifiers_diodes/merged_pin_schottky/GB25MPS17-247.pdf/ (visited on 10/02/2018).

[36] Cree Wolfspeed. (2018). "C2M0080170P Silicon Carbide Power MOSFET", [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/1238/product/286/c2m0080170p.pdf (visited on 10/02/2018).

[37] GeneSic Semiconductor. (2018). "GB50MPS17-247 1700 V Silicon Carbide Schottky Diode", [Online]. Available: http://www.genesicsemi.com/sic_rectifiers_diodes/merged_pin_schottky/GB50MPS17-247.pdf (visited on 10/02/2018).

[38] Cree Wolfspeed. (2018). "C2M0025120D Silicon Carbide Power MOSFET", [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/161/product/8/c2m0025120d.pdf (visited on 10/02/2018).

[39] ——, (2015). “C4D40120D Silicon Carbide Schottky Diode”, [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/109/product/79/c4d40120d.pdf (visited on 10/02/2018).

[40] GeneSic Semiconductor. (2018). “GR25MT12K N-channel SiC power MOSFET”, [Online]. Available: http://www.genesicsemi.com/sic_transistors/mosfet/GR25MT12K.pdf (visited on 10/02/2018).

[41] ——, (2018). “GC50MPS12 SiC Schottky Barrier Diode”, [Online]. Available: http://www.genesicsemi.com/sic_rectifiers_diodes/merged_pin_schottky/GC50MPS12-247.pdf (visited on 10/02/2018).

[42] ROHM. (2018). “SCT3030KL N-channel SiC power MOSFET”, [Online]. Available: https://www.rohm.com/datasheet/SCT3030KL/sct3030kl-e (visited on 10/02/2018).

[43] ——, (2015). “SCS240KE2 SiC Schottky Barrier Diode”, [Online]. Available: https://www.rohm.com/datasheet/SCS240KE2/scs240ke2-e (visited on 10/02/2018).

[44] Littelfuse. (2017). “LSIC1MO120E0080 SiC power MOSFET”, [Online]. Available: http://www.littelfuse.com/~/media/electronics/datasheets/power_semiconductors/littelfuse_power_semiconductor_silicon_carbide_lsic1mo120e0080_datasheet.pdf.pdf (visited on 10/02/2018).

[45] ——, (2018). “LSIC2SD120E30CC SiC Schottky Barrier Diode”, [Online]. Available: http://www.littelfuse.com/~/media/electronics/datasheets/power_semiconductors/littelfuse_power_semiconductor_sic_schottky_lsic2sd120e30cc_datasheet.pdf.pdf (visited on 10/02/2018).

[46] STMicroelectronics. (2017). “SCT30N120 SiC power MOSFET”, [Online]. Available: https://www.st.com/content/ccc/resource/technical/document/datasheet/group3/6f/96/4f/95/a0/02/42/56/DM00053079/files/DM00053079.pdf/jcr:content/translations/en.DM00053079.pdf (visited on 10/02/2018).

[47] ——, (2018). “STPSC20H12 SiC Schottky Barrier Diode”, [Online]. Available: https://www.st.com/content/ccc/resource/technical/document/datasheet/group3/32/a4/82/fa/7b/f8/49/04/DM00295145/files/DM00295145.pdf/jcr:content/translations/en.DM00295145.pdf (visited on 10/02/2018).

[48] Texas Instruments. (2008). “UCC25600 8-Pin High-Performance Resonant Mode Controller”, [Online]. Available: http://www.ti.com/lit/ds/symlink/ucc25600.pdf (visited on 03/22/2018).

[49] ON Semiconductor. (2012). “FAN7631 Advanced Pulse Frequency Modulation (PFM) Controller for Half-Bridge Resonant Converters”, [Online]. Available: https://www.onsemi.com/pub/Collateral/FAN7631-D.pdf (visited on 03/30/2019).

[50] Infinion. (2010). “ICE2HS01G High Performance Resonant Mode Controller”, [Online]. Available: https://www.infineon.com/dgdl/Infineon-ICE2HS01G-DS-v02_01-en.pdf?fileId=db3a30432a40a650012a458289712b4c (visited on 03/30/2019).

[51] *Cree C2M SiC MOSFET PSPICE MODEL Quick start guide*, Cree Wolfspeed, Feb. 2018. [Online]. Available: https://usermanual.wiki/Document/Wolfspeed20SiC20Mosfet20OrCad20Pspice20Model20Quick20Start20Guide2020Rev201020 2143847398.pdf (visited on 04/25/2018).

[52] FerroxCube. (2010). “FerroxCube Design Tool”, [Online]. Available: https://www.ferroxcube.com/en-global/design_tool/index (visited on 03/17/2018).

[53] ——, (2008). “FerroxCube data sheet 3C94 material specification ”, [Online]. Available: https://www.ferroxcube.com/upload/media/product/file/MDS/3c94.pdf (visited on 04/17/2018).

[54] ——, (2018). “FerroxCube - Materials Power Conversion - Low Freq”, [Online]. Available: https://www.ferroxcube.com/en-global/ak_material/index/power_conversion (visited on 04/23/2018).

[55] ON Semiconductor. (2017). “FFSH40120ADN-F155 Silicon Carbide Schottky Diode”, [Online]. Available: https://www.onsemi.com/pub/Collateral/FFSH40120ADN-D.PDF (visited on 05/18/2018).

[56] Texas Instruments. (2006). “LM5020 100V Current Mode PWM Controller”, [Online]. Available: http://www.ti.com/lit/ds/symlink/lm5020.pdf (visited on 03/22/2018).

[57] Liteon Opto-electronics. (2018). “Photocoupler Product Data Sheet LTV-2X7 series”, [Online]. Available: https://www.mouser.se/datasheet/2/239/Lite-On-07-31-2018-LTV-2X7_sereis_Apr18-1384800.pdf (visited on 05/07/2018).

[58] EPCOS/TDK. (2018). “Metallized Polypropylene Film Capacitors (MKP)”, [Online]. Available: https://en.tdk-electronics.tdk.com/inf/20/20/db/fc_2009/MKP_B32651_658.pdf (visited on 12/02/2018).

[59] ——, (2016). “Aluminum electrolytic Snap-in capacitors”, [Online]. Available: https://en.tdk-electronics.tdk.com/inf/20/30/db/aec/B43642.pdf (visited on 05/10/2018).

[60] Vishay. (2018). “Metallized Polypropylene Film Capacitor DC-Link Capacitor”, [Online]. Available: https://www.vishay.com/docs/26015/mkp1848cdclink.pdf (visited on 05/10/2018).

[61] *Aluminum Electrolytic Capacitors General technical information*, EPCOS TDK, Dec. 2016. [Online]. Available: https://de.tdk.eu/download/185386/5f33d2619fa73419e2a4af562122e90c/pdf-generaltechnicalinformation.pdf (visited on 03/25/2018).

[62] IXYS Corporation. (2018). “High Voltage Power MOSFET”, [Online]. Available: http://ixapps.ixys.com/DataSheet/IXTA3N150HV.pdf (visited on 05/10/2018).

[63] ON Semiconductor. (2018). “MM5ZxxxT1G Series Zener Voltage Regulators”, [Online]. Available: https://www.onsemi.com/pub/Collateral/MM5Z2V4T1-D.PDF (visited on 05/12/2018).

[64] TE Connectivity. (2015). “SMD Power Resistors Type 3522 Series”, [Online]. Available: https://www.mouser.se/datasheet/2/418/NG_DS_9-1773463-7_B-1113509.pdf (visited on 05/10/2018).

[65] Ohmite. (2015). “Ohmite TUM/TUW Series Ceramic Housed Axial Terminal Power”, [Online]. Available: https://datasheet.octopart.com/TUW7JR27E-Ohmite-datasheet-27849336.pdf (visited on 05/10/2018).

[66] TE Connectivity. (2015). “TE T9A Series, DC Coil 30A PCB or Panel Mount Relay”, [Online]. Available: https://www.mouser.se/datasheet/2/418/NG_DS_1308242_T9A_0312-199688.pdf (visited on 05/10/2018).

[67] Federal Aviation Administration. (2013). “Extinguishment of Lithium Batteries”, [Online]. Available: https://www.fire.tc.faa.gov/pdf/systems/May13Meeting/Hill-0513-ExtinguishmentofLithiumBatteriesrev2.pdf (visited on 02/13/2018).

[68] Y. Suzuki, T. Teshima, I. Sugawara, and A. Takeuchi, “Experimental studies on active and passive pfc circuits”, *Telecommunications Energy Conference*, Oct. 1997.

A

Circuit schematic

This appendix contains the full circuit schematic of the designed battery charger.

Page 1 shows all power and signal connectors, as well as mounting holes for the large magnetic components, i.e the transformer and power inductors.

Pages 2 to 4 contain the schematic of a low voltage power supply providing power to all controllers, gate drivers and other low voltage circuitry. Everything on these pages is previously developed by Aros Electronics and has not been designed as part of this project.

Pages 5 and 6 describe the boost converter stage and its associated controller IC with supporting circuitry.

On page 7 is the capacitor bank complete with mounting holes for the precharge resistors and an LED circuit indicating the presence of high voltage on the capacitor bank. The circuit has been updated after the schematic were made, and as such the schematic in Section 6.4 shall be used.

Page 8 contains the overvoltage protection circuit developed by Aros Electronics. This circuit design is also not part of the project but added for safety reasons.

Pages 9 and 10 cover the LLC converter stage with controller IC and additional components.

Page 11 shows the gate driver circuitry for both converter stages. The bootstrap circuits used on the high-side gate drivers of the LLC converter are developed by Aros Electronics.

Pages 12 and 13 contain the voltage and current measurement points. The non-isolated voltage measurement devices were taken from a previous project at Aros Electronics. The isolated measurement circuit was developed in the project.

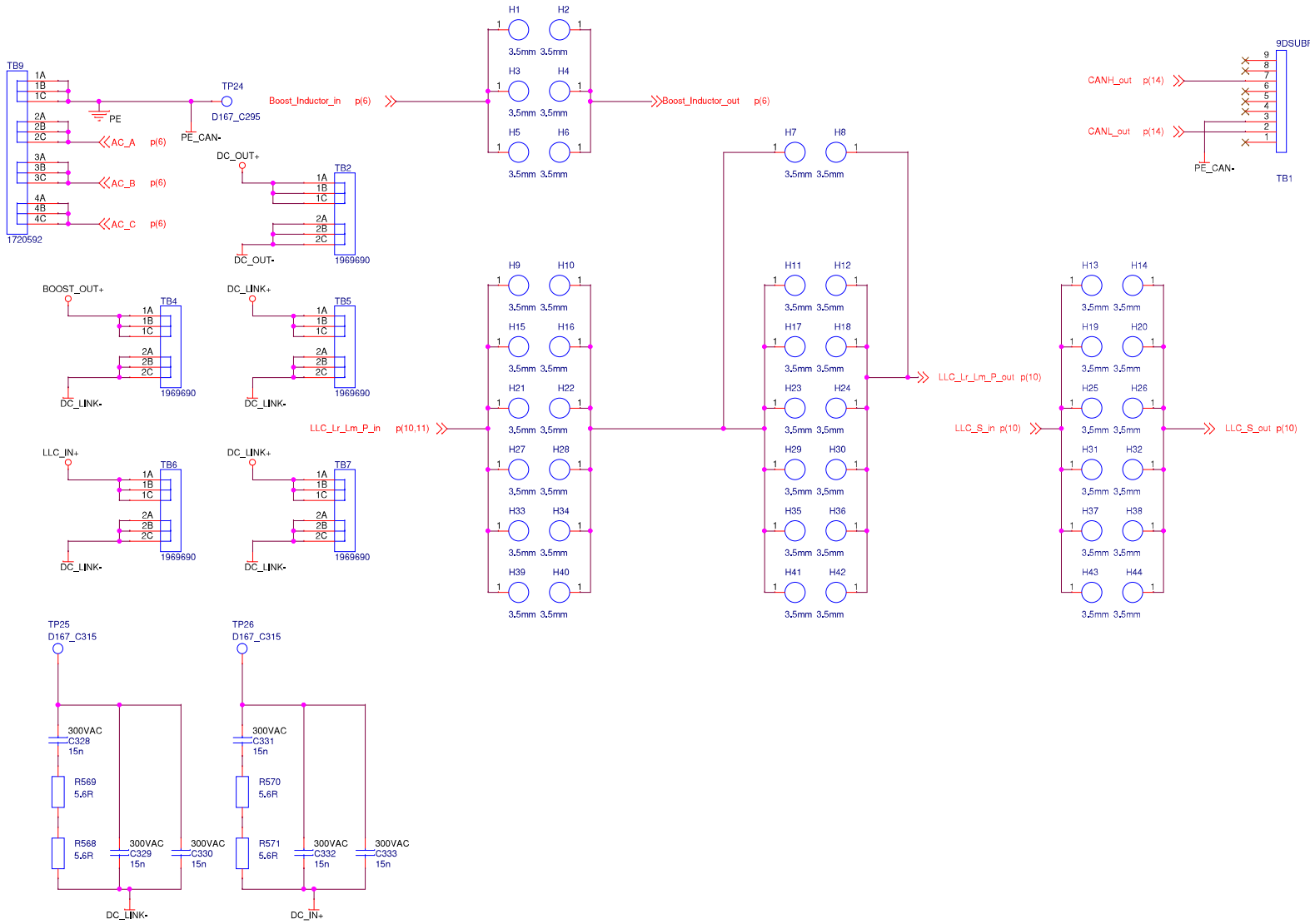
On page 14 is an isolated CAN interface for communicating with the XMC micro-controller. It was originally developed by Aros Electronics for a different project.

Page 15 contains the XMC microprocessor with all its inputs and outputs. This processor has been used in other projects by Aros Electronics and some auxiliary circuitry has been reused.

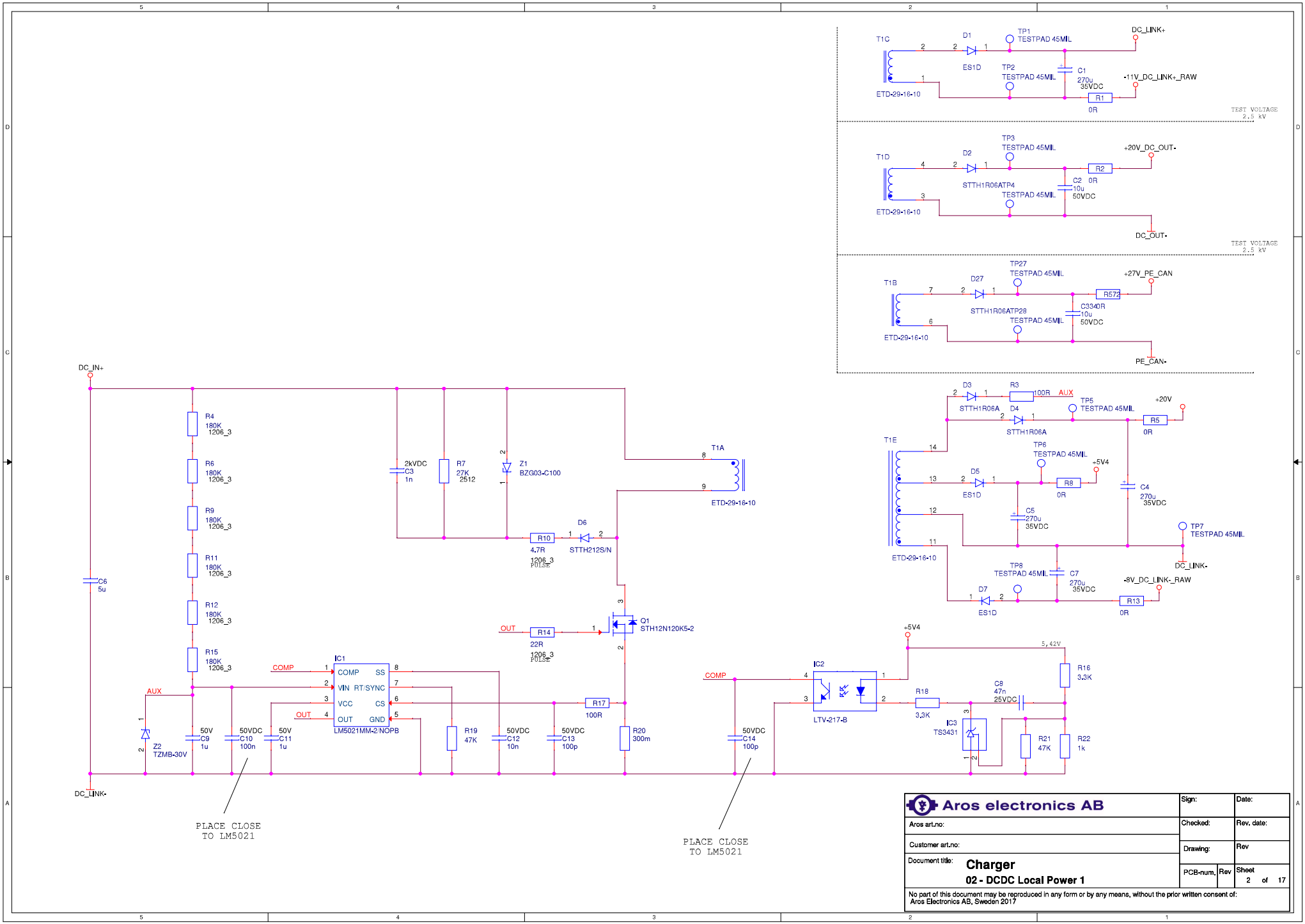
A.1 Schematic update list

Due to minor design changes late in the project, the circuit schematic attached in this appendix is somewhat out of date. Below follows a list of updated subcircuits with updated design explanations.

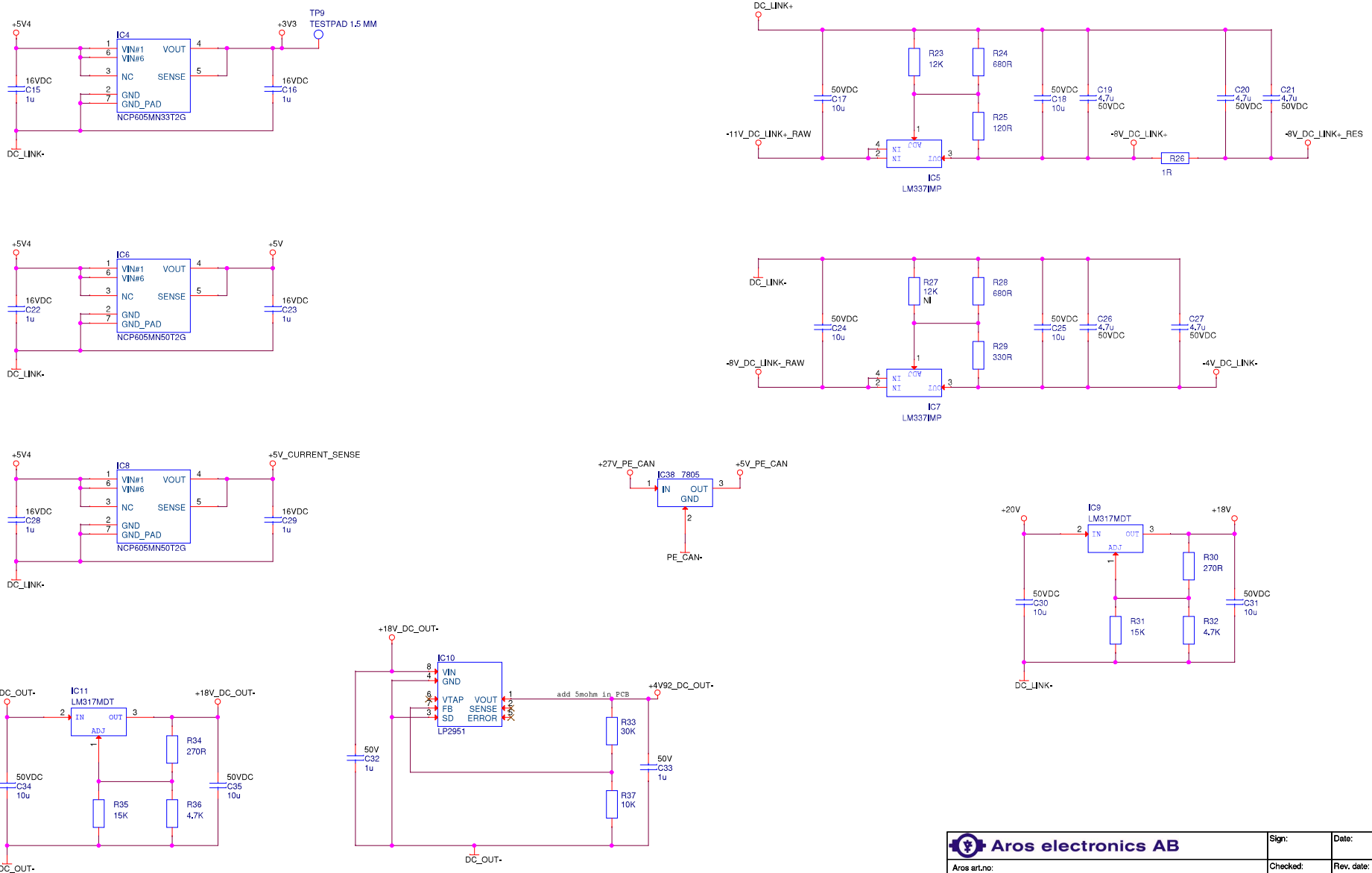
- Page 7, precharge diode D25 has been discarded completely, function replaced by boost converter diode.
- Page 7, number of capacitors in DC-link have increased and number of resistors in balancing circuit has decreased, see Figure 6.14 for updated circuit.
- Page 11, all gate drivers should be supplied from PWM_POWER_H_BOOST, not PWM_POWER_L_BOOST.



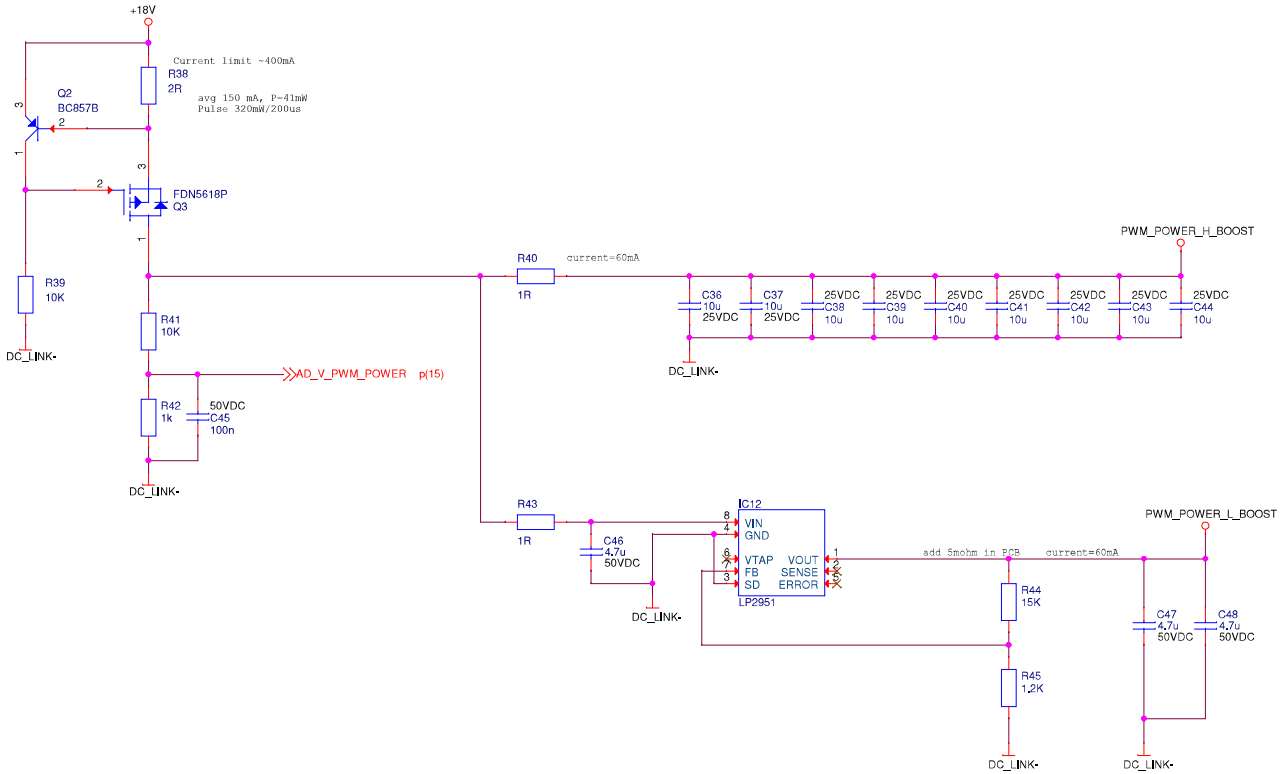
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **01 - Connectors**	PCB-num. / Rev		Sheet 1 of 17



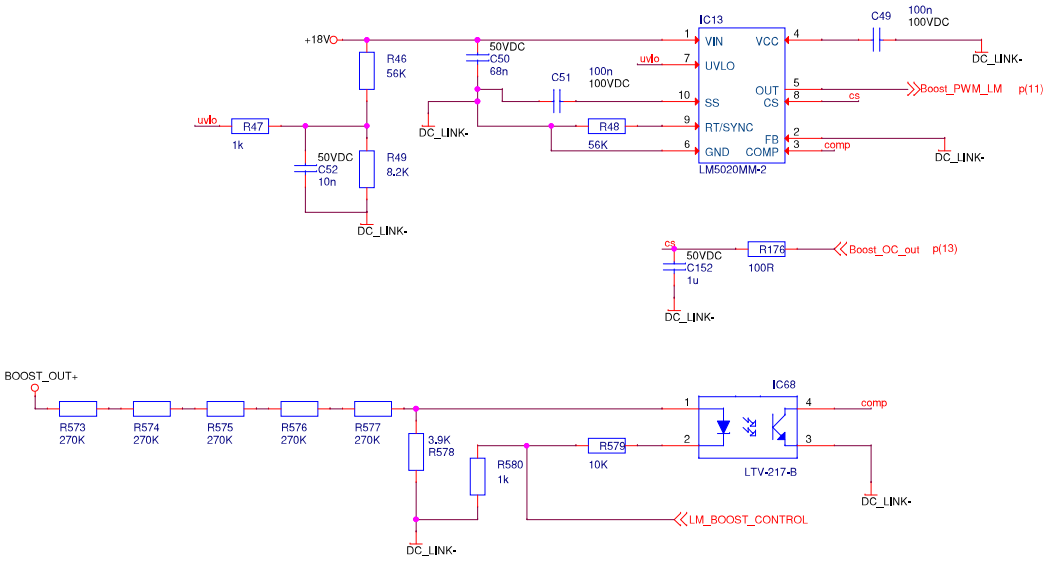
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **02 - DCDC Local Power 1**		PCB-num.	Rev / Sheet 2 of 17



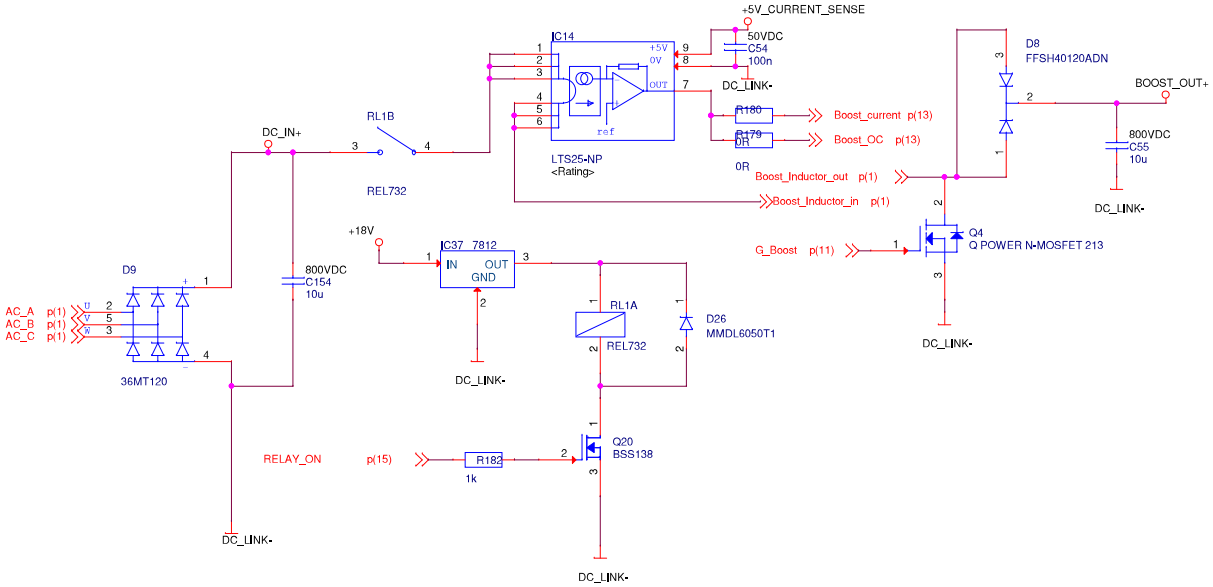
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **03 - DCDC Local Power 2**	PCB-num.	Rev	Sheet 3 of 17



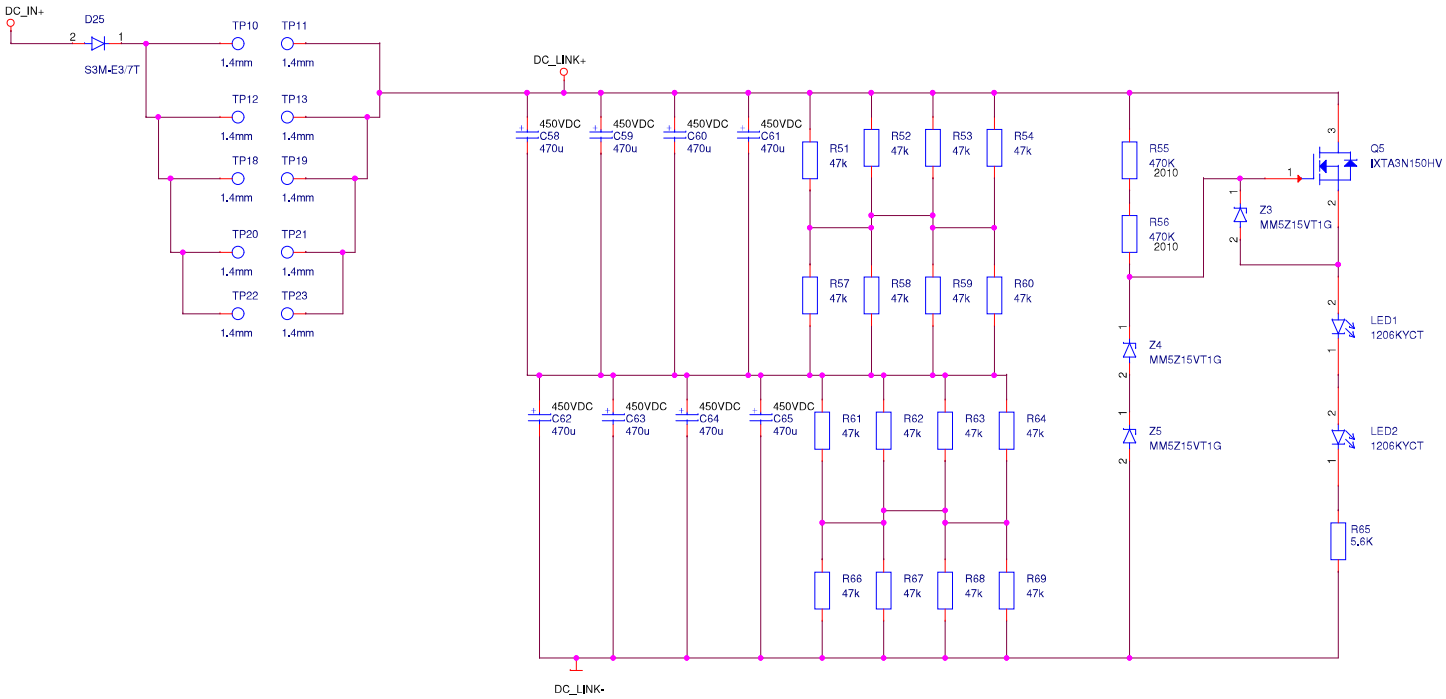
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **04 - PWM power**	PCB-num. / Rev		Sheet 4 of 17



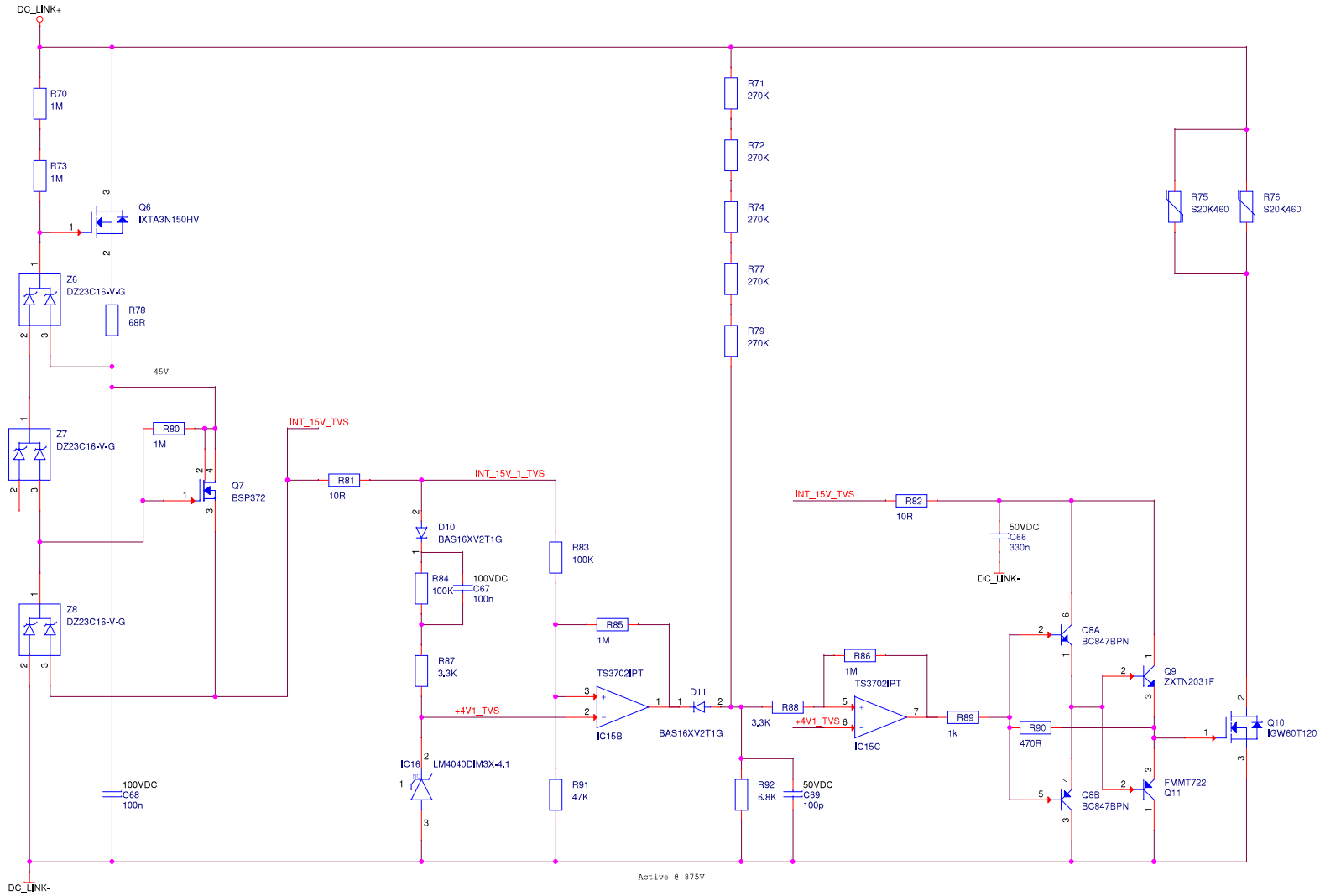
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **05 - Boost control**	PCB-num. / Rev		Sheet 5 of 17



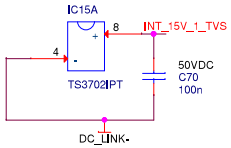
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **06 - Boost power**	PCB-num.	Rev	Sheet 6 of 17



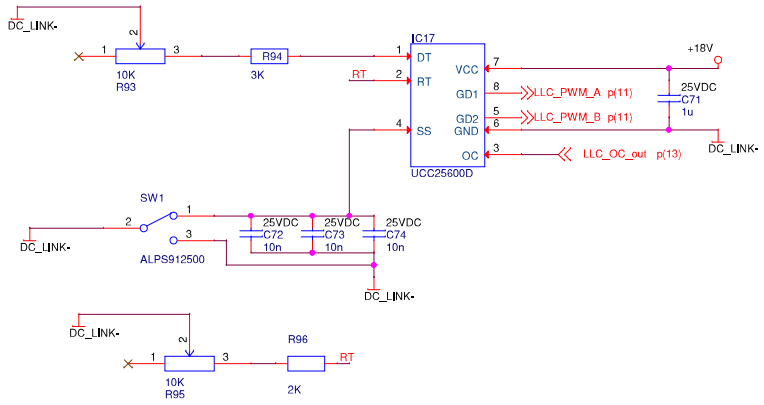
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **07 - Capacitor bank**	PCB-num.	Rev Y	Sheet 7 of 17



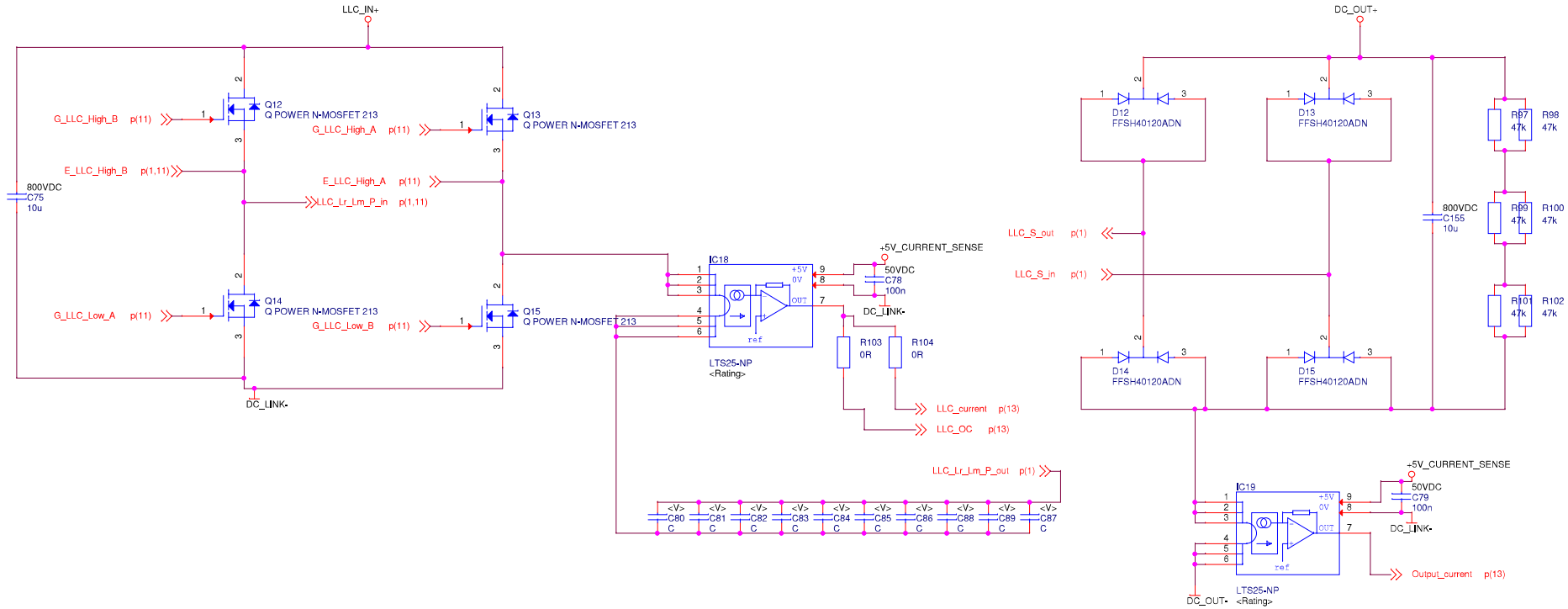
ska bytas till ts3702
dual komparator



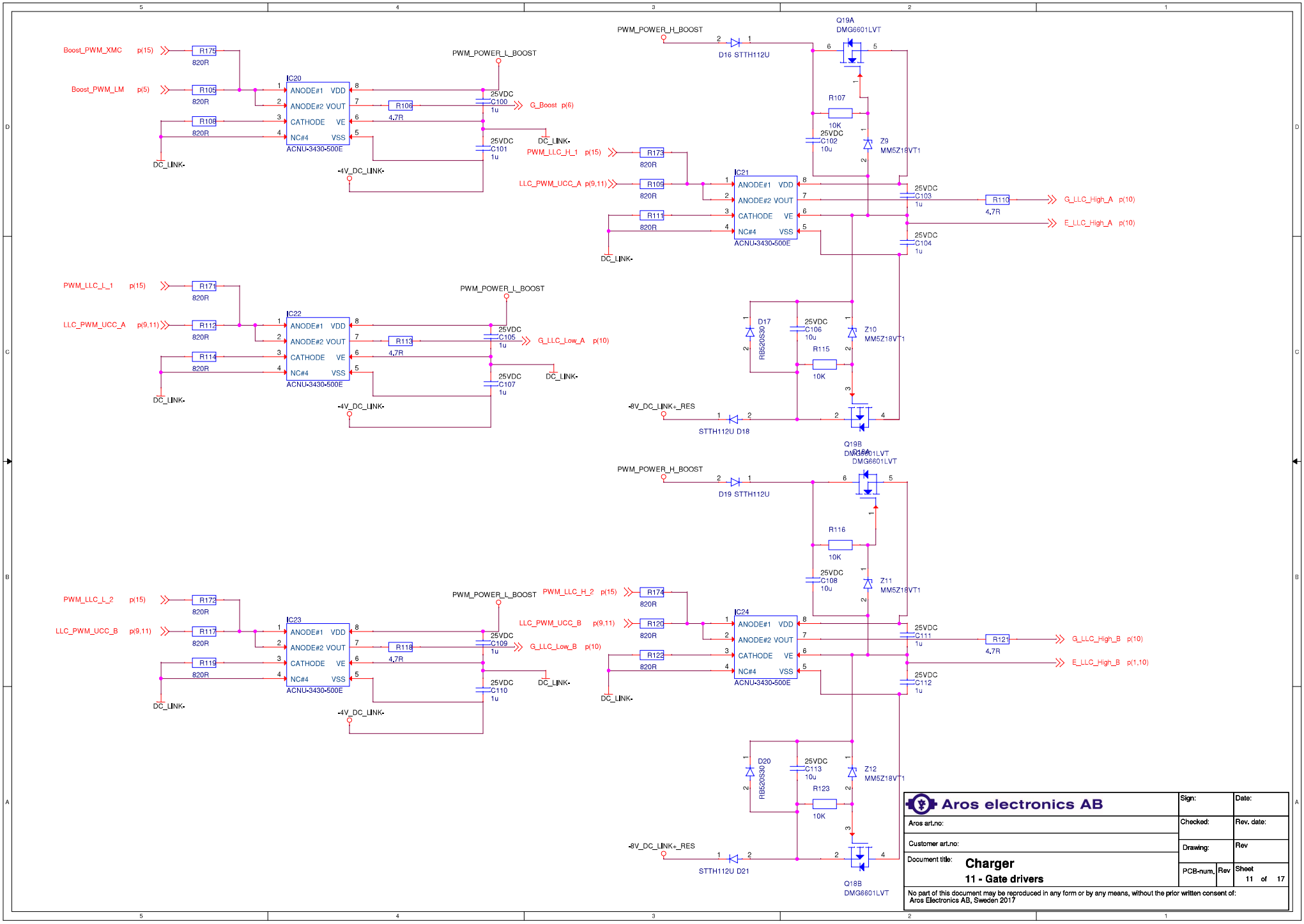
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **08 - Over Voltage Protection**		PCB-num. / Rev	Sheet 8 of 17



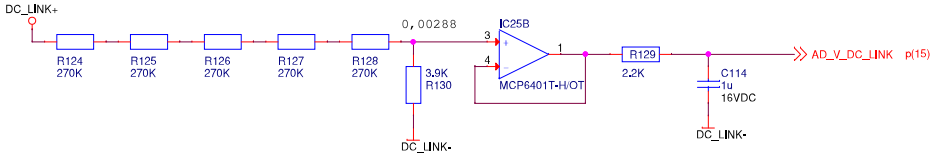
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **09 - LLC control**	PCB-num. / Rev		Sheet 9 of 17



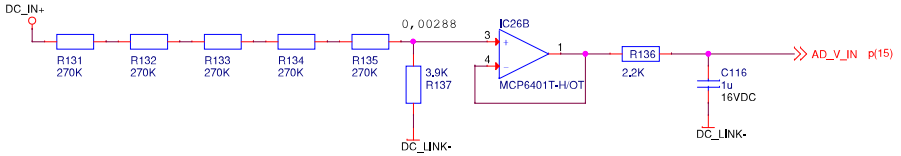
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **10 - LLC power**		PCB-num. / Rev	Sheet 10 of 17


Boost_PWM_XMC p(15)
R175 820R
Boost_PWM_LM p(5)
R105 820R
R108 820R
DC_LINK-
IC20
ANODE#1 VDD
ANODE#2 VOUT
CATHODE VE
NC#4 VSS
ACNU-3430-500E
R106 4.7R
PWM_POWER_L_BOOST
25VDC C100 1u
G_Boost p(6)
25VDC C101 1u
DC_LINK-
-4V_DC_LINK-
PWM_POWER_H_BOOST
D16 STTH112U
Q19A DMG6601LVT
R107 10K
25VDC C102 10u
Z9 MM5Z18VT1
PWM_LLC_H_1 p(15)
R173 820R
LLC_PWM_UCC_A p(9,11)
R109 820R
R111 820R
IC21
R110 4.7R
25VDC C103 1u
G_LLC_High_A p(10)
E_LLC_High_A p(10)
25VDC C104 1u
PWM_LLC_L_1 p(15)
R171 820R
LLC_PWM_UCC_A p(9,11)
R112 820R
R114 820R
IC22
R113 4.7R
PWM_POWER_L_BOOST
25VDC C105 1u
G_LLC_Low_A p(10)
25VDC C107 1u
DC_LINK-
-4V_DC_LINK-
D17 RB520S30
25VDC C106 10u
Z10 MM5Z18VT1
R115 10K
-8V_DC_LINK+_RES
STTH112U D18
Q19B DMG6601LVT
PWM_POWER_H_BOOST
D19 STTH112U
R116 10K
25VDC C108 10u
Z11 MM5Z18VT1
PWM_LLC_H_2 p(15)
R174 820R
LLC_PWM_UCC_B p(9,11)
R120 820R
R122 820R
IC24
R121 4.7R
25VDC C111 1u
G_LLC_High_B p(10)
E_LLC_High_B p(1,10)
25VDC C112 1u
PWM_LLC_L_2 p(15)
R173 820R
LLC_PWM_UCC_B p(9,11)
R117 820R
R119 820R
IC23
R118 4.7R
PWM_POWER_L_BOOST
25VDC C109 1u
G_LLC_Low_B p(10)
25VDC C110 1u
DC_LINK-
-4V_DC_LINK-
D20 RB520S30
25VDC C113 10u
Z12 MM5Z18VT1
R123 10K
-8V_DC_LINK+_RES
STTH112U D21
Q18B DMG6601LVT
Aros electronics AB
Sign:
Date:
Aros art.no:
Checked:
Rev. date:
Customer art.no:
Drawing:
Rev
Document title:
Charger
11 - Gate drivers
PCB-num.
Rev
Sheet 11 of 17
No part of this document may be reproduced in any form or by any means, without the prior written consent of:
Aros Electronics AB, Sweden 2017

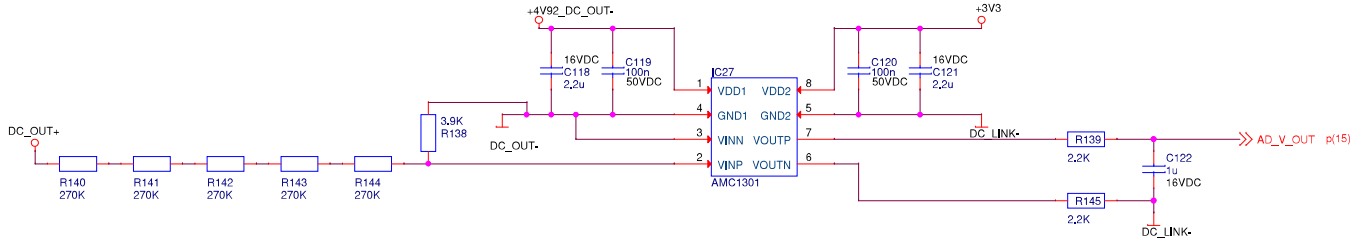
Capacitor bank voltage measurement



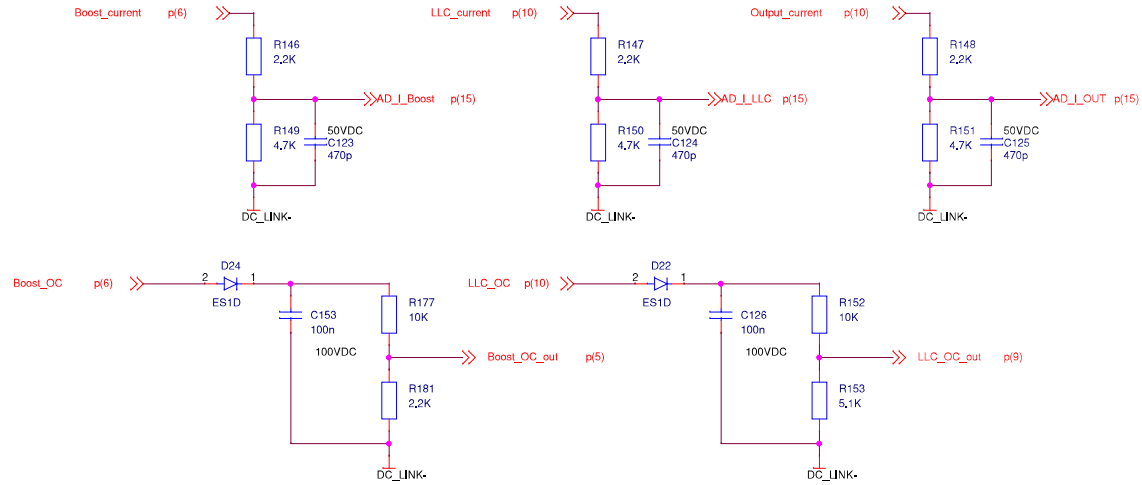
Input DC voltage measurement



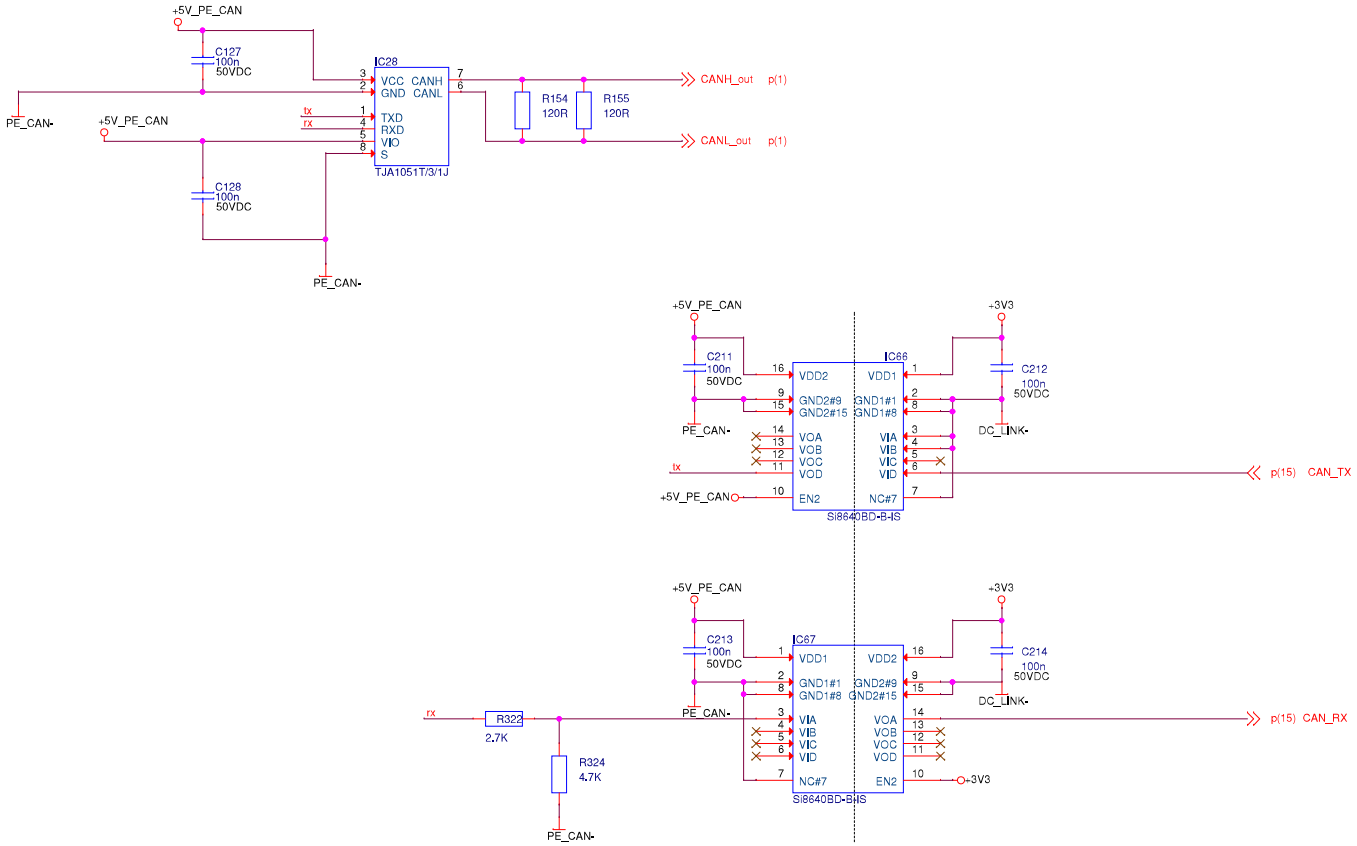
Isolated output DC voltage measurement



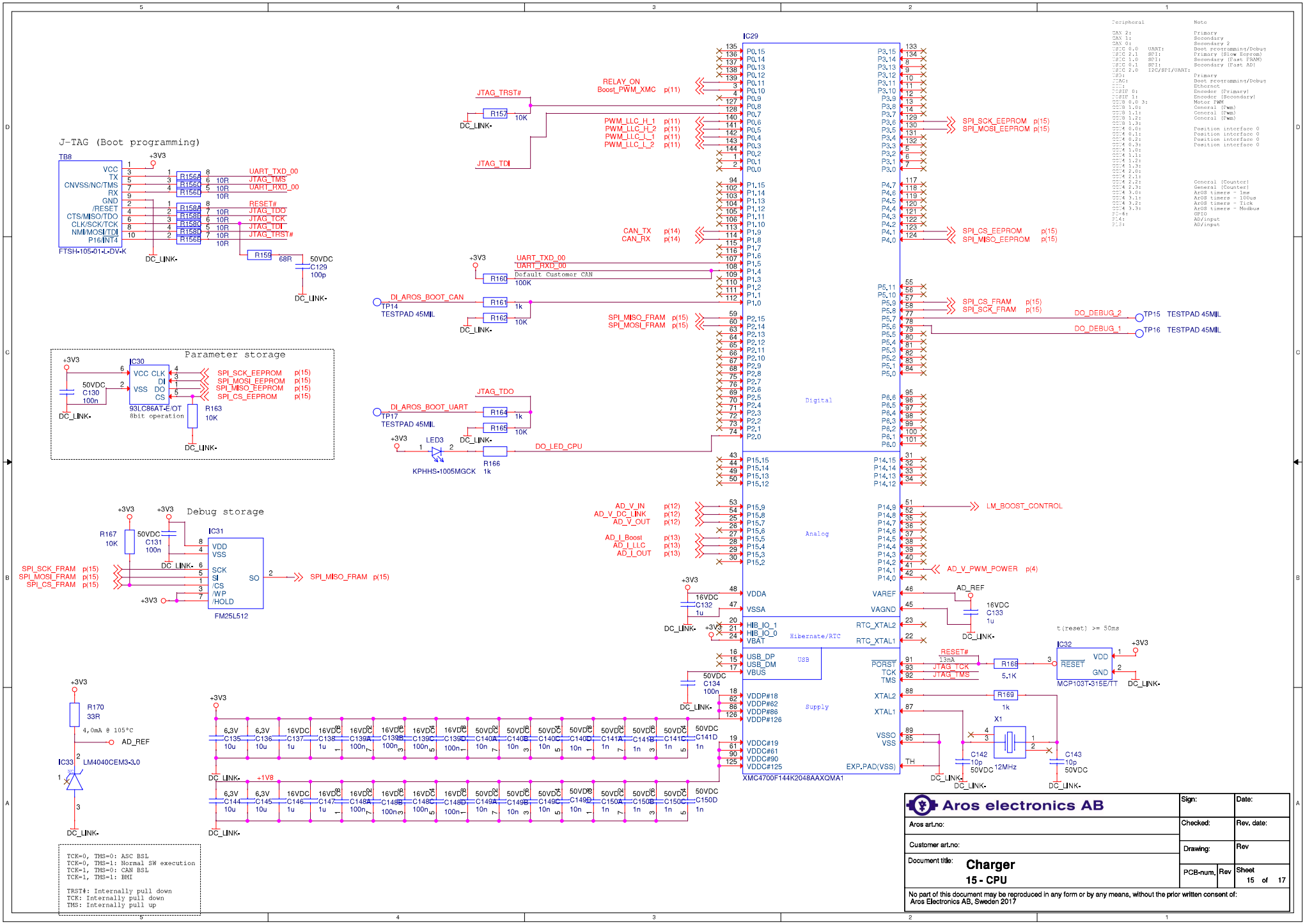
Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **12 - Voltage measurement**	PCB-num.	Rev	Sheet 12 of 17



Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **13 - Current measurement**	PCB-num.	Rev	Sheet 13 of 17



Aros electronics AB		Sign:	Date:
Aros art.no:		Checked:	Rev. date:
Customer art.no:		Drawing:	Rev
Document title: **Charger** **14 - CAN**	PCB-num. / Rev		Sheet 14 of 17


J-TAG (Boot programming)
TB8
FTSH-105-01-L-DV-K
Parameter storage
IC30
93LC86AT-E/OT
8bit operation
Debug storage
IC31
FM25L512
IC29
XMC4700F144K2048AAXQMA1
Digital
Analog
Hibernate/RTC
USB
Supply
IC32
MCP103T-315E/TT
IC33
LM4040CEM3-3.0
X1
12MHz
TCK=0, TMS=0: ASC BSL
TCK=0, TMS=1: Normal SW execution
TCK=1, TMS=0: CAN BSL
TCK=1, TMS=1: BMI
TRST#: Internally pull down
TCK: Internally pull down
TMS: Internally pull up
Aros electronics AB
Aros art.no:
Customer art.no:
Document title:
Charger
15 - CPU
Sign:
Date:
Checked:
Rev. date:
Drawing:
Rev
PCB-num.
Rev
Sheet
15 of 17
No part of this document may be reproduced in any form or by any means, without the prior written consent of:
Aros Electronics AB, Sweden 2017