CHALMERS
UNIVERSITY OF TECHNOLOGY

Modelling, Simulation and Investigation of Losses and Ripple in Traction Inverters.

Master's Thesis in Electric Power Engineering

KELECHI JUDE EGBE, BHARATH REDDY MURALI

DEPARTMENT OF ENERGY AND ENVIRONMENT
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2021
www.chalmers.se

Master's thesis 2021

Modelling, Simulation and Investigation of Losses and Ripple in Traction Inverters

Kelechi Jude Egbe, Bharath Reddy Murali

Department of Energy and Environment
Electrical Engineering Division
Chalmers University of Technology
Gothenburg, Sweden 2021

Modelling, Simulation and Investigation of Losses and Ripple in Traction Inverters.
Kelechi Jude Egbe, Bharath Reddy Murali

Supervisors: Kooros Moabber and Lars Johansson
Examiner: Torbjörn Thiringer

Master’s Thesis 2021
Department of Energy and Environment
Division of Electrical Engineering
Electric Power Engineering MPEPO
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover: A traction power train inverter
Typeset in LaTeX
Printed by Chalmers Reproservice
Gothenburg, Sweden 2021

Abstract

The decreasing cost for High-Voltage (HV) batteries and a growing requirement to reduce CO2 emissions has led to considerable interest in the electrification of vehicles within the automotive sphere. Additionally, the evolution of semiconductor switches has seen an increase in HV battery electric vehicle research. The traction inverter is an essential component of the electric power train and can account for some significant percentage of the electric drive train losses. This work therefore models, simulates and studies the losses and DC link ripple in an 800 V, 350 kW traction inverter. Utilizing the PLECS software, an inverter model is built considering thermal properties of the power module. Preliminary results of the DC link ripple and the inverter electrical losses are compared with analytical models and finally, comparisons of inverter losses between two different SiC power modules and an IGBT power module are presented.

The DC link ripple investigation shows good agreement of the simulation with the analytical model, however, it has a 17.5% and 5.8% discrepancy for voltage and current ripple respectively, close to maximum torque operating current.

Electrical losses of the simulation at selected operating points and assuming constant on-state resistance of the power module are seen to have even better agreement with the analytical model with a maximum variance of 0.3% observed for the conduction losses and 7% realized for the switching losses. Including the temperature dependency of the on-state resistance increases the discrepancy of the conduction loss with the analytical model to about 17% at high operating currents.

Analysis carried out on another power module manufacturer - Semikron - shows an 8% increase in power dissipation when switching energies for PLECS thermal lookup tables are derived manually from its SPICE model than when switching energies were only derived from its datasheet.

Assuming a fixed coolant flow rate of $10l/min$ and a coolant fluid temperature of 80°C three different power modules are compared. Using the recommended gate resistances from the manufacturers, it is observed that Type 1 power module - CREE from Wolfspeed manufacturer - has a maximum power dissipation of 3.1 kW. while Type 2 power module - Semikron manufacturer - has maximum power loss of 4.9 kW. Finally, Type 3 power module - DYNEX - shows a maximal power dissipation of 10 kW. These analysis illustrate that the CREE power module should be preferred for this particular application due to its reduced power dissipation.

Keywords: SiC MOSFET Modelling, PLECS, Reverse Conduction, Thermal Modelling, Loss Investigation, DC link ripple, Traction Inverter, Electrical losses, Electric Vehicle.

Acknowledgements

We would like to express our gratitude to our supervisors Kooros Moabber and Lars Johansson, for their relentless enthusiasm, patience and motivation throughout this journey. Additionally, we would like to thank our examiner Prof. Torbjörn Thiringer for his unwavering support and guidance that kept us on track throughout this thesis work. Finally, Xiaoliang Huang, whose insights opened our eyes to more fascinating aspects of this work.

I, Bharath would like to thank my parents and family for their encouragement and support throughout my master's program.

I, Kelechi would like to appreciate the following people who supported me during this study: My parents and siblings for their comforting words during the "dark times" of this research; and my Swedish network built during the course of this program who assisted emotionally and otherwise to release pent up stress during this program. You all helped directly or indirectly, and for this, I am profoundly grateful.

Kelechi Jude Egbe & Bharath Reddy Murali, Gothenburg, August 2021

Contents

Acronyms

CFD Computational Fluid Dynamics. 27

DPT Double Pulse Testing. ix, 16
DPWM Discontinuous Pulse Width Modulation. 7
DUT Device Under Test. 17

EM Electric Machine. 1, 6
ESR Equivalent Series Resistance. 14
EV Electric Vehicle. v, 59

HV High-Voltage. v

IEEE Institute of Electrical and Electronics Engineers. 59
IGBT Insulated Gate Bipolar Transistor. 3
IGBT Insulated Gate Bi-polar Transistor. ix, 4

MOSFET Metal Oxide Field Effect Transistor. ix, 3
MTPA Maximum Torque Per Ampere. 46, 48, 49

SiC Silicon Carbide. 1, 4
SPWM Sinusoidal Pulse Width Modulation. ix, 7
SVPWM Space Vector Pulse Width Modulation. 7, 8, 11

UN United Nations. 1

VSI Voltage Source Inverter. 1, 6
VSIs Voltage Source Inverters. 1

1

Introduction

According to the United Nations (UN) 2018 policy brief on energy and transport [1], road transport vehicles are responsible for the largest share of transport energy use. In recent years, there have been increasing interests in enhancing the efficiency of road vehicles, which helps manage energy demand, save money, and decrease climate and air quality impacts in alignment with the Sustainable Development Goals. Electrification of vehicles, in particular, has become crucial with the increase in the demand for sustainable transportation, hence growing the need to advance electric vehicle studies and design.

1.1 Background

Most drive trains of electric vehicles utilize three-phase Voltage Source Inverters together with an appropriate control system to drive the Electric Machine (EM) connected to the wheels. The VSI is a crucial component of the electric drive train which converts direct current (DC) from the vehicle battery to alternating current (AC) which is demanded by the control system for the EM. However, energy losses from the semiconductor switches are usually significant and decrease inverter and drive train performance. Therefore accurate determination of losses is a necessity for a detailed study of the inverter working process.

Another important component that influences these losses is the DC-link capacitor. The DC-link capacitor's role in the inverter system provides a low impedance path for ripple currents that arise from hard switching [2]. Previous studies have shown that an increase in switching frequency reduces the DC-link voltage and current ripple [3][4]. With the use of wide-bandgap semiconductors such as Silicon Carbide (SiC), higher switching frequencies can be achieved. The need to study the influence of switching frequency and the size of the DC-link capacitor on the current ripple is key in drive train design. Hence, this work will study the losses associated with the inverter power module and DC-link capacitor.

1.2 Purpose of the Thesis

The main purpose of the thesis is to quantify the losses and DC-link ripple in an 800 V, 350 kW traction inverter with a primary focus on the dc-link capacitor and transistors for various selections of switching frequencies and gate resistances at selected operating points. In addition, this study will compare the ripple and losses from the simulated model with analytical models for verification. Eventually, it will also investigate the thermal impact of the losses on the main power components at selected operating points.

1.3 Scope and Delimitations

Since this study focuses mainly on the inverter, loss investigation will be carried out on three different power module types at predetermined operating points. The influence of selected operating points, switching frequency and dc-link capacitors on the dc-link ripple will also be evaluated. Due to time and resource constraints, the closed control loop system of the drive train will not be considered. Furthermore, all analyses will only be carried out using space vector pwm technique, other modulation techniques will not be assessed. Finally, the impact of snubber circuits, detailed battery modelling and study, filter design, gate driver design and the influence of driving cycles and blanking time on these losses will not be taken into account.

2

Theoretical Background

This section highlights the relevant theoretical background and literature that are important to understand in carrying out this thesis work. Semiconductor switches are first discussed, followed by the three-phase inverter, then control techniques of the inverter, after that, the DC-link capacitor is highlighted, and finally, the power losses in the inverter including electro-thermal interactions and double pulse testing.

2.1 Switching devices description

Initially, Si-based semiconductor devices were used for most power conversion applications. While IGBTs were used for high power applications, MOSFETs were used for low and medium power applications. Soon after, the Wide bandgap devices emerged. These devices offer better overall performance, high efficiency and can operate at high switching frequencies, thereby reducing the size of the peripheral components like filters, capacitors and inductors [5]. Since we deal with high power in this thesis, SiC MOSFETs are used because of their aforementioned advantages.

2.1.1 The Metal Oxide Field Effect Transistor (MOSFET)

The MOSFET is a three-terminal voltage-controlled device with gate, drain and source. This type of semiconductor device is used for fast switching low and medium voltage applications. It requires continuous gate-source voltage to remain in the on-state. A conduction channel gets created between the drain and the source when the voltage given to the gate is above the threshold value [6].

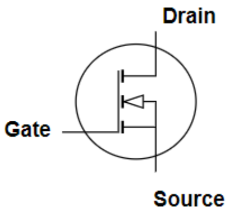


Figure 2.1: MOSFET symbol

The output characteristics of the MOSFET shown in Figure 2.2 depicts the change in drain current (I_{ds}) with respect to the gate voltage as a function of the drain-source voltage (V_{DS}). It consists of three operating regions, the cutoff region, the ohmic region and the saturation region.

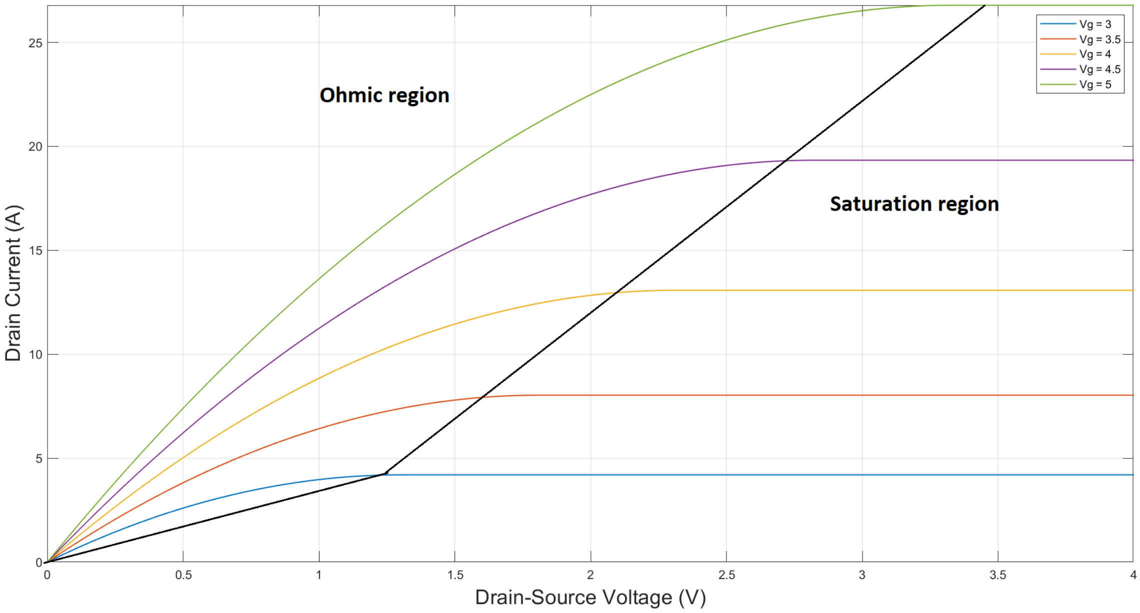


Figure 2.2: MOSFET Output characteristics

In the cutoff region, the MOSFET behaves like an open switch with no current flowing through it, whereas, in the ohmic region, an increase in V_{DS} increases the drain current; thereby, the MOSFET can be used as an amplifier in this region. Finally, in the saturation region, the drain current remains constant despite the increase in V_{DS} and when it increases beyond the pinch-off voltage, the device acts as a closed switch with a saturated current flowing through it [7].

2.1.2 Silicon Carbide (SiC) MOSFET

SiC MOSFETs exhibit better overall performance because of their inherent material advantages over Si devices. The larger energy gap provided by these devices makes them suitable for high-temperature applications. In addition to these, SiC MOSFETs have high electric field breakdown strengths and thermal conductivity compared to Si devices [6]. These devices have lower on-state resistance, thereby reducing the conduction losses to a greater extent. They can also block high voltages, making them a superior choice in high power applications [5].

2.1.3 Insulated Gate Bi-polar Transistor (IGBT)

The IGBT is a three-terminal unidirectional voltage controlled device with gate, emitter and collector as shown in Figure 2.3. The development of this device is through the fusion of BJT and MOSFET monolithically on the same silicon wafer. These devices are primarily used for high power applications. IGBTs have the input characteristics of a MOSFET and the output characteristics of a BJT.

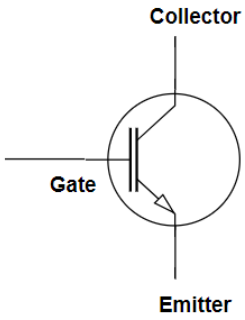


Figure 2.3: IGBT symbol

The output characteristics of the IGBT shown in Figure 2.4 depicts the change in collector current (I_c) with respect to the gate voltage as a function of the collector-emitter voltage (V_{ce}). It consists of three operating regions, the linear region, the active region and the turn-off region.

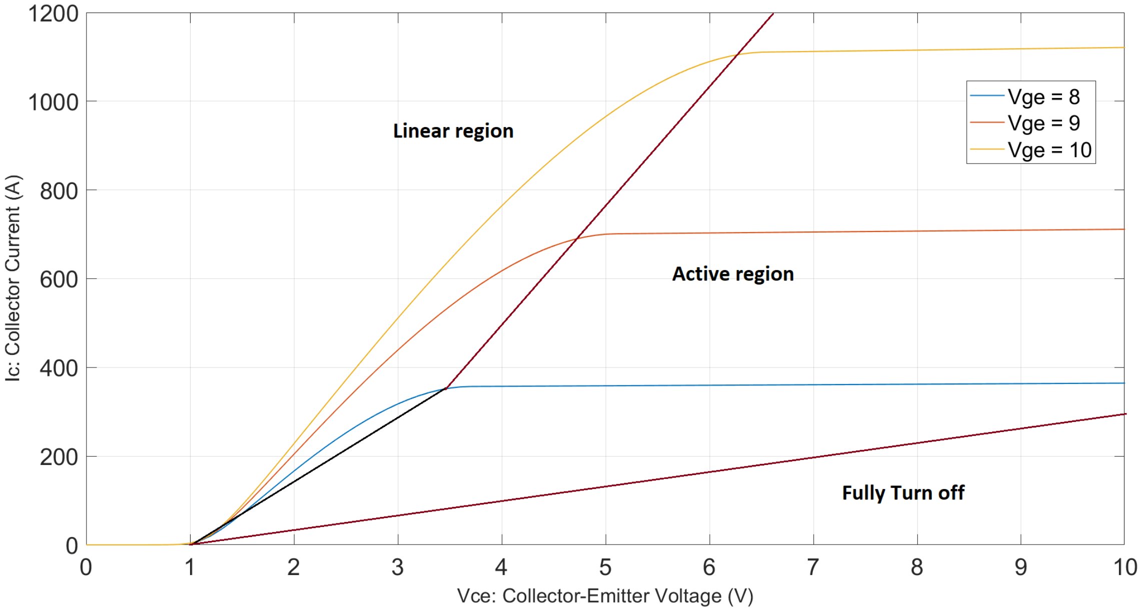


Figure 2.4: IGBT Output characteristics

In the turn off region, the IGBT behaves like an open switch with no current flowing through it, whereas, in the linear region, an increase in V_{ce} increases the collector current; thereby, the IGBT can be used as an amplifier in this region. Finally, in the active region, the drain current remains constant despite the increase in V_{ce} and when it increases beyond the pinch-off voltage, the device acts as a closed switch with saturated current flowing through it. It can also be seen that the current increases with increasing gate voltage from Figure 2.4.

2.2 The Three phase, Two level, Voltage Source Inverter

The three phase inverter converts direct current and voltage into alternating current and voltage for the electrical machine. It accomplishes this by modulating sinusoidal waveforms using high-frequency switching of power semiconductors. As a result, it produces the three phases of sinusoidal current that are 120° phase-shifted required to enable the EM to produce an output torque. This torque can further be controlled by changing the amplitude and frequency of its stator waveforms.

The frequency of the produced waveforms determine the speed of rotation of the EM, while the amplitude determines the motor power or torque. Thus, if more torque or speed is requested, the motor controller regulates the switching to give the required amplitude and frequency for the demanded torque or speed. Of concern in this thesis, is the two level VSI shown in the Figure 2.5.

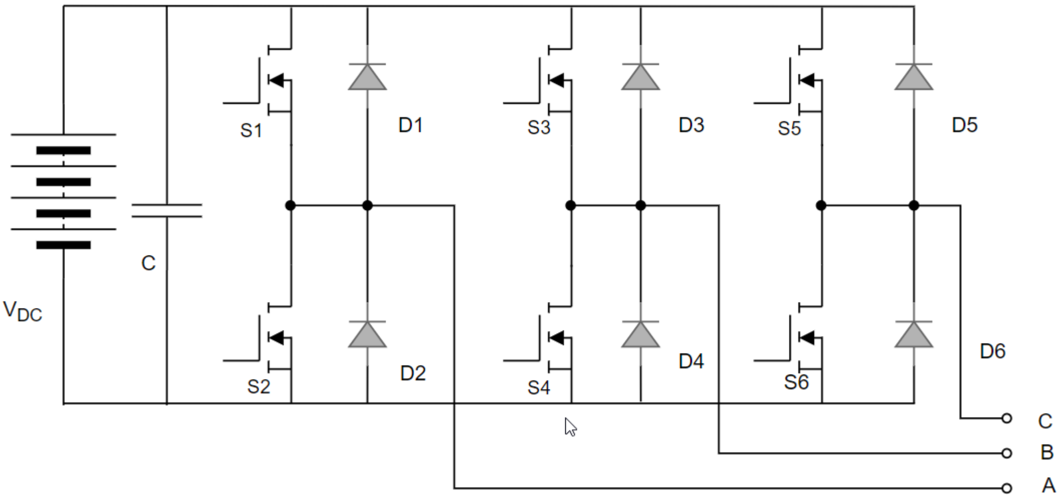


Figure 2.5: Simple three phase inverter

Because of its lightweight, compact, and relatively good performance, the three-phase 2-level VSI is the standard inverter structure used in small scale systems [8] especially in power train design where small size is crucial. It consists of six semiconductor switches S1 - S6 (either IGBTs or MOSFETs) whose switching times are intuitively selected to achieve the demanded fundamental voltage amplitude and frequency. Each switch consists of antiparallel diodes, D1 - D6 that provide free-wheeling paths for negative inductive currents when the switch is turned on [9]. Its output consists of three identical waveforms that are phase-shifted by 120° from each other.

The input to the inverter usually referred to as the dc-link, consists of a power source, V_{DC} (battery in this case), and the dc-link capacitor, C.

2.3 Different Pulse Width Modulation techniques

Pulse-width modulation techniques are used to regulate the switching of the semiconductor devices to provide the required AC amplitude and frequency to the connected electric machine. Some different types of modulation techniques are Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM),and Discontinuous Pulse Width Modulation (DPWM). The DPWM is outside the scope of this thesis and will not be discussed further.

2.3.1 Sinusoidal Pulse Width Modulation (SPWM)

In this type of modulation technique, three sinusoidal reference waves phase shifted by 120 degrees from each other are compared with the triangular carrier wave [10]. Consider the first leg of the inverter; When the amplitude of the sinusoidal reference of phase A is greater than the amplitude of the carrier wave, the top switch (S1) is turned on to carry the current. If the amplitude of the sinusoidal reference of phase A is lower, then the bottom switch (S2) is turned on to carry the current, this can be seen in Figure 2.6 The references are described as,

$$V_{ref,a}(\omega t) = m_a V_{dc} sin(\omega t) \tag{2.1}$$
$$V_{ref,b}(\omega t) = m_a V_{dc} sin(\omega t - (2\pi/3)) \tag{2.2}$$
$$V_{ref,c}(\omega t) = m_a V_{dc} sin(\omega t + (2\pi/3)) \tag{2.3}$$

where, m_a is the modulation index and Vdc is the DC-link voltage.
The modulation index for SPWM can be obtained as,

$$m_a = \frac{2\sqrt{2}V_{ref}}{V_{dc}} \tag{2.4}$$

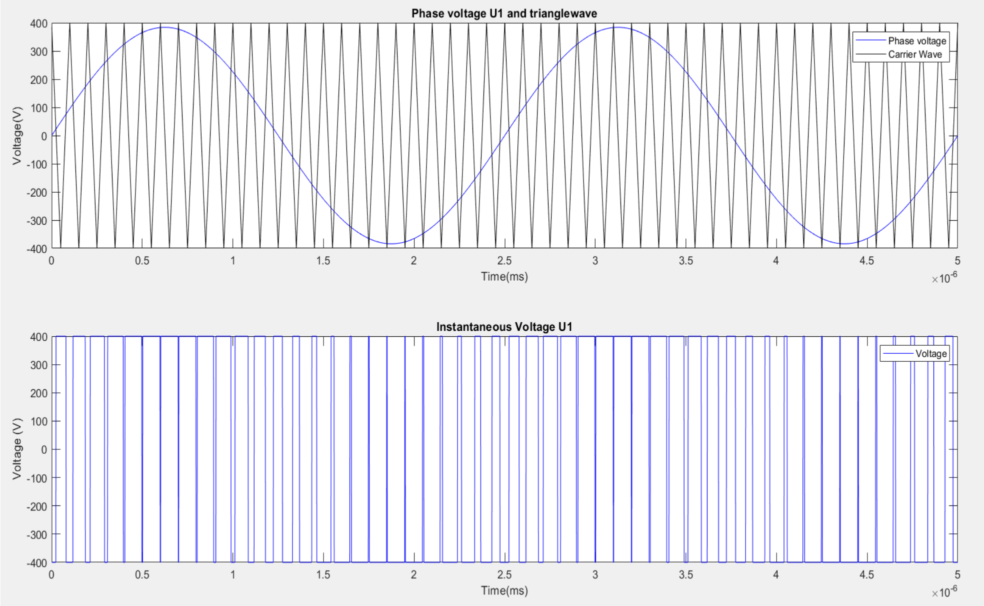


Figure 2.6: Sinusoidal PWM for Phase A

As described in [11], some major drawbacks of the SPWM technique are its low DC bus utilization and its inability to position zero space vectors, hence its evolution into the third harmonic injection PWM types which account for these setbacks.

2.3.2 Space Vector Pulse Width Modulation

The Space Vector Pulse Width Modulation (SVPWM) utilizes mathematical transformation to extract digital signals used for controlling inverter switches [12]. The demanded three phase voltages are transformed to the $\alpha\beta$-frame (Clark transformation) in order to calculate the average period of the required pulses. The location of this reference vector on the $\alpha\beta$-frame determines the ON or OFF states of the switches. The switching states of the three phase inverter depicted in Figure 3.1 can be described as being either 0 or 1 depending on whether the upper or lower switches are on. Therefore, each of the pole voltages can assume one of these two values and it is possible to have eight different switch combinations which comprise six active vectors and two zero vectors [13].

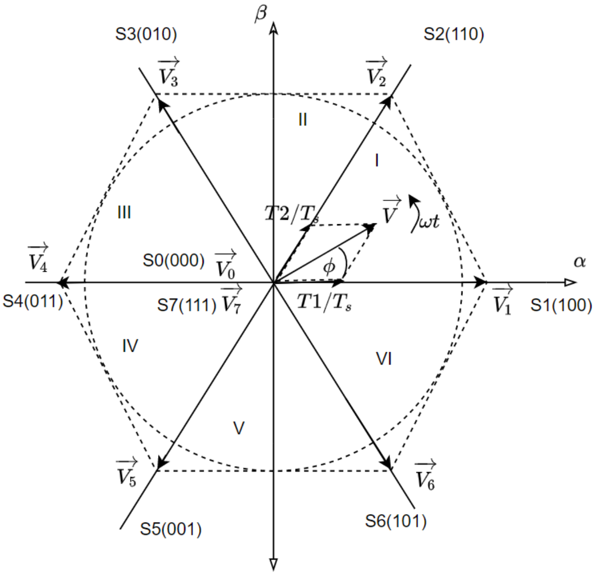


Figure 2.7: Space Vector PWM Sectors

Figure 2.7 shows a voltage reference vector within the different sectors of the space vector plane. The active switch states are represented by the voltage vectors $\overrightarrow{V_1} to \overrightarrow{V_6}$ while $\overrightarrow{V_0}$ and $\overrightarrow{V_7}$ represent the zero vectors. The lengths of the active vectors are unity while the lengths of the zero vectors are zero [14]. Decomposing a voltage vector reference, $\overrightarrow{V}$ (from Figure 2.7) into the space vector plane can be done in infinite ways, however, it is usually split just between the adjacent active voltage vectors and zero vectors $\overrightarrow{V_0}$ and $\overrightarrow{V_7}$ to make full use of the active turn-on time of the space vectors and to reduce the amount of switching during one cycle. A common implementation of the SVPWM technique centres the active space vectors in each half sample period and divides the remaining time equally between the two zero vectors.

This technique can be implemented using the following steps as illustrated in [15].

2.3.2.1 Determination of $\mathbf{V}_\alpha$ & $\mathbf{V}_\beta$

Assuming the three phase system is balanced, the voltages in alpha and beta frame are given as,

$$V_\alpha = \frac{2}{3}(V_a - \frac{1}{2}V_b - \frac{1}{2}V_c) \tag{2.5}$$

$$V_\beta = \frac{2}{3}(\frac{\sqrt{3}}{2}V_b - \frac{\sqrt{3}}{2}V_c) \tag{2.6}$$

$$V_{ref} = V_\alpha + jV_\beta \tag{2.7}$$

where V_α is the alpha component of the reference voltage in the alpha-beta frame, V_β is the alpha component of the reference voltage, V_a is the phase-a to neutral voltage, V_b is the b phase voltage, V_c is the c phase voltage and V_{ref} is the reference voltage.

2.3.2.2 Time duration of the vectors

For sector 1 in the SVPWM plane, V_{ref} can be identified using the vectors V_1, V_2 and V_0. When considered with the time duration, it can be decomposed as,

$$V_{ref} = \overrightarrow{V_1}\frac{T_1}{T_s} + \overrightarrow{V_2}\frac{T_2}{T_s} + \overrightarrow{V_0}\frac{T_0}{T_s} \tag{2.8}$$

where T_s is the sampling time of the space vector controller, T_1 is the turn-on time of $\overrightarrow{V_1}$, T_2 is the turn-on time of $\overrightarrow{V_2}$ and T_0 is the turn-on time of $\overrightarrow{V_0}$ and $\overrightarrow{V_7}$. The total sample time is the sum of the time duration of two active and zero vectors.
The voltage vectors in sector can also be described by their magnitudes and angles as,

$$V_{ref} = V_{ref}r^{j\theta}, V_0 = 0, V_1 = \frac{2}{3}V_{dc}, V_2 = \frac{2}{3}V_{dc}e^{j\frac{\pi}{3}} \tag{2.9}$$

Substituting (2.9) in (2.8) and dividing it into real and imaginary parts gives - real part.:

$$T_sV_{ref}cos(\theta) = T_1\frac{2}{3}V_{dc} + T_2\frac{1}{3}V_{dc} \tag{2.10}$$

Imaginary part:

$$T_sV_{ref}sin(\theta) = T_2\frac{1}{\sqrt{3}}V_{dc} \tag{2.11}$$

Solving (2.10) & (2.11)

$$T_1 = T_s\frac{\sqrt{3}V_{ref}}{V_{dc}}sin(\frac{\pi}{3} - \theta) \tag{2.12}$$

$$T_2 = T_s\frac{\sqrt{3}V_{ref}}{V_{dc}}sin(\theta) \tag{2.13}$$

where $\frac{\sqrt{3}V_{ref}}{V_{dc}} = m_\mathrm{a}$ is the modulation index.

Similarly, the time duration of the voltage vectors of other sectors can be determined as [15], shown

$$T_1 = T_s\ m_a\ sin(\frac{\pi}{3} - \theta + \frac{(n-1)\pi}{3}) \tag{2.14}$$

$$T_2 = T_s\ m_a\ sin(\theta - \frac{(n-1)\pi}{3}) \tag{2.15}$$

$$T_0 = T_s - T_1 - T_2 \tag{2.16}$$

where n is the number of the sector ranging from 1 to 6.
The advantage of the SVPWM scheme over the SPWM method is that it provides 15% more improved bus utilization than SPWM [13], low current ripple and easy implementation of hardware [15].

2.4 DC-link capacitor

Dc-link capacitors in power electronics are generally utilized as storage elements. They usually act to provide a relatively constant voltage across the dc-link. However, they are also designed to absorb the high frequency ripple currents caused by pulse width modulation. Therefore the voltage stress on the dc-link capacitor and the current ripple through the capacitor are important design considerations [16]. In addition, optimization of the DC link capacitor size is equally important in traction applications since it takes around one-third of the inverter's size. In power inverters for electric vehicles, the dc-link capacitor ripple current comprises several frequency components that vary according to the PWM strategies used.

2.4.1 DC-link Ripple Voltage Equations

According to [17], the DC-link voltage ripple in three-phase pwm inverters can be represented by

$$\Delta v_{pp} = max\{\Delta v_{pp}^{A1}, \Delta v_{pp}^{B1}\} \tag{2.17}$$

where Δv_{pp} is the peak to peak amplitude of the high frequency component of the dc-link voltage. It is further delineated for the first sector of the SVPWM by [18] as

$$\Delta v_{pp}^{A1} = \frac{3}{4}\frac{I_0 T_{sw}}{C} m_a cos\phi(1 - \sqrt{3} m_a sin(\pi/3 + \theta) \tag{2.18}$$

and

$$\begin{aligned}\Delta v_{pp}^{B1} = \frac{3}{4}\frac{I_0 T_{sw}}{C} m_a \cdot |cos\phi(1 - \sqrt{3} m_a sin(\pi/3 + \theta)\\ + \frac{4}{\sqrt{3}} sin(\pi/3 - \theta)(\frac{3}{2} m_a cos\phi - cos(\theta - \phi))|\end{aligned} \tag{2.19}$$

where I_0 is the peak output current of the inverter, m_{a} is the modulation index, T_{sw} is the switching period, C is the DC-link capacitance, ϕ is the power factor angle and θ is voltage angle. The voltage ripple peak evaluated based on comparing the current contribution of one transistor leg (say i_1) to the output current peak with the average dc current input (I_{dc}). v_{pp}^{A1} is derived for when $i_1 \geq I_{dc}$ while v_{pp}^{B1} is derived for when $i_1 < I_{dc}$.

Since some operating points to be tested were in sector II of the SVPWM circle, equivalent formulas for Δv_{pp} are derived using [18] and [14] as

$$\Delta v_{pp}^{A2} = \frac{3}{4}\frac{I_0 T_{sw}}{C} m_a cos\phi(1 - \sqrt{3} m_a sin\theta) \tag{2.20}$$

and

$$\begin{aligned}\Delta v_{pp}^{B2} = \frac{3}{4}\frac{I_0 T_{sw}}{C} m_a \cdot |cos\phi(1 - \sqrt{3} m_a sin\theta) + 2\sqrt{3} m_a cos\phi sin(\theta - \pi/3) \\ - \frac{4}{\sqrt{3}} cos(\theta - 2\pi/3 - \phi) sin(\theta - \pi/3))|\end{aligned} \tag{2.21}$$

2.4.2 DC-link Ripple Current Equations

The rms ripple current in the DC-link capacitor of an inverter utilizing SVPWM is described according to [19] as

$$I_{C,rms} = I_{0,rms}\sqrt{2m\left[\frac{\sqrt{3}}{4\pi} + cos^2\phi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}m\right)\right]} \tag{2.22}$$

where $I_{C,rms}$ is the rms capacitor current ripple and $I_{0,rms}$ is the rms output current. Equation (2.22) shows us that the rms current ripple is dependent on the power factor angle, modulation index, and output current values. It has also been shown by [20] that the rms current ripple is not influenced by the PWM switching method in contrast to the voltage ripple.

2.5 Loss Calculations in a Three Phase Inverter

The losses in the three phase inverter can be split into power semiconductor losses and ohmic losses. The power semiconductor losses can be further split into the switching and conduction losses, highlighted in [21] as

$$P_{tot} = P_{sw} + P_{cond} \tag{2.23}$$

where P_{tot} are the average total power losses in the semiconductor device, P_{sw} are the average switching losses and P_{cond} are the average conduction losses. The ohmic losses on the other hand, are the losses from other components that have an equivalent resistance while conducting. It is the product of the square of the rms current value and the equivalent resistance of the component

$$P_{lossohmic} = I_{rms}^2 R \tag{2.24}$$

where I_{rms} is the rms value of the current flowing through the device and R is the equivalent resistance of the device.
It is important to note that in reality, there are more sources of losses in the inverter such as the losses from the snubber circuits, gate driver circuits, controller circuits, cable and busbar impedances, however, these are not discussed here as they are beyond this scope of work.

2.5.1 Switching Losses

These losses occur in the semiconductor switches and diodes because of the non-instantaneous change of the current and voltage during turn on and turn off. The switching energies during turn on and turn off are shown in Figure 2.8, where I_{DS} is the current through the switching device, I_{rr} is the reverse recovery current of the body diode, t_{rr} is the reverse recovery time, t_{ri} is the rise time of the current, t_{rv} is the rise time of the voltage, t_{fi} is the fall time of the current, and t_{fv} is the fall time of the voltage.

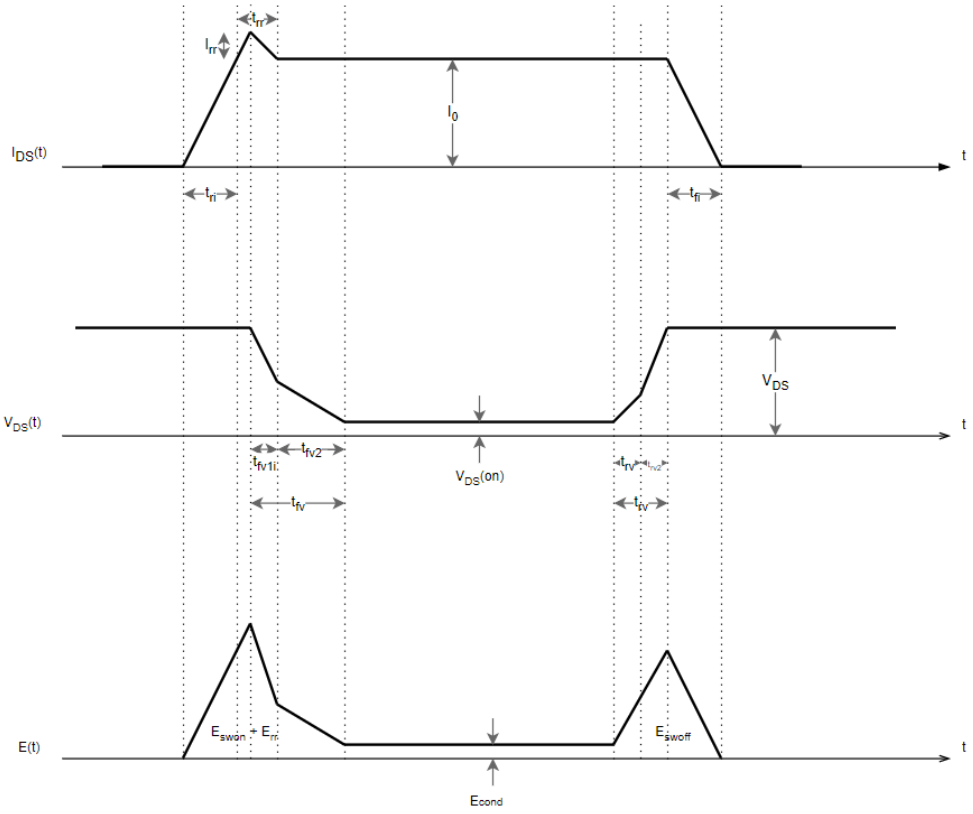


Figure 2.8: Power semiconductor switching waveforms

The switching losses are a function of the switching energy of the device and the switching frequency. The switching energy of the device is in turn dependent on the device junction temperature, the voltage across the device at switching and the final current through the device.

$$P_{sw} = f_{sw} E_{sw} \Big(I, V_{DS}, T_j \Big) \tag{2.25}$$

Equation (2.26) highlights this dependency; where f_{sw} is the switching frequency, E_{sw} is the switching energy (the sum of the turn on, turn off and reverse recovery energies), I is the current through the device. The switching losses in a three-phase inverter can be approximated according to [22] as

$$P_{sw} = f_{sw} E_{sw} \left(\frac{1}{\pi} \frac{\hat{I}_0}{I_{ref}} \right)^{K_i} \cdot \left(\frac{V_{DS}}{V_{ref}} \right)^{K_V} \tag{2.26}$$

where $\hat{I}_0$ is the peak value of the inverter output phase current, I_{ref} and V_{ref} are the test conditions from the semiconductor datasheet where the corresponding E_{sw} values are obtained, V_{DS} is the drain-source voltage across the device (dc-link voltage), K_i and K_v are the constants that describe the current and voltage dependency with the switching energies.

2.5.2 Conduction losses

These losses occur in the semiconductor switches and diode because of the conduction of current through it. The on state losses of the MOSFET can be written as,

$$P_{MOSFET} = \frac{1}{T} \int_0^T v(i(t)) i(t) dt \tag{2.27}$$

$$P_{MOSFET} = \frac{1}{T} \int_0^T R_{on} i^2(t) dt \tag{2.28}$$

$$P_{MOSFET}(t) = v(i(t)) i(t) = R_{on} i^2_{rms}(t) \tag{2.29}$$

where $P_{MOSFET}(t)$ is the instantaneous on-state loss and P_{MOSFET} is the average on state loss in the MOSFET for one fundamental period.

The on state losses of the diode can be written as,

$$P_{diode} = \frac{1}{T} \int_0^T v(i(t)) i(t) dt \tag{2.30}$$

$$P_{diode} = \frac{1}{T} \int_0^T (R_d i(t) + V_d) i(t) dt \tag{2.31}$$

$$P_{diode} = \frac{1}{T} \int_0^T (R_d i^2(t) + V_d i(t)) dt \tag{2.32}$$

$$P_{diode}(t) = v(i(t)) i(t) = R_d i^2_{rms}(t) + V_d i_{avg}(t) \tag{2.33}$$

where $P_{diode}(t)$ is the instantaneous on state loss and P_{diode} is the average on state loss in the diode for one fundamental period. V_d is the forward voltage of the diode.

Similarly, the on state losses of the IGBT can be written as,

$$P_{IGBT} = \frac{1}{T}\int_0^T v(i(t))i(t)dt \tag{2.34}$$

$$P_{IGBT} = \frac{1}{T}\int_0^T (R_f i(t) + V_T)i(t)dt \tag{2.35}$$

$$P_{diode} = \frac{1}{T}\int_0^T (R_f i^2(t) + V_T i(t))dt \tag{2.36}$$

$$P_{IGBT}(t) = v(i(t))i(t) = R_f i_{rms}^2(t) + V_T i_{avg}(t) \tag{2.37}$$

where $P_{IGBT}(t)$ is the instantaneous on state loss and P_{IGBT} is the average on state loss in the IGBT for one fundamental period. V_T is the forward voltage of the IGBT.

2.5.3 Ohmic losses

The losses that occur due to the current flowing through the resistances present in the DC-link capacitor module, busbar and cable models are described as ohmic losses. In this thesis, the losses present in the busbar and cable models are not considered. The Equivalent Series Resistance (ESR) of the DC-Link capacitor is made up of several mechanisms, including resistance in elements and connections, viscous forces within the dielectric and defects producing current bypass paths [23].

2.6 Reverse Conduction in SiC MOSFETs

The internal pn junction present in the IGBT semiconductors does not allow the current to flow in the negative direction without an antiparallel diode. Whereas, the MOSFETs allows negative current to flow from source to drain. If the negative current flowing through the MOSFET is high enough to forward bias the body diode, the current splits between the MOSFET and the diode. This can be calculated as shown in (2.38) and (2.39). This condition of current splitting between the MOSFET and diode reduces the on-state losses in the negative half of the fundamental period [24].

$$i_{MOSFET}(t) = \frac{R_d i(t) - V_d}{R_{on} + R_d} \tag{2.38}$$

$$i_{diode}(t) = \frac{R_d i(t) + V_d}{R_{on} + R_d} \tag{2.39}$$

where V_d is the forward voltage of the diode, R_d is the resistance of the diode, R_{on} is the On state resistance of the MOSFET and $i(t)$ is the instantaneous value of the phase current.

2.7 Electro-Thermal Interactions

Power losses due to various types of loss mechanisms in high power density power electronics systems make electro-thermal interactions unavoidable. Joule heating which is a major source of these losses causes a temperature rise in these components, which, in turn, alter the electrical characteristics of these components. These electro-thermal interactions can be captured by modelling components within the electrical network with regard to the components' temperature dependency and thereafter coupled to (a) thermal model(s).

Heat propagation in electronic components is usually done by conduction, and it is shown in [25] that a simplified one-dimensional heat conduction equation is analogous to the electric transmission line equation. Therefore the thermal conduction description can be represented by a transmission line equivalent diagram that consists only of R/C elements. The equivalences between thermal and electrical variables are shown in Table 2.1

Table 2.1: Electro-Thermal Analogous Equivalences

Thermal		Electrical	
Temperature	T in K	Voltage	U in V
Heat flow	P in W	Current	I in A
Thermal resistance	Rth in K/W	Resistance	R in V/A
Thermal capacitance	Cth in Ws/K	Capacitance	C in As/V

where K is Kelvin, V is Volts, A is Amperes, W is Watt, and s is seconds. Figure 2.9 shows the thermal circuit that is analogous to the electrical transmission line

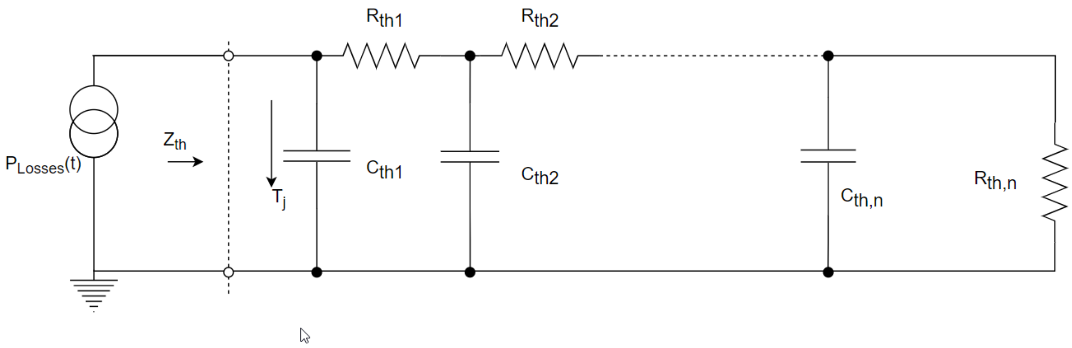


Figure 2.9: Thermal Circuit Analogous to the Electrical Transmission Line

where P_{Losses} represents the losses in the semiconductor, Z_{th} represents the equivalent thermal impedance of the network, R_{th} is the thermal resistance, C_{th} the thermal capacitance and n is the position of the conduction segment in the semiconductor. Each RC network represents different layers of material in the semiconductor/power module. This model, also called the Cauer Network, is the only network model that accurately describes the temperature distribution between equivalent elements and physical elements [25]. [26].

A further simplified model called the Foster network, or fraction equivalent circuit (shown in Figure 2.10), is also popular and represents each layer of the MOSFET as RC pairs in parallel. The transfer function of this simplified circuit makes it easy to describe the step response thermal impedance from junction to case. However, it cannot describe the internal nodal voltages (temperatures) at different layers. It therefore, can only be considered as a ’blackbox’[26] in which one feeds in losses as input and obtains junction temperature rise as output. Additionally, if a thermal description extension is needed, such as the addition of heat sink impedance, the fraction equivalent circuit is inadequate for a simulation model.

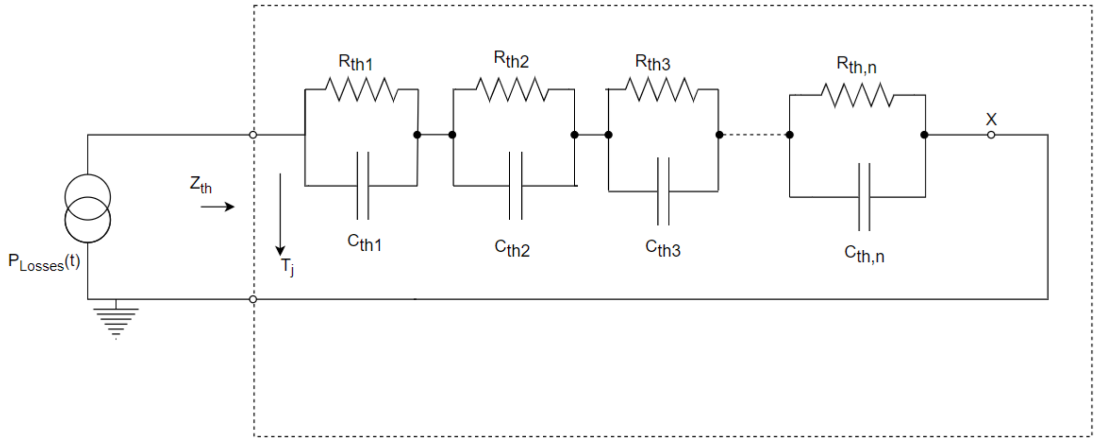


Figure 2.10: Foster thermal Network

Circuit simulators such as PLECS use these RC-type networks to estimate the junction temperatures of semiconductor components. An equivalent thermal RC network can be produced from supplier-provided datasheet parameters, experimental or finite element analysis extracted parameters [27] [26]. It should be highlighted that these compact thermal models ignore specific details of physical behaviour but provide fast computation [27].

2.8 Double Pulse Testing (DPT)

While selecting switches suitable for specific switching frequency and dynamic performance, it is pertinent to understand the switching behaviour concerning its specific application. Hence, DPT is developed to characterize this [28]. It is a circuit setup that enables power switches to be turned on and off at different current levels [29]. Figure 2.11 shows a simple DPT setup. It consists of a half-bridge converter topology with an inductive load.

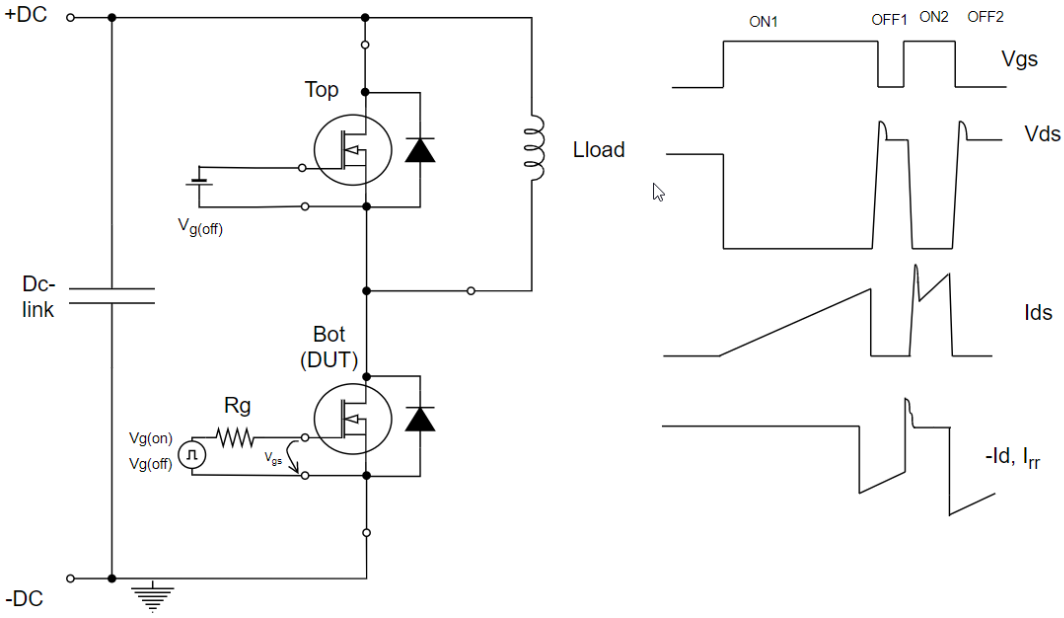


Figure 2.11: Simple DPT Setup and Corresponding Waveforms

The circuit is constructed such that the Device Under Test (DUT) (the bottom MOSFET) is turned on and off twice. Although, during the first pulse ON1, the current increases to a specific level (I_ds), the load inductance must be high enough to keep the current constant during OFF1 when the current is freewheeling through its intrinsic diode. Thus, the dynamic parameters can be measured only during the first turn off and the second turn-on [28].

In this thesis work the IEC 60747-9 and 60747-9 specifications are used to determine the calculation of the MOSFET switching energies [28]. For calculation of E_{on}, the integration limits of the switching curves are measured from the time at 10% of gate voltage (V_G) to the time at 2% of V_{DS}. E_{off} is calculated by taking limits from the time at 90% of $+V_G$ to the time at 2% of the drain source current (I_d), and E_{rr} is solved by taking limits from the time at the zero crossing of the diode reverse recovery current (I_{rr}) to the time at 2% of I_{rr}.

3

Case setup

To obtain results that are as close to reality as possible, it is important to obtain accurate information about the physical properties of the inverter constituent parts. Information about the physical drive system is sourced and used as a base for the modelling process. Modelling the entire system is carried out in PLECS, while extra post processing of the data is done in MATLAB and MS Excel. Three power modules from different manufacturers - CREE SiC, SEMIKRON SiC and DYNEX IGBT - are set up to be studied. While the CREE and DYNEX power module already had their complete thermal model available from their manufacturers' website, the SEMIKRON module's thermal model had to be created manually. Two methods in creating this model are used and a comparison is made between these methods. The setup of each part of these investigations is highlighted in this chapter.

3.1 Electric machine specification

The Inverter modelled and investigated in this thesis work is designed for the 230 kW and 800 V permanent magnet traction motor. The parameters of this machine are shown in Table 3.1.

Table 3.1: Radial flux permanent magnet Electric machine parameters

Specifications	Value	Units
Continuous Power rating	230	kW
Peak Power rating	350	kW
Number of pole pairs	4	-
Number of slots	48	-
Base speed	6000	RPM
Maximum speed	14000	RPM
Rated Current	650	Arms
Peak Torque	650	Nm

3.2 Battery, DC-link capacitor, Power Module and EM Modelling

The inverter model has to be built and tested before any investigations can be carried out. This section highlights the methodology used in modelling the major parts of the inverter. Figure 3.1 shows and overview of the model used for the DC-link ripple investigation which comprises the battery model, cable, bus-bar and power module models.

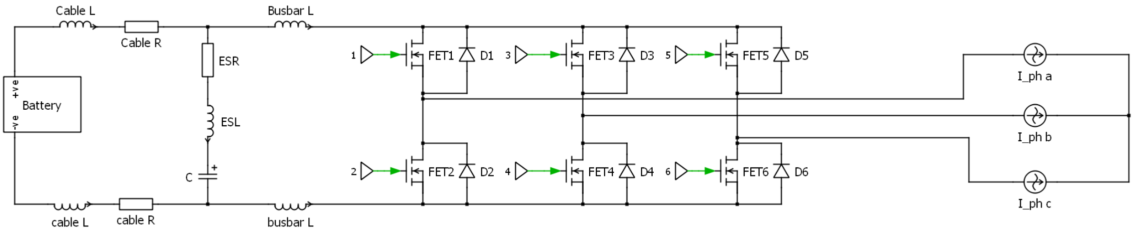


Figure 3.1: PLECS setup of two level three phase VSI

Figure 3.2 displays the thermal model utilised for the loss modelling. It can be observed that the cable, bus bar and ESL models are not considered in this set up. This is due to the overvoltages that become prevalent in the setup when it contains lots of inductances. This negatively affects the loss calculations of which are of major concern for this thesis. It should be noted that if these inductances are considered fully, snubber circuits for this model would have to be designed which is outside this scope of work.

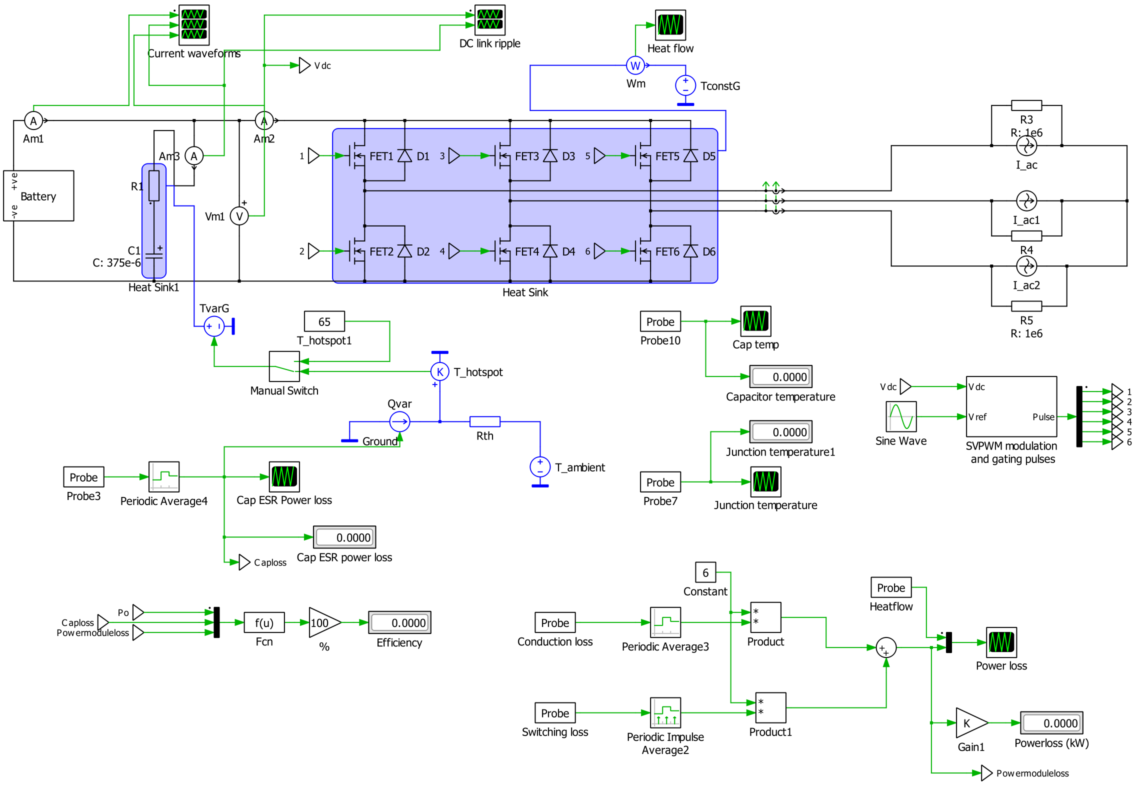


Figure 3.2: PLECS complete thermal VSI setup

3.2.1 Battery Model

The battery impedance behaviour is implemented as an R+ (R//C) series connection since we aim to study frequency ranges over 1 kHz [4].

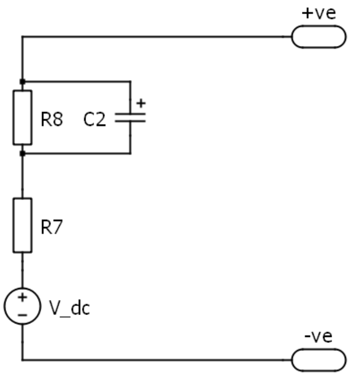


Figure 3.3: Battery model

Table 3.2: Battery Model Data

Vdc	R7	R8	C2
820 V	0.07 Ω	0.03 Ω	770 F

Table 3.2 shows the numeric values of the battery circuit components.

3.2.2 Cable Model

The cable impedance from the batteries is modelled as a resistance in series with an inductor, with values from existing rated cables for this requirement. The numeric values are measured by the supplier and found to be 1.5 mΩ and 420 nH respectively.

3.2.3 Busbar Model

The busbar is modelled as an inductor with rated values typically used to connect the battery with the power module. Valued at 1.2 nH as measured by the supplier.

3.2.4 DC-link Capacitor Model

The DC-link capacitor used in this study is an electrolytic type and is implemented as a capacitor with equivalent series inductance and resistance as shown in Figure 3.4.

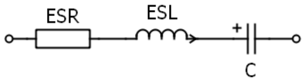


Figure 3.4: DC-link capacitor model

Table 3.3 highlights the numeric values of the capacitor model assumed in this modelling process.

Table 3.3: Capacitor model data for ripple investigation

ESR	ESL	C
0.5 mΩ	8 nH	375 uF

For the loss investigation, one-third of ESR i.e, 0.17 mΩ is assumed.

3.2.5 Power Module Model

The default power MOSFETs model in the PLECS library is employed in this inverter especially since it characterizes the reverse conduction phenomenon of SiC MOSFETS. A single ideal MOSFET with an external freewheeling diode that represents the actual intrinsic body diode is used. This allows for more accurate thermal modelling as explained in [21] and [30]. Figure 3.5 and Figure 3.6 show the model of a SiC and IGBT power module respectively. For the IGBT power module, the IGBT switch along with an antiparallel diode model in PLECS library is utilized, since it fulfils the requirement needed for this work.

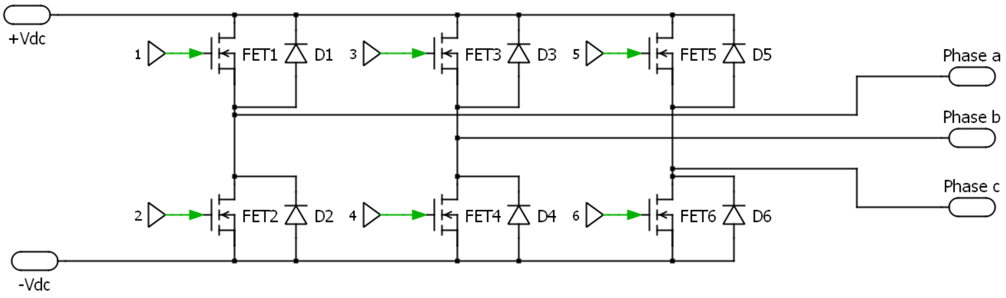


Figure 3.5: Simulation setup of SiC Power module

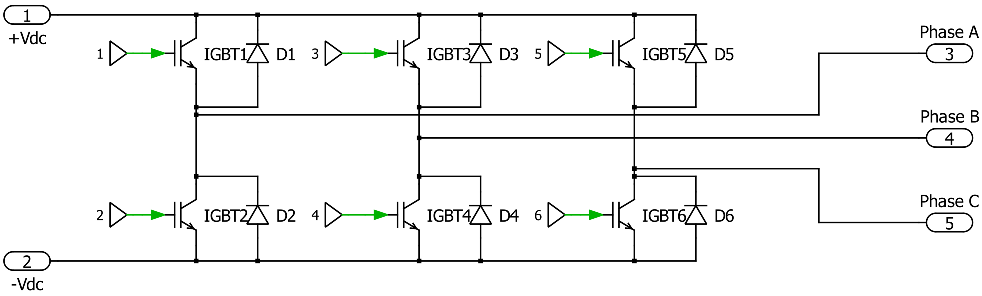


Figure 3.6: Simulation setup of IGBT Power module

3.2.6 Electric machine Model

For the sake of simplicity, the electric machine part of the inverter is modelled as a three-phase constant current source, phase-shifted by 120°with a current angle lagging the voltage angle to depict the inductive behaviour of an electric machine. This can be seen in Figure 3.1

3.3 Ripple investigation setup

This test set up considers the listed operating points in Table 3.4

Table 3.4: Test Operating Points

n (kRpm)	Torque (Nm)	U (Vrms)	I (Arms)	CurAngle (°)	Vang (°)	ϕ (°)	f (Hz)	Pel (kW)	Pmech (kW)
1.577	50	54.3	52.8	15.02	24.3	-9.3	105.1	8.5	8.3
2.787	45	94.8	47.9	14.1	22.5	-8.4	185.8	13.5	13.13
3.896	35	130.5	37.9	11.9	18.5	-6.5	259.7	14.7	14.3
6.606	48	225.1	51.5	15.0	23.9	-8.9	440.4	34.3	33.2
6.937	48	236.3	51.5	15.04	23.9	-8.8	462.5	36.1	34.9
2.42	37	81.5	39.7	12.3	19.2	-6.9	161.3	9.6	9.38
5	650	278.9	647.7	47.5	95.3	-48.2	333.3	361.3	340.3
6	550	313.6	526.9	46.4	89.6	-43.2	400	361.7	345.6
14	200	323.8	318.3	73.7	80.6	-6.9	933.3	307	293.2

3.3.1 Voltage Ripple

In this thesis work, the voltage ripple is defined as the peak to peak voltage value across the capacitor. Firstly, a simple inverter model is built without the cable and busbar impedances. After the above inverter modelling is achieved, the dc-link voltage ripple at various operating points is then compared to theoretical calculations from (2.17) - (2.21) to confirm a proper functioning model. The voltage ripple is measured by using the PLECS probe block to probe the DC-link capacitor's voltage and is viewed through a scope block. The discrepancy with simulated voltage ripple at some operating points are shown in Table 4.1.

After the simulation is confirmed to work satisfactorily, the cable and busbar impedances are added and the voltage ripple behavior is further investigated by varying some other parameters - these are further highlighted in Chapter 4 - the results section.

3.3.2 Current Ripple

The current ripple in this work is defined as the RMS current through the dc-link capacitor. As with the voltage ripple, the RMS current ripple in the dc-link capacitor of the simulated inverter model is measured and these values are compared with the analytical equation from (2.22). It is likewise measured by probing the dc-link capacitor current using the PLECS probe block and connecting its output to the RMS calculation block. For the first six operating points in Table 3.4, the following current ripple values were obtained and shown in Table 4.2

3.4 Electrical losses determination setup

The next step is to determine the electrical losses of the inverter at selected operating points. The main losses considered in this setup are the switching and conducting losses of the power module and the ohmic losses in the dc-link capacitor. The switching and conduction losses are first calculated analytically at an operating point, then these values are used to compare the losses obtained from the PLECS model. No analytical model is done for the DC-link capacitor electrical losses since it is just the product of the square of the RMS value of the current passing through the equivalent series resistor (ESR).

3.4.1 Analytical Electrical losses

Analytical losses of the inverter are calculated using MATLAB script that uses the current switching and conduction paths to quantify the losses according to the theoretical equations. This MATLAB script utilizes information of the fundamental output voltage and current, load angle, and other parameters to determine the SVPWM switching signals and instantaneous voltage signals of the switches. By defining the current through each component at each instant in time, the conduction loss is easily calculated. The analytical switching loss is then calculated using (2.26).

3.5 Thermal network setup

All semiconductor devices have a maximum junction temperature specified in their datasheet which, when exceeded, can lead to permanent breakdown of the component. The thermal description of the components determines the change in junction temperature caused by the increase in losses. At certain operating points, the junction temperature can go beyond the breakdown limits of the component which leads to permanent breakdown. This requires an accurate design of the heat sink and the coolant flow for a proper functioning of the component. The thermal setup used is defined as a thermal impedance network as shown in Figure 3.7 which is the exact characterization of the thermal properties of the component. A detailed heat sink design will not be carried out in this study. The initial coolant fluid and junction temperatures are set to 65°C for the single operating points loss calculation, while for the machine loss map generation it is set to 80°C since this is the same temperature point that was used in generating the machine torque and speed data.

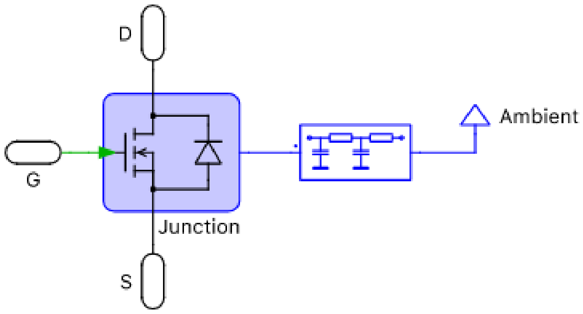


Figure 3.7: Thermal impedance network from Junction to Ambient

3.5.1 Thermal description of CREE and DYNEX power module

The thermal description of CREE and DYNEX power module is obtained as an .xml file from the manufacturers website and imported into the PLECS thermal library. This thermal description contains the V-I-T characteristics, turn on and turn off switching energies, thermal impedance network and other variables for the switching devices as shown in Figures 3.8, 3.9 and 3.10 respectively. The thermal description of the DYNEX IGBT power module can be seen in Appendix 4.

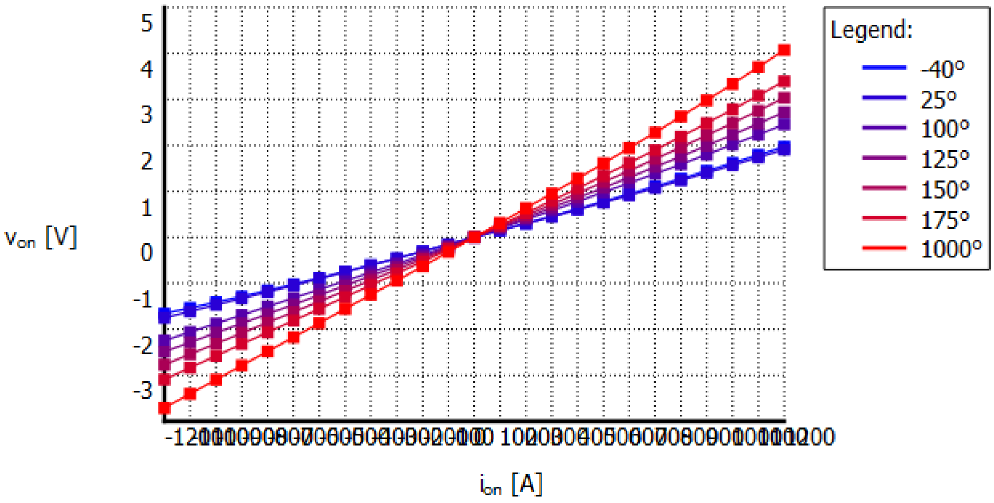
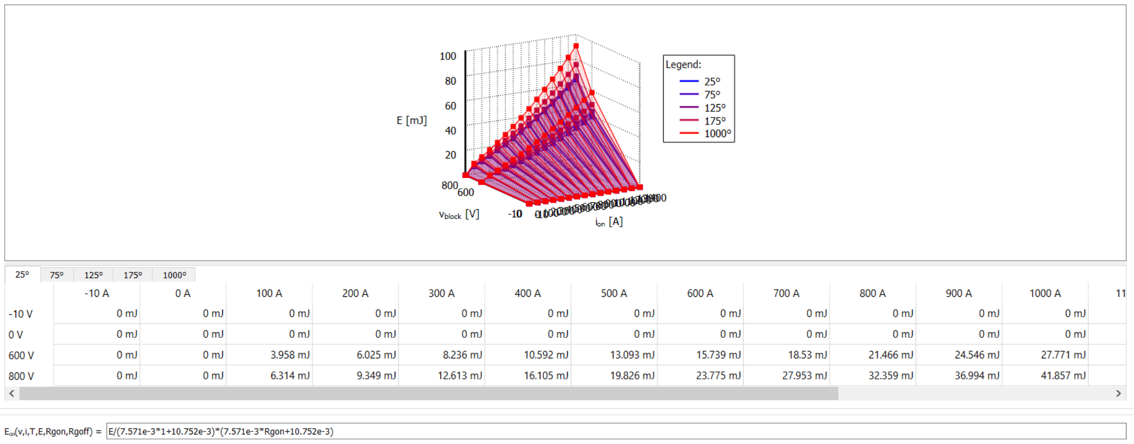


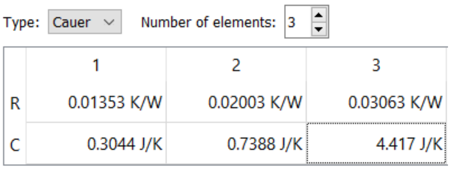
Figure 3.8: V I characteristics of CREE CAB760M12HM3



	-10 A	0 A	100 A	200 A	300 A	400 A	500 A	600 A	700 A	800 A	900 A	1000 A	11
-10 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	
600 V	0 mJ	0 mJ	3.958 mJ	6.025 mJ	8.236 mJ	10.592 mJ	13.093 mJ	15.739 mJ	18.53 mJ	21.466 mJ	24.546 mJ	27.771 mJ	
800 V	0 mJ	0 mJ	6.314 mJ	9.349 mJ	12.613 mJ	16.105 mJ	19.826 mJ	23.775 mJ	27.953 mJ	32.359 mJ	36.994 mJ	41.857 mJ	

E_{on}(v,i,T,E,Rgon,Rgoff) = E/(7.571e-3*1+10.752e-3)*(7.571e-3*Rgon+10.752e-3)

Figure 3.9: Switching energy lookup table of CREE CAB760M12HM3



Type: Cauer

Number of elements: 3

	1	2	3
R	0.01353 K/W	0.02003 K/W	0.03063 K/W
C	0.3044 J/K	0.7388 J/K	4.417 J/K

Figure 3.10: Thermal impedance network of CREE CAB760M12HM3

These descriptions are given as lookup tables at different temperatures and with different test conditions and are then assigned to the MOSFETs and diodes used in the PLECS model. It is important to note that this CREE model defines the switching energies using the "lookup table and formula" approach within PLECS [30].

$$E_{swon} = \frac{E((7.571e^{-3}R_{gon}) + 10.752e^{-3})}{(7.571e^{-3} \cdot 1) + 10.752e^{-3}} \tag{3.1}$$

$$E_{swoff} = \frac{E((6.659e^{-3}R_{goff}) + 8.400e^{-3})}{(6.659e^{-3} \cdot 1) + 8.400e^{-3}} \tag{3.2}$$

(3.1) and (3.2) highlight the dependency of the turn on and turn off resistances on the switching energies where E_{swon} and E_{swoff} are the final turn on and turn off energies at the tested operating points, E is the initial turn on or turn off energy at a specific operating test point with gate resistances as 1 Ω, and R_{gon} and R_{goff} are the turn on and turn off gate resistances.

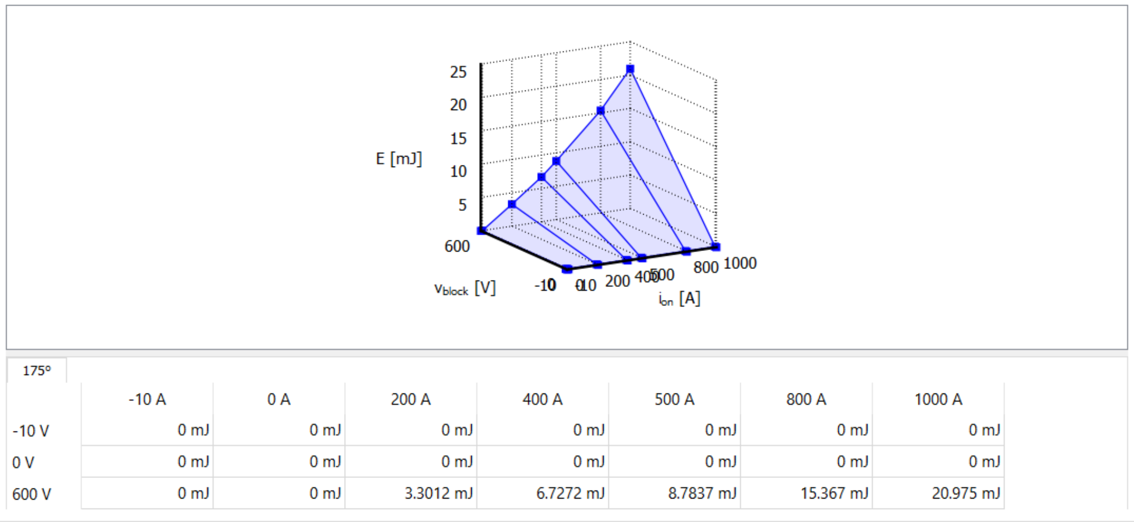
The switching energies can be adapted by varying numeric parameters of R_{gon} and R_{goff} which are displayed as compulsory inputs in PLECS. For the first case study, these values are kept at 1 Ω which represent switching resistances similarly used in the datasheet test conditions while for the second study, values of 4.1 Ω are assumed to make a comparison with the second power module type.

It should be noted that the default thermal impedance network for the CREE power module is used for single analysis of its losses while for loss map calculation and comparison with semikron power module, the thermal impedance used is provided from Computational Fluid Dynamics (CFD) calculations for 10 liter/minute coolant flow rate at the cooling fins.

3.5.2 Thermal description of the Semikron power module

3.5.2.1 Case 1 - Using datasheet plots

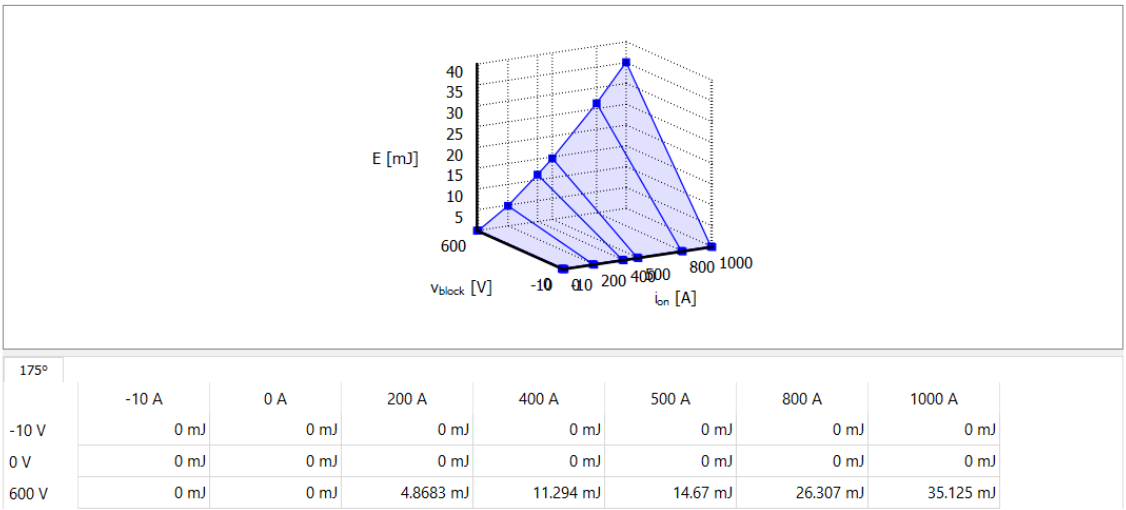
Initially, the datasheet of the power module is used to construct the I-V-T characteristics and switching energy curves for the conduction and switching loss calculation in PLECS. PLECS can interpret data points from datasheets of switches as long as the proper axes and units are defined [30]. The I-V-T characteristics is used to generate the lookup tables for the conduction losses at four different temperatures - 25°C, 85°C, 150°C and 175°C. The switching characteristics is only given at a V_{DS} voltage of 600 V and 175°C as this is the only operating point for switching highlighted in its datasheet. Figures 3.16 and 3.17 show the switching energies generated from its datasheet while Figure 3.13 shows the generated I-V-T characteristics for this module.



175°

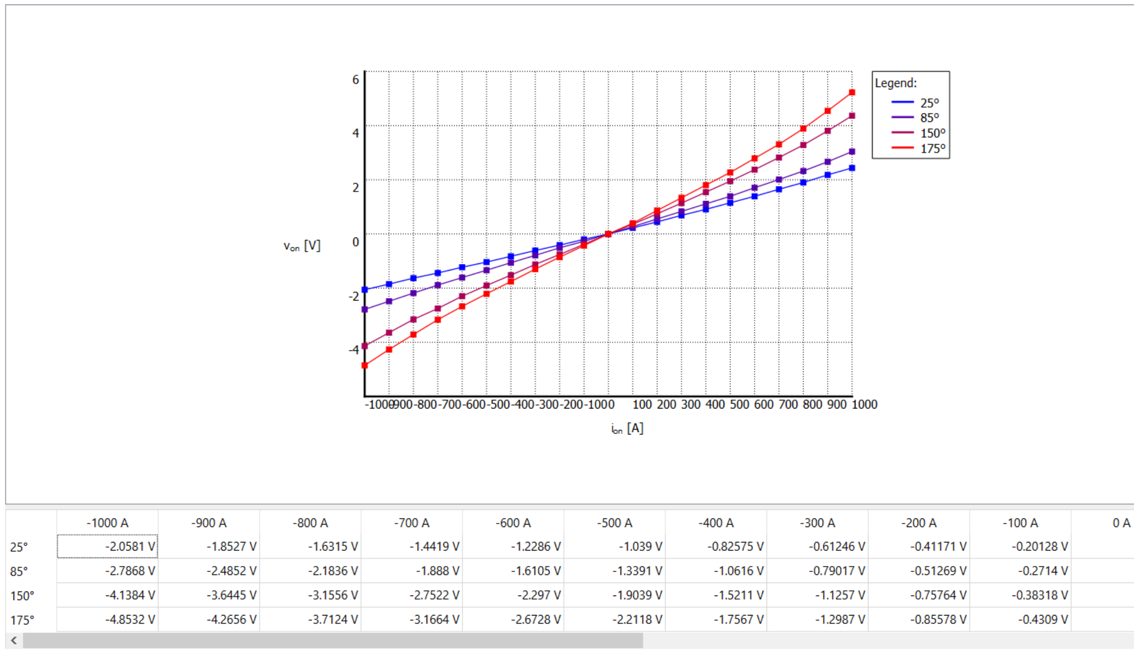
	-10 A	0 A	200 A	400 A	500 A	800 A	1000 A
-10 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
600 V	0 mJ	0 mJ	3.3012 mJ	6.7272 mJ	8.7837 mJ	15.367 mJ	20.975 mJ

Figure 3.11: Semikron Turn-on switching energies obtained using datasheet



	-10 A	0 A	200 A	400 A	500 A	800 A	1000 A
-10 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
600 V	0 mJ	0 mJ	4.8683 mJ	11.294 mJ	14.67 mJ	26.307 mJ	35.125 mJ

Figure 3.12: SemiKron Turn-off switching energies obtained using datasheet



	-1000 A	-900 A	-800 A	-700 A	-600 A	-500 A	-400 A	-300 A	-200 A	-100 A	0 A
25°	-2.0581 V	-1.8527 V	-1.6315 V	-1.4419 V	-1.2286 V	-1.039 V	-0.82575 V	-0.61246 V	-0.41171 V	-0.20128 V	
85°	-2.7868 V	-2.4852 V	-2.1836 V	-1.888 V	-1.6105 V	-1.3391 V	-1.0616 V	-0.79017 V	-0.51269 V	-0.2714 V	
150°	-4.1384 V	-3.6445 V	-3.1556 V	-2.7522 V	-2.297 V	-1.9039 V	-1.5211 V	-1.1257 V	-0.75764 V	-0.38318 V	
175°	-4.8532 V	-4.2656 V	-3.7124 V	-3.1664 V	-2.6728 V	-2.2118 V	-1.7567 V	-1.2987 V	-0.85578 V	-0.4309 V	

Figure 3.13: SemiKron I-V-T Characteristics

3.5.2.2 Case 2 - Using SPICE model

Since this power module is in the development phase, the authors realized the testing points of the switching energies from the datasheet required for the setup of the lookup tables may not be sufficient to obtain accurate results. Thus double pulse testing on the SPICE model of the Semikron power module is carried out in the ORCAD Pspice environment to determine the turn on and turn off switching energies of the SEMIKRON power module at more operating test conditions. The setup is shown in Figure 3.14. 16 V and -4 V are used as the turn-on and turn-off gate voltages respectively similar to the testing conditions from its datasheet. The switching energies of a single chip are obtained and multiplied by six since this module consists of six chips.

Switching energies are derived at 500 V, 705 V and 850 V; and 25°C and 175°C using the IEC 60747 specifications stated in Section 2.8. The values of switching energies obtained at these test conditions are used to form the final lookup tables in PLECS as shown in Figures 3.16 and 3.17 for determining switching losses. The conduction loss look up table is left the same as before since its data points are sufficient. The thermal impedance network from the junction to the coolant of this power module is represented as a cauer network as shown in Figure 3.18.

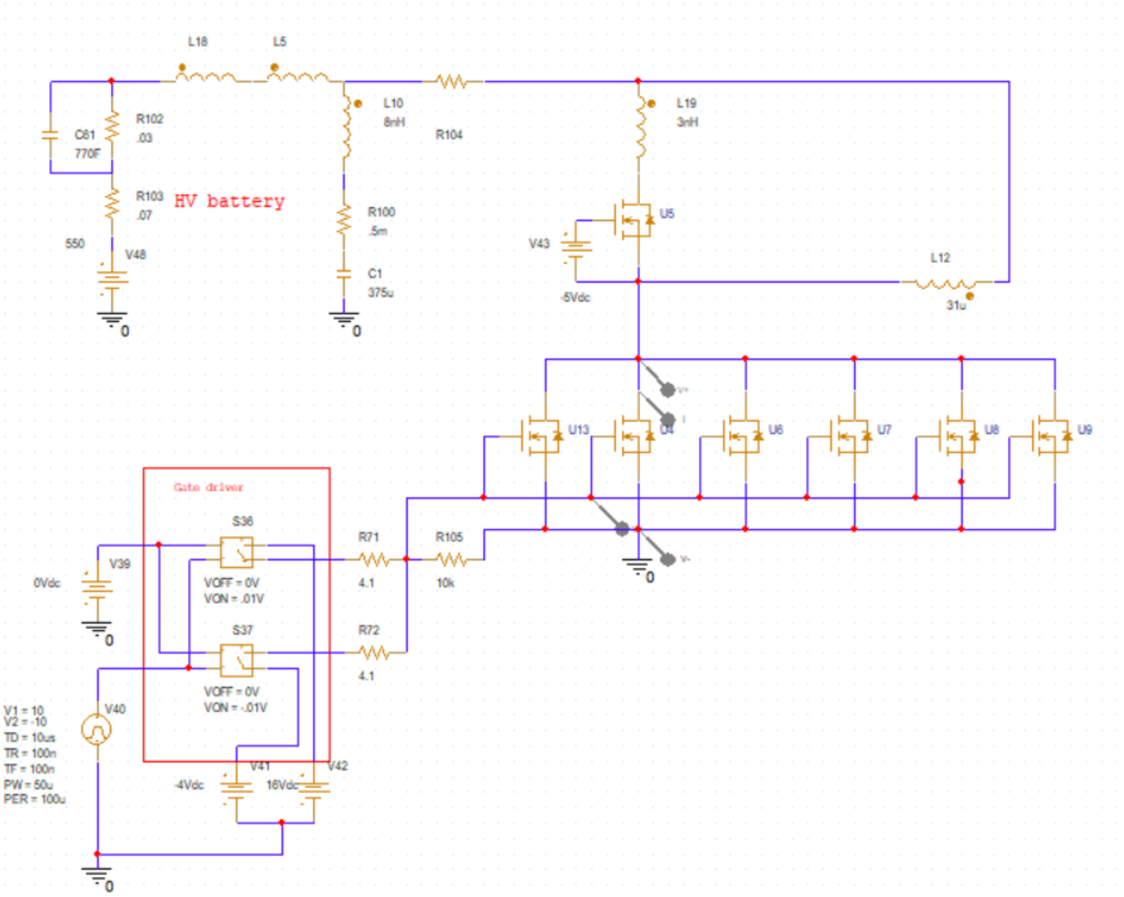


Figure 3.14: PSpice setup to determine the Semikron Power module switching energies from its SPICE model

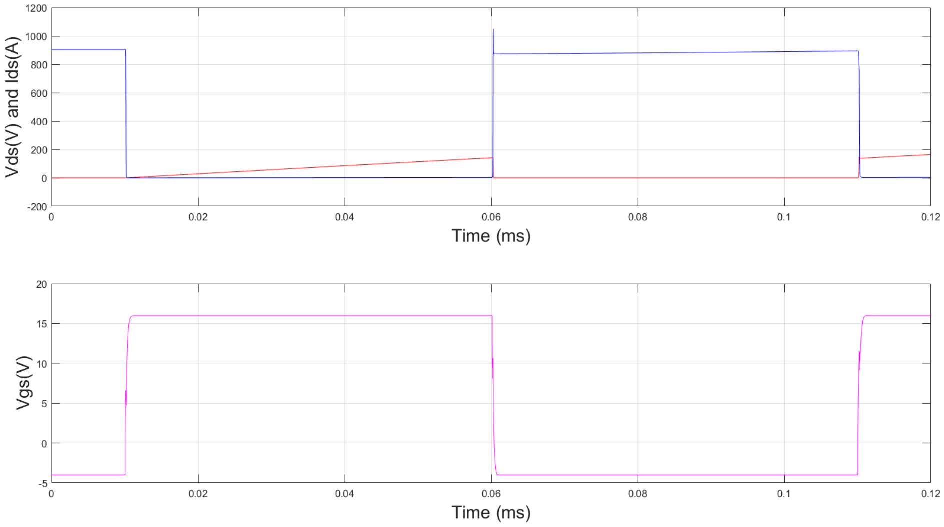
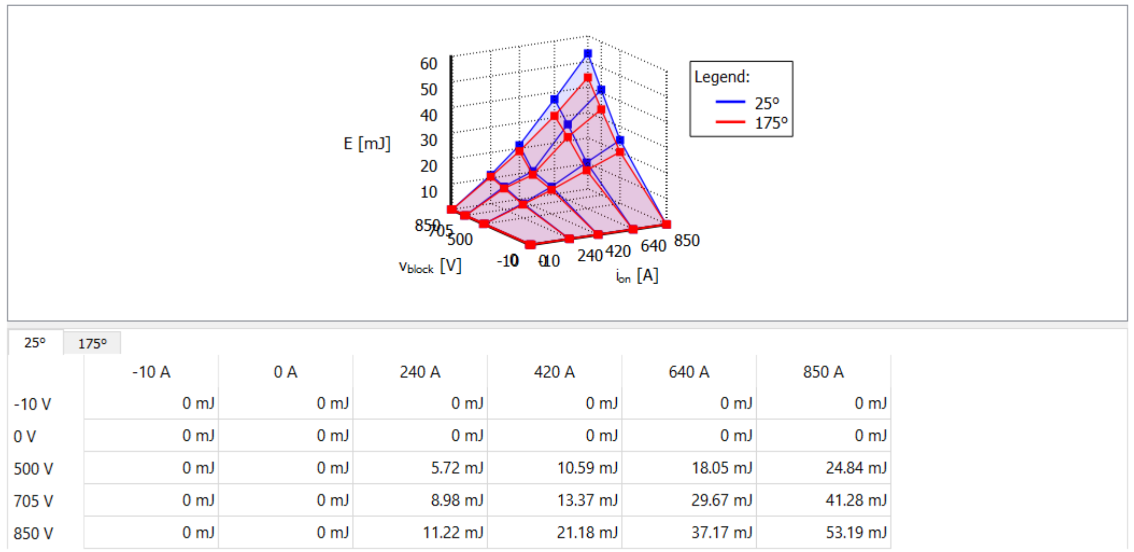


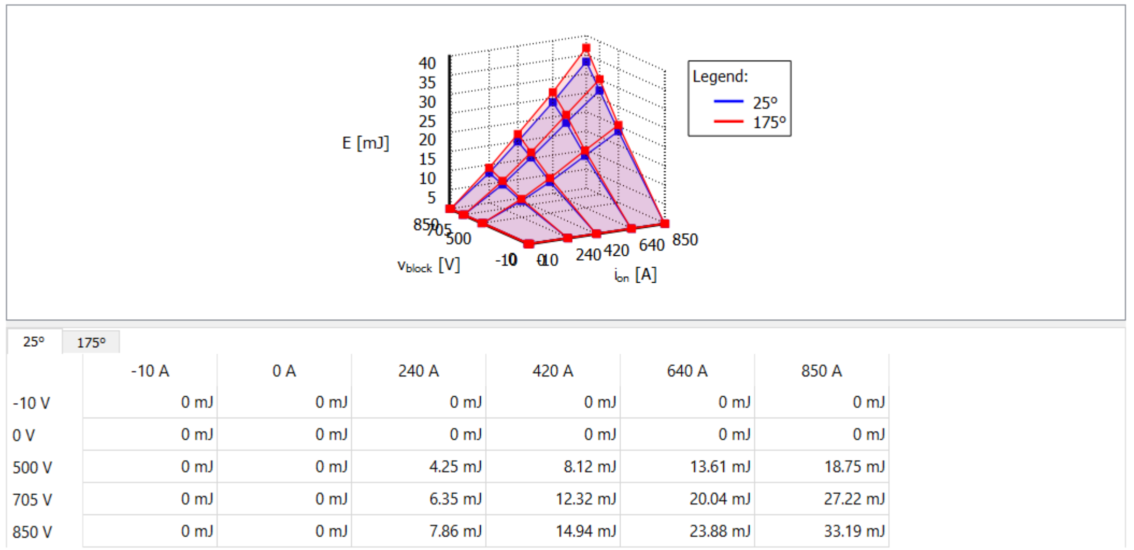
Figure 3.15: Semikron PSpice DPT plots at L = 190 µH

Figure 3.15 shows the switching curves of the semikron power module gotten at an operating point with inductance values of 190 µH, a temperature of 25°C and Vavg of 850 V.



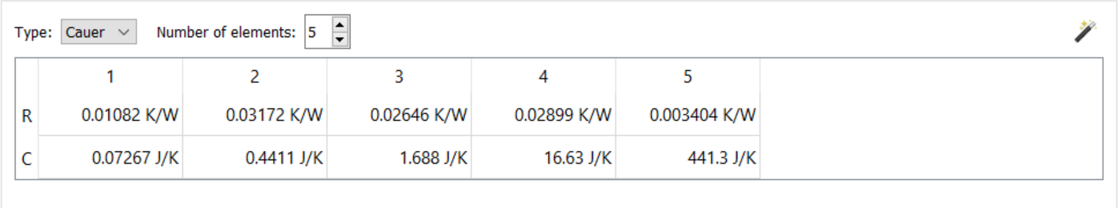
	-10 A	0 A	240 A	420 A	640 A	850 A
-10 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
500 V	0 mJ	0 mJ	5.72 mJ	10.59 mJ	18.05 mJ	24.84 mJ
705 V	0 mJ	0 mJ	8.98 mJ	13.37 mJ	29.67 mJ	41.28 mJ
850 V	0 mJ	0 mJ	11.22 mJ	21.18 mJ	37.17 mJ	53.19 mJ

Figure 3.16: Turn on switching energies of Semikron Power module



	-10 A	0 A	240 A	420 A	640 A	850 A
-10 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
500 V	0 mJ	0 mJ	4.25 mJ	8.12 mJ	13.61 mJ	18.75 mJ
705 V	0 mJ	0 mJ	6.35 mJ	12.32 mJ	20.04 mJ	27.22 mJ
850 V	0 mJ	0 mJ	7.86 mJ	14.94 mJ	23.88 mJ	33.19 mJ

Figure 3.17: Turn off switching energies of Semikron Power module



Type: Cauer Number of elements: 5

	1	2	3	4	5
R	0.01082 K/W	0.03172 K/W	0.02646 K/W	0.02899 K/W	0.003404 K/W
C	0.07267 J/K	0.4411 J/K	1.688 J/K	16.63 J/K	441.3 J/K

Figure 3.18: Thermal impedance network of the Semikron Power module

3.5.3 Thermal network of the DC-link capacitor

The determination of the hotspot temperature is of main importance because it is one of the main inducers of failure. It can be monitored by proper thermal modelling of the DC-link capacitor. Figure 3.19 shows the thermal network of the DC-link capacitor. The hotspot temperature is dependent on the thermal impedance and the ESR loss of the DC-link capacitor.

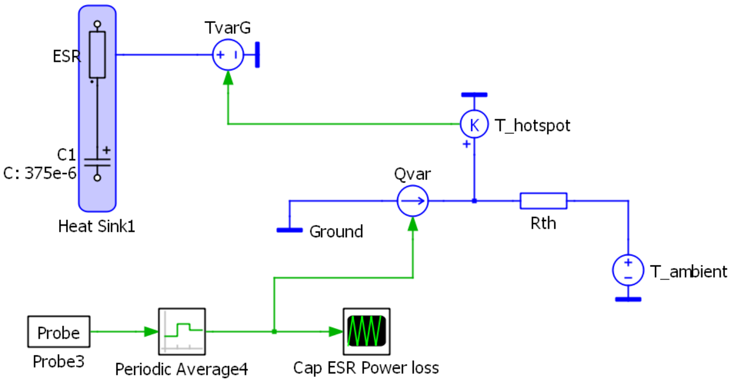


Figure 3.19: Thermal network of the DC-link capacitor

3.5.4 Thermal losses from PLECS

The lookup tables from the thermal descriptions are used to calculate the conduction and switching losses at the initial temperature and then sent as inputs to the thermal network to determine the change in temperature for the next iteration. This new temperature is used to calculate the losses during the next iteration. This procedure is repeated until the system reaches some steady state temperature. The simulated power module losses using CREE and Semikron types with and without temperature dependency for the selected operating points are shown in the results section.

3.5.5 MATLAB - Simscape Program

A simscape model of the inverter is also built with the main purpose of comparing penultimate results in terms of both values and speed of calculations with the PLECS model. In this study, however, some shortcomings of this setup are discovered which are illuminated in Section 5.

4

Results Evaluation and Analysis

This chapter highlights the results of the already discussed case setups. Firstly, preliminary ripple studies are presented, followed by preliminary electrical loss investigations on CREE SiC power module along with some analysis on this module. Then, studies with complete thermal incorporation of the three different power modules are compared and illustrated. Finally, derived loss maps using current and voltage data from the electric machine highlighted in Section 3.1, for the different power modules are then portrayed.

4.1 Preliminary Ripple Study

As stated in Section 3, ripple investigation proceeded after discrepancies with analytical values are known. Table 4.1 shows the comparison between the simulated voltage ripple values without cable and busbar impedances and, the theoretical values.

Table 4.1: Simulated Voltage Ripple vs Analytical

n(kRpm)	Tq(Nm)	Analytical Voltage ripple (Vpp)	Simulated Voltage Ripple(Vpp)	% discrepancy
1.577	50	1.186	1.171	1.26
5	650	42.489	35.16	17.25
14	200	9.816	10.4	-5.62

Table 4.1 highlights the voltage ripple discrepancies at selected operating points. At most, a 17% disparity is seen at high operating currents. This may be attributed to the positioning of the voltage and current angles in different sectors of the SVPWM plane at this operating point since the analytical equations assume both current and voltage angles to be in the same sectors.

Additionally, Table 4.2 shows the variation of the simulated current ripple values with the theoretical values.

Table 4.2: Simulated Current Ripple vs Analytical

n(kRpm)	Tq(Nm)	Analytical Current ripple (Arms)	Simulated Current ripple (Arms)	% discrepancy
1.577	50	24.43	23.98	1.84
5	650	335.86	316.34	5.81
14	200	103.81	103.26	0.53

From the data obtained in Table 4.2, it is observed that at most only a 6% discrepancy between the theoretical and simulated current ripple is observed, hence confirming reasonable agreement with the simulation.

Table 4.3 highlights the voltage and current ripple simulated at the entire open-loop operating points with cable and busbar impedances included.

Table 4.3: Simulated voltage and current ripple at selected operating points

n(kRpm)	Tq(Nm)	Simulated Voltage ripple (Vpp)	Simulated Current Ripple (A) rms
1.577	50	1.250	25.88
2.787	45	1.807	29.90
3.896	35	1.770	26.30
6.606	48	2.730	35.8
6.937	48	2.700	35.01
2.42	37	1.330	23.382
5	650	47.35	369.9
6	550	40	274.7
14	200	13.5	112.5

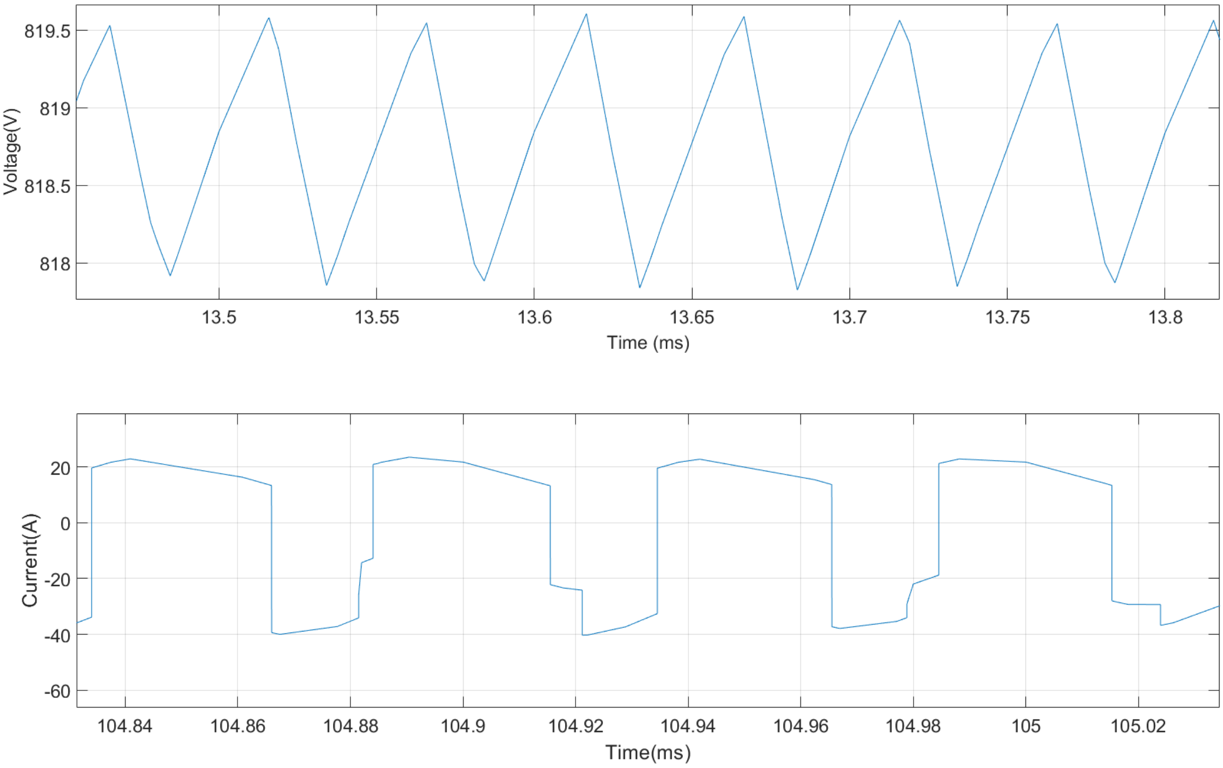


Figure 4.1: Voltage and Current Ripple waveforms at 3.90 kRpm and 35 Nm

Figure 4.1 shows the capacitor voltage and current waveforms at a speed of 3900

Rpm and torque of 35 Nm. A peak to peak voltage ripple of 1.7 V is observed while the RMS value of the current waveform at this point is found to be about 26.3 Arms.

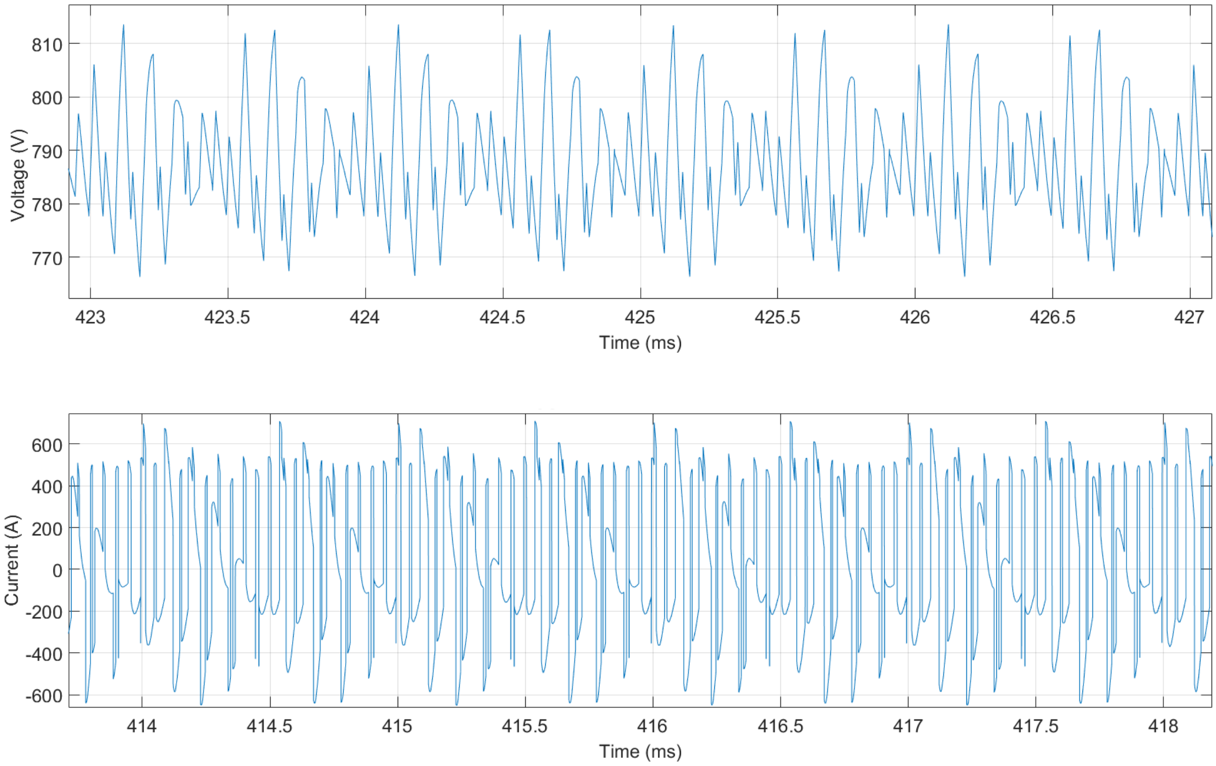


Figure 4.2: Voltage and Current Ripple waveforms at 5 kRpm and 650 Nm

Figure 4.2 displays the capacitor voltage and current waveforms at a higher operating point of 5000 Rpm and torque of 650 Nm. A peak to peak voltage ripple of 47 V is observed while RMS value of the current waveform at this point is found to be about 370 Arms.

4.1.1 Ripple vs Switching Frequency

The current and voltage ripple values are then analyzed for their response to changes in the switching frequency. Figure 4.3 shows the change in voltage and current ripple with switching frequency. Different operating points such as 1.5 kRpm, 50 Nm; 5 kRpm, 650 Nm; and 14 kRpm, 200 Nm are analysed. It is observed that increasing the switching frequency decreases the voltage ripple proportionally at different operating points. For the 14 kRpm operating condition, increasing the switching frequency from 10 kHz to 40 kHz reduces the voltage ripple to around 81%. On the other hand, a negligible decrease of 12.5% is observed in the current ripple. The maximum percentage variation is seen at 14 kRpm, 200 Nm operating point.

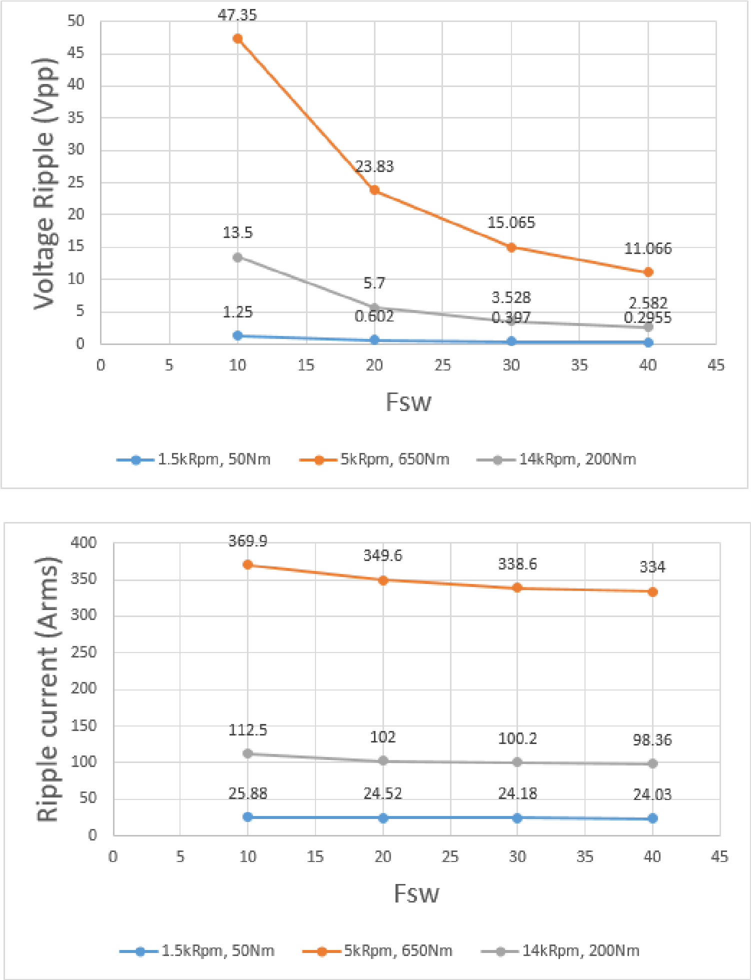


Figure 4.3: Voltage and Current Ripple variation with switching Frequency

4.1.2 Ripple vs DC-link Capacitor Brands

The dc-link capacitor brands investigated here are, for the sake of anonymity, identified as Cap 1, Cap 2 and Cap 3. Relevant parameters of these components are shown in Table 4.4. The ripple attenuation of these dc-link capacitors are studied at three different operating points: 1.5 kRpm, 50 Nm; 5 kRpm, 650 Nm; and 14 kRpm, 200 Nm.

Table 4.4: Dc-link Capacitors Parameters

Dc-link Capacitor	Capacitance (µF)	ESR (mΩ)	ESL (nH)
Cap 1	400	0.4	6
Cap 2	375	0.6	7
Cap 3	375	0.8	9

Figure 4.4 shows almost similar ripple values of the three capacitors at the different operating points, however, there is less voltage ripple observed for Cap 1 capacitor

at the 5 kRpm and 14 kRpm operating points. This is expected since it has a capacitance of 400 µF which is greater than the capacitance of the other two and the voltage ripple is known to be inversely proportional to the dc-link capacitance. On the other hand, the current ripple is roughly the same for all capacitors and operating points. This is expected since the current ripple mainly depends on the modulation index, load angle and peak value of output current. Since these values remain the same at each operating point, the observed behaviour of the current ripple is expected.

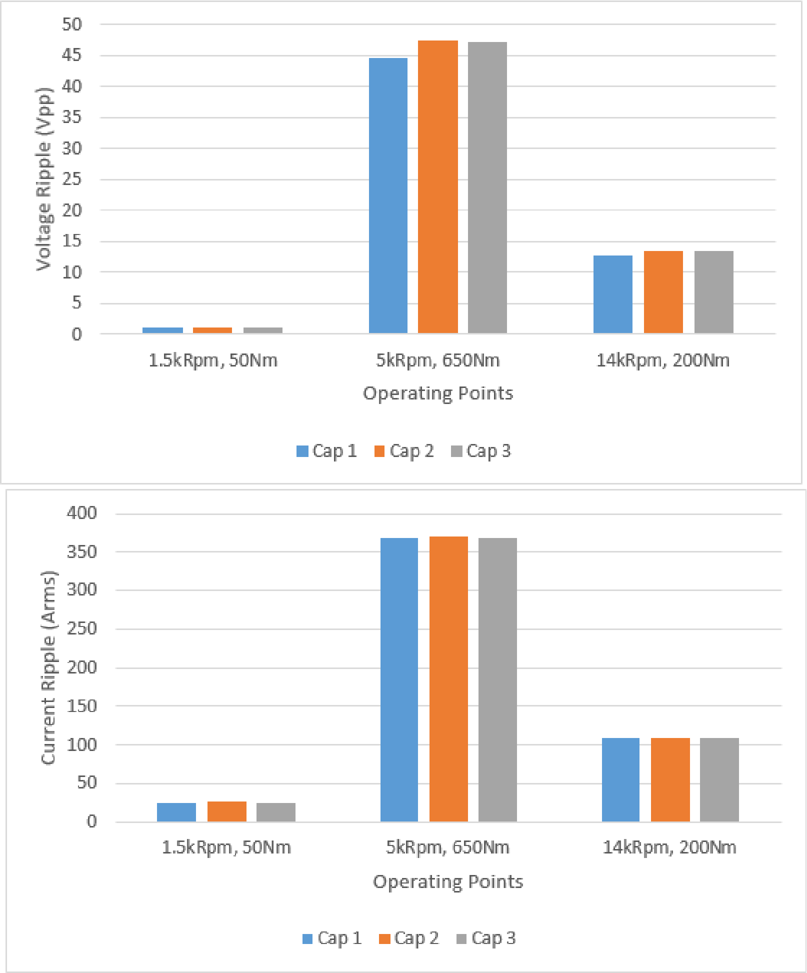


Figure 4.4: Voltage and Current Ripple variation with Dc-link capacitor brands

4.2 DC-link capacitor loss

In this section, the losses present in the DC-link capacitor along with its hot spot temperature at different operating points are made. An ideal cooling of the surface is assumed.

Table 4.5 shows the DC-link capacitor ratings and the test conditions used as given in the datasheet.

Table 4.5: Test setup

DC-link capacitor	375 µF
Ambient temperature (°C)	80
Thermal resistance (°C/W)	0.76
Max.hot spot temperature (°C)	105
ESR (mΩ)	0.17

Table 4.6 shows the DC-link capacitor losses and its hot spot temperature at three different operating conditions. And, it is observed that with an increase in current demanded by the load, the DC-link capacitor losses and its hot spot temperature increase. It is also seen that at the maximum current operating condition, the DC-link capacitor's hot spot temperature is well within its maximum limit of 105 °C.

Table 4.6: Simulated DC-link capacitor losses and its hot spot temperature

n (kRpm)	Tq (Nm)	DC-link capacitor loss (W)	Hot spot temperature (°C)
1.577	50	0.1	80.07
5	650	16.9	92.87
14	200	1.7	81.27

4.2.1 DC-link capacitor loss Vs switching frequency

The dc link capacitor loss is analyzed with varying switching frequency for three different operating points. A maximum of 8.5% increase in loss is observed at 5000 Rpm operating point when increasing the switching frequency from 10 kHz to 25 kHz. Whereas, at low operating points the losses do not vary much with the increase in switching frequency. These can be seen in Figure 4.5.

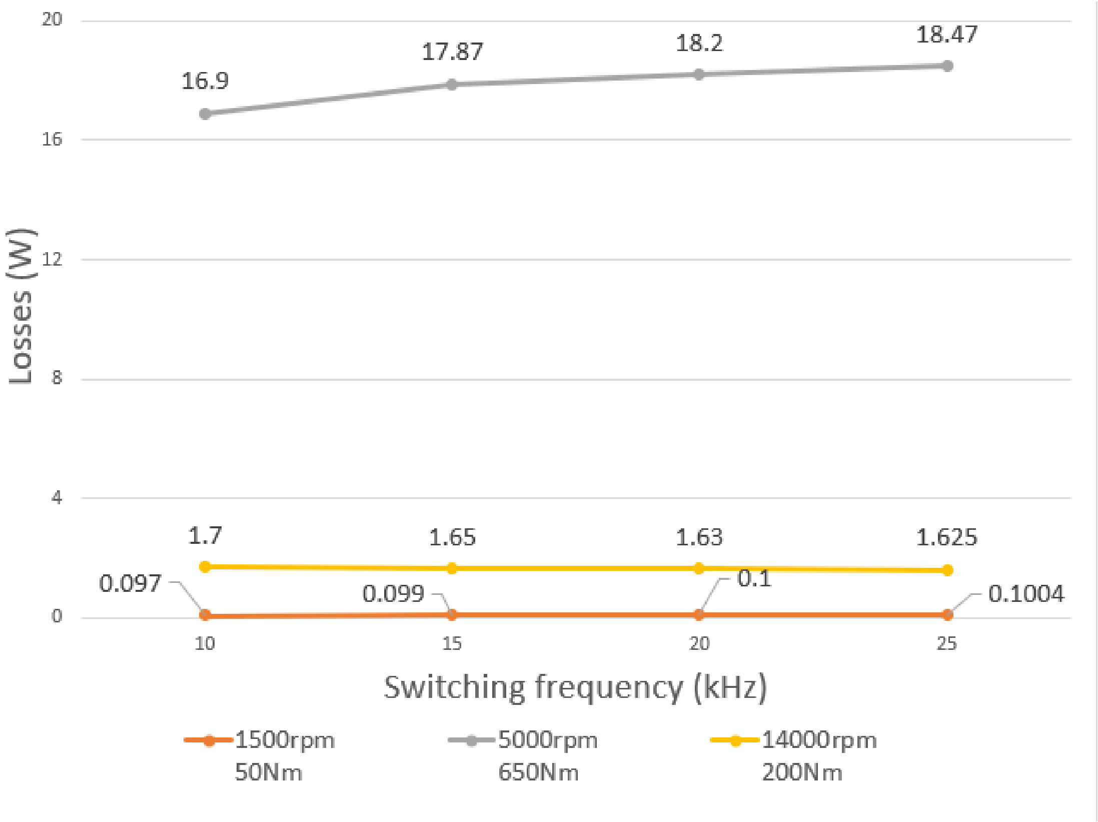


Figure 4.5: DC-link capacitor loss Vs Switching Frequency

4.2.2 ESR Versus DC-link capacitor losses

The ESR present in the DC-link capacitor is varied up to 200% of the nominal value, i.e 0.34 mΩ, and the losses are noted and shown in Figure 4.6. It can be seen that increasing the ESR increases the losses proportionately. A maximum of 66.8 W power loss is observed at 200% of the nominal value.

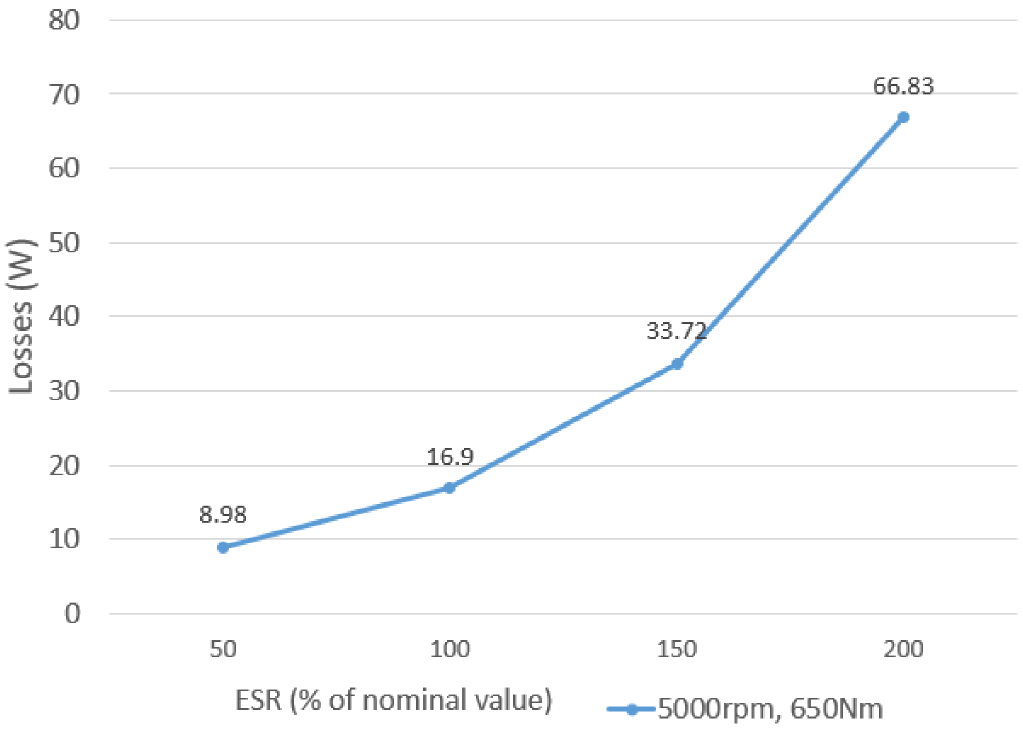


Figure 4.6: DC-link capacitor loss Vs Switching Frequency

4.3 Preliminary Electrical Loss Analysis using CREE Power module

In this section, the discrepancy between simulated and analytical electrical loss values of a single switch in a power module are first described, then electrical loss analysis which consists of studying the influence of the different operating points, switching frequency, and gate resistances on the losses are done.

Table 4.7 shows the discrepancy between the simulated and analytical loss values using a fixed on-state resistance of 1.45 mΩ.

Table 4.7: Simulated electrical losses vs analytical using a fixed Rdson for a single MOSFET

n(kRpm)	Tq(Nm)	Conduction loss -Analytical (W)	Conduction loss- Simulated (W)	% discrepancy
1.577	50	2.0172	2.017	0.01
5	650	304.3459	303.55	0.26
14	200	73.55	73.7	-0.20

n(kRpm)	Tq(Nm)	Switching loss -Analytical (W)	Switching loss- Simulated (W)	% discrepancy
1.577	50	17.64	18.8	-6.58
5	650	202.23	210.6	-4.14
14	200	95.91	100.2	-4.47

Table 4.8 shows the impact of the variation of on-state resistance with temperature on the conduction losses. And it is observed that at 5000Rpm, 650Nm operating point, the variance is around 17.35% because of the influence of junction temperature rise on the losses.

Table 4.8: CREE Simulated Conduction losses with temperature dependency for a single MOSFET

n(kRpm)	Tq(Nm)	Simulated Conduction loss with temp dependency (W)	% discrepancy
1.577	50	2.12	4.86
5	650	367.3	17.35
14	200	79	6.71

Figure 4.7 shows the analytical conduction loss of the upper and lower transistors with reverse conduction at 14kRPM, 200Nm operating condition.

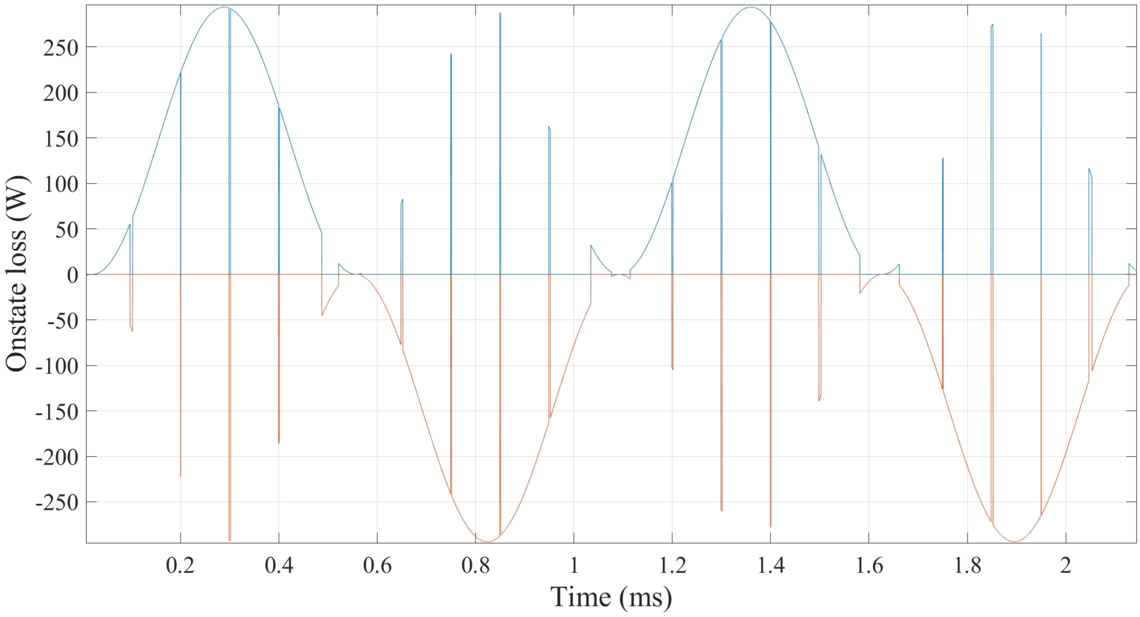


Figure 4.7: Analytical conduction loss of the SiC MOSFET at 14 kRPM,200 Nm

4.3.1 Electrical losses vs Different operating points

The variation of electrical losses at three different operating points with a constant switching frequency of 10 kHz for one MOSFET is illustrated in Figure 4.8. The operating points are selected because of the different voltage and current demands they place on the inverter. Since the conduction and switching losses are dependent on the current flowing through the switches, the losses at operating points with low current demand have lower losses. For example, at an operating point of 1.5 kRpm, 50 Nm, the current demanded by the electric machine is small compared to the 5 kRpm, 650 Nm operating condition. Thus the losses are low in the 1.5 kRpm, 50 Nm operating point, as observed in Figure 4.8.

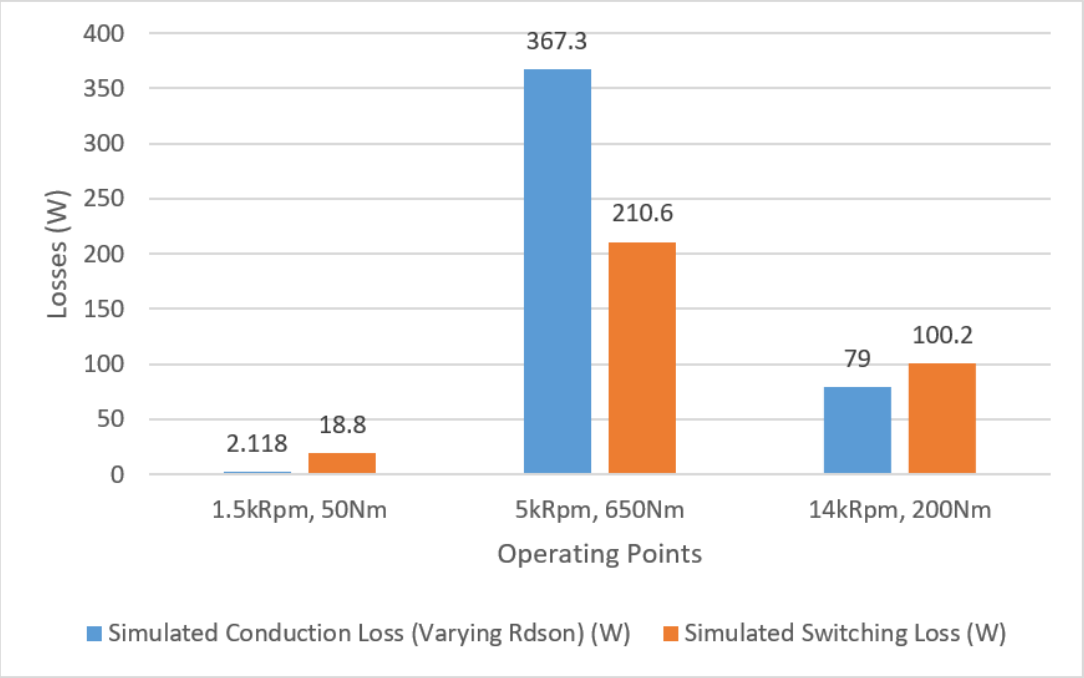


Figure 4.8: Electrical Losses vs Different Operating Points

4.3.2 Electrical losses vs switching frequency

The examination of the variation of electrical losses with switching frequency is shown below. The behaviour of the conduction losses with increasing switching frequency can be seen in Figure 4.9. A slight increase in conduction losses with switching frequency is observed at the 1.5 kRpm and 14 kRpm operating points while a more prominent increase is observed at the 5 kRpm operating point. Firstly, this change of conduction losses with respect to switching frequency is due to the temperature dependency of the on-state resistance of the MOSFET which changes during an iteration of the PLECS model. Secondly, at higher currents, the conduction losses are expected to increase in the switch, which increases the temperature and a thermal calculation loop is formed, hence a greater change is observed at the 5 kRpm operating point.

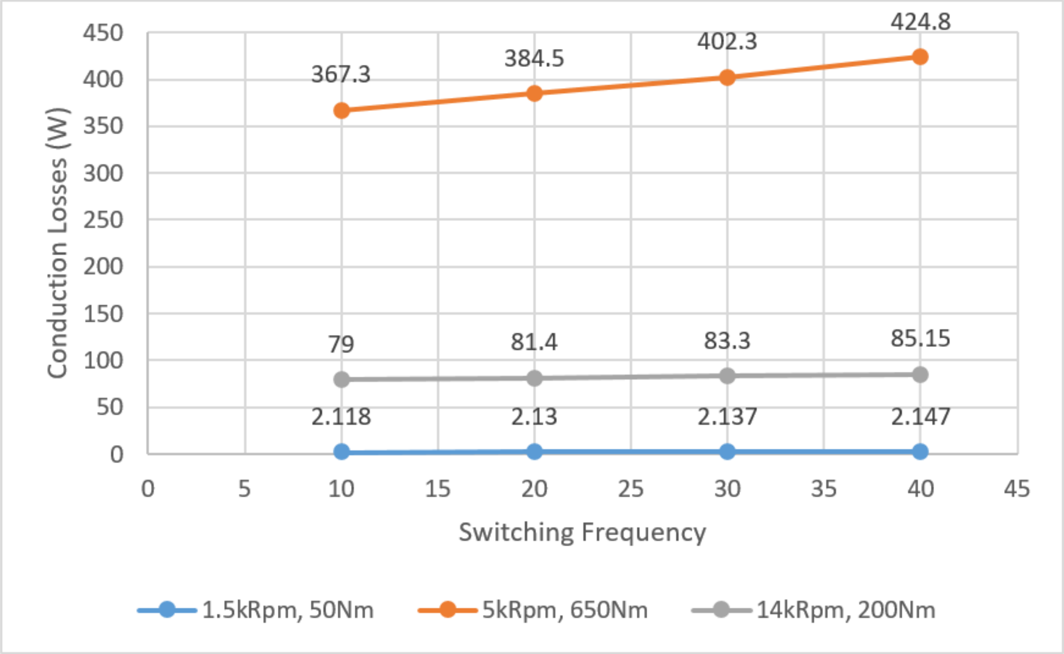


Figure 4.9: Conduction Losses vs Switching Frequency

The change in switching losses with switching frequency is highlighted in Figure 4.10. Switching losses are seen to increase linearly with increasing switching frequency in line with the theoretical background. This demonstrates the proper functioning of the model.

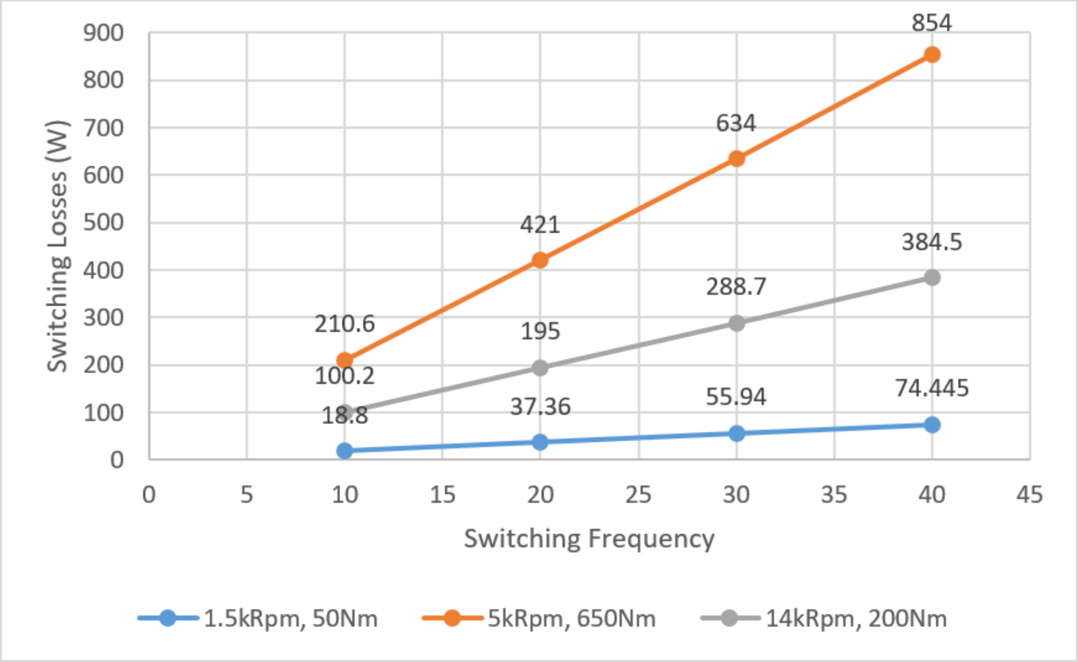


Figure 4.10: Switching Losses vs Switching Frequency

4.3.3 Electrical losses vs MOSFET Gate Resistances

Figures 4.11 and 4.12 assert the variation of the turn-on and turn-off gate resistances on the losses at an operating point of 5 kRpm and 650 Nm with a constant switching frequency of 10 kHz on the inverter.

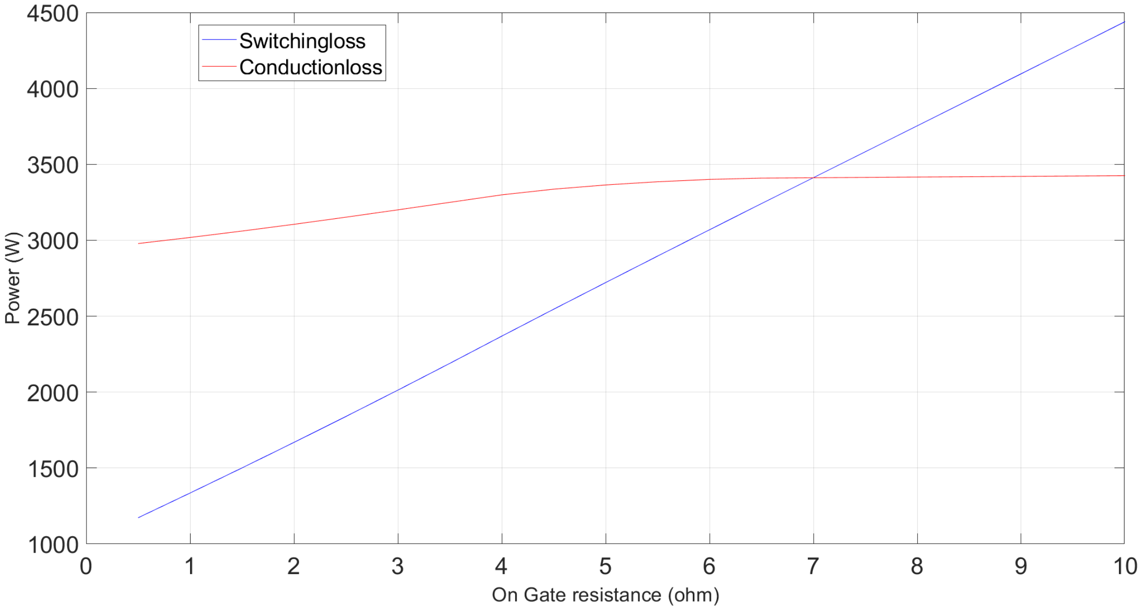


Figure 4.11: Power module losses vs Turn-On Gate Resistance

By keeping the turn off gate resistance constant at a recommended value of 1Ω and varying the turn-on resistance, it is observed in Figure 4.11 that the switching losses are increased with increasing turn-on gate resistance while the conduction losses change slightly. The change in the conduction losses is a result of the temperature dependence of the conduction losses. As the switching losses increase, the temperature of the system increases, which affects the value of the on-state resistance of the MOSFET used in the next loss iteration in PLECS.

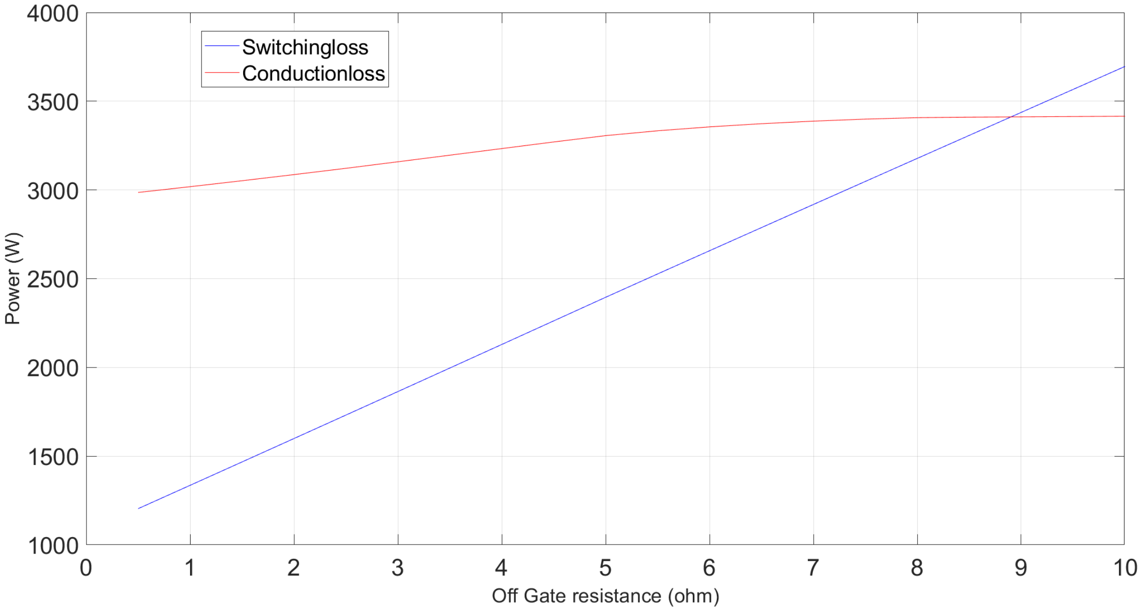


Figure 4.12: Power module losses vs Turn-Off Gate Resistance

Similarly, by keeping the turn-on gate resistance constant at 1Ω and varying the turn-off resistance, it is also observed in Figure 4.12 that the switching losses increase with increasing turn off resistance. However, it is quite interesting to note that for this particular MOSFET model, the turn-on gate resistance has a more significant impact on the switching losses than the turn-off gate resistance.

4.4 Complete Thermal Model Evaluation

This section illustrates the complete thermal model results and evaluation between different power modules used in this modelling. The parameters of the electric machine used to obtain the loss maps are shown in Table 3.1 and the test conditions used are shown in Table 4.9. To have a fair comparison between the two SiC power modules, same thermal impedance network shown in Figure 3.18 with a coolant flow rate of 10l/min has been used.

Table 4.9: Test conditions to obtain loss maps

Ambient temperature (°C)	80
Coolant flow rate (l/min)	10
CREE SiC datasheet gate resistance (Ω)	1
Semikron SiC datasheet gate resistance (Ω)	4.1
DYNEX IGBT datasheet gate resistance (Ω)	2.2
Switching frequency (kHz)	10

4.4.1 Cree SiC Power Module

The dependency of the CREE power module's losses with varied peak current at a fixed speed of 5000 Rpm is shown in Figure 4.13. It is observed that the maximum loss of 3.1 kW is obtained at 790 A peak current. Another interesting thing to note is that the switching losses vary linearly as a function of current whereas, the conduction losses increases as a polynomial function.

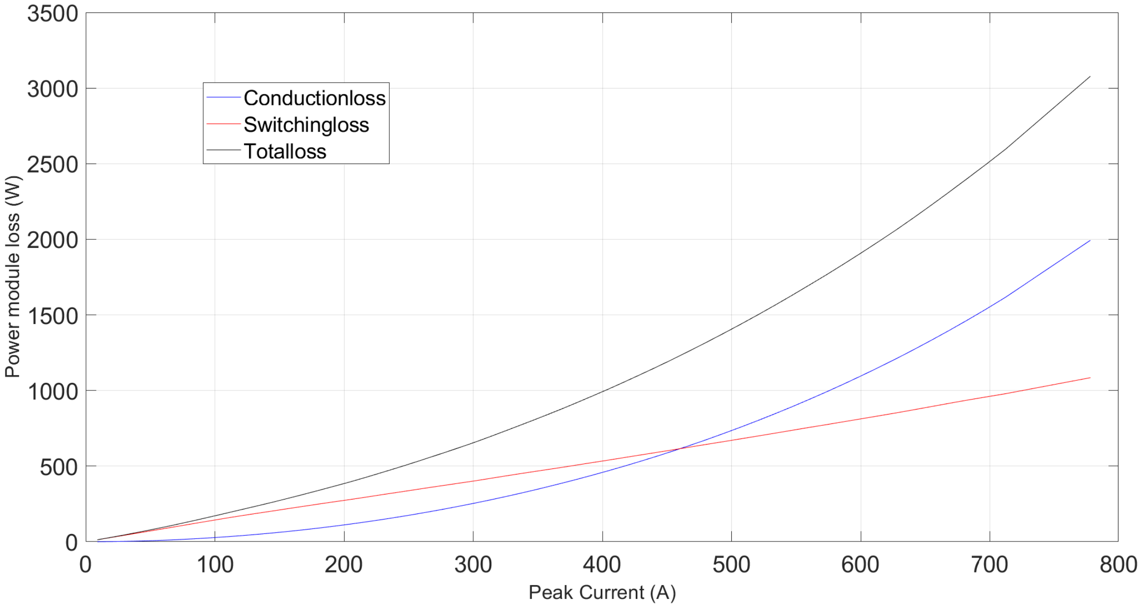


Figure 4.13: Cree Power module loss with 1Ω gate resistance Vs Current at 5000Rpm

Figure 4.14 shows the power module loss map of the electric machine operating in the motoring region. It is observed that the losses stay constant in the Maximum Torque Per Ampere (MTPA) region till 7000 Rpm,i.e. the base speed and once it enters the field weakening region, the losses reduce. A maximum loss of around 3 kW is seen at high operating torque condition.

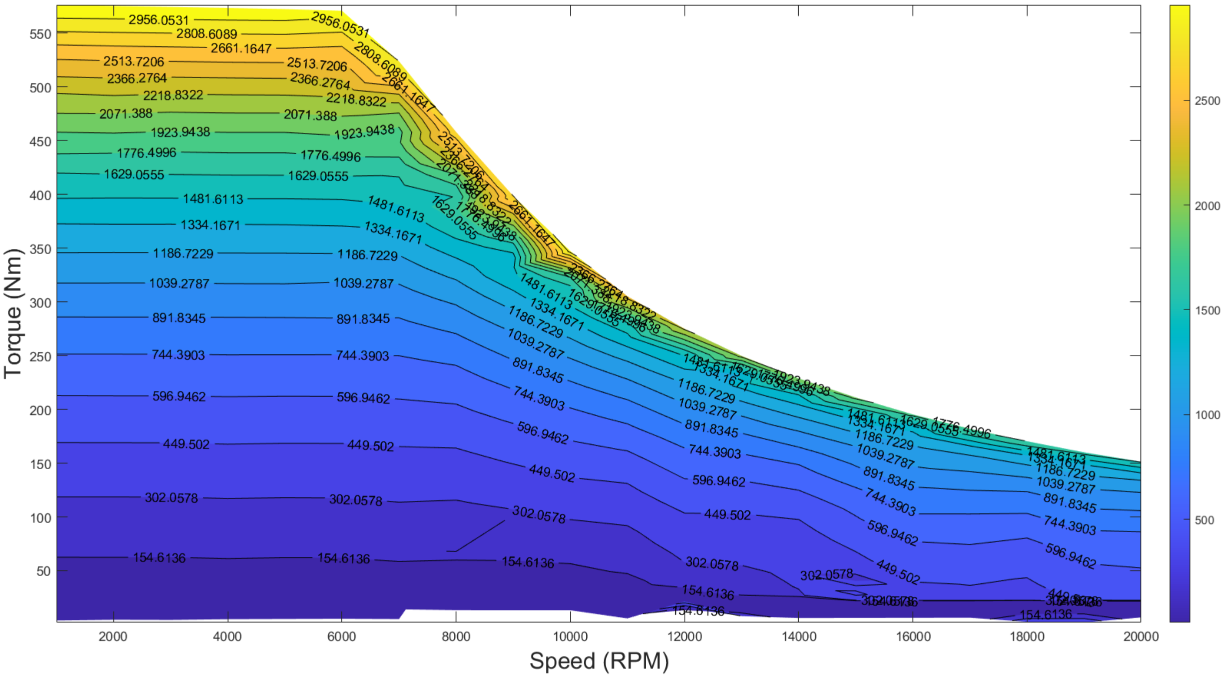


Figure 4.14: Cree Power module Loss Map

4.4.2 Semikron SiC Power Module

4.4.2.1 Case 1 - Using Switching energies from datasheet

The dependency of the Semikron power module's losses with varied peak current at a fixed speed of 5000 Rpm is shown in Figure 4.15. It is observed that the maximum loss of 4.6 kW is obtained at 790 A peak current. This power module's switching and conduction also have a similar pattern, likewise CREE, except for the magnitudes.

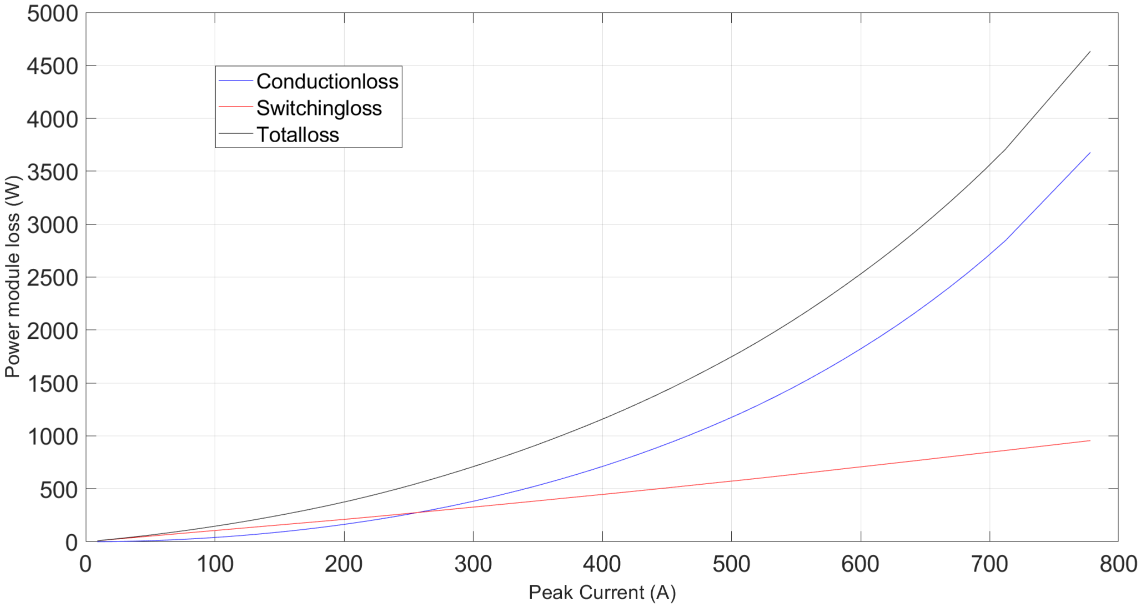


Figure 4.15: Semikron Power module loss with 4.1 Ω gate resistance Vs Current at 5000 Rpm

Figure 4.16 shows the power module loss map of the electric machine operating in the motoring region. It is observed that the losses stay constant in the Maximum Torque Per Ampere (MTPA) region till 7000 Rpm, i.e. the base speed and once it enters the field weakening region, the losses reduce. A maximum loss of around 4.5 kW is seen at high operating torque condition.

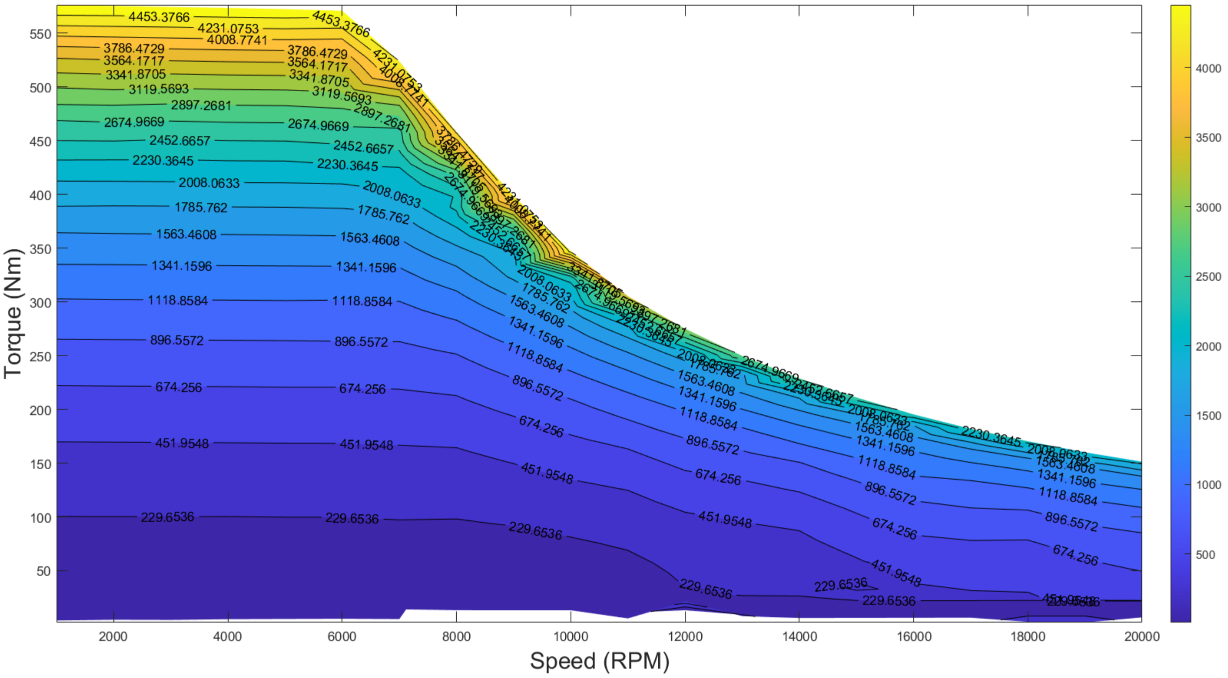


Figure 4.16: Semikron Power module Loss Map - Datasheet only configuration

4.4.2.2 Case 2 - Using Derived Switching Energies from SPICE model

The dependency of loss to the current for the Semikron power module is shown in Figure 4.17. It can be observed that the total losses increased to around 8% when compared with Figure 4.15 because of the more data points obtained for calculating switching energies through the spice double pulse testing.

Figure 4.18 shows the power module loss map of the electric machine operating in the motoring region. It is observed that the losses stay constant in the Maximum Torque Per Ampere (MTPA) region till 7000 Rpm, i.e. the base speed and once it enters the field weakening region, the losses reduce. A maximum loss of around 4.9 kW is seen at the high torque region.

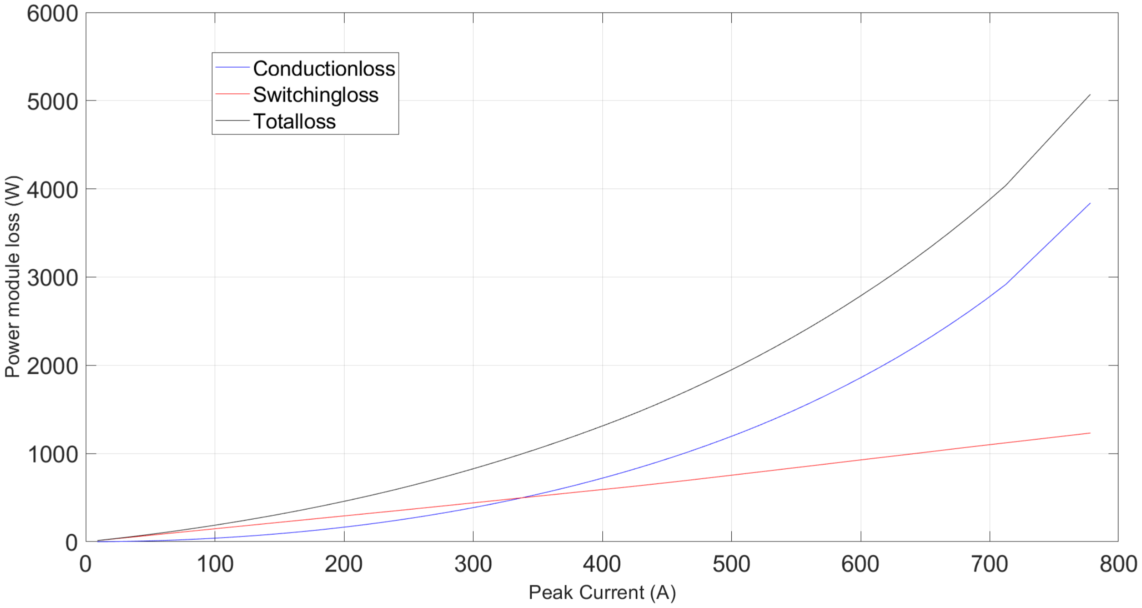


Figure 4.17: Semikron Power module loss with 4.1 Ω gate resistance Vs Current at 5000 Rpm using switching energies obtained through PSpice

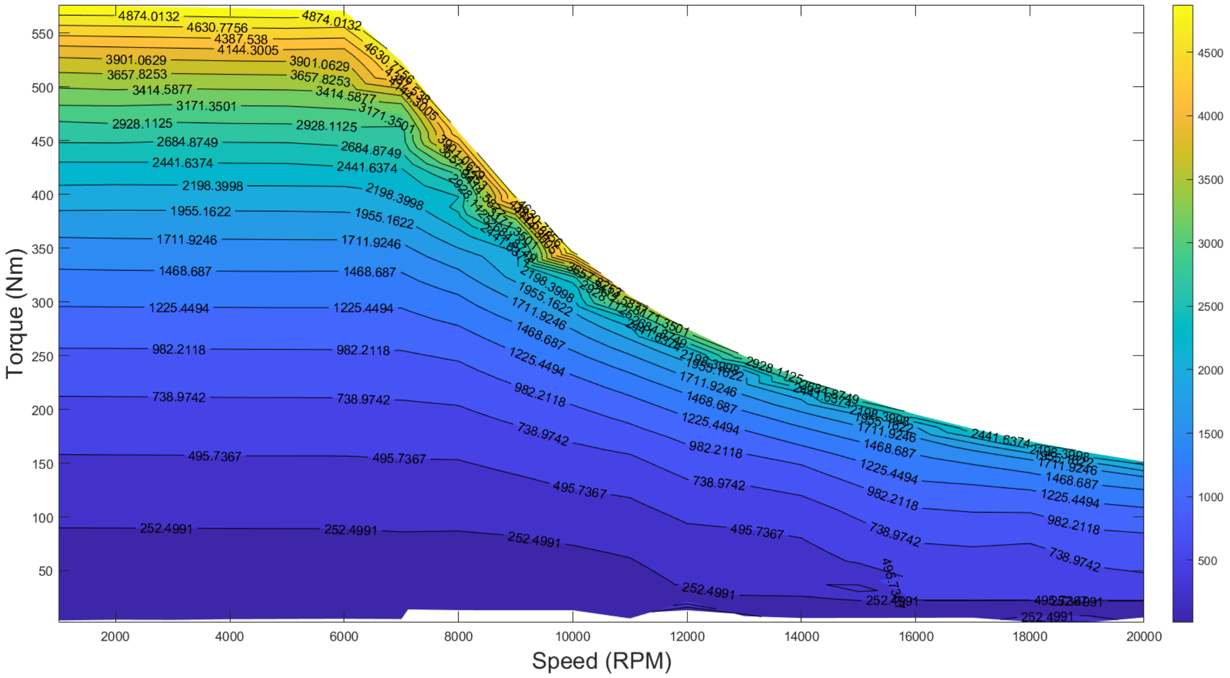


Figure 4.18: Semikron Power module Loss Map - with SPICE Configuration

4.4.3 DYNEX IGBT Power Module

The generated total loss map of the DYNEX IGBT switch is shown in Figure 4.20. At maximum power, around 10 kW of losses are detected, with the IGBT accounting for 77 % of the loss and the antiparallel diode accounting for the remainder.

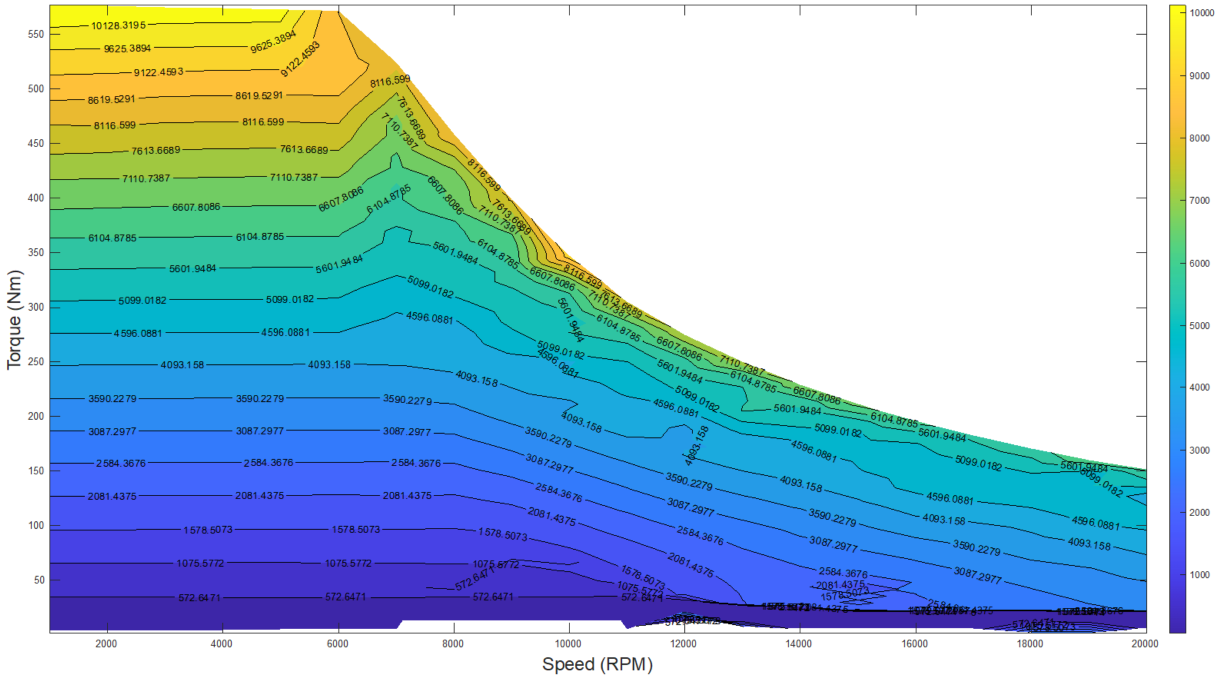


Figure 4.19: DYNEX IGBT Total Loss map

The dependency of the DYNEX power module's losses with varied peak current at a fixed speed of 5000 Rpm is shown in Figure 4.20. It is observed that the maximum loss of around 10.5 kW is obtained at 790 A peak current. Another intriguing fact is that IGBT losses account for 77% of the overall losses, with the diode accounting for the remainder.

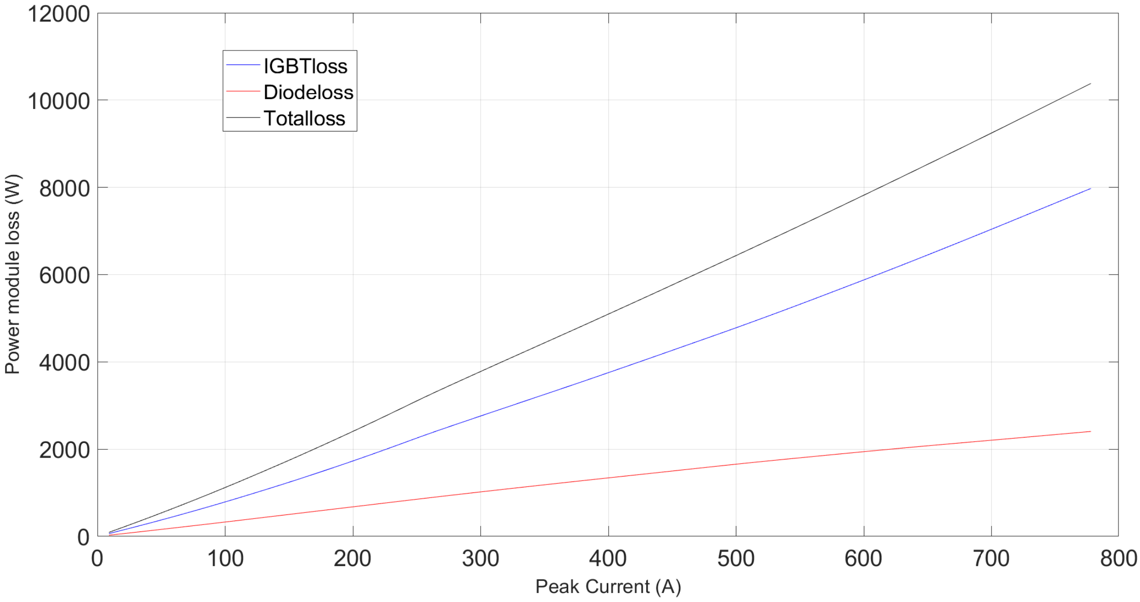


Figure 4.20: DYNEX Power module loss Vs Current at 5000 Rpm

4.4.4 Comparison of losses between two different SiC and a IGBT power module

Comparing the total loss, conduction loss, switching loss and junction temperatures of three different power modules at selected operating points with its own recommended gate resistance of 1 Ω(CREE), 4.1 Ω(Semikron) and 2.2 Ω(DYNEX) are shown in Figures 4.21, 4.22, 4.23 and in Table 4.10 respectively. It should be noted that the semikron results compared in this case are from case 1 highlighted above since case 2 came as an additional investigation towards the end of the project.

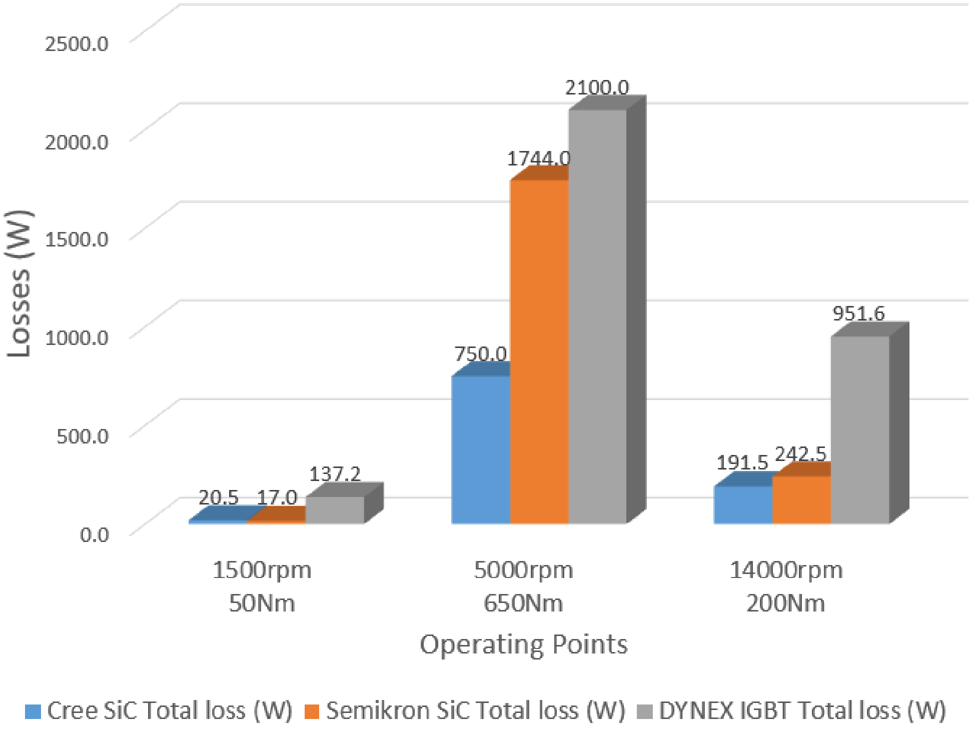


Figure 4.21: Cree, SemiKron and DYNEX IGBT total losses comparison

It is observed from Figures 4.22 and 4.23 that the CREE power module has a lower conduction losses compared to the other two power modules because of its lower on-state resistance, whereas the switching losses are a bit higher than the semikron power module because of its increased switching energies. It can also be seen that a maximum of 1548 W conduction loss is observed at 5000 Rpm operating point for the semikron power module because of its increased junction temperature which directly impacts the on-state resistance of the power module. Additionally, It is found that the switching losses are way more higher in dynex IGBT when compared with the SiC power modules.

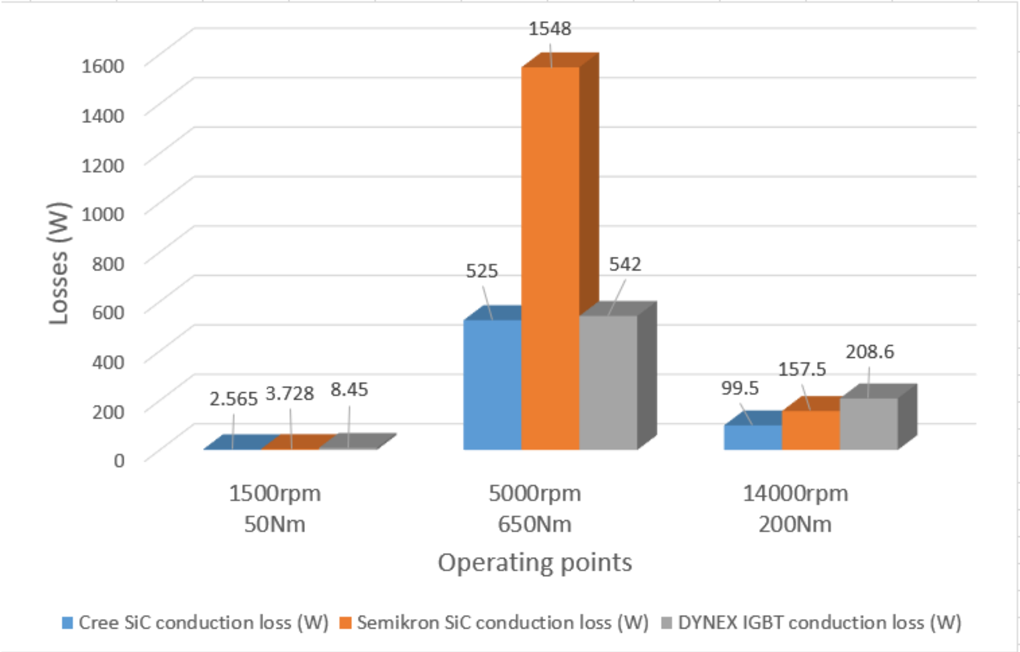


Figure 4.22: Cree SiC, SemiKron SiC and DYNEX IGBT conduction Losses Comparison

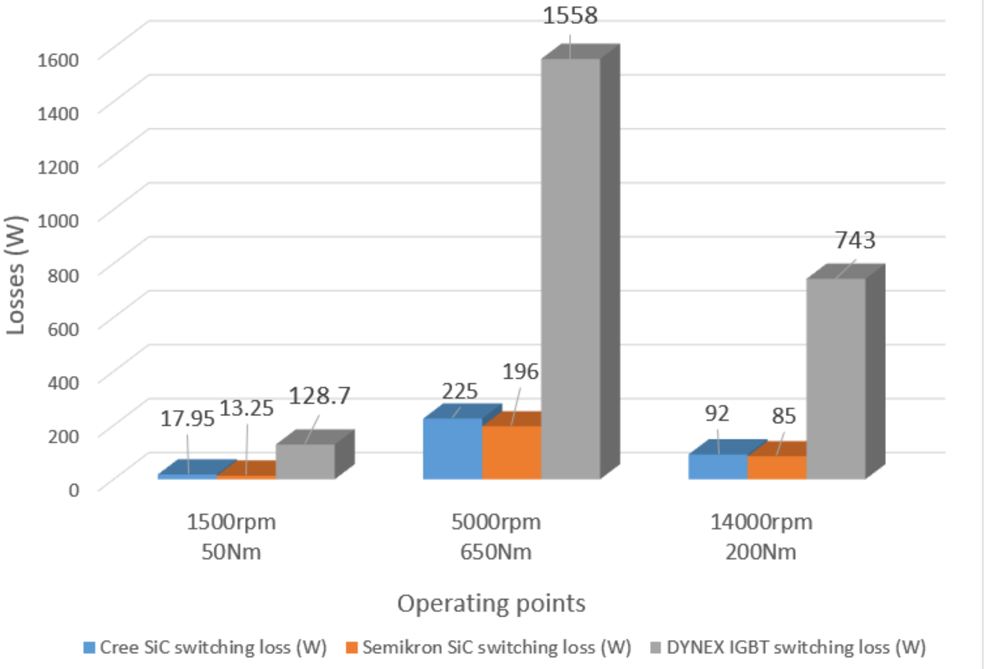


Figure 4.23: Cree SiC, SemiKron SiC and DYNEX IGBT Switching Losses comparison

The final steady state junction temperature of a single switch in the respective power modules at different operating conditions are shown in Table 4.10. A maximum temperature of 269.4°C, 152.3°C and 112.8°C are observed in Semikron, CREE and Dynex power module at 5000 Rpm, 650 Nm operating point respectively.

Table 4.10: Cree SiC, Semikron SiC and DYNEX IGBT Final Junction Temperature at Selected Operating points with recommended gate resistance

Operating Conditions	Cree SiC $T_j (°C)$	Semikron SiC $T_j (°C)$	DYNEX IGBT $T_j (°C)$
1500rpm, 50Nm	81.94	82	81.9
5000rpm, 650Nm	152.3	269.4	112.8
14000rpm, 200Nm	99.52	103.1	94.5

5

Discussion

As with engineering studies in general, it should be remarked that computer simulations and hardware prototype laboratory work complement each other. Simulation results should not be interchanged for prototype studies [6]. This chapter firstly addresses the perceived deficiencies of this project, then the sustainability aspects of this work, and finally, the ethical perspectives of this thesis are presented.

5.1 Shortcomings in Simulation work

The significant challenges in computer simulation are often: long simulation times, non-linearities of solid-state switches, inaccurate models and controller modelling [6]. Therefore, the authors carefully evaluated the simulation's objective before proceeding to avoid long simulation times and complicated outputs that could cloud phenomena of interest. Hence, this simulation work was simplified as much as possible to satisfy our immediate objectives. However, these simplifications could have some impact on the achieved results. These impacts are highlighted below.

5.1.1 Shortcomings from Delimitations

Power Module Losses: Since this study did not consider the effect of snubber circuits, the case set up for the power module losses eliminated the inductances of the cables, busbars and DC-link capacitor since these cause overvoltages across the switches which cannot be mitigated without snubbers. In reality, these over voltages are a major part of the losses of the power module and should not be neglected. Perhaps as a consideration for future work, snubber circuits may be designed with respect to the stray inductances in the power module and then the losses in the power module could be studied to achieve results closer to reality.

Power Module Loss Maps: In calculating the loss maps of each power module, it should be noted that the authors set the simulation time for each PLECS blockset iteration for one second. An implication of this is that the losses currently observed for the high torque (current) operating points could be higher in reality. This difference will result from the simulation not reaching its steady-state junction temperatures before the next operating point iteration for the high torques. This setup gave a total simulation time for entire operating points of about ten hours, which would have been a lot longer if the simulation time for each iteration was increased.

DC-link Capacitor Losses: It should be highlighted that the DC-link capacitor losses calculated in this project, neglected the temperature dependency of the ESR on its results. Actual temperature in reality will defer from results since its ESR is temperature dependent.

5.1.2 Shortcomings from Software

5.1.2.1 PLECS Vs Simscape

As mentioned previously, the authors also utilized the Simscape toolbox in MATLAB version 2020b in building a similar inverter model. Though Simscape presents its users with more precise modelling control options over one's model, it has a significant drawback regarding high power applications utilizing wide-bandgap devices such as this project. When carrying out these investigations, simscape did not have a MOSFET model that accounts for reverse conduction. When comparisons were made between waveforms from PLECS and Simscape, it was observed that for the same operating points and assuming a constant on-state resistance, the MOSFET in simscape conducts only during the positive half cycle of the load current, while its body diode conducts during the negative half-cycles. This is not the case with PLECS as the MOSFET model can conduct in both directions.

Additionally, this version of Simscape does not also allow for the assignment of lookup tables with negative current and voltage values as thermal description. Correspondence was made with the MATLAB team and these drawbacks may be corrected soon.

In summary, Simscape has an advantage over Plecs mainly due to its more realistic options in defining semiconductor switches and gate driver properties it gives to its users. It also has the facility to calculate switching, conduction and gate driver losses of the model directly using their current and voltage waveforms. It can be inferred that using simscape for this kind of modelling will require the creation and modelling of a MOSFET that has the SiC characteristics, perhaps a prospect for future work.

5.1.2.2 PLECS Vs PSPICE

Since the PLECS software uses instantaneous switching to simplify its simulation methods, it cannot be used to carry out an accurate component level simulation especially for nonlinear components as power semiconductors. Therefore OrCAD PSPICE was utilized for the double pulse testing of the Semikron switches. Additionally, PSPICE cannot be easily used to model control elements as it is created mainly for circuit design [31], thus emphasising the need to use PLECS and PSPICE simultaneously.

To summarize, PLECS provides a faster, relatively accurate and a simple method for modelling inverter system level properties, while PSPICE provides greater component level accuracy.

5.2 Sustainability Aspects

The EU commission has set high requirements for CO_2 emissions produced by vehicles and vans [32]. One possibility for automakers to achieve this goal is to go electric. However, the electricity required to power these cars must be supplied by the national grid, which imposes a high demand. If non-renewable energy sources are used to generate additional electricity, CO2 emissions will still rise. The use of renewable energy to produce additional electricity would be a wise choice to mitigate climatic change. In the best-case scenario, it is proved that electric cars in the EU produce 80 % less CO_2 than petrol or diesel cars and do not release dangerous chemicals such as NOx, SO_2, or lead, which is emitted by combustion engines [33]. Investigating and quantifying the losses in the power inverter of EVs, therefore aid in studying and improving efficiency, which reduces the input power to EVs, lower the consumption of electrical devices and reduce the adverse impact on the environment. In this way, the use of electric vehicles alongside green energy production and recycling of batteries will help to achieve the goal set by the EU commission.

5.3 Ethical aspects

When conducting any project, it is one's responsibility to consider the ethical implications of the actions or products related to the activities. There are some technologies, such as weaponry production or monitoring systems, where ethical dilemmas are straightforward to imagine within the engineering field. However, while some moral problems may be easy to spot, others could be more inconspicuous. With this in mind, the authors utilized the Institute of Electrical and Electronics Engineers (IEEE)' Code of Ethics [34] during this project to avoid potential ethical misconduct. Highlighted below are the perceived ethical risks during this work, alongside discussions on how the authors mitigated them.

Considering the third point of the IEEE code of ethics which states, *"to avoid real or perceived conflicts of interest whenever possible, and to disclose them to affected parties when they do exist;"*, there is often a risk of conflicts of interest whenever projects like these are carried out since the engineering space is quite small. For example former ties with a software company could feed some bias in carrying out one's study. Only the positive aspects of the software may then be highlighted which contradicts this third ethics code. To avoid situations like these, conflicts of interest cases should be disclosed and studies should be made on presented facts eliminating biases.

Concerning the fifth point in the code which says, *"to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, to be honest and realistic in stating claims or estimates based on available data, and to credit properly* *the contributions of others;"* Since this work is simulation based, there is a risk of data manipulation to suit needed results. This is avoided by making due consultations and seeking salient inputs to the project, highlighting the delimitations of the project and listing all possible differences in results when considering these delimitations.

Regarding the seventh point in the IEEE code which states, *"to treat all persons fairly and with respect, and to not engage in discrimination based on characteristics such as race, religion, gender, disability, age, national origin, sexual orientation, gender identity, or gender expression;"*

As with diverse groups, there is often a risk of some members feeling unimportant due to perceived or actual discrimination. This is avoided by openness and clear communication during meetings. For instance, there is always a tendency to regard the suggestions of a team member with higher qualifications than another with less. In such cases reasons for discarding anyone's suggestions must be stated clearly and simply so that no form of discrimination is perceived. Speaking up is often encouraged in situations where team members feel disenfranchised. Utilizing these methods, the seventh point of the IEEE code is upheld.

6

Conclusions

In this thesis work, the losses and ripple in an 800 V, 350 kW traction inverter were quantified with a specific focus on the dc-link capacitor and transistors for various selections of switching frequencies and gate resistances at selected operating points. Analytical models for electrical losses and ripple were also created and compared with simulated values.

The ripple current and voltage analysis showed a maximum current and voltage ripple of about 370 Arms and 47 V peak to peak, respectively, at the highest torque request of 650 Nm. Also, comparing the simulated and analytical ripple equations revealed a 17% and 6% discrepancy for the voltage and current ripple, respectively, at the high torque operating point. The outcome of comparing the properties of different dc-link capacitor brands presented a maximum voltage ripple attenuation from the brand with the highest capacitance. In contrast, the current ripple remained roughly alike in all brands - which agrees with the background theory.

The losses in the default dc-link capacitor at the highest torque operating point was observed to be about 17 W and gave rise to a maximum hot spot temperature of 93°C, which was below its maximum allowable limit of 105°C. Hence, this dc-link capacitor can be comfortably used for this operation.

This work further compared the electrical and analytical losses of a power module manufacturer - CREE. While assuming a fixed on-state resistance, a 0.3% discrepancy was observed in its conduction losses; however, this difference increased to a maximum of 17% at high operating torque when considering the on-state resistance temperature dependence. On the other hand, its switching loss revealed a maximum of 7% discrepancy with its analytical equations at the lowest operating torque. This thesis also inferred that the turn-on gate resistances significantly impact the switching losses than the turn-off gate resistances for this power module.

A complete thermal model of the inverter was further modelled and simulated. Analysis carried out on another power module manufacturer - Semikron - showed an 8% increase in power dissipation when switching energies were derived manually from its SPICE model compared to when switching energies were only derived from its datasheet.

Comparing the two SiC power module brands showed that CREE had lower conduction losses when utilizing their recommended gate resistances than Semikron but slightly higher switching losses at the high operating torques. In total, a maximum power dissipation of 3.1 kW was noted for the CREE power module, while 4.9 kW was observed for Semikron. A maximum junction temperature of 152°C and 270°C was also noticed for CREE and Semikron power modules respectively. Additionally, the DYNEX IGBT power module displayed a maximal power loss of 10 kW and maximum junction temperature of 112°C. This lower junction temperature of the IGBT power module is because of its stronger thermal network i.e, lower thermal impedance values. This shows that using a SiC module rather the IGBT module improves the losses by 50% with Semikron and 70% with the CREE power module.

These results show that using similar thermal characteristics and recommended gate resistances, the CREE module should be preferred in this application due to its lower power dissipation. But in reality, each power module has its own optimised thermal network which when used may produce different results. It should also be noted that while the electrical and thermal losses are some factors that can determine the selection of the power modules, other factors such as mechanical properties, cost, performance at standard driving cycles and during short circuit conditions should also be considered to make a holistic decision.

6.1 Future work

There are several interesting studies that could be extended from this work.

- In the near future whenever there is an update to the current Matlab- simscape toolbox, it will be interesting to compare the results from PLECS and those from Simscape. Comparing results in terms of discrepancies and speed of resolution could be an extension from this work.
- Another software, such as Simscape could also be used to quantify the other losses not covered in this work such as the gate driver losses, snubber losses and other parasitic losses, and the influence of these losses on the total losses could be investigated.
- The influence of the modulation techniques on the losses and ripple can also be studied.
- A more precise component level simulation and modelling could be done on the dc-link capacitor to assess the influence on the ripple currents at the different operating points of the inverter while considering the temperature dependence of its properties. In addition, different capacitor types could be studied alongside the harmonic spectrum of the current ripple to better quantify the dc-link capacitor losses.

Bibliography

[1] United Nations, "Policy Brief 16: Interlinkages Between Energy And Transport," no. July, pp. 1–6, 2018. [Online]. Available: `https://sustainabledevelopment.un.org/content/documents/17480PB8.pdf`.

[2] M. Salcone and J. Bond, "Selecting film bus link capacitors for high performance inverter applications," *2009 IEEE International Electric Machines and Drives Conference, IEMDC '09*, pp. 1692–1699, 2009. DOI: `10.1109/IEMDC.2009.5075431`.

[3] A. Holm, "SiC Converter for Electrical Vehicle – DC-Link Ripple," p. 1, 2017.

[4] A. Bergqvist, A. Henriksson, J. Lektenius, J. Simonsson, P. Jacobsson, P. Ankarson, and S. S. Nursebo, "Ripple and Electromagnetic Fields in Electric Vehicles," 2018.

[5] *Wolfspeed SiC MOSFET*. [Online]. Available: `https://www.wolfspeed.com/knowledge-center/article/basics-of-sic-series-comparing-sic-mosfets-to-si-mosfets`.

[6] N. Mohan, T. Underland, and W. Robbins, *Power electronics converters, applications and design*, 1. John Wiley and Sons INC, 1997, vol. 28, pp. 105–106. DOI: `10.1016/s0026-2692(97)87859-7`.

[7] *Electrical4u MOSFET characteristics*. [Online]. Available: `https://www.electrical4u.com/mosfet-characteristics/`.

[8] L. H. Opsahl, "Design and Testing of Voltage Source Inverter and Motor Control System for Electric Vehicle," no. July, 2015.

[9] A. Huges and W. Drury, *Electric Motors and Drives fundamentals*, 7-8. Elsevier Ltd, 1985, vol. 225.

[10] *tntech SPWM*. [Online]. Available: `https://www.tntech.edu/engineering/pdf/cesr/ojo/asuri/Chapter2.pdf`.

[11] Y. He, "A comparison of modulation techniques and motor performance evaluation Department of Electrical Engineering," *Master Thesis*, 2018.

[12] H. Khan, "Optimised space vector modulation for variable speed drives," *Revue Teledetection*, vol. 8, no. 1, pp. 17–34, 2009.

[13] M. Giesselmann, H. Salehfar, H. Toliyat, and T. Ur Rahman, "Modulation Strategies," no. 408, 2001. DOI: `10.1201/9781420037067.ch7`.

[14] K. Zhou and D. Wang, "Relationship Between Space-Vector Modulation," vol. 49, no. 1, pp. 186–196, 2002.

[15] B. Tolunay, "Space Vector Pulse Width Modulation for Three-Level Converters - a LabVIEW Implementation," Ph.D. dissertation, Uppsala Universitet, Mar. 2012, pp. 29–40. DOI: `10.1109/TLA.2013.6533965`. [Online]. Available: `http://ieeexplore.ieee.org/document/6533965/`.

[16] Y. Yang, K. Ma, H. Wang, and F. Blaabjerg, “Instantaneous thermal modeling of the DC-link capacitor in PhotoVoltaic systems,” *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2015-May, no. May, pp. 2733–2739, 2015. DOI: `10.1109/APEC.2015.7104737`.

[17] M. Vujacic, M. Hammami, M. Srndovic, and G. Grandi, “Analysis of dc-link voltage switching ripple in three-phase PWM inverters,” *Energies*, vol. 11, no. 2, 2018. DOI: `10.3390/en11020471`.

[18] M. Vujacic, M. Hammami, M. Srndovic, and G. Grandi, “Evaluation of DC voltage ripple in three-phase PWM voltage source inverters,” *IEEE International Symposium on Industrial Electronics*, pp. 711–716, 2017. DOI: `10.1109/ISIE.2017.8001333`.

[19] J. Zhang, “Modeling of DC Link Capacitor Current Ripple for Electric Vehicle Traction Converter,” 2013.

[20] J. Guo, J. Ye, and A. Emadi, “DC-Link Current and Voltage Ripple Analysis Considering Antiparallel Diode Reverse Recovery in Voltage Source Inverters,” *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5171–5180, 2018. DOI: `10.1109/TPEL.2017.2738327`.

[21] B. Alikhanzadehalamdari, “Comparison of High-Power DC-DC Con- verters for Solar Applications with Re- spect to Efficiency and Chip-area,” 2018.

[22] A. Wintrich, *Theory of loss and temperature calculation 1.1*, 2009.

[23] AVX, *AVX Capacitor Technical Summary and Application Guidelines.* [Online]. Available: `https://www.avx.com/docs/techinfo/TechSumAppGuide.pdf`.

[24] Q. Wang, “Investigation and Implementation of MOS- FETs Losses Equations in a Three-phase Inverter,” 2015.

[25] M. März and P. Nance, “Thermal Modeling of Power Electronic Systems,” *Infineon Technologies AG Munich*, no. December, pp. 1–20, 2000. [Online]. Available: `http://www.ocsimize.com/download/download_doc/thermique/thermal_management_power_electronics.pdf`.

[26] I. M. Aljanabi, “Experimental evaluation and model- ing of the thermal behavior of a TO- 247 Mosfet,” 2013.

[27] M. Shahjalal, “Electric-thermal modelling of power electronics components,” *PQDT - UK & Ireland*, no. April, 2018. [Online]. Available: `https://proxying.lib.ncsu.edu/index.php/login?url=https://search.proquest.com/docview/2307442090?accountid=12725%0Ahttp://js8lb8ft5y.search.serialssolutions.com/directLink?&atitle=Electric-thermal+modelling+of+power+electronics+components&author=Shahjalal`.

[28] U. Nicolai, “Determining Switching Losses of SEMIKRON IGBT Modules (Application Note AN1403),” *Application Note*, pp. 1–15, 2014.

[29] D. Levett, Z. Zheng, and T. Frank, “Double Pulse Testing: The How, What and Why,” no. April, 2020. [Online]. Available: `www.bodospower.com`.

[30] U. M. Version, *PLECS MANUAL*. PLECS.

[31] P. Johansson and B. Andersson, “Comparison of Simulation Programs for Supercapacitor Modelling,” *Electrical Engineering*, p. 131, 2008.

[32] T. Union, O. Journal, and E. Union, “REGULATION (EU) 2019/631 OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL,” vol. 10, no. December 2016, pp. 1–21, 2017.

[33] Transport & Environment, “How clean are electric cars?,” pp. 1–33, 2020. [Online]. Available: `https://www.transportenvironment.org/sites/te/files/downloads/T%26E%E2%80%99s%20EV%20life%20cycle%20analysis%20LCA.pdf`.

[34] IEEE, *IEEE Code of Ethics*, 2020. [Online]. Available: `https://www.ieee.org/about/corporate/governance/p7-8.html`.

A

Appendix 1 - PLECS standalone models

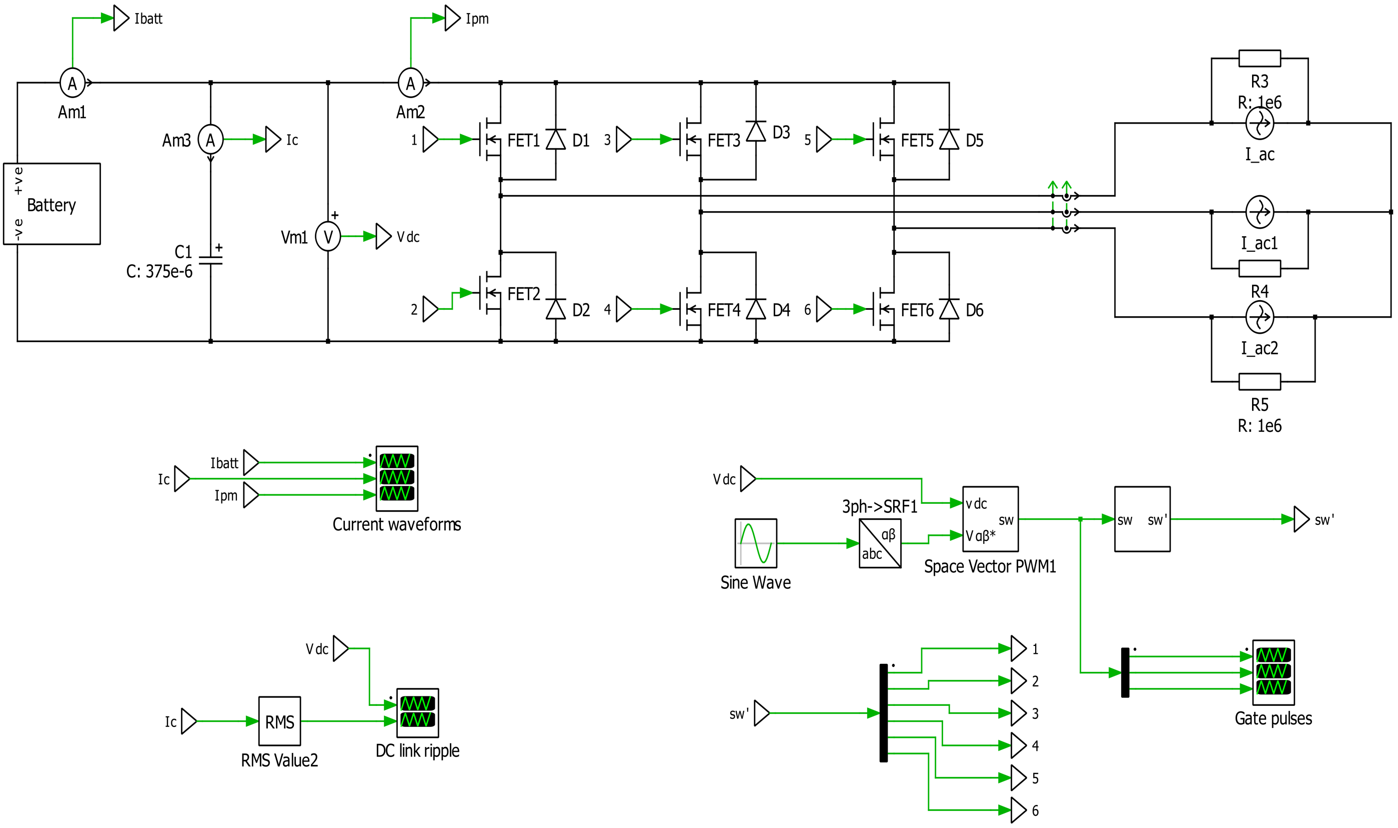


Figure A.1: PLECS setup for determining DC link voltage and current ripple without cable and busbar model.

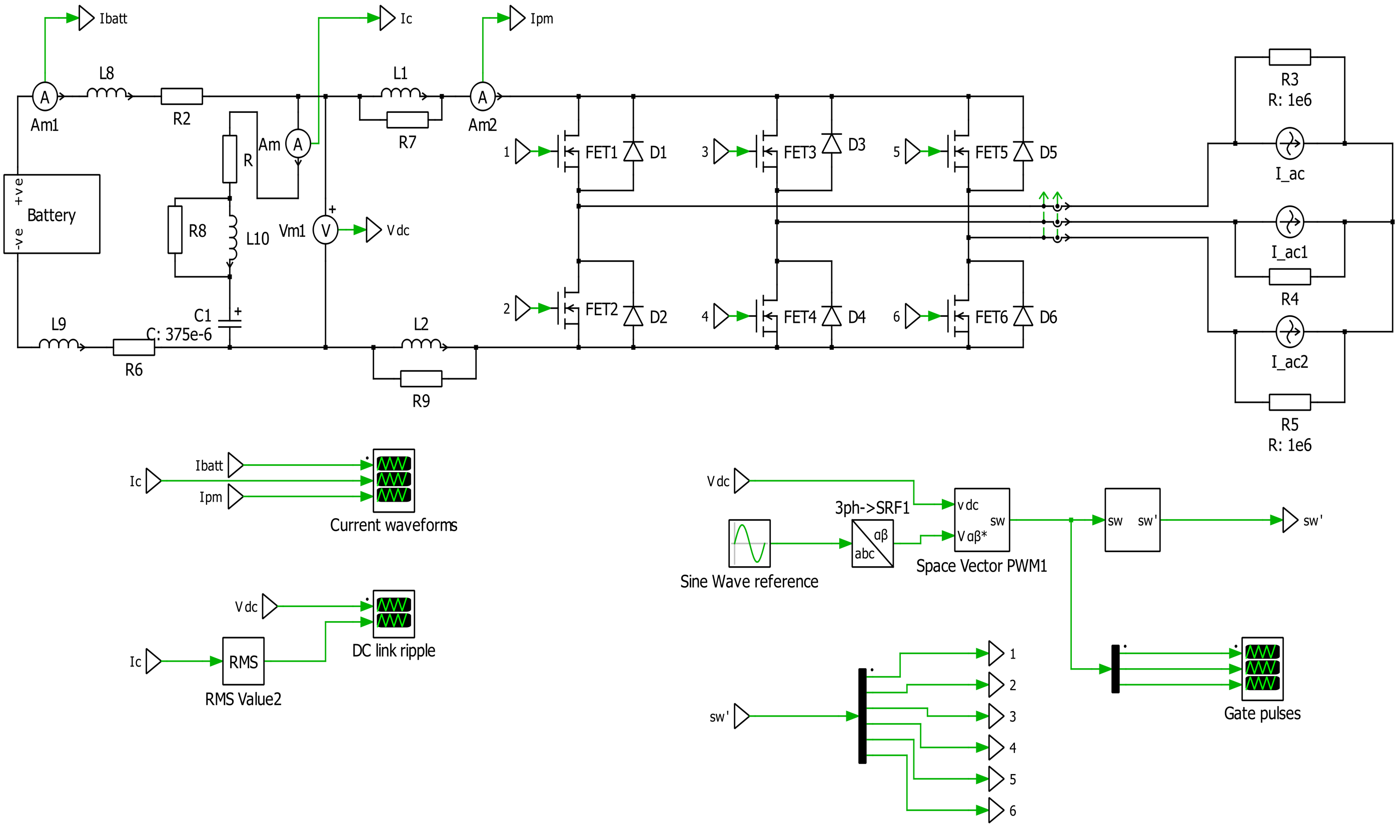


Figure A.2: PLECS setup for determining DC link voltage and current ripple with cable and busbar model.

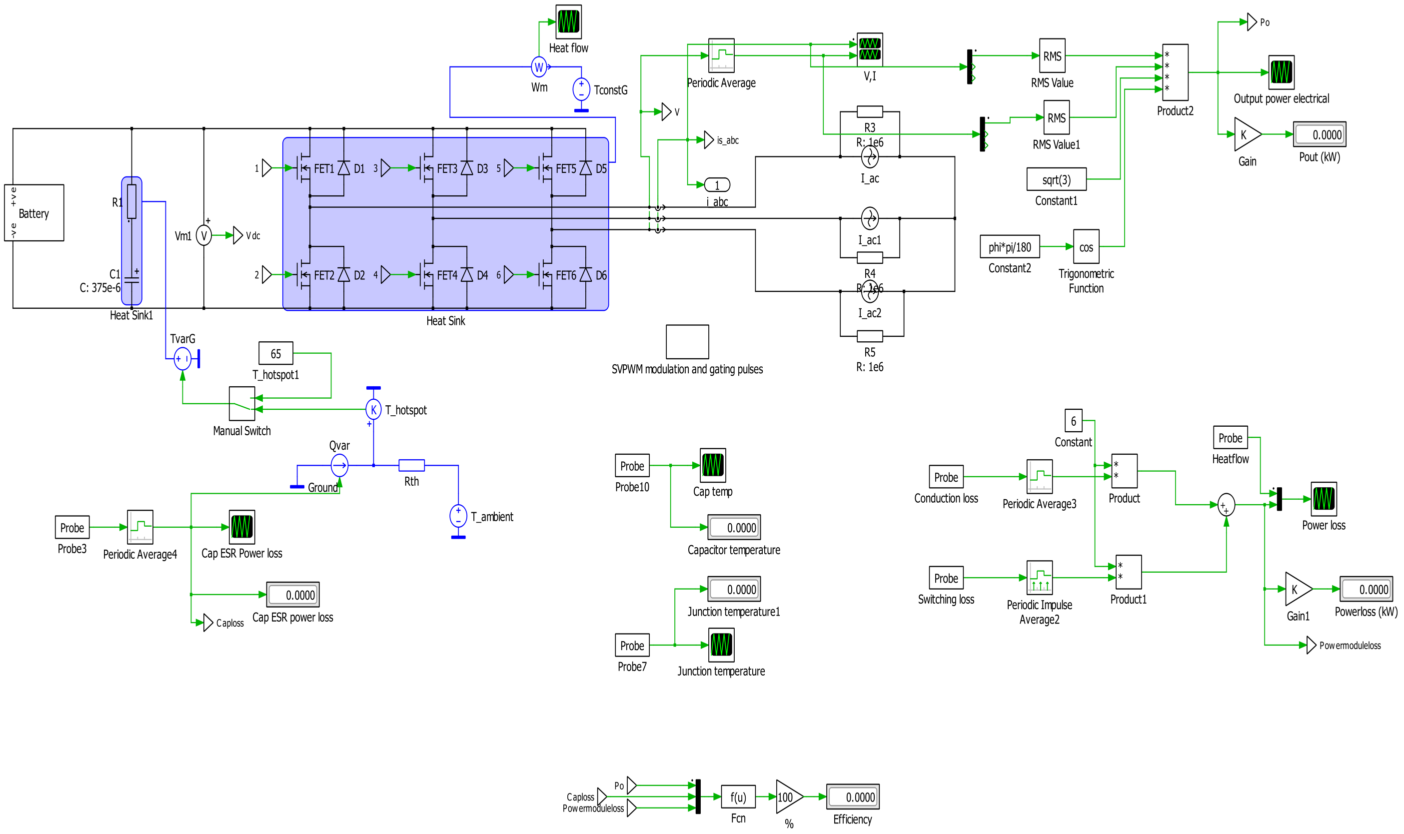


Figure A.3: Complete PLECS thermal losses setup.

B

Appendix 2 - MATLAB scripts

B.1 Ripple in sector 1

MATLAB script to determine the ripple of the DC link capacitor when the Voltage and current vectors lie in sector 1 of the SVPWM plane.

```
clc;
clear;

C = 375e-6;                      % DC link capacitance(F)
fsw = 10e3;                      % Switching frequency(Hz)
Tsw = 1/fsw;                     % Switching period(s)
Vdc =820;                        % DC voltage(V)
I0=52.745*sqrt(2);               % Output peak phase current(A)
V0=54.324;                       % Output rms phase voltage(V)
m = (V0*sqrt(2)/Vdc);            % Modulation index

% Voltage ripple
theta =(0*pi/180:5*pi/180:60*pi/180);% Voltage angle(radians)
phi = (9.2495*pi/180);                 % Powerfactor angle (rad)
a= 60*pi/180;
vppa = 0.75*I0*Tsw * m*cos(phi).*((1-(sqrt(3)*m*sin(a+theta))))/(C);
vppb = 0.75*I0*Tsw*m*abs((((cos(phi).*(1-(sqrt(3)*m*sin(a+theta)))+((4/sqrt(3))*sin(a-theta).*(1.5*m*cos(phi)-cos(theta-phi)))))/(C));
vpp = max(vppa,vppb);

%Current ripple
t1= (m*sqrt(3)*Tsw*sin(a-theta))/2;
t2= (m*sqrt(3)*Tsw*(sin(theta)))/2;
sa= (t1+t2);
sb= (t2-t1);
sc= (-t1-t2);
i1= I0*cos(theta-phi);
```

```
i2= I0*cos(theta-phi-120);
i3= I0*cos(theta-phi-240);
Ip= ((sa.*i1)+(sb.*i2)+(sc.*i3))-(1.5*m*I0*cos(phi));

ma= 2*m;
Icrms= I0* sqrt((sqrt(3)*ma/(4*pi))+(cos(phi)^2*((sqrt(3)*ma/(pi))-(9*(ma^2))/16)));
```

B.2 Ripple in sector 2

MATLAB script to determine the ripple of the DC link capacitor when the Voltage and current vectors lie in sector 2 of the SVPWM plane.

```
clc;
clear;

C = 375e-6;                      % DC link capacitance(F)
fsw = 10e3;                      % Switching frequency(Hz)
Tsw = 1/fsw;                     % Switching period(s)
Vdc = 800;                       % DC link voltage(V)
I0=318.29*sqrt(2);               % Output peak phase current(A)
V0=323.84;                       % Output rms phase voltage(V)
m = (V0*sqrt(2)/Vdc);            % Modulation index

% Voltage ripple
theta =(60*pi/180:5*pi/180:120*pi/180); %Voltage angle(rad)
phi = (6.8693*pi/180);                  % Powerfactor angle(rad)
a= 120*pi/180;
vppa = 0.75*I0*Tsw * m*cos(phi).*((1-(sqrt(3)*m*sin(theta))))/(C);
vppb = 0.75*I0*Tsw*m*abs(((cos(phi).*(1-(sqrt(3)*m*sin(theta)))+((4/sqrt(3))*sin(theta-(a/2)).*(1.5*m*cos(phi)-cos(theta-phi-a)))))/(C));
vpp = max(vppa,vppb);

% Current ripple
t1= (m*sqrt(3)*Tsw*sin((a)-theta))/2;
t2= (m*sqrt(3)*Tsw*(sin(theta-(a/2))))/2;
sa= (-t1+t2);
sb= (t2+t1);
sc= (-t1-t2);
i1= I0*cos(theta-phi);
i2= I0*cos(theta-phi-120);
i3= I0*cos(theta-phi-240);
```

```
Ip= ((sa.*i1)+(sb.*i2)+(sc.*i3))-(1.5*m*I0*cos(phi));

ma= 2*m;
Icrms= I0* sqrt((sqrt(3)*ma/(4*pi))+(cos(phi)^2*((sqrt(3)*ma/(pi))-(9*(ma^2))/16)));
```

B.3 Theoretical Power module loss calculation

```
% Inverter Powermodule Loss Calculation based on theoretical equations
clear
close all
clc
%% Input Parameters

% Static characteristics:
VT_MOS  =  0;
VT_D  =     5.6;
Rf_MOS  =  1.45e-3;
Rf_D  =     0.004;
p  =  4;                 % Pole pair number
Vdc  =  800;             % DC link voltage

% Generation of waveforms using modulation index(ma)
Irms  =  318.29;              % Output rms phase current(A)
ma  = 0.57247365*2/1.15;   % Modulation index
Urms_phase  =  Vdc/2*ma/sqrt(2); % assuming no addition of zero sequence
fi  =  6.8693*pi/180;     % Powerfactor angle(rad)
elfreq  =  933.33;        % Fundamental frequency(Hz)


% parameters for Switching loss calculation
Vref  =  800;          % Test conditions from the datasheet
Iref  =  700;
% Scaling factor
KiMOS  =  1.05;
KvMOS  =  1;
% Corresponding Switching energies from the test condition
Esw_MOS_on  = 27.953e-3;
Esw_MOS_off  = 22.774e-3;

%% Creation of vectors
fsw  =  10e3;
Tsw  =  1/fsw;
```

```matlab
Tstop  =  1/elfreq*2;
Tstep  =  1000e-11;
time   =  (Tstep:Tstep:Tstop);

% Creation of u1, u2, u3, i1, i2 and i3:
u1_sin  =  sqrt(2)*Urms_phase*sin(time*elfreq*2*pi);
u2_sin  =  sqrt(2)*Urms_phase*sin(time*elfreq*2*pi - 2*pi/3);
u3_sin  =  sqrt(2)*Urms_phase*sin(time*elfreq*2*pi + 2*pi/3);

i1  = round(sqrt(2)*Irms*sin(time*elfreq*2*pi-fi),2);
i2  =  round(sqrt(2)*Irms*sin(time*elfreq*2*pi-fi-2*pi/3),2);
i3  =  round(sqrt(2)*Irms*sin(time*elfreq*2*pi-fi-4*pi/3),2);

% Space Vector Modulation
u_min  =  min([u1_sin; u2_sin; u3_sin]);
u_max  =  max([u1_sin; u2_sin; u3_sin]);
u_svm  =  0.5.*(u_min + u_max);
u1_svm  =  (2/sqrt(3))*(u1_sin - u_svm);
u2_svm  =  (2/sqrt(3))*(u2_sin - u_svm);
u3_svm  =  (2/sqrt(3))*(u3_sin - u_svm);

% Third Harmonic Injection
u1_3rd  =  u1_sin + (1/6)*sqrt(2)*Urms_phase*sin(3*time*elfreq*2*pi);
u2_3rd  =  u2_sin + (1/6)*sqrt(2)*Urms_phase*sin(3*time*elfreq*2*pi);
u3_3rd  =  u3_sin + (1/6)*sqrt(2)*Urms_phase*sin(3*time*elfreq*2*pi);

% Select which curveform to use
u1  =  u1_svm;
u2  =  u2_svm;
u3  =  u3_svm;

% u1  =  u1_sin;
% u2  =  u2_sin;
% u3  =  u3_sin;

% Plotting of the phase voltage, phase current and Trianglewave:
figure
plot(time, u1, 'r'), hold on;
```

```
plot(time, u2, 'g')
plot(time, u3, 'b')
plot(time, u1_svm, 'r--')
plot(time, u2_svm, 'g--')
plot(time, u3_svm, 'b--')
plot(time, u1_3rd, 'r-.')
plot(time, u2_3rd, 'g-.')
plot(time, u3_3rd, 'b-.')
xlabel('Time(ms)')
ylabel('Voltage(V)')
legend('U1', 'U2', 'U3')
title('Reference Voltages (Sin, SVM and 3rd Harm)')

% Creation of a triangle wave:
t_onehalfswitchingperiod = Tsw/Tstep/2;
OnePiece = Vdc/2 - Vdc*time(1:t_onehalfswitchingperiod)/(Tsw/2);
OneTriangleperiod = [OnePiece, -OnePiece];

NumberOfTrianglePeriods = ceil(Tstop/Tsw)

TriangleWave_unadapted = [];
TriangleWave = [];

for j = 1:NumberOfTrianglePeriods
    TriangleWave_unadapted = [TriangleWave_unadapted, OneTriangleperiod];
end

TriangleWave = TriangleWave_unadapted(1:length(time));

% Plotting of the phase voltage, phase current and Trianglewave:
figure
subplot(3, 1, 1)
plot(time, u1, 'b')
xlabel('Time(ms)')
ylabel('Voltage(V)')
legend('Phase voltage')
title('Phase voltage, phase current and trianglewave')
subplot(3, 1, 2)
plot(time, i1, 'g')
ylabel('Current(A)')
legend('Phase current')
subplot(3, 1, 3)
plot(time, TriangleWave, 'k')
```

```matlab
xlabel('Time(ms)')
ylabel('Voltage(V)')
legend('Triangle wave')


%%  Creation of the instantaneous voltage vectors: ************************

% Bipolar
u1_inst = (Vdc*sign(u1 - TriangleWave))/2;
u2_inst = (Vdc*sign(u2 - TriangleWave))/2;
u3_inst = (Vdc*sign(u3 - TriangleWave))/2;


% Unipolar
% u1_inst = (Vdc + Vdc*sign(u1 - TriangleWave))/2;
% u2_inst = (Vdc + Vdc*sign(u2 - TriangleWave))/2;
% u3_inst = (Vdc + Vdc*sign(u3 - TriangleWave))/2;

% Plotting of the instantaneous voltage vectors:
figure
subplot(3, 1, 1)
plot(time/1000, u1_inst, 'b')
xlabel('Time (ms)')
ylabel('Voltage (V)')
legend('u1inst')
title('')
subplot(3, 1, 2)
plot(time/1000, u2_inst, 'g')
xlabel('Time (ms)')
ylabel('Voltage (V)')
legend('u2inst')
subplot(3, 1, 3)
plot(time/1000, u3_inst, 'k')
xlabel('Time (ms)')
ylabel('Voltage (V)')
legend('u3inst')


u12 = u1_inst - u2_inst;
u23 = u2_inst - u3_inst;
u31 = u3_inst - u1_inst;

%% Creation of Diode and IGBT Currents

i_T1U = 0*time;
```

```matlab
i_T1L = 0*time;
i_D1U = 0*time;
i_D1L = 0*time;

i_T2U = 0*time;
i_T2L = 0*time;
i_D2U = 0*time;
i_D2L = 0*time;

i_T3U = 0*time;
i_T3L = 0*time;
i_D3U = 0*time;
i_D3L = 0*time;

% Determination of current paths

for count = 1: length(time)
  % leg 1
   i_investigate = i1(count);
   u_investigate = u1_inst(count);

   if i_investigate>0
      if u_investigate>0
         i_T1U(count) = i_investigate;
      elseif u_investigate<0 && i_investigate < VT_D/Rf_MOS
            i_T1L(count) = i_investigate;
         else
            i_T1L(count) = ((Rf_D * i_investigate) + VT_D)/(Rf_D + Rf_MOS);
            i_D1L(count) = ((Rf_MOS *i_investigate) - VT_D)/(Rf_D + Rf_MOS);

      end
    else
      if u_investigate<0
         i_T1L(count) = i_investigate;
      elseif u_investigate>0 && i_investigate >- VT_D/Rf_MOS
            i_T1U(count) = i_investigate;
         else
            i_T1U(count) = ((Rf_D * i_investigate) - VT_D)/(Rf_D + Rf_MOS);
            i_D1U(count) = ((Rf_MOS * i_investigate) + VT_D)/(Rf_D + Rf_MOS);
      end
```

```
    end

    % leg 2
    i_investigate = i2(count);
    u_investigate = u2_inst(count);

if i_investigate>0
        if u_investigate>0
            i_T2U(count) = i_investigate;
        elseif u_investigate<0 && i_investigate < VT_D/Rf_MOS
                i_T2L(count) = i_investigate;
            else
                i_T2L(count) = ((Rf_D * i_investigate) + VT_D)/(Rf_D + Rf_MOS);
                i_D2L(count) = ((Rf_MOS * i_investigate) - VT_D)/(Rf_D + Rf_MOS);

        end
     else
        if u_investigate<0
            i_T2L(count) = i_investigate;
        elseif u_investigate>0 && i_investigate > -VT_D/Rf_MOS
                i_T2U(count) = i_investigate;
            else
                i_T2U(count) = ((Rf_D * i_investigate) - VT_D)/(Rf_D + Rf_MOS);
                i_D2U(count) = ((Rf_MOS * i_investigate) + VT_D)/(Rf_D + Rf_MOS);
        end
    end

    % leg 3
    i_investigate = i3(count);
    u_investigate = u3_inst(count);

 if i_investigate>0
        if u_investigate>0
            i_T3U(count) = i_investigate;
        elseif u_investigate<0 && i_investigate < VT_D/Rf_MOS
                i_T3L(count) = i_investigate;
            else
                i_T3L(count) = ((Rf_D * i_investigate) + VT_D)/(Rf_D + Rf_MOS);
```

```
                i_D3L(count) = ((Rf_MOS * i_investigate) - VT_D)/(Rf_D + Rf_MOS);

        end
     else
        if u_investigate<0
            i_T3L(count) = i_investigate;
        elseif u_investigate>0 && i_investigate > -VT_D/Rf_MOS
                i_T3U(count) = i_investigate;
            else
                i_T3U(count) = ((Rf_D * i_investigate) - VT_D)/(Rf_D + Rf_MOS);
                i_D3U(count) = ((Rf_MOS * i_investigate) + VT_D)/(Rf_D + Rf_MOS);
        end
    end

end

% correcting into postive current
i_T1L= -i_T1L;
i_T2L= -i_T2L;
i_T3L= -i_T3L;

i_D1U = -i_D1U;
i_D2U = -i_D2U;
i_D3U = -i_D3U;

%% Calculation of on-state losses

p_Onstate_T1U = 0*time;
p_Onstate_T1L = 0*time;
p_Onstate_D1U = 0*time;
p_Onstate_D1L = 0*time;

p_Onstate_T2U = 0*time;
p_Onstate_T2L = 0*time;
p_Onstate_D2U = 0*time;
p_Onstate_D2L = 0*time;

p_Onstate_T3U = 0*time;
p_Onstate_T3L = 0*time;
p_Onstate_D3U = 0*time;
p_Onstate_D3L = 0*time;

```

```
for count = 1:length(time)
%  leg 1
if i_T1U(count)>0
     p_Onstate_T1U(count) = (VT_MOS + Rf_MOS*i_T1U(count))*
         i_T1U(count);
else
     p_Onstate_T1U(count) = (VT_MOS + Rf_MOS*(i_T1U(count)))
         *(i_T1U(count));
end
if i_T1L(count)>0
     p_Onstate_T1L(count) = (VT_MOS + Rf_MOS*i_T1L(count))*
         i_T1L(count);
else
     p_Onstate_T1L(count) = (VT_MOS + Rf_MOS*(i_T1L(count)))
         *(i_T1L(count));
end

if i_D1U(count)>0
     p_Onstate_D1U(count) = (VT_D + Rf_D*i_D1U(count))*i_D1U(
         count);
else
     p_Onstate_D1U(count) = (VT_D + Rf_D*i_D1U(count))*i_D1U(
         count);
end
if i_D1L(count)>0
     p_Onstate_D1L(count) = (VT_D + Rf_D*i_D1L(count))*i_D1L(
         count);
else
     p_Onstate_D1L(count) = (VT_D + Rf_D*i_D1L(count))*i_D1L(
         count);
end


% leg 2

if i_T2U(count)>0
     p_Onstate_T2U(count) = (VT_MOS + Rf_MOS*i_T2U(count))*
         i_T2U(count);
else
     p_Onstate_T2U(count) = (VT_MOS + Rf_MOS*i_T2U(count))*
         i_T2U(count);
end
if i_T2L(count)>0
     p_Onstate_T2L(count) = (VT_MOS + Rf_MOS*i_T2L(count))*
         i_T2L(count);
else
```

```
        p_Onstate_T2L(count) = (VT_MOS + Rf_MOS*i_T2L(count))*i_T2L(count);
end

if i_D2U(count)>0
        p_Onstate_D2U(count) = (VT_D + Rf_D*i_D2U(count))*i_D2U(count);
else
        p_Onstate_D2U(count) = (VT_D + Rf_D*i_D2U(count))*i_D2U(count);
end
if i_D2L(count)>0
        p_Onstate_D2L(count) = (VT_D + Rf_D*i_D2L(count))*i_D2L(count);
else
        p_Onstate_D2L(count) = (VT_D + Rf_D*i_D2L(count))*i_D2L(count);
end

% leg3
if i_T3U(count)>0
        p_Onstate_T3U(count) = (VT_MOS + Rf_MOS*i_T3U(count))*i_T3U(count);
else
        p_Onstate_T3U(count) = (VT_MOS + Rf_MOS*i_T3U(count))*i_T3U(count);
end
if i_T3L(count)>0
        p_Onstate_T3L(count) = (VT_MOS + Rf_MOS*i_T3L(count))*i_T3L(count);
else
        p_Onstate_T3L(count) = (VT_MOS + Rf_MOS*i_T3L(count))*i_T3L(count);
end

if i_D3U(count)>0
        p_Onstate_D3U(count) = (VT_D + Rf_D*i_D3U(count))*i_D3U(count);
else
        p_Onstate_D3U(count) = (VT_D + Rf_D*i_D3U(count))*i_D3U(count);
end
if i_D3L(count)>0
        p_Onstate_D3L(count) = (VT_D + Rf_D*i_D3L(count))*i_D3L(count);
else
```

```
    p_Onstate_D3L(count) = (VT_D + Rf_D*i_D3L(count))*i_D3L(count);
end

end


P_Onstate_T1U = mean(p_Onstate_T1U)
P_Onstate_D1U = mean(p_Onstate_D1U)
P_Onstate_T1L = mean(p_Onstate_T1L)
P_Onstate_D1L = mean(p_Onstate_D1L)

P_Onstate_T2U = mean(p_Onstate_T2U)
P_Onstate_D2U = mean(p_Onstate_D2U)
P_Onstate_T2L = mean(p_Onstate_T2L)
P_Onstate_D2L = mean(p_Onstate_D2L)

P_Onstate_T3U = mean(p_Onstate_T3U)
P_Onstate_D3U = mean(p_Onstate_D3U)
P_Onstate_T3L = mean(p_Onstate_T3L)
P_Onstate_D3L = mean(p_Onstate_D3L)

%% Calculation of Switching losses

Psw_MOS_SK = fsw*(Esw_MOS_on + Esw_MOS_off)*(1/pi*Irms*sqrt(2)/Iref)^KiMOS*(Vdc/Vref)^KvMOS;
Psw_T1U= Psw_MOS_SK;
Psw_T1L= Psw_MOS_SK;
Psw_T2U= Psw_MOS_SK;
Psw_T2L= Psw_MOS_SK;
Psw_T3U= Psw_MOS_SK;
Psw_T3L= Psw_MOS_SK;

%% start total loss summation

T1U = [Psw_T1U + P_Onstate_T1U, P_Onstate_T1U, Psw_T1U];
T2U = [Psw_T2U + P_Onstate_T2U, P_Onstate_T2U, Psw_T2U];
T3U = [Psw_T3U + P_Onstate_T3U, P_Onstate_T3U, Psw_T3U];
T1L = [Psw_T1L + P_Onstate_T1L, P_Onstate_T1L, Psw_T1L];
T2L = [Psw_T2L + P_Onstate_T2L, P_Onstate_T2L, Psw_T2L];
T3L = [Psw_T3L + P_Onstate_T3L, P_Onstate_T3L, Psw_T3L];


%% Final Plotting

labelfont = 14;
```

```
tickfont  =  14;
figure()
start  =  1;
stop  =  length(time);
h  =  plot(time(start:stop)*1000, i_T1L(start:stop));grid;
%set(h, 'LineWidth', 2);
% set(h(2), 'LineWidth', 2);
% set(h(3), 'LineWidth', 2);
ax1 = gca;
set(ax1, 'FontName', 'times', 'FontSize', tickfont)
title('Current, Lower Transistor', 'FontName', 'times', 'Fontsize', labelfont)
xlabel('Time (ms)', 'FontName', 'times', 'Fontsize', labelfont)
ylabel('Currents (A)', 'FontName', 'times', 'Fontsize', labelfont)

labelfont = 14;
tickfont = 14;
figure()
start = 1;
stop = length(time);
h  =  plot(time(start:stop)*1000, p_Onstate_D1L(start:stop));grid;
%set(h, 'LineWidth', 2);
% set(h(2), 'LineWidth', 2);
% set(h(3), 'LineWidth', 2);
ax1 = gca;
set(ax1, 'FontName', 'times', 'FontSize', tickfont)
title('On-State Loss, Lower Diode', 'FontName', 'times', 'Fontsize', labelfont)
xlabel('Time (ms)', 'FontName', 'times', 'Fontsize', labelfont)
ylabel('Onstate loss (W)', 'FontName', 'times', 'Fontsize', labelfont)


labelfont = 25;
tickfont = 20;
figure()
start = 1;
stop = length(time);
h  =  plot(time(start:stop)*1000, p_Onstate_T1U(start:stop), time(start:stop)*1000, -p_Onstate_T1L(start:stop));grid;
%set(h, 'LineWidth', 2);
% set(h(2), 'LineWidth', 2);
```

```
% set(h(3), 'LineWidth', 2);
ax1 = gca;
ax1.FontSize = 20;
set(ax1, 'FontName', 'times', 'FontSize', tickfont)
title('On-State Loss, Upper Transistor and Lower Transistor at 14kRPM,200Nm', 'FontName', 'times', 'Fontsize', labelfont)
xlabel('Time (ms)', 'FontName', 'times', 'Fontsize', labelfont)
ylabel('Onstate loss (W)', 'FontName', 'times', 'Fontsize', labelfont)


% Plot Iphase a and T1U and D1L losses
figure
plot(1000*time, i1, 'k--', 1000*time, i_T1U, 'r', 1000*time, i_D1L, 'c', 1000*time, i_T1L, 'b', 1000*time, i_D1U, 'g-')
```

C

Appendix 3 - PLECS blockset and Simscape models

C.1 PLECS blockset Model

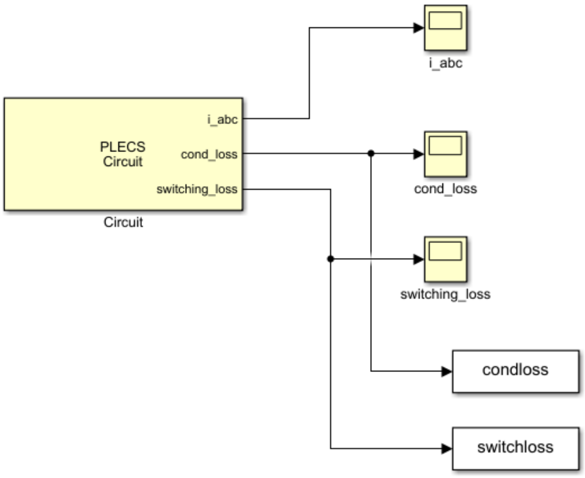


Figure C.1: PLECS blockset setup to obtain lossmaps.

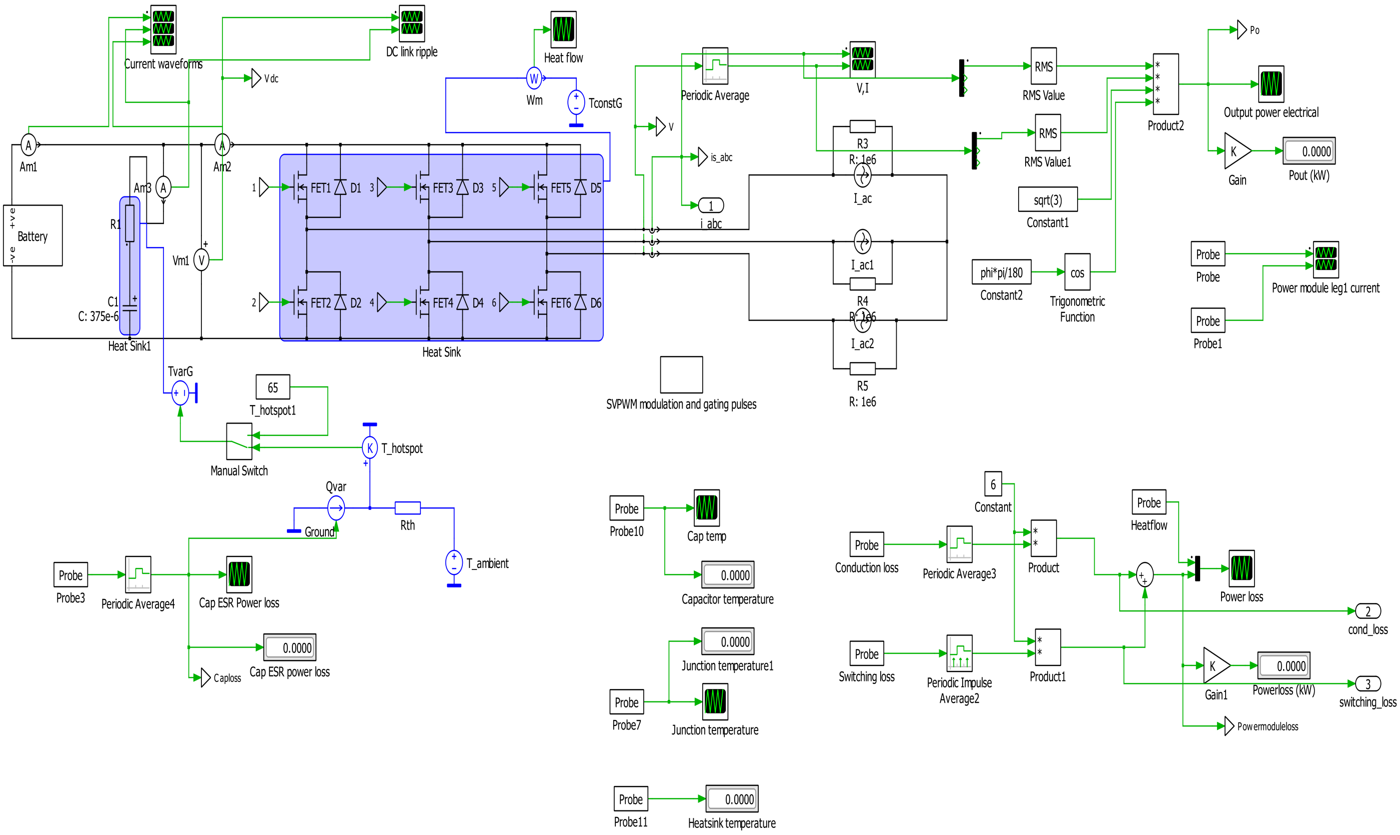


Figure C.2: PLECS blockset complete thermal circuit.

```
%% Generating lossmaps using electric machine motoring region operating points
clear all
close all
clc

%% Load data from .mat file

a= load('EMdata.mat');
b= a.param.calc_results.performance_maps.data(2).PF;
c= a.param.calc_results.performance_maps.data(2).CurrAng;
d= a.param.calc_results.performance_maps.data(2).VoltAng;
e= a.param.calc_results.performance_maps.data(2).CurrMag;
f= a.param.calc_results.performance_maps.data(2).VoltMag;
g= a.param.calc_results.performance_maps.data(2).Torques;
h= a.param.calc_results.performance_maps.data(2).nref_Map;
PF= b.data;
CurrAng= c.data;
VoltAng= d.data;
CurrMag= e.data;
VoltMag= f.data;
Torque= g.data;
```

```
speed= h.data;

% static characteristics
Vdc= 820;
p= 8;
Rgon= 4;
Rgoff= 2.5;
fs=10e3;

%% Losses determination
  for k= 1:20
     disp(k)
  for i= 1:62
     disp(i)
    Tinit= 80;
    Th=0;
    Ta= 80;
    Vang= VoltAng(i,k);
    phi= (VoltAng(i,k)-CurrAng(i,k));
    Vref= VoltMag(i,k);
    I= CurrMag(i,k);
    f= speed(i,k)*p/120;
    a= 2*pi*(f/fs/2)*180/pi;
    sim('plecsthermalmodel')
    P_conductionloss(i,k)= condloss(length(condloss),1);
    P_switchingloss(i,k)= switchloss(length(switchloss),1);
    P_total(i,k)= P_conductionloss(i,k)+P_switchingloss(i,k)
       ;
  end
  end

figure (1)
contour(speed,Torque,P_total,20,'ShowText','on')
ax = gca;
ax.XAxis.Exponent = 0;
xlabel('Speed (RPM)')
ylabel('Torque (Nm)')
title('Loss map at 80 degree C')
grid on

figure (2)
contour(speed,Torque,P_switchingloss,20,'ShowText','on')
ax = gca;
ax.XAxis.Exponent = 0;
xlabel('Speed (RPM)')
ylabel('Torque (Nm)')
```

```
title('Switching Loss map at 80 degree C')
grid on

figure (3)
contour(speed,Torque,P_conductionloss,20,'ShowText','on')
ax = gca;
ax.XAxis.Exponent = 0;
xlabel('Speed (RPM)')
ylabel('Torque (Nm)')
title('Conduction Loss map at 80 degree C')
grid on
```

C.2 Simscape model

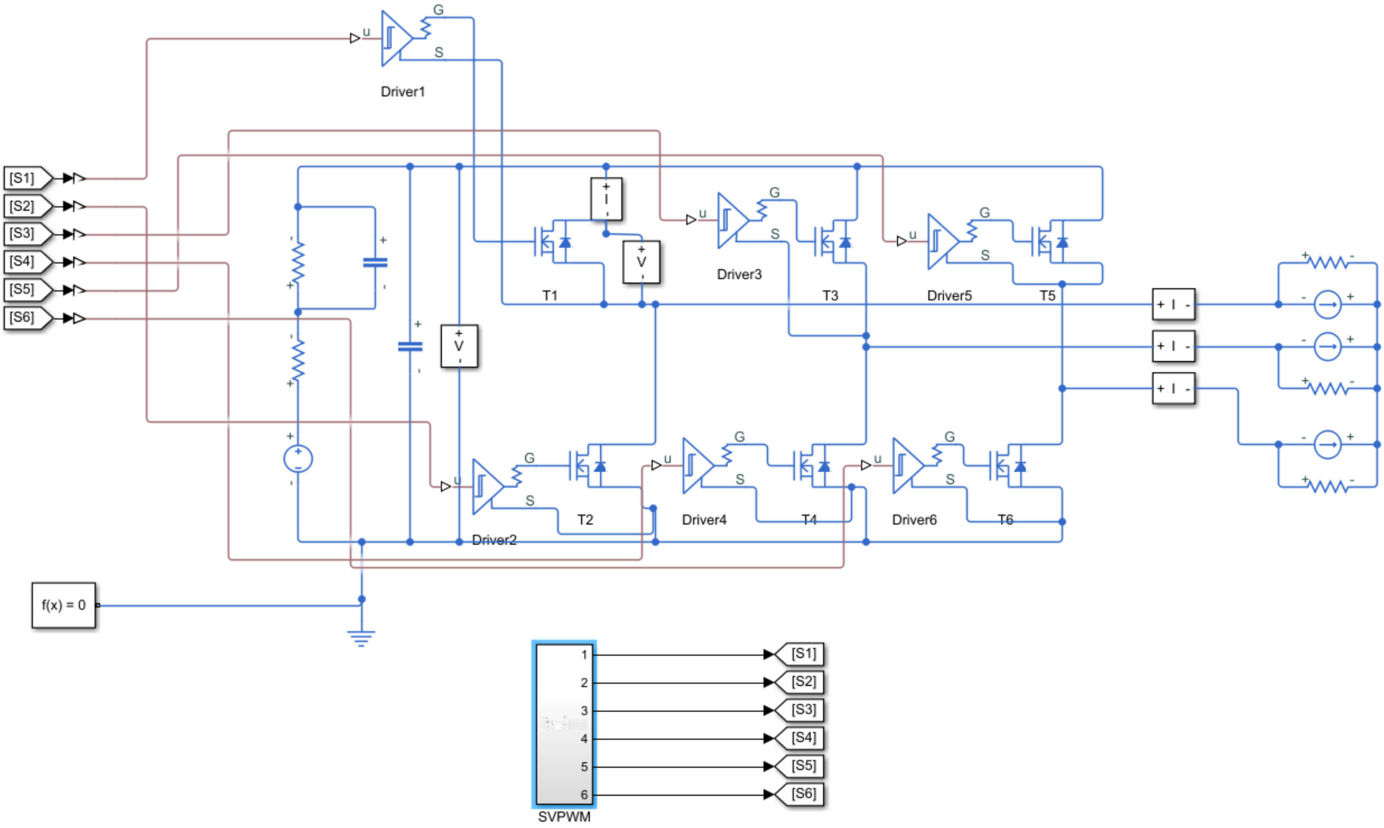


Figure C.3: Simscape Model.

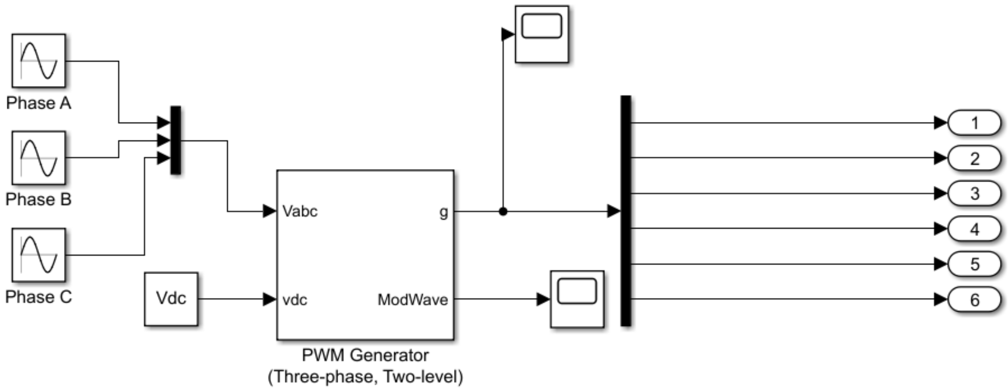


Figure C.4: Simscape Model's SVPWM block.

D

Appendix 4 - Thermal description of DYNEX Power module

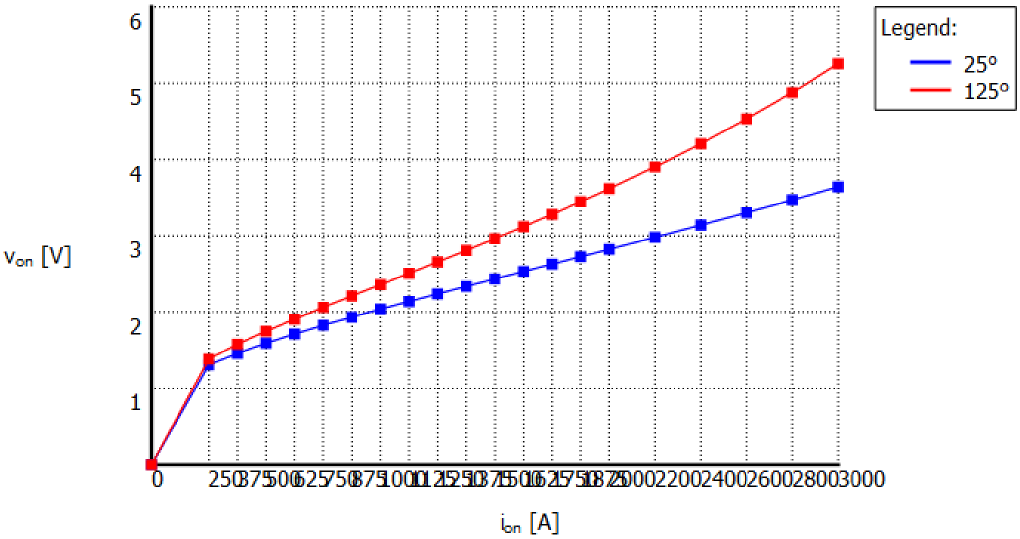


Figure D.1: V I characteristics of DYNEX IGBT DIM1200FSS12-A000

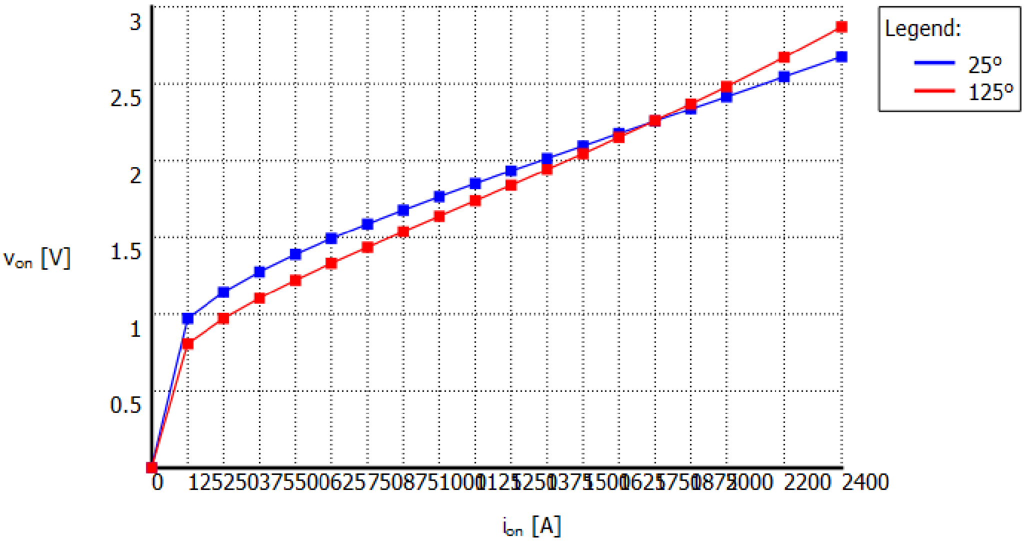
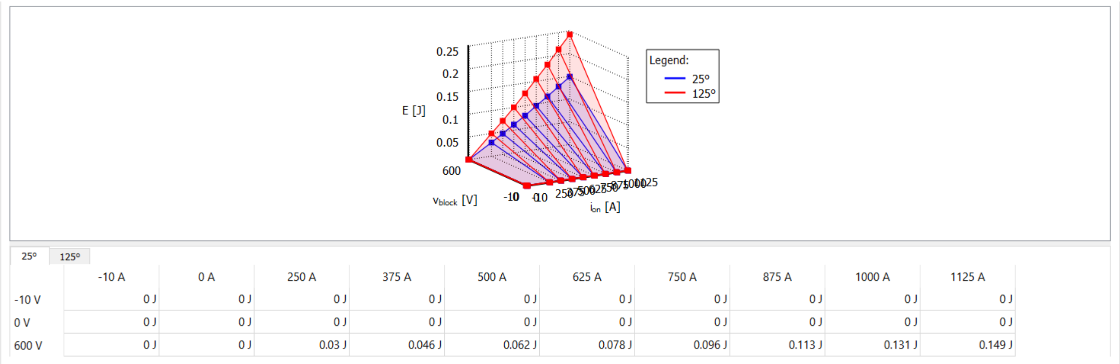
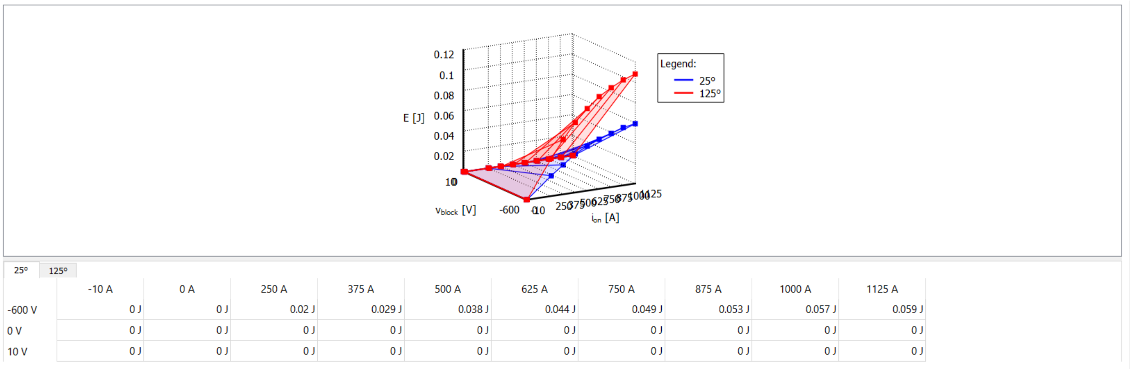


Figure D.2: V I characteristics of DYNEX IGBT's antiparallel diode DIM1200FSS12-A000



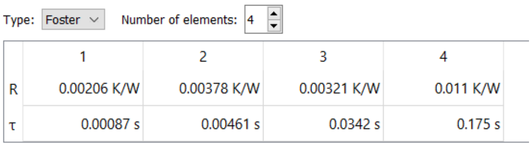
	-10 A	0 A	250 A	375 A	500 A	625 A	750 A	875 A	1000 A	1125 A
-10 V	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J
0 V	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J
600 V	0 J	0 J	0.03 J	0.046 J	0.062 J	0.078 J	0.096 J	0.113 J	0.131 J	0.149 J

Figure D.3: Switching energy lookup table of DYNEX IGBT DIM1200FSS12-A000



	-10 A	0 A	250 A	375 A	500 A	625 A	750 A	875 A	1000 A	1125 A
-600 V	0 J	0 J	0.02 J	0.029 J	0.038 J	0.044 J	0.049 J	0.053 J	0.057 J	0.059 J
0 V	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J
10 V	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J	0 J

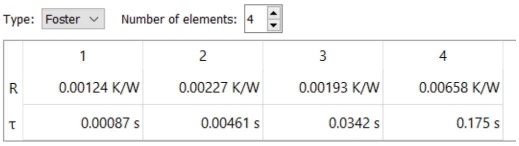
Figure D.4: Switching energy lookup table of DYNEX IGBT's antiparallel diode DIM1200FSS12-A000



Type: Foster
Number of elements: 4

	1	2	3	4
R	0.00206 K/W	0.00378 K/W	0.00321 K/W	0.011 K/W
τ	0.00087 s	0.00461 s	0.0342 s	0.175 s

Figure D.5: Thermal impedance network of DYNEX IGBT DIM1200FSS12-A000



Type: Foster
Number of elements: 4

	1	2	3	4
R	0.00124 K/W	0.00227 K/W	0.00193 K/W	0.00658 K/W
τ	0.00087 s	0.00461 s	0.0342 s	0.175 s

Figure D.6: Thermal impedance network of DYNEX IGBT's antiparallel diode DIM1200FSS12-A000

DEPARTMENT OF SOME SUBJECT OR TECHNOLOGY
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden
www.chalmers.se