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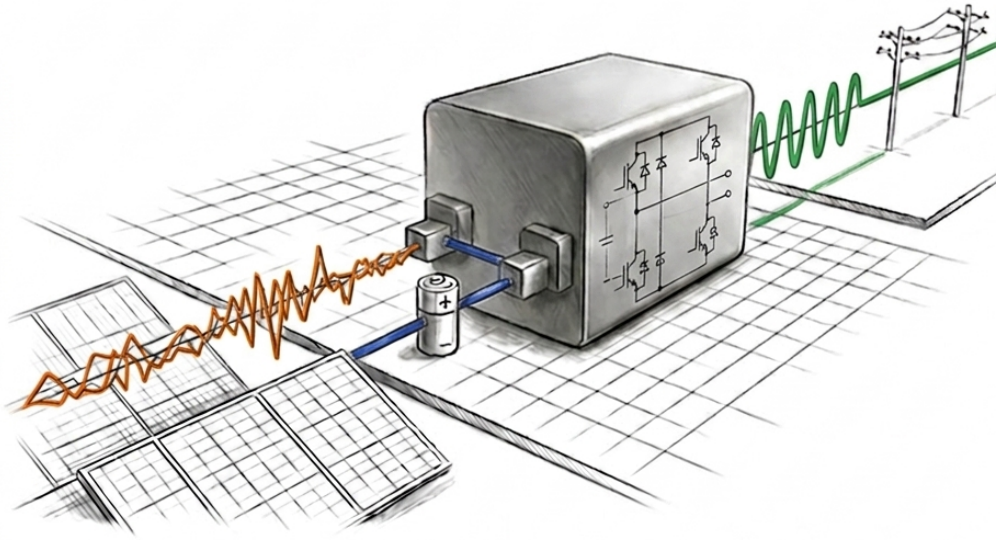

Design & Development of a CHB-Based Converter for Direct Integration of Renewables to the Grid

Master's thesis in Sustainable Electric Power Engineering and Electromobility

NAZANIN ABBASI

DEPARTMENT OF Electrical Engineering

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Supervisor: Abhijit Choudhury, Hitachi Energy
Examiner: Massimo Bongiorno, Department of Electrical Engineering

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Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 (0)31 772 1000

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NAZANIN ABBASI
Department of Electrical Engineering
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Abstract

The integration of solar photovoltaic (PV) and battery energy storage systems (BESS) into the power grid requires high-performance power electronic interfaces to replace traditional, inefficient separate converter setups. This thesis investigates a unified 10 MW/10 kV modular multilevel architecture utilizing a cascaded H-bridge (CHB) inverter integrated with dual active bridge (DAB) stages. Unlike previous models, this system uses high-frequency transformers (HFT) within the DAB stages to provide galvanic isolation and improve power density. This configuration aims to reduce power conversion stages and enhance overall system efficiency.

The first phase of the research focuses on the design and implementation of the power stage and its control systems. A modular architecture is developed, and closed-loop controllers are designed to manage the bidirectional power flow between the PV-BESS common DC-link and the utility grid. To evaluate the thermal behavior and efficiency of the system, the proposed model is simulated in PLECS. This allows for detailed thermal modeling to determine the relationship between the electrical dynamics and switching losses.

Finally, a comprehensive comparative analysis is performed between 1.7 kV and 3.3 kV silicon carbide (SiC) MOSFETs. The study evaluates these two semiconductor technologies based on conduction and switching losses, overall system efficiency, and cost-effectiveness. The results show that while the 1.7 kV SiC model provides higher overall system efficiency, the choice of the 3.3 kV SiC model allows for a significant reduction in the cost and the total number of sub-modules while maintaining acceptable thermal performance, providing a clear design roadmap for next-generation, high-density modular systems.

Keywords: Cascaded H-Bridge (CHB), Dual Active Bridge (DAB), Silicon Carbide (SiC) MOSFETs, Common DC-link, BESS-PV Integration.

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On a personal note, my parents deserve recognition for their lifelong encouragement and the many sacrifices they made to ensure I had every educational opportunity. Finally, this achievement would not have been possible without my husband. His love, patience, and constant belief in me were my greatest source of support.

Nazanin Abbasi,
Gothenburg, Sweden,
June 2026

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

BESS	Battery Energy Storage System
CHB	Cascaded H-Bridge
FC	Flying Capacitor
IMC	Internal Model Control
LFT	Low-Frequency Transformer
MLC	Multilevel Converter
MMC	Modular Multilevel Converter
MPPT	Maximum Power Point Tracking
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
PLL	Phase Locked Loop
PS-PWM	Phase-Shifted Pulse Width Modulation
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable-Based Energy Sources
THD	Total Harmonic Distortion
VSG	Virtual Synchronous Generator
WBG	Wide Bandgap
YCHB	Star-Connected Cascaded H-Bridge
ZVS	Zero Voltage Switching

Nomenclature

This section summarizes the indices, parameters, and variables used throughout the thesis.

Indices

i	Index of cascaded H-bridge cell or submodule
j	Index of system node or module
t	Time index

Parameters

P	Rated system power
V_{LL}	Grid line-to-line RMS voltage
$V_{ph,\mathrm{rms}}$	Grid phase RMS voltage
V_{dc}	DC-link voltage of one H-bridge module
$V_{dc,\mathrm{total}}$	Total DC-link voltage per phase
$V_{dc,op}$	Operating DC voltage per H-bridge module
$V_{dc,ref}$	DC-link voltage reference
V_p	Primary-side DC voltage of DAB
V_s	Secondary-side DC voltage of DAB
$P_{\max}$	Maximum transferable power
P_{cond}	Conduction losses
P_{sw}	Switching losses
m	Modulation index
f_{sw}	Switching frequency
$f_{sw,\mathrm{CHB}}$	Switching frequency of CHB inverter
$f_{sw,\mathrm{DAB}}$	Switching frequency of DAB converter

f_{eff}	Effective output switching frequency
N_{SM}	Number of cascaded submodules per phase
n	Transformer turns ratio (N_p/N_s)
L_{lk}	Transformer leakage inductance
L_f	Grid-side filter inductance
R_f	Grid-side filter resistance
C_{dc}	DC-link capacitance
ΔV	DC-link voltage ripple
η	System efficiency
UF	Semiconductor utilization factor

Variables

v_o	Output voltage of a single H-bridge module
$v_{cell,i}$	Output voltage of submodule i
v_{abc}	Three-phase output voltage vector
v_d, v_q	Converter output voltage in dq reference frame
i_{abc}	Three-phase grid current vector
i_d, i_q	Grid current in dq reference frame
i_d^*, i_q^*	Reference currents in dq frame
S_{11}, S_{12}	Switching states of H-bridge devices
$S_{i,L1}, S_{i,L2}$	Switching states of lower and upper legs of submodule i
m_a, m_b, m_c	Modulation signals for phases A, B, and C
θ	Phase angle between DAB primary and secondary voltages
d	Normalized phase-shift ratio in DAB modulation
K_p, K_i	Proportional and integral gains of PI controller
K_{pc}, K_{ic}	PI gains of CHB current controller
K_{pd}, K_{id}	PI gains of DAB voltage controller

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1
Introduction

1.1 Background

As industries grow and more activities become electrified worldwide, the demand for electricity keeps increasing annually. The building and industrial sectors consume almost 90% of global electricity which will continue to increase over the next several decades according to predictions [1]. The expansion of power generation has led to increased amount of CO_2 emissions since fossil fuels still provide the majority of the electricity consumption. More than 900 million tons of CO_2 entered the atmosphere due to the production of heat and electricity in 2021 [1]. These recent developments show the need for more sustainable energy sources.

Solar photovoltaics (PV) is growing faster than almost any other clean energy solutions. Europe had already installed around 78 GW of PV capacity by 2013, and this trend has continued due to the decreasing price of PV modules and not affecting the current system setups [2]. However, solar energy often fails to match the real power needs of commercial buildings. While PV generation peaks around 12 pm, commercial loads often peak later between 2 pm and 8 pm [3]. Consequently, PV generation alone is not able to reduce peak load in commercial buildings.

This is where battery energy storage systems (BESS) become important. BESS can store solar energy when it is available and support the grid when the load demand is high. Integrating BESS units can significantly improve power system reliability, enhance voltage stability while, most importantly, reducing related environmental emissions [4]. Combining PV and BESS can also lead to a significant decrease in annual operational costs by optimal sizing and fully utilization of BESS unit's capacity [5]. A case study in a Malaysian factory showed that combining PV panels with BESS units contributed to a 6.9% reduction in energy costs and a 8.6% decrease in CO_2 emissions [1]. Furthermore, another research about PV ramp rate control indicates that BESS can be used as energy buffer, preventing voltage swings and smoothing sudden fluctuations [6]. To improve transient stability and provide necessary inertia during mode transitions, researchers are deploying virtual synchronous generator (VSG) frameworks integrated with neural networks to mitigate performance lags [7]. These results show that combination of PV modules and BESS, rather than operating separately and independently, can lead to environmental sustainability.

After it becomes clear that PV needs to be supported by BESS, the next questions are: how are these technologies currently integrated into the grid, and how can be this integration effectively improved?

In conventional architectures, as shown in Fig 1.1, PV modules and BESS units each operate with their own dedicated DC/AC conversion stages. Both systems are connected to the grid through separate, bulky low-frequency transformers (LFT). This topology requires large passive filters and heavy transformers, which increases the total volume and weight of the system. As illustrated in Fig 1.1, there are two primary power paths for supplying the grid: the PV path (P_{PV}) and the BESS path (P_{BESS}). When the PV generation is sufficient, it supplies the grid through the MPPT and DC/AC stages with an efficiency of $\eta_1 \cdot \eta_2$. When the PV generation is not sufficient, the BESS supports the grid through the DC/DC and DC/AC stages with an efficiency of $\eta_3 \cdot \eta_4$. However, a significant drawback occurs during charging periods ($P_{PV-PBESS}$), where the PV system must charge the battery. In this scenario, the energy must pass through four consecutive conversion stages, resulting in a cumulative efficiency of $\eta_1 \cdot \eta_2 \cdot \eta_3 \cdot \eta_4$. This multiple-stage conversion leads to a significant reduction in overall efficiency; for instance, conventional two-stage grid-interfaced architectures reported in the literature typically achieve system efficiencies below 95% due to these cumulative conduction and switching losses [8, 9].

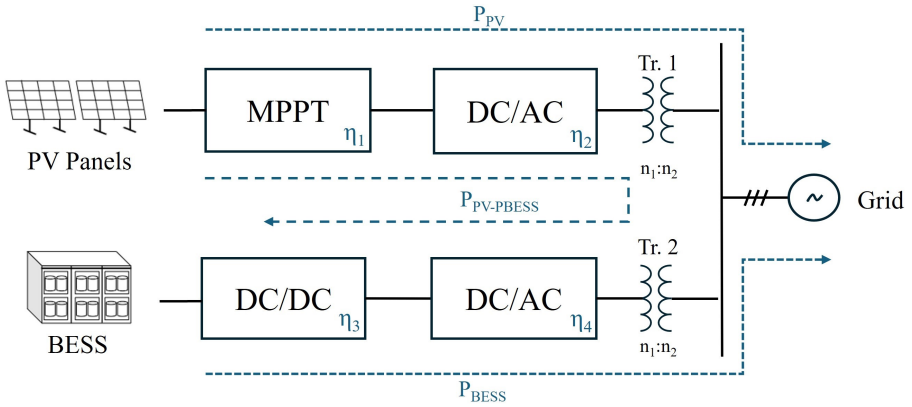

Figure 1.1: Conventional architecture for integration of PV and BESS to the grid.

To address the limitations of bulkiness and weight, transformerless architectures have been proposed as shown in Fig. 1.2. As illustrated in Fig. 1.2, both the PV path (P_{PV}) and the BESS path (P_{BESS}) to the grid share the same efficiency, resulting in path efficiencies of $\eta_1 \cdot \eta_2$ and $\eta_2 \cdot \eta_3$, respectively. A key advantage of this architecture is seen during the battery charging phase ($P_{PV-PBESS}$). Unlike the conventional four-stage process, the energy transfer from PV to BESS now only passes through two conversion stages. The resulting efficiency of proposed system ($\eta_1 \cdot \eta_3$) is significantly higher than conventional one ($\eta_1 \cdot \eta_2 \cdot \eta_3 \cdot \eta_4$).

The overall weight reduction is achieved by using MMC which directly integrates to the grid without LFT [10]. By eliminating the low-frequency transformer, this topology significantly reduces the overall weight and volume of the system. To fur-

ther enhance power density, researchers utilize optimization algorithms to minimize the footprint of arm inductors, heat sinks, and cell capacitors. This is done by identifying the ideal balance between the quantity of sub-modules and the total system volume [11].

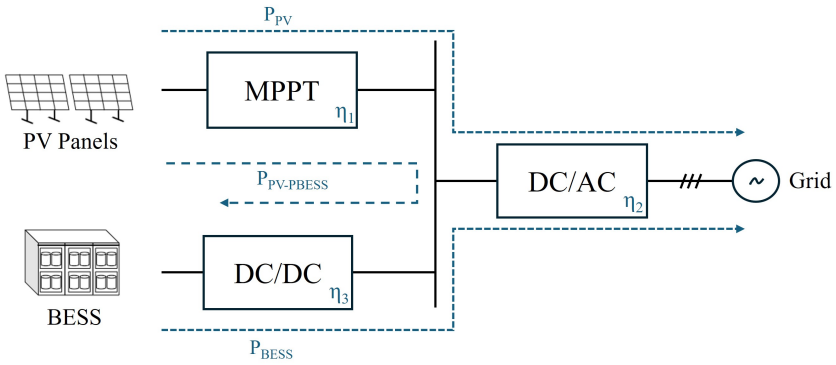

Figure 1.2: Proposed architecture for integration of PV and BESS to the grid.

Another approach is to use cascaded H-bridge (CHB) topology presented in [12]. Each cell can handle a single panel or string, which enables efficient maximum power point tracking (MPPT) due to the modular structure. However, CHB-based solid-state transformer (SST) architectures are particularly susceptible to power imbalance under asymmetric grid conditions, as each phase effectively operates as an independent single-phase converter. During unbalanced voltage sags, negative-sequence components can cause active power redistribution among phases, potentially leading to DC-link overvoltage and system shutdown if not properly controlled [13]. This issue can be effectively mitigated through active power balancing techniques such as zero-sequence voltage compensation [13, 14].

To address the major inefficiencies of traditional AC-coupled systems, DC-link integration has become a popular alternative [15]. This development shows a logical shift from separate units of conventional method toward more integrated structures. A direct DC-link between the PV arrays and individual sub-modules in the modular structure is considered as in [16]. This direct connection prevents intermediate stages between the PV panels and the converter sub-modules. At a broader system level, the DC link integration has been particularly proposed for renewable energy or datacenter applications which requires high power as well as high efficiency [17]. Common dc-bus systems often suffer from significant dc-link current ripples, necessitated by large, bulky capacitors. To address this, modern design techniques utilize optimal interleaving and carrier wave phase-shifting to suppress these harmonics, which ultimately enhances capacitor durability and reduces component size [18].

DC-link as a part of MMC architectures can improve power quality, regulate voltage, provide galvanic isolation and make controllability easier between power stages [19]. The effect of this DC-link integration can be significantly enhanced by the use of wide bandgap (WBG) semiconductors. SiC switches enable higher electric field

strength and switching frequencies and reduce the volume of the isolation stage and passive component sizes compared to silicon-based modules [20, 21]. By using SiC technology in these designs, it is also possible to manage internal power fluctuations without adding extra hardware components. This approach, known as active power decoupling, helps keep the system compact and efficient while protecting the circuit from voltage and current stress [22].

Despite these developments, the integration of DC-link with MMCs introduces significant control complexities, particularly regarding power balance and thermal management of SiC devices. While SiC devices offer high switching capabilities, their operation at high frequencies can lead to increased stress on the isolation stage. Therefore, there is a critical need for optimized control strategies that can utilize the full potential of SiC-based MMCs. This research proposes mutlilevel-based topology which aims to maximize the efficiency of PV-BESS integration in high-voltage networks.

1.2 Problem Statement

Conventional AC-coupled architectures as shown in Fig. 1.1 have inherently low efficiency, primarily as a result of redundant power conversion stages. Energy must undergo multiple DC-AC transformations to facilitate power transfer between the PV arrays, the BESS units, and the utility grid. Each intermediate stage introduces cumulative semiconductor switching and conduction losses, which significantly degrade the overall system efficiency.

Furthermore, these systems suffer from significant physical bulkiness due to their reliance on low-frequency transformers. The inherent limitations of low-frequency transformers and traditional silicon-based power electronics further constrain system performance, as they cannot support the high switching frequencies required to reduce the volume of passive components.

Consequently, there is an immediate need for an integrated DC-link architecture utilizing MMC and WBG semiconductors. Such a system can eliminate power conversion stages and substantially enhance the efficiency and power density of modern electrified systems.

1.3 Purpose & Aim

This master thesis aims to investigate and evaluate a DC-link architecture for the integration of Solar PV and BESS into a high-power grid. The research focuses on utilizing modular topologies and SiC technology to maximize system efficiency and power density while maintaining grid stability.
The project includes the following objectives:

- Perform a comprehensive literature review of MMC topologies, with a specific focus on the role of DAB converters and SiC semiconductors.

- Design and model a CHB inverter architecture, including calculation of the required DC-link voltage and the determination of optimal sub-module numbers for systems using 1.7 kV and 3.3 kV SiC switches.

- Develop simulation models in MATLAB/Simulink and PLECS to analyze the operational stability and bidirectional power flow of the integrated system.

- Conduct a detailed loss and efficiency evaluation and comparative system study for both 1.7 kV versus 3.3 kV SiC switches across various load conditions to identify technical and economic trade-offs.

- Perform a power quality analysis to assess total harmonic distortion (THD) and ensure the system complies with stringent grid-connection standards.

- Perform a cost-benefit analysis to evaluate the economic and technical trade-offs between utilizing 1.7 kV and 3.3 kV SiC-based sub-modules within the proposed modular architecture.

- Provide design recommendations for next-generation, high-density converter systems based on the findings of the performance and cost evaluations.

1.4 Delimitation

The scope of this research is centered on the simulation-based performance analysis of a 10 MW, 10 kV grid-connected converter system, designed to facilitate the integration of solar PV and battery energy storage systems via a common DC bus. The study focuses on the structural design of a CHB inverter architecture for high-voltage grid interfacing, supported by DAB isolation stages to manage bidirectional power flow and provide galvanic isolation. A primary objective of this work is a detailed technical comparison between 1.7 kV and 3.3 kV SiC MOSFETs to quantify the impact of these specific wide-bandgap device ratings on switching losses, conduction losses, and overall system efficiency. By simulating varying operational conditions, the research provides a comprehensive loss and cost-benefit analysis to determine the technical trade-offs associated with each semiconductor rating.

To maintain a manageable focus, the following delimitations are established: the investigation is conducted exclusively within a simulated environment using MATLAB/Simulink and PLECS, and therefore does not include physical hardware prototyping or experimental validation. The analysis is limited to the converter's steady-state performance, dynamic performance and loss and efficiency estimation; detailed thermal management system design (e.g., heat-sink geometry) are considered outside the scope of this work. Furthermore, the study assumes idealized grid conditions

and does not account for long-term aging effects or reliability degradation of the SiC components.

1.5 Thesis Outline

The thesis is organized into five chapters, beginning with Chapter 1, which establishes the background, motivation, and primary contributions of the research. Given that the focus of this work is on a modular converter structure for the effective integration of renewable energy resources, Chapter 2 provides a detailed overview of the system modeling, including the SST topology and the mathematical framework of the proposed architecture. Chapter 3 presents the core control strategy for the integrated system, covering the design of closed-loop controllers and the implementation of PWM modulation. Chapter 4 focuses on simulation and results, where the dynamic performance and steady-state behavior of the proposed system are evaluated through extensive simulations, including a comparative study of 1.7 kV and 3.3 kV SiC switches. Chapter 5 is dedicated to a detailed loss, efficiency, and cost analysis, examining conduction and switching losses under various operating conditions and assessing the trade-offs between different device voltage ratings and sub-module counts. Finally, Chapter 6 concludes the thesis with a summary of the key findings, a discussion of their technical implications, and recommendations for future work.

2

System Study and Modeling

2.1 Introduction

At the highest level of power electronics, voltage source converters are the standard systems used to turn DC power into AC power. Within this category, multilevel converters shift the focus from traditional two-level power conversion. These converters use several small power sources and switches to change voltage levels. Many different types of multilevel converters have been developed and presented over the last few decades, with the most common categories shown in Fig 2.1.

Integrated multilevel converters produce multiple output voltage levels using a single common DC-link, providing high power density and compact system integration. The neutral point clamped (NPC) converters achieve multiple voltage levels from a single DC-link by its use of clamping diodes. NPC is a well-established benchmark for BESS units due to simple control algorithms and implementation [23]. In PV-BESS applications, the NPC provides a stable interface; however, it typically uses a single DC-link, which complicates the independent management of energy sources. Furthermore, while NPC structures are effective for improving power quality, they lack the inherent modularity required for scaling [24]. The main issue with the NPC topology is the rapid increase in the number of clamping diodes as the voltage levels increase, making it bulky and complex for high-voltage applications [25].

The Flying Capacitor (FC) converter is the second common integrated topology, which used the replacement of clamping diodes with floating or flying capacitors to make voltage levels. It is suitable for high-voltage operation because the DC bus voltage is distributed across multiple series-connected capacitors and switching devices. The FC topology requires a large number of capacitors, which increases the physical size of the converter and control complexity [25]. Balancing capacitor voltage needs advanced control strategies in FC converters. This challenge becomes more visible as the voltage level increases, which limits its applicability in high-voltage and high-power systems.

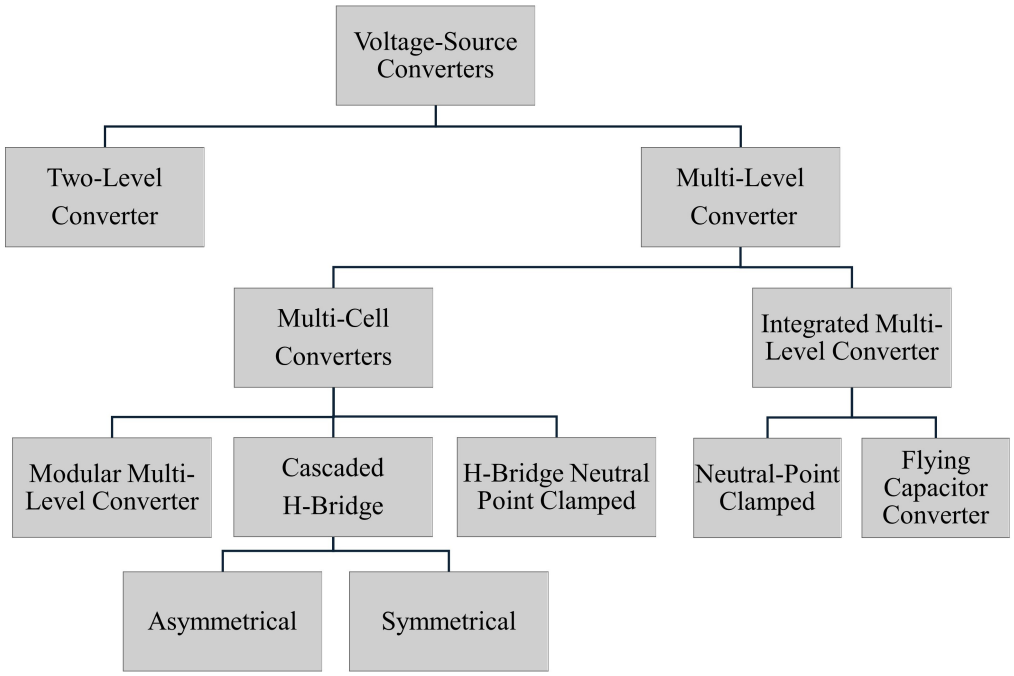

Figure 2.1: Classification of high-power voltage source converters.

In contrast to integrated multilevel converters, multi-cell converters reach higher voltage levels by connecting multiple converter cells in series, which offer improved modularity and flexibility for high-voltage applications. H-bridge neutral point clamped converters combine features of cascaded H-bridge and integrated NPC structures. While mentioned topology is discussed in academic literature for grid-connected PV systems, they are rarely used in large-scale industrial BESS. As highlighted in [26], these systems combine NPC structures with H-Bridge cells, which significantly increases the semiconductor count to eight switches per phase. Furthermore, the integration of quasi-impedance networks and the need for modified level-shifted PWM techniques introduce control complexities that make them less standardized than the modular multilevel converter or cascaded H-bridge.

While both MMC and CHB are considered as the modular branch of Figure 2.1, this research focuses on the CHB topology for several reasons. The CHB is better for battery integration because it provides higher efficiency, smaller number of modules and semiconductors. Studies in [23] show that for a given voltage level, the MMC needs more active components than the CHB. This increased number of components and control complexities make the MMC less ideal for this study's primary objective. Besides, the CHB architecture offers better battery handling, which is essential for large-scale storage [27].

Another challenge of the MMC is the presence of circulating currents within its phase arms. As confirmed by [28]. The circulating current has double-line frequency components that increase the peak arm current and power losses. It is necessary to eliminate these currents to ensure stable operation. Since the CHB does not possess common DC-bus arms, it inherently avoids this specific type of internal loss and the

associated control complexities. The CHB is also chosen for its high-quality output. As noted by [29], the CHB topology has the advantage of generating an output voltage with extremely low harmonic distortion.

For this research, a symmetrical star-connected CHB (YCHB) configuration is employed. The YCHB is advantageous because its phase clusters are rated at line-to-neutral voltage, which allows for both a reduction in the number of power cells and the use of semiconductors with lower blocking voltage ratings compared to a delta configuration [14]. Furthermore, the star connection simplifies the system by avoiding the internal circulating currents that must be actively managed in delta-connected structures.

Although the CHB topology provides an effective modular grid interface, it does not inherently offer galvanic isolation or voltage adaptation between battery modules and inverter DC links. These functions are essential in medium-voltage systems for both protection and system integration. To address this limitation, an isolated DC-DC conversion stage is introduced between the battery modules and the CHB submodules. This architecture directly aligns with the principles of solid-state transformer systems, enabling galvanic isolation, bidirectional power flow, and flexible voltage control.

2.2 System Architecture

The architecture of the proposed MMC-based converter is shown in Fig. 2.2. The system architecture follows a modular, multi-stage conversion process designed to scale power and voltage while providing galvanic isolation. The primary energy input consists of a central DC bus, acting as the collection point for renewable energy sources. This common DC bus serves as the input to a single-primary, multi-secondary DAB assembly. The configuration utilizes a high-power primary H-bridge that drives a multi-winding high frequency transformer. This arrangement splits the 10 MW total power into multiple isolated secondary paths. Each secondary path consists of a full H-bridge module that rectifies the high-frequency AC power to charge a dedicated DC-link capacitor.

These capacitors function as independent, isolated DC voltage sources for the grid-interfacing stage. The final conversion to the 10 kV AC grid is performed by a CHB inverter. In this stage, the inverter modules are connected in series per phase to reach their individual output voltages. To ensure power quality and meet grid standards, an output filter is placed in output stage to smooth the multilevel voltage waveforms. The following sections provide the detailed mathematical design and parameter selection for the CHB and DAB stages to further explain the implementation of this system.

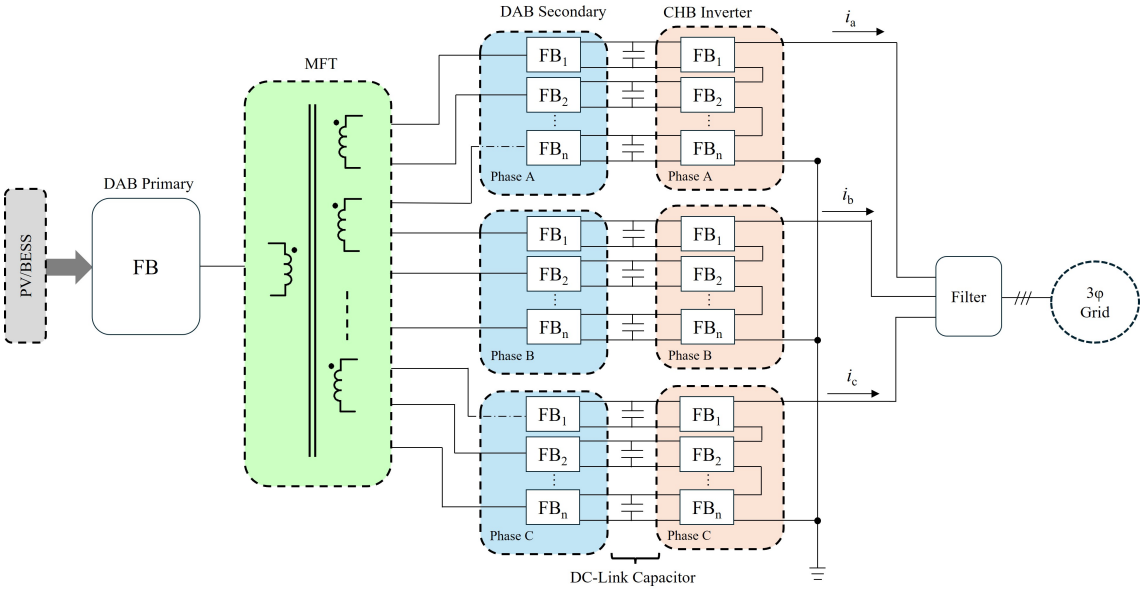

Figure 2.2: Selected MMC-based converter.

2.2.1 Cascaded H-Bridge Converter Design

For a 10 MW, 10 kV system, the design must ensure that the cascaded series of modules can withstand the peak grid voltage while maintaining a safe operating margin for the power semiconductors. To achieve this, we utilize a full H-bridge module as the primary building block for cascading, following the detailed design parameters outlined below.

2.2.1.1 The Fundamental H-Bridge Module

The fundamental building block of the CHB topology is the single-phase full-bridge module, as shown in Fig. 2.3. Each module consists of four active switches arranged in two phase-legs connected to a DC source. The top and bottom switches within each phase leg are operated in a complementary manner to avoid short-circuiting the DC source. By controlling the switching states of these legs, each H-bridge module generates a three-level output voltage v_o of $+V_{dc}$, 0, or $-V_{dc}$. The possible output voltage levels and their corresponding switch combinations are illustrated in Table 2.1, where logic "0" and "1" denote the OFF and ON states of the switches, respectively.

The relationship between the DC-link voltage and the output voltage of a single H-bridge module is defined by:

$$v_o = (S_{11} - S_{12})V_{dc} \tag{2.1}$$

Where S_{11} and S_{12} represent the switching states of the upper switches in the two phase legs. Extending this concept, a cascaded H-bridge rectifier or inverter is constructed by series-connecting multiple H-bridge modules, allowing the generation of higher voltage levels with reduced device voltage stress and improved output

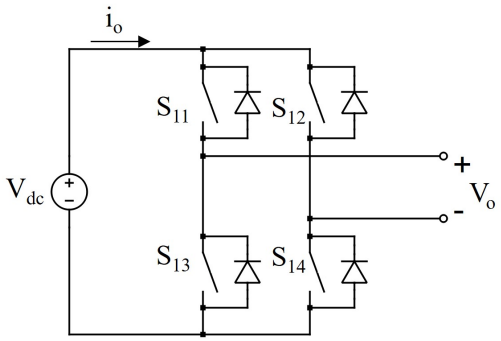

Figure 2.3: Basic structure of H-Bridge converter.

waveform quality. In the context of the 10 MW system considered in this research, multiple H-bridge modules are cascaded per phase to synthesize the required output voltage. Each module must therefore be designed to withstand high current and voltage stresses while maintaining electrical insulation, thermal stability, and reliable long-term operation.

Table 2.1: H-bridge Converter Switching Combinations.

S_{11}	S_{12}	V_o	i_o
0	0	0	0
1	0	V_{dc}	i_o
0	1	-V_{dc}	$-i_o$
1	1	0	0

2.2.1.2 Required Total DC Voltage

To ensure proper current control and linear modulation, the total DC-link voltage for each phase ($V_{dc,\text{total}}$) must be higher than the peak of the grid voltage. This additional voltage margin acts as a buffer, allowing the converter to inject power into the grid even when the AC voltage reaches its maximum value. Assuming a star-connected interface to the grid, the corresponding RMS phase voltage is given by:

$$V_{ph,\text{rms}} = \frac{V_{LL}}{\sqrt{3}} = \frac{10{,}000}{\sqrt{3}} \approx 5773.5 \text{ V}. \tag{2.2}$$

Where V_{LL} denotes the line-to-line RMS grid voltage. The DC-link voltage must be sized to cover the peak value of the phase voltage ($\sqrt{2}\,V_{ph,\text{rms}}$). In addition, a modulation index $m = 0.8$ is selected to provide sufficient operating margin.
This choice is motivated by two considerations:

- It provides approximately 20% voltage headroom to accommodate grid disturbances and voltage drops across passive components.
- It ensures operation within the linear modulation range, enabling low-distortion waveform synthesis.

Using $m = 0.8$, the required total DC-link voltage per phase is then calculated as:

$$V_{dc,\text{total}} = \frac{\sqrt{2}\, V_{ph,\text{rms}}}{m} = \frac{\sqrt{2} \cdot 5773.5}{0.8} \approx 10.2 \text{ kV}. \tag{2.3}$$

This value represents the sum of the individual DC-link voltages of all cascaded H-bridge modules within one phase. If the available DC-link voltage were lower than the grid voltage peak, the converter would be unable to properly regulate the output current, resulting in degraded power quality and loss of controllability.

2.2.1.3 Maximum Operating Voltage per Module

Semiconductor devices cannot be operated at their full rated blocking voltage (V_{rat}) due to risks associated with switching transients and temperature fluctuations. To ensure reliable operation, a Utilization Factor (UF) is employed to define the safe steady-state DC operating voltage of each H-bridge module ($V_{dc,op}$).
The operating voltage is calculated as:

$$V_{dc,op} = V_{rat} \cdot UF \tag{2.4}$$

For SiC MOSFETs, a UF of 0.7 is commonly adopted, meaning only 70% of the device's voltage rating is utilized for the DC-link operating point of each individual H-bridge cell. For the standard voltage classes considered in this study, the corresponding safe operating voltages are defined as follows.
For 1.7 kV switches:

$$V_{dc,op,1.7} = 1700\,\text{V} \cdot 0.7 = 1190\,\text{V} \tag{2.5}$$

For 3.3 kV switches:

$$V_{dc,op,3.3} = 3300\,\text{V} \cdot 0.7 = 2310\,\text{V} \tag{2.6}$$

These values represent the maximum allowable DC operating voltage of each individual H-bridge module within the cascaded structure. The total phase-level DC voltage is obtained by summing the operating voltages of all series-connected H-bridge cells, and directly determines the number of required sub-modules per phase for a given grid voltage level.

2.2.1.4 Calculation of the Number of Cascaded Modules

The number of modules per phase is determined by dividing the total required phase voltage by the operating capacity of a single module. Since a fractional number of modules cannot be implemented, the ceiling function ($\lceil\rceil$) is used to round up to the nearest integer:

$$N_{SM} = \left\lceil \frac{V_{dc,total}}{V_{dc,op}} \right\rceil \tag{2.7}$$

For a case study comparison involving a total required DC-link voltage of 10.2 kV, the results are as follows:
For the 1.7 kV design:

$$N_{SM,1.7} = \left\lceil \frac{10.2\,\text{kV}}{1190\,\text{V}} \right\rceil = \lceil 8.57 \rceil = 9 \text{ modules} \tag{2.8}$$

For the 3.3 kV design:

$$N_{SM,3.3} = \left\lceil \frac{10.2\,\text{kV}}{2310\,\text{V}} \right\rceil = \lceil 4.41 \rceil = 5 \text{ modules} \tag{2.9}$$

To reach the total required output voltage for the 10 MW system, these modules must be connected in a series-cascaded configuration. This cascading arrangement allows the converter to build the high-voltage grid waveform by adding the individual output voltages of each connected H-bridge. Once the number of modules (N_{SM}) is fixed at 9 and 5 respectively, the exact DC-link voltage for each H-bridge module (V_{dc}) is recalculated. This ensures that the sum of the voltages exactly matches the target $V_{dc,total}$ required for the 10 kV grid interface:

$$V_{dc,1.7} = \frac{V_{dc,total}}{N_{SM,1.7}} = \frac{10.2}{9} = 1133V \tag{2.10}$$

$$V_{dc,3.3} = \frac{V_{dc,total}}{N_{SM,3.3}} = \frac{10.2}{5} = 2000V \tag{2.11}$$

These specific DC-link voltage values are essential parameters for the design and calculation of the DAB isolation stage, which will be detailed in the next section.

2.2.2 Isolated DAB Converter Design

The passive components of the DC/DC stage are dimensioned to ensure that the system can handle the rated 10 MW total power while maintaining stable DC voltages with minimal ripple. Two critical factors in this design are the transformer turns ratio (n) and the leakage inductance (L_{lk}), which are selected to achieve the desired power transfer characteristics and facilitate zero-voltage switching (ZVS). ZVS is essential at the selected switching frequency of 5 kHz to minimize switching losses and reduce thermal stress on the SiC-based H-bridge modules. In addition, the DC-side capacitors are sized to limit voltage ripple and support transient power imbalance during dynamic operating conditions. The coordinated design of the transformer parameters, leakage inductance, and DC-link capacitance ensures efficient and reliable operation of the isolated DAB converter.

2.2.2.1 Zero Voltage Switching

The transformer turns ratio n, defined as the ratio of primary to secondary turns N_p/N_s, is a critical design factor used to match the primary DC bus to the isolated secondary DC links. These specific ratios are chosen to ensure that the reflected secondary voltage (V_s) matches the primary source (V_p), such that $nV_s = V_p$. This alignment is vital for achieving ZVS, as it allows the converter to operate near the unity voltage conversion ratio. By operating at this point, reactive power circulation is minimized and the energy stored in the leakage inductance is optimized to discharge the switch capacitances. This allows the system to maintain high efficiency and reduces thermal stress, even when operating at a high switching frequency of 5 kHz.

2.2.2.2 Leakage Inductance Calculation

The leakage inductance is the primary energy transfer element within the DAB stage. From a fundamental viewpoint, the DAB converter can be represented by two AC voltage sources, generated by the primary and secondary bridges, connected through a total series inductance L_{lk}. This inductance consists of the transformer leakage inductance and any additional auxiliary inductors. The instantaneous current through L_{lk} is driven by the voltage difference between the two bridges and is controlled by the phase shift between their switching functions.
The average power transferred by the DAB converter over one switching period can be expressed as:

$$P = \frac{nV_pV_s}{2f_{sw}L_{lk}}\,\theta\left(1 - \frac{|\theta|}{\pi}\right), \tag{2.12}$$

Where:

- V_p is the primary (input) DC-link voltage.
- V_s is the secondary (output) DC-link voltage.
- n is the transformer turns ratio (N_p/N_s).
- f_{sw} is the DAB switching frequency.
- L_{lk} is the total leakage inductance referred to the primary side.
- θ is the phase shift between the two bridges.

The maximum transferable power occurs at a phase shift of $\theta = \pi/2$, corresponding to the peak of the power-transfer characteristic. Substituting this condition into the above expression yields the maximum power relationship, from which the required leakage inductance can be derived as

$$L_{lk} = \frac{nV_pV_s}{8f_{sw}P_{max}}. \tag{2.13}$$

By substituting the design parameters into the above expression and applying the safety factor, the required leakage inductance is obtained as 77.76 μH. This value is selected for both the 1.7 kV and 3.3 kV systems, since the DAB modules are designed to transfer the same per-module power at identical switching frequency and primary DC voltage. Consequently, despite the different device voltage ratings and transformer turns ratios, the maximum-power condition leads to the same effective leakage inductance requirement in both cases.

2.2.2.3 DC-Link Capacitance Calculation

The capacitor is sized to limit the voltage ripple to 3% ($\Delta V = 0.03 \cdot V_s$) to maintain a stable DC input for the cascaded inverter stage. The calculation is based on the nominal DC current and the switching frequency.
The nominal DC current is calculated as:

$$I_{dc} = \frac{P_{sec}}{V_s} \tag{2.14}$$

The required capacitances for both systems are:

$$C_{dc,1.7} = \frac{I_{dc,1.7}}{(\Delta V_{1.7} \cdot f_{sw})} = 1.92\text{mF} \tag{2.15}$$

$$C_{dc,3.3} = \frac{I_{dc,3.3}}{(\Delta V_{3.3} \cdot f_{sw})} = 1.11\text{mF} \tag{2.16}$$

These calculated values ensure that the DC-link voltage remains stable under full load conditions, providing the necessary energy buffer for the secondary H-bridge modules. The following table provides a comprehensive overview of the DAB and CHB stage parameters used for the system implementation.

Table 2.2: Design parameters for MMC-based converter implementation.

Parameter	1.7 kV System	3.3 kV System
Grid Power (P)	10 MW	10 MW
Grid Voltage (V_{LL})	10 kV	10 kV
DAB Primary Voltage (V_p)	1200 V	1200 V
DAB Secondary Voltage (V_s)	1133 V	2000 V
Number of Cascaded Modules (N_{SM})	9	5
Transformer Turns Ratio (n)	1.06	0.6
CHB Switching Frequency ($f_{sw,CHB}$)	1 kHz	1 kHz
DAB Switching Frequency ($f_{sw,DAB}$)	5 kHz	5 kHz
Leakage Inductance (L_{lk})	77.76 μH	77.76 μH
DC-Link Voltage Ripple (ΔV)	3%	3%
DC-Link Capacitance (C_{dc})	1.92 mF	1.11 mF

3

Control Strategy

3.1 Introduction

The primary objective of a modulation is to translate control references into precise gate signals for the power semiconductors. The choice of modulation directly impacts system efficiency, thermal stress on the devices, and the THD of the output voltage. As shown in Fig 3.1, modulation techniques for power converters are categorized based on their switching frequency, as described in the reviews by [25, 30].

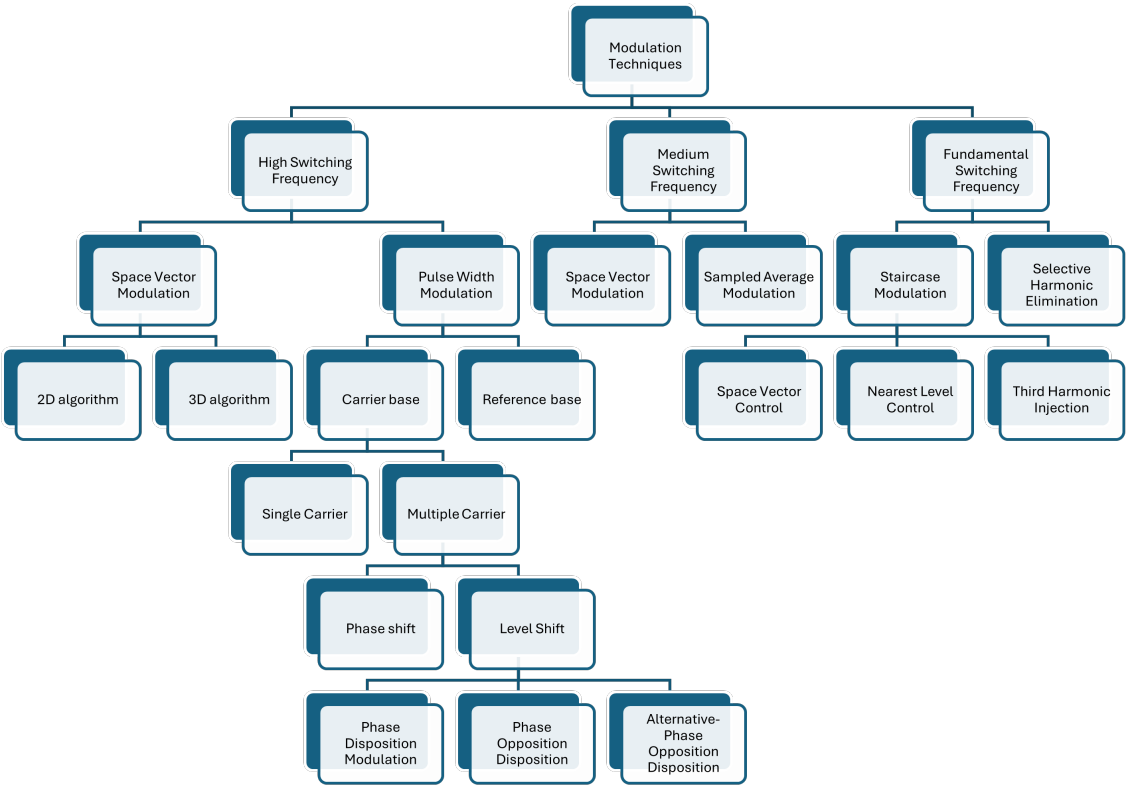

Figure 3.1: Classification of modulation techniques based on switching frequency.

For high-performance grid-connected systems, a two-layer control architecture is employed. The high-level regulation is performed using *dq* control, which transforms three-phase AC variables into a synchronous rotating reference frame. This transformation allows for the independent (decoupled) regulation of active and reactive power by treating AC quantities as DC signals. The resulting voltage references

generated by this *dq* controller are then processed by the modulation stage.

For power converters, high-frequency carrier-based PWM is the industry standard for controlling numerous power cells simultaneously. Within this category, Phase-Shifted PWM (PS-PWM) and Level-Shifted PWM (LS-PWM) are the most popular methods, offering an optimal balance between switching efficiency and power quality. While LS-PWM offers several advantages such as easy implementation and waveform quality improvement [25], it needs precise synchronization among carriers which increases the complexity of the control software [31].

In this research, PS-PWM is selected for the control of star-connected CHB system to reach a 10 kV system voltage because of its good performance in modular architectures. According to [32], PS-PWM is adopted to suppress the current ripple, because it uses a framework in which the carrier of each module is independent. This independency of carriers is a significant advantage as it ensures the system can maintain the output performance when module fault occurs. Moreover, PS-PWM facilitates an even distribution of power among the submodules (SMs) [33]. This uniform distribution is critical for preventing localized thermal stress and ensuring balanced aging of the submodules.

While the *dq* controller and PS-PWM handle the inverter stage, the DAB converter in the SST isolation stage requires a robust closed-loop controller to maintain a stable DC-link voltage. The closed loop control in the isolation phase is used to maintain the DC output voltage at a constant value. To evaluate these strategies, the full power converter and required controllers are modeled in simulation software as illustrated in the system architecture in Fig 3.2. The model incorporates two dedicated control systems—one for DAB and another for CHB—both of which are analyzed in technical detail in the following sections.

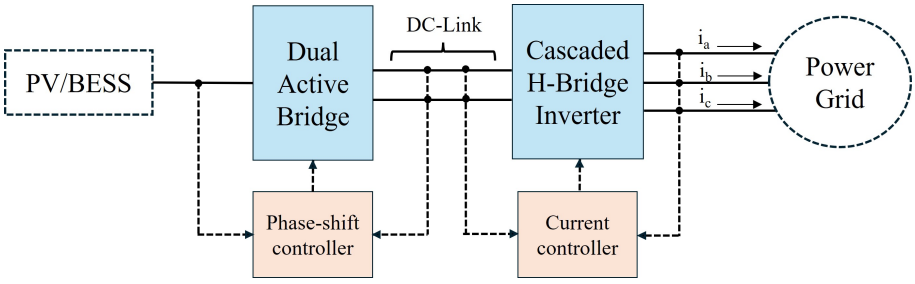

Figure 3.2: Overview of the control system structure.

3.2 CHB Control Implementation

The CHB converter acts as the power electronics interface between the high-frequency isolation stage and grid. In this architecture, the DC-link voltage of each cell is regulated and maintained at a fixed value by DAB stage. Consequently, the CHB control system focuses exclusively on grid current and power factor correction.

3.2.1 Synchronous Reference Frame (dq) Current Control

The control is implemented in the synchronous rotating reference frame (dq frame). This approach is preferred because it transforms sinusoidal grid variables into DC quantities, allowing the use of standard PI controllers to achieve zero steady-state error. The grid dynamics in the abc frame can be described by:

$$v_{s,abc} = Ri_{abc} + L\frac{d}{dt}i_{abc} + v_{conv,abc} \tag{3.1}$$

By applying the Park transformation, the dynamics in the dq frame become:

$$v_{sd} = Ri_d + L\frac{di_d}{dt} - \omega Li_q + v_d \tag{3.2}$$

$$v_{sq} = Ri_q + L\frac{di_q}{dt} + \omega Li_d + v_q \tag{3.3}$$

Where v_{sd}, v_{sq} are the grid voltages, v_d, v_q are the converter output voltages, and ωLi represents the cross-coupling terms. To decouple these axes and ensure high-performance tracking, the control laws for the reference voltages v_d^* and v_q^* are defined as:

$$v_d^* = v_{sd} + \omega Li_q - \left(K_p + \frac{K_i}{s}\right)(i_d^* - i_d) \tag{3.4}$$

$$v_q^* = v_{sq} - \omega Li_d - \left(K_p + \frac{K_i}{s}\right)(i_q^* - i_q) \tag{3.5}$$

The three-phase grid currents (i_{abc}) are measured and converted to the stationary $\alpha\beta$ frame using the Clarke transformation, and subsequently to the rotating dq frame using the Park transformation. To ensure precise synchronization with the grid, a Phase-Locked Loop (PLL) is utilized to track the grid voltage angle (θ). The PLL operates by continuously adjusting its internal frequency to match the grid's phase, thereby extracting the fundamental frequency and phase required for accurate coordinate transformations.
Two independent PI controllers are used to regulate the d and q components of the current:

- The d-axis reference (i_d^*) is set based on the desired active power exchange with the grid. Since the DC-link voltage is regulated by DAB stage, the CHB controller treats the DC bus as a fixed-voltage source.
- The q-axis reference (i_q^*) is typically set to zero to ensure unity power factor operation.

To decouple the d and q dynamics and improve tracking performance, feed-forward terms ($l\omega i$) and grid voltage compensation (v_{dq}) are added to the PI controller outputs. The resulting reference voltages v_d^* and v_q^* are then transformed back to the abc frame (v_{abc}^*) to serve as the modulating signals. Once the reference voltage v_{abc}^* is generated, it is normalized by the total available DC-link voltage to produce the three-phase modulation indexes m_a, m_b and m_c:

$$m_{abc} = \frac{v_{abc}^*}{n_{cell} \cdot V_{dc}} \tag{3.6}$$

Where; n_{cell} is the number of cells per phase and V_{dc} is the average voltage of a single DC link. These modulating signals are used to compare with carriers to generate the gate pulses for the CHB sub-modules, a process which is explained in detail in the next section. A comprehensive block diagram showing the implemented *dq* current control strategy is presented in Fig 3.3. The figure provides a detailed overview of the control flow, starting from the sensory input to the final modulation signals.

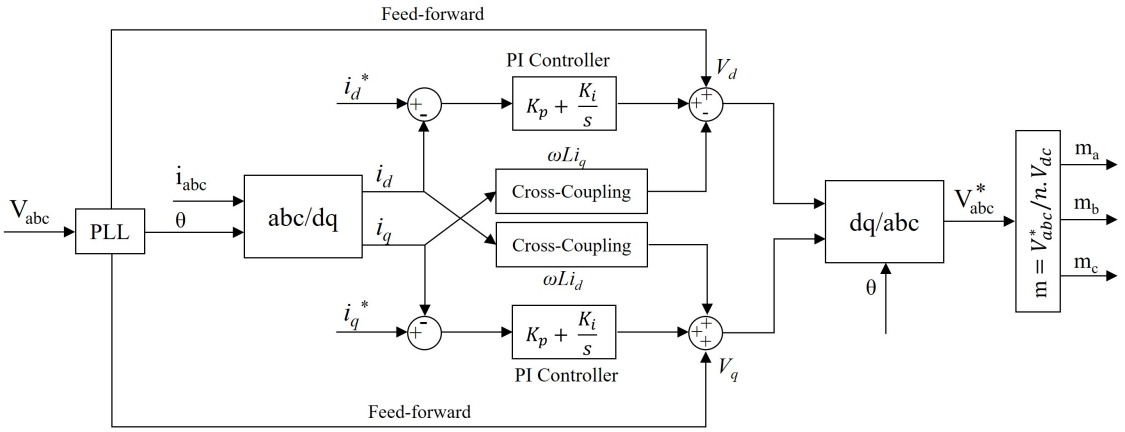

Figure 3.3: Block diagram of the *dq* current control structure.

3.2.2 Phase-Shifted PWM Mathematical Implementation

In PS-PWM, each cell i (where $i = 1, 2, \ldots, n$) compares generated modulation indexes with dedicated triangular carriers (C_i). The phase shift θ_i for each carrier is mathematically defined as:

$$\theta_i = (i-1)\frac{180^\circ}{n_{cell}} \tag{3.7}$$

For each H-bridge cell, a unipolar switching strategy is employed to effectively double the apparent switching frequency. As illustrated in Fig 3.4, this is achieved by comparing the modulation signal m_a and its inverse $-m_a$ against the same triangular carrier $C_i(\theta_i)$. This generates the gate pulses for the two H-bridge legs ($S_{i,L1}$ and $S_{i,L2}$):

$$S_{i,L1} = \begin{cases} 1 & \text{if } m_a > C_i(\theta_i) \\ 0 & \text{if } m_a \leq C_i(\theta_i) \end{cases} \tag{3.8}$$

$$S_{i,L2} = \begin{cases} 1 & \text{if } -m_a > C_i(\theta_i) \\ 0 & \text{if } -m_a \leq C_i(\theta_i) \end{cases} \tag{3.9}$$

The logical operation described in Equations (3.8) and (3.9) is illustrated in Fig 3.4. As shown, the switching state for each leg is determined by a simple comparison: when the modulation signal is higher than the carrier, the leg state is 1; otherwise, it is 0. During the positive half-cycle, m_a is frequently higher than the carrier while $-m_a$ remains mostly below it, whereas during the negative half-cycle, $-m_a$ is higher

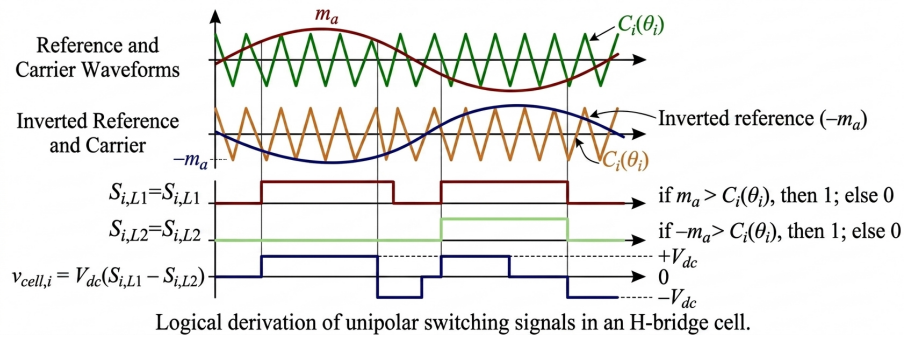

Figure 3.4: Logical derivation of unipolar switching signals in H-bridge module.

more often. The resulting output voltage of a single cell is defined by the difference between these two leg states:

$$v_{cell,i} = V_{dc}(S_{i,L1} - S_{i,L2}) \tag{3.10}$$

By subtracting the signals in this manner, the output voltage pulses between 0 and $+V_{dc}$ during the positive half-cycle and between 0 and $-V_{dc}$ during the negative half-cycle. This unipolar switching ensures that the voltage only transitions between adjacent levels, avoiding direct jumps between $+V_{dc}$ and $-V_{dc}$. This specific implementation effectively doubles the switching frequency at the cell level ($2 \cdot f_{sw}$) due to the harmonic cancellation between the two legs. When expanded to a CHB configuration with n submodules per phase, the phase-shifted carriers provide additional harmonic interleaving. This leads to an effective output switching frequency (f_{eff}) for the total phase leg of:

$$f_{\text{eff}} = 2 \cdot n_{cell} \cdot f_{\text{sw}} \tag{3.11}$$

The practical implementation of the PS-PWM stage is depicted in Fig 3.5. This diagram shows the transition from the control references to the physical switching commands for the n H-Bridge cells.

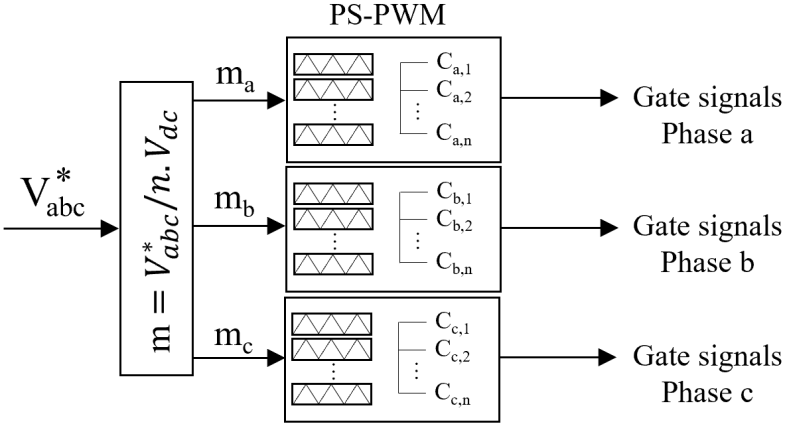

Figure 3.5: Block diagram of the Phase-Shifted PWM generation stage.

3.2.3 CHB Controller Tuning

The current controller gains are initially estimated using the Internal Model Control (IMC) tuning method. For a first-order RL plant consisting of the grid filter inductance and resistance, the PI controller transfer function $G_c(s) = K_p + \frac{K_i}{s}$ is designed to cancel the plant pole. Under the IMC framework, the gains are calculated as:

$$K_p = \frac{L_f}{\tau} \tag{3.12}$$

$$K_i = \frac{R_f}{\tau} \tag{3.13}$$

Where:

- L_f is the grid filter inductance.
- R_f is the equivalent series resistance of the filter.
- τ is the desired closed-loop time constant.

While the IMC method provides a systematic starting point, the final gains used in the simulation were reached through trial-and-error manual tuning. This adjustment was necessary because the standard IMC formula (typically using $\tau \approx 10/f_{sw}$) does not fully account for the high effective switching frequency (f_{eff} = 18 kHz) and the discrete-time delays inherent in a multi-level CHB configuration. The manual increase of K_i ensures a faster elimination of steady-state error, while the chosen K_p optimizes the transient response without inducing oscillations. The specific design parameters and the final tuned controller gains for both SiC-based implementations are summarized in Table 3.1.

Table 3.1: CHB dq current controller parameters.

Parameter	1.7 kV SiC System	3.3 kV SiC System
Filter Inductance (L_f)	2 mH	2 mH
Filter Resistance (R_f)	4 $m\Omega$	10 $m\Omega$
Proportional Gain of CHB controller (K_{pc})	1	4
Integral Gain of CHB controller (K_{ic})	10	10

3.3 DAB Control Implementation

The dual active bridge converter provides the necessary galvanic isolation and voltage regulation within the system. In this architecture, the primary role of the DAB is to provide a fixed and stable DC-link voltage for the subsequent CHB inverter stage. The power flow between the primary and secondary bridges is managed using the Single Phase Shift (SPS) modulation technique, which is described in the following subsections.

3.3.1 Single-Phase Shift Modulation Logic

In SPS control, all semiconductor switches in both the primary and secondary H-bridges are operated with a fixed 50% duty cycle. This results in two high-frequency

square wave voltages, V_p and V_s, being applied to the primary and secondary terminals of the high-frequency transformer, respectively.

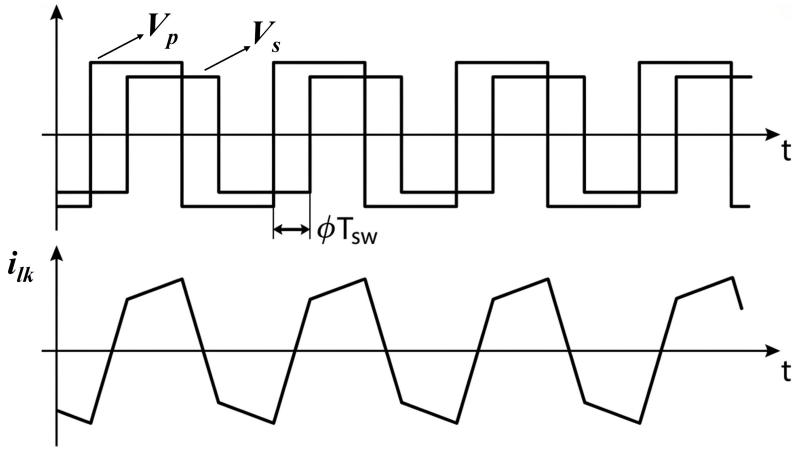

Figure 3.6: Operating waveforms of the DAB converter under single phase shift modulation: (a) Primary voltage V_p; (b) Secondary voltage V_s; and (c) Transformer leakage inductor current I_{lk}.

As shown in Fig 3.6, the phase shift ϕ is measured as the horizontal displacement between the corresponding transitions of v_p and v_s. The primary control variable is the phase shift ratio (d), which represents the normalized displacement between the primary and secondary voltage waveforms. This ratio is defined as:

$$d = \frac{\phi}{\pi} \tag{3.14}$$

Where ϕ is the phase shift angle in radians. The value of d typically ranges from -0.5 to 0.5. The sign of d determines the direction of power flow: a positive value denotes power transfer from the primary to the secondary side, while a negative value indicates reverse power flow. From a circuit perspective, the phase shift creates a voltage difference across the transformer's leakage inductance (L_{lk}). During the interval ϕ, the instantaneous voltage across the inductor is $(V_p + nV_s)$, causing the leakage current L_{lk} to rise or fall linearly. The amount of energy stored and subsequently transferred depends entirely on this displacement.

3.3.2 Closed-Loop Phase-Shift Controller

To ensure the CHB stage receives a constant supply, a closed-loop controller is implemented to fix V_s at the required DC-link reference. The relationship between the phase shift d and the transmitted power P is non-linear but remains monotonic within the standard operating range of $|d| \leq 0.5$.
The controller adjusts d dynamically based on the following dynamics:

- **Increasing d:** Expands the interval where the primary and secondary voltages have opposite polarities. This enhances the energy stored in the leakage inductor L_{lk} during the overlap period, thereby increasing the active power transfer to support the CHB load.

- **Zero Phase Shift ($d = 0$):** Represents the condition where the primary and secondary square waves are perfectly aligned. This results in zero active power transfer, as the instantaneous voltage across the leakage inductance is minimized throughout the cycle.
- **Maximum Power:** The theoretical power limit occurs at $|d| = 0.5$. Operating beyond this limit is generally avoided as it leads to a decrease in active power while significantly increasing reactive power circulation and current stress, which degrades system efficiency.

The overall control architecture for this stage is depicted in Fig 3.7. The controller continuously monitors the secondary DC-link voltages of H-bridge modules and compares them against the desired reference $V_{dc,ref}$. The resulting error is processed through a PI controller to generate the required phase shift ratio d, which is then converted into gate signals for the H-bridges. This closed-loop mechanism ensures precise regulation and rapid recovery during load transients.

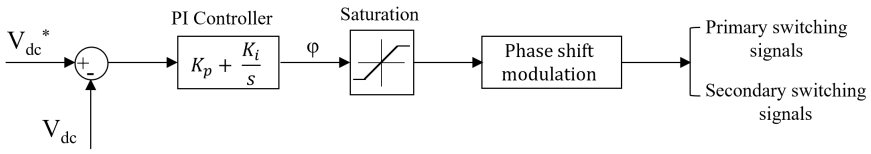

Figure 3.7: Block diagram of closed-loop phase-shift control structure.

3.3.3 DAB Controller Tuning

The tuning process specifically targets a crossover frequency significantly lower than the switching frequency ($f_{sw} = 5$ kHz) to avoid interference with the high-frequency sampling ripples. In DAB systems, the plant's gain effectively changes depending on the DC-link voltage levels; therefore, the controller must be robust enough to handle the non-linear power-to-phase-shift curve. While analytical methods provide a solid theoretical baseline, they often result in conservative gains that lead to a slow recovery time during the rapid load transients characteristic of CHB switching. The final parameters used for both the 1.7 kV and 3.3 kV SiC-based systems are summarized in Table 3.2.

Table 3.2: DAB phase-shift controller parameters.

Parameter	1.7 kV SiC System	3.3 kV SiC System
Proportional Gain of DAB controller (K_{pd})	0.5	0.001
Integral Gain of DAB controller (K_{id})	0.05	0.05

In summary, the coordinated control of the DAB and CHB stages ensures that the SST operates with high efficiency and superior power quality. While the DAB controller maintains a stiff DC bus through closed-loop voltage regulation and soft-switching, the CHB controller utilizes a decoupled dq current control scheme to interface with the 10 kV grid at unity power factor. The combination of PS-PWM for

the inverter and SPS modulation for the isolation stage provides a robust framework for comparing the performance of 1.7 kV and 3.3 kV SiC MOSFET technologies in high-power applications.

4

Simulation & Results

The simulation is carried out in PLECS, where the solid-state transformer topology—incorporating the dual active bridge, cascaded H-bridge, and grid interface—is modeled. For the electro-thermal analysis, CAB650M17HM3 and CAB600M33LM3 SiC power modules are used to represent the switching devices. The electrical characteristics, switching energies, and thermal parameters of these devices are defined according to the manufacturer specifications reported in [34, 35]. Using realistic switch models ensures that the simulated conduction losses, switching losses, and thermal behavior accurately represent practical device performance.

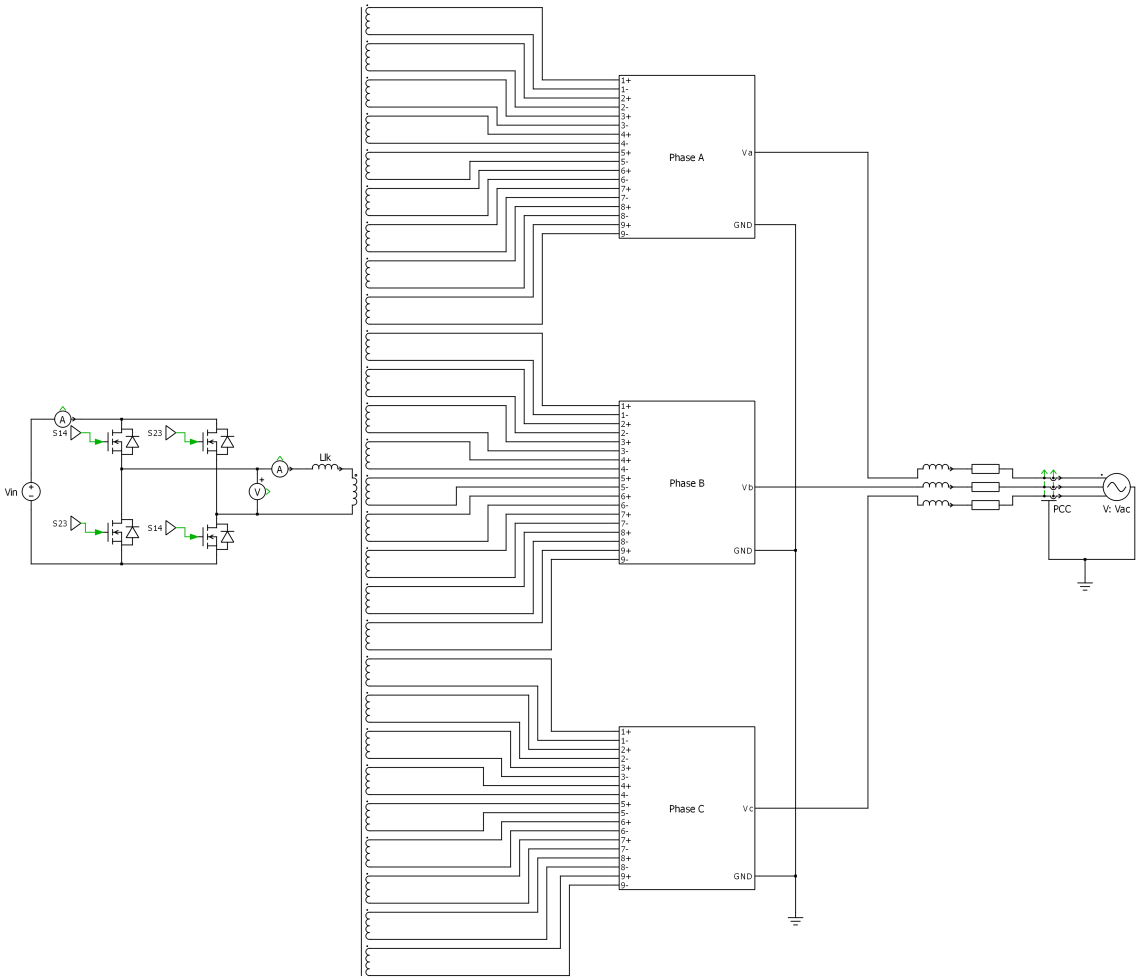

Figure 4.1: Simulink model.

4.1 System Performance

In this study, the SST is modeled using two different switch ratings to compare their impact on performance. The primary side of the DAB is identical for both systems, utilizing 1.7 kV switches. However, the secondary side of the DAB and the CHB stages are separately designed to use 1.7 kV and 3.3 kV switches, as discussed in the following sections. While the overall topology remains the same as shown in Fig. 4.1, the modular configuration is adjusted for each case: the 1.7 kV system utilizes 9 cascaded modules per phase with DC voltage of 1133 V, whereas the 3.3 kV system is designed with 5 cascaded modules per phase with DC voltage of 2000 V. The active power of 10 MW is transferred from the DAB H-bridge through the multi-winding high-frequency transformer and distributed to the phase-level CHB modules, which interface with the grid through the output filter and provide 10 kV line to line rms voltage at PCC.

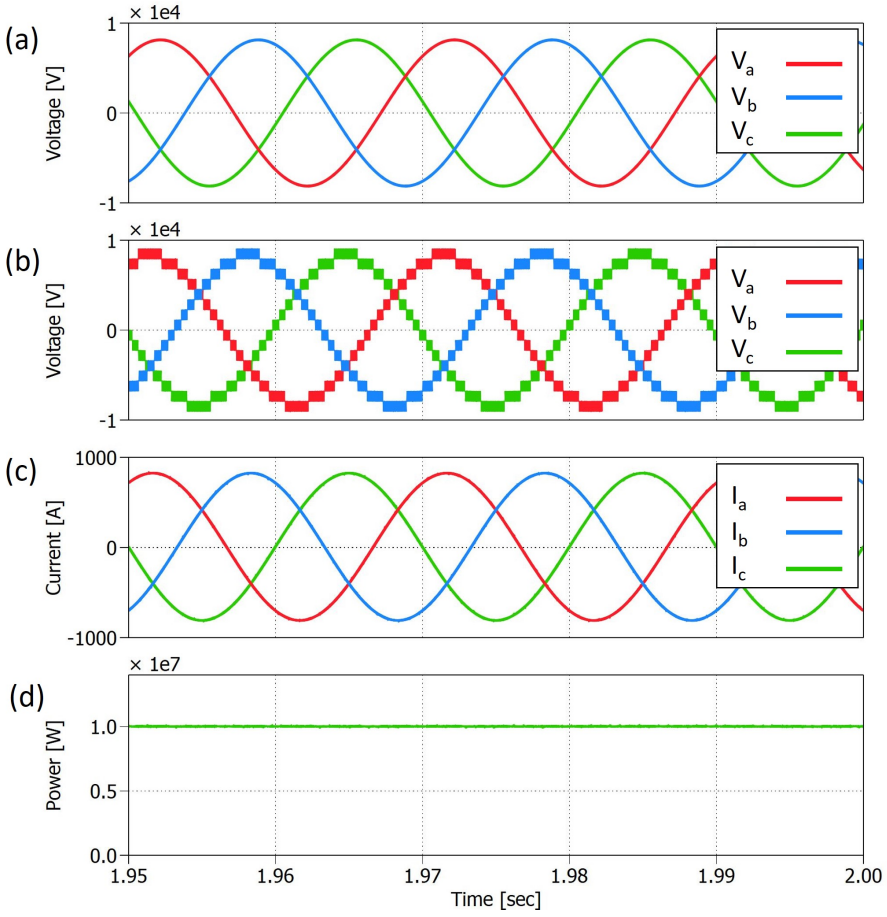

Figure 4.2: Steady-state output performance under nominal conditions while delivering 10 MW power to the grid: (a) Grid voltage; (b) Inverter voltage (c) Grid current and (d) Grid power.

4.1.1 Case A: System design using 1.7 kV SiC MOSFET

The output voltage and current waveforms, presented in Fig. 4.2 (a) and (c), shows minimal ripple and stable synchronization, validating the effectiveness of the system design. It can be observed that the system delivers a line-to-line output voltage of approximately 10 kV, while Fig. 4.2 (d) shows the delivery of a total active power of 10 MW under nominal operating conditions. The three-phase 19-level inverter voltage waveforms at the converter terminals are shown in Fig. 4.2 (b). This high number of levels is achieved through the cascaded H-bridge stages, resulting in a waveform that closely approximates a sine wave even before any filtering is applied. At the Point of Common Coupling (PCC) connection to the grid, the system demonstrates excellent power quality. The voltage THD is effectively 0%, while the current THD is as low as 0.27%.

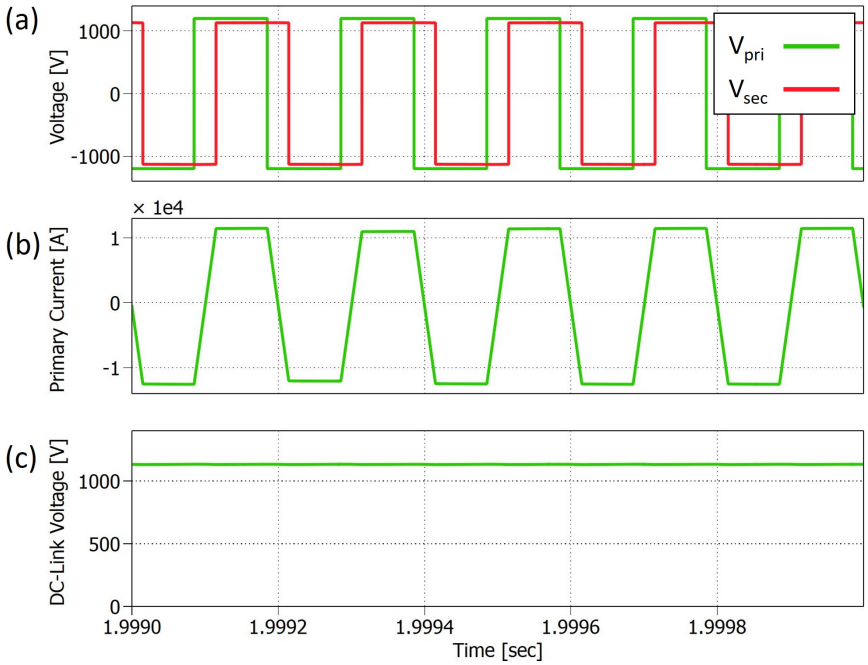

Figure 4.3: DAB simulation results with one of the cell units at the secondary side: (a) Primary and secondary side voltages; (b) Primary current; and (c) Output DC-link voltage waveforms.

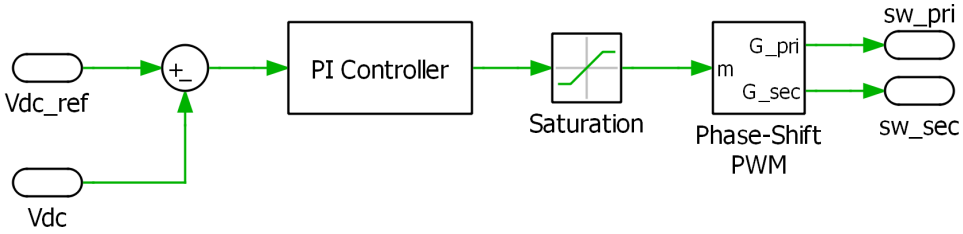

Figure 4.4: Closed-loop phase-shift controller of the DAB.

The isolation stage provides critical insight into the transformer utilization. The DAB input voltage, output voltage, primary side current, and dc-link voltage are displayed in Fig. 4.3. The dc-link voltage is maintained at 1133 V, ensuring stable operation and proper voltage levels for the subsequent cascaded stages. The inductor current waveform, in particular, confirms the accuracy of the phase-shift command generated by the DAB controller. Depending on the specific power transfer requirements, the controller dynamically calculates and adjusts this phase shift between the primary and secondary bridges to regulate energy flow with high precision. By modulating this phase angle, the system maintains the 1133 V dc-link provided by the real device parameters of the SiC modules. These results confirm that the SST architecture successfully meets the design specifications for grid-tied power conversion.

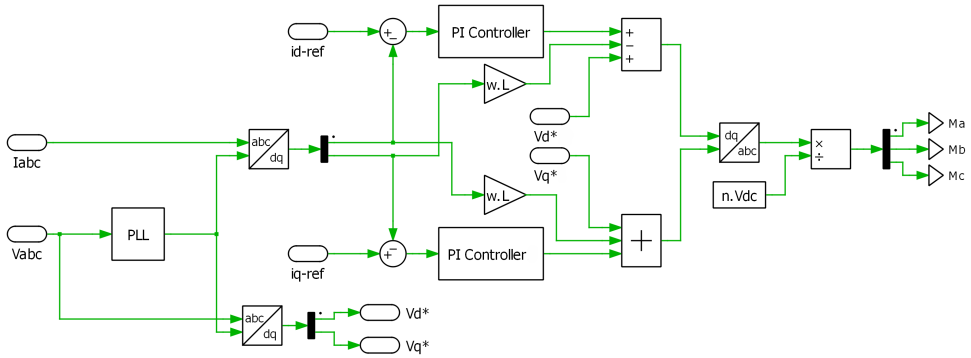

Figure 4.5: Closed-loop dq-axis current controller of the CHB with grid synchronization.

The precise regulation of system parameters is maintained by the control strategies implemented for the DC/DC and DC/AC stages. The implementation of DAB and CHB controllers is shown in Figs. 4.4 and 4.5, respectively. These figures detail the control loops and PWM generation logic required to manage the system operation.

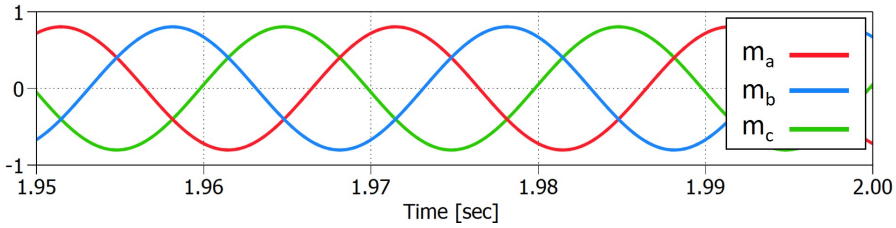

Figure 4.6: Three-phase modulation signals produced by CHB controller.

The control strategy is demonstrated through the interaction between the modulation signals and the carriers. Figs. 4.6 shows the three-phase modulation signals, which are the output of the CHB closed-loop controller. These signals are used to compare with PSPWM carriers to generate the switching pulses for the inverter, as

shown in Figs. 4.7. For each phase (A, B, and C), the controller output is compared against nine phase-shifted triangular carrier waves, each separated by 20°, corresponding to the nine cascaded H-bridge cells per phase. This comparison determines the firing pulses for the individual H-bridge cells, ensuring a high-quality multilevel output voltage and stable grid synchronization.

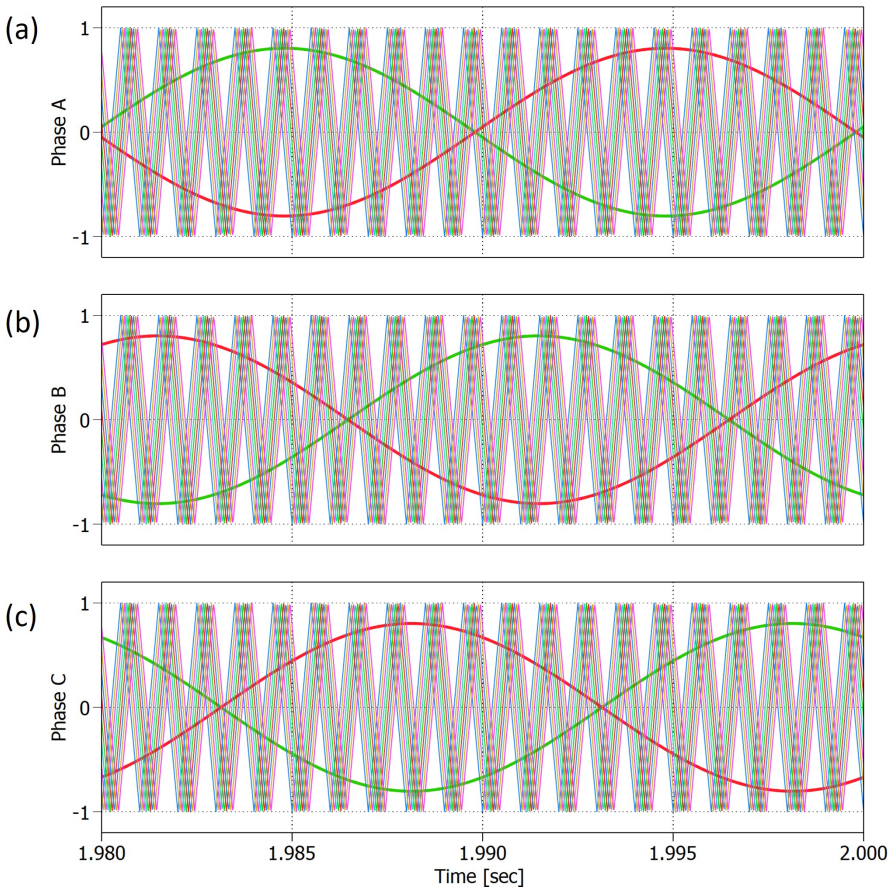

Figure 4.7: Controller output modulation signals for Phase A, B, and C compared with PSPWM carriers.

The steady-state performance of the proposed power converter system is evaluated under three distinct operating points. Figures 4.8, 4.9, and 4.10 illustrate the grid-side performance at 10%, 50%, and 75% load conditions, respectively. The dynamic response of the system to power scaling is primarily observed through the line current amplitudes and the total active power output:

- **Case 1 (10% Load):** As shown in Fig. 4.8, when operating at a light load condition of 10%, the balanced three-phase line currents stabilize with a peak amplitude of approximately 90 A.

- **Case 2 (50% Load):** When the system is scaled up to 50% load condition as shown in Fig. 4.9, the current waveforms remain highly sinusoidal with mini-

mal distortion, scaling proportionally to peak amplitude of 400 A.

- **Case 3 (75% Load):** Under the heavy-load condition of 75% illustrated in Fig. 4.10, the converter successfully delivers the 7.5 MW active power, with the corresponding line currents increasing stably to peak value of approximately 620 A.

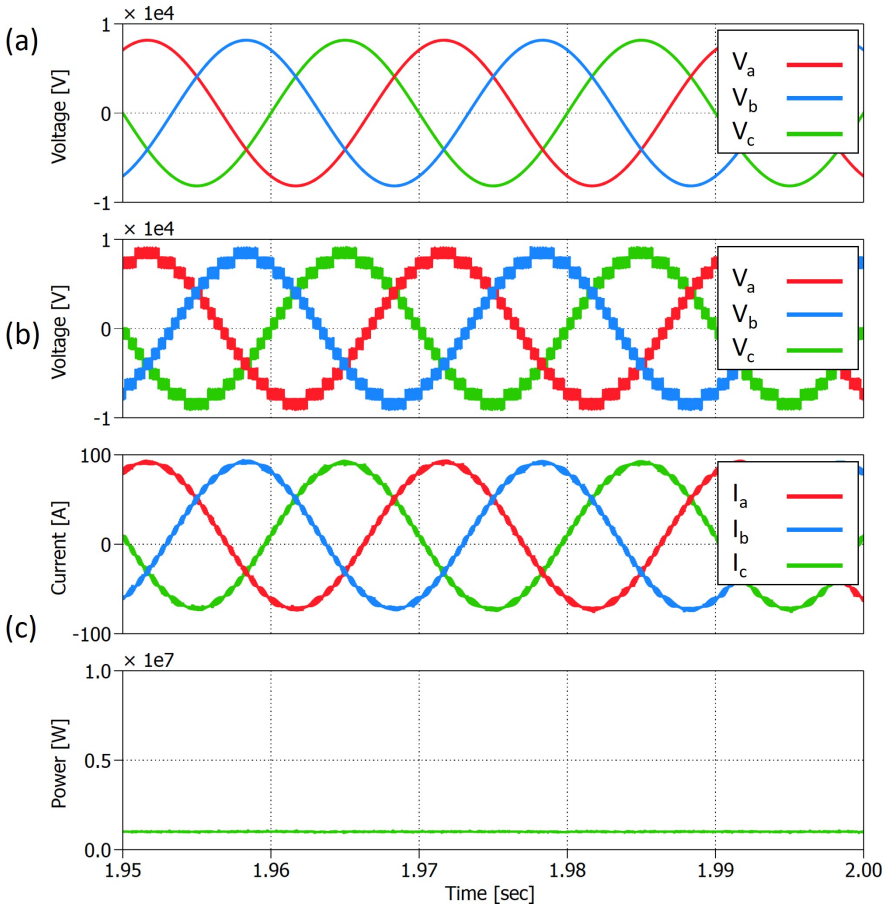

Figure 4.8: Steady-state output performance at 10% load conditions: (a) Grid Voltage; (b) Inverter voltage; (c) Grid current and (d) Grid power.

Furthermore, the power quality of the system improves significantly as the operating load increases. The THD of the line currents is measured at 2.28%, 0.49%, and 0.34% for the 10%, 50%, and 75% loading conditions, respectively. This inverse relationship occurs because at light loads (10%), the fundamental current amplitude is small, making the high-frequency switching ripples more prominent in proportion to the total signal. As the system scales up to 50% and 75% capacity, the fundamental current increases substantially while the absolute switching ripple remains relatively constant, leading to a much cleaner signal-to-noise ratio. This trend is clearly reflected in the current subplots of Figs. 4.8, 4.9, and 4.10, where the waveforms show an increasingly smooth, ideal sinusoidal profile at higher power levels.

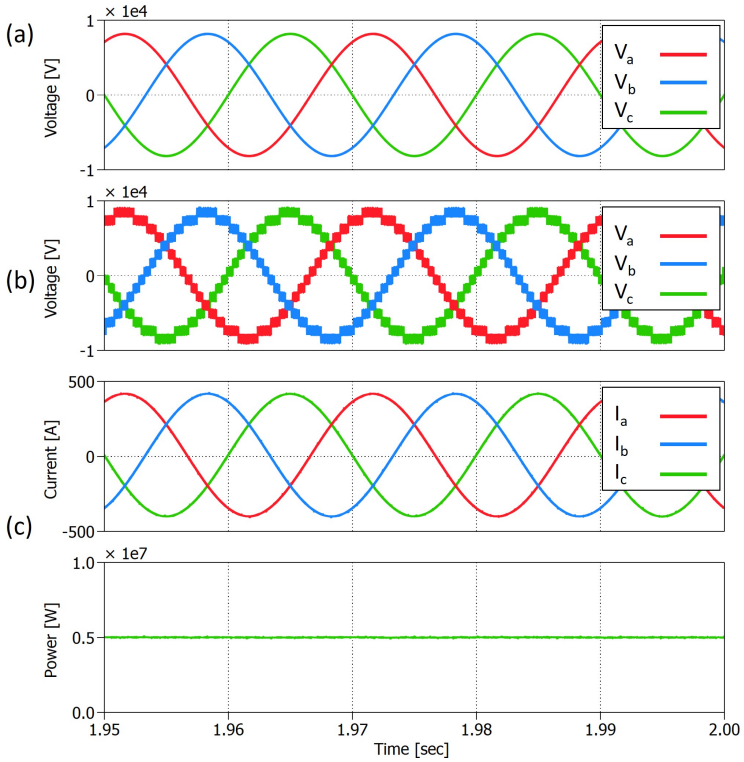

Figure 4.9: Steady-state output performance at 50% load conditions: (a) Grid Voltage; (b) Inverter voltage; (c) Grid current and (d) Grid power.

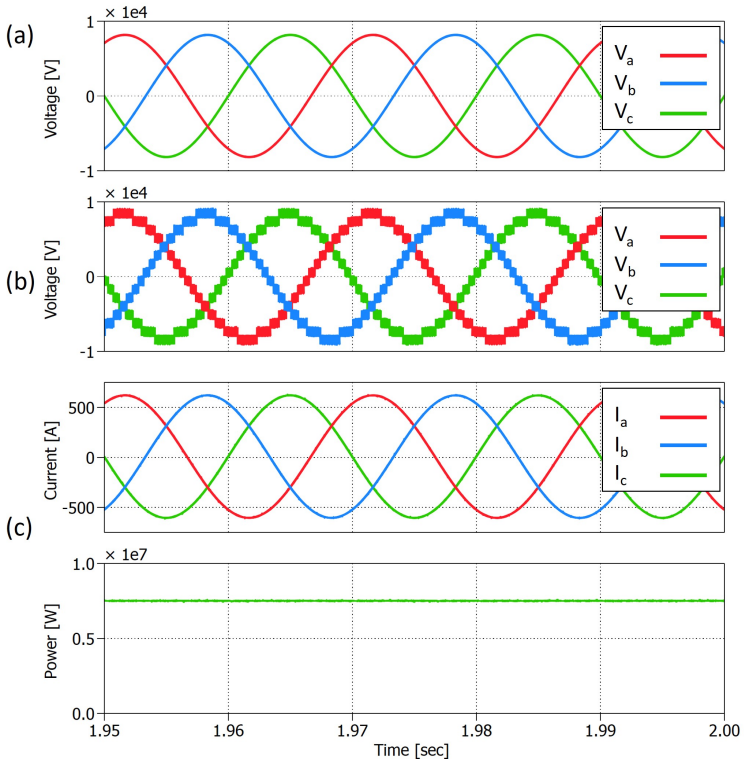

Figure 4.10: Steady-state output performance at 75% load conditions: (a) Grid Voltage; (b) Inverter voltage; (c) Grid current and (d) Grid power.

4.1.2 Case B: System design using 3.3 kV SiC MOSFET

In this configuration, the secondary side of the DAB and the CHB units are implemented using 3.3 kV SiC MOSFETs. Due to the higher voltage rating of these devices, the system is optimized by reducing the number of cascaded modules from 9 down to 5 modules per phase. The steady-state output performance for the 3.3 kV configuration is presented in Fig. 4.11 (a) and (c). The waveforms show that even with a reduced number of modules, the system maintains stable synchronization and precise current control under nominal conditions.

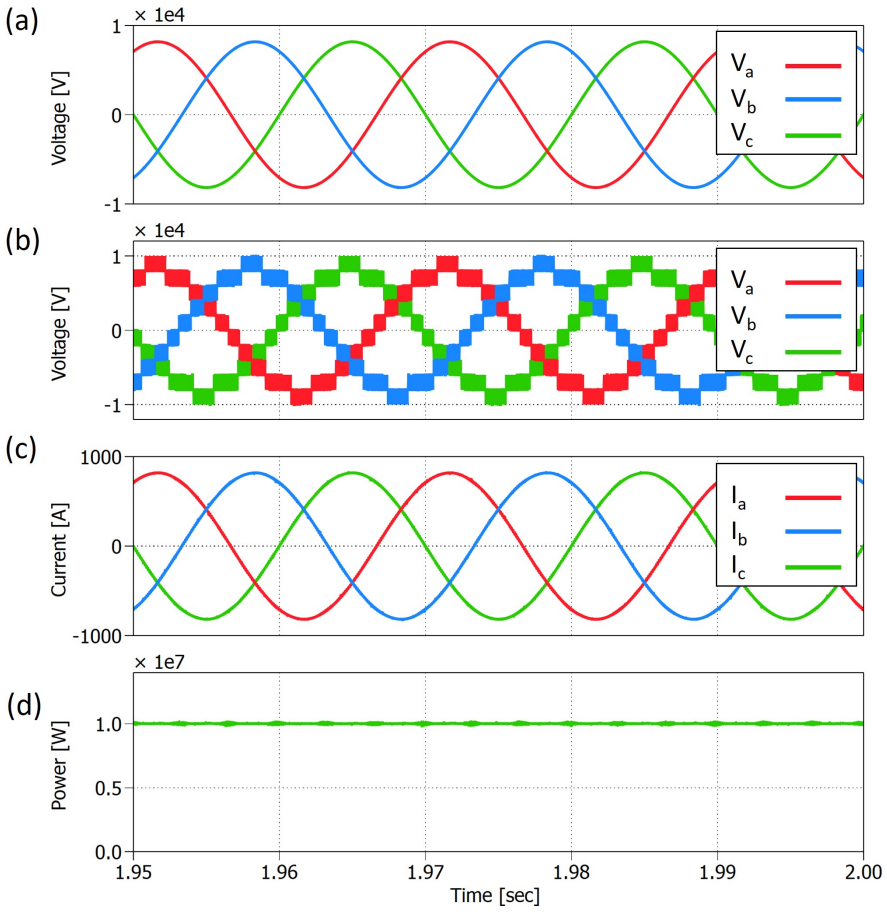

Figure 4.11: Steady-state output performance under nominal conditions while delivering 10 MW power to the grid: (a) Grid Voltage; (b) Inverter voltage; (c) Grid current and (d) Grid power.

The reduction in the number of H-bridge cells results in a three-phase 11-level inverter voltage waveform at the converter terminal, as shown in Fig. 4.11 (b). While there are fewer steps compared to the 1.7 kV case, the 11-level waveform still provides a high-quality approximation of a sine wave. At the PCC connection, the control strategy ensures the harmonic content of current remains well within regulatory limits at 0.78%.

The DAB characteristics for the 3.3 kV switches are illustrated in Fig. 4.12. In this case, the dc-link voltage is maintained at a higher level of 2000 V. The inductor current and bridge voltages confirm that the DAB efficiently manages power transfer at this higher voltage stress.

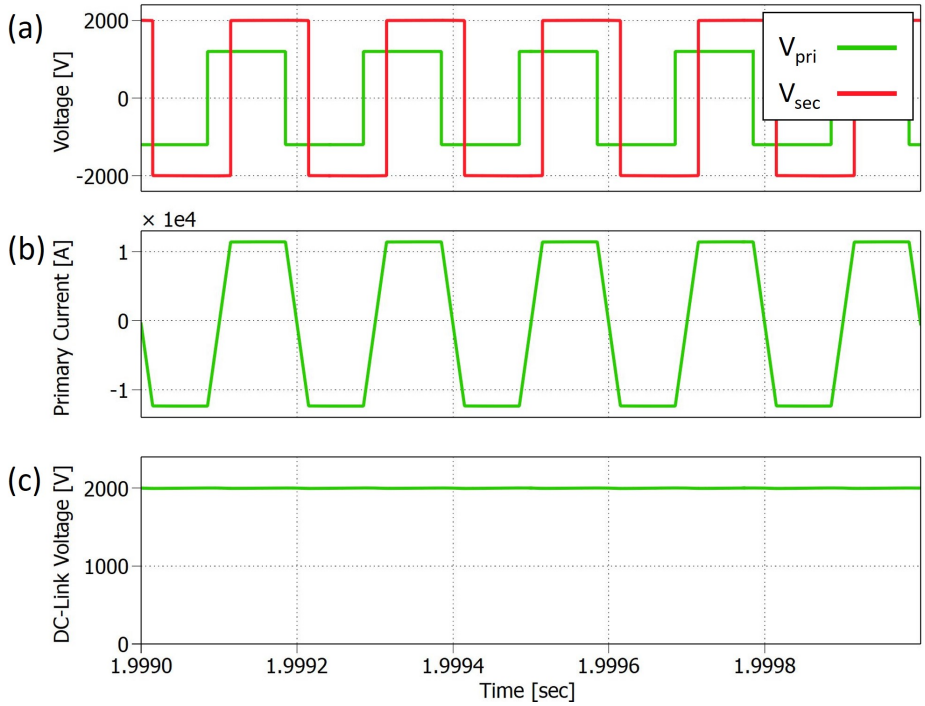

Figure 4.12: DAB simulation results with one of the cell units at the secondary side: (a) Primary and secondary side voltages; (b) Primary current; and (c) Output DC-link voltage waveforms.

Regarding the control implementation, the fundamental structures of the DAB and CHB controllers remain identical to those shown in Fig. 4.4 and Fig. 4.5. However, to account for the different device parameters and the reduced number of modules, different tuning constants and gains have been utilized. These specific parameters are detailed in the control strategy chapter to ensure optimal dynamic response for the 3.3 kV configuration. The interaction between the control loop and the modulation stage is shown in Fig. 4.13 and Fig. 4.14. The modulation signals, produced by the CHB closed-loop controller, are compared with a set of five phase-shifted triangular carriers per phase, each separated by 36°. This comparison generates the switching pulses for the 3.3 kV H-bridge chain, validating the effectiveness of the PSPWM technique for this modular configuration.

To validate the scalability of the topology, the system performance is also evaluated in second configuration utilizing 3.3 kV MOSFETs. Figures 4.15, 4.16, and 4.17 present the steady-state waveforms under identical loading conditions of 10%, 50%, and 75% load capacity, respectively.

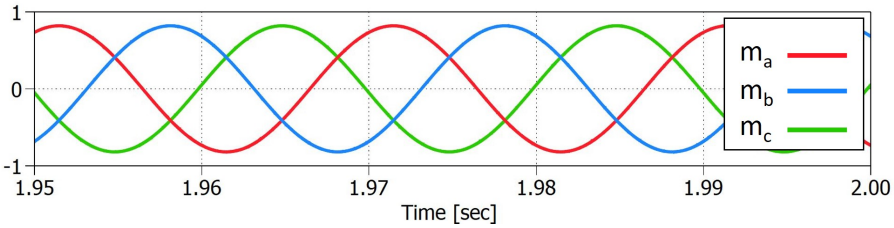

Figure 4.13: Three-phase modulation signals produced by CHB controller.

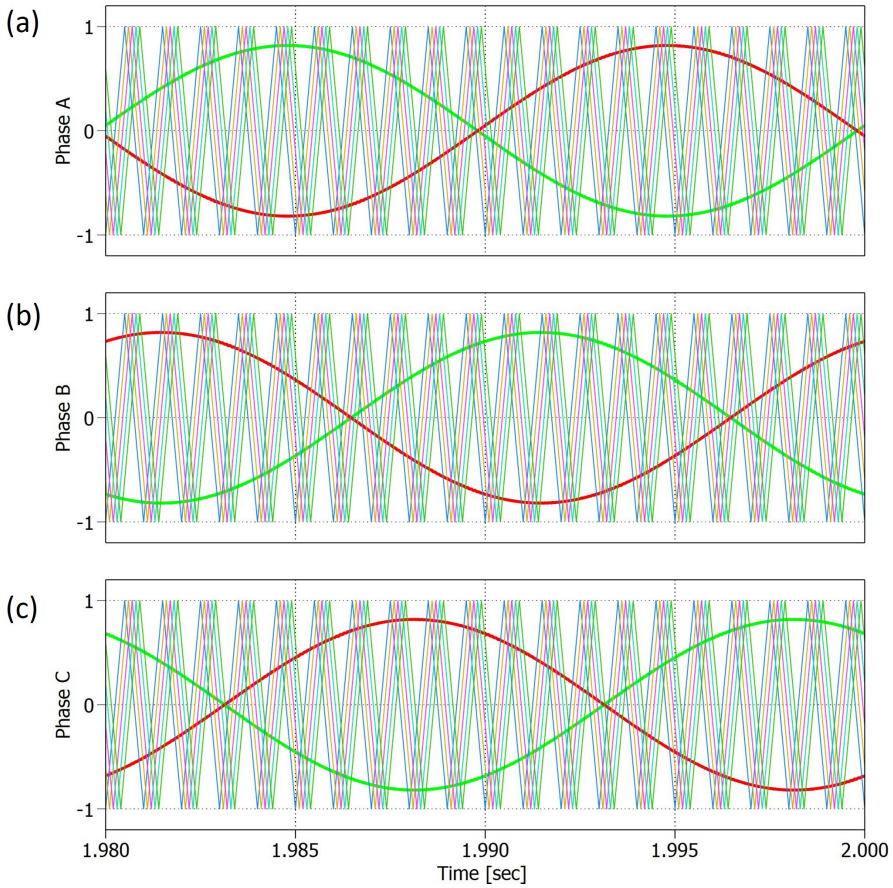

Figure 4.14: Controller output modulation signals for Phase A, B, and C compared with PSPWM carriers.

The line currents track their respective power references cleanly, scaling from an initial peak of approximately 90 A at 10% load up to roughly 620 A under the 75% heavy-load condition. The THD of the line currents for this 3.3 kV system is measured at 7%, 1.48%, and 1.03% for the 10%, 50%, and 75% load points, respectively. Although these harmonic percentages are higher than those of the 1.7 kV system—particularly at the 10% light-load condition where the switching distortion is visibly more pronounced in Fig. 4.15—the system maintains the same highly favorable inverse relationship. As the load scales up to 50% and 75%, the relative impact of the high-frequency switching ripples diminishes rapidly. This results in highly smooth, sinusoidal grid currents at higher operating limits.

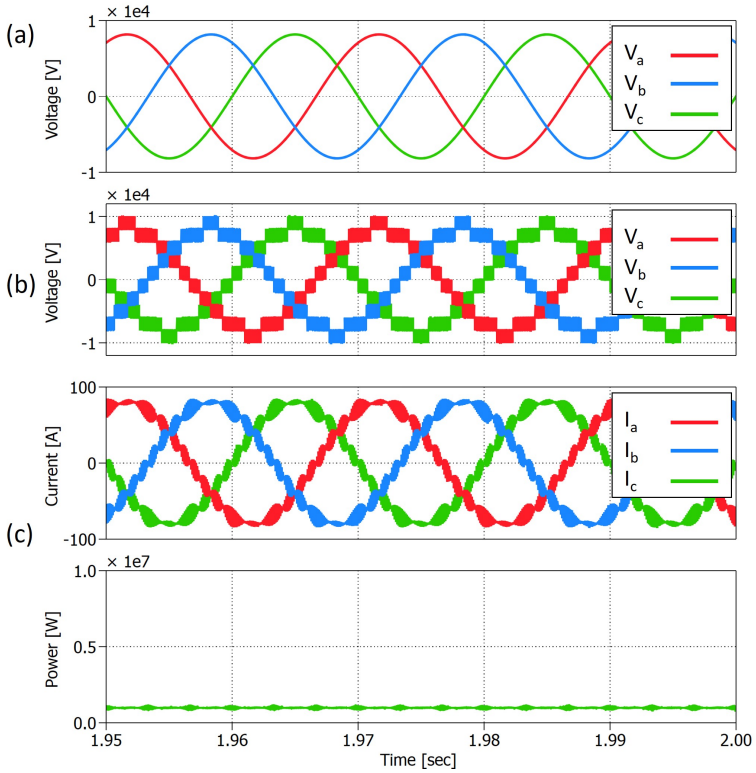

Figure 4.15: Steady-state output performance at 10% load conditions: (a) Grid Voltage; (b) Inverter voltage; (c) Grid current and (d) Grid power.

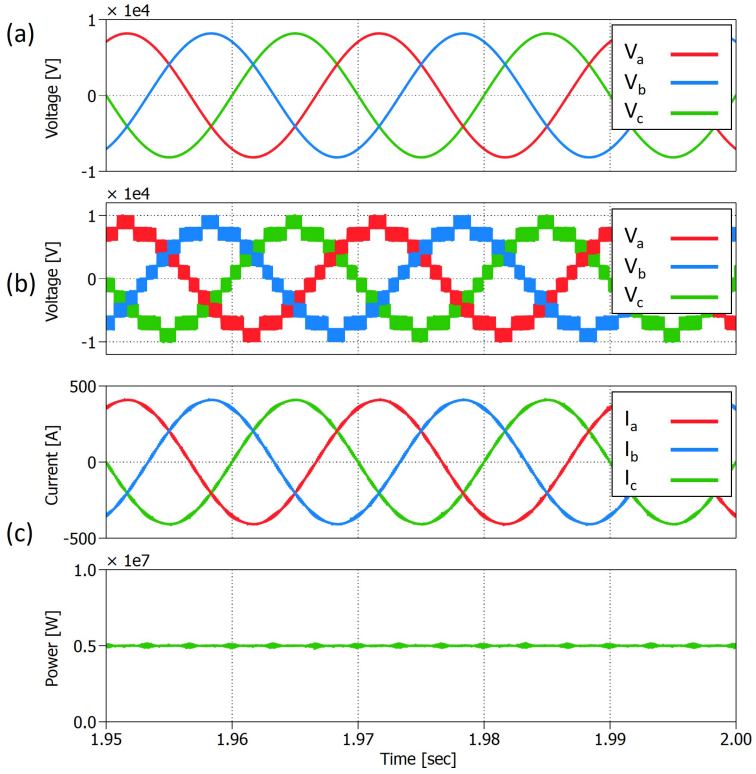

Figure 4.16: Steady-state output performance at 50% load conditions: (a) Grid Voltage; (b) Inverter voltage; (c) Grid current and (d) Grid power.

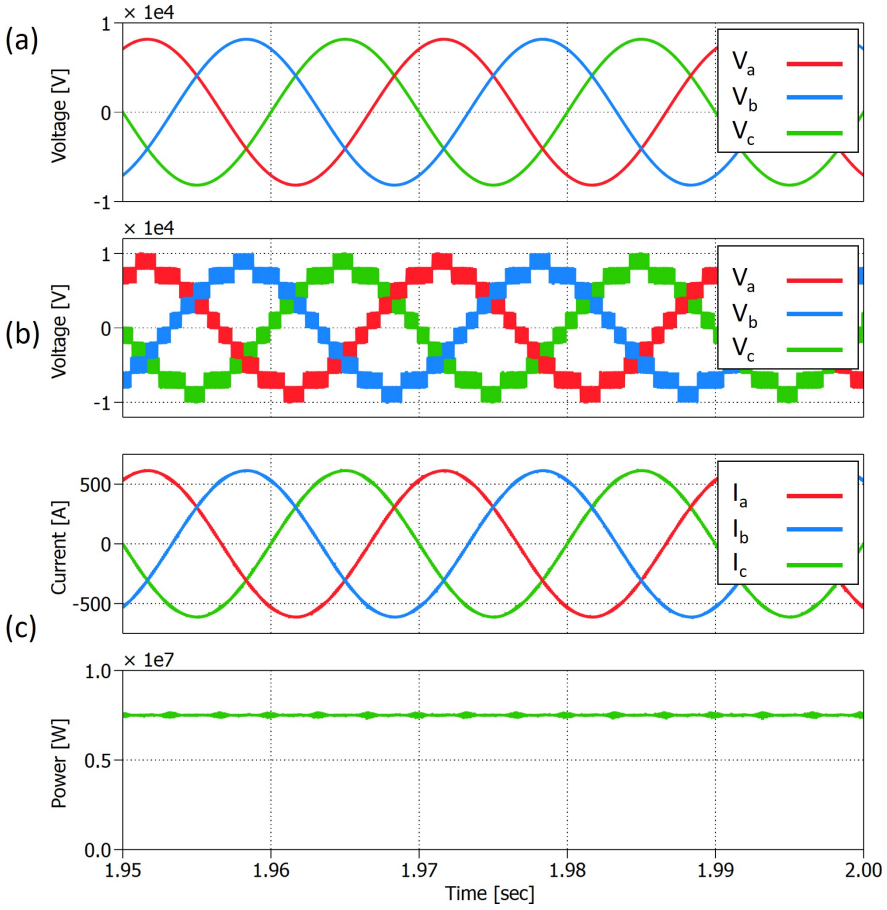

Figure 4.17: Steady-state output performance at 75% load conditions: (a) Grid Voltage; (b) Inverter voltage; (c) Grid current and (d) Grid power.

While this chapter focuses on validating the electrical performance and control behavior of the proposed MMC architecture, a detailed loss, efficiency, and cost analysis is not addressed here. These aspects are investigated in the following chapter, where the conduction and switching losses of the 1.7 kV and 3.3 kV SiC MOSFET-based designs are quantified using electro-thermal simulation results. Furthermore, the impact of switch voltage rating on overall system efficiency, modular complexity, and cost is analyzed to provide a comprehensive comparison and support the final design recommendations.

5

System Loss & Cost Analysis

5.1 Loss Analysis

To evaluate the practical performance of the 1.7 kV and 3.3 kV SiC MOSFET-based systems, a comprehensive loss analysis was conducted. Unlike theoretical estimations, this analysis utilizes the thermal modeling capabilities of PLECS, incorporating real-world device characteristics (look-up tables for E_{on}, E_{off}, and $V_{ce,sat}$) obtained from manufacturer datasheets reported in [34, 35]. The losses are calculated by mapping the switching and conduction loss data directly onto the simulation components.

A heat sink component is implemented for each H-bridge module to act as a thermal collector for the dissipated energy. It should be noted that the physical design and optimization of the cooling system, are outside the scope of this research. Instead, the heat sink serves as a centralized tool to aggregate losses and calculate the overall efficiency of the DAB and CHB stages under various operating conditions. This approach ensures that the total power loss results accurately reflect the device behavior defined in the manufacturer data.

The simulation results demonstrate high efficiency for both SiC-based implementations, confirming the performance benefits of the proposed MMC converter configuration in high-power applications. A detailed breakdown of the converter's performance at nominal load is provided in Table 5.1.

Table 5.1: Overall MMC-based converter efficiency at nominal load conditions.

Parameter	1.7 kV System	3.3 kV System
Conduction Loss Share (P_{cond})	67.7%	73.9%
Switching Loss Share (P_{sw})	32.3%	26.1%
Total Efficiency (η)	99%	98.8%

As shown in the data, the 1.7 kV system achieves a total efficiency (η) of 99%, while the 3.3 kV system operates at 98.8%. In addition to the slight difference in overall efficiency, the distribution of losses also varies between the two configurations. In the 1.7 kV system, switching losses (P_{sw}) account for 32.3% of the total loss profile. In contrast, the 3.3 kV system reduces the switching loss share to 26.1%, which is a direct result of the reduced component count and fewer switching transitions required for the same voltage level. However, the 3.3 kV system exhibits a higher

conduction loss share (P_{cond}) of 73.9% compared to 67.7% in the 1.7 kV counterpart. This suggests that while the higher-voltage switches excel at reducing switching-related stress, their on-state resistance contributes a larger portion to the total energy dissipation. These findings highlight a critical trade-off between switching frequency optimization and conduction efficiency when selecting SiC device ratings for modular multilevel architectures.

5.1.1 Loss Analysis Under Different Load Conditions

To evaluate the system performance across the full operating range, the efficiency was simulated from 10% to 100% load for both the 1.7 kV and 3.3 kV configurations. The total system efficiency, representing the combined performance of the DAB and CHB stages, is illustrated in Fig 5.1. Both systems maintain a high efficiency above 98% across the entire load spectrum. Notably, the 1.7 kV system exhibits a very flat efficiency curve, peaking early at approximately 30% load and maintaining superior performance at light loads. In contrast, the 3.3 kV system shows a steeper drop in efficiency below 30% load. This is primarily attributed to higher fixed losses and the specific switching characteristics of the higher-voltage devices at lower power levels; however, the efficiency gap narrows significantly as the system approaches nominal power. This trend is in accordance with the results reported in [37].

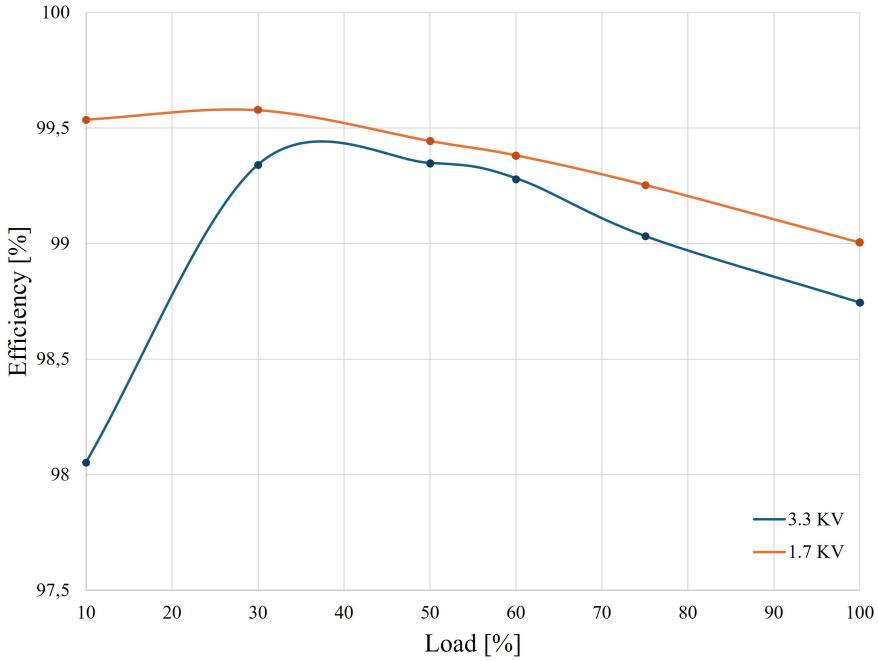

Figure 5.1: Overall MMC-based converter efficiency under different load conditions.

To further analyze these behavioral differences, Fig 5.2 details the percentage share of semiconductor losses for both configurations at nominal operation. For the 1.7 kV system, conduction losses constitute approximately 67.7% of the total semiconductor

losses, with switching losses accounting for the remaining 32.3%. In comparison, the 3.3 kV configuration exhibits an even higher dominance of conduction losses, which rise to roughly 74.0% of the share, while its switching loss share drops to 26.0%. This higher share of conduction losses in the 3.3 kV system is primarily driven by the higher $R_{\mathrm{DS(on)}}$, causing ohmic losses to dominate at nominal current levels.

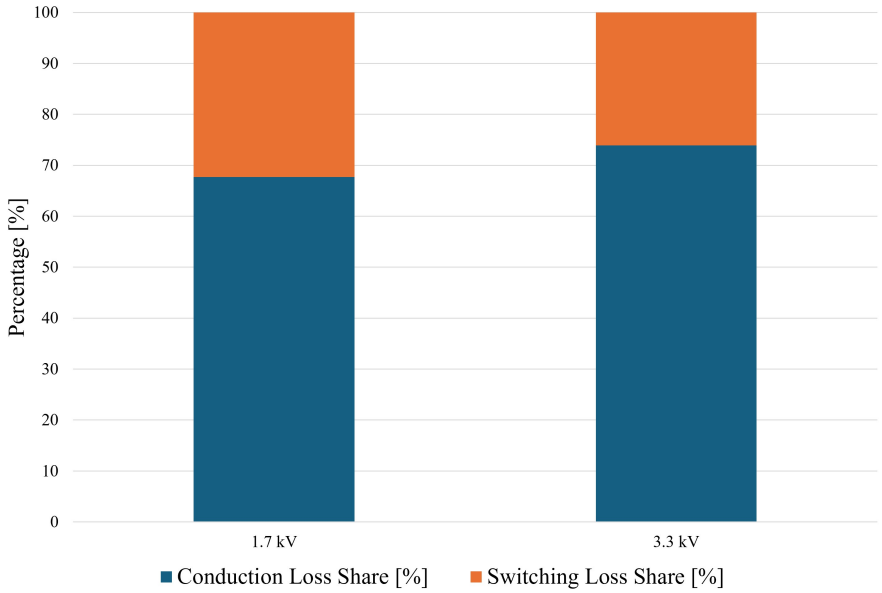

Figure 5.2: Overall Loss distribution.

The individual conversion stages provide further insight into these results. The efficiency of the isolated DAB stage is shown in Fig 5.3. In this stage, switching losses are significantly minimized due to the ZVS mechanism. While the 1.7 kV system maintains a consistently higher efficiency above 99.3%, the 3.3 kV system exhibits a characteristic efficiency drop at light loads (dropping to roughly 98.1% at 10% load) and peaks near 40% load, demonstrating that the ZVS benefits for the 3.3 kV SiC switches are most effective at moderate to high current levels.

The physical basis for this difference is detailed in the loss distribution breakdown presented in Fig 5.4. Both systems utilize the same primary-side switches, resulting in an identical loss share of approximately 59% conduction and 41% switching for the DAB primary bridge. However, the secondary-side bridges utilize different SiC MOSFETs tailored to their respective voltage levels. The 1.7 kV secondary stage exhibits a loss profile of roughly 61% conduction and 39% switching, benefiting from a lower on-resistance of $R_{\mathrm{DS(on)}} = 1.42\ \mathrm{m\Omega}$. In contrast, the 3.3 kV secondary stage uses devices with a higher resistance of $R_{\mathrm{DS(on)}} = 2.7\ \mathrm{m\Omega}$. As illustrated in Fig 5.4, this higher resistance shifts its loss profile further, leading to an increased conduction loss share of approximately 68% and a reduced switching loss share of 32% in the 3.3 kV secondary bridge.

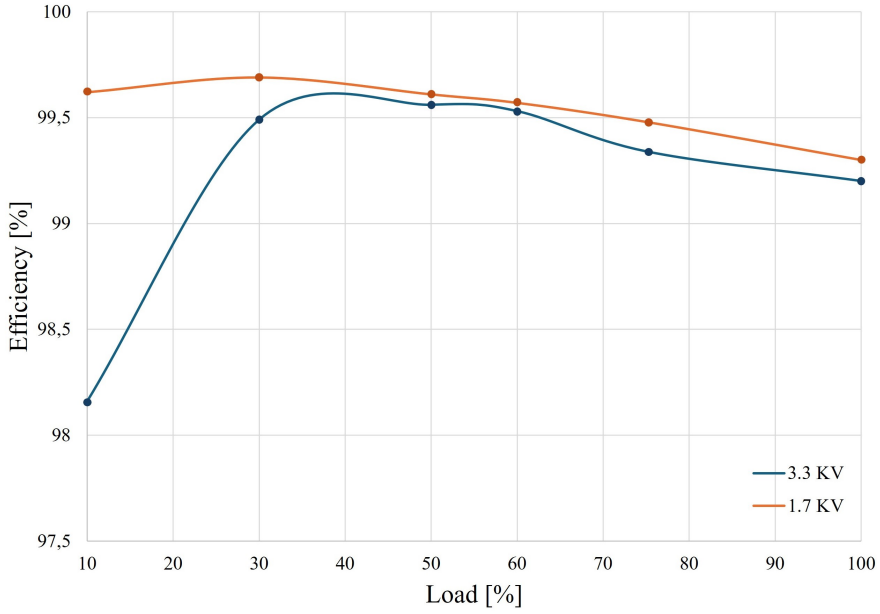

Figure 5.3: Isolated DAB converter efficiency under different load conditions.

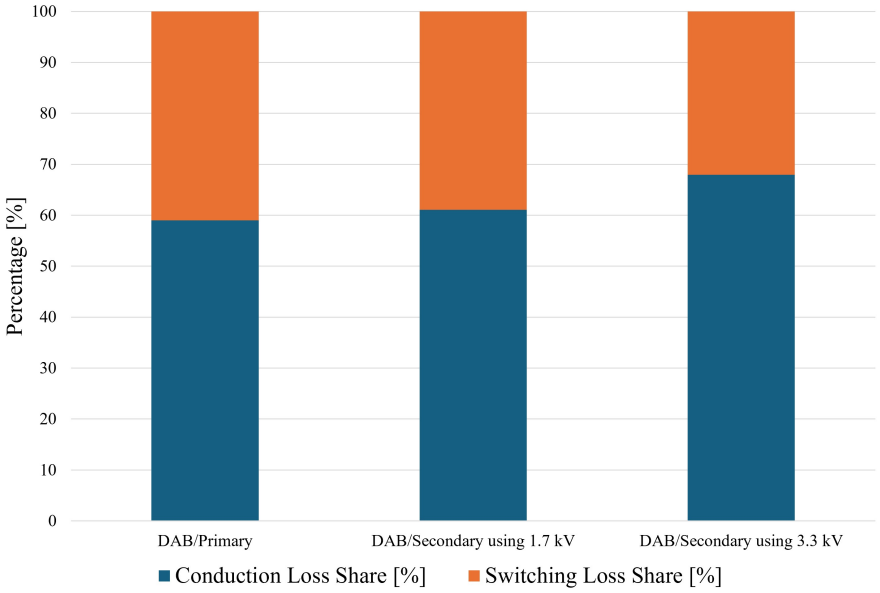

Figure 5.4: DAB Loss distribution: Comparison of primary and secondary bridge shares.

Finally, the CHB converter efficiency, shown in Fig 5.5, demonstrates extremely high and stable performance for both systems, consistently exceeding 99.5%. The efficiency in this stage decreases almost linearly as the load increases, which is typical for a stage dominated by I^2R conduction losses. The 1.7 kV CHB stage performs slightly better than 3.3 kV variant. Even though the 1.7 kV system requires a higher number of submodules, the lower $R_{\mathrm{DS(on)}}$ of the 1.7 kV SiC MOSFETs results in lower total conduction losses in the phase leg compared to the 3.3 kV configuration.

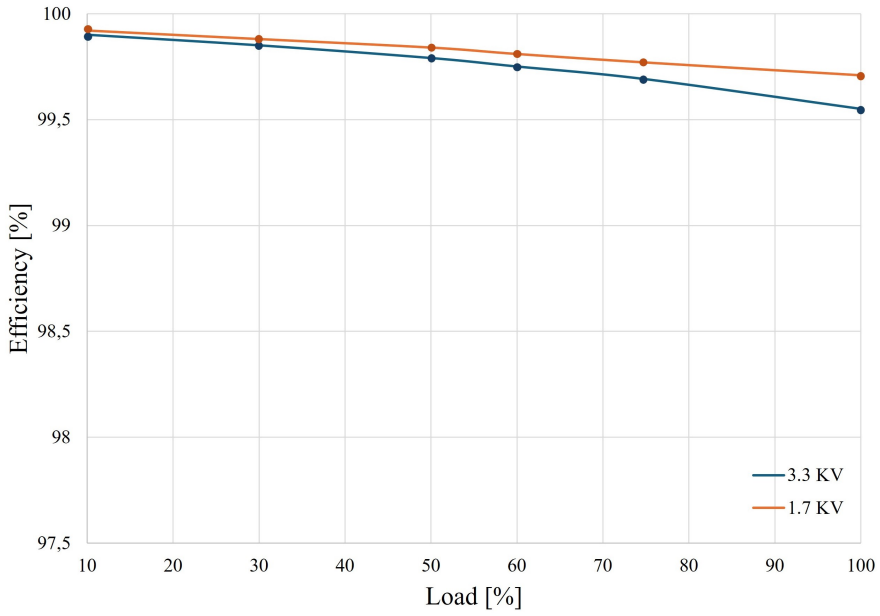

Figure 5.5: Cascaded H-bridge converter efficiency under different load conditions.

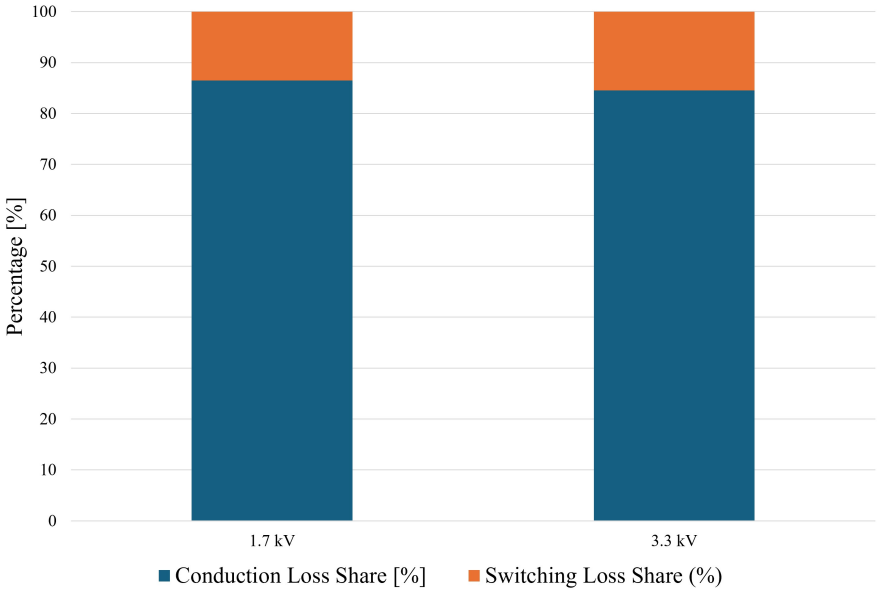

Figure 5.6: CHB Loss distribution.

The underlying loss distribution presented in Fig 5.6 confirms that conduction causes most of the losses for both voltage levels at nominal operation. For the 1.7 kV CHB configuration, conduction losses make up approximately 86.5% of the total semiconductor losses, while switching losses are only 13.5%. Similarly, the 3.3 kV configuration has a very similar split, where conduction losses make up roughly 84.5% of the total and switching losses account for the remaining 15.5%. This high amount of conduction losses shows that the total resistance of the switches is the main factor deciding the CHB stage's overall efficiency.

This detailed analysis confirms that while the 1.7 kV system offers slightly higher peak efficiency due to lower on-resistance, the 3.3 kV system provides a highly competitive alternative. By utilizing higher-voltage devices, it significantly reduces the overall component count and system complexity of the 10 kV MMC architecture while maintaining excellent efficiency.

5.2 Cost Analysis

In the development of this system, the architectural framework and component selection strategies are derived from the research presented by [36]. This work adopts a high-frequency link featuring a single primary and multiple secondary windings (twenty-seven for 1.7 kV switches and fifteen for 3.3 kV switches), which follows the methodology presented in the article of using multi-winding transformers to reduce magnetic component count and increase power density. By integrating multiple outputs into a single transformer core, the system achieves a significant reduction in total volume compared to traditional modular designs.

For the economic evaluation, the cost of the high-frequency multi-winding transformer is estimated based on current market rates for specialized magnetic cores and windings suitable for high-power, high-frequency applications, totaling 380,000 USD. Notably, this cost remains constant across both the 1.7 kV and 3.3 kV scenarios, as the rated power and operating frequency—the primary drivers of transformer sizing and material costs—are identical for both system designs. The specific results of the component selection and cost analysis for the 1.7 kV and 3.3 kV systems are summarized in Table 5.2 and 5.3.

Table 5.2: Components design results of the 1.7 kV system.

Parameter	Component	Type	Cost (USD)
DAB primary side	Transformer	-	380,000
	Half-bridge module	CAB650M17HM3	3891.62
	Gate driver	CGD1700HB3P-HM3	498.53
	DC-link capacitor	947D481K132DGRSN	131.33
DAB secondary side	Half-bridge module	CAB650M17HM3	3891.62
	Gate driver	CGD1700HB3P-HM3	498.53
	DC-link capacitor	947D481K132DGRSN	131.33
CHB stage	Half-bridge module	CAB650M17HM3	3891.62
	Gate driver	CGD1700HB3P-HM3	498.53

As observed in Figure 5.7, the transition from a 1.7 kV architecture to a 3.3 kV architecture offers a clear economic advantage. While the 1.7 kV configuration provides higher operational efficiency, the 3.3 kV system is the more cost-effective solution. The total system cost is reduced because the higher voltage rating of the 3.3 kV modules allows for a lower submodule count, thereby reducing the complexity and quantity of components in the CHB and DAB secondary stages.

Table 5.3: Components design results of the 3.3 kV system.

Parameter	Component	Type	Cost (USD)
DAB primary side	Transformer	-	380,000
	Half-bridge module	CAB650M17HM3	3891.62
	Gate driver	CGD1700HB3P-HM3	498.53
	DC-link capacitor	947D481K132DGRSN	131.33
DAB secondary side	Half-bridge module	FF4000UXTR33T2M1	2846.11
	Gate driver	1SP0635V2M1-33	317.38
	DC-link capacitor	C44PXGR5680RASK	134.13
CHB stage	Half-bridge module	FF4000UXTR33T2M1	2846.11
	Gate driver	1SP0635V2M1-33	317.38

The visual breakdown in Figure 5.7 shows that while "Magnetic Components" remain a fixed expenditure due to the transformer's constant parameters, the "MOSFET" category sees the most significant reduction. This validates the shift toward 3.3 kV SiC technology for large-scale grid integration; the savings gained from reduced semiconductor volume and fewer required submodules.

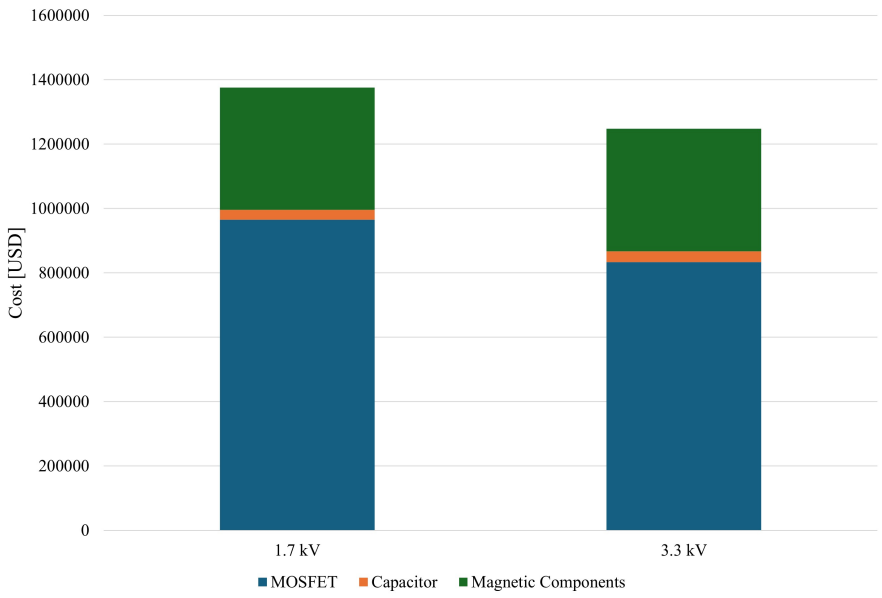

Figure 5.7: Total estimated system cost breakdown in USD.

In conclusion, this comprehensive evaluation highlights a decisive trade-off between operational efficiency and economic viability when selecting SiC device ratings for the 10 kV MMC architecture. Performance analysis confirms that both configurations achieve excellent total efficiency around 99%, with the 1.7 kV system offering a slightly higher nominal efficiency and a flatter light-load curve due to its lower device on-resistance ($R_{\mathrm{DS(on)}} = 1.42$ mΩ). However, the economic analysis reveals that the 3.3 kV system serves as a highly competitive and practical alternative; by using higher-voltage components, it lowers the required submodule count, signifi-

cantly reducing system complexity, semiconductor volume, and auxiliary component expenditures while managing an exceptional nominal efficiency of 98.8%.

6
Conclusion

This thesis investigated the integration of renewables through a common DC-link architecture using modular multilevel converter principles. The primary objective was to evaluate whether a cascaded H-bridge inverter combined with an isolated dual active bridge stage and SiC semiconductors could provide high efficiency, high power density, and stable grid-connected operation at the medium-voltage level. To achieve this, a comprehensive simulation framework was developed in MATLAB/Simulink and PLECS, incorporating realistic semiconductor device models, control strategies, and loss mechanisms.

The proposed converter architecture successfully demonstrated stable steady-state and dynamic performance for a 10 MW, 10 kV grid-connected application. The control of the DAB and CHB stages ensured a regulated DC-link voltage and high-quality output currents with low harmonic distortion. The synchronous reference frame current control combined with phase-shifted PWM enabled accurate current tracking and unity power factor operation, while the single phase-shift control of the DAB stage effectively maintained DC-link voltage stability under varying operating conditions.

A comparative study between 1.7 kV and 3.3 kV SiC MOSFET-based implementations highlighted important trade-offs in modular converter design. The 1.7 kV system achieved slightly higher peak efficiency due to its lower on-state resistance, particularly under light-load conditions. However, this performance advantage was accompanied by an increased number of cascaded submodules and higher system complexity. In contrast, the 3.3 kV system significantly reduced the cost and number of required submodules, resulting in a simpler architecture with fewer components and reduced switching events, while still maintaining an overall efficiency close to 99%.

The loss analysis based on electro-thermal simulations confirmed that conduction losses dominate in the CHB stage, whereas the DAB stage benefits strongly from zero-voltage switching, leading to comparatively low switching losses. Across a wide operating range, both system configurations maintained efficiencies above 98%, validating the effectiveness of the proposed DC-link-based solid-state transformer architecture for high-power applications. The cost evaluation further indicated that higher-voltage SiC devices can offer system-level advantages by reducing converter complexity and component count, despite higher individual device costs.

The cost analysis reveals that the 3.3 kV architecture offers a distinct economic advantage over the 1.7 kV configuration at the system level. While the high-frequency multi-winding transformer remains a fixed capital expenditure for both designs, the 3.3 kV system drastically reduces the total component count by scaling down from twenty-seven secondary channels to fifteen. This reduction in submodule count significantly lowers cumulative spending on MOSFET modules, gate drivers, and passive components. Consequently, despite the different unit costs of higher-voltage semiconductor devices, the 3.3 kV configuration serves as the more cost-effective and practical solution for 10 MW large-scale integration by minimizing overall manufacturing complexity and material volume.

Overall, the results demonstrate that integrating PV and BESS through a modular DC-link architecture using CHB and DAB converters is a technically feasible and efficient solution for medium-voltage grid applications. The close agreement between theoretical design calculations and simulation results suggests that the conclusions drawn from the simulated models can be regarded as reliable for system-level evaluation. The proposed architecture preserves the original functionality of grid-connected power conversion while enabling high efficiency, modular scalability, and improved power density, making it a promising candidate for next-generation renewable energy integration systems.

6.1 Future Work

Although this thesis demonstrated the feasibility and performance of a common DC bus architecture for large-scale PV and Battery Energy Storage System (BESS) integration through simulation, several aspects can be further developed to enhance system performance, and practical applicability.

First, the presented work is primarily based on detailed PLECS simulation models. A natural continuation of this research would be the experimental validation of the proposed architecture using a laboratory-scale prototype. Hardware implementation would enable verification of switching behavior, thermal performance, parasitic effects, and control robustness under non-ideal operating conditions that are difficult to fully capture in simulation-based studies.

One important extension of this work concerns the control of DAB converter. In the present study, single phase shift modulation was employed to regulate power flow due to its simplicity and ease of implementation. Future work could investigate advanced DAB control strategies, such as Triple Phase Shift (TPS) modulation, which allows for additional degrees of freedom in optimizing current waveforms, reducing circulating currents, and improving efficiency over a wider operating range. Furthermore, the application of predictive or adaptive control techniques may enhance dynamic performance and robustness under varying load and source conditions.

Similarly, the grid-side inverter control strategy can be further improved. While

control methods provide satisfactory steady-state and dynamic performance, future studies could explore advanced inverter controller structures, including model predictive control (MPC), virtual inertia emulation, or grid-forming control strategies. These approaches are particularly relevant for power systems with high penetration of renewable energy sources and weak-grid conditions.

Another important area for future work is the explicit modeling and integration of renewable energy sources. In the present thesis, the focus was placed on the DC bus and converter-level behavior, and the PV and BESS subsystems were therefore represented in a simplified manner and not modeled in detail. Future research could extend the developed framework by incorporating dedicated PV and battery models connected to the DC input source, enabling a more comprehensive assessment of source–converter interactions.

In particular, advanced PV panel models that capture the effects of irradiance and temperature variations could be implemented, together with electrochemical battery models that consider state-of-charge dynamics, aging effects, and power and energy constraints. Within such an extended framework, the implementation of MPPT algorithms would represent a natural continuation of the present work. Integrating MPPT techniques, such as perturb-and-observe or incremental conductance methods, would allow the PV system to operate under realistic operating conditions and enable a more detailed evaluation of the interaction between the renewable sources, the common DC bus, and the power electronic converters.

Bibliography

[1] N. E. M. Zahari et al., "Integrating Solar PV, Battery Storage, and Demand Response for Industrial Peak Shaving: A Systematic Review on Strategy, Challenges and Case Study in Malaysian Food Manufacturing," *IEEE Access*, vol. 12, pp. 106832-106856, 2024.

[2] C. Bussar et al., "Large-scale Integration of Renewable Energies and Impact on Storage Demand in a European Renewable Power System of 2050," *Energy Procedia*, vol. 73, pp. 145–153, 2015.

[3] H. S. Zhou, R. Passey, A. Bruce, and A. B. Sproul, "Aggregated impact of coordinated commercial-scale battery energy storage systems on network peak demand, and financial outcomes," *Renew. Sustain. Energy Rev.*, vol. 144, p. 111014, Jul. 2021.

[4] H. A. Taha, M. H. Alham, and H. K. M. Youssef, "Multi-Objective Optimization for Optimal Allocation and Coordination of Wind and Solar DGS, BESSs and Capacitors in Presence of Demand Response," *IEEE Access*, vol. 10, pp. 16225-16241, 2022.

[5] O. Khoubseresht, M. Rajabinezhad, and S. Y. M. Mousavi, "An analytical optimum method for simultaneous integration of PV, wind turbine and BESS to maximize technical benefits," *IET Gener. Transm. Distrib.*, vol. 17, no. 10, pp. 2207–2227, May 2023.

[6] G. V. B. Kumar, G. A. Kumar, S. Eswararao, and D. Gehlot, "Modelling and Control of BESS for Solar Integration for PV Ramp Rate Control," in *Proc. 2018 Int. Conf. Comput. Power, Energy, Inf. Commun. (ICCPEIC)*, Chennai, India, 2018, pp. 165–170.

[7] Z. Shi, X. Dou, and F. Yue, "Multi-Mode Control Strategy for PV-BESS VSG in Microgrid Based on RBF Neural Network," in *Proc. 2025 6th Int. Conf. Adv. Elect. Energy Syst. (AEES)*, Nanjing, China, 2025, pp. 623–627.

[8] J. Wang, D. Zhu, C. Liu, Z. Pei, H. Sun, and C. Liu, "Single-Stage Isolated PV-Battery-Hybrid (PVBH) Cascaded Grid-Connected System Based on Multiplexing Converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 13, no. 3, pp. 3698-3714, Jun. 2025.

[9] M. Z. Farooqi, B. Singh, and B. K. Panighiri, "Performance Enhancement of Single-Phase Two-Stage AC-DC Converter With Reduced DC-Link Capacitance," *IEEE Trans. Ind. Appl.*, vol. 59, no. 5, pp. 5739-5751, Sep./Oct. 2023.

[10] L. Zhang, Z. Zhang, J. Qin, D. Shi, and Z. Wang, "Design and Performance Evaluation of the Modular Multilevel Converter (MMC)-based Grid-tied PV-Battery Conversion System," in *Proc. 2018 IEEE 4th Southern Power Electron. Conf. (SPEC)*, Singapore, 2018, pp. 1-8.

[11] T. Nakanishi and J.-I. Itoh, "High Power Density Design for a Modular Multilevel Converter With an H-Bridge Cell Based on a Volume Evaluation of Each Component," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1967–1983, Mar. 2018.

[12] M. Coppola, A. Dannier, E. Fedele, G. Saggese, and P. Guerriero, "Design and Control of an Enhanced Grid-Tied PV CHB Inverter," *Energies*, vol. 18, no. 8, p. 2056, Apr. 2025.

[13] T. Zhao and D. Chen, "Active Power Backflow Control Strategy for Cascaded Photovoltaic Solid-State Transformer During Low-Voltage Ride Through," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 440-451, Jan. 2022.

[14] I. Marzo, A. Sanchez-Ruiz, J. A. Barrena, G. Abad, and I. Muguruza, "Power Balancing in Cascaded H-Bridge and Modular Multilevel Converters Under Unbalanced Operation: A Review," *IEEE Access*, vol. 9, pp. 110512-110543, 2021.

[15] A. L. Maryani, M. M. Mohamad, and M. F. Hamdan, "Towards Realizing Value of Grid Connected Battery Energy Storage System (BESS) with Solar Photovoltaic (PV) Generation: A Case Study," in *Proc. 2024 IEEE AEES*, Kuala Lumpur, Malaysia, 2024, pp. 1-6.

[16] S. Haq et al., "An Advanced PWM Technique for MMC Inverter Based Grid-Connected Photovoltaic Systems," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 8, Art. no. 0601605, Nov. 2021.

[17] J. Huber, P. Wallmeier, R. Pieper, F. Schafmeister, and J. W. Kolar, "Comparative Evaluation of MVAC-LVDC SST and Hybrid Transformer Concepts for Future Datacenters," in *Proc. 2022 Int. Power Electron. Conf. (IPEC-Himeji 2022 - ECCE Asia)*, Himeji, Japan, 2022, pp. 2649–2656.

[18] S. Baburajan et al., "Design of Common DC-Link Capacitor in Multiple-Drive System Based on Reduced DC-Link Current Harmonics Modulation," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9703-9717, Aug. 2022.

[19] H. Shadfar, M. G. Pashakolaei, and A. A. Foroud, "Solid-state transformers: An overview of the concept, topology, and its applications in the smart grid," *Int. Trans. Electr. Energy Syst.*, vol. 31, no. 8, p. e12996, Aug. 2021.

[20] M. A. Hannan et al., "State of the Art of Solid-State Transformers: Advanced Topologies, Implementation Issues, Recent Progress and Improvements," *IEEE Access*, vol. 8, pp. 19113-19132, 2020.

[21] M. S. Mollik et al., "The Advancement of Solid-State Transformer Technology and Its Operation and Control with Power Grids: A Review," *Electronics*, vol. 11, no. 17, Art. no. 2648, Aug. 2022.

[22] I. Serban, C. Marinescu, and D. Munteanu, "Performance analysis of a SiC-based single-phase H-bridge inverter with active power decoupling," in *Proc. 18th Eur. Conf. Power Electron. Appl. (EPE'16 ECCE Europe)*, Karlsruhe, Germany, 2016, pp. 1-10.

[23] S. A. Abdul-Azeez, J. K. Banda, L. S. Araujo, and E. Tedeschi, "Multi-level BESS Power Conversion Topologies for Isolated Grids: a Systematic Comparison," in *Proc. 2024 Int. Symp. Power Electron., Electr. Drives, Autom. Motion (SPEEDAM)*, Ischia, Italy, 2024, pp. 381–386.

[24] A. Marzoughi, R. Burgos, D. Boroyevich, and Y. Xue, "Design and Comparison of Cascaded H-Bridge, Modular Multilevel Converter, and 5-L Active Neutral Point Clamped Topologies for Motor Drive Applications," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1404–1413, Mar./Apr. 2018.

[25] J. O. Uwagboe and A. K. Saha, "A Comprehensive Review of Multilevel Inverter Topologies and Control Strategies for Grid-Connected Photovoltaic Battery Energy Storage Systems Integrating Active Power Filter," *IEEE Access*, vol. 13, pp. 170016-170045, 2025.

[26] S. Bayhan, M. Trabelsi, O. Ellabban, H. Abu-Rub, and R. S. Balog, "A five-level neutral-point-clamped/H-bridge quasi-impedance source inverter for grid connected PV system," in *Proc. 6th Int. Conf. Power Eng., Energy Electr. Drives (CPE-POWERENG)*, Florianopolis, Brazil, 2016, pp. 138-143.

[27] L. Baruschka and A. Mertens, "Comparison of Cascaded H-Bridge and Modular Multilevel Converters for BESS Application," in *Proc. 14th Eur. Conf. Power Electron. Appl. (EPE 2011)*, Birmingham, UK, 2011, pp. 1-10.

[28] J. B. Soomro, F. Akhtar, R. Hussain, J. A. Ansari, and H. M. Munir, "A Detailed Review of MMC Circuit Topologies and Modelling Issues," *Int. Trans. Electr. Energy Syst.*, vol. 2022, Art. no. 8734010, Mar. 2022.

[29] Swarnim and S. Kamlu, "Comparative analysis for Cascaded H-Bridge Multilevel Inverter," in *Proc. 2024 3rd Int. Conf. Innov. Technol. (INOCON)*, Karnataka, India, 2024, pp. 1-6.

[30] S. B. Bashir et al., "Modular Multilevel Converter-Based Microgrid: A Critical Review," *IEEE Access*, vol. 11, pp. 67910-67936, 2023.

[31] P. Sochor and H. Akagi, "Theoretical and Experimental Comparison Between Phase-Shifted PWM and Level-Shifted PWM in a Modular Multilevel SDBC Inverter for Utility-Scale Photovoltaic Applications," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4695–4707, Sep./Oct. 2017.

[32] T. Chen, G. Zeng, F. Tang, L. Wu, L. Jing, W. Zhang, and Y. Wu, "Improved Phase-Shifting Algorithm of Modular Multilevel DC/DC Converter for BESS Under Module Fault Conditions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 3, pp. 2718-2728, Jun. 2024.

[33] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4-30, Jan. 2015.

[34] Wolfspeed, Inc., "CAB650M17HM3 Silicon Carbide Power Module Datasheet," Jan. 2024. [Online]. Available: `https://assets.wolfspeed.com/uploads/2024/01/Wolfspeed_CAB650M17HM3_data_sheet.pdf`

[35] Wolfspeed, Inc., "CAB600M33LM3 3300 V Silicon Carbide Half-Bridge Power Module Datasheet," Rev. 3, Aug. 2025. [Online]. Available: `https://assets.wolfspeed.com/uploads/2024/01/3.3_kV_CAB600M33LM3_data_sheet.pdf`

[36] J. Teng, X. Sun, Y. Pan, X. Liu, Y. Zhang, W. Zhao, and X. Li, "An Inductive-Filtering Strategy of Submodule Ripple-Power in Triple-Port MMC-Based SST Applied to Hybrid Medium and Low Voltage AC/DC Interface," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8015-8028, Jul. 2022.

[37] J. Zhuang, M. Shi, W. Liu, G. Cai, and Y. Zhuang, "Solid-State Transformers for Medium Voltage PV Applications," in *Proc. 2026 Int. Power Electronics Conf. (IPEC-Nagasaki ECCE Asia)*, Nagasaki, Japan, 2026.

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