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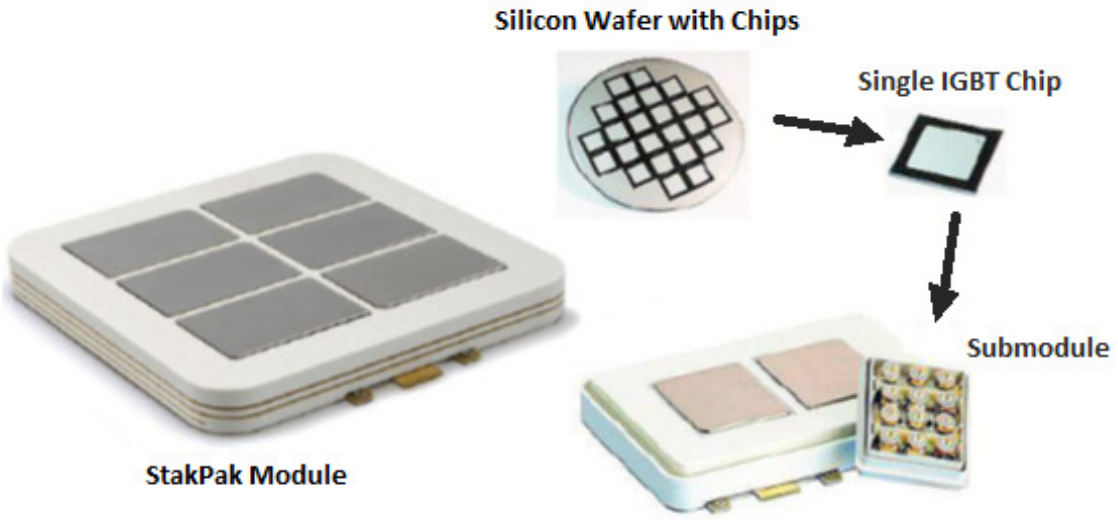

Evaluation of IGBT Gate Parasitics by Means of a PEEC Based Tool

Master of Science Thesis in Electric Power Engineering

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Gothenburg, Sweden, 2013

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by

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Abstract

In this thesis work, as a part of SEMikado project, a modeling platform is developed in BusBar Tool for studying the IGBT StakPak gate prints to be used in HVDC Light and SVC Light applications. Parasitic elements of two IGBT StakPak gate print designs have been extracted and the effects of several parameters including emitter plate, couplings and skin effect have been modeled and analyzed. SPICE models obtained from BusBar Tool simulations have been imported into PSpice and have been put into the desired test circuit in each simulation scenario to evaluate the IGBT positions. A PSpice circuital schematics test circuit has been built for studying the separated gate print which provides a better overview on parasitic elements. Two gate print designs have been compared through several simulation scenarios, regarding their parasitic elements, hence maximum voltage overshoots and time delays.

Key words: IGBT, parasitic elements, gate print, emitter plate, coupling effect, skin effect

Preface

Apart from my own efforts in this thesis work, it would have not been possible without the kind support and generous contributions of many individuals whom I am highly indebted to. I would like to gratefully acknowledge the supervision of Dr. Filippo Chimento and great support of Professor Lina Bertling Tjernberg during this project. I would also wish to express my sincere gratitude to Dr. Didier Cottet for his invaluable guidances and to Melek Mentes for his kind assistance.

Finally I would like to express my heartfelt thanks to my parents for all their encouragements and invaluable support, and to all my beloved ones for being beside me in all difficult moments.

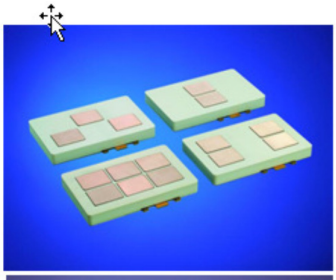
Aryan Madadi

CONTENTS

1 INTRODUCTION

Power transmission systems involving voltage source converters (VSC) offer several advantages compared to earlier technology based on thyristor current source converters (CSC) and forms a successful new product range within ABB labeled *HVDC Light™* and *SVC Light™*. Currently IGBT transistors are used for implementing the semiconductor valves required.

ABB portfolio considers several semiconductors solutions for its power system applications i.e. StakPak IGBT, HiPak IGBTs and IGCT.



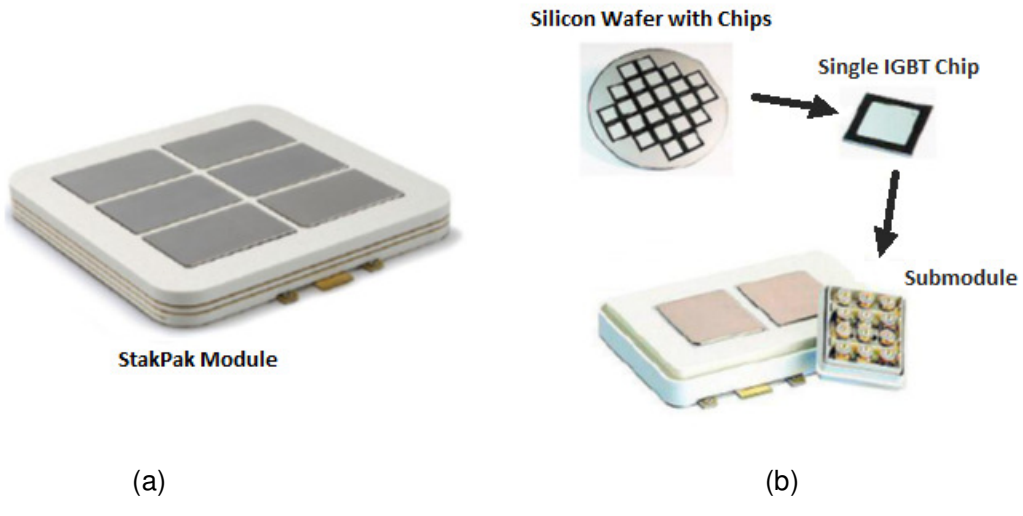
STAKPAK IGBT
- ABB is the only supplier and customer
- Expensive, complex packaging
- Modular in terms of current
- Made for series connection

IGCT
- ABB proprietary technology
- Three suppliers worldwide, several customers
- Robust semiconductor and package
- Low losses
- Series connection possible

HIPAK IGBT (wirebonded)
- Many suppliers and big overall market (drives, traction)
- Scale economies reduce cost
- Not inherently suited for series connection
- Siemens choice for HVDC PLUS

Figure 1-1: Choice of power semiconductors for VSC transmission applications

The IGBT StakPak power module and its hierarchical structure are shown in figure 1-2 [1].



(a) (b)

Figure 1-2: (a) An ABB StakPak power module, (b) hierarchical structure of a StakPak

In HVDC applications, dozens of IGBT packages are connected in series to block DC-link voltages up to several hundred kV. To avoid system shut-down due to a defect (1) redundant packages are included and (2) a stable short-circuit failure mode (SCFM) through the failed device is established by formation of a conductive alloy between an Al platelet and the Si chip.

The aim of this thesis work as a part of the SEMikado project is to develop a modeling platform for studying IGBT StakPak gate print designs, all-one and separated, to be used in HVDC Light and SVC Light applications. SEMikado (carried out at SECRC, project manager: Filippo Chimento) investigates and develops novel gate driving concepts and technologies targeted to the utilization with ABB semiconductor products.

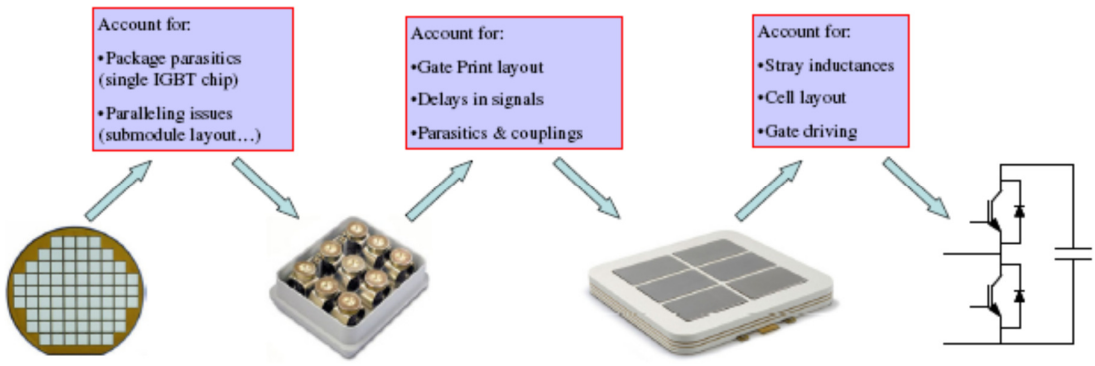


Figure 1-3: Overall modeling platform for semiconductor cells

2 STATE OF THE ART ANALYSIS

2.1 Insulated Gate Bipolar Transistor (IGBT)

IGBT modules are used as the active switches in whole range of power electronic appliances, especially high power converters, such as industrial motor drives, traction applications or pulsed power systems, due to their high-current density capability, high voltage ratings, low-power driving requirements and high switching speed.
In power electronic systems, high current ratings are typically achieved by parallel connection of semiconductor switching devices. The paralleling can be applied at different system levels such as paralleled IGBTs and diodes within modules, paralleled modules within subsystems or paralleled subsystems within systems.
As the required converter high blocking voltage in HVDC applications or multilevel converters exceed the maximum blocking voltage of a single IGBT, a series connection of several semiconductor devices is applied. The press pack IGBT was originally designed for these applications, where an easy series connection is achieved through a stacked construction. [2,3,4]

2.2 Parasitic Elements and their Effect

In order to reduce power losses and increase system power density, IGBT switching speeds in industrial motor drives continue to increase. These fast switching speeds, combined with high switching frequencies, have increased the interaction between the IGBT and the parasitic circuit elements distributed throughout all power electronic systems. Parasitics exist inside and outside the modules and can't be completely eliminated regardless of the kind of package and topology used. The interaction between the IGBT and parasitics can result in added power losses, an increase in the power device peak voltage and current, and ultimately power device failure.
Power device switching performance is strongly dependent on the operating conditions and layout of the gate drive and power circuits. The interaction of power devices with external parasitic circuit elements ultimately determines the behavior of the device switching transients. These parasitic circuit elements are present in all sections of the drive system including the power devices themselves. They are inherent in the device structure of the IGBT and are typically modeled as shown in Figure 2-1. Furthermore the device packaging, typically a power module, adds parasitic elements. The charging and discharging of the parasitic capacitance contributes to the IGBT switching behavior and power loss.

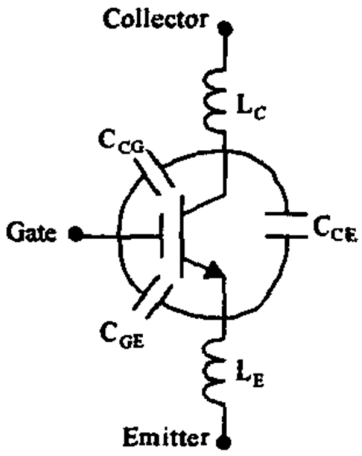


Figure 2-1: Equivalent circuit model of an IGBT showing the parasitic capacitive elements

The switching behavior of IGBTs is governed by many factors including the dc bus voltage, current magnitude, gate voltage, gate resistance, junction temperature, and circuit parasitic impedance. These factors affect the shape of the voltage and current waveforms and ultimately determine the power losses in an IGBT.

The total power loss generated by the semiconductor devices in any power electronics circuit are distributed between conduction and switching losses. The addition of reactive parasitic elements does not affect the conduction loss however the switching loss can increase in the presence of additional capacitance. Since the parasitic inductance resonates with the junction capacitance of the device and causes ringing in the circuit, which increases the switching losses. [2,5,6]

The parasitic inductance is also detrimental to the diode during turn-off. Due to the rapid change in current through the parasitic inductance during diode turn-off, the reverse voltage appearing across the device can be higher than the supply voltage, which may initiate the process of impact ionization in the device. Under uncontrolled circuit conditions, this may lead to the destructive breakdown of the device. [7]

In high power IGBT modules (up to 2kA and 6.5kV), where several chips are connected in a parallel configuration to achieve the specified high currents, the overall substrate area typically increases, the commutation current paths get longer, and the gate signals more difficult to route. These issues are related to module parasitics (i.e. resistances, inductances, mutual inductances, and capacitances) and need to be well controlled for optimum package design.

These parasitics have a major impact on the module's power losses, current distribution, switching waveforms and finally on the module's de-rating and reliability. Non-equal current loading of paralleled switches lead to unequal thermal losses within a power module. The optimum silicon utilization can only be achieved when losses are distributed equally, because otherwise hot-spots can degrade the module performance, reliability and lifetime. [3,4,8,9]

The parasitic inductance exists from the IGBT chip collector, emitter and gate to their terminal connections, no matter what kind of package is used. This inductance leads to several undesirable effects, such as over-voltage stress and ringing. Gate inductance in an IGBT module may lead to spurious turn-on or turnoff of the IGBT due to ringing during transitions. It has been shown that IGBT turn-on and turnoff

times are not only influenced by the input capacitance and the driver capability, but also IGBT internal stray inductance.

The influence of emitter lead inducatnce, L_E , has been carefully evaluated by Brambilla *et al.* It has been shown how the presence of L_E delays the turnoff of IGBT. In particular, as the collector current starts to fall, a certain negative voltage is applied across L_E due to the di/dt. This voltage reduces the driver voltage applied to the IGBT gate and the charge extraction capability of the gate driver, thus increasing the turn-off time of the IGBT. It should be noted that hard-switching turn-off of IGBT involves a storage time and fall-time of current. Unlike BJT, the voltage across the IGBT starts rising as soon as the gate voltage is turned-off. The storage time is due to the time required by the device voltage to rise to bus voltage, causing the clamping diode to turn-on. The subsequent fall-time is due to the trapped charge in the drift region. Since the inductor only delays the turn-off, it is difficult to extract its value based on the hard-switching turn-off. [10]

The most common implementation of the IGBT module is in switching system with Clamped Inductive Load (CLD). Distributed parasitics of a half bridge module together with the gate driver is illustrated in Figure 2-2.

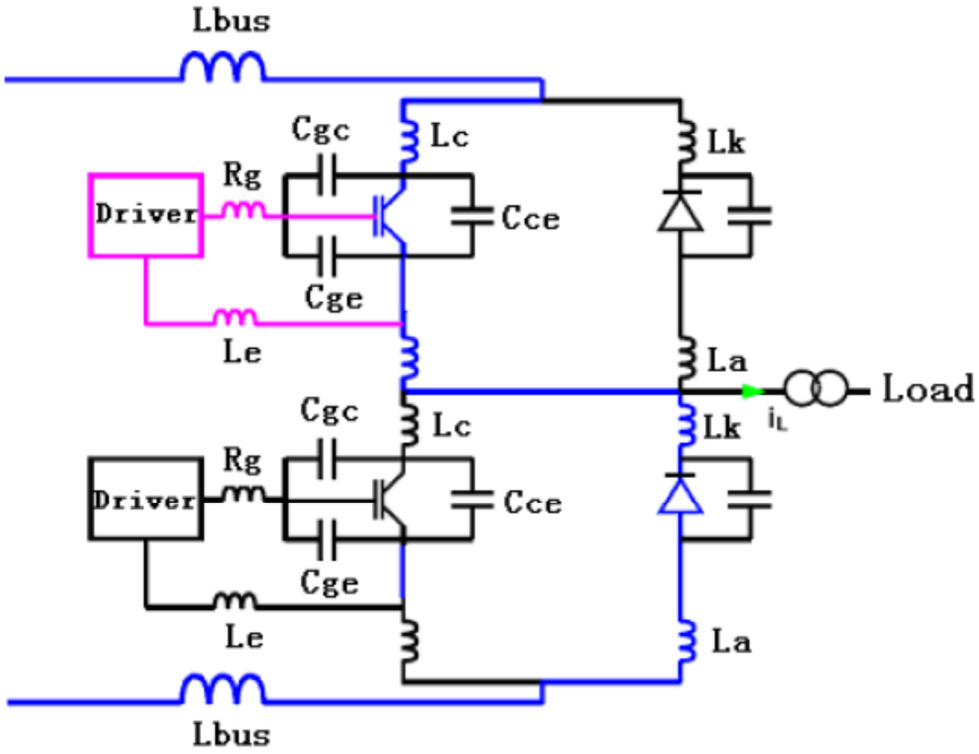


Figure 2-2: Distributed parasitics of a half bridge

A Auxiliary Emitter Inductance

There are three sources for parasitic auxiliary emitter inductance in series, the bond wire, the emitter lead and the printed circuit board wiring inductance between the lead and the common ground. At the beginning of the switching transitions, the gate current is increasing very rapidly. The rise of gate voltage will be slowed down based on the emitter inductor. Consequently, the time required to turn-on or turn-off the IGBT gets longer, it's called delays time.

B Collector Inductance

Another parasitic inductance of the switching network is the collector inductance L_C, which is composed of several components. They are the bond wire, power terminal and DC busbar inductance. Their effect can be lumped together since they are in series. During turn-on they limit the di/dt of the collector current and reduce the collector to emitter voltage across the chips. In fact, L_C can reduce the turn-on losses significantly, but considerable problems are encountered at turn-off when the collector current must ramp down quickly.

C Gate Mesh Resistance

The next important parameter to mention is the gate mesh resistance, $R_{G,IN}$. This parasitic resistance describes the resistance associated by the gate signal distribution within the device. Its importance is very significant in high speed switching applications, because it is in between the gate driver and the input capacitor of the IGBT.

D Capacitor of Free Wheel Diode

In general an anti-parallel diode chip is also used in conjunction with IGBT chip. It becomes important to characterize whole IGBT module for accurate prediction of the performance of both the devices instead of characterizing independently. [2]

Typical package components of power modules are power and auxiliary terminals, substrate copper metallization, base plates, and externally also heat sinks and bus bars attached to the modules. [6]

Base on the circuit operation analysis and measurement of IGBT characteristics, it's shown that the larger parasitic loop inductance will result in more turn-off losses but less turn-on losses, while the emitter inductance of the IGBT also has a significant effect on the gate drive circuit because it's included not only in the main power circuit but also in the gate drive circuit. It's proved that the emitter inductance slows down the turn-on and turn-off procedure thus increases the turn-on and turn-off switching power losses. [11]

2.3 Parasitics Influence on Paralleled IGBTs

2.3.1 Chips In Parallel

The increasing power ratings of converters necessitate power modules with higher ampacity. Thus, high power electronic module usually contains a number of transistors in parallel to provide higher currents. The overall substrate area typically increases, the commutation current paths get longer, and the gate signals more difficult to route. The imbalance among the layout impedances associated with the layout results in high current spikes and long time lags among the paralleled devices. The imbalance of currents can cause quite different junction temperatures, degrading reliability of the power modules. [2]

2.3.2 Modules In Parallel

Though IGBT chips in parallel is the basis, paralleled IGBT modules is more practical for most user. [2]

2.4 Press-pack IGBTs

The press-pack IGBT module is designed for a low inductance series connection in a module stack, where additional requirements such as a uniform mechanical pressure distribution or a proper handling of fault conditions are essential. Additionally, the pressure contacted switches exhibit advantageous thermomechanical properties, which lead to an increased module lifetime in comparison to bonded IGBT modules, where thermal load cycles are causing bond wire lift-off. In these high voltage IGBTs, switching losses are dominant in comparison to conduction losses.
The press-pack IGBT module is designed with a short and hence a very low inductance collector-emitter current path. Figure 2-3 shows an explosion drawing of the power module internals. When the switch is in on-state, the current enters the collector plate (bottom), propagates through the semiconductors into the press-pack spring connectors and leaves the module through the emitter plate (top). [3]

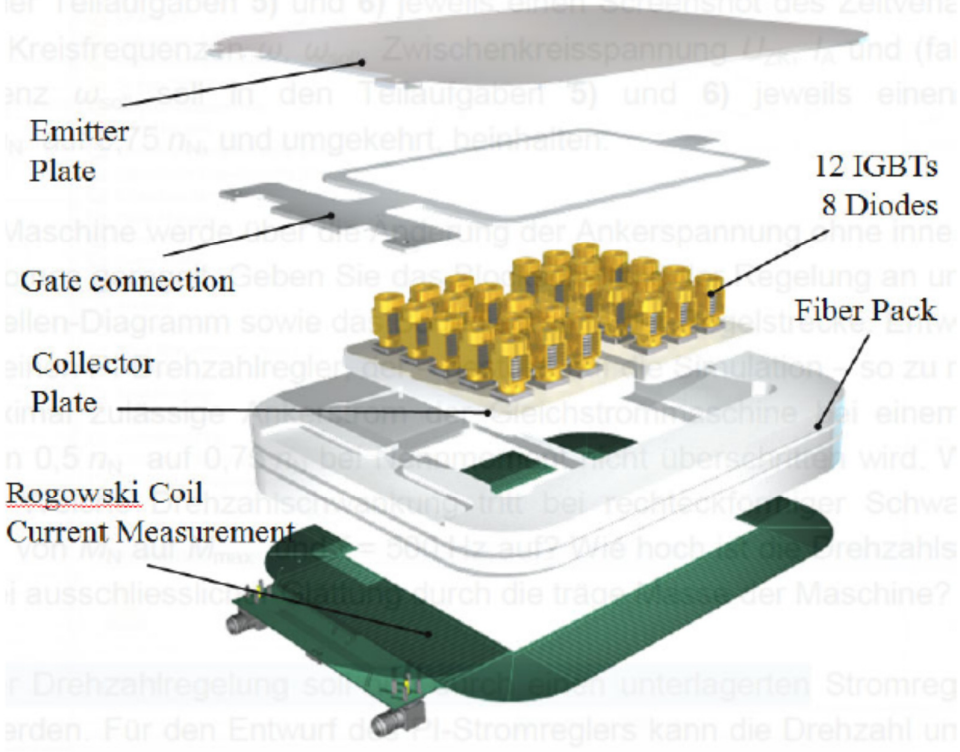


Figure 2-3: CAD explosion drawing of the stack pack IGBT power module.

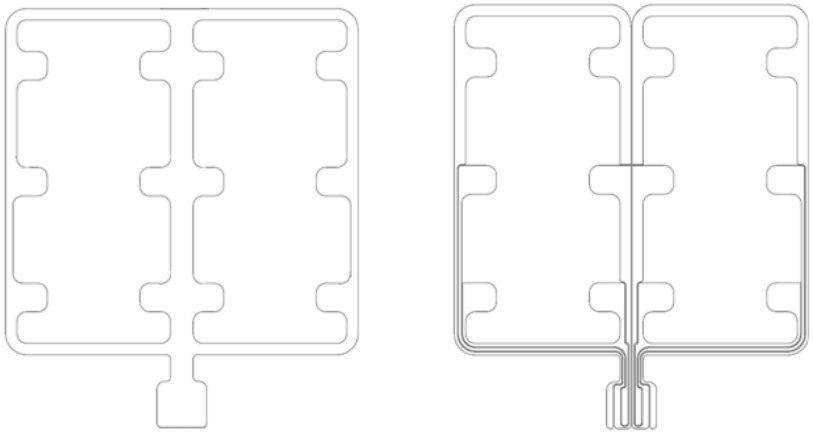
Measurement of the internal module electromagnetic effects is quite cumbersome, especially when they are done in high voltage environment during operation. Typically the accessibility inside the modules is limited, isolation requirements are difficult to respect and interferences with the measurement equipment unavoidable. For that reason, a simulation approach is applied to gain insight into the electromagnetic effects. [3,6]

It has been stated in several publications that a finite element method (FEM) based software is not very well suited for such kind of simulation, because the large aspect ratio between width and height of flat conducting structures leads to an excessive mesh refinement in FEM solvers, and thus to long simulation times and convergence problems.[3]

Therefore in this work the software BusBar Tool has been used which is based on Partial Element Equivalent Circuit (PEEC) method. Skin- and proximity effect have been considered in the simulations and stray inductances and couplings between power and gate circuits in the internal module interconnection paths which lead to switching delays have been extracted.

3 MODEL DESCRIPTION AND ITS OUTCOMES

As discussed earlier in the introduction the new design of the gate print so called "separated gate print", due to the separations between the gate paths, has been studied and compared with the previous design so called "all-one gate print" regarding their parasitic elements. Figure 3-1 shows the previous and new gate prints respectively. Both gate prints are belonging to a 6 sub-module IGBT StakPak. In the case of all-one gate print there is a common gate path for all sub-modules, while in the case of separated gate print each sub-module has a particular gate path which receives the gate signal from the gate unit independently from the other sub-modules and transfer it to the gates of IGBTs in the respective sub-module.



(a) (b)

Figure 3-1: (a) All-one gate print, (b) Separated gate print

The separations between the gate paths of the new design bring the following advantages over the previous design:

- Increasing the reliability
- Providing an extended functionality for different sub-parts
- Improving the protection circuit

On the other hand it leads to some new challenges which are going to be studied in this thesis work:

- Gate paths with different shapes and lengths are formed, which lead to different values of inductances (L) and resistances (R) for each gate path
- The independency between the sub-modules gate paths and the different values of R and L for each gate path mean that the gate signals might be received by different time delays leading to unbalanced switching of IGBTs

- Plenty of mutual couplings are created which intensify the parasitic effects such as voltage spikes and unbalanced transient current sharing between paralleled IGBTs
- Different junction temperatures (future work)

Together with the gate print, either separated or all-one, the emitter plate which is located in 1.6 mm distance from the module gate print should be modeled as well. Due to its small distance from the gate print it affects on the impedance values through induced eddy currents and also it forms the return path for the gate-emitter voltage applied to IGBTs. Therefore the studied models in this project include the gate print and the emitter plate.

The approach to the model studies in this project is Partial Element Equivalent Circuit (PEEC) method, because of its strengths and advantages in studying the power electronic systems.

4 BUSBAR TOOL MODELING

4.1 Introduction to BusBar Tool [12]

BusBar Tool is a modeling interface with electromagnetic solvers which performs numerical simulations. The software is based on the partial element equivalent circuit method (PEEC) and includes MultiPEEC software from Luleå University of Technolgy, Sweden. BusBar Tool is developed in ABB Corporate Research Center in Switzerland and is ABB proprietary.

Figure 4-1: BusBar Tool software, ABB proprietray

BBT software has a graphical user interface (GUI) dedicated to geometry and material definition, simulation parameters setup, result analysis and post-processing including plotting current density distribution and electromagnetic field patterns. BusBar Tool is specifically designed and developed as a three dimensional bus bar simulation tool, but due to its accuracy in studying the power electronic systems, we have used it for studying the gate print of IGBT StakPak in this thesis work.

BBT is capable of performing the following simulations:

- Impedance extraction
- AC frequency sweep
- Transient analysis
- RL matrix impedance extraction

The latest simulation is of our interest in this work, which generates the following outputs:

- SPICE models for desired frequencies
- Voltage distribution
- Current density distribution

BusBar Tool was chosen as the modeling software in this project because it is an ABB proprietary based on the advantages PEEC method, and as mentioned above it is able to display the simulation results in the form of SPICE outputs, which is of our interest due to the previous accomplishments in SPICE.

4.2 Model Geometry Preparation

The first step in PEEC method, is the 3D description and material definition of the model structure to be simulated. In BusBar Tool software complex geometries can be built by attaching a number of blocks.

Figure below shows the dimensions of the separated gate print, which are the same for the all-one gate print excluding the separations. The thickness of both gate print designs is 15.5 µm which is not shown in the figure 4-2. The material of both gate prints is Cupper.

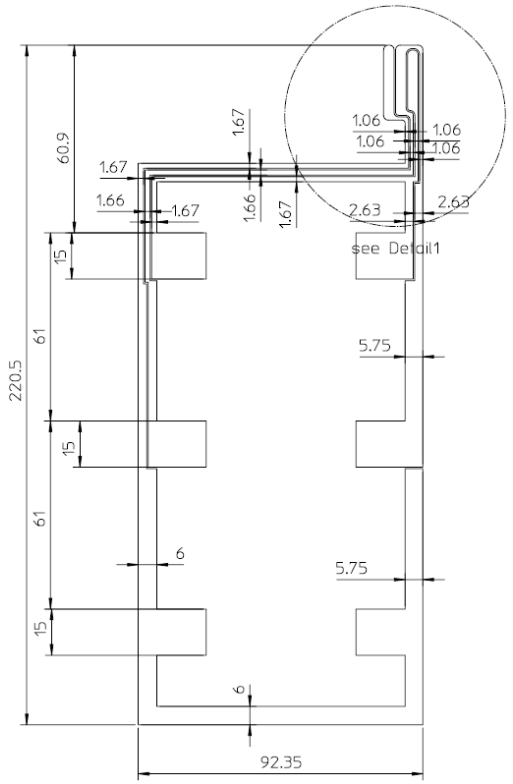


Figure 4-2: Separated gate print dimensions

Figure 4-3 shows the separated gate print and the emitter plate modeled in BusBar Tool software. The model is built considering the fact that it is not possible to model the curvatures in this software.

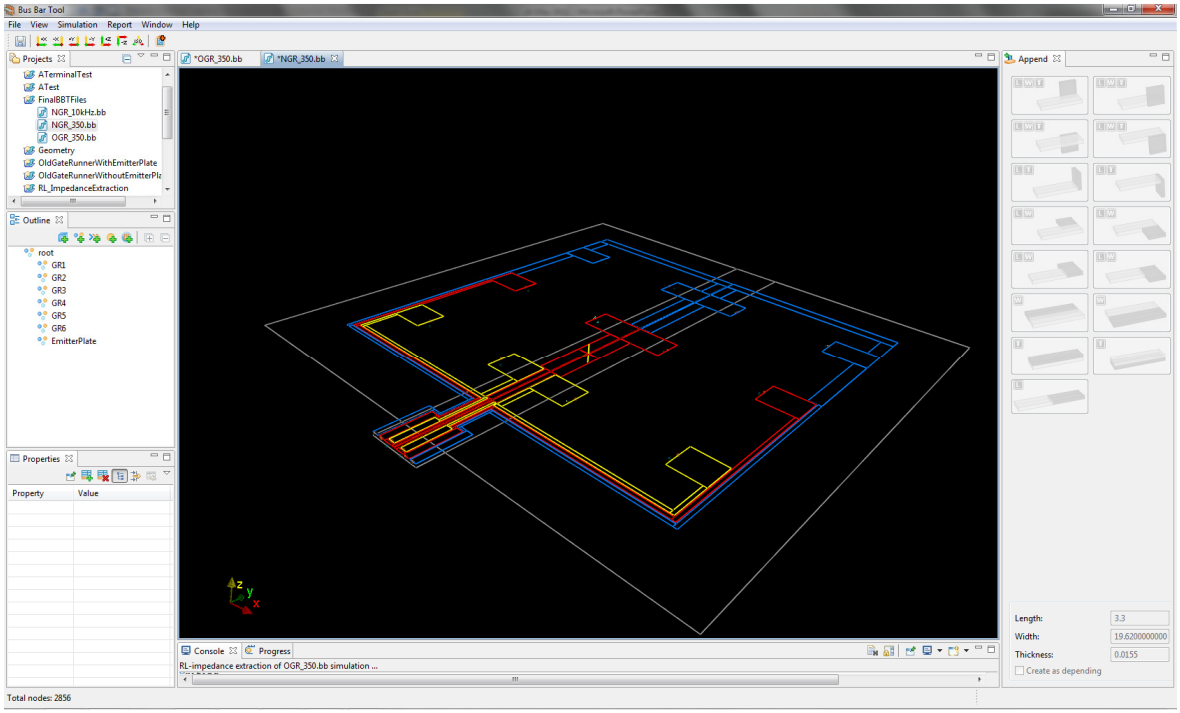


Figure 4-3: Separated gate print and the emitter plate modeled in BusBar Tool software

4.3 Terminal Location

Terminals are the access points to the model geometry which should be placed in the correct locations before performing the parasitic extraction. This is explained further in the section 4.5.

In the case of separated gate print, three terminals have been placed on each gate path. One input terminal at the point where the gate signal is received from the gate unit, and two output terminals at the points where the gate signal is transmitted to the gates of the IGBTs in each sub-module, as shown in figure 4-4 as an example. Three terminals for each of the six gate paths mean that 18 terminals in total have been placed over the separated gate print.

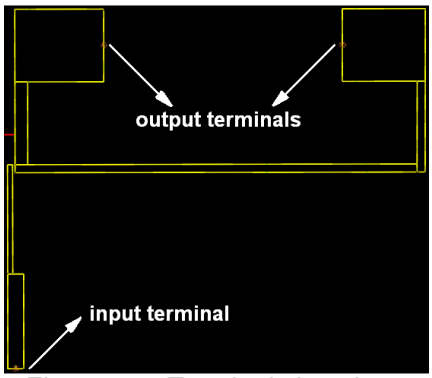


Figure 4-4: Terminals locations

In the case of all-one gate print, one input terminal has been placed for the whole gate print at the point where the gate signal enters to the gate print, and six output terminals have been placed at the points where the gate signal is transmitted to the gates of the IGBTs in each sub-module, which are the same points as output terminals of the separated gate print.

There are two input terminals placed on the emitter plate, one for each half, at the point where the gate unit is connected to the emitter plate, which is almost beneath the gate print input terminal. And there are twelve output terminals placed on the emitter plate, right beneath the output terminals of the gate print.

4.4 Model Geometry Meshing

The second step in PEEC method, is subdividing the geometry according to the problem to be simulated. Subdividing the geometry in BBT can be performed by meshing the building blocks manually, means by determining the number of meshing for length, width and thickness of each single block.

In order to be able to determine the required fineness of the accurate meshing for the studied model, first the input signal which is the gate voltage was decomposed to its constituent frequencies by the help of FFT (Fast Fourier Transform). Then in the next step the mesh size was set according to the skin depth at the dominant frequency.

The gate voltage source in this work has the following characteristics:

Value when the pulse is not turned on (V1) = -5 V

Value when the pulse is fully turned on (V2) = 15 V

Delay time (TD) = 1 µs

Rise time (TR) = 0.5 µs

Fall time (TF) = 0.5 µs

Pulse width (PW) = 10 µs

Period (PER) = 100 µ

Figure 4-5 shows the above mentioned gate voltage signal simulated in PSpice, and Figure 4-6 and 4-7 show its FFT result.

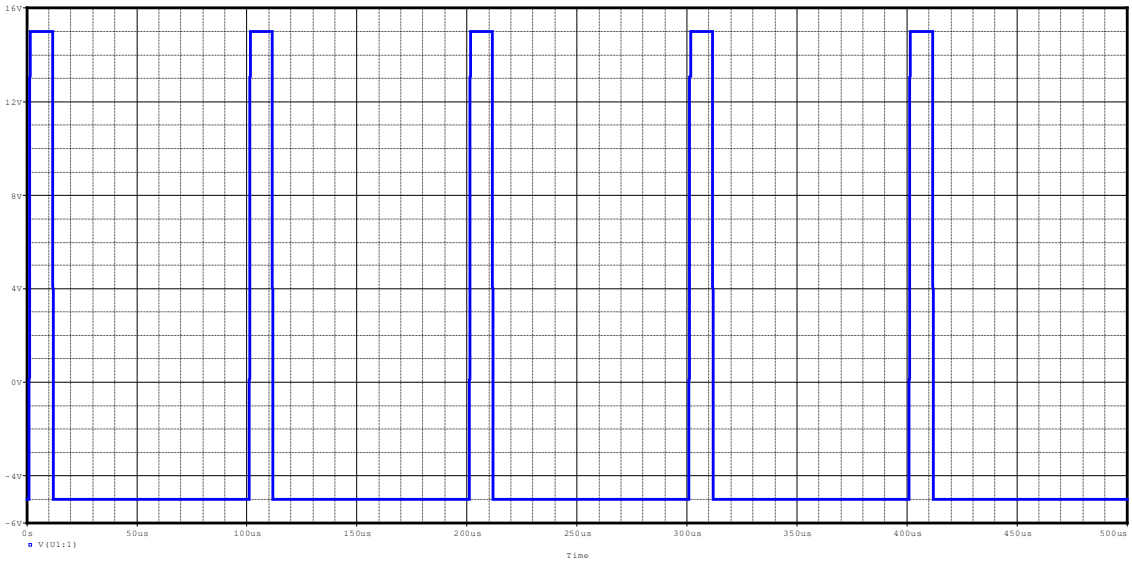


Figure 4-5: Simulated gate voltage signal in PSpice

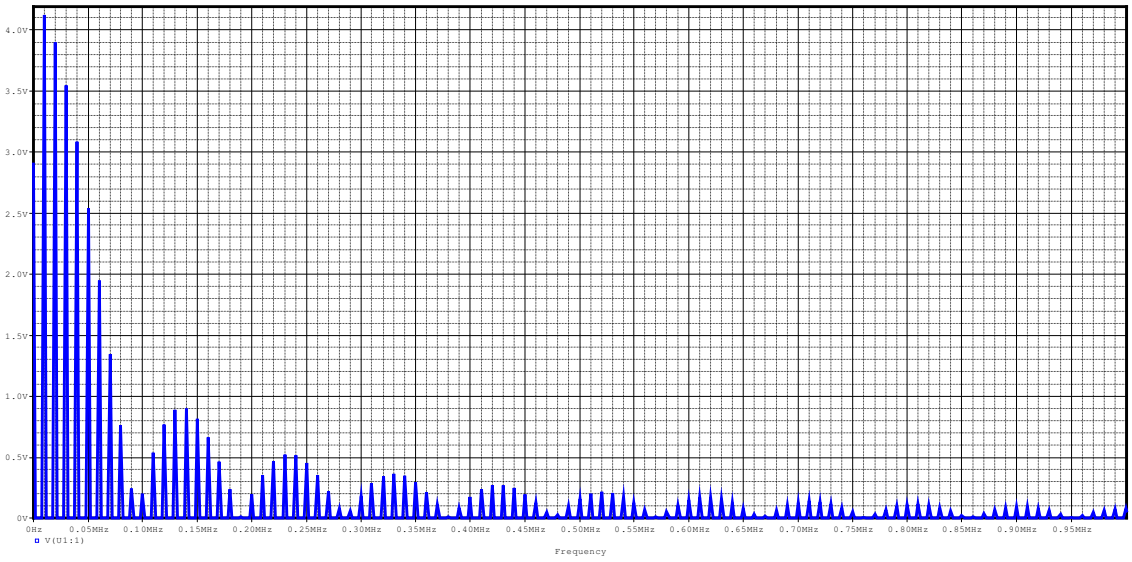


Figure 4-6: FFT result of the gate voltage signal

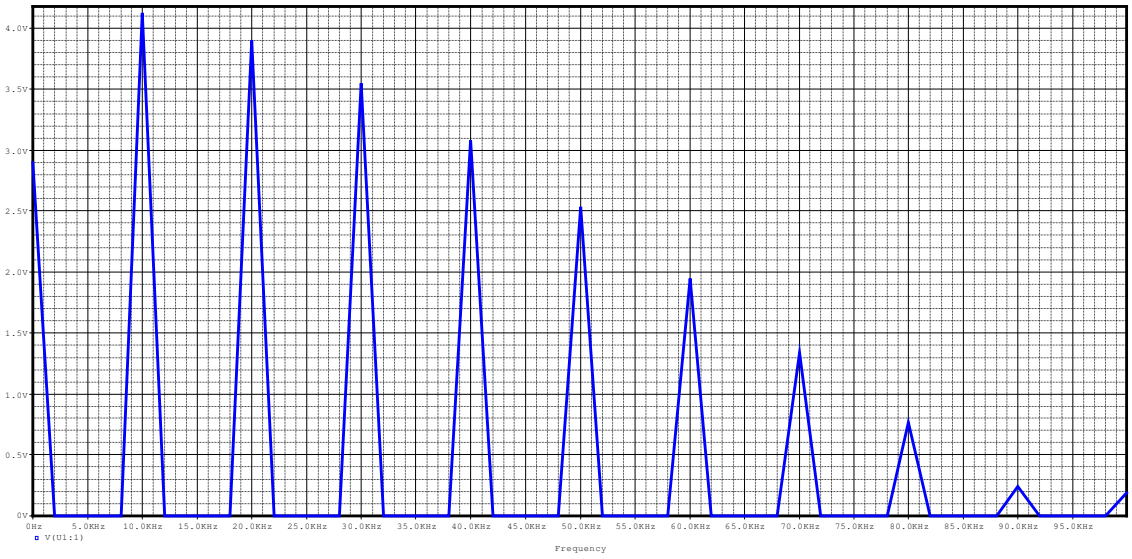


Figure 4-7: Zoomed in FFT result of the gate voltage signal

As it can be seen in the figures above, the dominant frequency of the gate voltage signal is 10 kHz. It means that it is required to fine the mesh sizes up to the skin depth at 10 kHz. The skin depth is calculated by the following formula:

$$\delta = \sqrt{\frac{2}{\omega \, \mu \, \sigma}}$$

δ : Skin depth [m]

ω : Angular frequency of current = 2π × frequency

μ : Absolute magnetic permeability of the conductor = 1.2566290 × 10^{-6} [H/m] for Copper

σ : Conductivity of the conductor = 5.88 × 10^{7} [S/m] for Copper

The skin depths at frequencies up to 10 kHz have been calculated and the result can be seen in the table below:

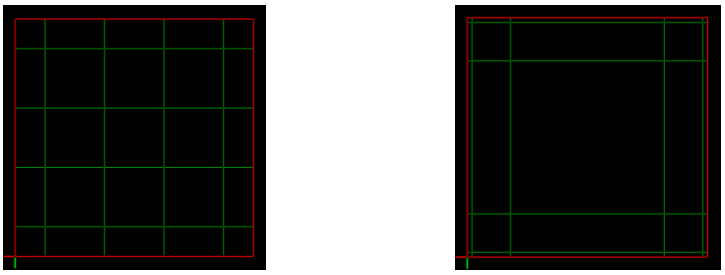
Table 4-1: Skin depth at different frequencies

	Frequency [kHz]						
	0.350	**1**	**2**	**3**	**4**	**5**	**10**
Skin Depth [mm]	3.50	2.075	1.467	1.198	1.037	0.928	0.656

As a common rule in numerical methods, there should be a few mesh layers in the studied area, in order to obtain an accurate result. In this case, the studied area is

limited to the skin depth, which requires a dense mesh, while it will be useless to apply that dense mesh to the areas deeper than the skin depth, since they do not contain much current density and applying a dense mesh to them will only lead to longer simulation time and convergence problem. This necessitates a non-uniform meshing.

BusBar Tool has made the non-uniform meshing possible by adding the feature of mesh ratio. This feature allows meshing of areas and cross sections with higher mesh density at the edges by providing a ratio between the subsequent discretization steps toward the borders [12]. Figure 4-8 shows the surface view of a cross section with (a) uniform meshing with meshing ratio equal to one and (b) non-uniform meshing with meshing ratio equal to four.



(a) (b)

Figure 4-8: Surface view of a cross section with (a) uniform meshing with meshing ratio equal to one and (b) non-uniform meshing with meshing ratio equal to four

In BusBar Tool, there are two parameters, n and r, which should be expressed for defining the mesh quality in each dimension of a block. n+1 represents the number of segments and r is the ratio between two adjacent segments. By matching the outermost cell size to the skin depth, it is possible to reflect the skin effect with using the minimum number of cells and consequently less simulation time [13].

In this project, the outermost cell sizes should be set to 0.656 mm which is the skin depth at 10 kHz (see table 4-1). In order to be able to determine the correct values of n and r for each block, the following tables were calculated for a sample segment with the width of W.

Table 4-2: The outermost cell size for different values of n and r

		N						
		1	**2**	**3**	**4**	**5**	**6**	**7**
r	**1**	$\frac{W}{2}$	$\frac{W}{4}$	$\frac{W}{6}$	$\frac{W}{8}$	$\frac{W}{10}$	$\frac{W}{12}$	$\frac{W}{14}$
	2	$\frac{W}{2}$	$\frac{W}{6}$	$\frac{W}{10}$	$\frac{W}{18}$	$\frac{W}{26}$	$\frac{W}{42}$	$\frac{W}{58}$
	3	$\frac{W}{2}$	$\frac{W}{8}$	$\frac{W}{14}$	$\frac{W}{32}$	$\frac{W}{50}$	$\frac{W}{104}$	$\frac{W}{158}$
	4	$\frac{W}{2}$	$\frac{W}{10}$	$\frac{W}{18}$	$\frac{W}{50}$	$\frac{W}{82}$	$\frac{W}{210}$	$\frac{W}{338}$
	5	$\frac{W}{2}$	$\frac{W}{12}$	$\frac{W}{22}$	$\frac{W}{72}$	$\frac{W}{112}$	$\frac{W}{372}$	$\frac{W}{622}$
	6	$\frac{W}{2}$	$\frac{W}{14}$	$\frac{W}{26}$	$\frac{W}{98}$	$\frac{W}{170}$	$\frac{W}{602}$	$\frac{W}{1034}$
	7	$\frac{W}{2}$	$\frac{W}{16}$	$\frac{W}{30}$	$\frac{W}{128}$	$\frac{W}{226}$	$\frac{W}{912}$	$\frac{W}{1598}$

Table 4-3: The cell sizes of a segment in case of using n=2

		n = 2
r	**1**	$\frac{W}{4}, \frac{2W}{4}, \frac{W}{4}$
	2	$\frac{W}{6}, \frac{4W}{6}, \frac{W}{6}$
	3	$\frac{W}{8}, \frac{6W}{8}, \frac{W}{8}$
	4	$\frac{W}{10}, \frac{8W}{10}, \frac{W}{10}$
	5	$\frac{W}{12}, \frac{10W}{12}, \frac{W}{12}$
	6	$\frac{W}{14}, \frac{12W}{14}, \frac{W}{14}$
	7	$\frac{W}{16}, \frac{14W}{16}, \frac{W}{16}$

Table 4-4: The cell sizes of a segment in case of using n=3

		n = 3
r	1	$\frac{W}{6}, \frac{2W}{6}, \frac{2W}{6}, \frac{W}{6}$
	2	$\frac{W}{10}, \frac{4W}{10}, \frac{4W}{10}, \frac{W}{10}$
	3	$\frac{W}{14}, \frac{6W}{14}, \frac{6W}{14}, \frac{W}{14}$
	4	$\frac{W}{18}, \frac{8W}{18}, \frac{8W}{18}, \frac{W}{18}$
	5	$\frac{W}{22}, \frac{10W}{22}, \frac{10W}{22}, \frac{W}{22}$
	6	$\frac{W}{26}, \frac{12W}{26}, \frac{12W}{26}, \frac{W}{26}$
	7	$\frac{W}{30}, \frac{14W}{30}, \frac{14W}{30}, \frac{W}{30}$

Table 4-5: The cell sizes of a segment in case of using n=4

		n = 4
r	1	$\frac{W}{8}, \frac{2W}{6}, \frac{2W}{6}, \frac{2W}{6}, \frac{W}{8}$
	2	$\frac{W}{18}, \frac{4W}{18}, \frac{8W}{18}, \frac{4W}{18}, \frac{W}{18}$
	3	$\frac{W}{32}, \frac{6W}{32}, \frac{18W}{32}, \frac{6W}{32}, \frac{W}{32}$
	4	$\frac{W}{50}, \frac{8W}{50}, \frac{32W}{50}, \frac{8W}{50}, \frac{W}{50}$
	5	$\frac{W}{72}, \frac{10W}{72}, \frac{50W}{72}, \frac{10W}{72}, \frac{W}{72}$
	6	$\frac{W}{98}, \frac{12W}{98}, \frac{72W}{98}, \frac{12W}{98}, \frac{W}{98}$
	7	$\frac{W}{128}, \frac{14W}{128}, \frac{98W}{128}, \frac{14W}{128}, \frac{W}{128}$

It should be mentioned that the number of meshing nodes does not depend on the meshing ratio (r), but only on the number of segments (n+1).

Since current flow between the adjacent blocks in BBT is only possible through the common meshing points, so called nodes, the “meshing node to node requirement” should always be followed in order to keep the electrical contact between the adjacent blocks. This was one of the biggest troubles in working with BBT to match the outermost cell size to the skin depth and follow the meshing node to node requirement at the same time. Considering the different dimensions of adjacent blocks in the model geometry, it was very difficult to set the number of meshing in each dimension of a block in a way that it would lead to the outermost cell size

matching with the skin depth and also common nodes with its adjacent blocks which have different dimensions.

Another challenge in applying a suitable meshing to the model geometry in BBT is that too few common nodes between the interconnected blocks leads to incorrect current density and too many common nodes (in case of dense meshing) leads to long simulation times [13]. Therefore, although the current density was not of interest in this thesis work, still finding a trade-off between the simulation time and the meshing accuracy was a hard task in this project. It should be highlighted here that the number of meshing nodes is one of the affecting parameters on BBT simulation time.
Based on the calculated cell sizes presented in tables 4-2 through 4-5 and by considering the skin depth and meshing node-to-node requirement, the values of n and r have been determined for all dimensions of the gate print geometry for 350 Hz and 10 kHz as in table 4-6.

Table 4-6: n and r values of each model geometry dimension for 350 Hz and 10 kHz

	f = 350 Hz	**f = 10 kHz**
Dimensions (mm)	**Skin Depth = 3.50 mm**	**Skin Depth = 0.656 mm**
1.06	n = 1 , r = 1	n = 1 , r = 1
1.66	n = 1 , r = 1	n = 2 , r = 1
1.67	n = 1 , r = 1	n = 2 , r = 1
2.63	n = 1 , r = 1	n = 2 , r = 1
3.3	n = 1 , r = 1	n = 2 , r = 2
5.75	n = 1 , r = 1	n = 2 , r = 4
6	n = 1 , r = 1	n = 2 , r = 4
15	n = 2 , r = 2	n = 3 , r = 6
17.17	n = 2 , r = 2	n = 3 , r = 7
18.37	n = 2 , r = 2	n = 3 , r = 7
19.33	n = 2 , r = 2	n = 3 , r = 7
21.5	n = 2 , r = 3	n = 4 , r = 4

Since the current paths in the emitter plate will probably follow the gate traces, the emitter plate meshing should be in a way to allow that. Hence a non-uniform meshing may not be suitable. Therefore, a uniform meshing has been used for the emitter plate.

It should be added that another trouble in working with BBT was that later on during the simulations it was found out that if a terminal was not located exactly on a meshing node, it would automatically snap to the closest meshing node, even if it was located on another block or another element. And this would waste all the simulation time and efforts since it would lead to wrong simulation results; the reason for that was unknown until finding out this bug in the software. Therefore, it was really exhausting to obtain a correct meshing in BBT considering all of its weaknesses.

4.5 RL Impedance Extraction

As mentioned earlier, RL Impedance Extraction simulation was of interest in this project since it is able to generate SPICE models from the studied geometries by calculating all resistances, inductances, mutual couplings and sources. For performing this simulation, it is required to introduce the access points on the model, which are terminals. An ordered list of terminals which are connected through a DC path forms a net, and a pair of two terminals from a common net form a port. For each specified frequency a SPICE model will be generated which contains the impedance value of each port in the model and the value of mutual couplings between the different ports calculated at that specific frequency. After accomplishment of this simulation a number of files will be generated in the output directory. A folder containing .vtk files will be generated which are currents, current densities and voltage values. The .m files include the voltage vector components, a .inp file saves the MultiPEEC solver input and a .srf file shows the 3D simulation results. There will be a .sp file generated for each specified frequency which contains the corresponding SPICE model extracted from the model geometry.

Figure 4-9 shows the shortest gate path existing in the separated gate print, with non-uniform meshing matched to the skin depth of 350 Hz, and the figure 4-10 shows the SPICE model generated from RL Impedance Extraction of the mentioned model at 350 Hz simulation frequency.

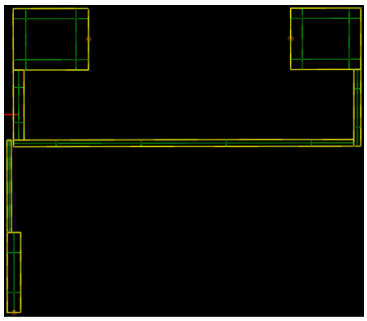


Figure 4-9: Single gate path with non-uniform meshing matched to the skin depth of 350 Hz

```
* Creator: ABB Bus Bar Tool
* Project: SingleGatePathWithoutEmitterPlate
* Model: NGR_GR1_350.bb
* Author: SEARMAD
* Frequency: 350.0
* Date: Mon Jul 25 10:16:09 CEST 2011
* Terminals:
*          1 = root.GR1.terminalD
*          2 = root.GR1.terminalUL
*          3 = root.GR1.terminalUR
.subckt BusBar 1 2 3
LZ_0 1 int_node0_2 6.67077e-08
LZ_1 1 int_node1_2 1.41496e-07
KZ_1_0 LZ_1 LZ_0 0.486998
RZ_0_0 int_node0_2 int_node0_3 0.0412033
HZ_0_1 int_node0_3 int_node0_4 Vam_1 0.0310013
Vam_0 int_node0_4 2 dc 0
HZ_1_0 int_node1_2 int_node1_3 Vam_0 0.0310013
RZ_1_1 int_node1_3 int_node1_4 0.100973
Vam_1 int_node1_4 3 dc 0
.ends BusBar
```

Figure 4-10: SPICE model generated from RL Impedance Extraction of the gate path shown in figure 3-9 at 350 Hz

In order to have a better understanding from the RL Impedance Extraction output, it is necessary to go through the generated SPICE model. As mentioned earlier three terminals have been located on the studied gate path, which are visible in figure 4-9. As it can be seen in figure 4-10 a node number has been assigned to each of these three terminals throughout the RL Impedance Extraction simulation. Terminal D, which is the input terminal of the studied gate path model, is considered as node 1. Terminals UL and UR which are the output terminals are considered as nodes 2 and 3 respectively. Figure 4-11 gives a clearer picture of the SPICE model shown in figure 4-10.

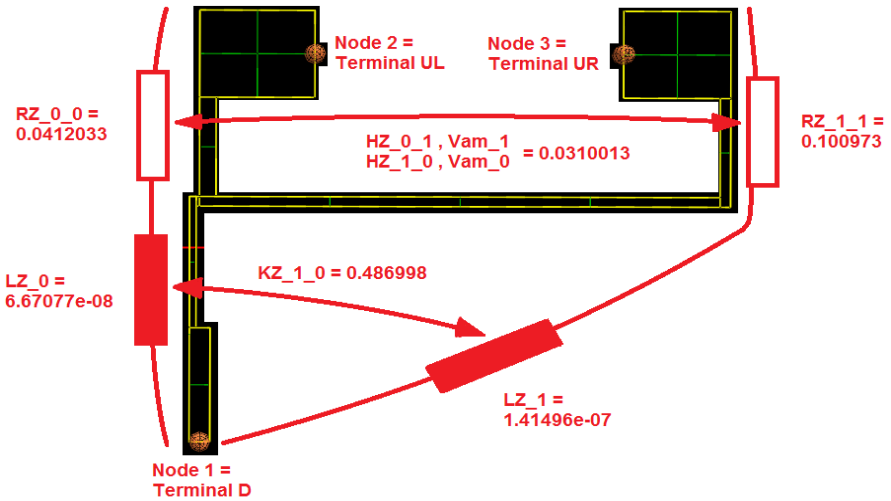


Figure 4-11: Interpreted SPICE model shown in figure 4-10

It is possible to sketch the electrical circuit corresponding to each generated SPICE model. Figure 4-12 shows the electrical circuit corresponding to the SPICE model shown in figure 4-10, built in PSpice.

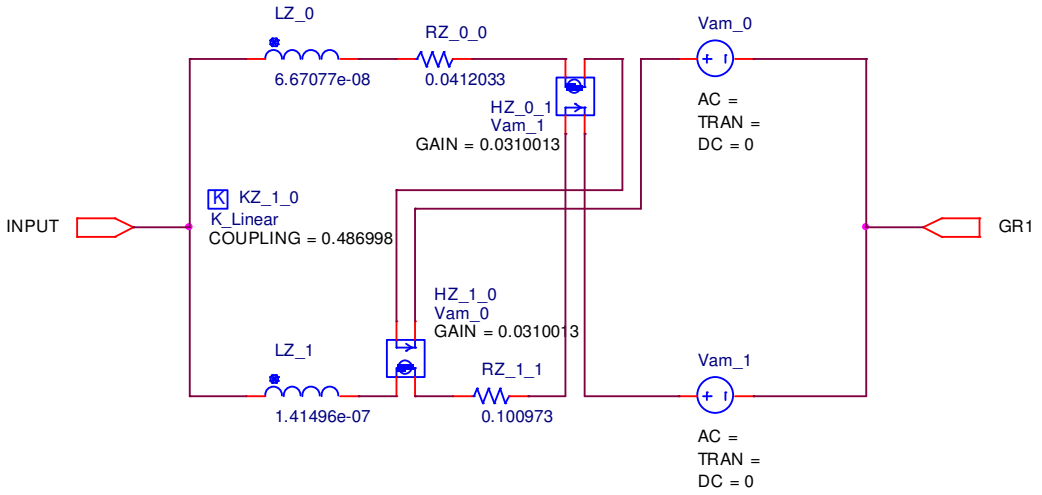


Figure 4-12: Electrical circuit corresponding to SPICE model shown in figure 4-10

It should be explained that LZ and RZ components are the self inductances and resistances respectively. There is always a mutual inductance (M) for each pair of inductors in SPICE, which is defined by the coupling coefficient KZ. The value of coupling factor must be equal to or between zero and one $(0 \leq \mathrm{KZ} \leq 1)$, and is calculated by $\frac{\mathrm{M}}{\sqrt{\mathrm{L1L2}}}$. HZ components are current controlled voltage sources which are used to model the mutual resistances. The controlling currents are measured by Vam components which are the zero value DC voltage sources.

As mentioned earlier each pair of two terminals from a common net forms a port. There will be a resistance, an inductance, and a mutual resistance value calculated for each port, and a mutual inductance calculated for each pair of inductances. As it can be seen in figure 4-11 as an example, the first port is formed between the terminals D and UL and the second port is formed between the terminals D and UR. Consequently a resistance, an inductance, and a mutual resistance value have been calculated for each of these ports, and a mutual inductance has been calculated between the two self inductances.

Since the studied model in this case was a single element with only two ports created from its three terminals, see figure 4-9, it led to a short SPICE model as in figure 4-10, with a few number of elements. But the generated SPICE models are not always as short as the one presented in figure 4-10. As soon as the number of terminals, hence number of ports increase the size of the corresponding SPICE model increases due to the increased number of elements including resistances, inductances, mutual resistances and mutual inductances. It should be noted that for any “n” number of ports, there will be “n” number of resistances, “n” number of

inductances, n(n-1) number of mutual resistances, and $\frac{n(n-1)}{2}$ number of mutual inductances.

In the case that gate print, either all-one or separated, and emitter plate are studied together and modeled completely there will be 24 ports created, which leads to generation of 24 resistances, 24 inductances, 276 mutual inductances and 552 mutual resistances, which forms a 17 pages SPICE netlist.

It is noteworthy that the RL Impedance Extraction simulation time increases with the number of terminals, hence the number of elements which should be calculated for each SPICE model. Another affecting parameter on RL Impedance Extraction simulation time is the number of meshing nodes which is explained in section 4.4.

5 SPICE SIMULATIONS AND RESULTS

5.1 Simulation Scenarios

As it was mentioned earlier, two IGBT StakPak gate print designs are studied and compared in this project regarding their parasitic elements. The effect of some important parameters including emitter plate, couplings between the gate paths, and skin effect have been analyzed and determined as well. In order to cover all mentioned studies the simulations have been performed in different scenarios.

In the first simulation scenario, separated gate print has been studied without and with emitter plate respectively. The effects of emitter plate, couplings, and meshing frequency have been determined in the next scenarios. The circuital schematics approach for the case of separated gate print has been presented, all-one gate print has been studied without and with emitter plate respectively, and two gate print designs have been compared regarding their parasitic elements in the next scenarios.

5.2 Importing BusBar Tool Output into PSpice

In order to study the effect of extracted parasitic elements, the SPICE models should be put into the desired test bench in a simulation software, such as PSpice in this project. Therefore it is necessary to first import the generated SPICE models into PSpice. There are two ways for performing this.

The first way is to sketch the electrical circuits corresponding to the generated SPICE models by interpreting their netlists, which was explained in the section 4.5. The drawback of this way is that it is only feasible for the short netlists such as the one shown in figure 4-10. Because in case of a long netlist there are plenty of coupling elements between the ports and this leads to a huge and complicated electrical circuit which may be very difficult to sketch. Therefore, in this project the first way is only used for importing the SPICE models of single gate paths, which as mentioned earlier have only three terminals. For the models with more than three terminals the second way of importing has been used.

The second way is to create new parts in PSpice from the desired SPICE models. As mentioned earlier the SPICE models which have been generated by performing the RL Impedance Extraction simulation on BusBar Tool models are .sp files which are SPICE netlists including the RL values of the studied models. In order to proceed with the second way, the first step is to save a copy of the SPICE netlist as a .lib file. Then in Model Editor which is a PSpice accessory, the .lib file as an input model library should be exported to capture part library resulting a .olb file which can be edited in this step if needed. In the next step, the generated .olb file should be added to the list of PSpice libraries so that its corresponding part can be placed in the schematics page. The last step is to make the corresponding netlist available for the PSpice simulator before running the PSpice project. This can be performed by adding the .lib file to the design in Configuration Files tab under the Simulation Settings.

5.3 Evaluation of Separated Gate Print

5.3.1 Separated Gate Print without Emitter Plate

5.3.1.1 Single Gate Path without Emitter Plate

In this scenario each gate path has been modeled and studied separately, since the gate paths in separated design have different parasitic elements due to their different lengths and shapes.

Each BBT model in this scenario possesses three terminals, hence two ports. The SPICE models obtained from the RL Impedance Extraction simulation look the same as the SPICE model shown in figure 4-10 regarding the size, number of extracted resistances, inductances, mutual resistances and mutual inductances. Due to the few numbers of parasitic elements in this scenario the required simulation time is very small.

A numbering has been used for each gate path in the separated design, which is shown in figure 5-1. The shortest gate path in the half right side is called GR1, the middle gate path in the right half side is called GR2, the longest gate path in the right half side is called GR3, the shortest gate path in the half left side is called GR4, the middle gate path in the half left side is called GR5, the longest gate path in the half left side is called GR6.

The SPICE models obtained in this scenario will also be used in the circuital schematics approach, presented in section 5.7.

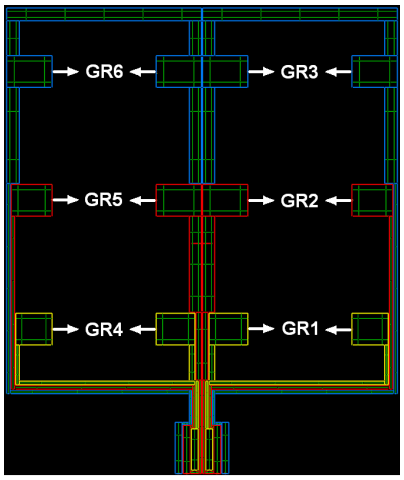


Figure 5-1: Numbering used for the gate paths in separated gate print

Gate Runner One without Emitter Plate (GR1)

The BBT model geometry in this case includes only GR1. The model meshing has been carried out according to 350 Hz and 10 kHz skin depths, by using the n and r values according to table 4-6, in order to study the effect of skin effect on parasitic elements. The RL Impedance Extraction simulation has been performed on each of the mentioned models for two simulation frequencies of 350 Hz and 10 kHz, in order to see the effect of simulation frequency. It means that four different simulations have been carried out in this section hence four SPICE models have been obtained.

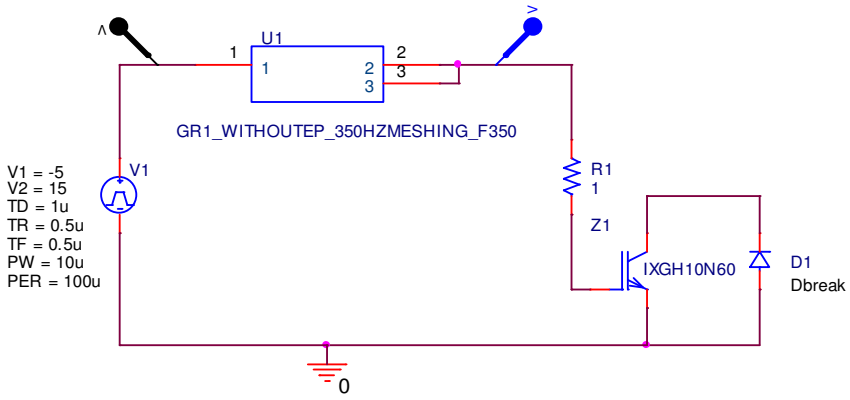


Figure 5-2: PSpice test circuit for GR1

The obtained SPICE models have been imported as new parts into PSpice, by using the second way explained in the section 5.2, and have been put into the desired test circuit. The created PSpice parts in this scenario have three nodes since their corresponding BBT models have three terminals. The part which is created from the SPICE model corresponding to GR1 BBT model with 350 Hz meshing and RL Impedance Extraction with 350 Hz simulation frequency is called GR1_WithoutEP_350HzMeshing_F350 and is shown as an example in figure 5-2. The reason that the nodes number two and three are short circuited is that the IGBT in PSpice test circuit represents all the 6 IGBTs in the sub-module which GR1 carries the gate signal into. The test circuit layout shown in figure 5-2 is the same for all four SPICE models in this section.

Figures 5-3 and 5-4 show the turn-on and turn-off voltage waveforms for GR1 respectively, in the case of 350 Hz meshing and simulation frequency of 350 Hz. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-2. Means that the black wave is the gate voltage received at the node number one (V_{gate}) and the blue wave is the gate voltage received at nodes number two and three (V_{output}) which can be considered as the IGBT gate voltage since the voltage drop over R1 is negligible.

In each of the mentioned simulations, turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for GR1 in tables 5-1 and 5-2 by using the equations 5-1 and 5-2 respectively.

$$\frac{\Delta V}{V_{Max}} = \frac{Max(V_{output}) - Max(V_{gate})}{Max(V_{output})} \times 100 \quad (5\text{-}1)$$

$$\frac{\Delta V}{V_{Min}} = \frac{Min(V_{output}) - Min(V_{gate})}{Min(V_{output})} \times 100 \quad (5\text{-}2)$$

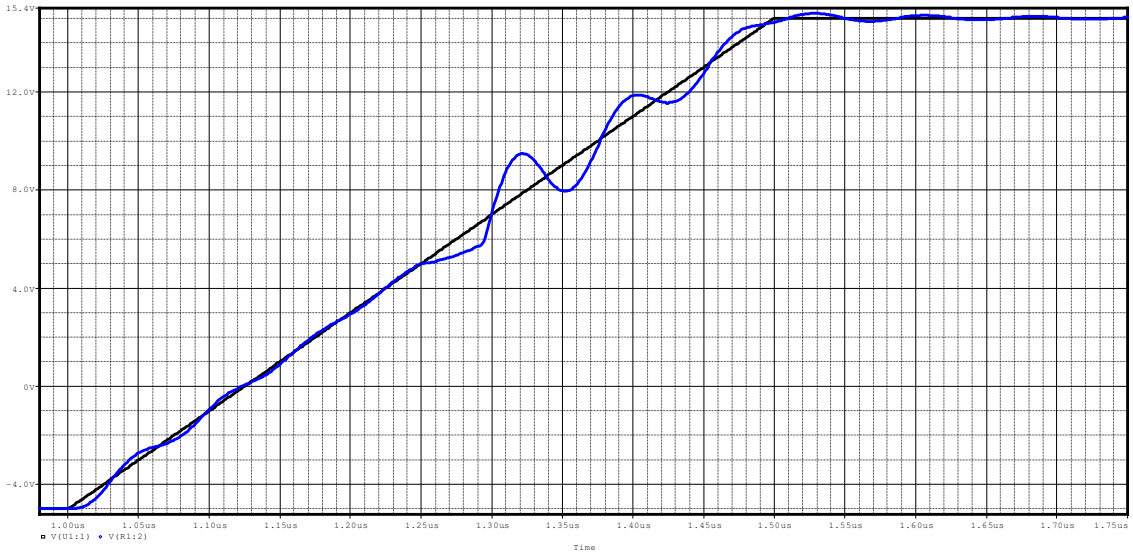


Figure 5-3: Turn-on voltage waveform for GR1

Table 5-1: Turn-on voltage overshoots in percentage for GR1

$\Delta V / V_{Max}$ (%)		Frequency to which the mesh sizes are set [Hz]	
		350	**10000**
Simulation Frequency	**350**	2.74	2.52
	10000	2.74	2.52

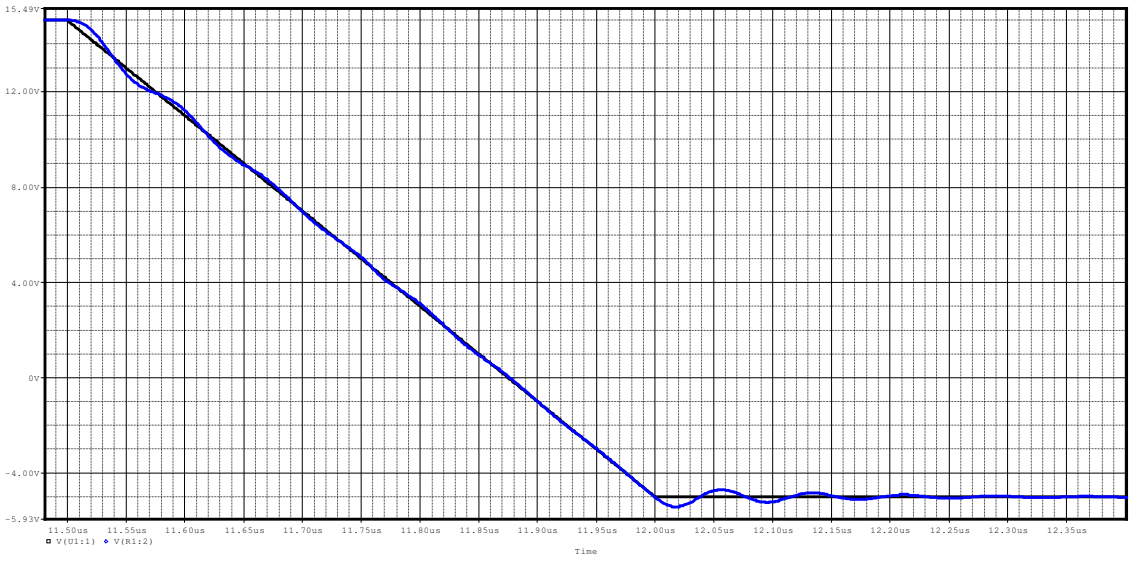


Figure 5-4: Turn-off voltage waveform for GR1

Table 5-2: Turn-off voltage overshoots in percentage for GR1

$\Delta V/V_{Min}$ (%)		Frequency to which the mesh sizes are set [Hz]	
		350	**10000**
Simulation Frequency	**350**	7.74	7.93
	10000	7.74	7.93

Gate Runner Two without Emitter Plate (GR2)

The BBT model geometry in this case includes only GR2. The model meshing has been carried out according to 350 Hz and 10 kHz skin depths. The RL Impedance Extraction simulation has been performed on each of the mentioned models for two simulation frequencies of 350 Hz and 10 kHz. It means that four different simulations have been carried out in this section hence four SPICE models have been obtained.

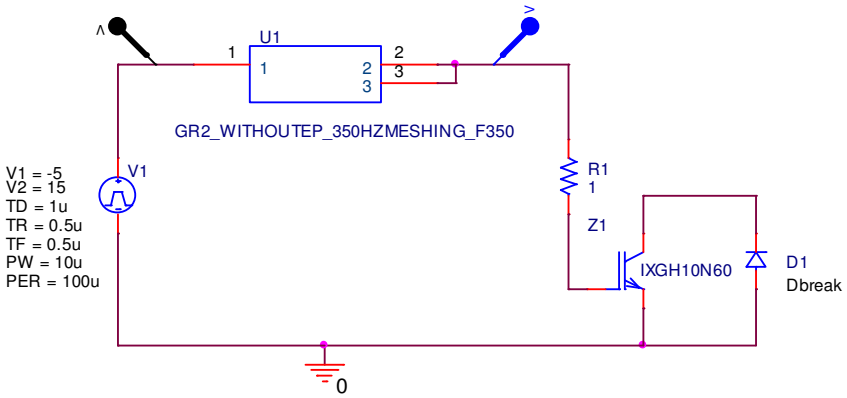


Figure 5-5: PSpice test circuit for GR2

The part which is created from the SPICE model corresponding to GR2 BBT model with 350 Hz meshing and RL Impedance Extraction with 350 Hz simulation frequency is called GR2_WithoutEP_350HzMeshing_F350 and is shown as an example in figure 5-5. The reason that the nodes number two and three are short circuited is that the IGBT in PSpice test circuit represents all the 6 IGBTs in the sub-module which GR2 carries the gate signal into. The test circuit layout shown in figure 5-5 is the same for all four SPICE models in this section.

Figures 5-6 and 5-7 show the turn-on and turn-off voltage waveforms for GR2 respectively, in the case of 350 Hz meshing and simulation frequency of 350 Hz. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-5. Means that the black wave is the gate voltage received at the node number one (V_{gate}) and the blue wave is the gate voltage received at nodes number two and three (V_{output}) which can be considered as the IGBT gate voltage since the voltage drop over R1 is negligible.

In each of the mentioned simulations, turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for GR2 in tables 5-3 and 5-4 by using the equations 5-1 and 5-2 respectively.

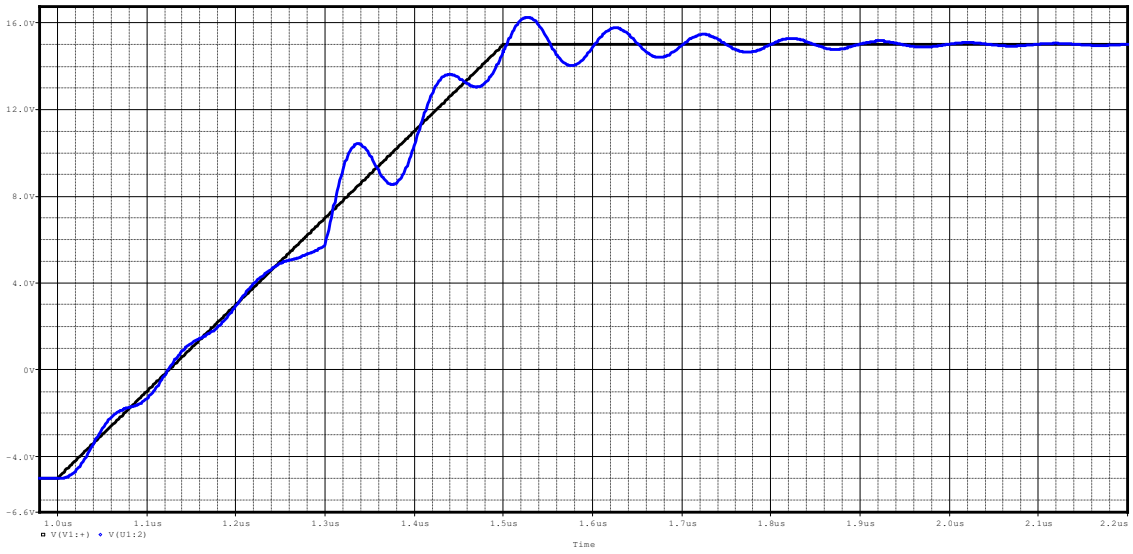


Figure 5-6: Turn-on voltage waveform for GR2

Table 5-3: Turn-on voltage overshoots in percentage for GR2

$\Delta V / V_{Max}$ (%)		**Frequency to which the mesh sizes are set [Hz]**	
		350	**10000**
Simulation Frequency	**350**	7.80	7.76
	10000	7.80	7.76

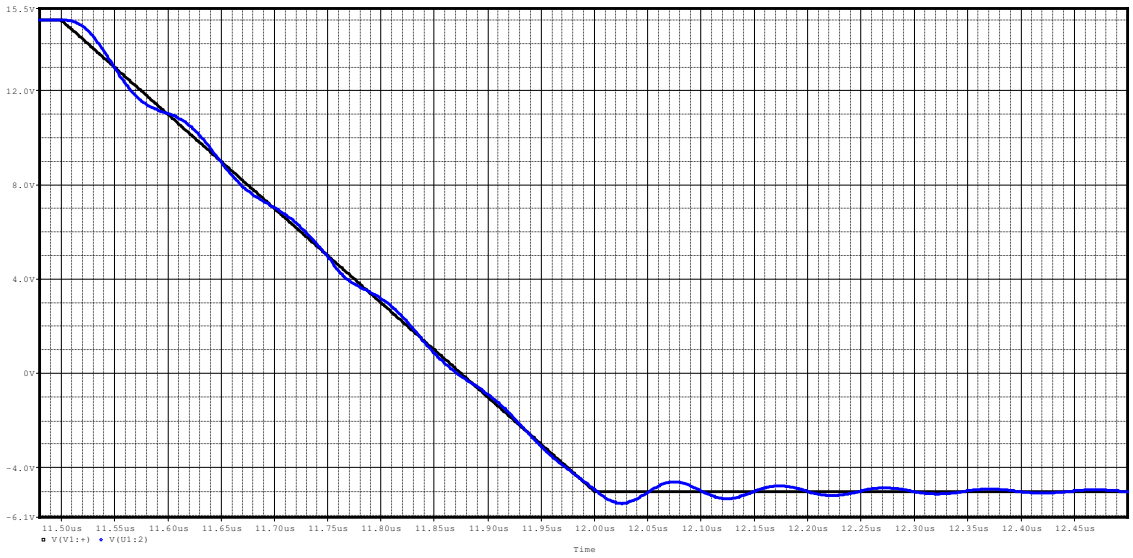


Figure 5-7: Turn-off voltage waveform for GR2

Table 5-4: Turn-off voltage overshoots in percentage for GR2

$\Delta V/V_{Min}$ (%)		Frequency to which the mesh sizes are set [Hz]	
		350	**10000**
Simulation Frequency	**350**	9.21	9.03
	10000	9.21	9.03

Gate Runner Three without Emitter Plate (GR3)

The BBT model geometry in this case includes only GR3. The model meshing has been carried out according to 350 Hz and 10 kHz skin depths. The RL Impedance Extraction simulation has been performed on each of the mentioned models for two simulation frequencies of 350 Hz and 10 kHz. It means that four different simulations have been carried out in this section hence four SPICE models have been obtained.

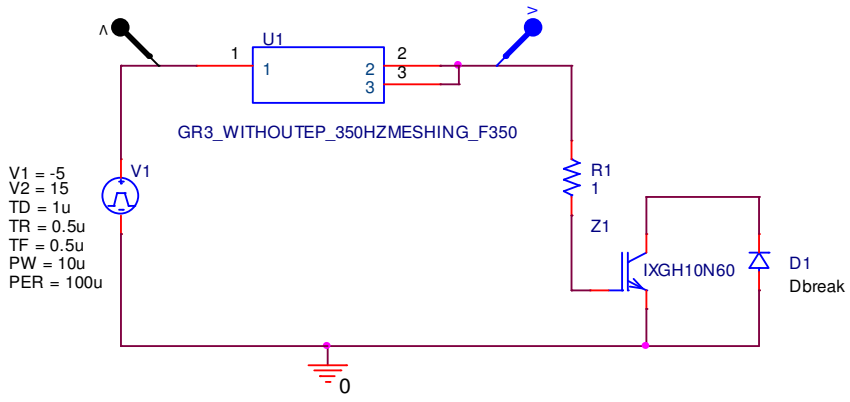


Figure 5-8: PSpice test circuit for GR3

The part which is created from the SPICE model corresponding to GR3 BBT model with 350 Hz meshing and RL Impedance Extraction with 350 Hz simulation frequency is called GR3_WithoutEP_350HzMeshing_F350 and is shown as an example in figure 5-8. The reason that the nodes number two and three are short circuited is that the IGBT in PSpice test circuit represents all the 6 IGBTs in the sub-module which GR3 carries the gate signal into. The test circuit layout shown in figure 4-8 is the same for all four SPICE models in this section.

Figures 5-9 and 5-10 show the turn-on and turn-off voltage waveforms for GR3 respectively, in the case of 350 Hz meshing and simulation frequency of 350 Hz. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-8. Means that the black wave is the gate voltage received at the node number one (V_{gate}) and the blue wave is the gate voltage received at nodes number two and three (V_{output}) which can be considered as the IGBT gate voltage since the voltage drop over R1 is negligible.

In each of the mentioned simulations, turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for GR3 in table 5-5 by using the equations 5-1 and 5-2 respectively.

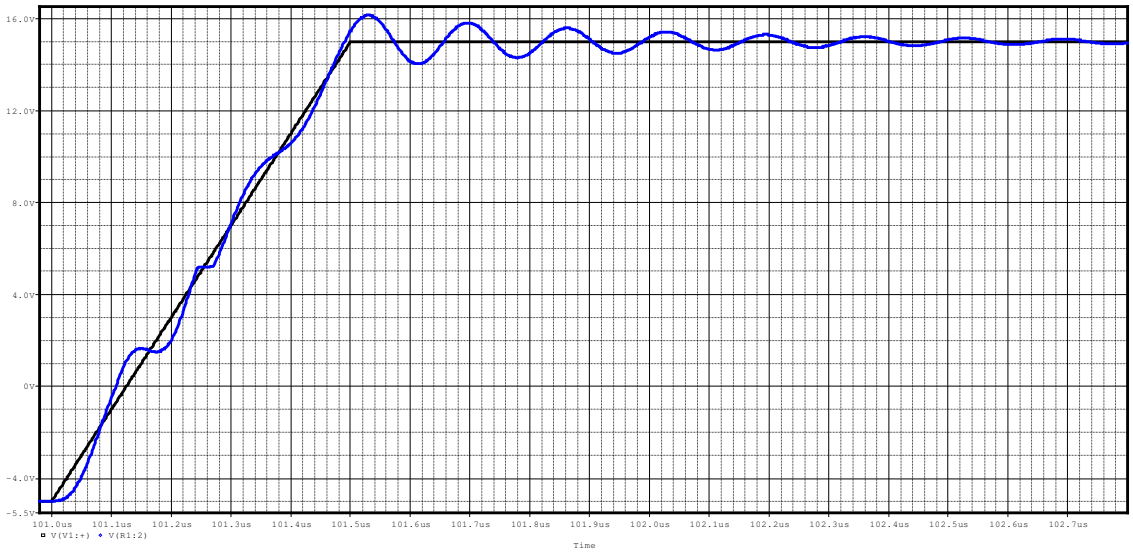


Figure 5-9: Turn-on voltage waveform for GR3

Table 5-5: Turn-on voltage overshoots in percentage for GR3

$\Delta V / V_{Max}$ (%)		**Frequency to which the mesh sizes are set [Hz]**	
		350	**10000**
Simulation Frequency	**350**	7.12	7.27
	10000	7.12	7.27

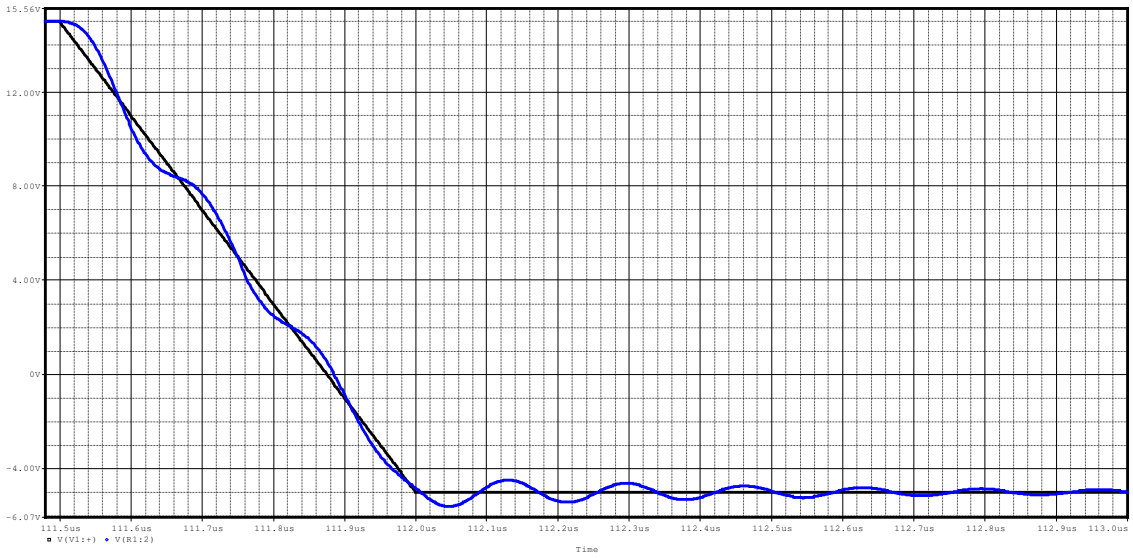


Figure 5-10: Turn-off voltage waveform for GR3

Table 5-6: Turn-off voltage overshoots in percentage for GR3

$\Delta V/V_{Min}$ (%)		Frequency to which the mesh sizes are set [Hz]	
		350	**10000**
Simulation Frequency	**350**	10.93	10.65
	10000	10.93	10.65

It should be mentioned that it is neglected to show the results obtained from studying GR4, GR5, and GR6 since due to the gate print symmetry their results are exactly the same as the results of GR1, GR2, and GR3 respectively.

5.3.1.2 Six Coupled Gate Paths without Emitter Plate

In this scenario the whole separated gate print has been modeled and studied. The BBT model geometry in this case includes all six coupled gate paths. The model meshing has been carried out according to 350 Hz and 10 kHz skin depths. The RL Impedance Extraction simulation has been performed on each of the mentioned models for two simulation frequencies of 350 Hz and 10 kHz. It means that four different simulations have been carried out in this section hence four SPICE models have been obtained.

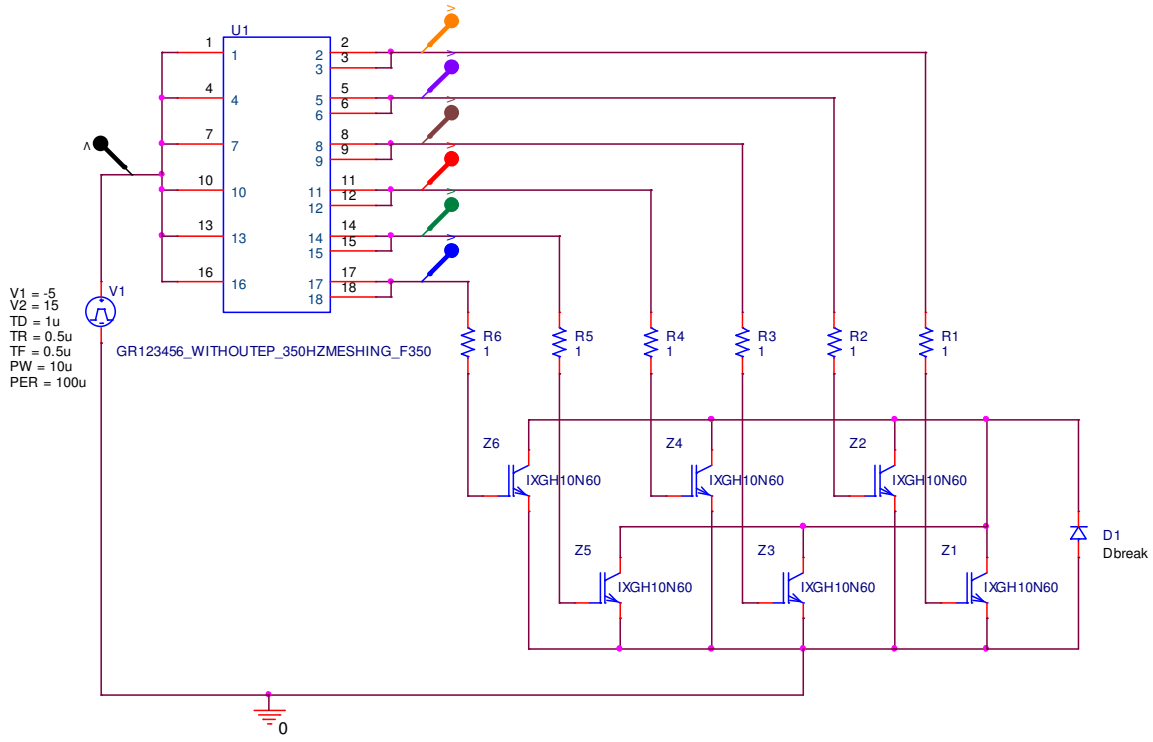


Figure 5-11: PSpice test circuit for separated gate print

The created PSpice parts in this scenario have eighteen nodes since six coupled gate paths have been modeled and each gate path BBT model possesses three terminals. The nodes 1,4,7,10,13 and 16 are the input terminals corresponding to GR1, GR2, GR3, GR4, GR5, and GR6 respectively. The remaining 12 nodes are corresponding to the gate paths output terminals. The nodes 2 and 3 are the output terminals corresponding to GR1, the nodes 5 and 6 are the output terminals corresponding to GR2, the nodes 8 and 9 are the output terminals corresponding to GR3 and so on. Due to the relations between the number of ports, which is twelve in this case, and the number of parasitic elements mentioned in the section 4.5, there are 12 resistances, 12 inductances and 66 mutual inductances in the SPICE netlist in this scenario. Extracting this number of elements requires a much longer simulation time in comparison to previous scenarios. The part which is created from the SPICE model corresponding to gate print BBT model with 350 Hz meshing and RL Impedance Extraction with 350 Hz simulation frequency is called GR123456_WithoutEP_350HzMeshing_F350 and is shown as an example in figure 5-11. The reason that the nodes corresponding to output terminals of each gate path are short circuited is that each of the IGBTs in PSpice test circuit represents all the 6 IGBTs in the sub-module which that specific gate path carries the gate signal into. The test circuit layout shown in figure 5-11 is the same for all four SPICE models in this section.

Figures 5-12 and 5-13 show the turn-on and turn-off voltage waveforms at each gate path respectively, in the case of 350 Hz meshing and simulation frequency of 350 Hz. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-11. Means that the black wave is the gate voltage received at the input terminals of the gate paths (V_{gate}) which are the nodes number 1, 4,7,10, 13, and 16 and the color waves are the gate voltages received at the output terminals of the gate paths (V_{output}) which are the same as the gates of IGBTs. Due to the gate print symmetry the gate voltages received at the gate of IGBTs Z4, Z5 and Z6 are the same as the gate voltages received at the gate of IGBTs Z1, Z2 and Z3 respectively. Therefore their corresponding waveforms are overlapping and that is why there are three voltage waveforms visible in figures 5-12 and 5-13 and not six.

In each of the mentioned simulations, turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for each gate path in tables 5-7 and 5-8 by using the equations 5-1 and 5-2 respectively.

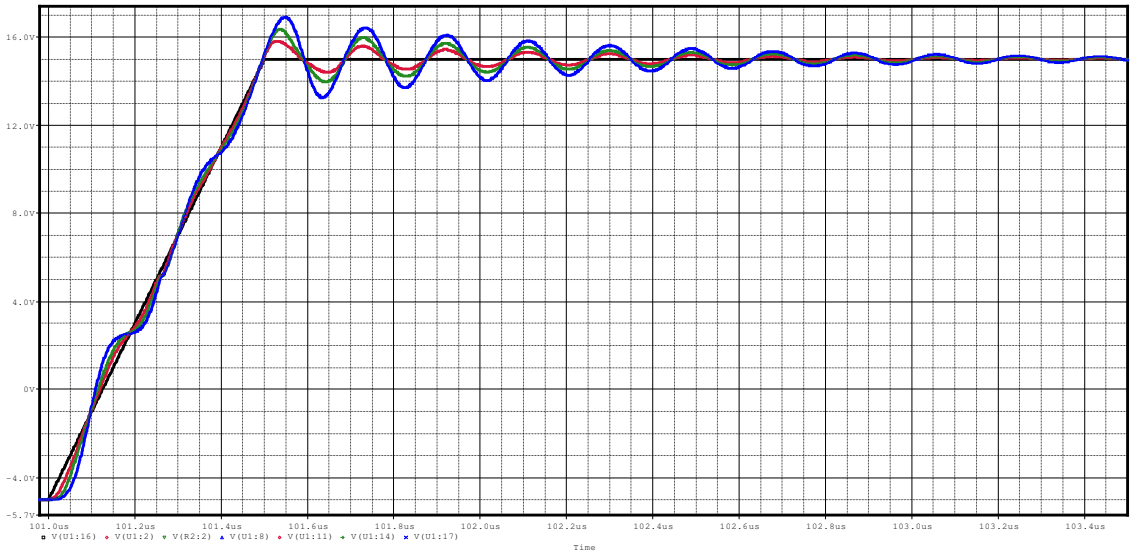


Figure 5-12: Turn-on voltage waveform for separated gate print

Table 5-7: Turn-on voltage overshoots in percentage for each gate path

$\Delta V / V_{Max}$ (%)		Frequency to which the mesh sizes are set [Hz]											
		350						10000					
		GR1	GR2	GR3	GR4	GR5	GR6	GR1	GR2	GR3	GR4	GR5	GR6
Simulation Frequency	350	5.17	8.28	11.27	5.17	8.28	11.27	5.33	8.53	11.74	5.33	8.53	11.74
	10000	5.17	8.28	11.28	5.17	8.28	11.28	5.33	8.53	11.74	5.33	8.53	11.73

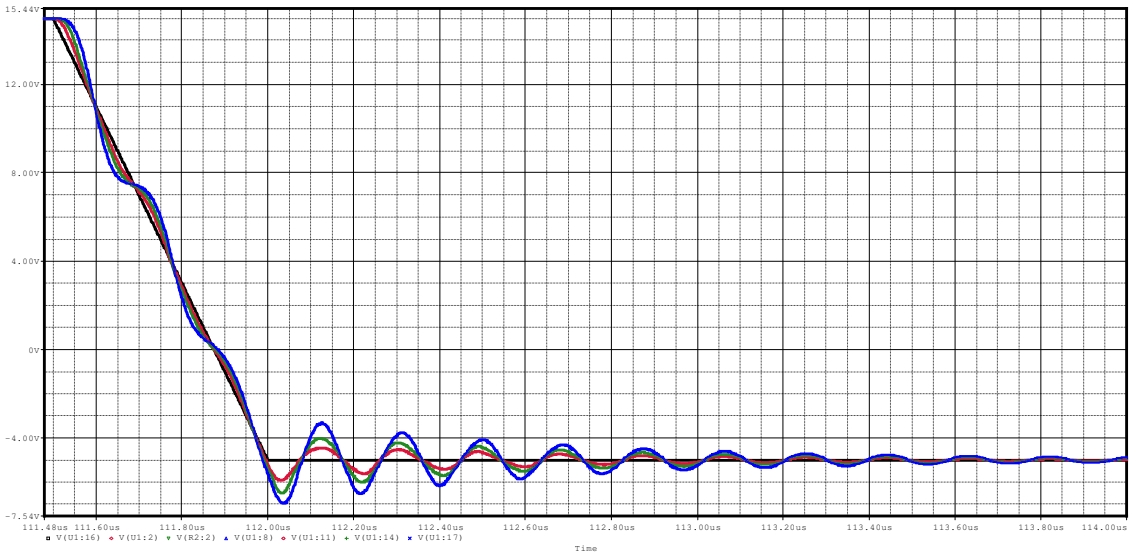


Figure 5-13: Turn-off voltage waveform for separated gate print

Table 5-8: Turn-off voltage overshoots in percentage for each gate path

$\Delta V/V_{Min}$ (%)		Frequency to which the mesh sizes are set [Hz]											
		350						10000					
		GR1	GR2	GR3	GR4	GR5	GR6	GR1	GR2	GR3	GR4	GR5	GR6
Simulation Frequency	350	15.62	23.15	28.01	15.62	23.15	28.01	16.31	24.03	29.42	16.31	24.03	29.42
	10000	15.62	23.15	28.01	15.62	23.15	28.01	16.31	24.03	29.42	16.31	24.03	29.42

5.3.2 Separated Gate Print with Emitter Plate

As explained in chapter 4, the emitter plate affects on parasitic elements through the induced eddy currents and couplings with the gate paths. Therefore, in this scenario the emitter plate model has been added to the studied models in previous scenario.

5.3.2.1 Single Gate Path with Emitter Plate

In this scenario each separated gate path and the emitter plate have been modeled and studied together. BBT models in this scenario possess six terminals: three of them belong to the studied gate path and the other three belong to the emitter plate and are located below the gate path terminals. Hence there will be four ports: two of them are the gate path ports and two of them are the emitter plate ports. Since BBT models in this scenario have two ports more than the ones in single gate path without emitter plate scenario, the SPICE models obtained from the RL Impedance Extraction simulation are longer ones with more parasitic elements. Due to the

relations between the number of ports and the number of parasitic elements, mentioned in the section 4.5, there are four resistances, four inductances, twelve mutual resistances and six mutual inductances in each SPICE netlist in this scenario. Extracting these elements requires a much longer simulation time in comparison to the single gate path without emitter plate.

As mentioned earlier, other than number of terminals, it is the number of meshing nodes which affects the RL Impedance Extraction simulation time. In this scenario, emitter plate, which has a large number of meshing nodes due to its geometry, has been added to the model and has increased the total number of meshing nodes. Therefore the number of meshing nodes is the main effecting parameter on the simulation time in this scenario.

In order to keep the simulation accuracy without increasing the simulation time more than required, the models meshing in this scenario have been carried out according to 350 Hz skin depth, by using the n and r values according to table 4-6, and the RL Impedance Extraction has been performed with 350 Hz simulation frequency.

Gate Runner One with Emitter Plate (GR1)

The BBT model geometry in this case includes GR1 coupled with emitter plate. The obtained SPICE model has been imported as a new part into PSpice and has been put into the desired test circuit. The created PSpice part has six nodes since its corresponding BBT model has six terminals. The created part in this simulation scenario is called GR1_WithCompleteEP_350HzMeshing_F350 and is shown in figure 5-14. The reason that the nodes corresponding to each pair of output terminals are short circuited is that the IGBT in PSpice test circuit represents all the 6 IGBTs in the sub-module which GR1 carries the gate signal into.

Figures 5-15 and 5-16 show the turn-on and turn-off voltage waveforms for GR1 coupled with emitter plate respectively. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-14. Means that the black wave is the gate voltage received at the node number one (V_{gate}) and the blue wave is the gate voltage received at nodes number two and three (V_{output}) which can be considered as the IGBT gate voltage since the voltage drop over R1 is negligible.

Turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for GR1 coupled with emitter plate in table 5-9.

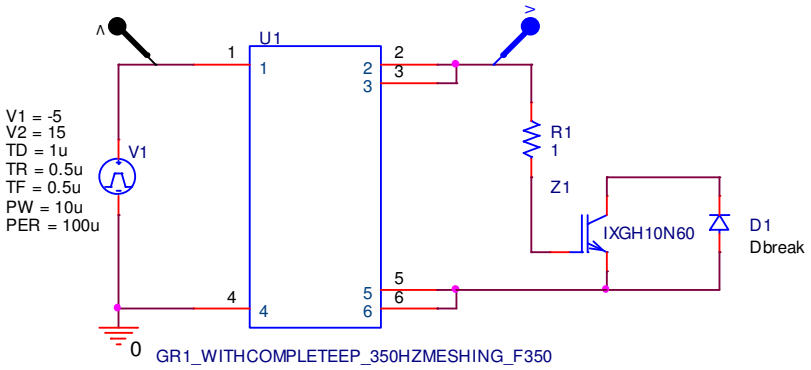


Figure 5-14: PSpice test circuit for GR1 coupled with emitter plate

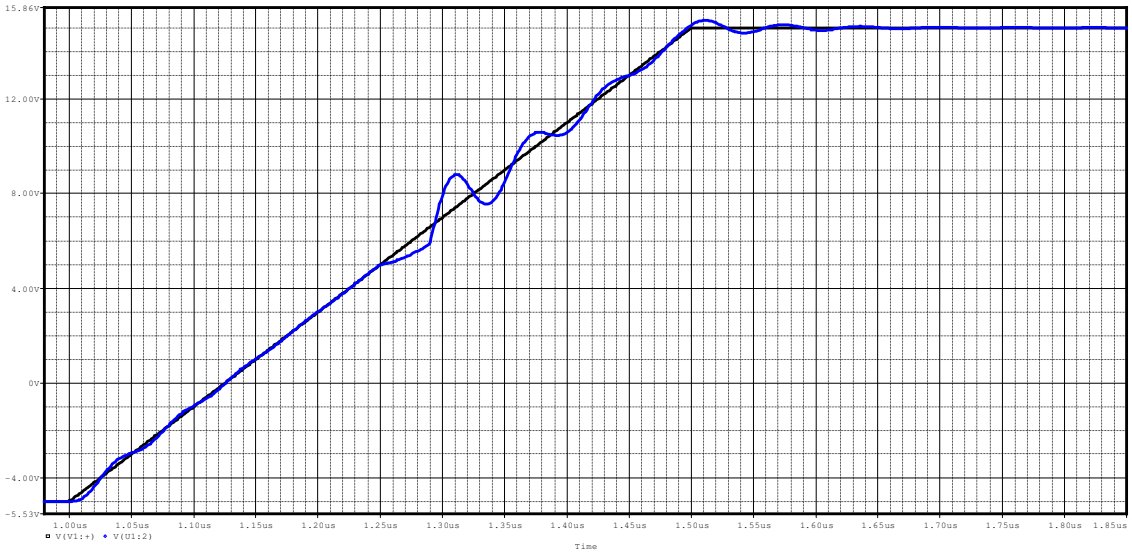


Figure 5-15: Turn-on voltage waveform for GR1 coupled with emitter plate

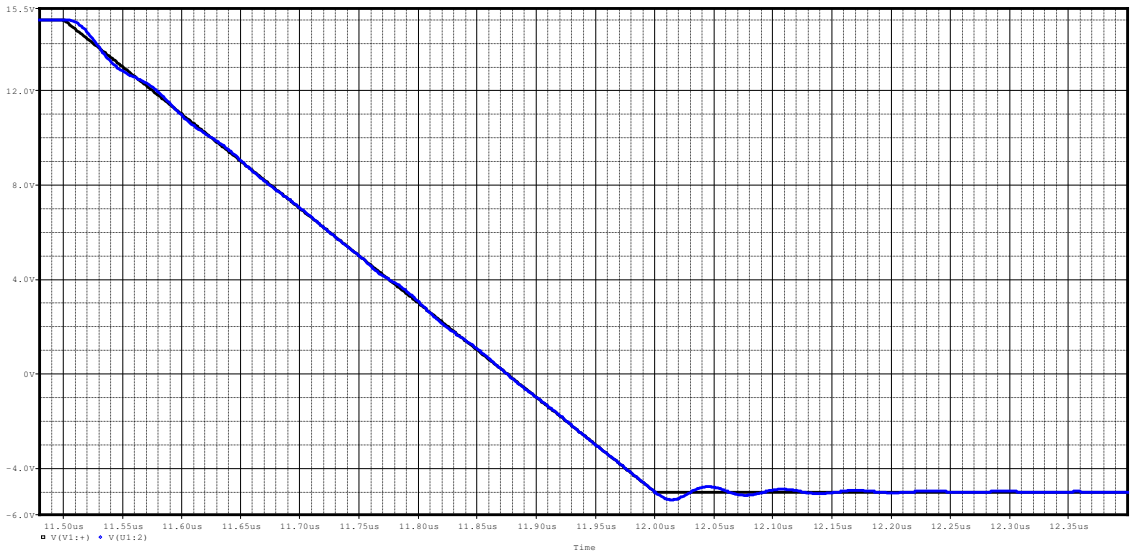


Figure 5-16: Turn-off voltage waveform for GR1 coupled with emitter plate

Table 5-9: Voltage overshoot in percentage for GR1 coupled with emitter plate

$\Delta V/V_{Max}$ (%)	2.08
$\Delta V/V_{Min}$ (%)	6.25

Gate Runner Two with Emitter Plate (GR2)

The BBT model geometry in this case includes GR2 coupled with emitter plate. The created part in this simulation scenario is called GR2_WithCompleteEP_350HzMeshing_F350 and is shown in figure 5-17. The reason that the nodes corresponding to each pair of output terminals are short circuited is that the IGBT in PSpice test circuit represents all the 6 IGBTs in the sub-module which GR2 carries the gate signal into.

Figures 5-18 and 5-19 show the turn-on and turn-off voltage waveforms for GR2 coupled with emitter plate respectively. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-17. Means that the black wave is the gate voltage received at the node number one (V_{gate}) and the blue wave is the gate voltage received at nodes number two and three (V_{output}) which can be considered as the IGBT gate voltage since the voltage drop over R1 is negligible.

Turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for GR2 coupled with emitter plate in table 5-10.

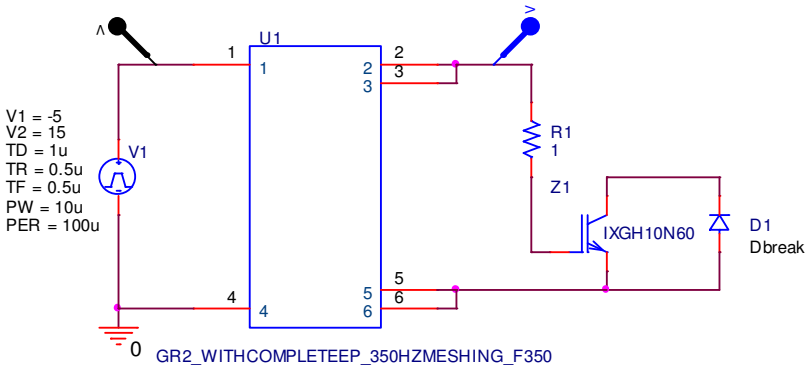


Figure 5-17: PSpice test circuit for GR2 coupled with emitter plate

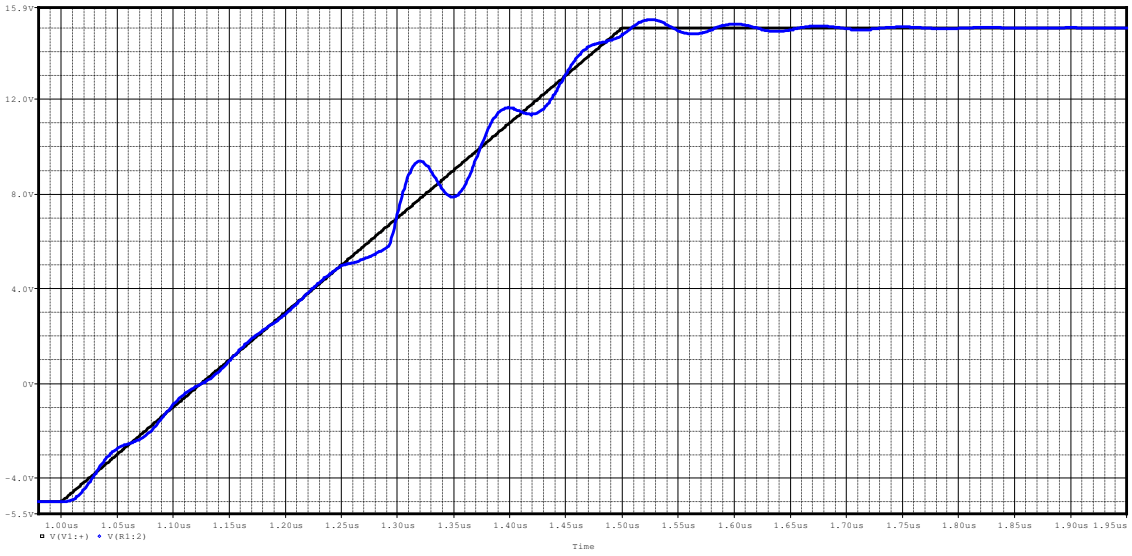


Figure 5-18: Turn-on voltage waveform for GR2 coupled with emitter plate

Figure 5-19: Turn-off voltage waveform for GR2 coupled with emitter plate

Table 5-10: Voltage overshoot in percentage for GR2 coupled with emitter plate

$\Delta V/V_{Max}$ (%)	3.06
$\Delta V/V_{Min}$ (%)	7.26

Gate Runner Three with Emitter Plate (GR3)

The BBT model geometry in this case includes GR3 coupled with emitter plate. The created part in this simulation scenario is called GR3_WithCompleteEP_350HzMeshing_F350 and is shown in figure 5-20. The reason that the nodes corresponding to each pair of output terminals are short circuited is that the IGBT in PSpice test circuit represents all the 6 IGBTs in the sub-module which GR3 carries the gate signal into.

Figures 5-21 and 5-22 show the turn-on and turn-off voltage waveforms for GR3 coupled with emitter plate respectively. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-20. Means that the black wave is the gate voltage received at the node number one (V_{gate}) and the blue wave is the gate voltage received at nodes number two and three (V_{output}) which can be considered as the IGBT gate voltage since the voltage drop over R1 is negligible.

Turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for GR3 coupled with emitter plate in table 5-11.

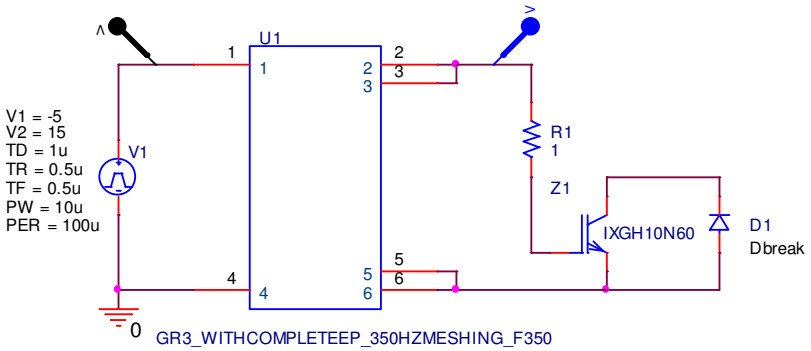


Figure 5-20: PSpice test cicuit for GR3 coupled with emitter plate

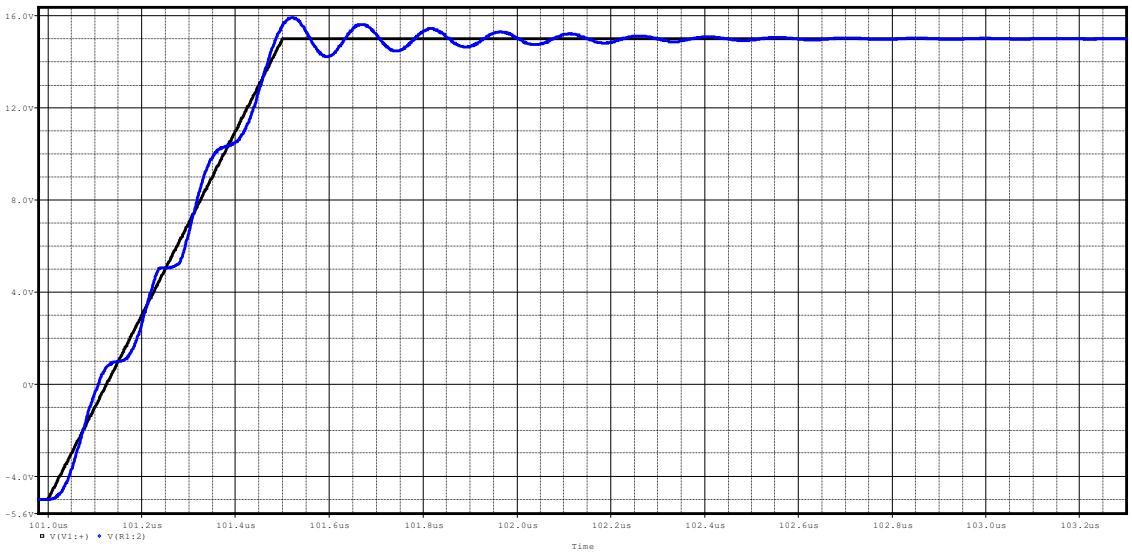


Figure 5-21: Turn-on voltage waveform for GR3 coupled with emitter plate

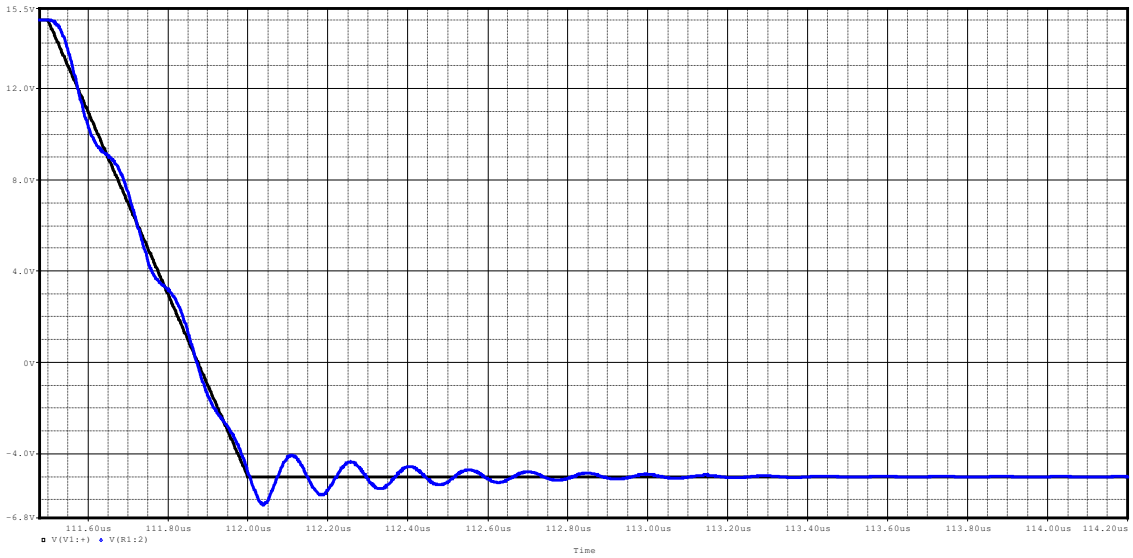


Figure 5-22: Turn-off voltage waveform for GR3 coupled with emitter plate

Table 5-11: Voltage overshoot in percentage for GR3 coupled with emitter plate

$\Delta V/V_{Max}$ (%)	5.83
$\Delta V/V_{Min}$ (%)	19.73

It should be mentioned that it is neglected to show the results obtained from studying GR4, GR5, and GR6 coupled with emitter plate since due to the gate print symmetry their results are exactly the same as the results of GR1, GR2, and GR3 coupled with emitter plate respectively.

5.3.2.2 Six Coupled Gate Paths with Emitter Plate

In this scenario the whole separated gate print and the emitter plate have been modeled and studied together. The couplings exist between each pair of gate paths and also between the emitter plate and each single gate path. BBT model in this scenario possesses 32 terminals: 18 of them belong to the gate print and the other 14 belong to the emitter plate and are located below the gate path terminals. Hence there will be 24 ports: 12 of them are gate path ports and 12 of them are the emitter plate ports. Due to the relations between the number of ports and the number of parasitic elements, mentioned in the section 4.5, there are 24 resistances, 24 inductances, 552 mutual resistances and 276 mutual inductances in the SPICE netlist in this scenario. Extracting this huge number of elements requires a very long simulation time: more than 24 hours. Other than number of terminals, the number of meshing nodes has increased a lot. Therefore, in order to keep the simulation accuracy without increasing the simulation time more than required, the model meshing in this scenario has been carried out according to 350 Hz skin depth, by

using the n and r values according to table 4-6, and the RL Impedance Extraction has been performed with 350 Hz simulation frequency.

The BBT model in this case includes separated gate print with emitter plate. The obtained SPICE model has been imported as a new part into PSpice and has been put into the desired test circuit. The created PSpice part in this scenario has 32 nodes since its corresponding BBT model has 32 terminals. The nodes 1,4,7,10,13 and 16 are the input terminals corresponding to GR1, GR2, GR3, GR4, GR5 and GR6 respectively and the nodes 19 and 26 are the input terminals corresponding to emitter plate. The remaining 24 nodes are corresponding to the output terminals of the gate paths and the emitter plate. The created part in this simulation scenario is called GR123456_WithEP_350HzMeshing_F350 and is shown in figure 5-23. The reason that the nodes corresponding to each pair of output terminals are short circuited is that each of the IGBTs in PSpice test circuit represents all the 6 IGBTs in the sub-module which that specific gate path carries the gate signal into.

Figures 5-24 and 5-25 show the turn-on and turn-off voltage waveforms at each gate path respectively in the case of separated gate print coupled with emitter plate. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-23. Means that the black wave is the gate voltage received at the input terminals of the gate paths and the emitter plate (V_{gate}) and the color waves are the gate voltages received at the output terminals of the gate paths and the emitter plate (V_{output}) which are the same as the gates of IGBTs. Due to the gate print symmetry the gate voltages received at the gate of IGBTs Z4, Z5 and Z6 are the same as the gate voltages received at the gate of IGBTs Z1, Z2 and Z3 respectively. Therefore their corresponding waveforms are overlapping and that is why there are three voltage waveforms visible in figures 5-24 and 5-25 and not six.

Turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for each gate path in table 5-12 for the case of separated gate print coupled with emitter plate.

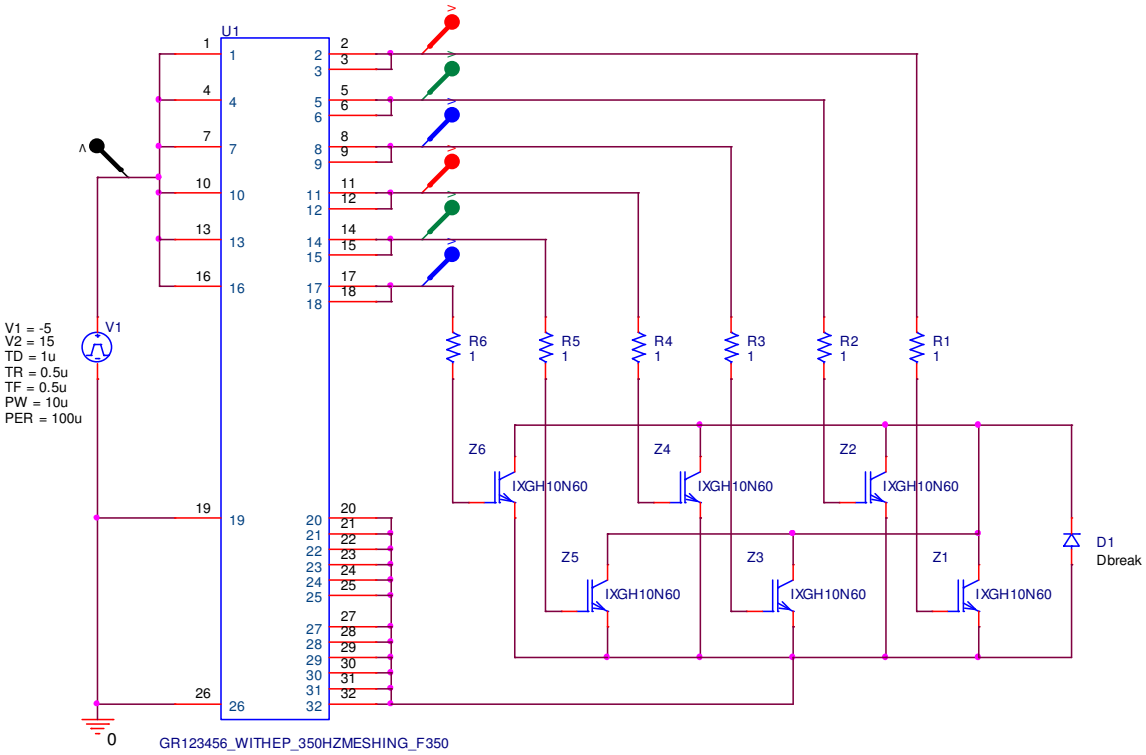


Figure 5-23: PSpice test circuit for separated gate print coupled with emitter plate

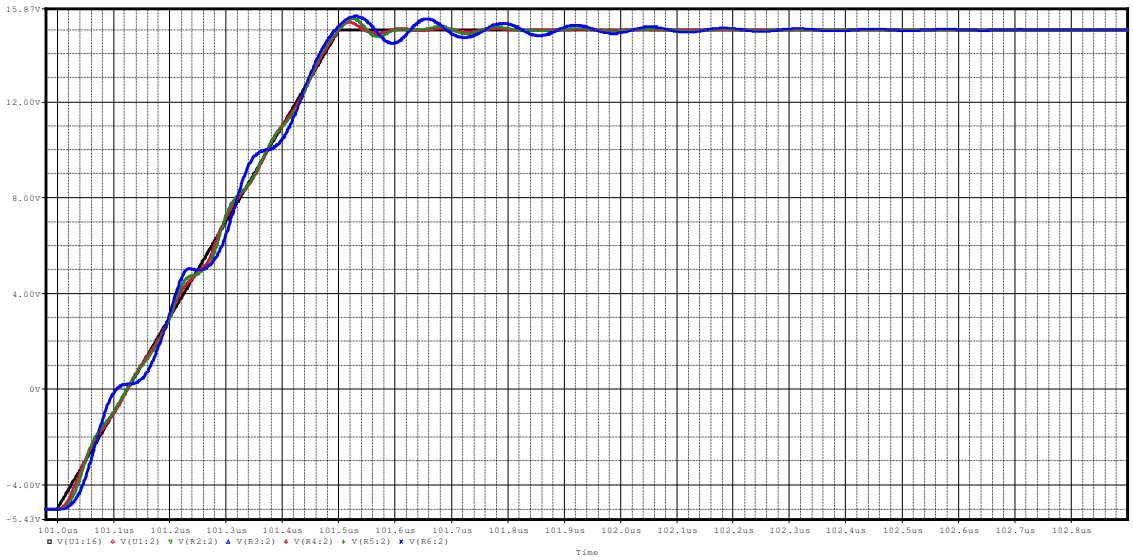


Figure 5-24: Turn-on voltage waveform for separated gate print coupled with emitter plate

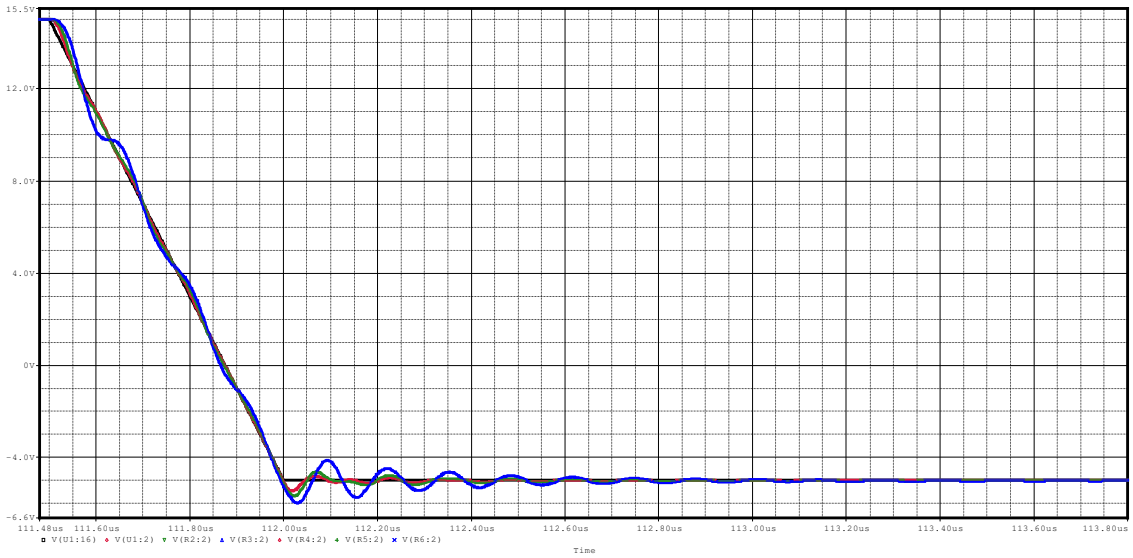


Figure 5-25: Turn-off voltage waveform for separated gate print coupled with emitter plate

Table 5-12: Voltage overshoot for separated gate print coupled with emitter plate

	GR1	**GR2**	**GR3**	**GR4**	**GR5**	**GR6**
$\Delta V/V_{Max}$ (%)	2.20	3.10	3.70	2.20	3.10	3.70
$\Delta V/V_{Min}$ (%)	8.18	11.70	16.35	8.18	11.70	16.35

5.4 Frequency Effect

By comparing the voltage overshoots corresponding to the cases with model meshing according to 350 Hz and 10 kHz frequencies in the scenario of without emitter plate, it is found out that that the skin effect has such a small effect on parasitic elements that it can be neglected. Hence even in the case of gate voltages with high frequencies it is possible to set the size of the meshings according to the skin depth of smaller frequencies. This decreases the simulation time up to a great extent while it keeps the same simulation accuracy.

In the same scenario, the voltage overshoots corresponding to RL Impedance Extraction simulation frequencies of 350 Hz and 10 kHz have been compared and it is found out that the simulation frequency does not have any effect on parasitic elements in almost all cases.

5.5 Emitter Effect

In the previous sections, each single gate path and six coupled gate paths have been studied in two scenarios of with and without emitter plate. In order to be able to judge about the emitter plate effect, the results of two scenarios are going to be compared for each case from the aspect of maximum voltage overshoots. It should be mentioned that in this part it is only focused on the results corresponding to 350 Hz meshing and 350 Hz simulation frequency.

In the following parts turn-on and turn-off voltage waveforms of both scenarios are shown in the same figure for each case. The blue curves are corresponding to the scenario without the emitter plate and the red curves are corresponding to the scenario with the emitter plate. Turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for each case in the following tables for both scenarios of with and without emitter plate.

Single Gate Path

GR1

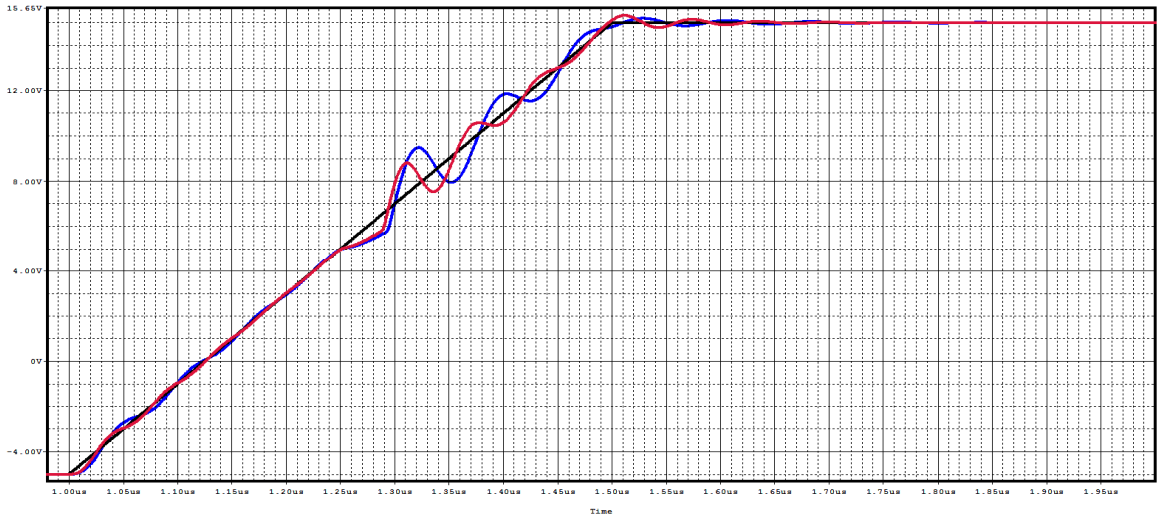


Figure 5-26: Turn-on voltage waveform for GR1

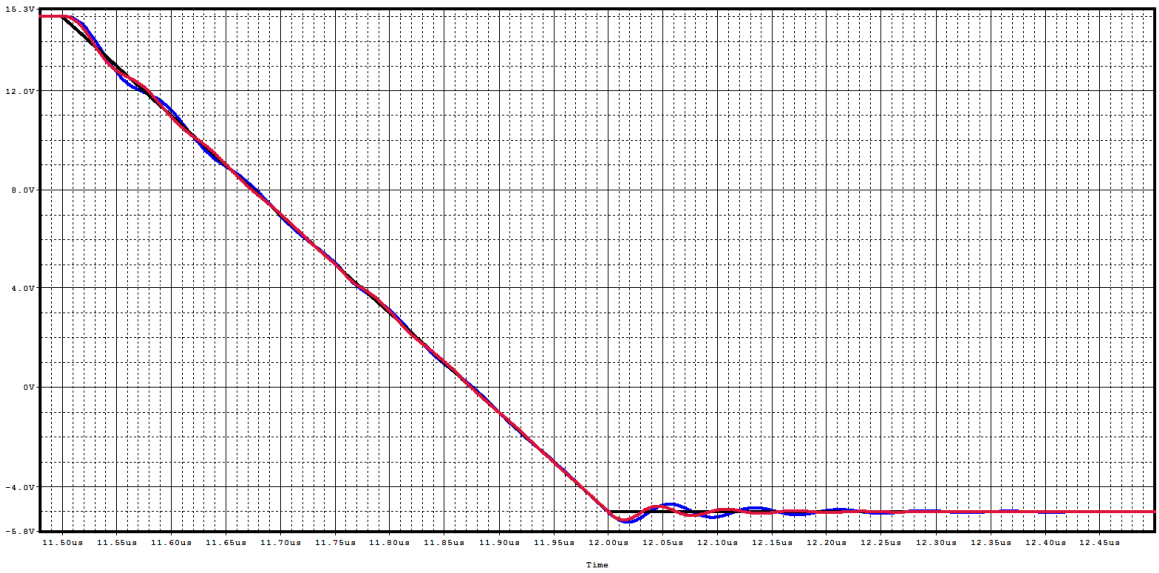


Figure 5-27: Turn-off voltage waveform for GR1

Table 5-13: Voltage overshoots for GR1

$\Delta V/V_{Max}$ (%)	**Without Emitter Plate**	2.74
	With Emitter Plate	2.08
$\Delta V/V_{Min}$ (%)	**Without Emitter Plate**	7.74
	With Emitter Plate	6.25

GR2

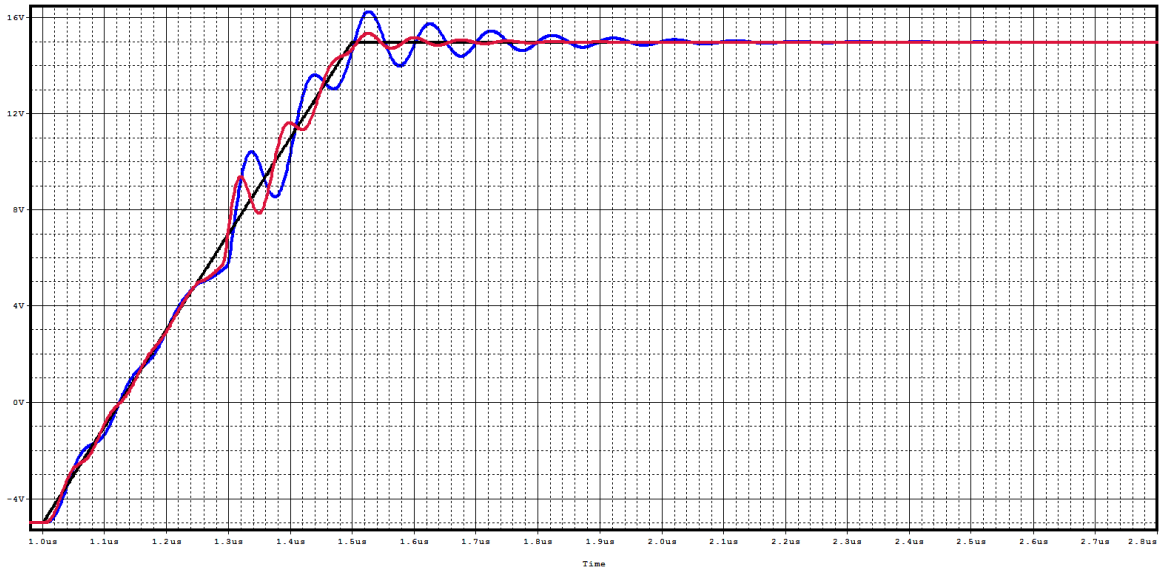


Figure 5-28: Turn-on voltage waveform for GR2

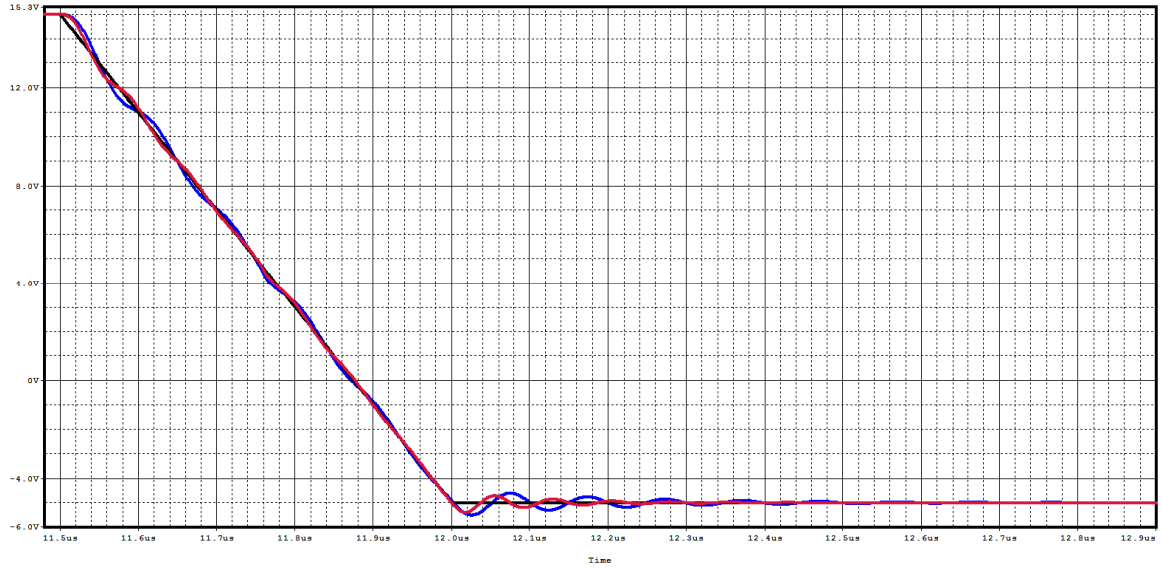


Figure 5-29: Turn-off voltage waveform for GR2

Table 5-14: Voltage overshoots for GR2

$\Delta V/V_{Max}$ (%)	**Without Emitter Plate**	7.80
	With Emitter Plate	3.06
$\Delta V/V_{Min}$ (%)	**Without Emitter Plate**	9.21
	With Emitter Plate	7.26

GR3

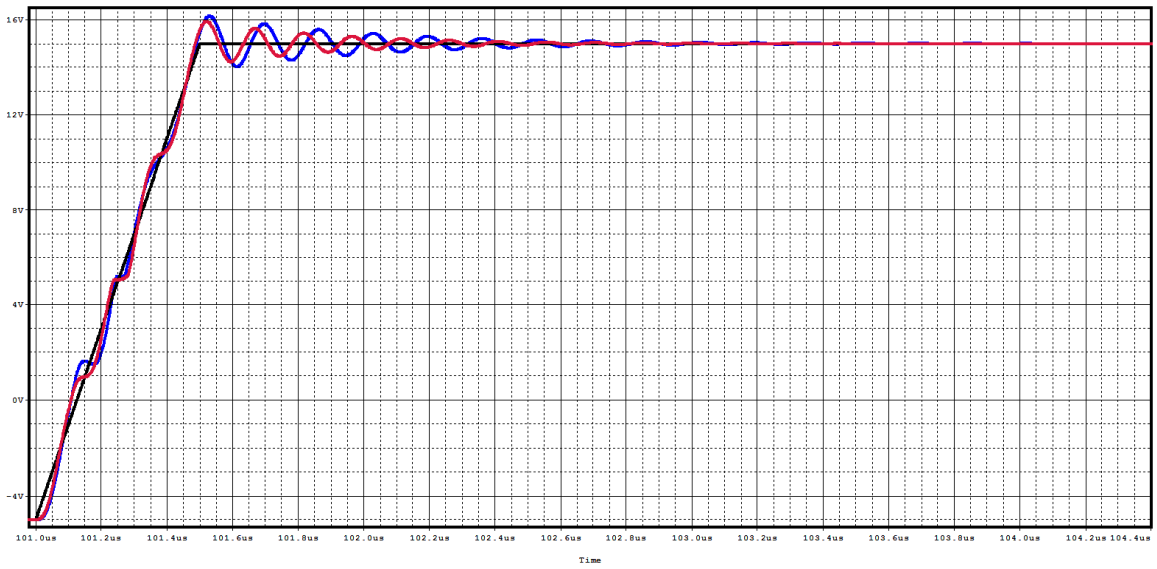


Figure 5-30: Turn-on voltage waveform for GR3

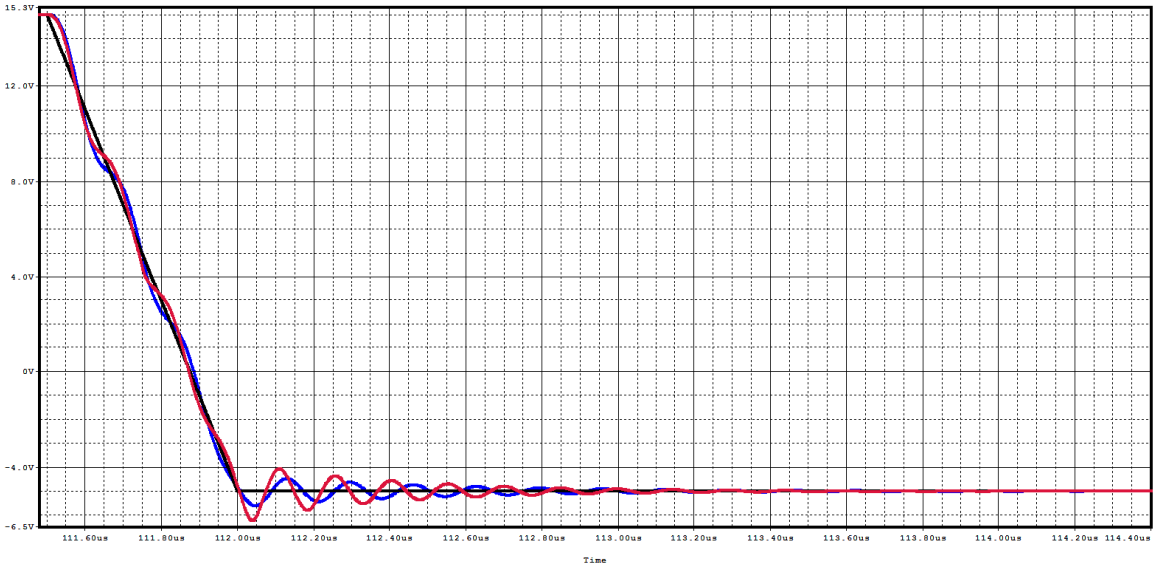


Figure 5-31: Turn-off voltage waveform for GR3

Table 5-15: Voltage overshoots for GR3

$\Delta V/_{V_{Max}}$ (%)	**Without Emitter Plate**	7.12
	With Emitter Plate	5.83
$\Delta V/_{V_{Min}}$ (%)	**Without Emitter Plate**	10.93
	With Emitter Plate	19.73

As it can be seen, for GR1 and GR2 both turn-on and turn-off voltage overshoots are more in the scenario without emitter plate. But for GR3, turn-on voltage overshoot is more in the scenario without emitter plate, while turn-off voltage overshoot is more in the scenario of with emitter plate.

It should be mentioned that it is neglected to show the results obtained from studying GR4, GR5, and GR6 since due to the gate print symmetry their results are exactly the same as the results of GR1, GR2, and GR3 respectively.

Six Coupled Gate Paths

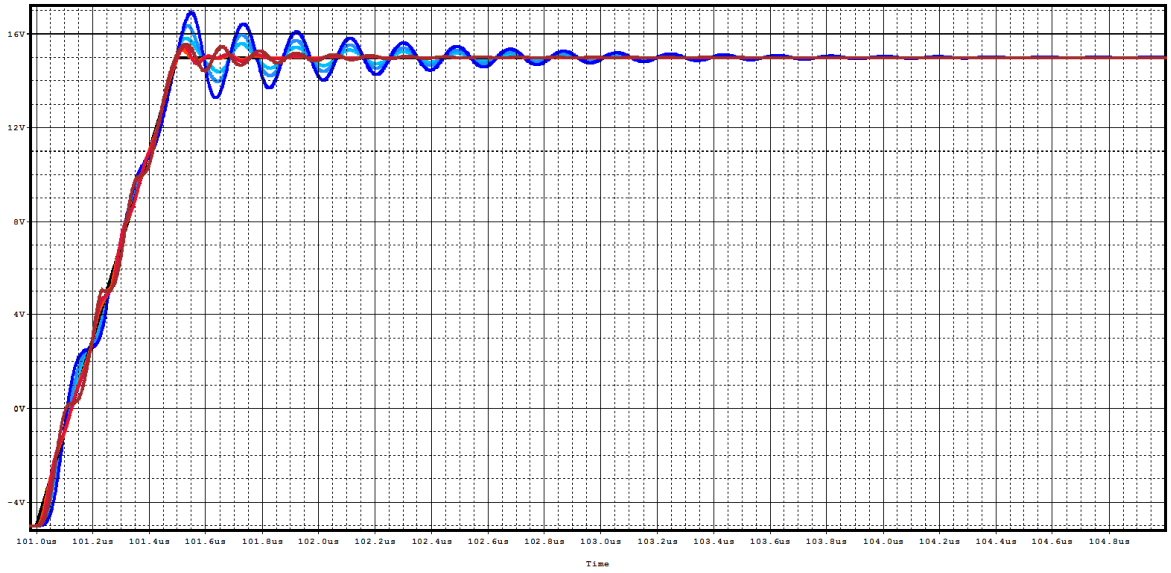


Figure 5-32: Turn-on voltage waveform for six coupled gate paths

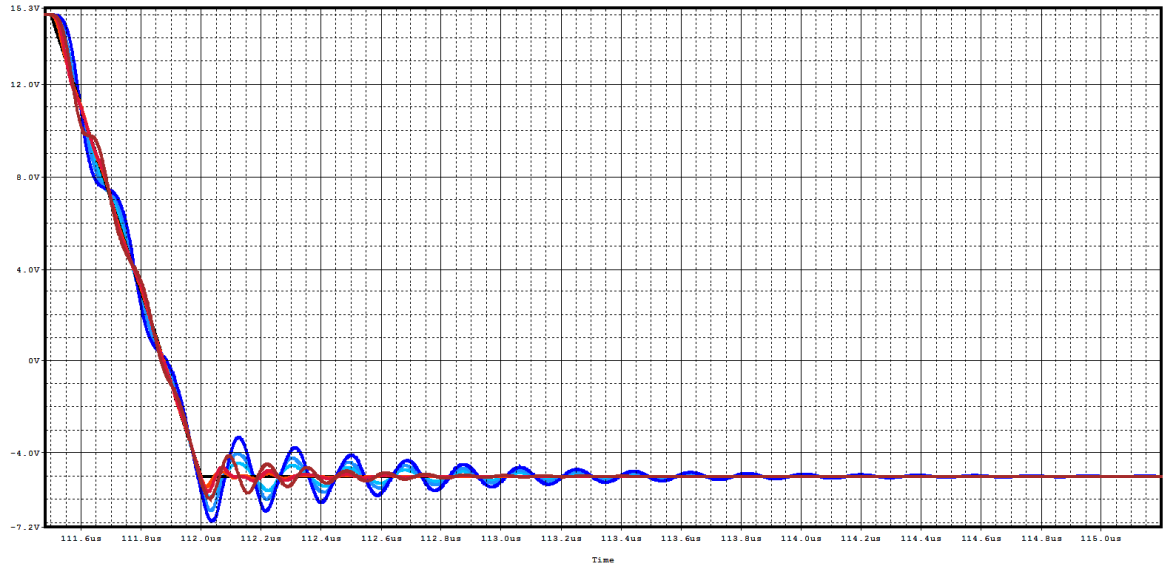


Figure 5-33: Turn-off voltage waveform for six coupled gate paths

Table 5-16: Voltage overshoots for six coupled gate paths

		GR1	GR2	GR3	GR4	GR5	GR6
$\Delta V/V_{Max}$ (%)	**Without Emitter Plate**	5.17	8.28	11.27	5.17	8.28	11.27
	With Emitter Plate	2.20	3.10	3.70	2.20	3.10	3.70
$\Delta V/V_{Min}$ (%)	**Without Emitter Plate**	15.62	23.15	28.01	15.62	23.15	28.01
	With Emitter Plate	8.18	11.70	16.35	8.18	11.70	16.35

As it can be seen for all of the six gate paths both turn-on and turn-off voltage overshoots are more in the scenario of without emitter plate.

This is explained that in the scenario of without emitter plate, only a partial inductance of the entire gate-emitter loop inductance has been considered, hence the current loop is not closed. By considering L1 as the inductance of gate source to each IGBT gate, and L2 as the inductance of emitter source to each IGBT emitter, L1 has a value of X nH and L2 has the zero value, since the emitter plate has not been considered. Hence the mutual inductance between L1 and L2 has a zero value. Therefore the apparent loop inductance which is determined by L_loop = L1 + L2 – 2 × M, is equal to L1 means X nH. But in the scenario of with emitter plate that the current loop is closed, L1 has a value of X nH and L2 has a value of Y nH. Since gate print and emitter plate are very close to each other, the coupling coefficient of K is very close to 1. Hence the mutual inductance between L1 and L2 which is determined by M_L1_L2 = K × $\sqrt{\mathrm{L1} \times \mathrm{L2}}$ has a large value this time. The apparent loop inductance is therefore much smaller than the scenario without emitter plate. Due to the smaller loop inductance in the scenario of with emitter plate, the voltage overshoot which is equal to V = - L × $\frac{\mathrm{dI}}{\mathrm{dt}}$ is also smaller.

Other than the emitter plate effect on voltage overshoots, it is observed that the voltage waveforms of different gate paths are quite in phase in the scenario of without emitter plate, while this is not true for the scenario of with emitter plate. This has been shown in figures 5-34 and 5-35.

This is because a large capacitance is formed between the gate paths and the emitter plate when the emitter plate is considered. The mentioned capacitance element does not exist in the scenario of without emitter plate and the voltage waveforms are in phase with each other. But when that capacitance is added the voltage waves are not any more in phase.

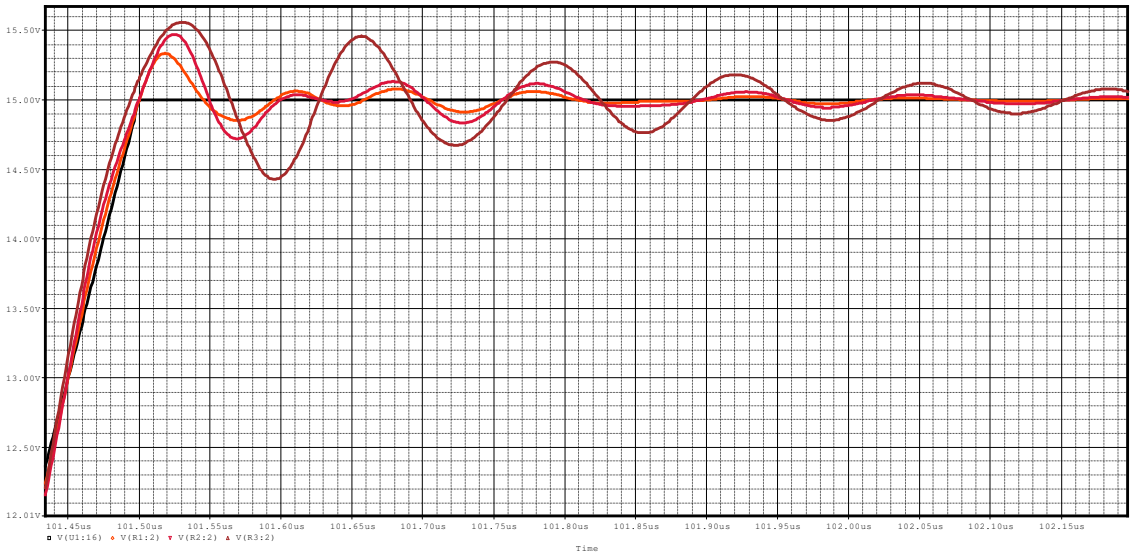


Figure 5-34: Turn-on voltage waveform for six coupled gate paths with emitter plate

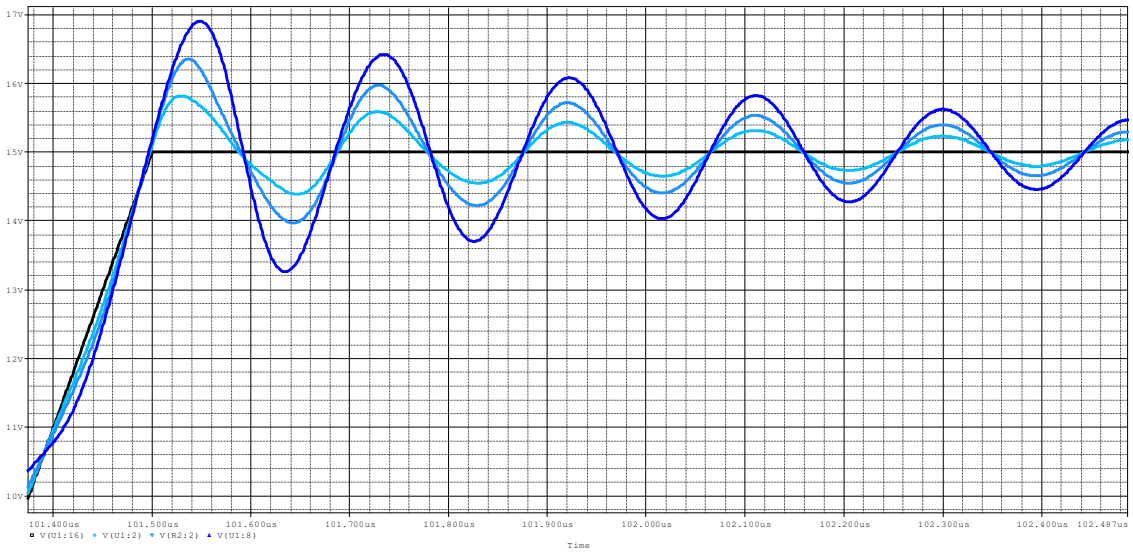


Figure 5-35: Turn-off voltage waveform for six coupled gate paths without emitter plate

5.6 Coupling Effect

In this section, the effect of the couplings between the different gate paths has been studied. In order to be able to judge about the couplings effect, the results of six gate paths without emitter plate is going to be compared in both scenarios of with and without couplings from the aspect of maximum voltage overshoots.

The PSpice parts created in the section 5.3.1.1 have been used in this section to build the PSpice test circuit for six decoupled gate paths without emitter plate as shown in figure 5-36.

Figures 5-37 and 5-38 show the turn-on and turn-off voltage waveforms at each gate path respectively in the case of six decoupled gate paths without emitter plate. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-36. Means that the black wave is the gate voltage received at the input terminals of the gate paths (V_{gate}) and the color waves are the gate voltages received at the output terminals of the gate paths (V_{output}) which are the same as the gates of IGBTs. Due to the gate print symmetry the gate voltages received at the gate of IGBTs Z4, Z5 and Z6 are the same as the gate voltages received at the gate of IGBTs Z1, Z2 and Z3 respectively. Therefore their corresponding waveforms are overlapping and that is why there are three voltage waveforms visible in figures 5-37 and 5-38 and not six.

Turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for each gate path in table 5-17 for the case of six decoupled gate paths without emitter plate.

Six Decoupled Gate Paths without Emitter Plate

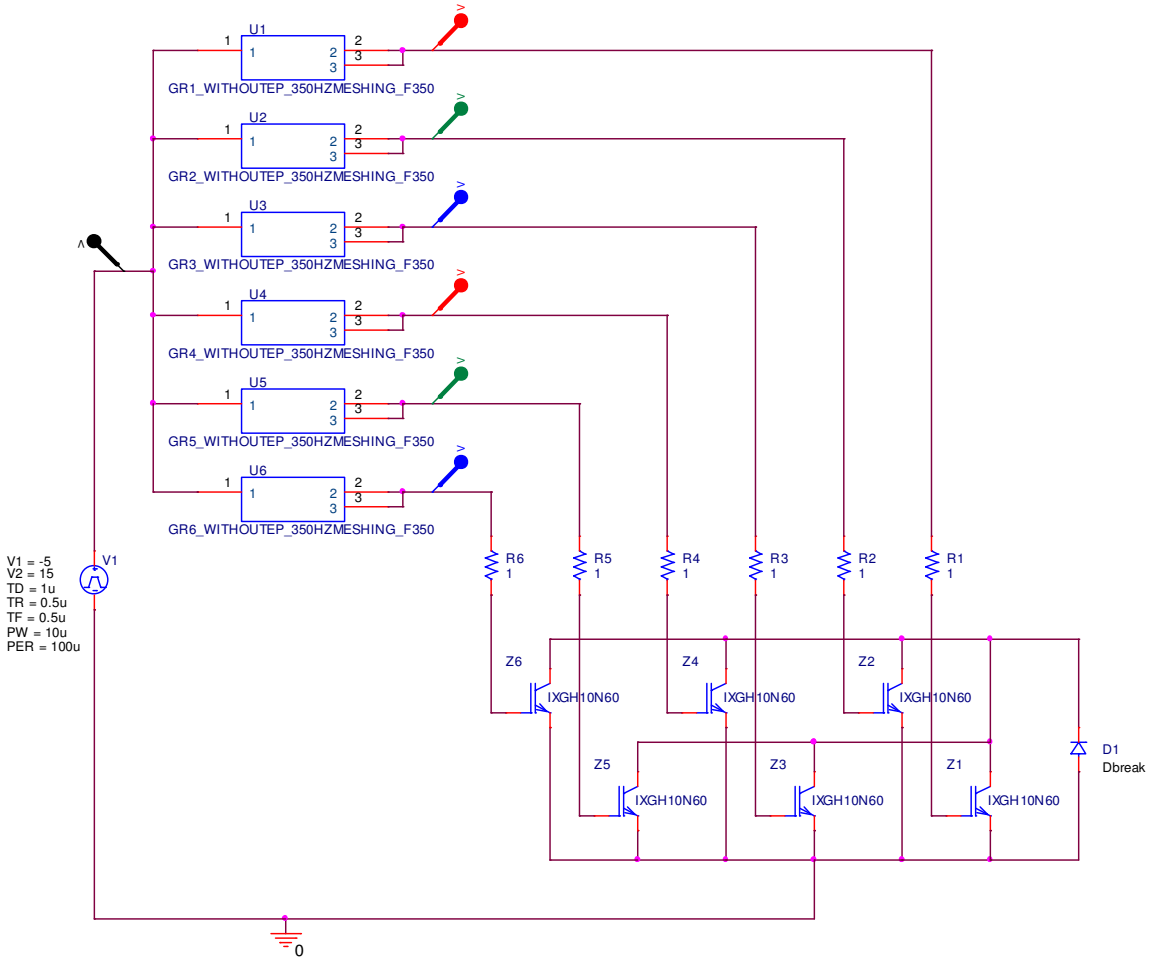


Figure 5-36: PSpice test circuit for six decoupled gate paths without emitter plate

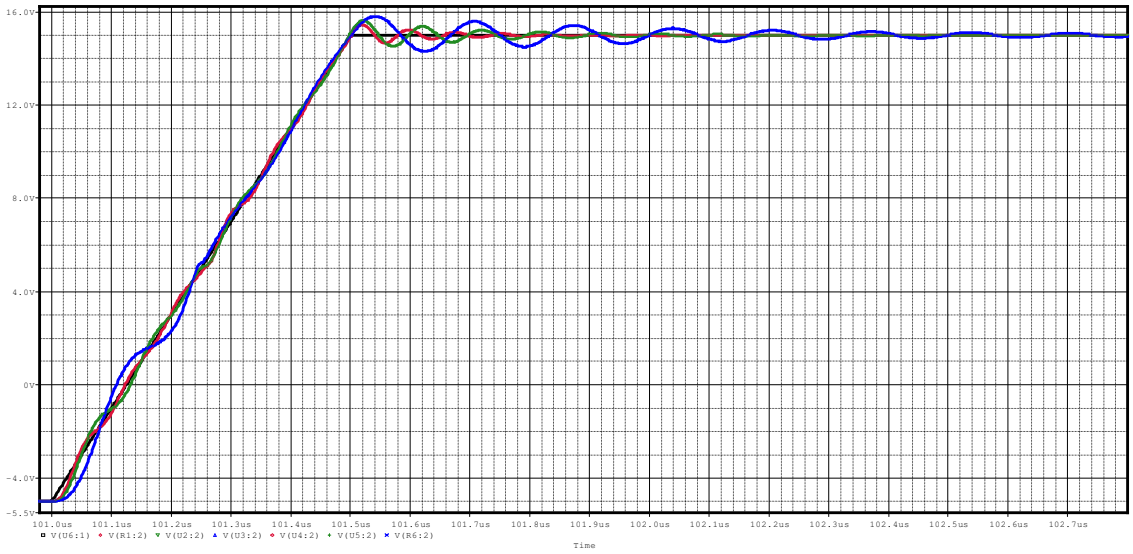


Figure 5-37: Turn-on voltage waveform for six decoupled gate paths without emitter plate

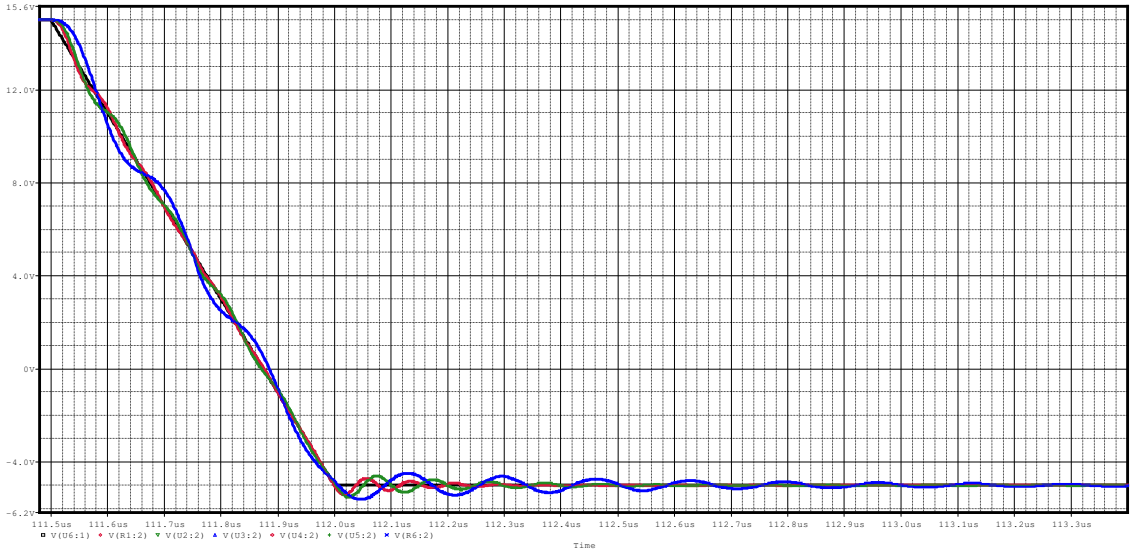


Figure 5-38: Turn-off voltage waveform for six decoupled gate paths without emitter plate

Table 5-17: Voltage overshoots for six decoupled gate paths without emitter plate

	GR1	**GR2**	**GR3**	**GR4**	**GR5**	**GR6**
$\Delta V/V_{Max}$ (%)	2.90	3.97	5.18	2.90	3.97	5.18
$\Delta V/V_{Min}$ (%)	7.72	9.20	10.89	7.72	9.20	10.89

After studying the six decoupled gate paths without emitter plate, it is now time for comparing its results with six coupled gate paths without emitter plate. The following figures show the turn-on and turn-off voltage waveforms of both scenarios of coupled and decoupled gate paths in the same figure for six gate paths without emitter plate. The blue curves are corresponding to the scenario of coupled gate paths and the red curves are corresponding to the scenario of decoupled gate paths. Turn-on and turn-off voltage overshoot in percentage of each gate path have been calculated and gathered in the following tables for both scenarios of coupled and decoupled gate paths.

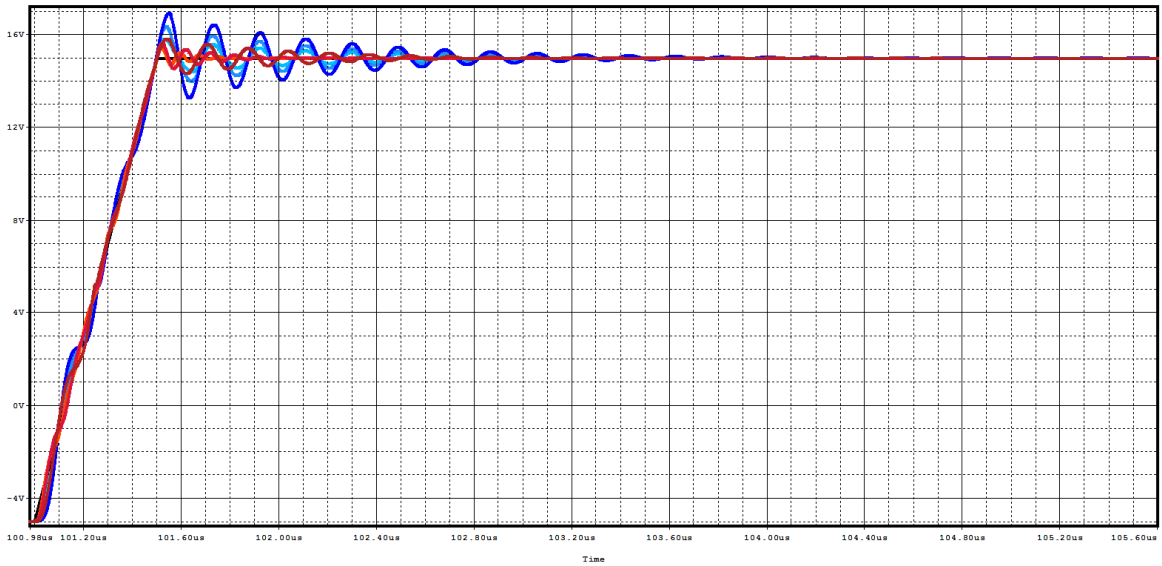


Figure 5-39: Turn-on voltage waveform for six gate paths without emitter plate

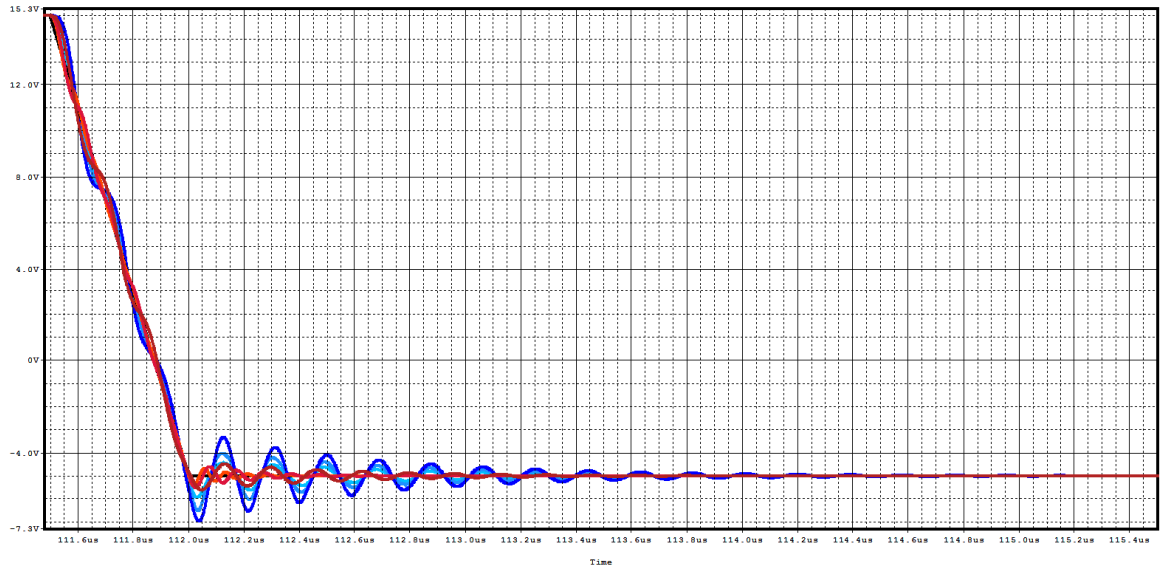


Figure 5-40: Turn-off voltage waveform for six gate paths without emitter plate

Table 5-18: Voltage overshoot for six gate paths without emitter plate

		GR1	GR2	GR3	GR4	GR5	GR6
$\Delta V/V_{Max}$ (%)	**Coupled Gate Paths**	5.17	8.28	11.27	5.17	8.28	11.27
	Decoupled Gate Paths	2.90	3.97	5.18	2.90	3.97	5.18
$\Delta V/V_{Min}$ (%)	**Coupled Gate Paths**	15.62	23.15	28.01	15.62	23.15	28.01
	Decoupled Gate Paths	7.72	9.20	10.89	7.72	9.20	10.89

As it can be seen, for all six gate paths without emitter plate, both turn-on and turn-off voltage overshoots are more in the scenario of coupled gate paths.

This is explained by the fact that in the scenario of decoupled gate paths, the total inductance for any gate path is equal to its self inductance since there is not any coupling with other gate paths. In the scenario of coupled gate paths, most coupling coefficients of K have small values, smaller than 0.5, in the corresponding SPICE netlist. Therefore the total inductance of any gate path is larger than its self inductance. Due to the larger total inductances for any gate path in the scenario of coupled gate paths, the voltage overshoot which is equal to V = - L × $\frac{dI}{dt}$ is also larger.

5.7 Circuital Schematics Approach

In the section 5.6, the PSpice parts created in the section 5.3.1.1 have been used to build the PSpice test circuit for six decoupled gate paths without emitter plate. But as mentioned earlier in the section 4.5, other than creating new parts in PSpice from the SPICE models (netlist approach), there is another way of importing the SPICE models into PSpice which is sketching the electrical circuit corresponding to each generated SPICE model by interpreting its netlist (circuital approach).As mentioned earlier the later way is only feasible for short netlists. Since the netlists obtained in 5.3.1.1 are short ones, they have been imported into PSpice by the later way in this section, and resulted to the test circuit shown in figure 5-41.

Figures 5-48 and 5-49 show the turn-on and turn-off voltage waveforms for six decoupled gate paths without emitter plate, built by the circuital approach, respectively.

Turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for each gate path in table 5-19 for the case of six decoupled gate paths without emitter plate built by circuital approach.

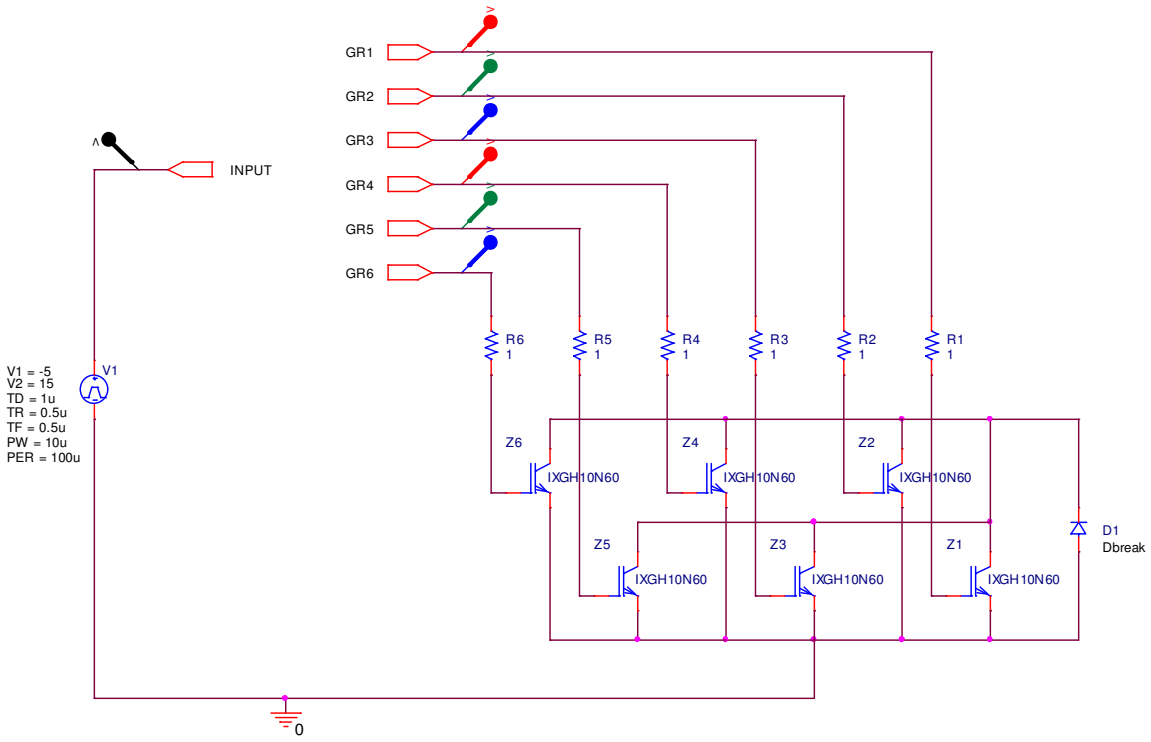


Figure 5-41: PSpice test circuit for six decoupled gate paths without emitter plate built by circuital approach

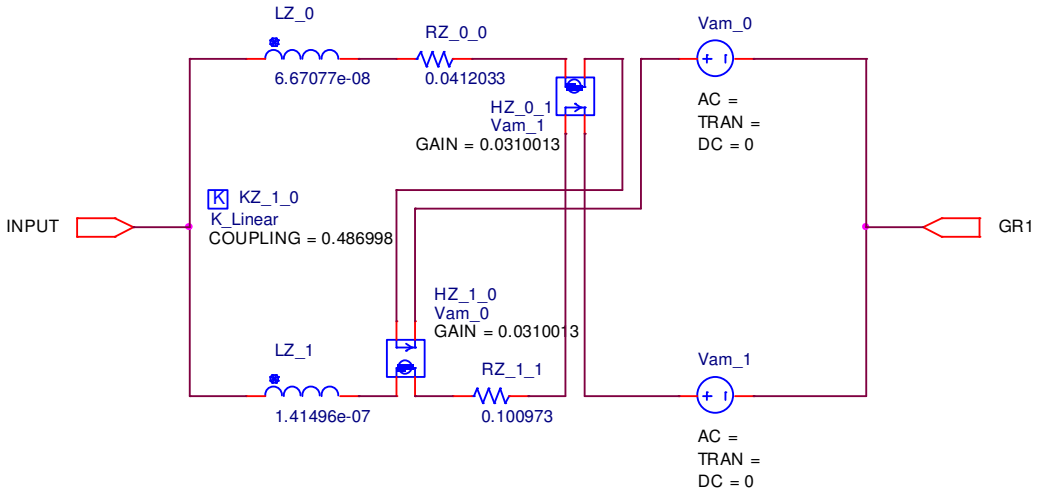


Figure 5-42: Electrical circuit corresponding to GR1

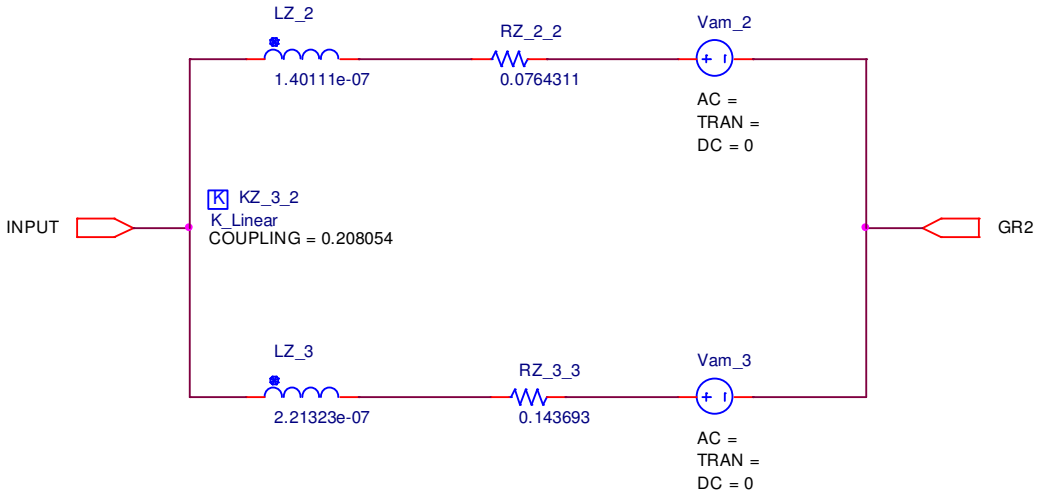


Figure 5-43: Electrical circuit corresponding to GR2

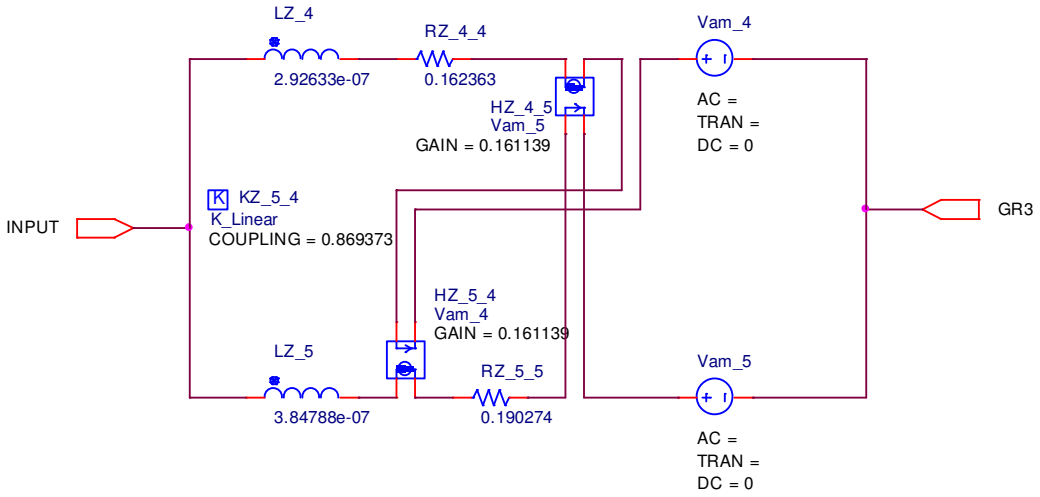


Figure 5-44: Electrical circuit corresponding to GR3

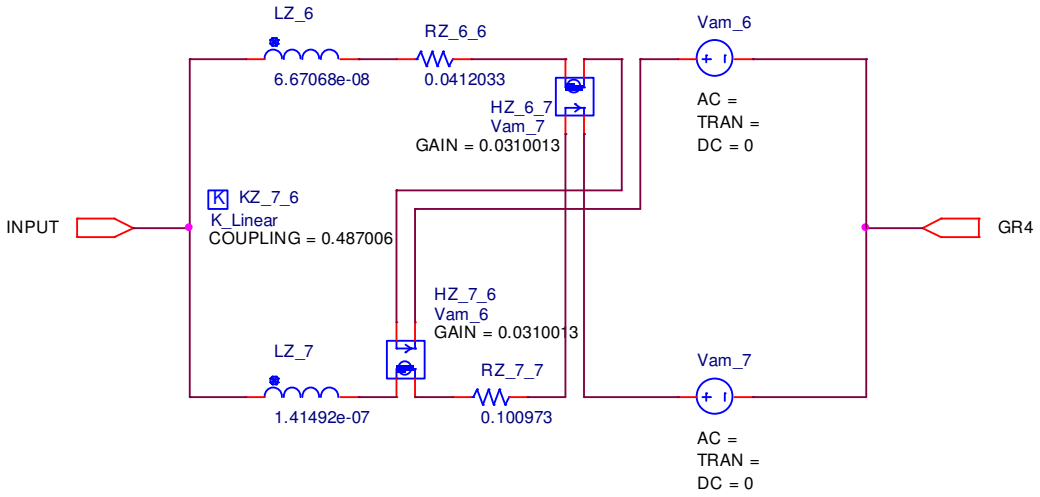


Figure 5-45: Electrical circuit corresponding to GR4

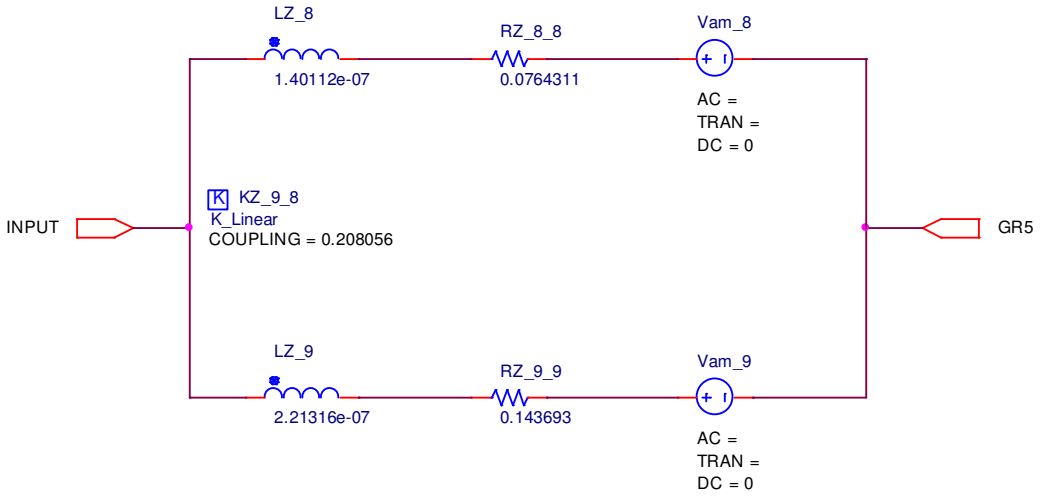


Figure 5-46: Electrical circuit corresponding to GR5

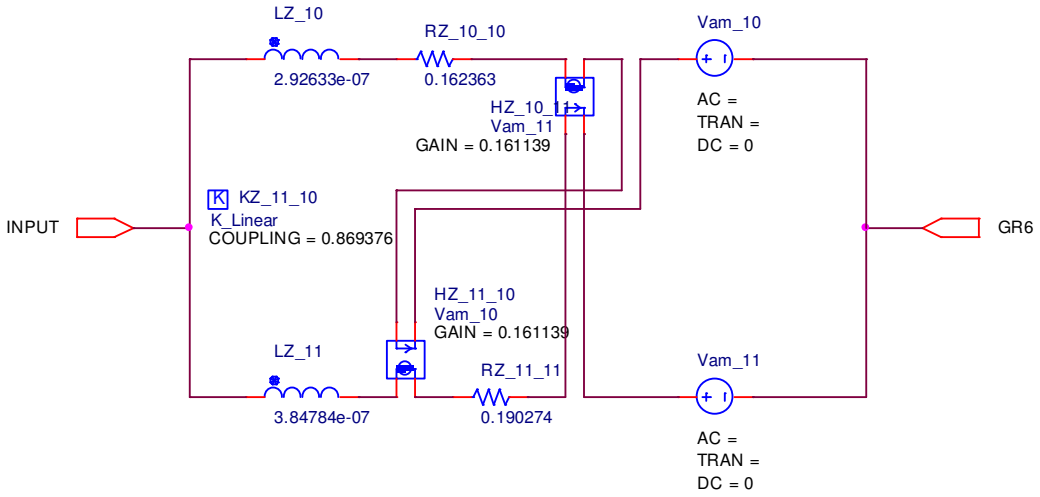


Figure 5-47: Electrical circuit corresponding to GR6

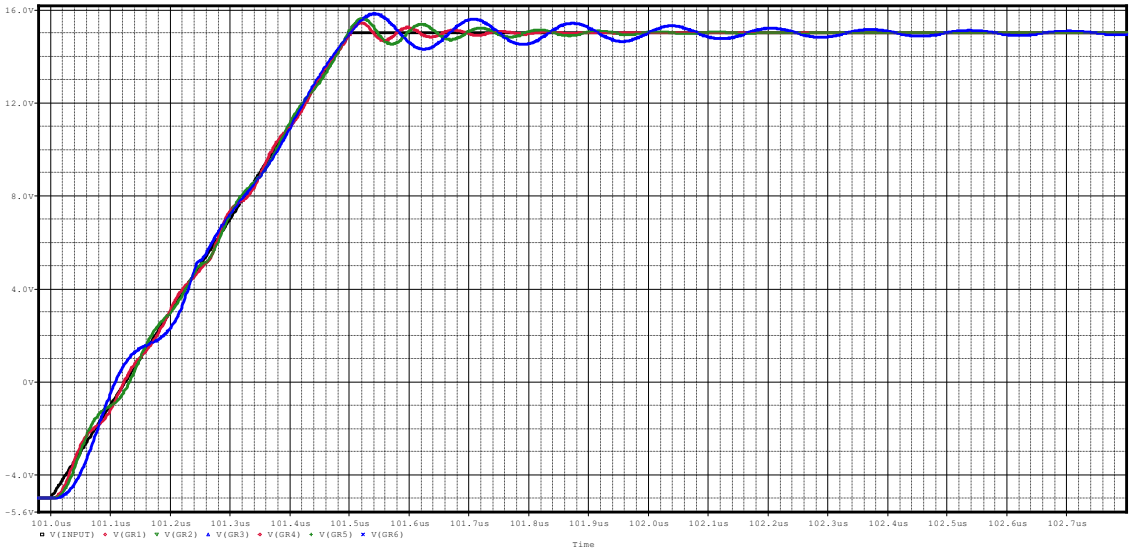


Figure 5-48: Turn-on voltage waveform for six decoupled gate paths without emitter plate, circuital approach

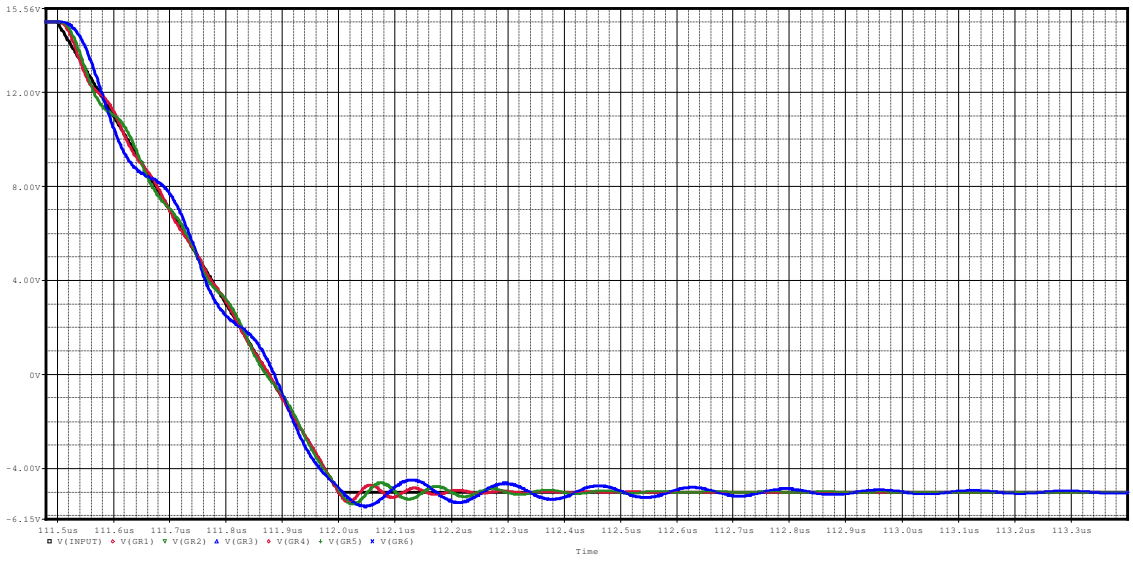


Figure 5-49: Turn-off voltage waveform for six decoupled gate paths without emitter plate, circuital approach

Table 5-19: Voltage overshoots for six decoupled gate paths without emitter plate, circuital approach

	GR1	**GR2**	**GR3**	**GR4**	**GR5**	**GR6**
$\Delta V/_{V_{Max}}$ (%)	2.90	3.97	5.18	2.90	3.97	5.18
$\Delta V/_{V_{Min}}$ (%)	7.72	9.20	10.90	7.72	9.20	10.90

By comparing the tables 5-17 and 5-19, it is found that there is a perfect match between the results obtained with circuital and netlist approach. **The advantage of working with the PSpice test circuit built by the circuital approach is that it provides the possibility to have a better view over the existing parasitic elements.**

Turn-on and turn-off voltage overshoot in percentage have been summed up in table 5-20 for six gate paths.

Table 5-20: Voltage overshoots for six gate paths

		GR1	**GR2**	**GR3**	**GR4**	**GR5**	**GR6**
$\Delta V/_{V_{Max}}$ (%)	**Coupled Gate Paths with Emitter Plate**	2.20	3.10	3.70	2.20	3.10	3.70
	Coupled Gate Paths without Emitter Plate	5.17	8.28	11.27	5.17	8.28	11.27
	Decoupled Gate Paths without Emitter Plate	2.90	3.97	5.18	2.90	3.97	5.18

$\Delta V/V_{Min}$ (%)	**Coupled Gate Paths with Emitter Plate**	8.18	11.70	16.35	8.18	11.70	16.35
	Coupled Gate Paths without Emitter Plate	15.62	23.15	28.01	15.62	23.15	28.01
	Decoupled Gate Paths without Emitter Plate	7.72	9.20	10.89	7.72	9.20	10.89

As it can be seen, the case of coupled gate paths without emitter plate has the highest voltage overshoots both at turn-on and turn-off.

5.8 Evaluation of All-One Gate Print

5.8.1 All-One Gate Print without Emitter Plate

In this scenario all-one gate print has been modeled and studied. Due to the frequency effect, as mentioned in section 5.4, the model meshing has been carried out according to 350 Hz skin depth and the RL Impedance Extraction simulation has been performed for the simulation frequency of 350 Hz.

The created PSpice part in this scenario has thirteen nodes since its corresponding BBT model possesses thirteen terminals. The node number 1 is the gate print input terminal and the remaining 12 nodes are the gate print output terminals. Due to the relations between the number of ports, which is twelve in this case, and the number of parasitic elements mentioned in the section 4.5, there are 12 resistances, 12 inductances, 132 mutual resistances and 66 mutual inductances in the SPICE netlist in this scenario. Extracting this number of elements requires a long simulation time. The created part in this simulation scenario is called AllOneGPWithoutEP_350HzMeshing_F350 and is shown as an example in figure 5-50. The reason that the nodes corresponding to each pair of output terminals are short circuited is that each of the IGBTs in PSpice test circuit represents all the 6 IGBTs in that specific sub-module.

Figures 5-51 and 5-52 show the turn-on and turn-off voltage waveforms at each sub-module respectively. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-50. Means that the black wave is the gate voltage received at the input terminal (V_{gate}) and the color waves are the gate voltages received at the output terminals (V_{output}) which are the same as the gates of IGBTs. Due to the gate print symmetry the gate voltages received at the gate of IGBTs Z4, Z5 and Z6 are the same as the gate voltages received at the gate of IGBTs Z1, Z2 and Z3 respectively. Therefore their corresponding waveforms are overlapping and that is why there are three voltage waveforms visible in figures 5-51 and 5-52 and not six.

Turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for each sub-module in table 5-21 for all-one gate print without emitter plate.

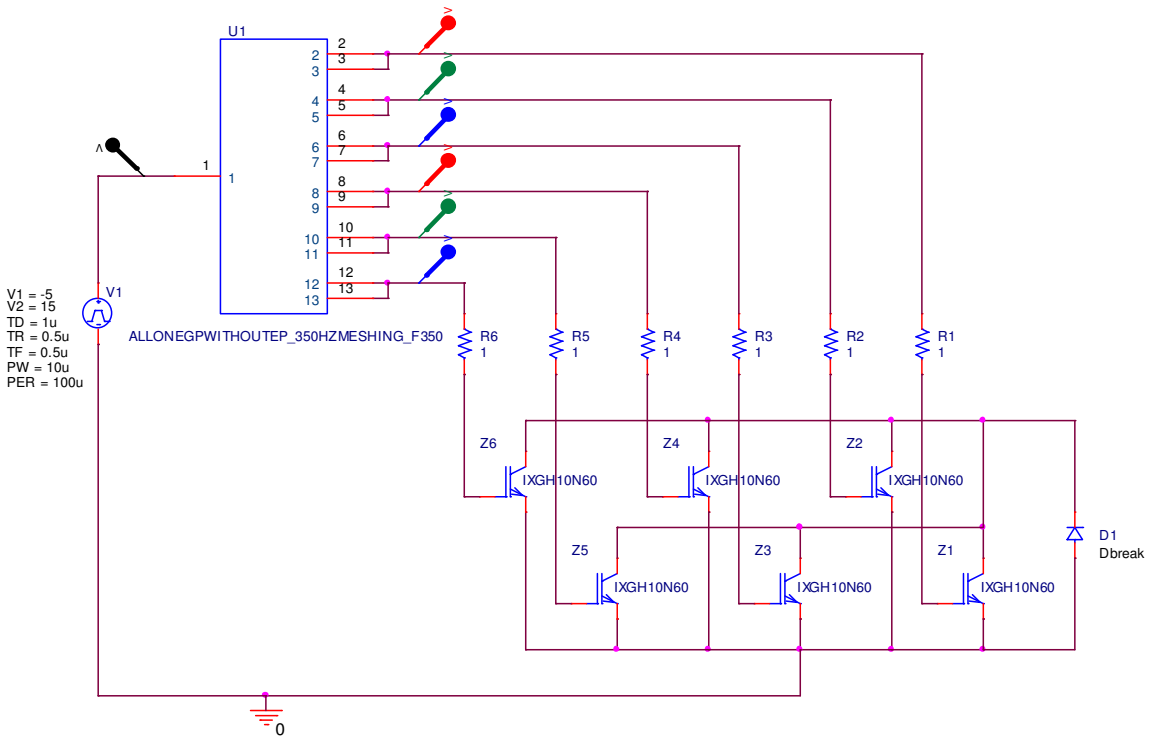


Figure 5-50: PSpice test circuit for all-one gate print without emitter plate

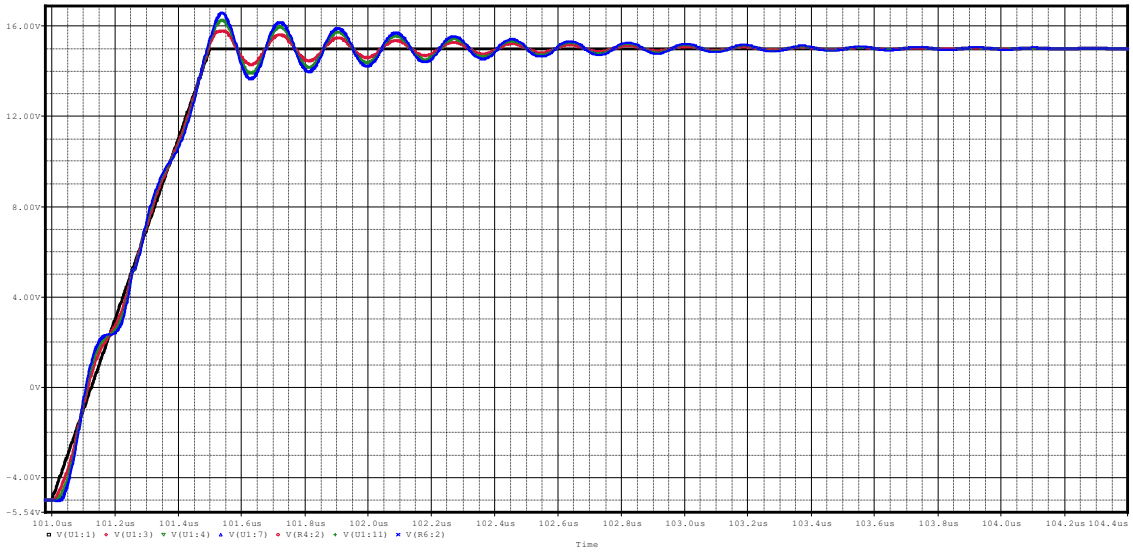


Figure 5-51: Turn-on voltage waveform for all-one gate print without emitter plate

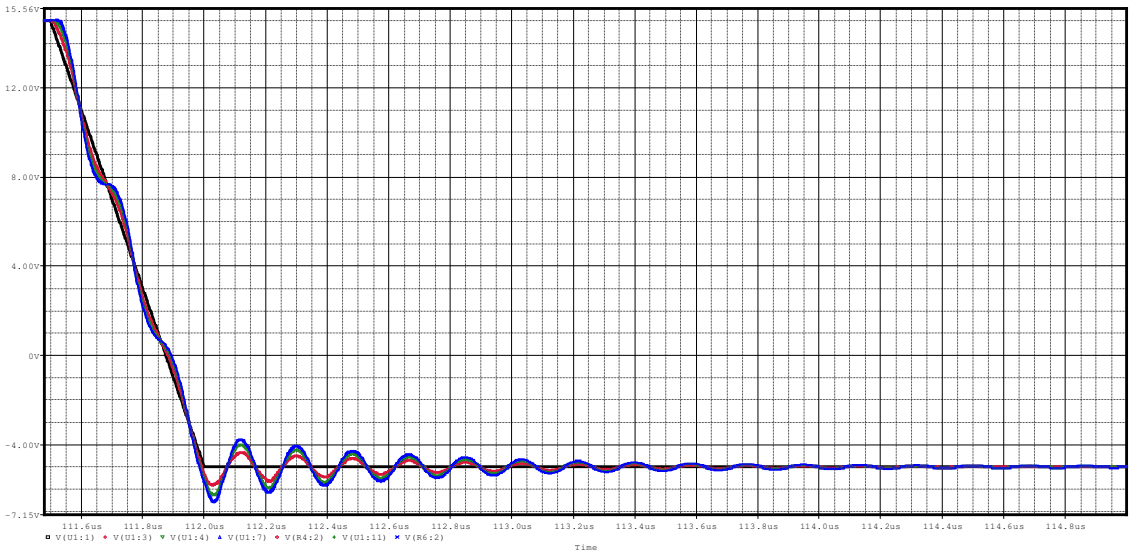


Figure 5-52: Turn-off voltage waveform for all-one gate print without emitter plate

Table 5-21: Voltage overshoot in percentage for all-one gate print without emitter plate

	Sub-Module 1	**Sub-Module 2**	**Sub-Module 3**	**Sub-Module 4**	**Sub-Module 5**	**Sub-Module 6**
$\Delta V/V_{Max}$ **(%)**	4.88	7.63	9.52	4.88	7.63	9.52
$\Delta V/V_{Min}$ **(%)**	14.12	20.16	24.00	14.12	20.16	24.00

5.8.2 All-One Gate Print with Emitter Plate

In this scenario all-one gate print and the emitter plate have been modeled and studied. The model meshing has been carried out according to 350 Hz skin depth and the RL Impedance Extraction simulation has been performed for the simulation frequency of 350 Hz.

The created PSpice part in this scenario has 27 nodes since its corresponding BBT model possesses 27 terminals, which 13 of them belong to the all-one gate print and the other 14 belong to the emitter plate and are located below the gate print terminals. Hence there will be 24 ports which 12 of them are gate print ports and 12 of them are the emitter plate ports. The node number 1 is the input terminal corresponding to gate print and the nodes number 14 and 21 are the input terminals corresponding to emitter plate. The remaining nodes are the output terminals of both gate print and emitter plate. Due to the relations between the number of ports, and the number of parasitic elements mentioned in the section 3.5, there are 24 resistances, 24 inductances, 552 mutual resistances and 276 mutual inductances in

the SPICE netlist in this scenario. Extracting this huge number of elements requires a very long simulation time more than 24 hours. The created part in this simulation scenario is called AllOneGPWithEP_350HzMeshing_F350 and is shown as an example in figure 5-53. The reason that the nodes corresponding to each pair of output terminals are short circuited is that each of the IGBTs in PSpice test circuit represents all the 6 IGBTs in that specific sub-module.

Figures 5-54 and 5-55 show the turn-on and turn-off voltage waveforms at each sub-module respectively. Each voltage waveform corresponds to the voltage probe with the same color shown in figure 5-53. Means that the black wave is the gate voltage received at the input terminals (V_{gate}) and the color waves are the gate voltages received at the output terminals (V_{output}) which are the same as the gates of IGBTs. Due to the gate print symmetry the gate voltages received at the gate of IGBTs Z4, Z5 and Z6 are the same as the gate voltages received at the gate of IGBTs Z1, Z2 and Z3 respectively. Therefore their corresponding waveforms are overlapping and that is why there are three voltage waveforms visible in figures 5-54 and 5-55 and not six.

Turn-on and turn-off voltage overshoot in percentage have been calculated and gathered for each sub-module in table 5-22 for all-one gate print with emitter plate.

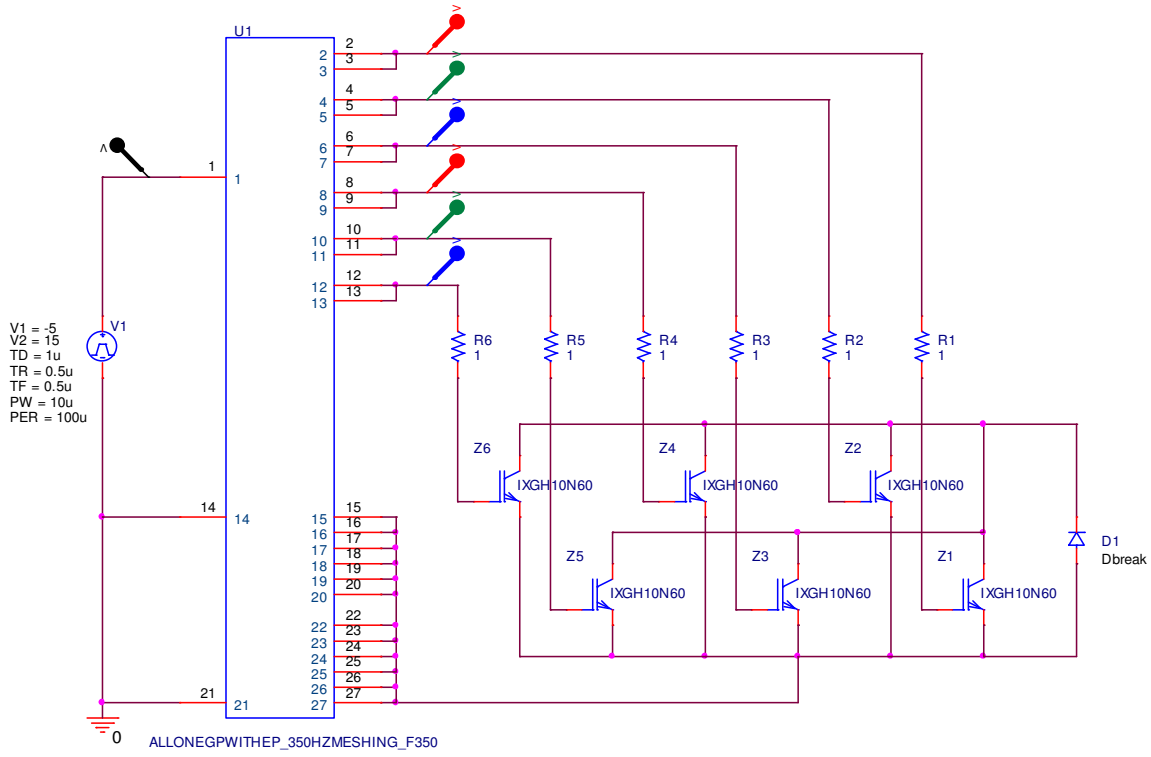


Figure 5-53: PSpice test circuit for all-one gate print with emitter plate

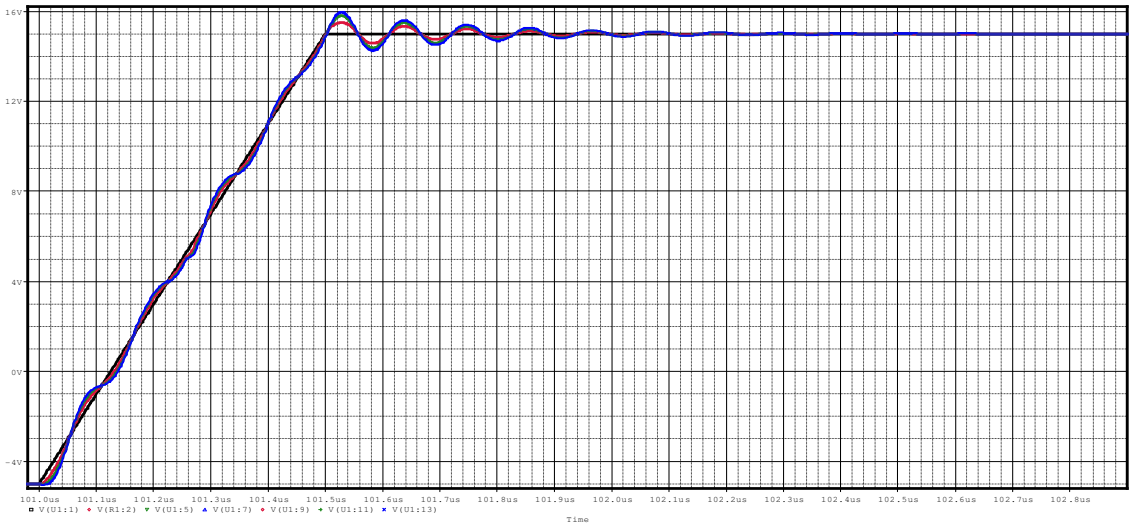


Figure 5-54: Turn-on voltage waveform for all-one gate print with emitter plate

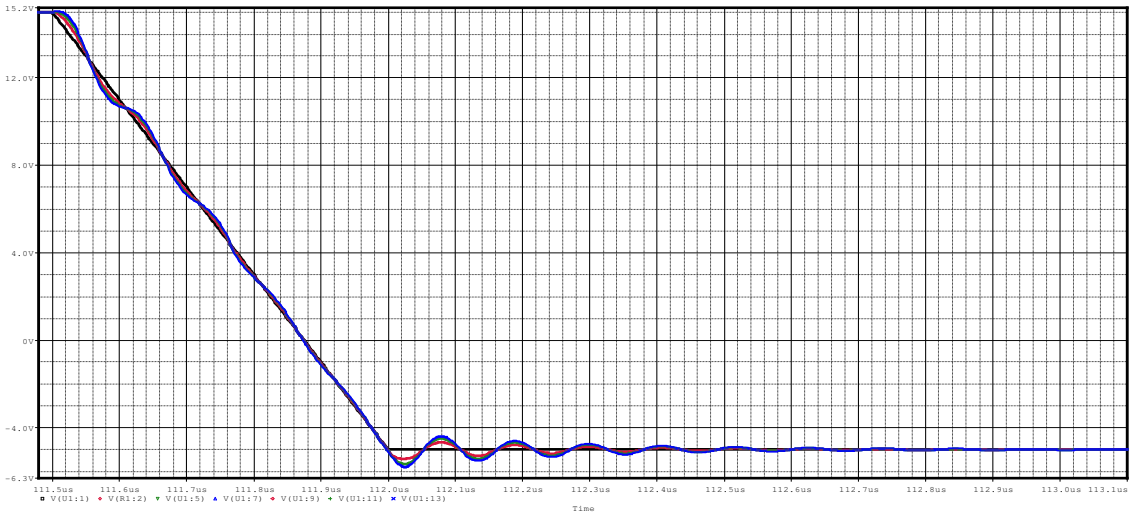


Figure 5-55: Turn-off voltage waveform for all-one gate print with emitter plate

Table 5-22: Voltage overshoot in percentage for all-one gate print with emitter plate

	Sub-Module 1	**Sub-Module 2**	**Sub-Module 3**	**Sub-Module 4**	**Sub-Module 5**	**Sub-Module 6**
$\Delta V / V_{Max}$ **(%)**	3.24	5.06	6.04	3.24	5.06	6.04
$\Delta V / V_{Min}$ **(%)**	7.57	11.73	13.96	7.57	11.73	13.96

5.9 Comparison of Gate Print Designs

In this section, two designs of the gate print are compared in both scenarios of with and without emitter plate from the aspect of maximum voltage overshoots. It should be mentioned that for separated gate print, the case of coupled gate paths has been considered in this comparison. In the following figures the blue curves are corresponding to all-one design and the red curves are corresponding to separated design.

Without Emitter Plate

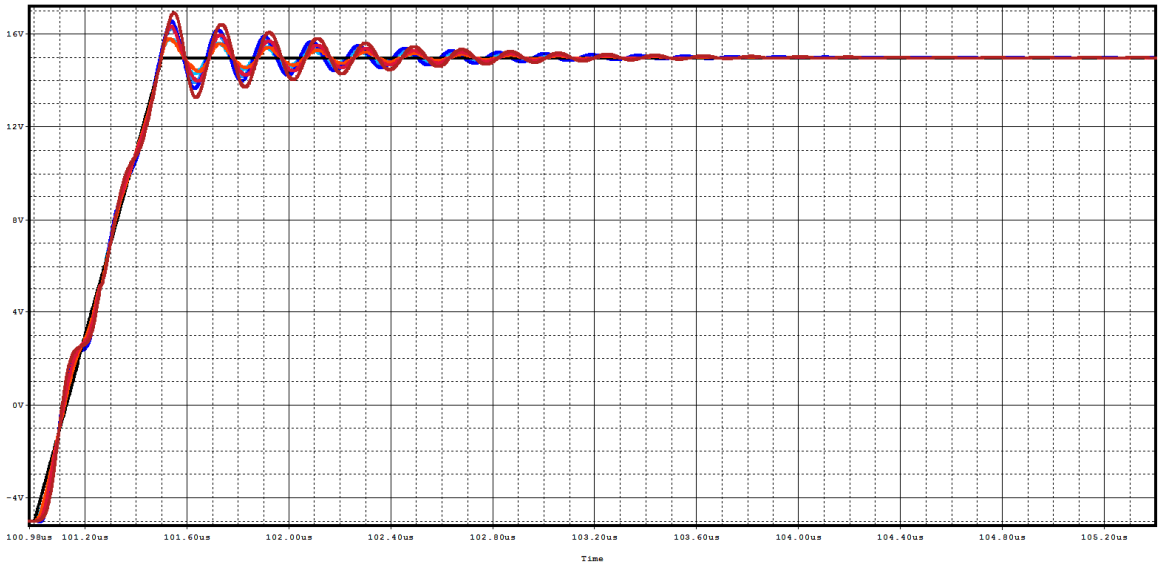


Figure 5-56: Turn-on voltage waveform of both gate print designs without emitter plate

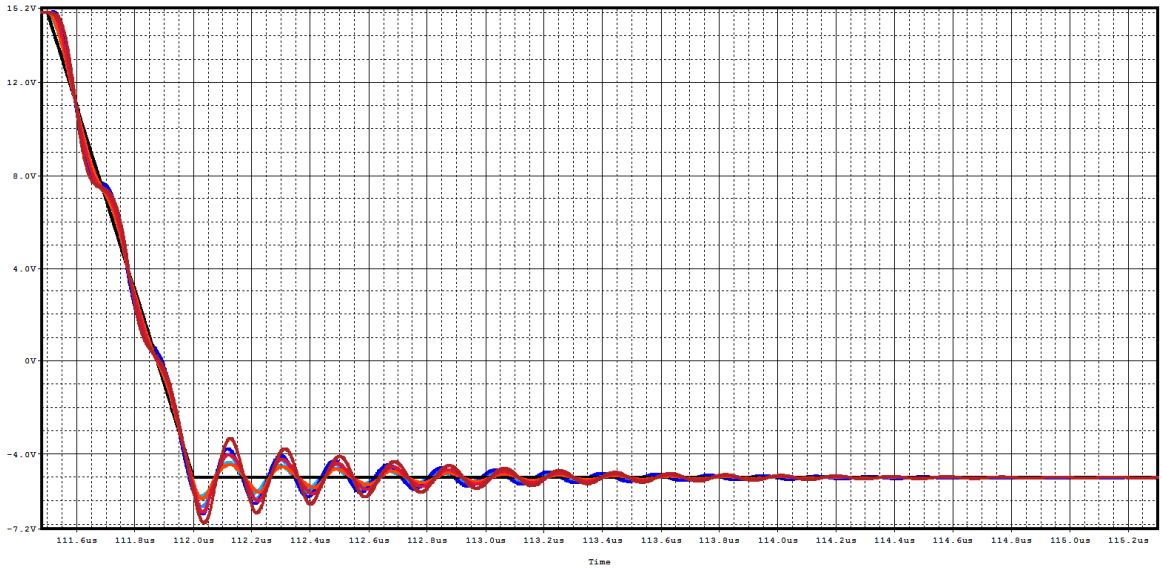


Figure 5-57: Turn-off voltage waveform of both gate print designs without emitter plate

Table 5-23: Voltage overshoot in percentage for both gate print designs without emitter plate

		Sub-Module 1	Sub-Module 2	Sub-Module 3	Sub-Module 4	Sub-Module 5	Sub-Module 6
$\Delta V/V_{Max}$ (%)	Separated Design	5.17	8.28	11.27	5.17	8.28	11.27
	All-One Design	4.88	7.63	9.52	4.88	7.63	9.52
$\Delta V/V_{Min}$ (%)	Separated Design	15.62	23.15	28.01	15.62	23.15	28.01
	All-One Design	14.12	20.16	24.00	14.12	20.16	24.00

As it can be seen, in the scenario of without emitter plate, both turn-on and turn-off voltage overshoots are up to 15.5% higher in the case of separated gate print.

With Emitter Plate

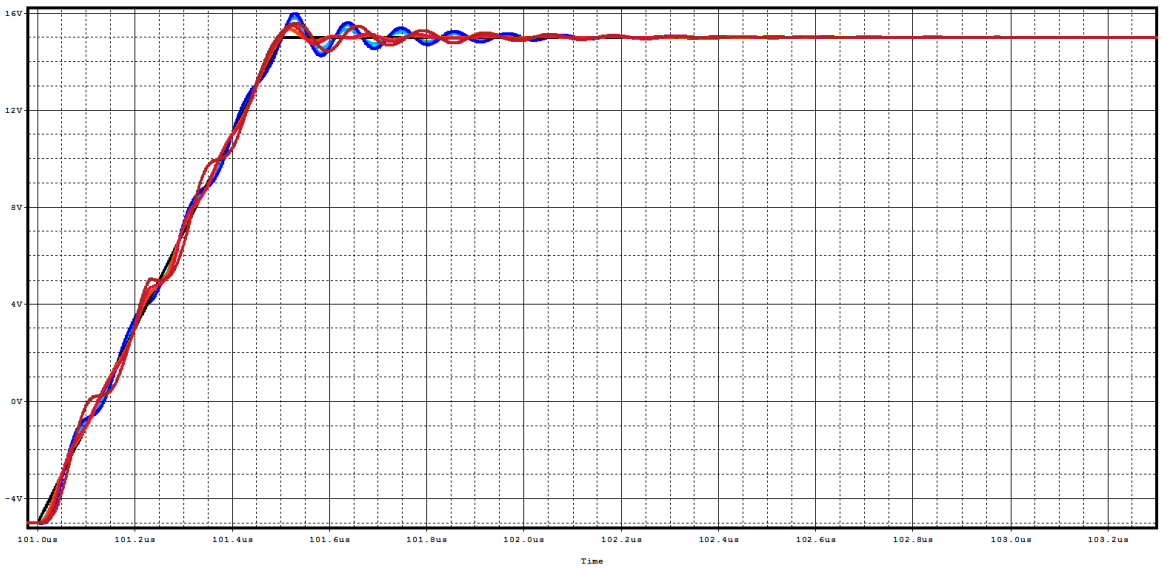


Figure 5-58: Turn-on voltage waveform of both gate print designs with emitter plate

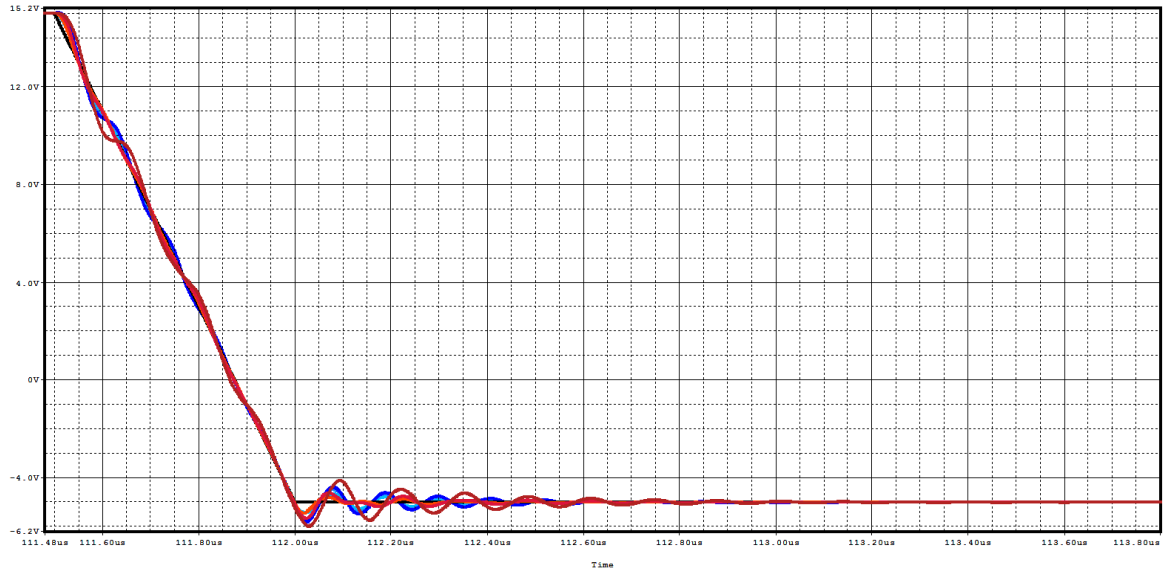


Figure 5-59: Turn-off voltage waveform of both gate print designs with emitter plate

Figure 5-24: Voltage overshoot in percentage for both gate print designs with emitter plate

		IGBT Sub-Module 1	IGBT Sub-Module 2	IGBT Sub-Module 3	IGBT Sub-Module 4	IGBT Sub-Module 5	IGBT Sub-Module 6
$\Delta V/V_{Max}$ (%)	**Separated Design**	2.20	3.10	3.70	2.20	3.10	3.70
	All-One Design	3.24	5.06	6.04	3.24	5.06	6.04
$\Delta V/V_{Min}$ (%)	**Separated Design**	8.18	11.70	16.35	8.18	11.70	16.35
	All-One Design	7.57	11.73	13.96	7.57	11.73	13.96

As it can be seen, in the scenario of with emitter plate, turn-on voltage overshoots are up to 39% higher in the case of all-one gate print, but turn-off voltage overshoots are up to 15% higher in the case of separated gate print.

6 CONCLUSION AND FUTURE WORK

Parasitic elements of two IGBT StakPak gate print designs have been extracted by the modeling platform built in BusBar Tool software. The effects of several parameters including emitter plate, couplings and skin effect have been modeled and analyzed. SPICE models obtained from BusBar Tool simulations have been imported into PSpice and have been put into the desired test circuit in each simulation scenario to evaluate the IGBT positions. A PSpice circuital schematics test circuit has been built for studying the separated gate print which provides a better overview on parasitic elements. Two gate print designs have been compared through several simulation scenarios, regarding their parasitic elements, hence maximum voltage overshoots and time delays.

The IGBTs PSpice library models used in test circuits can be replaced in the future by StakPak Lauritzen model built by N. Mora in ABB SECRC.

The model can be studied in another PEEC software capable of capacitance calculation which was not possible in BusBar Tool. Parasitic elements can also be extracted by an FEM software and the results can be compared with BBT.

Possible different junction temperatures due to the different gate print designs can be studied.

It is necessary to validate the modeling platform built in this project with experimental results (Didier Cottet from ABB CHCRC has been the reference for all-one model).

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