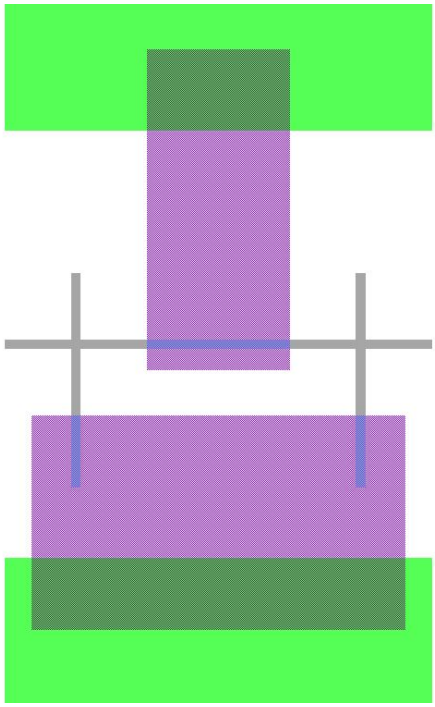

Reliability and reproducibility of Josephson junction fabrication

- Steps towards an optimized process

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With the support of the
Erasmus+ Programme
of the European Union

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Thesis for the degree of Erasmus Mundus Master of Science in Nanoscience and Nanotechnology

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Reliability and reproducibility of Josephson junction fabrication

Steps towards an optimized process

Amr Osman

Abstract

We investigated the reliability and reproducibility of the fabrication process of Al/AlOx/Al Josephson junctions with varying sizes using the cross-type lithography technique. Room temperature resistance measurements on thousands of junctions showed a standard deviation varying from 0.8% and 5.5% depending on the junction size, and a fabrication yield higher than 97%. Additionally, we investigated two steps towards optimizing the fabrication process. Firstly, the Ar-ion milling duration was reduced, whose effect on the junction quality remains to be investigated. Secondly, a one-step fabrication technique of Josephson junction is proposed in this thesis. Such a technique reduces the number of lithography steps needed, and in addition, Ar-ion milling of the substrate is avoided. This technique proves to be very reliable for small JJ sizes, with a fabrication yield also higher than 97%. However, further work is needed in order to reduce its standard deviation, in addition to low temperature measurements to investigate the quality of qubits fabricated using these JJs. Finally, a tentative study for the ageing of Josephson junctions was investigated over the course of 180 days showing an average increase in the resistance of only $\sim$5%.

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Acknowledgement

I would like to express my gratitude and appreciation to anyone who assisted me in this thesis, and anyone who helped me be where I am. Thank you ...

... Anita Fadavi for your supervision and guidance. Your elaborate explanations, cleanroom trainings, our discussion and your patience allowed me to learn a lot in a short time. Your supportive attitude made a big difference in this project.
... Philip Krantz for giving me the opportunity to work on this project and for your guidance, advice and continuous support. Your door is always open to everyone.
... Per Delsing and Jonas Bylander for your supervision and valuable input.
... James Simon for working with me through some parts of the project. You always came up with smart ideas.
... Andreas Bengtsson for your valuable input and the fabrication recipes you took great part in providing.
... Henrik Frederiksen for your training and continuous support on the *Plassys*.
... Bengt Nilsson for your EBL training and the knowledge you provided.
... David Niepce for training me in the low temperature measurement lab.
... the whole Chalmers QT group for being of great support, and always willing to help.
... Thilo Bauch for taking care of all EMM-Nano students in Chalmers, and answering our many questions throughout the year. Also for being my external referee.
... Guido Groeseneken, Bart Soree and Mark Heyns for allowing me to be part of EMM-Nano, and your guidance throughout the whole master's. The knowledge I gained in this program is more than I ever thought of.
... Joris Van de Vondel for being my KU Leuven co-promoter.
... Michel Houssa, my mesoscopic physics and electronic transport professor. I do not think I ever had a professor that explained physics better.
... Ahmed Kenawy, my friend who convinced me to study the second year of my master's at chalmers and informing me about the QT group.
... Hassanein Amer, my bachelor electronics professor and the head of the first research group I joined. With your supervision and support, I published my first paper as an undergraduate. Thanks for always believing in me.
... the American University in Cairo for granting me the scholarship to study my bachelor. That was the first step that opened lots of opportunities in my life.
... my parents for always encouraging me to be a better person.

To anyone who ever taught me something, and anyone who ever wished me success and happiness, I am grateful!

Contents

Chapter 1

Introduction

1.1 Motivation

Since the prediction of Josephson Effect in 1962, Josephson junctions have been widely used in superconducting circuits with a role as important as that of transistors in semiconducting circuits. The Josephson Effect manifests itself when two superconducting electrodes are connected via a weak link; a superconducting constriction or a thin insulating layer. If the weak link is thin enough such that the wave-functions of the electrodes overlap, Cooper pairs can tunnel through the barrier, resulting in a flow of supercurrent. As important building blocks in low temperature devices, Josephson junctions are found in many superconducting circuits, including superconducting qubits, and parametric amplifiers.

Nowadays, there is a worldwide competition towards building quantum computers. As the race heats up and the qubit numbers in a device increase, it becomes more evident that one requires robust fabrication processes which deliver devices that match the design parameters. It would be severely difficult to operate a multi-qubit system if the qubit frequencies[1] do not agree with the design. Or in the case of a travelling wave parametric amplifier, the circuit is composed of a long chain of Josephson junctions (inductors) and capacitors, arranged like a lumped element transmission line. In most cases, these junctions must be identical and impedance matched with the capacitors; otherwise the signal amplification will suffer due to unwanted reflections in the circuit. As such, it is essential to set up a procedure to monitor the fabrication process and measure and characterize the devices that are made, to tune the process parameters, and indicate possible shortcomings or drifts.

This thesis is focused on investigating the reliability and reproducibility of one of the techniques of fabricating Josephson junctions. The Josephson test junctions are

[1] A qubit frequency is $\omega_q = E_{01}/\hbar$, where E_{01} is the difference between the two lowest energy levels of the qubit

thereafter characterized by obtaining their normal resistance (at room temperature), using 4-point probe measurement. Since the normal resistance is inversely proportional to the critical current of the Josephson junction, it provides vital information about the junction's behavior at low temperature. Furthermore, an essential part of the characterization is providing statistically significant results, which involves acquiring a large enough data set. Therefore, in this thesis, we fabricate more than four thousand test junctions with different dimensions on 2-inch wafers. In addition, we design a programmable, automated 4-point probe measurement set-up to enable fast and reliable measurement of this large number of test junctions.

Furthermore, we explore the possibility of optimizing the fabrication process by reducing the number of required steps. Typically the process needs two lithography/ deposition steps; one for making the junctions, and a second one to connect the junctions to the rest of the circuit. In this thesis, we propose a method of fabricating both the junction and the patch layer in one lithography/deposition run, by tweaking the design layout, deposition and ion milling angles.

In the following, we briefly introduce Josephson junctions, and some of their applications. Then we explain how the room temperature resistance of a Josephson junction is related to the junction properties at low temperature.

1.2 Josephson Effect

Josephson junction (JJ), named after Brian D. Josephson [1], is the most important component in superconducting electronic circuits. A junction is formed when two superconducting electrodes are separated by a weak link or an insulating layer. The junction barrier has to be such that it allows for the wave functions of the Cooper pairs Ψ_1 and Ψ_2 on both sides to overlap (Fig. 1.1 (a)). Josephson predicted that the electron pairs can tunnel through the barrier from either side of the junction, even in the absence of an applied voltage, and generate a supercurrent [1] . The current across the junction is given by the following relation:

$$I = I_c \sin \varphi \ , \tag{1.2.1}$$

where I_c is the *critical current*, i.e. the maximum supercurrent that can flow through the junction before it becomes resistive, and $\varphi = \varphi_2 - \varphi_1$ is the phase difference between the superconductors. In the absence of an applied voltage, φ is constant, and this is referred to as *dc Josephson effect*. However, if there is a potential difference V across the junction, the phases of the two superconductors are not locked anymore but they slip relative to each other [2]. And the rate of change of φ is given by,

$$\frac{d\varphi}{dt} = \frac{2e}{\hbar} V, \tag{1.2.2}$$

where $\hbar$ is Plank's constant over 2π. This is referred to as *ac Josephson effect*, which results in an oscillatory behaviour for the current passing through the junction, leading to a time-dependent current $I_s = I_c \sin\varphi(t)$ (Fig. 1.1 (c)). However, if the bias voltage is high enough to break the bond of Cooper pairs, the junction will behave as a normal resistance with linear $I - V$ characteristics. This takes place when $V > 2\Delta/e$, where Δ is the superconducting gap shown in Fig. 1.1 (d) [3]. The symbol for JJ is also shown in Fig. 1.1 (b), which can be represented by a junction and a capacitor in parallel.

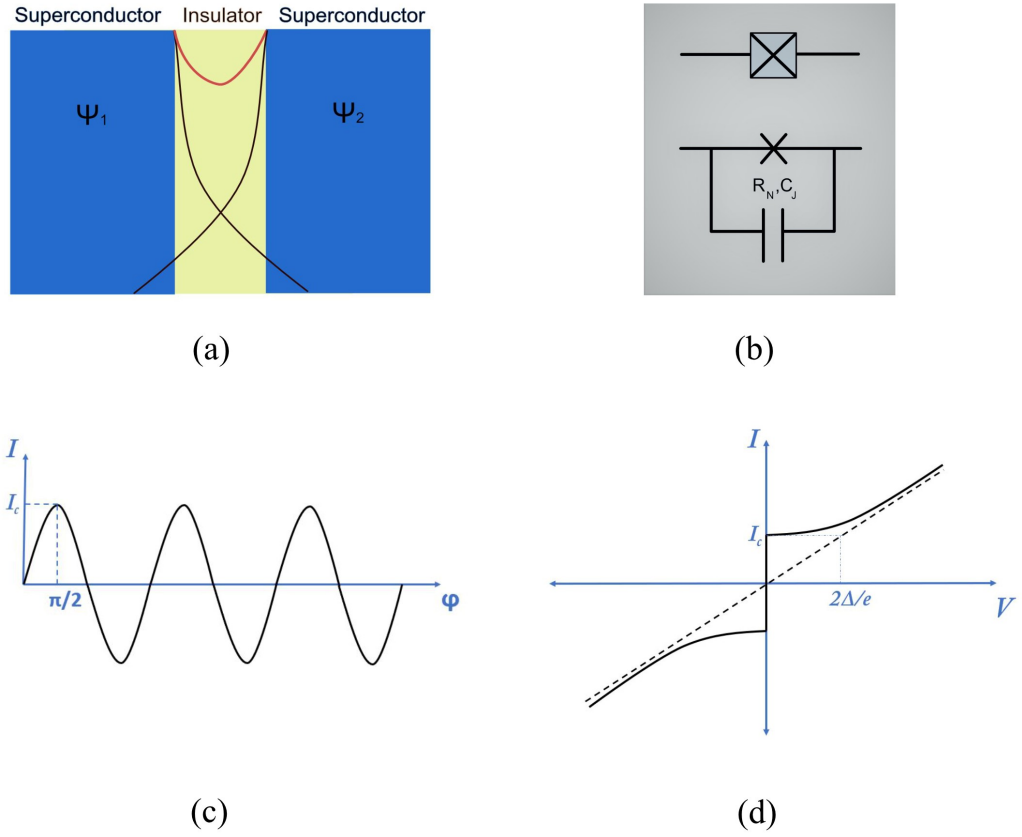


Figure 1.1: (a) JJ structure, where the wave function of both superconductors (black) overlap resulting in one wave function (red), (b) JJ symbol, (c) The current-phase relation, and (d) I-V characteristics at low temperature (solid curve), and at high temperature (dashed line).

1.3 dc-SQUID

One of the most common circuit elements that is composed of JJs is the Superconducting Quantum Interference Device *(SQUID)*, which may consist of two or multiple junctions in a parallel array interconnected by superconducting lines. In this section, we focus our discussion on the *dc SQUIDs* where two junctions are connected in a loop (Fig. 1.2). In this case, Eq. (1.2.1) can be expanded into

$$I = I_{c1}\sin(\varphi_1) - I_{c2}\sin(\varphi_2), \tag{1.3.1}$$

The relation between the the phases and the flux inside the loop is given by [2]

$$\varphi_2 = \varphi_1 + 2n\pi - 2\pi\frac{\Phi}{\Phi_o}, \tag{1.3.2}$$

indicating that the flux inside the loop is quantized. In Eq. (1.3.2), Φ is flux inside the loop and $\Phi_o = h/2e$ is the magnetic flux quantum. Combining Eq. (1.3.1) and Eq. (1.3.2), we find the equation

$$I = I_c\cos\left(\pi\frac{\Phi}{\Phi_o}\right)\sin(\varphi), \tag{1.3.3}$$

that shows the dependence of the SQUID current I to the flux Φ across the loop and the phase difference φ. I_c is the effective critical current given by $I_c = I_{c1} = I_{c2}$, and φ is the effective phase difference $(\varphi_1 + \varphi_2)/2$. Such a relation is a key for a wide range of applications of *dc SQUID* as will be explained later.

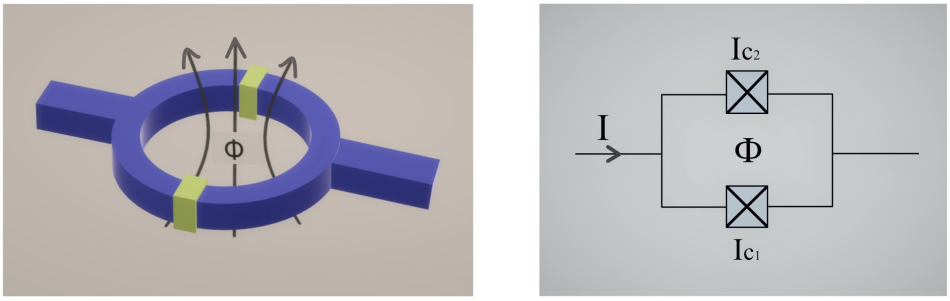


Figure 1.2: (a) *dc-SQUID* where two junctions are connected in parallel with flux Φ through the loop (b) *dc-SQUID* symbol

1.4 Non-linear inductance

The tunnelling of Cooper pairs through the JJ barrier leads to the accumulation of energy, which is known as *Josephson Energy*. This indicates that the junction works as an inductor. In order to derive the equation for the inductance of a *dc SQUID*, we use (1.3.1) to find the time derivative of the current

$$\frac{dI}{dt} = I_c \, \cos\left(\pi \frac{\Phi}{\Phi_o}\right) \, \cos(\varphi) \, \frac{d\varphi}{dt}. \tag{1.4.1}$$

Using this equation along with Eq. (1.2.2), and recalling that $V = L(dI/dt)$, we can derive an equation for the inductance of the *dc SQUID*

$$L_s = \frac{\Phi_o}{I_c \, |\cos(\pi\Phi/\Phi_o)| \, \cos(\varphi)}. \tag{1.4.2}$$

Eq. (1.4.2) indicates that the inductance of JJs is non-linear due to the dependence on the applied flux Φ and the phase difference φ, i.e. the applied bias. In absence of these two, the inductance of the *dc SQUID* is $L_s^0 = \hbar/(2eI_c)$.

Knowing that the energy of an inductor is $E = \int_{-\infty}^{t'} dt I(t')V(t')$, and using Eq. (1.2.2) and (1.3.1), we arrive at an equation for the *Josephson Energy* stored in the *dc SQUID*

$$E_{Js} = I_c \, \frac{\Phi_o}{2\pi} \, \cos(\pi \frac{\Phi}{\Phi_o}) \, [1 - \cos(\varphi)]. \tag{1.4.3}$$

Non-linearity of the SQUID inductance and its sensitivity to the applied magnetic field allows one to use SQUIDs in various applications in biotechnology, quantum computing and superconducting electronic circuits. In this section, we explain two commonly used applications of the *dc SQUID*, namely, the superconducting qubit (transmon qubit) and parametric amplifiers.

1.4.1 Superconducting qubit

For a quantum bit (qubit) system, it is crucial to have two well defined energy levels with a unique energy separation for each qubit. This is easily achievable in atomic qubits and quantum dots. However, atomic qubits interact weakly with the environment and therefore, they are hard to control; while quantum dots suffer from short decoherence time. As an alternative to those microscopic qubits, JJ-based qubits were proposed, forming what is known as *artificial atoms*, allowing for the fabrication of qubits on the macroscopic level [4]. Due to the non-linear inductance

of JJs, these qubits show two well defined energy levels representing the ground and the excited state, and they are well separated from higher energy levels. A variety of superconducting circuits were proposed aiming at reaching better coherence and higher quality factors.

The first demonstration was based on Single Cooper pair Box (SCB), which is the ancestor of all superconducting qubits [4]. Fig. 1.3 (a) (excluding the shunt capacitors parallel to JJs) shows an example of the SCB with a *dc SQUID*, which enables the tuning of the E_J of the qubit [5]. When solving the Hamiltonian of such a circuit, we find that the energy levels of this SCB is mainly characterized by E_J/E_C and N_g, where E_C is the charging energy which is inversely proportional to the total capacitance of the box, and N_g is the reduced gate charge given by $N_g = C_g V_g/2e$. This leads to two limiting cases of $E_J/E_C \ll 1$ and $E_J/E_C \gg 1$, representing charge and phase qubit, respectively (Fig. 1.3 (b)). Taking a cross section at a value of $E_J E_c \ll 1$ (=0.1) (Fig. 1.3 (c)), we find that the most optimum point to operate at is $N_g = 0.5$; however, this system suffers from short coherence time due to charge noise at this *sweet spot* [6], which leads to fluctuations in the difference between the two energy levels.

Later, a charge-insensitive qubit design was proposed by *Koch et al.* as a solution for the charge noise, which is also referred to as the *transmon* qubit [7]. In the transmon regime, the ratio E_J/E_C is significantly higher, $(20 - 50)$, which suppresses the effect of the noise at the operating point. This could be achieved by shunting each of the JJs with a large capacitor (C_J in Fig. 1.3 (a)). (Fig. 1.3 (d)) shows a cross section of the 3D map where $E_J/E_c \gg 1$ (=20). E_J, hence the frequency of the qubit, is minimally affected in response to the gate charge fluctuation compared to the previous system that did not include the shunt capacitors, and this is a significant improvement of the charge dispersion relation. At Chalmers, we focus on the transmon qubit, and a lot of investigation is done in order to improve the coherence time and the quality factors of the qubit system [8].

In these superconducting qubits, it is critical to have well-defined E_J and E_C. Each qubit is defined by its frequency ω, which is given by $E_{01}/\hbar$, where E_{01} is the energy difference between the two lowest energy levels. In a *transmon* qubit, for example,

$$E_{01} \approx \sqrt{8E_J E_C} - E_C, \tag{1.4.4}$$

$$v_p = \sqrt{8E_J E_C}/h, \tag{1.4.5}$$

where v_p is the plasma frequency of the qubit, and $E_{01} \approx hv - E_C$. This shows that uncertainties in the value of E_J and E_C lead to an indeterministic qubit frequency. In a multiple qubit system this results in severe difficulties in addressing the qubit during the control and readout process.

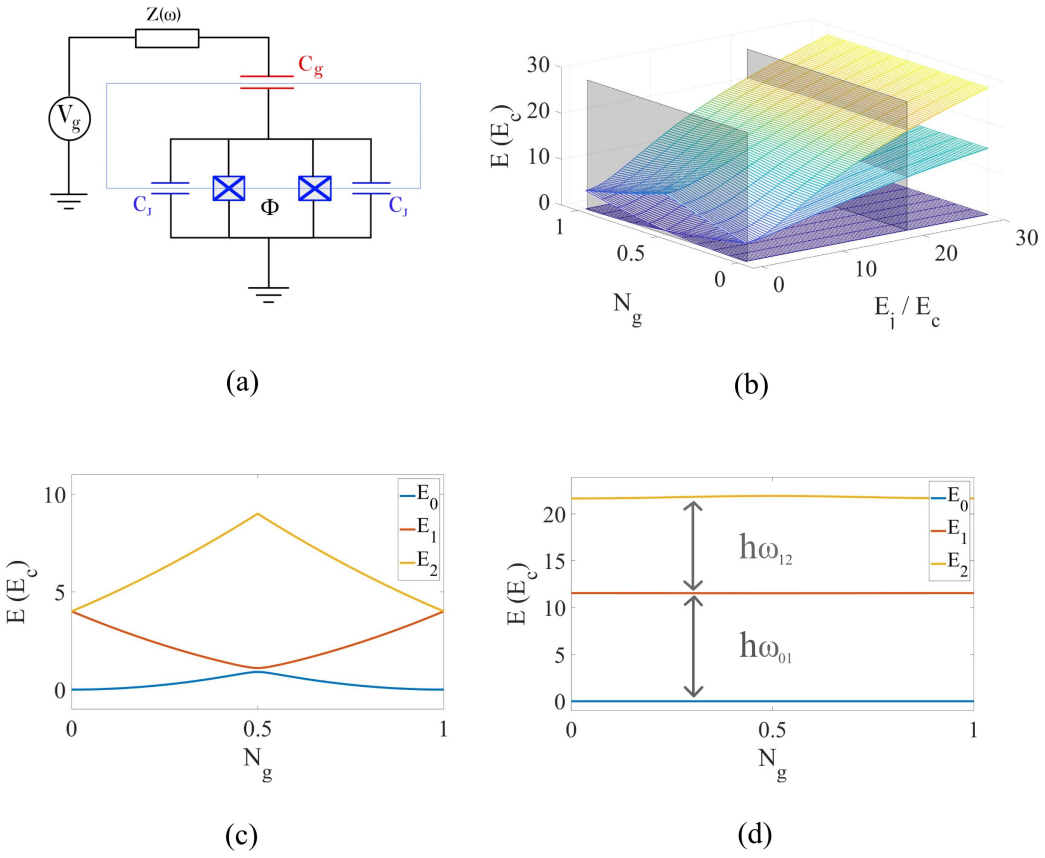


Figure 1.3: (a) A circuit schematic for *SCB* charge qubit (excluding the shunt capacitors) or a *transmon* qubit (including the shunt capacitors), (b) a 3D map of the lowest three energy levels as a function of E_J/E_C and N_g, (c) and (d) two cross sections for the lowest 3 energy levels at $E_J/E_c = 0.1$ and $E_J/E_c = 20$, respectively.

1.4.2 Superconducting parametric circuits

Josephson junctions are also used in superconducting parametric circuits, providing the non-linear element in e.g. parametric amplifiers and oscillators [11–17]. In superconducting quantum processors, low noise signal read-out is essential, and this is where the narrow band Josephson Parametric Amplifiers (JPA) and the wide band Traveling Wave Parametric Amplifiers (TWPA) play an important role [18–24]. Depending on the type, parametric amplifiers use one or an array of Josephson junctions, where the nonlinearity of the Josephson inductance is used for frequency

mixing, and the energy transfer from a powerful pump into the signal. Compared with normal JPAs, TWPAs are more attractive for qubit readout due to their wide bandwidth [22–24].

Figure 1.4 shows an example circuit for the TWPA, where a chain of Josephson junctions and capacitors are used to form a transmission line. When implementing such TWPA, two important criteria must be met. Firstly, the implemented Josephson junctions must agree with the design requirements to match the capacitors and form a 50 Ω transmission line. Secondly, since normally in the design all of the capacitors have the same value, the fabricated Josephson junctions must be identical to each other. If these requirements are not satisfied, the energy will be lost due to impedance mismatch. This example again emphasizes the importance of having a robust fabrication process.

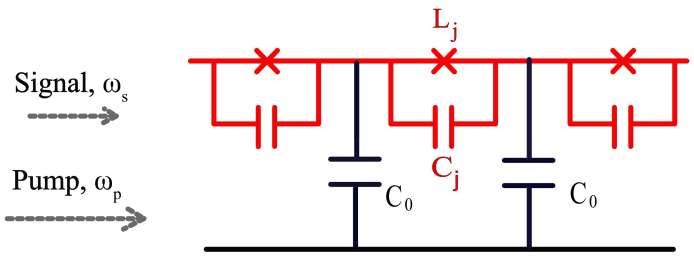


Figure 1.4: TWPA circuit using an array of JJs, shunted by capacitors C_0 to the ground. The Josephson inductance and the capacitance must be selected such that the characteristic impedance is 50 Ω

1.5 Characterization of the fabrication process

So far we have discussed the role that JJs play in a qubit and in a parametric amplifier, and the important parameters of the junction, namely E_J and L_J. From Eq. (1.4.2) and Eq. (1.4.3) , we can see that both parameters depend on the critical current I_C of the junction. In this section, I explain how the resistance of the junction is an indicative of the critical current, and what the sources of variation in resistance are.

1.5.1 Ambegaokar-Baratoff relation

One year after the discovery of the Josephson effect, Ambegaokar and Baratoff used the thermodynamic Green's function and perturbation theory to arrive at the Josephson relation [25]. Using this method, the maximum zero-voltage current, or the critical current of the junction is given by the relation

$$I_c = \frac{V_{AB}}{R_N}, \tag{1.5.1}$$

where $G_N = 1/R_N$ is the normal state conductance of the junction when the applied voltage $V \gg 2\Delta/e$, and

$$V_{AB} = \frac{\pi\Delta(T)}{2e}\ \tanh\left(\frac{\Delta(T)}{2k_BT}\right), \tag{1.5.2}$$

is the temperature dependent Ambegaokar and Baratoff potential, where k_B is Boltzman constant and Δ is the superconducting gap ($\approx 180\ \mu$eV for aluminum). This is implies that I_cR_N is a constant at a given temperature, and both values depend on the transparency of the barrier.

At a low enough temperature V_{AB} can be approximated to $V_{AB} = \frac{\pi\Delta(T)}{2e}$ since $\Delta \gg 2K_BT$. By substituting in Eq. (1.5.1), and subsequently in Eq. (1.4.3), (1.4.5) and Eq. (1.4.2), the critical current is given by,

$$I_c = \frac{\pi\Delta}{2eR_N}, \tag{1.5.3}$$

while the Josephson energy and the plasma frequency of the qubit are given by

$$E_J = \frac{\Delta\Phi_o}{4eR_N}, \tag{1.5.4}$$

and

$$v_p = \frac{\sqrt{8E_JE_C}}{h}, \tag{1.5.5}$$

and finally, the junction inductance is

$$L_s = \frac{\Phi_oR_N}{2\pi\Delta}. \tag{1.5.6}$$

Eqs. (1.5.4) and (1.5.6) relate both the Josephson energy and the Josephson inductance to the normal resistance of the junction. As a result, one can obtain statistical information and predict E_J and L_J at low temperature by measuring the

resistance at room temperature, which is explained in section 4.2. One should consider that R_N in Eq. (1.5.1) is the resistance at low temperature $R_{N_{LT}}$. However, $R_{N_{LT}} = c.R_{N_{RT}}$, where c is a constant and $R_{N_{RT}}$ is the resistance at room temperature, which means that the statistical analysis for the resistance measurements does not differ between low and room temperature.

1.5.2 Sources of variation in R_N

Variation in R_N of a JJ, hence I_C, is mainly attributed to the uncertainties in the junction size A and the barrier thickness l. Assuming a uniform barrier thickness, the resistance per unit area for a tunnel barrier R_o is given by the relation

$$R_o = \rho \, e^{l/\lambda}, \tag{1.5.7}$$

assuming a constant l, where ρ is dependent on the work function of the tunnel barrier, and λ is the attenuation length inside the barrier [28]. However, variation in l has an exponential influence on R_o [29], which is expressed by

$$R_o = \rho \, e^{l_o/\lambda} \, e^{{\sigma_l}^2/2\lambda^2}, \tag{1.5.8}$$

where l_o is the mean thickness, and σ_l is the normalized standard deviation of the barrier thickness over a single junction. Since $R_N = R_o/A$, the normalized standard deviation of R_N, denoted by σ_{R_N}, between different junctions is given by

$$\sigma_{R_N}^2 = \sigma_{R_o}^2.\sigma_A^2 + \sigma_{R_o}^2 + \sigma_A^2, \tag{1.5.9}$$

where σ_{R_o} is the normalized standard deviation of the resistance per unit area, and σ_A is the normalized standard deviation of the junction area, assuming that $\sigma_{1/A} = \sigma_A$.

There are several factors that can cause variations in the barrier thickness, including oxidation pressure, oxidation time and uniformity of the bottom electrode [30]. On the other side, variations in the Junction size can be attributed to the non-uniformity in the pattern size over the wafer area during the lithography and development, variation of the resist thickness, and also junction fabrication techniques.

1.6 Thesis overview

The objective of this work is to investigate the reliability and reproducibility of the fabrication process of Josephson junctions, and propose steps for the optimization of this process. Based on this, in the remainder of this thesis, the following are presented:

- A summary of different techniques that are used to fabricate Josephson junctions, including the approach that is used in this work.
- Fabrication and room temperature resistance measurement of thousands of JJs and collecting statistical data to determine fabrication yield and junction reproducibility.
- Proposed optimization steps including:
  - Reduction of the ion milling time. A step that is used to remove the native aluminum oxide before making electrical connections.
  - One-step fabrication of JJs, which reduces the number of fabrication steps.
- Tentative experimental study of junction ageing.

Chapter 2

Background

2.1 Fabrication Methods of JJs

This section describes different techniques of fabricating Josephson junctions that are based on superconducting/insulating/superconducting trilayer. Such JJs are usually fabricated using aluminium (Al) or niobium (Nb) metals due to their relatively high critical temperatures (1.2K and 9.3K, respectively [31]), and the possibility of controllably growing an oxide layer. In this section, an overview of the fabrication methods of Nb-based and Al-based JJs is explained. Nb-based fabrication process is mentioned very briefly, since firstly, despite of niobium being widely used in superconducting circuits, qubits fabricated using niobium-based Josephson junctions showed significantly lower coherence time compared to Al-based qubits [34] [35]. Secondly, Al can be grown by evaporation methods which provides a great platform for fabricating JJs using the lift-off technique. Nb, on the other hand, is not ideal for evaporation due to its high melting point of 2,477 °C compared to that of Al, which has a melting point of 660.3 °C [31]. And finally, our fabrication process relies on $Al/AlO_x/Al$ tunnel junctions.

2.1.1 Al-based JJ

When fabricating JJs, one should note that the properties and performance of a JJ strongly depends on the size of the junction, as well as the thickness and the quality of the insulating layer. Considering that Al reacts with oxygen extremely quickly [32], it important to grow Al in chambers held at low vacuum pressure. For the same reason, and to have control over the growth of the junction, it is best to grow all three layers of the junction in such a way that the vacuum in between the growth steps is not broken. In this approach, after depositing the first Al layer, Oxygen (O_2) is let into the chamber under well-controlled flow and pressure for a

given time, to create the insulating layer. Afterwards the oxygen is pumped out from the chamber, and the second Al layer is deposited to complete the junction [1].

It is not impossible to fabricate the Al-based JJs by patterning and etching; however, they are normally fabricated using the liftoff method that is described in detail in appendix A.3. In short, the shape of the junction is first transfered into a resist using the lithography techniques, followed by evaporation of aluminum. The aluminum layer fills the patterned regions as well as the remaining resist layer. The excess Al is then removed by submerging the sample in a solution that dissolves the resist.

Since the goal is to grow all three layers of a Josephson junction in one chamber, the entire pattering must be done before loading the sample into the vacuum chamber. What is important is to engineer the patterning and evaporation steps such that one can access both electrodes (Al ends) of the JJ for electrical connection. Different techniques are developed to achieve this, which are described in the following subsections.

Dolan bridge

The first method is based on shadow evaporation with a suspended shadow mask (Dolan bridge) that was first proposed by Dolan in 1977 [36] [37] [38]. The schematic of this technique is shown in Fig. 2.1 (a), where the suspended metallic bridge is shown in dark blue above the PMGI layer [39]. To create the junction, first the bottom electrode is deposited at an angle θ_1, and then oxidized. The Second electrode is next deposited at another angle, θ_2. The combination of the bridge with angled evaporation protects some areas of the substrate from the evaporated aluminum. At the end of the two evaporation steps, a region is formed, where the two electrodes overlap, sandwiching the dielectric layer and thus creating the junction. The junction size is determined by the θ_1, θ_2, bridge height h and the exposed region a for a given bridge width.

The Dolan bridge beautifully manages to create the Josephson junction, using only one lithography run. It also provides access to each junction electrode, as shown in the figure. However, using this technique can lead to some challenges that arise from the method being dependent on both the deposition angle, and the resist thickness. Variation in the resist thickness h, even the less likely variation in the deposition angles θ_1 and θ_2 from run to run, can change the junction size. This results in indeterministic JJs, making the process not quite reliable and robustly reproducible. In addition, the mechanical and thermal stability of the suspended

[1] An alternative method is to remove the native oxide off the first Al layer, and then regrow the insulating layer in a controlled way, followed by the second Al film [33].

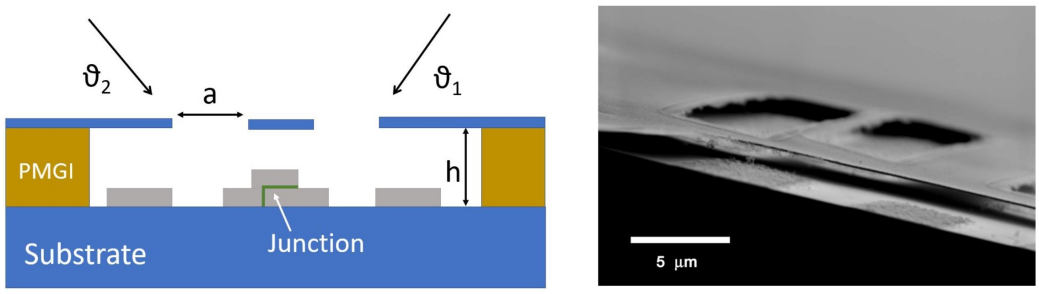


Figure 2.1: JJ fabrication using shadow mask and angled evaporation (Dolan bridge). (a) schematic of the fabrication process and (b) SEM image of the suspended bridge [39].

bridge can be problematic when fabricating wide junctions, where the long sagging bridge cannot provide the necessary shadow. Finally, the Dolan bridge creates unwanted replicas of patterned areas and metallic islands that can act as sources of charge and disrupt the normal operation of circuits.

Bridge-free technique (BFT)

A second technique that also uses shadow evaporation was proposed as a solution for the mechanical instability of the suspended bridge [40]. In this method, the suspended bridge is avoided by creating asymmetric undercuts in a bilayer resist. To create these undercuts, features are written by electron beam lithography using two different doses (Fig. 2.2 (a)), where the lower exposure dose can only cure the lower resist layer (PMMA/MMA in Fig. 2.2 (b)). This allows for creating customized asymmetric or symmetric undercut layers. The junctions metal is deposited in an angle, $\pm 45^\circ$ for example, and depending on the undercut shape, the metal is deposited either on the substrate, where it stays and becomes part of the circuit, or on the resist wall, where is will be washed away during lift off.

In order to realize a junction with accessible electrodes, the resist is patterned such that it has a wide section with symmetric undercuts at the center (the junction), and a section with asymmetric undercutting on the two sides that form the electrode wires (Fig. 2.3). During the first evaporation, the bottom plate of the junction and the upper connecting wire are deposited, as shown in Fig. 2.3 (c), while on the lower side, the deposition is on the resist wall. Similarly, during the second evaporation, the top plate of the junction is deposited along with the lower wire (Fig. 2.3 (e)). As a result, the junction is fabricated as shown in Fig. 2.3 (d),

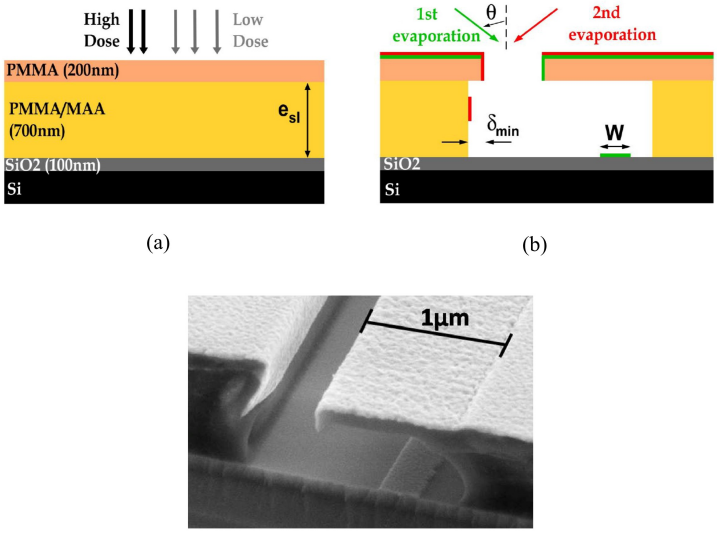


Figure 2.2: JJ fabrication using bridge-free technique (BFT). (a)High and low dose exposure using electron beam lithography, (b) asymmetric undercut with angled deposition on the substrate and the side walls, and (c) SEM image before lift-off [40].

and the SEM pictures in Fig. 2.3 (a) and (b).

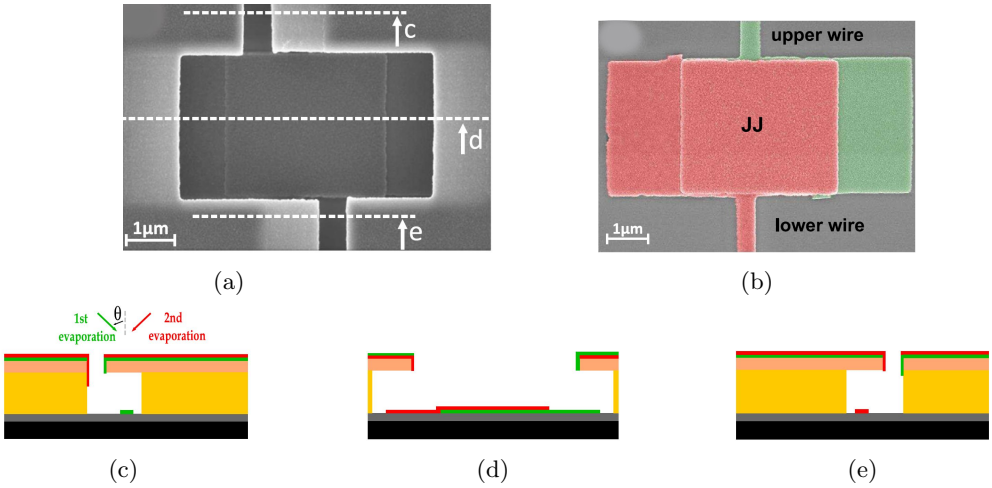


Figure 2.3: (a)-(b) SEM pictures of a Josephson junction fabricated using the BFT method, before and after lift-off, respectively. (c), (d) and (e) show schematic of the upper wire, a cross section of the junction and the lower wire, respectively [40].

The BFT technique addresses the problems that are related to the instability of the bridge. It is also very flexible in terms of the junction size, not imposing any limit of the junction area. However, the need for two exposures can double the lithography time. Additionally, the resist thickness and evaporation angles are still critical parameters, whose variations lead to variation in the junction size.

Cross-type Technique

The third technique of Al-based JJ fabrication, which we adopt in our fabrication, was again proposed to overcome the aforementioned challenges in the Dolan bridge method. This method is also bridge free, which uses a cross shaped pattern to fabricate the JJ at the center of the cross. To fabricate a JJ, one ensures that Al is deposited on only one of the intersecting trenches of the cross during each evaporation run. This is achieved by tuning the orientation of the pattern, combined with shadow evaporation [39]. As shown in Fig. 2.4, during each angled deposition, the pattern is aligned such that the plane normal to the desired trench is parallel to the evaporation direction. This strategy guaranties that the trench will receive the evaporating metal, if it is longer than $s/\tan(\theta)$, where s and θ are the resist thickness and the evaporation angle, respectively. Since the other trench is orthogonal to the first one, it will not receive any metal deposition if the trench width is narrower than $s/\tan(\theta)$. In order to create the junction, after oxidation and before the second deposition, the pattern is rotated by 90° such that the second trench can receive the evaporating metal. The trenches intersect at the center of the cross, and hence that is where the junction is created.

The cross fabrication method manages to overcome the shortcomings of the Dolan bridge with regard to the dependency of the junction size to the resist thickness and evaporation angle. The accuracy of the JJ size is mainly controlled by lithography, not by the height of the resist. Furthermore, the challenge of the thermal and mechanical stability of the suspended bridge is avoided.

Although adjusting the evaporation angle can help one to fabricate junctions that are wider than the resist thickness, it is better to use the BFT method (that was discussed previously) to fabricate junctions with large areas in the order of μm^2. Aside from the size, the main challenge of this technique is the possibility of depositing Al on the side walls of the resist, which may lead to a bad lift off with pieces of loosely connected metal. As a solution, it was proposed to have a trilayer of resist instead of a single layer in order to achieve an undercut profile that prevents the deposition on the side wall [39]. In our fabrication, however, we use a bilayer resist to avoid this problem (Appendix A.3).

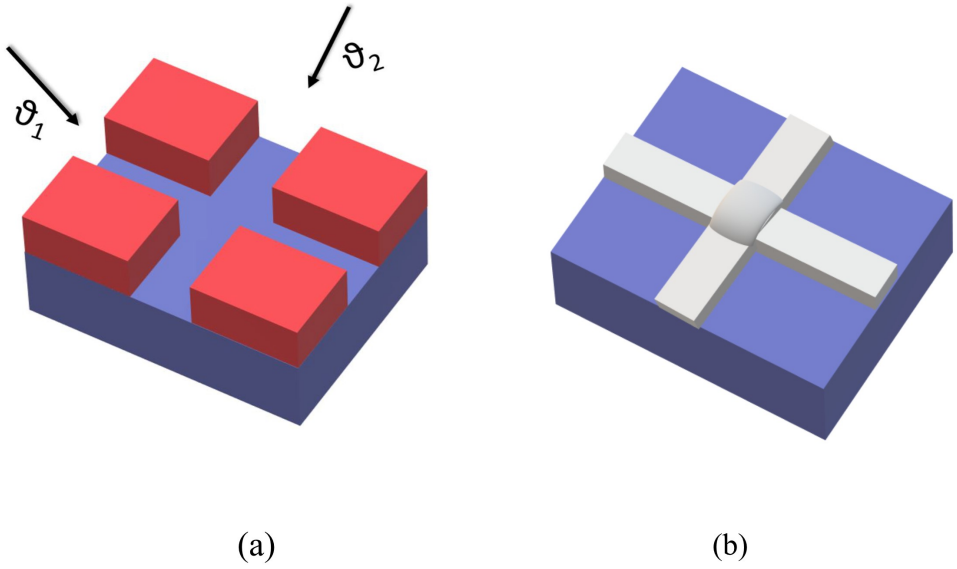


Figure 2.4: JJ cross-type fabrication using cross-type shadow evaporation. (a) after patterning and before the two evaporations with angles θ_1 and θ_2 , (b) after Al deposition and lift-off

2.1.2 Nb-based JJs

Although there are some special techniques to evaporate Nb [41, 42], fabrication of Nb-based JJs is mainly based on sputtering, then etching in order to have separate contacts to each electrode. One of the early common techniques, initially proposed in 1983 [43] and later modified by [44–46], relies on a trilayer of $Nb/AlO_x/Nb$. Fig. 2.5 shows an example of Nb-based JJs fabrication process after depositing the trilayer of $Nb/AlO_x/Nb$ [47], where

- The bottom electrode is firstly patterned with a positive resist then etched using reactive-ion etching (RIE) in a CF_4-O_2-gas.
- Ion-beam etching (IBE) is used to etch the oxide barrier.
- Another lithography step is needed in order to define the dimensions of the JJ
- Top electrode is etched using RIE
- SiO_2 is deposited to form an insulation layer from the top wiring

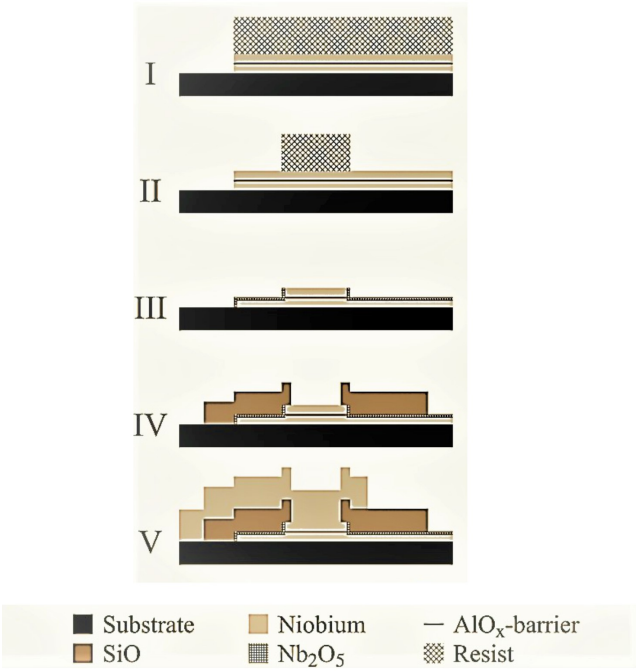


Figure 2.5: Schematic of an example fabrication process for Nb-based JJs [47].

2.2 Resistance measurement

Typical resistance measurement techniques rely on passing current through a wire across the resistance (JJ in our case), and measure the voltage drop across the same wire. However, this technique lacks accuracy as it cannot exclude the residual resistances that arise form the measurement wires and contacts. As an alternative, 4-point probe measurement solves this problem by placing the voltmeter outside the circuit that current is passing through (Fig. 2.6) [48]. In this case, the potential drop along the resistive wires is not measured, which results in a more accurate resistance measurement. This is especially important for resistances with small values compared to the parasitic resistances.

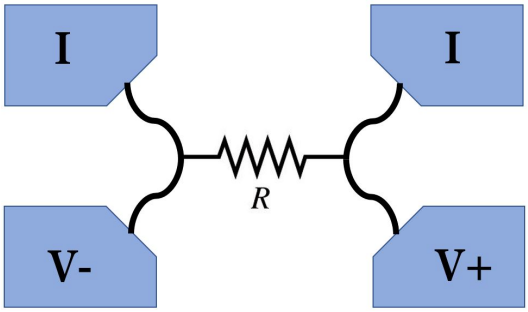


Figure 2.6: 4-point measurement. The current is passed between the two top pads, while the voltage is measured using the two bottom pads.

Chapter 3

Experiment

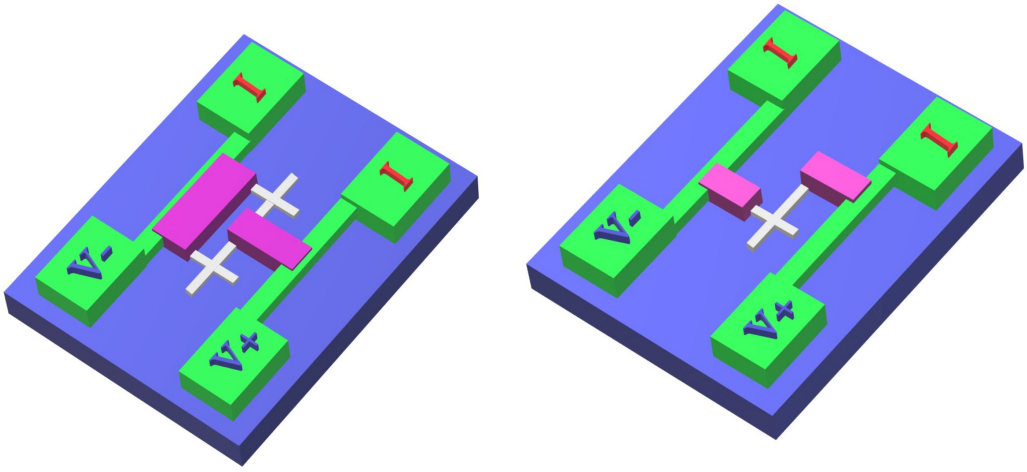
3.1 Design of JJ Test Device

In order to prepare JJs for resistance measurements, a test structure has to be fabricated such that it allows for proper electrical connection to the junctions. Since the dimensions of the junctions are very small (order of 100s of nm) compared to the tip of the probe needles (of the measurement tool, order of 10 μm), one needs to fabricate some metallic pads that are in contact with the junction electrodes. Fig. 3.1 shows the 3D schematic of a test device, where the green, grey and purple layers represent the contact pads, JJs, and the patches, respectively deposited on a substrate (blue layer). Fig. 3.1 (a) shows the layout of a *dc-SQUID* test device, while Fig. 3.1 (b) shows the layout of a single JJ test device, whose corresponding circuits are shown in Fig. 1.1 (b) and 1.2 (b), respectively.

As mentioned in section 2.1.1, in our fabrication process, we use the cross-type technique for JJs. Following are the general steps for fabricating such a test device.

1. Contact Pads
2. Josephson Junctions
3. Patches

Please note that the patches in the third step are needed in order to obtain an ohmic contact between the junctions and the contact pads. The reason for using a patch layer, and not directly depositing JJs on top of the contact pads is that the oxidation of the bottom electrode also leads to the oxidation of the contact pads, hence, a parasitic JJ between the top electrode and the contact pad would exist. This is explained in more details in the following section.



(a) (b)

Figure 3.1: 3D structure of test devices showing JJs (grey), contact pads (green) and patches (purple), where (a) is a test device for a SQUID and (b) for a single JJ.

3.2 Fabrication process

In this section, I explain our design layout, the fabrication process steps, and the characterization method of the fabricated devices. This section is dedicated for the standard fabrication process followed in Chalmers QT for JJ circuits. Next, other designs and fabrication steps are followed as part of the optimization process.

3.2.1 CAD Layout

The three different colors in Fig. 3.2 represent the three layers of the test device; and each layer would be fabricated in a separate lithography and metalization step. The green, purple and dark grey represent the contact pads, the patch layer, and the JJ, respectively.

The layout was designed using L-EDIT software toolbox [49], and part of the design was scripted using C language in order to optimize the layout design process by integrating variable parameters into the design. The layout was designed for a 2-inch wafer (Fig. 3.2 (a)) and it includes 10 identical chips, where the layout of the chip is shown in Fig. 3.2 (b). The dimensions of each chip is 10 mm by 10 mm, with each including $\sim$ 374 test device shown in Fig. 3.2 (c), (d) and (e). A

DUT can be either a JJ or a SQUID, as shown in Fig. 3.2 (d). Each junction is a square with side d, where d take values of 100, 150, 200, 250, 300, 400, 500, 600, 700, 800 nm, distributed over each chip. The two junctions are identical in a SQUID.

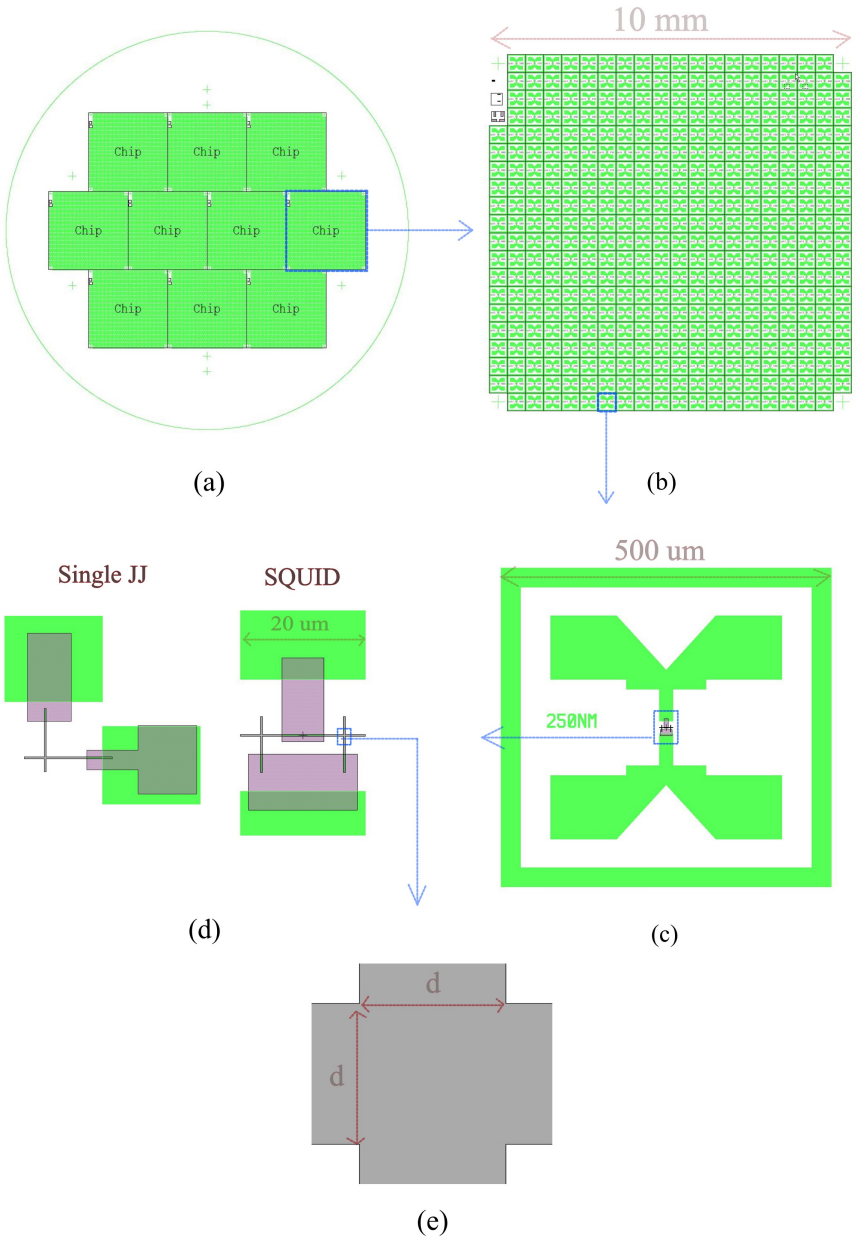


Figure 3.2: (a) wafer, (b) chip, (c) DUT, (d) SQUID and JJ layout and (e) junction layouts for the standard fabrication process

3.2.2 Fabrication Steps

There are three main sequential fabrication steps; contact pads, JJ and patch layer. The process flow shown in Fig. 3.3 explains the general steps for fabrication of each of these layers; however, the layers vary in the way they are implemented, as will be explained.

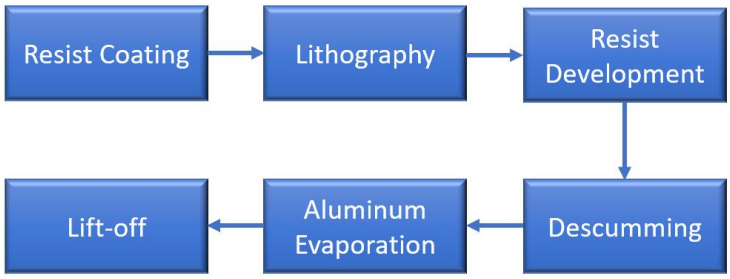


Figure 3.3: Fabrication process flow

Refer to appendix A for more details about the equipment and recipes used for each of these process steps.

Layer 1: Contact Pads

The contact pads (green layer in Fig. 3.2) are patterned by mask-less optical lithography using *DWL 2000* from Heidelberg Instruments [50]. Due to the micrometer feature size, the pads can be fabricated with optical lithography, and it is unnecessary and time consuming to pattern them using electron-beam lithography (EBL). The dimensions of each pad is within $100 \times 100um$, which makes it convenient for the touch down of the probe tips. After patterning, development and descumming, 160 nm of aluminum is deposited using the *Plassys* electron beam evaporator [51], with a subsequent *in situ* oxidation at 10 mbar for 10 minutes for Al surface protection. Fig. 3.4 shows a micrograph of the contact pads after the lift-off process.

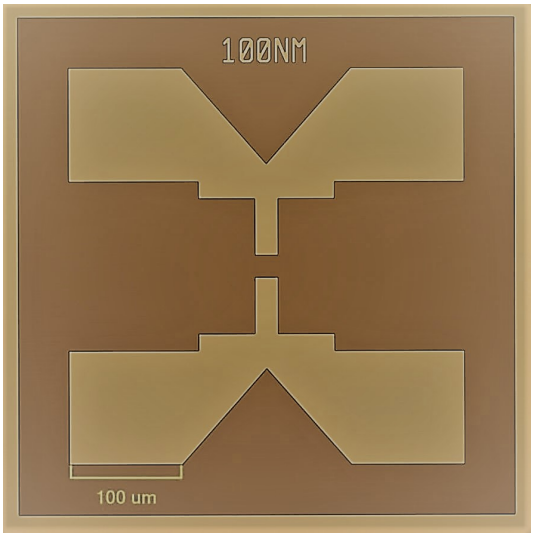


Figure 3.4: Micrograph of the contact pads after aluminum evaporation and lift-off

Layer 2: JJ

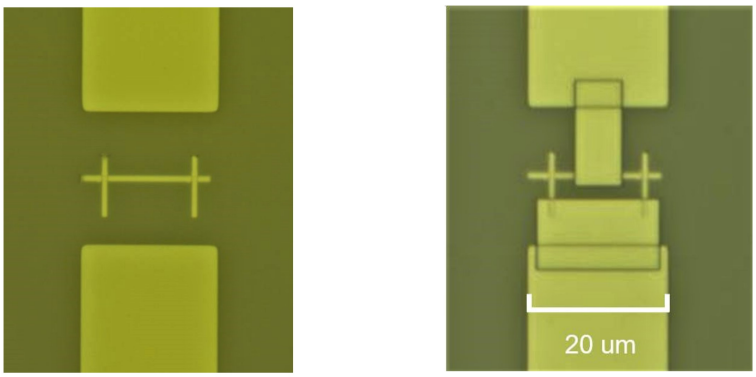
In order to fabricate the JJs (dark grey layer in Fig. 3.2), patterning is done using EBL due to the small feature sizes (100-800 nm). The junctions metal evaporation is carried out in *Plassys*, where firstly the horizontal part (Fig. 3.2, bottom electrode) of the junction is deposited from right to left with Al thickness of 50 nm at 45° tilt. Then *in situ* oxidation takes place at 0.1 mbar for 6 minutes to form the oxide barrier. The wafer is then rotated 90° keeping the 45° tilt in order to deposit the vertical part (top electrode). The Al is thicker than the first layer (110 nm), in order to ensure step coverage. Lastly, the film surface is oxidized at 10 mbar for 10 minutes for surface protection. Fig. 3.5 (a) shows a micrograph of some of the fabricated JJs after the lift-off process.

Layer 3: Patch Layer

The patch layer in our design is used to provide electrical connection between the JJ ends and the contact pads. Here the goal is to remove the surface oxide layer on the aluminum pads and the electrodes, by means of ion milling, and then deposit an aluminum blanket for connecting the pieces. The milling step is necessary in order to avoid the fabrication of parasitic junctions. Although the patch layer (purple layer in Fig. 3.2) has a relatively large minimum feature size ($\sim 5 \times 15um$), it is

patterned by EBL. The reason is that high power Ar-milling heats the substrate to a temperature that is higher than the glass transition temperature of a typical photo-resist such as Shipley 1805. An electron beam resist like PMMA can withstand a higher temperature and hence, EBL is used to pattern the patches.

After patterning and development of the substrate, the wafer is loaded into *Plassys*, and milled at 400 V and 20 mA. Next 200 nm of Al is depositied and finally oxidized at 10 mbar for 10 minutes. Fig. 3.5 (b) shows a micrograph of the device with the patches connecting the JJs to the contact pads, forming a SQUID.



(a) (b)

Figure 3.5: Micrograph of (a) JJs without the patch layer and (b) the full DUT with the patch layer

3.3 Steps towards optimization of the Fabrication Process

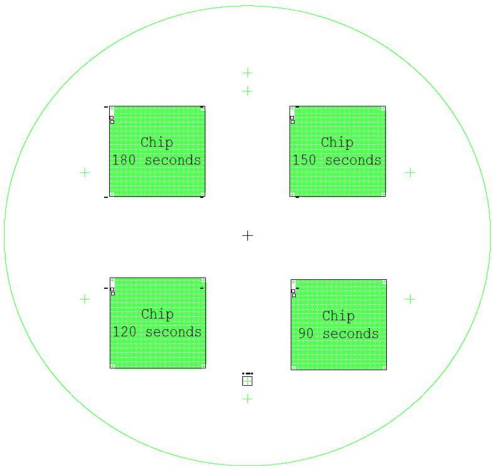
In this section, I explain two modifications in the standard process described in subsection 3.2.2. These steps were explored in order to find ways to improve the junction quality, and simplify the fabrication. While the statistical data for the junctions that are made using these modifications is presented and analyzed in the next chapter, further low temperature measurements are required to investigate the junctions behavior and this is out of the scope of this work.

3.3.1 Milling Time

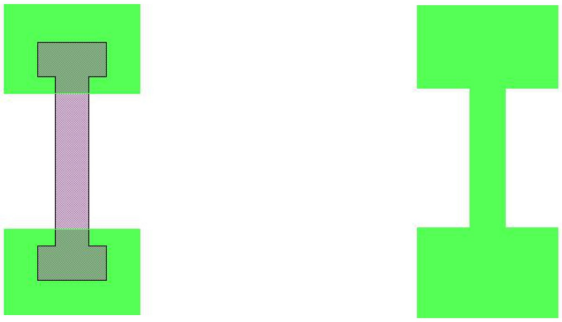
Milling parameters are critical for the fabrication of JJs and integrating them with the rest of the circuit. Since the main reason for milling is to remove the oxide layer and obtain an ohmic contact between two metallic layers, it is important for it to be strong enough. However, exposing the substrate to aggressive Argon ions ($Ar+$) has been proven to cause further decoherence for superconducting qubits due to amorphization of the substrate and the added losses at the substrate-metal and substrate-vacuum interface [52] [53]. As a result, two-level systems (TLS) are enhanced, which is a main source of decoherence [54, 55].

There are different milling parameters that can be controlled such as, voltage, current, distance between ion gun source and substrate, angle of milling and milling duration. In our experiment, we investigate the milling duration, and the objective is to obtain the minimum milling time that could maintain an ohmic contact between the patch layer and both the contact pads and JJ electrodes.

Different milling durations were experimented on a single wafer. The layout of the wafer is shown in Fig. 3.6 (a), where four chips are fabricated and each is dedicated for a specific milling time. To simplify the experiment and to purely study the effect of milling, we did not fabricate any JJ on the chips. The patches instead connect two pads of a test device to provide a resistive contact. A bad patch (short milling time) does not remove the oxide properly, resulting in an increase in the resistance. A representative structure is shown in Fig. 3.6 (b). Different sizes of the patch layer were designed on each chip; $1um$ line width with $2 \times 2um$ patch size, $2um$ line width with $2.5 \times 4um$ patch size and $5um$ line width with $5 \times 10um$ patch size. Reference devices where also fabricated without patching, by fabricating the whole device in one step with the contact pads (Fig. 3.6 (c)).



(a)



(b) (c)

Figure 3.6: Wafer design for milling duration experiment: (a) wafer, (b) test device and (c) reference device

Fabrication of the contact pads, and the patches (purple layer) follows the same steps mentioned in section 3.2.2. The only exception is that the milling time before depositing the patch layer is changed to 180, 150, 120 and 90 seconds for each of the four chips.

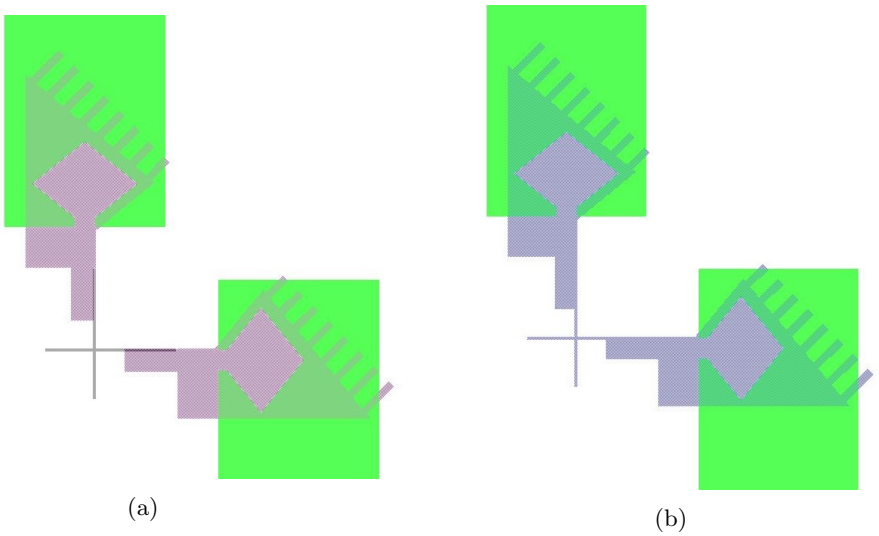
3.3.2 One Step Fabrication of JJ

As previously explained, fabricating JJs on a circuit is a two-step process: fabricating the junction, and a patch layer to connect it to the rest of the circuit. Each layer requires a separate lithography and deposition step. Here, the objective of optimization is to fabricate both layers in one step, in order to simplify the fabrication process by reducing the number of the required steps. In this experiment, we only

focus on the fabrication of single JJs instead of SQUIDs. To have a fair comparison between the junctions made by our new approach and those that were fabricated by the two step method, we tried to keep the new process flow very similar to what described earlier in section 3.2. The fabrication steps are summarized below:

1. Patterning the junctions and the patches in one electron beam lithography run
2. Deposition of the first electrode of the junction
3. Oxidation to form the oxide barrier
4. Deposition of the second electrode of the junction
5. Oxidation to protect the aluminum surface
6. Selectively milling the oxide on the contact pad and the corresponding end of the junction in order to locally remove the aluminum oxide.
7. Deposition of the patch layer
8. Final oxidation of the aluminum surface for protection

The main challenge here is the selective milling, hence, the design has to be tweaked in a way that satisfies this condition. Fig. 3.7 (a) shows the layout intended for the one-step process, where the purple and dark grey layers correspond to the patch layer and the JJ, respectively. Since we intend to deposit both layers in one step, Fig. 3.7 (b) shows the same design where the two layers are merged.



(a) (b)

Figure 3.7: CAD design for the one-step fabrication process

Following the aforementioned process steps and after finishing step 5, the contact pad area is covered with layers of Al, and its surface oxide from steps 2-5, except for the region where the fringes are. The shadow evaporation together with the shape of the fringes prevent this area from being buried underneath the junction Al layers, making part of the pads accessible for the subsequent milling. In this case, if milling is done at a 45° planar rotation angle, i.e parallel to the fringes, in addition to a tilt angle of 60° to avoid milling around the junction area, the surface Al oxide of the contact pad in the fringe area can be removed. Deposition of the patch Al layer can then be carried out at the same angle of the milling, also, in order to avoid deposition at the junction area (which can lead to a short circuit between the junction electrodes).

Some conditions must be met in order to successfully fabricate the patch layer.

- The diamond cut in the contact pad guarantees a good contact to the electrodes; otherwise, the contact pad would shadow the evaporation of the electrodes.
- The width of the fringes should be small enough to avoid deposition of Al in the fringe area, during evaporations in steps 2-5. This depends mainly on the thickness of the resist.
- The tilt angle during the milling and patch deposition depends on the junction width and resist thickness. Assuming the junction is a square with side d, the resist thickness is s and the planar rotation angle is 45°, the tilt angle θ, i.e the angle between the milling/deposition and the wafer plane, must meet the following condition:

$$\tan\theta < \frac{s}{d\sqrt{2}} \tag{3.3.1}$$

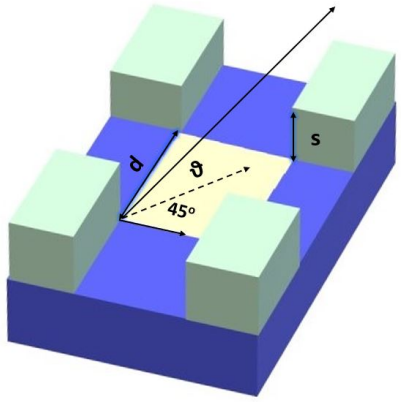


Figure 3.8: Milling and patch layer deposition angle for one-step fabrication process

Fig. 3.9 shows a scanning electron microscope (SEM) image of a one-step fabricated JJ. Such a fabrication technique has some advantages over the two-step process including:

- Less fabrication time by removing one lithography, deposition and lift-off step.
- Avoids exposing JJ to resist baking and coating, and lift-off during the fabrication of the patch layer.
- Avoids milling the substrate which is a main source of decoherence as mentioned in section 3.3.1.

However, we note that one-step fabrication has some challenges due to the more complex deposition/milling process, and the limit on the JJ size, which is mainly controlled by the resist thickness and the deposition/milling angle range that is provided by the machine (Eq. (3.3.1)).

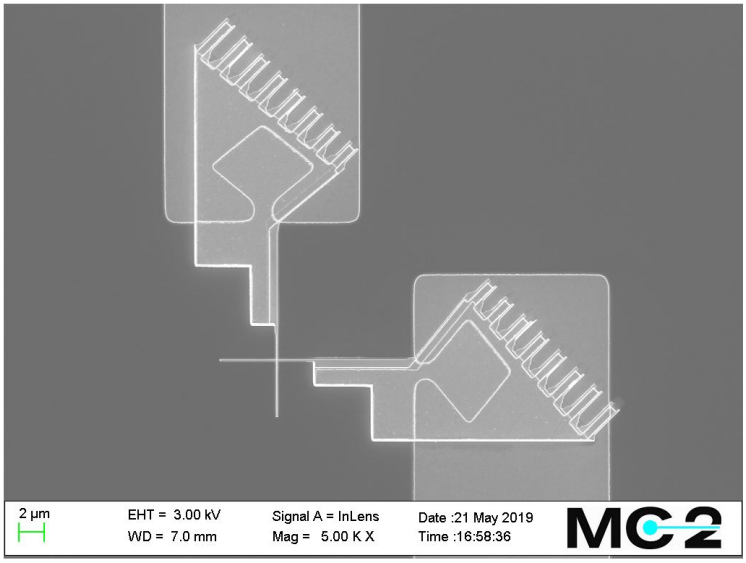


Figure 3.9: SEM image of the one-step-fabricated JJ

Chapter 4

Results

4.1 Standard fabrication process

In this section, the resistance measurements of DUTs fabricated using the standard process are shown and analyzed. 734 single JJ and 826 SQUID DUTs were measured using the automated probe station, *MBI TS2000* [56]. The yield of fabrication is 97.2%, where a DUT is considered successfully fabricated if its resistance lies within 3σ from the mean (σ is the standard deviation). Fig. 4.1 (a) and (b) show the mean resistance R, for different JJ sizes d, where the resistance of the SQUID (blue curve) is multiplied by 2 for comparison with single JJ (red curve). Only a small increase ($\sim 10s$ of ohms) was observed for the single JJs, which can be attributed to the resistance of the connecting electrodes (Fig. 3.2 (d)). The logarithmic scale plot in Fig. 4.1 (b) shows a linear relation between the resistance and the junction size, which is consistent with $R = R_o/d^2$. The resistance per unit area, R_o, for the fabricated junctions is $\sim$54 $\Omega/\mu m^2$.

Fig. 4.2 (a) through (j) show histograms of the junction resistances per junction size. The histograms fit properly into Gaussian distributions. The standard deviation as a percentage of the mean resistance (coefficient of variation) is shown in Fig. 4.2 (k). The standard deviation is highest for small junctions, e.g. $\sim$ 5% for 100 nm junctions, then decreases with bigger junctions. This is expected, and is attributed to the variation of junction size as a result of precision error in fabrication. Such variations become more negligible as the junction size gets larger. The increase of the standard deviation observed in the larger junctions (d $\geq$ 600 nm) is mainly caused by the measurement device, as well as the residual resistance of the contact pads that become comparable with the actual resistance of the junctions.

A mid-point exists on each curve showing a minimum standard deviation, e.g. 400 nm for the SQUID curve with $\sigma = 1.1\%$ and 600 nm on the single JJ curve with $\sigma = 0.8\%$.

The obtained results indicate that the fabrication process is reliable and reproducible to a very good extent. Additionally one can find the right junction size that corresponds to a required resistance by interpolating through the curve in Fig. 4.1 with an uncertainty that can be interpolated from the curve in Fig. 4.2 (k). More details about how one translates these results into useful data in terms of the qubit plasma frequency and Josephson inductance are mentioned in the following section.

We remark that for the results presented here, the junction oxidation parameters are kept fixed. For the same junction size, other resistance values can be obtained by changing the oxygen pressure and the oxidation time. Studying the test junctions that are fabricated under different oxidation conditions can be helpful in finding out if the oxidation step is a major cause of uncertainty in the junction resistance.

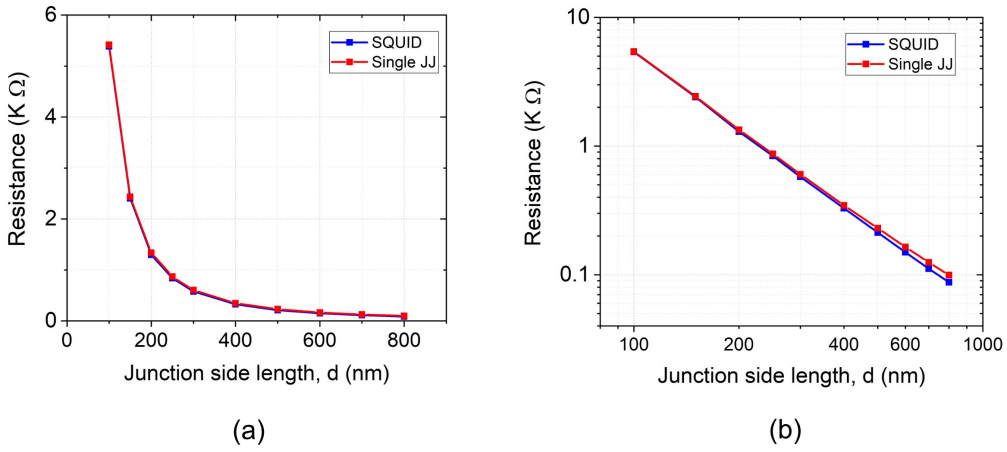


Figure 4.1: Mean resistance, R, for all DUTs as a function of side length d, on a (a) linear and (b) log scale

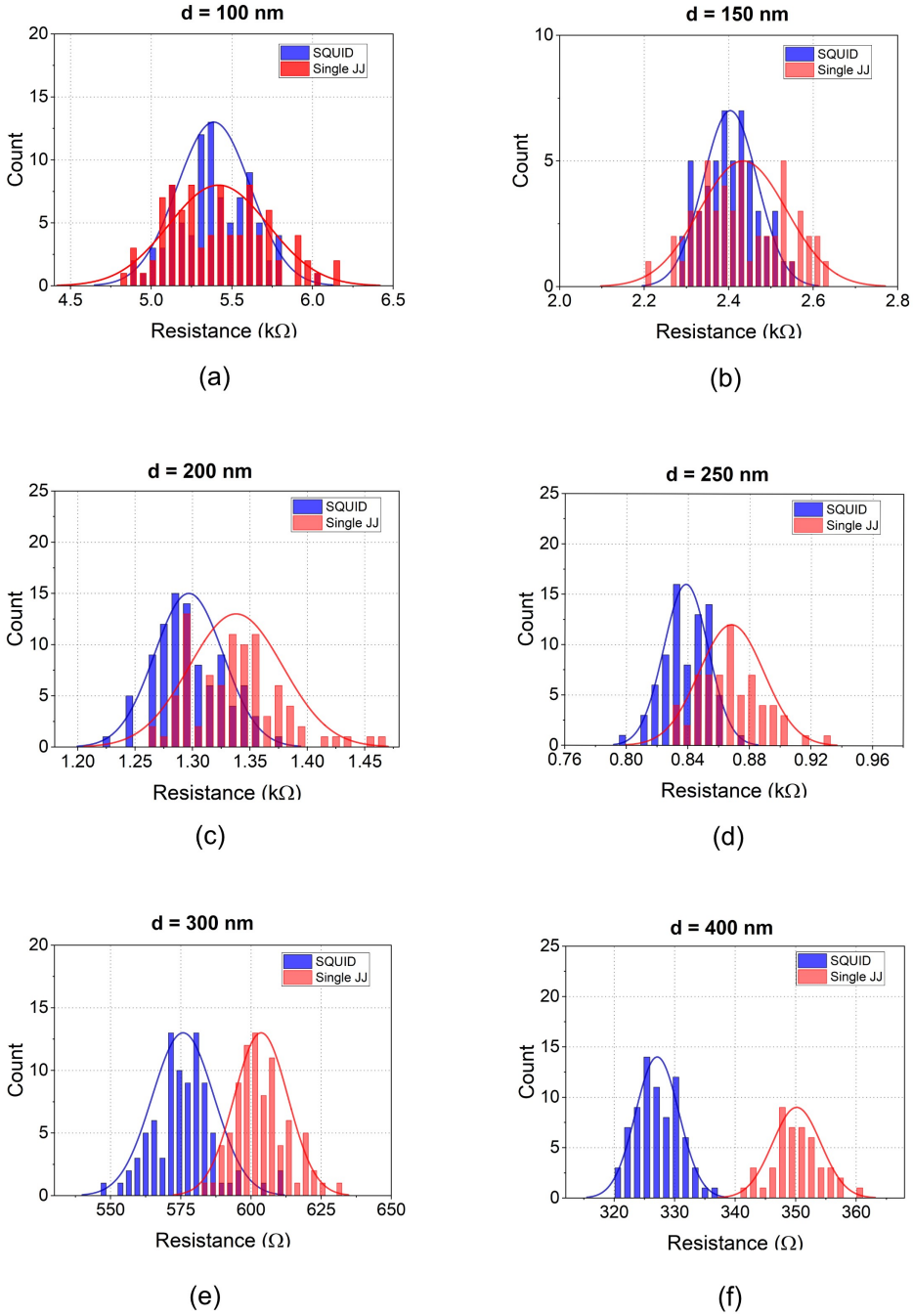


Figure 4.2: Histograms of 100 to 800 nm junctions fabricated using the standard process are shown in (a) through (j), and the standard deviation percentage for each size is shown in (k) -continued on next page-

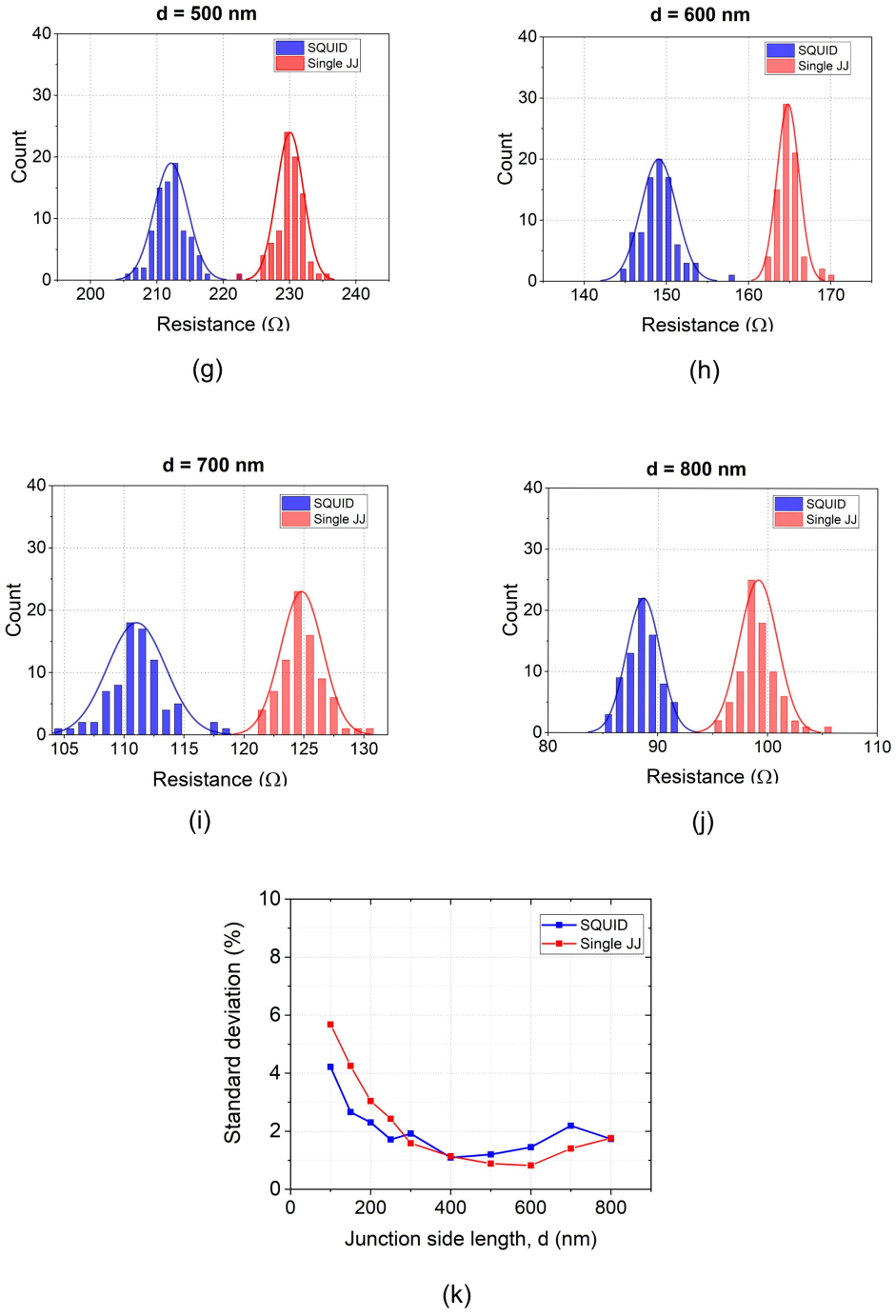


Figure 4.2: Histograms of 100 to 800 nm junctions fabricated using the standard process are shown in (a) through (j), and the standard deviation percentage for each size is shown in (k)

4.2 Predictability of the transmon plasma frequency and TWPA inductance

The objective of this section is to translate the obtained statistics and the variation in resistance values into a scheme that predicts the accuracy of the transmon plasma frequency, v_p, the Josephson energy, E_J, and inductance, L_J. From Eq. (1.5.4), using the Delta method, one deducts that the standard deviation

$$\frac{\delta E_J}{E_J} \approx \frac{\delta R_N}{R_N}, \tag{4.2.1}$$

In order to have a better understanding of what this equation implies, consider a 100 nm junction, that has a mean resistance of 5.4 kΩ in the single JJ devices (where the standard deviation is highest). Assuming $\Delta = 180$ μeV, this junction results in an $E_J/h \approx 26$ GHz, with uncertainty of 1.4 GHz. For v_p, however, the accuracy is higher. Following the analysis presented in [27] [1], and starting from Eq. (1.5.5), one can deduct that the standard deviation

$$\frac{\delta v_p}{v_p} = \frac{1}{2}\frac{\delta R_N}{R_N}, \tag{4.2.2}$$

which means that one can fabricate a qubit to have a well-defined plasma frequency with uncertainty percentage half that of the resistance and E_J/h. For example, considering a transmon that has an $E_c/h = 0.2$ GHz, the same 100 nm junction would have a plasma frequency of 6.24 GHz, with uncertainty of ~ 170 MHz.

For the inductance (Eq. (1.5.6)), the standard deviation is given by

$$\frac{\delta L_s}{L_s} = \frac{\delta R_N}{R_N}. \tag{4.2.3}$$

Following the same analogy with the 100 nm junction, L_J has a value of 6.3 nH, with uncertainty of 0.34 nH. And since the impedance of the junction, $Z = \sqrt{L_s/C_\Sigma}$, uncertainty of Z is also lower that of the resistance and L_J.

[1] Please note that in this analysis, it is assumed that $\delta\frac{R_N}{R_N} \gg \frac{\delta C_\Sigma}{C_\Sigma}$, and $\frac{\delta\Delta}{\Delta}$.

4.3 Milling time optimization

In this section, I explain the results of the milling test explained in section 3.3.1. Additionally, the reliability and reproducibility of the fabrication process after reducing the milling time are also presented.

4.3.1 Ohmic contact with shorter milling duration

As explained in section 3.3.1, we tried four milling durations of 90, 120, 150 and 180 seconds to patch the contact pads together. Then we measured the resistance in between the two pads to investigate (i) if the milling time was long enough to remove the native oxide, and (ii) if any of the milling times is statistically more reliable than the others.

The measurement results of different milling times are shown in Fig. 4.3 (a) - (d). Comparing the four figures indicates that regardless of the milling time, similar values for the resistors of the same size are obtained. This is also confirmed in Fig. 4.3 (e), where the average values are plotted (Refer to Appx. B for more statistics).

In addition, in Fig. 4.3 (e), when we compare the resistance of the 5 μm patched test structures with the control structures that are not patched at all (lines with green and blue markers in Fig. 4.3 (e); for schematics see Fig. 3.6 (b) and (c)), we find comparable resistances. We can therefore conclude that ohmic contacts are obtained for all four cases and in terms of providing an electrical contact, even the shortest milling time of 90 seconds is satisfactory.

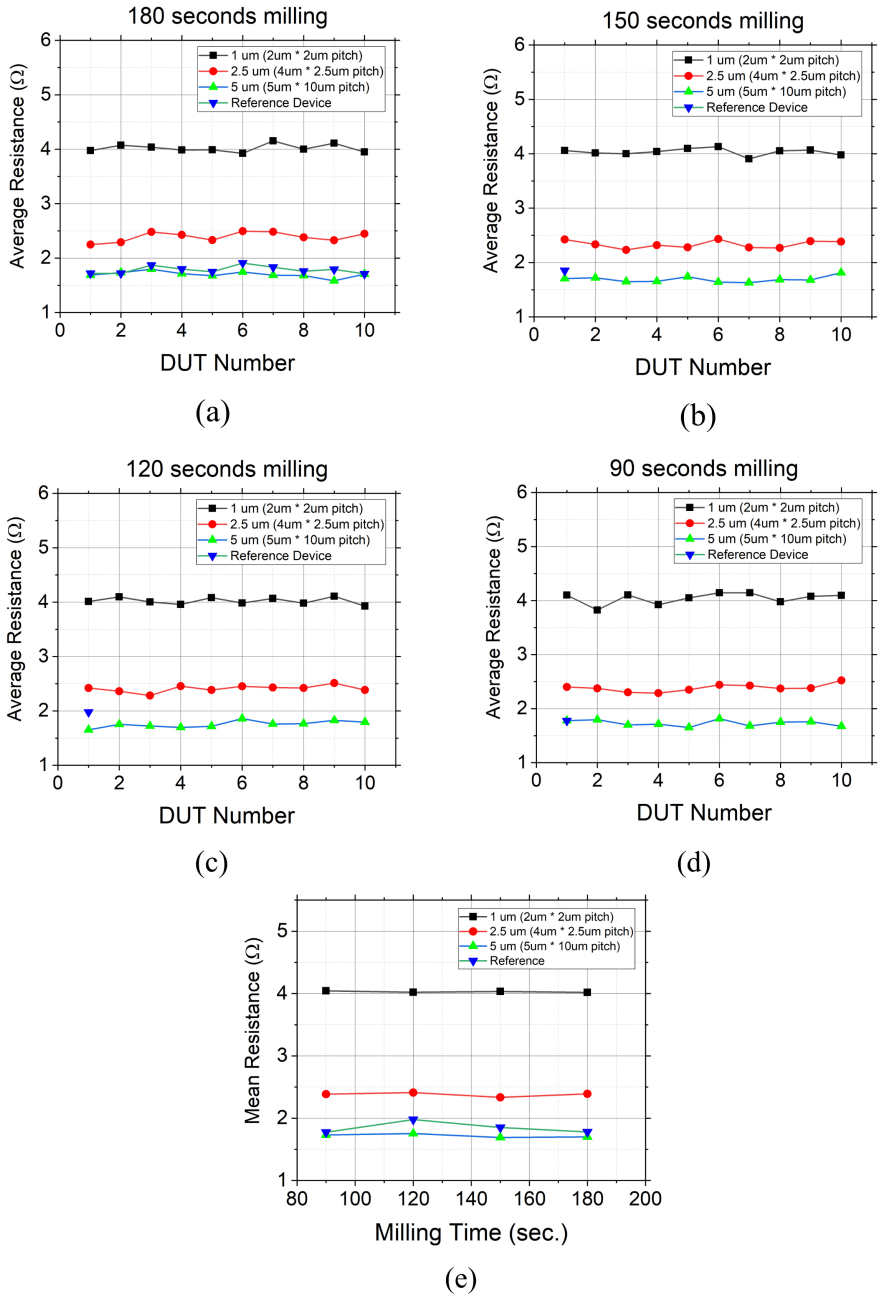


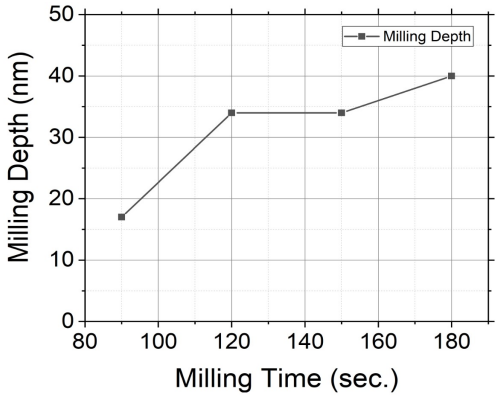
Figure 4.3: Measured resistance for 4 different milling durations with different patch sizes; (a) 90 seconds, (b) 120 seconds, (c) 150 seconds and (d) 180 seconds, and (e) shows the mean resistance of each DUT size over different milling durations

To quantify the amount of aluminum layer that can be removed during ion milling, we initially measured the milled profiles by Dektak profilometer [58]. The results are shown in Fig. 4.4 (a). Although there is a clear indication of aluminum removal during the milling process, the measurement was not accurate as the measured profiles were close to the tool's resolution limit [2].

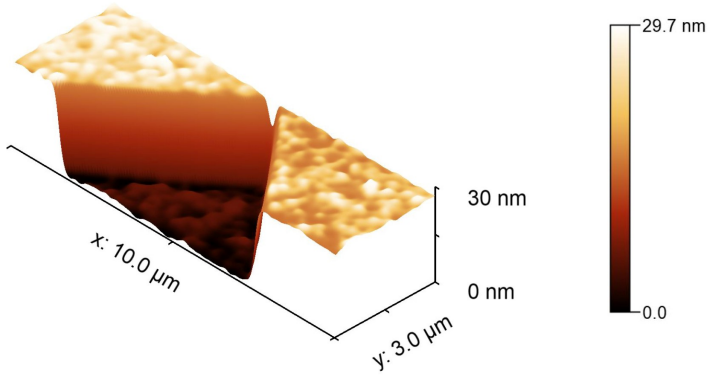
To acquire more accurate data, we patterned some openings on aluminum pads, and then milled the Al for 180, and 60 seconds. Then we measured the profile of the milled area on Al by atomic force microscopy (AFM). The results, illustrated in Fig. 4.4 (b) and (c), indicate that 180 seconds of ion milling removes about 26 nm of aluminum (including the oxidized surface), while this is about 6 nm for the case of 60 seconds milling.

The thickness of the aluminum surface oxide is normally about 2 nm, but it can be as thick as 7 nm [57, 59]. As a result, 60 seconds of ion milling may be a bit marginal for the worst case of oxide thickness, although this needs to be carefully investigated for the case of our Al films. For the experiments presented in section 4.3.2, we selected 90 seconds of ion milling that gives a safe margin.

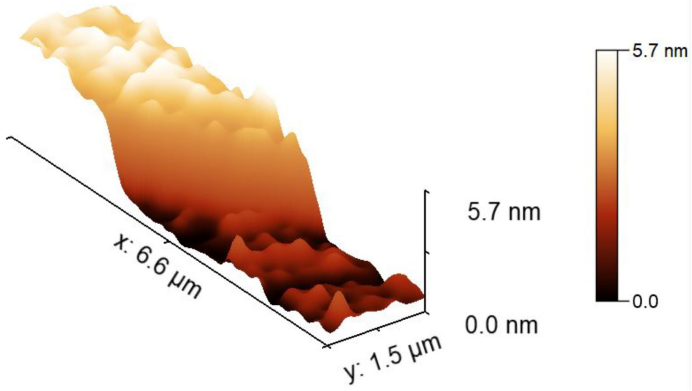
[2]The area was milled first and then covered by aluminum during the process. The numbers shown in the plot are calculated after measuring the profile on the aluminum and subtracting the background thickness



(a)



(b)



(c)

Figure 4.4: Effect of milling duration on the milling depth of aluminum, where (a) is a profilometer measuremnt, while (b) and (c) are AFM measurements for 180 seconds and 60 seconds of milling, respectively.

4.3.2 Reliability and reproducibility

After concluding that 90 seconds of milling is enough to obtain an ohmic contact, we decided to investigate the effect of milling time on the test junctions resistance, and the measurements results are presented here. Compared with the devices presented in section 4.1, the only difference is the milling time before depositing the patch layer, which is 90 seconds. 820 single JJs and 790 SQUIDs were measured using the automated probe station resulting in a yield of 97.2%.

Fig. 4.5 shows the resistance mean and standard deviation for JJs and SQUIDs fabricated using 90 and 210 seconds milling times, where the SQUIDs resistances are multiplied by 2. The mean resistances in Fig. 4.5 (a) and (c) show no big difference between the two cases (within 2%) except that the resistance is lower for smaller junctions in case of 90 seconds milling. For example, the difference in 100 nm junctions is 300 Ω for SQUIDs, and 200 Ω for single JJs. The reason for this change is not well-understood yet, but it is an additional confirmation that an ohmic contact is obtained. Histograms for different junction sizes are shown in Appx. C.

The standard deviation results (Fig. 4.5 (b) and (d)) are also comparable, with 90-second-milling process showing a standard deviation that is lower for small junctions, and slightly higher for bigger junctions. Overall, this shows that using the reduced milling time during the fabrication process, results in reliable and reproducible resistance values. More importantly, a shorter milling time can decrease the negative effect of aggressive milling of the substrate mentioned in section 3.3.1. As a further study, experimenting with even shorter milling times, and lower milling powers is suggested.

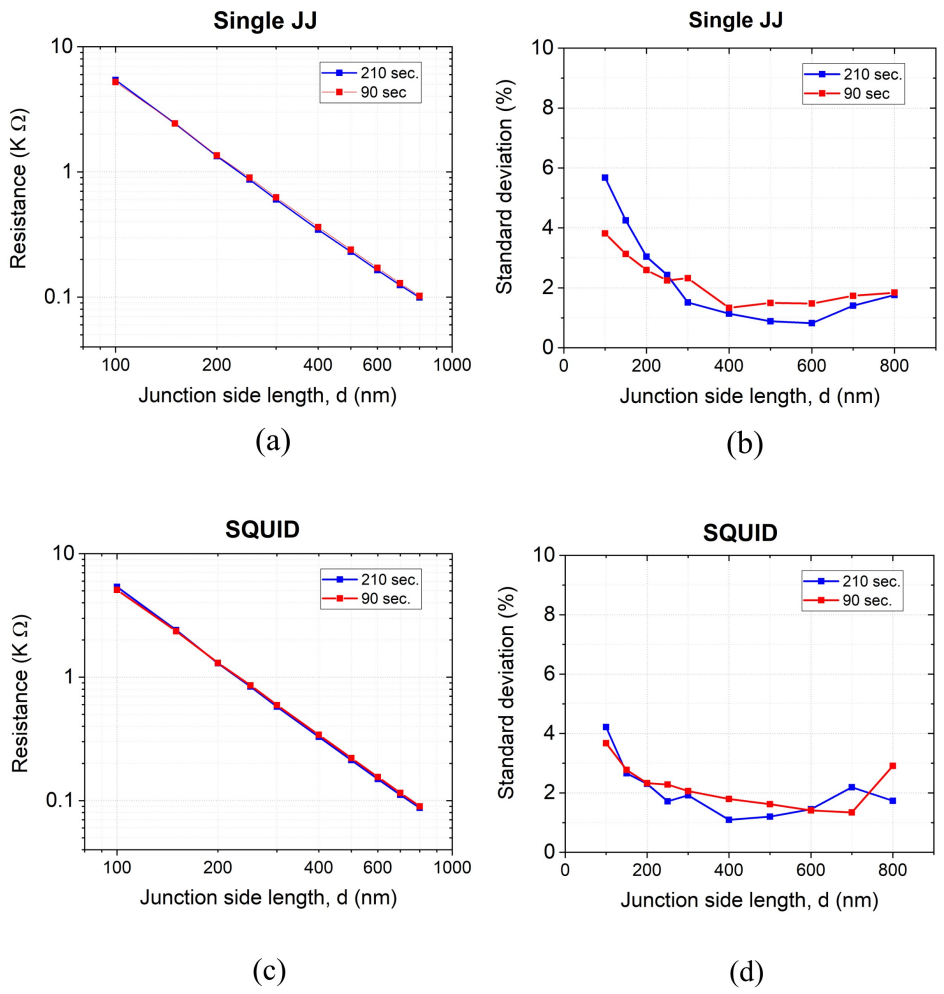


Figure 4.5: Comparison between the mean resistance and standard deviation, using 210 and 90 seconds of milling in case of JJ in (a) and (b), and in case of SQUIDs in (c) and (d)

4.4 One-step fabrication process

The fabrication results of the proposed one-step process are presented in this section. Only single JJs (∼2200 junctions) were fabricated using this technique with varying sizes similar to the previous experiments. As mentioned in section 3.3.2, this technique has potential advantages over the standard process. However, the size of JJs is limited by the deposition and milling angle.

A high fabrication yield above 97% was achieved for junctions with d = 100, 150, 200, 250 nm. For bigger junctions, the yield decreases until junctions with d $\geq$ 600 nm are completely short-circuited, as a result of the patch layer connecting both electrodes. The resistance histograms for different junction sizes are presented in Fig. 4.6, where they fit into a Gaussian distribution. The mean and standard deviation are shown in Fig. 4.7 (a) and (b), respectively.

Fig. 4.7 (a) also compares the mean resistance obtained from the one-step process to the standard process, and it shows that the resistance values are significantly higher for the latter. The difference is 1.8 kΩ for 100 nm junctions, and it gradually decreases to 75Ω for 400 nm junctions. Such a difference is too big to be caused by contact resistance, and the causes are still under investigation and a topic for further study.

The standard deviation of the two aforementioned processes is presented in Fig. 4.7 (b). Compared with the standard process, the Josephson junctions fabricated by the one-step method have a larger standard deviation, about 10% for 100 nm junctions down to about 3% for 400 nm junctions, and the standard deviation increases again for the 500 nm junctions. Since the major difference of the two approaches is the angle of milling/ deposition for the patch layer, the difference in standard deviation is most probably initiated from the same cause, but this needs to be investigated.

In summary, we think that the one-step fabrication is potentially a strong process that offers high yield and simplicity of fabrication. However, it has to be optimized to achieve lower standard deviation values and support fabrication of wider junctions.

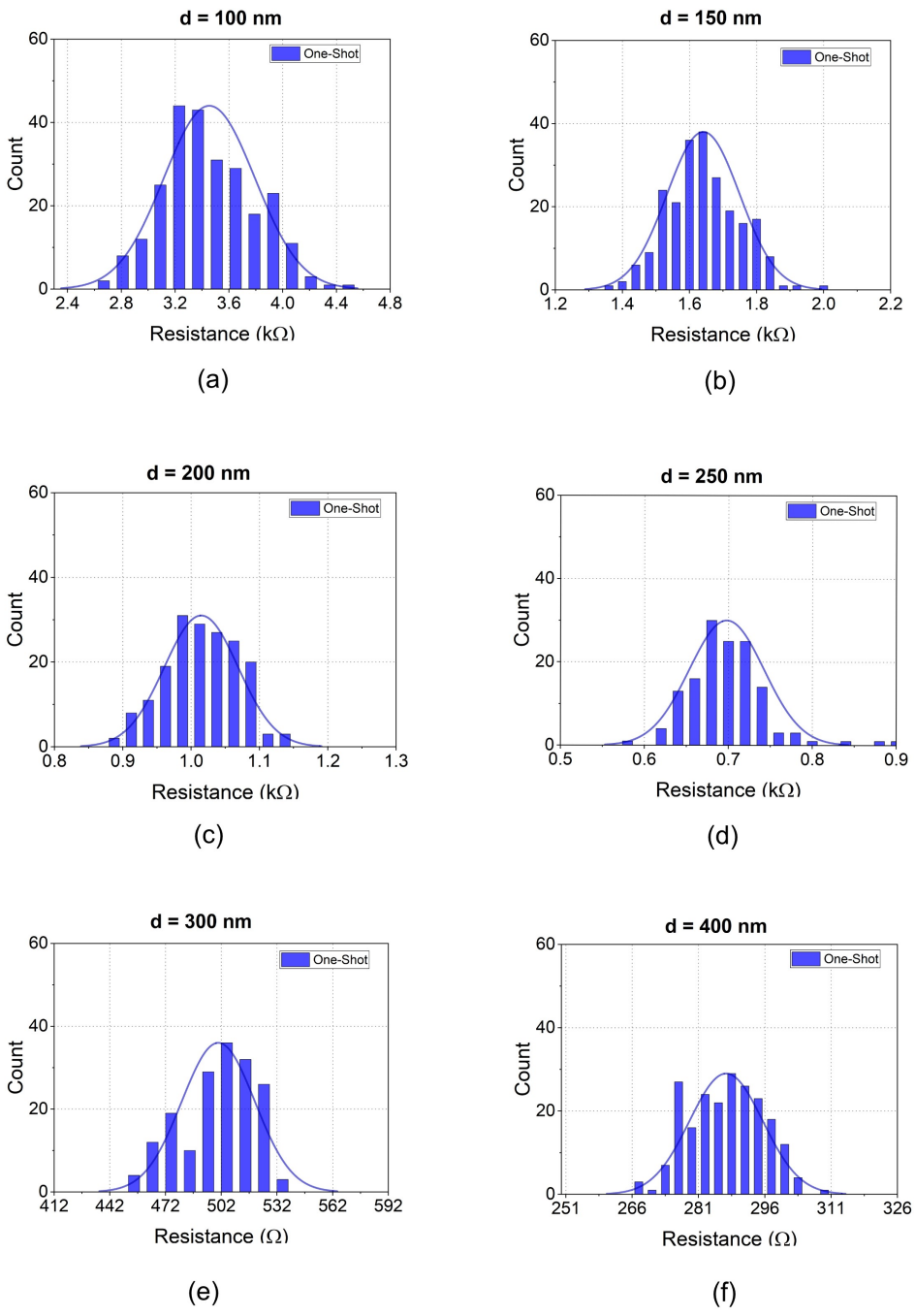


Figure 4.6: Histograms for different junction sizes fabricated using the one-step process

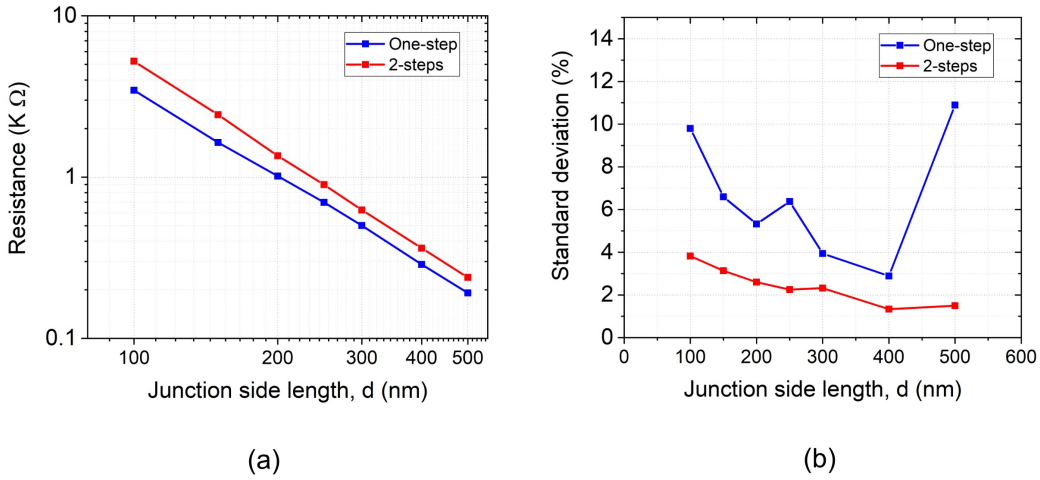


Figure 4.7: Comparison between the one-step and the 2-step standard process in terms of the (a) mean resistance and (b) standard deviation

Chapter 5

Conclusion and outlook

In this thesis, the reliability and reproducibility of the cross-type lithography technique of JJ were analyzed. The fabrication yield was higher than 97%, and the resistance of junctions with different sizes fitted into a Gaussian distribution with a standard deviation between 0.8% and 5.5%, depending on the junction size. With these statistics, one can predict the accuracy of the transmon plasma frequency, v_p, and the Josephson inductance, L_J prior to fabrication. The standard deviation of v_p was calculated to lie between 0.4% and 2.75%, while for L_J, it is similar to that of the resistance.

In an attempt to optimize the fabrication process, $Ar+$ milling test was done in order to find a reduced milling duration, with which one can still maintain an ohmic contact. As a result of this test, the milling time before the patch layer was reduced from 210 seconds to 90 seconds. This might have a positive effect on the quality of the qubit, which is encouraged to be investigated in a future work. The reliability and reproducibility of the fabrication process after reducing the milling time was also investigated, and found to be comparable to that of the standard process. The standard deviation window was even smaller in this process, ranging from 1.3% to 3.8%. Additionally, comparing the mean resistance obtained in the two processes, junctions with small sizes had lower resistance in case of 90 seconds of milling (down to 300 Ω lower resistance). The causes for such a difference are yet to be investigated; however, we think that this number is too big to be caused by the contact resistance only.

Finally, we proposed a one-step fabrication technique, where the JJ and the patch layer are fabricated in one lithography step, reducing the junction fabrication time by 50%. More importantly, this technique avoids milling the substrate, which is known to reduce the quality of the qubit [52, 53]. Additionally, exposing the JJ to subsequent processes like resist baking and lift-off is avoided. Reliability and reproducibility analysis performed on the test junctions that are fabricated by this

approach show a high fabrication yield of more than 97.5% for small junctions (100 to 250 nm); however, the yield decreases with bigger junctions until it reaches a zero for junctions that are 600 nm and wider. This is expected due to the limitations imposed by the resist thickness, in addition to the milling and deposition angles. The results indicate that the one-step technique at the current stage is most suitable for junctions with small width. One can however use a thicker bilayer to fabricate wider junctions.

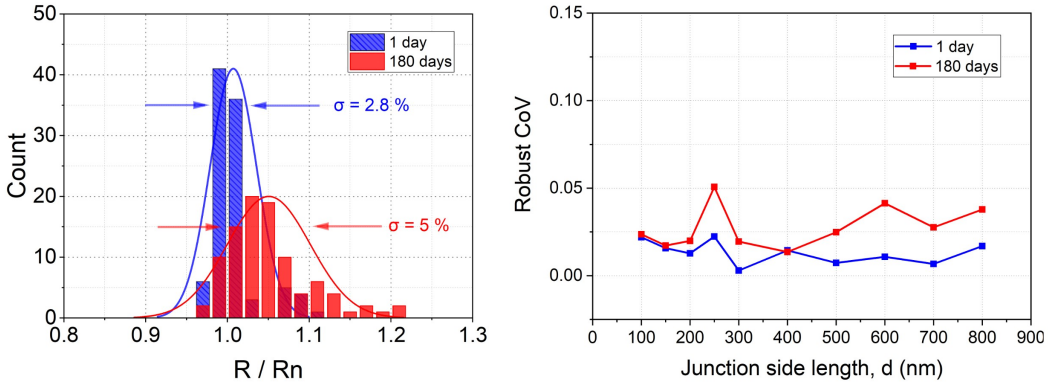
We also found that compared with the test junctions that are fabricated by the two-step process, similar size junctions made by the one-step method show a smaller resistance. Understanding the causes for the lower resistance, and later running coherence measurements on the qubits fabricated by this method are other subjects that we suggest for future study.

Future work also includes the study of JJ ageing, i.e. increasing the resistance overtime [61]. The amount by which the resistance increases is highly dependent on the fabrication process and the conditions (e.g. pressure and temperature) at which the JJs are preserved. For example, in [60] and [61], resistances increased between 100% and 400%. However, in [62], prior to evaporating the junction metal, the resist residue was removed by reactive ion etching (RIE) (similar to our de-scumming process in Appx. A. The junctions fabricated this way showed very little or no increase in the resistance.

A tentative aging study is made over about 100 test devices (10 different sizes with about 10 devices each) that compares the resistances measured right after fabrication and 6 month later. Fig. 5.1 (a) shows a histogram of the normalized resistances of all the test devices [1] one day (blue) and 180 days (red) after the fabrication process. While on average the devices aged by about 5%, the resistance standard deviation increased from 2.8% to 5%. The increase of the standard deviation can be attributed to the redistribution in the oxide barrier. Fig. 5.1 (b) shows the robust coefficient of variation (CoV)[2] for each size. From the curves it is hard to find a clear dependency of resistance ageing to the junction size, except for the bigger junction widths that show a larger deviation. To obtain a better understanding on the junction ageing behavior, study of a larger dataset, and resistance measurements in more time intervals are suggested.

[1] The resistance of each test device is divided over the mean resistance of all test devices with the same size JJ

[2] The robust coefficient of variation is the normalized standard deviation excluding outliers



(a) (b)

Figure 5.1: Aging of JJs. (a) Histogram of the normalized resistances of JJs, 1 day (blue), and 180 days (red) after fabrication. (b) Robust coefficient of variation of the measurements in (a).

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Appendix A

Fabrication Process

A.1 Mask-less Lithography

The two mask-less lithography machines used in our fabrication are the Laser Writer *DWL 2000* (optical lithography) and *JEOL JBX 9300FS* (Electron Beam Lithography or EBL). The choice of the lithography technique determines the type of the resist used and accordingly how it is treated, i.e. coating, development and descumming.

A.1.1 Treatment of Laser Writer Resist

Resist Coating

1. Dehydrate the wafer at 200°C for 5 minutes
2. Spin coat LOR 3A [63] at 3000 rpm with acceleration 2000 rpm/s for 60 seconds
3. Pre-bake the resist at 200°C for 5 minutes
4. Spin coat S1805 [64] at 3000 rpm with acceleration 2000 rpm/s for 60 seconds
5. Pre-bake the resist at 110°C for 1 minute

Resist Development

1. Develop in CD26 for 45 seconds.
2. Dip in deionized water for 60 seconds
3. Rinse with deionized water for 2 minutes
4. De-scum (ashing) using oxygen plasma at 40 watts for 30 seconds

A.1.2 Treatment of EBL Resist

Resist Coating

- Spin coat MMA [66] at 3000 rpm with acceleration 1500 rpm/s for 60 seconds
- Pre-bake the resist at 160°C for 5 minutes
- Spin coat PMMA [66] at 6000 rpm with acceleration 2000 rpm/s for 60 seconds
- Pre-bake the resist at 160°C for 5 minutes

A.1.3 Resist Development

- Develop in MIBK:IPA (1:1) [67] for 90 seconds.
- Rinse in IPA [67] for 30 seconds.
- De-scum (ashing) using oxygen plasma at 25 watts for 20 seconds

A.2 Al Evaporation

Aluminum evaporation for all layers is done using electron beam evaporation in *Plassys MEB 550 S*, which supports planetary rotation and tilt, in addition to *in situ* oxidation and ion-milling. This is mainly useful for the fabrication of layer 2 and 3. For all three layers, aluminum is deposited at rate of 1 nm/s in the vacuum pressure of about 10^{-7} mbar at room temperature.

A.3 Lift-off Process

Lift-off is a technique used for patterning a thin film on a substrate, where the photoresist is firstly deposited, and patterned; then coated by the thin film. The film will be deposited both on the substrate, and on top of the resist layer, as shown in Fig. A.1. The next step is then to dissolve the resist by submerging it in a proper solvent. Once the resist is removed, the metallic layer that was deposited on it will be washed away too, leaving only the desired, patterned film on the substrate.

One of the main challenges of the liftoff process is the deposition of the thin film on the sidewall of the resist, that prevents the solvent from reaching the resist layer as in Fig. A.1 (a). Side wall deposition can be problematic if the resist is not thick enough, or if a positive tone resist [68] is used for the optical lithography. A negative tone resist naturally has a negative slope that prevents the metal deposition on the sidewalls. Alternatively, one can use a bi-layer stack in Fig. A.1 (b), where the top layer is the resist, and the bottom layer is an undercut layer. With appropriate development of the resist, the undercut layer would be slightly overdeveloped compared with the resist layer. This causes a discontinuous profile between the metal that is deposited on the substrate and the sidewalls.

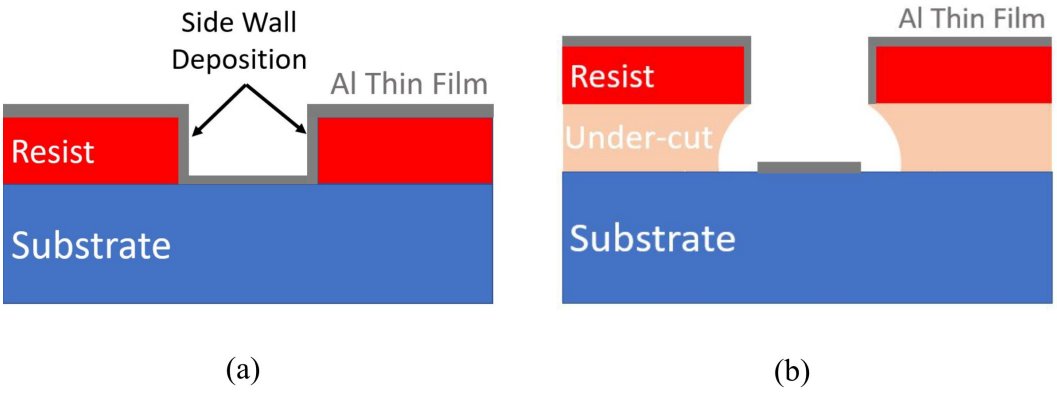

Figure A.1: Aluminum thin film deposition on (a) single layer resist with sidewall deposition and (b) bilayer resist with discontinuous sidewall deposition

Appendix B

Patching Reproducibility

Table B.1: Mean and Standard Deviation for the resistances of different DUTs and milling durations explained in section 4.3.1, where layout 1 has $1um$ line width with $2 \times 2um$ patch size, layout 2 has $2um$ line width with $2.5 \times 4um$ patch size and layout 3 has $5um$ line width with $5 \times 10um$ patch size (Fig. 3.6)

Milling Time (Seconds)	Layout 1 (Ω)	Layout 2 (Ω)	Layout 3 (Ω)
90	4.04 ± 0.1	2.39 ± 0.07	1.73 ± 0.06
120	4.02 ± 0.06	2.41 ± 0.06	1.75 ± 0.06
150	4.03 ± 0.06	2.33 ± 0.07	1.69 ± 0.06
180	4.02 ± 0.07	2.39 ± 0.09	1.7 ± 0.06

Appendix C

90-second milling process histograms

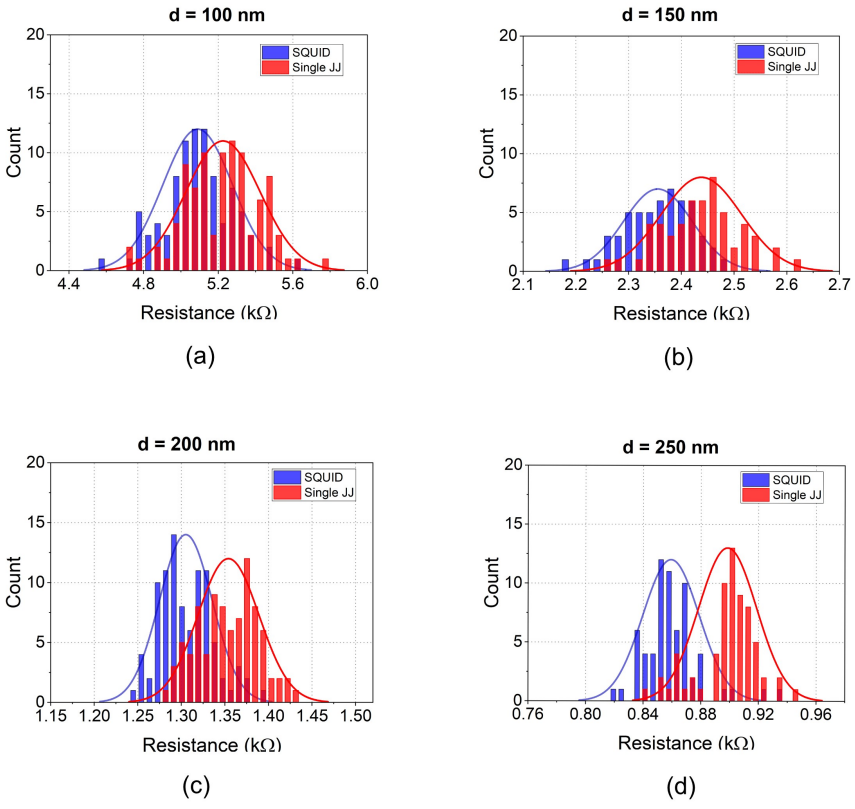

Figure C.1: Histograms of 100 to 800 nm junctions fabricated using the 90-second milling process are shown in (a)-(j) -continued on next page-

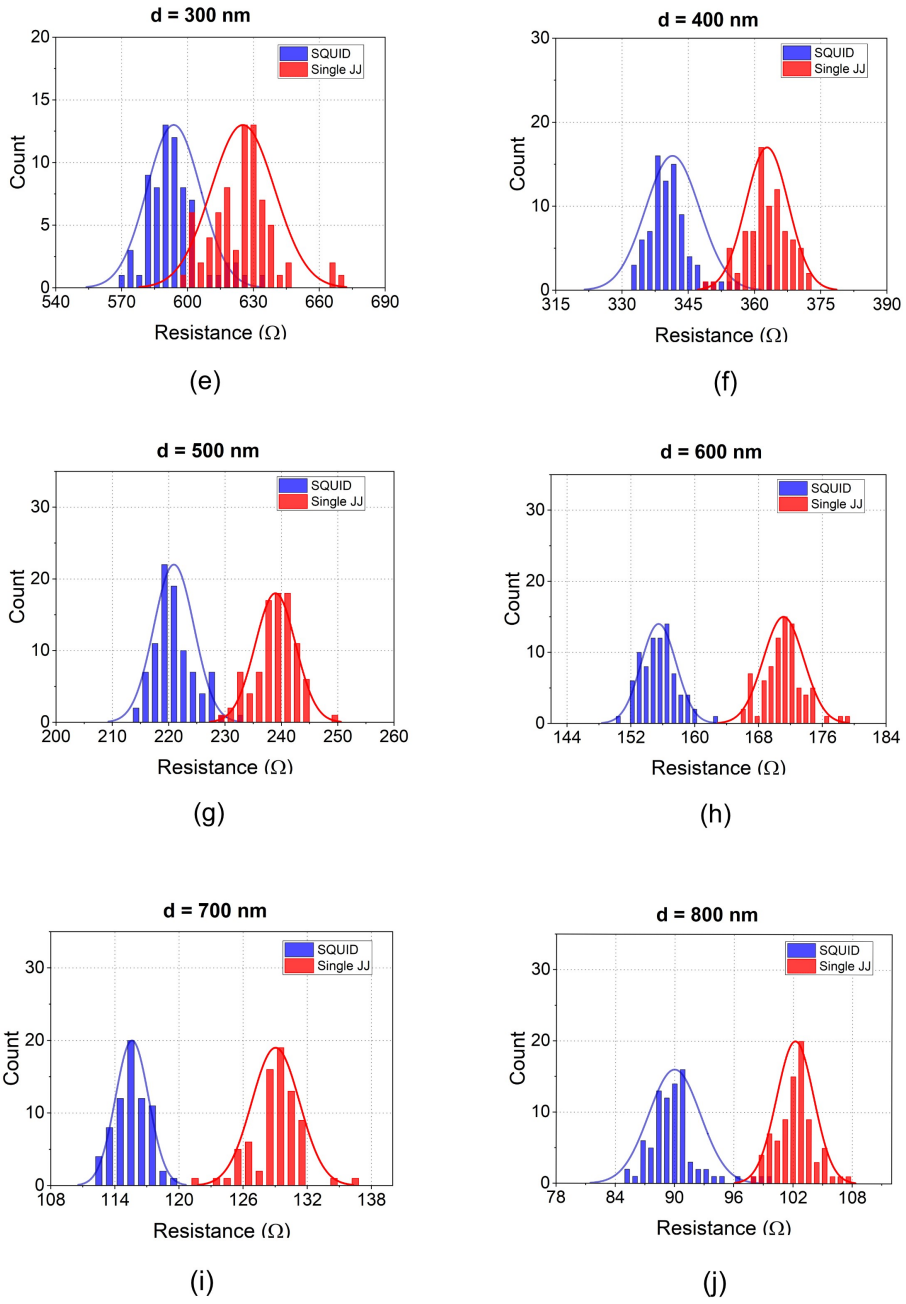

Figure C.1: Histograms of 100 to 800 nm junctions fabricated using the 90-second milling process are shown in (a)-(j)