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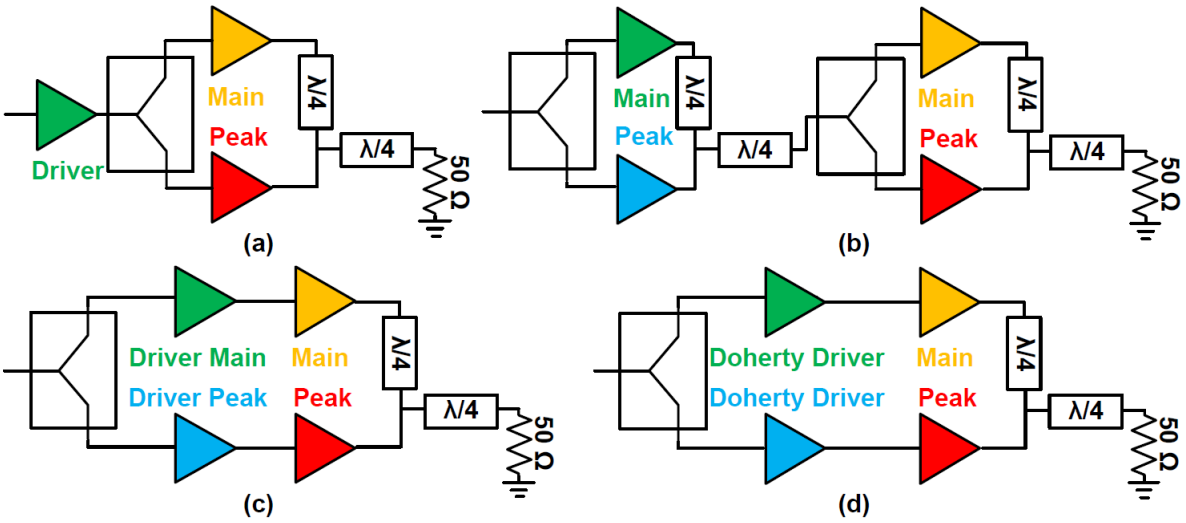

Comparison of Different Driver Topologies for RF Doherty Power Amplifiers

Master's Thesis in Wireless, Photonics and Space Engineering

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Gothenburg, Sweden 2015

Thesis for the degree of Master of Science in Wireless, Photonics and Space Engineering

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Abstract

This thesis investigates different driver topologies for RF Doherty power amplifiers (DPAs). The investigation is based on the simulation of four different driver configurations in Matlab and Advanced Design Systems (ADS) tools. The topologies of the two-stage PA are as follows: (1) cascaded class-AB and a DPA, (2) two-stage cascaded DPAs, (3) DPA with embedded class-ABs and (4) DPA with embedded Dohertys as drivers.

Using ideal transistor models, the analysis of the different two-stage power amplifier topologies have been compared through Matlab simulations. The results show that the two-stage cascaded DPA provide the best performance since its efficiency in back-off is higher than the other topologies.

To verify the Matlab simulations, the different topologies have been designed and simulated in ADS using real transistor models. The driver and final-stage desined based on 10W (CGH40010F) and 45W (CGH40045F) GaN-HEMT transistors from Cree devices respectively. The required fundamental source and load impedances are obtained from the source- and load-pull simulations. Moreover, the second and third harmonic terminations have been simulated and tuned in order to get the highest possible Power-Added Efficiency (PAE). These amplifiers have made the basis to simulate the four different two-stage power amplifier efficiencies. The ADS simulation results are in good agreement with the Matlab simulations and confirm that the two-stage cascaded DPAs outperforms the other topologies in term of efficiency.

All four different topologies have been designed in band-I (2.11-2.17 GHz). The two-stage cascaded Doherty PA exhibits the highest PAE. It consists of the Doherty driver-stage that exhibits a peak output power of 42dBm, a power gain of 13 dB, a PAE of 60% at 6dB back-off and 74% at peak output power. The Doherty-final-stage has 58% PAE at 6-dB back-off and a peak PAE of 73%. Its power gain and peak output power are 12 dB and 50 dBm, respectively. The simulation results of the two-stage-cascaded DPA provides 26 dB power gain at 50 dBm peak output power, a PAE of 58% at 6-dB back-off and 73% PAE. The desired topology (2) exhibits 3% and 5% more PAE comparing to the topology (1) and (3) at 6-dB output back-off respectively. In addition it has about 3% more PAE comparing to the topology (4) at the peak output power. Regarding to the total gain, topology (1) has the highest gain. However, topology (4) has a very flat gain of 30.5-31.5 dB over P_{out} = 34-49.5 dBm which can result in a more linear behavior. The obtained results demonstrate the importance of the driver topology on total efficiency of the two-stage power amplifiers when signals with large PAPR are used.

Keywords: Driver amplifier, Doherty power amplifier, GaN-HEMT, Two-stage power amplifier.

Acknowledgements

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Abbreviations and acronyms

ADS	Advanced Design System
BLC	Branch line coupler
DPA	Doherty power amplifier
EER	Envelope elimination and restoration
GaN	Gallium-Nitrite
G	Gain
IMN	Input matching network
MIMO	Multiple input-multiple output
OBO	Output Back-Off
OFDM	Orthogonal frequency division multiplexing
OMN	Output matching network
PA	Power Amplifier
PAE	Power added efficiency
PAPR	Peak to average power ratio
PDF	Probability distribution function
Pin	Input power
Pout	Output power
RBS	Radio base station
RF	Radio frequency
Vgs	Gate-Source voltage
Vth	Threshold Voltage
WCDMA	Wide-band code division multiple access
Zs	Fundamental source harmonic
ZL	Fundamental load harmonic
Z2fs	Second harmonic source impedance
Z2fL	Second harmonic load impedance
Z3fL	Load harmonic third impedance

Contents

1

Introduction

1.1 Background

The demand for wireless communications is growing rapidly [1]. Therefore, new techniques for increasing the network capacity such as advanced modulation schemes are needed. Orthogonal Frequency Division multiplexing (OFDM) and Single Carrier Frequency Domain Equalization (SC-FDE) are two examples of the new modulation schemes.

Unlike conventional modulation schemes, the new ones have a time varying envelope and generally have Peak-to-Average Power ratio (PAPR) of 6-10 dB. This can affect the performance of the traditional PAs, since they were mainly designed to have high efficiency at peak power. Therefore it is highly desired to have new PAs that can provide high efficiency at wider range of output power levels. Doherty power amplifier (DPA) is a technique which enhances the energy efficiency of the PAs at lower input levels and therefore decreases the heat generated by the PAs. In addition, increasing the efficiency affects the weight and reliability of Radio Base Stations (RBSs) and mobile phones [2].

1.2 Thesis contributions

In modern wireless communication systems, the efficiency of multi-stage PA lineup is an important figure of merit. For the final-stage, the Doherty and the envelope tracking techniques are used to boost the linearity, power, and efficiency [3]. To achieve highly efficient two-stage PA, it is not only important to have high efficiency final-stage, but to have an efficient driver-stage as well.

Although numerous DPA designs have been demonstrated in the literature such as [4, 5], the main focus is barely on the driver-stage amplifiers. In [6] a two-stage cascade Doherty power amplifiers is demonstrated and the efficiency is compared with a DPA which is driven by a class-AB amplifier. However, the results are not compared in the same fair condition since different PAs are used in DPAs. In this thesis, all topologies

are compared by utilizing the same PAs. DPAs with embedded driver-stage are demonstrated in [7, 8, 9]. However, in this thesis, it is shown that the embedded topologies have a lower efficiency due to the extra DC power consumption.

One of the important issues that should be considered in designing a PA, is the amplifier linearity. This is because the non-linearity not only distorts the signal in the desired band, it can also damage neighboring channels. Due to the time limitation of this thesis, the assessment of the linearity of different topologies is postponed to the future.

In this thesis, different driver topologies for DPA are presented in order to investigate the total efficiency of the two-stage PA lineup. In our topologies, two GaN-HEMT transistors are used for the driver and the final-stage amplifiers respectively. The scope of this thesis is to design and simulate different two-stage topologies and the best configuration will be fabricated and measured in the future. Next section describes the design specifications of the PA.

1.3 Technical Specifications

The Design specification of the PA is presented in table 1.1. The PA is designed based on the nonlinear model of the devices.

Table 1.1: Design specifications for band-1 PA

Parameter	Specification
Frequency	Band-I (2.11-2.17 GHz)
Peak Output Power	100W (50dBm)
Gain	$\geq$ 20dB
PAE at Peak	$\geq$ 70%
PAE at 6dB Output Back-Off	$\geq$ 60%

1.4 Thesis outline

This thesis focuses on the study and design on highly efficient two-stage PAs. Chapter 2 reviews briefly the theory of different traditional PA classes, harmonically tuned PAs, and Doherty PAs. In chapter 3, the different two-stage PA topologies and their efficiency simulations is introduced in Matlab. In chapter 4, different steps of two-stage PA design including bias point selection, Source/Load-Pull simulations, and matching networks are presented together with the complete two-stage PA simulation results. These simulations are done in ADS tool. Finally, the conclusion is given in chapter 5 followed by suggestions for the continuation of this work.

2

Theory

Amplifiers are essential components of RF circuits. They take a small signal and make it larger by converting DC power from supplies into RF power as shown in Fig. 2.1. The effectiveness of this conversion is known as the drain efficiency of the amplifier and is defined by:

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.1}$$

Efficiency in PAs is much more important than that of small signal amplifiers. From above equation, it is seen that $P_{DC} = P_{out}/\eta$. In small signal amplifiers even with low efficiency, the absolute DC consumption is small. However, in PAs even with high efficiency, the absolute DC consumption is high. Hence, efficiency is indeed one of the key parameters in PAs design.

In order to take into account the effect of the amplifier gain on the efficiency, PAE

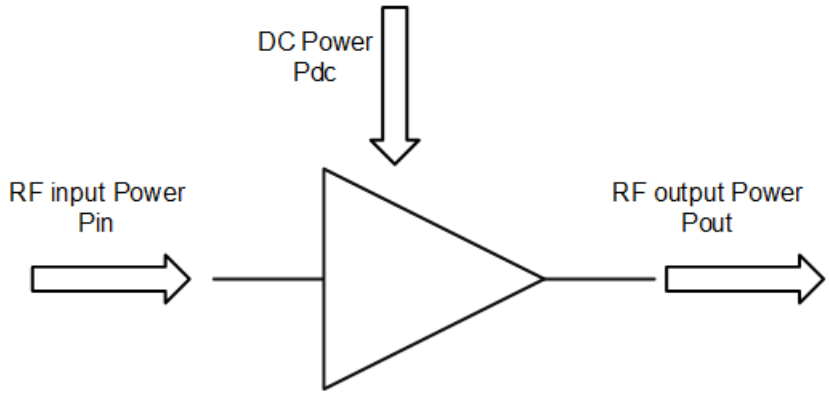

Figure 2.1: Energetic schematic representation of amplifier operation.

is introduced as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}(1 - \frac{1}{G}) = \eta(1 - \frac{1}{G}) \tag{2.2}$$

where G is the amplifier gain. It can be noticed from Eq 2.2 that when the amplifier exhibits high gain, the PAE and the drain efficiency become almost equal.

2.1 Classes of Operations

The PAs are normally classified based on the operating conditions which can refer to the bias point selection (Class A, AB, B or C), choosing of matching network topologies (Tuned Load, Class F, etc.) or transistor operating conditions (Class E, Class S, etc.) [10, 11].

2.1.1 Conventional Classes A, B, AB and C

Conventional PA Classes are classified based on quiescent bias point which is chosen in the design of the PA (Fig. 2.2). This can be identified in terms of device current conduction angle (CCA, Φ) which is the fraction of the RF signal period where the device has a non-zero current. However, it should be noted that CCA depends on the input RF level (table 2.1).

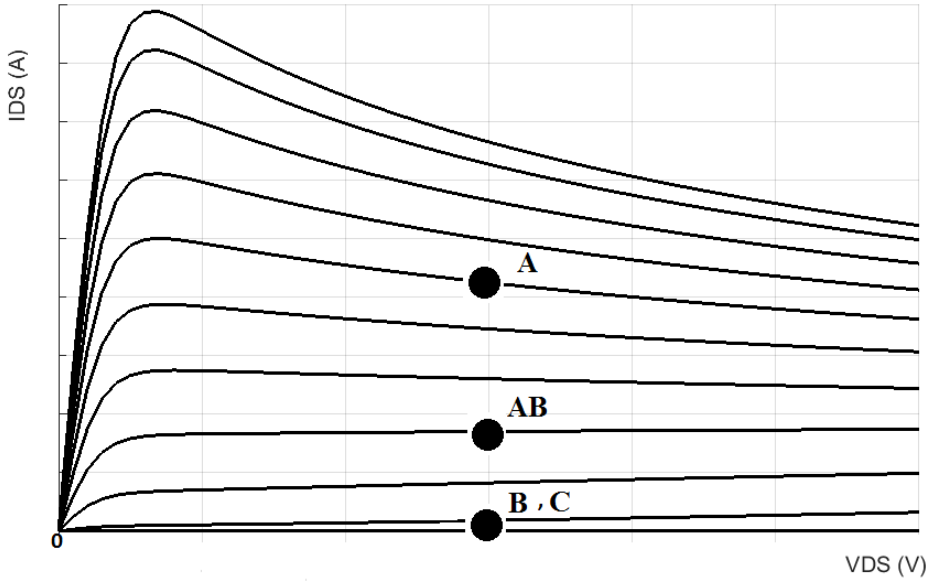

Figure 2.2: Class of operation defined by the device quiescent bias point.

Table 2.1: PA classification in term of output current conduction angle or biasing point

Operating Class	CCA Φ	Drive level dependency	Bias
A	$\Phi = 2\pi$	No	Between Pinch-off and Saturation
AB	$\pi < \Phi < 2\pi$	Yes	Above Pinch-off
B	$\Phi = \pi$	No	Pinch-off
C	$\Phi < \pi$	Yes	Below Pinch-off

In class A, the transistor is biased between pinch-off and saturation regions and conducts at all times. The main drawback of this Class of operation is its power consumption even without any RF input drive, however, its high linearity is the main advantage. In class B, the transistor is biased at pinch-off gate voltage and conducts half of the cycle. The advantage of this class is that there is no DC current consumption without RF input signal. In class AB, the transistor is conducting slightly more than the half cycle. By operating in this class, more linearity will be achieved comparing to the class B and more efficiency can be obtained comparing to the class A. In class C, the transistor is biased below the pinch-off and conducts less than the half cycle. This class has a higher efficiency, however, it is very nonlinear.

In order to evaluate the performance of above amplifier classes quantitatively, Tuned-Load (TL) operation mode is assumed [10]. In this operation mode, high order harmonics are short-circuited. Hence, the output voltage is purely sinusoidal but the current contains high order harmonics as well (Fig. 2.3). By taking the Fourier series of the output current, the output power and the efficiency can be calculated as

$$P_{RF,TL} = \frac{I_{Max}(V_{DC} - V_k)}{4\pi} \frac{\Phi - sin(\Phi)}{1 - cos(\Phi/2)} \tag{2.3}$$

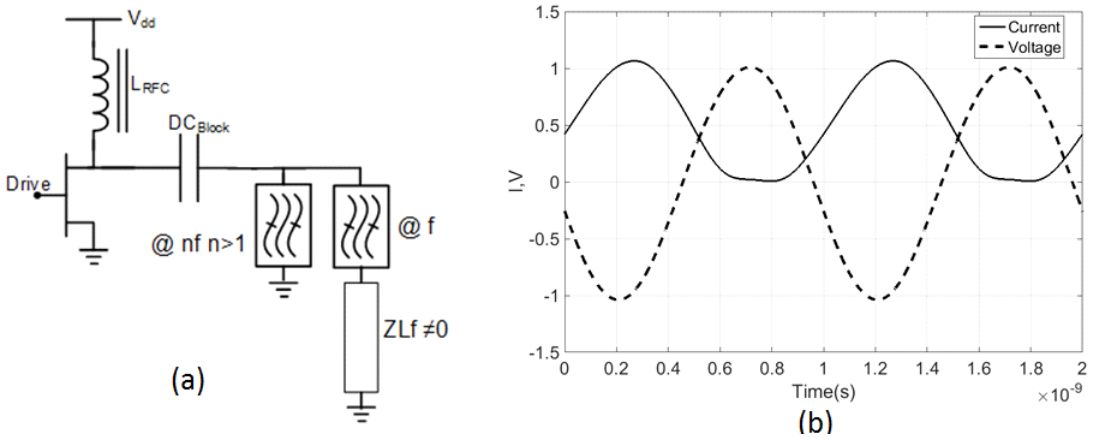

Figure 2.3: (a) Circuit topology of tuned load amplifiers (b) Voltage and current waveforms for tuned load amplifiers.

$$\eta_{TL} = 0.5(1 - \frac{V_k}{V_{DC}})\frac{\Phi - sin(\Phi)}{2sin(\Phi/2) - \Phi/2cos(\Phi/2)} \tag{2.4}$$

The above equations are plotted in Fig.2.4 with $\chi = V_k/V_{DC}$. It can be seen that class A and B amplifiers have the same output power but class B amplifier needs 6-dB more input power to reach the same output power as class A amplifier. The highest output power can be achieved in class AB. The efficiency in this plot is normalized to $1-\chi$. Hence, if the device has a high χ value, the efficiency can be severely degraded. It should be noted that the above efficiency is the maximum efficiency that can be achieved at a given Φ with $V_{swing} = V_{DC} - V_k$. By reducing the drive level, the efficiency decreases rapidly (Fig. 2.5).

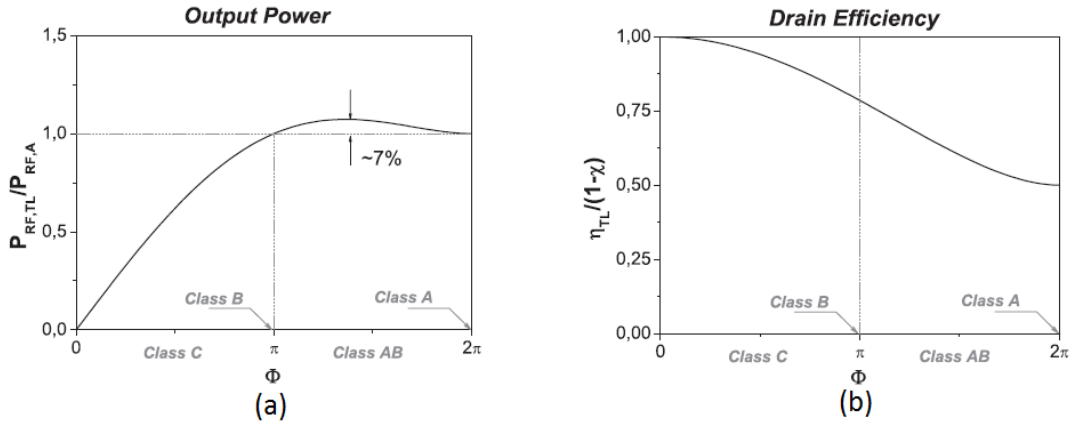

Figure 2.4: Optimum output power $P_{RF,TL}$ for the tuned load operating condition,normalized to the corresponding class A quantities and the drain efficiency η_{TL} [10].

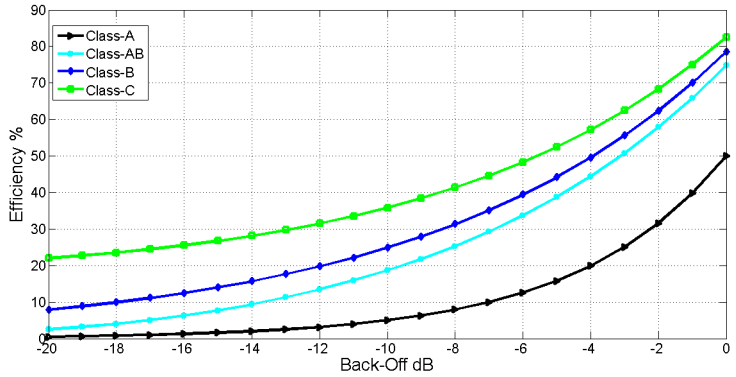

Figure 2.5: TL normalized efficiency as function of the normalized input power, for different bias conditions ξ=$I_{d,DC}/I_{max}$.

2.1.2 Harmonically Tuned Power Amplifiers

The power balance condition for the amplifier states that the power delivered to the termination at the fundamental and harmonic frequencies plus the dissipated power in the transistor should be equal to the total supplied DC power (assuming lossless matching networks and a negligible P_{in} contribution). This can be written as

$$P_{DC} = P_{out,f} + \sum P_{out,nf} + P_{diss} \tag{2.5}$$

hence

$$\eta = \frac{P_{out,f}}{P_{DC}} = \frac{P_{out,f}}{P_{out,f} + \sum P_{out,nf} + P_{diss}} \tag{2.6}$$

As can be seen, in order to increase the efficiency the power delivered to the harmonic frequencies and the dissipated power in the transistor should be reduced. There are several approaches for achieving this goal such as utilizing Class E and F amplifiers [12, 13, 14]. These approaches are suitable at low frequencies where a large number of harmonic terminations can be effectively controlled. At microwave frequencies, the control of higher order harmonics (n>3) become unfeasible, since the output capacitances of the transistor practically short-circuit higher frequency components. Assuming short-circuit conditions for higher-order (n>3) harmonic components, drain efficiency becomes

$$\eta = \frac{P_{out,f}}{P_{DC}} = \frac{P_{out,f}}{P_{out,f} + P_{out,2f} + P_{out,3f} + P_{diss}} \tag{2.7}$$

In high frequency harmonic tuning approach, the second and third harmonics are tuned to maximize the output power delivered at fundamental frequency. The approach can be interpreted mathematically as follow: Unlike TL operation mode where the drain voltage has only the fundamental mode, the output voltage in this case is written as:

$$V_{DS}(t) = V_{DD} - V_1(cos(\omega.t) + k_2 cos(2\omega.t) + k_3 cos(3\omega.t)) \tag{2.8}$$

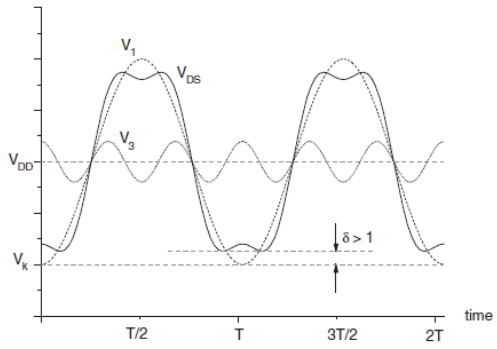

Figure 2.6: Output voltage obtained by adding DC, fundamental and third harmonic components [10].

$V_{DS}(t)$ is restricted by the device limitations, i.e. V_k and the breakdown voltage. In this method, the aim is to increase V_1 while by choosing proper k_2 and k_3, $V_{DS}(t)$ is kept in the allowed range (Fig. 2.6). In practice by performing load-pull and source-pull simulations on fundamental and harmonics (2nd and 3rd), the optimum terminations will be achieved.

2.2 Doherty Power Amplifiers

New modulation schemes such as OFDM have time-varying envelopes with typical PAPR in the range 6–12 dB [15]. As shown in Fig. 2.5, the efficiency is decreased more than two times when the input drive decreases 6-dB. Therefore, classical amplifiers are not suitable in terms of efficiency for the new modulation schemes. The need to develop cheaper and more efficient PAs to reach this requirement has pushed research to achieve to different techniques. In the new modulation techniques, it has been proposed to increase the average efficiency of PAs for the signals with different PAR. The latter efficiency depends on the instantiations efficiency and the probability density function (PDF) of the input signal. The PDF which depends on the modulation signals, can be driven either by simulation or measurement. PA's average efficiency which operates at maximum efficiency levels only for small time slots while mainly operates in a special range of output Back-Off is affected by PDF. As a result, input signals with different PAR causes to have a lower average efficiency in the classical power amplifiers and therefore this has become an important issue in the modern modulation techniques. Hence, we need to have new PA topologies that have higher efficiency at lower input levels. Envelope tracking (ET), Doherty amplifiers and varactor based dynamic load modulation are the most common techniques to solve this problem. The ease of structure and circuit simplicity give the DPA many advantages over the other techniques.[2, 10, 16, 17, 18].

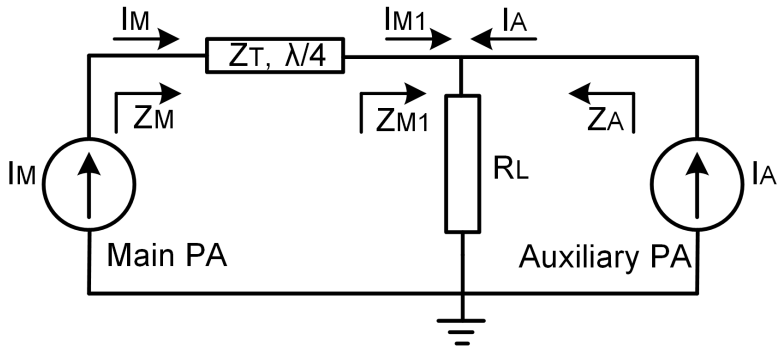

Figure 2.7: Operational diagram of DPA.

The idea behind Doherty amplifier simply explained as follows. In a class B amplifier the efficiency depends on the output swing voltage as

$$\eta_B = \frac{\pi}{4}\frac{V_{output}}{V_{DC}} \tag{2.9}$$

If we can keep the maximum output swing voltage over a special range of input drive, the efficiency will remain at the highest value in that range. Since $V_{output} = RI$, by increasing the current by increasing the input power, the load (R) should be reduced in such a way that V_{output} remain constant. For example if the output current is doubled the load should be halved. In that case the V_{output} have the same value while the output power is doubled ($P_{out} = \frac{1}{2}RI^2$). This concept is called a load modulation. The load modulation in DPA is performed by using two amplifiers called main and auxiliary as shown in Fig. 2.7. In this configuration the impedances (Z_M and Z_A) are modulated by the ratio of amplifier currents (I_M and I_A) as follow

$$Z_M = \frac{Z_T^2}{R_L} - jZ_T\frac{I_A}{I_M} \tag{2.10}$$

$$Z_A = \frac{I_M R_L}{jI_A} \tag{2.11}$$

In above equation in order to have real impedance there should be 90-degree phase difference between I_M and I_A. It is seen that if $Z_T = 2R_L$ then by changing I_P from 0 to $-jI_M$ then Z_M varies from $4R_L$ to $2R_L$ and Z_A varies from ∞ to $2R_L$. Fig. 2.8 and 2.9 show the impedance and current variation of the main and auxiliary amplifiers during load modulation technique. Impedance in Fig. 2.8 is normalized to 1 Ω.

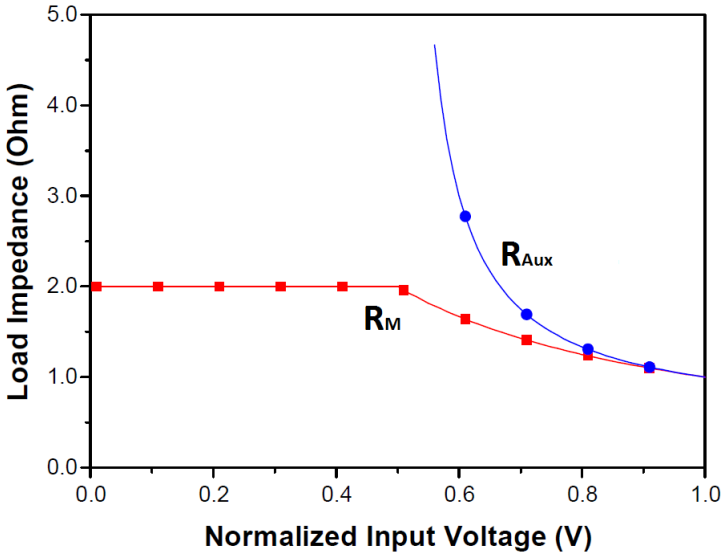

Figure 2.8: Fundamental load impedance of the main and the auxiliary amplifiers vs. normalized input voltage.

A typical DPA can be realized as the schematic shown in Fig. 2.10. In this figure $R_L = 25$ Ω and the quarter wavelength transformer of 50 Ω impedance has to be used to properly compensate the phase difference of the signals arising from the Main and Auxiliary amplifiers at the Doherty output. An alternative approach is to replace the

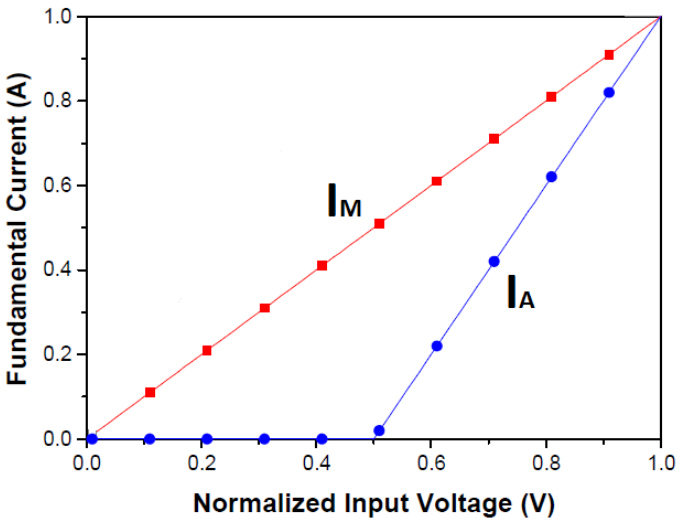

Figure 2.9: Current of the main and the auxiliary amplifiers vs. normalized input voltage.

power divider and the quarter wavelength transformer by a 3-dB 90-degree hybrid coupler. For the sake of linearity, the main amplifier is biased in class-B (class AB) and since the auxiliary amplifier should be kept off in the low power region of the DPA,it is normally biased in class-C.

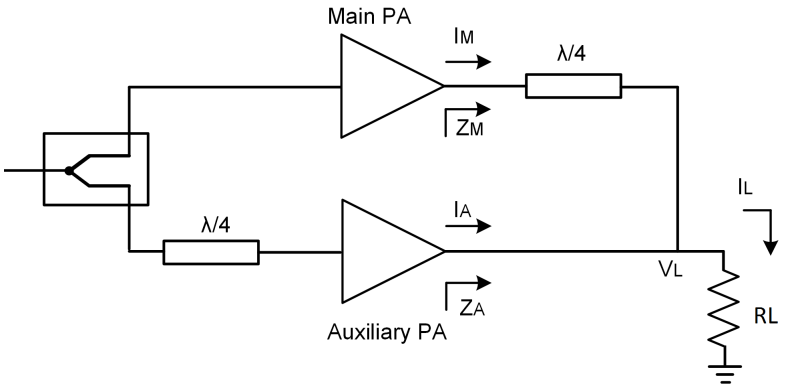

Figure 2.10: Typical DPA configuration.

Theoretical drain efficiency of DPA is depicted in Fig. 2.11. When the auxiliary amplifier is off, the main amplifier is loaded with 100 Ω. When the auxiliary is turned on, and hence conducting current, the load of the main amplifier decreases from 100 Ω to 50 Ω, while the impedance of the auxiliary decreases from infinity to 50 Ω. These performances are shown in Fig. 2.11 as "Low Power Region" and "Doherty Region" respectively.

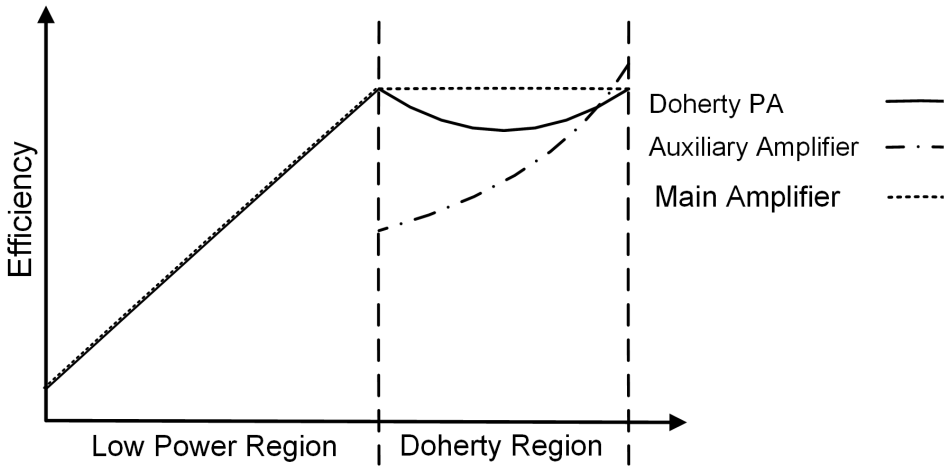

Figure 2.11: Theoretical drain efficiency of DPA.

It should be noticed that dividing of input power by two results a balanced DPA which corresponds to 6-dB OBO. If the input power is divided with different ratios, an unbalanced DPA is achieved. The effect of the balanced and unbalanced DPAs on total lineup efficiency is shown with Matlab simulation in the next chapter. In this chapter also, by using Matlab simulation, the effect of driver-stage on the total lineup efficiency will be assessed.

3

Matlab Simulation

3.1 Two-Stage Doherty Power Amplifiers

Power amplifiers can reach their maximum efficiencies only when they are driven at a certain input power level. Generally the available input power is far below the needed levels. Therefore, a driver stage is required to provide the desired input power for the PA.

3.1.1 Different Topologies

In this thesis, four different driver topologies for two-stage amplifiers are considered which are depicted in Fig. 3.1. Reffering to this figure, these topologies are as follows: (a) Cascaded class-AB and a DPA, (b) Two-stage cascaded DPAs, (c) DPA with embedded class-ABs and (d) DPA with embedded Doherty as drivers. For simplicity, these topologies in figures and tables are labeled as (a) Doherty + B, (b) Doherty + Doherty, (c) Doherty with em.B and (d) Dohery-em.DB. It is seen that the driver can consist of single-stage amplifiers (Class AB) as in (a) and (c) or of DPAs as in (b) and (d). In (c) and (d) the drivers are embedded. In topology (c) Class-AB amplifiers are inserted before the main and the auxiliary amplifiers. Topology (d) is the same as topology (c) but class-AB amplifiers are replaced by the Doherty power amplifiers. The purpose of the Matlab simulations are to investigate the efficiency vs. output power for all these different driver topologies.

3.2 Efficiency of Parallel and Series Amplifiers

Since the topologies consists of cascade and parallel configurations, first the efficiency of such configurations needs to be calculated. The efficiency of two parallel and cascaded amplifiers, as shown in Fig.3.1 and 3.2, can be written as

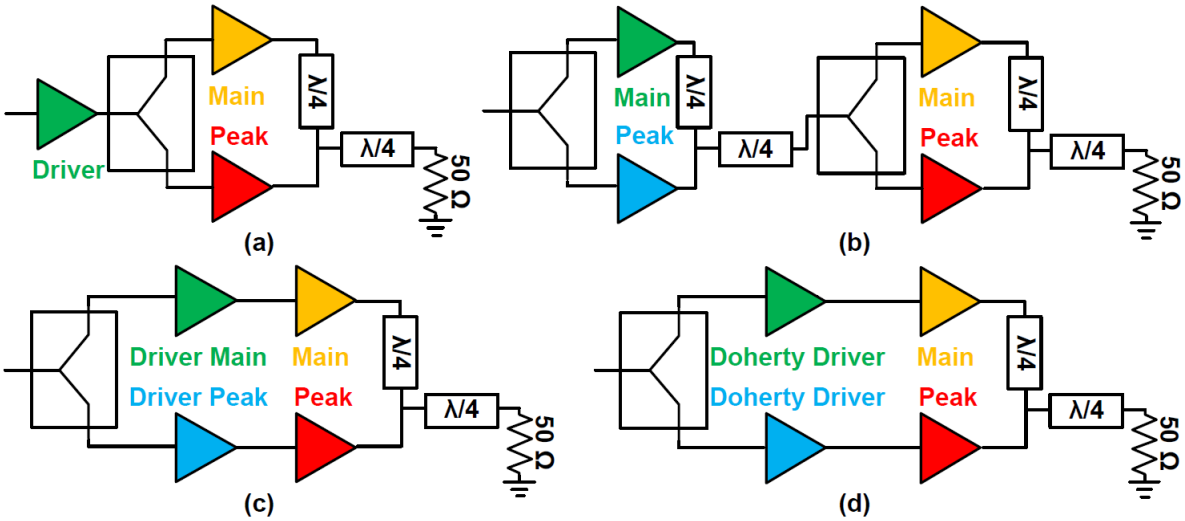

Figure 3.1: Driver topologies for two-stage power amplifiers.

$$\eta_{tot,P} = \frac{P_{out}}{P_{dc}} = \frac{P_{out}}{P_{dc1} + P_{dc2}} = \frac{P_{out}}{\frac{P_{out1}}{\eta_1} + \frac{P_{out2}}{\eta_2}} \tag{3.1}$$

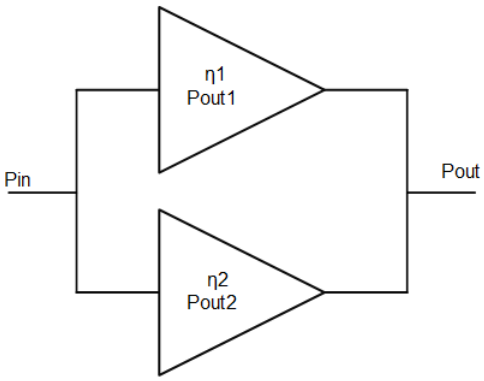

Figure 3.2: Schematic of a two-parallel amplifiers.

and the efficiency of two-stage cascaded amplifiers can be found as

$$\eta_{tot,C} = \frac{P_{out}}{P_{dc}} = \frac{P_{out}}{P_{dc1} + P_{dc2}} = \frac{P_{out}}{\frac{P_1}{\eta_1} + \frac{P_{out2}}{\eta_2}} = \frac{P_{out}}{\frac{P_{out}}{G_2\eta_1} + \frac{P_{out}}{\eta_2}} = \frac{\eta_1\eta_2}{\eta_1 + \frac{\eta_2}{G_2}} \tag{3.2}$$

The assumption used to derive (3.2) is that the two stages are perfectly isolated, so that their individual characteristics are maintained. In addition, the total efficiency is dependent on η_1, η_2 and the G_2 but not on G_1.

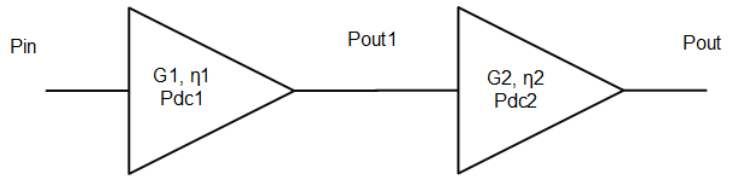

Figure 3.3: Schematic of a two-stage series amplifiers.

3.3 Matlab Codes Implementation

By calculating the efficiency of different classes (A, AB, B and C) as a function of output power, $\eta(P_{out})$, and using above equations, the efficiency of different driver topologies is simulated. Even though in the reality the gain of PAs varies with the output power, we assume that the gain is independent of the output power. Therefore these simulations qualitatively compare different topologies. In addition for the Doherty amplifiers we assume, for simplicity, that the main and the auxiliary amplifiers have the same gain. Finally since the x-axis of plots is the Output Back-Off (OBO), we normalize the maximum output power, where the maximum efficiency occurs, to 1 W.

Simulations start with the decomposition of topologies shown in Fig. 3.1 into cascade and parallel configurations (Fig. 3.2 and 3.3). For cascaded structure, we need to know the efficiency of both stages and the gain of the second stage and for the parallel structure, the output power and the efficiency of both are required. For example, topology (a) is a two-stage amplifier where the second stage is made up of two parallel amplifiers. To find the total efficiency by (3.2), it is needed to calculate the efficiency of each stage as a function of the output power and have the gain of the second stage. The first stage is a simple class AB and its efficiency as a function of its output power is calculated (Fig. 2.5). Since the second stage consists of two parallel amplifiers, its efficiency can be calculated by (3.1). To use this equation, it is needed to evaluate how its output power is divided between the two amplifiers and since these amplifiers are class AB and C, by having their output power their efficiencies can be achieved. The only factor in (3.2) which is left is the gain. As mentioned before we assume it is independent of the output power and therefore assume it as a constant value.

The embedded topologies (c) and (d) consist of two cascaded amplifiers in the main and auxiliary branches which are parallel to each other. Since we assume a symmetric case, when the output power is more than 6-dB below the maximum value, the auxiliary branch is turned off. Therefore we have only two cascaded amplifiers and (3.2) provides the efficiency in terms of output power. If the output power is higher than 6-dB below the maximum output power, the amplifiers in the auxiliary branch start to turn on. Therefore we face two parallel branches each of which have two cascaded amplifiers. By using (3.2) we can calculate the efficiency of each line separately. Finally, the efficiency of two parallel PA branches are calculated by (3.1).

3.4 Simulation Results

The topologies (a) and (c) have the almost same PAE in the Doherty region. However, in the low power region, it can be shown that $P_{DC,driver}$ is $2P_{out}/[G_{main}\eta(2P_{out}/G_{main})]$ and $2P_{out}/[G_{main}\eta(P_{out}/G_{main})]$ for topology (a) and (c) respectively. Therefore, in the low power region, the drivers in topology (c) consume more DC power and therefore its efficiency is lower than that of topology (a). Since in our study the main focus is on the Doherty region, in the MATLAB simulations , for simplicity, we assume that topology (a) and (c) have the same efficiency. Fig. 4.29 shows the efficiency behavior of these two topologies in terms of output power.

Four different efficiency comparison studies have been done. The studies are based on different final gain (G_{final}), different driver and final-stage's efficiencies, either 6-dB or 9-dB OBO for driver and final stages, and finally the loss for dividers. These classifications are explained in detail in the next sections.

3.4.1 Efficiency Comparison of Different Topologies based on Different Final Stage Gain

Fig. 3.4 and table 3.1 show the simulation results of different driver topologies based on a constant final-stage's gain. It can be seen that a higher gain can provide a higher total efficiency since it can reduce the effect of driver stage efficiency on the total efficiency (3.2). In addition, with increasing the value of the G_{final}, topologies perform similarly and Two-stage cascaded Doherty power amplifiers has the highest efficiency at 6-dB OBO. Furthermore, from table 3.1 we can see that at low gain the difference between efficiency of these topologies at 6-dB OBO increases.

Table 3.1: Efficiency at 6-dB OBO at different final-stage gain Fig. 3.4

Top. Type	η_{total} (G_f=7dB)	η_{total} (G_f=10dB)	η_{total} (G_f=13dB)	η_{total} (G_f=16dB)
Doherty+B	55%	65%	71%	74%
Doherty+Doherty	65%	70%	75%	76%
Doherty with em.B	55%	65%	71%	74%
Doherty-em.DB	60%	68%	73%	75%

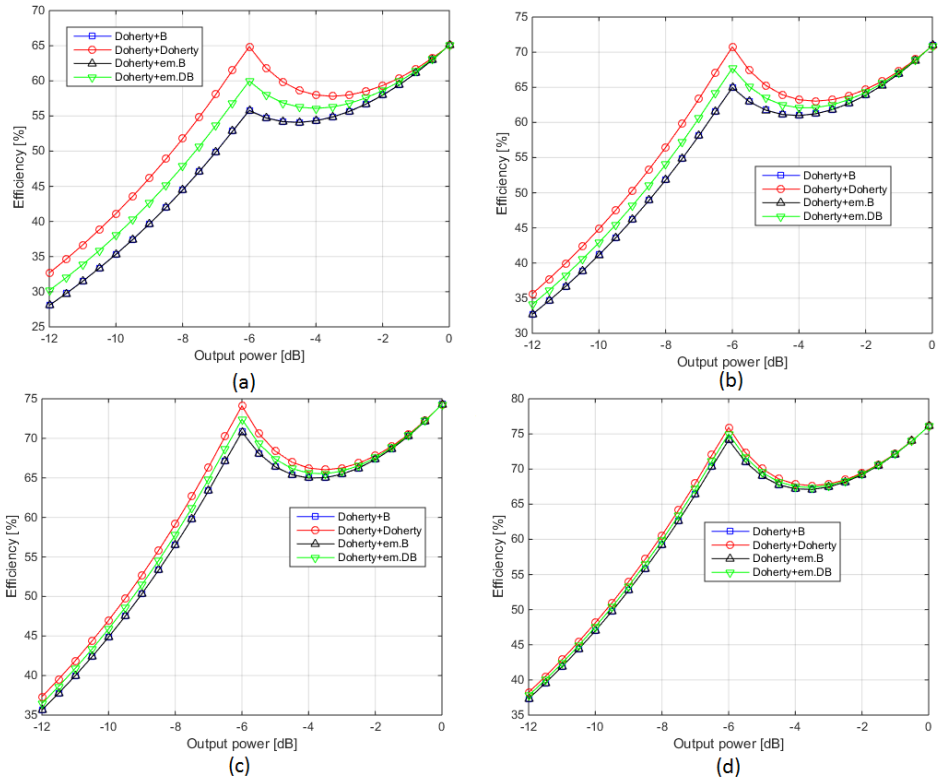

Figure 3.4: Comparison of different topologies. Both main and driver have maximum efficiency of 78 %, (a) G_{final}=7 dB, (b) G_{final}=10 dB, (c) G_{final}=13 dB, (d) G_{final}=16 dB.

3.4.2 Effect of Various Driver and Final-Stage Efficiencies on the Total Efficiency of Different Topologies

Since all the amplifiers in practice do not have the efficiency of 78.5%, therefore in this part it has been tried to simulate the different topologies based on different driver and final-stage efficiencies to see how they could perform in reality. In addition, for all the topologies a constant final-stage gain of 10 dB is considered. Fig. 3.5 assesses the effect of driver stage efficiency on the total efficiency. Generally if the gain of the final-stage is high enough (e.g. G = 10 dB), the total efficiency is mainly dictated by the final-stage efficiency. For example in Fig. 3.5 (a) Doherty+B and (b) Doherty+Doherty , the final-stage has the maximum efficiency of 50 % and the total efficiency is almost the same even with different driver-stage efficiencies. However, if the driver efficiency is too low, the total efficiency of the amplifier can be reduced considerably. For example in Fig. 3.5 (c) Doherty with em.B and (d) Doherty+ em.DB, the final-stage amplifiers have maximum efficiency of 78 %, but the drivers have different maximum efficiency of 30 % and 50 % respectively. The total efficiency in (d) Doherty+ em.DB is about 5 %

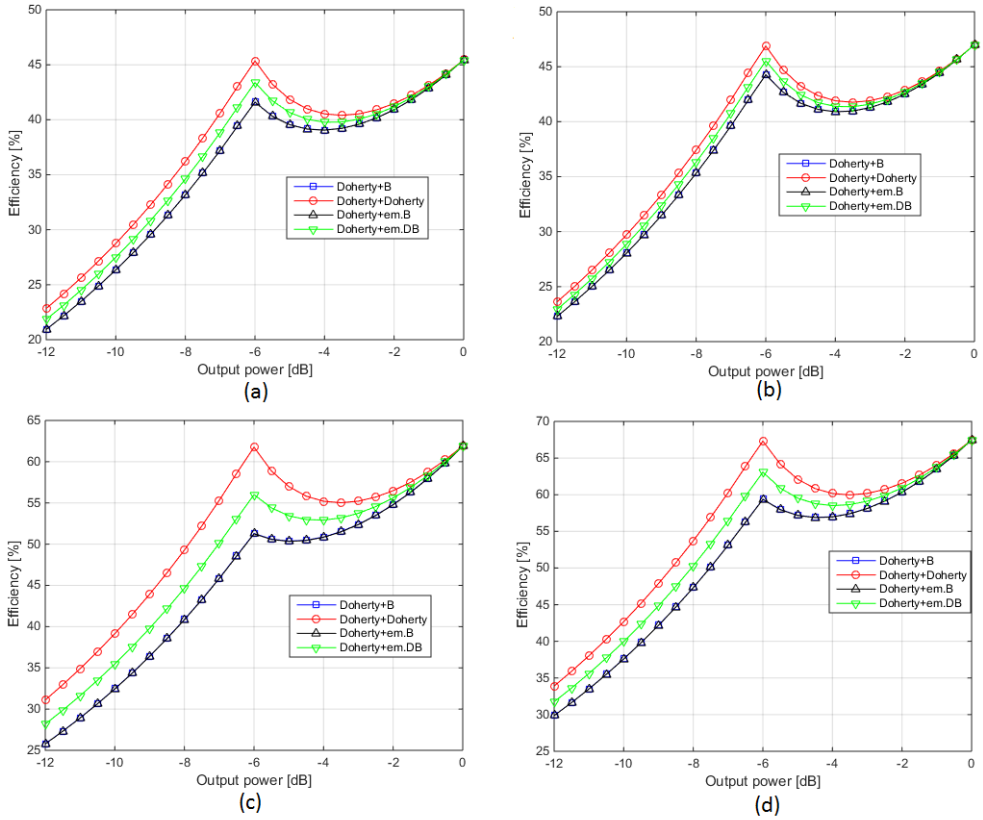

Figure 3.5: (a) η_{driver} = 50 %, η_{final} = 50 %,(b) η_{driver} = 78 %, η_{final} = 50 %,(c) η_{driver} = 30 %, η_{final} = 78 %,(d) η_{driver} = 50 %, η_{final} = 78 % (G=10dB).

higher than that of (c) Doherty with em.B. In addition, from table 3.2 it is seen that the cascaded class-AB and DPA topology has the highest difference between efficiencies at the peak and 6-dB OBO and two-stage cascaded DPAs has the lowest difference values.

Table 3.2: Efficiency at peak and 6-dB OBO for different topologies described in figure 3.5

Driver/Final Stageη(%)	Doherty+B	Doherty+Doherty	Doherty with em.B	Doherty-em.DB
50%/50%	45%/42%	45%/45%	45%/42%	45%/43%
78%/50%	47%/44%	47%/47%	47%/44%	47%/46%
30%/78%	63%/52%	63%/63%	63%/52%	63%/55%
50%/78%	68%/60%	68%/68%	68%/60%	68%/63%

3.4.3 Efficiency Comparison of Different Topologies based on Various OBO for Driver and Final Stages

In this section the effect of different OBOs of driver and final-stage has been investigated. Fig. 3.6 show the efficiency of different Doherty configurations. In the topologies of this section an unbalanced power splitter is used. Therefore the input power doesn't divided equally between the main and auxiliary amplifiers [10]. In Fig. 3.6 (a) and (c), the driver-stage has an OBO of 9-dB while in Fig. 3.6 (b) and (c), the final-stage has an OBO of 9-dB. It is seen that the OBO of the total amplifier is governed by the final-stage OBO. In addition, by comparing Fig. 3.6 (b) and (c), it is seen that in order to have an OBO of 9-dB, it is more beneficial in terms of efficiency to use a driver with a 9-dB OBO as well.

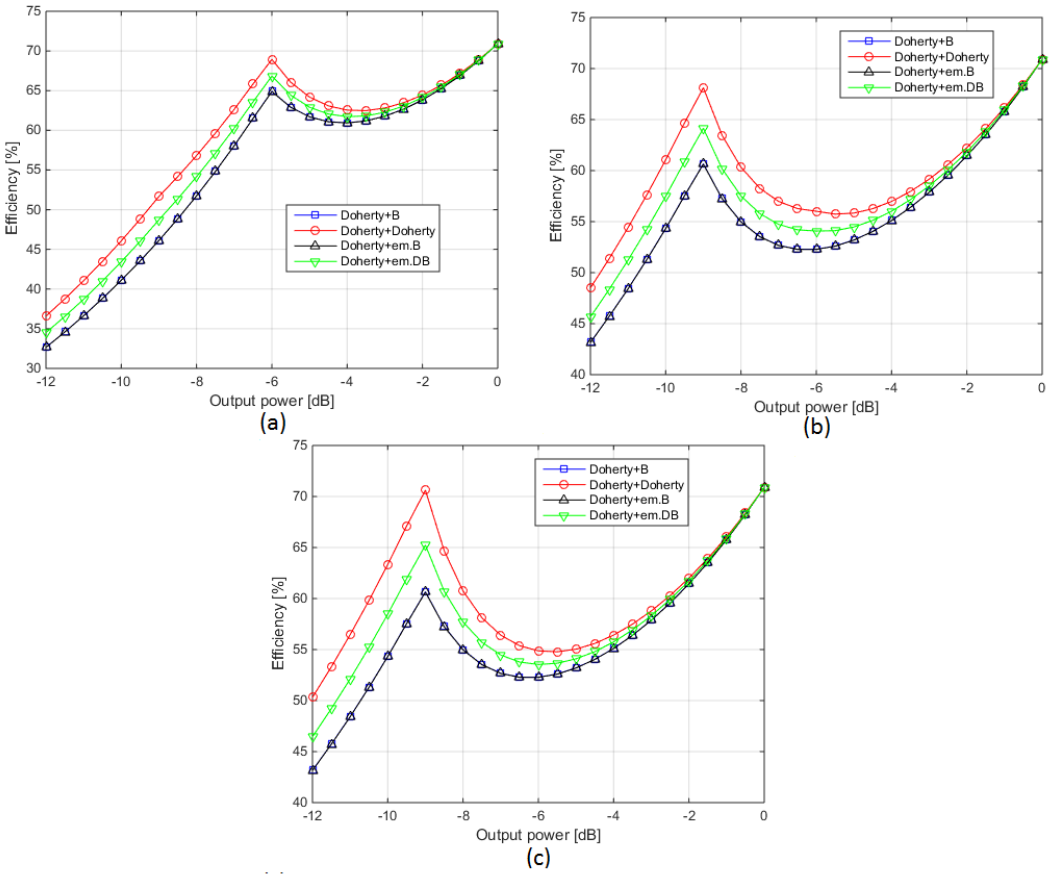

Figure 3.6: (a) OBO_{driver} = 9-dB , OBO_{final} = 6-dB, (b) OBO_{driver} = 6-dB , OBO_{final} = 9-dB, (c) OBO_{driver} = 9-dB , OBO_{final} = 9-dB.

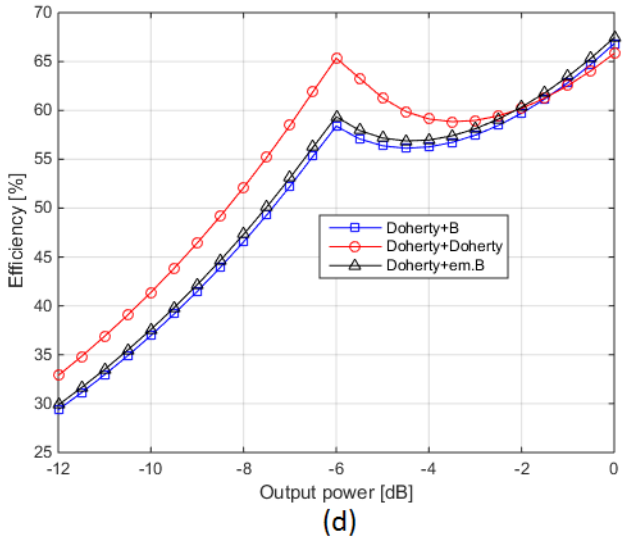

Figure 3.7: Efficiency of different driver topologies on Doherty amplifiers with considering 0.3 dB loss for the divider

3.4.4 Effect of Divider Loss on the Efficiency of Different Topologies

Finally, the effect of losses in the power divider are investigated by Matlab simulations. In simulations a gain of 10 dB is considered and the input power in all the topologies is divided equally. Fig. 3.7 shows the results of the different topologies at peak and 6-dB OBO. Even though, at the OBO the two-stage cascaded Doherty power amplifier has the highest efficiency, due to the more loss in this topology, at peak it exhibits a lower efficiency.

3.4.5 Overall Conclusion on the Efficiency of Different Topologies

Generally having Doherty configurations in both driver and final-stage results in a high efficiency in the total Doherty region. The embedded Doherty has a little lower efficiency compared to the cascaded Doherty topology. One possible reason can be that when the auxiliary amplifier is off, the corresponding driver consumes DC power. Hence, the cascaded two-stage Doherty provides the highest efficiency. This will be verified in the next chapter by designing real PAs.

4

Two-Stage Power Amplifier Design and Simulations

In this chapter, the four topologies will be designed, simulated and finally compared using the real device models in ADS. To do this, a final-stage amplifier and its driver are designed at Band-I (2.11-2.17GHz). The aim is to achieve a 100 W (50 dBm) output power and find the best driver topologies in the Doherty configuration which gives the highest efficiency. The design process starts with DC simulations and all the next steps will be explained in details.

4.1 Bias Point

The amplifier class (A, AB, B or C) determines the characteristics of the amplifier such as gain, output power, efficiency and linearity. Since the aim is to get high efficiency as well as good linearity, the amplifiers are biased in deep class AB (Chap.2.1). Two GaN-HEMT transistors, CGH40010F and CGH40045F, are used for the driver and the final-stage amplifiers respectively. Fig. 4.2 and 4.1 show the DC characteristics of these transistors. The bias current is selected to be 5% of the maximum drain current which results in 170 mA and 300 mA for the driver and the final-stage amplifiers respectively.

4.2 Device Characterization

4.2.1 Source/Load-Pull Results

As can be seen in Fig 4.2, the transistor knee voltage, V_k, is about 5 V and $\chi = V_k/V_{DS}$ = 0.18. Therefore, if we use TL operating mode, the efficiency in class AB will be limited to 64 % ($78\times(1-\chi)\%$). As mentioned in the last chapter, by using harmonic tuning

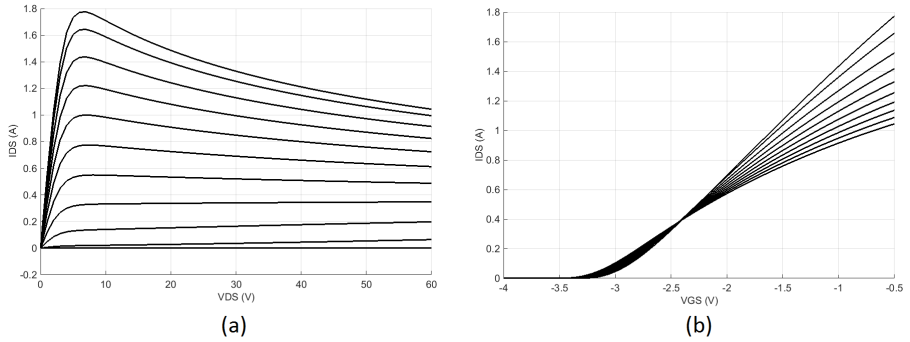

Figure 4.1: Output (a) and transfer (b) characteristics of the driver stage transistor

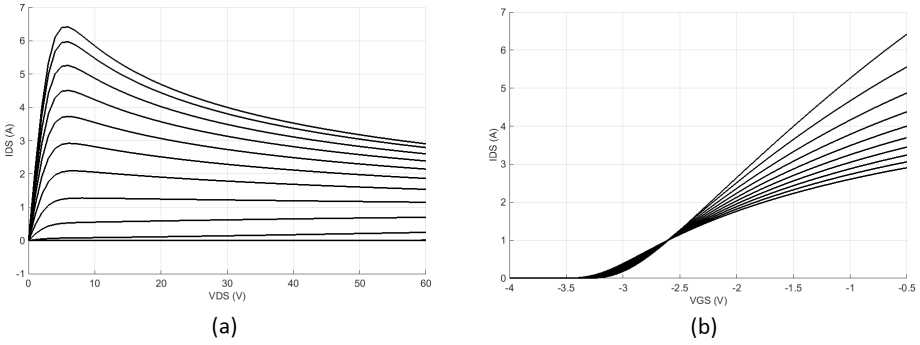

Figure 4.2: Output (a) and transfer (b) characteristics of the final stage transistor

the efficiency can be enhanced. For that purpose we use Load-Pull and Source-Pull simulation technique to find proper impedances at different harmonics.

The process starts with the load-pull simulation on fundamental frequency. All the harmonic terminations in load and source are kept at 50 Ω. After finding proper load impedance, we use it in source-pull simulation for getting proper source impedance. We repeat this process until reach to an acceptable level of PAE and output power. For high order harmonics, impedance optimization is used to achieve desired PAE and output power. For the termination of high order harmonics, especially for the 2^{nd} harmonic, there are regions in the smith chart that can severely degrade PAE. Hence, the sensitivity of high order harmonic terminations is needed to be checked in order to avoid performance drop due to slightly change in harmonics impedance. This process is repeated for several frequencies. Table 4.1 shows the load-pull and source-pull simulation results for the final-stage amplifier. The input power for the driver and the final-stage amplifier are 27 and 35 dBm respectively. An output power of 42 dBm, gain of 15 dB and PAE of 80 % for the driver-stage amplifier is achieved. In addition the final-stage amplifier has an output power of 48 dBm, gain of 13 dB and PAE of 78 %.

As mentioned in the latter paragraph, the matching networks for the high order

Table 4.1: Load-Pull, Source-Pull simulation results for the final-stage amplifier (P_{in}= 35 dBm)

Freq(GHz)	P_{out}(dBm)	G(dB)	PAE(%)	$Z_S(\Omega)$	$Z_L(\Omega)$	$Z2f_s(\Omega)$	$Z2f_L$ (Ω)	$Z3f_L$ (Ω)
2	48	13	75.6	$3.7-j*7.3$	$5.3-j*0.4$	$3+j*1e3$	$2-j*1e3$	$2-j*23$
2.1	48.2	13.2	77	$3.5-j*2.6$	$5-j*0.7$	$2.5-j*1e3$	$4.9+j*1e3$	$2-j*41.5$
2.15	47.8	12.8	77.8	$3.7-j*2.9$	$4.7-j*0.7$	$2.8+j*31.6$	$10-j*1e3$	$2-j*78$
2.2	47.8	12.8	79.4	$3.8-j*4.9$	$5.2-j*0.5$	$6.5-j*29$	$156-j*1e3$	$23+j*1e3$
2.3	47.8	12.8	77.6	$3.1-j*5.9$	$5.2-j*0.6$	$7-j*1e3$	$4-j*1e3$	$2.9+j*1e3$

Table 4.2: Load-Pull, Source-Pull simulation results for the driver-stage amplifier (P_{in}= 27 dBm)

Freq(GHz)	P_{out}(dBm)	G(dB)	PAE(%)	$Z_S(\Omega)$	$Z_L(\Omega)$	$Z2f_s(\Omega)$	$Z2f_L$ (Ω)	$Z3f_L$ (Ω)
2	42	15	80	$6.3+j*3$	$18+j*12$	$3-j*1e3$	$6+j*200$	$24+j*189$
2.15	41.6	14.6	79.4	$7+j*3$	$15.4+j*12$	$150-j*1e3$	$4.8-j*1e3$	$2.8+j*23$
2.2	41.3	14.3	78.3	$7-j*0$	$15.5+j*15$	$63-j*1e3$	$4.3+j*1e3$	$7+j*1e3$
2.3	41.4	14.4	78	$6.5-j*1.6$	$14.2+j*12$	$1e3-j*1e3$	$2.6-j*1e3$	$3+j*1e3$

harmonics does not necessarily need to provide the same impedances obtained from load pull/source pull simulations. By sweeping the phase of the harmonics at the periphery of the smith chart, some investigations have been done on the effects of the harmonics. Based on these investigations, we should get terminations which are not in the sensitive area. For example Fig. 4.3 shows the sensitivity of the PAE with respect to the phase of the 2^{nd} and 3^{rd} harmonic load terminations. As can be seen the phase of the load termination at the 2^{nd} harmonic should not be in the range of $170-300^o$. Fig. 4.4 also shows the sensitivity of the second harmonic of the source. As it can be seen, the phase of the source termination should not be in the range of $0-150^o$.

For the driver-stage amplifier, the linearity is very important. The reason is that the

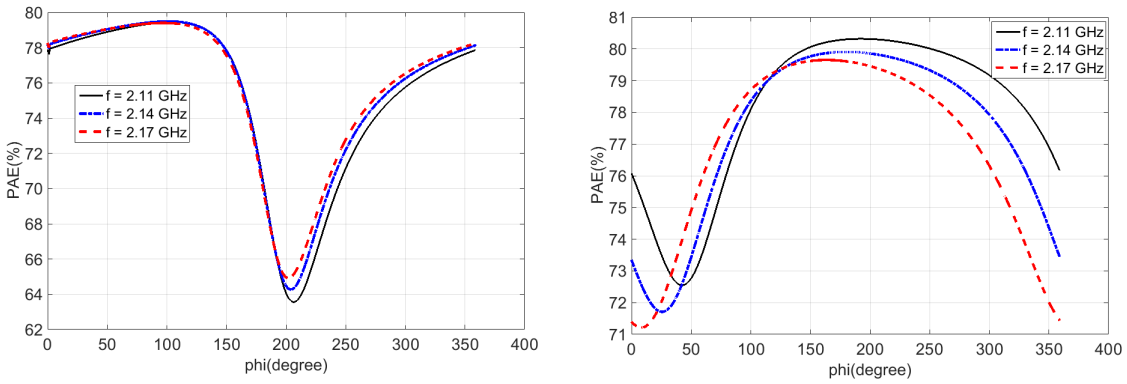

Figure 4.3: Sensitivity of the PAE with respect to the phase of the second and third harmonic load termination(impedances are based on the values of the table 4.1)

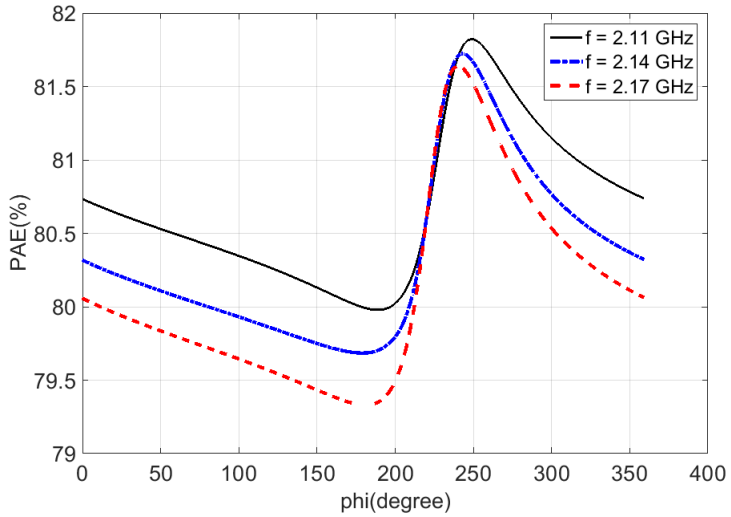

Figure 4.4: Sensitivity of the PAE with respect to the phase of the second harmonic source termination (impedances are based on the values of the table 4.1)

transferred signal from the driver amplifier to final-stage should be without distortion. Therefore, the driver-stage is designed at a higher output power level (41 dBm) but it is driven at lower power (35 dBm) in order to be in the linear region. Table 4.2, shows the Load-Pull source-Pull simulation results for the driver-stage.

4.3 Matching and Bias Networks

Matching networks are needed to realize the desired impedances. For the source network, fundamental and 2^{nd} harmonic and for the load network, fundamental, 2^{nd} and 3^{rd} harmonics should be taken into account. Fig. 4.5 shows the topology of the amplifiers. It should be noticed that minor changes has been done on the mentioned topology, when the layout is designed. For the source matching, both fundamental and 2^{nd} harmonic should be matched simultaneously. The 2^{nd} harmonic matching is provided by a shorted stub ($\lambda/4$ at f_o) and a transmission line at the gate of the transistor. The stub allows to have a short-circuit at the 2^{nd} harmonic before the transmission line. Hence, by adding the rest of the matching network, 2^{nd} harmonic matching will not be affected. The two open stubs and transmission lines are used for a wide-band matching at the fundamental frequency. For the load matching, the same procedure is used. However, after matching the 2^{nd} harmonic, the 3^{rd} harmonic is needed to be matched as well. An open stub ($\lambda/4$ at $3f_o$) is used to avoid disrupting the matching of the 3^{rd} harmonic while matching the fundamental.

Fig. 4.6, 4.7, 4.8 and 4.9 show impedances of the source and load matching networks for the final-stage amplifier and driver-stage amplifier at 2.11-2.17 GHz. From the figures, it can be seen that fundamental harmonics from design is almost the same as the values

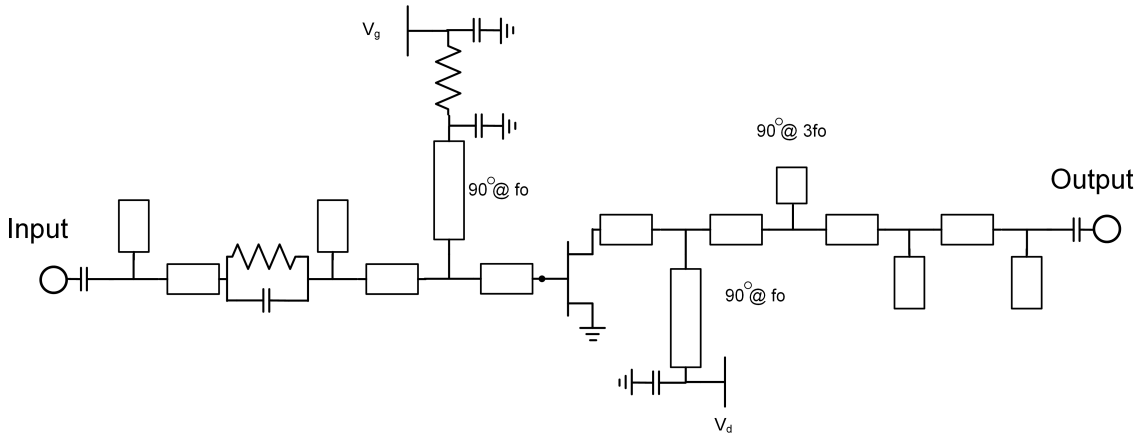

Figure 4.5: Topology of the final-stage and driver-stage amplifier at 2.11-2.17 GHz

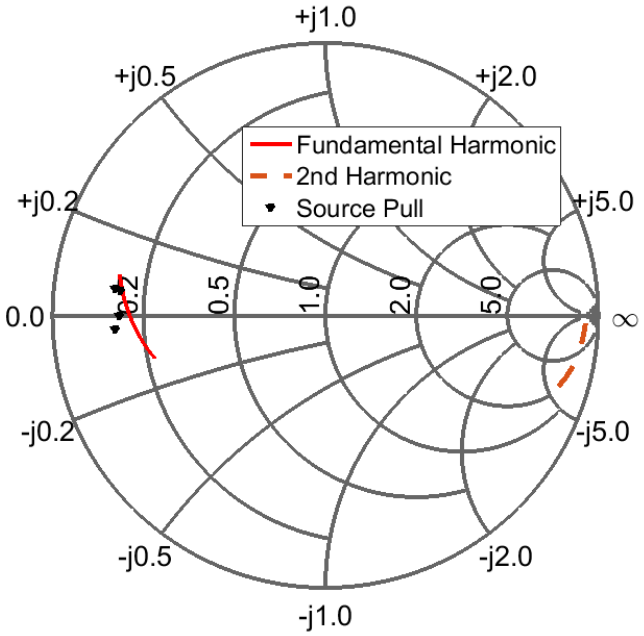

Figure 4.6: Fundamental and second harmonic impedance of driver-stage source matching network

from load-pull and source-pull simulations. Also comparing of Fig. 4.3, 4.4 and Fig. 4.6, 4.7, 4.8 and 4.9 shows that the second and third harmonics are not in the their sensitive area and therefore the total efficiency won't decrease by their current position.

In addition, it is seen that bias voltages are applied via two stubs which are used for the 2^{nd} harmonic matching. The capacitors are used to provide RF grounds at the bias sources.

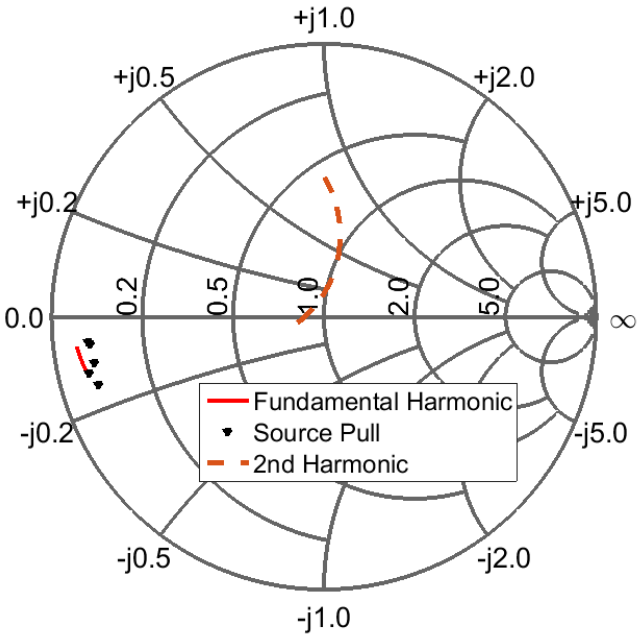

Figure 4.7: Fundamental and second harmonic impedance of final-stage source matching network

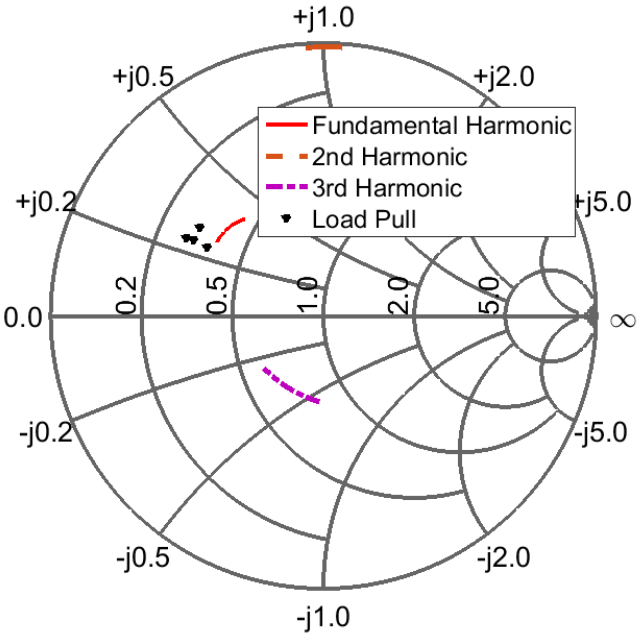

Figure 4.8: Fundamental, second and third harmonic impedance of driver-stage load matching network

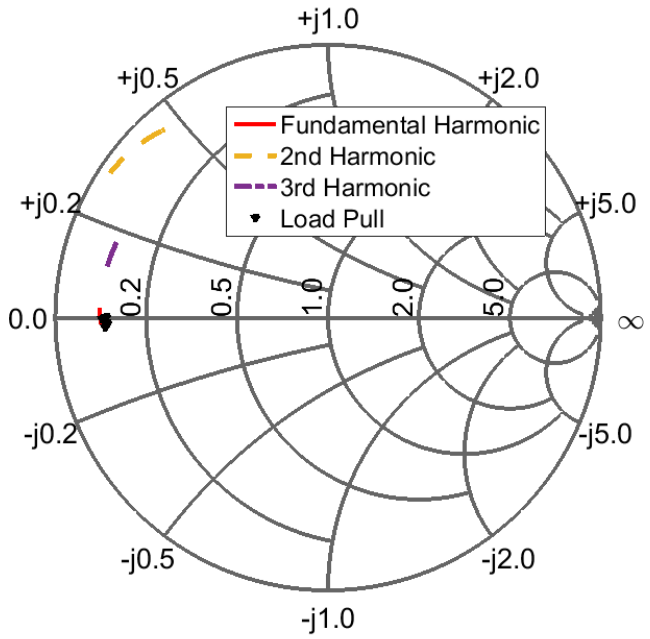

Figure 4.9: Fundamental, second and third harmonic impedance of final-stage load matching network

4.4 Small Signal Gain and Stability

Driver and the final-stage amplifiers are stabilized separately. It should be noticed that the total stability of amplifiers must be fulfilled not only in the operating band but also for all frequencies; specially for the lower frequency which oscillations can be occurred due to the higher gain. For low frequency stabilizing, a resistor and a capacitor are added to the gate biasing networks. However, for in band stabilization, the RC network should be inserted in the source matching network (Fig. 4.5). In addition, it is more effective to put the RC network more closer to the gate of the transistor. Stability conditions are verified based on the either Rollet factor, K, [19, 20] or μ [21]. Figure 4.10 and 4.11 show the gain, return loss and the stability of the driver and the final-stage amplifiers respectively. As can be seen, both the driver and final-stage have the small signal gain of 19 dB. In addition, from S_{11}, both stages have a low return loss (5 dB). This is because the design is based on a large signal simulation and the aim is to achieve the highest PAEs. This is done by matching the source impedance to the values obtained from the source-pull simulations. Fig. 4.12 shows the source-pull contour plot of the large signal $|S_{11}|^2$ at 2.15 GHz for P_{in}= 35 dBm. The inner contour corresponds to $|S_{11}|^2$=-18 dB and the outer contour where the source impedance is located corresponds to $|S_{11}|^2$=-6 dB. Since the $|S_{11}|^2$ increases rapidly by moving away from the optimum point (maximum output power), the selected source impedance (maximum PAE) doesn't show a good match even in the large signal. Furthermore, the stability K factors for

both stages indicate that the amplifiers are unconditionally stable not only in the design band but also in the lower frequencies where the transistors have the highest gain.

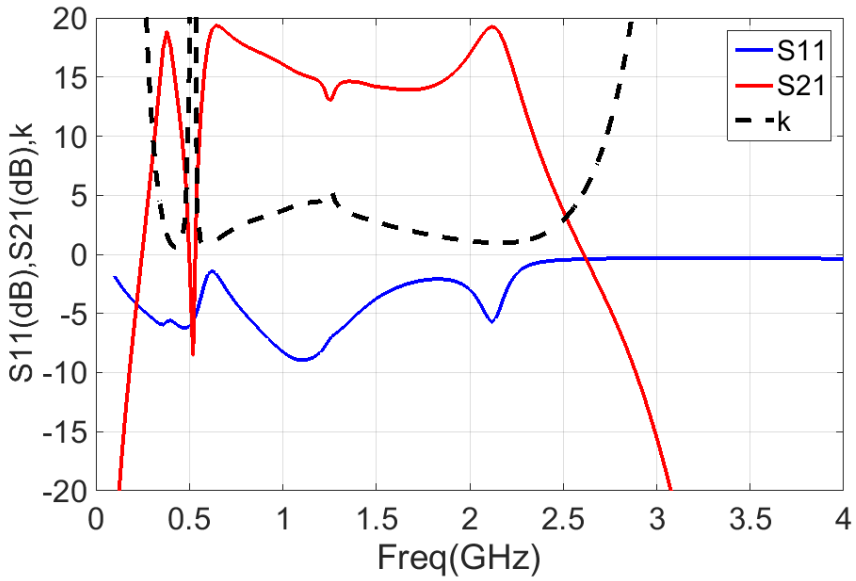

Figure 4.10: Gain, return loss and stability factor of the driver-stage amplifier

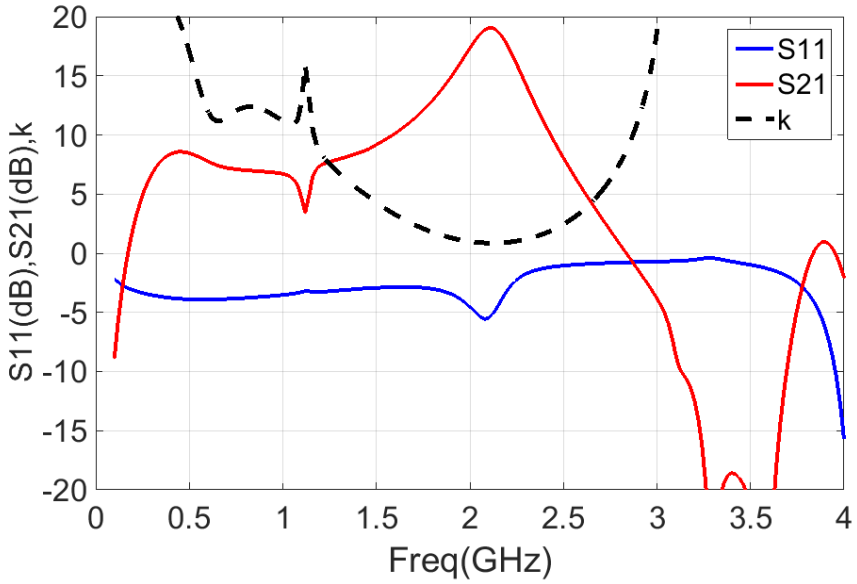

Figure 4.11: Gain, return loss and stability factor of the final-stage amplifier

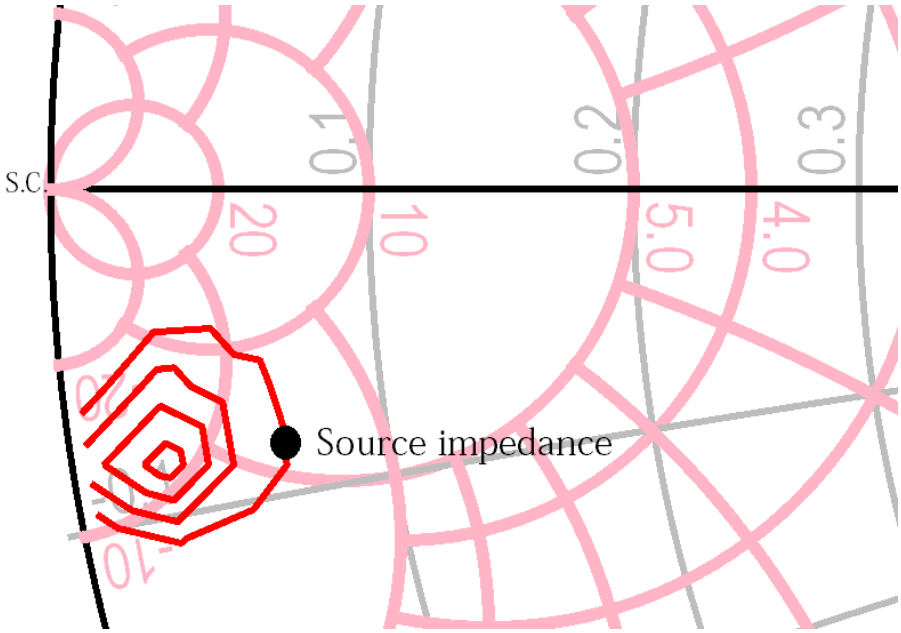

Figure 4.12: Source-pull contour plot of the large signal $|S_{11}|^2$ at 2.15 GHz for P_{in}= 35 dBm. The inner contour corresponds to $|S_{11}|^2$=-18 dB and the outer contour where the source impedance is located corresponds to $|S_{11}|^2$=-6 dB.

4.5 Layout

Fig. 4.13, 4.15 show the load and the source matching networks of the driver amplifier. In these matching networks, stubs and transmission lines are used for matching at the fundamental, second and third harmonics. In the Fig. 4.13, the RC networks in the gate bias and the main lines are for the stabilizing of the low frequencies and the in band frequencies respectively. In addition, several capacitors in the gate bias are used for forming the RF ground at the gate bias point and coupling capacitors are used in the main line to avoid the DC current flow to the source. The load matching network has a coupling capacitor and bypass capacitors as well. Fig 4.14 and 4.16 show the layout of the final-stage amplifier. These networks have the same structure as the driver-stage layout.

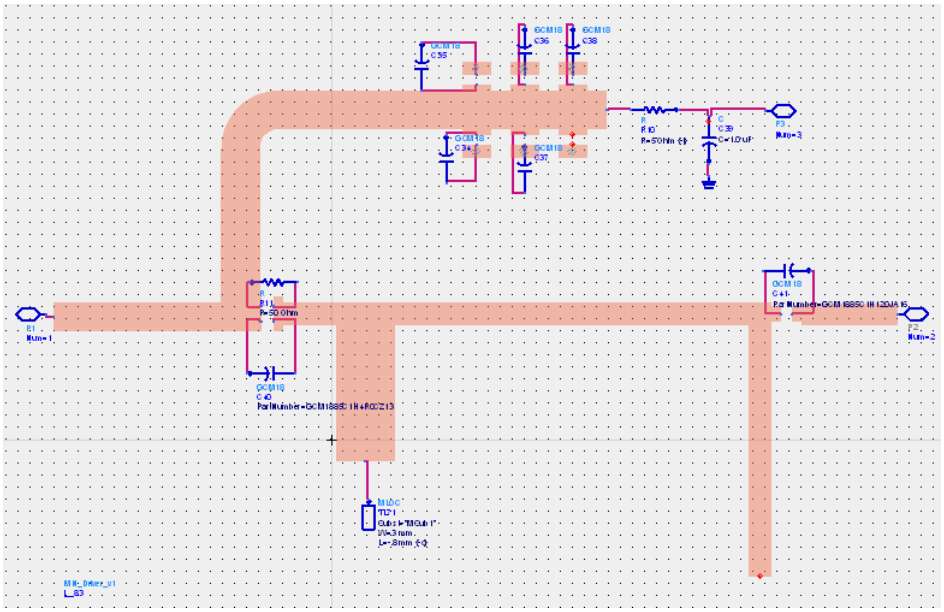

Figure 4.13: Layout of the source matching network of the driver-stage amplifier

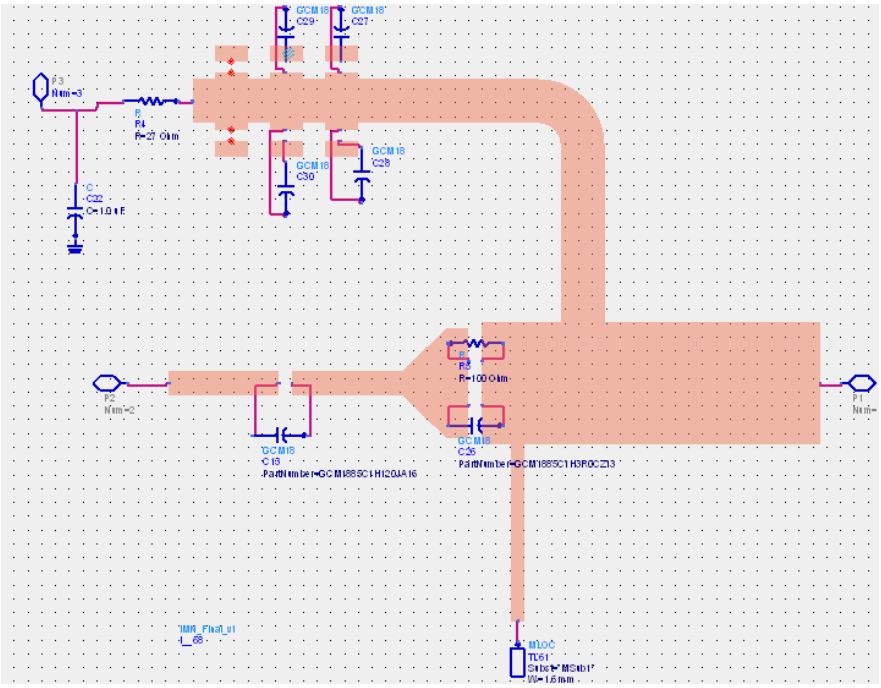

Figure 4.14: Layout of the source matching network of the final-stage amplifier

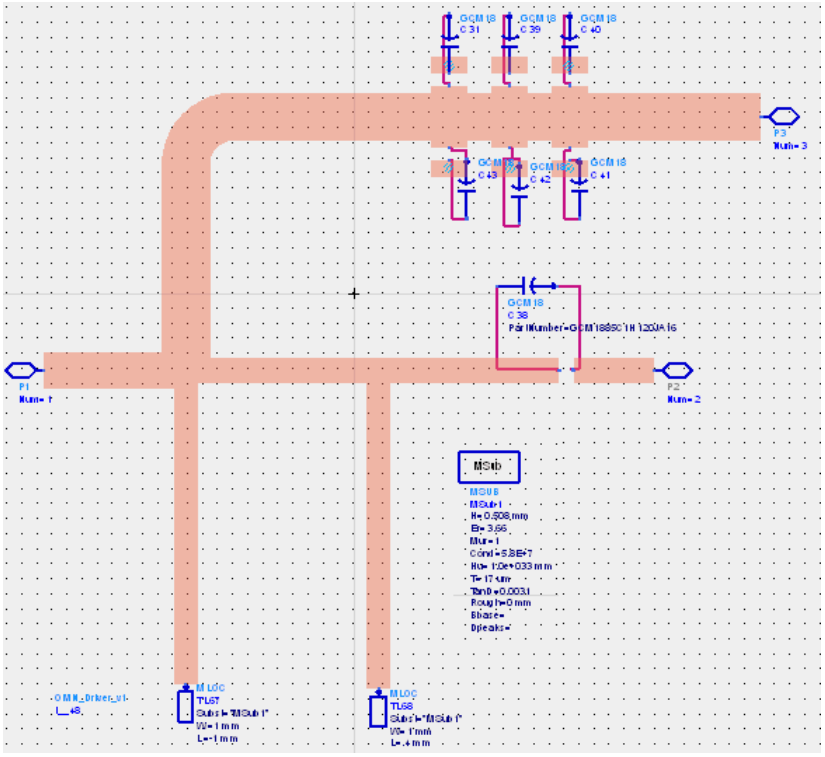

Figure 4.15: Layout of the load matching network of the driver-stage amplifier

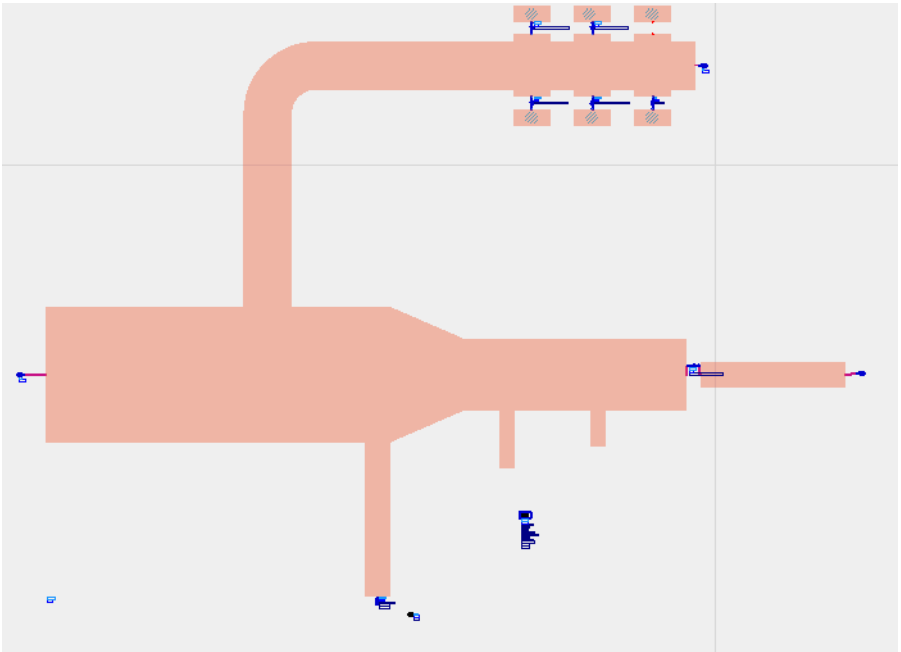

Figure 4.16: Layout of the load matching network of the final-stage amplifier

4.6 Large Signal Simulation Results

4.6.1 Final-stage and Driver-stage amplifiers

After matching networks are designed, the length and width of the transmission lines and stubs should be tuned or optimized in a way to provide the best results for PAE, output power and gain. Fig 4.17 shows the ADS schematic of the final-stage amplifier. In order to achieve a design which is less sensitive to the fabrication errors, the aim is to get a flat frequency response. Fig. 4.18, 4.19, 4.20 and 4.21 show the simulation results of the final-stage and the driver-stage amplifiers in terms of frequency and input power respectively. In the design band (2.11-2-17 GHz), the driver amplifier has a gain of 13.5-14 dB for P_{in}= 27 dBm and PAE of 70-74%. The final-stage amplifier exhibits a gain of 12.3-12.7 dB for P_{in}= 35 dBm in the design band and PAE of 76-77%. From Fig.4.20 it is seen that at P_{in}= 27 dBm and f=2.14 GHz, the driver amplifier reaches its maximum output power with a gain of 16 dB. At this point PAE of 75% is achievable. Fig. 4.21 shows that the final-stage amplifier reaches its maximum output power at P_{in}= 35 dBm. At this input power level, the amplifier provides a gain of 14dB and PAE of 75%.

After designing of the amplifiers based on the ADS models, the momentum simulations has been done. It is because the ADS models don't take into account the coupling effects between the different adjacent elements.

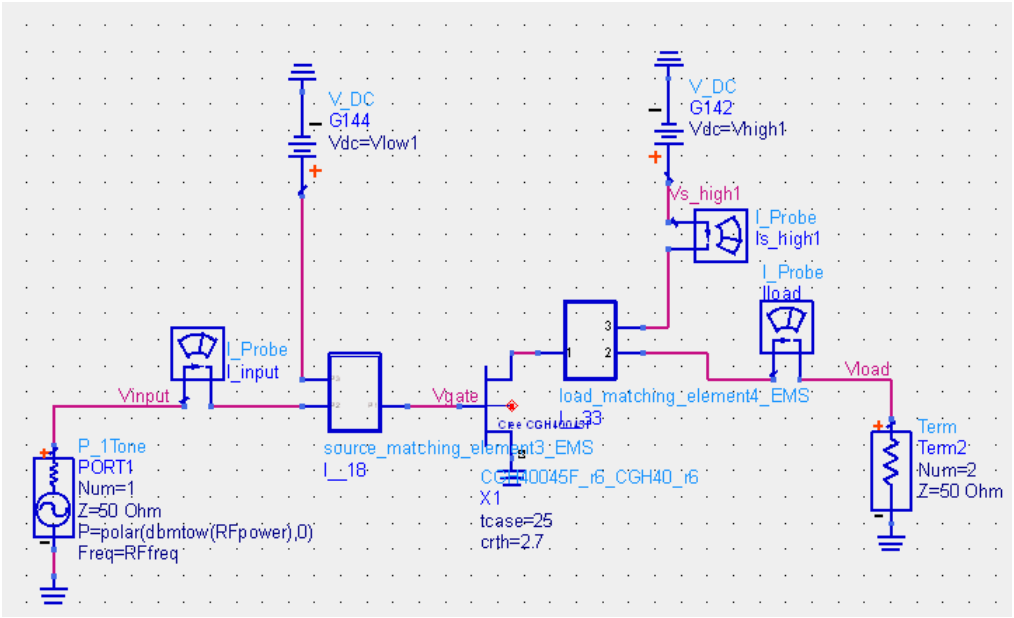

Figure 4.17: Schematic of the driver and the final-stage amplifier

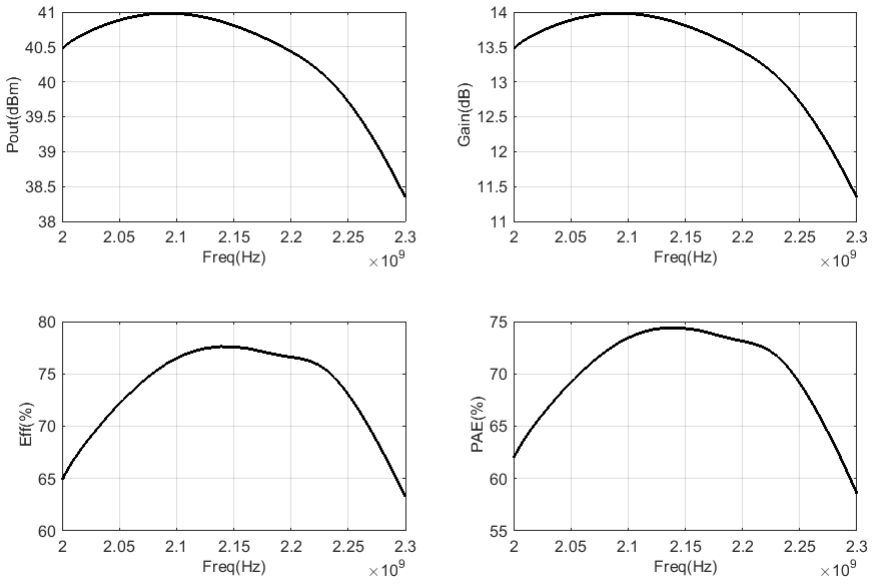

Figure 4.18: Driver-stage amplifier simulated characteristic (design band: 2.11-2.17 GHz, p_{in}=27dBm)

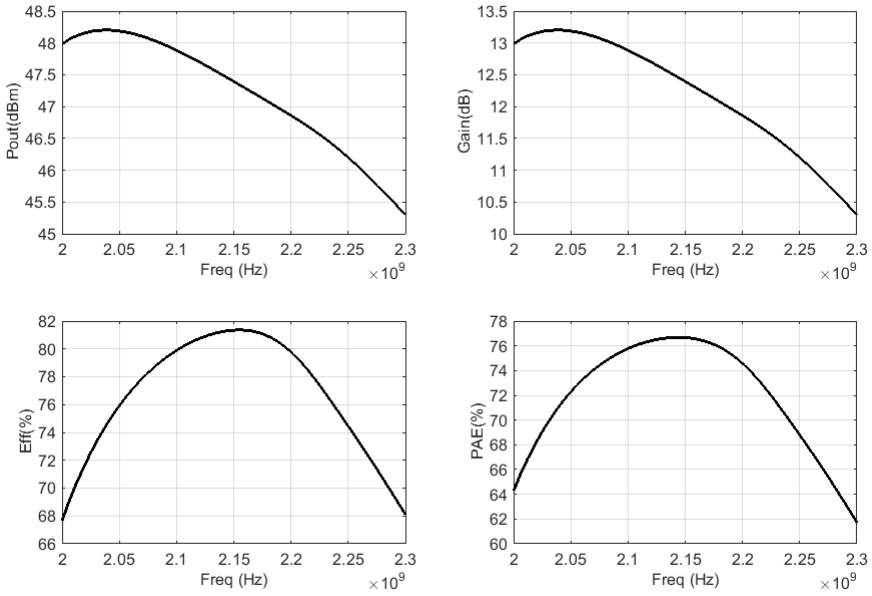

Figure 4.19: Final-stage amplifier simulated characteristic (design band: 2.11-2.17 GHz , p_{in}=35dBm)

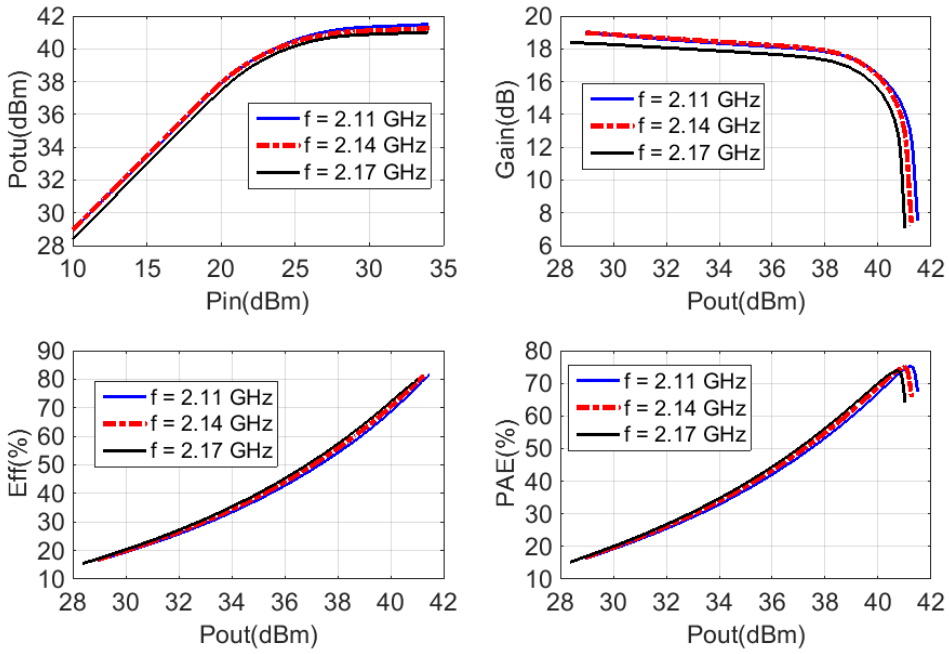

Figure 4.20: Driver-stage amplifier simulated characteristic

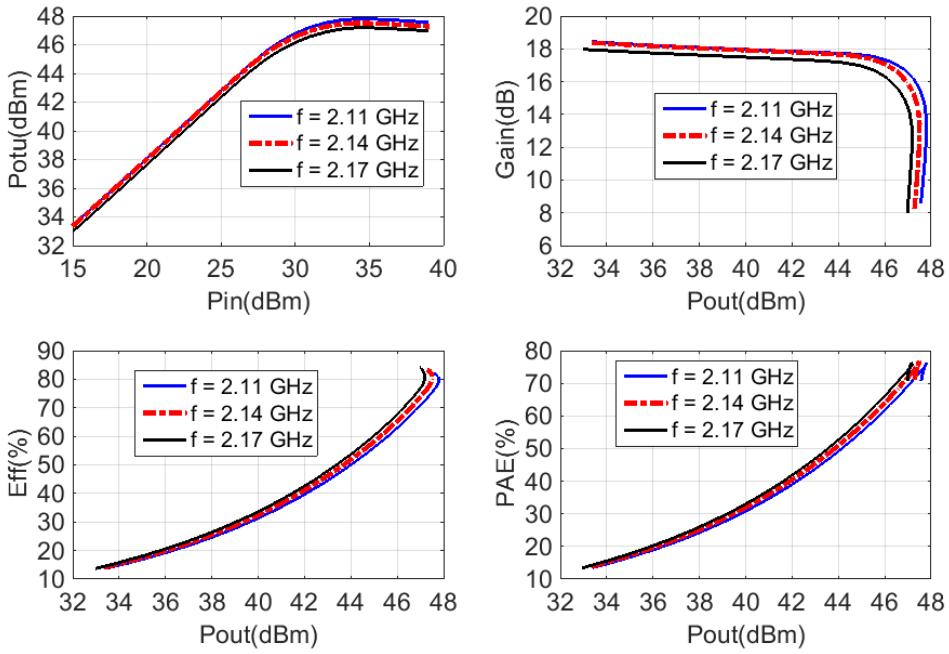

Figure 4.21: Final-stage amplifier simulated characteristic

4.6.2 Doherty-driver and Doherty-final amplifiers

As described in the previous chapter, a Doherty configuration has two amplifiers, main and auxiliary Fig. 4.22. The designed amplifiers in the previous section are in class-AB and hence are used as main amplifier for the driver and final Doherty power amplifiers. For the auxiliary amplifiers the same amplifiers are used, however, they are biased in class-C (V_{gs}= -5 V). In order to realize 25Ω load in the Doherty configuration, a quarter wavelength transmission line with 35Ω characteristic impedance is used to transfer a 50Ω load to the 25Ω. Further more, a $\lambda/4$ TL in the output of the main amplifier is used. The auxiliary amplifier modulates the load of the main amplifier via this TL. Fig 4.23 shows the layout of the Doherty combiner. In addition, an external 3-dB 90-degree hybrid coupler is used for power dividing and providing 90^o phase delay to the main and auxiliary amplifiers. Fig. 4.24 shows the characteristics of the X3C21P1-03S power divider [22]. As can be seen, in the design band, the power difference between port two and three is less than 0.2 dB. The phase difference in this two ports is about 90.7 degree.

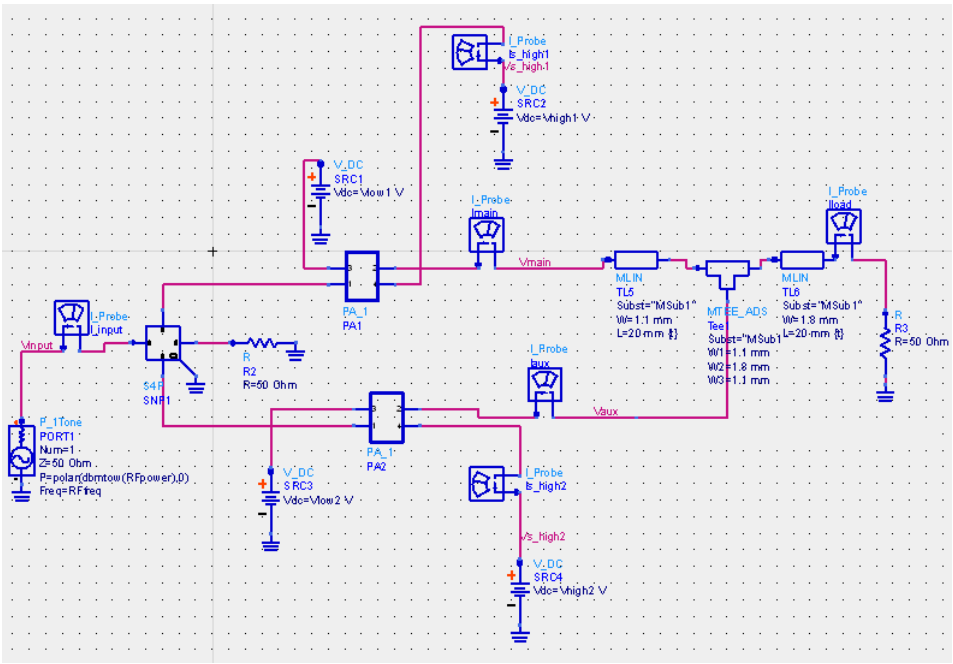

Figure 4.22: Schematic of the Doherty-final-stage

Fig. 4.25 and 4.26 show the final results of the Doherty-driver and Doherty-final-stage respectively. It is seen that the Doherty-driver has a maximum PAE of 74% and at 6-dB output back-off, PAE of 60% is achieved. From Fig. 4.26 we can observe that the maximum input power level for the Doherty-final-stage is 38 dBm. Therefore the output power of the Doherty-driver-stage should not exceed 38 dBm. Below this output power level, the Doherty-driver exhibits a gain of 14-16.2 dB.

Fig. 4.25 shows that the Doherty-final-stage has a maximum PAE of 73% and at

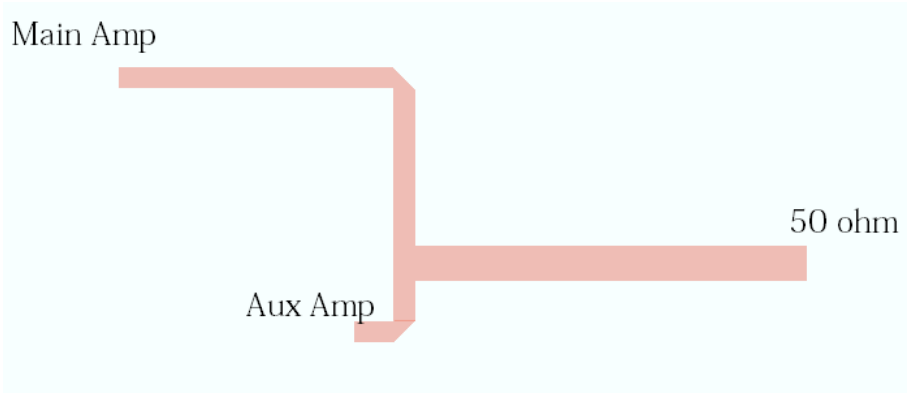

Figure 4.23: Layout of the Doherty combiner

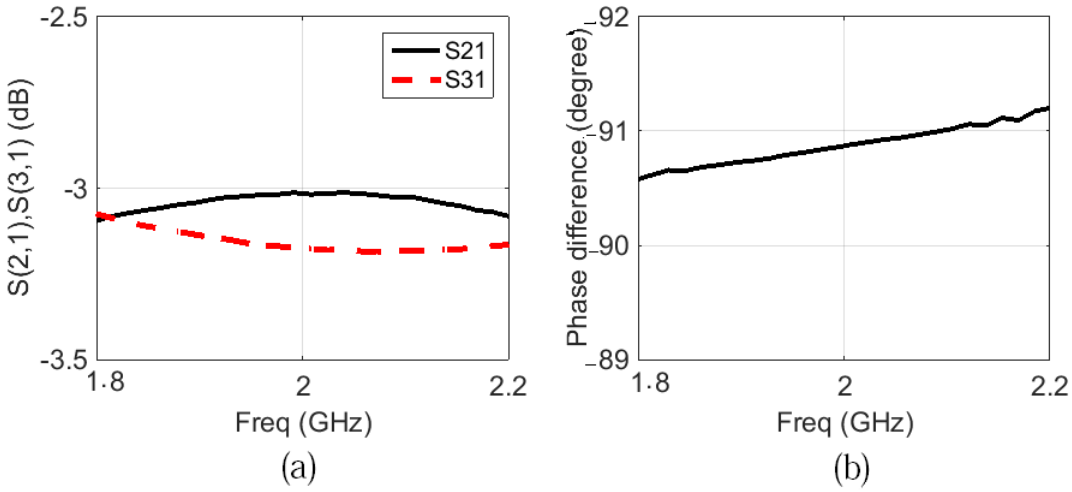

Figure 4.24: (a) $|S_{21}|$, $|S_{31}|$ and (b) phase difference between S_{21} and S_{31} of the X3C21P1-03S power divider

6-dB output back-off, PAE of 60% is obtained. The Doherty-final-stage reaches to its maximum output power level of 50 dBm at P_{in} =38 dBm. Below this input power level, the gain varies from 12-15 dB.

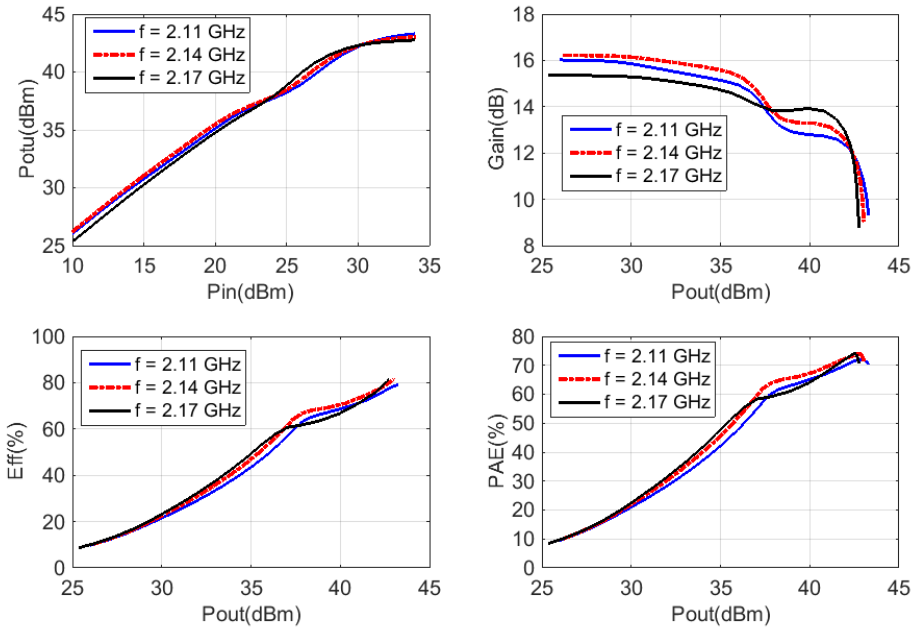

Figure 4.25: Doherty driver-stage simulated characteristic at 2.11, 2.14 and 2.17 GHz

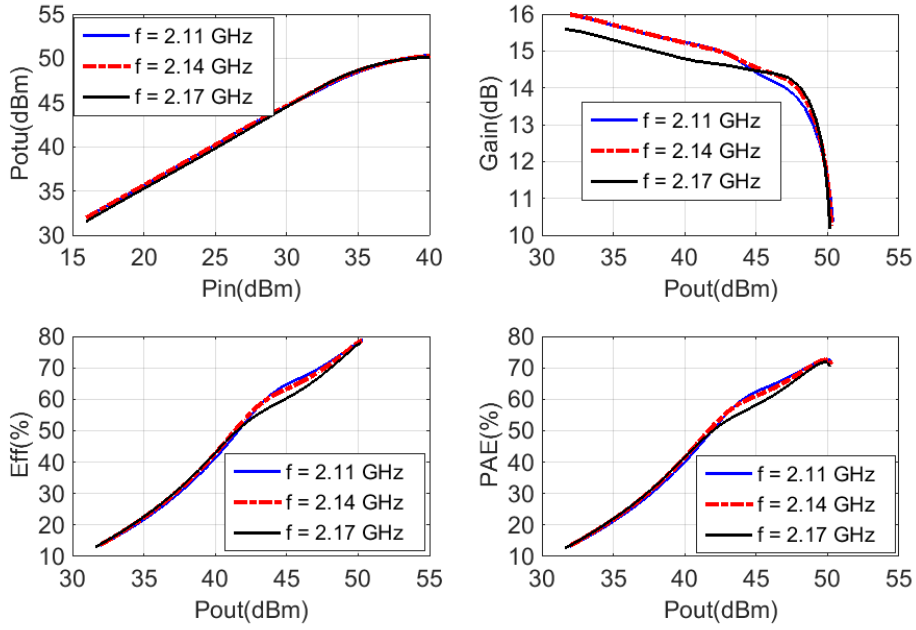

Figure 4.26: Doherty final-stage simulated characteristic at 2.11, 2.14 and 2.17 GHz

It should be noticed that the efficiency and the gain of the Doherty configuration is sensitive to the value of the gate voltage of the auxiliary amplifier. In Fig. 4.25 V_{gs-aux} = -5 V. In this gate voltage gain variation is acceptable and efficiency value is good enough. By varying the gate-voltage from -5 V to -7 V a higher efficiency in 6-dB OBO can be achieved. However, this will comes at the price of high gain compression and lower output power.

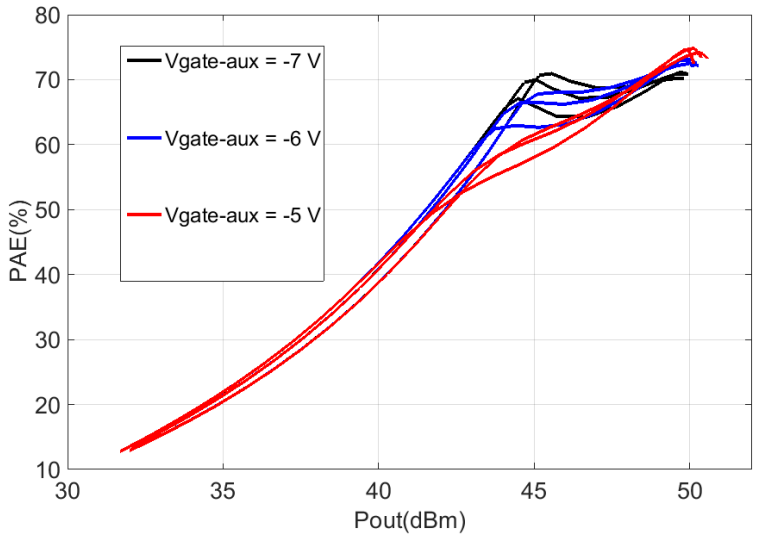

Figure 4.27: Efficiency performance of the final-Doherty based on different V_{gs-aux}

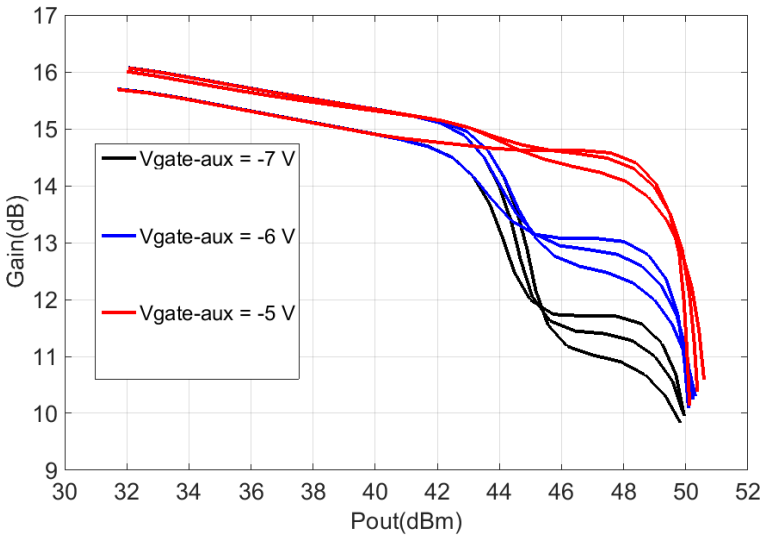

Figure 4.28: Gain performance of the final-Doherty based on different V_{gs-aux}

4.6.3 Comparison of driver topologies for two-stage power amplifiers

The PAE of different topologies described in Fig. 3.1 is simulated by using amplifiers designed in this chapter. As can be seen in Fig. 4.29, the two-stage cascaded Doherty power amplifier has the highest efficiency as expected from the Matlab simulations. In addition, Fig. 4.30 shows the total gain of different topologies. It is seen that the cascaded Class AB and a DPA topology has the highest gain. However, DPA with embedded Doherty drivers topology has the most flat gain which can result in more linear behaviour. The summary of the performance of these topologies at the peak power and 6-dB OBO is presented in table 4.3.

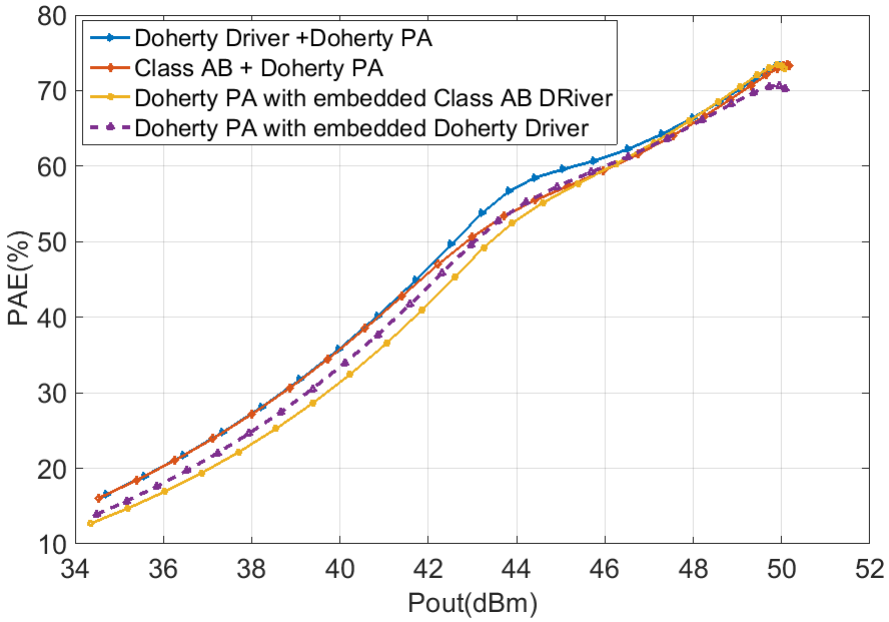

Figure 4.29: Efficiency comparsion of different topologies (f=2.14 GHz)

Table 4.3: Gain and PAE of different topologies at peak and 6-dB OBO (fig 4.29)

/	Cascaded class-AB and a DPA	Two-stage cascaded DPAs	DPA with embedded class-ABs	DPA with embedded DPAs as drivers
Gain (dB)at peak	30	26	29.5	29
Gain (dB) at 6-dB OBO	34	31	33	31
Peak PAE (%)	73	73	73	70
6 dB OBO PAE (%)	53	58	52	55

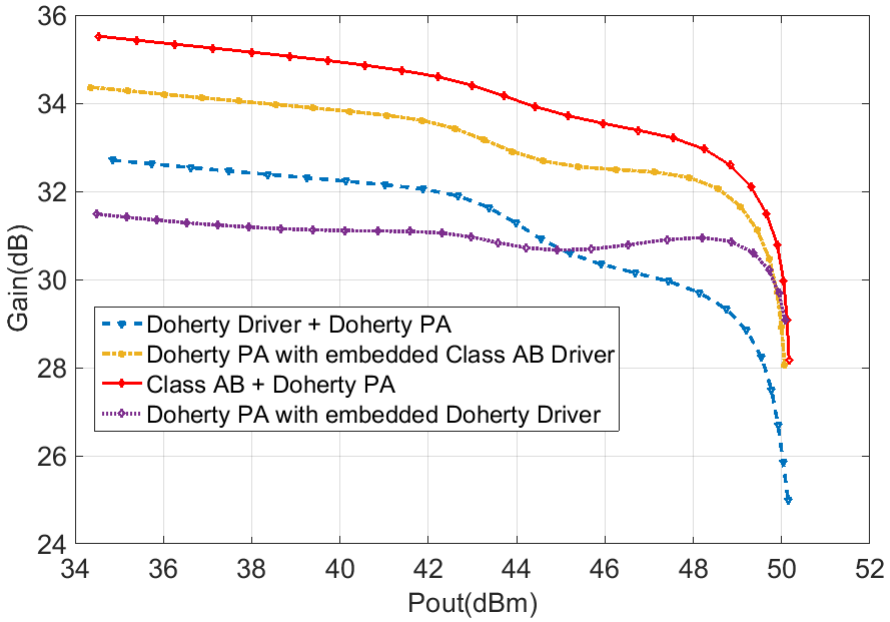

Figure 4.30: Gain comparsion of different topologies (f=2.14 GHz)

Table 4.4: PAE comparison of Matlab and ADS results.

Characteristics	ADS PAE at OBO= 6-dB	Matlab PAE at OBO= 6-dB
Class-B+Doh.	55	50
Doh+Doh	58	54
Emb.Doh	54	50
Emb.Dohwith Doh.drvs	55	52

Finally the comparison between the ADS and Matlab simulations at 6-dB OBO is shown in 4.4. The Matlab results are in good agreement with ADS simulations.

4.6.4 Two-stage cascaded Doherty PA

Fig. 4.31 and 4.32 show the ADS schematic and results of the two-stage cascaded Doherty amplifiers respectively. As mentioned before, this topology has the maximum PAE of 73% and at 6-dB output back-off, PAE of 58% is achievable. The two-stage cascaded Doherty PA reaches to its maximum output power level of 50 dBm at P_{in}= 24 dBm and it exhibits a gain of 30-32 dB at 6-dB OBO.

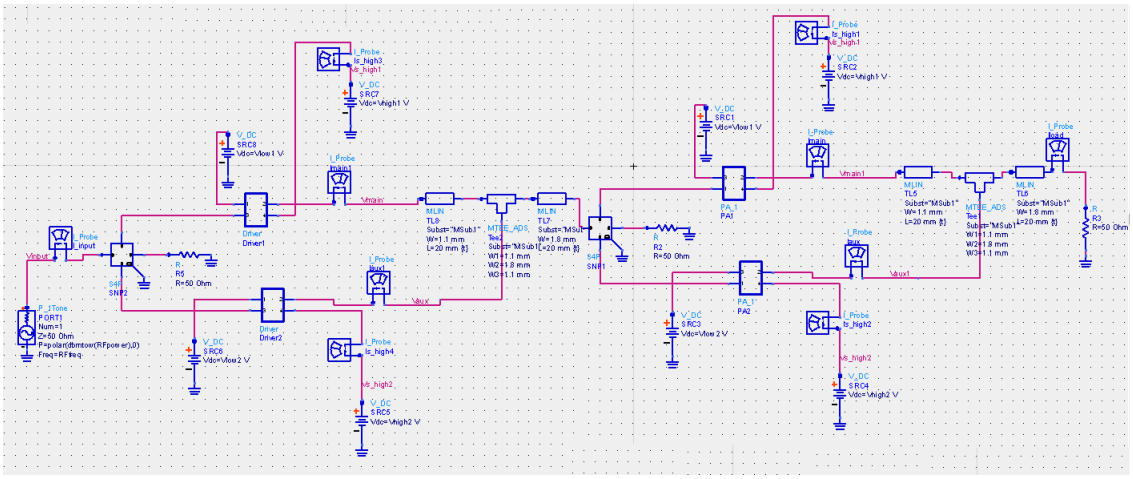

Figure 4.31: Schematic of the two-stage cascaded Doherty

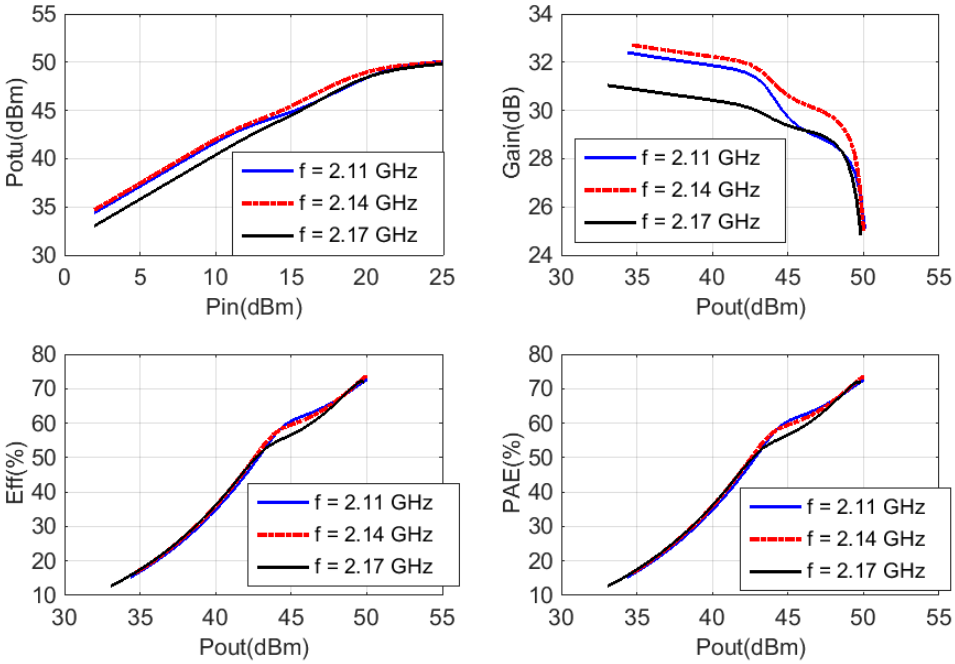

Figure 4.32: Simulation results of the two-stage cascaded Doherty

5

Conclusion and Future Work

5.1 Conclusion

In this master thesis, four driver topologies for the RF DPA have been investigated. These configurations are presented, discussed and compared based on simulation results.

The investigation is based on Matlab and ADS simulations. Matlab simulations are formed by the ideal transistor models while ADS simulations use real transistor models. High efficiency amplifiers (Driver and Final stages) have been designed as stand alone PAs. These amplifiers are designed based on 10W (CGH40010F) and 45W (CGH40045F) GaN-HEMT transistors in ADS. In ADS tool, source and load impedance are obtained from source and load pull simulations. Furthermore, in order to have a higher efficiency, impedance of second and third harmonics are tuned. In addition, stability is provided by the RC networks for both in-band and low frequencies. From the results we observed that The Doherty +Doherty has the best PAE, therefore it is discussed in more details. Based on these PAs, different topologies have been designed and compared. In the Doherty configurations, a 3 dB BLC is used to divide power by two with 90 degree phase shift in the input of the PAs to compensate the phase delay in the output of the amplifiers.

Finally we observed that Matlab and ADS simulation results are similar and two-stage Cascaded Doherty PAs provides the best efficiency. The schematic simulation results show that the two-stage cascaded DPAs gives the maximum lineup peak and average PAE of 73% and 58% respectively. It also has a maximum output power of 50 dBm and a corresponding gain of 26 dB.

The good agreement between theoretical (Matlab) and real simulations (ADS) validate this study and show the importance of the driver topology for the total performance in two-stage power amplifiers. Finally, this study will help PA designers to select the best topology for their applications when two-stage PAs are required and thus lead to build new transceivers with improved performance in terms efficiency and energy consumption.

5.2 Future Work

We would like to experimentally compare the performance of two different topologies: two-stage cascaded DPAs and DPA with embedded Doherty drivers. For that purpose, the layouts of both topologies will be designed and fabricated. Extensive measurements will be performed to fully characterize the two topologies to compare the results with the simulated ones.

It would be interesting to simulate the linearity performance of the four topologies based on the AM/AM and AM/PM functions of the designed PAs in ADS. In addition, linearity will be characterized, with and without digital pre-distortion, using real communication signals.

In this thesis, the DPAs are based on equal power division between the main and the auxiliary PAs. It is interesting to compare these topologies by using asymmetric input power division. Moreover, it may be possible to get a better performance if different matching networks are designed for the auxiliary amplifiers because the ones used in this thesis are the same for the main and auxiliary amplifiers.

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