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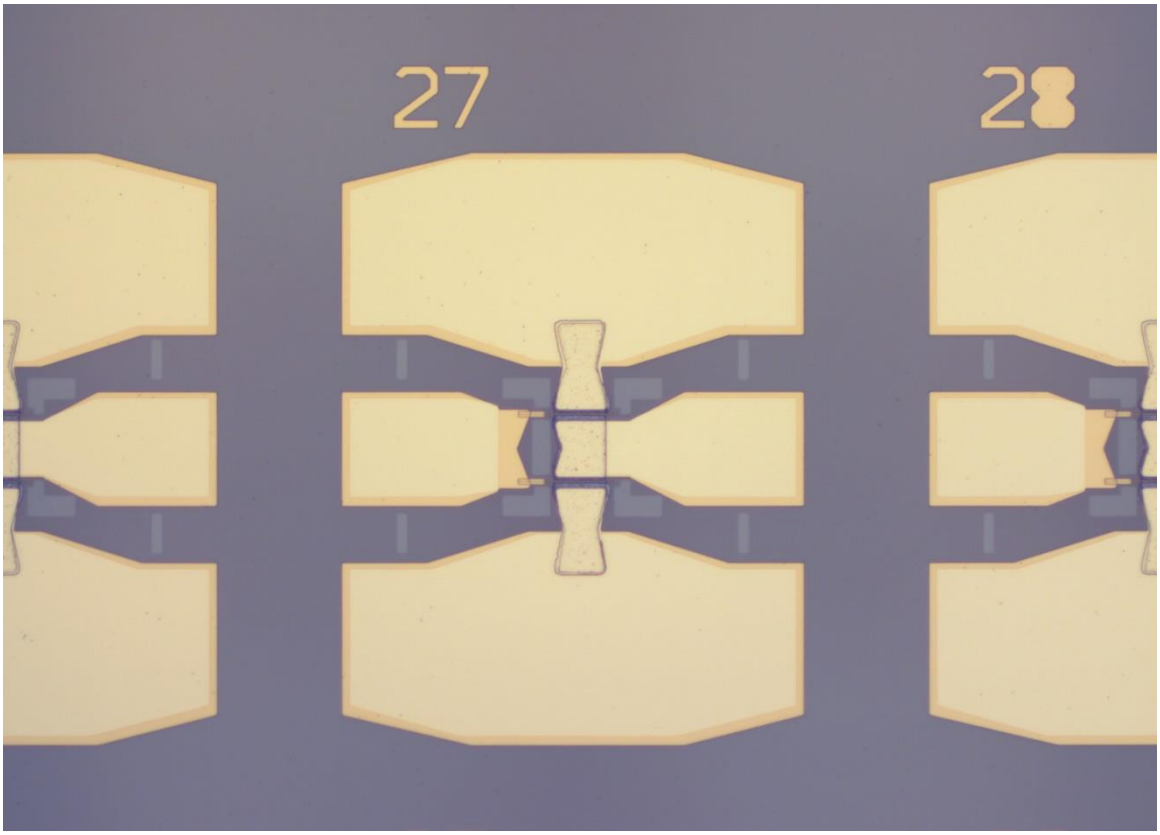

The Impact of GaN-buffer C-doping Profile on Short-Channel Effects and Ohmic Contact Formation for Millimeter Wave III-Nitride HEMTs

Master's Thesis in Electrical Engineering

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Abstract

The InAlN/AlN/GaN HEMT has a high breakdown field which allows for excellent power performance. In order to increase frequency operation, a reduction in device size is required, inherently increasing the short-channel effects and limiting device efficiency and linearity. It is possible to mitigate drain-induced barrier lowering (DIBL) and subthreshold swing by increasing the carrier confinement in the 2DEG channel of the HEMT through optimizing the buffer design with the use of GaN-buffer C-doping.

The impact of different C-doping profiles on short-channel effects is investigated by the fabrication and characterization of two-finger U-shaped HEMTs with 2 x 25 µm gate width and 50, 100 and 180 nm gate length. DC and S-parameter analysis show decreased short-channel effects for devices with constant levels of intentional C-doping to the buffer, but that the high frequency and power performance is impaired by a reduction of the on-state conductance. Compared to HEMTs with no intentional C-doping in the buffer, the DIBL was decreased from 385 to 195 mV/V and the subthreshold swing from 2140 to 1440 mV/dec in highly C-doped devices at a drain bias of 20 V.

Best RF performance was achieved for a ramped C-doping profile with values of f_T and f_{max} of 66 and 180 GHz respectively. Although, these devices showed a deteriorated performance in terms of short-channel effects, including pinch-off, output conductance and current leakage. Consequently, there is a trade-off between the reduction of short-channel effects and an increase of f_T and f_{max}.

Ohmic contact formation and the reduction of contact resistance and specific contact resistivity is important to consider in order to increase the efficient operation of HEMTs. Ohmic contacts which induce low voltage drop and heat generation compared to the bulk resistance of the semiconductor, are difficult to realize in wide-bandgap materials. It is possible to assist the formation of ohmic contacts and lower the resistivity by contact recess etching down to the substrate channel and by altering the metallization.

Ta-based contacts are considered for their low optimum anneal temperature. Ta/Al/Ta contacts to AlGaN/AlN/GaN heterostructures have been found to be reproducible and to have good performance with concern to contact resistance, specific contact resistivity, surface morphology and line edge acuity. A contact resistance of 0.38 Ωmm and corresponding specific contact resistivity of $4.2 \cdot 10^{-6}$ Ωcm^2, were gained after optimal anneal at 550°C.

The layer formed in between the contacts and the semiconductor during anneal, causes N-vacancies in the buffer and promotes electron tunnelling through the barrier, which in turn lowers the contact resistance. The lower resistivity of ZrN compared to TaN, yields an interest in Zr-based contacts. Zr/Al/Zr/Ta/Au contacts to AlGaN/AlN/GaN show low optimum anneal temperature of 650°C and contact resistance of 0.87 Ωmm, but further research is required.

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List of Abbreviations

2DEG	Two-Dimensional Electron Gas
ALD	Atomic Layer Deposition
ICP	Inductively Coupled Plasma
DIBL	Drain-Induced Barrier Lowering
DWL	Direct Write Lithography
HEMT	High Electron Mobility Transistor
RIE	Reactive-Ion Etching
RTP	Rapid Thermal Processing
SS	Subthreshold Swing
TLM	Transfer Length Method
UHV	Ultra High Vacuum

List of Elements

Al	Aluminium
Ar	Argon
As	Arsenic
Au	Gold
C	Carbon
Cl	Chlorine
Cr	Chromium
F	Fluorine
Fe	Iron
H	Hydrogen
Hf	Hafnium
In	Indium
Mg	Magnesium
N	Nitrogen
Nb	Niobium
Ni	Nickel
O	Oxygen
P	Phosphorus
Si	Silicon
Ta	Tantalum
Ti	Titanium
V	Vanadium
Zr	Zirconium

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Introduction

The current development and need for communication applications at high frequencies is pushing research further into the THz gap. Not yet allocated frequency bands, wider bandwidths, higher bit-rates, less atmospheric attenuation, longer range and smaller devices are just a few of the many appealing benefits. Although, the reduction in size which is required by the increase of frequency, also lowers the output power levels of electronic devices.

The field of solid state microwave electronics shows great potential in reaching high power levels at high frequencies. As the dimensions of a solid state device is scaled down, its breakdown voltage is lowered which in turn leads to lower output power. So far, the market has been dominated by relatively narrow bandgap semiconductors such as GaAs and InP. Although, the breakdown field is naturally higher in wide-bandgap materials, which would allow for an increase in power.

By introducing wide-bandgap semiconductors such as the III-nitrides, a new transistor technology capable of meeting current and future demands can be established. Nitride-compounds of Al, In and Ga have both high breakdown voltage to provide high power and high electron velocity to allow high frequency operation. Their ability to form heterojunctions also makes them suitable for fabrication of HEMTs and enables the possibility to mass produce less bulky, faster, more reliable, and more energy efficient devices by the use of low-cost semiconductor processes.

This work aims to study III-nitride HEMTs and the advanced processes to laterally and vertically scale the transistor dimensions, while maintaining electron confinement and low loss. It involves an investigation of ohmic contact formation to AlGaN/AlN/GaN heterostructures, and of the impact on short-channel effects of different carbon doping profiles of the GaN buffer layer in InAlN/AlN/GaN HEMTs.

Chapter 2 will discuss the properties of the III-nitride HEMT, while clarifying the effect of the main process steps of contact recess, metallization and anneal, describing the most prominent short-channel effects of drain-induced barrier lowering and subthreshold swing and discussing the possibilities of reducing these effects, especially by the introduction of carbon doping, while also providing the underlying theory of the measurement techniques later used to extract valuable data.

The following chapters 3, 4 and 5 will go through the topics of ohmic contact formation, fabrication of InAlN/AlN/GaN HEMTs and characterization of HEMTs respectively. Each chapter will describe the experimental procedures associated with that part, present the results and have its own summary and discussion. There will also be a general conclusion drawn in Chapter 6.

2

Theory on III-Nitride HEMTs

The configuration of high electron mobility transistors offers high carrier concentration, electron mobility and current density while keeping a low channel resistance and providing good noise performance [1]. These are all useful characteristics for high power switching applications at high frequencies. The electron mobility, concentration and saturation velocity of the semiconductors are essential properties for reaching expert transistor performance [2], and this is what makes the III-nitride materials so promising for HEMT technology. The III-nitride components in power switch applications make it possible to combine a low resistance with very fast switching.

On account of their wide bandgap, combined with several other beneficial qualities, the III-nitrides show superior device efficiency at high voltages and with lower loss. The wide bandgap allows for high temperature operation and high breakdown field. Although, the wide bandgap also makes it difficult to realize metal-semiconductor contacts to source and drain that are ohmic, with low contact resistance and specific contact resistivity [3]. This topic is discussed further in Section 2.1.

Many have succeeded in finding low-resistive ohmic contacts to III-nitride heterostructures, especially regarding contacts to AlGaN/AlN/GaN. Nevertheless, there is still no reliable process of fabrication available, and more research is needed. Among all the influencing parameters, the contact resistance has been found to be sensitive to matters such as pre-evaporation cleaning, choice of contact metals, etch depths, and anneal. [4, 5]

The anneal procedure efficiently reduces the resistance of the contacts by providing strong vertical material diffusion, while the lateral diffusion of metals is unwanted. Annealing at high temperatures deteriorates the surface morphology of the contacts, worsens the line edge definition and causes surface and gate leakage, which are problems that prevent the downscaling of the devices [3, 6]. By the choice of contact metals and anneal, as explained in Section 2.1.2, these issues as well as the contact resistance can be minimized.

There has been many advances in the fabrication of GaN-based HEMTs, for instance regarding material purity, gate contact stability and ohmic contact formation [2]. GaN transistors can be grown on SiC substrates and fabricated with standard semiconductor processes [7]. AlGaN is commonly used as barrier layer and InAlN also shows benefits as barrier material. The approximate band gap, electron mobility and thermal conductivity for the III-nitride alloys, InGaAs and GaAs can be studied in Table 1 [8].

Table 1: The direct band gap energy E_0, electron mobility μ_e, and thermal conductivity σ_T, at room temperature, for In, Al and Ga nitride compounds, InGaAs and GaAs. The values for InAlN and AlGaN have been calculated as the materials are lattice matched to GaN at In-content of 17 % and Al-content of 25 % respectively. The InGaAs has an In-content of 53 % which is as it is lattice matched to InP. All values are calculated from the relations in [8], using proposed bowing parameters intended for each ternary alloy.

		GaN	AlGaN	AlN	InAlN	InN	InGaAs	GaAs
E_0	$[eV]$	3.4	3.9	6.2	4.7	0.7	0.7	1.4
μ_e	$\left[\frac{cm^2}{Vs}\right]$	1250	796	125	631	3100	15400	9340
σ_T	$\left[\frac{W}{cm\,K}\right]$	1.95	0.15	3.19	0.36	0.45	0.05	0.45

InAlN can be grown lattice matched to GaN at an In concentration of approximately 17 %, which reduces strain in the structure and leads to better structural stability and reliability. Due to the high polarization discontinuities for InAlN and AlN compared to AlGaN, the barrier can be grown thinner while maintaining an equally high carrier concentration in the 2DEG channel. This enables reduced short-channel effects and parasitic resistances in devices operating at higher frequencies. [4, 9]

The main short-channel effects and different techniques proposed to mitigate them are discussed in Section 2.2, along with the effects of C-doping on DC and RF performance and how to extract parameters from DC and S-parameter measurements in order to characterize the devices.

2.1 Ohmic Contacts

Semiconductor devices, such as the HEMT, need to have an interface where carriers can be injected into or extracted out of the semiconductor. This is accomplished by adding layers of metal to the source and drain, thus constructing metal-semiconductor junctions. The ambition is that the contacts should have low resistance in both forward and reverse operation. For optimal performance of the HEMT, the voltage drop and heat generation caused by the contacts should be negligible in comparison to that of the active region of the device. It is desired to have a linear I-V characteristic, with a constant contact resistance, often referred to as an ohmic contact. However, plain contacts of metal on wide-bandgap semiconductors behave as Schottky contacts by being intrinsically rectifying. [10, 11]

A wide-bandgap material, with its many advantages mentioned in the previous section, makes ohmic contact formation more challenging. The Schottky barrier height, determined by the Fermi level across the junction and the level of the majority carrier band edge of the semiconductor, becomes too high for carriers to cross and thermionic emission is extensively reduced. To overcome this difficulty, it is possible to increase the electron transport and density of states on the semiconductor surface near the interface by heavy doping. This will decrease the width of the depletion region and yield a narrow enough barrier for carriers to be able to tunnel through [10, 11], as illustrated in Figure 1. In a junction between a metal and a heavily doped wide-bandgap semiconductor, it is theoretically possible for equally large currents to flow under both forward and reverse operation. [10]

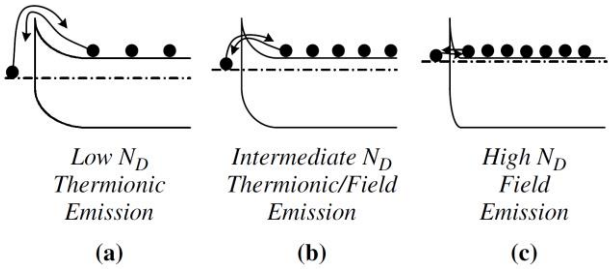

Figure 1: Conduction mechanisms with increasing doping concentration. (a) With low carrier concentration, thermionic emission dominates the current flow. A semiconductor with a wider bandgap would cause an increase of the barrier height and choke the current. (b) At an intermediate doping level, thermionic emission excites the carriers to an energy level where the barrier is narrow enough for them to tunnel through. (c) With a high doping concentration, the depletion region is exceedingly decreased and field emission dominates. The carries can tunnel directly through the narrow barrier. [17]

The quality of the metal-semiconductor contacts is measured in specific contact resistivity and contact resistance. The specific contact resistivity has a strong dependence on carrier concentration and the barrier [5, 11]. It includes the resistance of the metal-semiconductor junction as well as the regions immediately above and below the interface. Specific contact resistivity has a unit of Ωcm^2 and does not depend on the geometry of the contacts [12], which makes it a convenient measurement for comparing devices of different sizes. The contact resistance however, only describes the resistance of the junction itself. It can be related to the width of the contact and then has a unit of Ωmm [5]. It is used to compare the effect of different materials or methods in structures fabricated to have the same geometry. The methods used to extract these quantities are discussed in 2.1.3.

The total resistance of a typical horizontal HEMT can be summed up by the resistances in the path of the current flowing from source to drain. This can be extracted from a simple model of the device like the one shown in Figure 2. The total resistance is mainly comprised by the resistance caused by the two metal contacts, the two junctions and the semiconductor in between [5]. Additional resistance due to the pads could also prove significant. The contacts and the contact formation therefore contribute greatly to the total resistance, which shows the importance of reducing the contact resistance of a HEMT.

2.1.1 Contact Structures

It is of importance in which way the metal contacts are added to the semiconductor surface. Three recognized methods, presented in the following sections, are planar contacts, recessed contacts, regrown contacts and ion-implanted contacts. They differ by how the contacts are positioned in relation to the barrier, the spacer and the 2DEG channel in the buffer. The resulting contact resistance can vary vastly between different methods.

Planar contacts are constructed as the metal is applied on top of the compound semiconductor, see Figure 2. The barrier then stays intact and there is no increased local doping which would reduce the contact resistance. These are the most commonly used contacts on account of them being comparably easy to manufacture [13]. Planar contacts perform well enough when applied to materials having a smaller bandgap, but on wide-bandgap semiconductors the barrier becomes too high.

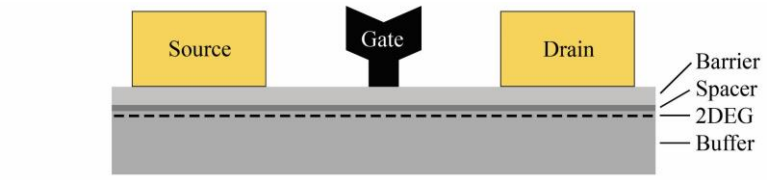

Figure 2: Planar metal contacts on top of the wide-bandgap barrier. There is no local increase of doping present.

On wide-bandgap materials the width of the barrier can be reduced by etching down into the semiconductor structure and applying the metal contacts to the submerged region [14], as seen in Figure 3. This will increase the effect of tunnelling and lower the contact resistance. [11] Recessed contacts are also less sensitive to variations of the epitaxial layers, such as the thickness of the exclusion layer [4].

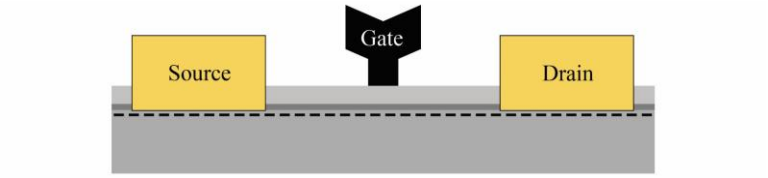

Figure 3: The contacts have been recess etched down through the barrier. This allows for an increase in carrier tunnelling and a lower contact resistance.

The method of recessed contacts has been shown to be delicate to etch depth [4]. It is presumed that optimal contact resistance is achieved by etching down to get close to the 2DEG in the buffer but to not etch completely through the spacer. The etch depth will be studied further in Section 3 for contacts on AlGaN/AlN/GaN and in Section 4 for contacts on InAlN/AlN/GaN.

It is also possible to reduce the contact resistance by etching away the barrier and spacer at source and drain in order to regrow a highly doped version of the buffer material in these regions, as in Figure 4. It can be very difficult and consuming to regrow the buffer. Another approach is to achieve the highly doped regions by ion-implantation. However, this requires high temperature anneal to activate the implants and introduces surface degradation that impacts the properties of the gate. [13]

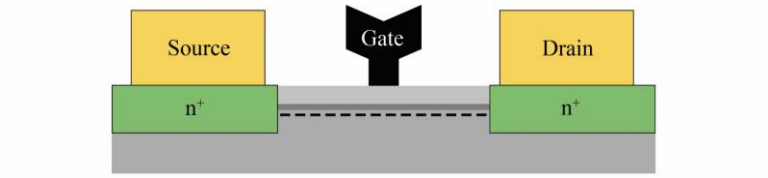

Figure 4: Regrown contacts where the epistructure has been etched down in the areas of contact metallization and regrown (or implanted) with highly doped buffer material, for instance n^+-GaN.

Tries have also been made where highly doped GaN has been added on top of the barrier to reduce contact resistance and then the gate metal has been recess etched to gain contact with the barrier. In order to controllably etch through GaN-related materials, plasma etch is needed. The plasma etching also causes damage to the semiconductor surface and degrades gate formation. [5, 13]

2.1.2 Contact Metals & Anneal

The metal contacts used to form ohmic contact to the semiconductor of a HEMT is often comprised of several layers of different metals. Ti/Al-based contacts are the most commonly used contacts to AlGaN/AlN/GaN and provide low contact resistance [15]. It is unknown to what extent the metals in the stack affect the properties of the contact, but it is presumed that the two bottom layers are the ones responsible for causing a low resistance and forming the ohmic contact [5]. It is common for an additional layer to be applied to the contact in order to avoid oxidation, but this also implies that a barrier metal with high melting point [3] has to be included to prevent that layer from diffusing towards the semiconductor and degradation of the ohmic contact [5].

The transport of carriers over the barrier of a metal-semiconductor contact due to thermionic emission increases with increasing temperature. The specific contact resistivity can therefore be further reduced by contact anneal [11]. It is believed that the anneal causes nitrogen vacancies in the metal contacts to generate a highly doped region in between the contact and the semiconductor, which allows for low contact resistance [4, 5, 15, 16].

The anneal time and temperature is of great importance to the properties of the metal contacts [5]. The sheet resistance of the semiconductor increases with anneal temperature. Unlike the contact resistance which has its minimum at a certain temperature. When annealed at this temperature, the contact resistance decreases with time until it slowly stabilizes. However, if the temperature is too high, a longer anneal time will instead increase the contact resistance [15]. The ramp profile of the anneal temperature can be of importance to the contact resistance. It is possible to use a slope or multi-step anneal, where the temperature is carefully increased at a certain rate [16]. In this work, the anneal temperature is ramped up to the desired value in a matter of seconds, and cooled between steps.

To obtain low contact resistance, Ti/Al-based contacts require very high anneal temperatures of 800°C or more [15]. Annealing at high temperatures not only increases the sheet resistance, it also deteriorates the surface morphology and worsens the edge acuity [6]. The morphology of the contacts can indicate phase changes, which is good to have under control [3], and a rough surface morphology makes e-beam or optical pattern recognition more difficult [6, 11].

Ta/Al/Ta contacts have shown to reach low values of optimum contact resistance already at anneal temperatures of 550°C to 600°C [4, 15], which is below the low melting point of Al at 660°C. This provides for good morphology, precise line edge definition, and reduces surface and gate leakage [6].

The thickness of the metal layers are relevant for ohmic contact formation [5]. Ta/Al/Ta contacts with a bottom Ta layer of 5 nm have been found to provide lower contact resistance than contacts of the same type with both thicker and thinner bottom layer thickness [4, 15]. The thickness of the Al layer does not show an equally strong impact on contact resistance, but needs to be sufficiently large, in the order of a few hundred nm. For planar Ti/Al contacts, it has been determined that the ratio between the thickness of the Ti and Al layers is of importance for the contact resistance. Ta/Al/Ta contacts with a thickness of 5/280/20 nm yielded good performance with regard to ohmic contact formation [15].

2.1.3 Transfer Length Method

The TLM measurement technique is well-known and widely used for characterization of ohmic contacts [5, 11, 12, 17]. TLM is based on four-point probe measurements, and measures the total resistance of metal contacts to a semiconductor surface. An optical micrograph of a linear TLM structure is depicted in

Figure 5 (a), and a model of the same type of structure is seen in Figure 5 (b). While the current flows through the entire structure, from the lower-most contact to the upper one, the voltage is measured over the different distances d_1 to d_5.

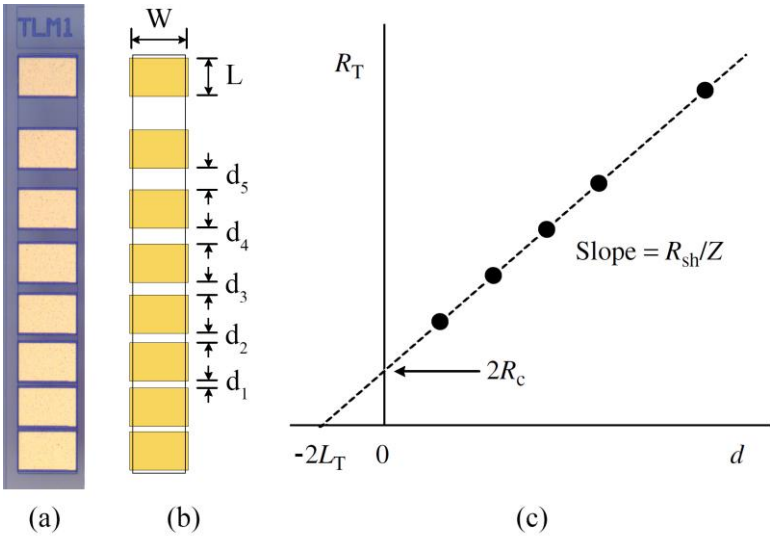

Figure 5: (a) Optical micrograph of a TLM structure with Ta/Al/Ta contacts to InAlN/AlN/GaN, (b) a model of the structure, and (c) a plot of the total measured resistance R_T versus the distance d between contacts.

The mesa isolates the contacts and forces current to flow only in one direction, across the distances d. If linear TLM structures are not isolated, the current can flow between contacts through the region beyond the test structure [17]. To further avoid edge effects, the width of the contacts needs to be larger than the distance between the contacts, since the current will flow in the path of least resistance [11]. In circular TLM structures, the problems caused by edge effects are eliminated and the outside lines of the contacts do not contribute to the measured resistance. In addition to not requiring mesa isolation [17], this makes for more accurate measurements as the contact resistance is very small [5, 11].

The measured total resistance R_T will have a linear relation to the distances between contacts, as in the plot of Figure 5 (c). The total resistance is comprised of the sum of two times the contact resistance R_C and the semiconductor bulk resistance, which can be written in terms of sheet resistance R_{sh}, according to (1). [17]

$$R_T = 2R_C + R_{sh}\frac{d}{W} \tag{1}$$

The specific contact resistivity ρ_C, can be derived from the contact resistance by the relation in (2), and the transfer length L_T is expressed as in (3) [17]. The transfer length is the average distance that a carrier travels in the semiconductor beneath the contact before it reaches up to the contact itself. The TLM calculations presume that the sheet resistance is the same in the channel as well as under the contacts. However, the channel is slightly depleted by the metal contacts, and the anneal also has an influence on the sheet resistance. Even so, the value of the transfer length is fairly well estimated by TLM. [11]

$$\rho_C \approx R_C W L \tag{2}$$

$$L_T = \sqrt{\frac{\rho_C}{R_{sh}}} \tag{3}$$

As shown in Figure 5 (c), the measured data is fitted to a straight line by utilizing the method of least squares. The correlation of the fitted curve can be calculated and used to determine the validity of the results.

2.2 Short-Channel Effects

Lateral downscaling of HEMTs allows for high frequency operation but introduces short-channel effects which deteriorate the transistor performance. Drain-induced barrier lowering is the most prominent short-channel effect and takes the form of threshold voltage shift, soft pinch-off, high subthreshold current and increased output conductance [18, 19, 20, 21]. An increased level of DIBL effectively degenerates the linearity and efficiency of the device [19, 20, 21] and causes an elevation in current leakage [22, 23]. Another important short-channel effect is the subthreshold swing, which is determined by the relation between gate voltage and drain current and gives an indication of how fast the transistor can be switched on or off.

The short-channel effects of DIBL and subthreshold swing are mainly caused by poor confinement of charge in the 2DEG channel of the buffer [19, 20, 21, 22, 23, 24]. This causes current to flow within the bulk of the GaN buffer. By enhancing the carrier confinement, the gate is able to better modulate the electrons under high drain voltages, and the control of the drain current is thereby improved [21].

An improvement of the carrier confinement can be achieved by scaling down the gate-to-channel distance d, with the gate length L_g, to maintain a high aspect ratio $\frac{L_g}{d}$ [25]. For GaN technology, an aspect ratio of 15 is required to sufficiently mitigate the short-channel effects [9, 25, 26], while an aspect ratio of 10 is enough to suppress most of the effects on the frequency response [18, 25, 26], and an aspect ratio of six is needed in order for the gate to maintain control of the channel in small signal operation [26].

The aspect ratio can be increased by simply growing a thinner barrier. However, excessive scaling of the top barrier causes serious limitations in terms of increased gate leakage, as well as a reduction of the 2DEG density and the carrier mobility in the channel [9, 25]. The aspect ratio can also be improved by the means of using AlN or InAlN as barrier materials or by gate recess etching. AlN and InAlN have larger polarization discontinuities than AlGaN which allows for a reduction of the barrier thickness. Recess of the gate by dry etching down through the barrier reduces the gate-to-channel distance, but induces surface damage to the channel. [23, 24]

The carrier confinement in the 2DEG channel can also be improved by methods involving a redesign of the GaN buffer layer, for instance by utilizing an InGaN channel, applying a back barrier, or increasing the deep level density. The carriers experience better confinement in a narrow InGaN channel compared to a GaN channel [18]. The high polarization-induced electric fields in a back barrier increases the confinement of the 2DEG [21] but at the expense of a degraded thermal conductivity of the structure [23]. A high density of deep level donors and acceptors in the GaN buffer provides a confining potential beneath the channel [19, 20, 27]. The increase of the deep level density can be achieved either by intrinsic defects or extrinsic dopants,

such as iron, carbon or magnesium [19, 27], of which the approach utilizing intrinsic defects is difficult to control and yields poor crystal quality [27].

The optimal buffer design is determined by several HEMT characteristics other than the short-channel effects. It is of importance to find a balance between device parameters such as breakdown voltage, subthreshold leakage, current collapse, and maximum drain-source current [27]. In this work, the impact of GaN buffer C-doping on InAlN/AlN/GaN HEMTs is investigated.

2.2.1 Buffer C-Doping

During growth, the GaN buffer is unintentionally C-doped to a concentration presumed to be in the order of 10^{16} cm^{-3}. It is possible to controllably add dopants to obtain a compensation-doped buffer having a certain profile. In contrast to Fe which is the most commonly used buffer dopant, C allows for growth of materials with discontinuous doping profiles and sharp transitions to the GaN channel [27]. When using Fe and C-dopants, the compensation-doped buffer needs to be placed a certain distance from the GaN channel in order to avoid severe current collapse, a reduction of the drain current due to trapping effects [27].

Intentional C-doping improve buffer isolation and carrier confinement and should reduce leakage currents and improve pinch-off [10, 20, 22, 27]. On the downside, the trap states and associated dispersion give rise to a dynamic shift in the threshold voltage and may reduce the on-state conductance and maximum drain current of the device, causing high current collapse and effectively limiting the linearity, output power and frequency performance [10, 21, 27]. A more negative threshold voltage will increase the slope of the energy band in the AlGaN/GaN interface, and promote carrier tunnelling which will increase the gate leakage [27]. In spite of the high gate leakage, an improved carrier confinement can still show lower levels of DIBL, by reduced output conductance and drift of the threshold voltage [24].

The trap induced issues can be suppressed by a high carrier mobility and velocity [24, 28]. This will increase the maximum drain current and transconductance of the device [10, 24], thus improving the subthreshold swing. However, the mechanisms which determine the carrier mobility and velocity can be influenced by factors such as material variations and strain in the buffer [26, 27]. Highly C-doped structures can also show large non-uniformity, which can give a variance in sheet resistance and affect the 2DEG properties, the carrier mobility and velocity [27].

A SiNx or AlN passivation layer can be used to reduce the surface induced dispersion effects [22]. A passivation on top of the device can provide sufficient charge to neutralize the surface charge of the barrier and prevent depletion of the 2DEG. It will also provide stability at high temperature operation and contribute to reduced channel resistance [11]. However, it has been reported that passivated devices have higher parasitic capacitances, and that this limits the high frequency performance [21].

2.2.2 DC Performance

The transfer and output characteristics of a device give information on threshold voltage, transconductance, and maximum saturated drain current, and allow extraction of the level of DIBL and subthreshold swing. The DIBL is calculated as the negative difference in threshold voltage V_{th} between two points, divided by the difference in drain bias voltage V_{ds} at these same points, see (4).

$$DIBL = -\frac{\Delta V_{th}}{\Delta V_{ds}} \tag{4}$$

The DIBL is expressed in terms of mV/V and in InAlN/GaN HEMTs, the DIBL starting from values below 50-60 mV/V begins to increase sharply as the gate length decreases below 100 nm [9].

The subthreshold swing SS, an important parameter in the sub-threshold regime, represents the efficiency of coupling between the gate potential and the channel potential, and is defined as the gate voltage swing required to reduce the sub-threshold current I_{ds}, by one decade, seen in (5). The subthreshold swing can also be expressed by the charge placed on the gate that does not result in inversion layer charge, as in (6).

$$SS = \frac{dV_{gs}}{d\big(log(I_{ds})\big)} \tag{5}$$

$$SS = \frac{k_B T}{q} \cdot ln(10) \cdot \left(1 + \frac{C_Q + C_{it}}{C_i}\right) \tag{6}$$

Here, $\frac{k_B T}{q}$ is the thermal voltage, where k_B is the Boltzmann's constant, T is the absolute temperature in K, and q is the magnitude of the electron charge. C_Q is the quantum capacitance, C_{it} is the interface trap density capacitance and C_i is the barrier layer capacitance. The subthreshold swing is expressed in mV/dec and has a fundamental limit of 60 mV/dec. [17, 27]

The transfer characteristics also provide values of the transconductance, which is defined as in (7).

$$g_m = \frac{\Delta I_{out}}{\Delta V_{in}} = \frac{\Delta I_{ds}}{\Delta V_{gs}} \tag{7}$$

The transconductance increases with decreasing gate length, until the short-channel effects take overhand and the gate loses the ability to control the channel [25, 26]. On the other hand, with increased carrier confinement and 2DEG density, the peak transconductance is reduced [9, 22]. A higher density also yields a more negative threshold voltage and thereby a stronger vertical peak field at the drain edge of the gate and increased current leakage [9, 20, 22]. A high gate leakage current will obstruct the complete pinch-off of the device [24].

The current I_{th} related to the threshold voltage V_{th}, can be defined as 1% of the maximum saturated drain current as in (8).

$$I_{th} = 0.01 \cdot \max(I_{DSS}) \tag{8}$$

A high carrier mobility results in an increased saturation current and transconductance. However, by designing the buffer to have a ramped C-doping profile, the saturation current can be held at an equally high level as a non-doped buffer while the transconductance can be slightly improved. [27]

2.2.3 RF Performance

By the extraction of scattering parameters, the high frequency performance of the devices can be investigated. The unity short-circuit current gain frequency f_T, and the maximum oscillation frequency f_{max}, are two standard figure of merits for dynamic transistor performance. f_T and f_{max} are highly dependent on gate length, but in short-channel devices the respective values become scattered over a wider frequency range [9, 26]. f_T is limited by the short-channel effects [20, 22, 25, 26] and f_{max} is sensitive to the output conductance, variations in materials, contacts and other processing parameters [9, 23, 26, 27]. Traps in the semiconductor can also deteriorate the high-frequency and power performance of the HEMTs [21]. This degradation is due to a reduction of the on-state conductance [23, 27], which in turn varies with differences in sheet resistance and contact resistance [27].

f_T is deduced from the hybrid parameter h_{21}, which can be transformed from the measured S-parameters as in (9). The h_{21}-data is extrapolated with a slope of -20 dB/dec, and $f_T$is found at the 0 dB intersection [9, 23].

$$h_{21} = \frac{-2S_{21}\sqrt{Re\{Z_S\}Re\{Z_L\}}}{(1-S_{11})(Z_L^* + S_{22}Z_L) + S_{12}S_{21}Z_L} \tag{9}$$

Z_S, Z_L are the source and load impedances of the system [29]. Values of f_{max} are similarly achieved by extrapolating the values of the unilateral gain U, which can be transformed from S-parameters as in (10), where **1** is a unit matrix and $\boldsymbol{S}$ is the scattering parameter matrix [30].

$$U = \frac{|S_{12} - S_{21}|^2}{det[\mathbf{1} - \boldsymbol{S}\boldsymbol{S}^*]} \tag{10}$$

To evaluate the degradation of f_T and f_{max} as the gate length varies, the $1/L_g$ line is often introduced. Alternatively, the product $f_T \cdot L_g$ is calculated. f_T increases with decreasing gate length but falls short of the $1/L_g$ line, due to the short-channel effects and the fringing capacitance [26].

Under low frequency conditions, the output conductance $g_{ds,ext}$ and the maximum transconductance $g_{m,ext}$, can be derived from the Y-parameters according to (11) and (12).

$$g_{ds,ext} = \frac{Re\{Y_{22} - Y_{12}\}}{W_g} \tag{11}$$

$$g_{m,ext} = \frac{Re\{Y_{21} - Y_{12}\}}{W_g} \tag{12}$$

3

Recessed Ohmic Contact Formation

For the efficient operation of a HEMT, the metal contacts should have a negligible impact on the overall total resistance of the device. The contact resistance is sensitive to the choice of recess etch depth, the metals in the contact layer stacks and the anneal time and temperature. These parameters also vary for different semiconductor epi-layer structures.

Previous research on the most commonly used AlGaN/AlN/GaN heterostructures indicate that recessed ohmic contacts enable low contact resistance. It is particularly of interest to study the behaviour of contacts that have been recess etched down to different depths close to the substrate channel [4]. In this work, the etch depth was altered for already proven Ta/Al/Ta contacts. These contacts have shown very low contact resistance and have the advantage of a low optimal anneal temperature [15].

The metals used in the contact layer stacks play an important role for the ohmic contact formation. The effect of applying a Au layer to the Ta/Al/Ta metal stack was tested. The Au layer prevents oxidation of the contact and is presumed to form Ga-vacancies in the semiconductor, which would lower the contact resistance. However, Au is believed to cause long-term contact degradation and is also best avoided in Si-fabrication laboratories [31].

Another option that will be explored is Zr-based contacts, with altering contact metal layer stacks and varying layer thicknesses. The ZrN, formed in between the contacts and semiconductor during anneal, has much lower resistivity than TaN, and this makes Zr-based contacts interesting for ohmic contact formation. Previous tests on Zr/Al/Zr contacts have not yet yielded notable results but may have the potential to do so.

3.1 Experimental Procedure

For the contact formation study, the linear transfer length method was used, as further described in 2.4.1. The fabrication of TLM structures involves several steps but is mainly divided into the parts of mesa isolation, ohmic recess, evaporation, and anneal.

All samples in the ohmic contact formation tests originated from the same 4” wafer, which had a standard epitaxial layer structure. It consisted of a GaN buffer layer, an AlN spacer, an $Al_{0.29}Ga_{0.71}N$ barrier, a GaN cap and a SiN_x passivation layer, in accordance to Table 2.

The fabrication procedure was identical for all samples except for the time of the GaN/AlGaN recess etch, the contact metal layer stacks, the metal layer thicknesses, the anneal time and anneal temperature.

Table 2: Epitaxial layer structure of the material used in the contact formation study.

Layer	Material	Thickness
Passivation	SiN_x	10 nm
Cap	GaN	3 nm
Barrier	$Al_{0.29}Ga_{0.71}N$	17 nm
Spacer	AlN	0.8 nm
Buffer	GaN	1700 nm

Mesa and ohmic contact definition was done by standard UV-photolithography. The Oxford Plasmalab 100 ICP/RIE was used for NF_3-etch of the Si-based passivation layer and Cl_2/Ar-etch of the GaN-related materials. Mesa isolation required a SiN_x-etch with an RF-power of 25 W, ICP-power of 60 W, chamber pressure of 5 mTorr, and NF_3-flow of 50 sccm. The duration of the SiNx-etch was set to 2 min, which was considered an over etch. It should however not affect the thickness of the underlying GaN-based layers.

The Cl_2/Ar-etch operated with an RF-power of 100 W, ICP-power of 50 W, chamber pressure of 3 mTorr, Cl_2/Ar-flow of 20/10 sccm, and a duration of 2 min 40 s. The Dektak 150 mechanical surface profiler was used to measure the total mesa etch depth, which was found to be 255 ± 2.5 nm. Assuming the GaN-based layers are etched at a constant pace, this corresponds to an etch rate of approximately 1.53 nm/s.

Ohmic recess was formed by NF_3- and Cl_2/Ar-etching after a conditioning with Cl_2/Ar plasma at high power levels for 5 minutes. The SiN_x-etch settings were the same as for mesa isolation. The low power Cl_2/Ar-etch used an RF-power of 25 W, ICP-power of 25 W, chamber pressure of 3 mTorr, and Cl_2/Ar-flow of 40/10 sccm. Various Cl_2Ar-etch durations were to be tested, ranging from 65 to 115 s. The target was to look into recess depths reaching from just above the 2DEG channel and extending down into the substrate. The depths were measured after metallization to range from 13 to 34 nm. The etch rate was 0.25 ± 0.05 nm/s.

The metal contacts were deposited by a Lesker Spectros UHV electron beam evaporator and annealed in an AccuThermo AW610 rapid thermal processing chamber in nitrogen ambient on a graphite carrier, with the temperature being determined by a pyrometer. A Keithley 4200-SCS parameter analyzer was used to measure IV-characteristics by 4-point TLM-measurements, enabling calculations of specific contact resistivity, contact resistance, sheet resistance and transfer length.

3.2 Ta-based Contacts

Ta/Al/Ta contacts to AlGaN/AlN/GaN heterostructures with a contact resistance of 0.06 Ωmm have been reported [15], and Ta/Al/Ta contacts to InAlN/AlN/GaN HEMTs have shown a contact resistance of 0.14 Ωmm at an optimum recess etch depth close to the substrate channel [4], which was 7 nm as the InAlN/AlN was 7.8 nm thick. While testing varying metal stack layer thickness and anneal, both of these results were obtained for a metallization of 5/280/20 nm and an anneal temperature of 550°C. Ta/Al/Ta contacts were also shown to be less sensitive to Al layer thickness compared to Ti/Al contacts [15].

In this attempt, the contact metal stacks, from bottom to top, consisted of 10 nm of Ta, 28 nm of Al and 20 nm of Ta. Adding a 40 nm Au layer to the top of the metal stack was also tested for an AlGaN/GaN etch of 85s. Anneal and TLM measurements were conducted in steps, according to Table 4.

Table 4: Anneal procedure for the Ta-based contact tests. TLM measurements were performed after each anneal step.

Anneal step	Temperature	Time
Anneal 1	500°C	2 min
Anneal 2	525°C	2 min
Anneal 3	550°C	2 min
Anneal 4	550°C	2 min
Anneal 5	550°C	4 min
Anneal 6	550°C	8 min
Anneal 7	575°C	2 min
Anneal 8	600°C	2 min
Anneal 9	600°C	2 min
Anneal 10	600°C	4 min
Anneal 11*	650°C	1 min
Anneal 12*	650°C	1 min
Anneal 13*	650°C	2 min

* Only for Ta/Al/Ta/Au contacts.

The results for the minimum obtained contact resistance are presented in Table 3. The results were averaged over at least three measurements. The sheet resistance for all measurements, with exception to the results from Anneal 1 which showed lower values for R_{sh}, ranged in between 260-350 Ω/□.

Table 3: TLM measurement results for Ta/Al/Ta contacts with a recess etch varying between 13 and 34 nm.

Recess etch		Optimum					
Time [s]	**Depth [nm]**	**anneal**	R_C **[Ωmm]**	R_{sh} **[Ω/□]**	L_T **[µm]**	ρ_C **[10^{-6} Ωcm^2]**	**Correlation**
65	13	Anneal 8	0.65	318	2.1	13.4	0.99999
74	17	Anneal 5	0.42	295	1.4	5.90	0.99999
80	-	Anneal 6	0.41	341	1.2	5.00	0.99841
85	19	Anneal 5	0.41	294	1.4	5.60	0.99996
85	-	Anneal 6	0.38	345	1.1	4.20	0.99875
85	23	Anneal 6*	0.39	302	1.3	5.00	0.99998
90	-	Anneal 6	0.43	332	1.3	5.60	0.99962
100	30	Anneal 6*	0.47	306	1.5	7.04	0.99995
115	34	Anneal 6*	Not ohmic				

* Performed anneal only at 550°C for 16 min and 600°C for 1+3 min.

The combined thickness of the layers on top of the buffer is 20.8 nm, according to the epi-specifications in Table 2. The etch depths close to the 2DEG corresponds to etch times of 80-90 s. For these etch times, the results of minimum contact resistance versus temperature are plotted in Figure 6. The results

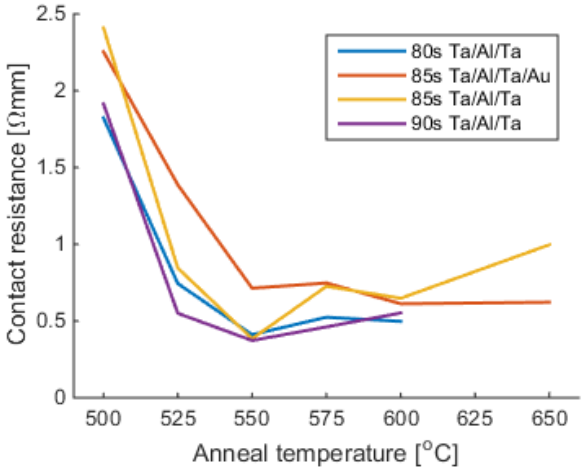

Figure 6: Minimum contact resistance for three types of Ta/Al/Ta contacts, recess etched for 80, 85 and 90 s, and Ta/Al/Ta/Au contacts that have been recess etched for 85 s.

from application of an additional Au layer are also included in the figure.

From the results in Table 3 and Figure 6, it can be seen that the Ta/Al/Ta-samples all reached optimal contact resistance after 8 or 16 min of anneal at 550°C, while the Ta/Al/Ta/Au contacts kept improving to a minimum contact resistance of 0.61 Ωmm as the anneal temperature was increased to 600°C.

Optical micrographs of the contact surface were obtained for both types of metal contacts. In Figure 7, the surface morphology and edge acuity can be studied for Ta/Al/Ta contacts and Ta/Al/Ta/Au contacts,

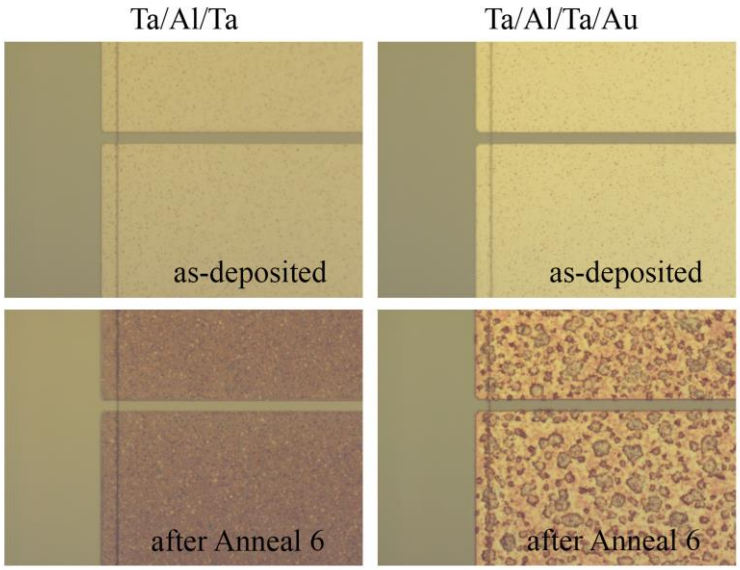

Figure 7: Optical micrographs of the surface of the TLM structures of Ta/Al/Ta and Ta/Al/Ta/Au contacts.

recesses etched for 85 s, as-deposited and after Anneal 6. The morphology of the Ta/Al/Ta contacts stayed the same throughout the entire anneal procedure. The Ta/Al/Ta/Au obtained a rough morphology already at first anneal and then stayed the same for the remainder of the anneal steps.

3.3 Zr-based Contacts

Zr-based contacts have not yet come to deliver low-resistive ohmic contacts to GaN heterostructures. The low resistivity of ZrN shows promise and Zr-based contacts also require lower anneal temperatures than Ti-based contacts.

Previous research has found that there is a relation between the thickness of the Al layer and the bottom metal layer that yields an optimum contact resistance. In Ta-based contacts the ratio $\frac{t_{Al}}{t_{Ta}}$ is estimated to be between 14 to 28 [4, 15], while Zr-based contacts are more similar to Ti-based contacts, thus the ratio $\frac{t_{Al}}{t_{Zr}} \approx \frac{t_{Al}}{t_{Ti}} = 5.5$. The notion of using Zr/Al/Zr in a certain thicknesses ratio was here combined with using the result of an AlGaN/GaN recess etch time of 85 s from the previous test in Section 3.2.

The Zr/Al/Zr stack consisted of 20 nm of Zr, 110 nm of Al and 20 nm of Zr. On top of these three layers, a combination of Ta/Au, and one of Ti/Ta/Au were added. The thickness of the Ta/Au was 20/20 nm. Zr/Al/Zr/Ti contacts and plain Zr/Al/Zr contacts were also tested.

The anneal and TLM measurement procedure was conducted with focus on temperature. The procedure can be seen in Table 5, where the temperature was raised in steps of 50°C from the starting temperature of 500°C up to 800°C. Not more than one minute of anneal was performed in each step.

Table 5: Anneal procedure for the Zr-based contact tests. TLM measurements were performed after each anneal step.

Anneal step	Temperature	Time
Anneal 1	500°C	1 min
Anneal 2	550°C	1 min
Anneal 3	600°C	1 min
Anneal 4	650°C	1 min
Anneal 5	700°C	1 min
Anneal 6	750°C	1 min
Anneal 7	800°C	1 min

During anneal, the surface morphology changed considerably for the Zr/Al/Zr/Ta/Au and Zr/Al/Zr contacts, while the stacks with Ti stayed relatively smooth, which shows the robustness of the metal. The mayor change occurred already at the first anneal and then the morphology stayed almost the same throughout the subsequent anneal steps. The surface morphology for the contacts after Anneal 1 is shown in Figure 8.

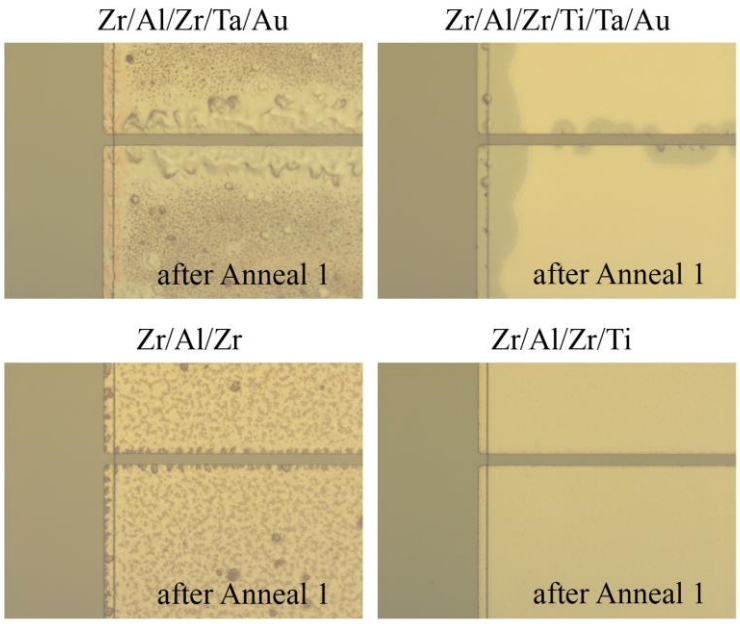

Figure 8: Optical micrographs of the surface morphology of Zr-based contacts after anneal at 500°C for 1 min.

The Zr/Al/Zr and Zr/Al/Zr/Ti contacts showed non-ohmic behaviour with significant variations in the measured resistance. The observed values of the measured resistance were also very high, in the order of kΩs, and the mean correlation was as low as 38 % and 24 % respectively.

The Zr/Al/Zr/Ta/Au contacts delivered ohmic characteristics with high correlation. The measured resistance was consistent and low, below 200 Ω, and the results from TLM measurements for the entire anneal procedure are seen in Table 6. According to Figure 9, the optimum contact resistance was achieved after anneal at 650°C. The same minimum contact resistance was almost reached after anneal at 700°C.

Table 6: TLM measurement results for Zr/Al/Zr/Ta/Au contacts to AlGaN/AlN/GaN heterostructures.

Anneal step	R_C [Ωmm]	R_{sh} [Ω/□]	L_T [μm]	ρ_C [10^{-6} Ωcm^2]	Correlation
Anneal 1	Not ohmic				
Anneal 2	2.36	385	6.1	145	0.99336
Anneal 3	1.09	320	3.4	37	0.99972
Anneal 4	0.87	341	2.6	22	0.99984
Anneal 5	0.88	345	2.5	22	0.99972
Anneal 6	1.42	341	4.2	60	0.99972
Anneal 7	1.47	305	4.8	70	0.99988

Zr/Al/Zr/Ti/Ta/Au contacts gave results with a mean correlation of 93 %, although the measured resistance was still high and significantly varying over the voltage sweep. The calculated minimum contact resistance for these contacts was as high as 4.33 Ωmm.

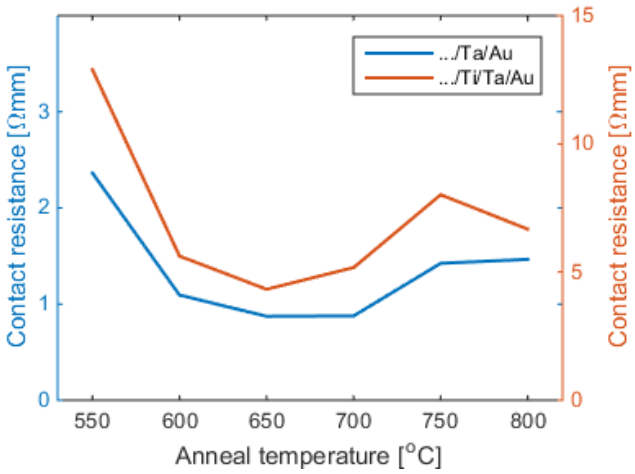

Figure 9: Minimum contact resistance for Zr/Al/Zr/Ta/Au contacts to the left, and Zr/Al/Zr/Ti/Ta/Au contacts to the right.

3.4 Summary & Discussion

It was shown that contact resistance for Ta/Al/Ta contacts on standard AlGaN/AlN/GaN semiconductor material was minimized as the contact metal stack was recess etched 22 ± 2 nm, close to the substrate channel. The resulting minimum contact resistance of 0.38 Ωmm was relatively insensitive to etch times of 85 ± 5 s. In accordance to previous research, the optimal contact resistance was achieved by etching down to depths close to the 2DEG in the buffer.

The best results were gained after anneal at 550°C for a total of 16 min. This optimal anneal temperature is what was expected, and it is very low compared to the anneal temperature of standard Ti-based contacts. According to Figure 7, the Ta-based contact structures had well-defined edges, and a smooth enough morphology. The effect of the choice of anneal procedure on contact resistance has not been examined. It is presupposed that other methods of anneal, such as a sloped anneal or multistep anneal, would make a difference in the resulting contact properties. Although, the gain in terms of lowered contact resistance would most likely be insignificant in the context.

Applying Au to the top of the Ta/Al/Ta-stack did not yield any improvement to the contact formation. The surface morphology in Figure 7 was deteriorated and the contact resistance reached a minimum of 0.61 Ωmm, which is 0.23 Ωmm higher than without the 40 nm of Au. A higher anneal temperature was also required. So, the Au layer did not better the performance of the contacts and can best be avoided.

The sheet resistance of the Ta-based contacts ranged in between 260-350 Ω/□, and this low and narrow range reinforces the validity of the TLM measurement results, along with the high values of correlation. Overall, the Ta/Al/Ta contacts to AlGaN/AlN/GaN show good performance and fabrication repeatability. Additional research on metal layer stack combinations and thicknesses for Ta-based contacts show potential for further improvement.

The Zr-based contacts did not reach the desired performance. It was however found that Au has an impact on Zr/Al/Zr contact formation. Relevant results were only gained for the Zr/Al/Zr/Ta/Au contacts after anneal at 650°C, and the minimum contact resistance obtained was 0.87 Ωmm. The other types of

contacts, Zr/Al/Zr, Zr/Al/Zr/Ti and Zr/Al/Zr/Ti/Ta/Au, where either non-ohmic or showed values of contact resistance that were altogether too high.

In order to determine whether Zr-based contacts can be useful or not, more tests need to be conducted. An interesting approach is to measure Zr/Al contacts with various metal layer combinations and thickness of Zr, Ni, Ta and Au stacked on top. Other exclusion layer compounds such as HfN, NbN and VN, also have a lower resistivity than TaN, and might be interesting to follow up on.

4

Fabrication of HEMTs

The enhanced carrier concentration and mobility of C-doped InAlN/AlN/GaN HEMTs makes it possible to improve high frequency performance while scaling down the devices. The high polarization discontinuities of InAlN and AlN enable thinner barrier and spacer layers which in turn increases the aspect ratio and limits the short-channel effects. The impact of different carbon doping profiles of the GaN buffer layer will be investigated.

Prior to the fabrication of the HEMTs, the processing of the InAlN/AlN/GaN materials needs to be optimized for lowest contact resistance. The results of the contact formation tests in Chapter 3 will be applied to Ta/Al/Ta contacts for the new compound semiconductor materials. Based on previous results, TLM structures will be fabricated and measurements of these structures will supply appropriate settings for optimal recess etch and anneal.

Once the contact resistance has been optimized for each material, the HEMTs can be fabricated. The main process steps involve mesa isolation, contact recess, evaporation and anneal, forming of gates, contact pad application, and deposition of the passivation layer. With exception to which photolithography mask that is used, the steps of mesa and contact formation are the same for the TLM structures as well as for the HEMTs.

4.1 Material specification

The sample materials originated from three different 3" wafers, which consisted of similar composite semiconductor structures having a variation in carbon doping in the buffer. The epitaxial layer structures can be studied in Table 7. The materials have a slightly varying In concentration in the barrier layer and in the combined thickness of the barrier and spacer.

The main difference in the materials lie in the C-doping of the GaN buffer, which is described in Figure 10. Material (a) *Low-C* is only intrinsically doped and has no carbon compensation in the buffer, material (b) *Ramped-C* has a carbon doping with a ramped profile rising from $2 \cdot 10^{17}$ cm^{-3} to $1 \cdot 10^{18}$ cm^{-3} and material (c) *High-C* has a constant carbon concentration of about $4 \cdot 10^{17}$ cm^{-3}. Materials (b) and (c) have an unintentionally doped channel region of 90 nm on top of the C-doped GaN in order to avoid current collapse.

Table 7: Epitaxial layer structures of the three InAlN/AlN/GaN materials used in the study of the impact of different GaN buffer C-doping profiles on short-channel effects. (a) The Low-C material with intrinsic C-doping of ~10^{16} cm^{-3}, (b) the Ramped-C material with C concentration ranging from $2 \cdot 10^{17}$ cm^{-3} to $1 \cdot 10^{18}$ cm^{-3} in the C-doped GaN, and (c) the High-C material with C concentration of $2 \cdot 10^{17}$ cm^{-3}.

	Wafer	Layer	Material	Thickness
(a)	TS320 w6 *Low-C*	Barrier	$In_{19.8}Al_{80.2}N$	8 nm
		Spacer	AlN	
		Channel	GaN	1700 nm
(b)	TS565 w6 *Ramped-C*	Barrier	$In_{18.5}Al_{81.5}N$	7.3 nm
		Spacer	AlN	
		Buffer	GaN	90 nm
		Buffer	C-doped GaN	1700 nm
(c)	TS738 *High-C*	Barrier	$In_{17.3}Al_{82.7}N$	7.8 nm
		Spacer	AlN	
		Buffer	GaN	90 nm
		Buffer	C-doped GaN	1700 nm

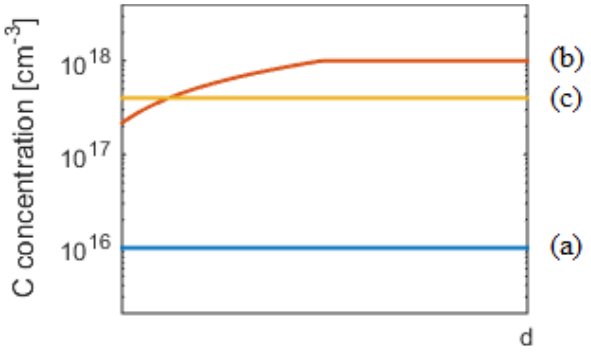

Figure 10: GaN buffer layer C-doping profiles of the three materials (a) Low-C, (b) Ramped-C and (c) High-C, referring to the wafers TS320 w6, TS565 w6 and TS738 respectively.

Table 8: Values of charge density and sheet resistance provided by the epi-grower, for the three materials.

	n_S [10^{13} cm^{-2}]	R_{sh} [Ω/□]
Low-C	1.72	251
Ramped-C	2.08	215
High-C	1.70	206

The epi-grower provided measured values of the sheet charge density n_S and the sheet resistance R_{sh}, which are listed in Table 8. In order to compare the materials during the characterization in the following chapter, the aspect ratios were calculated for three different transistor gate lengths in Table 9, with values for the barrier-spacer thickness in Table 7 set as gate-to-channel distance.

Table 9: Calculated aspect ratio $\frac{L_g}{d}$ for the three materials, where L_g is the gate length and d is the gate-to-channel distance of the material.

	$L_g = 50$ nm	$L_g = 100$ nm	$L_g = 180$ nm
Low-C	6.25	12.5	22.5
Ramped-C	6.85	13.7	24.7
High-C	6.41	12.8	23.1

4.2 Experimental procedure

The fabrication of TLM structures was identical for all samples. Standard lithography was used for mesa isolation with a positive resist and exposure in a mask aligner for UV-photolithography. Since there was no initial passivation or cap on top of the barrier layer, a Cl_2Ar etch was sufficient for mesa isolation. Both mesa and recess etch was performed by the Oxford Plasmalab 100 ICP/RIE. For the mesa isolation, an RF-power of 100 W, ICP-power of 50 W, and a chamber pressure of 3 mTorr was applied. The gas flow was set to 20 and 10 sccm respectively for Cl_2 and Ar.

Ohmic contact lithography by a DWL 2000 laser pattern generator was done on reversible resist. To ease the focusing of the laser, a layer of chromium was applied prior to exposure and then etched away with Ni/Cr etchant. The recess etch was initiated with a high power conditioning session and then operated with an RF- and ICP-power of 25 W, chamber pressure of 3 mTorr, Cl_2-flow of 40 sccm and Ar-flow of 10 sccm.

In these attempts, the depths of the recess etch were not measured. The results of the higher power mesa etch was measured with the Dektak 150 mechanical surface profiler. The mean mesa etch rate was 1.40 nm/s for the three materials. As the TLM structures were fabricated, the mesas were etched for a few tens of seconds longer than when the HEMTs were fabricated, in order to prevent parasitic resistances of the pads. The HEMT mesas were etched for 2 min 20 s and this yielded an average mesa etch depth of 189 nm.

Prior to metal contact evaporation, an oxide-strip was performed by immersing the samples for 4 min in $HF:H_2O$ 1:10, and 4 min in $HCl:H_20$ 1:10. The deposition of metal contacts was made by electron beam evaporation. The contacts were Ta-based and consisted of 5 nm of Ta, 280 nm of Al and 20 nm of Ta, from bottom to top. Anneal was performed by RTP in nitrogen ambient on a graphite carrier, with the temperature being determined by a pyrometer.

A Keithley 4200-SCS parameter analyzer was used to extract IV-characteristics by 4-point TLM measurements, enabling calculations of specific contact resistivity, contact resistance, sheet resistance and transfer length. The results from measurements on the TLM structures are shown in Figure 11 (a). It was found that the optimum recess etch time was 80 s for all of the materials, after anneal at 550°C for 10 min followed by 2 min at 575°C and 2 min at 600°C. Previous results suggest that the contact recess depth should be close to the channel in the buffer, which is at a depth of about 7.3 to 8 nm in these materials. This corresponds to an approximated etch rate of 0.10 nm/s.

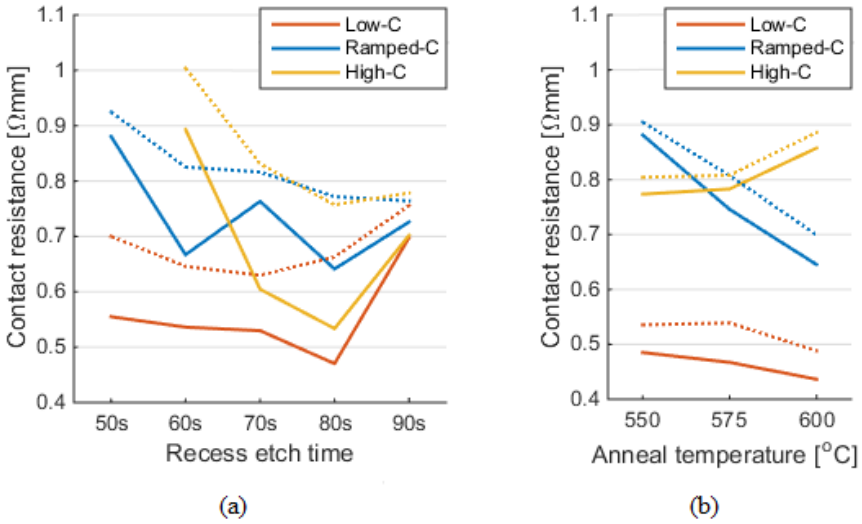

Figure 11: Measurement results for (a) the TLM structures, and (b) the HEMT TLM structures. The solid lines represent the minimum contact resistance while the dotted lines denote the mean value of all measurements taken.

From these results, the optimum etch time and anneal for HEMT fabrication was determined to be 80 s and 550/575/600°C for 10/2/2 min. The results from TLM measurements made on the same samples as the HEMTs were fabricated on are seen in Figure 11 (b). Unlike for previous samples, the contact resistance was no longer optimized at 600°C for the High-C material.

In Table 10, the TLM measurement results for the HEMT samples are stated. The Low-C material differed from the intentionally C-doped materials by having a lower contact resistance, transfer length and specific contact resistivity, while having a higher sheet resistance. The sheet resistances have an offset of about 60-80 Ω/□ compared to the values provided by the epi-grower, seen in Table 8. This is mainly due to the material changes the samples go through during fabrication of the devices.

Table 10: TLM measurement results, prior to passivation, for Ta/Al/Ta contacts to InAlN/AlN/GaN HEMTs.

	R_C [Ωmm]	R_{sh} [Ω/□]	L_T [µm]	ρ_C [10^{-6} Ωcm^2]	Correlation
Low-C	0.49	328	7.3	1.5	0.99999
Ramped-C	0.70	272	18	2.6	0.99998
High-C	0.89	285	28	3.1	0.99997

The fabrication of HEMTs continued with formation of T-gates by e-beam lithography, due to the delicate features of the gates. Also in this case a chromium layer was applied to ease focusing to the transparent samples by the JEOL JBX-9300FS high resolution e-beam lithography system. The evaporation of gate metals was done by a Lesker Spectros UHV e-beam evaporator and consisted of 30 nm of Ni with 300 nm of Au on top.

Application of the metal pads was done by laser lithography with reversible resist and electron beam evaporation of 30 nm of Ti with 300 nm of Au on top. Passivation of the devices was performed by the Oxford FlexAl system, in a plasma assisted ALD chamber at a temperature of 300°C. An initial conditioning preceded the Al_2O_3 deposition of 432 cycles. The operation was set to an RF-power of 400 W, O_2-flow of 60 sccm and trimethylaluminium Ar-purge of 60 sccm. The passivation was opened up on top of the pads by immersion in HF:H_2O 1:10 for 2 min. The thickness of the passivation layer was measured by the Dektak mechanical surface profiler to be 50 ± 5 nm.

The HEMTs fabricated in this section have two series gates, with gate widths of 2 x 25 µm and gate lengths of 50, 100 and 180 nm. An optical micrograph of the top view of one of the devices is presented in Figure 12. A model of the side view in cross-section of the device is shown in Figure 13. The lateral distances of the model has been reduced in order to save space, but otherwise it has accurate layout and vertical dimensions.

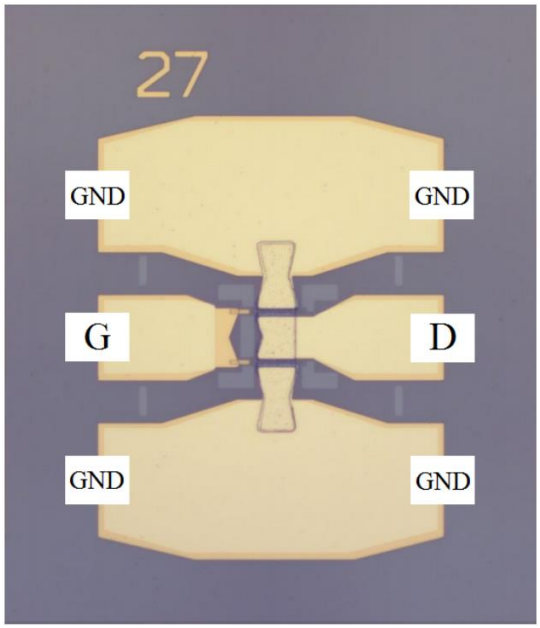

Figure 12: Optical micrograph of a finished HEMT, with two gates in series, each with a width of 25 µm and a gate length of 100 nm.

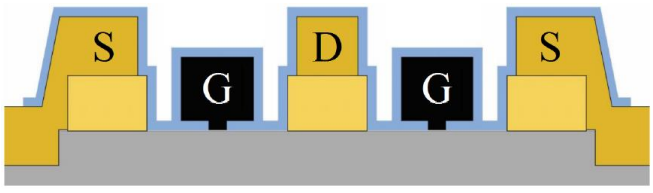

Figure 13: Cross section of a horizontal semiconductor HEMT with ohmic contacts at sources and drain. The lateral distances have been significantly reduced while the vertical distances are roughly proportional.

4.3 Summary & Discussion

The TLM measurement results for the samples with HEMTs in Table 10 showed good consistency with sheet resistances in a narrow enough range and high correlation factors. The sudden increase in contact resistance at higher anneal temperature for the High-C material is presumed to be related to a non-uniformity in the C-distribution over the wafer, which can be expected in highly C-doped structures [27].

The non-doped wafer stands out from the other two materials when it comes to sheet resistance, contact resistance, transfer length and specific contact resistivity. The Low-C material also etches slightly faster than the others, this could be due to the lower amount of impurities in the material. However, the Ramped-C shows the highest sheet charge density, while the other two are fairly equal. The Ramped-C material also has the highest aspect ratio, followed by the High-C and then the Low-C.

The contact resistance was determined to be 0.49, 0.70 and 0.89 Ωmm for the Low-C, Ramped-C and High-C material respectively, which was low enough to continue with fabrication of transistor devices. In order to reach low contact resistance, the materials required an unusually long oxide-strip of at least 4 min prior to contact metallization. The sheet resistance after processing of TLM structures was measured to be 60-80 Ω/□ higher than for the untreated material, when compared to measurement results provided by the epi-grower.

The optimum anneal temperature of 600°C was higher for Ta/Al/Ta contacts to InAlN/AlN/GaN tested in this chapter, than the 550°C for the Ta/Al/Ta contacts to AlGaN/AlN/GaN in the ohmic contact formation study. The contact resistance was degraded for the High-C material as it was annealed at 575°C and 600°C, which had previously not been shown by the contact tests. This is believed to be caused by non-uniformities in the wafer.

When fabricated, it is desired for the contact structures to have well-defined edges, and preferably a smooth morphology. The Ta/Al/Ta contacts to InAlN/AlN/GaN showed good surface morphology and line edge acuity for all samples.

The fabrication of HEMTs was impaired by an ohmic laser lithography that was not completely successful. The HEMT devices seemed to be unaffected but other structures on the samples showed bends of the ohmic layer in the gate area. There were also issues with the lithography and etching of the passivation openings. As the fabrication was complete, the devices showed extremely high resistances during DC measurements, until a point where they had been exposed to a certain amount of bias. This was attempted to be resolved by anneal at 300°C for 5 min. However, this seemed only to worsen the issue.

Overall, in this section three types of InAlN/AlN/GaN HEMTs with Low-C, Ramped-C and High-C doping profiles and of three different gate lengths were successfully fabricated with some minor issues which were mostly resolved.

5

Characterization of HEMTs

DC and S-parameter measurements are applied for HEMT characterization. The DC measured drain-induced barrier lowering, DIBL, which is a short-channel effect that influences transistors in both small signal and large signal analysis, is aimed to be as low and constant as possible. As the high-frequency performance is explored, high values of f_T and f_{max} are desired.

The devices under test are the InAlN/AlN/GaN HEMTs fabricated in Chapter 4 , seen in Figure 12. The two-finger, U-shaped devices have gate widths of 2 x 25 µm and gate footprints of 50, 100 and 180 nm. The gate pitch is 32.1 µm and the source-drain spacing is 2 µm.

The (a), (b) and (c) C-doping profiles seen in Figure 10 are associated with the Low-C, Ramped-C and High-C materials respectively. The aspect ratio is the highest for the Ramped-C devices, followed by the High-C and then the Low-C. The contact resistance was measured to be (a) 0.49 Ωmm for the Low-C, (b) 0.7 Ωmm for the Ramped-C and (c) 0.89 Ωmm for the High-C material. The specific contact resistivity and the transfer length follows the contact resistance. The sheet resistance is highest for the Low-C material, lower for the High-C and least for the Ramped-C.

DC-measurements of the HEMTs was performed by the Keithley 4200-SCS parameter analyzer, with voltages in between -10 and 1 V applied to gate, and 0 to 20 V applied to drain. DC measurements provide information on the amount of DIBL and subthreshold swing, as well as values for the transconductance g_m, pinch-off voltage V_{th} and saturated drain current I_{DSS}.

The high frequency performance of the HEMTs are determined by S-parameter analysis, and the extraction of the unity short-circuit current gain frequency f_T and the maximum oscillation frequency f_{max}. The output conductance $g_{ds,ext}$, maximum transconductance $g_{m,ext}$, and the product $f_T \cdot L_g$ can also be calculated for comparison. S-parameters were measured up to 110 GHz by a Cascade Microtech probe station, subsequent to calibration and surface alignment of the probes. The gate bias was swept from -5 to 1 V with a step of 0.5 V, while the drain bias ranged in between 0 and 15 V with a step size of 1 V.

5.1 DC characterization

The transfer and output characteristics of the three different C-doping profiles for a gate length of 100 nm is displayed in Figure 14. The data is averaged over measurements on 3 up to 7 separate devices. The Low-C HEMTs clearly have the lowest current flow and the least negative threshold voltage. The transconductance for the devices is plotted in Figure 15 and values for the pinch-off voltage at V_{ds} = 10 V, the maximum saturated drain current at V_{gs} = 1 V, and the maximum transconductance are listed in Table 11.

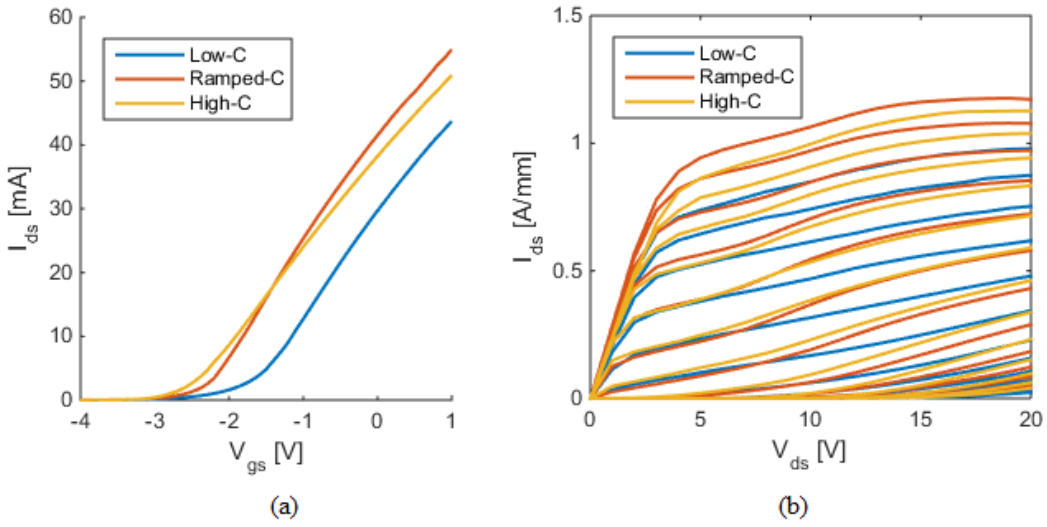

Figure 14: (a) Transfer and (b) output characteristics for the Low-C, Ramped-C and High-C devices, with a gate length of 100 nm. In (a) the drain bias is set to 10 V.

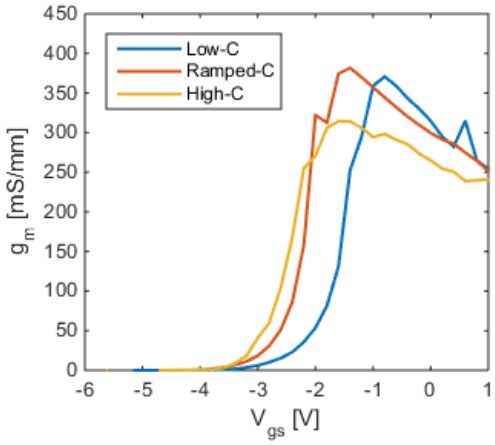

Figure 15: The transconductance of the 100 nm devices at V_{ds}=10V, corresponding to the data in Figure 14 (a).

The threshold voltage was found through association to the threshold current of 1 % of the maximum saturated drain current, as defined in (8), which was calculated to be 0.49, 0.59 and 0.56 mA for the Low-C, Ramped-C and High-C devices respectively. The transistors were difficult to fully pinch-off with an increasing drain bias. At V_{ds} = 15 V the Low-C, Ramped-C and High-C devices pinched of at -3.8, -4.1 and -4.0 V respectively. And as V_{ds} kept increasing to about 19-20 V, the devices would barely pinch-off at all.

Table 11: The pinch-off voltage V_{th}, saturated drain current I_{DSS}, and maximum obtained transconductance g_m, for the three different C-doping profiles. g_m was only measured up to a drain bias of 10 V.

	V_{th} @V_{ds}=10 V [V]	I_{DSS} @V_{gs}=1 V [A/mm]	g_m [mS/mm]
Low-C	-2.5	0.98	371
Ramped-C	-2.8	1.18	382
High-C	-2.9	1.13	315

The V_{th} shift can be studied in Figure 16 (a), where the threshold voltage becomes more negative with increasing drain voltage. The V_{th} shift in terms of DIBL is seen in Figure 16 (b). The High-C device clearly performs best compared to the others and the Ramped-C device behaves well in the region below V_{ds}= 10 V, but escalates for higher drain voltages.

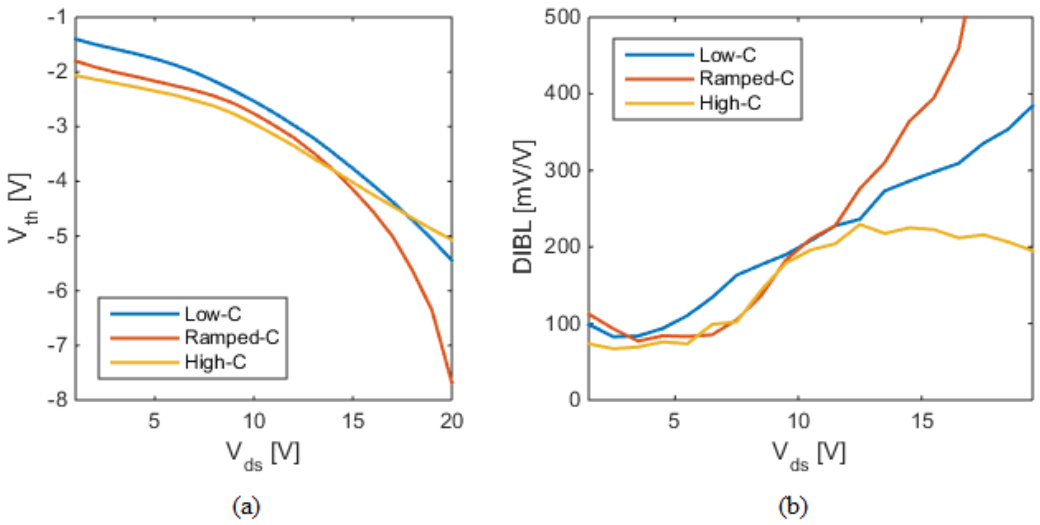

Figure 16: Threshold voltage versus drain bias and the calculated DIBL for the 100 nm transistors.

In Figure 17 (a) and (b), the DIBL is presented for two different drain voltages, in relation to the gate length of the devices. The amount of DIBL is the highest for the Ramped-C device at both biases, and the High-C devices show best performance.

Due to the inability to completely pinch the very short 50-nm-gate-length transistors, the DIBL in Figure 17 was estimated through linear extrapolation of the threshold down to the voltage which would correspond to 1 % of the maximum saturated drain current. The High-C 50-nm devices were just able to pinch-off at 20 V while the Low-C and Ramped-C devices did not go below 1.18 % and 3.25 % of I_{DSS} in drain current respectively.

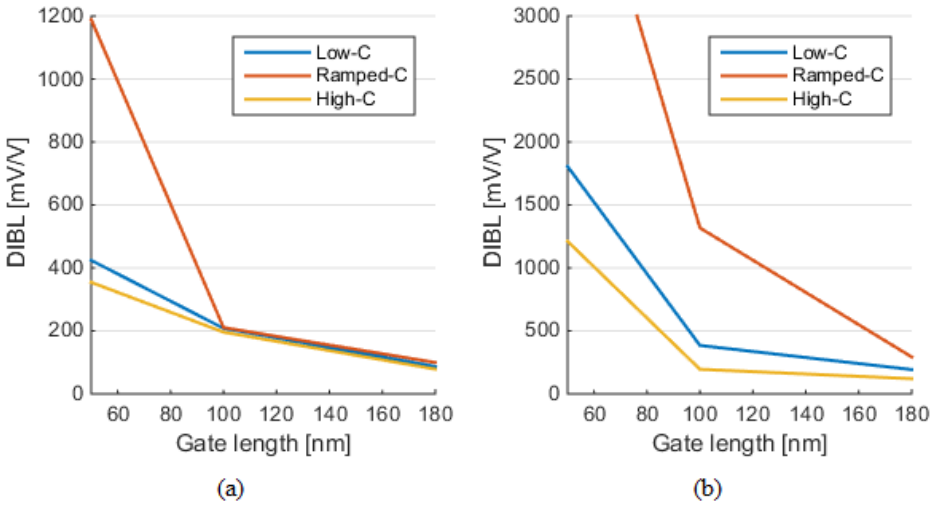

Figure 17: The amount of DIBL relative to gate length, for (a) V_{ds} = 10 V, and (b) V_{ds} = 20 V.

The current flow of the transistors with a gate length of 100 nm are plotted in Figure 18 (a). Overall, the Low-C devices have the lowest current leakage, followed by the High-C and lastly the Ramped-C devices. The subthreshold swing of the transistors is plotted in Figure 18 (b). The High-C devices perform the best over the entire drain voltage span, and the Ramped-C transistors only have a slight improvement in performance for the region in between a drain bias of 3 and 14 V, compared to the Low-C devices.

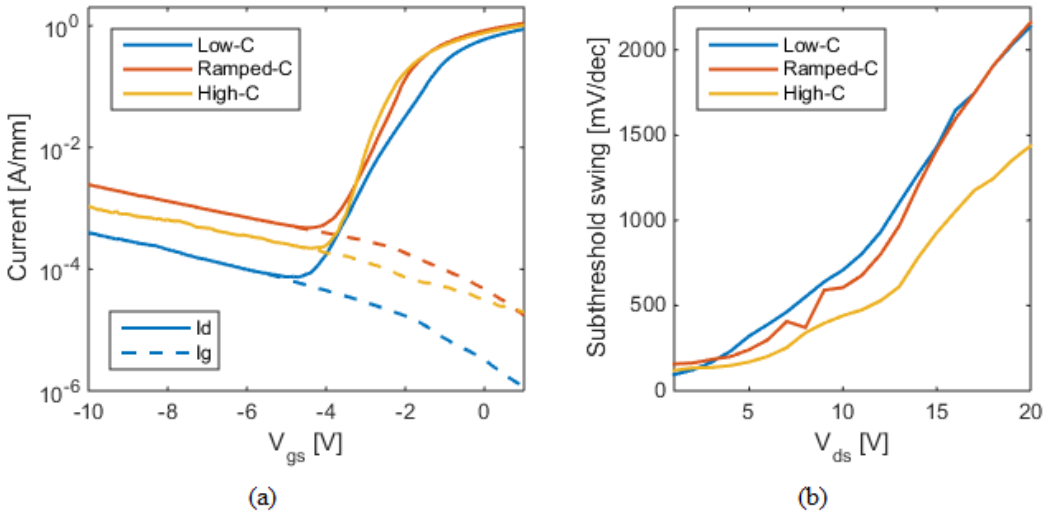

Figure 18: (a) The drain and gate currents versus gate bias at V_{ds} = 10 V, and (b) the subthreshold swing for varying drain bias. The measurements in (a) and (b) correspond to devices with a 100 nm gate length.

In Figure 19 (a) and (b), the subthreshold swing is presented for two different drain voltages, in relation to the gate length of the devices. The overall best performance is obtained by the High-C HEMTs. The Low-C and Ramped-C devices have similar levels of subthreshold swing but the Low-C devices perform slightly better and are more consistent in their behaviour.

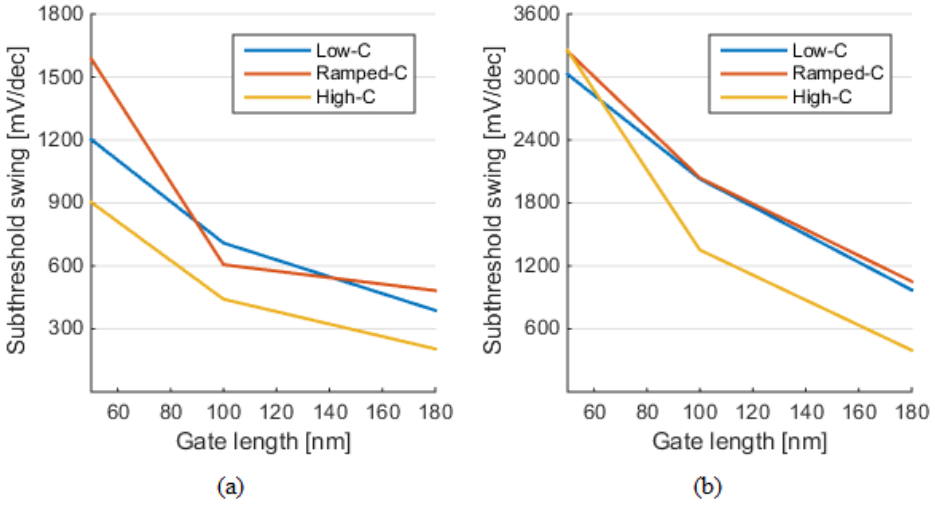

Figure 19: The subthreshold swing versus gate length, for (a) V_{ds} = 10 V, and (b) V_{ds} = 20 V.

Hall measurements were performed to extract values of sheet charge density, mobility and sheet resistance. The results are listed in Table 12 and the Low-C material shows the lowest charge density and mobility while having the highest sheet resistance. The intentionally C-doped materials are much more similar in terms of these parameters.

Table 12: Sheet charge density, mobility and sheet resistance for the three differently C-doped materials.

	n_S [cm^{-2}]	μ [cm^2/Vs]	R_{sh} [Ω/□]
Low-C	1.5	1580	257
Ramped-C	1.8	1615	215
High-C	1.9	1705	197

5.2 S-parameter analysis

The contour lines of the magnitude of the unity short-circuit current gain frequency f_T and the maximum oscillation frequency f_{max}, for a device with a Low-C doping profile and a gate length of 100 nm, are depicted in Figure 20 (a) and (b) respectively. For high values of f_T, the optimum bias point was at V_{gs} ≈ -1 V and V_{ds} ≈ 7 V. For a high f_{max}, the optimum bias was as V_{gs} was set to -1.5 and -2.0 V for the Low-C and intentionally C-doped devices respectively, and V_{ds} set above 15 V.

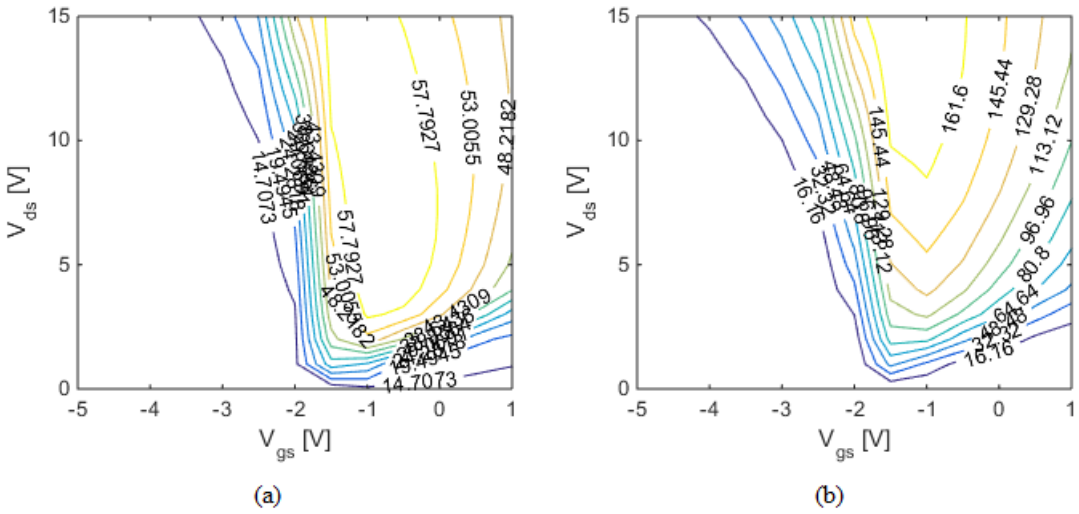

Figure 20: (a) f_T, and (b) f_{max} for devices with a Low-C doping profile and a gate length of 100 nm.

Values for maximum f_T and f_{max} where obtained for all three C-doped materials and for three different gate lengths for the unintentionally doped devices, seen in Table 13. The results were averaged over the performance of two separate devices. The Low-C and High-C devices have the best performance in terms of maximum f_T and f_{max}. A shortened gate length yields much higher values of f_T and $f_{\max}$.

Table 13: Values of f_T and f_{max} for devices with (a) a gate length of 100 nm, and (b) a Low-C doping profile.

		f_T [GHz]	f_{max} [GHz]
(a)	Low-C	63	176
	Ramped-C	66	180
	High-C	58	143
(b)	L_g = 180 nm	48	144
	L_g = 100 nm	63	160
	L_g = 50 nm	83	206

The output conductance $g_{ds,ext}$ and the maximum transconductance $g_{m,ext}$, was extracted from measured S-parameters at low frequencies, and the results are shown in Table 14. The Low-C devices exhibit the lowest output conductance and the Ramped-C the highest. The transconductance is highest in the Ramped-C devices, followed by the Low-C devices, while the High-C devices yield much lower values.

Table 14. Output conductance and maximum transconductance for the devices with a gate length of 100 nm, extracted from measured S-parameters.

	$g_{ds,ext}$ [mS/mm]	$g_{m,ext}$ [mS/mm]
Low-C	18.9	377
Ramped-C	24.2	407
High-C	21.7	323

5.3 Summary & Discussion

The DC and RF performance of three types of HEMTs with varying C-doping profiles was investigated in this chapter. It was shown that the levels of DIBL and subthreshold swing was reduced in highly C-doped devices, although the values of f_T and f_{max} were reduced as well.

In order to lower the amount of short-channel effects, the carrier confinement and gate modulation was improved by intentional C-doping. However, instead of lowering the current leakage and improving pinch-off, the higher C-doping together with a high carrier mobility lead to higher saturated drain current and overall current leakage. The slightly higher aspect ratio of the intentionally C-doped devices was not enough to overcome these effects and lower the leakage currents.

A more negative threshold voltage was also observed for the intentionally doped devices compared to the Low-C devices. The ability to fully pinch-off of the devices was improved in the High-C transistors by the improved carrier confinement, while the Ramped-C devices were the most difficult to pinch-off as the gate lengths decreased down to 50 nm.

The Ramped-C devices have the highest maximum transconductance, followed by the Low-C devices, while the High-C devices experience a significant reduction in peak transconductance. This could be explained by the greater contact resistance and presumably an increased 2DEG density in the High-C devices, and the improved mobility in the Ramped-C compared to the Low-C HEMTs. The sheet resistances obtained from Hall measurements showed consistency with the sheet resistances provided by the epi-grower, and the Hall measured carrier mobility.

The Ramped-C devices suffered most from DIBL and subthreshold swing with its high levels of output conductance and threshold voltage drift. In terms of f_T and $f_{\max}$, the Ramped-C devices gave the best results due to their high transconductance, but the performance was nearly matched by the unintentionally C-doped devices, which additionally showed much better immunity to short-channel effects. The High-C devices suppressed the DIBL and lowered the subthreshold swing but were limited in RF performance.

6

Conclusion

The downscaling of HEMTs leads to improved high frequency and power performance but also induces an increase in short-channel effects. The levels of DIBL and subthreshold swing in InAlN/AlN/GaN HEMTs are reduced by constant GaN-buffer C-doping. This improves carrier confinement and enhances the modulation efficiency of the electrons in the channel, in addition to improving the device pinch-off. However, the increase in deep level density and carrier concentration results in more negative threshold voltages and higher gate and drain current levels. But most importantly, this limits the on-state conductance and therefore reduces the high frequency and power performance of the devices.

A ramped GaN-buffer C-doping profile can in contrast improve f_T and $f_{\max}$, although devices of this type showed deteriorated performance in terms of short-channel effects, including pinch-off, output conductance and current leakage. Consequently, the buffer design can be optimized by the use of a ramped C-doping profile to increase RF performance, but poses a challenge in mitigating the short-channel effects for increased drain voltages.

In future work, the presence of filled traps in the near-gate region will be investigated by pulsed IV measurements. This will confirm the levels of dispersion in the C-doped materials. Measurements of low frequency S-parameters, and determining the output power density by load-pull will also yield valuable results.

Furthermore, Ta/Al/Ta contacts to AlGaN/AlN/GaN heterostructures have been found to be reproducible and to have good performance with concern to contact resistance and specific contact resistivity. The method of recessed etched contacts make best results for ohmic contact formation as the recess is close to the depth of the 2DEG channel, where a slight under or over etch is allowed. The Ta/Al/Ta contacts have a low optimal anneal temperature of 550°C, smooth surface morphology and precise line edge definition.

Zr/Al/Zr contacts to AlGaN/AlN/GaN heterostructures showed mostly non-ohmic behaviour, except for Zr/Al/Zr/Ta/Au contacts. Further research is required to estimate the applicability of Zr-based contacts.

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