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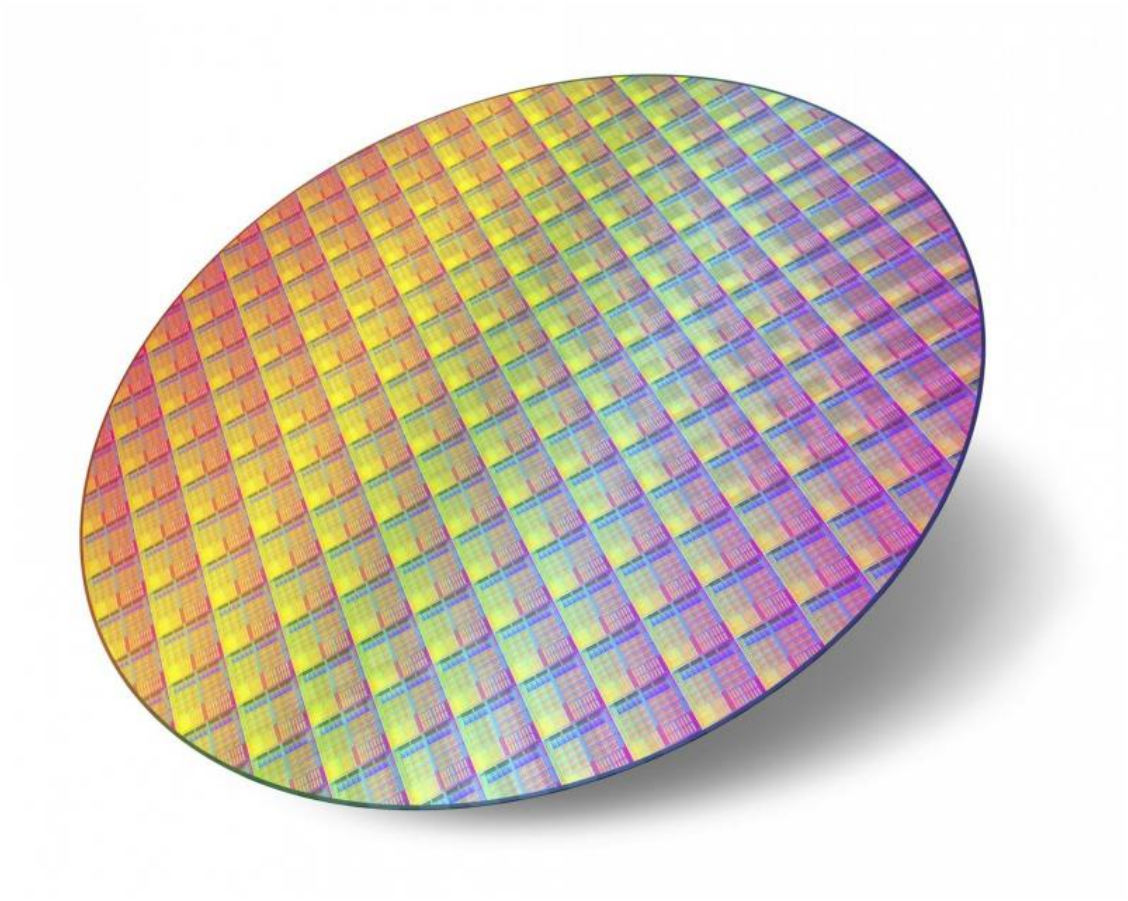

Measurements of different Silicon Carbide Transistors and their Varying Conduction Losses when used in Three-Phase Inverters

Bachelor's Thesis in Electrical Engineering

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Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2025
www.chalmers.se

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Abstract

In this bachelor thesis, the spread of $R_{\mathrm{DS(on)}}$ is measured and quantified for five SiC MOSFET samples from each of three different manufacturers. The resulting spread in on-state resistance was then applied theoretically to a three-phase inverter model in order to calculate the corresponding conduction loss variation. The conduction loss was determined using an algebraic equation based on the MOSFET parameters, specifically the on-state resistance and drain-source current. Finally, the measured maximum and minimum conduction losses were compared to typical values from each manufacturer's datasheet, with the results expressed as relative percentage deviations, scaled to represent the total conduction loss across all six MOSFETs in a three-phase inverter.

The results show that the spread of $R_{\mathrm{DS(on)}}$ was significant within each manufacturer, with standard deviations ranging from 3.1 mΩ for Onsemi to 6.4 mΩ for Infineon. This spread was calculated for two gate voltages. When the measured $R_{\mathrm{DS(on)}}$ values were used to calculate conduction losses, the variation resulted in substantial differences in total inverter loss. For Infineon, the conduction loss ranged from –34.8% to +42.4% relative to the typical datasheet-based value. STM exhibited the largest deviation, reaching up to +52.2%. In contrast, Onsemi showed a more modest variation, with losses between –7.7% and +26.5%. These findings highlight the importance of accounting for $R_{\mathrm{DS(on)}}$ spread when estimating conduction losses in practical three-phase inverter designs.

Keywords: Power electronics, SiC, MOSFET, Conduction losses, Python, Three-phase inverter

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This work has been carried out at the Department of Electrical Engineering. First, I would like to thank one of my favorite teachers at Chalmers, Thomas Hammarström, for helping me find this Bachelor's degree project. Without him, I wouldn't have been able to find one in time for graduation. Furthermore, I would like to thank my examiner, Torbjörn Thiringer, and especially my supervisor, Rafael Bausone Solano, for his never-ending support and valuable advice. Finally, I would like to thank the Division of Electric Power Engineering for providing hardware support for the measurements.

GEORGE KOURJIAN, Gothenburg, June 2025

Acronyms and Abbreviations

SiC	Silicon Carbide
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
$R_{DS(ON)}$	On-state drain-to-source resistance
V_{GS}	Gate-Source Voltage
V_{DS}	Drain-Source Voltage
I_{DS}	Drain-Source current
V_{TH}	Voltage Threshold
CSV	Comma Separated Values
Infineon	Infineon Technologies
STM	STMicroelectronics
Onsemi	On Semiconductor Corporation
μ	Mean
s	Sample Standard Deviation
PCB	Printed Circuited Board
M	Modulation index
φ	Power factor
DUT	Device Under Test
R_d	Diode resistance
V_d	Diode forward voltage drop

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1
Introduction

Silicon carbide (SiC) has emerged as a key enabler in the development of energy-efficient power semiconductor devices. Compared to conventional silicon-based components, SiC MOSFETs offer significantly lower conduction and switching losses, making them highly attractive for high-voltage, high-efficiency applications such as electric vehicles and renewable energy systems [5]. This chapter presents the problem background, describes the purpose and outlines the scope of the thesis.

1.1 Problem Background

SiC is a relatively new technology that has gained significant usage in recent years. In Chalmers University of Technology at the Division of Electric Power Engineering, we have access to three different types mentioned above. Unfortunately, all transistors are individual in nature, and designing a robust Three-Phase Inverter therefore requires knowledge of the parameter spread for each component. Ideally, it would be possible to create a design that can accommodate all three types, including their respective spread.

1.2 Purpose of the Thesis

The purpose of this thesis is to present and quantify the spread of $R_{\mathrm{DS(on)}}$ among three different manufacturers, and to theoretically implement the quantified results in a three-phase inverter design in order to calculate the resulting variation in conduction losses.

1.3 Delimitations

This project focuses mainly on the presentation and quantification of $R_{\mathbf{DS(on)}}$ among the three manufacturers, and on the resulting variation in conduction losses.

Although discussions with the examiner and supervisor considered the inclusion of additional parameters such as temperature dependence, threshold voltages, and switching losses, it was agreed that limiting the scope would ensure a balanced workload for the student. As a contribution to the Division of Electric Power Engineering, the author has nonetheless performed threshold voltage measurements for

the same SiC MOSFETs. While these are not analyzed in this thesis, the data have been made available for potential use in future research.

2

Theoretical Background

In this chapter, the author provides the method of how the spread of the on-state resistance $R_{\mathrm{DS(on)}}$ can be quantified for the SiC MOSFETs from different manufacturers and derives a simplified conduction loss equation for a three-phase inverter. The derivation isolates the contribution of the MOSFETs by excluding all other inverter components, such as the intrinsic body diode and the load. Through a series of justified assumptions, the full analytical loss expression is reduced to a form that depends solely on $R_{\mathrm{DS(on)}}$ and the drain current I_{DS}, enabling a focused analysis of conduction loss variation due to $R_{\mathrm{DS(on)}}$ differences between devices.

2.1 Quantification of $R_{\mathrm{DS(on)}}$ Spread

In order to quantify how much the measured $R_{\mathrm{DS(on)}}$ parameter varies between the three manufacturers, the sample standard deviation is used. The sample standard deviation, denoted by s, quantifies the dispersion of $R_{\mathrm{DS(on)}}$ values relative to the mean for each SiC type. A low sample standard deviation indicates that the values are closely grouped around the mean, indicating low spread, whereas a high sample standard deviation reflects a wider spread in the data. In other words, the closer the standard deviation is to zero, the less spread there is among the five SiC MOSFETs from each manufacturer.

The Sample Standard Deviation is calculated using

$$s = \sqrt{\frac{\sum_{i=1}^{5}(x_i - \mu)^2}{n-1}} \tag{2.1}$$

where s denotes the sample standard deviation, x_i represents the measured $R_{\mathrm{DS(on)}}$ value at a specific I_{DS} for each individual MOSFET, μ is the mean $R_{\mathrm{DS(on)}}$ value for the five SiC MOSFETs from each manufacturers and n is the total number of MOSFETs per manufacturer.

2.2 Three-Phase Inverter

2.2.1 Introduction of a Three-Phase Inverter

In this thesis, the three-phase inverter is used solely as a theoretical framework to calculate the MOSFET conduction losses, both individually and in total for the complete inverter. The primary focus is the variation in conduction loss caused by differences in the on-state resistance $R_{ds(on)}$ of the SiC MOSFETs. As shown in Section 2.2.2, the spread in on-state resistance among devices is directly reflected in the resulting conduction loss variation. All other components such as the intrinsic body diode, the load, and the rest of the inverter circuitry are held constant throughout the analysis. The study focuses exclusively on the six switching devices, where the SiC MOSFETs are located. Conduction loss is first calculated for a single MOSFET and then scaled to represent the total loss in a full three-phase inverter, which is compared to the corresponding typical values stated in each manufacturer's datasheet.

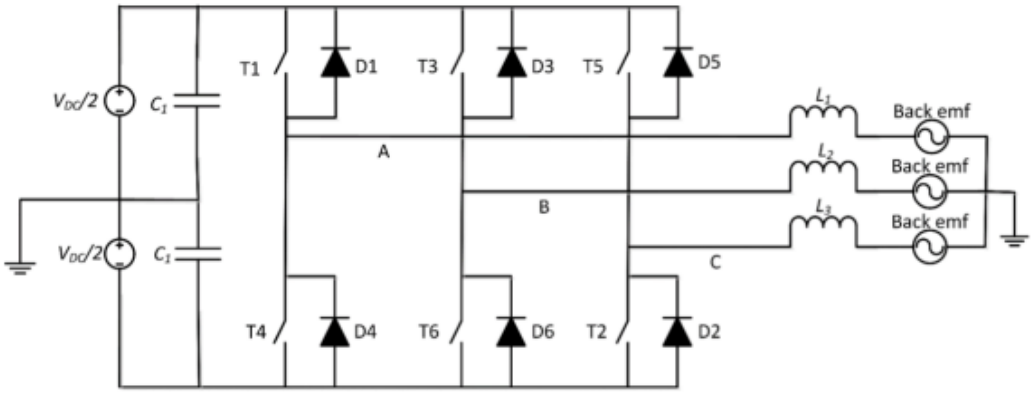

Figure 2.1: The three-phase inverter serves as a theoretical basis for conduction loss calculations in this thesis. The intrinsic body diodes, load, and switching losses are excluded from the analysis and are treated as fixed. The primary focus is on the conduction loss of individual SiC MOSFETs and how it scales to the total conduction loss in a three-phase inverter, which consists of six switches, two switches per leg.

2.2.2 Conduction Loss Calculations

The conduction loss equation for one SiC MOSFET according to the appendix of [1] is

$$\begin{aligned} P_{C,T} = {} & \frac{R_{\text{on}}\hat{I}^2}{4\pi}(AB + CD) \\ & + \frac{R_{\text{on}}}{4\pi(R_{\text{on}} + R_d)^2}\Big(\hat{I}^2 R_d^2(A(\pi - B) - CD) \\ & + V_d^2((\pi - 2\beta)A - D\cos(\beta)) \\ & + \hat{I}R_d V_d(4A\cos(\beta) - (\pi - \beta)D)\Big) \end{aligned} \tag{2.2}$$

where A,B,C and D is defined as

$$A = \begin{cases} 1 & \text{for } t_{\text{bl}} = 0 \\ 1 - 2t_{\text{bl}} f_{\text{sw}} & \text{for } t_{\text{bl}} > 0 \end{cases} \tag{2.3}$$

$$B = \frac{\pi}{2} + \beta - \frac{\sin(2\beta)}{2} \tag{2.4}$$

$$C = \cos(\beta) - \frac{\cos^3(\beta)}{3} \tag{2.5}$$

$$D = 2M\cos(\varphi) \tag{2.6}$$

The parameters A, B, C, and D are defined above and are used to express the full analytical conduction loss equation. However, in this thesis, several simplifying assumptions are applied to eliminate their influence.

Firstly, the blanking time t_{bl} is set to zero, since it simplifies the expressions and the goal in this thesis is to compute the same set-up all the time [2][3]

Secondly, the intrinsic body diode is neglected throughout the analysis of this thesis. According to [1], the diode conducts when the following criterion is fulfilled

$$sin(\beta) = \frac{V_d}{R_{on}\hat{I}} < 1 \tag{2.7}$$

Where V_d is the forward voltage drop over the diode and β is the parallel conduction angle. In order to disregard the intrinsic body diode, this condition must not hold. By setting $\sin(\beta) = 1$, the diode is assumed to cease conduction. This corresponds to $\beta = \pi/2$. Under these assumptions, the parameters simplify to

$$\begin{aligned} A &= 1 \\ B &= \pi \\ C &= 0 \\ D &= 2M\cos(\varphi) \end{aligned} \tag{2.8}$$

where

$$\begin{aligned} AB &= \pi \\ CD &= 0 \end{aligned} \tag{2.9}$$

Moreover, by neglecting the intrinsic body diode, there is no voltage over the diode V_d or resistance associated with the diode R_d. Therefore, all diode-related terms in

the conduction loss expression vanish, eliminating the last three lines of Equation 2.2. The conduction loss equation thus reduces to

$$P_{C,T} = \frac{R_{\text{on}}\hat{I}^2}{4\pi}(AB + CD) = \frac{R_{\text{on}}\hat{I}^2}{4\pi}(\pi + 0) = \frac{R_{\text{on}}\hat{I}^2}{4} \tag{2.8}$$

And the difference between a peak value and RMS is a factor of $\frac{1}{\sqrt{2}}$. The DC equivalent in AC circuits is considered to be the RMS. Thus, the equation can be simplified by using our I_{DS} as the RMS

$$P_{C,T} = \frac{R_{ds(on)(I_{DS}\sqrt{2})^2}}{4} \tag{2.9}$$

To conclude this chapter, the final conduction loss equation used throughout this thesis has been derived through a series of simplifications. Starting from the full analytical expression, terms associated with blanking time and diode conduction were removed under justified assumptions. This led to a simplified form

$$P_{C,T} = \frac{R_{\text{DS(on)}}I_{\text{DS}}^2}{2} \tag{2.10}$$

Where the result shows a linear relationship between the conduction loss and the measured values of $R_{\text{DS(on)}}$, given a constant drain current I_{DS}.

3
Method

This chapter presents the methodology and approach used to obtain the results of this degree project. First, the actual measurement setup is introduced, followed by a table describing each numbered component. Finally, the output characteristic (I_D–V_{DS}) used for extracting $R_{DS(on)}$ is briefly discussed.

3.1 Measurement Setup

The overall measurement setup used to acquire the data is first introduced in Figure 3.1, which provides a complete overview of the instrumentation involved in the characterization process.

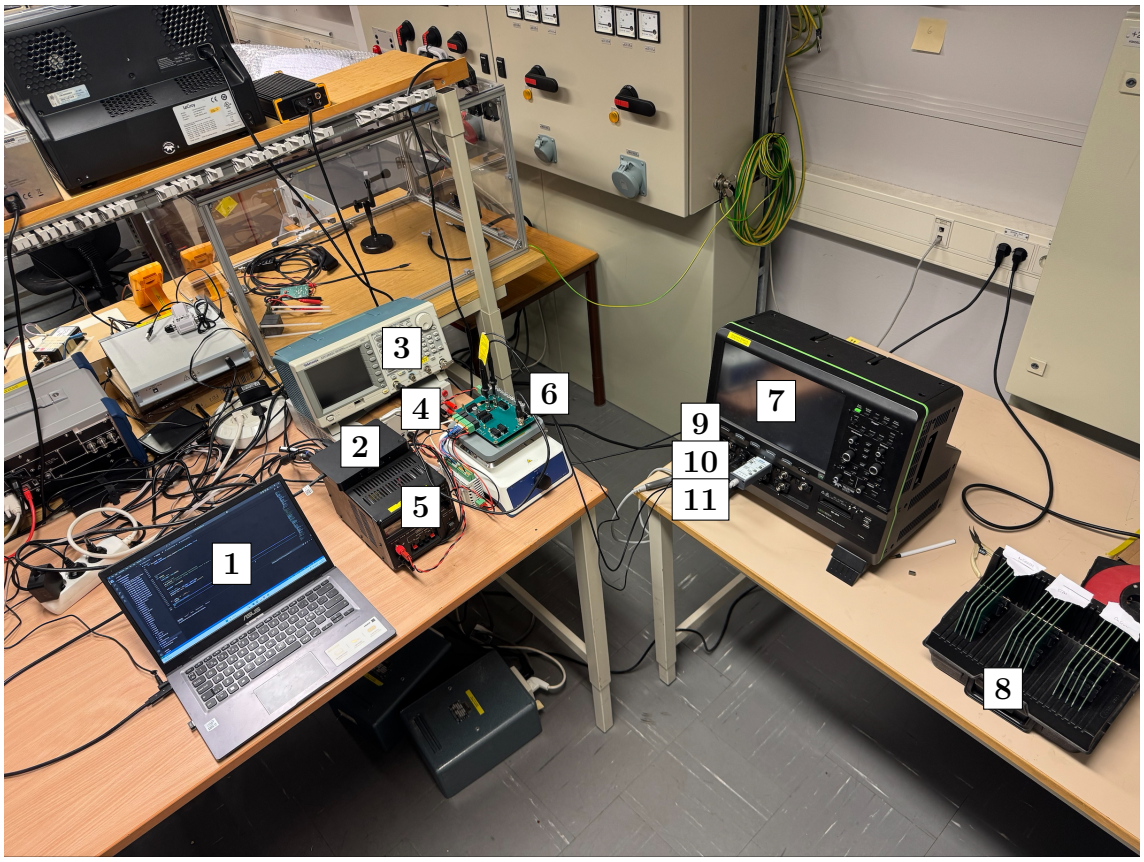

Figure 3.1: Actual measurement setup environment.

Figure 3.2 presents a close-up view of the auxiliary board, highlighting the probe connections and coaxial cables used during the measurements. The figure also shows the two different I_{ds} probe connection points used respectively for on-state resistance $R_{ds(on)}$ and threshold voltage V_{TH} measurements.

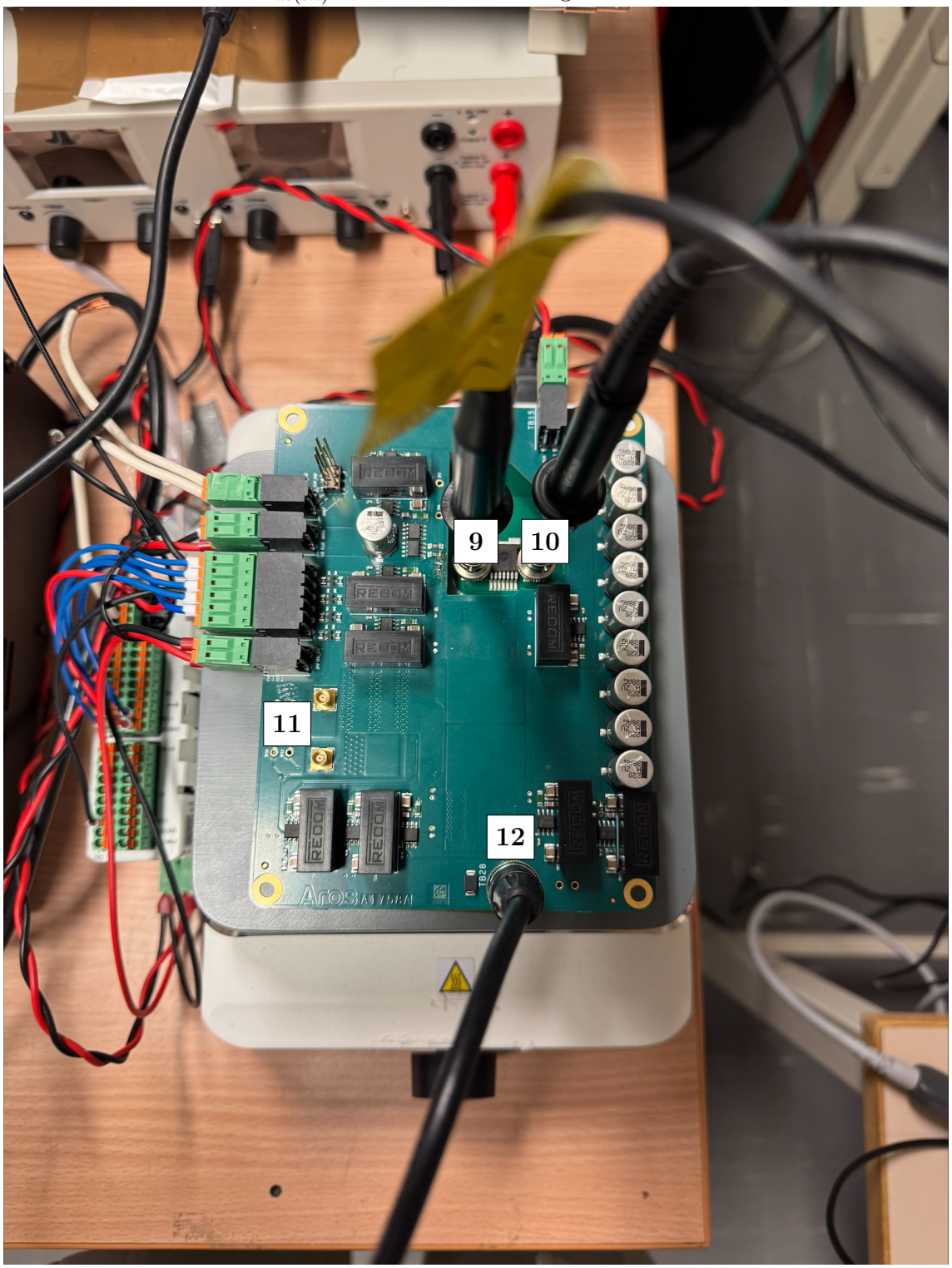

Figure 3.2: Zoom-in on the MOSFET PCB module showing measurement points 9–12.

Finally, Figure 3.3 displays a representative SiC MOSFET mounted on its dedicated PCB. During testing, each individual device under test (DUT) was sequentially swapped and mounted onto the auxiliary board for characterization.

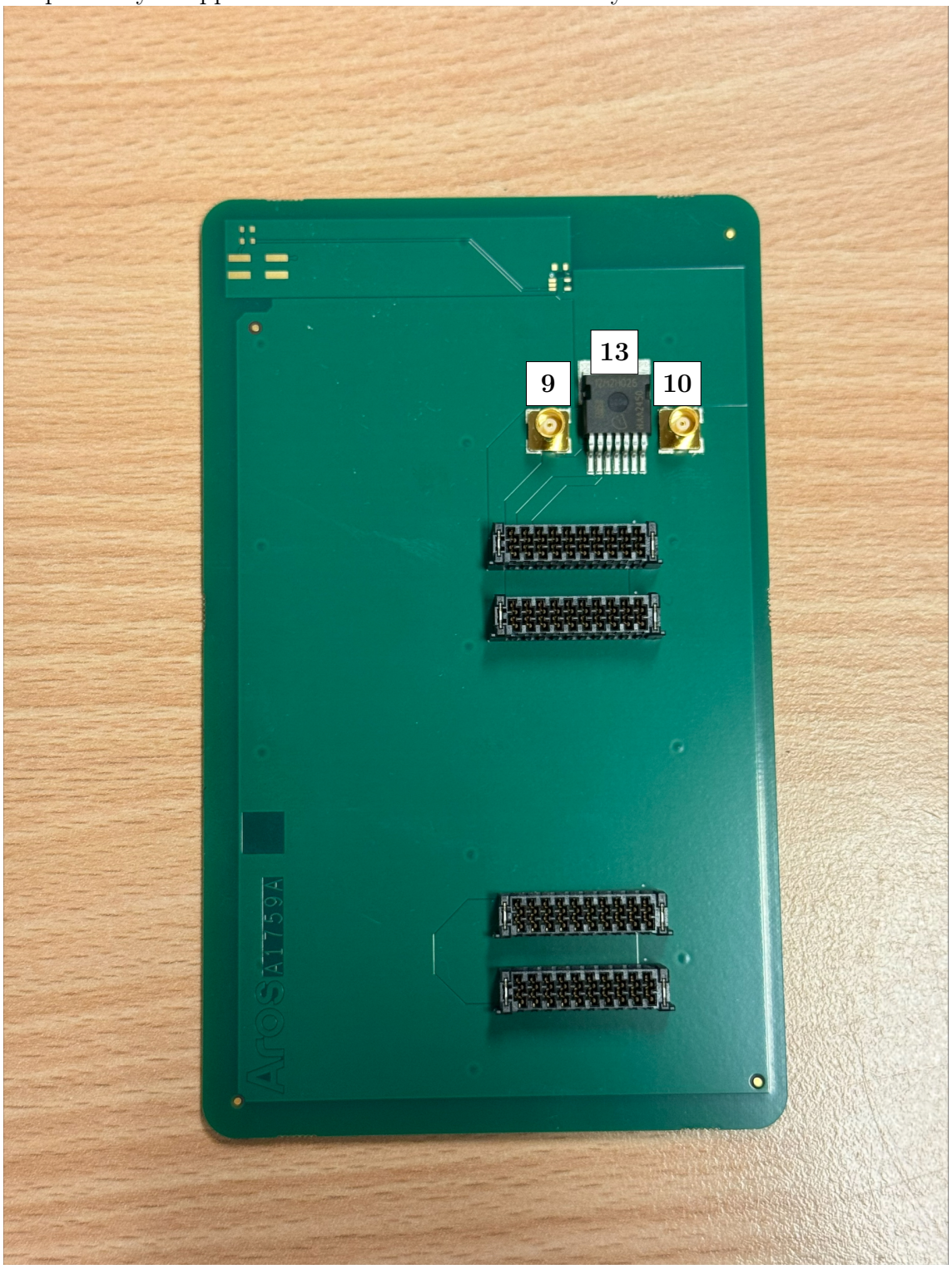

Figure 3.3: One SiC MOSFET PCB module out of fifteen showing measurement points 9,10 and 13.

Each numbered component in Figures 3.1–3.3 is described in Table 3.1 below.

Table 3.1: Measurement setup component description

No.	Component
1	Laptop for data acquisition
2	Docking Station
3	Tektronix AFG3022C Dual Channel Arbitrary/Function Generator
4	Power Supply EA-PS-2384-05 B
5	DC Power Supply
6	Auxiliary board
7	MDA805A Oscilloscope
8	The total fifteen SiC MOSFETs
9	V_{GS} probe point
10	V_{DS} probe point
11	I_{DS} probe point
12	Coaxial cable
13	The SiC MOSFET itself

3.2 Measurement Procedure

The measurement setup constitutes a central part of this thesis. All measurements were automated and controlled through Python scripts. Both the software and hardware were provided by the Division of Electric Power Engineering. However, several I–V characteristic parameters had to be manually adjusted to ensure a valid correlation between the measured data of the DUT and the corresponding datasheet values. This included the selection of fixed V_{GS} levels, the definition of the V_{DS} sweep range and increments, and the assignment of correct identifiers for each SiC MOSFET device.

The main objective of the measurement was to determine $R_{\mathrm{DS(on)}}$ at different drain currents I_{D} and fixed gate-source voltages V_{GS}. Since $R_{\mathrm{DS(on)}}$ increases with junction temperature T_{j} [4], it was important to prevent thermal self-heating during the measurement. This was accomplished by pulsing the DUT into a temporary on-state which enables accurate measurement of its electrical behavior under controlled thermal conditions, without significant heating effects.

3.2.1 Calculation of $R_{\mathrm{DS(on)}}$ in the Ohmic Region

According to [4], the on-state resistance is extracted from the output characteristic using the relation

$$R_{\mathrm{DS(on)}} = \frac{V_{\mathrm{DS}}}{I_{\mathrm{D}}} \tag{3.1}$$

where Ohm's law is applicable only in the *ohmic* (or linear) region of the MOSFET, characterized by a clear linear relationship between the drain-source voltage V_{DS} and the drain current I_D. In contrast, measurements taken in the saturation region are not suitable for this calculation, as the channel no longer exhibits resistive behavior. Figure 3.4 illustrates this linear relationship more clearly [7].

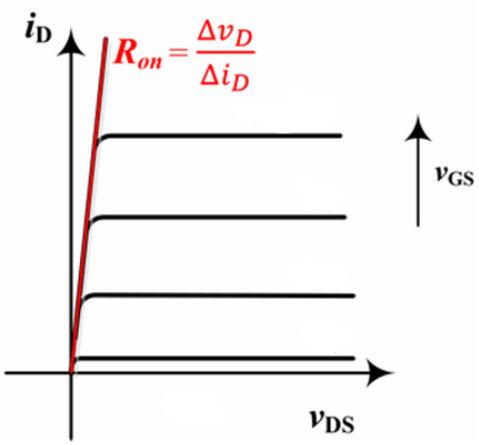

Figure 3.4: The simplified MOSFET characteristics include a linear approximation, where the slope of the curve represents the device's on-state resistance, R_{on}, referred to as $R_{\text{DS(on)}}$ in this thesis.

To ensure that data points fall within the ohmic region, V_{DS} was swept in two stages: initially in 0.25 V increments up to 2 V, and then in 0.5 V increments beyond 2 V. This approach ensured high resolution in the region of interest and minimized total test time.

The drain current I_{D} was derived indirectly by measuring the voltage drop across shunt resistors, which are located on the backside of the auxiliary board. The relation used was

$$I_{\text{D}} = \frac{V_{\text{shunt}}}{R_{\text{shunt}}} \tag{3.2}$$

where V_{shunt} is the voltage drop measured by the oscilloscope, and R_{shunt} is the known resistance of the shunt. The same resistor value was used consistently for all measurements to maintain comparability.

Since V_{DS} and I_{D} are captured simultaneously for each pulse, $R_{\text{DS(on)}}$ could be calculated accurately at each test point. These values were saved automatically as CSV files, labeled according to device name, gate voltage, and junction temperature. The files were then used in the post-processing stage to visualize $R_{\text{DS(on)}}$ as a function of I_{D} for each tested device.

3.3 Post-Processing

Once the measurements were completed, the data was automatically saved as CSV files. These files could then be imported into Python, Excel, or other tools such as MATLAB for further analysis. Within the same Python project directory, additional scripts were used to generate plots of $R_{DS(ON)}$ as a function of I_D. These plots were produced in parallel with the measurement process, allowing immediate visualization and verification of each SiC MOSFET.

During the interpretation of the plots, particular attention was given to identifying any significant deviations of $R_{DS(ON)}$ compared to the corresponding values stated in each manufacturer's datasheet (Infineon, STM and Onsemi). This comparison was essential to validate the measured data and assess the consistency of the devices with their specified characteristics.

4

Results

In this chapter, the spread of $R_{\mathrm{DS(on)}}$ as a function of I_{D} is presented for three types of SiC MOSFETs, based on measurements performed on five devices of each type. From these results, the spread is quantified for each manufacturer at the current levels specified in their respective datasheets. Furthermore, the resulting variation in conduction loss is calculated based on the measured spread in $R_{\mathrm{DS(on)}}$ and compared to the typical $R_{\mathrm{DS(on)}}$ values from the datasheets in the form of a ratio.

In order to evaluate whether the measured $R_{\mathrm{DS(on)}}$ values are accurate and representative, they must be compared against a known reference. For this reason, the drain current and gate-source voltage levels used in this Thesis are selected to match those specified in the datasheets of each manufacturer. This alignment ensures that the measured values can be meaningfully compared to typical datasheet values.

4.1 Spread and Quantification of $R_{\mathrm{DS(on)}}$ Among SiC MOSFET Manufacturers

The MOSFET modules used in this thesis are listed below.

- Infineon: **IMBG120R026M2H**
- STMicroelectronics: **SCT025H120G3AG**
- ON Semiconductor: **NVBG030N120M3S**

The corresponding values of $R_{DS(on)}$ specified for a particular junction temperature, V_{GS}, and I_D, are summarized in Table 4.1.

Table 4.1: Datasheet-based numerical values for each manufacturer.

Manufacturer	**Infineon**	**STM**	**ON Semi**
I_{D}	27.3 A	25 A	30 A
T_{C}	25 °C	25 °C	25 °C
V_{GS}	15 V / 18 V	15 V / 18 V	15 V / 18 V

4.1.1 Infineon

Figure 4.1 presents the spread of $R_{\mathrm{DS(on)}}$ for five SiC MOSFETs from Infineon. Each device is identified in the legend located in the lower right corner of the plot, and the corresponding reference current level is based on the MOSFET module listed previously.

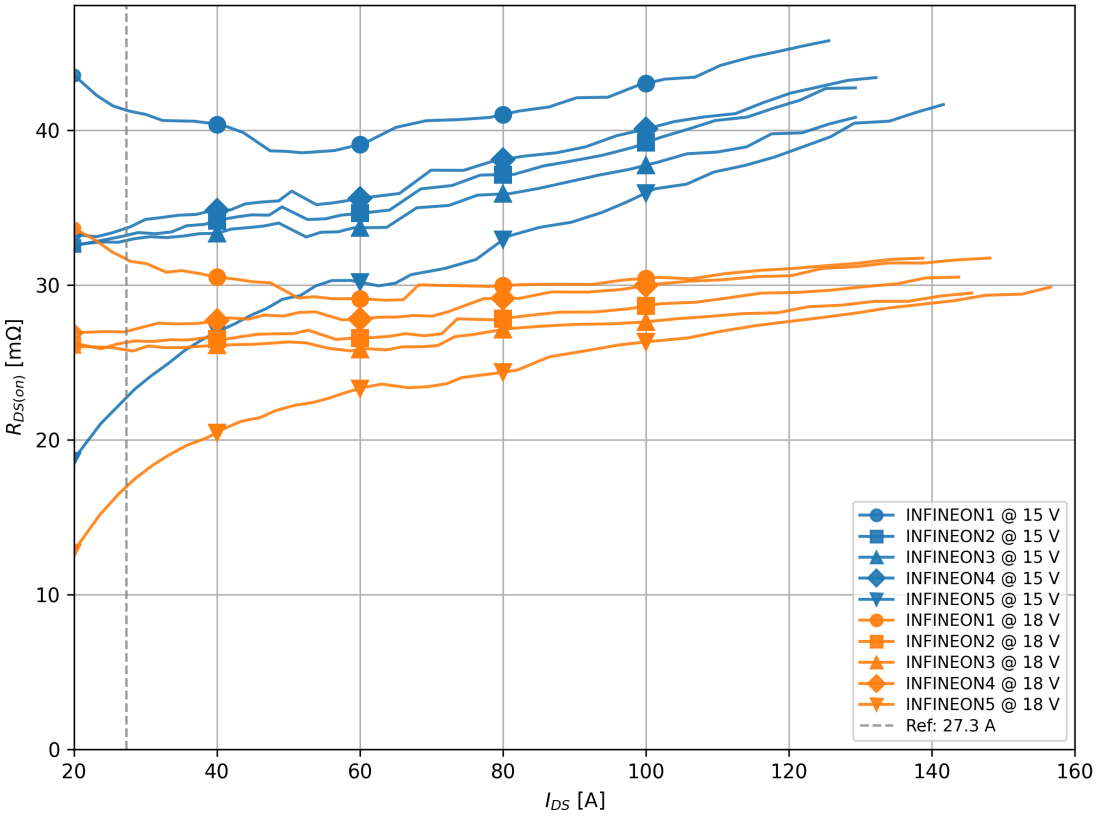

Figure 4.1: The spread of $R_{\mathrm{DS(on)}}$ for Infineon SiC MOSFETs measured at $T_{\mathrm{j}} = 25°\mathrm{C}$. The typical $R_{\mathrm{DS(on)}}$ value according to the datasheet is 31.7 mΩ at $V_{\mathrm{GS}} = 15, \mathrm{V}$ and 25.4 mΩ at $V_{\mathrm{GS}} = 18, \mathrm{V}$, both specified at a reference current of 27.3 A.

It can be observed that the yellow curves lie below the blue ones, indicating a clear correlation between a higher V_{GS} and a lower $R_{\mathrm{DS(on)}}$ [6]. The spread at both V_{GS} levels, quantified at the same reference current as specified in the datasheet, is summarized numerically in Table 4.2. This current level was selected to clearly highlight the deviation in $R_{\mathrm{DS(on)}}$.

Table 4.2: Quantified spread of $R_{\mathrm{DS(on)}}$ for five Infineon SiC MOSFETs per V_{GS} level, measured at $I_{\mathrm{DS}} = 27.3\,\mathrm{A}$ and $T_{\mathrm{j}} = 25\,°\mathrm{C}$.

V_{GS} [V]	μ [mΩ]	s [mΩ]	Max–Min [mΩ]
15	32.9	6.4	18
18	25.4	5.5	15

4.1.2 STM

Figure 4.2 illustrates the measured variation in $R_{ds(on)}$ for five SiC MOSFETs from STM. As in the previous case, measurements were conducted at two values of V_{GS}, and each device is represented by an individual curve, identifiable through the plot legend.

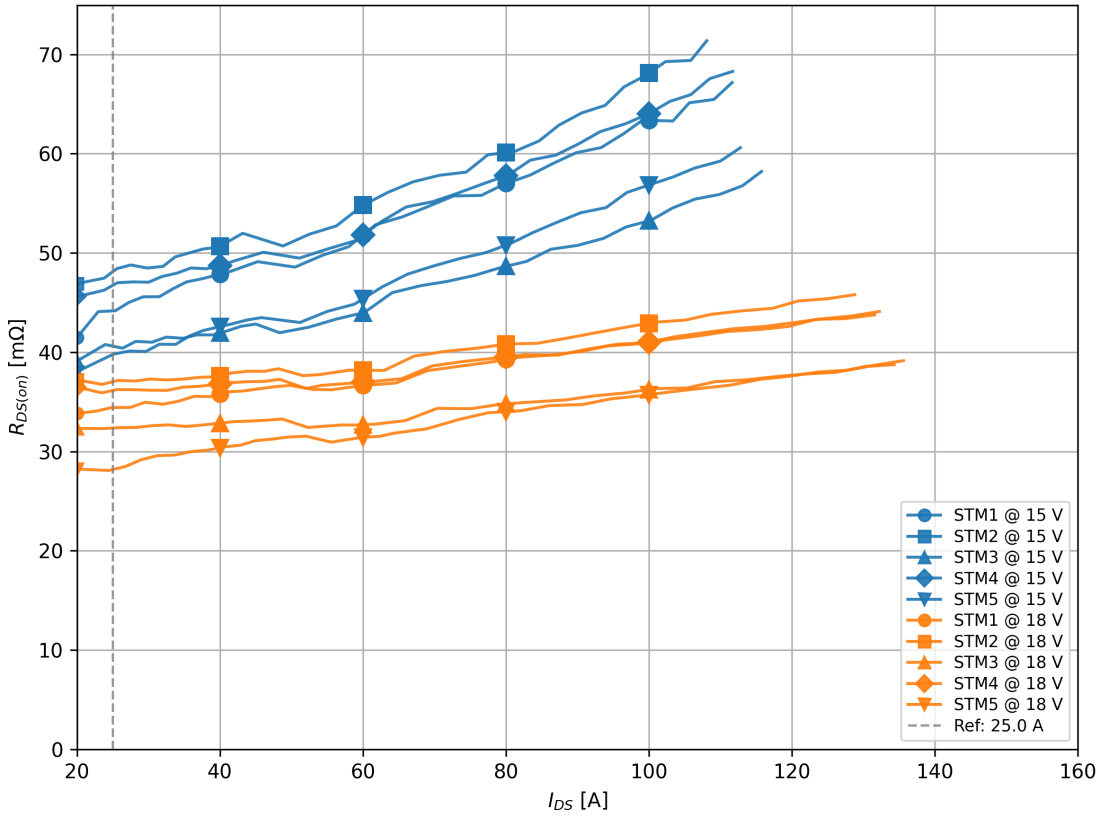

Figure 4.2: The spread of $R_{\mathrm{DS(on)}}$ for STM SiC MOSFETs measured at $T_{\mathrm{j}} = 25°\mathrm{C}$. The typical $R_{\mathrm{DS(on)}}$ value according to the datasheet is 32mΩ at $V_{\mathrm{GS}} = 15, \mathrm{V}$ and 27mΩ at $V_{\mathrm{GS}} = 18, \mathrm{V}$, both corresponding to a reference current of 25A.

Compared to the Infineon devices presented in Figure 4.1, the spread among the STM MOSFETs appears noticeably narrower. For both V_{GS} levels, the curves are more tightly clustered, suggesting a lower variation in $R_{\mathrm{DS(on)}}$ between the individual devices. A numerical summary of the measured values for each gate voltage is provided in Table 4.3.

Table 4.3: Quantified spread of $R_{\mathrm{DS(on)}}$ for five STM SiC MOSFETs per V_{GS} level, measured at $I_{\mathrm{DS}} = 25\,\mathrm{A}$ and $T_{\mathrm{j}} = 25\,°\mathrm{C}$.

V_{GS} [V]	μ [mΩ]	s [mΩ]	Max–Min [mΩ]
15	44.0	3.8	8.6
18	33.7	3.6	9.1

4.1.3 Onsemi

Figure 4.3 presents the measured $R_{\mathrm{DS(on)}}$ characteristics for five SiC MOSFETs from Onsemi. As with the previous devices, the measurements were carried out at two different V_{GS} levels, and the results for each device are shown as individual curves, identified in the accompanying plot legend.

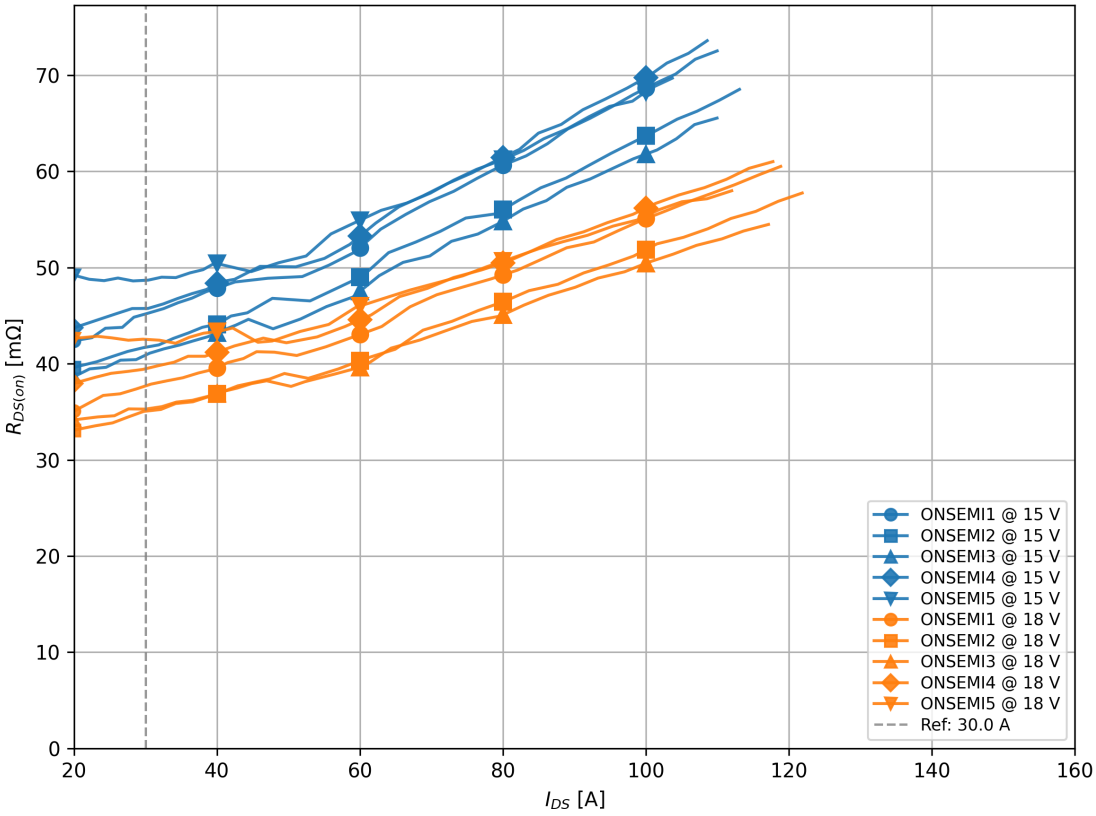

Figure 4.3: The spread of $R_{\mathrm{DS(on)}}$ for Onsemi SiC MOSFETs measured at $T_{\mathrm{j}} = 25°\mathrm{C}$. The typical $R_{\mathrm{DS(on)}}$ value according to the datasheet is 29mΩ at $V_{\mathrm{GS}} = 18\mathrm{V}$, specified at a reference current of 30.0A. No typical value is provided for $V_{\mathrm{GS}} = 15\mathrm{V}$.

Compared to figure 4.1 and figure 4.2, the Onsemi devices exhibit the smallest spread in $R_{\mathrm{DS(on)}}$ among the three manufacturers. This observation is supported both visually in Figure 4.3 and numerically in Table 4.4.

Table 4.4: Quantified spread in $R_{\mathrm{DS(on)}}$ for five Onsemi SiC MOSFETs per V_{GS} level, measured at $I_{\mathrm{DS}} = 30\,\mathrm{A}$ and $T_{\mathrm{j}} = 25\,°\mathrm{C}$.

V_{GS} [V]	μ [mΩ]	s [mΩ]	Max–Min [mΩ]
15	44.5	3.1	7.6
18	38.0	3.1	7.5

4.2 Measured Conduction Loss Variation in a Three-Phase SiC Inverter

The conduction loss variation is calculated using the derived formula presented in Chapter 2. For each manufacturer, two plots are provided. One for $V_{\mathrm{GS}} = 15\,\mathrm{V}$ and one for $V_{\mathrm{GS}} = 18\,\mathrm{V}$. Each plot displays the maximum, minimum, and mean values of the conduction loss across the five SiC MOSFETs for different I_{DS}. These plots clearly illustrate the conduction loss variation both within each manufacturer and between the different manufacturers.

4.2.1 Infineon

Figure 4.4 illustrates the variation in conduction loss. The legend, located in the upper left corner, identifies each curve. The conduction loss variation is visualized as the deviation from the average value (green curve), with the maximum and minimum values indicated by the red and blue curves, respectively.

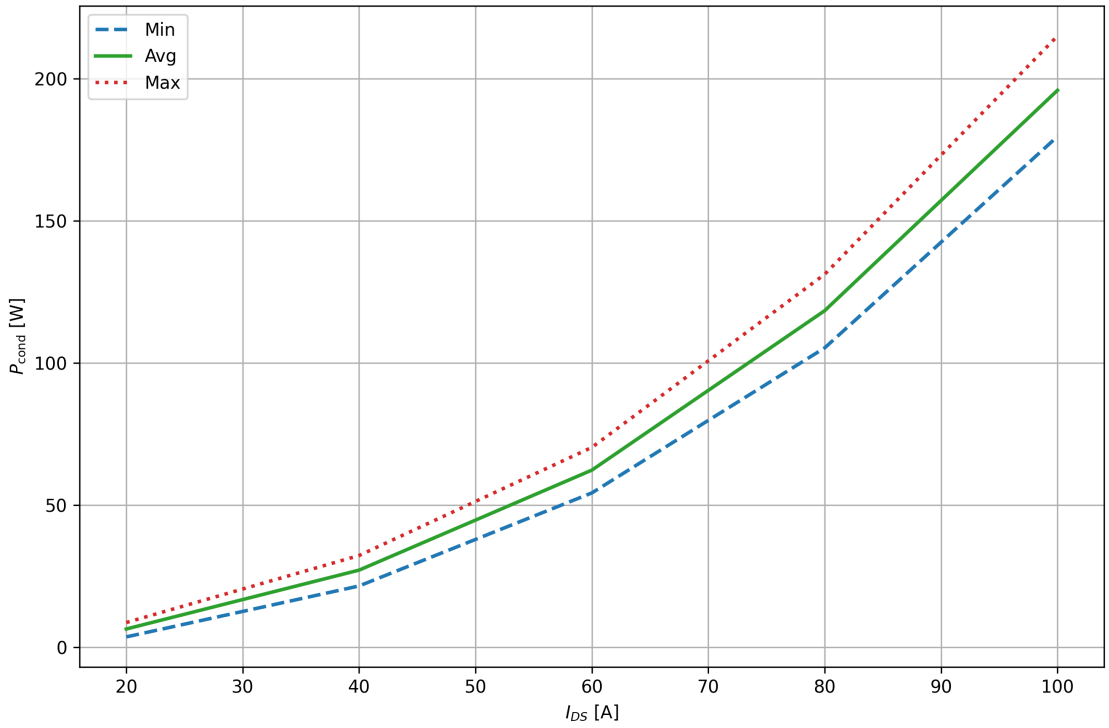

Figure 4.4: Conduction loss variation of five SiC MOSFETs from Infineon at $V_{\mathrm{GS}} = 15\,\mathrm{V}$. The plot shows the minimum, maximum, and mean conduction loss calculated from measured $R_{\mathrm{DS(on)}}$ values. The variation illustrates device spread within the same manufacturer under identical conditions.

Notice how the area between both the maximum and minimum conduction loss curves and the mean curve increases with rising I_{DS}. This indicates that the conduction loss variation grows with current, consistent with the linear relationship between figure 4.4 and figure 4.1 as derived in Chapter 2.

The corresponding variation in conduction loss at $V_{GS} = 18V$ is shown in Figure 4.5.

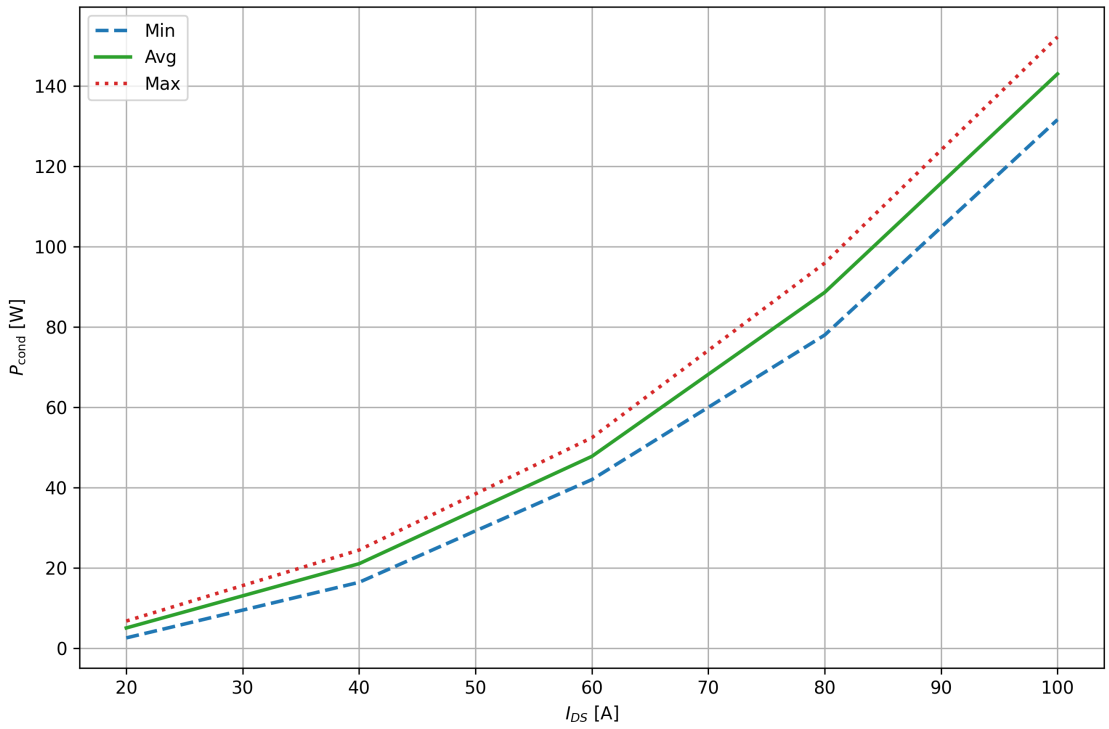

Figure 4.5: Conduction loss variation of the same set of five SiC MOSFETs from Infineon at $V_{\mathrm{GS}} = 18\,\mathrm{V}$. The plot shows the minimum, maximum, and mean conduction loss calculated from measured $R_{\mathrm{DS(on)}}$ values. The variation illustrates device spread within the same manufacturer under identical conditions.

4.2.2 STM

Figure 4.6 presents the results for conduction loss variation among the five STM SiC MOSFETs. As before, the plotted curves illustrate how the variation evolves across different I_{DS} levels, and the legend provides a visual reference for distinguishing between curves.

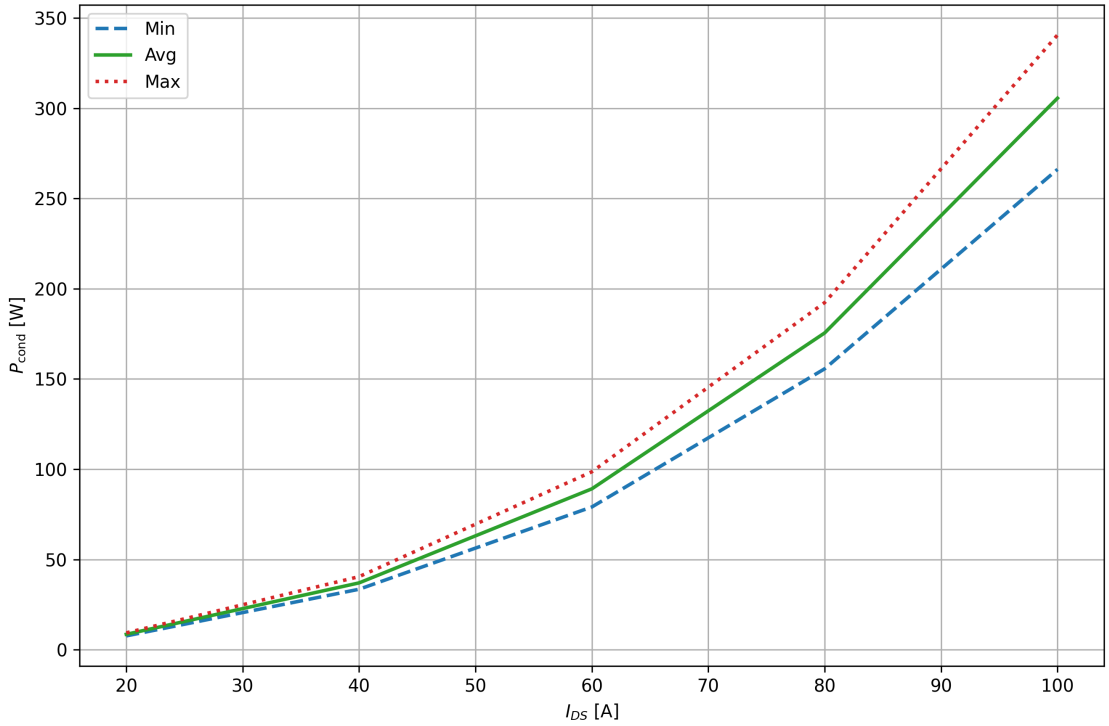

Figure 4.6: Conduction loss variation of five SiC MOSFETs from STM at $V_{GS} = 15\,V$. The plot shows the minimum, maximum, and mean conduction loss calculated from measured $R_{DS(on)}$ values. The variation illustrates device spread within the same manufacturer under identical operating conditions.

Furthermore, Figure 4.7 presents the conduction loss variation for the STM SiC MOSFETs corresponding to the yellow curves shown in Figure 4.2.

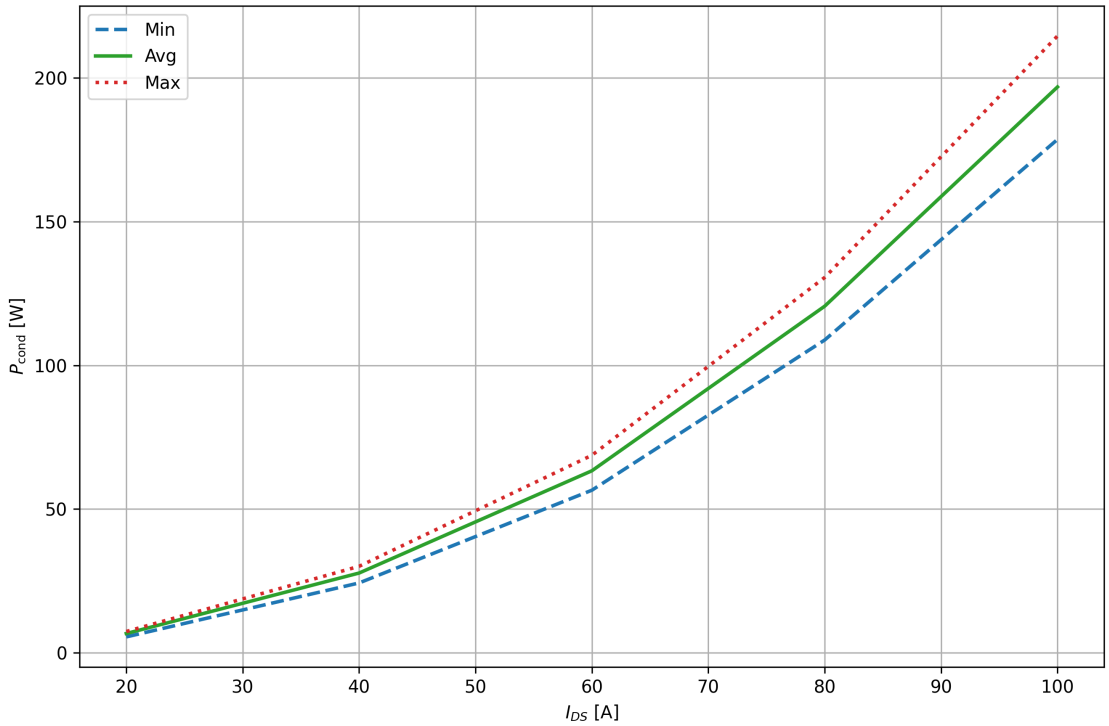

Figure 4.7: Conduction loss variation of the same set of five SiC MOSFETs from STM at $V_{GS} = 18\,V$. Minimum, maximum, and average conduction losses are derived from measurements and illustrate the internal consistency and spread of devices under the same conditions.

4.2.3 Onsemi

Figure 4.8 illustrates the conduction loss variation among the five Onsemi SiC MOSFETs, corresponding to the blue curves in Figure 4.3, across different I_{DS} levels.

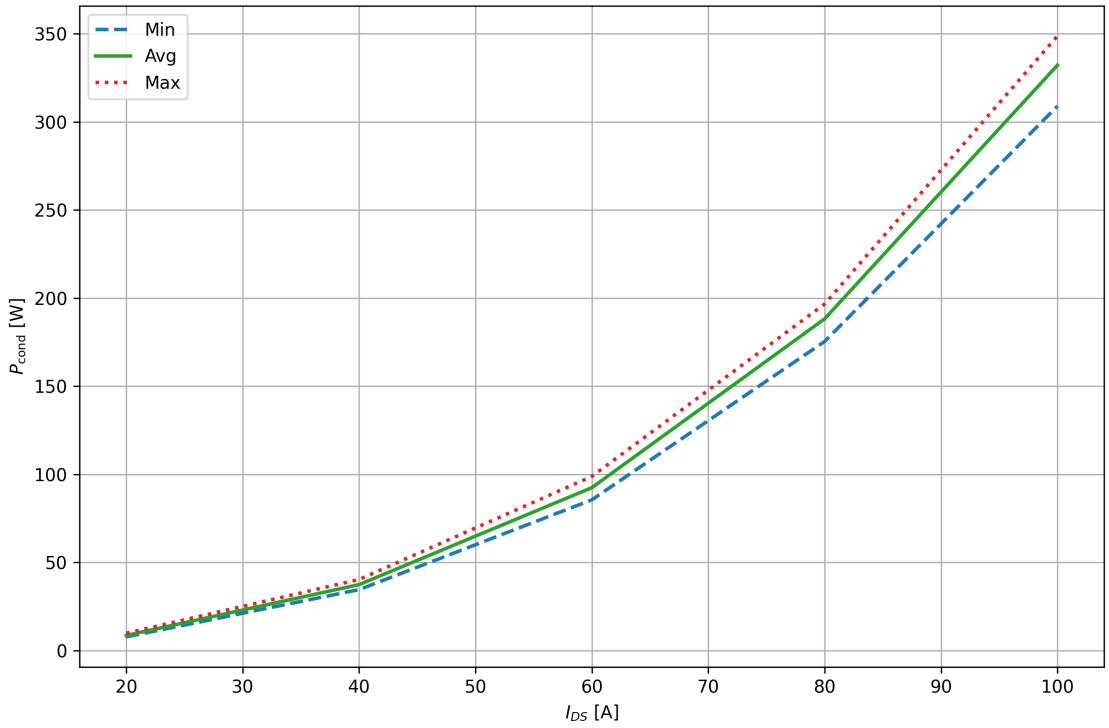

Figure 4.8: Conduction loss variation of five SiC MOSFETs from Onsemi at $V_{\mathrm{GS}} = 15\,\mathrm{V}$. The plot presents the minimum, maximum, and mean conduction loss values based on measured $R_{\mathrm{DS(on)}}$ data, highlighting the variation between nominally identical devices.

Notice that the area between the three curves is smaller compared to the corresponding V_{GS} plots in figure 4.4 and figure 4.6, indicating a lower variation in conduction loss.

Finally, Figure 4.9 shows the conduction loss variation for the Onsemi SiC MOSFETs at $V_{GS} = 18V$.

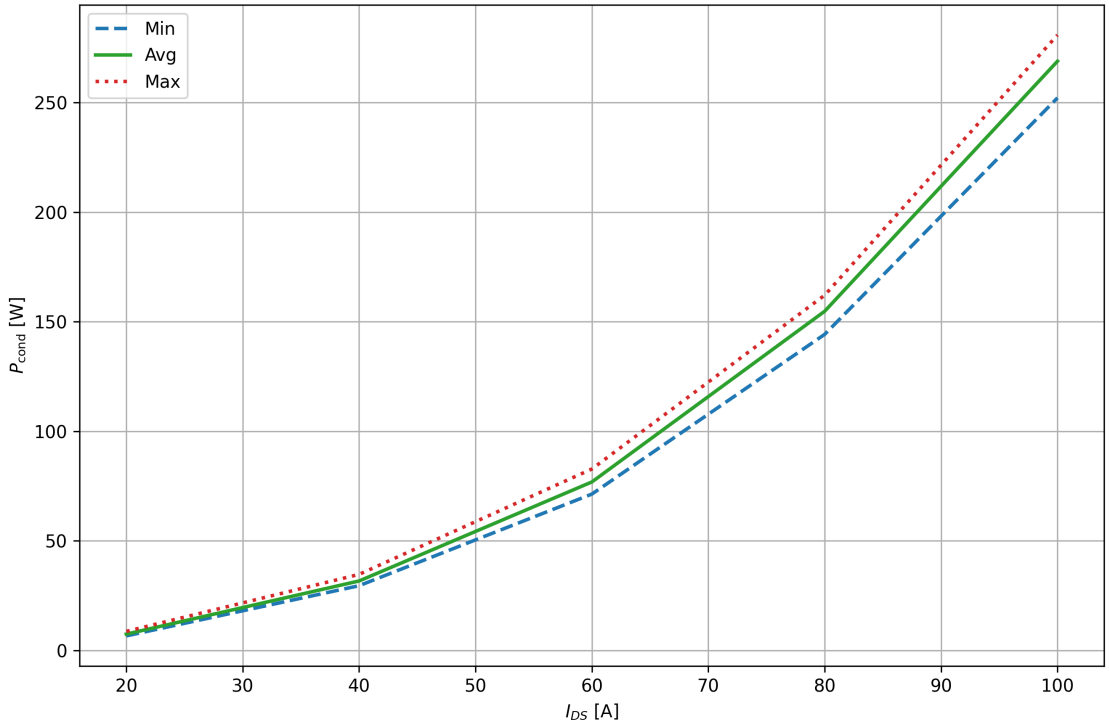

Figure 4.9: Conduction loss variation of the same set of five SiC MOSFETs from Onsemi at $V_{\mathrm{GS}} = 18\,\mathrm{V}$. The figure shows how conduction loss differs between devices of the same type, which is important for evaluating performance tolerance and design margins in inverter applications.

Interestingly, the conduction loss variation for figure 4.9 is slightly smaller than in Figure 4.8 and significantly lower compared to all previous conduction loss variation plots. This is indicated by the narrower spacing between the minimum, average and maximum curves. This indicates that the five Onsemi SiC MOSFETs exhibit the lowest variation in conduction loss at a gate voltage of 18V.

4.3 Comparison of Measured and Datasheet-Based Total Conduction Loss in a Three-Phase Inverter

In order to evaluate how the measured conduction losses compare to typical datasheet values, the total conduction loss is calculated for each manufacturer. This is done by inserting the typical $R_{\mathrm{DS(on)}}$ value from the datasheet into the conduction loss formula derived in Chapter 2. The resulting single-device loss is then multiplied by 6 to reflect the total conduction loss in a three-phase inverter, which consists of six MOSFETs (two per phase leg). All calculations are performed at a common junction temperature of $T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$ to ensure fair comparison. For each manufacturer, the maximum and minimum measured values are taken from the conduction loss plots shown in Section 4.2, which illustrate the device-to-device variation. These extreme cases are also scaled to total inverter level.

A ratio is then computed between each measured total conduction loss and the corresponding datasheet-based total conduction loss. This allows for a percentage-based comparison of deviation from typical datasheet expectations, as shown in the tables below from table 4.5 to table 4.9

Table 4.5: Total conduction loss comparison for Infineon SiC MOSFETs at $V_{GS} = 15\,V$ and $I_D = 27.3\,A$, based on measured data and typical datasheet value.

Source	Total $P_{C,T}$ [W]	Difference from Typical [%]
Datasheet (Typ.)	70.8	0.0
Measured (min)	46.2	–34.8
Measured (max)	100.8	+42.4

Table 4.6: Total conduction loss comparison for Infineon SiC MOSFETs at $V_{GS} = 18\,V$ and $I_D = 27.3\,A$.

Source	Total $P_{C,T}$ [W]	Difference from Typical [%]
Datasheet (Typ.)	56.8	0.0
Measured (min)	45.2	–20.4
Measured (max)	75.0	+32.0

Table 4.7: Total conduction loss comparison for STM SiC MOSFETs at $V_{GS} = 15\,V$ and $I_D = 25\,A$.

Source	Total $P_{C,T}$ [W]	Difference from Typical [%]
Datasheet (Typ.)	60.0	0.0
Measured (min)	73.0	+21.7
Measured (max)	91.3	+52.2

Table 4.8: Total conduction loss comparison for STM SiC MOSFETs at $V_{GS} = 18\,V$ and $I_D = 25\,A$.

Source	Total $P_{C,T}$ [W]	Difference from Typical [%]
Datasheet (Typ.)	50.6	0.0
Measured (min)	54.5	+7.7
Measured (max)	71.5	+41.3

Table 4.9: Total conduction loss comparison for Onsemi SiC MOSFETs at $V_{GS} = 18\,V$ and $I_D = 30\,A$. A typical value for $V_{GS} = 15\,V$ is not provided in the Onsemi datasheet.

Source	Total $P_{C,T}$ [W]	Difference from Typical [%]
Datasheet (Typ.)	78.3	0.0
Measured (min)	72.3	–7.7
Measured (max)	99.0	+26.4

5

Conclusion

Since the MOSFET conduction loss equation used in this thesis excludes the modulation index M, power factor φ, switching losses and the average conduction loss of the intrinsic diode, the resulting total conduction loss is directly proportional to the measured variation in $R_{\mathrm{DS(on)}}$ at the specified current levels. As such, the observed spread in conduction loss is a direct consequence of the $R_{\mathrm{DS(on)}}$ variation. Higher resistance values lead to proportionally higher conduction losses, while lower values reduce the total loss accordingly.

The quantified comparison in Section 4.3 between measured and datasheet-based total conduction losses further illustrates how device-to-device variation can lead to substantial deviation from expected values. In some cases, the measured maximum conduction loss exceeded the datasheet-based estimate by more than 50%, while the minimum fell below 20%. These deviations emphasize the importance of accounting for such spread in design-stage calculations to avoid underestimating conduction losses and to ensure that inverter performance expectations are realistically aligned with actual device behavior.

When comparing the quantified spread in $R_{\mathrm{DS(on)}}$ between the manufacturers, Infineon exhibited the largest variation, with a sample standard deviation of up to 6.4mΩ and a maximum range of 18mΩ. STM showed a more moderate spread, with sample standard deviation below 4mΩ and a slightly narrower range of around 9mΩ. Onsemi demonstrated the most consistent device performance, with sample standard deviation of 3.1mΩ and the smallest max–min difference of approximately 7.6mΩ.

When designing a three-phase inverter, the maximum and minimum deviations in $R_{\mathrm{DS(on)}}$ relative to the datasheet values must be taken into account, as this thesis has shown a clear linear relationship between increased on-state resistance and increased conduction losses. Moreover, from a sustainability perspective, consideration of parameter spread is essential for minimizing the environmental footprint. Oversizing the inverter to cover all possible variations leads to unnecessary material usage and a larger physical footprint. Conversely, undersizing the inverter may result in a design that fails to accommodate the actual spread in $R_{\mathrm{DS(on)}}$, rendering the system non-functional and equally wasteful. Therefore, accurate knowledge of device variation is crucial for achieving both reliable performance and responsible resource usage in inverter design.

5.1 Future Work

Although each measurement for Infineon devices was repeated to ensure consistency, the results still deviated notably from those of STM and Onsemi. Future work should therefore include additional measurements or alternative test setups for Infineon devices to verify the accuracy of the observed spread of $R_{\mathrm{DS(on)}}$.

Furthermore, to obtain a more detailed and accurate estimation of the total conduction loss in a three-phase inverter, future analyses should incorporate additional contributing factors. These include the average conduction loss of the intrinsic body diodes and the switching losses. Accounting for these effects, together with the modulation index M and power factor φ, would improve the conduction loss model beyond the linear approximation used in this thesis and offer a more complete representation of the total three-phase inverter conduction loss under realistic operating conditions.

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A

Appendix 1

Table A.1 presents the measured values at the same reference current specified in the datasheet for Infineon's IMBG120R026M2H. These values were used to calculate the mean, sample standard deviation, and max–min range for two gate voltages, shown in Table 4.2.

Table A.1: Measured $R_{\mathrm{DS(on)}}$ values in mΩ for Infineon SiC MOSFETs at $V_{\mathrm{GS}} = 15\,\mathrm{V}$ and 18 V, measured at $I_{DS} = 27.3\ A$ according to the manufacturer's datasheet.

Device	15 V	18 V
1	41.24	31.53
2	33.14	26.39
3	32.99	25.73
4	33.76	26.97
5	23.26	16.45

Table A.2 lists the measured values at the reference current specified in the datasheet for STM's SCT025H120G3AG. These values form the basis for the statistical results presented in Table 4.3.

Table A.2: Measured $R_{\mathrm{DS(on)}}$ values in mΩ for STM SiC MOSFETs at $V_{\mathrm{GS}} = 15\,\mathrm{V}$ and 18 V, measured at $I_{DS} = 25\ A$ according to the manufacturer's datasheet.

Device	15 V	18 V
1	44.17	34.42
2	48.42	37.15
3	40.77	32.40
4	46.99	35.75
5	39.80	28.08

Table A.3 shows the measured values at the reference current defined in the datasheet for Onsemi's NVBG030N120M3S. These values were used to generate the results in Table 4.4.

Table A.3: Measured $R_{\mathrm{DS(on)}}$ values in mΩ for Onsemi SiC MOSFETs at $V_{\mathrm{GS}} =$ 15 V and 18 V, measured at $I_{DS} = 30\ A$ according to the manufacturer's datasheet.

Device	**15 V**	**18 V**
1	45.27	38.46
2	41.66	34.97
3	41.09	36.56
4	45.75	37.72
5	48.69	37.64

Data sheet of IMBG120R026M2H.

IMBG120R026M2H
CoolSiC™ 1200 V SiC MOSFET G2

Final datasheet
CoolSiC™ 1200 V SiC MOSFET G2 : Silicon Carbide MOSFET

Features

- V_{DSS} = 1200 V at T_{vj} = 25°C
- I_{DDC} = 53 A at T_C = 100°C
- $R_{DS(on)}$ = 25.4 mΩ at V_{GS} = 18 V, T_{vj} = 25°C
- Very low switching losses
- Overload operation up to T_{vj} = 200°C
- Short circuit withstand time 2 µs
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.2 V
- Robust against parasitic turn on, 0 V turn-off gate voltage can be applied
- Robust body diode for hard commutation
- .XT interconnection technology for best-in-class thermal performance
- Suitable Infineon gate drivers can be found under https://www.infineon.com/gdfinder

Halogen-free
Green
Lead-free
RoHS

Potential applications

- EV Charging
- Online UPS/Industrial UPS
- String inverter
- General purpose drives (GPD)

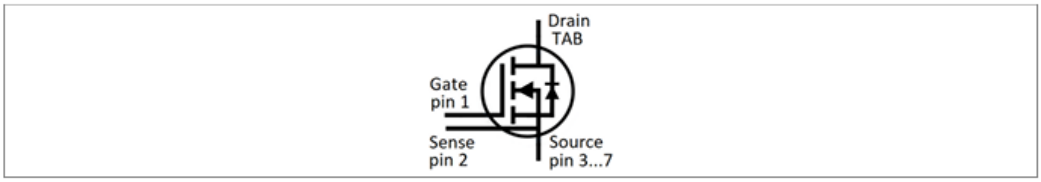
Product validation

- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

Pin definition:
- Pin 1 - Gate
- Pin 2 - Kelvin sense contact
- Pin 3…7 - Source
- Tab - Drain

Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction (only for 4pin, TO263-7L)



Type	Package	Marking
IMBG120R026M2H	PG-TO263-7-U01	12M2H026

Figure A.1: First page of the datasheet for the Infineon IMBG120R026M2H SiC MOSFET.

Table 3 **Recommended values**

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Table 4 **Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 27.3 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		25.4		mΩ
			T_{vj} = 150 °C, $V_{GS(on)}$ = 18 V		52	68	
			T_{vj} = 175 °C, $V_{GS(on)}$ = 18 V		60		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		31.7		
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 8.6 mA, V_{DS} = V_{GS} (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.2	5.1	V
			T_{vj} = 175 °C		3.2		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C			240	µA
			T_{vj} = 175 °C		4		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 23 V			120	nA
			V_{GS} = -10 V			-120	
Forward transconductance	g_{fs}	I_D = 27.3 A, V_{DS} = 20 V			18.3		S
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			5.6		Ω
Input capacitance	C_{iss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			1990		pF
Output capacitance	C_{oss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			85		pF
Reverse transfer capacitance	C_{rss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			7.4		pF
C_{oss} stored energy	E_{oss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			36		µJ
Output charge	Q_{oss}	Calculated by $C_{oss}(f)V_{DS}$ @100 kHz			132.6		nC
Effective output capacitance, energy related	$C_{o(er)}$	V_{DD} = 0...800 V, V_{GS} = 0 V			112.5		pF
Effective output capacitance, time related	$C_{o(tr)}$	I_D = constant, V_{DD} = 0...800 V, V_{GS} = 0 V			165.7		pF
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 27.3 A, V_{GS} = -2/18 V, turn-on pulse			60		nC

(table continues...)

Figure A.2: Fourth page of the datasheet for the Infineon IMBG120R026M2H SiC MOSFET.

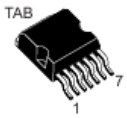
Data sheet of SCT025H120G3AG.

life.augmented

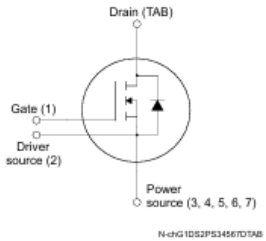
SCT025H120G3AG

Datasheet

Automotive-grade silicon carbide Power MOSFET 1200 V, 27 mΩ typ., 55 A in an H²PAK-7 package



H²PAK-7



Features

Order code	V_{DS}	$R_{DS(on)}$ typ.	I_D
SCT025H120G3AG	1200 V	27 mΩ	55 A

- AEC-Q101 qualified
- Very low $R_{DS(on)}$ over the entire temperature range
- High speed switching performances
- Very fast and robust intrinsic body diode
- Source sensing pin for increased efficiency

Applications

- Main inverter (electric traction)
- DC/DC converter for EV/HEV
- On board charger (OBC)

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 3rd generation SiC MOSFET technology. The device features a very low $R_{DS(on)}$ over the entire temperature range combined with low capacitances and very high switching operations, which improve application performance in frequency, energy efficiency, system size and weight reduction.

STPOWER

Product status link
SCT025H120G3AG

Product summary	
Order code	SCT025H120G3AG
Marking	25H120G3AG
Package	H²PAK-7
Packing	Tape and reel

Figure A.3: First page of the datasheet for the STM SCT025H120G3AG SiC MOSFET

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. **On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1200			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1200 V			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 5 mA	1.8	3.0	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 15 V, I_D = 25 A		32		mΩ
		V_{GS} = 18 V, I_D = 25 A		27	37	
		V_{GS} = 18 V, I_D = 25 A, T_J = 175 °C		48.5		

Table 4. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 800 V, f = 1 MHz, V_{GS} = 0 V	-	1990	-	pF
C_{oss}	Output capacitance		-	102	-	pF
C_{rss}	Reverse transfer capacitance		-	12	-	pF
Q_g	Total gate charge	V_{DD} = 800 V, V_{GS} = -5 to 18 V, I_D = 25 A	-	73	-	nC
Q_{gs}	Gate-source charge		-	23.5	-	nC
Q_{gd}	Gate-drain charge		-	23.5	-	nC
R_g	Gate input resistance	f = 1 MHz, I_D = 0 A	-	1.3	-	Ω

Table 5. **Switching energy (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	V_{DD} = 800 V, I_D = 25 A, R_G = 15 Ω, V_{GS} = -5 to 18 V	-	378	-	µJ
E_{off}	Turn-off switching energy		-	305	-	µJ

Table 6. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 800 V, I_D = 25 A, R_G = 15 Ω, V_{GS} = -5 to 18 V	-	23	-	ns
t_r	Rise time		-	27	-	ns
$t_{d(off)}$	Turn-off delay time		-	48	-	ns
t_f	Fall time		-	25	-	ns

Figure A.4: Third page of the datasheet for the STM SCT025H120G3AG SiC MOSFET

Data sheet of NVBG030N120M3S.

onsemi

DATA SHEET
www.onsemi.com

Silicon Carbide (SiC) MOSFET – EliteSiC, 29 mohm, 1200 V, M3S, D2PAK-7L
NVBG030N120M3S

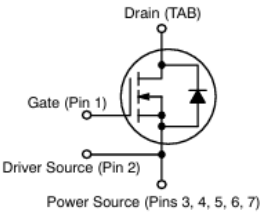
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
1200 V	39 mΩ @ 18 V	77 A

Features

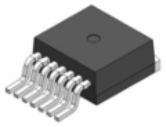
- Typ. $R_{DS(on)}$ = 29 mΩ @ V_{GS} = 18 V
- Ultra Low Gate Charge ($Q_{G(tot)}$ = 107 nC)
- High Speed Switching with Low Capacitance (C_{oss} = 106 pF)
- 100% Avalanche Tested
- AEC−Q101 Qualified and PPAP Capable
- This Device is Halide Free and RoHS Compliant with exemption 7a, Pb−Free 2LI (on second level interconnection)

Typical Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for EV/HEV



N−CHANNEL MOSFET



D2PAK−7L
CASE 418BJ

MARKING DIAGRAM

BG030N120M3S = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	1200	V
Gate−to−Source Voltage			V_{GS}	−10/+22	V
Recommended Operation Values of Gate−to−Source Voltage		T_C < 175°C	V_{GSop}	−3/+18	V
Continuous Drain Current (Notes 2, 3)	Steady State	T_C = 25°C	I_D	77	A
Power Dissipation (Note 2)	Steady State	T_C = 25°C	P_D	348	W
Continuous Drain Current (Notes 2, 3)	Steady State	T_C = 100°C	I_D	54	A
Power Dissipation (Note 2)	Steady State	T_C = 100°C	P_D	174	W
Pulsed Drain Current (Note 4)	T_C = 25°C		I_{DM}	207	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode) T_C = 25°C, V_{GS} = −3 V (Note 2)			I_S	68	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 21 A, L = 1 mH) (Note 5)			E_{AS}	220	mJ
Maximum Temperature for Soldering (10 s)			T_L	270	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR−4 board using1 in^2 pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. The maximum current rating is based on typical RDS(on) performance.
4. Repetitive rating, limited by max junction temperature.
5. E_{AS} of 220 mJ is based on starting T_J = 25°C; L = 1 mH, I_{AS} = 21 A, V_{DD} = 100 V, V_{GS} = 18 V.

ORDERING INFORMATION

Device	Package	Shipping†
NVBG030N120M3S	D2PAK−7L	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Figure A.5: First page of the datasheet of the Onsemi NVBG030N120M3S SiC MOSFET

NVBG030N120M3S

THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Junction–to–Case – Steady State (Note 2)	$R_{\theta JC}$	0.43	°C/W
Junction–to–Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	40	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF–STATE CHARACTERISTICS						
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	1200	–	–	V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 1 mA, referenced to 25°C (Note 7)	–	0.3	–	V/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V	–	–	100	μA
Gate–to–Source Leakage Current	I_{GSS}	V_{GS} = +22/–10 V, V_{DS} = 0 V	–	–	±1	μA
ON–STATE CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 15 mA	2.04	2.4	4.4	V
Recommended Gate Voltage	V_{GOP}		–3	–	+18	V
Drain–to–Source On Resistance	$R_{DS(on)}$	V_{GS} = 18 V, I_D = 30 A, T_J = 25°C	–	29	39	mΩ
		V_{GS} = 18 V, I_D = 30 A, T_J = 175°C (Note 7)	–	58	–	
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 30 A (Note 7)	–	30	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 800 V	–	2430	–	pF
Output Capacitance	C_{OSS}		–	106	–	
Reverse Transfer Capacitance	C_{RSS}		–	9.4	–	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = –3/18 V, V_{DS} = 800 V, I_D = 30 A	–	107	–	nC
Threshold Gate Charge	$Q_{G(TH)}$		–	6	–	
Gate–to–Source Charge	Q_{GS}		–	17	–	
Gate–to–Drain Charge	Q_{GD}		–	28	–	
Gate–Resistance	R_G	f = 1 MHz	–	3.4	–	Ω
SWITCHING CHARACTERISTICS						
Turn–On Delay Time	$t_{d(ON)}$	V_{GS} = –3/18 V, V_{DS} = 800 V, I_D = 30 A, R_G = 4.7 Ω inductive load (Notes 6, 7)	–	16	–	ns
Rise Time	t_r		–	20	–	
Turn–Off Delay Time	$t_{d(OFF)}$		–	48	–	
Fall Time	t_f		–	11	–	
Turn–On Switching Loss	E_{ON}		–	310	–	μJ
Turn–Off Switching Loss	E_{OFF}		–	138	–	
Total Switching Loss	E_{tot}		–	448	–	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Continuous Source–Drain Diode Forward Current (Note 2)	I_{SD}	V_{GS} = –3 V, T_C = 25°C (Note 7)	–	–	68	A
Pulsed Source–Drain Diode Forward Current (Note 4)	I_{SDM}		–	–	207	
Forward Diode Voltage	V_{SD}	V_{GS} = –3 V, I_{SD} = 30 A, T_J = 25°C	–	4.6	–	V

Figure A.6: Second page of the datasheet of the Onsemi NVBG030N120M3S SiC MOSFET

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