CHALMERS
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600 V DC-DC Converter for Battery Charger Investigation

For Heavy Electric Machinery

Master's thesis in Electric Power Engineering

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Department of Electrical engineering

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Abstract

This thesis is intended to investigate the bi-directional DC-DC converter topologies for battery charger applications. Unlike other battery chargers where the input voltage is a constant DC source, an external battery is used as the input source in this application. The literature review of DC-DC converters available in isolated and non-isolated topolgies are performed. Two converter topologies — one from each topology — has been selected based on a defined selection criteria. A three-phase dual active (DAB) bridge converter is chosen amongst the isolated topologies, and among the non-isolated topologies, a four-phase interleaved buck/boost (IBC) converter is chosen. The selected converters were designed for a nominal input voltage of 600 V and an output voltage of 720 V with a rated power of 150 kW. For the three-phase DAB, three single-phase planar transformers were designed to achieve a galvanic isolation of the converter. To ensure a constant power flow, a closed-loop controller has been designed for both converters, namely, a power flow controller for the DAB and a dual-loop controller for the IBC converter.

The switching and conduction losses in the converter's MOSFETs have been calculated in PLECS software using their thermal descriptions provided by the manufacturer. The transformer's core and copper losses have been calculated analytically where the core losses accounted for 73% of the total transformer losses. Based on the loss components, the efficiency has been calculated and compared between the selected converters. The results show that the interleaved buck/boost converter has an efficiency of 99.56% whereas the three-phase DAB has an efficiency of 96.1% at the rated power. Although the interleaved buck/boost converter has higher efficiency than the three-phase DAB, the IBC has a significant disadvantage since it can only operate when the source's battery voltage is lower than the load's battery voltage. On the other hand, the three-phase DAB is independent of the source's battery voltage, making it more reliable but at reduced efficiency. A rough size estimation has been carried out on both converters where it was found that — due to a large inductance — the size of the interleaved buck/boost converter was significantly larger than the three-phase DAB. Therefore, because of its reliability and relatively small volume, the three-phase DAB was concluded to be the best option for this type of application.

Keywords: Battery charger, bi-directional DC-DC converter, three-phase dual active bridge, four-phase interleaved buck/boost converter,planar transformer, PLECS, phase shift controller, dual loop controller.

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Contents

1

Introduction

1.1 Background

Nowadays, batteries are used for multiple applications, such as vehicle propulsion [1]. Conventionally, the nominal voltage of lithium-ion battery cells is low ($\leq 4.2\,\mathrm{V}$), so these are connected in series and parallel to obtain the required load voltage and battery capacity, respectively [2]. In this manner a battery module or pack can be formed to comply with applications' requirements. Typically, the operating characteristics of all battery cells in a battery module are assumed to be similar. To power heavy machinery equipment such as an excavator, a battery with a high capacity and higher voltage is required for satisfying the system's voltage level and energy demands. The work of this heavy machinery equipment depends on the energy transferred from the battery for each day. Due to this, researchers are working on attaining a battery with high energy density and increased volume efficiency. Recharging an equipment's battery each day using a high-quality DC power source is mandatory for the regular equipment usage. Power banks are considered to be one of the DC power sources with high-power ratings consisting of batteries with much higher capacity. Unfortunately, the power banks are not ideal dc voltage sources because their batteries' terminal voltage varies according to different operating conditions and its state of charge. Hence, power banks cannot be connected directly to the equipment's battery for satisfying stringent load requirements. Several applications employ power converters at the output of batteries to mitigate the above problem, thereby providing a stable DC supply. Rechargeable battery-powered electronics have become omnipresent in several other sectors than the electronic field. Inserting a DC/DC converter at the power bank's output provides an option to step up or step down the battery voltage to the desired voltage level. Under such operating conditions, the converter allows lesser usage of the batteries in the power bank and increases the possibility of controlling the battery's state of charge. The selection of these power converters must be bidirectional to ensure the power flow of both the charge and discharge of the batteries. Bidirectional power converters are classified into two categories, namely, isolated and non-isolated types. In general, isolated converter topologies have the advantage of providing galvanic isolation between input and output using a transformer. But the transformer's size and weight increase as the rating of the converter increases. On the other hand, non-isolated converter topologies have the advantage of a simple structure with high efficiency and reduced weight. Silicon is the commonly used raw material in the field of power semiconductor devices because of its high abundance, crystal structure, and low cost. However,

a significant shift has taken place with requirements of improved efficiency. Silicon Carbide and Gallium Nitride have proven to be a potential replacement for silicon semiconductors providing various advantages. Some of their advantages include high switching frequency, sustaining high voltages, higher bandgap, and high breakdown field. In addition, gallium Nitride has a higher electron mobility than silicon carbide, which makes it suitable for high-frequency applications. On the other hand, the thermal conductivity of silicon carbide is superior to gallium nitride, making it the best candidate for high power, high-temperature applications.

1.2 Purpose

The purpose of this thesis is to investigate various converter topologies for a 600V 150kW DC-DC converter that will be used as a battery charger. The objective is to gain a better understanding of the topologies that can support a converter capable of charging a 600V Energy Storage System from an external battery.

1.3 Method

A systematic literature review of possible DC/DC converter topologies will be performed first, followed by a detailed list of technical advantages and disadvantages for each topology. Next, the criteria for selecting the most promising converter topology for this application will be defined. Two converters, one from an isolated and the other from a non-isolated topologies, will be selected. Then, the selected converter topologies will be designed and dimensioned based on the voltage and power rating of the converters. In PLECS, the designed converters will be modelled and simulated to determine the efficiency by identifying the loss components in the switch and transformer. Finally, a comparison is made between the two converters based on the defined selection criteria.

1.4 Scope

For the selected converter topology, a closed-loop PI controller is implemented for both the converters to determine efficiency for different operating points. For an isolated converter, the high-frequency planar transformer is designed based on the power rating. Losses in semiconductors and high-frequency transformers are analyzed in PLECS by adding a thermal description to the switches. At last, detailed thermal model analysis is performed for the selected topologies. The actual hardware design of the chosen typology is not covered in this thesis. Since the thesis focuses mainly on the converter design, no detailed battery modelling is carried out, and the impact of dead time in the semiconductor device is not considered.

2

Investigation of DC/DC Converters

2.1 Selection criteria

DC-DC converter is necessary for interfacing the batteries of heavy machinery equipment for charging purpose. In order to interface, bidirectional converter requirement is mandatory to ensure the charge and discharge of the battery. So, detailed literature study has been done on different converter topologies for interfacing energy storage systems. The investigated DC-DC converter topologies are available in isolated and non-isolated types.

A selection criterion is defined for selecting the best converter topologies that are suitable for this application. These criteria are set based on the converter's purpose in this application. The chosen converter topology must fulfil the following criteria:

- High efficiency
- Light weight
- Small volume
- Low cost
- Low current ripple
- Low voltage ripple at the input and the output
- Capability of high voltage ratio of the converter
- High reliability
- Less control complexity
- Low semiconductor stress
- Possibility of soft switching for the active components

Passive components (Inductor and capacitor) of the converter occupies major volume of the converter. So, the comparison of different converter's size is based on the net volume of the passive component. On the other hand, voltage and current stress across the semiconductor device of each converter is investigated and compared.

2.2 Preliminary selection of converter toplogies

This section presents different DC-DC converter topologies in the isolated and non-isolated types that best suit this application. The advantages and disadvantages of each converter are discussed and compared according to the defined selection

criteria. Based on the comparative analysis, the best converter in the isolated and non-isolated topologies are selected.

2.2.1 Non-isolated converter selection

The selection of a high power rated non-isolated DC-DC converter for this application is challenging due to the high current requirement and operation of a wide voltage range at each side. Non-isolated converter topologies can operate at high efficiency providing high power density simultaneously [3]. According to the literature study, the following non-isolated converter topologies are reviewed and compared: SEPIC/Luo converter, half-bridge converter, multilevel DC-DC converter, multiphase interleaved buck/boost converter, Cuk converter, cascaded buck/boost converter and boost converter with resonant circuit.

Resonant converters are different from the standard PWM converters. The output voltage of those converters can be controlled by varying the switching frequency relative to the resonant frequency. The switching losses of the converter are low at the particular operation of the converter. Nevertheless, the main drawback of the resonant converters is that they suffer significant losses at the light load operation and provide high efficiency only at the operation of the optimal switching frequency [4].

The conventional boost converter faces the problem of high switching loss. A boost converter with a resonant circuit is employed to overcome this problem. Soft switching configuration handles the switching loss problem, which supports the converter to operate at high switching frequencies. Due to the presence of the resonant circuit, the converter can work at zero current switching (ZCS) and zero voltage switching (ZVS) modes [5]. The soft switching characteristic of the converter has a significant impact on the size of the converter and its heat sink requirement. The converter meets the safety regulations without affecting the power flow to the load. During abnormal conditions such as over-voltage and under-voltage, the converter remains protected. However, some of the disadvantages of this converter are low voltage ratio and no bidirectionality, which does not meet the defined selection criteria.

Cascaded buck/boost converter topology is used to obtain an improved voltage ratio compared to a single-stage converter. In a cascaded boost operation, the ripple content in the current is high, whereas the startup current gets reduced compared to the conventional boost topology [6]. The performance of the bidirectional buck-/boost converter is compared with the cascaded buck/boost topology for electrical motor drive applications powered by batteries [7]. According to the comparison, the electrical and thermal stress of the active and passive components of the cascaded buck/boost converter is low, while it requires twice the number of active components. Similarly, the cascaded buck/boost converter is compared with the half-bridge converter in [8]. Based on the findings, the half-bridge converter contains a lower passive component count with lower volume and higher efficiency with lower conduction loss in semiconductor devices. Thus, the half-bridge converter

proves to be a better solution than the cascaded buck/boost converter.

Cuk and SEPIC/Luo converters are current-voltage-current converters suitable for applications involving energy storage systems such as batteries and supercapacitors [5]. They perform the voltage step up and step down operation. Cuk converter is also referred to as a two inductor inverting converter as it produces a negative polarity output voltage, whereas the SEPIC/Luo converter does not invert its output voltage, making it a more suitable converter for this application [9]. The input current of the SEPIC/Luo converter is non-pulsating, while the Cuk converter achieves continuous current both at the input and the output side. Implementation of the gate drive circuit is simple in the SEPIC/Luo converter.

The maximum stresses across the active and passive components of the converter topologies must be carefully considered before selecting the appropriate topology for applying the wide voltage range at the input and the output. Cuk converter, SEPIC/Luo converter and the half-bridge topologies are investigated in [**?**], [9] and [10]. According to the investigations, Table 2.1 summarizes the voltage stress across different components of Cuk, SEPIC/Luo and the half-bridge converters. The input and output voltage of the corresponding converters are represented by V_{in} and V_{out}, respectively. It can be seen that the voltage stress of the semiconductor device is lower in the half-bridge topology compared to the Cuk and SEPIC/Luo converters. In the same way, the SEPIC/Luo converter's transfer capacitor has lower voltage stress than the Cuk converter's case.

Table 2.1: Comparison of active and passive components voltage stress in Cuk, SEPIC/Luo and half-bridge converters

Components	**Half-bridge converter**	**Cuk converter**	**SEPIC/Luo converter**
Transfer capacitor	-	V_{in}+V_{out}	V_{in}
Switch	V_{out}	V_{in}+V_{out}	V_{in}+V_{out}
Diode	V_{out}	V_{in}+V_{out}	V_{in}+V_{out}

The duty cycle variation of the half-bridge, Cuk and the SEPIC/Luo topologies is analysed for the change in the voltage ratio of the respective converters. The Cuk and SEPIC/Luo converters have similar duty cycle variations for the buck and boost operations. During the buck operation, the half-bridge converter's duty cycle is higher than the Cuk and SEPIC/Luo converters, and vice-versa occurs during the boost operation. This fact results in a higher ripple current for all the three topologies during different voltage ratio operations of the converters [8].

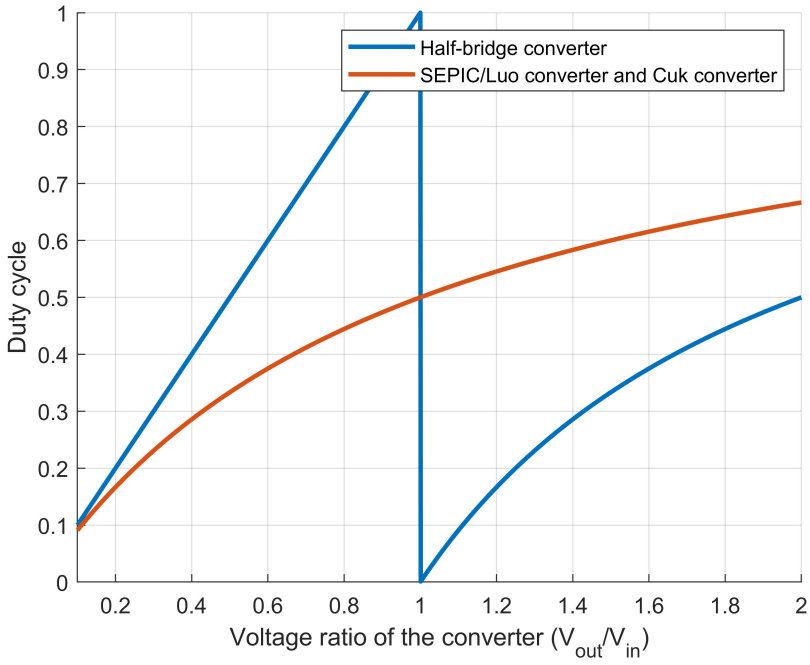

Figure 2.1: Comparison of duty cycle variation as a function of the converter's voltage ratio

Cuk and SEPIC/Luo converters use two inductors, both having the same inductance and energy handling requirements. The RMS current in the inductor of the half-bridge converter is similar to that of the input inductor's RMS current of the Cuk and SEPIC/Luo converters. In Cuk and SEPIC/Luo converters, an output inductor consumes additional power with lower current stress than the input inductor [10]. In comparison between the input and the output inductor, the conduction losses are high in the input inductor, making the heat dissipation more critical.

The current stress of the active components is higher in Cuk and SEPIC/Luo converters than in the half-bridge converter during the same voltage ratio and power operation [10]. As a result, the switching and conduction losses of the active components are low, increasing the efficiency of a half-bridge converter. Due to high current stress, active components with higher current handling capabilities are required for the Cuk and SEPIC/Luo converters than the half-bridge converter. Furthermore, the half-bridge converter's active component cooling is less critical than the Cuk and SEPIC/Luo converters [8].

The significant advantage of the Cuk converter is that it produces a low ripple in the input and output current. The fact that it can be easily isolated makes this converter more appealing [8]. However, the major drawbacks include the requirement of two large inductors leading to high converter volume and from Table 2.1, the voltage rating of the transfer capacitor is high ($V_{in} + V_{out}$). In the case of the SEPIC/Luo converter, the voltage rating of the transfer capacitor is comparatively low (V_{in}). The main drawbacks are the requirement of two large inductors, a discon-

tinuous output current and a large output capacitor [8]. Therefore, for high power operation, the size of the converter tends to be significant.

One of the main advantages of the half-bridge converter over the Cuk and SEPIC/Luo converters is the requirement of a single inductor (instead of two) with half the size. Nevertheless, during boost operation, it produces a discontinuous output current leading to a large output capacitor requirement [8]. Based on the comparative analysis, the half-bridge converter determines to be a better candidate for this application than the Cuk and SEPIC/Luo converters.

The performance of a three-level bidirectional DC-DC converter is evaluated and compared with that of the half-bridge converter. The size of the inductor and the switching frequency is compared for maintaining the same inductor ripple current. According to the analysis, the switching frequency can be much lower in the three-level converter [11]. Moreover, the inductor size of the three-level converter is only one-third of that in the half-bridge converter. For high power applications, inductors with high inductance and current requirements tend to be very heavy, expensive and inefficient [10].

Stress across active components of the three-level and the half-bridge converters are examined. The voltage stress of the semiconductor devices is lower in the three-level converter, while the current stress of the active and passive components of both topologies are similar [11]. The active device component count is two times higher in the three-level converter but with only half the voltage rating in the half-bridge converter.

The efficiency of the half-bridge converter reduces rapidly with lower battery pack voltage. The efficiency is improved by adopting a variable frequency pulse width modulation (VFPWM) scheme [10]. Investigation of the three-level converter shows that it provides higher efficiency than the half-bridge topology. Furthermore, the audible noise as well is drastically reduced in the three-level converter. Hence, the three-level converter shows better performance in almost all aspects when compared to the half-bridge converter.

Multiphase converters are introduced for reducing the size of the converter. The power stage of the converter is split into multiple more minor power stages using an interleaving technique. As a result, the size of each component gets reduced [12]. The multiphase interleaved converter allows minimizing the ripple content in the input and output current. The voltage ratio of the converter increases by n (number of phases connected) times with minimized ripple at the output voltage. The total volume of the inductor gets reduced by n times. With a low ripple at the input and the output current, the required size of the input and output filter becomes low [5].

The interleaving technique has several benefits, including reduced filtering, improved dynamic response, multi-functional capabilities, high efficiency, improved thermal management and better reliability for battery-related applications [5]. Due to the

improved dynamic performance of the converter, a flexible control system can be implemented. Based on the analysis, the cost estimation of the converter is high in the case of complex control and switching circuit implementation [5]. The design of the converter includes components that are surface mounted for getting better efficiency. From the point of view of the converter's cost estimation, surface mounted devices drastically reduce the cost compared with a manual assembly [12]. The heat sink requirement can be avoided by proper design as the converter demonstrates high thermal performance. The size of the power inductors, filter capacitor and heat sink are the bulky components of the converter, which are downsized by the interleaving technique and a high switching frequency operation.

Increasing the number of phases interleaved decreases the current stress of the multiphase converter's active components. The semiconductor with a lower rating can be implemented for the higher number of phase operations [12]. The interleaved converter can operate in synchronous conduction mode (SCM) to achieve soft switching to reduce the switching loss. Under SCM operation, the upper and lower switches turn on complimentarily. However, this operation requires a higher peak current for the same average current as that of CCM mode, which is unacceptable if it exceeds the current limit. Thus, additional soft switching circuits need to be implemented for further improvement in the converter's efficiency during a wide load range [13].

Interleaved converters have an additional characteristic, which is the ability to be fault-tolerant. It operates in the conventional boost operation when any phase is disconnected or a single switch open fails [6]. Industries use this feature and deactivate any single phase for improving efficiency during light load conditions. However, some of the disadvantages of this converter are the converter's sensitivity to the duty cycle change and contains a high ripple in the phase current [5].

Finally, the comparison of multilevel bidirectional DC-Dc converter and multiphase interleaved buck/boost converter is performed for obtaining the best non-isolated topology suitable for the application. Concerning the same number of switching events, a multiphase converter with N_p phase is equivalent to the architecture of a multilevel converter with (N_l-1) levels [14]. From Table 2.2, it can be seen that the component count of both topologies is almost identical. The count of flying capacitors in the multilevel converter is compensated by the number of inductors in the multiphase converter.

Table 2.2: Active and passive component count of the multiphase and multilevel converters depending on the number of phases N_p and levels N_l

Components	**Multiphase converter**	**Multilevel converter**
Capacitors	2	N_l
Inductors	N_p	1
Switches	$2N_p$	$2(N_l\text{-}1)$

The complexity of the drive circuit of both topologies is analysed. Based on the analysis, the drive circuit of the multiphase converter is simple, and it requires a

current balancing algorithm for synchronising each phase current. In the multilevel converter, the flying capacitors need to be balanced and require an additional voltage balancing control to be implemented [15]. Thus, both topologies use a separate algorithm for the drive circuit, and it needs higher effort for the multilevel topology.

The net inductor volume is determined based on the inductance value, the inductor current, the maximum allowed core flux density, the maximum current density and the winding fill factor. These values are determined based on the topologies performance. The comparison of the net inductor volume of both topologies takes place for the same current ripple. Based on the comparison, it can be concluded that the net inductor volume is always higher in the multiphase converter than the multilevel converter [14]. The benefit of smaller inductor volume gets increased when the ratio of ripple to nominal current increases. However, this advantage is compensated by the additional flying capacitor volume absent in the multiphase converter. Electrolytic capacitors have a high capacitance-to-volume ratio but a low current rating. Ceramic and film capacitors have lower capacitance per volume but can withstand higher currents. So, the size of the multilevel converter can be drastically reduced if ideal capacitor technology related to rating and its volume is available.

Fault behavioural analysis is performed on both topologies. In the multiphase converter, if a short circuit of low-side semiconductor devices occurs, the low voltage side gets shorted. On the other hand, low and high voltage sides get connected if it occurs in the high side device. For resolving this issue, the multiphase converter requires the connection of additional protective devices. These protective devices carry nominal current during normal operation and lower the converter's efficiency [14]. Depending on the cost, they can be added to each phase or a group of phases. Open circuit faults cause the degraded performance of the converter with a single-phase disconnected.

Short-circuit faults are tolerated better by the multilevel converter. The serial switch can disconnect the faulty switch during short circuit conditions, and the converter performs in degraded operation with one level less. Such operations need semiconductor devices with higher voltage ratings, but it causes higher losses during normal operation as the on-resistance increases. In contrast, the open-circuit fault of any active component leads to a total system failure [14].

The voltage stress of the switches in the multilevel converter is half the converter's output voltage, while the switches in the multiphase converter get stressed to the total output voltage. Furthermore, the peak voltage across the switches can be significantly higher than this level due to resonance between the circuit's parasitic inductances and the switch's parasitic output capacitances [15]. As a result, a safety margin must be established while selecting the switch's ratings. From the above analysis, it is clear that the voltage rating of the multiphase converter is two times higher than the multilevel converter.

The net loss of the multilevel converter is equivalent to that of the multiphase

converter. The semiconductor losses are comparatively higher in the multiphase converter. The core loss of the inductor in the multilevel converter is lower because of its smaller inductor volume for the same current ripple. At the same time, the conduction loss in the inductor is almost the same for both topologies. Flying capacitors produce additional losses in the multilevel converter, which is not present in the multiphase converter. At last, it can be concluded that the efficiency of both topologies is similar [14].

Table 2.3: Comparison of multilevel and mutliphase converter

Factors	**Multiphase converter**	**Multilevel converter**
Component count	Similar	Similar
Control complexity	Simple	Needs additional effort
Inductor size	Low	Comparatively lower
Capacitor size	Comparatively lower	Low
Fault tolerance	Tolerant to open circuit fault	Tolerant to short circuit fault
Efficiency	Similar	Similar

The result of the comparison between the multilevel DC-DC converter and the multiphase interleaved buck/boost converter is shown in Table 2.3. According to the comparative analysis, both converter's advantages and disadvantages are analysed. According to the comparison, the multiphase converter provides a slightly improved performance than the multilevel converter. Finally, the multiphase interleaved buck-/boost converter is chosen as the best non-isolated topology suitable for the application.

2.2.2 Isolated converter selection

For an isolated converter, galvanic isolation is an inherent property responsible for voltage adjusting. An AC transformer (galvanic isolation) isolates the two active bridges during a DC fault and prevents the fault from propagating. However, one of the drawbacks of using an AC transformer is that they occupy a large footprint as they are large for high power applications[16]. The considered isolated converters are divided into two groups based on the high frequency (HF) network,

- Dual active bridge without resonant HF network
    1. Single-phase dual active bridge
    2. Three-phase dual active bridge
    3. Bidirectional and isolated push pull converter
    4. Bidirectional and isolated current doubler topology
- Dual active bridge with resonant HF network
    1. Series resonant LLC converter

For the first group of converters, a high-frequency transformer couples the DC-AC and AC-DC network. In this configuration, a basic non-resonant HF network, usually an inductor, is connected in series with the transformer's leakage inductance. In general, this group of converters has an advantage over traditional flyback and

forward converters in that it operates with low switching loss. The second group of converters are the so-called resonant DC-DC converters which employ a resonant HF network. By adding a resonant network, the current waveforms of the switches can be modified, allowing for lower switching loss compared to the converters of group one.

2.2.2.1 Single-phase dual active bridge

In a single-phase dual active bridge, two voltage sourced full bridges are connected through a high-frequency transformer. An inductor is connected in series with the leakage inductance of the transformer for power transfer. Since the circuit is symmetric, a bidirectional power flow can be achieved using a phase shift between the two bridges. The main advantages of this converter are the low number of passive components, and the currents in the switch are evenly shared. Apart from this, the dual active bridge has inherent soft switching properties, thereby increasing the efficiency[17]. The drawback in the dual active bridge is that the transformer current waveform changes depending on the operating point, and for specific operating points, the transformer RMS is very high. Above all, the output ripple voltage is very high, and thus a large capacitor is needed as a filter, and the capacitor RMS current is high.

2.2.2.2 Three-phase dual active bridge

In a three-phase dual active bridge, three half bridges on the primary and three half bridges on the secondary are connected via three single-phase transformers. Similar to a single-phase DAB, an inductor is needed for each phase for power transfer[18]. For the transfer of power, a phase shift modulation scheme is employed in the three-phase DAB. The advantage of the three-phase DAB is that the total transformer VA rating, switch VA ratings, and magnetic energy storage capacity are low. The ripple voltage is relatively low in a three-phase DAB, and hence the size of the filter capacitor and the capacitor RMS current is reduced. Depending on the operating point, the three-phase DAB has the property of soft switching, which results in increased efficiency. The main disadvantage of three-phase DAB is the high number of switches (12 semiconductor switches) and a high number of gate drivers accordingly. Apart from this, the converter efficiency drops down drastically for a specific operating point due to high conduction and switching loss as the converter operates in hard switching.

2.2.2.3 Full bridge converter with current doubler and push-pull circuit

For a bidirectional and isolated full-bridge converter, a voltage sourced full bridge on the primary side and a current sourced full-bridge is connected on the secondary side through a transformer. The control of power flow is carried out using the duty cycle ‘D’[19]. For bidirectional and isolated full-bridge converters, zero voltage

switching occurs on the primary side switches and zero current switching occurs on the secondary side switches. Compared to a single-phase DAB, the capacitor RMS current is considerably low in the isolated full-bridge converter. One of the significant drawbacks in the isolated full-bridge is the volume consumption of the DC inductor[20]. In addition to this, the secondary switches often connect with the DC inductor in series to the transformer leakage inductance, resulting in voltage spikes. Hence, a snubber circuit is needed. Compared to LLC and DAB converters, the VA rating of the semiconductor switches is considerably higher in the isolated full-bridge converter.

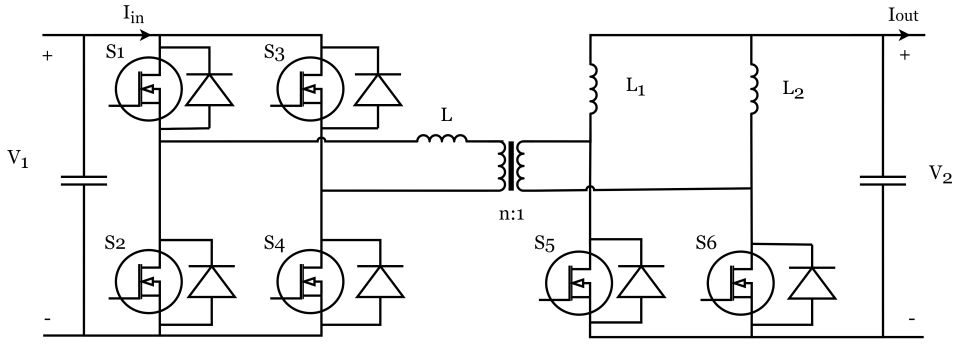

Figure 2.2: Bidirectional and isolated converter with current doubler on the secondary side

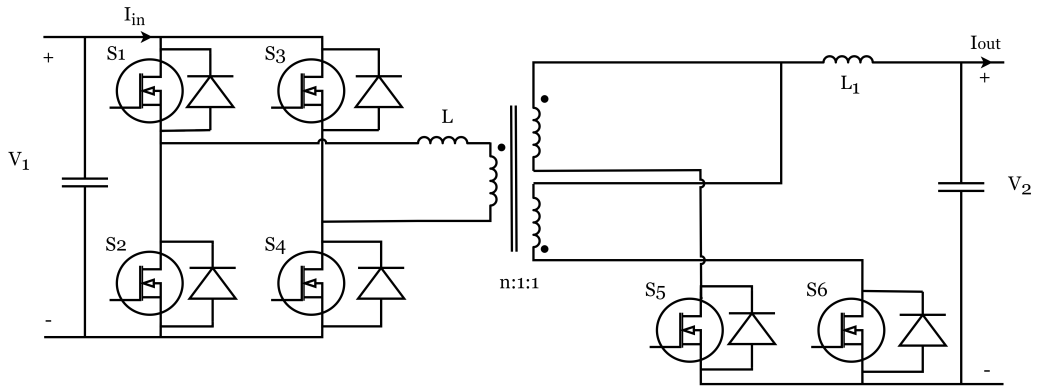

Figure 2.3: Bidirectional and isolated converter with push-pull circuit on the secondary side

Different AC-DC converter topologies like the current doubler[21] and push-pull topology[22] can be employed for the secondary side of the isolated full-bridge converter. Compared to a full-bridge converter, two inductors are needed for the current doubler, as shown in figure 2.2 and the current magnitude of two inductor currents is significantly higher, resulting in higher transformer VA ratings. For the current doubler, the voltage rating of the semiconductor switches on the secondary side is twice the rated voltage of the full-bridge switches[20]. A centre-tapped transformer with two LV side windings connects with the secondary side for the push-pull circuit as shown in figure 2.3. Hence, current flows in each winding only during half a

switching period, resulting in higher transformer VA ratings. Similar to the current doubler, the rated voltage on the secondary side is twice that of the full-bridge converter.

2.2.2.4 Series resonant LLC converter

Figure 2.4 shows the series resonant LLC converter. In a series resonant LLC converter, a capacitor, which acts as a DC blocking capacitor, prevents the HF transformer's saturation, is connected in series with the leakage inductance of the transformer[23]. The converter's performance varies based on the modulation scheme employed. The conventional modulation scheme is very similar to that of a single-phase DAB, i.e., a power transfer is obtained by a phase shift between primary and secondary side voltage. To improve the efficiency, an optimal modulation scheme is employed, which utilizes the ability of the full-bridge to generate a zero-voltage state across the transformer instead of a triangular voltage[20]. This reduces the transformer RMS current and switching loss. Hence the converter can be operated at a higher frequency, thereby increasing the power density of the converter when compared to DAB converters. Apart from the phase shift between primary and secondary side voltage, there are inner phase shifts between the two legs of the input and output bridges in the optimal modulation scheme[24].

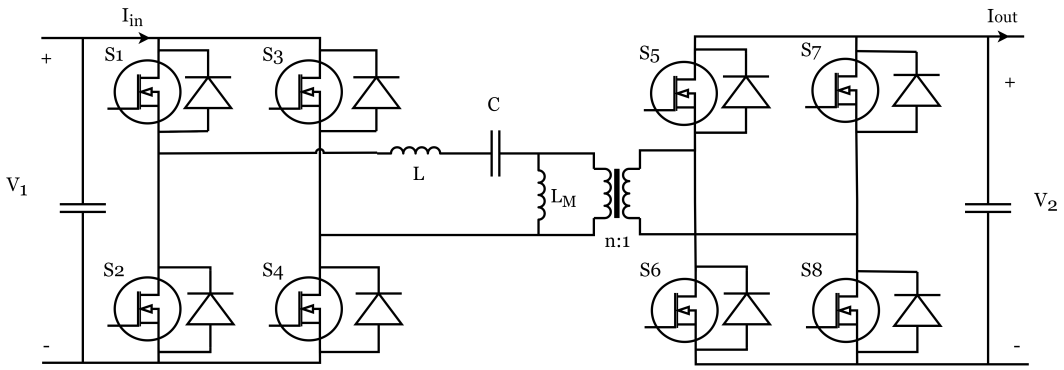

Figure 2.4: Bidirectional series resonant LLC converter with two voltage sourced ports

Compared to the single-phase DAB, when the series resonant LLC converter is operated using the conventional modulation scheme, the transformer VA ratings and switch VA ratings are low. On the other hand, an inductor with a higher maximum energy storage capability and a series capacitor is required for the resonant tank. Hence the volume consumption of the LLC converter is increased compared to a DAB configuration, which requires less volume for the inductor. The best average efficiency is achieved for the series resonant LLC converter with an optimal modulation scheme among the examined DC-DC converters with two voltage sources.

2.2.2.5 Comparison of isolated converter topologies

Based on the analysis made, a comparison bar graph is made, as shown in figure 2.5. Among the considered bi-directional DC-DC converter topologies, the three-phase DAB has the highest number of active components with 12 semiconductor switches (6 for the primary bridge and 6 for the secondary bridge). Thus, the number of gate driver circuits needed is high. A wide input and output voltage range is achieved for a single-phase and a three-phase DAB with reduced efficiency. In contrast, all the other converters are operated at a limited voltage range. A large soft-switching range is achievable in a series resonant LLC with an optimal modulation scheme, while the other converters operate at hard switching at light loads. Due to low transformer RMS current and low switching loss, an LLC with an optimal modulation scheme, has the highest average efficiency among the considered topologies. The transformer rating is relatively lower for a three-phase DAB and a resonant converters. The modulation scheme needs to control the switching current waveforms for soft switching, making the controller more complex for a series resonant LLC with an optimal modulation scheme.

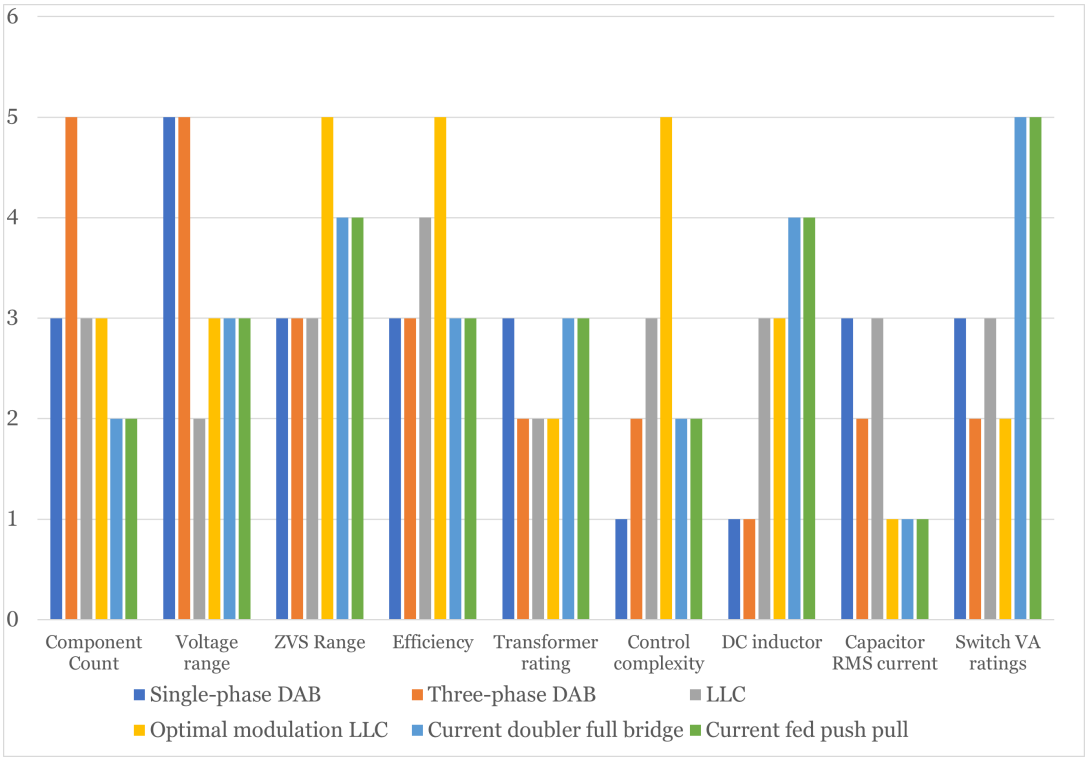

Figure 2.5: Comparison of isolated converter topologies based on the selection criteria

For dual active bridge converters, the leakage inductance of the transformer provides the required phase inductance for power transfer, or an external inductor smaller in size can be connected in series with the leakage inductance. On the other hand, for other converters, an external inductor is needed, which makes the power density of the converter low. The single-phase DAB and the LLC converter has higher ca-

pacitor RMS current, while the three-phase DAB has one-third of the RMS current compared to a single-phase DAB. One of the critical criteria is the switch VA rating because MOSFETs cannot be used for higher VA ratings, and an IGBT must be used instead. Using an IGBT as the semiconductor switch limits the converter's operating frequency, resulting in low power density, which is undesirable. Comparing the switch VA ratings, the three phase-DAB and the LLC with an optimal modulation technique shows the lowest power rating of the switches.

Based on the findings, the three-phase DAB is considered to be the most promising converter topology in the isolated family due to its low switch ratings, less control complexity, high power density and high voltage range capability.

3

Theory

3.1 Non-isolated converter topology

3.1.1 Boost converter

A boost converter is a high voltage gain DC-DC converter that operates by controlling the switching events of the switch S_1 as seen in Figure 3.1. It can operate within two modes, namely, continuous conduction mode (CCM) and discontinuous conduction mode (DCM) depending in the current flowing through L_1. Here, the operation of CCM is considered. The conventional boost converter circuit diagram is depicted in Figure 3.1.

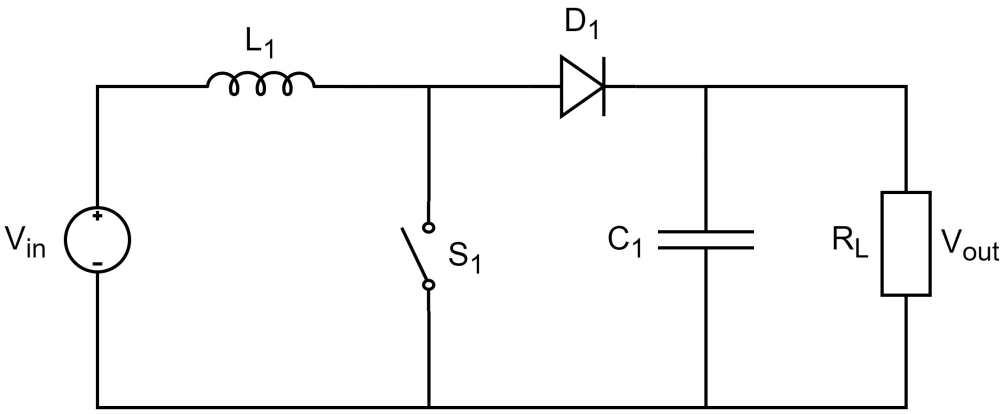

Figure 3.1: Boost converter circuit diagram

When the switch S_1 is closed, diode D_1 gets reverse biased. During this period, the capacitor C_1 gets discharged across the load R_L, and the inductor gets charged from the supply.
On the other hand, when S_1 is closed, diode D_1 becomes forward biased and starts to conduct the inductor current to the load. In this case, the inductor discharges some of its stored energy to the load, and the capacitor gets charged. The voltage gain between the input and output voltage of the converter is given by,

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{3.1}$$

where D represents the duty ratio of the switch S_1, V_{in} and V_{out} are the input and output voltage of the converter, respectively. According to this relation, a large duty

ratio is required to achieve a high voltage gain. This causes a very high capacitance requirement leading to a large volume and weight of the converter. During switch on conditions, the capacitor supplies its stored energy to the load limiting ripple in the output voltage. Furthermore, during high power operation, the inductor must be designed so that its core does not get saturated as the saturation flux of the core gets reduced at elevated temperatures [25]. In the case of inductor reaching saturation, it begins to store less energy, and the ripple current rises, resulting in a decrease in efficiency. Finally, it can be concluded that a conventional boost converter requires larger capacitance and inductance for reducing ripple voltage and current ripple at high power conversion.

3.1.2 Interleaved boost converter

Interleaving, also called multi-phasing, is a technique that connects DC-DC converter in parallel operation for sharing power between different phases. This technique lowers the ripple at the input and output, which helps in reducing the size, weight and volume of the filter components of the converter. The supply current is split into n phases reducing conduction loss and inductor loss in each phase leading to higher efficiency. This converter is used for applications requiring low current ripple, improved dynamic performance, high frequency and high power density [26].

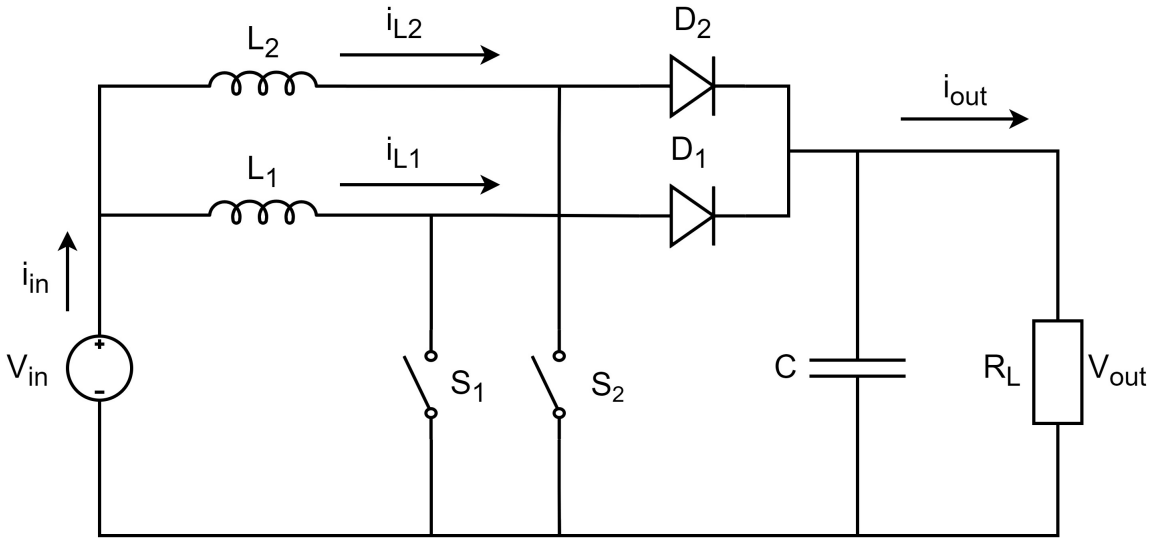

Figure 3.2: Schematic diagram of a two-phase interleaved boost converter

The circuit diagram of a 2 phase interleaved boost converter is depicted in Figure 3.2. It is operated by phase shifting the switching events of the switches in the 2 phases. The phase difference between switching events is given by

$$P.D = \frac{360^\circ}{n} \tag{3.2}$$

where n represents the total number of phases connected, and $P.D$ provides the phase difference of switching between each switch for the n-phase interleaved boost converter. Thus, for a two-phase interleaved boost converter (n=2), two switches

are operated at 180° phase shift. This causes the inductor currents in each phase to be phase shifted by 180°. As a result, the input current becomes the sum of the phase currents as they are out of phase and thus cancel the ripples of each other, so that ripple content in input current gets reduced.

3.1.2.1 Modes of operation

The operation of this converter for the ideal case condition (input power P_{in} = output power P_{out}) is discussed in this section. The inductance of each phase is assumed to be the same ($L_1 = L_2$). Therefore, the switches in each phase are operated under the same duty ratio ($D_1 = D_2$) with a time delay of $T_s/2$. This topology operates in 4 different modes of operation[27].

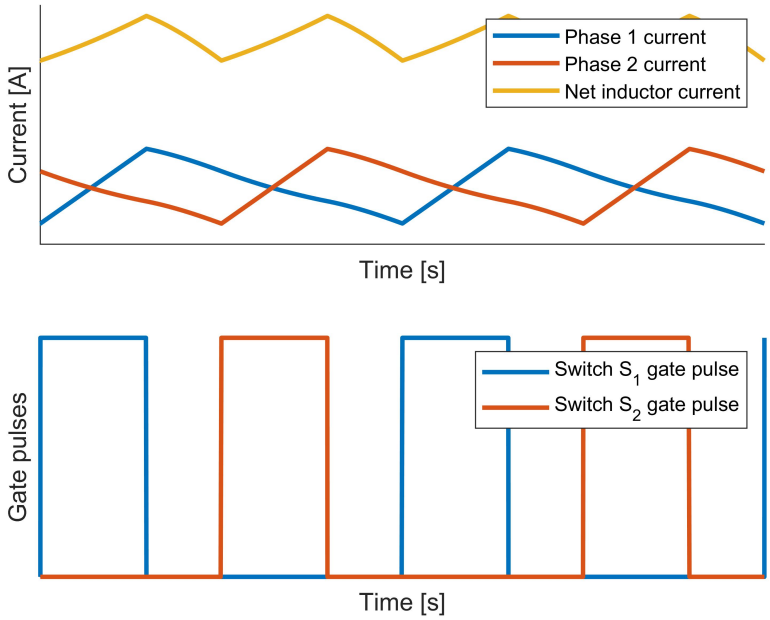

Figure 3.3: Ideal current waveforms of a two-phase interleaved boost converter

1. **Mode 1 (Both switches S_1 and S_2 are closed)**
   During this mode of operation, diodes D_1 and D_2 get reverse biased, and the capacitor discharges to supply the load. The input supplies energy to the inductor in both phases. The voltage across each phase inductance is provided by

$$V_{L_1} = V_{in} \tag{3.3}$$

$$V_{L_2} = V_{in} \tag{3.4}$$

   where V_{L_1} and V_{L_2} are the voltage across phase 1 inductance L_1 and phase 2 inductance L_2 respectively.

According to (3.3) and (3.4), L_1 and L_2 get charged, their phase currents i_{L_1} and i_{L_2} increase linearly during this period.

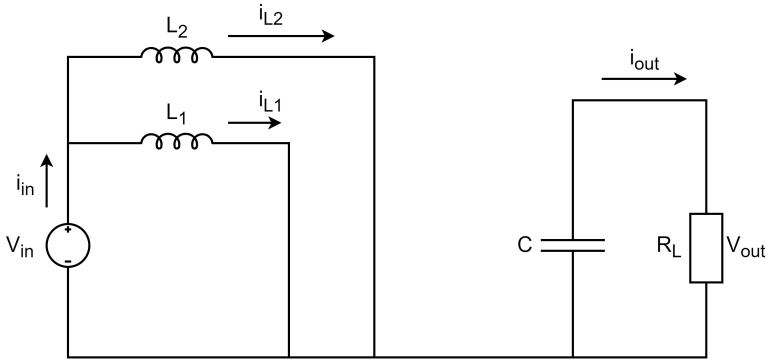

Figure 3.4: Mode 1 of a two-phase interleaved boost converter

2. **Mode 2 (Switch S_1 is closed and switch S_2 is open)**
   During this mode of operation, diode D_1 gets reverse biased and the inductor L_1 gets charged from the supply. Diode D_2 becomes forward biased and conducts phase current i_{L_2} to transfer some of the inductor L_2's stored energy to the load. In this mode, the capacitor gets charged from the phase 2 current and the voltage across each phase inductance is given by

$$V_{L_1} = V_{in} \tag{3.5}$$

$$V_{L_2} = V_{in} - V_{out} \tag{3.6}$$

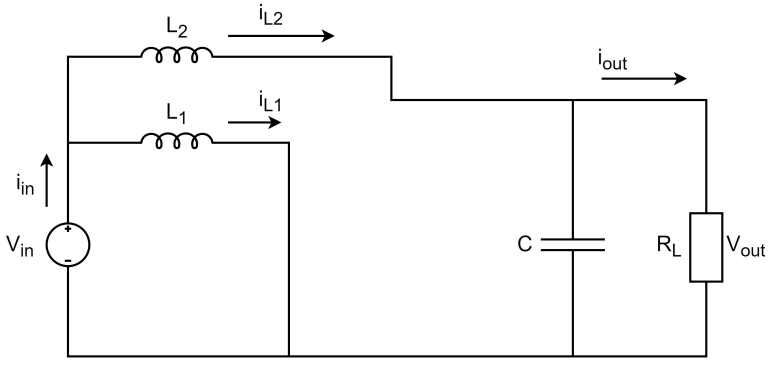

Figure 3.5: Mode 2 of a two-phase interleaved boost converter

According to (3.5) and (3.6), L_1 gets charged and L_2 discharges, their phase currents i_{L_1} and i_{L_2} increases and decreases respectively during this period.

3. **Mode 3 (Switch S_1 is open and switch S_2 is closed)**
   During this mode of operation, diode D_1 becomes forward biased and the inductor L_1 discharges some of its stored energy to the load. Inductor L_2 gets charged from the supply as diode D_2 becomes reverse biased. In this mode,

the capacitor gets charged from the phase 1 current and the voltage across each phase inductance is given by

$$V_{L_1} = V_{in} - V_{out} \tag{3.7}$$

$$V_{L_2} = V_{in} \tag{3.8}$$

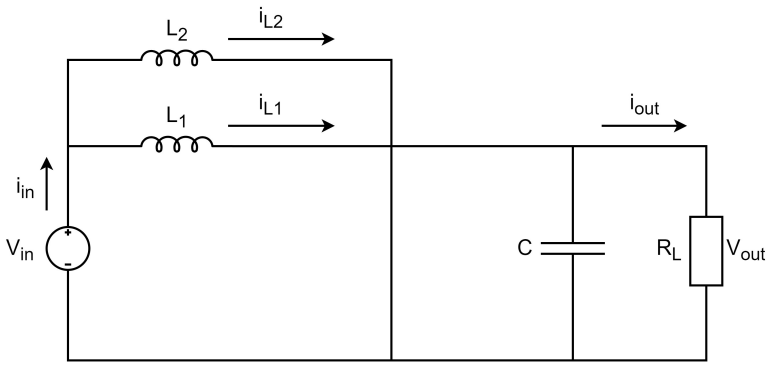

Figure 3.6: Mode 3 of a two-phase interleaved boost converter

According to (3.7) and (3.8), L_1 discharges and L_2 gets charged, their phase currents i_{L_1} and i_{L_2} decreases and increases respectively during this period.

4. **Mode 4 (Both switches S_1 and S_2 are open)**
During this mode of operation, diodes D_1 and D_2 becomes forward biased. This causes inductor L_1 and L_2 to discharge some of its stored energy to the load. In this mode, the net inductor current starts to charge the capacitor and voltage across each phase inductance is given by

$$V_{L_1} = V_{in} - V_{out} \tag{3.9}$$

$$V_{L_2} = V_{in} - V_{out} \tag{3.10}$$

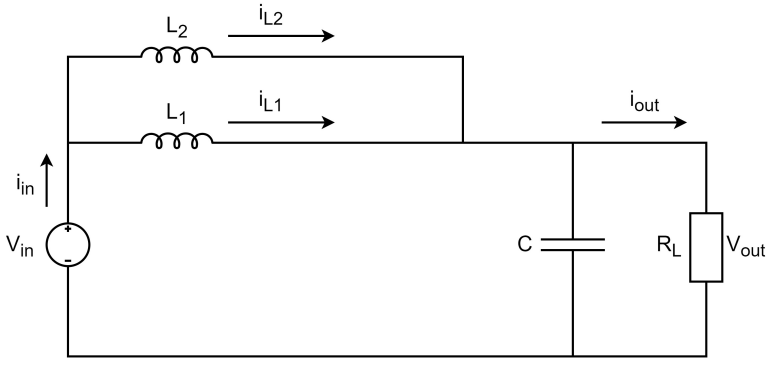

Figure 3.7: Mode 4 of a two-phase interleaved boost converter

According to (3.9) and (3.10), L_1 and L_2 discharge, their phase currents i_{L_1} and i_{L_2} decrease linearly during this period.

3.1.3 Buck converter

A buck converter is a step-down DC-DC converter. It is a switched-mode power supply that uses active and passive components for regulating DC voltages.

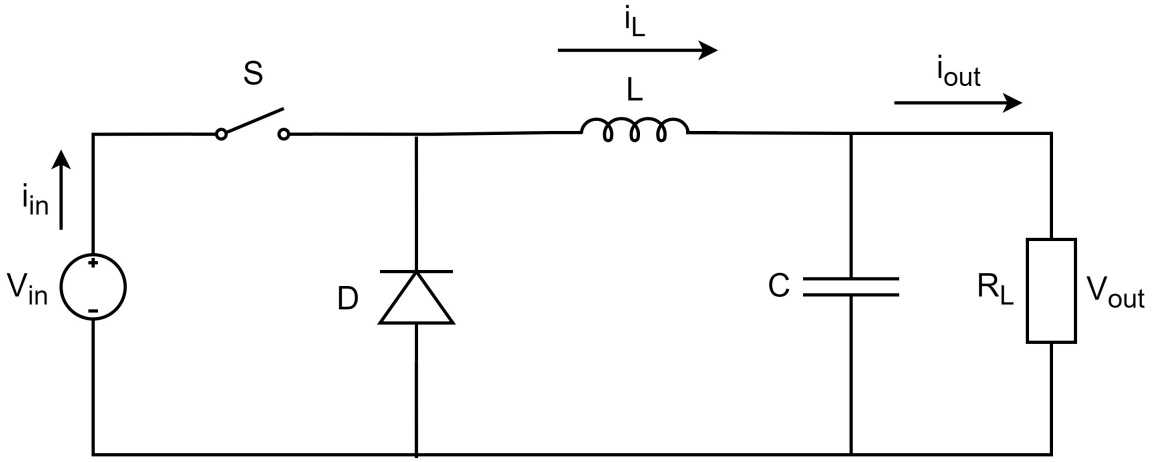

Figure 3.8: Buck converter circuit diagram

When the switch S is on, diode D gets reverse biased, and the input transfers energy to the load and the inductor. Thus, the inductor current increases during this period. On the other hand, when the switch is off, the diode gets forward biased and starts to conduct the inductor current. During this period, the inductor discharges its stored energy to load, making the current to decrease. The relation between the output voltage and the input voltage is

$$\frac{V_{out}}{V_{in}} = D \tag{3.11}$$

where D represents the duty cycle of the switch, V_{out} and V_{in} are the output and input voltage of buck converter, respectively. This equation is valid only for continuous conduction mode, which occurs when the average current of the inductor is greater than zero.

3.1.4 Interleaved buck converter

An interleaved buck converter is obtained by connecting multiple buck converters using the same interleaving technique as that of the boost topology. This type of converter is typically used in applications that require non-isolation, step down conversion ratio and high output current with low ripple content.

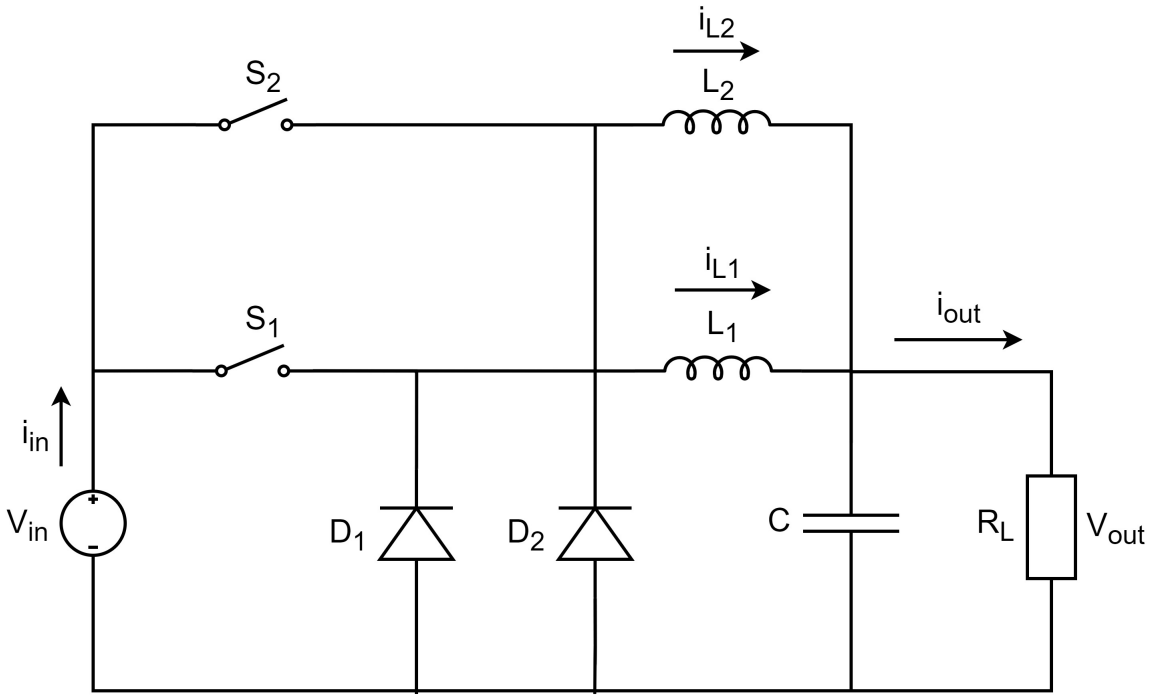

Figure 3.9: Schematic diagram of a two-phase interleaved buck converter

The model of a two-phase interleaved buck converter is shown in Figure 3.9. In this converter, switches S_1 and S_2 operate at 180°phase shift, which makes the inductor currents phase-shifted by 180°. In an n-phase interleaved buck converter, the phase shift between each phase is similar to that of an interleaved boost converter.

From Figure 3.9, the sum of the inductor currents is i_{out}, and in this way, the net power supplied to load is shared by each phase. Due to current ripple cancellation between phase currents, the ripple value of the load current becomes low in comparison with the inductor current. Therefore, a current with lower ripple content enters the capacitor. This results in less need of capacitance for the same output ripple voltage implementation compared to a simple buck topology. Similarly, the ripple frequency of the load current is two times higher than that of the phase currents. As a result, the average inductor current is half of the average inductor current in a simple buck topology. This results in a low inductance requirement for each phase for an interleaved operation compared with a simple buck topology.

3.1.4.1 Modes of operation

An interleaved buck converter operates in several modes depending on the number of phases connected in parallel. The waveforms of phase current and load current of a 2 phase interleaved buck converter is depicted in Figure 3.10. This converter works in 4 different modes of operation depending upon the duty cycle of the switches connected [28].

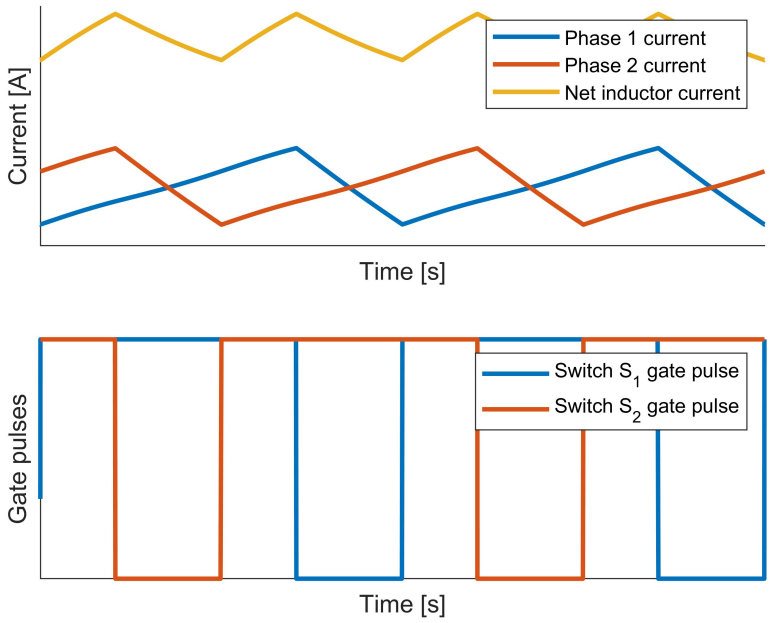

Figure 3.10: Current waveform and switching schemes of a two-phase interleaved buck converter for D>0.5

These wave-forms are plotted for the ideal case of the converter, assuming phase inductance L_1 and L_2 to be equal along with ideal switches used.

1. **Mode 1 (Both switches S_1 and S_2 are closed)**
   When both switches S_1 and S_2 are closed, the inductor in phase 1 and phase 2 gets charged from the supply. As a result, the diodes in both phases get reverse biased. This causes currents in both phases to increase linearly. The voltage across each phase inductance is given by

$$V_{L_1} = V_{in} - V_{out} \tag{3.12}$$

$$V_{L_2} = V_{in} - V_{out} \tag{3.13}$$

   where V_{in} and V_{out} represents the supply voltage and output voltage respectively.

2. **Mode 2 (Switch S_1 is closed and switch S_2 is open)**
   During this mode of operation, only inductor L_1 gets charged from the supply. On the other hand, inductor L_2 discharges and freewheels through the diode in phase 2, transferring some of its stored energy to the load. The voltage across each phase inductance become

$$V_{L_1} = V_{in} - V_{out} \tag{3.14}$$

$$V_{L_2} = -V_{out} \tag{3.15}$$

causing phase 1 current to increase linearly and phase 2 current to decrease linearly during this period.

3. **Mode 3 (Switch S_1 is open and switch S_2 is closed)**
   During this mode of operation, inductor L_1 discharges and freewheels through the diode in phase 1, transferring some of its stored energy to the load. At the same time, inductor L_2 gets charged from the supply. The voltage across each phase inductance are

$$V_{L_1} = -V_{out} \tag{3.16}$$

$$V_{L_2} = V_{in} - V_{out} \tag{3.17}$$

   causing phase 1 current to decrease linearly and phase 2 current to increase linearly during this period.

4. **Mode 4 (Both switches S_1 and S_2 are open)**
   During this mode of operation, both the inductor L_1 and L_2 discharge and transfer some of its stored energy to the load. The diodes in both phases become forward-biased and start to conduct inductor current during this period. The voltage across each phase inductance

$$V_{L_1} = -V_{out} \tag{3.18}$$

$$V_{L_2} = -V_{out} \tag{3.19}$$

   causeing currents in both phases to decrease linearly.

The relation between the output voltage and the input voltage,

$$\frac{V_{out}}{V_{in}} = D \tag{3.20}$$

is similar to that of simple buck topology. The voltage stress across each switch is similar to that of the buck converter and equals the supply voltage. Thus, the high voltage rated switches need to be used in this converter to withstand the supply voltage. However, switches are operated in hard switching conditions, and this disturbs the efficiency of the converter. Therefore, in order to achieve better dynamics and improved power density, the converter needs to be operated at higher switching frequencies [29]. Nevertheless, at very high switching frequencies, switching losses are high, affecting the converter's efficiency. Therefore, the switching frequency of the converter needs to be optimized based on its efficiency.

3.1.5 Number of phase selection

The interleaved buck/boost converter operates in boost mode for the forward direction and buck operation in the reverse direction. Single-phase converters handle all the output power flowing through a pair of MOSFETs and inductor combinations. All the power losses occur within those components. Designing such converters for applications requiring an output current greater than 100 A becomes difficult and

expensive [30].

Multiphase converters provide an even distribution of losses across each phase. The selection of components becomes more accessible as each phase handles only a part of the output current. This type of converter offers a much higher efficiency over a wide load range compared to an equivalent single-phase converter. The performance of a multiphase converter is further improved by a lower requirement of input and output capacitance. Nowadays, the controller of multiphase converters allow phases to be added and dropped depending on the load current requirement [30]. This helps in tuning the phase count of the converter for optimal efficiency across various applications.

At lower currents, converters with few phases are operated under DCM mode to minimize switching losses. However, as the load current increases, the conduction losses become dominant, and in order to improve the efficiency, converters with an increased phase count are employed.

An increasing number of phases affect the efficiency of the converter as the switching losses become dominant [31]. The graph in Figure 3.11 depicts the change in efficiency as the number of phases increases. Hence, a compromise needs to be made between the efficiency and phase count of the converter.

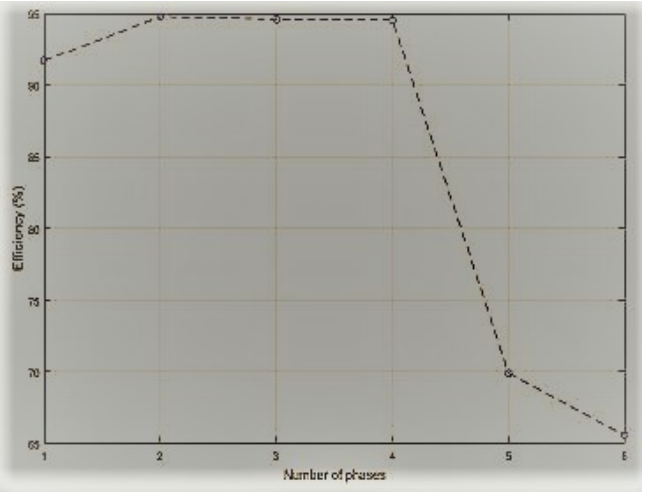

Figure 3.11: Change of efficiency with number of phases [31]

For increased phase operation, input and output current ripple gets reduced in the buck mode of operation. In contrast, the input current ripple and output voltage ripple gets reduced in the boost mode of operation. For selecting the optimal number of phases for the converter, operation of the converter in boost mode and buck mode are analysed for different phases:

1. **Interleaved boost operation**
   The input current ripple of a single-phase boost converter is given as

$$\Delta I_{in} = \frac{V_{out}T}{L} DD' \tag{3.21}$$

where V_{out} is the output voltage, T is the switching time period according to the switching frequency of the switches, while D and D' represents the on and off duty ratios of the switches, respectively. Unlike a single-phase converter, the input current ripple of an n-phase interleaved converter (IBC) consists of n parts according to the duty ratio of the switches [32]. Therefore, the frequency of the input current gets increased by n times for n-phase operation. For various phase operations, the variation of input current ripple according to duty ratio is given by

$$\Delta I_{in} = \frac{V_{out}}{L_{ph}} (N_{on\_sw} - nD) \frac{T}{n} d \tag{3.22}$$

where n is the number of phases, N_{on_sw} is the number of on switches during a time period τ of input current, while d and d' are the rising and falling time period of the input current ($d = \frac{t_r}{\tau}$, d' = 1-d). The rising time of the input current within the time period τ is given by t_r.

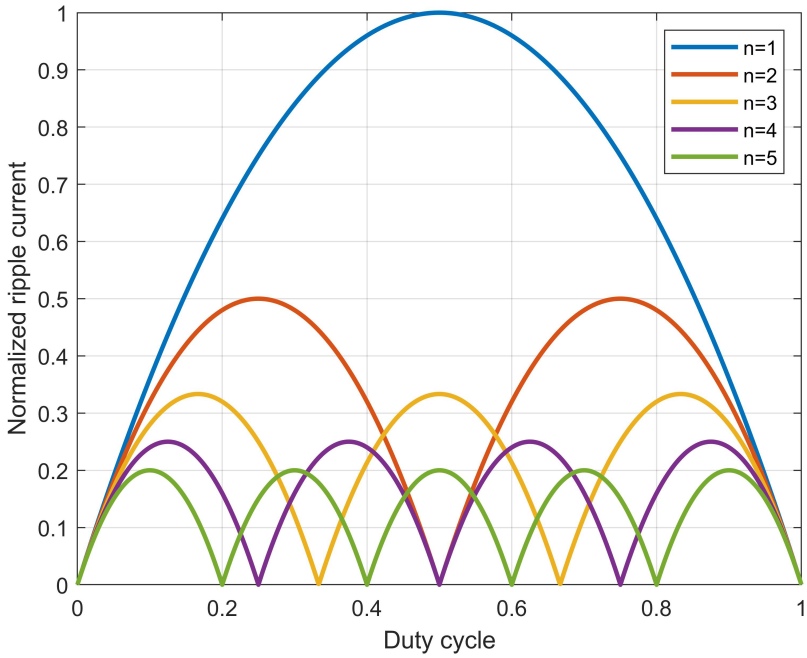

Figure 3.12: Input current ripple as a function of duty cycle for a different number phases.

Figure 3.12 shows the normalized variation of input ripple current to duty cycle for constant output voltage and identical inductors for each phase operation. It can be seen that the input current ripple becomes zero at D/n times the duty ratio (for example, at 0.25, 0.5 and 0.75 for four-phase IBC), and it is inversely proportional to the number of phases. Thus, the input current ripple gets reduced significantly in the three-phases and above compared to a

single-phase boost converter.

The output voltage ripple is determined by the charge of the output current ripple (Q_C) caused by the charging/discharging of the capacitor. The average charge is identical for the case of n-phase IBC. The output voltage ripple of n-phase IBC for a selected switching frequency f_{sw} is given as,

$$\Delta V_o = \frac{Q_C}{C} = \frac{I_{out} dd'}{f_{sw} C n^2 D'} \tag{3.23}$$

gets reduced by a factor of $1/n^2$ as the number of phases increases. From Figure 3.13, it is evident that for a multiphase IBC, the output voltage ripple is lower compared to a single-phase boost converter.

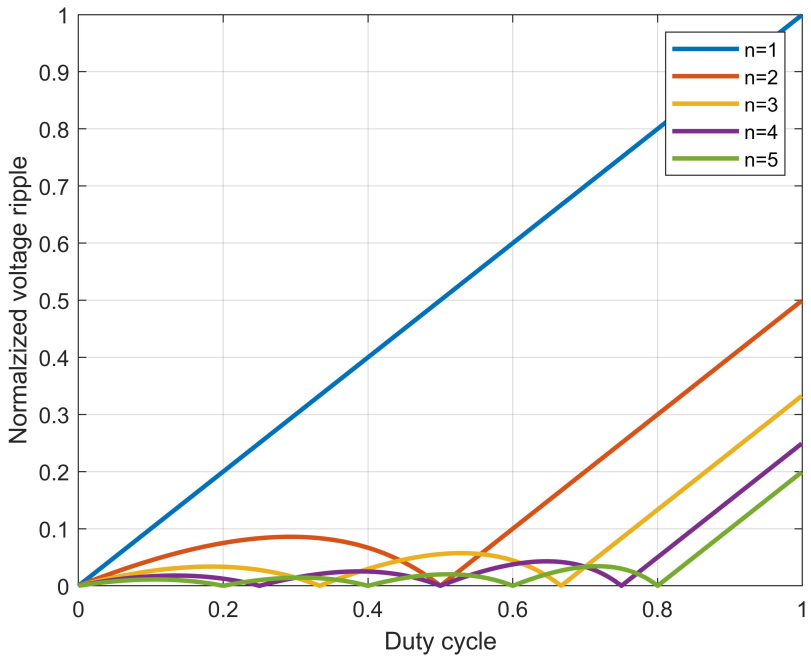

Figure 3.13: Output voltage ripple as a function of duty cycle for a different number phases.

2. **Interleaved buck operation**
   Designing a multiphase buck converter decreases the RMS input current flowing through the input capacitor, which reduces the ripple in the input voltage V_{in} [30]. This allows for a reduced input capacitance requirement for keeping the input voltage ripple within its limits.

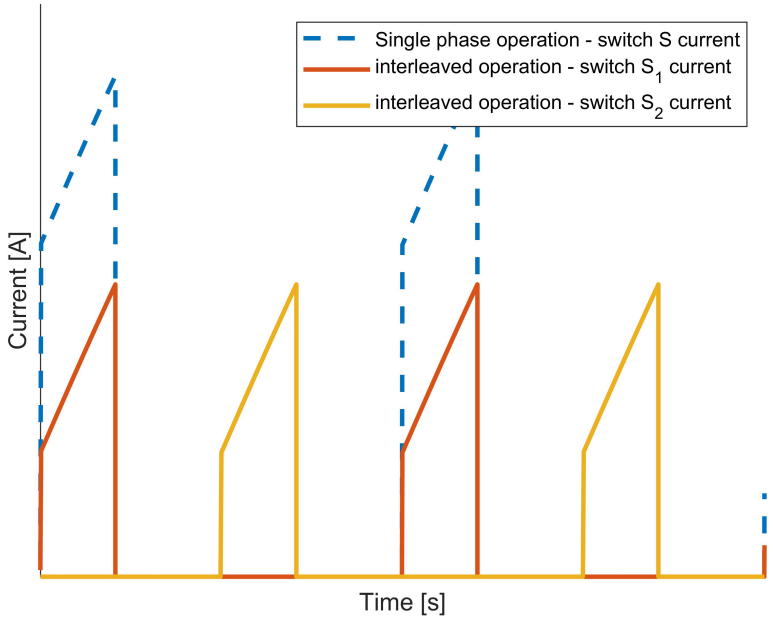

Figure 3.14: Input current waveform of an interleaved buck converter

Figure 3.14 shows the comparison of the input current waveform of the single-phase and two-phase operation. It can be seen that the input RMS and peak current have been significantly reduced by adding a phase. This reduces the input capacitance requirement and lowers the stress across switch in each phase. The normalized input RMS current of an n-phase interleaved buck converter is as follows,

$$I_{in_{norm}}(RMS) = \sqrt{\left(D - \frac{m}{n}\right)\left(\frac{1+m}{n} - D\right)} \tag{3.24}$$

where m = floor (nD). floor(x) is a MATLAB function used to round the element x to the nearest integer equal to or lesser than the element.

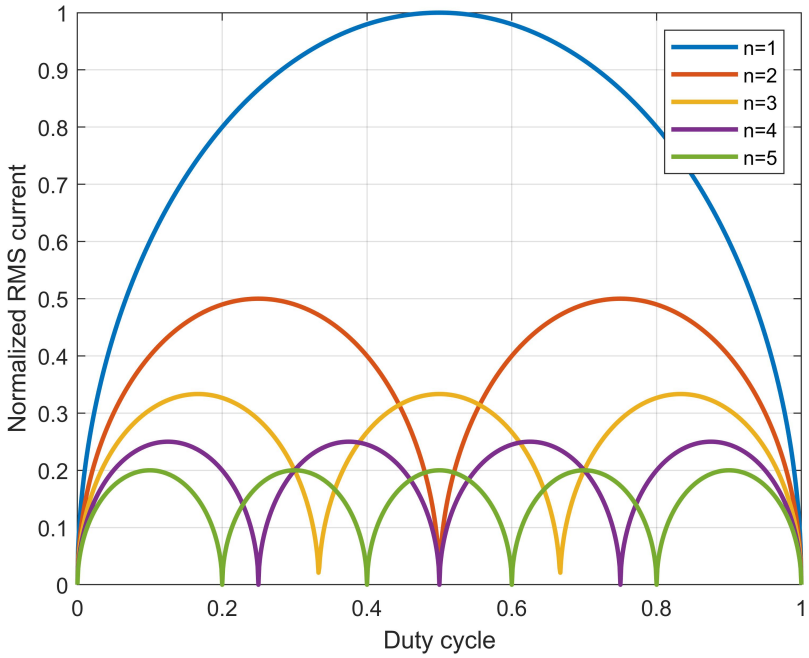

Figure 3.15: Normalized input RMS current as a function of duty cycle for a different number of phases

Figure 3.15 shows that as the number of phases increases, the amount of current that needs to be handled by the input capacitor reduces by 50% or more depending on the duty cycle. For each multiphase operation, the input RMS current drops to zero at certain duty cycle as the ripple current in each phase cancels each other.

The output current ripple is much lower in comparison with phase inductor current ripple. Therefore, a smaller output current ripple produces a lower output voltage ripple which in turn lowers the output capacitance requirement for keeping V_{out} within tolerance. The normalized output ripple current through the output capacitor is given by

$$I_{out_{ripple\_norm}} = \frac{n}{D(1-D)}\left(D - \frac{m}{n}\right)\left(\frac{1+m}{n} - D\right) \tag{3.25}$$

$$I_{out_{ripple\_norm}} = \frac{n}{D(1-D)}(D - \frac{m}{n})(\frac{1+m}{n} - D) \tag{3.26}$$

and it is not valid for single-phase operation. Similar to the input current, each phase inductor current at various duty cycle operations cancels out each other producing no output current ripple. Operating these multiphase buck converters near one of those zero output ripple current conditions leads to a much-reduced output capacitance requirement [30].

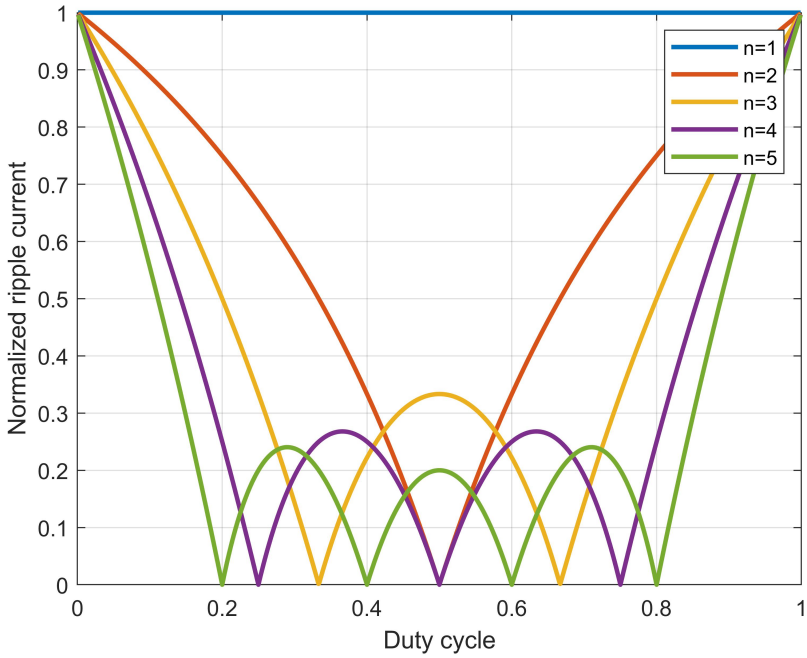

Figure 3.16: Normalized output ripple current as a function of duty cycle for a different number of phases

According to Figure 3.11, the efficiency reaches its highest for phases between 2 and 4. However, when 2,3, and 4 phase operations are compared, the ripple factor is lowest in the case of 4 phases, as shown in Figure 3.12, Figure 3.13, Figure 3.15, and Figure 3.16.Based on the above considerations of efficiency, input current ripple, output current ripple and output voltage ripple, the number of phases is selected as 4 for the optimal design of the non-isolated converter topology for this application. Figure 3.17 depicts the circuit diagram of a four-phase interleaved buck/boost converter to be designed.

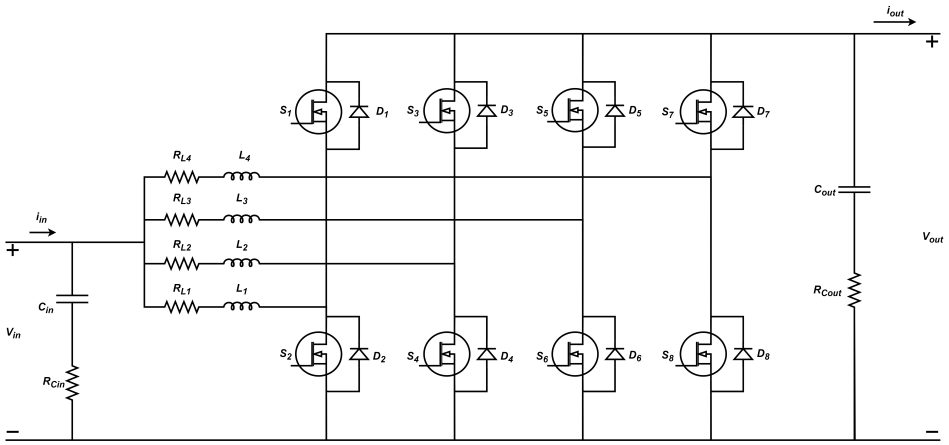

Figure 3.17: Circuit diagram of a four-phase interleaved buck/boost converter

3.2 Isolated converter topology

3.2.1 Three-Phase Dual Active Bridge Converter

The basic topology of a 3ph-DAB consists of three half-bridges at the input and output sides, which makes the power flow bi-directional[18]. The AC link of two three-phase active bridges is coupled via a high-frequency three-phase transformer as shown in figure 3.18. The phase inductance (L_{ph}) is the sum of the transformer's leakage inductance and the external inductance that serves as the energy transfer component.

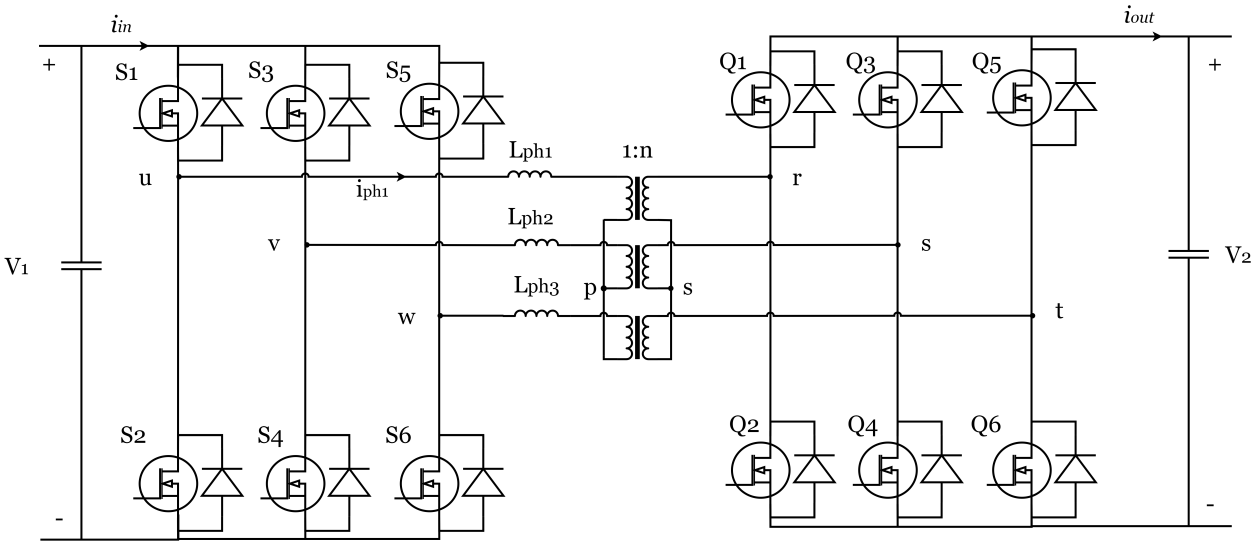

Figure 3.18: Circuit diagram of a 3ph-DAB

3.2.1.1 Operating Scheme

There are numerous advanced modulation schemes[33] for a 1ph-DAB that can improve the overall efficiency of the converter. In comparison, the advanced modulation techniques[34] for a 3ph-DAB become more complex due to the fixed(120°) phase shift between the phases. Hence, single-phase shift modulation is the most frequent modulation strategy at nominal operating conditions (where the voltage ratio between the primary and secondary sides is close to one).

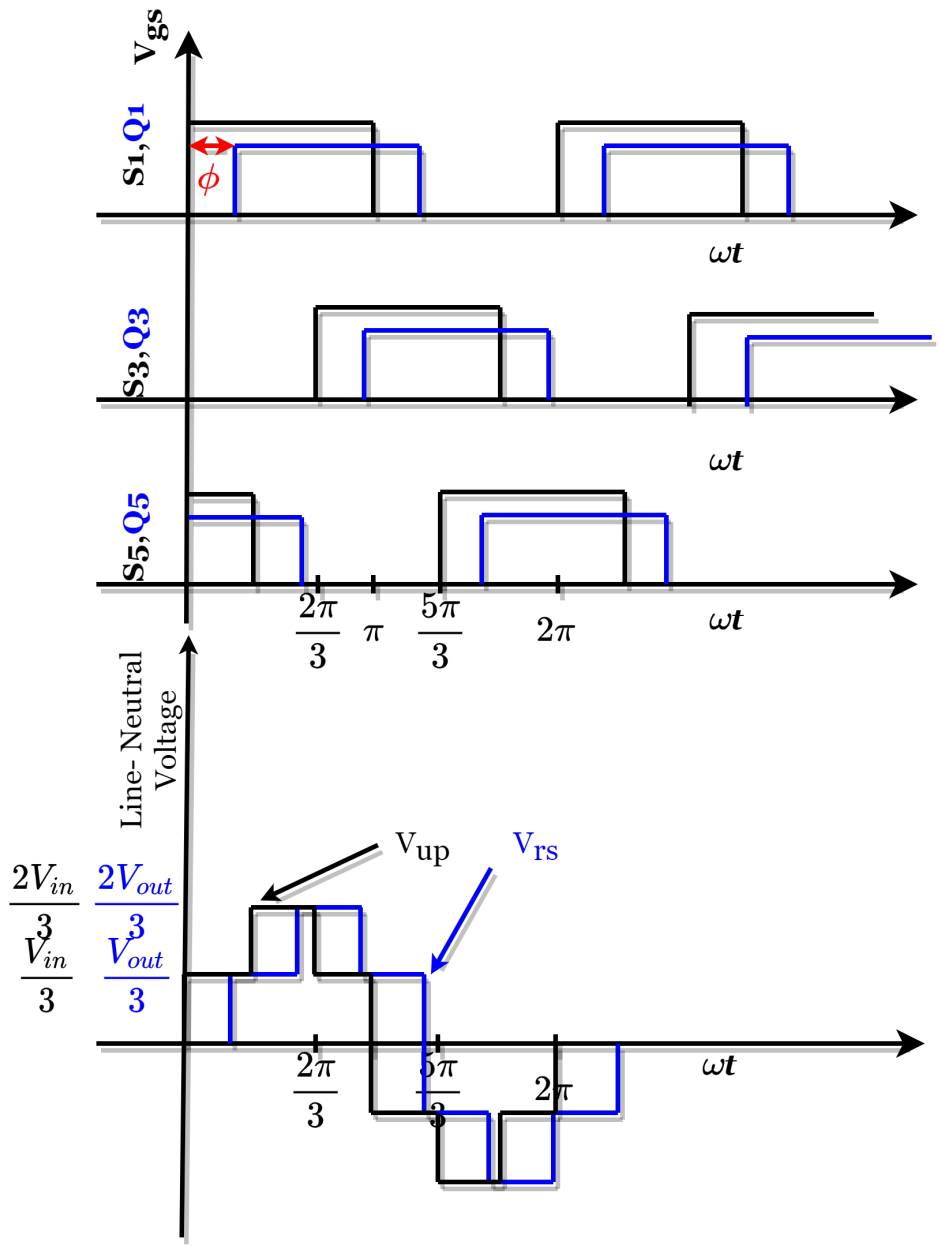

Figure 3.19: Gate source voltage (switching signals (Vgs)) for high voltage switches

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In single-phase shift modulation, complementary signals with a 50% duty cycle are used to operate the switches in one phase leg, and the three half-bridges of each side are operated with a phase shift of 120°. As shown in figure 3.19, the half-bridge S3/Q3 is delayed by 120°with respect to S1/Q1 and S5/Q5 lags by 240°. Hence a six-step line to neutral voltage waveforms are imposed on the transformer, and the waveforms of the other two phases are identical with a phase delay of 120°. The power flow is controlled by introducing a phase shift ϕ between primary and secondary side voltages. This is done by generating a voltage difference across the phase inductance. As shown in figure 3.20 the current shape differs for $\phi < \pi/3$

and $\phi > \pi/3$. For a positive value of ϕ, a positive power flow is achieved from the primary to secondary side; on the other hand, for reverse power flow, a negative value of ϕ is applied between the primary and secondary side voltages.

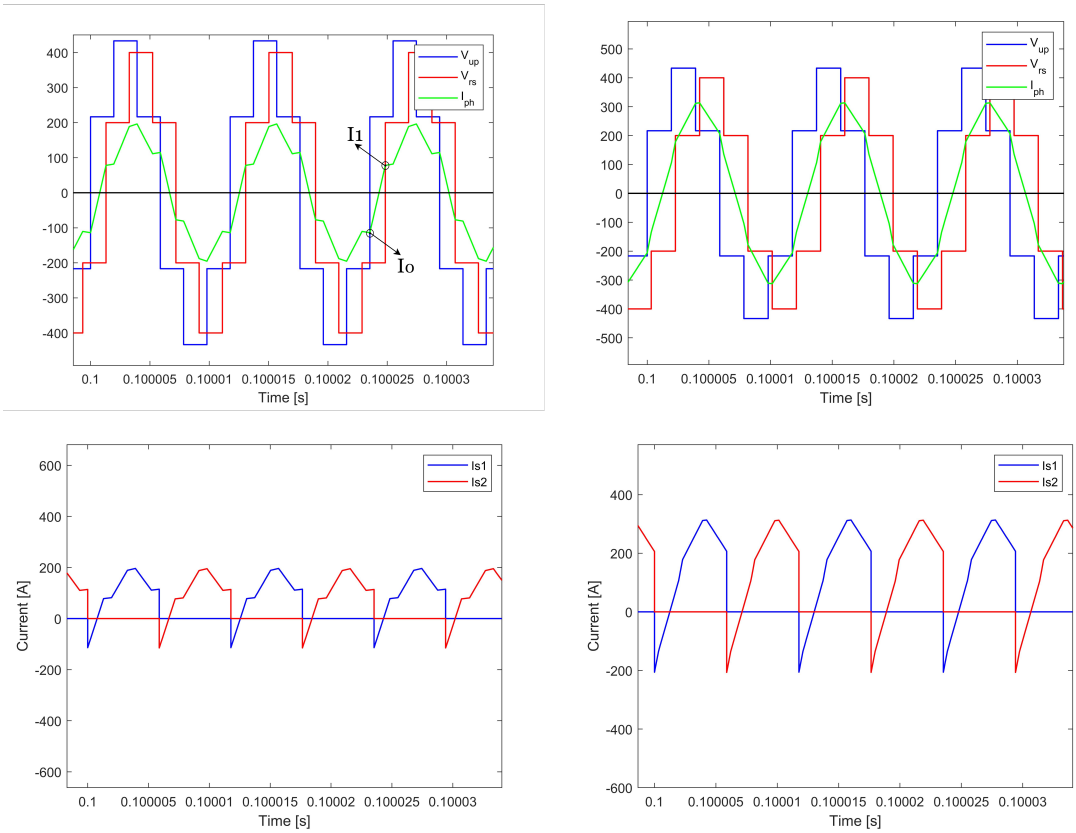

Figure 3.20: Operating waveforms of three-phase DAB converter (a) $\phi < \pi/3$ (b) $\phi > \pi/3$

The output power[18] is given as

$$P = \begin{cases} \frac{nV_1V_2}{12\pi^2 f_{sw} L_{ph}} \phi(4\pi - 3\phi), & 0 \leq \phi \leq \frac{\pi}{3} \\ \frac{nV_1V_2}{36\pi^2 f_{sw} L_{ph}} (18\phi^2 - 18\pi\phi + \pi^2), & \frac{\pi}{3} \leq \phi \leq \frac{2\pi}{3} \end{cases} \tag{3.27}$$

where V_1 and V_2 are the input voltage and the output voltage respectively, f_{sw} is the switching frequency and L_{ph} is the phase inductance. When the phase shift ϕ= 0, no active power is transferred. As the phase shift is increased, the power increases, and the maximum power is obtained at ϕ=$\pi/2$,

$$P_{max} = \frac{7nV_1V_2}{72 f_{sw} L_{ph}}. \tag{3.28}$$

Beyond this (ϕ>$\pi/2$), the transmitted power reduces, which is undesirable since it results in increased reactive power and RMS current. Hence this operating range is not considered. The RMS current of the phase inductance can be calculated[35] by

integrating the current square for one switching period,

$$I_{Lph_{rms}} = \begin{cases} \frac{\sqrt{-9nV_1V_2\phi^3+18\pi nV_1V_2\phi^2+\frac{5\pi^3(nV_1-V_2)^2}{3}}}{18f_{sw}L_{ph}\pi^{\frac{3}{2}}}, & 0 \leq \phi \leq \frac{\pi}{3} \\ \frac{\sqrt{nV_1V_2(-18\phi^3+27\pi\phi^2-3\pi^2\phi)+\pi^3(\frac{5n^2V_1^2}{3}+\frac{5V_2^2}{3}-3(nV_1V_2)}}{18f_{sw}L_{ph}\pi^{\frac{3}{2}}}, & \frac{\pi}{3} \leq \phi \leq \frac{2\pi}{3} \end{cases} \tag{3.29}$$

The required phase shift for a specific power transfer can be calculated[20] as,

$$\phi = \begin{cases} \frac{2\pi}{3}(1-\sqrt{1-\frac{9f_{sw}L_{ph}P}{nV_1V_2}}), & 0 \leq \mathrm{P} \leq P_1 \\ \frac{\pi}{6}(3-\sqrt{7-\frac{72f_{sw}L_{ph}P}{nV_1V_2}}), & P_1 \leq \mathrm{P} \leq P_{max} \end{cases} \tag{3.30}$$

where P_1=$nV_1V_2/(12f_{sw}L_{ph})$ which is achieved at ϕ=$\pi/3$ and P_{max}=$7nV_1V_2/(72f_{sw}L_{ph})$ which is achieved at ϕ=$\pi/2$.

3.2.1.2 Soft switching borders

In figure 3.20, the points I_0 and I_1 indicate the turn-on currents of the switches in the primary and the secondary sides, respectively. At this operating point, all the switches operate under zero voltage switching (ZVS) conditions. This means that the body diode conducts before the switch conducts the current, resulting in a zero voltage across the switch. However, during turn-off, hard switching occurs, which can be minimized by using a snubber circuit. The criteria for soft switching is that I_0 should be less than zero for primary switches, and I_1 should be greater than zero for secondary switches. The hard switching borders[20] can be expressed by,

$$P_{hard,prim} = \frac{V_1(nV_2^2 - V_1^2)}{9f_{sw}L_{ph}V_2}, \text{for } nV_2 < V_1 \tag{3.31}$$

$$P_{hard,sec} = \frac{nV_2(V_1^2 - nV_2^2)}{9f_{sw}L_{ph}V_1}, \text{ for } V_1 > nV_2 \tag{3.32}$$

At phase shift ϕ=$\pi/2$, the maximum phase inductance L_{max} for a specified power can be calculated using (3.28) as,

$$L_{max} = \frac{7nV_{1,min}V_{2,min}}{72f_{sw}P}. \tag{3.33}$$

where P is the maximum rated power and $V_{1,min}$ and $V_{2,min}$ are the minimum voltages.

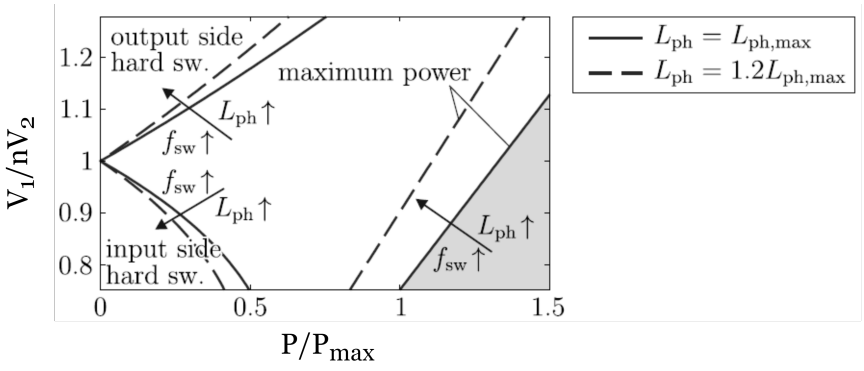

Figure 3.21: Influence of phase inductance and frequency in ZVS boundary

Increasing the inductance beyond L_{max} lowers the converter's maximum rated power, as shown in figure 3.21. From hard switching borders (3.31),(3.32), it can be seen that the phase inductance and the switching frequency influence the maximum power and soft switching area. As shown in figure 3.21, by increasing the value of phase inductance and frequency, the soft switching area can be increased. It is also important to note that providing a wide power range down to zero and a broad voltage range without hard switching is usually not practicable. The maximum inductance L_{max} produces the largest soft-switching ranges for a fixed frequency f_{sw}.

3.2.2 Planar transformer

In recent years, power electronic converters have been operating at high frequencies to boost efficiency and increase power density, resulting in smaller passive components and transformers. This trend has shown certain drawbacks in the use of traditional wire-wound transformers. Planar magnetics has grown increasingly popular for high-frequency applications because of its low profile, outstanding thermal characteristics, high repeatability, and simple production process[36]. As shown in figure 3.22, compared to the wire-wound transformer, the height of the planar magnetic is typically 25% to 50 % less, resulting in a low profile and better thermal characteristics[37].

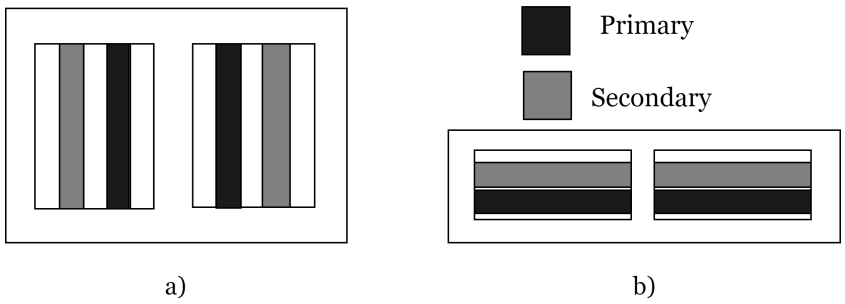

Figure 3.22: Core geometry of transformers: a) Conventional wire-wound transformer b) Planar transformer

The planar transformer can be standalone or integrated into a multi-layer board. The planar wound transformers are made by laminating planar copper windings and dielectrics into multi-layered printed circuit boards (PCBs) that are enclosed by a flat magnetically permeable core.

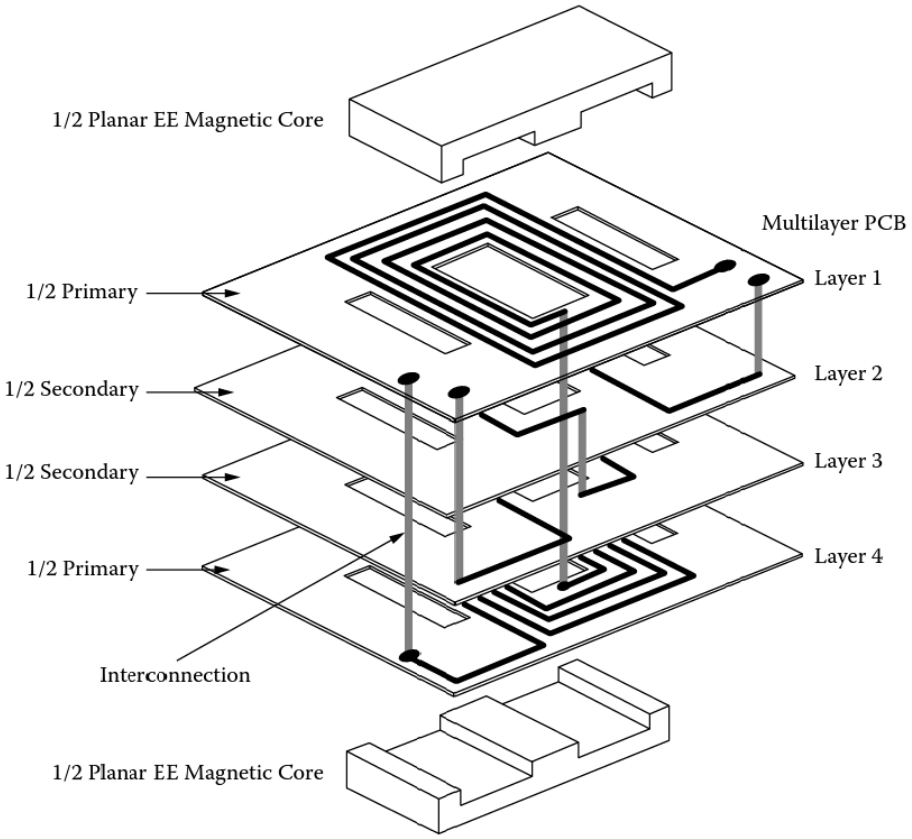

Figure 3.23: Typical planar transformer[38]

3.2.2.1 Magnetic core shapes

For a high-frequency transformer, the core shape and window configuration are crucial parameters to minimize the losses. Planar core transformers have a higher ratio of surface area to core volume than a wire wound transformers[37]. As a result, planar cores conduct heat more efficiently and have lower thermal resistance as more surface area is in contact with a heat sink. The core area product, which is determined by multiplying the available window area by the core cross-sectional area, is the best technique for initial estimation for selecting the proper core. The planar E core has the advantage of adjusting the leg length and window height without new tooling, allowing the final core to accommodate the planar conductor with minimal space wasted[39]. Thus, a planar transformer with E core is considered for the isolated converter.

3.2.2.2 Material Selection

Inductive power devices, such as inductors and transformers, commonly use soft magnetic materials as the core material. The ideal core material properties include a high saturation flux density, low core losses, a high permeability, and a high resistivity. Ferrites, iron powder, and soft iron are some potential core materials. Ferrite cores are commonly employed because of their high permeability and non-conductive property. The switching frequency, operational flux density, core loss,

and operating temperature are essential elements to be considered while designing a planar transformer[40].

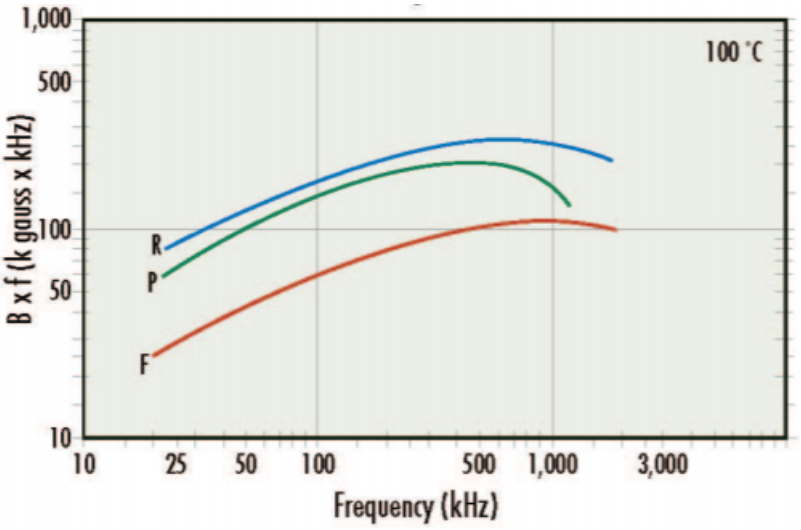

Figure 3.24: Performance curve of ferrite core materials at a power loss density of 300 mW/cm^3 [41]

One recent trend in the material selection process of a ferrite core has been to depict curves of a so-called performance factor (B x f) versus frequency at a particular core loss density[41]. The performance factor measures how much power a ferrite core can tolerate at a given amount of loss. Figure 3.24 shows the measure of material utility, i.e. compared to ferrite material 'P' & 'F', for the same core loss density of 300 (mW/cm^3), the ferrite material 'R' results in a reduced core volume (Area product) at 100 kHz. This is because the core volume (A_p) is inversely proportional to the performance factor. In figure 3.24 the term 'R', 'P' and 'F' refers to the ferrite material available for different core shapes provided by Magnetics (supplier of soft magnetic components)

3.3 Dual loop controller

The four-phase interleaved buck/boost converter's output voltage and inductor current are controlled by controlling the switching of MOSFETs to ensure a bidirectional power flow. A proportional-integral (PI) control method is widely used and preferred in control applications. PI controllers are highly desirable because of their easy implementation in industrial applications [42]. However, a single PI controller is not enough to ensure dynamic control of voltage and current. This problem can be eliminated by implementing a double-loop control in the non-isolated topology. PI-type controllers are chosen for both the voltage and current loops due to their adequate performance, simple and failure tolerant structure.

Several methods are used for tuning the PI control parameters, such as Ziegler Nichols, particle swarm optimization (PSO),genetic algorithm(GA) and simulated

annealing (SA). However, the state-space technique is preferred to analyze controllers for the non-isolated topology due to its simpler approach [43]. *Smallsignalanalysis* is a well-known linearization technique that employs state-space averaging and perturbation. The complexity of equations and transfer functions makes designing a controller for an IBC more difficult as the number of phases increases [43].

3.3.1 Voltage controller

The output voltage control of the interleaved buck/boost converter has two different topologies, namely current mode control and voltage mode control [42]. A voltage mode control topology is a single loop topology, whereas a current-mode control uses a dual-loop for controlling the output voltage. In our case, the current-mode control topology is chosen as it satisfies the industry-standard method for controlling the switching power [42]. As a result, the output voltage of the four-phase interleaved buck/boost converter is regulated using two cascaded control loops, which consists of an inner current control loop and outer voltage control loop.

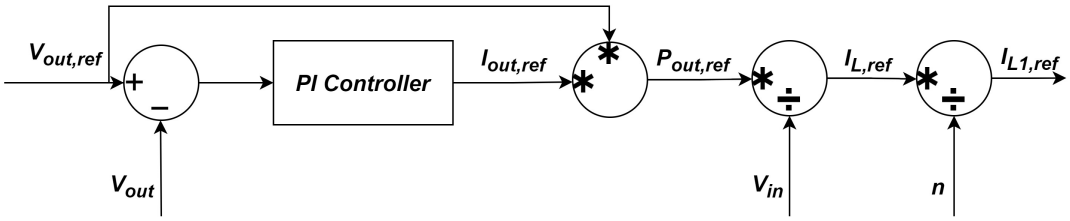

Figure 3.25: Control block diagram of a voltage controller in the boost mode operation

Figure 3.25 depicts the closed-loop control block diagram of the voltage controller implemented to control the converter's output voltage in boost mode during positive power flow. The voltage controller generates the net inductor current reference for the system. Therefore, according to the equal current sharing between interleaved phases, the phase current reference can be obtained.

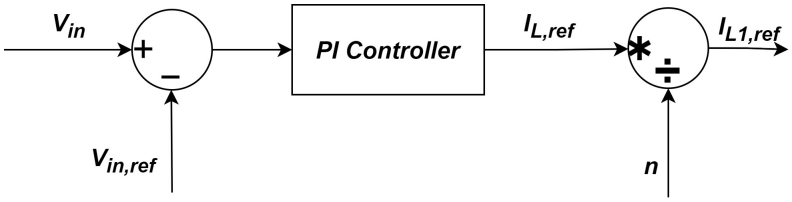

Figure 3.26: Control block diagram of a voltage controller in the buck mode operation

It can be seen that the instantaneous value of the output voltage of the converter is compared with the reference voltage and provided as the input to the PI controller. Therefore, the output voltage and the inductor current measured using the sensor are taken as input by the dual-loop controller. Figure 3.26 depicts the voltage control

scheme that is used for controlling the input voltage of the converter during the buck mode operation. The current flows in the reverse direction, and for obtaining a proper reference as the output, the input voltage is compared oppositely to that of the boost voltage controller.

3.3.2 Current controller

A PI controller is implemented as the current controller for controlling a single-phase inductor current. The current controller outputs the required duty ratio of the MOSFET connected to the particular phase so that the phase current matches the reference current. According to the interleaving technique, the duty ratio of MOSFETs in other phases is phase-shifted to achieve the required phase shift between each phase current. This helps control each phase current with the required phase shift using a single current controller instead of using an individual current controller for each phase.

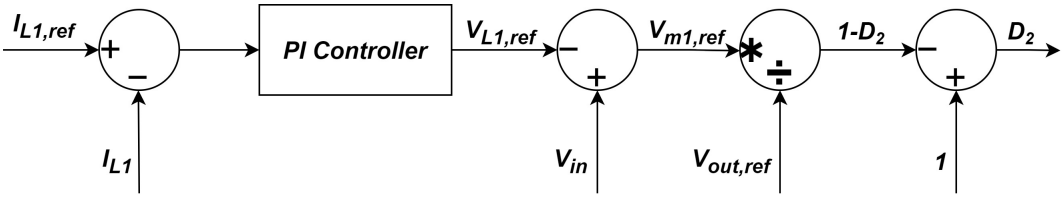

Figure 3.27: Control block diagram of a current controller in the boost mode operation

The generated duty ratio of each MOSFET from the current controller is given as an input to a pulse width modulation (PWM) generator. The PWM generator provides gate pulses to each MOSFET according to the required duty ratio for the switching purpose of each MOSFET. Thus, each MOSFET switching is controlled by the current controller to obtain the required phase current, which is dictated by the output voltage requirement of the converter.

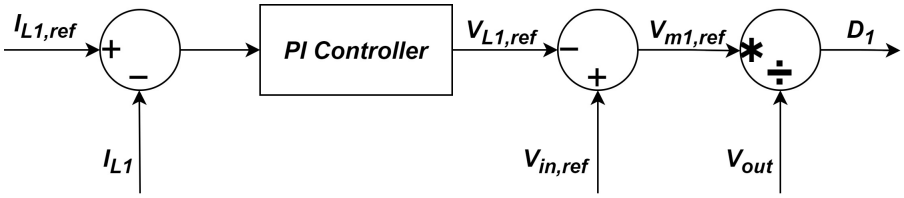

Figure 3.28: Control block diagram of a current controller in the buck mode operation

3.4 Power flow controller for three-phase DAB

The power flow can be controlled using the phase shift ϕ between the primary and secondary side voltages in three-phase DAB. A PI controller is implemented to control the power flow, which controls the phase shift based on the reference value.

The required phase shift generated by the PI controller is fed to the PWM generator, which gives the gating pulse to 12 switches.

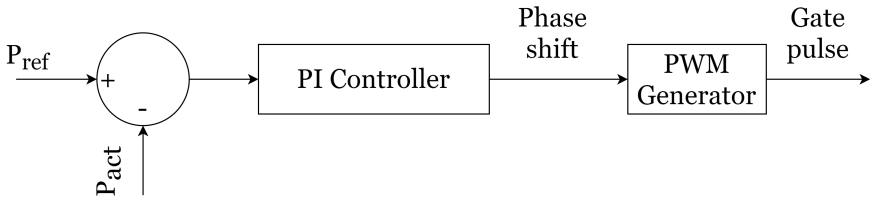

Figure 3.29: Control block diagram of a phase shift controller for three-phase DAB

This is a simple PI controller which controls only the power, but in reality, there will be an outer loop voltage control and an inner loop current control based on the phase shift ϕ.

3.5 Efficiency determination

3.5.1 Semiconductor loss

The loss components in a semiconductor switch are divided into switching loss and conduction loss. The switching loss occurs during the turning on and turning off of the switch, while the conduction loss occurs when the switch conducts.

3.5.1.1 Switching loss

To calculate the switching loss, the selected converters are modelled in the PLECS software by Plexim GmbH. PLECS uses a thermal description to calculate switching loss and conduction loss. The manufacturer provides the PLECS model of the power module on their website that can be imported into the PLECS thermal library. The thermal description of the power module provides the V-I characteristics, turn on and turn off switching energies based on the temperature. Figure 3.30 shows the switching energy lookup table for the CREE MOSFET. Based on the operating voltage and temperature, PLECS uses the lookup table to calculate the switching loss.

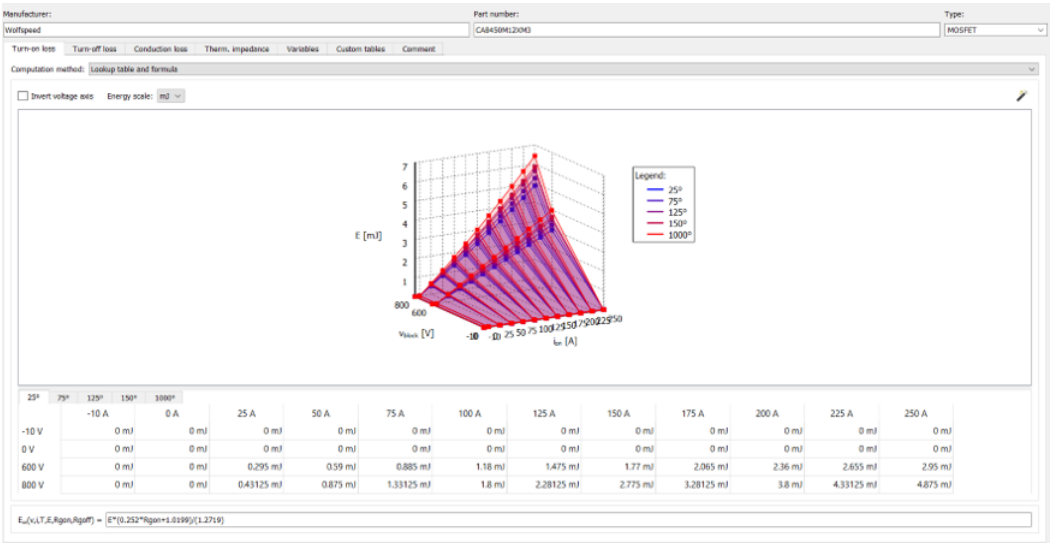

Figure 3.30: Switching energy look-up table for CREE MOSFET

3.5.1.2 Conduction loss

With the help of the V-I characteristics provided by the thermal description, $R_{ds,on}$ is calculated based on the operating voltage and temperature. With this setup, a temperature-dependent resistance is simulated, and a more accurate calculation of conduction loss is achieved.

3.5.2 Transformer loss

The sum of the copper loss and core loss contributes to overall transformer loss. The current flowing through the windings creates heat loss or I^2R loss due to winding resistance, and this loss is referred to as copper loss. The core loss is caused due to hysteresis loss and eddy current loss. During magnetization and demagnetization caused by alternating flux, the molecule's resistance in the core causes frictional loss, known as hysteresis loss. Eddy current loss is caused by circulating currents induced by an alternating magnetic field.

3.5.2.1 Core loss

There are three methods to model the core loss[44]: the hysteresis model, loss separation approach, and empirical method. The first two methods are based on parameters that are difficult to extract as they need extensive computation and measurement works. The empirical method calculates core loss using a simple calculation based on the manufacturer's data. The most frequently used approach to calculate core loss is to use the empirical Steinmetz equation (3.34) that relates power loss density with frequency and flux density using Steinmetz coefficients.

$$P_{core} = K(\hat{B})^{\alpha} {f_{sw}}^{\beta}. \tag{3.34}$$

where K, α, β are the Steinmetz coefficient which the manufacturer provides.

3.5.2.2 Copper loss

The transformer efficiency is significantly affected by the eddy current effect, which includes the skin effect and proximity effect. The time-varying magnetic field applied to the conductor induces a high frequency circulating current known as eddy current. The eddy current flows in such a way that the flux produced by it tends to oppose the primary alternating flux. As a result, at the centre of the conductor, the eddy current flows in the opposite direction of the primary current. In contrast, the eddy current flows in the same direction as the primary current near the surface. Hence, the current density is higher on the surface and decreases exponentially to the centre of the conductor. Thus, the current flows on the skin of the conductor, which depends on the level called the skin depth δ and expressed as,

$$\delta = \sqrt{\frac{1}{\pi f_{sw} \mu_o \sigma}}. \tag{3.35}$$

where $\mu_o = 4\pi * 10^{-7}$ (H/m) is the vacuum permeability, and $\sigma = 5.7 * 10^7$ (S/m) is the copper conductivity. In the same way, when two flat conductors carry current, the current in the first conductor induces a current in the adjacent conductor, which opposes the AC flux. As a result, the current density distribution in the conductor is uneven and depends on the direction of the current. This effect is known as the proximity effect. The proximity effect can be minimised by using a fully interleaved winding arrangement in the planar transformer[45]. Thus, in fully interleaved arrangements, the skin effect dominates the effective AC resistance, which can be minimised by the proper selection of copper thickness[45].

3.6 Battery model

Frequently modelled Li-ion battery models have a constant voltage source, which does not accurately reflect the I-V characteristics during the charging and discharging processes [46]. For optimising its performance, the I-V characteristics of the battery are taken into account.

An electrical model based on resistors connected to a controlled voltage source represents the Li-ion battery model. It has faster simulation speeds because it does not consider any time constants associated with the implementation of an RC-chain-based battery model. The battery model for both the input and output sides is a demo model of the R-only Li-ion battery model from the PLECS demo models library. This model uses information from the battery datasheet to represent the I-V characteristics exhibited by the battery pack. Three points on voltage as a function of the charge curve derives the R-only battery model. These are the voltage and charge at the end of the nominal zone, exponential zone, and when the battery gets fully charged.

4

Case setup

4.1 Interleaved buck/boost converter design

In the non-isolated converter topology, an interleaved buck/boost converter is selected as the most suitable converter for this application. In this section, the design of a 150 kW interleaved buck/boost converter is explained in detail.

4.1.1 Design specifications

A four-phase interleaved buck/boost converter is designed, simulated and evaluated based on the specifications listed in Table 4.1.

Table 4.1: Specifications of the four-phase interleaved buck/boost converter

V_{in}	600 V	Nominal input voltage
V_{out}	718.2 V	Output DC voltage
P_{out}	150 kW	Output power
f_{sw}	80 kHz	Switching frequency
ΔV_o	1 V	Output voltage ripple
ΔV_{in}	1 V	Input voltage ripple
ΔI_{ph}	10 %	Phase current ripple

The parameters in Table 4.1 are considered only for the initial design purpose of the converter. Input and output battery voltage range between 504 V - 765 V. The nominal voltage of the battery is 600 V which is considered as the input DC voltage for designing the converter. The battery attains its warning limit at 756 V, and 95% of that is taken as the output DC voltage for safety purposes.

4.1.2 Design equations

As previously mentioned, the interleaved buck/boost converter operates in the boost mode for a positive power flow and buck mode for a power flow in the reverse direction. The design of a multiphase converter is similar to that of a single phase converter. The relation between the multiphase converter's input current I_{in} and phase current I_{ph} is given by

$$I_{in} = nI_{ph} \tag{4.1}$$

Similarly, the frequency of input current can be represented by

$$f_{in} = nf_{sw} \tag{4.2}$$

There are three major components in the design of a multiphase interleaved buck-/boost converter, namely, the inductor for each phase, the output capacitor and the input capacitor. The design of the converter is derived under the following assumptions:

- Stray inductance and capacitance are negligible.
- MOSFETs are ideal.

According to the specifications of the converter, the on duty ratio D of each MOSFET is calculated as 0.16 using (3.1). For a four-phase operation with a duty ratio of 0.16, only one switch gets turned ON ($N_{on} = 1$) during the rising time of the input current. The relation between the rising time period d of the input current and the MOSFET on duty ratio d for this specific switching combination is given by

$$d = nD \tag{4.3}$$

According to the specifications, each phase inductor is designed to get a 10% ripple in the phase current considering single-phase operation. The value of each phase inductance is equal ($L_{ph} = L_1 = L_2 = L_3 = L_4$) and calculated as

$$L_{ph} = \frac{V_{in}DT}{\Delta I_{ph}} = 197.49\mu H \tag{4.4}$$

The value of the DC resistance (DCR) for each phase inductor are equal and chosen to be 1.2 mΩ from the datasheet of the inductor [47]. The net inductor current ripple at the input of the converter can be found by

$$\Delta I_{in} = \Delta I_{ph} \cdot \frac{n}{D(1-D)}(1 - D - \frac{m'}{n})(\frac{1+m'}{n} - (1-D)) = 2.55A \tag{4.5}$$

where m'=floor$((1 - D) \times n)$ [30]. Thus, the calculated phase inductance produces a net input current ripple of 1.02% of the rated input current of 250 A.

The next component to design is the output capacitor C_{out} function is to keep the output voltage constant with a ripple value of 1 V. The capacitor model consists of 2 quantities, namely the equivalent series resistance (ESR) and the equivalent series inductance (ESL). The effect of ESR dominates at higher frequencies when compared to ESL for the multiphase operation, hence the ESL can be neglected [48]. Thus the ESR and C_{out} needs to be designed for producing a combined output ripple value of 1 V. The ripple across the ESR is assumed to be 0.5 V, and the voltage ripple across the output capacitor is found from

$$\Delta V_o = \sqrt{\Delta V_C^2 + \Delta V_{ESR}^2} \tag{4.6}$$

where ΔV_o is the net output voltage ripple of 1 V, ΔV_C is the output voltage ripple due to the output capacitor, and ΔV_{ESR} is the output voltage ripple due to the ESR.

The value of ΔV_C is obtained as 0.87 V using (4.6), and for satisfying it, the value of the output capacitor C_{out} is determined to be 50.73 μF using (3.23). Similarly, the ESR of the output capacitor R_{Cout} is calculated using ΔV_{ESR} as

$$R_{Cout} = \frac{\Delta V_{ESR}}{I_{out}} = 2.4m\Omega \tag{4.7}$$

where I_{out} is the converter's average output current ($I_{out} = \frac{P_{out}}{V_{out}}$).

The third essential component is the input capacitor which can be calculated as [48]

$$C_{in} = \frac{\Delta I_{in}}{8nf_{sw}\Delta V_{in}} = 998.54nF \tag{4.8}$$

However, this capacitance value affects only the capacitive effect of the ripple voltage, and the ESR impacts the net ripple voltage. To limit the input ripple voltage to 1 V, the input capacitor's ESR should be less than

$$R_{Cin} < \frac{\Delta V_{in}}{\Delta I_{in}} \tag{4.9}$$

Therefore, 75% of the above value ($R_{Cin} = 0.29\ \Omega$) is chosen as the input capacitor's ESR value for limiting net input ripple voltage to 1 V. Figure 4.1 depicts the schematics of the designed converter simulated in PLECS.

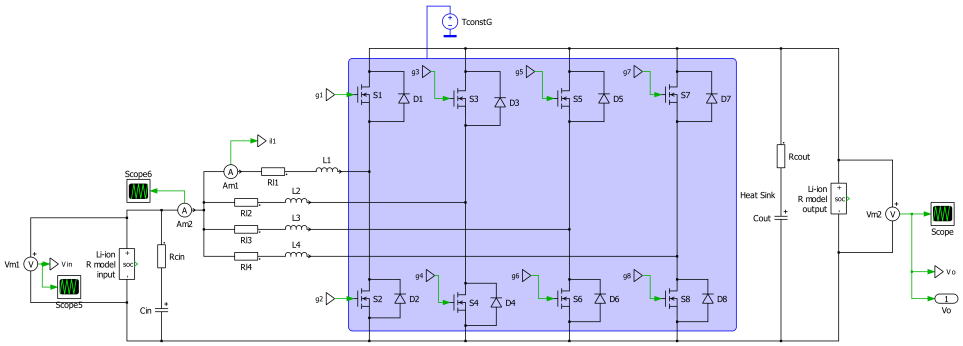

Figure 4.1: Four-phase interleaved buck/boost converter circuit in PLECS

4.2 Three-Phase Dual Active Bridge converter design

In this section, the design procedure of a three-phase dual active bridge is explained.Table 4.2 shows the design specifications for the converter.

Table 4.2: Specifications of the three-phase DAB converter

$V_{1,range}$	530 V - 720 V	Input voltage
V_1	600 V	Nominal input voltage
V_2	718.2 V	Output DC voltage
P_{out}	150 kW	Output power
$P_{rated,max}$	155 kW	Maximum rated power
f_{sw}	80 kHz	Switching frequency
ΔV_o	1 V	Output voltage ripple

The key parameters that influence the characteristics of a three-phase DAB are the phase inductances (L_{ph}) and the switching frequency f_{sw}). As seen in (3.31),(3.32), and (3.28) these parameters impact the soft switching boundaries and the maximum power transmission. With 530 V as the minimum primary voltage and 720 V as the secondary voltage, the maximum phase inductance that can generate a maximum rated power of 155kW is calculated using (3.33).

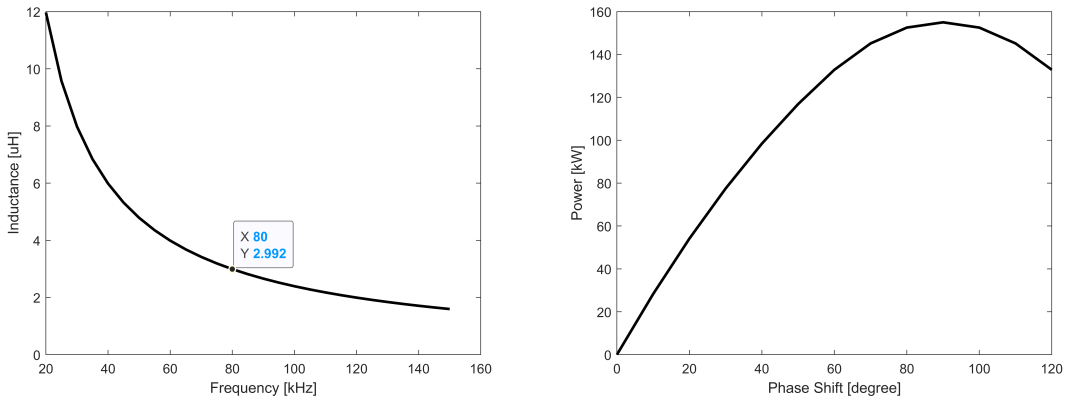

Figure 4.2: (a) Maximum inductance (L_{max}) for various frequencies. (b) Maximum power for different phase shift

Figure 4.2a shows the maximum inductance for various frequencies that results in a power flow of 155kW. With a phase inductance of 3 μH and 80 kHz as the frequency, the maximum power transfer is shown in figure 4.2b for different phase shifts. For the initial design, an arbitrary frequency of 80 kHz is chosen as the operating frequency, resulting in a maximum phase inductance of 3 μH. Although increasing the frequency has the advantage of reducing the size of passive components, it is severely limited by the transformer design.

4.3 High frequency planar transformer design

Based on the converter specification, the design requirements for the planar transformer are given in table 4.3

Table 4.3: Specifications of the planar transformer

V_1	530 V - 720 V	Input voltage
V_1	600 V	Nominal input voltage
V_2	718.2 V	Output DC voltage
P_{out}	150 kW	Output power
n	1	Turns ratio
f_{sw}	80 kHz	Switching frequency
L_{ph}	3 μH	Leakage inductance
T	25°C	Ambient temperature

In many ways, the design methodology of the planar transformer is similar to the conventional transformer design, i.e. in the worst-case scenario, the applied volt-seconds must not saturate the ferromagnetic material[49]. However, there is a slight variation in the copper design and the window utilization factor, which is usually much lower compared to traditional wire-wound transformers[38]. The design procedure is based on a typical transformer design, in which the area product is determined based on the power handling capability, frequency, and operating flux density such that the applied volt-second does not saturate the core. Figure 4.3 shows the design flow chart for the planar transformer.

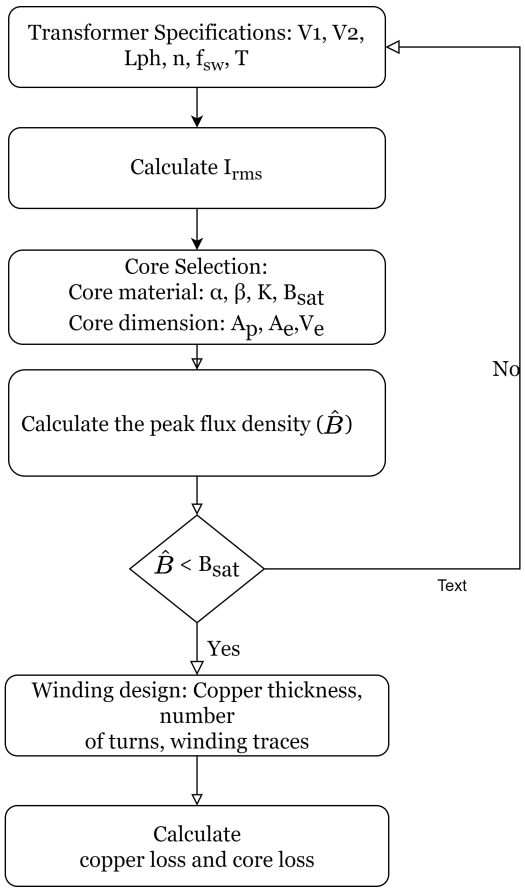

Figure 4.3: Design flowchart for a planar transformer

Based on the specifications of the transformer, the RMS current flowing in the phase inductance is calculated to be 192 A, using (3.29). Compared to a three-phase transformer, three single-phase transformers are simpler to build, and they can attain equal stray parameters, which helps balance the current among the three phases. Hence the thesis focuses on the design of a three single-phase transformer connected in a Y-Y configuration.

4.3.1 Core selection

The number of planar cores available on the market that can handle this amount of power is limited. For the initial core shape selection, the planar E core (E 102) from Magnetics[50] is selected as it has the largest area product amongst other planar cores. From figure 3.24, at 80 kHz, the ferrite core material 'R' has the highest performance factor, and hence it is chosen. Both core shape and core material need to be verified in the later stage.

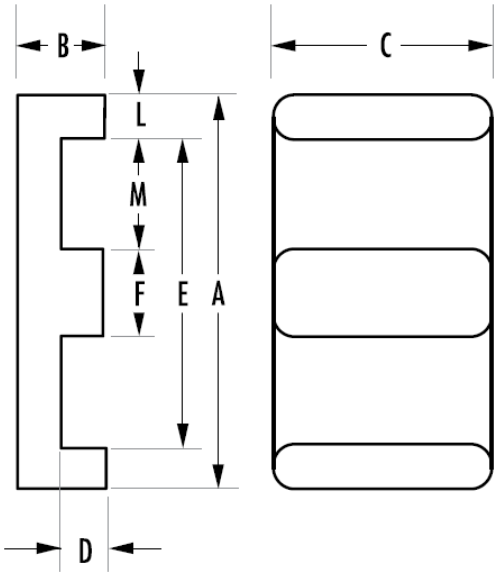

Figure 4.4: Core dimension of the planar E 102[50]

Figure 4.4 shows the geometric dimensions of the selected core and table (4.4) & (4.5) show the Steinmetz coefficient for material R and core parameters.

Table 4.4: Planar core geometry and Steinmetz coefficients

A	B	C	D	E	F	L	M
102 mm	20.3 mm	37.5 mm	13.3 mm	86 mm	14 mm	8 mm	36 mm

K	3.53
α	1.42
β	2.88

Table 4.5: Planar core dimensions

$A_e(cm^2)$	$A_w(cm^2)$	$A_p(cm^4)$	$V_e(cm^3)$	B_{sat}(T) @125°C
5.4	9.58	51.71	79.8	0.325

The power handling capability and the area product of the transformer core is given by the relation [38] and the criteria to check if the transformer can handle the applied power is given by the relation (4.11),

$$Required, A_p = \frac{P_t(10^4)}{K_f K_u \hat{B} J f_{sw}} \tag{4.10}$$

$$Required, A_p \leq A_w * A_e. \tag{4.11}$$

where A_e is the core-cross sectional area (cm^2), A_w is the window area (cm^2), P_t is the apparent power (VA), K_f is the waveform coefficient, K_u is the window utilization factor, $\hat{B}$ is the maximum magnetic flux density, J is the current density (A/cm^2), and f_{sw} is the operating frequency. After calculating the required area product using (4.10), it is verified with (4.11) using the values in table 4.5 to ensure that the selected core can handle the applied power without saturating, i.e. the calculated value needs to be less than the area product in table 4.5. For three-phase DAB, the apparent power rating of the transformer can be calculated as,

$$KVA_{rating} = \frac{3}{2}[V_{up,rms}.I_{P,rms} + V_{rs,rms}.I_{S,rms}] \tag{4.12}$$

where $I_{P,rms}$ & $I_{P,rms}$ are the primary and secondary RMS currents respectively. $V_{up,rms}$ & $V_{rs,rms}$ are the six-step line to neutral RMS voltages of the primary and secondary voltages, respectively

$$V_{up,rms} = \frac{\sqrt{2}V_1}{3} = 282.8V \tag{4.13}$$

$$V_{rs,rms} = \frac{\sqrt{2}V_2}{3} = 339.4V \tag{4.14}$$

Substituting (4.13) and (4.14) in (4.12) gives,

$$kVA_{rating} = \frac{(nV_1 + V_2)I_{rms}}{\sqrt{2}} = 179.21kVA \tag{4.15}$$

The calculated apparent power is the total power rating for three transformers, and thus, the rating of one transformer is 59.74 kVA. The primary winding and secondary winding handles the input power (P_{in}) and output power (P_{out}), respectively. As a result, the transformer must be designed to handle both input and output power. Thus, the apparent power (P_t) is calculated as,

$$P_t = P_{in} + P_{out} \tag{4.16}$$

$$P_{in} = \frac{P_{out}}{\eta} \tag{4.17}$$

where $P_{out} = V_{rs,rms}.I_{rms}$ and with an assumption of 97% as efficiency, the apparent power P_t is calculated as 132.98 kVA.

In (4.10), the window utilization factor (K_u) is the ratio of the total copper area to the window area. Compared to the wire-wound transformer, the window utilization factor for the planar transformer is significantly lower. The window utilization factor (K_u) for a typical planar transformer[35] is 0.21 , which will be used for the preliminary design. One of the key advantages of planar transformers is that their cores have a larger surface-to-volume ratio than conventional magnetic cores, allowing for faster heat dissipation. The copper loss and the temperature rise are controlled by the current density, and since the heat dissipation is better in planar transformer, it can accommodate a higher current density[38]. The current density is initialized with 12 A/mm^2. The next step is to calculate the waveform coefficient (K_f). Faraday's law of induction relates to the change in magnetic flux and induced voltage.

$$v = n\frac{d\phi}{dt} \tag{4.18}$$

$$\phi = \frac{1}{n}\int_0^T v(t)dt \tag{4.19}$$

By integrating the applied voltage over one half period, the peak flux ϕ can be calculated as

$$\phi = \frac{1}{2}.\left[\frac{1}{n6f_{sw}}\left(2\left(\frac{V_1}{3}\right) + \left(\frac{2V_1}{3}\right)\right)\right] \tag{4.20}$$

$$\phi = \frac{V_1}{9f_{sw}n}. \tag{4.21}$$

Rearranging and substituting (4.21) in (4.13) gives

$$V_{rms} = 3\sqrt{2}f_{sw}n\phi. \tag{4.22}$$

Thus, the waveform coefficient is $3\sqrt{2}$. In (4.10), to calculate the maximum flux density, half of the total transformer loss is assumed to be core loss[51]. This means that the temperature rise induced by core losses (P_{core}) should not be more than half of the maximum allowable temperature rise (T_{max})

$$P_{core}R_{th} \leq \frac{\Delta T_{max}}{2} \tag{4.23}$$

where R_{th} is the thermal resistance of the transformer and can be calculated[52] by,

$$R_{th} = 53(V_e)^{-0.54} = 4.98K/W \tag{4.24}$$

With the ambient temperature of the converter as 25°C, the core loss density can be estimated using (4.23) under the assumption that the maximum allowable temperature rise is 110°C. Using Steinmetz coefficient in table 4.4 and core loss density, the maximum flux density can be calculated by,

$$\hat{B} = \left(\frac{P_{core}}{K{f_{sw}}^{\alpha}}\right)^{\frac{1}{\beta}} = 0.16T \tag{4.25}$$

The calculated flux density is lower than the saturation flux density (0.325 T) of the selected core. By substituting the apparent power, waveform coefficient, window utilization factor, current density, frequency, and maximum flux density into (4.10), the calculated value is 105.3 cm^4 which is far greater than the area product of the selected core ($A_P = 51.71cm^4$). This indicates that the selected core is incapable of handling the applied power. Hence to maximize the power handling capability, two planar E cores are stacked together to increase the core area as shown in figure 4.5.

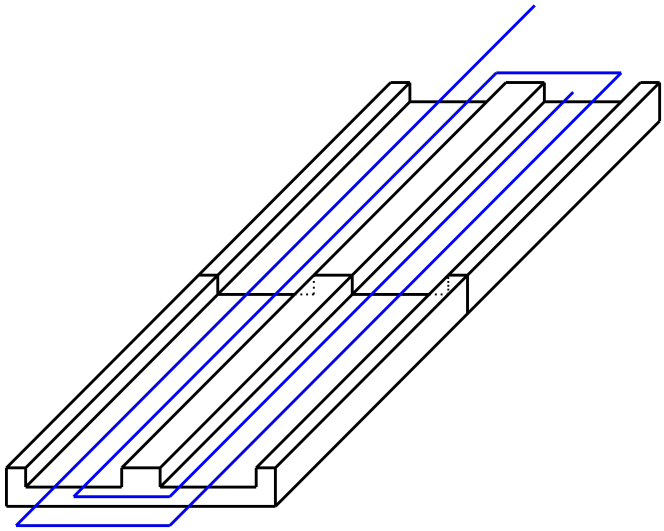

Figure 4.5: Cores in series to increase power handling capability

The new area product for the stacked core is then 103.42 cm^4 as the core area is increased to 10.8 cm^2. Even after modifying of the core, it is incapable of handling the supplied power. By optimising the operating frequency and the phase inductance, this mismatch can be eliminated.

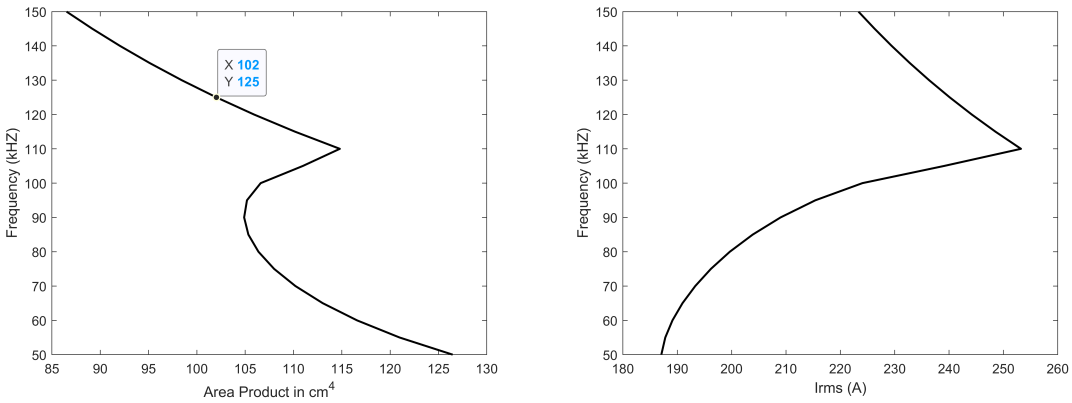

Figure 4.6: (a) Area product (A_p) for various frequencies. (b) RMS current (I_{rms}) for different frequencies

With a phase inductance of 3 μH, the figure 4.6a shows the required area product for different frequencies using (4.10) . As shown in the figure, the converter must

operate at a frequency of 125 kHz for the chosen core to handle the needed power. On the other hand, the corresponding RMS current at that frequency is high, leading to higher copper losses.

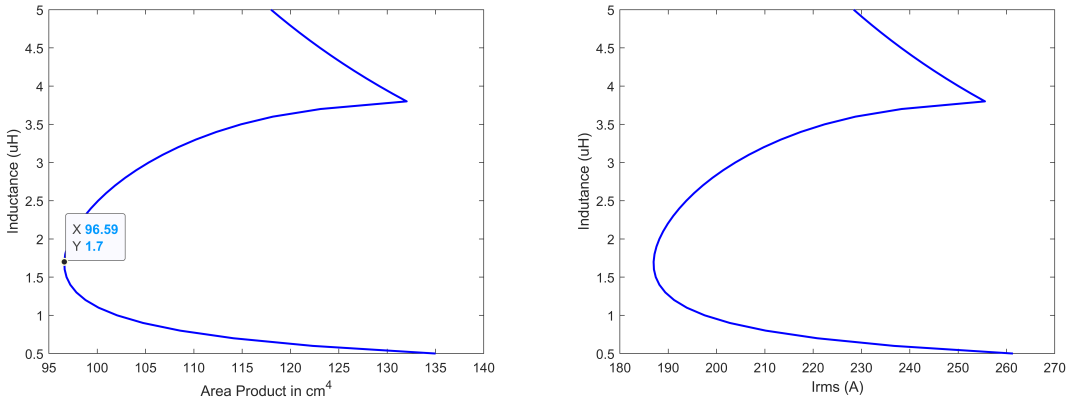

Figure 4.7: (a) Area Product (A_p) for various inductance (b) RMS current (I_{rms}) for different inductance

Figure 4.7a shows the required area product for different inductances at a frequency of 85 kHz. Below 85 kHz, the core can never deliver the power of 150 kW without surpassing the maximum allowable temperature. The figure shows that the minimum inductance that leads to the desired area product (103.42 cm^4) and the lowest RMS current is 1.7 μH. The soft switching borders are considerably affected by lowering the inductance; hence a trade-off is made. As a result, the phase inductance is chosen to be 2.4 μH, which is the maximum inductance that provides the needed area product. Hence the selected planar E core stacked in series can handle the power of 150 kW with the phase inductance of 2.4 μH and 85 kHz as the operating frequency.

4.3.2 Printed circuit board winding design

Using Faraday's law, the primary turns can be calculated as,

$$N_p = \frac{V_p * 10^4}{A_e \hat{B} K_f f_{sw}} = 10 \tag{4.26}$$

As the turns ratio is one, the secondary turns (N_s) are 10. To achieve the lowest AC resistance, the copper thickness (t) should be less than or equal to skin depth δ [45]. For a frequency of 85kHz, using(3.35), the skin depth calculated is 228.65μm. Hence, a two-layer PCB with a copper thickness of 6-oz (209μm), which is less than the skin depth, is selected as the production process is simple. To accommodate the number of turns, the winding is made up of two layers in series, each with five turns, i.e. in figure 4.8, the top and bottom layer of the first two-layer PC board is connected in series which represents the primary winding. The figure 4.8 shows the arrangement of 2 layer PC board where P1 & S1 are the primary and secondary winding. Table

4.6 shows the specification of the PCB selected. A standard thickness is selected for PCB substrate, and the total thickness of the PC board is 1.02 mm.

Table 4.6: Specification of PCB windings

Copper thickness (t)	0.210 mm
PCB substrate (FR4) thickness	0.3 mm
Insulation between PCBs	0.3 mm
Total thickness	1.02 mm

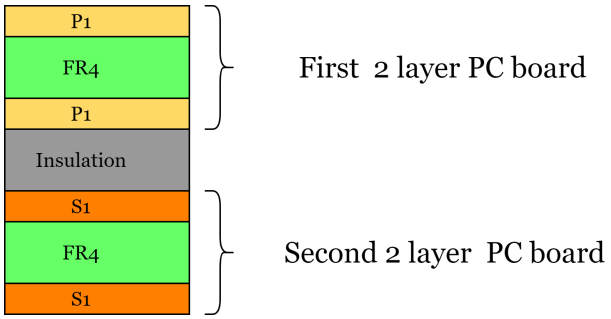

Figure 4.8: Structure of two layer printed circuit board

Based on the total thickness of the PC board and the available window length 'D' in figure 4.4, the number of PC boards that can be accommodated is calculated as 26. The calculation of trace width is one of the key parameters in PCB design since it determines the rise in temperature based on the current it carries. The total RMS current is split by 13 PC boards for primary windings and the remaining for secondary windings. Hence the RMS current in each layer is 15 A. The minimum trace width for a 10°C temperature rise and the turn to turn spacing is calculated[53] and shown in table 4.7

Table 4.7: Specification of trace width and turn to turn spacing

RMS Current for 1 layer	15 A
Minimum trace width	5.5 mm
Minimum spacing (S)	1.25 mm
Number of turns per layer (N_l)	5

The available trace width w_t can be estimated[51] from the window width 'M' of the chosen core by,

$$w_t = \frac{b_w - (N_l + 1).S}{N_l} = 5.7mm. \tag{4.27}$$

where b_w is the available window width, i.e. 'M' in figure 4.4 and S is the minimum turn to turn spacing and N_l is the number of turns per layer. Since the available trace width is larger than the minimum trace width, the windings can handle the current supplied without increasing the temperature. As the number of turns in

each layer and dimensions of PCB are estimated, it is easy to calculate the DC resistance for both primary and secondary windings. The mean length per turn must be calculated in order to compute the DC resistance of the windings. For a rectangular winding, as shown in figure 4.9, the mean length per turn can be calculated[38] as,

$$MLT = 2B + 2C + 2.82A = 280mm. \tag{4.28}$$

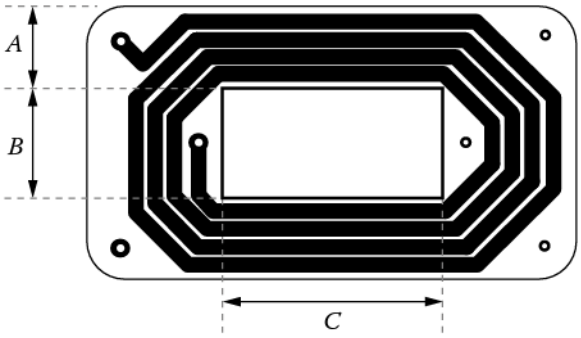

Figure 4.9: Mean Length per turn

As the number of turns in each layer and dimensions of PCB are estimated, it is easy to calculate the DC resistance for both primary and secondary windings,

$$R_p = \rho \frac{N_p MLT}{w_t.t} = 42.8m\Omega \tag{4.29}$$

$$R_s = \rho \frac{N_s MLT}{w_t.t} = 42.8m\Omega \tag{4.30}$$

where ρ is the resistivity of copper, t is the copper thickness in mm, R_p & R_s are the DC resistance for one PC board of primary winding and secondary winding, respectively. The total DC resistance of primary and secondary windings is 3.29mΩ. There are various winding arrangements possible like non-interleaved, partially interleaved and fully interleaved. To reduce the copper loss, the fully interleaved winding is best suited. Figure 4.10 shows the schematic diagram of the designed three-phase DAB in PLECS.

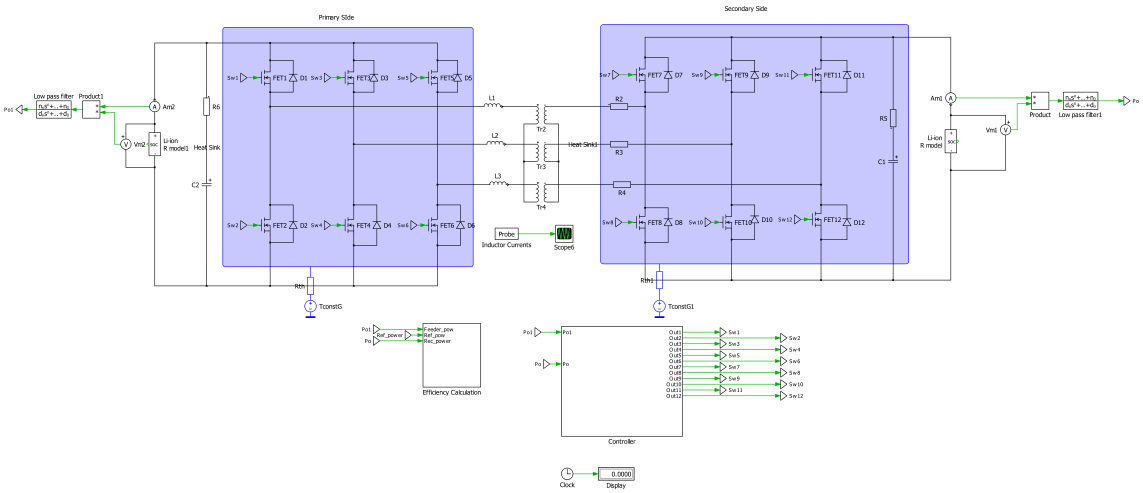

Figure 4.10: Schematic diagram of a three-phase DAB in PLECS

4.4 Controller design

A double loop controller controls the output voltage and the phase current of the 4-phase interleaved buck/boost converter. The inner loop controls the inductor current, while the outer loop generates the reference current. So, the inner loop response of these controllers is designed to be faster than the outer loop response. The transfer function of both the inner and the outer loops are written in this section based on a small-signal analysis of the converter. PI controllers are implemented based on the analysis. Calculations of the PI parameters are discussed in Appendix A. According to the calculation, the design of the voltage controller is slightly different from that of the current controller.

The transfer functions are obtained by considering the parasitics of the inductor, capacitor and the MOSFET. As a result, an accurate mathematical model that closely resembles the practical case of the converter is generated. This feature helps in designing a robust controller. Furthermore, the inductor current and the output voltage are used as state variables for the *smallsignalanalysis*.

4.4.1 Current controller

The converter operates in discharge mode (boost operation) and charge mode (buck operation), considering the source battery side. The transfer function of the proposed bidirectional converter is different for both modes of operation. Therefore, different controllers need to be designed [54]. The variation of the inductor current in the k^{th} leg with duty ratio is analysed. For a 4-phase IBC, the final equations after $small - signalanalysis$ are obtained by substituting $n = 4$.

4.4.1.1 Boost current controller

The transfer function between the inductor current in the k^{th} leg and the duty ratio is obtained as

$$\begin{aligned}\frac{\hat{i_{L_k}}(s)}{\hat{D}_k(s)} &= \frac{\frac{R}{L_k C_{out}(R+R_{Cout})}\left(\begin{array}{l} sC_{out}(V_{out}+R_{Cout}I_{L_k}) \\ \quad + \frac{1}{R+R_{Cout}}\left(V_{out}+R_{Cout}I_{L_k}+4(1-D)RI_{L_k}\right)\end{array}\right)}{\begin{array}{r} s^2 + s\left(\frac{(1-D)RR_{Cout}}{L_k(R+R_{Cout})} + \frac{R_{L_k}+R_{s(on)}}{L_k} + \frac{1}{C_{out}(R+R_{Cout})}\right) \\ + \frac{(1-D)R}{L_k C_{out}(R+R_{Cout})}\left(\frac{R_{Cout}}{R+R_{Cout}} + \frac{R_{L_k}+R_{s(on)}}{(1-D)R} + \frac{4(1-D)R}{R+R_{Cout}}\right)\end{array}} \\ &= \frac{3.635\cdot 10^6 s + 4.164\cdot 10^{10}}{s^2 + 5826s + 2.788\cdot 10^8}\end{aligned} \tag{4.31}$$

where L_k is the inductance of the k^{th} leg, I_{L_k} is the average inductor current flowing through the k^{th} leg, and R is the load resistance which can be obtained from the output power ($R = V_{out}^2/P_{out}$). The above transfer function is calculated based on the design values from the previous section and the specifications of the converter mentioned in Table 4.1. Similarly, from [43], the transfer function of the output voltage and the duty ratio is obtained as

$$\frac{\hat{V_{out}}(s)}{\hat{D}_k(s)} = \frac{-0.5996s^2 - 4.899\cdot 10^6 s + 2.388\cdot 10^{11}}{s^2 + 5826s + 2.788\cdot 10^8} \tag{4.32}$$

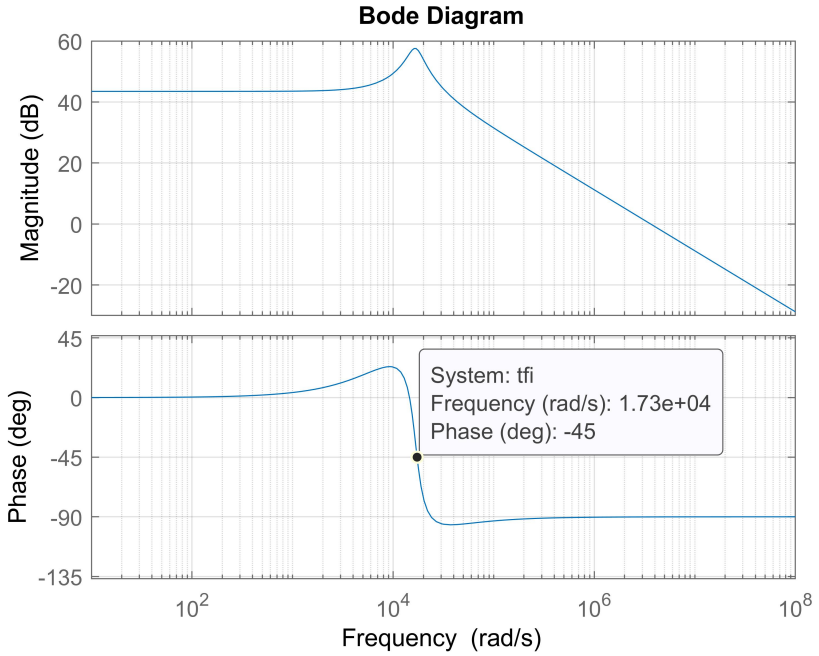

Figure 4.11: Frequency response of the inductor current to duty ratio transfer function in the discharge mode

The cutoff frequency is required for designing the PI controller. From the bode plot shown in Figure 4.11, we get the cutoff frequency as $\alpha_{cfi} = 1.73{\times}10^4$ rad/sec. The gain of the proportional and the integrator parts of the inner current controller are obtained as $k_{pfi} = 3.42$ and $k_{ifi} = 59207.61$. Active damping is designed for the current controller for reducing the oscillation and provide improved control performance. The current controller outputs desired duty ratio of each MOSFET, so the output of the current controller is limited between 0 and 1. Hence, an anti-windup scheme is necessary for preventing the integrator part from getting overcharged. According to the design, calculated values of the active damping term R_{afi} and the antiwindup term k_{awfi} are 3.4 and 0.29, respectively.

Based on the design, the current controller for the discharge mode is implemented in the PLECS software and the schematics of it is shown in Figure 4.12.

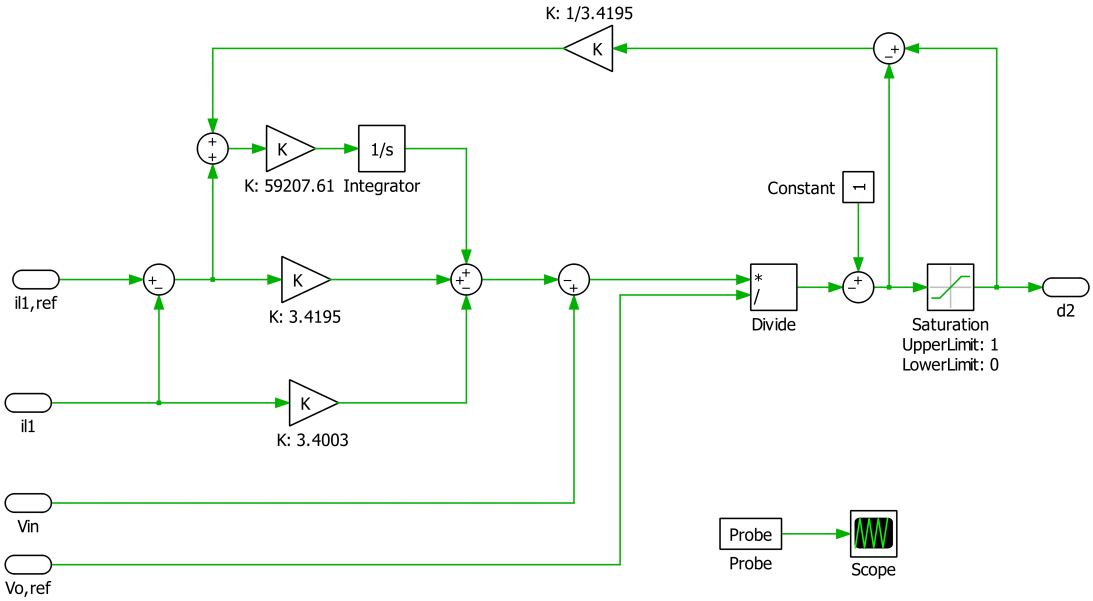

Figure 4.12: Boost current controller circuit in PLECS

4.4.1.2 Buck current controller

The *smallsignalanalysis* for the n-phase interleaved buck converter [55] provides the required transfer function for the buck controller case. The transfer functions from the output of the dual lop controller to the inductor current and the output voltage are obtained as

$$\begin{aligned}\frac{\hat{i_{L_k}}(s)}{\hat{D}_k(s)} &= \frac{V_{out(R_{in}C_{in}s+1)}}{R_{in}L_kC_{in}s^2 + (R_{in}R_{L_k}C_{in} + L_k)s + R_{L_k} + n_{R_{in}}} \\ &= \frac{3.637 \cdot 10^6 s + 1.517 \cdot 10^{12}}{s^2 + 4.173 \cdot 10^5 s + 2.029 \cdot 10^{10}}\end{aligned} \tag{4.33}$$

$$\begin{aligned}\frac{\hat{V_{in}}(s)}{\hat{D}_k(s)} &= \frac{nR_{in}V_{out}}{R_{in}L_kC_{in}s^2 + (R_{in}R_{L_k}C_{in} + L_k)s + R_{L_k} + n_{R_{in}}} \\ &= \frac{1.457 \cdot 10^{13}}{s^2 + 4.173 \cdot 10^5 s + 2.029 \cdot 10^{10}}\end{aligned} \tag{4.34}$$

where $R_{in} = V_{in}^2/P_{out}$.

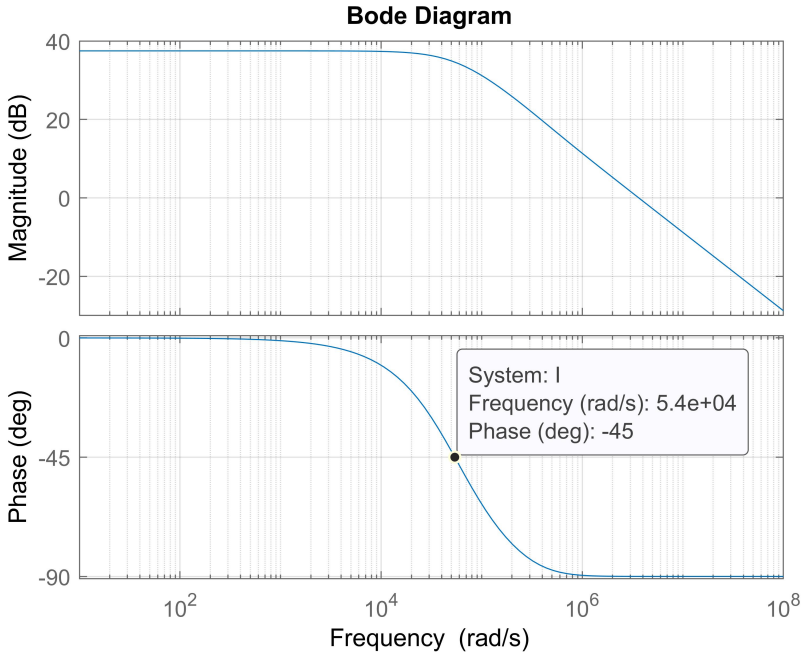

Figure 4.13: Frequency response of the inductor current to duty ratio transfer function in the charge mode

The cutoff frequency is obtained as $\alpha_{cbi} = 5.4{\times}10^4$ rad/sec from Figure 4.13. Based on the design, the calculated values of the proportional gain, integrator gain and the active damping terms are $k_{pbi} = 10.66$, $k_{ibi} = 143928.09$ and $R_{abi} = 10.38$, respectively. The simulated buck current controller model is shown in Figure 4.14.

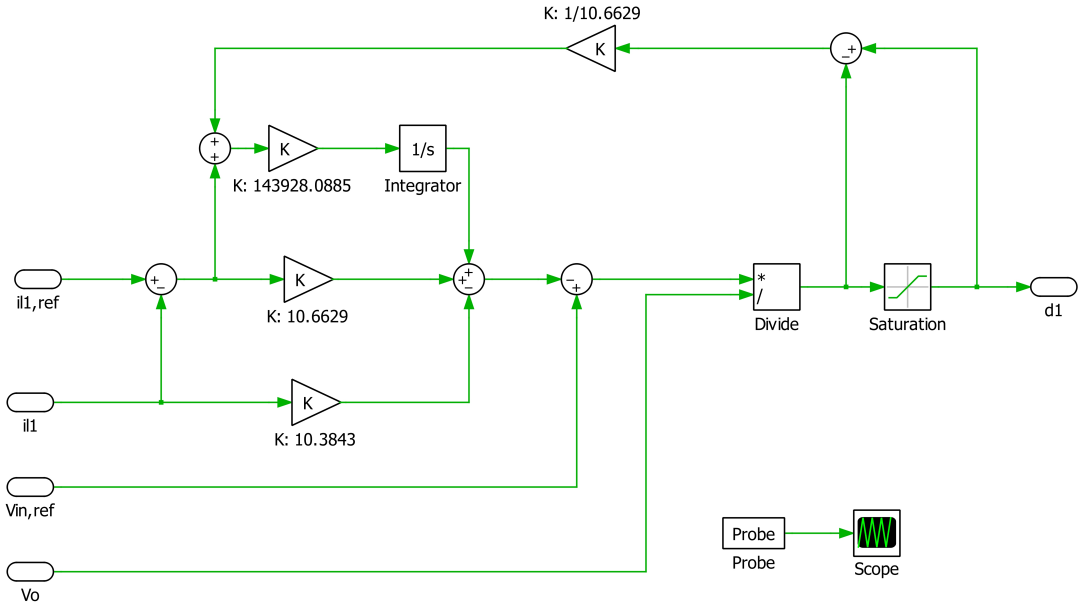

Figure 4.14: Buck current controller circuit in PLECS

4.4.2 Voltage controller

The voltage controller is the outer loop of the dual-loop control strategy implemented. It generates the desired current reference to the current controller. The output voltage is controlled in the discharge mode, while the input voltage is controlled during the charge mode of operation.

4.4.2.1 Boost voltage controller

The boost voltage controller controls the output voltage of the converter. So, the transfer function between the output voltage of the converter and the inductor current is analyzed. Using (4.31) and (4.32), the derived transfer function is

$$\frac{\hat{V_{out}}(s)}{\hat{i_{L_k}}(s)} = \frac{-1.65 \cdot 10^{-7} s^2 - 1.348 s + 6.569 \cdot 10^4}{s + 1.146 \cdot 10^4} \tag{4.35}$$

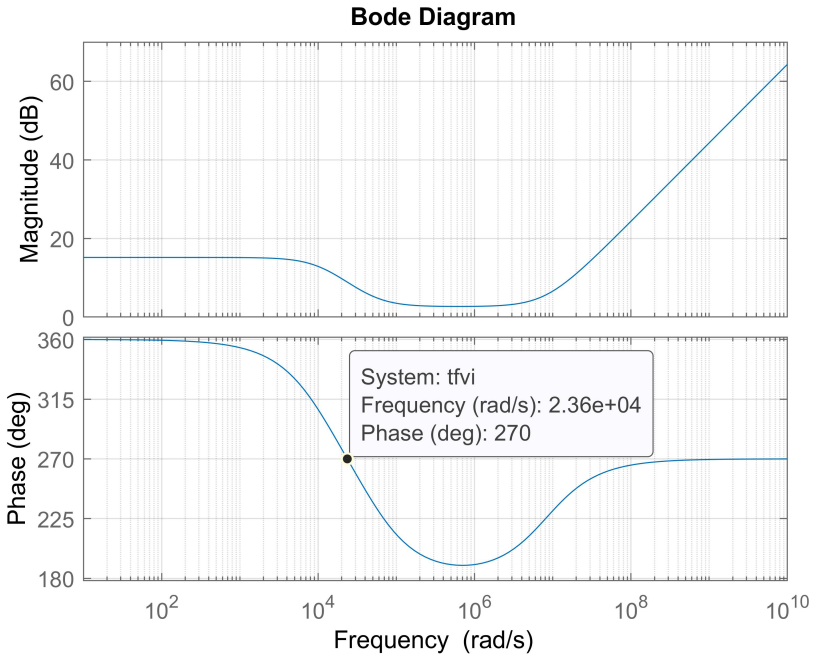

Figure 4.15: Frequency response of the output voltage to the inductor current transfer function in the discharge mode

The cutoff frequency for designing the boost voltage controller is 2.36×10^4 rad/sec from Figure 4.15. The designed values of the proportional and the integrator gain of the PI controller are $k_{pfv} = 1.44$ and $k_{ifv} = 8231.51$. The net inductor current reference is limited to be within a maximum value of 300 A. So, the designed value of the anti-windup term of the controller is $k_{awfv} = 0.7$. The simulated model of the boost voltage controller in PLECS software is shown in Figure 4.16.

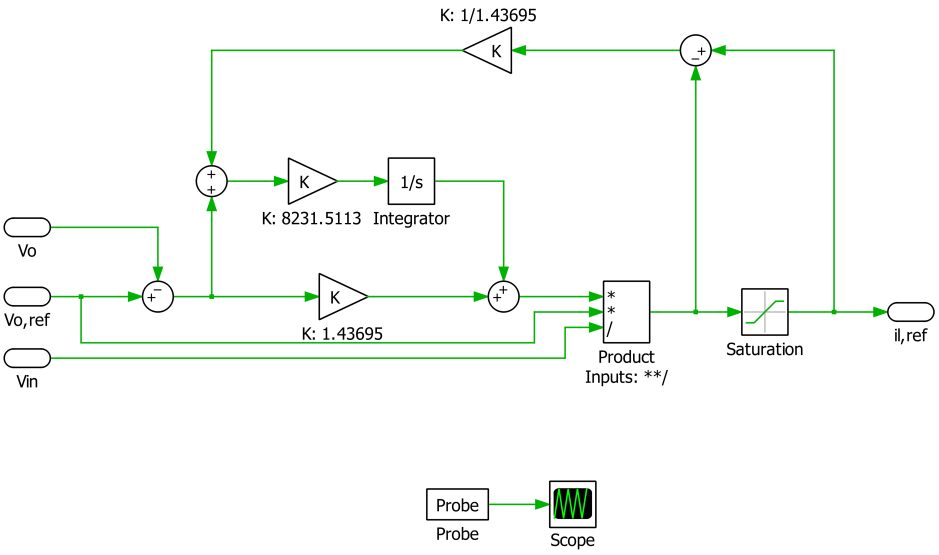

Figure 4.16: Boost voltage controller circuit in PLECS

4.4.2.2 Buck voltage controller

The buck voltage controller controls the input voltage of the converter during the charge mode of operation. Similar to the boost voltage controller, using (4.33) and (4.34), the transfer function is derived as

$$\frac{\hat{V_{in}}(s)}{\hat{i_{L_k}}(s)} = \frac{4.006 \cdot 10^6}{s + 4.173 \cdot 10^5} \tag{4.36}$$

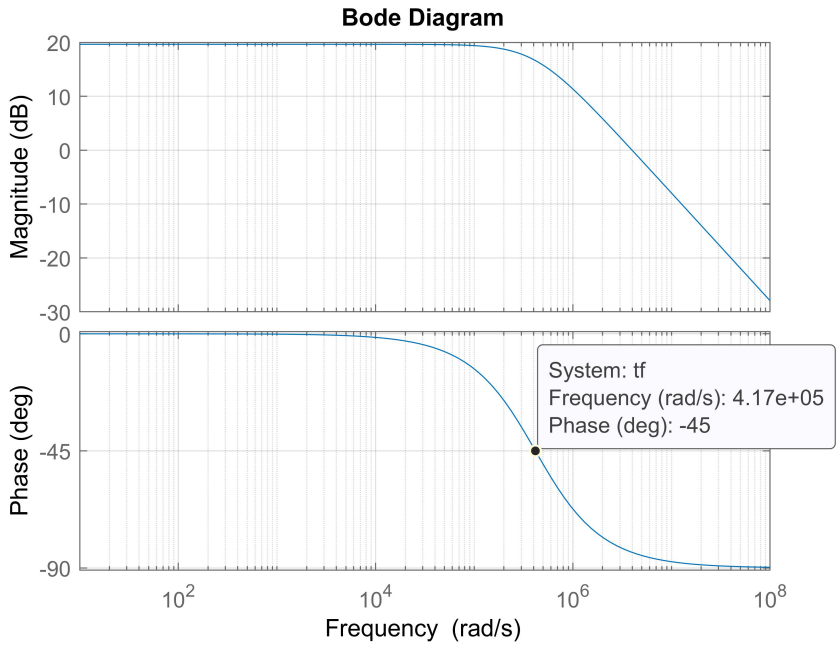

Figure 4.17: Frequency response of the output voltage to the inductor current transfer function in the charge mode

From Figure 4.17, the cutoff frequency for the design of the buck voltage controller is 4.17×10^5 rad/sec. According to the design, the values of the proportional gain, integrator gain and the anti-windup term are $k_{pbv} = 0.42$, $k_{ibv} = 173858.08$ and $k_{awbv} = 2.4$. The simulated model of the buck voltage controller is shown in Figure 4.18.

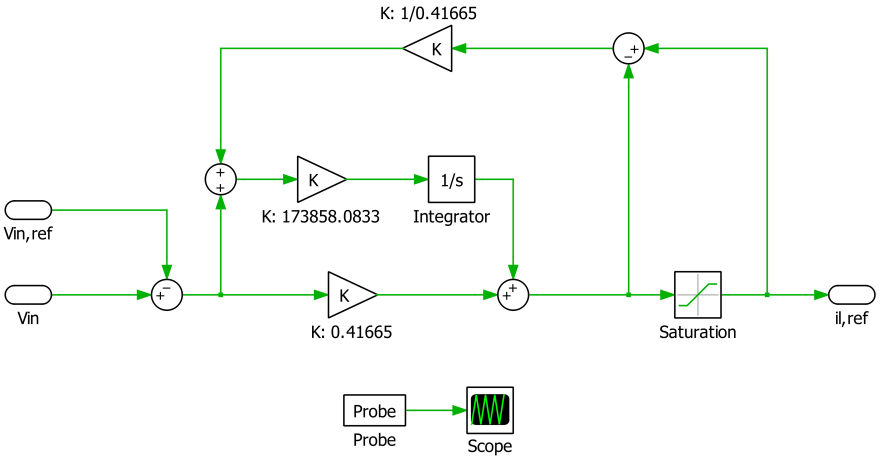

Figure 4.18: Buck voltage controller circuit in PLECS

4.4.3 Phase shift controller

Unlike the four-phase interleaved buck/boost converter, no small-signal analysis is carried for the phase shift controller of three-phase DAB. Determining the state space matrix for the three-phase DAB is a cumbersome process. Hence a simple PI controller is implemented, which controls the phase shift and thereby controlling the power flow. Figure 4.19 shows the control model implemented in PLECS with proportional gain Kp and integral gain Ki as 0.0013 and 0.68e-6, respectively. Figure 4.20 show the PWM generator model, which gives the gating pulse to the MOSFETs.

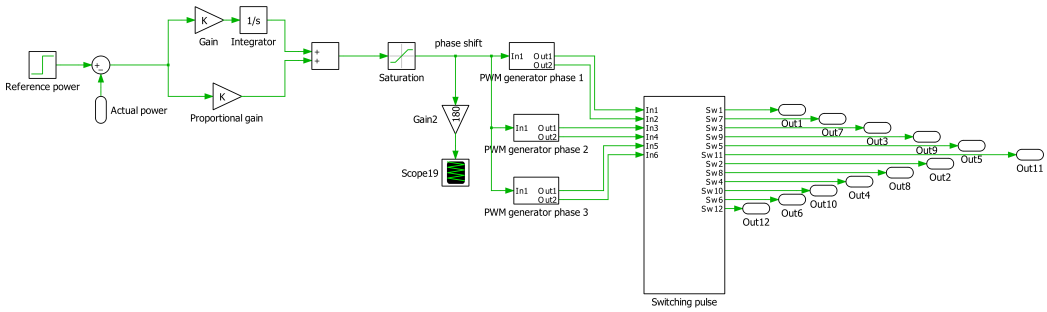

Figure 4.19: Phase shift controller for three-phase DAB

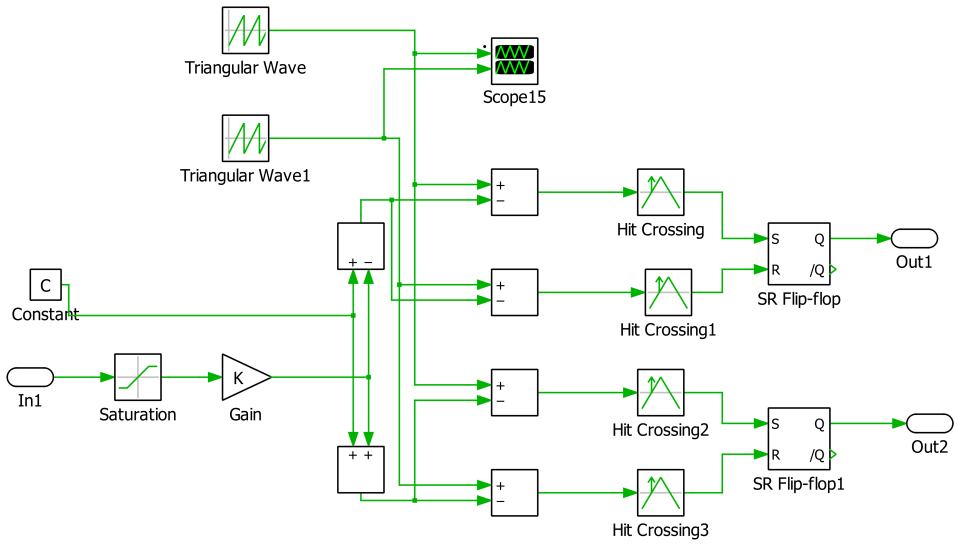

Figure 4.20: PWM generator for three-phase DAB

4.5 Battery model implementation

The battery model implements a Li-ion electrical circuit where the state of charge and the filtered current determine the battery's open-circuit voltage [46]. Table 4.8 specifies the data of battery parameters connected at the input and the output.

Table 4.8: Specification of battery parameters

Number of cells connected in series	180
Number of cells connected in parallel	2
Maximum cell voltage	4.25 V
Minimum cell voltage	2.8 V
Nominal cell capacity	50 Ah
Nominal discharge current	125 A
Internal cell resistance	1.7 mΩ

Figure 4.21 illustrates the R-only Li-ion battery model implemented in PLECS according to the specifications mentioned in Table 4.8. The battery's open-circuit voltage during the charging and the discharging gets determined, as stated in [46].

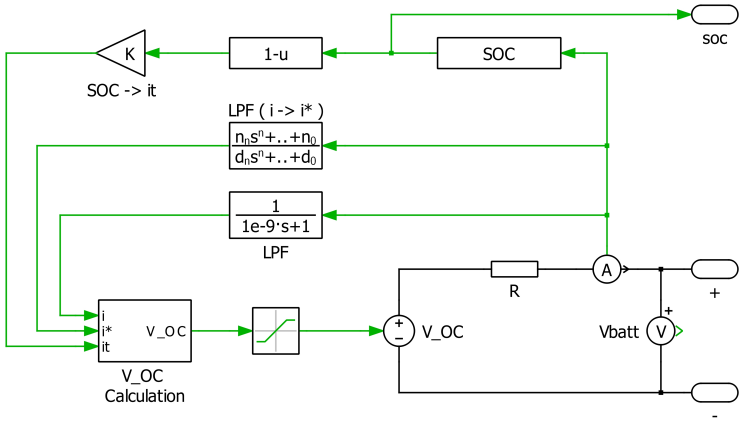

Figure 4.21: R-only based Li-ion battery model simulated in PLECS

5
Analysis

5.1 Four-phase interleaved buck/boost converter operation

The four-phase interleaved buck/boost converter is modelled based on the specifications mentioned in Section 4.1.1. The converter operates in boost and buck mode by controlling the switching of 8 MOSFETs. For the analysis, the designed converter is simulated in PLECS software for 100 ms. The source and load battery's initial SOCs are 90% and 10% during boost mode, while the SOCs are reversed in the buck mode.

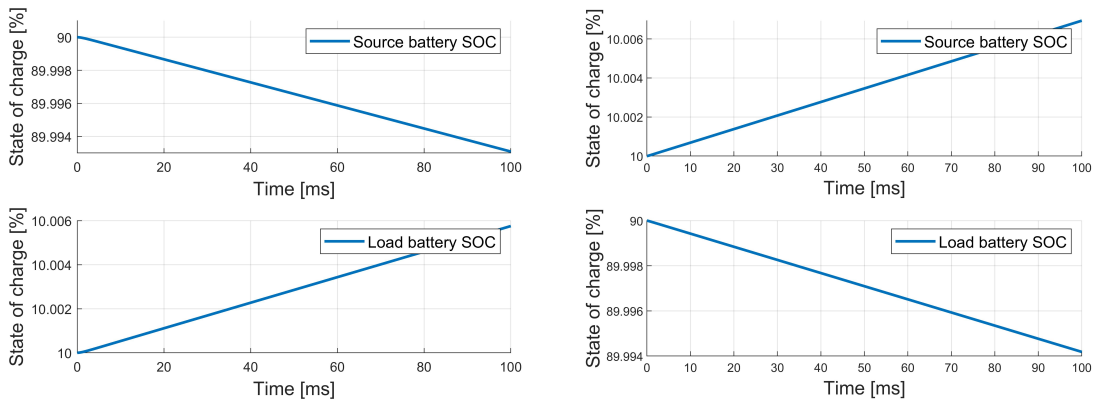

Figure 5.1: Change of SOC in source battery and load battery: a) during boost mode of operation and b) during buck mode of operation

The converter's purpose is to charge the load battery using the power from the source battery and vice versa. From figure 5.1, it is evident that the source battery discharges and charges the load battery during boost mode and vice versa occurs during buck mode of operation.

As discussed in Chapter 3.1.2, the switching of MOSFETs in each phase gets phase-shifted and generates phase currents with a phase shift of 90°. The plot of a single switching period has been shown in Figure 5.2 and Figure 5.3 for the analysis.

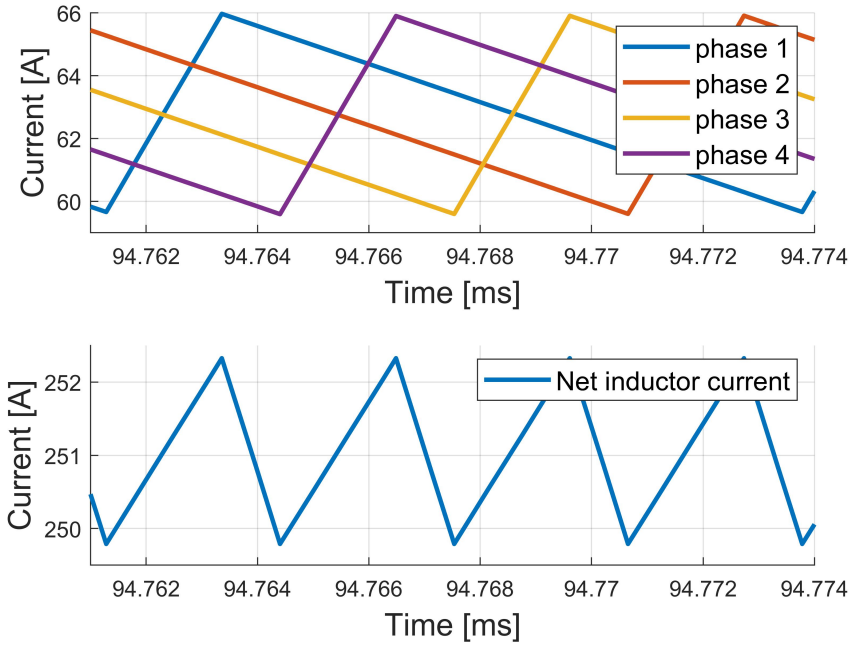

Figure 5.2: top: phase current waveforms during boost mode of operation and bottom: net inductor current waveform during boost mode of operation

The key advantage of the interleaving technique is net current ripple cancellation which is cross-checked with the simulation results. The ripple current cancellation can be observed since the inductor current in each phase overlaps each other. The ripple current in each phase is 6.3 A, with a maximum of 65.9 A and a minimum of 62.3 A, as shown in Figure 5.2. The average value of the inductor current is 62.75 A for each phase.

The net inductor current during boost mode can also be seen in Figure 5.2. It shows that the net inductor current contains a ripple of 2.535 A, which matches the calculated value from (4.5). This value is much smaller than the phase current ripple, which proves the current ripple cancellation effect. The average value of the net inductor current is 251.05 A, with a maximum value of 252.325 A and a minimum value of 249.79 A.

During buck mode of operation, the current flows in the reverse direction, so we get negative currents of the same amplitude and ripple content as the boost operation. From Figure 5.3, the average phase current value is -62.51 A with a ripple content of 6.2 A. On the other hand, the average value of the net inductor current is -250.06 A, containing a ripple value of 2.573 A, which is similar to that of the boost mode.

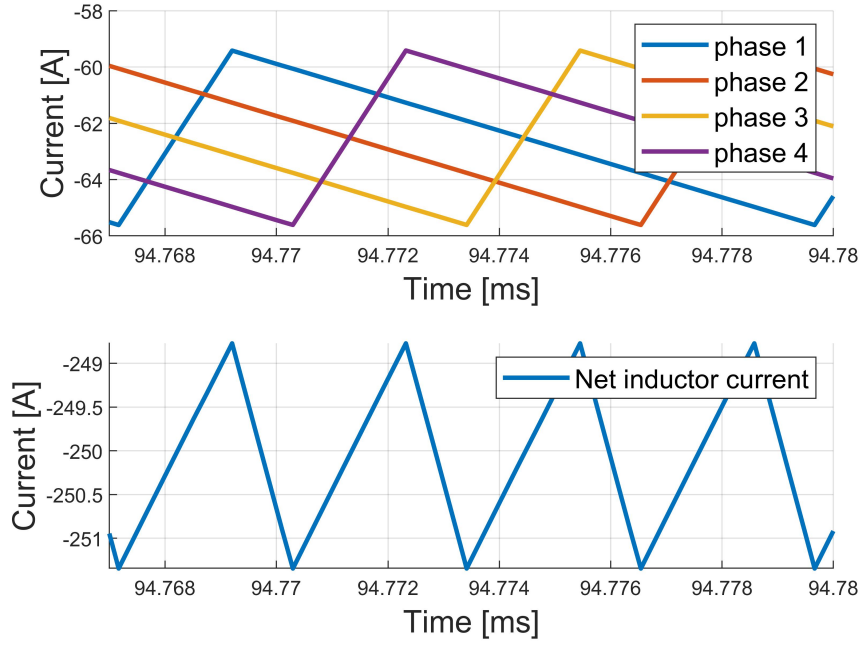

Figure 5.3: top: phase current waveforms during buck mode of operation and bottom: net inductor current waveform during buck mode of operation

Output voltage ripple is an important performance criterion. It is analysed from the output voltage plot as shown in Figure 5.4. It can be seen that the average value of the output voltage of the converter is 718.15 V with a ripple of 0.973 V for both operations. This satisfies the design requirement as mentioned in Section 4.1.1.

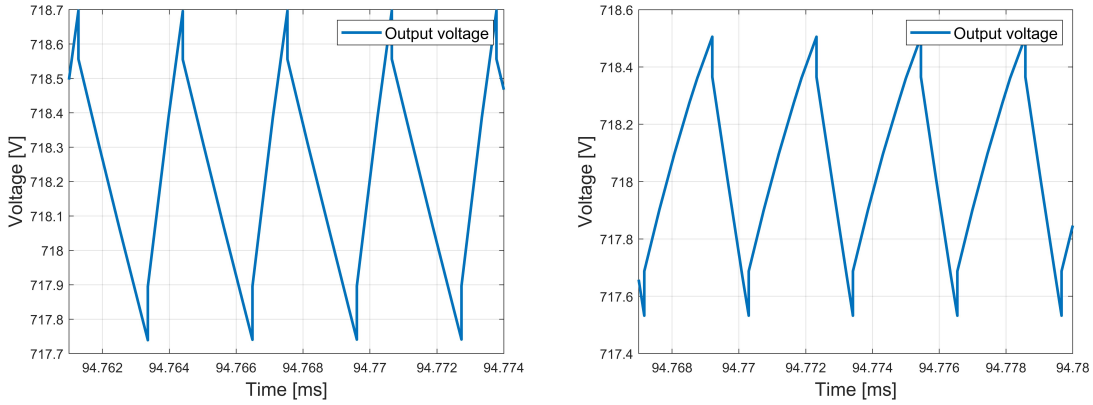

Figure 5.4: Output voltage of the converter: a) during boost mode of operation and b) during buck mode of operation

Similarly, the input voltage of the converter is taken from the source battery's terminal voltage. According to the design, this voltage needs to be maintained at the battery's nominal voltage, which is 600 V.

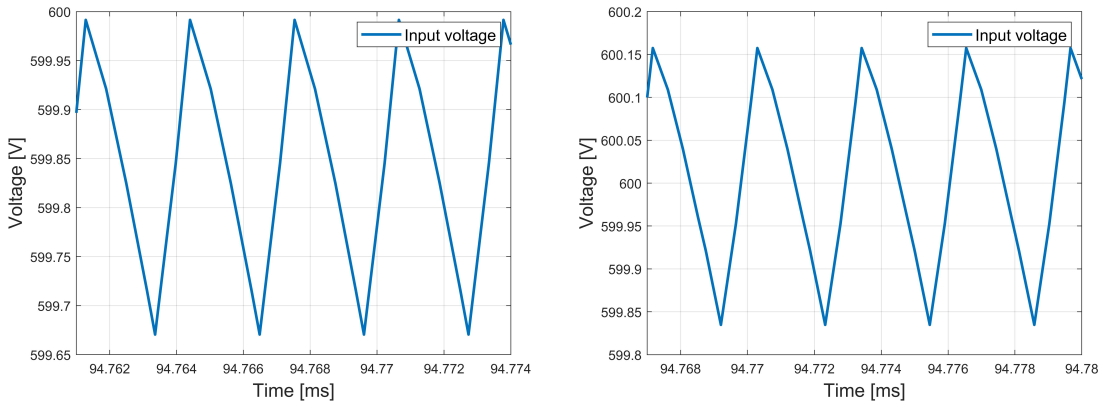

Figure 5.5: Input voltage of the converter: a) during boost mode of operation and b) during buck mode of operation

From Figure 5.5, we get the average input voltage of 599.85 V for the boost operation and 600.01 V for the buck operation. On the other hand, the ripple content does not vary and appears to be constant at 0.32 V for both operations, which is significantly below the design specifications.

5.1.1 Semiconductor component selection

Two MOSFETs are connected at each phase, and they are expected to withstand the converter's output voltage. The current rating of the MOSFET should be much higher than the phase current. Based on the above requirements, a silicon carbide (SiC) MOSFET [56] is selected and modelled in the converter simulation. Some of the benefits of using this MOSFET include reduced switching losses, support higher switching frequencies and reduced cooling requirements [56].

PLECS provides blocksets to implement the MOSFET based on their thermal parameters from the datasheet. The SiC MOSFET's part number is C3M0016120K from Cree (Wolfspeed group), and their thermal parameters can be obtained from the datasheet [56].

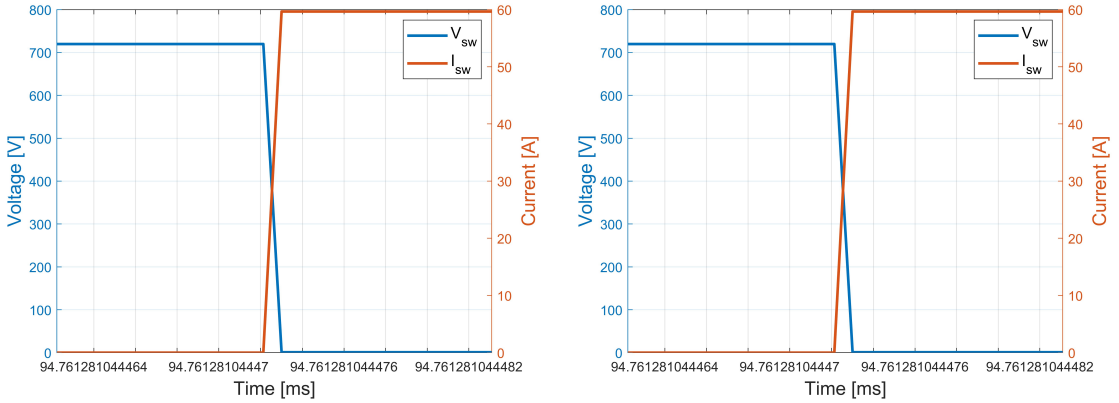

Figure 5.6: Voltage and current stress across MOSFET S_2 during boost mode of operation: a) ON-time stress and b) OFF-time stress

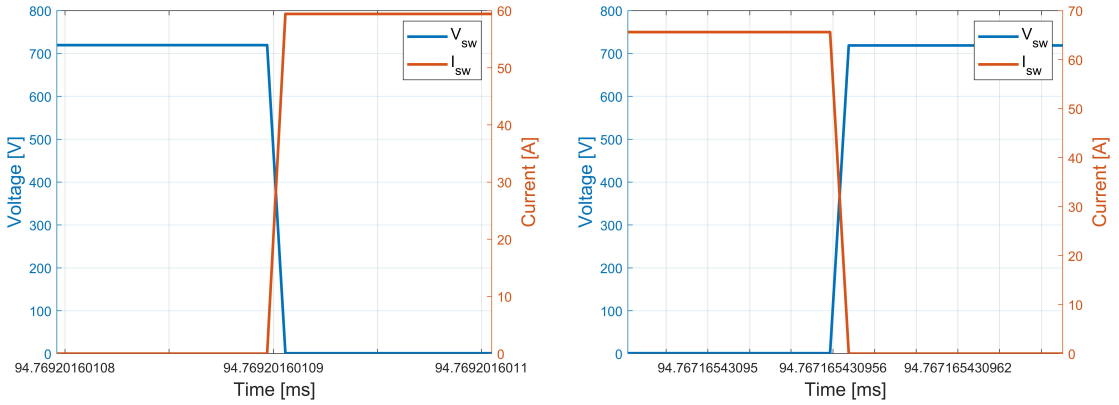

Figure 5.7: Voltage and current stress across MOSFET S_1 during buck mode of operation: a) ON-time stress and b) OFF-time stress

The stress across the MOSFET during boost and buck mode of operation is shown in Figure 5.6 and Figure 5.7, respectively. These graphs show that the voltage that each MOSFET must withstand during off time is 718.2 V. It is much below the MOSFET's drain-source breakdown voltage rating of 1200 V. On the other hand, the continuous drain current rating of the chosen SiC MOSFET is 115 A, which can handle the phase current of the converter.

The ambient temperature and the initial temperature of the heatsink are set to 25°. For the whole SiC MOSFET simulated in the converter, a single heat sink model from the PLECS library is chosen. For boost and buck modes of operation, the thermal performance of the chosen SiC MOSFET is investigated. The junction temperature of the MOSFET reaches a steady-state during boost and buck operation

at 52.42° and 68.87°, respectively, as shown in Figure 5.8.The maximum operating junction temperature of the chosen MOSFET is 175°.

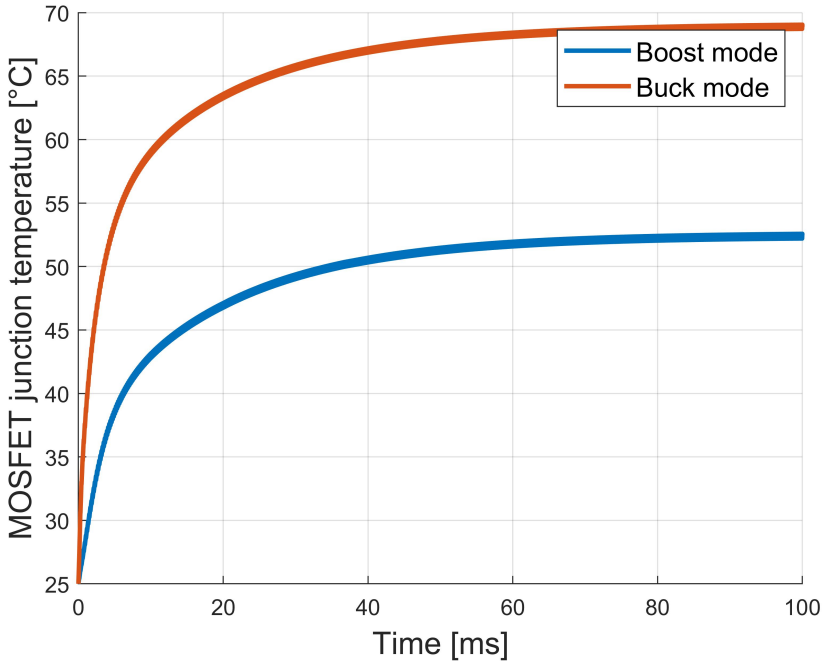

Figure 5.8: Comparison of MOSFET junction temperature during boost and buck mode of operation

5.1.2 Switching frequency optimisation

The parameters that influence the value of optimised switching frequency are losses and the size of the converter. For the initial design of the converter, the switching frequency is selected as 80 kHz. Net conduction loss and net switching loss contribute to the total loss of the converter. The total size of the converter is dominated by the size of the converter's passive components. Therefore, the loss component and the size of passive components are analysed for varied switching frequency to get the optimised switching frequency.

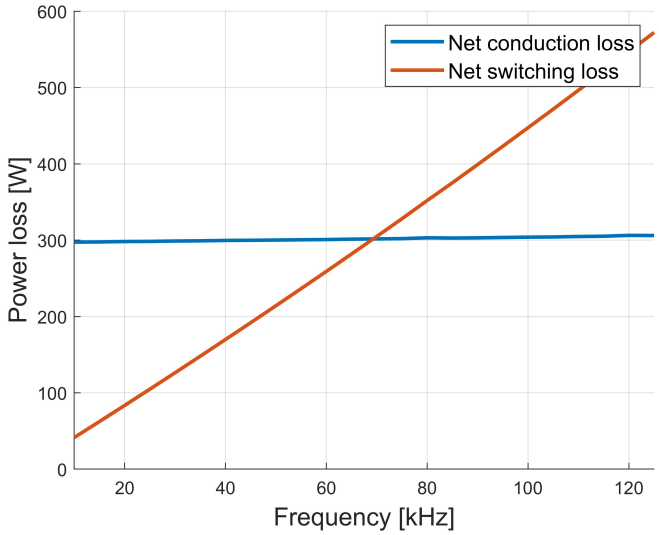

Figure 5.9: Comparison of net switching loss and net conduction loss of the converter for varied switching frequency

The converter is simulated for various switching frequencies according to the design, and the results are analysed. Figure 5.9 compares the net conduction loss with the net switching loss for various switching frequencies. It can be seen that the net conduction loss of the converter is constant for change in the switching frequency. However, the net switching loss increases linearly with an increase in the switching frequency. Therefore, the switching loss component alone is considered for optimising the switching frequency.

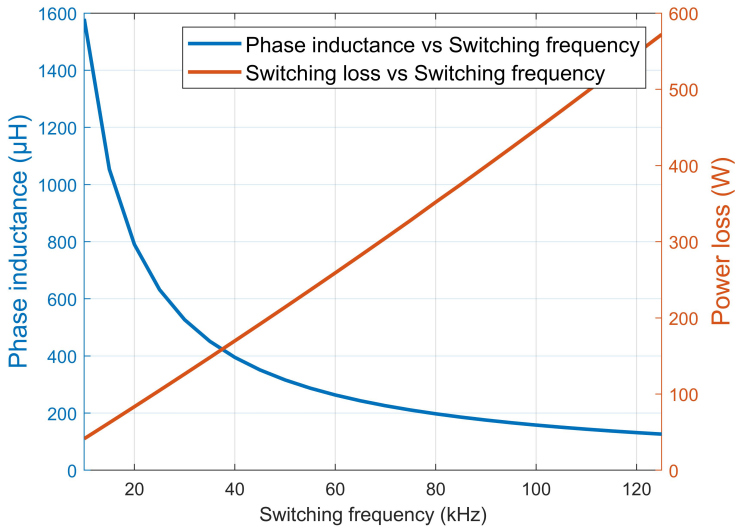

Figure 5.10: Comparison of net switching loss and phase inductance of the converter for varied switching frequency

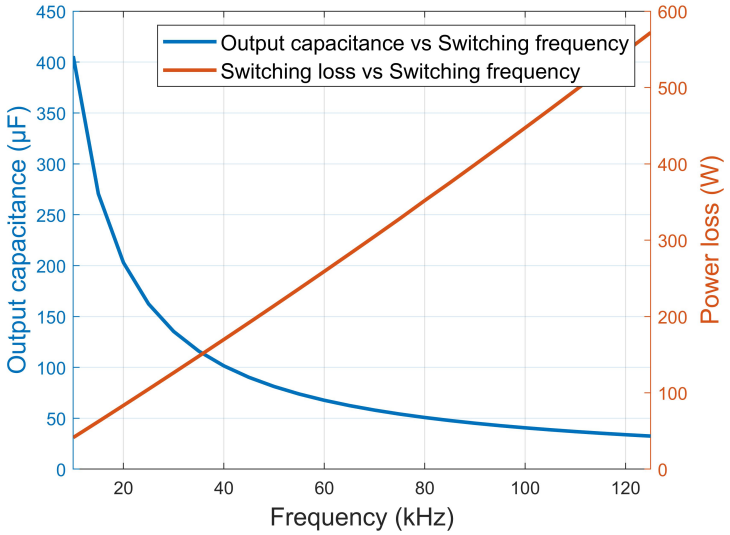

Figure 5.11: Comparison of net switching loss and output capacitance of the converter for varied switching frequency during boost mode of operation

The size of the phase inductor and the output capacitor dominates the total size of the converter. The input capacitor size is minimal compared to other components, so its variation for varying the switching frequencies is not considered. The size of the phase inductor and the output capacitor is inversely proportional to the switching frequency based on (4.4) and (3.23). Figure 5.10 and Figure 5.11 show that the converter's size decreases as the switching frequency increases, but the switching loss of the converter increases, reducing the converter's efficiency. Therefore, the passive component's size and the switching loss of the converter are compromised to achieve an optimised switching frequency of 80 kHz for this application.

5.2 3 Phase Dual Active Bridge converter operation

The three-phase dual active bridge is simulated in PLECS, and the results are reported & analyzed for the specifications stated in section 3. One of the key parameters designed for the converter is the voltage ripple. Figure 5.12 shows the output voltage of the receiver battery for a power level of 150 kW. As shown in the figure, the average output voltage value is 720 V with a voltage ripple of 1 V.

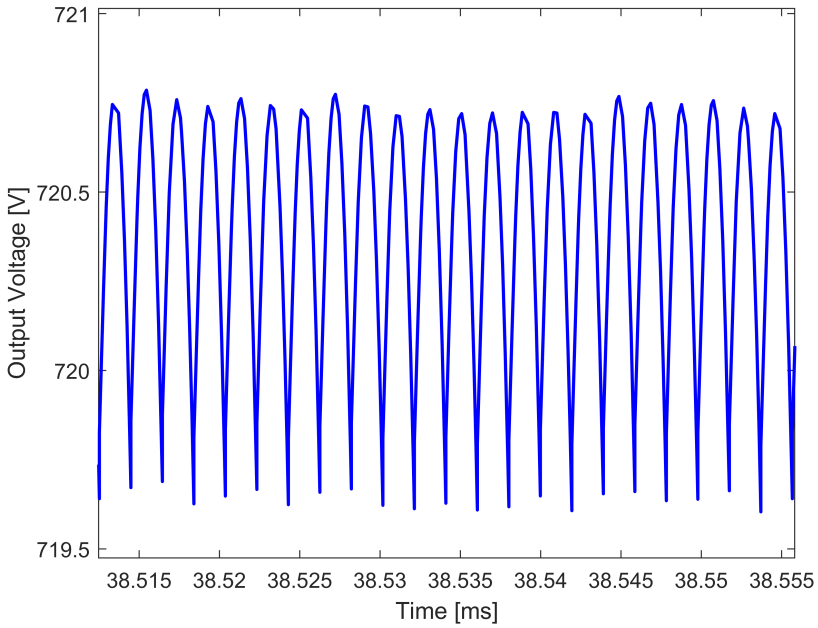

Figure 5.12: Output voltage of three-phase DAB

The figure 5.13a and 5.13b shows the inductor current for a phase shift of 40 degree and 70 degree, respectively. As described in section 3.2.1.1, when the shift is greater than 60 degrees, the current shape changes. This is due to the fact that when the shift is more than 60 degrees, the voltage difference applied across the inductor changes.

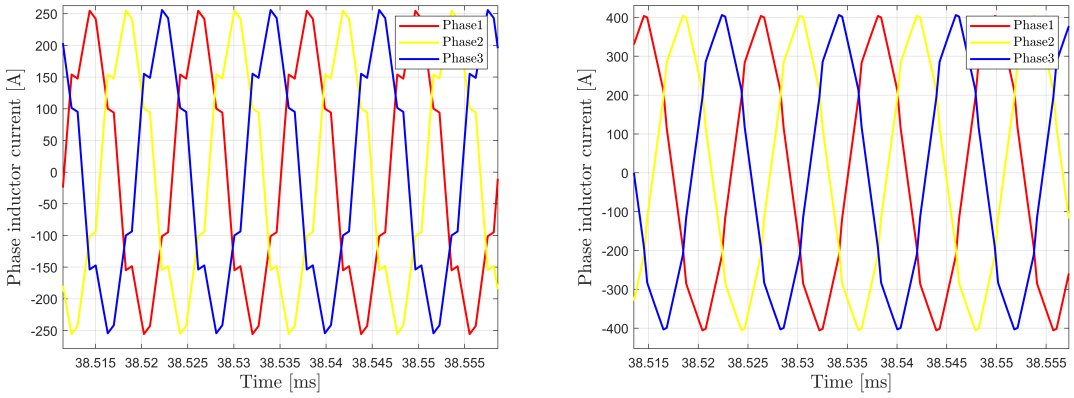

Figure 5.13: Inductor current of three-phase DAB: a)For a phase shift of 40°and b)For a phase shift of 70°

5.2.1 Soft switching boundaries

As shown in (3.31), the soft switching area is affected by the operating frequency and the phase inductance. Figure 5.14 shows the impact of frequency in soft switching

boundaries for the converter with a phase inductance of 2.4μH. As can be seen from the figure, increasing the frequency increases the soft switching area. The dashed green and black lines represent two operating points with input voltages of 600 V and 530 V, respectively. For an input voltage of 600 V and a frequency of 85 kHz, operating the converter below 73.59 kW leads to hard switching of the primary side switches. On the other hand, operating the converter at 530 V leads to primary hard switching even before that. Thus, operating the converter at a voltage ratio of one gives soft switching for the entire range of operation, i.e. to operate the converter at an input voltage of 725 V.

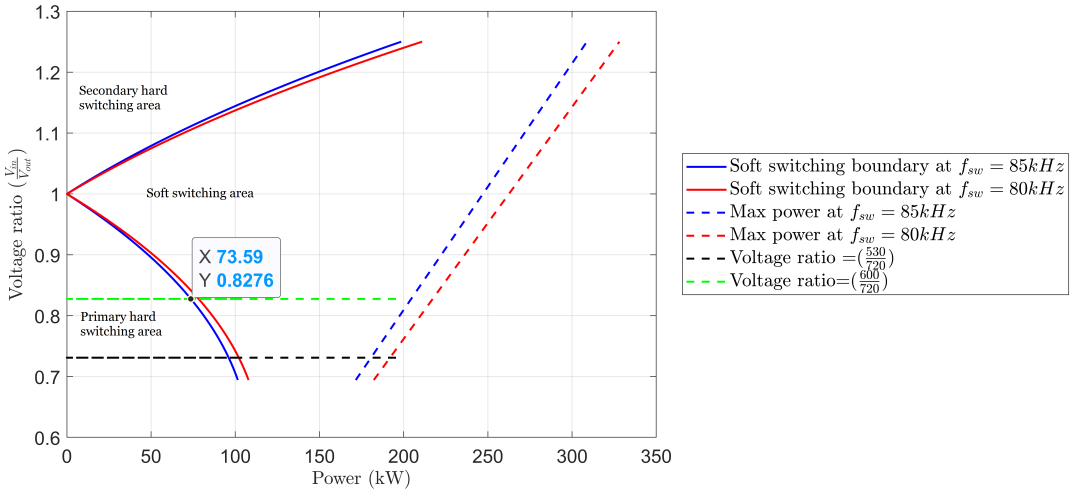

Figure 5.14: Soft switching boundaries for two different frequencies

In the same way, the impact of phase inductance on soft switching boundary for the converter operated at 85 kHz is shown in figure 5.15 . It is noticeable that the soft switching area can be increased by choosing a higher inductance value. Though the converter's maximum power can be increased with lower inductances, it significantly increases the switching loss of the converter. The phase inductance cannot be increased beyond 2.4 μH as it limits the power handling capability of the planar transformer. Hence operating the converter below 73.59 kW at an input voltage of 600 V with a frequency of 85 kHz, results in hard switching of the primary side switches.

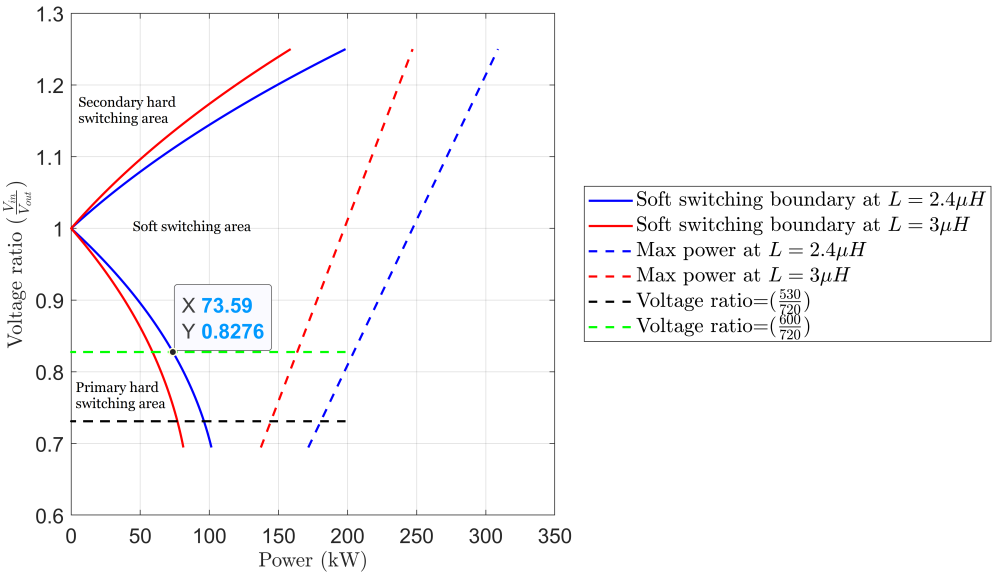

Figure 5.15: Soft switching boundaries for two different inductances

5.2.2 Semiconductor selection for three-phase DAB

One of the most important factors to consider when selecting a MOSFET is the voltage and current stress experienced by the MOSFET. Hence an ideal three-phase dual active bridge is modelled in Matlab/Simulink to identify the voltage and the current stress on the primary and secondary side switches. Figures 5.16a and 5.16b show the voltage and current stress of primary and secondary side switches, respectively.

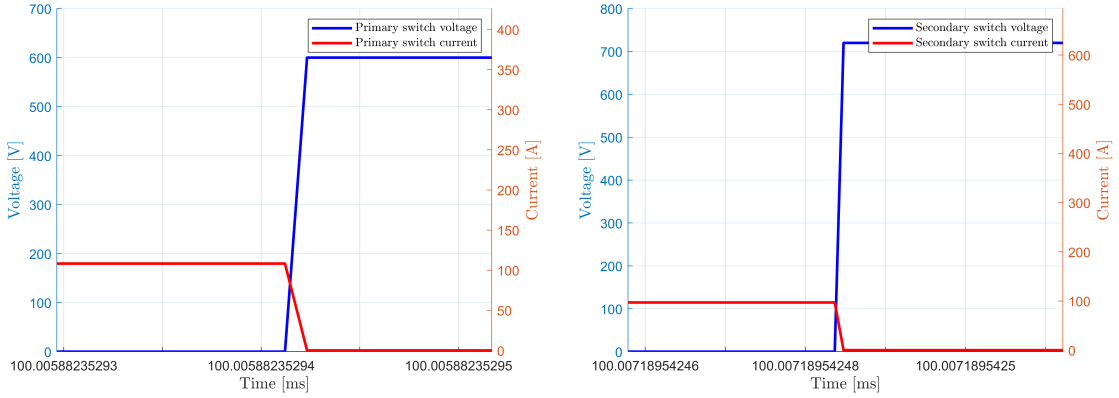

Figure 5.16: Voltage and current stress across MOSFET: a)For a primary switch and b)For a secondary switch

The MOSFET's ability to operate at 85 kHz is another critical parameter that must be verified. The manufacturer's datasheet includes a graph of the safe operating area, which shows how to operate the MOSFET in terms of voltage and current

safely. Based on this, silicon carbide (SiC) MOSFET [57] is selected, and its thermal description is used for modelling in PLECS. Figure 5.17 shows the safe operating area for the MOSFET selected.

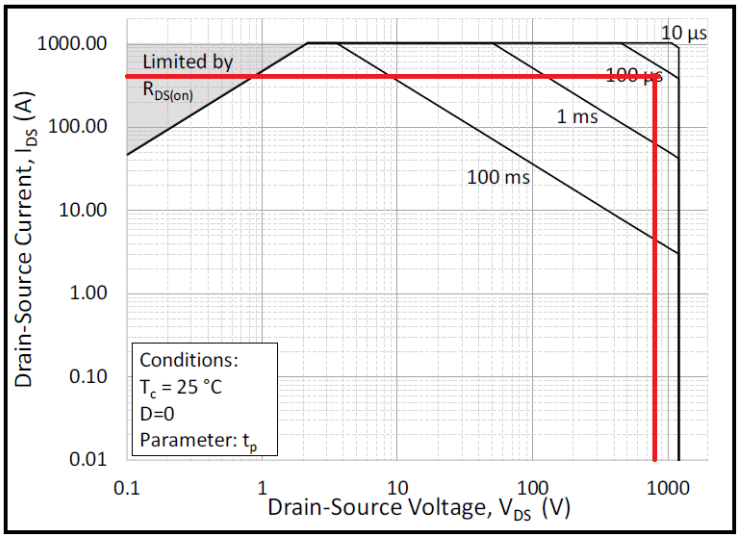

Figure 5.17: Safe operating area of the MOSFET CAB760M12HM3

It can be seen that the selected MOSFET can withstand a voltage of 800 V and a drain current of 300 A for more than 100 us. The converter is modelled in PLECS using a Cree semiconductor with a heat sink dedicated to the primary and secondary sides as shown in figure 4.10. Figure 5.18 shows the junction temperature of the MOSFET for the primary and secondary side switches. The junction temperature of the primary and secondary switch reaches 123°and 127°, respectively. The maximum junction temperature of the MOSFET is 175°.

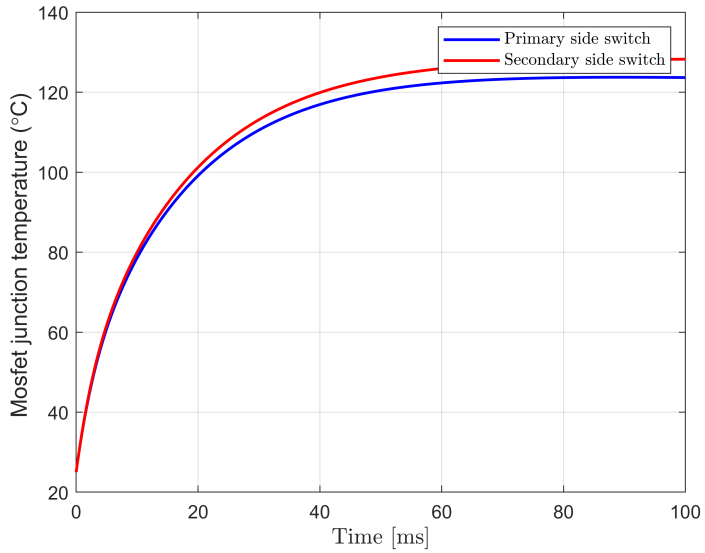

Figure 5.18: Comparison of MOSFET junction temperature between the primary and secondary switch

5.3 Response of dual loop controller

The dual loop controller with an internal current loop and external voltage loop is constructed separately for boost and buck operations. Controller model verification is performed for the converter using the electrical parameters specified in Section 4.1.1. From this analysis, the robustness of the controller for electrical parameter variations is realized.

5.3.1 Response of boost voltage controller

In this section, the converter's output voltage dynamic response is analysed by providing step changes to the output voltage reference. While the converter's output voltage operates at 718.2 V steady-state value, the output voltage reference is reduced to 710 V at 10 ms. The model is simulated for 30 ms by turning off the step change at 20 ms.

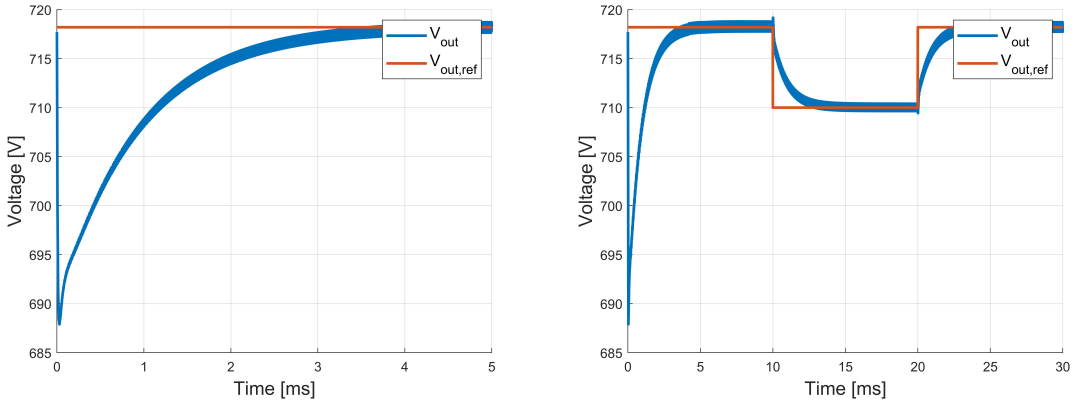

Figure 5.19: Output voltage response of the controller during boost mode of operation: a)For rated output voltage reference of 718.2 V and b)For change of output voltage reference from 718.2 V to 710 V

Figure 5.19 illustrates the step response of the converter's output voltage. The initial voltage of the output capacitor is given as 718.2 V. However, it can be seen from Figure 5.19 a) that the response curve decreases at its early phase and later increases. This is due to the boost operation, which is not a minimum phase system [58]. The settling time of the voltage response is approximately 4.2 ms. From Figure 5.19, it can be seen that the output voltage reference is changed at 10 ms and 20 ms, while the actual output voltage follows the reference value without deteriorating the system. The voltage controller works by setting the appropriate current reference value to the inner current loop for controlling the output voltage. From Figure 5.19 and Figure 5.20, V_{out} matches $V_{out,ref}$ when the output of the voltage controller reaches a steady-state value, which in this case is $i_{L1,ref}$.

5.3.2 Response of boost current controller

The output of the boost voltage controller determines the reference value of the boost current controller. The response of the inner current loop is examined for the same step change in the output voltage reference.

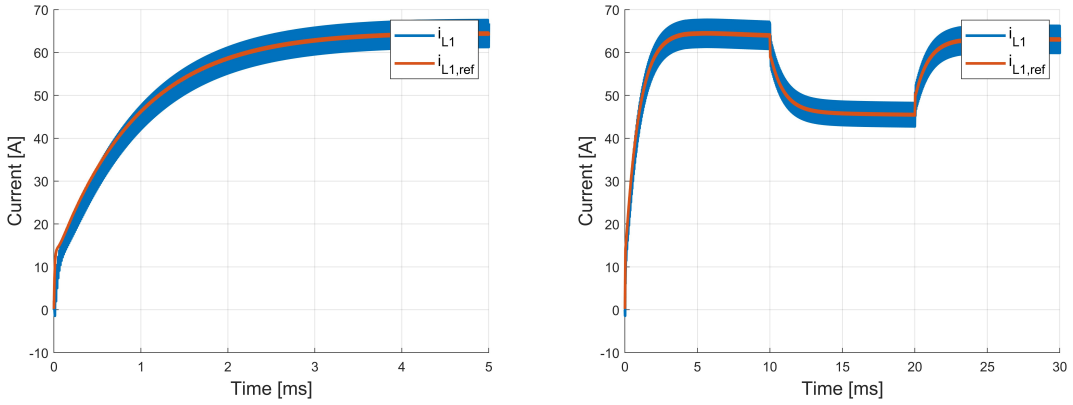

Figure 5.20: Inductor current response of the controller during boost mode of operation: a)For rated output voltage reference of 718.2 V and b)For change of output voltage reference from 718.2 V to 710 V

Initially, when $V_{out,ref}$ is set to 718.2 V, the value of $i_{L1,ref}$ starts to increase from zero. The actual phase current tracks the reference current almost instantaneously. Thus, the inner current loop response is much faster compared to the outer voltage loop response. Figure 5.20 b) shows the controller's dynamic performance with respect to change in $V_{out,ref}$. This is achieved as the current controller controls the duty cycle of the MOSFET connected to the particular phase. At t=10 ms, $V_{out,ref}$ drops by 10 V, and the duty cycle of the MOSFET is reduced to control V_{out}. Conversely, the duty cycle of the MOSFET increases at 20ms for the change of $V_{out,ref}$.

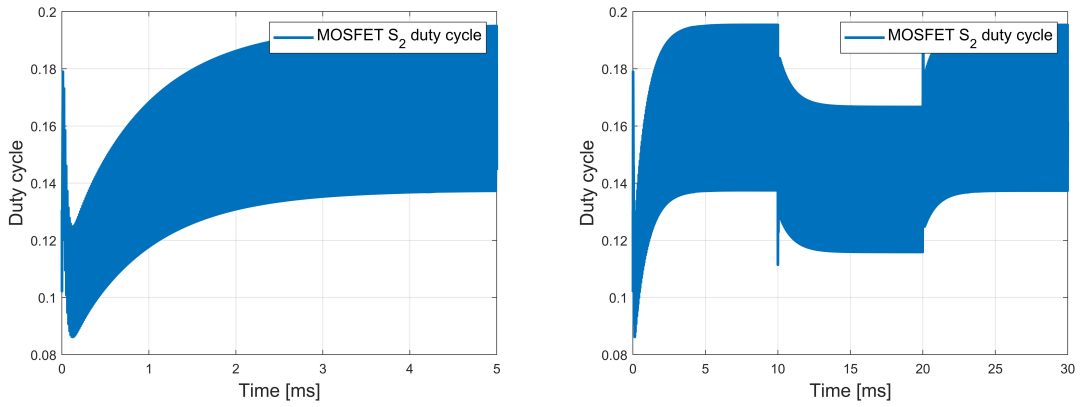

Figure 5.21: Variation of MOSFET S_2 duty cycle during boost mode of operation: a)For rated output voltage reference of 718.2 V and b)For change of output voltage reference from 718.2 V to 710 V

The boost current controller controls only phase 1 current. At the same time, other phase currents are indirectly controlled by phase-shifting the duty cycle of the MOSFETs connected to each phase. Figure 5.22 represents the phase shift between the duty cycle of each phase MOSFETs. PWM generator generates the gate pulses accordingly to 8 MOSFETs connected. The current controller's reference current $i_{L1,ref}$ attains a steady state when the MOSFET duty cycle reaches its steady-state value.

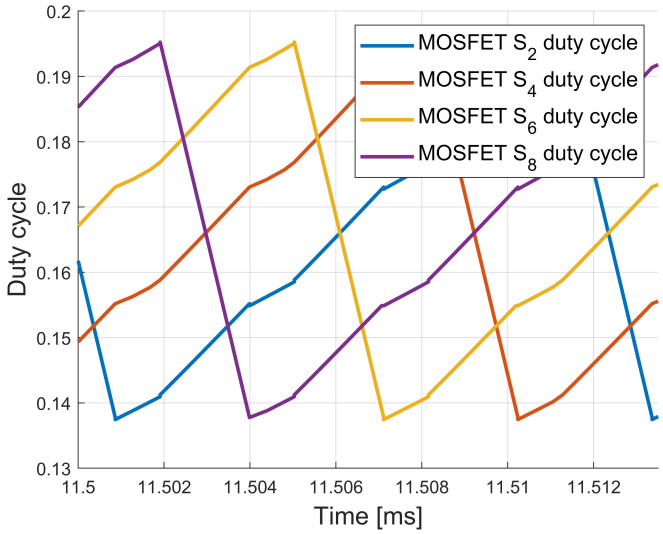

Figure 5.22: Duty cycle of each phase MOSFET during boost mode of operation

The range of the $V_{out,ref}$ variation depends on the SOC level of the source and the load batteries. The dual loop controller does not directly control the power flow from the source battery to the load battery. It can be seen from Figure 5.23 that by controlling V_{out} and i_{L1}, the dual loop controller indirectly controls the power flow

through the converter. The output power is 150 kW till 10 ms, and after the step change, it gets reduced to 110 kW.

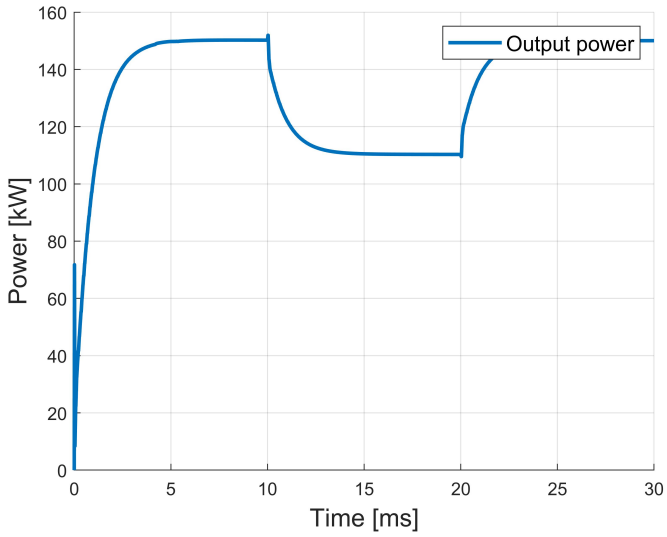

Figure 5.23: Converter's output power during boost mode of operation

5.3.3 Response of buck voltage controller

The buck voltage controller controls the converter's input voltage during the buck mode of operation. The dynamic response of the controller's behaviour for step-change in $V_{in,ref}$ is analysed. The converter's input voltage is maintained at the battery's nominal voltage of 600 V. The model is simulated for 15 ms with step changes provided to $V_{in,ref}$ at 5ms and 10 ms.

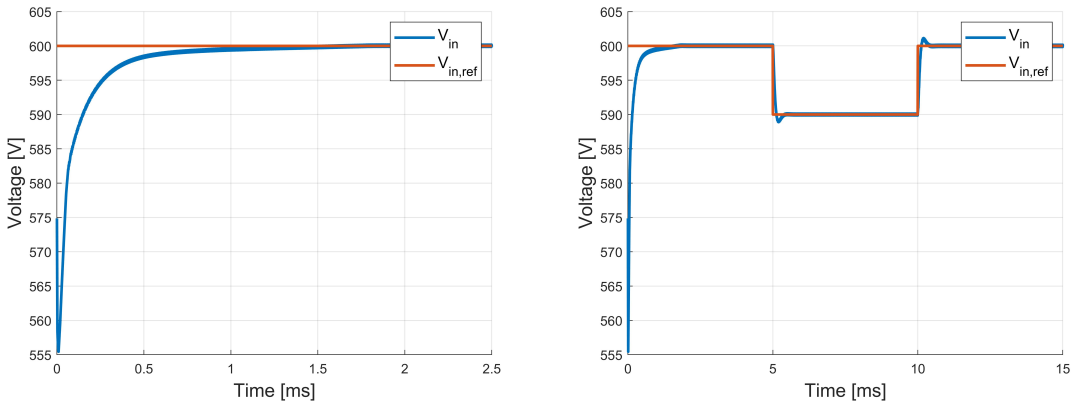

Figure 5.24: Input voltage response of the controller during buck mode of operation: a)For rated input voltage reference of 600 V and b)For change of input voltage reference from 600 V to 590 V

The initial voltage of the input capacitor C_{in} is given as 600 V. The settling time

of Vin is 1.8 ms which can be seen from Figure 5.24 a). From Figure 5.24 b), the dynamic response of the controller with V_{in} following $V_{in,ref}$ for the step changes can be seen. At t=5 ms, $V_{in,ref}$ is decreased by 10 V, so the controller controls $i_{L1,ref}$ and decreases it for controlling V_{in}.

5.3.4 Response of buck current controller

During the buck mode of operation, the controller controls the inductor current in the reverse direction. The buck current controller's dynamic response is evaluated for the same step-change in $V_{in,ref}$.

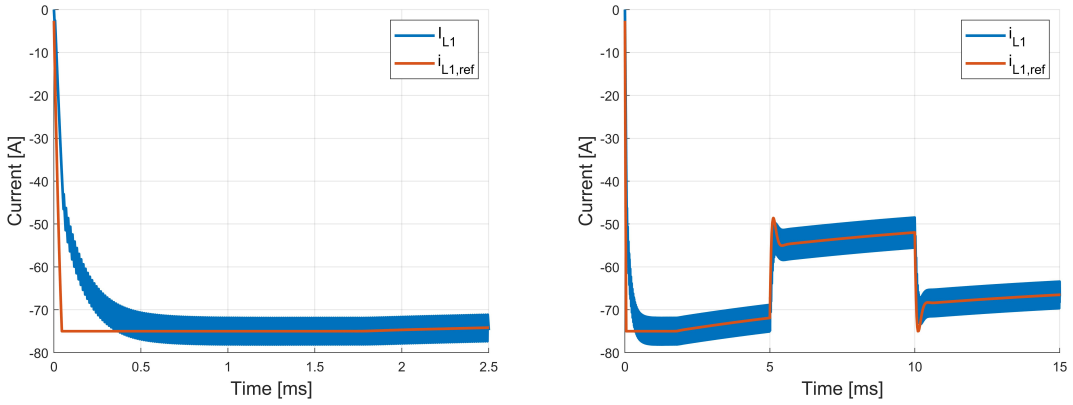

Figure 5.25: Inductor current response of the controller during buck mode of operation: a)For rated input voltage reference of 600 V and b)For change of input voltage reference from 600 V to 590 V

The buck voltage controller determines the value of $i_{L1,ref}$. Figure 5.25 a) presents the actual phase current i_{L1} following the reference value $i_{L1,ref}$ and getting settled at 0.5 ms. This confirms that the response of the buck current controller is much faster than the buck voltage controller's response.

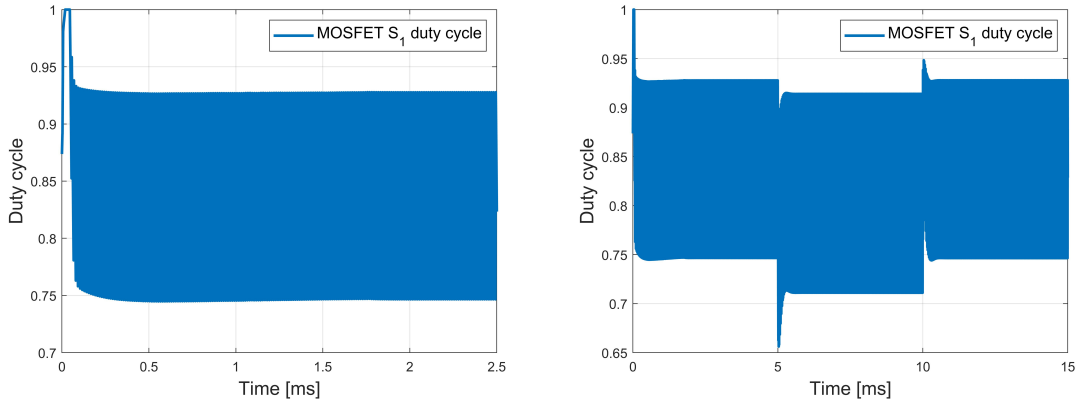

Figure 5.26: Variation of MOSFET S_1 duty cycle during buck mode of operation: a)For rated input voltage reference of 600 V and b)For change of input voltage reference from 600 V to 590 V

The converter's input voltage V_{in} acts as the output voltage of the buck topology. So, when $V_{in,ref}$ gets reduced at 5 ms, the current controller operates by controlling the duty cycle of MOSFET S_1. In this way, the duty cycle of MOSFET S_1 reduces at 5 ms and increases at 10 ms for matching the actual value V_{in} with that of the reference $V_{in,ref}$. Figure 5.25 b) illustrates the buck current controller's response to the step-change in $V_{in,ref}$. From Figure 5.25 a) and Figure 5.26 a), it can be interpreted that the current reference $i_{L1,ref}$ reaches the steady-state value when the MOSFET duty cycle attains its steady-state value.

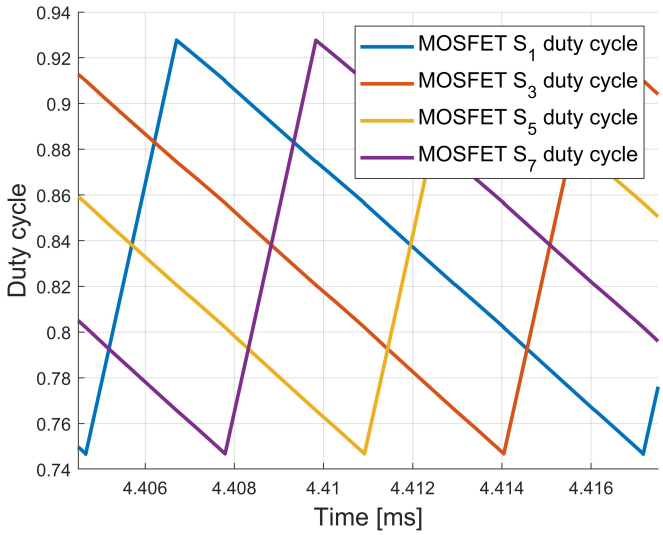

Figure 5.27: Duty cycle of each phase MOSFET during buck mode of operation

Like the boost controller, only phase 1 current is controlled in the reverse direction by the buck current controller. The other phase currents are controlled by phase-shifting the duty cycle of the MOSFET S_1. Figure 5.27 shows the phase shift

between the duty cycle of each phase MOSFET. In the buck operation, the dual loop controller eventually controls the converter's input power by controlling the converter's input voltage V_{in} and the phase current i_{L1}. Figure 5.28 exhibits the converter's input power variation for change in $V_{in,ref}$.

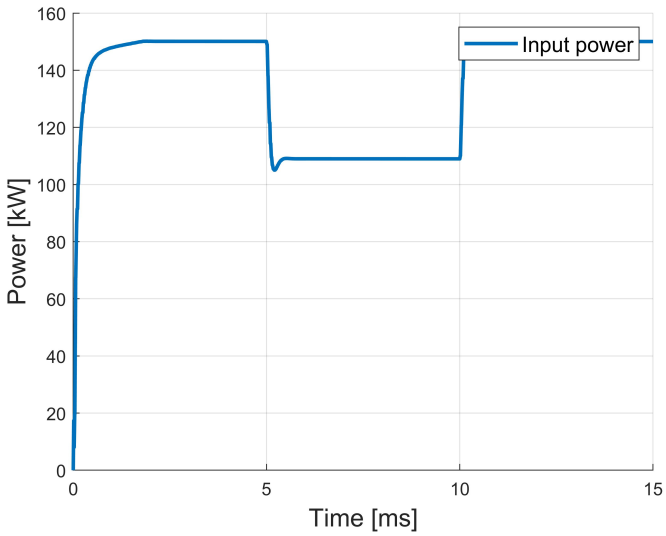

Figure 5.28: Converter's input power during buck mode of operation

5.4 Response of DAB controller

A phase shift controller is implemented for a bi-directional power flow of a three phase DAB. To control the power flow, the pulses produced by the controller must have phase shift between the primary and secondary side switches. To check the stability and the ability to track the power reference, a step response of the power flow is carried out for the controller. The converter model is simulated for 30 ms with initial power reference of 150 kW. The reference value is reduced by 30 kW at 10 ms and changed back to 150 kW at 20 ms as shown in the figure 5.29. From the figure, the controller is able to track the reference with a settling time of 5.4 ms.

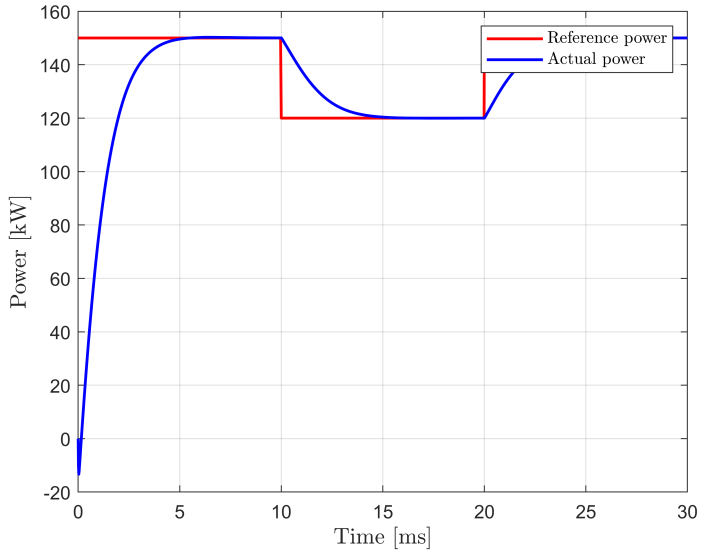

Figure 5.29: Step response of output power for the three-phase DAB

Figure 5.30 shows the phase shift response for the step change of the power transfer. As there is step change in power reference at 10 ms and 20 ms, the phase shift is controlled accordingly to track the reference. Based on the phase shift (ϕ), the PWM generator generates gate pulse for 12 switches.

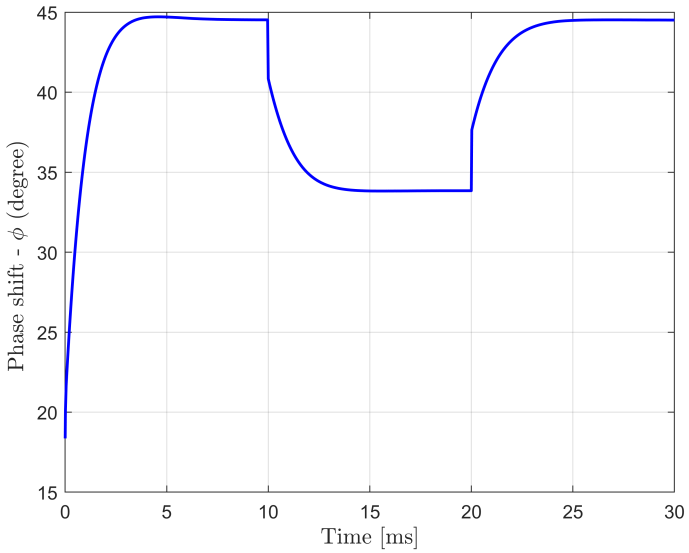

Figure 5.30: Phase shift (ϕ) for the step response of the controller

5.4.1 Response of power reversal in a three-phase DAB

Since a three-phase DAB is a bidirectional converter, the power flow can be positive or negative based on the phase shift. This phenomenon is tested by providing negative step change as the reference. Hence, a step change of -150 kW is provided at 15 ms, and the figure 5.31 shows the controller response.

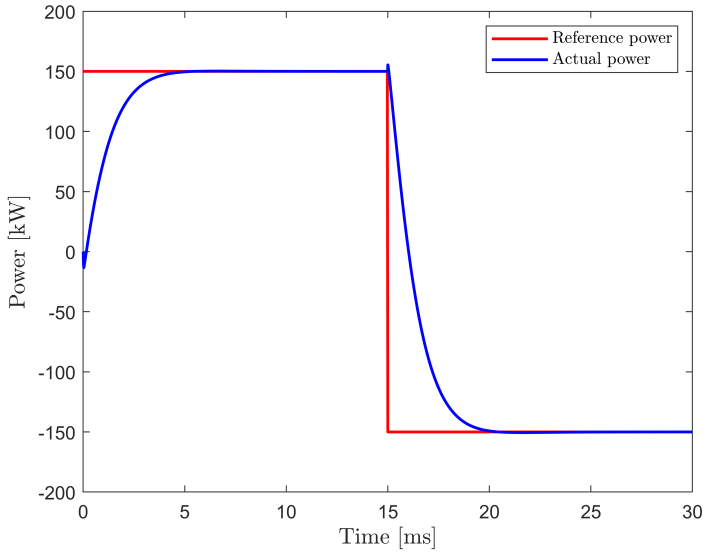

Figure 5.31: Power reversal response of the controller

With a settling time of 5.4 ms, the controller follows the reference value for positive and negative power values. Figure 5.32 shows the response of the phase shift for power reversal.

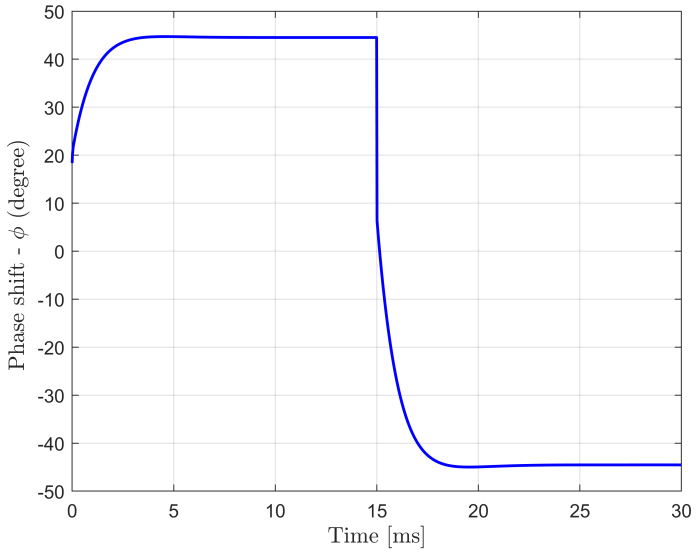

Figure 5.32: Phase shift response for the power reversal

For a negative power flow, the controller provides a negative phase shift as expected. From the figure, since the power level is the same for both directions, the corresponding phase shift is also the same. This implies that the equation (3.27) & (3.30) hold for negative power flow as well.

5.5 Efficiency calculation

In this section, the efficiency of both the converter topologies is analysed. Converter's efficiency calculation is as follows

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}} \tag{5.1}$$

where P_{out} and P_{losses} represent the converter's output power and the net power losses associated with the converter. However, losses associated with both the converter topologies vary and are explained in detail.

5.5.1 Four-phase interleaved buck/boost converter

Net losses in the interleaved buck/boost topology consist of losses in the inductors, capacitors and semiconductor losses. In general, these losses can be split into two types, namely, net switching loss and net conduction loss. Net semiconductor losses can be obtained by the calculation discussed in Section 3.5.1. For the inductor with a high current and low ripple current, the winding loss component becomes dominant compared to the core loss component. Hence, the inductor core losses are neglected during the calculation. Winding losses are composed of DC and AC components of the conductor resistance. For simplicity, the DC component of the conductor resistance alone is considered. The winding loss in the inductor is calculated by

$$P_{cond,loss} = R_{dc} I_{dc}^2 \tag{5.2}$$

where R_{dc} is the DC component of conductor resistance and I_{dc} is the average current flowing through the conductor. The equivalent series resistor in the capacitor is a summation of losses occurring within the metallic elements and the dielectric material. Therefore, ESRs of each phase inductor, input capacitor and output capacitor is taken as the value of R_{dc} for their respective loss calculations.

Total loss in the converter can be found by summing up the conduction loss in each phase inductor, input capacitor, output capacitor and the net semiconductor losses associated with 8 MOSFETs. In this calculation, battery losses at the input and output are neglected. This calculation of estimating the converter's efficiency is modelled in the PLECS software along with the converter simulation model.

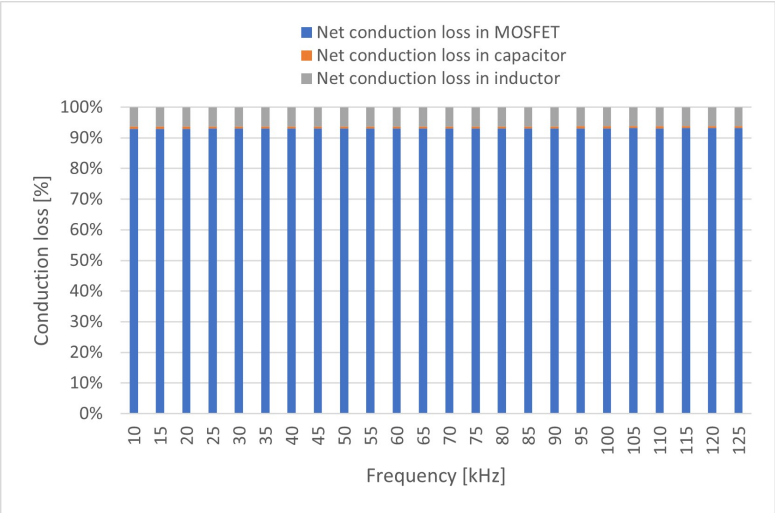

Figure 5.33: Proportion of conduction loss across different components of the converter for varied switching frequency

From Section 5.1.2, it has been found that the net conduction loss of the converter does not vary with the switching frequency. Figure 5.33 shows the split-up of the conduction loss across different components of the converter. It can be seen that the net conduction loss associated with the active components of the converter is much higher in comparison with the passive component's losses.

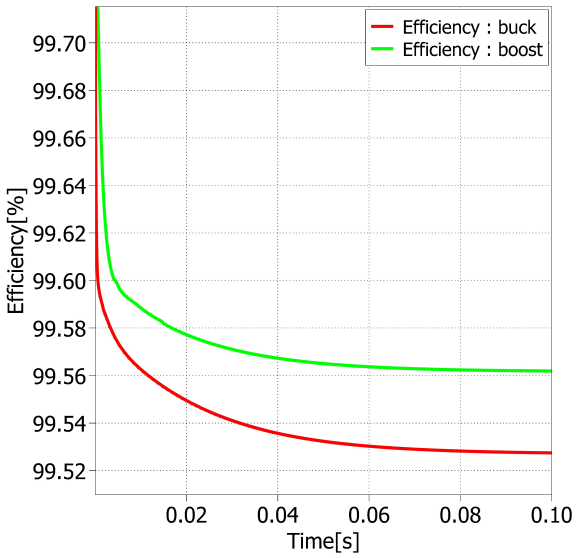

Figure 5.34: Comparison of converter's efficiency during boost and buck mode of operation

Figure 5.34 shows that the converter's efficiency at the defined operating point settles at 99.56% and 99.53% during the boost and buck operation, respectively. The slightly higher efficiency during the boost operation compared to the buck

operation can be explained by Figure 5.8. This shows that the MOSFET's junction temperature during the buck operation is higher than that of the boost operation. As a result, the net switching losses of the converter gets higher in the buck operation than in the boost operation.

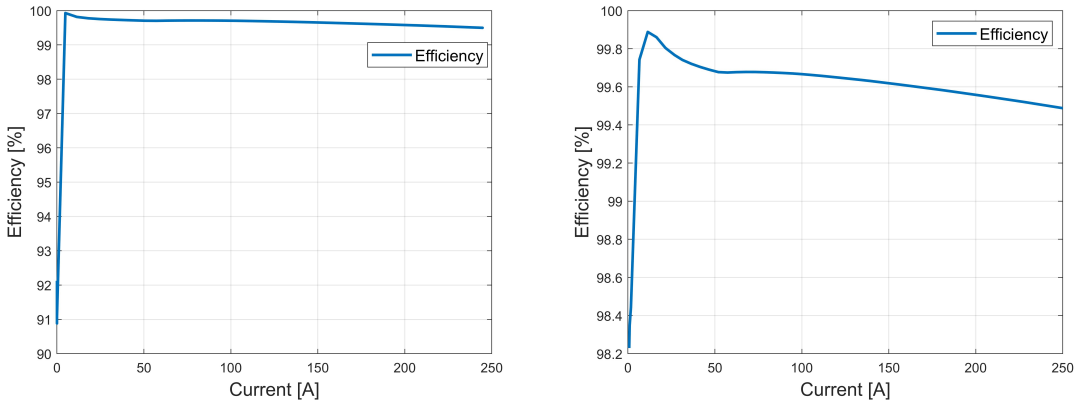

Figure 5.35: Comparison of four-phase interleaved buck/boost converter's efficiency with respect to load current a)during boost mode of operation and b)during buck mode of operation

Analysis of the converter's efficiency for change in the load current has been performed. Figure 5.35 displays the individual results of the analysis for the boost and buck operation separately. It can be concluded that the converter's efficiency is almost constant at 99.5% for change in the load current during both operations.

5.5.2 Dual Active Bridge converter

The major loss components in a three-phase DAB include the transformer's core loss & copper loss and the net switching loss & conduction loss of all the MOSFETs. The efficiency of the converter is calculated by (5.1). The net switching loss and conduction loss for each MOSFET are calculated in PLECS as described in section 3.5.1. The efficiency is calculated with an input voltage of 600 V and output voltage of 720 V for the converter. Figure 5.36 shows the net loss distribution of all the switches for different power levels.

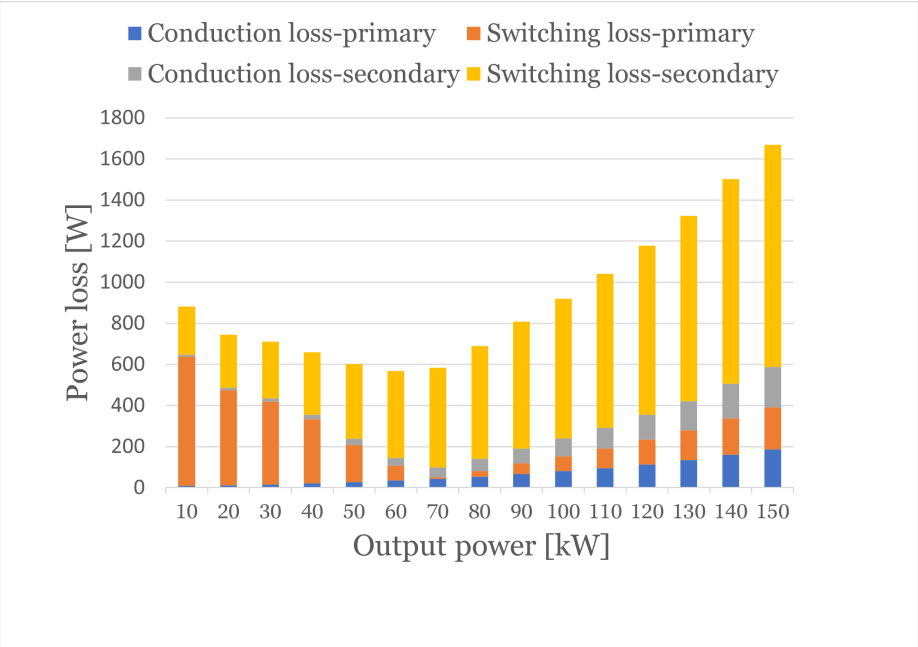

Figure 5.36: Net loss components associated with all the MOSFETs for various ouput power

The net conduction loss in primary and secondary side MOSFETs increase proportionally as the output power increases. This is because when the current rises, the conduction loss rises correspondingly.

5.5.2.1 Analysis of switching loss - secondary side MOSFET

The sum of the turn-on and turn-off losses for one switching period is the switching loss for the MOSFET. For an input voltage of 600 V, only the primary side switches undergo hard switching, as shown in figure 5.15. As a result, soft switching on the secondary side is achieved across the whole power range, i.e. no turn-on loss on the secondary side. Hence the total switching loss is contributed solely by turn-off loss for each MOSFET on the secondary side. As a result, the switching loss in the secondary side switches increases as the output power, as shown in figure 5.36. The turn off loss can be reduced by implementing a snubber circuit.

5.5.2.2 Analysis of switching loss - primary side MOSFET

The switching loss for primary-side switches reduces until 70 kW and increases after that. As shown in figure 5.15, hard switching occurs below 73.59 kW on the primary side and hence below 70 kW, the switching loss is due to turn-on and turn-off loss. Above 70 kW, the primary side switching loss is due to turn-off loss alone.

5.5.2.3 Analysis of transformer loss

As discussed in section 3.5.2, core loss and copper loss accounts for significant losses in the transformer. For the designed planar transformer in section 4.3, the core loss and winding loss are calculated for different output power of the converter. The

core loss is calculated based on (3.34), where the Steinmetz co-efficient are given in table 4.4. Flux density ($\hat{B}$) is calculated by,

$$\hat{B} = \frac{\phi}{A_e} \tag{5.3}$$

where A_e is the cross-sectional area of the transformer core and ϕ is calculated by (4.21). With an input voltage of 600 V and a frequency of 85 kHz, the core loss is calculated. Based on the PC board design, the calculated DC resistance is 3.29 mΩ and the winding loss associated with it calculated. Figure 5.37 shows the split up of copper loss and core loss of a single transformer for various output power.

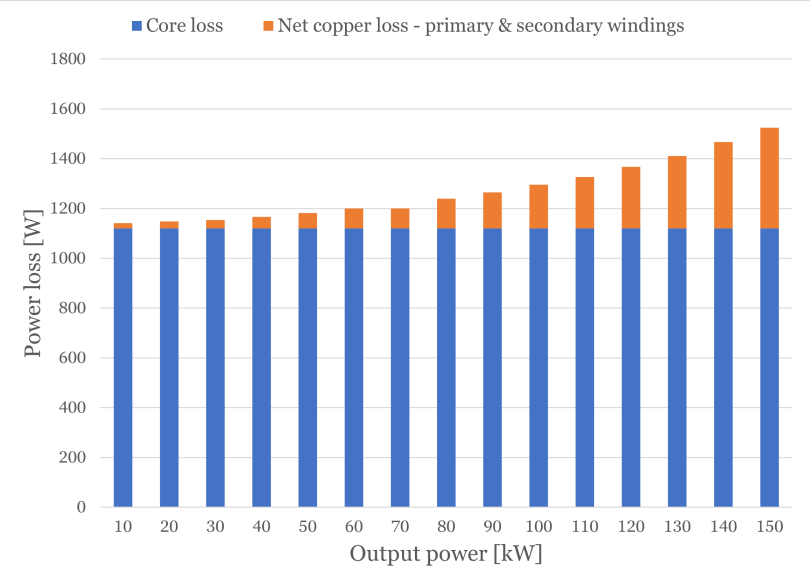

Figure 5.37: Split up of transformer loss for various output power

The core loss remains the same for the entire power range as the input voltage is unchanged. In contrast, the winding loss increases as the current increases. Figure 5.38 shows the overall efficiency of the designed three phase DAB for various output power. Below 70 kW, there is drastic reduction in the efficiency as the primary switches of the converter operates at hard switching. It can be concluded that the converter attains maximum efficiency of 96.1% at rated power.

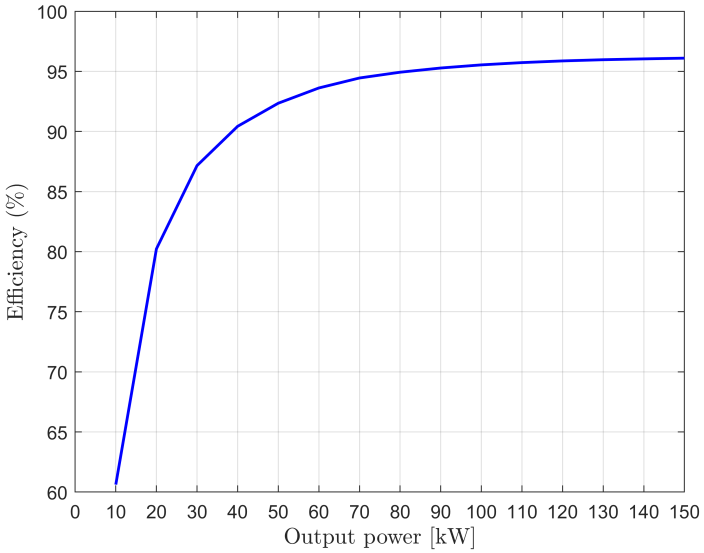

Figure 5.38: Efficiency of the three-phase DAB for various output power

6
Discussion

6.1 Comparison between isolated and non-isolated converter results

Realizing the characteristics between the four-phase interleaved buck/boost converter and the three-phase dual active bridge converter takes place. According to the design, both topologies have a voltage ripple of 1 V at the load battery side.

Based on the selection criteria defined in Section 2.1, soft switching is an essential feature for a DC-DC converter. From the analysis, it is clear that only the three-phase dual active bridge converter operates in the soft-switching technique. The four-phase interleaved buck/boost converter is a hard switching topology that requires additional soft switching circuits to be implemented. It increases cost and switching complexity. For rated power of 150 kW operation, the net switching loss of the DAB converter is approximately 3.5 times higher than the IBC converter. Despite the soft-switching operation, switching losses are higher in the DAB converter than in the IBC converter. This is because soft-switching occurs when the MOSFETs in the DAB converter are turned on, whereas hard switching turns the MOSFETs off. As a result, the soft-switching operation reduces turn-on losses alone, resulting in high turn off losses and high switching losses in the DAB converter.

The voltage stress of the MOSFETs is similar for both topologies. On the other hand, the current stress is higher in the DAB converter compared to the IBC converter. As high current flows through both the primary and secondary MOSFETs, the junction temperature of the MOSFET rises in the DAB converter compared to the IBC converter. Based on the findings, the IBC converter requires MOSFET with a comparatively lesser current rating, leading to the selection of a discrete SiC MOSFET that satisfies the stress requirement. As the current rating of the DAB converter MOSFET increases, a SiC half-bridge module that meets the stress requirement is chosen. Some of the disadvantages of using a half-bridge module are that it is expensive and occupies a comparatively large volume than the discrete MOSFET. The IBC converter uses a dual-loop controller to control these MOSFETs, and the DAB converter uses a power flow controller. The robustness and stability of these controllers can be seen from their response to the input variations.

The converter's efficiencies are plotted against the current and power level from the simulation. From the analysis, the efficiency of the IBC converter is comparatively

higher than the DAB converter for different power levels. The efficiency of the IBC converter and the DAB converter for the rated power operation of 150 kW is 99.56% and 96.1%, respectively. Nevertheless, the major disadvantage of the IBC converter is that it operates only when the voltage of the source battery is lower than the load battery's voltage. It operates either in the boost mode for positive power flow or buck mode for power reversal. So, the source voltage always needs to be lower than the load voltage for either the boost or buck mode to operate. The DAB converter, on the other hand, provides soft-switching operation of the MOSFETs up to 70 kW power operation of the converter for the selected switching frequency and the phase inductance. At the same time, the operation of the DAB converter is not affected by any parameter and provides continuous power flow irrespective of the soft-switching or hard-switching of the MOSFETs.

6.2 Sustainable Aspects

In this section, the sustainability aspects of this thesis work are explained in detail. The sustainability aspects of a DC-DC converter include an investigation of the materials and various components used that impact the environment. The literature study includes an investigation of the individual components as well as the construction of the converter. Various topologies have been investigated, and the selection of semiconductor materials and different components considers the environmental impact.

In the construction industry, electric equipment offers several benefits: reduced fuel costs, low carbon dioxide emission, and a safer environment with less noise pollution. For achieving high power availability for this equipment, bidirectional converters help supply power using a vehicle's battery. The operation of the selected converters and the generation of electricity for this equipment is designed to be environmentally friendly.

According to the literature review, converter with lower volume is taken into account for design purposes. Consequently, converters with reduced size decrease the component size, the PCB size and the number of components required per board. The reduction in the converter size reduces the amount of plastic waste generated during PCB fabrication and provides an advantage of occupying less space. Converters with improved efficiency are designed, thereby reducing the net loss in the application. As a result, the design of a converter with optimal behaviour helps the industries and the end-users.

6.3 Ethical Aspects

Based on the IEEE code of ethics [59], the isolated and the non-isolated converter topologies are designed and compared considering the ethical aspects of the con-

verter. This section contains a discussion of the three IEEE codes of ethics that have been followed.

The first code of ethics followed is "to be honest and realistic in stating claims or estimates based on available data, and to credit properly the contributions of others". For following this, proper research has been conducted on the designed converters, and the gathered facts support any claim regarding the design. Explanations regarding the converter's operation, strengths and weaknesses have been discussed. Simulation results are presented with practical data to help implement the prototype design in the hardware model.

The second code of ethics is "to improve the understanding of technology, its appropriate application, and potential consequences". For following this, literature studies on different technologies supporting the converters for interfacing the batteries are analysed. Selection criteria for selecting the best converter topology that handles various technical challenges are defined. Based on the analysis, converter topologies that provide enhanced technological support for this application has been selected.

The third code of ethics followed is "to avoid injuring others, their property, reputation, or employment by false or malicious actions, rumors or any other verbal or physical abuses". To follow this, before designing the converters, every assumption in deriving the topology is explained. In this way, proper knowledge of the working of the converter can be achieved. This provides opportunities regarding different parameter changes for performance improvement in the case of developing a hardware model.

7
Conclusion

The purpose of this thesis is to identify the most promising converter topology that can be used as the battery charger. After the qualitative study of different bi-directional DC-DC converters, two converters, namely, a three-phase dual active bridge and a four-phase interleaved buck/boost converter, are selected.

For a nominal voltage of 600 V and an output voltage of 720 V, the selected converters are designed for a rated power of 150 kW. For the three-phase DAB, three single-phase planar transformers are designed, including selecting core material and winding parameters based on the power handling capability. A phase shift controller is designed for the three-phase DAB to control the power transfer, and a dual loop controller with voltage control on the outer loop and current control on the inner loop is designed for the four-phase interleaved buck/boost converter. The designed three-phase DAB and the four-phase interleaved buck/boost is implemented and simulated in PLECS along with the controller.

In PLECS, the semiconductor loss and the conduction loss are calculated based on the thermal description provided by the manufacturer. Whereas the transformer losses are calculated analytically, and the result showed that the core loss accounts for 73% of the total loss at the rated power of 150 kW. The soft switching boundaries are calculated for the three-phase DAB and found that below 70 kW, hard switching occurs on the primary side of the switches leading to reduced efficiency under light load conditions. Comparing the loss components, the four-phase interleaved buck/-boost converter shows higher efficiency for the entire power range with an efficiency of 99.56% at rated power. On the other hand, the three-phase DAB has an efficiency of 96.1% at 150 kW.

It is noticeable that the interleaved buck/boost converter is highly dependent on the input and output voltage, i.e. the converter operates only when the source battery's voltage is lower than the load battery's. This disadvantage is mitigated in three-phase DAB, as the converter can operate at any operating point with reduced efficiency for light load conditions. Comparing the volume consumption, the three-phase DAB is relatively compact as the interleaved buck/boost converter consumes a higher volume due to its large inductance. Hence, the three-phase DAB is the best option for this application due to its reliability and volume consumption. The three-phase DAB is designed for a maximum power of 250 kW, but the planar transformer can handle a maximum power of 155 kW, thus limiting the overall rating of the converter.

7.1 Future work

- An optimised planar transformer can be designed with the needed phase inductance as the leakage inductance, thereby eliminating an external inductor for power transfer.
- A finite element method (FEM) can be used for simulating the planar transformer so that an accurate loss component can be obtained, including hysteresis and eddy current loss for various loads.
- A proper heat sink design and thermal modelling must be carried out using FEM simulation before implementing the hardware.
- The snubber circuit can be implemented to increase the efficiency of the three-phase DAB, which reduces the turn-off loss.
- The design of a planar inductor for the four-phase interleaved buck/boost converter can be carried out. As the planar inductor increases, the power density and a comparison can be made between the three-phase DAB and four-phase interleaved buck/boost converter.
- To get more accuracy during transients, an RC battery model can be implemented instead of R only battery model.

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A

Dual loop controller parameters calculation

This appendix contains the control parameter calculation for the 4-phase interleaved buck/boost converter.

A.1 Design of current controller parameters

The current controller is a PI controller designed to control inductor current. It contains an active damping term and anti-windup term to get designed along with the gain of proportional and integrator part of the PI controller. Series RL circuit accounts for the design of PI current controller in the case of boost and buck mode separately.

A.1.1 Design of boost current controller parameters

The cutoff frequency for designing the boost current controller is $\alpha_{cfi} = 1.731475 \times 10^4$ rad/sec. Based on the derivation, the gain of proportional and integrator parts of the controller are calculated as

$$k_{pfi} = \alpha_{cfi} \times L_{ph} = 3.4195 \tag{A.1}$$

$$k_{ifi} = \alpha_{cfi}^2 \times L_{ph} = 59207.61 \tag{A.2}$$

Similarly, the active damping term and anti-windup term for control purposes can be found by,

$$R_{afi} = k_{pfi} - \left(R_{Lk} + R_{s(on)} + (1-D)\frac{RR_{Cout}}{R + R_{Cout}} \right) = 3.4003 \tag{A.3}$$

$$k_{awfi} = \frac{1}{k_{pfi}} = 0.2924 \tag{A.4}$$

A.1.2 Design of buck current controller parameters

The cutoff frequency for designing the buck current controller is $\alpha_{cbi} = 5.39921 \times 10^4$ rad/sec. The derivation for calculating the control parameters is similar to that

of the boost controller. According to the derivation, the controller gains can be obtained as follows

$$k_{pbi} = \alpha_{cbi} \times L_{ph} = 10.6629 \tag{A.5}$$

$$k_{ibi} = k_{pbi} \times \frac{\alpha_{cbi}}{n} = 143928.0885 \tag{A.6}$$

The active damping term and anti-windup term for the buck case can be derived as

$$R_{abi} = k_{pbi} - \left(R_{L_k} + R_{s(on)} + \frac{R_{in}R_{Cin}}{R_{in} + R_{Cin}}\right) = 10.3843 \tag{A.7}$$

$$k_{awbi} = \frac{1}{k_{pbi}} = 0.0938 \tag{A.8}$$

A.2 Design of voltage controller parameters

The voltage controller is a PI controller designed to control the input and output voltage of the converter. It contains proportional and integrator gains to be designed along with the anti-windup term. A parallel RC circuit is taken into account for deriving the control parameters for the PI voltage controller.

A.2.1 Design of boost voltage controller parameters

During boost operation, the boost voltage controller regulates the converter's output voltage of the converter. Obtained cutoff frequency is $\alpha_{cfv} = 2.364658{\times}10^4$ rad/sec, and from this, the control parameters of the PI controller can be derived as

$$k_{pfv} = \alpha_{cfv} \times C_{out} \times \left(\frac{R + R_{Cout}}{(1-D)R}\right) = 1.4369 \tag{A.9}$$

$$k_{ifv} = \frac{\alpha_{cfv}}{(1-D)R} = 8231.5113 \tag{A.10}$$

$$k_{awfv} = \frac{1}{k_{pfv}} = 0.6959 \tag{A.11}$$

A.2.2 Design of buck voltage controller parameters

The buck voltage controller regulates the converter's input voltage when it is operating in buck mode. The effect of ESR is neglected due to its minor impact on the controller performance. The obtained cutoff frequency is $\alpha_{cbv} = 4.172594{\times}10^5$ rad/sec, and the PI controller control parameters can be calculated as follows:

$$k_{pbv} = \alpha_{cbv} \times C_{in} = 0.4166 \tag{A.12}$$

$$k_{ibv} = \frac{\alpha_{cbv}}{R_{in}} = 173858.0833 \tag{A.13}$$

$$k_{awbv} = \frac{1}{k_{pbv}} = 2.4 \tag{A.14}$$

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