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A Phase-Locked GaN Oscillator Using a Mechanically Tunable Cavity Resonator

Master's thesis in Embedded Electronic System Design

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Abstract

The demand for wireless data transfer is growing rapidly, and local oscillator phase noise has been identified as a performance limiting factor in radio communication systems. Two ways to reduce phase noise are to use a high power amplifier- and a high quality factor (Q) resonator in the oscillator design, such as a gallium nitride high electron mobility transistor (GaN HEMT) amplifier and a metallic cavity resonator. A free-running cavity oscillator is however a poor choice for use as a local oscillator, since they exhibit poor thermal frequency stability. This thesis presents the design and characterization of a phase-locked GaN HEMT cavity oscillator, utilizing mechanical tuning of the cavity as well as electronic tuning using a varactor.

The prototype oscillator works, but performed worse than expected with a phase noise of $-103.7\,\mathrm{dB}$ at $100\,\mathrm{kHz}$ offset, measured at the best operating point. The oscillation frequency of the oscillator was tunable from $11.51\,\mathrm{GHz}$ to $12.29\,\mathrm{GHz}$. Furthermore, the phase locked loop (PLL) was not able to lock the phase of the oscillator to a reference due to stability issues. Theoretical evidence that low phase noise can be achieved using this method is however presented, and reasons for the poor performance of the prototype are discussed.

Keywords: Cavity oscillator, Phase noise, Phase locked loop, GaN HEMT

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Alexander Oxklint, Gothenburg, June 2022

Contents

1

Introduction

In 1992 the global internet traffic was around 100 GB per day, and by 2017 that figure had risen to over four billion GB per day [1]. This rapid growth in traffic is expected to continue as the number of connected devices- and demand for data-intensive services increase [2]. Furthermore, wireless and mobile devices are expected to account for a large majority of all internet traffic looking forward [2]. This puts high requirements on the communication network infrastructure, as high speeds are demanded wirelessly with wide coverage. The development of 5G networks is a clear response to this issue, which will further require high speed wireless communication as the small cell size necessitates a partially wireless communication infrastructure as well [3]. Efficient use of wireless bandwidth in communications systems will therefore play an important role in maximizing network throughput.

In wireless communication systems, accurate local oscillators (LOs) are commonly used to convert between intermediate frequency signals and radio frequency signals for transmission over the air. An ideal oscillator should produce a single frequency at its output, but any real oscillator will also produce phase noise, widening the spectral linewidth of the output. This results in conversion to- or from undesired nearby frequencies, which introduces added uncertainty in the detection of digitally modulated signals and requires greater channel spacing. Phase noise furthermore negatively impacts techniques such as orthogonal frequency division multiplexing (OFDM) [4] and multiple input multiple output (MIMO) systems [5]. In millimeter-wave (mm-wave) and sub-mm-wave communication systems, LO phase noise far from the carrier frequency is observed as one of the major performance limiting factors [6, 7]. Considering that the 5G network will operate in the mm-wave band and utilize techniques such as OFDM and MIMO [8], it is apparent that reduction of phase noise in oscillators will be essential for reaching higher wireless data transfer rates.

Two possible methods to reduce oscillator phase noise are to use a resonator with a higher Q or to increase the power in the resonator, where the former determines the phase white frequency modulation (FM) noise corner and the latter reduces the white phase noise [9]. It is also beneficial to use a high fundamental frequency oscillator, since frequency multiplication degrades phase noise both near and far from the carrier frequency [6]. One way to achieve all of this is by constructing an oscillator using a metallic cavity resonator and a high-power GaN HEMT amplifier, since it is possible to construct cavity resonators with a high quality factor at a high fundamental frequency, and a high-power amplifier can lower the white phase

noise floor. Free-running cavity oscillators are however not well suited for use as LO frequency sources, since they have poor temperature stability and therefore drift in frequency.

1.1 Thesis Aim and Contribution

The aim of this thesis project was to design and construct a low phase noise frequency synthesizer by phase-locking a mechanically tunable cavity oscillator to a lower frequency reference oscillator in a PLL, such that it could be used as an LO in a radio. The output of the synthesizer should then acquire the long term frequency stability- and close-in phase noise of the reference oscillator, while maintaining the low far-out phase noise of the cavity oscillator. The oscillation frequency of the cavity oscillator should be adjusted coarsely by moving a perturbation inside the cavity with a motor, and finely with a varactor between the cavity and reflection amplifier.

To limit the scope of the project, available hardware for the mechanically tunable cavity resonator, oscillator amplifier, varactor, phase detector, and frequency divider was used. The cavity resonator used was the result of a previous thesis project [10], and a suitable high-power GaN HEMT reflection amplifier with an integrated varactor was provided by Chalmers University of Technology. An LMX2820 [11] was used to realize both the phase detector and frequency divider, limiting the design to a phase frequency detector with a charge pump and a digital delta-sigma modulated divider.

The contribution of this thesis is the system level design of a phase-locked cavity oscillator, optimized for low phase noise and suitable for use as an LO synthesizer in 5G communication infrastructure. Models for predicting phase noise in PLLs are presented and used to design the PLL control system. Theory on resonators and microwave oscillators is also presented and used, in conjunction with simulations, to optimize the phase noise of the cavity oscillator. Finally, suggestions and important considerations for anyone attempting to construct a similar synthesizer are given.

2

Theory

2.1 Phase Noise

The instantaneous output signal, $V(t)$, of an ideal oscillator with amplitude V_0 and frequency f_0 is given by

$$V(t) = V_0 \sin(2\pi f_0 t) \tag{2.1}$$

which yields a spectrum consisting of only two impulses at $\pm f_0$ in the frequency domain. In practice however, all oscillators are affected by random fluctuations in amplitude and phase. The instantaneous output of a practical oscillator can therefore be written as

$$V(t) = [V_0 + \varepsilon(t)] \sin[2\pi f_0 t + \phi(t)] \tag{2.2}$$

where $\phi(t)$ and $\varepsilon(t)$ are random processes that denote the phase- and amplitude fluctuations respectively. If the root-mean-square value of the phase fluctuations, ϕ_{rms}, is much smaller than one radian, which would be expected in a high quality oscillator, the power spectrum $S_V(f)$ of $V(t)$ may be approximated as [12]

$$S_V(f) \approx \frac{V_0^2}{2}[\delta(f - f_0) + S_\phi^{(TS)}(f - f_0) + S_A^{(TS)}(f - f_0)] \tag{2.3}$$

where $S_\phi^{(TS)}(f)$ is the two-sided power spectrum of $\phi(t)$ and $S_A^{(TS)}(f)$ is the two-sided power spectrum of the fractional amplitude fluctuations $A(t) = \varepsilon(t)/V_0$. Ignoring amplitude fluctuations, the phase fluctuations therefore effectively modulate the carrier to form noise sidebands as shown in Figure 2.1. An exact relation between phase fluctuation and $S_V(f)$ does exist, but it is not easily used in practice [12].

Historically, phase noise has been defined as the noise power in 1 Hz bandwidth at a frequency offset f from the carrier divided by the carrier power, and is denoted $\mathcal{L}(f)$ with units dBc/Hz [13]. Using this definition, Equation (2.3) can be used to approximate phase noise as

$$\mathcal{L}(f) \approx \frac{1}{2} S_\phi(f) \tag{2.4}$$

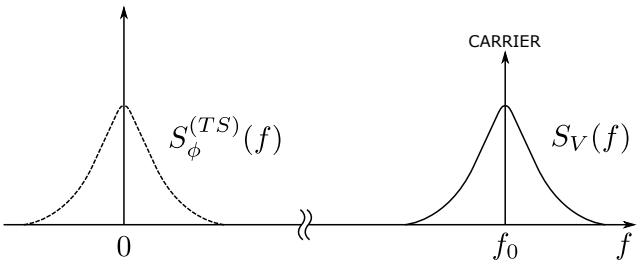

Figure 2.1: Illustration of how phase noise modulates the carrier frequency.

if amplitude fluctuation is negligible and $\phi_{\text{rms}} \ll 1$, where $S_\phi(f)$ is the one-sided power spectrum of $\phi(t)$. Because of the sensitivity to amplitude fluctuation and ϕ_{rms}, phase noise was redefined in the IEEE Standard 1139 as [14]

$$\mathcal{L}(f) \equiv \frac{1}{2} S_\phi(f) \tag{2.5}$$

This definition avoids ambiguity when phase fluctuations are significant.

2.1.1 Phase Noise Modeling

In Equation (2.2) and the subsequent handling of phase noise, it was assumed that the random phase fluctuation was a stationary random process. This assumption is false for physical oscillators in general, which means that an autocorrelation function and power spectrum of the phase fluctuation is not formally defined [15]. Slow drifts such as aging of components affect stationarity in a strict sense, but have little impact on phase noise at reasonable offset frequencies and should not be used to dismiss the assumption of stationarity [12]. More concerning is cyclo-stationary phenomena that can arise when the statistical properties of noise is dependent on the operating point of a device [16]. For example, a definitive increase in upconversion of flicker noise has been observed in a GaN HEMT based oscillator when cyclo-stationary effects are taken into account in the modeling of noise sources [17].

The usefulness of a model is, however, not necessarily dependent on the level to which it mimics the properties of a real system. Simple models that can make accurate predictions in a limited context are often preferred over more complex models whenever the application falls within those limits. In phase noise analysis, power-law spectral density models have proven useful [14], in which the noise spectrum is described by

$$S_\phi(f) = \sum_\alpha h_\alpha f^\alpha \tag{2.6}$$

where alpha typically ranges from -4 to 0 or a smaller range, and h_α are fitting-constants for each α. This essentially models phase noise as a set of independent noise processes that piecewise dominate the noise spectrum asymptotically with different slopes. A prominent example of a power-law spectral density model for oscillator phase noise is the one presented by Leeson [9], which is a semi-empirical

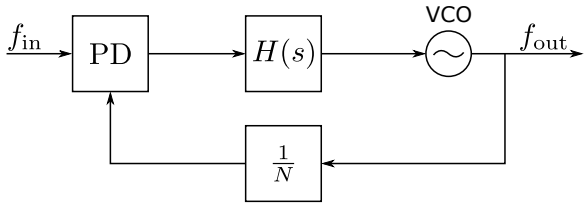

Figure 2.2: Basic building blocks of a PLL. The block labeled PD is the phase detector and $H(s)$ is the loop filter transfer function.

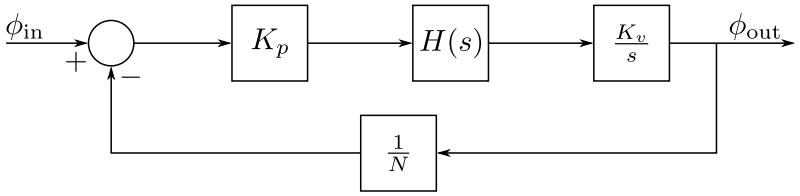

Figure 2.3: Block diagram of an ideal linear model of a PLL.

model that can be fitted well to oscillator phase noise even though it assumes phase fluctuation is a stationary process. Leeson's oscillator phase noise model is examined in greater detain in section 2.3.4.

2.2 Phase-Locked Loops

A PLL is an automatic control system that regulates the phase of a process to the phase of a reference input signal. When used for frequency synthesis, they typically consist of at least a phase detector, loop filter, voltage controlled oscillator (VCO), and a frequency divider, as shown in Figure 2.2. The output phase is compared to the phase of the input by the phase detector and a signal proportional to their difference is produced. This signal is subsequently filtered in the loop filter and used to control the VCO. The output frequency and phase is scaled by the frequency divider before it is fed back to allow for a difference in frequency between the input and output. A common linear model of such a system is shown in Figure 2.3 and has a transfer characteristic given by

$$\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{NK_pK_vH(s)}{Ns + K_pK_vH(s)} \tag{2.7}$$

where K_p is the gain of the phase detector, K_v is the gain of the VCO, $H(s)$ is the loop filter transfer function, and N is the feedback division factor. The use of a linear model allows for easy analysis of system stability and behavior with linear control theory.

The superposition property of linear systems furthermore makes it possible to model noise as additive noise sources, and analyze their impact on the output signal separately. Figure 2.4 shows the linear model with additive noise sources, where $S_{\phi,r}$ is the noise power spectrum of the input reference phase, $S_{\phi,p}$ is the noise power spectrum of the phase detector, $S_{\phi,l}$ is the noise power spectrum of the loop filter,

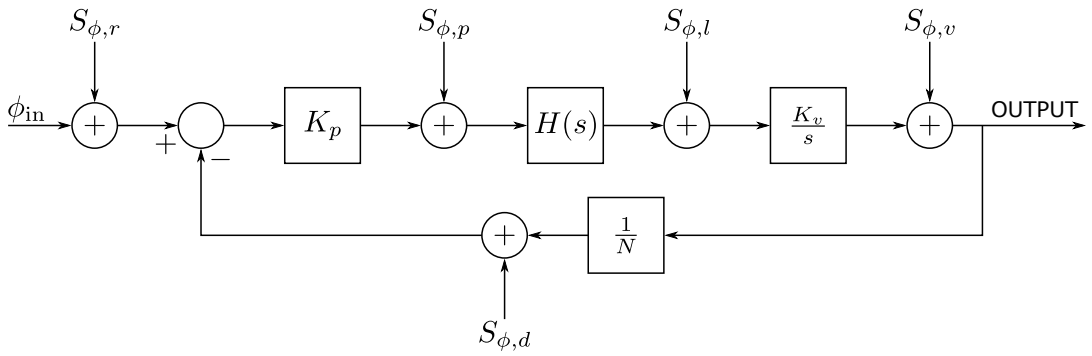

Figure 2.4: Block diagram of a linear model of a PLL with additive noise sources for each block.

$S_{\phi,v}$ is the noise power spectrum of the VCO, and $S_{\phi,d}$ is the noise power spectrum of the frequency divider. Describing the noise sources using power spectra is beneficial since the output power spectrum, $S_y(f)$, of a linear system is given by

$$S_y(f) = S_x(f)\,|G(f)|^2 \tag{2.8}$$

where $S_x(f)$ is the input power spectrum and $G(f)$ is the system's transfer function. Using this equation to find the total output noise power spectrum of the model gives

$$\begin{aligned} S_{\phi,\text{out}}(f) = {} & S_{\phi,r}(f)\left|\frac{NK_pK_vH(s)}{Ns+K_pK_vH(s)}\right|^2 + S_{\phi,p}(f)\left|\frac{NK_vH(s)}{Ns+K_pK_vH(s)}\right|^2 \\ & + S_{\phi,l}(f)\left|\frac{NK_v}{Ns+K_pK_vH(s)}\right|^2 + S_{\phi,v}(f)\left|\frac{Ns}{Ns+K_pK_vH(s)}\right|^2 \\ & + S_{\phi,d}(f)\left|\frac{NK_pK_vH(s)}{Ns+K_pK_vH(s)}\right|^2 \end{aligned} \tag{2.9}$$

where $s = j2\pi f$. Provided that the power spectrum of each noise source is known, this equation can be used during the design of the control system to optimize for noise performance. It should also be noted that all noise sources are suppressed for large values of s except for the VCO noise, and correspondingly the VCO noise is suppressed for small values of s. This means that the design parameters can be used to decide at which frequency the output noise should be decoupled from the input noise. The remaining part of this section will describe the components of a PLL and their noise properties in more detail.

2.2.1 Phase Detector

One of the most popular phase detector implementations in modern PLLs is the sequential-logic phase-frequency detector (PFD) in combination with a charge pump. Compared to many other implementations, it offers a wider tracking range, frequency aided acquisition, low cost, and zero residual phase error without active

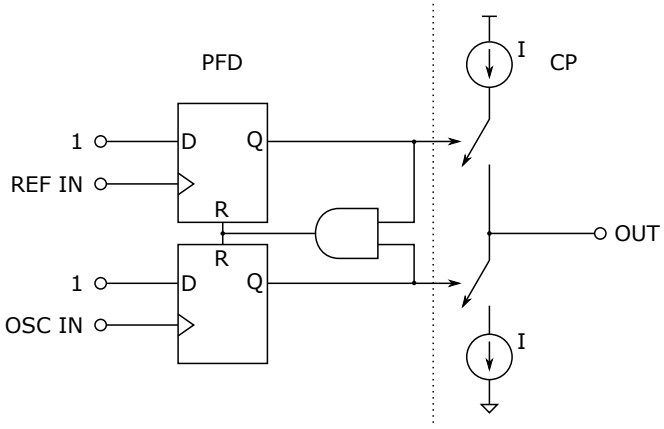

Figure 2.5: Illustration of a simple PFD circuit and charge pump.

loop filters [18, 19]. Figure 2.5 shows a common implementation of a PFD and charge pump. The circuit will produce either positive or negative current pulses on the output, depending on the phase relationship between the inputs, but this relationship is best described separately for operation under a phase-locked condition and a frequency acquisition condition.

2.2.1.1 Phase-Locked Condition

In the phase-locked condition, both inputs to the PFD have the same frequency, and the PLL only has to compensate for small disturbances and slow drifts in the controlled oscillator. Assuming the oscillator has been disturbed from the locked condition such that its phase lags the reference as shown in Figure 2.6a, each rising edge of the reference will close the top switch of the charge pump and the output will start sourcing a current. When the lagging edge of the oscillator arrives it will momentarily activate the other switch, but the AND gate also activates, causing both flip-flops to reset and the output to become high impedance. This cycle repeats, yielding a series of current pulses on the output where the pulse width is proportional to the phase error.

It is important to note that, because of the switching, the PFD and charge pump is a time-varying network that cannot be directly analyzed using transfer functions. If, however, the loop filter bandwidth is much lower than the frequency of the current pulses, the per-cycle behavior can be ignored, and the average behavior may instead be considered [18]. Denoting the pump current as I_p and the input phase error as ϕ_e, the average output current in the phase-locked condition is given by [18]

$$i_{\text{out}} = \frac{I_p \phi_e}{2\pi} \tag{2.10}$$

Using this equation, the phase detector gain, K_p, in Equation (2.7) can be identified as

$$K_p = \frac{I_p}{2\pi} \tag{2.11}$$

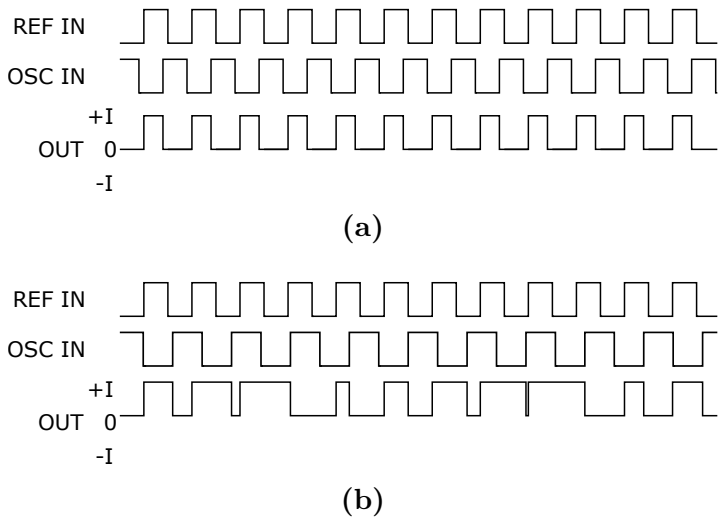

Figure 2.6: Examples of PFD charge pump outputs when the PFD has been disturbed from a phase-locked condition (a) and in the frequency acquisition condition (b). Note that the average output current is proportional to the phase difference in (a), but not in (b). It is still, however, indicated in (b) whether the oscillator frequency is higher or lower than the reference frequency.

with units A/rad. Note also that this makes the current-to-voltage transfer of the loop filter the important characteristic, since the VCO must be controlled with a voltage.

2.2.1.2 Frequency Acquisition Condition

In the frequency acquisition condition, the frequencies on the inputs of the PFD are not the same. This would typically occur when the PLL is first powered on or when the feedback division factor is changed. The principal of operation remains the same as in the phase-locked condition, but the average output current is no longer proportional to the phase error. Figure 2.6b shows an example where the oscillator has a lower frequency than the reference. While the relation to phase error is lost, it is important to note that the average output current still indicates whether the oscillator has a higher- or lower frequency compared to the reference. As long as there is integration in the loop filter, this means that no extra circuitry is needed to provide frequency acquisition. The transient response of the system during frequency acquisition, however, can not be described with a linear model and must be analyzed separately. Since rapid frequency acquisition is not the goal of this project, methods to analyze and optimize it will not be investigated.

2.2.1.3 Noise Properties

The additive noise caused by the PFD is highly dependent on implementation, which makes modeling difficult when the implementation details are not known. If only white noise is considered, and no device noise sources, the white noise power can however be shown to be proportional to $f_{\text{in}}N^2$ [20]. It has also been shown that the charge pump contributes to white noise level inversely proportional to the pump

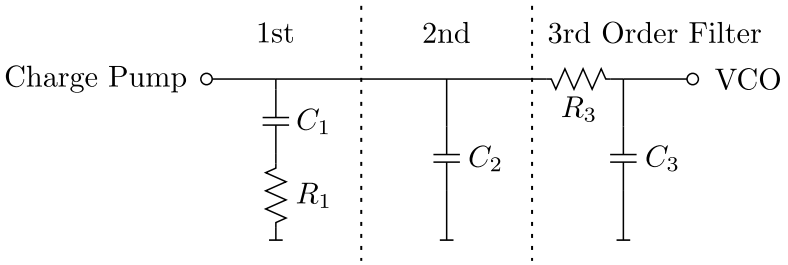

Figure 2.7: Common implementation of loop filter for PLLs utilizing charge pumps. Taking the output at one of the dashed lines reduces the order of the filter.

current I_p [21]. A semi-empirical model of the PFD white noise contribution can thus be written as

$$S_{\phi,p}(f) = \alpha \frac{f_{\text{in}} N^2}{I_p} \tag{2.12}$$

where α must be fitted from experimental data. Due to the N^2 factor, white noise in the PFD is minimized for a given output frequency when the reference frequency is as high as possible. It has however been suggested that additive noise is negligible in a well-designed PFD [19], and it is possible that PFD noise is masked by other noise sources. If that is the case, it will have no impact on the output phase noise and can be removed from the analysis.

Since the output of the charge pump is a current pulse train, noise in the form of spurs must nevertheless be accounted for in the design of a PLL system. Spurs occur at the reference frequency and its multiples and must be suppressed by the loop filter, but the exact level of the spurs again depends on the PFD implementation. Since the switches in the charge pump have finite turn-on and turn-off time, the PFD gain diminishes close to zero phase error. It is common to avoid this dead-zone by either introducing a leakage current on the charge pump output, or a delay in the PFD reset path, and the spur magnitudes are dependent on these values [22, 23].

2.2.2 Loop Filter

As is made apparent by Equations (2.7) and (2.9), the loop filter has significant impact on system performance. In a system utilizing a charge pump, a loop filter is also necessary to convert the charge pump current to a voltage for the VCO. Passive filters are often used in combination with a charge pump, since no active components are necessary to realize good integrators. Figure 2.7 shows a very common implementation of loop filters which result in either a 2nd, 3rd, or 4th order system. Note that the system order is one greater than the loop filter order due to the ideal integration of phase by the VCO. The transfer function of the loop filter for a 2nd order system is simply the complex impedance of the network and can be written as

$$Z_{\text{1st order}} = \frac{s\tau_1 + 1}{sC_1} \tag{2.13}$$

where $\tau_1 = R_1C_1$. The single pole of this filter is located at the origin. If $H(s)$ in Equation (2.7) is replaced with $Z_{\text{1st order}}$, the complete system transfer may be described as

$$\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{sR_1K + \dfrac{K}{C_1}}{s^2 + s\dfrac{R_1K}{N} + \dfrac{K}{NC_1}} \tag{2.14}$$

where $K = K_pK_v$. In this form, a natural frequency and damping factor of the loop can be identified as $\omega_n = \sqrt{K/NC_1}$ and $\zeta = \tau_1\omega_n/2$. For positive K, the second order loop is therefore inherently stable. When higher order loops are used this is not the case, and stability analysis is required. Theory on such analysis is given in Section 2.4. The loop filter- and system transfer functions for 3rd and 4th order systems are given in Appendix A.1.

2.2.2.1 Noise Properties

The thermal noise of the resistors in the loop filter can severely degrade phase noise if care is not taken in the filter design. In order to model the resistor thermal noise in a third-order filter, additive voltage noise sources may be added to the filter circuit as shown in Figure 2.8. The transfer from each noise source to the output may be considered separately, and the transfer function from V_{R1} to the output can then be written as

$$G_{R1}(s) = \left(\frac{\dfrac{s\tau_3 + 1}{s^2C_2\tau_3 + s(C_2 + C_3)}}{\dfrac{s\tau_3 + 1}{s^2C_2\tau_3 + s(C_2 + C_3)} + \dfrac{s\tau_1 + 1}{sC_1}} \right) \left(\frac{1}{s\tau_3 + 1} \right) \tag{2.15}$$

where $\tau_1 = R_1C_1$ and $\tau_3 = R_3C_3$. Similarly, the transfer function from V_{R3} to the output may be written as

$$G_{R3}(s) = \frac{\dfrac{1}{sC_3}}{\dfrac{s\tau_1 + 1}{s^2C_2\tau_1 + s(C_2 + C_1)} + \dfrac{s\tau_3 + 1}{sC_3}} \tag{2.16}$$

Finally, the power spectral density of the voltage noise at the VCO input, $S_{\phi,l}$, can be computed by multiplying the power spectral densities of the noise sources with their respective power transfer functions, yielding the expression

$$S_{\phi,l}(f) = 2kT(R_1 \left|G_{R1}(j2\pi f)\right|^2 + R_3 \left|G_{R3}(j2\pi f)\right|^2) \tag{2.17}$$

where k is Boltzmann's constant and T is temperature.

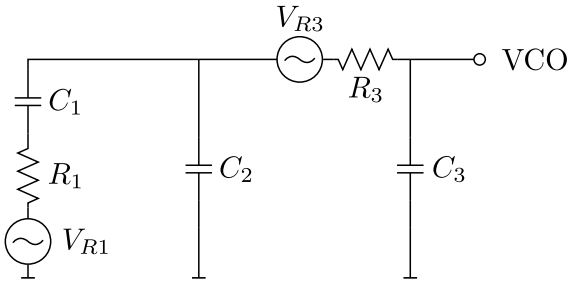

Figure 2.8: Loop filter with resistor thermal noise sources included.

2.2.3 Frequency Divider

The frequency divider in the control loop feedback path is used to set the output frequency of the PLL. For synthesizer applications, digital frequency dividers are most commonly used, since they can provide large division ratios and are easily made programmable. A drawback compared to their analog counterpart is that they often introduce more noise, but the benefits outweigh the additional noise in most applications [19]. For a PLL as shown in Figure 2.2, the output frequency is given by

$$f_{\text{out}} = N f_{\text{in}} \tag{2.18}$$

In practice, another divider is often placed in the input path so that the reference signal may be divided by a division factor R. The output frequency is then determined by

$$f_{\text{out}} = \frac{N}{R} f_{\text{in}} \tag{2.19}$$

This allows for higher resolution in the output frequency, but may require large values of N and R.

Digital dividers are commonly implemented using a combination of prescalers and counters to provide a large range of integer- and fractional values for N. Fractional divider are implemented by alternating between division ratios to produce an intermediate ratio on average, and often employ Σ-Δ modulation to do so. As a result they produce more noise compared to integer dividers, spurs in particular [24], but allows for smaller values of N for a given frequency resolution. Looking at Equation (2.9), it becomes apparent that minimizing N is highly beneficial for noise transfer. At very low frequencies, the equation may be approximated as

$$S_{\phi,\text{out}}(f) = \left(N^2\right)\left[S_{\phi,r}(f) + S_{\phi,p}(f)\frac{1}{K_p^2} + S_{\phi,l}(f)\left|\frac{1}{K_p H(j2\pi f)}\right|^2 + S_{\phi,d}(f)\right] \tag{2.20}$$

This shows that noise power transfer from the reference, phase detector, and divider is proportional to N^2 for low frequencies. Use of fractional dividers can therefore improve noise performance due to a smaller value of N being required for a given

frequency resolution. At very high frequencies the output noise instead becomes equal to the VCO noise, meaning that the impact of large N values mostly affects the phase noise close to the carrier.

2.2.3.1 Noise Properties

An ideal frequency divider with division ratio N reduces phase noise from input to output by $20\log(N)$, which is reflected by Equation (2.7). The additive noise of a digital frequency divider is less straight forward to describe, particularly for fractional Σ-Δ dividers, since they are time-varying and discrete. Fortunately, an accurate noise power spectral density model of fractional Σ-Δ dividers with a multi-stage noise shaping (MASH) structure, which this thesis intends to use, exists. Assuming white quantization noise in the Σ-Δ modulator, it may be described as [21, 25]

$$S_{\phi,d}(f) = \frac{1}{12f_{\text{ref}}^2}(2\pi)^2\left[2\sin\left(\frac{\pi f}{f_{\text{ref}}}\right)\right]^{2(m-1)} \tag{2.21}$$

where f_{ref} is the reference frequency and m is the order of the Σ-Δ modulator. It should be noted that the model only describes the impact of the Σ-Δ quantization noise and does not capture spurs caused by the divider.

2.2.4 VCO and Reference Oscillator

While theory on oscillators is covered more extensively in Section 2.3, some comments specific to their application in PLLs can be made. As described in Section 2.2.3, the VCO dominates the phase noise at high offset frequencies, beyond the loop bandwidth, and other components dominate at low offset frequencies, with a transition in between. This means that slow drifts in the VCO output phase or frequency will be corrected by the control loop, and long term frequency stability instead depends on the stability of the reference. In a system where the VCO is implemented with a cavity oscillator this is highly beneficial, since thermal expansion makes cavity oscillators prone to slowly drift in frequency, whereas it has excellent phase noise figures at higher offset frequencies. The reference oscillator on the other hand can be made much less sensitive to environmental conditions and aging. The phase noise due to random phase fluctuation in both the reference oscillator and VCO may be described using the model presented in Section 2.3.

2.3 Oscillators

The controllable oscillator is a central building block in any PLL, and its performance has significant impact on phase noise in synthesizer applications. Equation (2.9) shows that there is no mechanism in the PLL control loop that reduces the phase noise of the oscillator beyond the loop bandwidth. Careful consideration in the design of the oscillator is therefore required, and an accurate oscillator model is furthermore required in the design of the control loop.

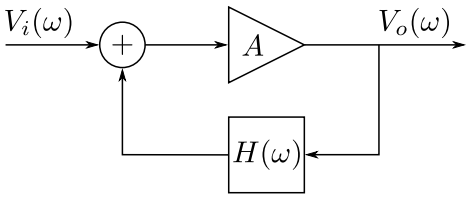

Figure 2.9: Block diagram of a linear feedback oscillator model.

2.3.1 Linear Feedback Oscillator Model

The simplest model that succeeds in describing the operation of an oscillator is the linear feedback model. The output of an amplifier with gain $A(\omega)$ is then fed back to the amplifier input through a frequency selective filter $H(\omega)$, as shown in Figure 2.9. The transfer from input to output of such a model is given by

$$\frac{V_o(\omega)}{V_i(\omega)} = \frac{A(\omega)}{1 - A(\omega)H(\omega)} \tag{2.22}$$

If there exists a frequency for which $A(\omega)H(\omega) = 1$, the system can oscillate at that frequency even if $V_i(\omega)$ is zero. This is called the Barkhausen criteria and is typically expressed in polar form as

$$|A(\omega)H(\omega)| = 1 \tag{2.23a}$$
$$\angle A(\omega)H(\omega) = 2\pi n, \quad n \in \mathbb{Z} \tag{2.23b}$$

Intuitively, Equation (2.23a) implies that the amplifier must compensate for any losses in the filter and Equation (2.23b) implies that the input and output must be in phase. These conditions are however not sufficient to start the oscillation from rest, since it only implies marginal stability. Practical oscillators are therefore designed such that $|A(\omega)H(\omega)| > 1$, which ensures that oscillation can start. Gain compression in the amplifier as the oscillation amplitude grows then forces the system into the marginally stable state where the oscillation is sustained.

2.3.2 Negative Resistance Oscillator Model

For RF oscillators, a negative resistance model is often favored over the linear feedback model. The amplifier is then viewed as a complex impedance $Z_{\text{amp}} = R_{\text{amp}} + jX_{\text{amp}}$, where the resistive part is negative, rather than a voltage- or power gain. When such an amplifier is connected to a resonator as shown in Figure 2.10, oscillation criteria can be formulated. Kirchhoff's voltage law implies that if any current should flow in the circuit, $Z_{\text{amp}} + Z_L$ must equal zero. Separating the resistance and reactance, the criteria for sustained oscillation are therefore

$$R_{\text{amp}} + R_L = 0 \tag{2.24a}$$
$$X_{\text{amp}} + X_L = 0 \tag{2.24b}$$

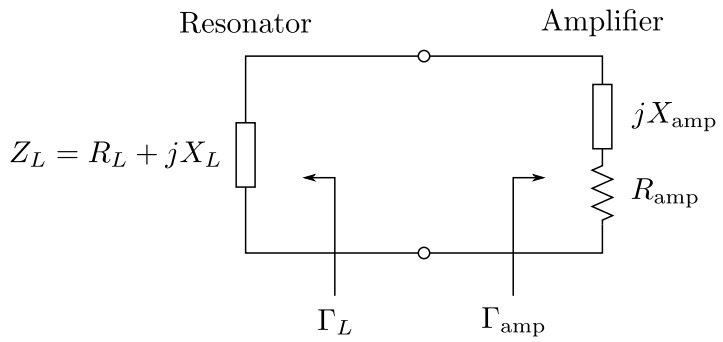

Figure 2.10: Simple circuit diagram of a negative resistance amplifier.

These two equations can provide an intuition similar to that seen in the linear feedback model, where the negative resistance of the amplifier compensates for losses in the resonator, and the matched reactance ensures constructive phase. The condition of matched reactance also highlights the possible use of a varactor to adjust the oscillation frequency. The oscillation criteria may also equivalently be rewritten in terms of reflection coefficients as $\Gamma_{\text{amp}}\Gamma_L = 1$. When expressed in polar form, this resembles the Barkhausen criteria from the linear feedback model as

$$|\Gamma_{\text{amp}}\Gamma_L| = 1 \tag{2.25a}$$

$$\angle\Gamma_{\text{amp}}\Gamma_L = 2\pi n, \quad n \in \mathbb{Z} \tag{2.25b}$$

Similarly to the Barkhausen criteria, these expressions do not guarantee that oscillation will start, and practical oscillators are designed such that $|\Gamma_{\text{amp}}\Gamma_L| > 1$ for the same reasons as in the feedback model.

The impedance of the amplifier is in practice dependent on frequency and amplitude. Nonlinearity and time-variant phenomena also affect the operation and performance of oscillators [16, 17, 26], but lie outside the scope of this thesis. If model parameters are determined close to the operating point of the oscillator, the model presented here should give sufficient insight into the oscillator to design a PLL control system.

2.3.3 Resonators

The simplest model of an electronic resonator is the ideal RLC circuit, which consists of a resistor, inductor, and capacitor connected in either series or parallel. Microwave resonators show very similar behavior as the RLC resonator close to their resonance frequencies, and an RLC circuit may therefore be used to model them. Since the analysis of series- and parallel RLC resonators is very similarly, only the series RLC resonator will be analyzed.

Figure 2.11 shows a circuit diagram of a series RLC resonator, for which the input impedance is given by

$$Z_{\text{in}} = R + j\omega L + \frac{1}{j\omega C} \tag{2.26}$$

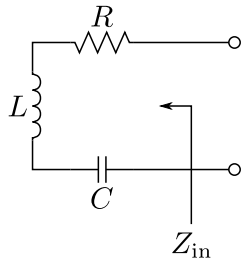

Figure 2.11: Circuit diagram of a series RLC resonator.

Resonance occurs when the average energy stored in the inductor and capacitor is equal, which happens when the reactance is zero. From Equation (2.26) it then follows that the resonance frequency is given by $\omega_0 = 1/\sqrt{LC}$.

2.3.3.1 Resonator Quality Factor

An important parameter of an oscillator is its quality factor, Q, which is defined at resonance as [27]

$$Q = 2\pi \frac{\text{average stored energy}}{\text{energy lost per cycle}} \tag{2.27}$$

The Q is therefore a measure of how lossy a resonator is, and for a series RLC resonator it can be shown to equal [28]

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC} \tag{2.28}$$

Figure 2.12 shows how different values of Q affect the input impedance, and it can be seen that a higher Q results in a more narrow-banded resonance peak and a faster phase transition. If the half-power bandwidth of the resonator is denoted $\Delta\omega$, it can be related to Q as [28]

$$Q = \frac{\omega_0}{\Delta\omega} \tag{2.29}$$

Computing the derivative of the phase at resonance, it can also be related to Q by utilizing Equation (2.28) as

$$\left.\frac{\partial \angle Z_{\text{in}}}{\partial \omega}\right|_{\omega=\omega_0} = \frac{2L}{R} = \frac{2Q}{\omega_0} \tag{2.30}$$

The narrow bandwidth and sharp phase transition of a high Q resonator is highly desirable in an oscillator, since it makes the system more frequency-selective and minimizes the impact of random phase fluctuations on frequency.

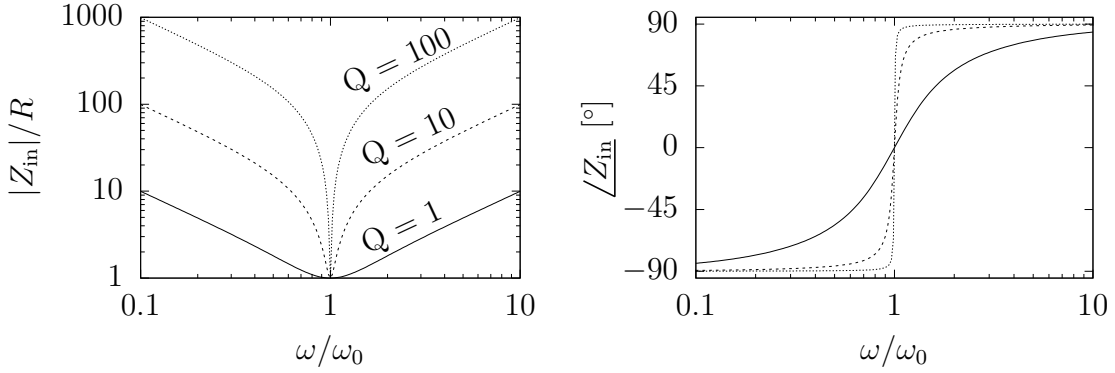

Figure 2.12: Normalized impedance and phase as a function of normalized frequency for series resonators with varying quality factor.

2.3.3.2 Loaded Quality Factor

In the analysis so far, Q has been used to denote the resonator quality factor for an unloaded resonator. In practice, a resonator needs to be coupled to external circuitry to be useful, which means that the resonator is also externally loaded. For a series RLC resonator, the external load may be modeled as a series resistance R_e, which increases the total resistance at resonance. Modifying Equation (2.28) to include this extra resistance we get the loaded quality factor, Q_L, as

$$Q_L = \frac{\omega_0 L}{R + R_e} = \frac{\omega_0 L}{R}\left(\frac{1}{1 + \frac{R_e}{R}}\right) = Q_0\left(\frac{1}{1+\beta}\right) \tag{2.31}$$

where Q_0 is the unloaded quality factor and $\beta = R_e/R$ is the coupling coefficient. A choice of $\beta < 1$ gives a higher Q_L, but if the external resistance represents the impedance of a source, $\beta = 1$ provides the maximum power transfer. How tightly the resonator is coupled with the source can therefore provide a trade-off between loaded Q and power in the resonator.

2.3.3.3 Resonator Termination

Since the input impedance of a resonator may rise to very high values far from any resonance point, it is also common to terminate the resonator to match it to the system impedance outside resonance. Doing so results in a reflection magnitude that is low far from resonance, and hence ensures that oscillation does not occur at an undesired frequency where the amplifier may still have reflection gain. Terminating the resonator does however affect how it is loaded and will further degrade the quality factor. Due to the effort required to calculate these effects accurately, it is more convenient to simulate a variety of termination resistances.

2.3.4 Phase Noise

As was explained in section 2.1.1, the origin of oscillator phase noise is fairly complex and involves time-variant and nonlinear behavior. Such detailed analysis falls outside

the scope of this thesis, but power-law spectral density models are able to provide accurate descriptions of oscillator phase noise at offset frequencies of interest. The most prominent such model is the one presented by Leeson, which is derived from the linear feedback oscillator model and augmented with empirical parameters to account for some device noise sources [9]. The model may be described as

$$\mathcal{L}(f_m) = \frac{FkT}{2P_r}\left[\left(\frac{f_0}{2Q_L f_m}\right)^2 + 1\right]\left[\frac{f_{\text{flicker}}}{f_m} + 1\right] \tag{2.32}$$

where F is the empirical excess noise figure, k is Boltzmann's constant, T is absolute temperature, f_0 is the oscillation frequency, f_{flicker} is the empirically determined flicker noise corner, f_m is the offset frequency, and P_r is the power dissipated in the resonator. Since both the loaded Q and the power in the resonator appears in the expression, it is possible to use it to optimize the coupling coefficient. Doing so yields an optimum for $\beta = 1$ [29].

Other linear models of phase noise exist, such as the one presented by Everard [30], which predicts an optimum coupling coefficient of $\beta = 1/2$, but experimental results indicate that the true optimum is closer to 1 due to nonlinear noise conversion not considered in Everard's model [29]. Since this thesis is not concerned with either resonator- or amplifier design, Leeson's model of oscillator phase noise is sufficient for gaining a qualitative understanding and insight in factors influencing the performance.

It should be noted that Leeson's model describes the phase noise inside the oscillator, but to measure or make use of the oscillator, a portion of the oscillator power needs to be coupled to an output load. The output coupling can have a large impact on the phase noise observed at the output of the oscillator [30]. If the coupling is strong it may lead to a degradation of resonator Q, with degraded phase noise as a consequence. On the other hand, if the coupling is weak, and low power is extracted from the oscillator, it will lead to a raised white phase noise floor without much degradation of neither the phase random walk noise nor the phase white FM noise. In the latter case, Leeson's equation will be of limited use for phase noise modeling, as the white phase noise floor then is proportional to the output power and not the resonator power, P_r, as suggested in Equation (2.32).

2.3.5 Varactor Frequency Tuning

This thesis project intends to use a mechanically tunable cavity as the resonator in the oscillator, but only tuning a cavity mechanically is not suitable for use in a PLL due to nonlinearities and severe challenges in delay and resolution. As hinted to in Section 2.3.2, a varactor could be used in conjunction with the mechanical tuning to provide voltage controlled fast and fine-grain tuning, albeit with a smaller tunable range. Placing a varactor in parallel with the amplifier in Figure 2.10 would modify Equation (2.24b) to include the variable capacitance, and thus allow tuning of the oscillation criteria. For the purposes of this thesis, the varactor will instead be considered as a phase shifter, since the S_{11} parameter of the varactor and amplifier

together is easily measured for various operating points. The relation between phase shift and frequency difference for an ideal oscillator is then given by [31]

$$\Delta f(\phi) = \frac{f_r \tan(\phi)}{2Q_L} \tag{2.33}$$

where Δf is the frequency offset, ϕ is the shift in phase, and f_r is the resonant frequency of the resonator itself. For small angles of ϕ, a first order Taylor series expansion reduces the equation to a linear dependency.

2.4 Control Theory

The purpose of a control system is usually to control certain parameters of a process in such a way that an output signal follows a reference signal as closely as possible. In designing a control system, it is therefore crucial to determine if the system is stable, what the residual error of the system is, and the dynamics of how the system adapts to changes in the reference signal. For linear time-invariant systems that may be described using transfer functions, classical control theory provides the tools necessary for such analysis.

2.4.1 System Stability

All transfer functions of linear time-invariant systems can be written as a fraction of two polynomials of the complex variable $s = \sigma + j\omega$ as

$$F(s) = \frac{N(s)}{D(s)} \tag{2.34}$$

The solutions to $N(s) = 0$ and $D(s) = 0$ are the zeroes- and poles of the system respectively. If all poles of the system lie in the left half-plane, any transients will decay exponentially and the system is stable. If one of more of the poles lie in the right half-plane, any transient will instead grow exponentially without bound and the system is unstable. For systems with a pole right on the imaginary axis, transients produce sustained oscillations and the system is marginally stable. By locating the poles of Equation (2.7), the stability of the PLL system in Figure 2.3 could be determined. However, due to historic difficulties in computing the poles of higher order systems, stability is often determined by looking at the forward transfer function from the input to the signal that is fed back instead. The reason for this becomes apparent if Equation (2.7) is rewritten as

$$\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{\frac{K_p K_v H(s)}{s}}{1 + \frac{K_p K_v H(s)}{Ns}} \tag{2.35}$$

The system is unstable if the denominator is zero, meaning that the condition that should be avoided is

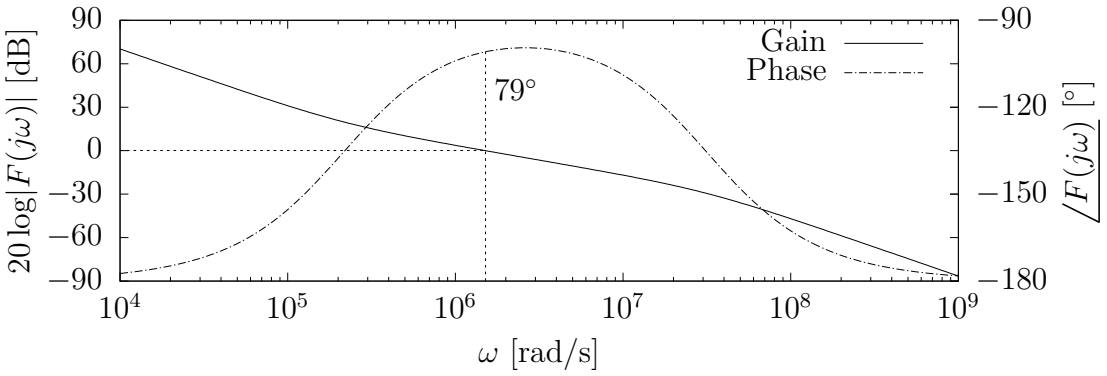

Figure 2.13: Bode plot of a third order PLL with 79° phase margin and infinite gain margin since the phase never reaches −180°.

$$\frac{K_p K_v H(s)}{Ns} = -1 \tag{2.36}$$

which can be written in polar form as

$$\left|\frac{K_p K_v H(s)}{Ns}\right| = 1 \tag{2.37a}$$

$$\angle\frac{K_p K_v H(s)}{Ns} = -180° \tag{2.37b}$$

From these two equations it is also natural to define the gain- and phase margin of a system as the additional gain needed to reach a gain of one at −180° and the additional phase delay needed to reach −180° at a gain of one. Figure 2.13 shows how a Bode diagram can be used to determine stability of a system.

2.4.2 Residual Error

Residual error in a control system can be determined by applying the final value theorem on the transfer function from input to error of a system. For a PLL as shown in Figure 2.3, the transfer from input to error is given by

$$\frac{\phi_{\text{error}}}{\phi_{\text{in}}} = \frac{1}{1 + \dfrac{K_p K_v H(s)}{Ns}} \tag{2.38}$$

The final value theorem states that if all poles of a system $F(s)$ lie in the left half plane or at the origin, with at most one pole at the origin, the following equality holds [32]

$$\lim_{s\to 0} sF(s) = \lim_{t\to\infty} f(t) \tag{2.39}$$

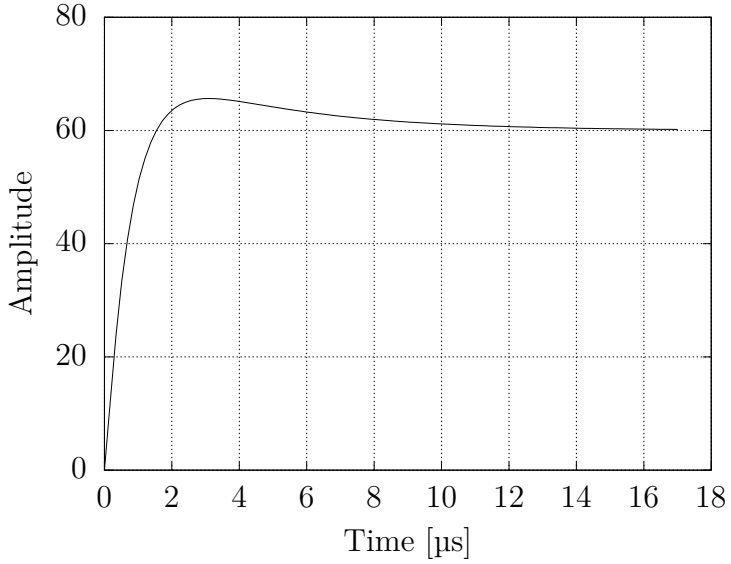

Figure 2.14: Step response of the same system as in Figure 2.13.

When a step function, $\frac{1}{s}$, is applied to the input of a system, the final error value is simply given by

$$\lim_{s \to 0} F(s) \tag{2.40}$$

Appendix A.2 lists the error transfer functions of PLLs with each loop filter as in Figure 2.7. Taking the limit as $s \to 0$ shows that the residual error of a step in the input is zero for each system order, provided the condition on pole placement is met.

2.4.3 System Dynamics

In addition to knowing the residual error of a system, knowledge about the transient response is typically also required since the maximum overshoot and time to settle may be constrained by system requirements. The response to an impulse, step, ramp, etcetera on the input of a linear time-invariant system is easily computed from the transfer function using computer tools such as MATLAB. Figure 2.14 shows an example of a step response for a third order PLL.

3
Design

An overview of the system-level design is shown in Figure 3.1. The strategy is to treat the cavity oscillator as a VCO through use of the varactor, and thereby control it using a conventional analog PLL design. The control voltage is then monitored by a microcontroller unit (MCU), which can control the cavity mechanically using a motor if certain conditions are met. The digital control of the mechanical tuning means that it is not limited to linear- or time-invariant control, which enables easy compensation for non-linearities in the mechanical tuning. The digital motor control also allows for hysteresis in the motor control, such that the motor normally is inactive and only activates when the phase shifter is close to its range limits. Doing so minimizes the wear on mechanical components and limits the noise contribution of the mechanical tuning to only when it is needed, such as when a new output frequency is demanded or the temperature of the cavity changes.

An LMX2820EVM development board [11] is used to realize the frequency divider and PFD, and an AMC7834EVM development board [33] is used to bias the reflection amplifier. The reflection amplifier and phase shifter are integrated on the same monolithic microwave integrated circuit (MMIC), which is provided from Chalmers University of Technology. Details about this MMIC are presented in Section 3.1. The cavity, including most of the design for the printed circuit board (PCB) test board, which connects the cavity to the amplifier, is taken from a previous thesis project [10]. As was shown in Equation (2.20), a high reference frequency is beneficial in regard to noise transfer, and the maximum frequency allowed by the PFD is 200 MHz. A 100 MHz reference output of a Rohde & Schwarz FSWP50 [34] is therefore used as the reference oscillator, with the option of multiplying it by two. Most of the design freedom of the system lies in the loop filter, $H(s)$, and MCU software to control the motor, biasing, division ratio, and PFD charge pump gain.

3.1 Reflection Amplifier Characterization

The reflection amplifier with integrated phase shifter MMIC used in this project was part of a separate research project at Chalmers University of Technology. The device technology used in the MMIC is GaN HEMT and the reflection amplifier consists of a single transistor with a common source and reflection gain on the gate terminal. An output is also connected to the drain of the transistor, providing a buffered output for the oscillator. The phase shifter is implemented as a varactor-loaded transmission line, utilizing the gate capacitance of four transistors identical

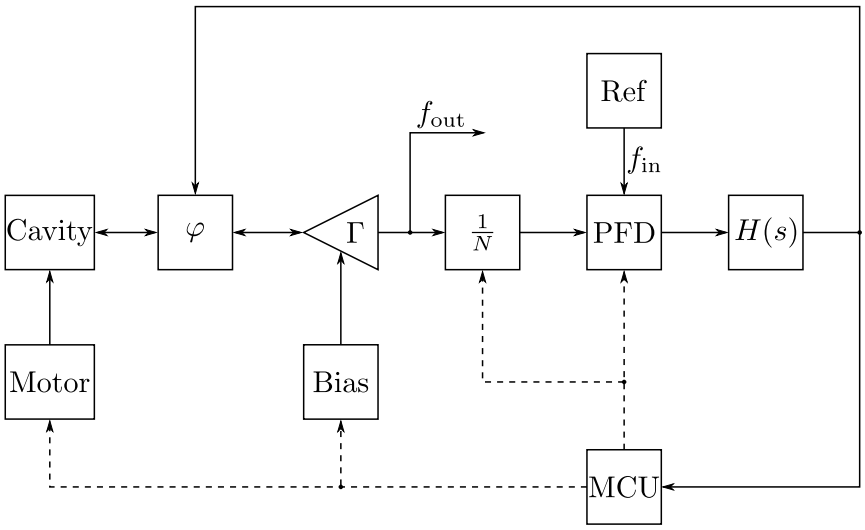

Figure 3.1: Overview of system design. Solid lines are analog connections and dashed lines are digital control connections. The box labeled φ denotes the phase shifter and Γ denotes the reflection amplifier.

to the one in the amplifier.

Magnitude and phase of the reflection amplifier gain was measured for several biasing points by probing directly on the chip. Figures 3.2a and 3.2b show how the reflection magnitude varies as a function of the gate bias voltage at varactor bias voltages of -2 and $-20\,\text{V}$ respectively. As expected from a depletion mode device, the reflection gain increases with rising gate bias voltage, and the varactor did not significantly affect the gain magnitude at these biasing points. Figure 3.3 shows the reflection phase for the same sweeps.

Figure 3.4 shows the reflection magnitude and phase for a sweep of the varactor bias voltage, where it can be seen that varactor bias voltages above $-2\,\text{V}$ start to significantly affect the reflection gain of the amplifier, while simultaneously providing the most tuning of the phase.

3.2 Test Board Design

Most of the test board was identical to the one used in [10]. In particular, no changes were made to the cavity mounting, board stack-up, or surface finishes. Out of the different methods for coupling to the cavity presented in [10], only probe coupling was used. The previous placement of the amplifier was kept, but supplemented with another alternative placement much closer to the cavity. The mechanical phase shifter of the previous work was kept in the old amplifier placement alternative to minimize changes, but removed in the new one since the integrated phase shifter of the amplifier makes it redundant. Figure 3.5 shows the layouts for the two amplifier positions and Figure 3.6 illustrates how the cavity- and mechanical phase shifter is mounted to the test board. Because a different amplifier from that in [10] was used, its mounting solution to the test board had to be redesigned. Resonator S-

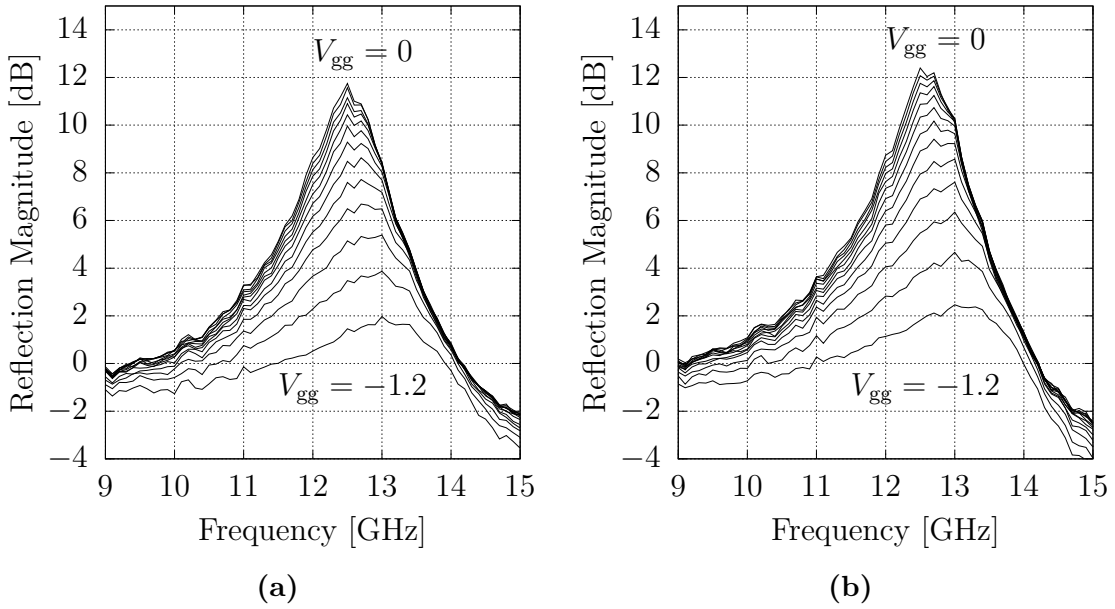

Figure 3.2: Reflection magnitudes for a sweep of gate bias voltage from −1.2 to 0 V in 0.1 V increments at −2 V varactor bias voltage (a) and −20 V varactor bias voltage (b). The drain was biased with 6 V and the drain output was terminated with 50 Ω in both cases.

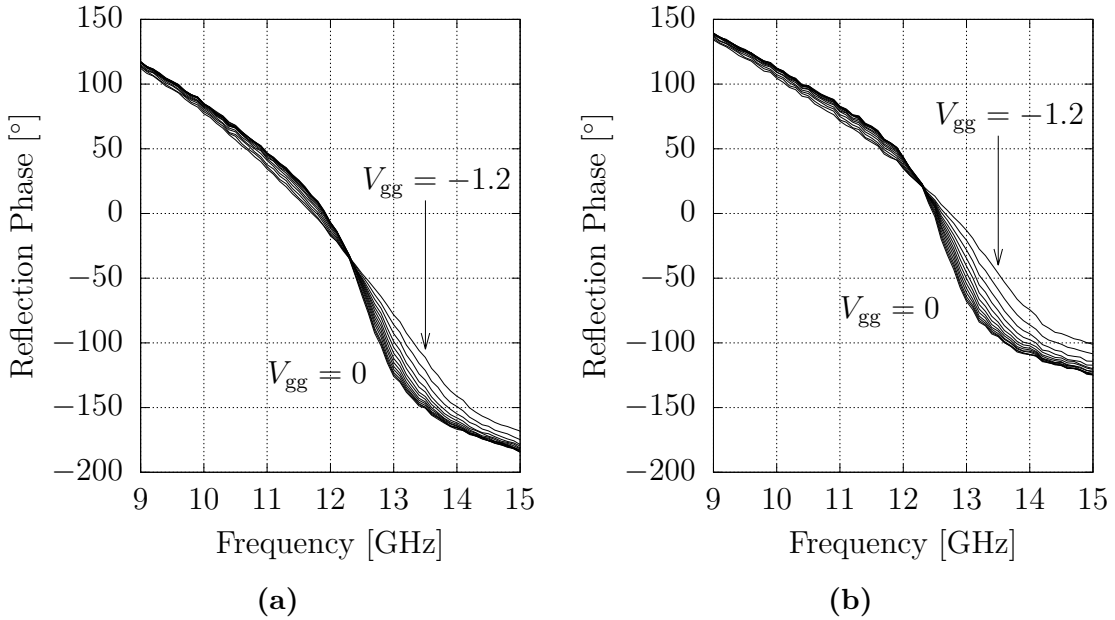

Figure 3.3: Reflection phase for a sweep of gate bias voltage from −1.2 to 0 V in 0.1 V increments at −2 V varactor bias voltage (a) and −20 V varactor bias voltage (b). The drain was biased with 6 V and the drain output was terminated with 50 Ω in both cases.

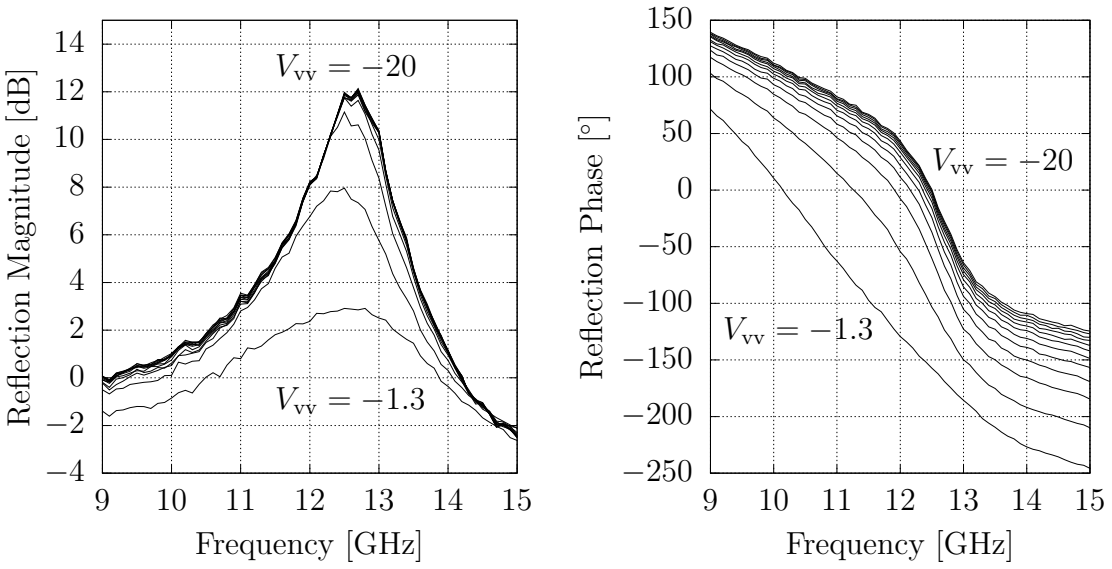

Figure 3.4: Reflection magnitude (a) and phase (b) for a sweep of varactor bias voltage with the drain biased with 6 V and the gate biased with −0.2 V. The varactor voltage sweep started at −20 V and was incremented in steps of 2 V to −2 V, then supplemented with measurements at −1.5 and −1.3 V.

parameters for varying length of the probe coupling to the cavity, in combination with different terminations, also had to be evaluated to ensure that the oscillation criteria could be fulfilled with the new amplifier. These steps are described in more detail in Sections 3.2.1 and 3.2.2.

3.2.1 Amplifier Mounting

The reflection amplifier was supplied as a bare die and needed to be wire bonded to the test board. This posed an issue, as the inductance of a bond wire could potentially diminish the reflection gain beyond usable levels. To determine the impact of bond wire length on gain, a network consisting of a bond wire model and measured S-parameters of the reflection amplifier was simulated in Keysight's Advanced Design System. Figure 3.7 shows how the simulated network was connected.

Simulating a sweep of the bond wire length for two varactor voltages at the amplifier bias point which yielded the highest gain gave the results shown in Figure 3.8. Since the lowest resonance frequency that the cavity can be tuned to is approximately 11.5 GHz, it is apparent that bond wire length has to be minimized for the oscillation criteria to be fulfilled over the entire tuning range for all varactor voltages. A mounting solution where the amplifier chip is placed in a milled pocket, such that its top surface is flush with the test board, was therefore decided on in order to minimize bond wire length. A bond wire length of approximately 500 µm was then achieved. A slightly shorter wire length would have been achievable if not for a design mistake in the test board that caused the chip to be slightly miss-aligned with the bonding target location, as shown in Figure 3.9. In order to protect the

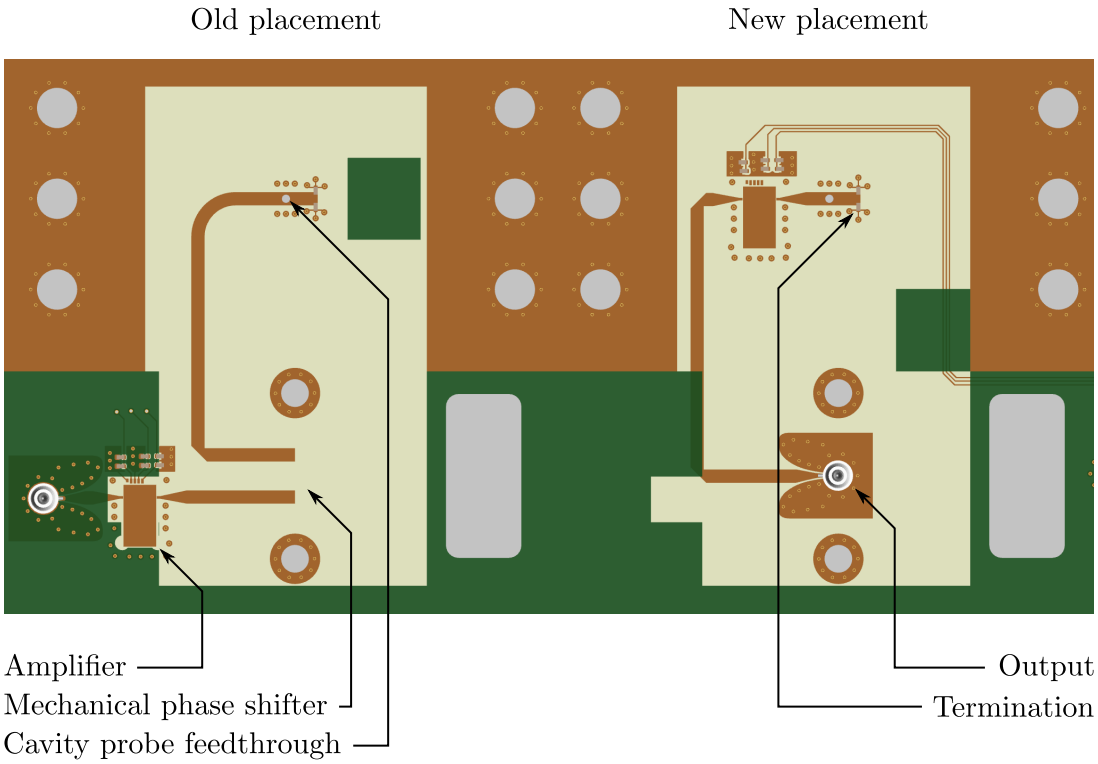

Figure 3.5: The layout for the two different amplifier placements.

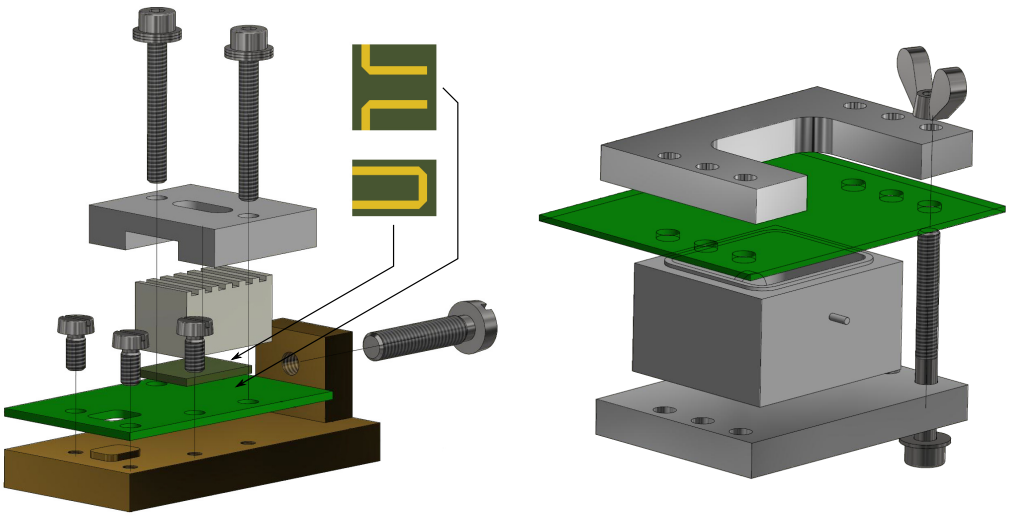

Figure 3.6: Illustration of mounting solution for the mechanical phase shifter (left) and cavity resonator (right). Source: adapted from [10].

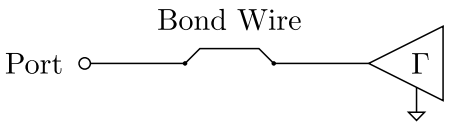

Figure 3.7: Network model used to simulate impact of bond wire length on reflection gain.

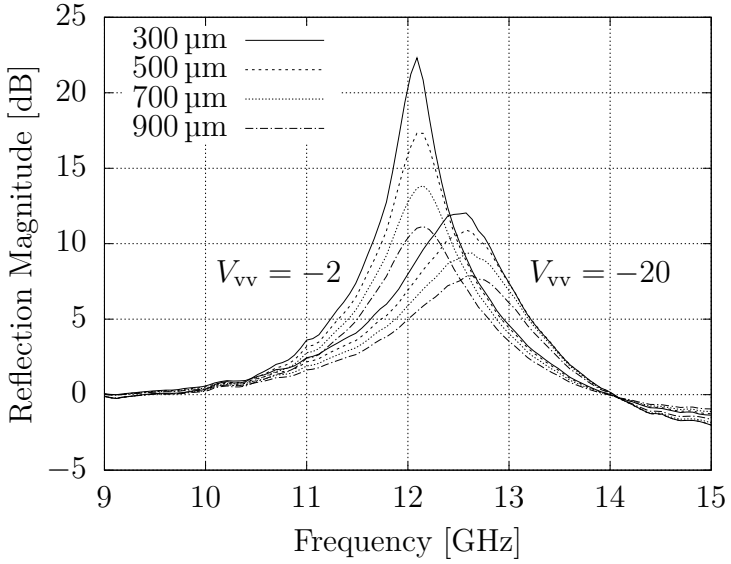

Figure 3.8: Simulated reflection gain of the amplifier for various bond wire lengths and varactor voltages in the network shown in Figure 3.7. The amplifier was simulated using the measurements from Section 3.1 with a drain bias voltage of 6 V and a gate bias voltage of 0 V, while the bond wire and transmission lines were modeled in Keysight's Advanced Design System. The amplifier did not produce any gain elsewhere in the span from 1 GHz to 20 GHz than what is shown in the figure.

delicate bond wires during handling, the chip was glob encapsulated using a dam and fill method.

3.2.2 Cavity Probe Length and Termination

The length of the cavity probe directly affects the coupling to the cavity. The strongest possible coupling occurs if the probe extends to the middle of the cavity, but since the perturbation also occupies this space, it must be shorter. Equation (2.31) suggests that the shortest possible probe length should be used to maximize Q_l, but with the structures of the test board taken into account, a longer probe length may yield higher loaded Q. Since the amplifier does not have gain outside the band of interest it should not be necessary to terminate the cavity, but different terminations were nonetheless evaluated for completeness.

To find the optimal probe length and termination load, measurements of the cavity were first performed for various probe lengths. The observed tuning range and loaded Q of the de-embedded cavity measurements are shown in Figure 3.10 and 3.11. The loaded quality factor was calculated from the phase of the port impedance using Equation (2.30), and the results are in agreement with those found in [10]. To simulate the impact of the test board structures and different termination loads, a network model consisting of the cavity, microstrip lines, a taper, and a termination load, Z_L, as shown in Figure 3.12 was used. In the case of no termination, the right transmission line and termination load were removed from the model. The quantities of interest are mainly the reflection magnitude at resonance and the loaded Q for

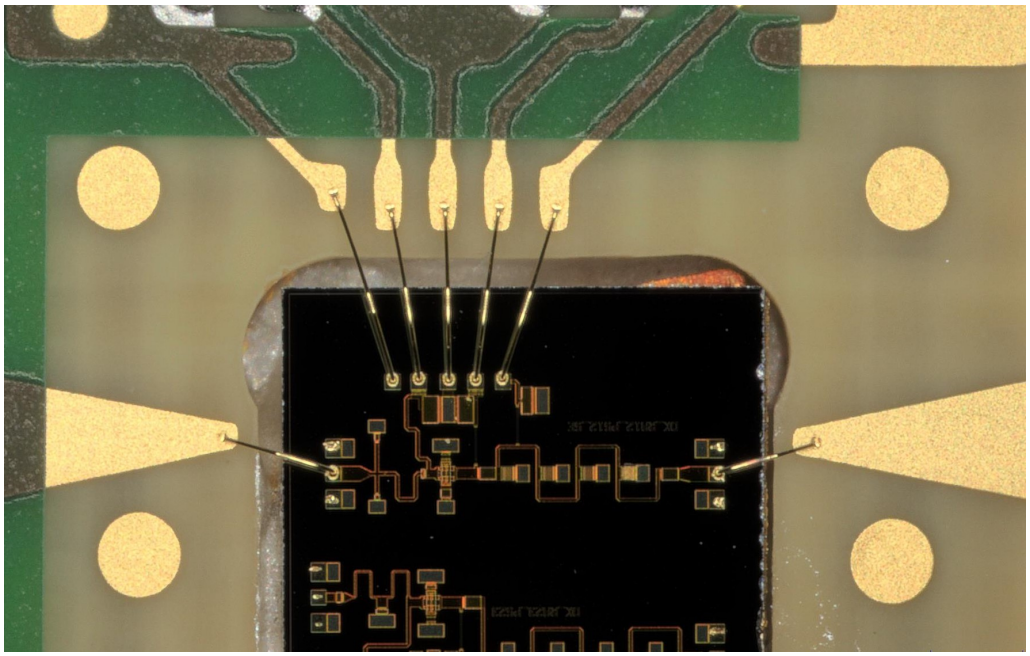

Figure 3.9: Image of the bonded reflection amplifier before encapsulation. The milled pocket was slightly offset, resulting in an angled and slightly longer critical bond wire length. The right-most bond wire is the critical bond wire and has a length of approximately 500 µm.

different terminations and probe lengths, since phase has the most uncertainty and can be adjusted using the phase shifter. The two different amplifier placements can be simulated by altering the length of the left microstrip line in Figure 3.12 to match each placement, as the other structures are identical in both cases. The mechanical phase shifter in the old amplifier placement had an insertion loss of 0.5 to 1 dB [10], which can simply be subtracted from the reflection magnitude in the simulation of the old amplifier placement, since phase is not considered.

By finding the reflection magnitude at resonance for several tuning positions, an envelope of the reflection gain required to fulfill the oscillation criteria of Equation (2.25a) for each position can be plotted. Figure 3.13a shows such a plot for the new amplifier placement when the cavity is not terminated, and Figure 3.13b shows the corresponding Q. As can be seen, there is now an optimal probe length in terms of maximizing Q, close to 1.85 mm, but a longer probe length also requires more gain from the amplifier to allow oscillation. It is furthermore clear that probe lengths beyond 1.85 mm are not desirable as they yield a lower Q while requiring higher gain. Simulations using termination loads of 50 Ω, 100 Ω, and 200 Ω were also conducted and can be found in Appendix B.1, but yielded lower Q and higher gain requirements than using no termination.

Figures 3.14a and 3.14b show the required gain and Q for each tuning position for the old amplifier placement. The 1.1 mm probe was exempted due to its very low Q. Compared to the new amplifier position, the gain requirements are higher and the Q is lower, but a probe length of 1.85 mm still gives the highest Q. No terminations were simulated for this amplifier placement.

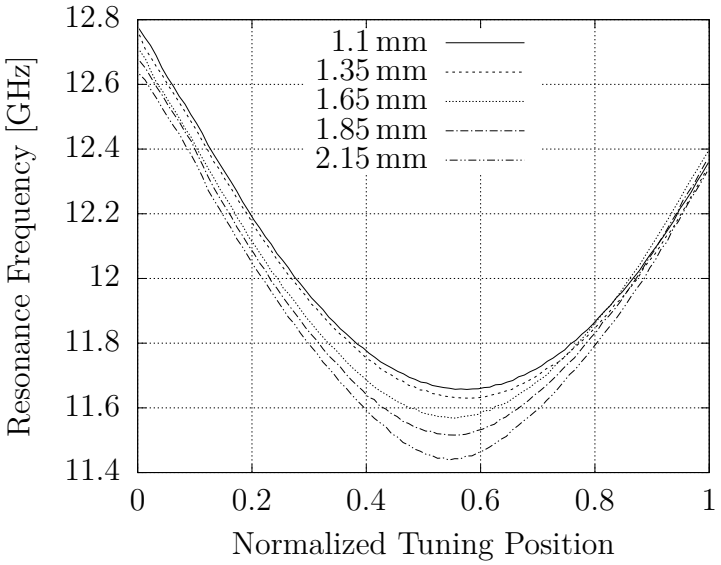

Figure 3.10: Resonance frequency for different tuning positions and probe lengths. The entire tuning range is shifted down in frequency for longer probe lengths since the longer probes result in a greater equivalent capacitance of the resonator.

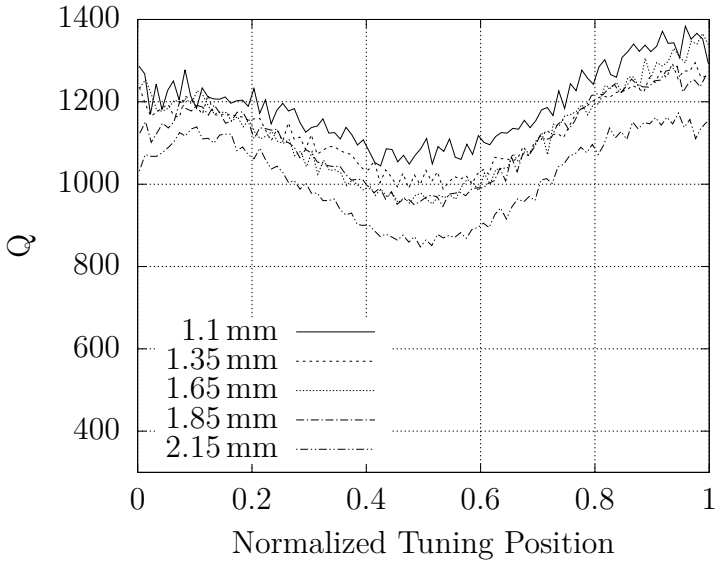

Figure 3.11: Quality factor for different tuning positions and probe lengths. Shorter probe lengths result in a weaker coupling to the cavity, making its Q approach the unloaded Q at the cost of less power being transferred to it.

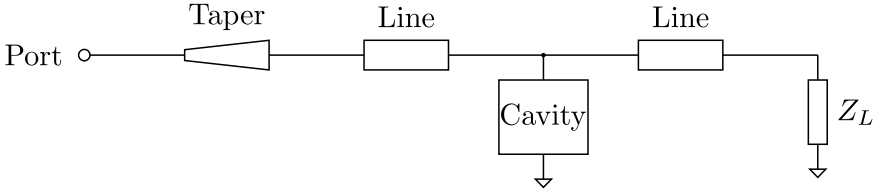

Figure 3.12: Network model used to simulate termination of the cavity resonator.

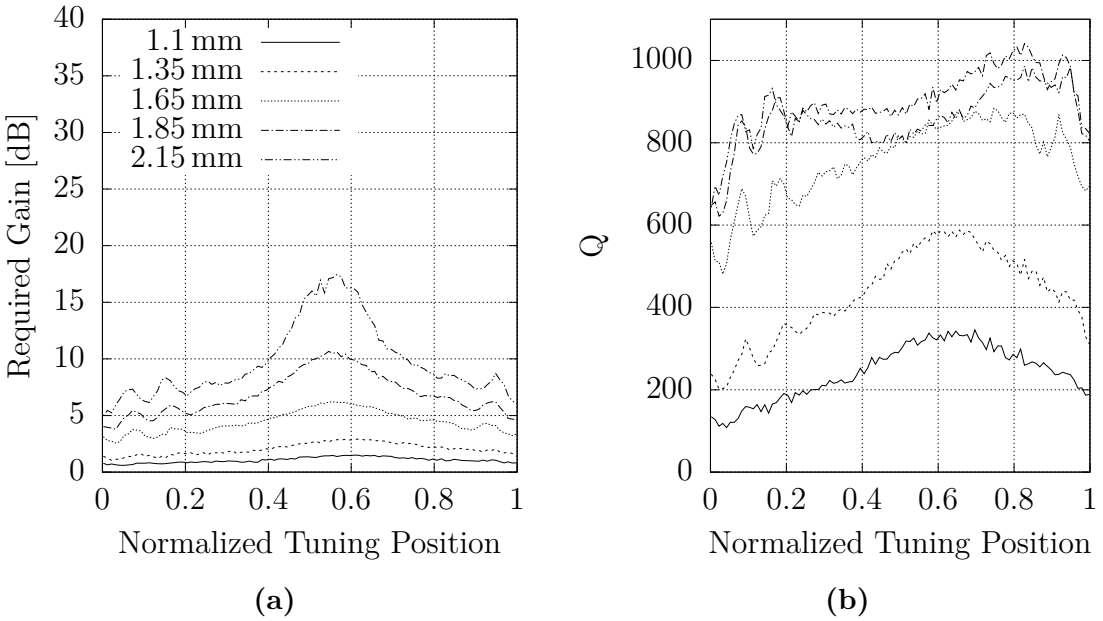

Figure 3.13: Simulated amplifier gain required to fulfill oscillation criteria (a) and Q (b) for different probe length and tuning position of the cavity without any termination using the new amplifier placement.

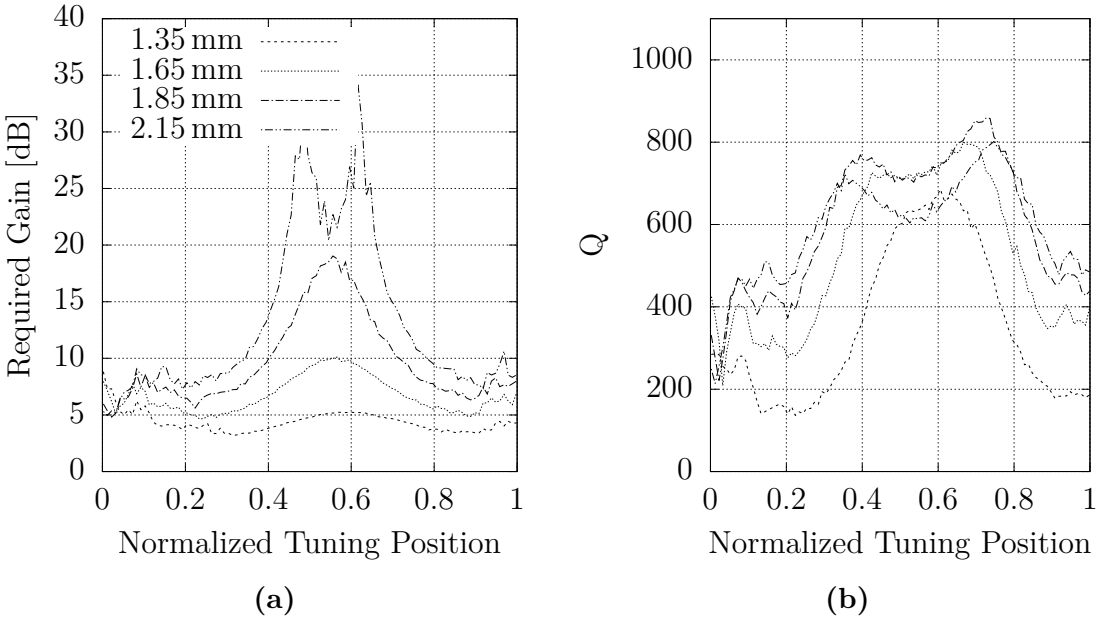

Figure 3.14: Simulated amplifier gain required to fulfill oscillation criteria (a) and Q (b) for different probe length and tuning position of the cavity without any termination using the old amplifier placement.

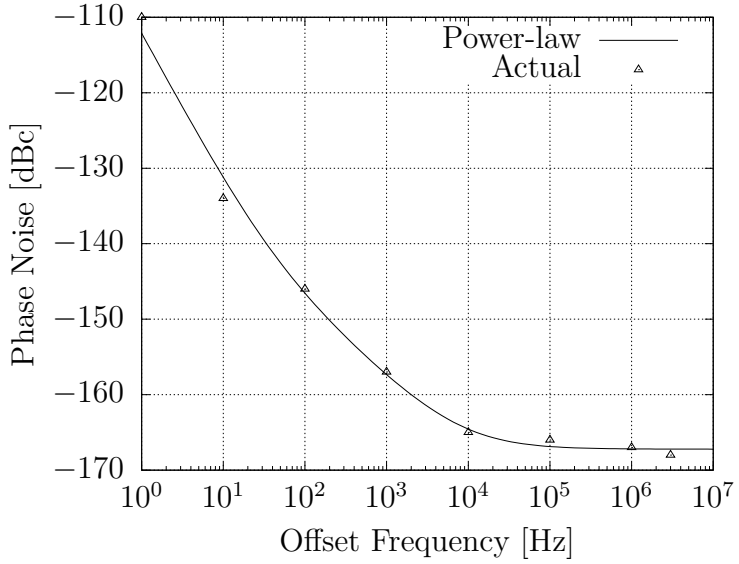

Figure 3.15: Phase noise of the FSWP50 100 MHz output according to its datasheet and the fitted power-law model.

Combining the results of Figures 3.8 and 3.13, it is apparent that maximization of Q conflicts with maximization of tuning range. Q is maximized with a probe length of approximately 1.85 mm for both amplifier placements, while full tuning with maximal varactor range requires a probe length closer to 1.35 mm. However, in all cases the Q was maximized when the resonator was not terminated.

3.3 Characterization of Noise Sources

In order to effectively design the loop filter to minimize phase noise, some of the noise sources which are described by empirical models, as outlined in Chapter 2, must be characterized. This includes both the reference- and cavity oscillator, as well as the PFD.

3.3.1 Reference Noise

A 100 MHz reference output of a Rohde & Schwarz FSWP50 [34] was used as the reference oscillator. The internals of the oscillator were not known, and a power-law model of the phase noise was therefore preferred over a physical model. A power-law model as in Equation (2.6), with α ranging from -2 to 0, was fitted to noise figures from the datasheet of the instrument. Figure 3.15 shows the actual data and the best fit, which has $\alpha_0 \approx 1.896 \times 10^{-17}$, $\alpha_{-1} \approx 1.596 \times 10^{-13}$, and $\alpha_{-2} \approx 5.985 \times 10^{-12}$. The maximum deviation of the model is within 3 dB for all the available data points.

3.3.2 Phase Detector Noise

Only white phase noise was considered from the PFD, which is described by Equation (2.12). Since changes to the reference frequency and feedback division factor

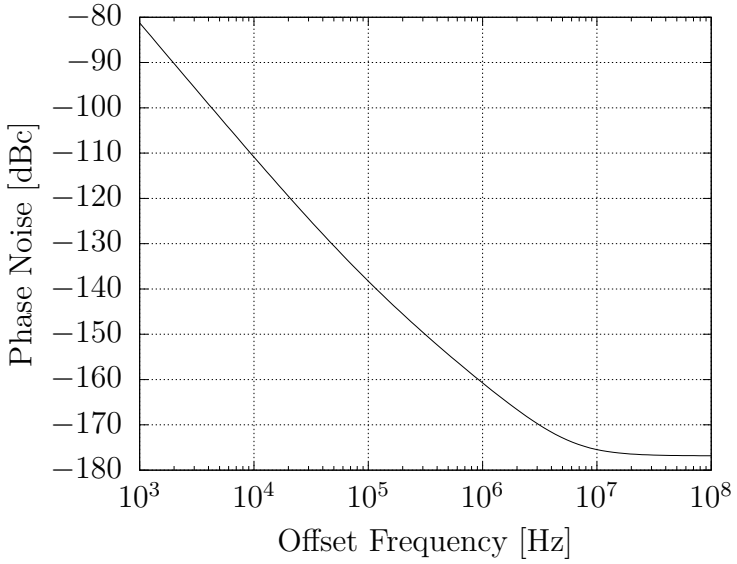

Figure 3.16: Estimated phase noise of the cavity oscillator based on Leeson's model, assuming $F = 100$, $Q_L = 1000$, $f_{\text{flicker}} = 100\,\text{kHz}$, and $P_r = 100\,\text{mW}$.

affect most other noise sources as well, the fitting constant, α, was determined by comparing the white phase noise of a system with the PFD to models of the same system where $\alpha = 0$. If a white-noise discrepancy following Equation (2.12) was observed as I_p was varied, α could be tuned to compensate for it.

Using the 100 MHz reference described above and a built-in VCO of the LMX2820, it was not possible to distinguish any noise from the PFD. It is possible that PFD noise will be visible once the cavity oscillator is used, but for the purposes of loop filter design, α will be assumed to equal zero, implying a noise-less phase detector.

3.3.3 Cavity Oscillator Noise

The phase noise of the cavity oscillator can be estimated using Equation (2.32) if F, P_r, Q_L, and f_{flicker} are determined. For the purpose of designing the loop filter, it will be assumed that $F = 100$, $f_{\text{flicker}} = 100\,\text{kHz}$, and $P_r = 100\,\text{mW}$. As was found in Section 3.2.2, the loaded Q can be improved at the cost of oscillator tuning range. The highest achievable loaded Q is approximately 1000, which would result in a phase noise as shown in Figure 3.16.

3.4 Analog Control System Design

The purpose of the analog control system is to minimize the output phase noise of the PLL according to Equation (2.9), but since the phase noise power spectral density is not a scalar value, the notion of minimizing it is ambiguous. From here and onwards, minimization of phase noise will be taken to mean minimizing the integral of the logarithm of phase noise from an offset frequency of 10 kHz to 10 MHz. Using this as the metric of minimization ensures that phase noise at large offset frequencies is

Table 3.1: Optimal loop filter component values.

Component	Optimal value	Closest common value
R_1	68 Ω	68 Ω
C_1	100 pF	100 pF
C_2	879 pF	910 pF
R_3	6321 Ω	6340 Ω
C_3	2.83 nF	2.7 nF

not neglected, and will in fact favor designs which minimize phase noise beyond the loop bandwidth. This is desired, since the phase noise at higher offset frequencies is more limiting to radio performance [6, 7]. An additional constraint that the loop bandwidth should not be less than 30 kHz was also used in the evaluation of designs, in order to ensure that noise from vibrations and the motor pulse width modulation control is rejected.

The design parameters of the analog control system are the loop filter, charge pump gain, and Σ-Δ modulation order. Both the feedback division ratio and resonator Q, which vary with output frequency, do however also affect the phase noise, which means that the design parameters can only truly be optimized for a single output frequency. In the interest of reaching the lowest possible phase noise, the system was optimized for an output frequency of 12 GHz, since the resonator exhibits its highest Q of approximately 1000 at that frequency. Furthermore, the varactor had a nonlinear response, meaning that the VCO gain was not static either. From Figure 3.4b it can be observed that the varactor produced the highest phase shift per volt at around -3 V without deteriorating the reflection gain, resulting in a VCO gain of approximately $3\,\mathrm{MHz\,V^{-1}}$ according to Equation (2.33). This was therefore chosen as the operating point for which the system was optimized. Limiting the varactor to the relatively small range of -2 to -4 V also reduces the effect of nonlinearities, but the resulting phase noise of ±50% variation in VCO gain was still taken into account in the system design.

Due to the difficulty in calculating the optimal design parameters analytically, a numerical approach was instead used. Component values within reasonable ranges were iterated over for each Σ-Δ modulation order and charge pump current, and each parameter combination was scored based on how well they minimized phase noise according to above. Capacitor values were limited to be greater than 100 pF, and $R1$ was fixed to 68 Ω, since the optimization issue would otherwise be unconstrained. As expected, third order loop filters performed better than first- and second order filters, and the highest charge pump gain and Σ-Δ modulation order also produced the best results. The computed component values and their closest common component values are shown in Table 3.1. The resulting theoretical phase noise of the PLL when the closest common component values are used is shown in Figure 3.17, and Figure 3.18 shows how changes in VCO gain affect the output phase noise. With these values, the control system had decent stability margins, with infinite gain margin and 45° phase margin.

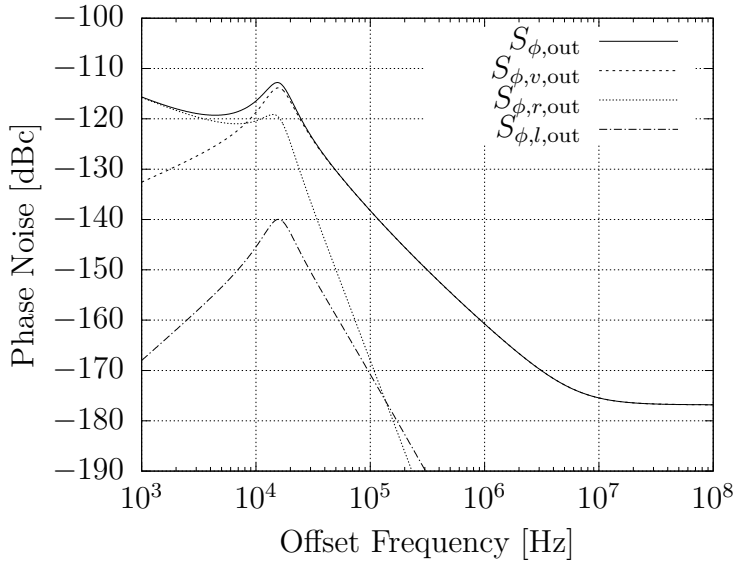

Figure 3.17: Theoretical output phase noise of the PLL when using the closest common component values in Table 3.1. Using the exact values lowers the peak at 20 kHz. The contribution of each noise source to the output is also shown, except for the divider noise, which was significantly lower than the output noise for all frequencies.

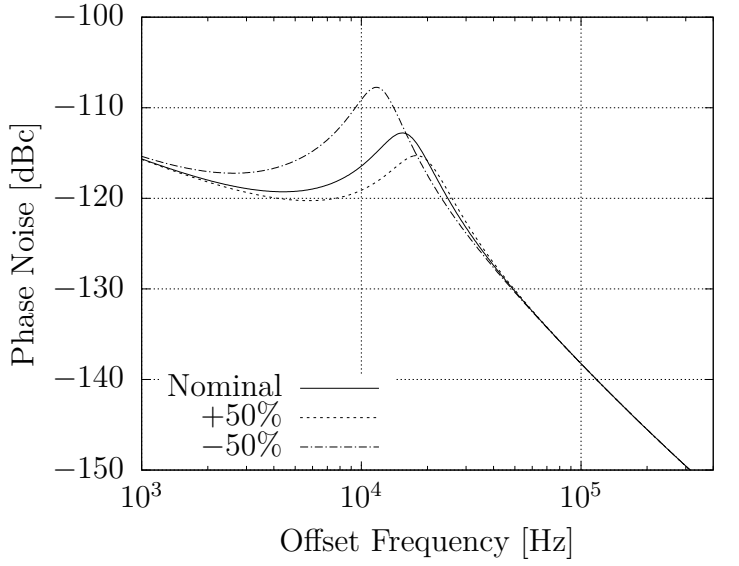

Figure 3.18: Output phase noise, as in Figure 3.17, when the VCO gain is varied with ±50%. The axes differ from Figure 3.17 to highlight the region where the change is visible.

3.5 Motor- and Bias Control

The strategy employed in the motor control, as described briefly in the chapter outline, is to first tune the motor to approximately the correct position based on a lookup table of position-to-frequency data. The MCU then monitors the VCO control voltage and tunes the motor with a constant speed until the VCO control voltage reaches the middle of its range. At that point the motor is deactivated, and remains inactive until the VCO control voltage has drifted beyond a threshold. The motor is then activated again to correct for the drift, and drive the control voltage back to the middle of its range. The advantage of this control scheme, beyond its simplicity, is that the motor is used only when necessary, which limits its noise contribution and minimizes wear on the threads of the cavity and tuning screw. Since the loop bandwidth of the analog control system is 35 kHz, which is far too high for the motor control, the VCO control voltage should be filtered before it is read by the MCU. A bandwidth on the order of a few hertz should be sufficient for the motor control.

The biasing of the amplifier also utilizes a lookup table of optimal amplifier biasing values for each desired frequency. No feedback is used in the biasing and the optimal values are determined empirically for a discrete number of tuning positions and interpolated linearly in between.

4

Results

The cavity oscillator was first tested without the PLL using a fixed varactor voltage of $-20\,\mathrm{V}$ to verify the performance of the free-running cavity oscillator. Only results of the new amplifier placement are presented, since the old amplifier placement had less tuning range and worse phase noise. The best phase noise was achieved at 11.65 GHz with the expected probe length of 1.85 mm, but with a termination resistance of $50\,\Omega$ rather than no termination. The amplifier was biased with a drain voltage of 10 V and a gate voltage of $-0.6\,\mathrm{V}$. The measured phase noise is shown in Figure 4.1. The amplifier drew a drain current of 38 mA, yielding a DC power consumption of 380 mW.

The cavity oscillator could be tuned from 11.51 GHz to 12.29 GHz using the mechanical tuning. Figure 4.2 shows the best-, worst-, and average phase noise over this tuning range when the cavity was terminated with $50\,\Omega$ and a 1.85 mm probe was used. The worst phase noise was observed at the highest frequency of 12.29 GHz. Figure 4.3 shows how much the varactor could offset the frequency of oscillation as a function of varactor voltage. No oscillation occurred for varactor voltages above $-1.3\,\mathrm{V}$, and the frequency offset was therefore calculated from the frequency at that varactor voltage. The varactor tuning range was measured for both a $50\,\Omega$ termination and no termination, both with a probe length of 1.85 mm.

It was not possible to phase-lock the oscillator, as the PLL control system was unstable and caused oscillation on the varactor control voltage.

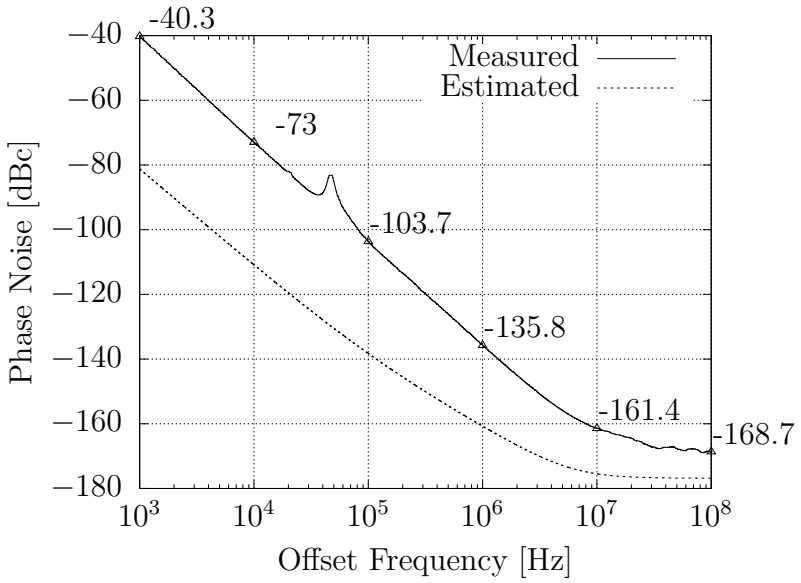

Figure 4.1: Measured phase noise of the free-running cavity oscillator at the optimal operating point, tuned to 11.65 GHz with a varactor voltage of −20 V, drain voltage of 10 V, and gate voltage of −0.6 V.

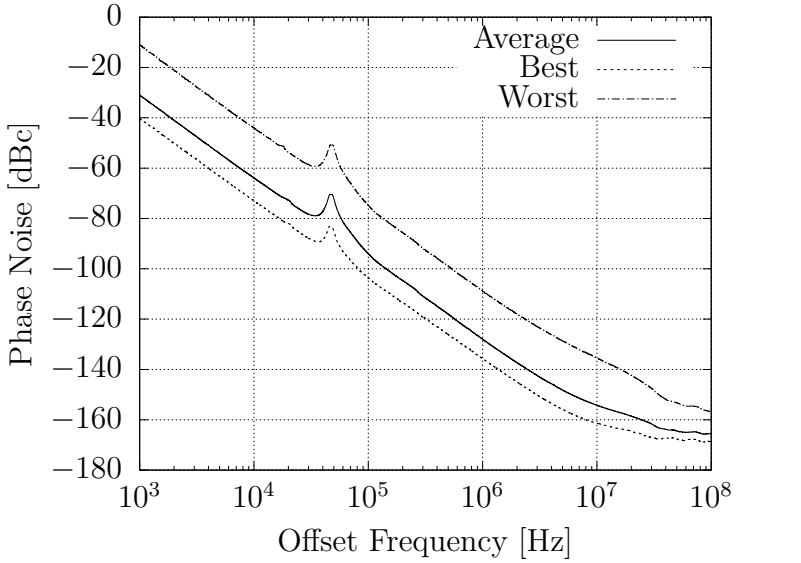

Figure 4.2: The best-, worst-, and average phase noise measured across the entire tuning range from 11.51- to 12.29 GHz. The best phase noise was measured at 11.65 GHz, and is the same as in Figure 4.1, while the worst phase noise was measured at 12.29 GHz. The average phase noise was computed per offset frequency for 13 phase noise measurements with equidistant frequency of oscillation across the entire tuning range.

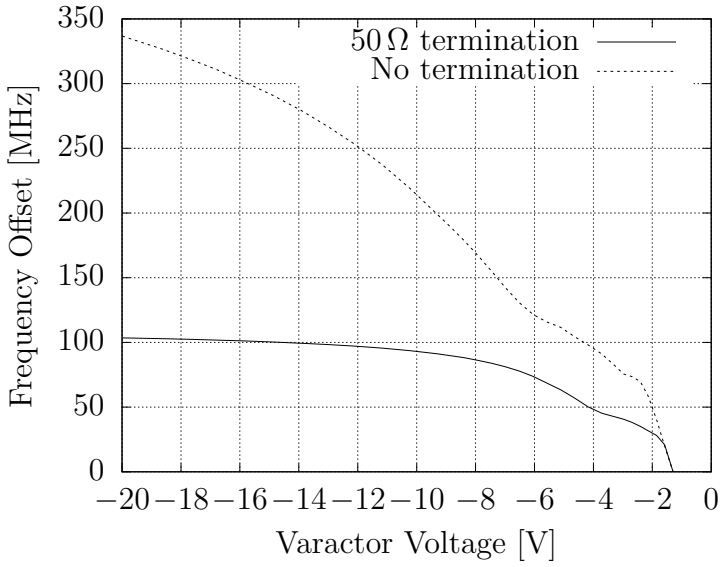

Figure 4.3: Tuning range of the cavity oscillator using the varactor, shown as the offset in oscillation frequency as a function of varactor voltage. The offset is computed from the frequency of oscillation at a varactor voltage of $-1.3\,\mathrm{V}$, since no oscillation occurred above that voltage.

5

Discussion

From the theoretical findings of this project, it appears possible to construct an oscillator with excellent tuning range and phase noise by phase-locking a mechanically tunable cavity oscillator to a lower frequency reference using a varactor. However, the free-running cavity oscillator phase noise shown in Figure 4.1 is clearly far worse than the anticipated phase noise in Figure 3.16. Furthermore, the PLL was not able to lock the phase of the oscillator to the reference. Some likely reasons for these shortcomings are that incorrect assumptions were made in the estimation of the cavity oscillator phase noise, that the layout of the hardware was not ideal, and that incomplete models were used to simulate the system. These possible reasons are explained in detail below, and suggestions on future work and how the system may be improved are presented.

5.1 Oscillator Characterization Assumptions

In the predicted phase noise of the free-running cavity oscillator in Figure 3.16, it was assumed that $f_{\text{flicker}} = 100\,\text{kHz}$, $F = 100$, $P_r = 100\,\text{mW}$, and $Q_L = 1000$. The DC power consumption of 380 mW and $P_r = 100\,\text{mW}$ would suggest a reasonable amplifier efficiency of 26%, but if the flicker noise corner and empirical excess noise figure is extrapolated from the measurements in Figure 4.1, they are closer to $f_{\text{flicker}} \approx 13\,\text{MHz}$ and $F \approx 430$. If these new values are used in Equation (2.32), with $Q_L = 450$ as predicted in Figure B.1b for a $50\,\Omega$ terminated cavity, the modeled phase noise agrees very well with the measured results, as shown in Figure 5.1. The deviation at lower offset frequencies is likely due to additional noise processes not captured in Equation (2.32), such as cyclo-stationary effects or random walk noise sources.

One important thing to note is that the empirical excess noise figure is a catch-all coefficient for any noise source that affects the noise floor, and does not necessarily reflect only the white phase noise sources intrinsic to the oscillator. In this case it is likely that the noise floor was also raised by the long biasing lines and board-to-board connections that resulted from the use of several development boards and custom boards, shown in Figure 5.2. In particular, any voltage noise on the varactor biasing net is directly translated into white phase noise. Tight integration of all components on a single printed circuit board would most likely have resulted in a lowered noise floor.

These results highlight the importance of considering flicker- and white noise from

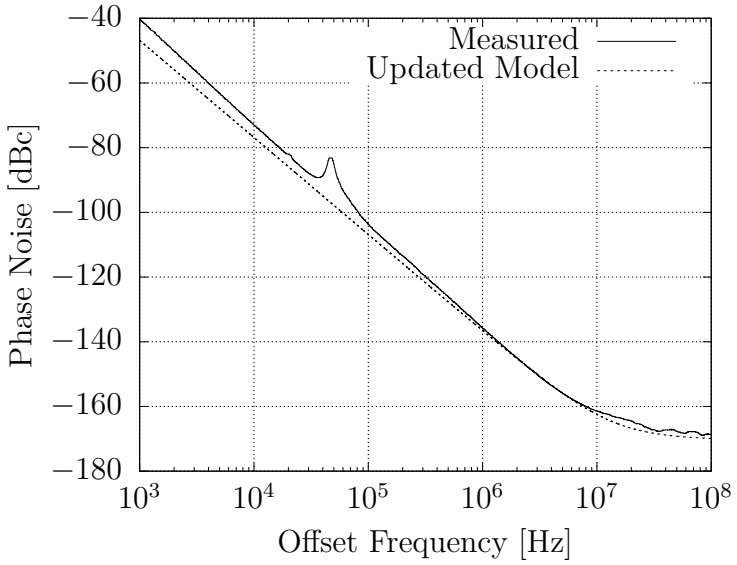

Figure 5.1: Measured phase noise of the free-running cavity oscillator at the best operating point, as in Figure 4.1, and modeled phase noise using Leeson's equation with the adapted values for Q_L, F, and f_{flicker}.

the amplifier, as well as other external noise sources, in the design of the oscillator, as even a resonator with a loaded Q of 3000 would not have yielded particularly impressive phase noise figures in this setup. The noise contribution of the varactor was furthermore not considered, which likely also degraded performance beyond expectations.

5.2 Simulation Model Insufficiencies

One likely reason for why a 50 Ω termination gave better phase noise performance than no termination is that incomplete models were used to calculate the quality factor. When the Q was calculated using the model in Figure 3.12, it was assumed that the varactor would not affect the Q significantly, but if a large portion of the resonating reactance comes from the varactor, meaning that the varactor is strongly coupled to the cavity, the Q would also have been degraded. It is possible that the 50 Ω termination load weakened the coupling between the varactor and cavity, and therefore improved the Q beyond the non-terminated case. Figure 4.3 shows that the varactor offered much less tuning range in the terminated case, suggesting that the termination load did indeed help to weaken the varactor coupling to the cavity.

It would have been beneficial for this project if S-parameters for the varactor in isolation had been available, as the varactor could then have been added to the simulation model in Figure 3.12 to provide more accurate calculations of the resonator Q.

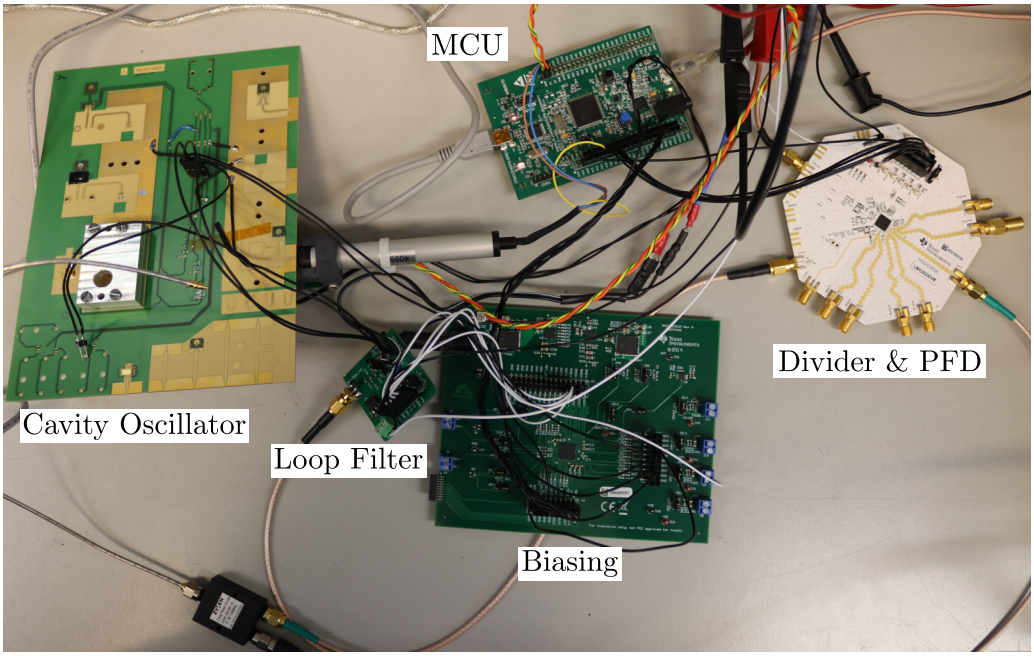

Figure 5.2: Overview of the hardware setup used. The long wires and traces used in the biasing network likely contributed to the raised white phase noise level and PLL instability. Everything is connected as in Figure 3.1.

5.3 PLL Instability

The instability in the PLL control system was most likely a consequence of the long biasing traces and wires, as shown in Figure 5.2. While the control system was designed to have a phase margin of 45°, the substantial inductance and parasitic capacitance of the biasing net may have caused the instability. Since the varactor also looks like a capacitance on the control input, the large inductance in the traces and wires would have resulted in large overshoots and resonant behavior. In order to ensure a stable control system, both the loop filter and PFD should have been placed on a single test board, and the trace length from the loop filter to the varactor should have been minimized.

5.4 Suggested Improvements and Future Work

In order to reach the desired phase noise performance, both the flicker noise corner of the amplifier and the white phase noise level must be reduced. Tighter integration of components would likely help to reduce the white phase noise level, but the flicker noise corner cannot easily be changed for a given amplifier. Use of an amplifier with a lower flicker noise corner would be advised, and for future work it should be evaluated if a different device technology can provide better performance. While GaN HEMT devices can lower the phase noise floor through supplying high power, the performance is lost if the flicker noise and excess noise figure cannot be kept low. An evaluation of noise contribution from the varactor would also be useful in future work, as it was assumed to be noiseless in this project and could have accounted for

a significant portion of the white phase noise.

Another possible improvement would be to use a smaller capacitance varactor, which would provide less tuning range, but also degrade the phase noise less. If design of the varactor had been included in the work, the varactor could then be sized to provide only the tuning range necessary to allow the PLL to compensate for the expected amount of high offset frequency phase noise within the loop bandwidth, while all low offset frequency phase noise and drift would be compensated for by the mechanical tuning.

6

Conclusion

A method for phase-locking a cavity oscillator to a reference oscillator using mechanical tuning of the cavity resonator, as well as electronic tuning with a varactor, has been presented; along with theoretical evidence that such an oscillator system may yield excellent phase noise. A prototype oscillator was also constructed, using a 12 GHz nominal frequency tunable cavity resonator and a GaN HEMT reflection amplifier with an integrated varactor.

The prototype oscillator did oscillate, but performed worse than expected with a phase noise of -103.7 dB at 100 kHz offset, measured at the best operating point. Furthermore, the PLL was not able to lock the phase of the oscillator to a reference due to stability issues in the control system. The oscillation frequency of the free-running oscillator was however tunable from 11.51 GHz to 12.29 GHz.

Three likely reasons for the difference in expected- and measured phase noise were identified. Firstly, poor hardware layout likely caused the PLL instability, as well as yielding additional phase noise. Secondly, incorrect assumptions about the amplifier resulted in very optimistic expectations on phase noise. Finally, incomplete models were used to simulate the oscillator, disregarding any impact on performance from the varactor.

For future studies, an evaluation of how the amplifier and varactor can be designed to minimize phase noise would be beneficial, since it was not done in this project, and it could have a significant impact on phase noise.

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A

Appendix 1

A.1 Loop Filters

The transfer function of a second order loop filter as shown in Figure 2.7 is again given by the complex impedance and can be written as

$$Z_{\text{2nd order}} = \frac{s\tau_1 + 1}{s^2\tau_1 C_2 + s(C_1 + C_2)} \tag{A.1}$$

where $\tau_1 = R_1 C_1$. When $H(s)$ in Equation (2.7) is replaced with $Z_{\text{2nd order}}$, the closed loop system transfer function is given by

$$\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{s\dfrac{K}{C_2} + \dfrac{K}{\tau_1 C_2}}{s^3 + s^2\dfrac{C_1 + C_2}{\tau_1 C_2} + s\dfrac{K}{NC_2} + \dfrac{K}{\tau_1 C_2 N}} \tag{A.2}$$

where $K = K_p K_v$. For a third order loop filter as in Figure 2.7, the transfer from input current to output voltage is no longer given directly by the impedance seen on the input. Computing the transfer function with this in mind gives

$$Z_{\text{3rd order}} = \frac{s\tau_1 + 1}{s^3\tau_1\tau_3 C_2 + s^2[\tau_1(C_2 + C_3) + \tau_3(C_2 + C_1)] + sC_{\text{sum}}} \tag{A.3}$$

where $\tau_3 = R_3 C_3$ and $C_{\text{sum}} = C_1 + C_2 + C_3$. The closed loop system transfer function of a fourth order system is then

$$\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{s\tau_1 K + K}{s^4\tau_1\tau_3 C_2 + s^3[\tau_1(C_2 + C_3) + \tau_3(C_2 + C_1)] + s^2 C_{\text{sum}} + \dfrac{s\tau_1 K}{N} + \dfrac{K}{N}} \tag{A.4}$$

A.2 Error Transfer Functions

The transfer function from input to error is useful to determine what the final error will be and how fast the system converges to a steady state. For a second order system, the error transfer function is given by

$$\frac{\phi_{\text{error}}}{\phi_{\text{in}}} = \frac{s^2}{s^2 + s\frac{KR_1}{N} + \frac{K}{NC_1}} \tag{A.5}$$

For a third order system it is given by

$$\frac{\phi_{\text{error}}}{\phi_{\text{in}}} = \frac{s^3 + s^2\frac{C_1 + C_2}{\tau_1 C_2}}{s^3 + s^2\frac{C_1 + C_2}{\tau_1 C_2} + s\frac{K}{NC_2} + \frac{K}{\tau_1 C_2 N}} \tag{A.6}$$

For a fourth order system it is given by

$$\frac{\phi_{\text{error}}}{\phi_{\text{in}}} = \frac{s^4\tau_1\tau_3 C_2 + s^3[\tau_1(C_2 + C_3) + \tau_3(C_2 + C_1)] + s^2(C_1 + C_2 + C_3)}{s^4\tau_1\tau_3 C_2 + s^3[\tau_1(C_2 + C_3) + \tau_3(C_2 + C_1)] + s^2(C_1 + C_2 + C_3) + \frac{s\tau_1 K}{N} + \frac{K}{N}} \tag{A.7}$$

B

Appendix 2

B.1 Cavity Termination Load Simulations

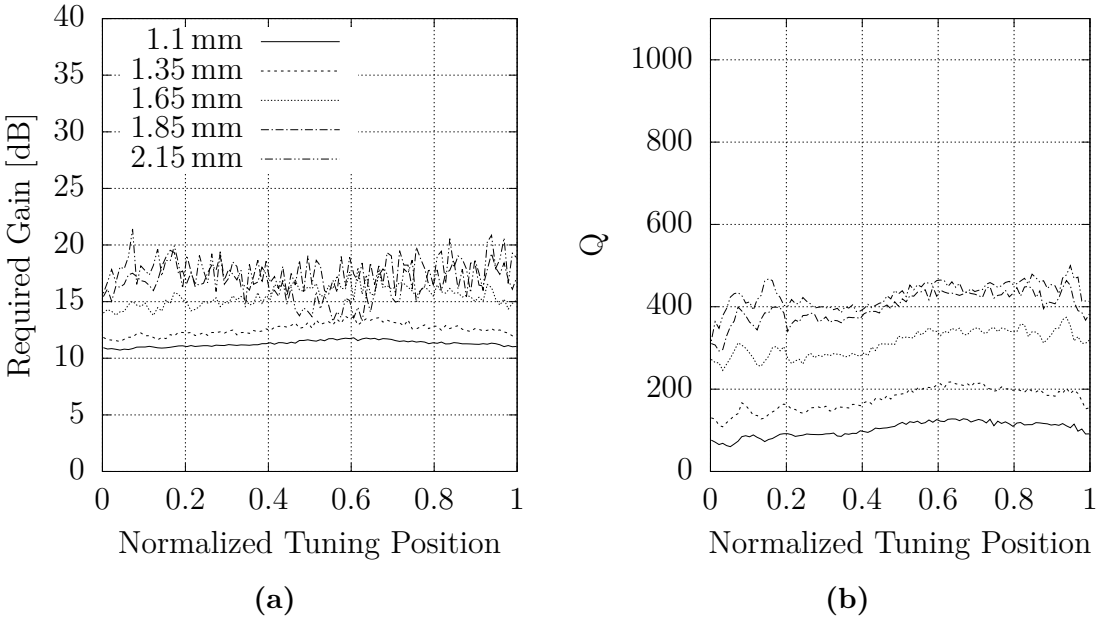

Figure B.1: Simulated amplifier gain required to fulfill oscillation criteria (a) and Q (b) for different probe length and tuning position of the cavity with a 50 Ω termination. The simulated network was modeled as in Figure 3.12.

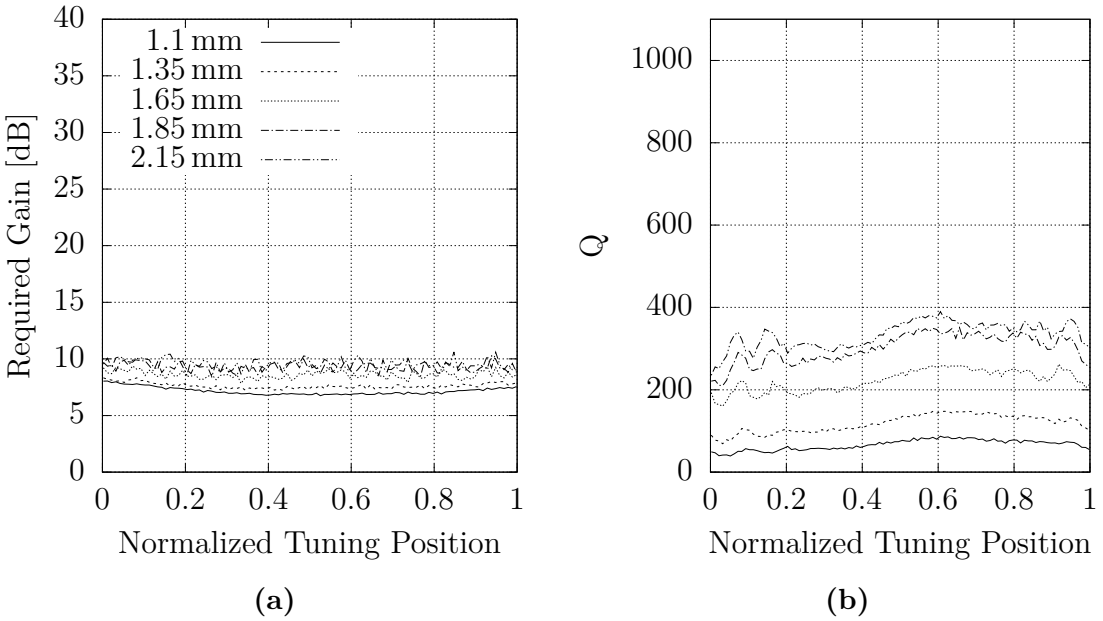

Figure B.2: Simulated amplifier gain required to fulfill oscillation criteria (a) and Q (b) for different probe length and tuning position of the cavity with a 100 Ω termination. The simulated network was modeled as in Figure 3.12.

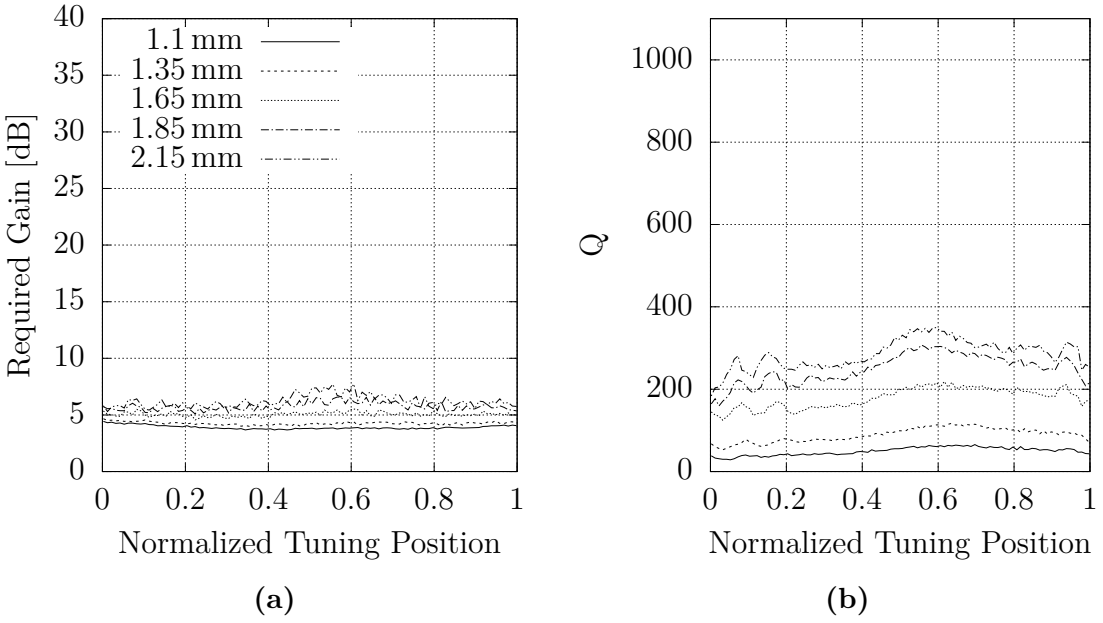

Figure B.3: Simulated amplifier gain required to fulfill oscillation criteria (a) and Q (b) for different probe length and tuning position of the cavity with a 200 Ω termination. The simulated network was modeled as in Figure 3.12.