Design of High Power Density Inverters for Traction Application

Master's Thesis in Sustainable Electric Power Engineering and Electromobility

HARI SANKAR NATESAN SUGUMAR

DEPARTMENT OF ELECTRICAL ENGINEERING

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Hari Sankar Natesan Sugumar

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Supervisor: Nimananda Sharma, Department of Electrical Engineering
Examiner: Yujing Liu, Department of Electrical Engineering

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Department of Electrical Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Sweden
Telephone +46 31 772 1000

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Department of Electrical Engineering
Chalmers University of Technology

Abstract

The shift towards electrification in the automobile industry aims to achieve net-zero emissions by 2050, with electric car sales reaching 10 million in the past decade. Based on the recent trend in automotive, the focus has shifted towards high power density than efficiency to reduce volume, weight, and cost, which may create additional space for batteries as well. A key technology, enhancing power density is the use of wide band gap (WBG) devices, which offer high efficiency, lower switching loss, and faster switching speeds in traction inverters. However, these devices also present thermal challenges and over voltage spikes causing EMI, switching losses and device breakdown due to high di/dt during high-frequency operations.
This thesis work addresses these challenges by first estimating the semiconductor losses and junction temperature using an analytical loss function-based model. Experimental verification of the same is performed with the prototype inverter built with Infineon HybridPack SiC power modules and the challenges are discussed. To mitigate the over voltage spikes, the impact of DC bus bar stray inductance is studied with two different designs, exhibiting a 26% difference in stray inductance. The influence of bus bar stray inductance on switching losses was analysed through switch-level Double Pulse Test (DPT) simulations, inverter-level drive cycle simulations, and experimental voltage overshoot measurements with the prototype inverter.
Key findings reveal that a 26% difference in bus bar stray inductance results in a 3.2% increase in losses for design-1, reduced to 2% with the improved overlap design-2 in DPT simulations. Drive cycle simulations showed similar trends, with a 2.53% increase for design-1 and a 1.14% increase for design-2. Voltage overshoot analysis indicated a 12% reduction in voltage stress on the switch due to reduced stray inductance, consistent across both simulations and experiments. These insights are crucial for designing high power density inverters, allowing for optimized thermal and bus bar designs that minimize voltage stress without compromising efficiency. voltage stress without compromising efficiency.

Keywords: Three phase inverter, Bus Bar, Stray inductance, High power density, inverter loss, Double pulse testing, Voltage overshoot analysis.

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Hari Sankar Natesan Sugumar, Gothenburg, June 2024

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

AC	Alternating Current
AHM	Axially Housing Mounted
ALEC	Aluminium Electrolytic Capacitor
ASM	Axially Stator iron Mounted
AWG	American Wire Gauge
BMS	Battery Management System
CSPR	Constant Power Speed Range
DC	Direct Current
DSC	Double Sided Cooling
DUT	Device Under Test
DWDSCPM	Direct Water and Double Sided Cooled Power Module
EMI	Electromagnetic Interference
EMC	Electromagnetic Compatibility
EV	Electric Vehicle
ESR	Equivalent Series Resistance
FEM	Finite Element Method
FFT	Fast Fourier Transform
GaN	Gallium Nitride
GE	General Electric
GM	General Motors
GTO	Gate Turn-Off Thyristor
HHDDT	Heavy Heavy-Duty Diesel Truck
HDT	Heavy-Duty Truck
HEMT	High Electron Mobility Transistor
HPDD	High Power Density Drive
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
IMD	Integrated Motor Drive
IMMD	Integrated Modular Motor Drive
IPMSM	Interior Permanent Magnet Synchronous Motor

MCT	MOS-Controlled Thyristor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPIMD	Multi Phase Inverter Motor Drives
MPI	Multi Phase Inverter
MPMLI	Multi-Pulse Multi-Level Inverter
MPCSI	Multi-Pulse Current Source Inverter
NCSU	North Carolina State University
OBC	On-Board Charger
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PHEV	Plug-In Hybrid Electric Vehicle
PLECS	Piecewise Linear Electrical Circuit Simulation
PLZT	Lead Lanthanum Zirconate Titanate
PMSM	Permanent Magnet Synchronous Motor
RHM	Radially Housing Mounted
RPM	Rotations Per Minute
RSM	Radially Stator iron Mounted
Si	Silicon
SiC	Silicon Carbide
SWOT	Strengths, Weaknesses, Opportunities, and Threats
US	United States
US DOE	United States Department of Energy
VSI	Voltage Source Inverter
WBG	Wide Bandgap
WLTP	Worldwide Harmonized Light Vehicles Test Procedure

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1 Introduction

1.1 Background

In the perpetual pursuit of sustainable and efficient transportation solutions, the automobile industry is undergoing a paradigm change towards electrification to align with the climatic goals of net zero emissions by 2050 [1]. According to Fig. 1.1 from the International Energy Agency, electric car sales spiked tenfold from 2012 to 10 million during the last decade, demonstrating the demand as well as customer interest in electric vehicles.

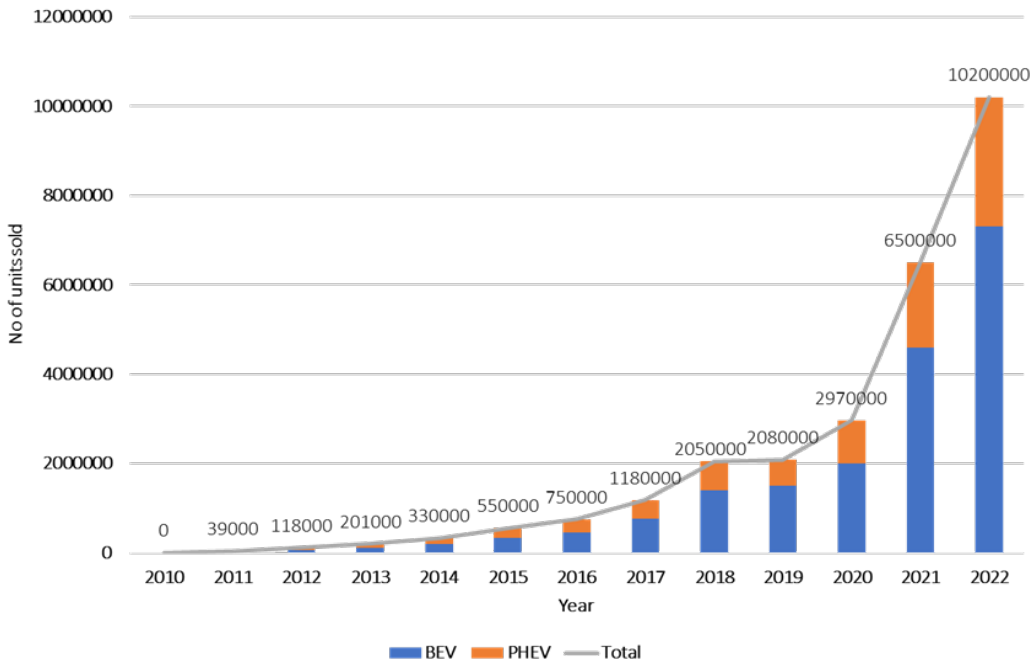

Figure 1.1: Worldwide EV cars sales from 2010 to 2022 [2]

Along with a growth in market demand and sales of electric cars, end customers' expectations for vehicle performance, range, cost, and charging time are also rising. Fig. 1.2 (left) depicts the shift of the average range growing from 127 km to 349 km during the last decade.Fig. 1.2 (right) depicts a comparison of acceleration specifications between the initial and current models of three major EV manufacturers, demonstrating a significant decrease in acceleration. Achieving acceleration poses a challenge without concurrent enhancements to battery and drive train specifications. However, augmenting these specifications inevitably results in a proportional

increase in both volume and weight, thereby directly impacting the overall range of the vehicle.

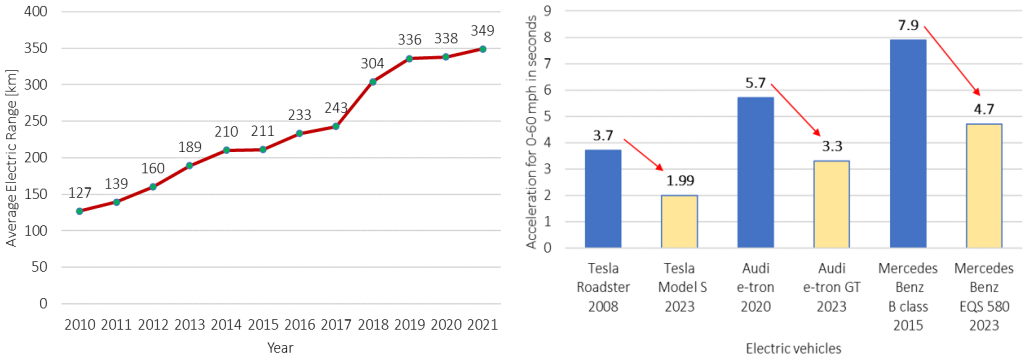

Figure 1.2: Trend of Electric vehicle Range (left) and Acceleration (right) over years

The key for achieving these performance requirements such as acceleration, and grade-ability along with range is to have a cutting-edge electric drive system with high power density. Hence, this study explores the state-of-the-art methods and opportunities to achieve high power density drives including the modelling and experimental verification of 2-level 3-phase and 6-phase inverter topologies, Thermal study with 6-phase radially integrated inverter topology which is briefly described in the Aim section.

1.2 Aim

The aim of this master thesis is to design the high power density inverter for traction application. Hence, this work focuses on exploring different technologies to enhance high power density inverter, Three-Phase Inverter Modelling and Experimental Verification and Analysis of DC Bus Bar inductance in 2-Level 3 phase inverter performance.

1.3 Scope

The scope of this work is to explore, model and experimentally verify methods to achieve high power density drives for traction applications through the below mentioned chapters.

1. Review of High Power Density Inverters

This chapter studies and summarizes the various high power density enabling technologies such as wide band gap devices, cooling methods, high-speed machines, integrated drives, passive component sizing, and inverter topologies to understand the opportunities.

2. Three-Phase Inverter Modelling and Experimental Verification
This part focuses on the implementation of three phase inverter in Simulink PLECS and implementation of an analytical loss function model of a MOSFET. Estimation of inverter losses and junction temperature measurement will be accomplished with both the simulation models and the losses will be experimentally verified and compared with the simulation results.
3. Analysis of DC Bus Bar inductance in 2-Level 3 phase inverter performance
This part studies the impact of stray inductance using two bus bars with 26% difference in stray inductance through a double pulse test simulation and an analytical loss function based drive cycle simulation. In addition to that the stray inductance impact is verified by conducting a voltage overshoot analysis in both simulation and experiment.
By addressing these interconnected aspects, the master thesis aims to provide a holistic understanding of power density enhancement in inverters for traction applications.

1.4 Limitations

In this thesis, the junction temperature measurement of power module was done experimentally which was not accurate with respect to the losses estimated in the power measurement. This has occurred since the temperature sensor was not placed near the MOSFET chip inside the Infineon SiC power module instead it was placed near the diode. This information was known at the final stages of the thesis. Hence, heatsink design was not discussed in detail in the thesis.

2

High Power Density Drives

At the core of all electric drive systems, is one or more traction machines that drive the entire vehicle. To control and drive them, A traction inverter is required to convert the DC power from the EV battery to a variable frequency alternating current dependent on the vehicle speed and drive torque. The power density of the drive system is an important aspect as it affects the vehicle's energy consumption, consequently affecting the driving range. To steer the importance of electrification and high-power density drives in the mass market, the US Department of Energy has set technical targets for light duty EVs for 2025. In that, target power density of 33 kW/L for electric drive and 100 kW/L for power electronic components are set to achieve by 2025 [3]. Fig. 2.1 summarizes the power density of various EV traction inverters [4] available in the market with various OEM vehicles. As can be seen, the power density of EV inverters has increased by more than 500% in the last two decades.

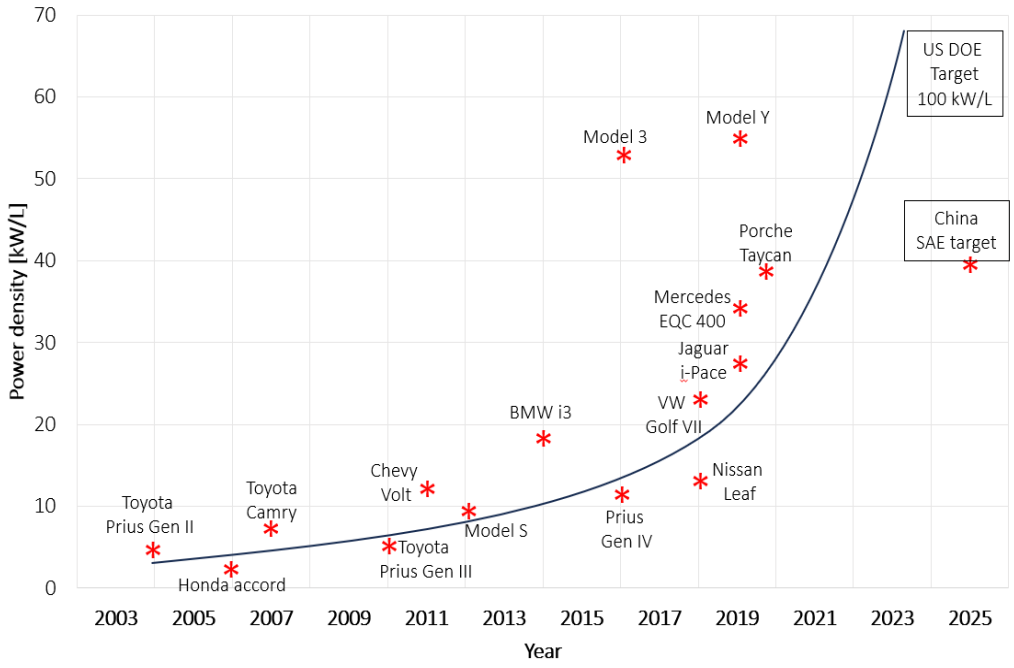

Figure 2.1: Power density Trend of various EV traction inverters

There are multiple technologies that enabled this increase in power density which are summarized in Fig. 2.2. As can be seen, the efforts are either put on the drive inverter or the electric machine. In some cases, it could be both, e.g., integrated

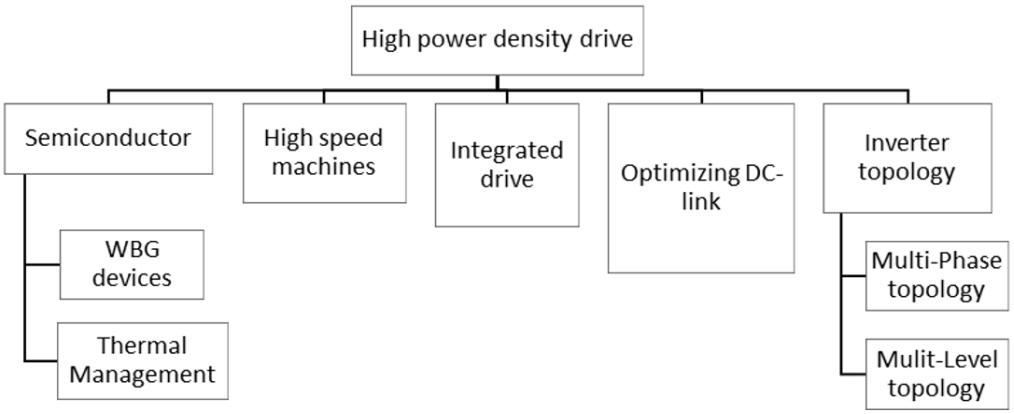

Figure 2.2: Enabling technologies for high-power density drive

drive. In the following sections, each enabler technology is discussed in detail.

2.1 Semiconductors

The key active components in an inverter are the semiconductor switches. Two leading semiconductor technologies are commonly used in traction drives, Si IGBT and SiC MOSFET. They are central to the performance and power density of inverters. Selecting the right semiconductor devices, managing their thermal characteristics, and optimizing their operation are critical factors in achieving high power density and efficiency.
There are various actively switched semiconductors such as MOSFET (Metal Oxide Semiconductor Field Effect Transistor), IGBT (Insulated Gate Bipolar transistor), GTO (Gate Turn-Off thyristor), IGCT (Insulated Gate Commutated Thyristor) and MCT(MOS controlled thyristor), available in the market for various applications. Comparing all these, MOSFET and IGBTs are having a number of applicational advantages such as active turn-off even at short circuit events, operation without snubbers, simple control, faster switching speeds and relatively lower switching losses.
The below section discusses,
a) A brief description of those key semiconductor switches,
b) How different semiconductor materials, such as Si, SiC, and GaN (WBG Devices) affect inverter switching performance in terms of losses and switching speeds and enhances the inverter to be a high power density drive,
c) Pros and cons of using the switches in discrete and modular form as power density enablers is also discussed.

Key Semiconductor devices:
MOSFET – Metal-Oxide-Semiconductor Field Effect Transistor
MOSFET is a three terminal (Gate, Source, Drain) voltage controlled unipolar semiconductor device which requires continuous application of a gate source voltage to be in On-state. Since it is a majority carrier device MOSFET has faster switching speeds and it's on state resistance has a positive temperature co-efficient which makes it easy to parallel for current handling capability [5].

IGBT – Insulated Gate Bipolar Transistor
Like MOSFET, IGBT is also a three terminal (Gate, Collector, Emitter) voltage controlled semiconductor but Bipolar device. Best qualities of MOSFET and BJT (Bipolar Junction Transistor) were combined together to make IGBT. So, the switching speed of IGBT is faster than a BJT and slower than a MOSFET [5].

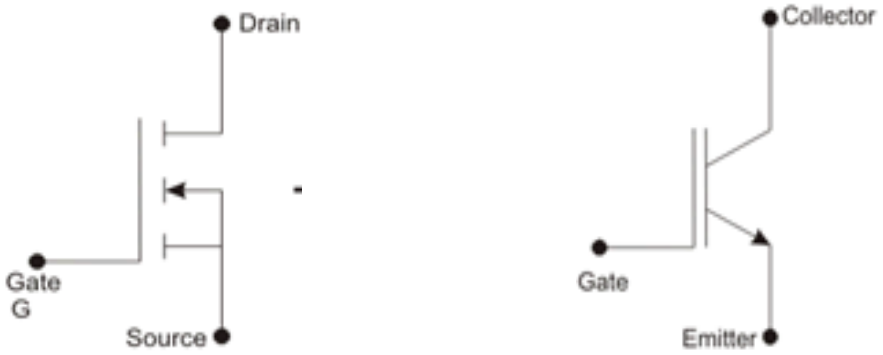

Figure 2.3: Pin configurations of left: MOSFET and right: IGBT

2.1.1 Wide Band Gap devices

The evolution of semiconductor technologies, driven by the need for smaller structures and precise process control, has pushed the boundaries of modern semiconductors beyond traditional silicon-based switches. This progression has led to the emergence of wide band gap materials like Silicon Carbide (SiC) and Gallium Nitride (GaN). These materials offer advantages over silicon, including higher energy gaps between valence and conduction bands, resulting in lower on-state losses and switching losses, as well as better heat conductivity [6].

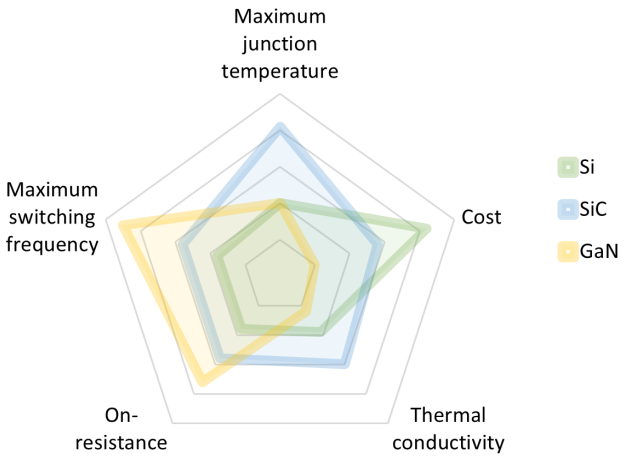

Figure 2.4: Comparison of key parameters of semiconductor materials [7]

In Fig. 2.4 Comparisons of GaN, Si, and SiC reveal varying attributes such as on-

state resistance, thermal conductivity, maximum junction temperature, maximum operating frequency, and cost. GaN demonstrates superiority in on-state resistance, with lower values compared to SiC and Si, making it a dominant parameter in this aspect. SiC emerges as a frontrunner in terms of thermal conductivity and maximum junction temperature, boasting the highest thermal conductivity and junction temperature around 175°C to 200°C compared to Si and GaN. Additionally, GaN exhibits a significantly higher operating frequency than Si and SiC, extending into the MHz range, which is advantageous for applications requiring high-speed operations. However, GaN faces challenges such as high electromagnetic interference, gate ringing [10], and oscillation due to parasitic effects. Thus, while GaN and SiC represent promising alternatives to traditional silicon, each comes with its own set of advantages and challenges in the realm of semiconductor technology.

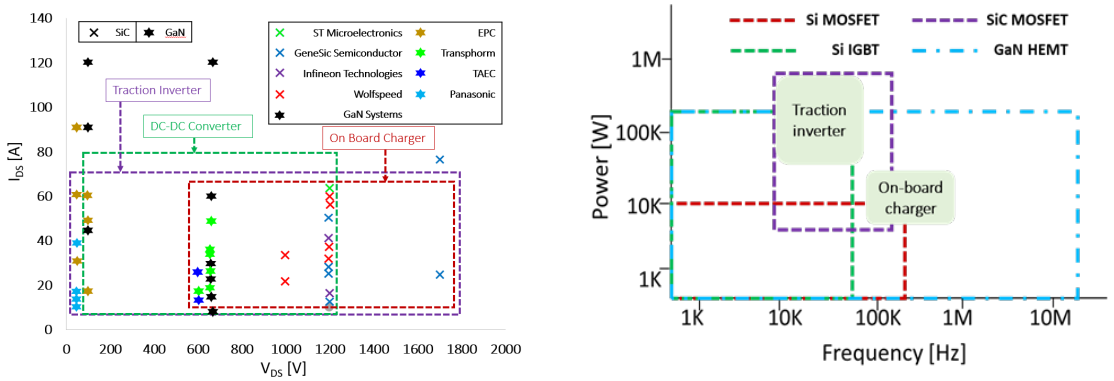

Figure 2.5: (a) Drain source voltage and current (Left), (b) Power and frequency envelop of power semiconductor in automotive application (Right) [7]

Fig. 2.5 (a) depicts the device voltage and current rating of several EV components such as the on-board charger, traction inverter, and DC/DC converter. It is seen that Silicon Carbide (SiC) can operate at higher voltage levels but lower frequency levels, whereas Gallium Nitride (GaN) operates only upto 650 V but excels in high frequency operation. Looking at the merits and challenges in the WBG devices, Studying the application of WBG devices in electric vehicles (EVs) is of a better idea, especially when considering the power ratings of various power electronic interfaces within an EV. In power electronics point of view, An EV power train consists of a traction inverter, a primary DC-DC converter, and a Battery Management System (BMS) interface, all of which are high-power components ranging from 60 to 150 kW [42]. For the On-Board Charger (OBC), designs range from 22 kW [43] for rapid charging to 43.5 kW [44] for AC charging. So, considering this, SiC devices may be utilized for high power/voltage components such as traction inverter, BMS, and fast charging. On-Board Chargers and GaN devices are ideal for low or medium power/voltage charging and auxiliary load components in an EV [45].

2.1.2 Advanced Packaging

The power semiconductor packaging can be categorized into discrete and modular. A comparison of the two packaging methods is summarized in Table 2.1. The discrete devices can provide more flexibility in overall inverter design and cost reductions. Although, some manufacturers like Tesla have used discrete SiC devices in their traction inverter, the modular design of the power semiconductor seems to be dominant due to improved layout and minimized design efforts [11]. More advanced designs such as integrated sensing, double sided cooling etc. makes the modular design more attractive. In 2-level configuration both half-bridge and six-pack power modules are readily available. The half-bridge module provides more flexibility in lay outing compared to the six-pack modules.
Because of this, integrating capacitors reduces the power loop parasites, suppresses the over voltage and improves the current sharing among parallel devices. Integrating gate driver reduces the gate driving loop inductances. Integrating capacitors in power module captures high frequency harmonics directly at source and integrating heat sink to the base plate of the module directly improves the thermal performance of the inverter. Finally integrated current, voltage and temperature sensors allows faster reaction in case of failure and more accurate information [12]. Enhancements of this advanced packaging and modular technologies into incorporation of cooling technologies are discussed in the next section.

S.No	Discrete design	Modular design
1	High flexibility in design	Natural separation of electrical and cooling paths provides a much lower risk of dust entering the electrical parts and has a much easier air-flow design.
2	More feasible solutions for cost-optimised design	Reduces risks due to lesser design efforts.
3	Relatively easy for second sourcing strategies	Improves current sharing by device paralleling inside module.
4	Risk of increased parasitic effects while integrating	Isolation between heat sink and high voltage contacts
5	-	Optimised layouts for minimised parasitic effects
6	-	More expensive for the same device rating

Table 2.1: Key details of modular and discrete design [9]

2.1.3 Advanced Cooling Technology

Power modules are the heart of the inverters that need to be operated under a safe temperature to maintain the best system efficiency, High Power density and a better reliability. Traditional single-sided cooling methods [4] prevalent in automotive applications present limitations for Si IGBTs and SiC power devices, characterized by higher parasitic inductance (15-20 nH) [12] and thermal resistance (0.1-0.8 K/W) [14]. Improvements in thermal resistance will help in reducing the volume of semiconductors which leads to reduction in overall packaging size. Technical advancements on direct liquid cooling [15] , advanced bonding techniques [16], transfer/injection mold [17], copper bonding [18] and micro and meander channel networks [19] helps to reduce the thermal resistance. Wire bonding, a standard interconnect approach in single-sided cooling, poses challenges including large parasitic parameters and susceptibility to thermal stress[20]. So, these wire bonds are resistant to heat dissipation in the top side of the power modules, refer Fig. 2.6. Planar interconnect techniques [21] facilitate double-sided cooling configurations, enabling heat dissipation on both sides of the semiconductor, potentially reducing thermal resistance by up to 50% [22].

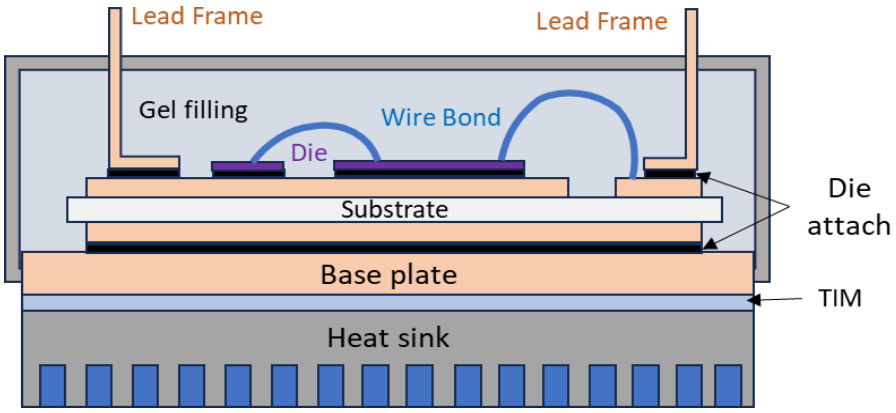

Figure 2.6: Structure of the single sided cooled power module [4]

In the past decade, double-sided cooling methods have garnered significant interest for enhancing inverter power density. Early explorations, initiated around 1995 [23], capitalized on planar interconnect technologies, demonstrating improvements in thermal resistance, stray inductance, switching losses, and current handling capabilities compared to single-sided cooling. The table 2.2 clearly shows the benefits from the early explorations done by the industries and research institutions.

Supplier & Technology	**Year**	**Voltage [V]**	Current [A]	**Thermal resistance** [K/W]	**Remarks**
Single sided Cooling for reference	-	-	-	0.1-0.8	1) Inductance 15nH to 20 nH
GE (Power overlay)	1995	1200	200	0.076 (40%↓)	1) Inductance 60%↓ 2) Voltage overshoot 40%↓ 3) Switching losses 22%↓ 4) Electrical resistance 70%↓
Boeing	2002	1200	25	20%↓	-
IR (CooliR2)	2010	650	300	30-39%↓	1) Inductance 12 nH 2) Max current capability 30%↑ 3) IGBT switch current rating 61% ↑
Semikron (skiN)	2011	600	400	0.44 Kcm2/W (35%↓)	1) Reliability x200↑ 2) Surge Current limit 27% ↑ 3) Stray inductance less than 1.4 nH
ABB	2011	1200	600	-	1) Output current 35%↑
Siemens (SiPLIT)	2012	-	-	0.321-0.345 (15%↓)	1) Inductance 6 nH 2) Reliability ↑
NCSU (PCoB)	2016	1200	100	0.5	1) Inductance 8 nH

Table 2.2: Performance of double sided cooling–early exploration phase [4]
Table Notes:
1) Comparisons made with % in table are with the conventional single sided cooling,
2) Data is not available wherever "-" is mentioned in the table

Commercialized double-sided liquid-cooled packages have witnessed substantial advancements in automotive applications, driven by leading industrial suppliers seeking enhanced performance and efficiency. Denso and Toyota pioneered the adoption of double-sided liquid cooling, implementing the first module in MY2008 Lexus LS 600h [24]. This innovation led to a remarkable increase in maximum switch current from 200 A to 300 A, coupled with a reduction in the number of switches from 40 to 24, aligning with inverter targets.

Subsequent developments, such as the MY2016 Toyota Prius Gen 4, introduced a 2-in-1 power card, consolidating two pairs of power IGBTs into one unit to con-

Supplier & Technology	**Voltage [V] & Current [A] & Max Temp [°C]**	**Application readiness**	**Thermal resistance K/W**		**L stray**
			J-C	**J-F**	
Denso	-	MY2008 Lexus LS600h	-	0.203-0.225	-
		MY2016 Toyota \Gen4 Prius	-	-	55% ↓
Delphi Viper	-	MY2016 Chevrolet Volt	33%↓	-	-
Hitachi DWDSCPM	-	MY2016 Cadillac CT6	35%↓	-	25% ↓
Infineon DSC	-	Available for usage	0.11	70%↓	13 nH (40% ↓)
Infineon DSC S1	700 & 400 & 175	Available for usage	0.1	0.24	15 nH
Infineon DSC S2	750 & 450 & 175	Available for usage	-	-	-
Infineon DSC L	700 & 200 & 150	Available for usage	0.18	0.35	20 nH
On semi Conductor VE-Trac Dual	750 & 550 & 175	Available for usage	0.05	0.14	8 nH
CRRC-Dynex	650 & 600 & 175	Available for usage	0.018-0.03	0.089 - 0.094	4.6 nH
BYD	1200 & 200 & -	Available for usage	-	-	-

Table 2.3: Performance of double sided liquid cooling – Commercially available modules [4]
Table Notes: 1) Comparisons made with % in table are with the conventional single sided cooling, 2) Data is not available wherever "-" is mentioned in the table

struct two three-phase inverters with only 7 switches, consequently reducing the power stack size by 22%. Delphi's 'Viper' technology, introduced in 2008, marked a significant departure from wire bonds, employing flip-chip soldering techniques to enhance current distribution and lifespan, resulting in a notable reduction in thermal impedance by 33% [26],[27] by 2016. Later stages, Delphi demonstrated power module packaging with 650 V, 500 A and 1200 V, 480 A which had achieved 45 kW/L and 58 kW/L of power densities respectively. Hitachi's DWDSCPM (Direct Water Double sided cooled Power Module) method [28],[29], introduced in 2013, exemplified a novel approach to direct cooling with a 2-in-1 configuration, signifi-

cantly reducing (40%) volume usage and thermal resistance (0.17 K/W) , thereby finding application in MY2015 Mercedes Benz S500 PHEV and MY2016 GM Cadillac, enhancing inverter power density to 23 kVA/L [30],[31]. Infineon's integrated power module [34] , launched in 2015, integrated double-sided cooling with insulation and sensor technologies, achieving substantial reductions in thermal resistance (0.11 K/W,70% reduction), paving the way for the commercialization of the HybridPack DSC-SFF400R07A01E3 [35] in 2017.
Semiconductor manufacturers like ON Semiconductor and Dynex Power contributed wire-bondless half-bridge configurations, reporting lower stray inductance (7 nH) and thermal resistance (0.05 K/W [36] & 0.094 K/W [37]) thereby enhancing power density in the inverter by 30%. BYD is also working on Si and SiC based double sided cooling methods [40]. Comparing with the single sided cooling, double sided cooling shown a significant difference in terms of improving the electrical parasitic, semiconductor utilization, Effective heat dissipation and finally the power density of inverters also in high terms.

2.2 Integrated drive topologies

Traditional motor drives kept the motor, inverter and driver boards separately, which increases the total weight, volume, and reduces the power density of the system. Furthermore, the drive units are linked to the motor via lengthy cables, resulting in additional losses and electromagnetic interference. Physically integrating the inverter and electric machine is an effective way to improve power density of the drive. This is referred to as an integrated motor drive system and has been studied in the literature. The recent advancements that was seen in the previous sections in the domains of WBG devices and semiconductor cooling technologies can help in the performance enhancement of Integrated Motor Drives.

The table 2.4 outlines three generations of Integrated Motor Drives (IMDs) and their respective characteristics. The first generation IMDs entail integration with independent housings for the motor and inverter, with the inverter mounted atop the motor using a contact plate. This design offers a straightforward structure without requiring modifications to the motor design, thereby enhancing power density. However, limitations arise concerning volume optimization due to restricted changes, and concerns persist regarding heat dissipation and electromagnetic interference (EMI). In contrast, second-generation IMDs represent a notable advancement, placing the inverter within the motor housing itself, either mounted on the stator iron or the end plate inside the housing. This configuration eliminates the need for external cables, leading to reduced volume and size compared to first-generation IMDs. Despite these advantages, second-generation IMDs present complexities in design, incur higher manufacturing costs, and encounter challenges related to serviceability and heat dissipation, albeit to a lesser extent than their predecessors. Meanwhile, third-generation IMMDs, characterized by modular units integrating motor stator poles, inverters, and controllers, offer high integration and power density. They boast lower manufacturing and maintenance costs and longer service lives. However, their design complexity contributes to heightened heat dissipation and EMI

concerns, underscoring the trade-offs between integration and performance.

A	1st Gen IMDs	2nd Gen IMDs	3rd Gen IMMDs
B	1) Integration with independent housings for motor and inverter 2) Inverter mounted on top of the motor with a contact plate	1) Integration of inverter and controller inside the motor housing 2) Allows to mount the inverter on stator iron or on end plate inside housing	1) IMMD - Integrated Modular Motor Drive Motor drive comprising multiple modular units, each module having a single motor stator pole, Inverter and a controller
C	1) Simple design structure 2) No motor design modification required 3) Improved power density	1) Reduced volume and size than 1st Gen IMDs 2) Cable usage is eliminated completely	1) High integration and high power density 2) Lower manufacturing and maintenance cost 3) Longer service life
D	1) Volume optimisation is limited due to changes are limited 2) Heat dissipation and EMI issues	1) Complex design 2) Higher manufacturing cost 3) Not easy to service 4) More heat dissipation and EMI issues than 1st Gen IMDs	1) Complex design 2) heat dissipation and EMI issues

Table 2.4: Advantages and disadvantages of different generations of integrated drives, A: Topology, B: Description, C: Advantages, D: Disadvantages [46]

All three generations of integrated motor drives can be categorized into four groups, based on the positioning of the inverter integrated with the motor housing, as shown in 2.7. The 1st-generation IMDs, RHM and AHM, feature inverters mounted externally to the motor housings. Both of these configurations offer enhanced feasibility for facilitating the cooling process of both the motor and the inverter. The radially integrated type (RHM & RSM) is particularly well-suited for high-speed motors, where the machine's stack length is longer than the diameter, enabling a rotor with reduced inertia and thereby creating additional axial space for a gearbox. Conversely, the axially integrated type (AHM & ASM) is most advantageous for high-torque motors, presenting an alternative to the radially integrated approach. Although both ASM and RSM drive configurations introduce a higher degree of integration and amplify power density, managing thermal issues becomes challenging due to constrained space and elevated ambient temperatures [46].
Commercially available integrated drives primarily embrace the RHM and AHM types due to their straightforward integration methodology. Siemens [47] and Nidec [48] have successfully reduced drive weights by 10-15% and 31%, respectively, com-

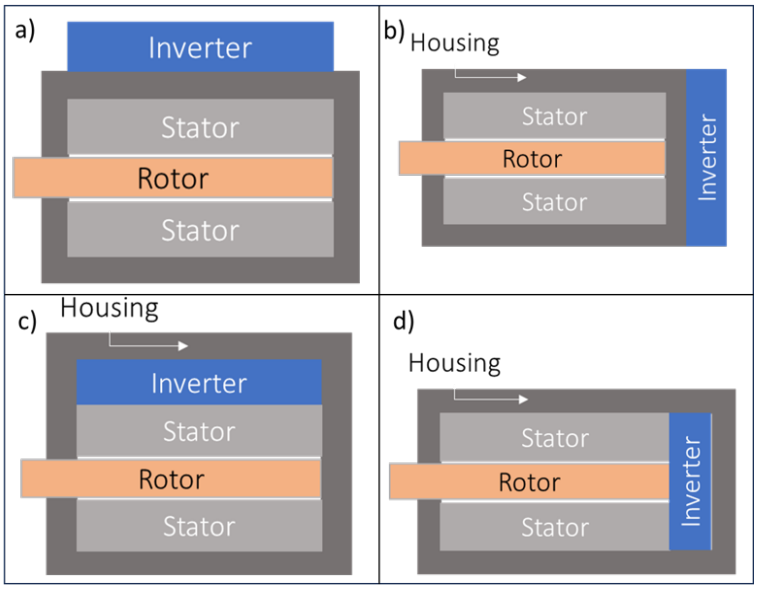

Figure 2.7: Conceptual images of various methods of integrating electric machine and inverter, a) RHM, b) AHM, c) RSM, d) RSM

Topology	**Examples**
Radially Housing Mounted - RHM	1. Allen-Bradley 1329I 2. Varmeca 30
Axially Housing Mounted - AHM	1. Tesla Model 3 2. Segment inverter IMD
Radially Stator iron Mounted - RSM	1. SPM IMD 2. Axial flux IMMD 3. Aviation IMMD
Axially Stator iron Mounted - ASM	1. Matrix converter IMMD 2. 5-Phase integrated SRM 3. GaN IMMD1 4. SPM IMMD 5. PMSM IMMD

Table 2.5: Examples of various methods of integrated topologies [46]

pared to conventional drive systems with their RHM designs. Manufacturers are currently exploring the integration of wide-bandgap devices and advanced cooling techniques to implement the stator-iron-mounted type, which promises higher power density but entails complex thermal management processes.

2.3 High Speed Machines

One of the approaches to increase the power density of the drive is to focus on increasing the power density of electric machine by increasing the electric machine speed. The design trend over the years shows interest to increase the maximum speed to increase the torque and power density of the machines since this will help in enhancing the packaging of the machine and efficiency as shown in Fig. 6 [52]. In the last decade, the maximum speed of the electric machine has increase by 50% and is expected to double according to US DOE targets.

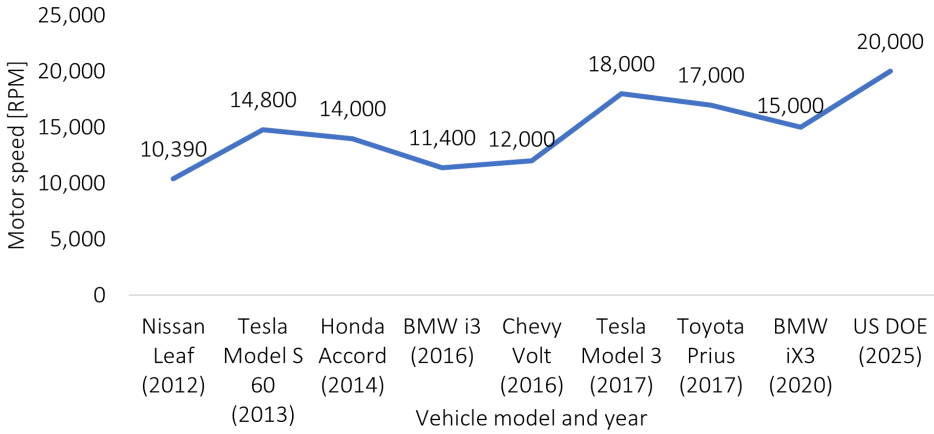

Figure 2.8: Design trend of electric machine maximum speed over the years [52]

Two of the key enablers for increasing the maximum speed of electric machine in automotive are higher battery voltage and use of SiC MOSFETs [52]. A higher battery voltage allows to have a higher maximum speed without increasing constant power speed range of the electric machine. Additionally, due to the higher switching frequencies possible with SiC MOSFETs, current control is possible at higher fundamental frequencies. Therefore, the electric machine speed can be increase without changing the number of pole-pairs.
In [66], the authors have designed four different machines with identical power rating and maximum speed of 12000 to 50000 RPM. The impact of increasing the maximum speed on the power density, volume and mass of the powertrain is studied and the results are summarised in Fig. 2.9. Increasing the maximum speed of electric machine leads to reduce size and less active materials. However, it places more burden on the transmission because the gear ratios increase with the speed. A higher gear ratio requires more gears reduction stages leading to bulkier transmission. From Fig. 2.9, it can be observed that the increase in transmission weight is offset by reduction in mass of electric machine. Therefore, the total mass of the powertrain shows a decreasing trend, and the gravimetric power density increases with speed. However, this is not true for volume of the powertrain. Beyond 30000 rpm, the increase in transmission volume is not offset by reduction in electric machine and hence the total transmission volume is increasing. This in turn results into a maximum volumetric power density at 30000 rpm.
Though increased maximum speed helps in enhancing the power density and re-

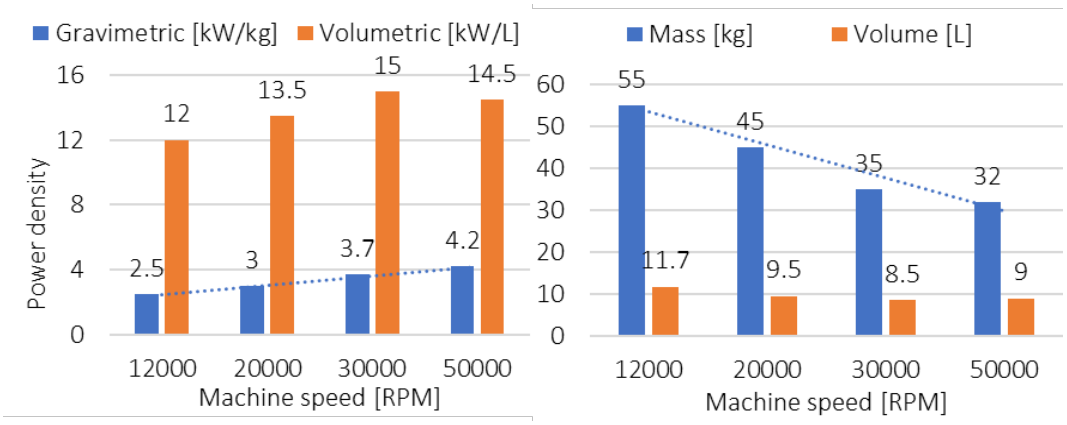

Figure 2.9: (Left) Power density, (Right) mass and volume of electric powertrain for various electric machine maximum speed [66]

duce system mass, the burden then falls on the transmission system which must be changed accordingly with respect to machine speed. The limitation on the maximum speed comes from the high frequency motor losses and transmission system constraints. The gears may require special coating to operate at higher speed. Though we expect to reduce volume for higher power density, the motor should meet the constant power speed range (CSPR) to maintain a single-gear transmission which would help in improving the transmission power density as well.

2.4 Optimising DC link

2.4.1 DC Link capacitor sizing

The DC link capacitor plays a crucial role positioned between the high voltage battery and traction inverter, tasked with suppressing the high-frequency current component and ensuring voltage stability [49]. For a three-phase VSI, the DC-link capacitor may draw up to 60% of the RMS load current [51], necessitating the storage of a significant amount of energy to maintain voltage stability, thereby occupying a substantial space (approximately two-thirds [50]) of the inverter's total size. This poses a significant challenge in enhancing inverter power density.

DC link capacitors can be broadly categorized as electrolytic and electrostatic capacitors. While electrolytic capacitors are commonly utilized in conventional motor drive applications, their limitations in current capability, lifespan, and low-frequency operation render them less desirable for traction inverter applications. In contrast, non-polar electrostatic capacitors employ polymer/plastic film or ceramic dielectric mediums. Film capacitors offer superior reliability, current handling, high-frequency operation, and lower losses compared to Aluminum Electrolytic Capacitors (AlEC). However, due to their lower relative permittivity, film capacitors are bulkier [52] and require additional cooling since their operating temperatures of commercially available capacitors are up to 125°C [53]. Ceramic capacitors, on the other hand, emerge

as promising options for traction inverters due to their higher RMS current rating and temperature limits compared to film capacitors. Classified based on dielectric material, ceramic capacitors are categorized into Class 1, Class 2, and PLZT (lead-lanthanum-zirconate-titanate). Class 1 capacitors find suitability in tank circuits and filter applications requiring constant capacitance, while Class 2 capacitors offer higher energy density, making them ideal for DC link applications. The most commonly used Class 2 capacitors, based on barium titanate, exhibit high temperature dependency and reliability concerns due to their rigid structure. However, PLZT-based capacitors feature an anti-ferroelectric dielectric material, providing superior current, temperature, frequency operation, and reliability characteristics [54].

While ceramic capacitors enhance inverter power density, their brittle nature poses challenges in manufacturing large blocks like film and AlEC types. Consequently, multiple capacitors are often required for DC-Link applications, leading to packaging difficulties. Additionally, parallel capacitor branches may cause current asymmetry, and layout inductance may result in voltage overshoot. Hence, selecting capacitors entails a trade-off based on system requirements, each possessing its own set of advantages and disadvantages. Various techniques exist to minimize capacitor volume, including the implementation of multi-phase topologies and segmented inverter types, which will be elaborated upon in the subsequent section on inverter topology.

2.4.2 DC Link Bus bar design

In inverter applications, the DC link bus bar or cable, which is assembled alongside the DC link capacitor, is critical for achieving lower voltage overshoot during switching, reducing electromagnetic interference (EMI), and minimizing switching losses [52]. As discussed in the previous sections, the faster evolution of WBG devices which can operate in higher frequencies with higher dv/dt can cause higher voltage overshoot in the presence of parasitic inductance in the bus bar. So, The design of the DC link bus bar must address considerations across three multi-physics domains: electrical, thermal, and mechanical. The following table 2.6 outlines the guidelines and requirements necessary for designing a DC bus bar that supports high power density.

In the conventional approach, laminated bus bars are commonly employed in inverters due to their lower parasitic inductance, which helps reduce voltage overshoot, electromagnetic interference (EMI), and switching losses [59], [60]. However, with the advancement of wide-bandgap (WBG) semiconductors and the growing need for higher power density, there is a demand for increased integration and packaging of passive components. This requirement can be effectively addressed through the adoption of PCB-based bus bar architectures which were discussed in [61]-[64] since they offer a lower inductance in the range of 10 nH.

S.No	Domain	Design requirement	Design guideline
1	Electrical	Lower ESR and lower ESL for lower voltage overshoots and lower di/dt	Shorter commutation loop lengths ensuring proper thermal requirements
2	Electrical	Maximizing magnetic field cancellation between positive and negative bus bars	1. Closer placement of bus bar layers ensuring proper isolation requirements 2. Symmetrical distribution of components for balanced design
3	Thermal	Lower temperature rise due to maximum RMS current through bus bar	Active cooling strategies or ensuring convective natural cooling is sufficient
4	Mechanical	Robustness against shock and vibration	Robust mechanical design
5	General	Higher level of integration and packaging	PCB based bus bar architecture is suggested from literature

Table 2.6: DC Link bus bar design requirements and guidelines [52]

2.5 Inverter Topology

Solutions based on wide band gap (WBG) devices, advanced thermal management, and high-speed machines provide substantial improvements in achieving high power density. However, the selection of inverter topology remains paramount in the design of high power density devices (HPDD). Researchers have explored beyond traditional inverter topologies, presenting extensive insights on multiphase and multilevel topologies in the literatures [7],[50],[65] with their potential and challenges.

2.5.1 Multiphase inverters

Multiphase inverters, known for their ability to reduce passive component size [67], enhance per phase power handling [7], and improve thermal management, are particularly well-suited for traction applications. With the increasing popularity of higher DC bus voltage ratings to facilitate fast charging in electric vehicles [68], there is a concurrent rise in insulation requirements. Failures in insulation can lead to significant device malfunctions [69], posing major risks in aerospace applications. To address these challenges, multiphase topologies can reduce the voltage rating by increasing the current, thereby meeting high power demands while ensuring reliability and safety in critical applications. In addition to that, they offer smoother operation, reduced torque ripple and improved noise characteristics [50].
The figure 2.10 illustrates the relationship between per-phase current requirements

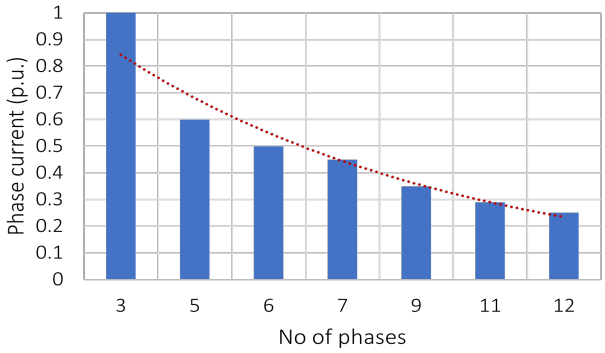

Figure 2.10: Impact of MPIs in phase current requirement [7]

and the number of phases in an inverter. It demonstrates that increasing the number of phases reduces the phase current demand up to a certain point. Specifically, a six-phase topology results in a 50% reduction in phase current requirements. This reduction not only lowers the per-phase current but also allows the use of the same modules as a three-phase VSI without needing to parallel multiple switches. Avoiding switch paralleling eliminates issues such as unbalanced currents and localized heating. The equation below shows how the phase current of multiphase inverters (MPIs) can be derived from the phase current of a three-phase topology, proving that the phase current is inversely proportional to the number of phases. This reduction also positively impacts the size of the DC bus cable, as demonstrated in table 2.7 . The overall cable cost, accounting the increased number of phases together, has decreased by 21% compared to a traditional three-phase VSI [7].

$$I_{\text{n-phase}} = \frac{3}{n} I_{\text{3-phase}}, \quad n > 3 \tag{2.1}$$

Number of phases	Per-phase current (A)	Cable size (AWG)
3	181	1
5	109	4
6	91	6
7	78	6
9	60	8

Table 2.7: Impact of MPIs in AC cable sizing [7]

Another significant advantage of using MPIs is the reduction in the size of DC link capacitors. These capacitors constitute about two-third of the total volume of the inverter [50], which is crucial for maintaining high power density. The required capacitance is influenced by the permissible DC voltage ripple [70], while the volume of the capacitors is determined by the DC link RMS current [71]. With MPIs, there is a notable 50% reduction in capacitance values. Although the decrease in the DC link RMS current is only around 10%, this still translates to a substantial 10% reduction in volume, which is a significant benefit which can be seen in Fig. 2.11.

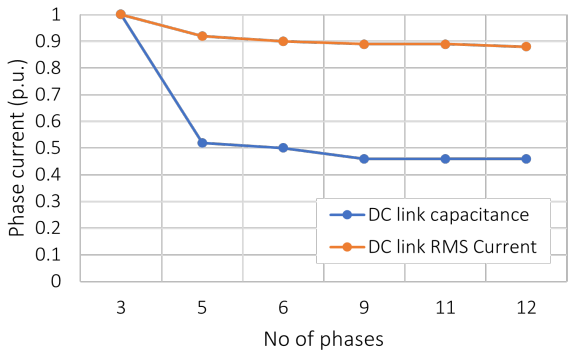

Figure 2.11: Impact of MPIs in capacitance and DC link RMS current [67]

Commercializing a single technology, such as MPIs, with substantial capital investment is not the best solution unless it offers a significant breakthrough. Therefore, integrating state-of-the-art technologies, including Wide Bandgap (WBG) devices, Integrated Modular Drives, Multilevel Topologies, advanced control schemes, and advanced thermal management, along with multiphase topologies, will be crucial in commercializing next-generation powertrains. This convergence of advanced technologies will enhance efficiency, reliability, and performance, making the investment more viable and fostering innovation in the powertrain industry. Literature [7],[50] has discussed on the potentials and challenges, enabling all the mentioned technologies which can be collated in the Table 2.8.

Strength	**Weakness**
1. Enhaced fault tolerance 2. Improved current handling 3. Reduced DC link capacitor size 4. Reduced DC link cable size 5. Modularity 6. Reliability enhancement by enabling MPCSI topology 7. Higher operating temperature by enabling MPCSI and GaN HEMT 8. High efficiency by enabling WBG 9. Improved EMC by enabling MPMLI and MPIMDs	1. Increased sensors and gate drives 2. Higher cost 3. Complexity in control 4. High EMI and oxide layer failures by enabling SiC MOSFET 5. Limited breakdown voltage by enabling GaN HEMT 6. Less space and Complex cooling system with MPIMD
Opportunities	**Threat**
1. In markets demand reliability 2. High power High current applications	1. Immature technology 2. Shift towards high voltage battery packs

Table 2.8: SWOT analysis of multiphase inverters [7], [50]

2.5.2 Multilevel inverters

As mentioned earlier, the rising trend of increasing battery voltage to facilitate fast charging in electric vehicles necessitates that both the electric machine and the inverter have to endure higher voltages [65]. In two-level topologies, the higher dv/dt associated with this increase can result in higher electromagnetic interference (EMI) and switching losses. This is where multilevel inverters come into play, offering the advantage of lower-rated switches with higher voltage handling capability. Consequently, they contribute to reduced harmonic distortion, reduced EMI, and enhanced power quality in the powertrain. These inverters are particularly beneficial in high-power applications where efficiency and minimal losses are crucial.

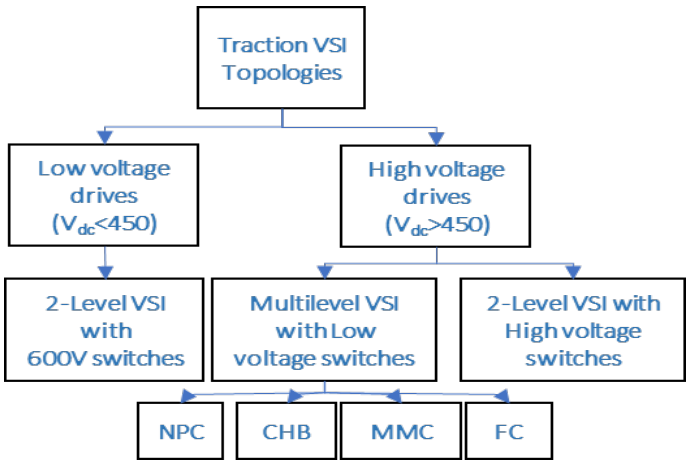

Figure 2.12: Classification of VSI topology based on DC bus voltage application showing the dominance of multilevel topolgy for high voltages [65]

Based on the advantages it has over the high voltage, Currently it is being used in high voltage, high power traction application [82],[83]. The Fig 2.12 below illustrates the classification of topologies for traction voltage source inverters (VSIs), highlighting the prevalence of multilevel inverters in high-voltage applications. In addition this, various multi-level topogies are discussed in literature such as Neutral point clamped inverter (NPC) [84]-[86], Modular Multilevel Converter (MMC) [83],[87], Flying Capacitor inverter (FC) [87] and Cascaded H-bridge inverter (CHB) [89],[90]. In [65], various control methods such as scalar, field oriented control and direct torque control are discussed. As future trend, model predictive control methods are suggested along with MLI hence it provides reduction in computation time for controller. Capacitor current balancing and smoother voltage transition are of some of the challenges in multi-level inverters which needs to be considered through modulation schemes. Modulation schemes such as carrier based, space vector and selective harmonic elimination are discussed and observed that carrier based are not flexible for NPC and specific harmonic elimination is not suitable for low power drives. Though space vector scheme offers better flexibility, it looks complex for high level structures. Based on these control methods and modulation methods reduction in the size of capacitor is explored but the paper concluded that it is not possible without reliable voltage balancing methods.

3

Modelling, Simulation and Experimental verification of 3-phase inverter

This chapter discusses the development of three phase 2-level inverter models using PLECS and Analytical loss function. The same was verified experimentally in a prototype inverter with RL load using infineon HybridPack SiC MOSFET modules. Results from this 3-phase inverter simulations and experiments are compared and studied.

3.1 Modelling and Simulation

In this chapter, the focus lies on the modeling of a 2-level 3-phase inverter using two distinct methodologies: Simulink-PLECS-based simulation and analytical loss function-based simulation. With these two simulations, inverter power loss calculation and Capacitor stress analysis is done.
1) Simulink-PLECS-based simulation offers a detailed circuit-level representation, enabling thorough analysis and precise results under various operating points of power factor, modulation index and switching frequency. PLECS based modelling eases the design of heatsink for the inverter which further helps in designing control of the inverter cooling strategies.
2) Analytical loss function-based simulations are employed alongside PLECS-based simulations to provide quicker computation times and facilitate the analysis of semiconductor losses under various operating points of power factor, modulation index, including drive cycle simulation.

3.1.1 Inverter specification

In this thesis, a 250 kW, 800 V, two level voltage source inverter with infineon HybridPack (Six pack) SiC MOSFET power modules (FS03MR12A8MA2B) are used and the specifications are tabulated in 3.3. The power module has a pin fin structure at the bottom, resulting in efficient cooling and low thermal resistance between the semiconductor junction and coolant which can be seen in the Fig. 3.1. The target specifications of the inverter are listed in the below table 3.1. A cylindrical film capacitor, Part number B25632E1117K000 from TDK [72], is selected as the DC link capacitor. As shown in Fig. 3.2, three capacitors with a total capacitance of

330 uF are used. The key specification of the capacitor is presented in table 3.2.

Parameters	Unit	Value
DC link voltage	V	800
Maximum DC Current	A	300
Maximum phase current RMS	A	260
Maximum power	kW	250
Volumetric power density	kW/L	63
Gravimetric power density	kW/kg	33
Switching frequency	kHz	20
Capacitance	µF	330

Table 3.1: Target specifications of the inverter

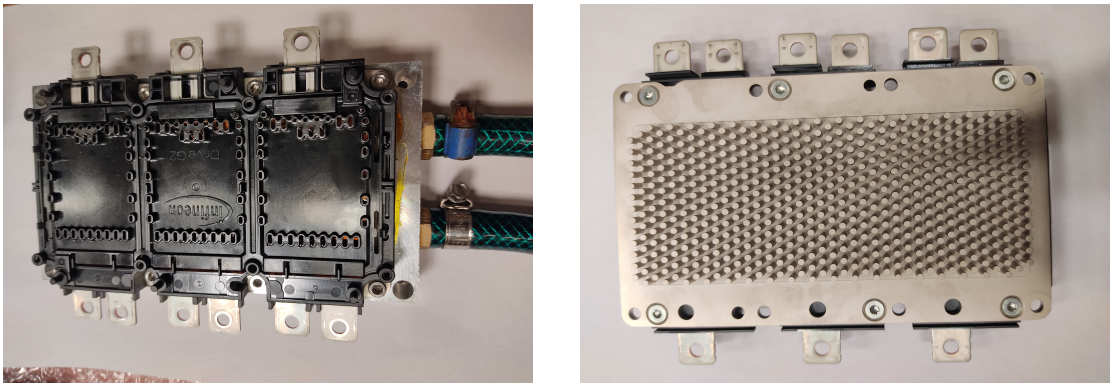

Figure 3.1: (a) HybridPack module assembled with heatsink and cooling circuit - Top side (Left), (b) HybridPack module pin fin structure - Bottom side (Right)

Figure 3.2: DC Link film capacitor from TDK [72]

3.1.2 3-phase Inverter modelling - Simulink-PLECS

PLECS is a specialized simulation tool tailored for the simulation of power electronics systems. Featuring multiple physics domains, PLECS simplifies the analysis of

Parameters	Value	Unit
Rated DC voltage	1000	V
Capacitance	110	uF
Maximum RMS current	50	A
ESR	1.2	mΩ
Self-inductance	13	nH
Thermal resistance hot spot to ambient	6.8	K/W
Weight	390	g

Table 3.2: Specifications of the film capacitor

Parameters	Value	Unit
Drain-source voltage	1200	V
DC drain current	360	A
On-state gate voltage	18	V
Off-state gate voltage	-5	V
Drain-source on-resistance (junction temperature = 25 °C)	2.2	mΩ
Drain-source on-resistance (junction temperature = 175 °C)	4.7	mΩ
Thermal resistance junction to coolant	0.118	K/W
Weight	800	g

Table 3.3: Specifications of the HYBRIDPACK power module

mechanical, thermal, and magnetic aspects of the system [73]. Employing an ideal switch model for transistors, PLECS dynamically adjusts integration time steps to accommodate instantaneous changes in transistor resistance. This approach grants PLECS a significant speed advantage over traditional circuit-level simulations, particularly in switching circuit applications [56].
Simulation model majorly consists of semiconductor loss model, DC Link capacitor model, DC link bus bar model, load model and heat sink model. Each model is briefly described below and the Fig. 3.3 shows the overall block diagram and Fig. 3.4 shows the block inside PLECS circuit with individual models marked.

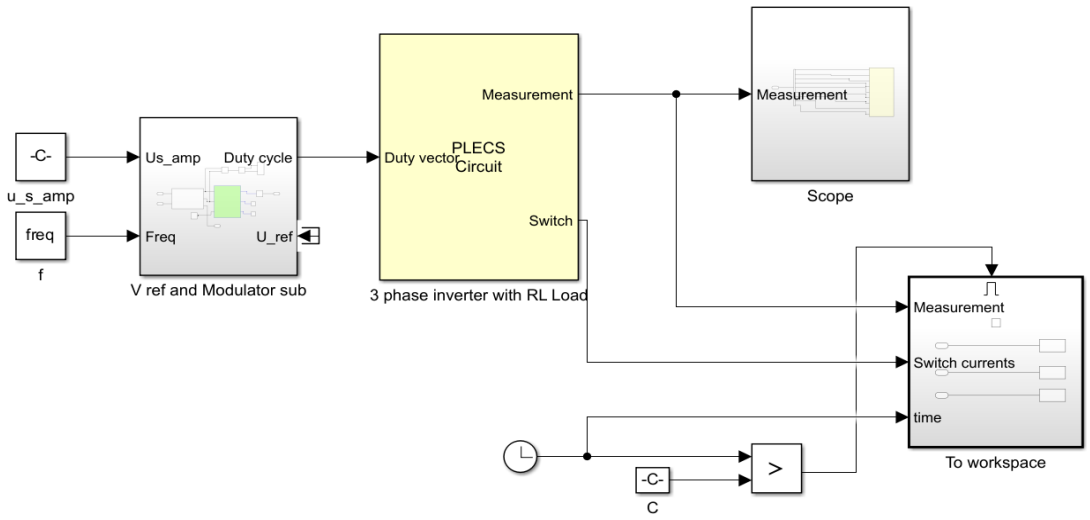

Figure 3.3: Overall simulink block diagram of 3-phase inverter

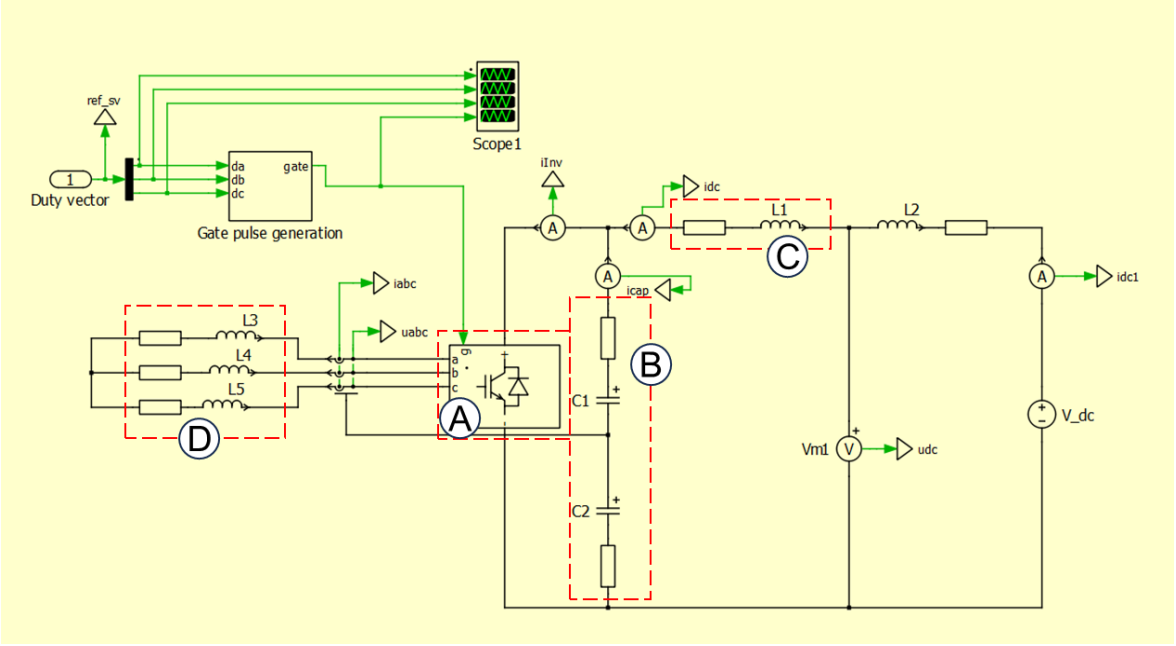

Figure 3.4: 3-phase Inverter with RL load (A-Inverter, B-DC Link capacitor, C-DC Link Cable, D-RL Load)

(a) Semiconductor Loss Model

PLECS utilizes analytical descriptions of power losses, either through lookup tables or functions. Input to the model is taken from the datasheet of HybridPack module. Turn-ON and Turn-OFF losses are mapped with respect to the drain source current for 25 °C (Blue) and 175 °C (Red) with DC link voltages from 150 V to 750 V. Conduction losses are mapped from the drain source voltage and current characteristic

curve from datasheet. Loss values are automatically interpolated by PLECS in the simulation, based on the input look-up table values. A sample image of loss model mapping window from PLECS is shown in Fig. 3.5 and the mapped switching losses and conduction losses are shown in 3.6 and 3.7 respectively.

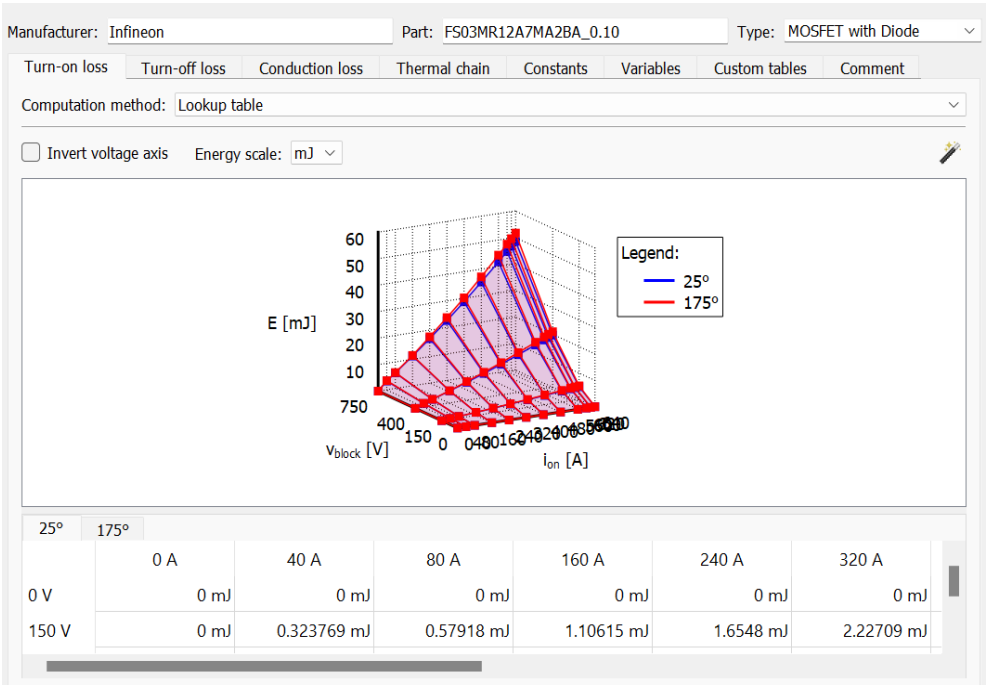

Figure 3.5: A sample image of Loss model in PLECS

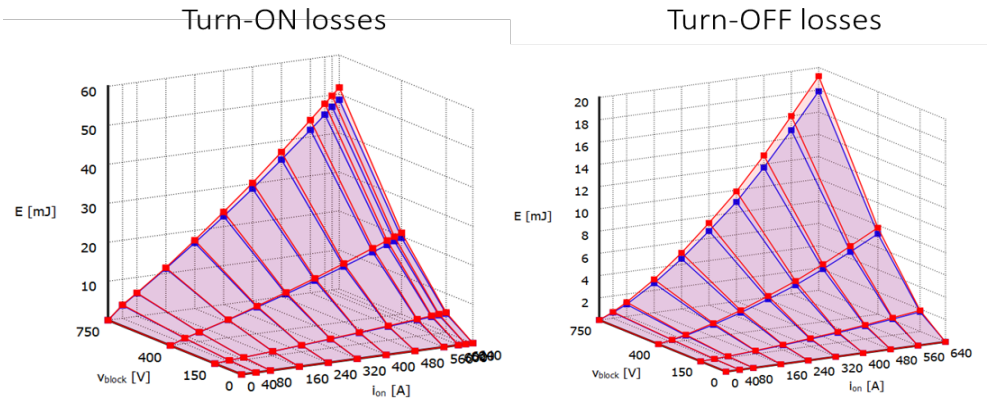

Figure 3.6: Turn-ON and Turn-OFF loss model (Blue: 25 °C, Red: 175 °C)

(b) DC Link Capacitor model

The DC link capacitor used in the thesis is of 110 μF film capacitor and three of those capacitors are used. To model that, Capacitor equivalent circuit model is made as mentioned in Fig. 3.4 marked as (B) with a capacitor and a Equivalent series resistance (ESR). The values of total capacitance is 330 μF and ESR is 0.4 mΩ [72]. There is a current measurement assigned to measure the capacitor current for stress analysis.

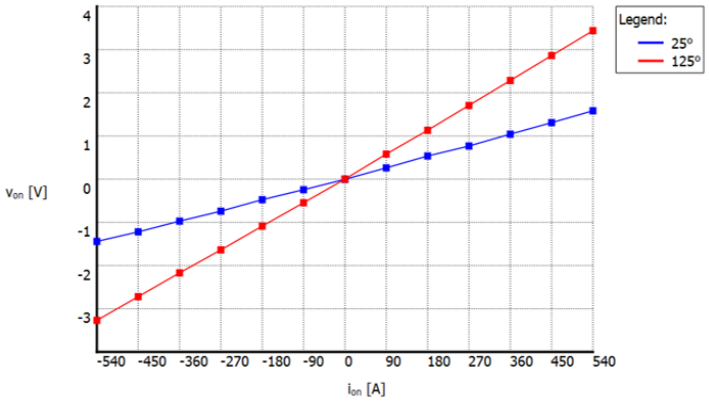

Figure 3.7: Conduction loss model

(c) DC Link Cable model

The cable used to connect in between the DC source and DC link bus needs to be modelled and series resistance and an inductance as mentioned in Fig. 3.4 marked as (C). The values of Cable resistance is 1mΩ and inductance is 2.4 $\mu\Omega$.

(d) RL Load model

To simulate the conditions of the machine, a RL load is modelled in this study. Resistance and inductance values have been back calculated from the experimental results of RMS current (I_{RMS}) , phase voltage (V_{RMS}) and power factor as per the below equations (3.1) to (3.3).

$$Z = \frac{V_{RMS}}{\sqrt{3} I_{RMS}} \tag{3.1}$$

$$L = \frac{Z}{2.pi.f} \tag{3.2}$$

$$R = Z.PF \tag{3.3}$$

where Z is the impedence, L is the inductance, PF is the power factor, f is the frequency and R is the resistance. The estimated R and L based on the experimental results are R=30 m Ω, L=0.5 mH which were used as the load values in the model.

(e) Thermal model

Heat sink was kept on covering all the six switches of the inverter. A constant temperature of 10°C was connected to the heat sink to set the initial ambient temperature that is equivalent to the coolant temperature which can be seen in Fig. 3.8.

The thermal description of the MOSFET switches has been taken from the transient thermal impedance data from the datasheet which is shown in Fig. 3.9. It can be done with foster model as mentioned here and in cauer model as well with the thermal resistance and thermal capacitance values based on the data availability from datasheet.

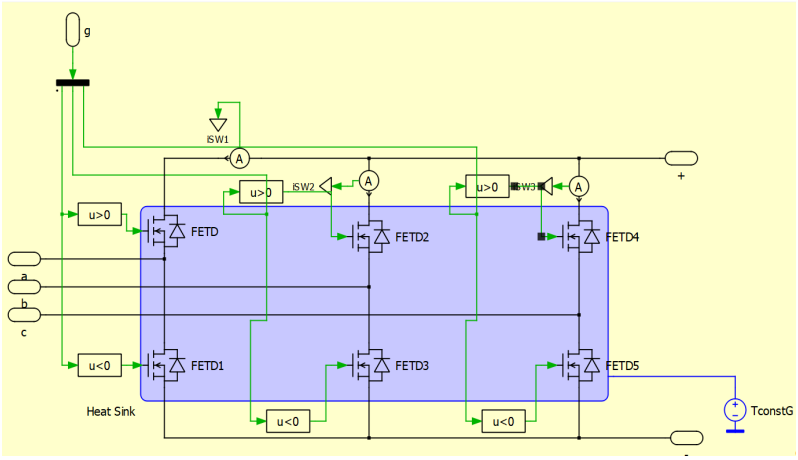

Figure 3.8: Heat sink model

Type: Foster Number of elements: 5

	1	2	3	4	5
R	0.002402 K/W	0.002402 K/W	0.002402 K/W	0.1641 K/W	0.09704 K/W
τ	0.001067 s	0.04133 s	0.04134 s	0.08558 s	0.7482 s

Figure 3.9: Transient thermal impedance with time

3.1.3 Results of PLECS simulation

The simulation is conducted at 400V DC and the peak phase current from 80 A to 335 A. The simulated results have been summarized and tabulated in 3.4 and the Fig. 3.10 shows the output waveform of the three phase inverter. The simulated phase currents (i_{a1},i_{b1},i_{c1}), phase voltages (u_{a1},u_{b1},u_{c1}), capacitor current (I_{cap}), Switching losses $P_{\text{loss\_SW}}$, conduction losses $P_{\text{loss\_COND}}$, DC bus voltage and currents have been extracted from the simulation and post processed with the below equations 3.4 to 3.13 for estimating the inverter losses. I and U in the eq. 3.4, 3.5, are the fundamental components of phase currents which were calculated by doing a FFT.

$$I_{\text{rms}} = \frac{I_{a1} + I_{b1} + I_{c1}}{3\sqrt{2}} \tag{3.4}$$

$$U_{\text{rms}} = \frac{U_{ab} + U_{bc} + U_{ca}}{3\sqrt{2}} \tag{3.5}$$

$$P_{\text{ac}} = u_{a1}i_{a1} + u_{b1}i_{b1} + u_{c1}i_{c1} \tag{3.6}$$

$$Q_{\text{ac}} = \frac{(u_{a1} - u_{b1}) \cdot i_{a1} + (u_{b1} - u_{c1}) \cdot i_{b1} + (u_{c1} - u_{a1}) \cdot i_{c1}}{\sqrt{3}} \tag{3.7}$$

$$P_{\text{loss\_cap}} = I_{\text{cap}}^2 R_{\text{ESR}} \tag{3.8}$$

$$P_{\text{loss\_inverter}} = P_{\text{loss\_SW}} + P_{\text{loss\_COND}} \tag{3.9}$$

$$P_{\text{loss}} = P_{\text{loss\_cap}} + P_{\text{loss\_inverter}} \tag{3.10}$$

$$P_{\text{dc}} = P_{\text{loss}} + P_{\text{ac}} \tag{3.11}$$

$$\text{PF} = \frac{P_{\text{ac}}}{\sqrt{P_{\text{ac}}^2 + Q_{\text{ac}}^2}} \tag{3.12}$$

$$\text{Eff} = \frac{P_{\text{ac}}}{P_{\text{dc}}} \tag{3.13}$$

where I_{rms} is Phase current RMS, U_{rms} is Phase voltage RMS, P_{ac} is Active power, Q_{ac} is Reactive Power, $P_{\text{loss\_cap}}$ is Losses in the capacitor, P_{loss} is the total losses including capacitor losses, P_{dc} is the DC power, PF is the Power factor and Eff is the Efficiency.

I_{peak}	I_{RMS}	U_{RMS}	I_{dc}	I_{cap} RMS	P_{dc}	P_{ac}	Q_{ac}	P_{loss}	$P.F$	Eff
Unit	A	V	A	A	kW	kW	kVAR	W	-	-
80	75.42	22.90	2.22	13.35	0.89	0.51	-1.03	378.02	0.44	0.57
160	107.45	32.62	4.01	21.07	1.60	1.03	-2.09	568.06	0.44	0.65
240	162.84	49.48	8.41	40.52	3.37	2.39	-4.82	979.27	0.44	0.71
335	197.69	60.09	12.08	54.20	4.83	3.52	-7.10	1313.30	0.44	0.73

Table 3.4: Summary of key parameters from the three phase inverter power calculation in PLECS

3.1.4 3-phase inverter modelling - Analytical Loss Function

In addition to a circuit level modelling with Simulink - PLECS, an analytical based model is made for a faster computation of losses with a manual inputs of operating points and a drive cycle input. The overall block diagram of the model is given in the figure 3.11.

Manual verification with different operating points

To verify and estimate the inverter losses at various operating points of peak phase current, power factor and modulation index, manual verification can be enabled through the toggle switch which can be seen in the figure 3.11.

Drive cycle simulation

To estimate the inverter switching and conduction losses for different drive cycle scenarios with with torque, speed operating points drive cycle input part can be enabled with the switch. Since this chapter does not focus on the drive cycle simulation, the modelling of this will be detailed in the next chapter.

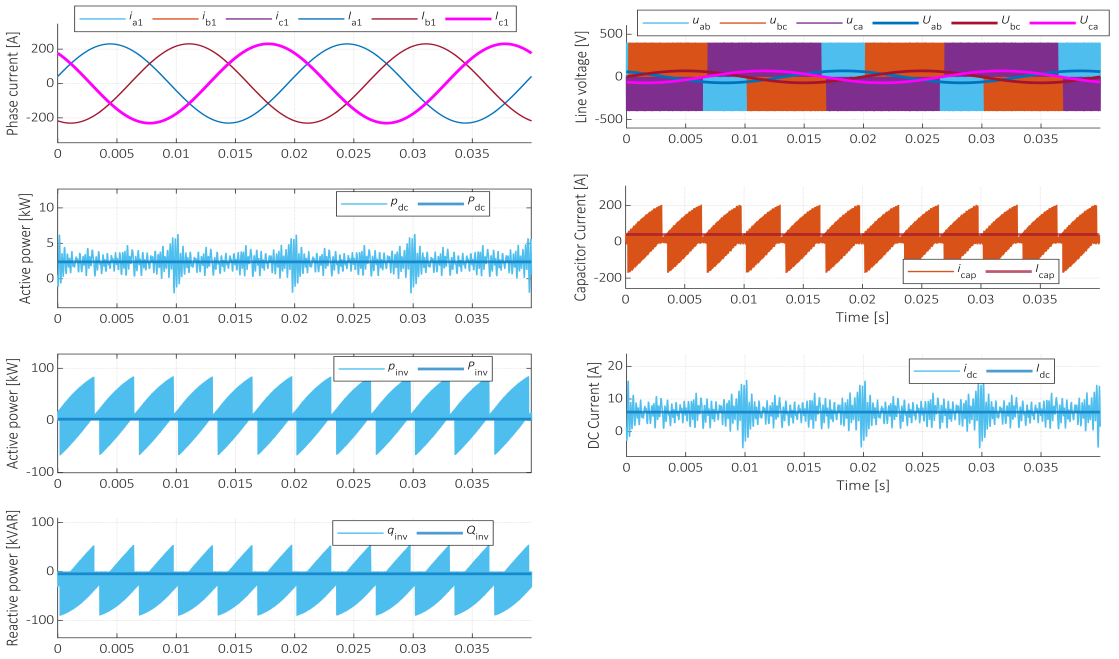

Figure 3.10: Output waveform of PLECS simulation for inverter loss at 400V DC and 240 A I_{peak}

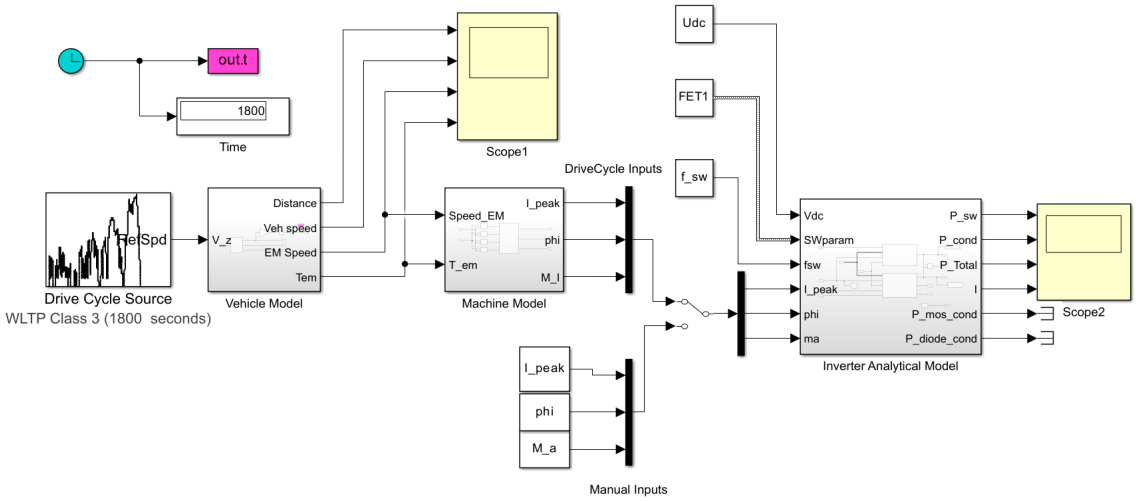

Figure 3.11: Overall image of analytical loss model

Inverter analytical loss model

The inverter loss model contains two major blocks which are switching loss calculation and conduction loss calculation. As per semikron application manual [57], The switching losses E_{on} and E_{off} are interpolated from datasheet with respect to the equivalent DC current value. The DC equivalent from peak value is calculated as,

$$I_{\text{DC}} = \frac{\hat{I}}{\pi} \tag{3.14}$$

where I_{DC} is the equivalent DC current, $\hat{I}$ is the peak value of the AC current. Since, the mapped losses with respect to drain source current is only at 750V as per datasheet, it is required to scale it to the DC link voltage values that is used in the simulation. Scaling of losses with DC link voltage is done as,

$$E_{\mathrm{on/off}}(I_{\mathrm{DC}}) = \left(\frac{V_{ds}}{V_{dc,\mathrm{ref}}}\right)^{K_{v,\mathrm{on/off}}} \tag{3.15}$$

where V_{ds} is the drain-source voltage used in simulation; $V_{dc,\mathrm{ref}}$ is the reference DC voltage as per datasheet; $K_{v,\mathrm{on/off}}$ is a scaling factor typically around 1.4 obtained from the supplier's data sheet. With the above details, switching loss is calculated by interpolation of losses with the corresponding DC equivalent current and Junction temperature T_{j} as,

$$P_{\mathrm{sw}} = f_{\mathrm{sw}}(E_{\mathrm{on}}(I_{\mathrm{DC}}, T_{\mathrm{j}}) + E_{\mathrm{off}}(I_{\mathrm{DC}}, T_{\mathrm{j}}) + E_{\mathrm{rr}}(I_{\mathrm{DC}}, T_{\mathrm{j}})) \tag{3.16}$$

where P_{sw} is the switching losses, f_{sw} is the switching frequency, E_{on} is the on-state loss, E_{off} is the off-state loss, E_{rr} is the reverse recovery loss.
As per the literature [58], The average MOSFET conduction loss (single switch) is calculated as,

$$\begin{aligned} P_{c,T} = \frac{R_{\mathrm{on}}\hat{I}^2}{4\pi}(AB + CD) + \frac{R_{\mathrm{on}}}{4\pi(R_{\mathrm{on}} + R_d)}\hat{I}^2 R_d^2(A(\pi - B) - CD) + \\ \Big(V_d^2((\pi - 2\beta)A - D\cos(\beta)) + \hat{I}R_d V_d(4A\cos(\beta) - (\pi - B)D)\Big) \end{aligned} \tag{3.17}$$

where R_{on} is the on-state resistance; $\hat{I}$ is the peak value of the phase current; A, B, C, D are simplification parameters which are shown below; R_d is the diode resistance; V_d is the diode voltage. β is limited to 90 ° since the parallel conduction of diode and MOSFET never occurs. The average diode conduction loss (single diode) is calculated as,

$$\begin{aligned} P_{c,d} = \frac{R_d}{4\pi(R_{\mathrm{on}} + R_d)}\Big(R_{\mathrm{on}}^2\hat{I}^2(\pi - B - CD) + V_d^2(\pi - 2\beta - D\cos(\beta)) \\ -R_{\mathrm{on}}\hat{I}V_d(4\cos(\beta) - (\pi - B)D) - \frac{V_d}{4\pi(R_{\mathrm{on}} + R_d)}\frac{1}{2}R_{\mathrm{on}}\hat{I}(\pi - B)D + 2R_{\mathrm{on}}\hat{I}\cos(\beta) \\ -V_d(\pi - 2\beta) + V_d D\cos(\beta) + t_{\mathrm{bl}}f_{\mathrm{sw}}\hat{I}(\frac{1}{2}\hat{I}R_d + \frac{2}{\pi}V_d)\Big) \end{aligned} \tag{3.18}$$

where t_{bl} is the blanking time, f_{sw} is the switching frequency. The simplified variables A,B,C,D are given below.

$$A = \begin{cases} 1, & \text{for } t_{\mathrm{bl}} = 0 \\ 1 - 2t_{\mathrm{bl}}f_{\mathrm{sw}}, & \text{for } t_{\mathrm{bl}} > 0 \end{cases} \tag{3.19}$$

$$B = \frac{\pi}{2} + \beta - \frac{\sin(2\beta)}{2} \tag{3.20}$$

$$C = \cos(\beta) - \frac{\cos^3(\beta)}{3} \tag{3.21}$$

$$D = 2M\cos(\phi) \tag{3.22}$$

where t_{bl} is the blanking time; f_{sw} is the switching frequency; β is the variable; M is the modulation index; ϕ is the power factor angle;

3.1.5 Results of Analytical loss model

The losses are calculated for the current amplitudes of 80A to 335A at 400V DC for easy comparison with the PLECS simulation and experimental measurement. The input of power factor $P.F$, Modulation index M, ambient temperature T_{amb}, Coolant Flow rate, Coolant temperature T_C are given to the simulation equivalent to that of experimental condition for the comparison. From the total inverter losses calculated, The junction temperature is estimated with the below equation. The experimental verification will be discussed in the next chapter. The summary of inverter losses calculated from the analytical loss function is given in table 3.5.

$$T_j = \frac{T_{amb} + R_{th}P_{Tot}}{6} \tag{3.23}$$

I_{peak}	f	M	$P.F$	T_{amb}	T_C	P_{sw}	P_{cond}	P_{Tot}	ΔT_j
Unit	Hz	-	-	°C	°C	W	W	W	°C
80	50	0.11	0.24	10	6.3	118.5	32.5	151.0	3.65
160	50	0.22	0.19	10	6.3	228.6	120.0	348.7	8.43
240	50	0.32	0.18	10	6.3	344.5	271.7	616.3	14.89
335	50	0.41	0.19	10	6.3	488.5	554.0	1042.0	25.18

Table 3.5: Summary of key parameters from the simulation of analytical loss calculation

3.2 Experimental Verification

This section covers the experimental verification of the above mentioned semiconductor loss model. The experimental setup used for the loss measurement is explained with list of components, equipment and measurement devices.

3.2.1 Experimental setup

For the verification of the loss models discussed in the previous sections, a Si IGBT based 2 level-VSI is protyped using Infineon HybridPack SiC MOSFET power module in a six pack configuration. A gate driver board from infineon is used to drive the power module switches. dSPACE DS1006 is used to generate PWM to the gate

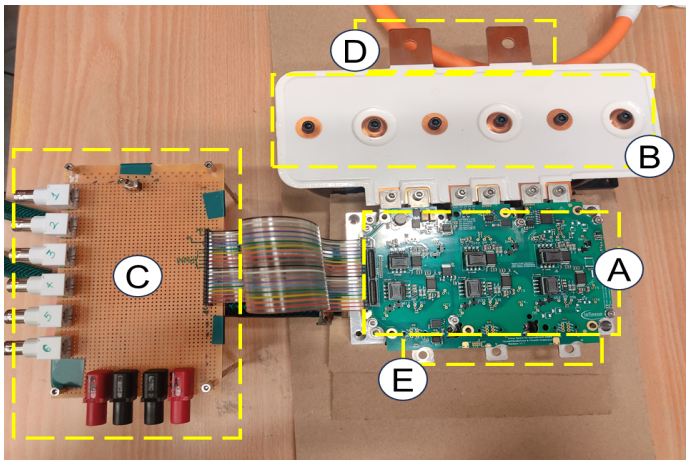

Figure 3.12: Closer view of the inverter prototype - A: Infineon gate driver assembled with power module, B: DC Link bus bar assembled with Capacitors in bottom, C: Interface board between gate driver and dSpace, D: DC terminals to DC source, E: 3 phase output to RL load

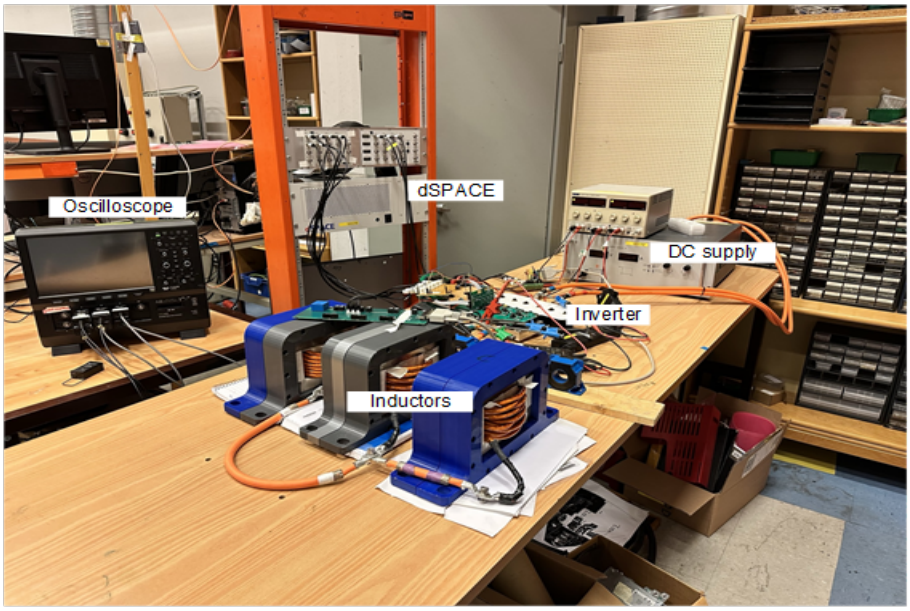

Figure 3.13: The laboratory setup used to evaluate the 3-phase 2-level inverter using the MOSFET-based HybridPack module

driver board. The key specifications of inverter, power module and capacitor were already given and discussed in section 3.1.1 from table 3.1 to 3.3.

The experimental lab setup is shown in the Fig. 3.13 and closer view of inverter in Fig. 3.12 for inverter loss measurements. The table 3.6 lists the power supply, measurement equipment and key components used for the measurements. The power module with the pin-fin structure at the bottom side, is connected with the heat sink through which the liquid cooling system is enabled which can also be seen from figure 3.1. Tap Water is used as the coolant medium for which the temperature can be controlled from 10°C to 45°C. The power modules are having in-built temperature

sensors to measure the junction temperature. To measure the water temperature and water flow rate, a temperature sensor and a flow meter is implemented in the water inlet. The switching frequency of 20 kHz, fundamental frequency of 50 Hz and DC link voltage of 400 V is selected. The load is an RL load with the R of 30 $m\Omega$ and L of 0.5 mH.

Device	**Manufacturer**	**Model**	**Purpose**
DC Power Source (600 V, 10 A)	DELTA ELEKTRONIKA	SM 600-10	Main DC supply
DC Power Source (30 V, 2 A)	TTI Instruments	EL302RT	Auxiliary supply for gate driver and rogowski current sensor
High Voltage Differential Probe (2000 V, 120 MHz)	Teledyne Lecroy	HVD3206A	Voltage measurement
AC Current probe (500 A, 2 MHz)	Teledyne Lecroy	CP500	Phase current measurement
DC Current probe (150 A, 120 kHz)	Teledyne Lecroy	AP011	DC current measurement
Rogowski Current transducer (0.6 kA, 10 mV/A)	CWT	CWTMini HF3R	Switch Current measurement
Motor Drive Analyser (500 MHz, 2.5 GS/s)	Teledyne Lecroy	MDA805	Measurement data visualization
dSPACE interface	dSPACE GmbH	DS6001, DS5101	PWM generation
Flow Meter	Swissflow	SF-800	Coolant flow rate measurement
Acquisition unit	FLUKE	2638A HYDRA SERIES III	Data acquisition of flow rate and coolant temperature

Table 3.6: List of equipment used in experiments

All the measurements have been taken with below mentioned conditions in 3.7. The list of parameters that were physically measured are phase currents i_a, i_b, DC bus current I_{DC}, DC bus voltage U_{dc}, Line voltages u_{ab}, u_{bc} and u_{ca}. From these measured parameters, phase current RMS I_{RMS}, Line voltage RMS V_{RMS}, Active power P_{ac}, reactive power Q_{ac}, Inverter losses P_{loss}, power factor and efficiency are calculated as per the below equations. I and U in the eq. 3.25, 3.26, are the fundamental components of phase currents which were calculated by doing a FFT. The junction temperature measurements are taken from the in-built temperature sensors of the HybridPack power modules for each phase.

$$i_c = -i_a - i_b \tag{3.24}$$

$$I_{\text{rms}} = \frac{I_a + I_b + I_c}{3\sqrt{2}} \tag{3.25}$$

$$U_{\text{rms}} = \frac{U_{ab} + U_{bc} + U_{ca}}{3\sqrt{2}} \tag{3.26}$$

$$P_{\text{ac}} = u_{ab} i_a - u_{bc} i_c \tag{3.27}$$

$$Q_{\text{ac}} = \frac{u_{ab} i_a + u_{bc} i_b + u_{ca} i_c}{\sqrt{3}} \tag{3.28}$$

$$P_{\text{dc}} = I_{\text{DC}} \cdot u_{\text{dc}} \tag{3.29}$$

$$P_{\text{loss}} = P_{\text{dc}} - P_{\text{ac}} \tag{3.30}$$

$$\text{PF} = \frac{P_{\text{ac}}}{\sqrt{P_{\text{ac}}^2 + Q_{\text{ac}}^2}} \tag{3.31}$$

$$\text{Eff} = \frac{P_{\text{ac}}}{P_{\text{dc}}} \tag{3.32}$$

3.2.2 Experimental results

The ultimate scope of the measurement is to estimate the inverter losses with respect various operating current amplitudes and compare it with simulations done in the previous section through which the models can be validated. Each measurement point was experimentally verified twice to verify the experimental setup.
The power measurements are taken at 400V DC at the phase current amplitudes from 80A to 335A. From the table 3.8, it can be confirmed that the two measurements produce same results and the setup is verified with the results observed. The Fig. 3.14 shows the comparison of inverter losses between the two measurements. Error between two measurements were checked and the maximum error observed is of 5.6% in the inverter losses which may be because of measurement at low power factor. The Fig. 3.15 shows the output waveforms observed from the measurement 1 which shows the phase currents and line voltage with corresponding fundamental components, Active, reactive power component with mean value, DC bus current and voltage plots.

Parameter	Value	Unit
Fundamental frequency	50	Hz
Switching frequency	20	kHz
Ambient Temperature	10	°C
Coolant flow rate	7	L/min
Coolant temperature	6.2-7	°C
DC bus voltage	400	V

Table 3.7: Key constant parameters for all the experiments

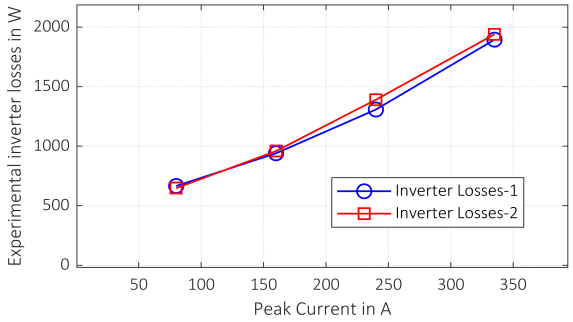

Figure 3.14: Comparison of inverter losses from the two measurements at 400V DC

I_{peak}	I_{RMS}		U_{RMS}		I_{dc}		P_{dc}	
	1	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Unit	A	A	V	V	A	A	W	W
80	50.38	51.29	15.24	15.56	2.01	1.95	0.78	0.80
160	107.54	108.31	30.91	31.14	3.56	3.55	1.42	1.42
240	164.13	165.22	45.34	45.61	5.89	6.01	2.40	2.34
335	236.57	238.30	57.89	58.05	9.78	9.96	3.97	3.90
I_{peak}	P_{ac}		Q_{ac}		P_{loss}		$P.F$	
	1	**2**	**1**	**2**	**1**	**2**	**1**	**2**
Unit	kW	kW	kVAR	kVAR	W	W	-	-
80	0.13	0.13	-0.57	-0.54	665.69	647.58	0.22	0.24
160	0.46	0.48	-2.52	-2.45	940.30	958.79	0.18	0.19
240	1.01	1.04	-5.64	-5.53	1307.65	1390.39	0.18	0.18
335	2.03	2.00	-10.19	-10.07	1894.58	1939.59	0.20	0.19

Table 3.8: Comparison between the key parameters of the two measurements in the prototype inverter

The table 3.9 shows the increase in junction temperature measured in the experiments in all the three phases of the inverter for peak current values from 80A to 335A. Temperatures in all the phases are in similar values with the maximum increase of 9 °C mean value in the 335A peak current.

I_{Peak}	ΔT_U	ΔT_V	ΔT_W
A	°C	°C	°C
80	2.72	3.17	1.62
160	4.42	3.43	3.45
240	5.59	5.61	5.42
335	8.75	8.40	9.51

Table 3.9: Increase in junction temperature measured in experiments for all three phases with different peak current values

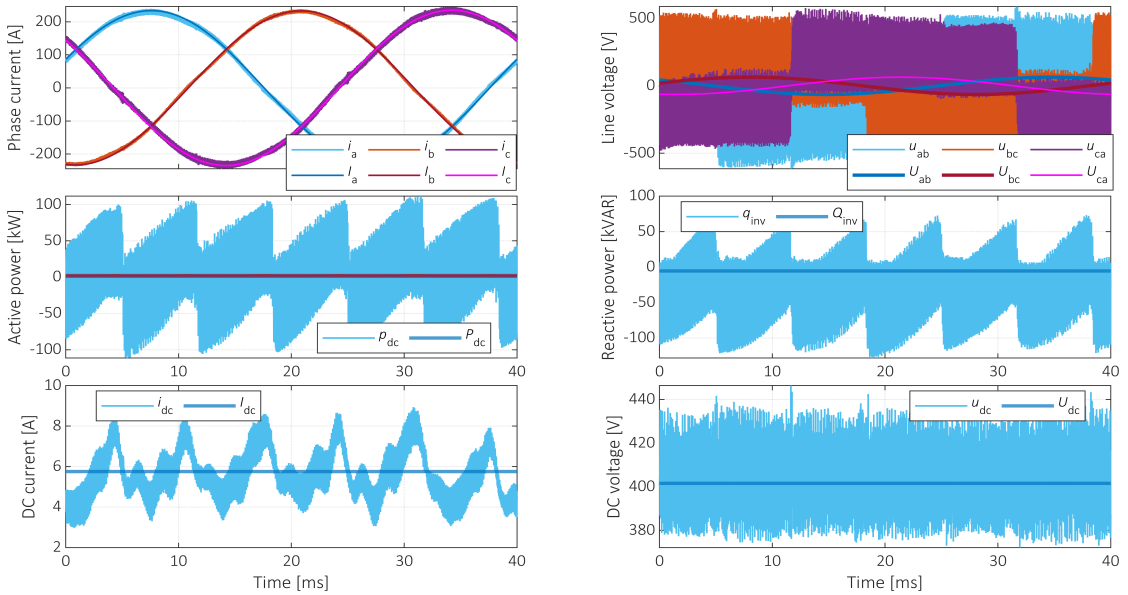

Figure 3.15: Output Waveforms of inverter power measurement at 400V DC and 240 A I_{peak}

3.3 Comparison of results and Discussion

This section discusses the comparison of the key results obtained from the simulations and experiments. Section 3.3.1 includes the comparison of inverter performance parameters of phase current RMS, line voltage RMS, DC bus current and inverter losses. The section 3.3.2 discusses the comparison of capacitor current measurement in experiments and simulation.

3.3.1 Steady State Analysis - Comparison

The load model can be verified from the comparison of phase current and line voltage values between experiments and PLECS simulation in Fig 3.16 and 3.17. The phase current RMS of simulation and experiments perfectly matched between peak current values 160A to 240A and it is having a maximum deviation of 49% only for the 80A peak current. The Line voltages seems to be matching at all points except the point at 80A with 47%. The reason is that R and L used for the PLECS load model is calculated from the mean R and L values estimated from the experimental results

as shown in eq. 3.1 to 3.3. That is clearly visible since the results perfectly match in the currents between 160A to 240 and not matching at lower and higher current zones.

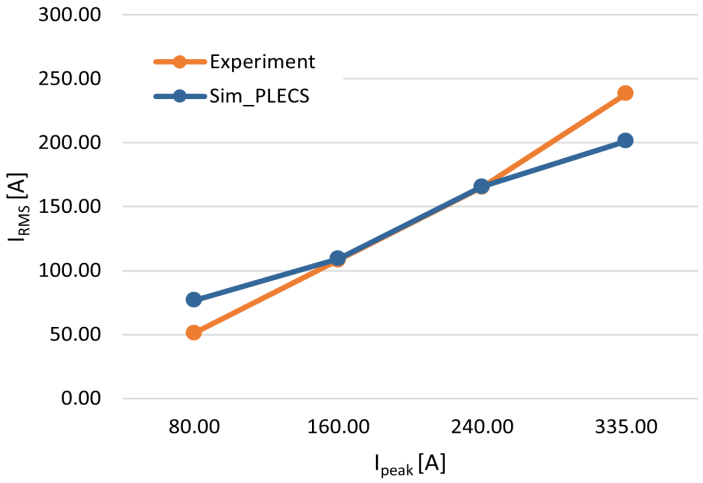

Figure 3.16: Comparison of phase current RMS between PLECS simulation and experimental results at 400V DC

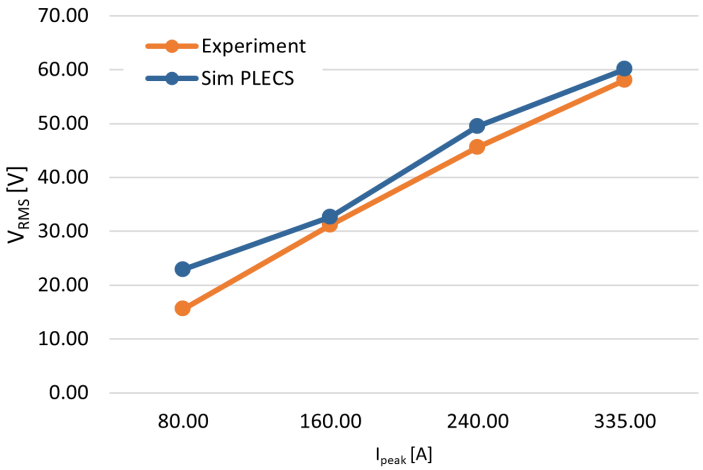

Figure 3.17: Comparison of Line voltage RMS between PLECS simulation and experimental results at 400V DC

The Fig 3.18 compares the inverter losses among experiments and the two simulations to validate the semiconductor loss models developed in both the simulations. It is observed that the simulation results were almost matching with the maximum error of 15% only at 335A peak current. Though the trend of losses with respect to peak current amplitude seems to be matching between experiments and both simulations, there is a factor of 2.4 times difference between the experiment and simulation result was observed. This huge difference is expected due to the measurements taken at low power factor of 0.2 which can be seen in 3.8. Since the

measurements at lower power factor might have led to errors in measurements, increased switching and conduction losses which is not considered in the simulations. Hence, a factor k is introduced to match the simulation results with the experiments and the factor was calculated to be 2.4 to proceed the analysis further in the next chapter.

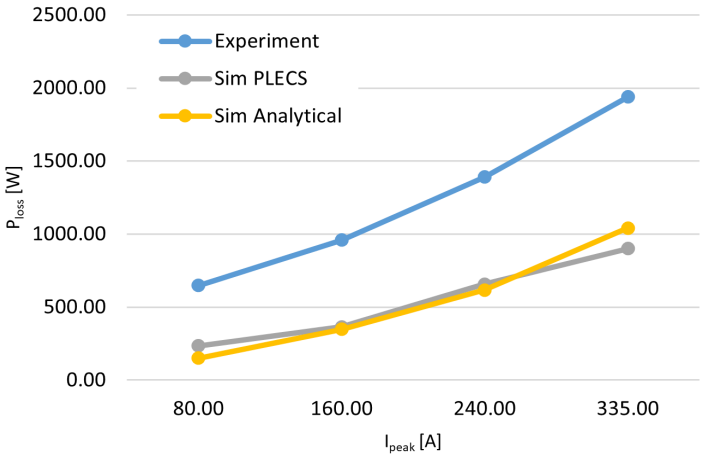

Figure 3.18: Comparison of total losses between PLECS, Analytical function and experimental results

As the measurement of junction temperature is of critical important, the below Fig.3.19 provides the comparison of increase in junction temperature values between simulation and experiments. When comparing the simulation and experimental measurements in orange and dark green plots, there is a huge error observed and the trend of increase also is not the same between those two. To cross verify measured temperature from the modules, the calculated power loss values where used to estimate the junction temperature as per 3.23 which was shown in the yellow line as estimated. The estimated line was matching the trend of simulation but not the measured. In the tear-down analysis of the power module, it was observed the the temperature sensor placement was near the diode and not the MOSFET chip which has created the huge error in the measurement. Further, the calibration of junction temperature will be carried out in the future work.

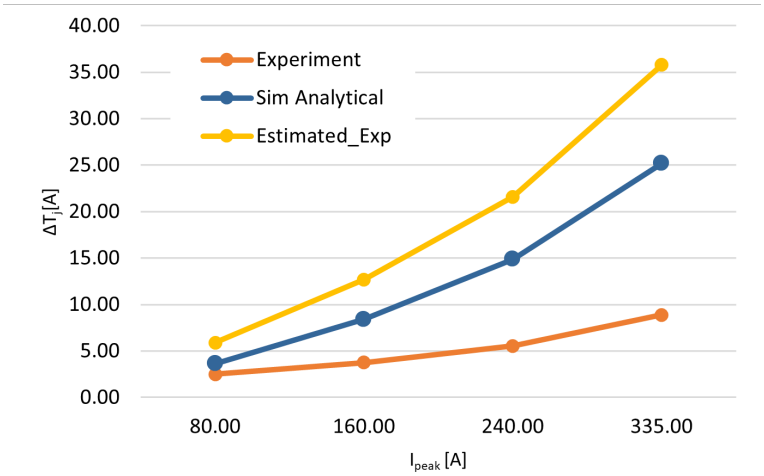

Figure 3.19: Comparison of increase in junction between Analytical function, Experimental and Estimated value experimental losses

3.3.2 Capacitor current measurement-Comparison

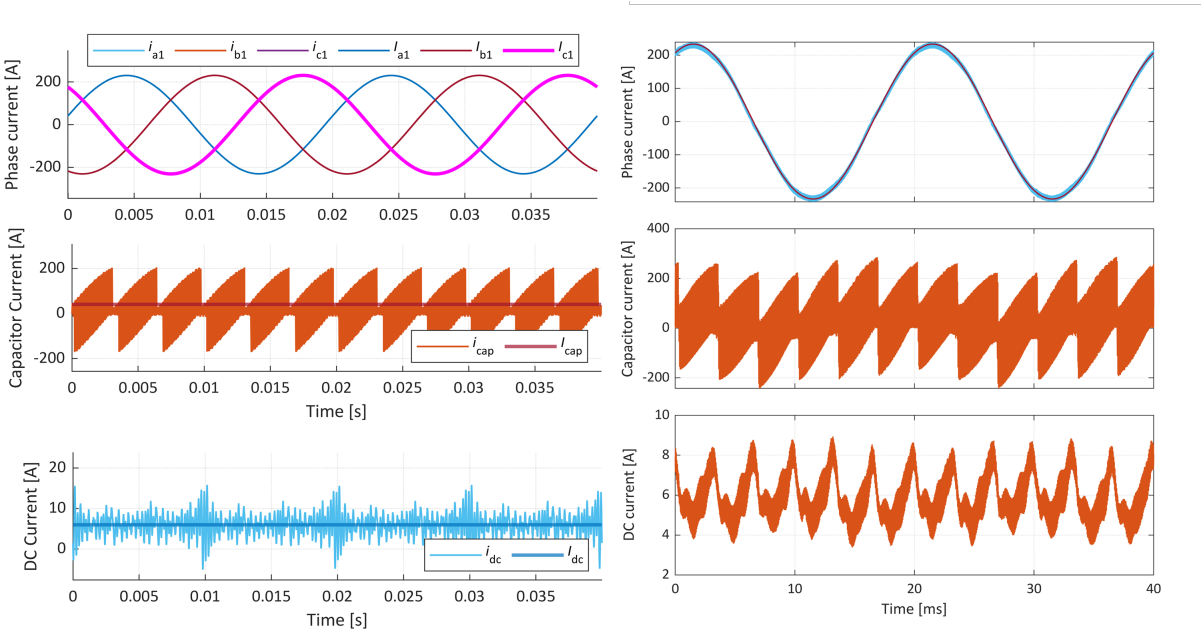

Figure 3.20: Comparison of capacitor current waveforms between simulation (left) and experiments (right)

The DC bus and capacitor model can be verified by comparing the capacitor current RMS values of both experiment and simulation which is shown in the 3.21. The RMS current estimated in simulation is found to be following the same trend and nearer values. There is a maximum error of 17% observed at 160A peak current. The capacitor current in measurements is calculated from the difference between the DC bus current and switch current. This indirect measurement is the expected reason for the slight errors observed.

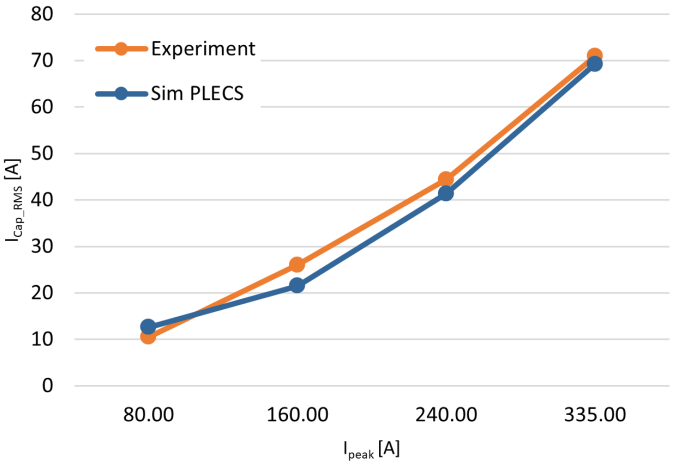

Figure 3.21: Comparison of capacitor current RMS values between PLECS and experimental results at 400V DC

The below Fig 3.20 shows the output waveforms of the capacitor current measurement at 400V DC and 240 A peak current. From the result, the profile of the capacitor can be seen that both the simulation and experiment results are similar and the RMS current was calculated from this waveforms which were compared above.

4

Analysis of bus bar inductance on 2-Level 3-phase inverter performance

4.1 Introduction

The performance of 2-Level 3-phase inverters is critically influenced by various parasitic elements which will present in DC link capacitors, Power semiconductors, Gate driver circuit, cables and DC Link bus bar. The power semiconductor can be a discrete device or power module in a half-bridge or six-pack configuration. Although some manufacturers have used discrete devices, power modules are preferred. The power module's AC and DC connection are screw-on copper terminals. Metalized film capacitors are mostly chosen for traction applications due to their higher current and temperature capability than electrolytic [11]. The capacitors provide reactive power support and act as a low-pass filter for the DC voltage and current by providing a low-impedance path to the high-frequency ripple current component [75]. These capacitors can be lumped or distributed. Since the DC link consists of several capacitors connected in parallel, a copper bus bar is used to connect the capacitor bank to the power semiconductor [11] and the High voltage battery. This bus bar is referred to as the DC bus bar in this work.

The main requirements on the DC bus bar design for a 2-level inverter are low weight, uniform distribution of ripple current path, and low inductance. The inductance of the bus bar is critical as it is responsible for the overvoltage spikes during the semiconductor turn-off event [52]. The overvoltage spikes can contribute to additional stress on the switches and capacitors, electromagnetic emissions, increased switching losses [60], and device breakdown [76]. The amplitude of the spikes is proportional to the inductance and di/dt of the semiconductor [52]. Using fast-switching SiC MOSFET-based devices has led to an increase in di/dt. Therefore, the only way to limit the overvoltage spikes is to focus on reducing the bus bar inductance. To minimize the inductance, overlapping between the positive and negative DC copper bars is preferred, leading to laminated bus bar technology. A laminated bus bar comprises two overlapping copper plates separated by insulation material. Therefore, the design of a low-inductance bus bar has been studied in the literature.

In [59], the influence of bus bar inductance on conducted electromagnetic interference of a 2-level VSC with IGBT switches is analyzed. In [63], Ansys Q3D extractor simulation (a finite element analysis) based estimation of stray inductance is stud-

ied, and based on the results, minimization of stray inductance is realized using a PCB-based bus bar and interconnect design. By using the mutual inductance cancellation with removing the bus bar side material, the commutation loop and Bus bar inductance are reduced by more than 50%. Experimental validation uses a double pulse test measuring the over voltage across the switching devices. The same paper was extended in [77] to present the further minimization of parasitic inductance by introducing a new inductance measurement technique of very low inductance with which individual loop inductance was measured and verified with simulation results. Though the optimized bus bar has a 50% improvement in the loop inductance, the overshoot voltage was reduced only from 22.88% to 20.38%. Hence, the voltage overshoot is not linearly related to parasitic inductance [78].
However, most of the work presented in the literature has focused on the EMC issues caused by voltage spikes [59],[79]. Very little focus is given to the impact of switching losses. The switching losses of the power semiconductor are directly proportional to the voltage across the switch. The stray inductance of the bus bar affects the switching losses by increasing device voltage and delaying turn-off. Therefore, this work presents the design of a low-inductance bus bar for a 2-level VSI and the estimation of stray inductance, focusing on losses. The main contribution is an analysis of the influence of DC bus bar inductance on losses of the inverter with drive cycle simulation.
This chapter has the following details discussed.
(a) The design of two laminated bus bars for a traction inverter utilizing a six-pack power module and cylindrical film capacitors to realize the above,
(b) The influence of the stray inductance on the switching losses is studied using a double-pulse circuit. Additionally, a drive cycle-based analysis of the losses of the two inverters is discussed,
(c) The insights observed from voltage overshot across the semiconductor switch due to the stray inductances of the bus bar through transient measurements.

4.2 Simulation of the Bus Bar

This section presents the design of the DC bus bar based on the requirements given in 4.1. The semiconductor used in the inverter is a HybridPack Drive six-pack power module with SiC MOSFET switches. Three cylindrical film capacitors from TDK, with the part number specified in 4.1, are used in the DC link. The bus bar is cooled using natural convection.

4.2.1 FEM results showing the current distribution

A laminated busbar is a multilayer construction of conductors made of copper or aluminum separated by thin dielectric materials, laminated in one structure. The inductance of the bus bar is proportional to the overlap between the positive and negative plates because then the flux produced by the currents flowing in two plates cancel each other. Therefore, most of the stray inductances of the bus bar are concentrated around the power module connection leads, where overlap is usually challenging to achieve. Two different bus bar designs are achieved by increasing the

Parameters	Value	Unit
DC link voltage	800	V
Maximum DC	300	A
Breakdown voltage DC	1200	V
Switching frequency	20	kHz
Power module	FS03MR12A8MA2B	
Film capacitor	B25632E1117K000	
Total capacitance	330	µF

Table 4.1: Design requirements of the DC bus bar

overlap close to the power module connection with the support of the stakeholders from Rogers corporation, Belgium as shown in Fig. 4.1.
The Fig. 4.1 shows the simulation results of current and flux distribution generated from the FEM model of the two bus bars. The figure shows a high current and flux distribution around the middle connection, which is the shortest impedance path between the switch and the capacitor. The current distribution in the remaining part of the bus bar is very low. However, some flux distribution is visible around the leads connecting the capacitor. A visible reduction in both current and flux distribution is observed in the second design with the increased overlap from Fig. 4.1 (b) and (d).

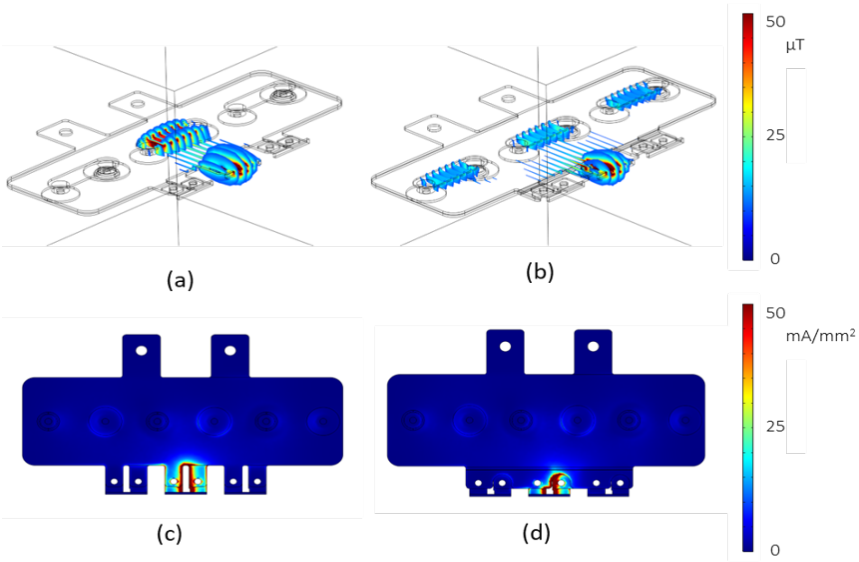

Figure 4.1: (a) and (b) Current and (c) and (d) flux distribution of the two bus bar designs.

4.2.2 Calculation of loop inductance

The loop inductance of the bus bar is calculated using the FEM model of the bus bar. To calculate the inductance, the terminals for all three capacitors are short-circuited, and a sinusoidal current excitation is used between the positive and negative ter-

minals of the corresponding phase leg. The current frequency of the excitation is the same as the switching frequency. The results of the simulation are presented in Table 4.2. As can be seen from the results, the increased overlap results in a 26% reduction in the stray inductance. Additionally, the stray inductance for phase B is the lowest, which is to be expected as it has the shortest loop length due to the geometric position. The increase in the volume of the bus bar due to the Increased overlap is around 3%, much smaller than the reduction in stray inductance. An average value of the stray inductance is calculated for the two designs and used for further analysis later.

Phase	**Unit**	**Design**	
		I	II
A	nH	32.18	23.78
B	nH	30.26	22.63
C	nH	32.68	24.3
Average	nH	31.7	23.6

Table 4.2: Estimated stray inductance using simulations

4.3 Switching Loss Analysis

4.3.1 Double pulse test simulation

The switching losses of a MOSFET can be analytically calculated as follows,

$$P_{\mathrm{sw}} = f_{\mathrm{sw}} E_{\mathrm{Tot}} \left(\frac{I_{\mathrm{out}}}{I_{\mathrm{ref}}}\right)^{k_i} \left(\frac{V_{\mathrm{DC}}}{V_{\mathrm{ref}}}\right)^{k_v} \tag{4.1}$$

where P_{sw} is the switching losses, f_{sw} is the switching frequency, E_{Tot} is the sum of turn-on and off energy, I_{out} is the average load current, I_{ref} and V_{ref} are the reference values of drain-source current and voltages used for switching loss measurements in the datasheet, k_i and k_v are the exponents for current and voltage dependency [55]. As can be seen from the equation, the switching losses are dependent on the voltage across the switch. The voltage across the switch will be influenced by the voltage overshoot provided by the stray inductance. However, the effect of the bus bar stray inductance is not included in the semiconductor datasheet. Therefore, using the datasheet values directly could result in underestimating switching losses. A solution is to simulate the effect of the stray inductance on the switching behavior and use it to scale the switching losses.
Performing the simulation on the entire model of the inverter may be time-consuming. Therefore, a double pulse test (DPT) circuit is modeled in the simulation. The schematic of a DPT circuit is shown in Fig. 4.2. It consists of a test device (DUT) and a freewheel diode connected to a load inductor in parallel. The DUT can also replace the freewheeling diode under test because it has a body diode. A DC voltage is applied between the diode and the MOSFET, and the MOSFET current and voltages are measured. The simulated waveform is presented in Fig. 4.3. As can be

seen, the device is turned on, and the DC link voltage is applied across the inductor, which causes the current through the inductor to increase. Once the current reaches the desired value, the device is turned off, which causes the current through the device to be interrupted, and it freewheels via the diode. After a short period, the device is turned on, forcing the current to flow through the device. When the diode turns off, an overvoltage spike is caused by stray inductance. The second turn-on and the first turn-off events characterize the devices.

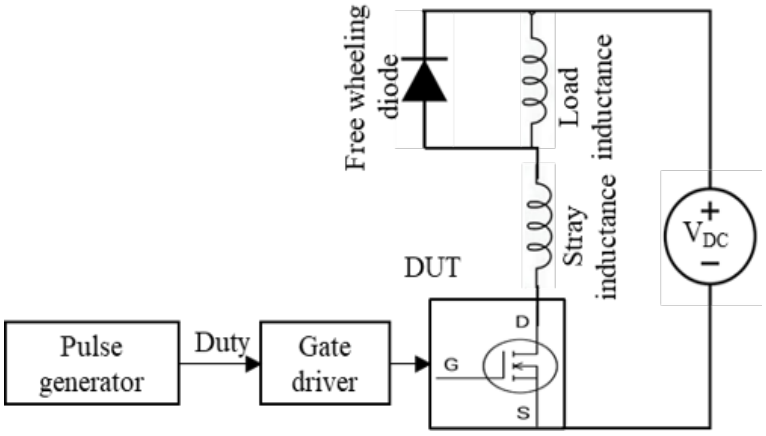

Figure 4.2: Schematic of Double pulse test circuit modelled in Simulink

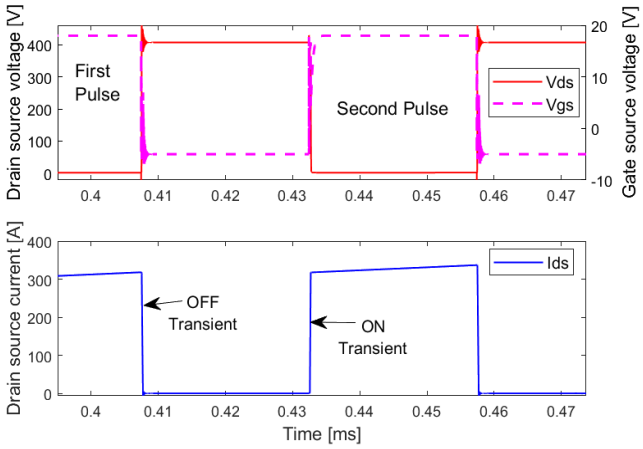

Figure 4.3: DP simulated waveform at 400V DC and I_{ds}=320A, V_{ds}=Drain-Source voltage, V_{gs}=Gate-Source voltage, I_{ds}=Drain-Source current

The MOSFET characterization results are illustrated in Fig. 4.4. This compares the total switching losses for two bus bar configurations with the base datasheet losses on the primary axis. Additionally, the secondary axis depicts the increase in total switching losses attributable to the bus bar stray inductance relative to the datasheet values. The figure demonstrates that the increase in switching losses, compared to the datasheet values, is minimal. Hence, the secondary axis provides insight as the increase in losses due to the two bus bar designs widens with the increase of drain-source current. However, the proportional increase in the switch

loss energy compared to the base datasheet values for design-1 is 1.55% to 2%, and design-2 is 2.7% to 3.2%, from 80A to 320A of Ids.

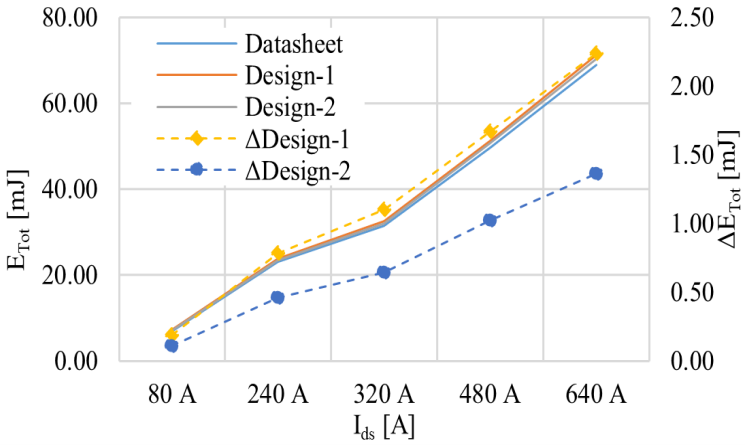

Figure 4.4: A graph showing the comparison of total switching energy losses for the two different bus bar designs compared to the datasheet value and increase of the switching losses energy in both the designs at 800V DC and I_{ds} of 320 A

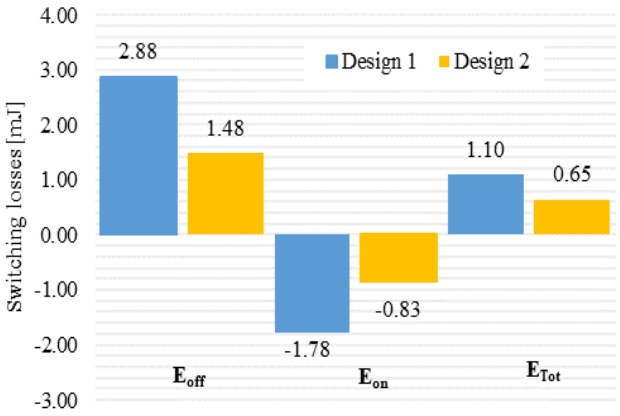

Figure 4.5: A comparison between increase in turn-on, turn-off and total losses of inverter for the two different designs. Case: Vds = 800V, Ids = 320A

The impact of stray inductance on turn-on and turn-off losses separately can be seen from Fig. 4.5 at 320 A phase current peak with both inductances. It is observed that turn-on losses are decreasing, and turn-off losses are increasing with an increase in stray inductance. Since increasing stray inductance gives a slower positive di/dt during the turn-on, the V_{ds} become less than V_{dc} during the over-lap period of V_{ds} and Ids, which tends to reduce the turn-on losses compared to datasheet values. However, a higher voltage peak of V_{ds} and slower di/dt during turn-off increases turn-off losses, which also increases the total inverter losses with an increase in stray inductance.

4.3.2 Inverter Losses for a Drive cycle

A 2-level three-phase inverter is modeled in MATLAB/Simulink as discussed in the previous chapter to evaluate the influences of the parasitic inductance on the switching losses considering the application. A simplified system modeling approach uses vehicle models, transmission, electric machine maps, and inverter loss estimation which can be seen from schematic 4.6 and the overall block diagram 3.11 from the previous chapter.

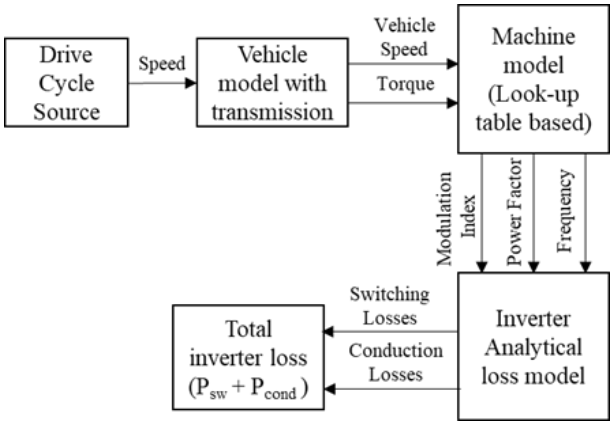

Figure 4.6: A block diagram representation of the analytical loss model

Drive cycle source
It contains various different drive cycle based on different global standards for automotive testing. To emulate the application, HHDDT (Heavy Heavy-Duty Diesel Truck) transient and cruise drive cycles for a Heavy-Duty Truck (HDT) are considered [80]. The speed output from drive cycle source is of m/s, which is given as input to vehicle model. The drive cycle input speed to vehicle model can be seen from the Fig. 4.8.

Vehicle model
A HDT is considered for the vehicle model for which the key the parameters are shown in the below Table 4.3.

Parameters	Value
Aerodynamic drag coefficient	0.53
Front cross-section area [m2]	9.7
Rolling resistance coefficient	0.0051
Mass [kg]	40000
Wheel radius [m]	0.5
Transmission ratio	19
Number of drive units	2
Vehicle model	HDT

Table 4.3: Key parameters of the vehicle model used in the simulation

The vehicle models represent the 1-D kinematic motion and calculate the traction force as follows,

$$F_t = m_v g C_r + \frac{1}{2}\rho C_d v^2 A + m_v \frac{dv}{dt} \tag{4.2}$$

where m_v is the vehicle mass, g is the gravity constant, ρ is the air density, C_d is the drag coefficient, v is the speed, A is the vehicle's frontal area and F_t is the traction force. An electric HDT truck is modeled in simulations for which the data is presented in Table 4.3 [81]. The electric machine torque and speed are calculated using the transmission model as follows,

$$T_m = \frac{F_w r_w}{k_g} \tag{4.3}$$

$$\Omega_e = \frac{v}{r_w k_g} \tag{4.4}$$

where T_m and Ω_e are the shaft torque and rotor speed of the traction machine, r_w is wheel radius, k_g is the transmission ratio.

Machine Model

A look-up table-based machine model is used which is shown in figure 4.7. The modelled machine is an IPMSM with 8 poles and 48 slots. The machine model consists of maps of the modulation index, Powerfactor and fundamental current frequency. These look-up tables are calculated for the entire torque-speed operating region of the machine assuming copper loss minimization strategy as described in [81]. Based on speed and torque from the simplified vehicle model, d and q axis currents and voltages are extracted through interpolation through which the phase current amplitude $\hat{I}$, modulation index M, and power factor cosϕ are calculated as per eq. 4.5 to 4.7.

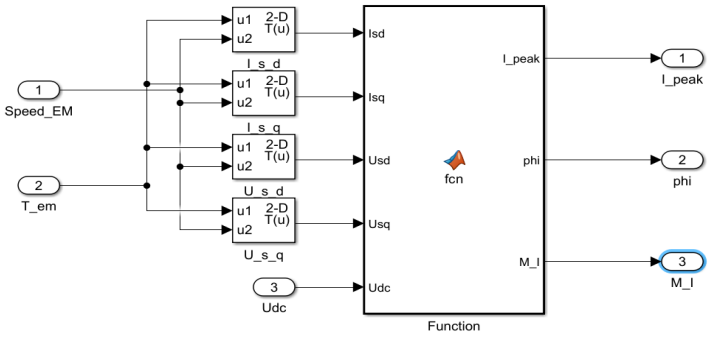

Figure 4.7: 2-D look-up table based machine model

$$\hat{I} = \sqrt{i_{\mathrm{d.ref}}^2 + i_{\mathrm{q.ref}}^2} \tag{4.5}$$

$$M = \frac{\sqrt{u_{\mathrm{d.ref}}^2 + u_{\mathrm{q.ref}}^2}}{\frac{u_{\mathrm{DC}}}{\sqrt{3}}} \tag{4.6}$$

$$\cos\phi = \frac{u_{\mathrm{d.ref}} i_{\mathrm{d.ref}} + u_{\mathrm{q.ref}} i_{\mathrm{q.ref}}}{\sqrt{u_{\mathrm{d.ref}}^2 + u_{\mathrm{q.ref}}^2}\sqrt{i_{\mathrm{d.ref}}^2 + i_{\mathrm{q.ref}}^2}} \tag{4.7}$$

where i and, u denote the current and voltage in the DQ plane, u_{DC} is the DC link voltage.

Inverter loss model

The switching losses and conduction losses of the MOSFET are calculated as described in the previous chapter. The switch loss energy from the datasheet is interpolated as follows,

$$P_{\mathrm{sw}} = f_{\mathrm{sw}} \left(E_{\mathrm{on}}(I_{\mathrm{DC}}, T_{\mathrm{j}}) + E_{\mathrm{off}}(I_{\mathrm{DC}}, T_{\mathrm{j}}) + E_{\mathrm{rr}}(I_{\mathrm{DC}}, T_{\mathrm{j}}) \right) \tag{4.8}$$

$$I_{\mathrm{DC}} = \frac{\hat{I}}{\pi} \tag{4.9}$$

where P_{sw} is the switching losses, f_{sw} is the switching frequency, E_{on} is the on-state loss, E_{off} is the off-state loss, and the E_{rr} is the reverse recovery loss. To simplify the calculation, AC current amplitude can be expressed as an equivalent DC (I_{DC}) as mentioned in the eq. 4.9.

Drive cycle simulation results

The results of the simulation of inverter energy loss for the HHDDT drive cycle with the two different bus bars are presented in Fig. 4.8. The total energy consumption per 100 km is calculated for both bus bars for the two different driving cycles. The switching loss energy increased by 2.53% for bus bar design-1 and by 1.17% for design-2 compared to the datasheet values, with HHDDT transient and cruise cycles. Design-2 with additional overlap design reduces the energy losses by 0.94% which was observed to be 1.14% in DPT. These results are inline with the MOSFET switch level DPT simulations which shows a 2.7-3.2% increase in energy losses for design-1 and 1.55-2% increase in energy losses for design-2. The difference occurs due to the real-world operating current demand by electric machines for the drive cycle, which can be seen in Fig. 4.8. In Fig. 4.8, the equivalent DC together for both cycles is given, which reaches up to a maximum of 100A and primarily operates around 60A. Hence, from the application point of view, the vehicle operates mostly in the lower operating current zone of the switch, which causes little difference in the increase in losses. Hence, % increase in energy losses for drive cycles are matching with the lower current points in the DPT simulation and the impact of stray inductance is verified.

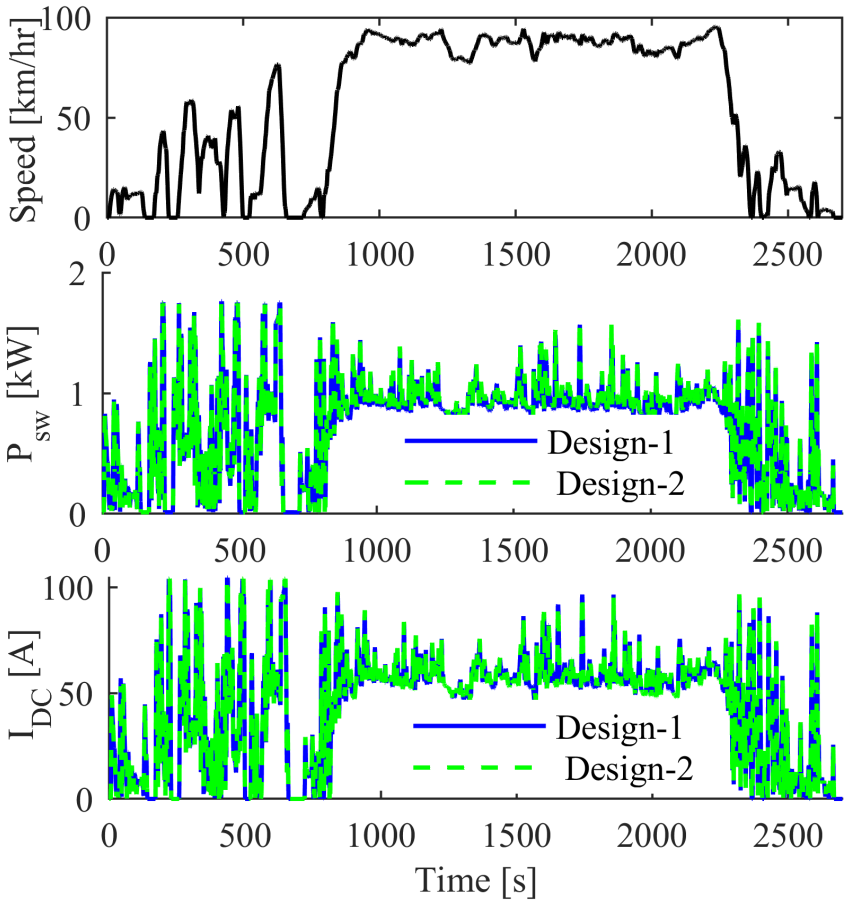

Figure 4.8: The switching loss value of two bus bar designs in HHDDT transient and cruise cycle together for an electric HDT with two 250 kW PMSM

4.3.3 Voltage overshoot analysis

In addition to the drive cycle simulation to analyze the impact of stray inductance on inverter losses, it is crucial to examine the voltage overshoot across the semiconductor that results from the inductive voltage drop during the switch-off event. The primary goal of this voltage overshoot analysis is to observe the peak voltage that arises due to an increase in bus bar stray inductance, using both simulation and experiments. As shown in Fig. 4.9, two 2-level inverters are prototyped with the two bus bar designs. The inverters are prototyped to the requirements presented in Table 4.1. The experimental lab setup of the prototype inverter is shown in Fig. 3.13 for the switching transient measurements. Power modules with SiC MOSFETs in a 6-pack configuration and three capacitors of 110 µF are used. dSPACE DS1006 is used to generate PWM to the gate driver board. A Rogowski coil is used to measure the current flowing through the switch. Moreover, the switch current is measured at the DC terminals of the module, while the switch voltage is measured between the DC- and phase output. The voltage overshoot simulation is done with DPT, considering the load conditions equivalent to the experimental setup.

The simulation results of the voltage overshoot are given in Fig. 4.10, which shows a reduction of 17.7% in voltage spike with the bus bar design-2. The measurements

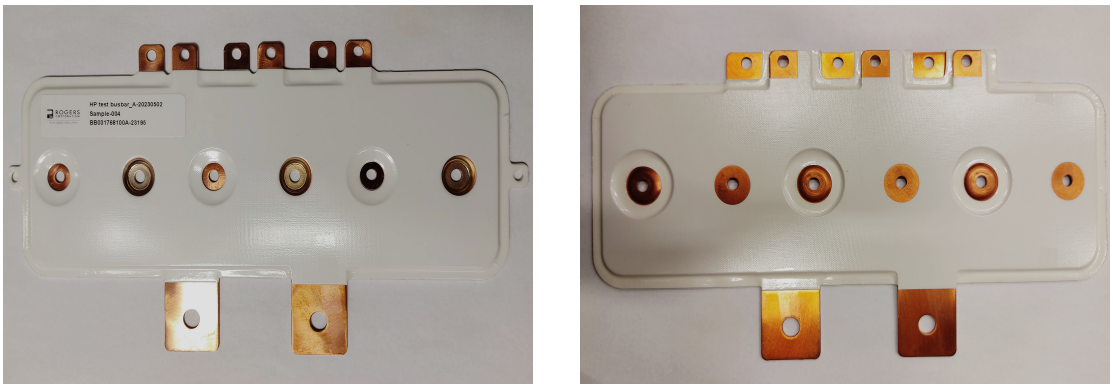

Figure 4.9: The prototype bus bars (a) Design 1 and (b) Design 2

of the inverter have been taken in phases A and B. Since it shows similar results, the measurement was not done in the third phase C. The results obtained from conducting the measurement are depicted in Fig. 4.11, which shows the voltage overshoot observed during the turn-off event of the measurement with both the bus bar designs. The overall summary of the comparison between the simulation and experiment on the overvoltage is given in Table 4.4. Comparing to design 1, design 2 shows a reduction of 12% on the over-voltage across the switch in the experiments, which is confirmed with the reduction trend from the simulation result of 17.7%. This little difference is expected due to the estimation error in the inductance measurement. Further, The decrease in stray inductance of 26% is not linearly proportion to the voltage overshoot reduction [78].

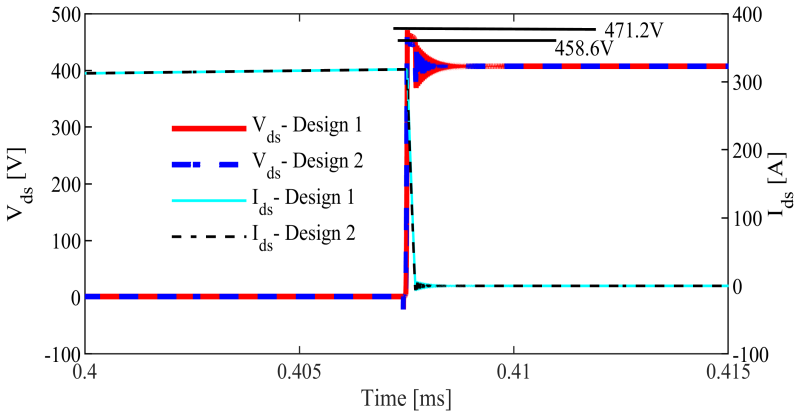

Figure 4.10: Simulation result of voltage overshoot in DPT, Case: Vds = 400V and Ids = 320A

4.4 Summary of the analysis

This chapter presents the design of bus bars with two different stray inductances and analyzes their impact on inverter switching losses using DPT, drive cycle simulations, and switching transient measurements. A drive cycle simulation was performed using an analytical loss function-based model to evaluate the impact of stray

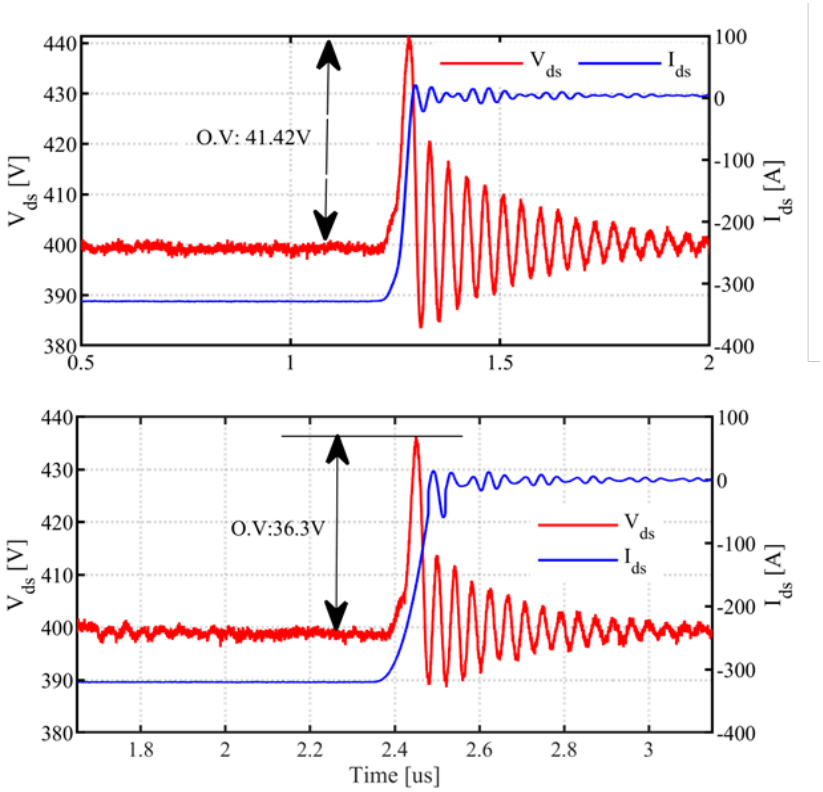

Figure 4.11: Experimental result with the two bus bar designs showing the voltage overshoot in Vds during turn-off, Case: Vds = 400V and Ids = 320A in Phase B, Design 1: Top, Design 2: Bottom

Bus Bar	$V_{overshoot}$ [V]		
	DPT Simulation	**Exp Phase A**	**Exp Phase B**
Design 1	71.2	41.3	40.2
Design 2	58.6	36.3	35.2
Δreduction	12.6	5.0	4.9
% reduction	17.7	12.1	12.3

Table 4.4: Comparison of voltage overshoot between simulation and experiment

inductance on inverter energy losses. The simulation results indicate that the increase in energy loss due to stray inductance is only 0.3%, whereas the DPT shows a 3.2-4% increase. Although simulations at specific operating current points at the component level indicate a significant impact on inverter losses, real-world drive cycle scenarios operate at these points for minimal durations, resulting in a negligible difference in energy losses. A 26% increase in stray inductance does not significantly affect inverter loss under real-world conditions. Given this minimal impact on inverter losses, the voltage stress on the switch was assessed through voltage overshoot analysis, revealing a 3-3.8% reduction in voltage overshoot with the lower inductance bus bar featuring an increased overlap design.

5
Conclusion

This thesis work majorly discusses, 1) different state-of-the-art technologies to achieve high power density in traction inverters, 2) the design, modelling and experimental verification of two level three phase voltage source inverter and 3) the influence of bus bar stray inductance in two level inverter performance in terms of switching losses and voltage overshoot. To achieve high power density various technologies such as impact of wide band gap devices, advanced cooling technologies for thermal management, methods and generations of various integrated drive topologies, high speed electric machines and different inverter topologies such as multiphase and multilevel inverters are studied in literature and presented.

The design, modelling and experimental verification of 250 kW two level three phase voltage source inverter is presented in this work. Modelling of the inverter is carried out in two methods, 1) Simulink PLECS based simulation for performance evaluation and 2) Analytical loss function based estimation of semiconductor losses and junction temperature measurement. A 250 kW prototype inverter is built using Infineon HybridPack SiC MOSEFT power modules with 6 pack configuration. Experiments were performed to measure the key parameters required for inverter power calculation and capacitor current measurement. Both the simulation models are compared, verified and discrepancies between simulations and experiments are discussed with justifications.

The impact of bus bar stray inductance in the two level inverter switching losses and voltage overshoot is studied and presented in this work. Two laminated prototype bus bars with a 26% difference in stray inductance was considered which analyzes their impact on inverter switching losses using DPT, drive cycle simulations, and switching transient measurements. A drive cycle simulation was performed using an analytical loss function-based model to evaluate the impact of stray inductance on inverter energy losses. The simulation results indicate that the increase in energy loss due to design-1 is 2.53% and design-2 is 1.14% whereas the DPT shows a 2.7-3.2% increase for design-1 and 1.55-2% increase for design-2. As simulations at specific operating current points in DPT indicate an impact upto 3.2% on inverter losses, real-world drive cycle scenarios reflected the same impact in the energy losses when comparing the losses with the lower operating points of DPT. Given this impact on inverter losses, the voltage stress on the switch was assessed through voltage overshoot analysis, revealing a 12% reduction in voltage overshoot with the lower inductance bus bar featuring an increased overlap design.

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